High Performance, Low-Power and Robust Multi-Gigabit Wire-Line Design

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To My Mother, Father and Sister

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SUMMARY

The object of this research is to develop robust wire-line systems which demonstrate high performance while simultaneously consuming low power. Most high performance designs come at the expense of high power consumption, while low power designs typically are not as robust as high power architectures. These problems have retarded the development of multi-gigabit wire-line systems. In this thesis, a holistic approach consisting of a system-level architecture modification, along with circuit-level innovations and optimizations has been presented to circumvent the stated problems. The main focus of this work is the Clock and Data Recovery (CDR) system which is the primary circuit of any modern wire-line transceiver. Ultra high-speed wire-line systems require high performance broadband amplifiers and buffers. A 62 GHz bandwidth amplifier has been presented to address this need. Package radiation and terrestrial radiation are liable to degrade the bit error rate (BER) of CDRs, especially high-speed ones. The scaling of process technology further exacerbates this issue. A new technique has been proposed to improve the radiation immunity of the latch, which is the block that is most sensitive to radiation. PLL-based CDRs are challenging to design at very high speeds and are also incapable of true burst-mode operation due to their substantial lock time. Injection-lock based clock recovery was investigated as an alternative to PLL based CDRs. Injection-locking can acquire the clock almost instantaneously from the data stream, and hence would be ideal for burst-mode communication. The investigation yielded the vulnerability of the method to jitter (false-locking and high jitter transfer), the attenuation of which is critical to commercial CDRs. PLL-based reference-less CDRs have traditionally suffered from the problem of false-locking, which is a major hindrance to the widespread use of such systems, albeit the cause of this is repetitive patterns occurring in data. A novel false-lock detector system has been proposed and demonstrated for the first time as a robust solution to this issue. The implementation of the final CDR system required the use of an L-C tank VCO, the components of which are generic for all

commercial CDRs. A new systematic layout technique for the VCO has been proposed and demonstrated in this work to substantially improve the layout area and the associated parasitics, approximately by 70 %. This new layout addresses a critical yet often neglected part of VCO design. Furthermore, a new concept has been proposed to optimize static dividers with respect to their power consumption and number of devices.

CHAPTER 1

INTRODUCTION

With the ever increasing demands on communications technology, and in particular the increasing demands for higher data rates, wire-line communication systems have seen the advent of successively higher data rates in excess of 10 Gigabits per second (Gb/s) to 40 Gb/s nodes. This research is motivated by the need to achieve these high data rates within the constraints of low power consumption, cost effectiveness, and robustness. Additionally, it is required that the solution be scalable with different applications, adaptable to present systems, and be easily implementable. The primary objective of this work is to identify and investigate the key hurdles we need to overcome the stated goals and to propose innovative solutions to address them.

In the first part of this work, the problem of achieving high performance at low power consumption was addressed. Various circuit-level, system-level, and layout-level techniques have been developed and utilized to achieve this goal.

As a part of this work, a low-voltage, low-power, silicon-germanium (SiGe) wide-band amplifier with a bandwidth of 62 GHz is presented to address speed and power issues with high-speed wire-line amplifier systems. The amplifier consumes only 125 mW from a 2.5 V supply. Compared to published reports, this is the lowest reported power for a non-distributed amplifier with more than 60 GHz bandwidth in a SiGe process technology. To address the issue of phase and frequency acquisition in high performance clock and data recovery (CDR) systems, an injection locking-based open-loop clock extraction technique has been explored as a low-power alternative to phase-locked loop (PLL)-based design. In this work, a new optimization methodology for maximizing extracted clock power is also presented.

The voltage controlled oscillator (VCO) is at the heart of any wire-line system, as the signal-to-noise ratio (SNR) of the system would depend to a large degree on its VCO performance. Furthermore, VCOs generally take up a large percentage of silicon real estate and

also have significant power consumption. Hence, the optimization of VCOs specifically for wire-line systems is being investigated. Design techniques for such VCOs are expected to be generically applicable to wire-line systems.

The simultaneous requirements of high performance and low-power consumption present a unique set of challenges in the design of wire-line communication systems. The prevention of false locking of CDRs is one such case. False locking is usually addressed with the design of special phase-frequency detectors (PFD). However, these PFD circuits are complicated in terms of architecture, and also they consume a large amount of power. Hence, a simpler solution to the problem of robust lock detection is being investigated. It must be noted that any proposed solution needs to be able to work at the same high-speed specification as the main CDR with as low-power consumption as possible.

Another reliability issue facing very high-speed wire-line systems is that of single-event upsets (SEUs). A SEU occurs due to the impact of high-energy ions and sub-atomic particles on a circuit. Since the objective of this work is to achieve robustness at low-power consumption, the traditional high-power consumption methods, such as triple-mode redundancy (TMR), cannot be used. A new circuit-level hardening technique for SEU mitigation, using high-speed SiGe bipolar and complementary metal oxide semiconductor (BiCMOS) digital logic, is presented to address the issue of SEUs without incurring large overheads over the corresponding unhardened design. A reduction in SEU vulnerability is accomplished through the implementation of an additional storage cell redundancy block to achieve the required decoupling. Compared with latch duplication, current sharing, or gated feedback techniques, this method incurs a lower power penalty and no speed penalty. The hardened circuit is implemented in the current mode logic (CML) and low-voltage logic (LVL) families, and the circuit simulation models predict significant reduction in the number of upsets compared to the corresponding unhardened versions. The technique is also easy to incorporate into existing designs.

In the next section, the issues facing a high performance wire-line system are discussed in more detail.

1.1 CHALLENGES IN HIGH-SPEED WIRE-LINE DESIGN

A defining feature of communication technology in the 21st century is perhaps the insatiable need for greater quality and quantity of information. The outcome of this need, over the last few years, has been a dramatic increase in the demand for high bandwidth in data transmission systems. The thrust toward high-definition (HD) video formats has improved the viewing experience for users, but has pushed the demand for bandwidth to unprecedented levels. Also, the demand for data processing, ranging from the personal computer (PC) to the aggregated server farms of corporate giants like Google, has been growing exponentially in keeping with Moore's law [1]. The upcoming cloud computing solutions from IBM, AMD, and Google will stress bandwidth limitations even further. These computing solutions involve the movement of massive amounts of data across networks, such as the internet, from the client nodes to the cloud and back. Even inside the server farms, high-speed and robust links would be needed for inter-node and intra-node links such as in rack-to-rack communications [2-3].

Wire-less data transmission, despite its rapid development, is confined to single-digit Gb/s speeds [4]. Therefore, there is a large market and enough motivation for the development of robust, high-speed, wire-line links capable of speeds from 10 Gb/s upward. Since the cost of wiring in wire-line networks is not negligible, every effort is to be made to utilize the full bandwidth capability of these links. This is especially true for expensive optical fiber-based data transportation systems. The serial throughput of wire-line transceivers, therefore, needs to be utilized before parallel transmission can be implemented. Maximizing serial throughput also leads to fewer components and lower power consumption and therefore incurs lower maintenance and infrastructure costs. With this reasoning, the IEEE 802.3 Higher Speed Study Group has been commissioned to study the possibilities of speeds beyond 10 Gb/s.

The challenge for wire-line integrated circuit (IC) design involves higher speeds, together with robust design and low power dissipation. Furthermore, the solution has to be cost effective to provide a greater incentive to end-of-line solution providers to replace their existing legacy infrastructure with the new technology instead of just providing extra parallel links in response to higher demand.

The first step toward achieving a cost-effective, robust, and high-speed chipset is to choose a fabrication technology that would be able to incorporate the above objectives. Currently, the complementary metal oxide semiconductor (CMOS) technology is the most popular technology for IC design due to its low cost per unit area and the very high level of transistor integration it can support. The supply voltage needed for CMOS also scales down with the channel-length, allowing lower power operation. A substantial research effort is being allocated toward the design of high-speed wire-less circuits in CMOS process, and recently published works point to the successful culmination of that effort [4-5]. In contrast to wire-less systems, circuits fabricated in the CMOS are generally absent for wire-line systems with speeds beyond 10 Gb/s. The primary reason for the absence of CMOS in high-speed serial links is because of its limited peak unity-gain frequency (f_T) and poor transconductance (g_m). This is because of the highly capacitive impedance presented by the gate of a MOS device. In narrow-band applications, such as wire-less systems, the issue of limited f_T can be circumvented by the use of impedance matching. The spectrum of a pseudo-random bit sequence (PRBS) coded in non-return-to-zero (NRZ) format, typically used for wire-line systems, is shown in Figure 1. As can be seen from the figure, preserving the integrity of the data stream would require a bandwidth approximately from direct current (DC) to the clock rate. This makes the required matching network very cumbersome, both in terms of area and also design time. CMOS, therefore, is not the right choice of technology for high-speed wire-line applications.

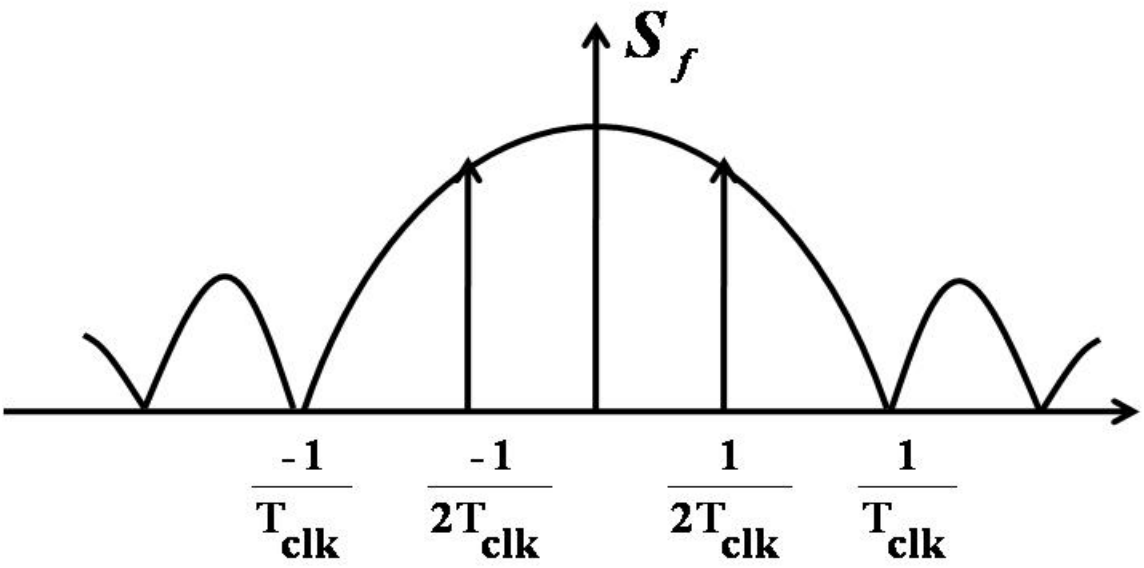


Figure 1. Spectrum of a PRBS data stream in NRZ format.

The III-V devices like gallium-arsenide (GaAs) and indium-phosphide (InP) have been extensively used in broad-band applications due to their high speed capabilities [5-6]. Unfortunately, these processes have lower yield and are more costly than silicon-based processes. Moreover, they do not have the high level of transistor integration that is necessary for successful monolithic solutions.

Considering the drawbacks of both CMOS and III-V devices, SiGe seems to be the ideal candidate for broad-band wire-line systems. SiGe offers III-V like speed and performance at a much lower cost. SiGe also has standard CMOS devices available on the same die, which facilitates high integration levels for the digital back-end. Thus, both the high-speed analog front-end as well as the digital back-end can be integrated monolithically [7].

Besides the constraints of speed and power, robustness to "soft errors" is another area of concern for high data rate systems, as these events occur from packaging material, terrestrial radiation, and harsh environments and severely degrade data integrity. If a degree of immunity to

such SEUs can be built into standard transmission systems at a minimal cost, then no significant time and resource would be wasted when they need to be adapted for more stressful conditions.

In the following chapters, specific system-level strategies and circuit-level components directed toward achieving low-voltage, low-power, high-speed operation and robustness to radiation are discussed.

CHAPTER 2

LOW-VOLTAGE, BROADBAND AMPLIFIER DESIGN

In cable-based (fiber optic or electrical) communication systems, broad-band amplifiers are a critical requirement. The eye diagram is commonly used to determine the signal quality of such amplifiers. The front-end amplifier of such systems must exhibit a clear output eye over a wide input dynamic range. These systems must also cover a large bandwidth [8]. For example, in a 10 Gb/s OC-192 compliant system, the lower cutoff needs to be approximately 30 KHz. The pass-band of such amplifiers must extend all the way to the clock rate; otherwise, the data would suffer from inter-symbol interference (ISI).

Broadly, there are two wide-band amplifier topologies: the distributed-element design and the lumped-element design. A distributed amplifier is composed of several stages working in parallel, as shown in Figure 2.

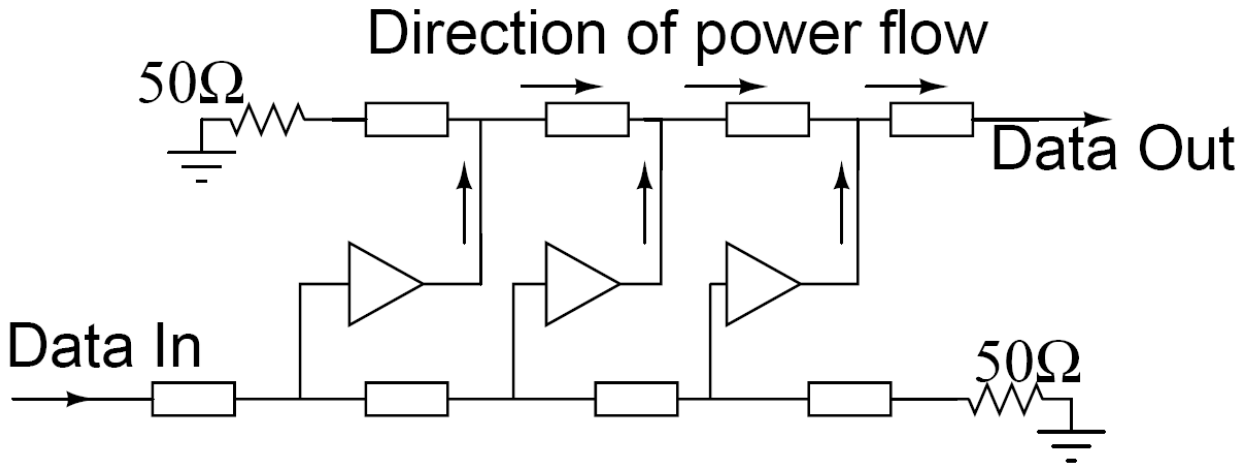


Figure 2. Distributed amplifier.

At first, each stage is individually optimized for performance specifications like low noise or high gain, and then they are optimally combined for maximum power transfer by either impedance matching or by using transformers [9]. The accuracy of the matching network determines the performance of the distributed amplifier. Therefore, process and temperature

variations, which cause the matching parameters to vary, can cause significant degradation in performance. In fact, it can very well happen that the network, instead of combining power from individual stages, creates local power circulations. Another problem of using extensive matching networks is the large area required. In terms of area, inductors are typically the largest devices on a chip. Hence, matching networks, which typically need a number of inductors, are costly in terms of real estate.

Figure 3 shows a lumped-element amplifier. Lumped-element designs are generally preferred for wire-line broad-band amplifier designs, as they do not require a high degree of accuracy in the value of their passive elements. With minor changes in component values, the same circuit can be used for buffering internal nodes, as a front-end amplifier, or as an output pre-driver, unlike a distributed amplifier which requires complete redesign.

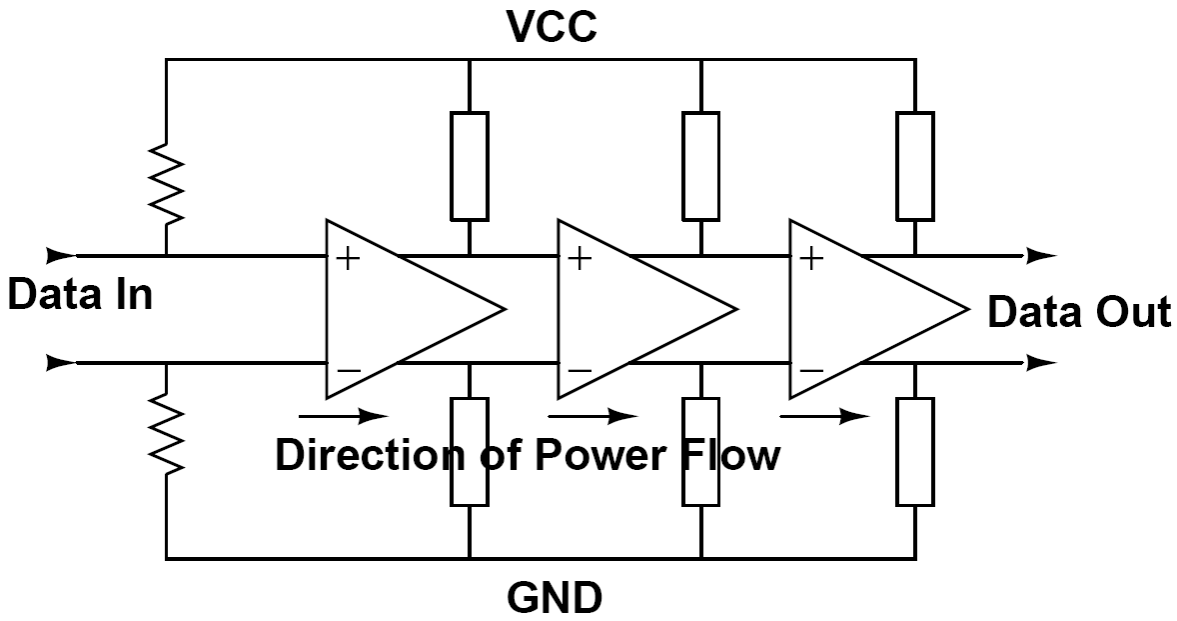


Figure 3. Lumped-element amplifier.

A lumped-element front-end amplifier can be implemented as an automatic gain control (AGC) or a limiting amplifier (LA) [10]. Figure 4 shows the schematic of an AGC amplifier. The AGC amplifiers have low deterministic signal jitter because of their negative feedback loop. The AGC, as the name suggests, adjusts its gain with the input voltage level. Thus, it reduces the

gain at high input voltage levels. This prevents the system from amplifying too much noise at high input levels. Therefore, AGC systems keep the SNR constant over the entire input dynamic range.

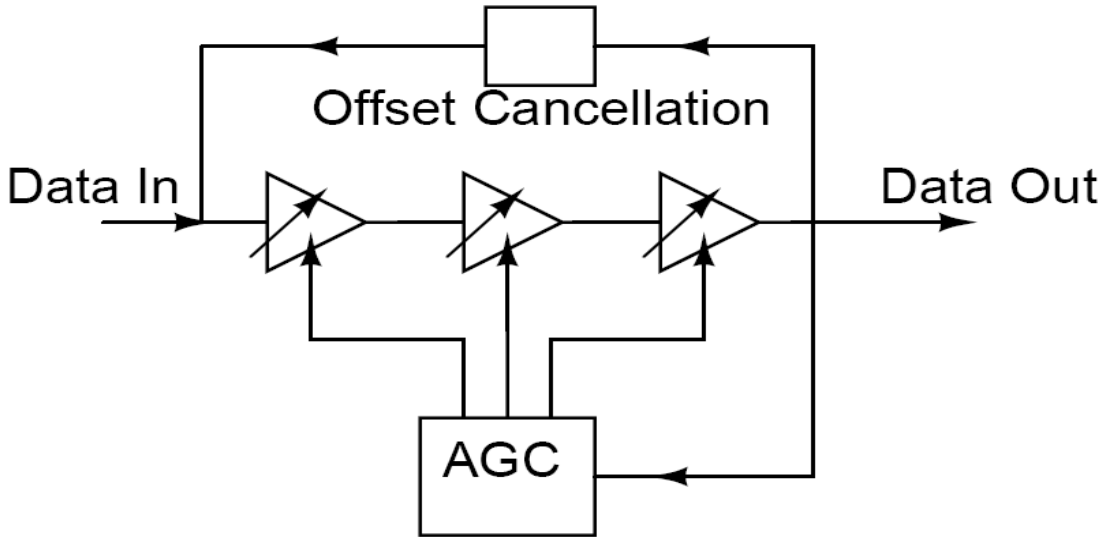


Figure 4. Schematic of an AGC amplifier**.**

Unfortunately, due to the closed-loop design involved, AGCs are difficult to design. The dependence on the closed loop also makes the amplifier slow to respond to input amplitude variations. Thus, AGCs cannot be used in CDRs aimed at fast data acquisition.

LAs are much simpler to design and characterize owing to their open-loop operation. An LA always presents the maximum possible gain to the input signal. Assuming Gaussian noise, we can separate out the noise, in the time domain, to portions near data zero crossings and portions near data saturation level. Since an LA operates in gain-saturation mode, the noise near the data top and bottom levels would get "limited" out. The noise at the zero-crossings is the one that presents the problem, as it will always be amplified up by the maximum gain. For high input voltage levels, the ratio of the signal gain to the noise gain degrades, as the gain for the data is low but the noise gain is high. This degrades the amplifier SNR.

The standard deviation for signal jitter is given by the standard deviation for noise divided by the slew rate of the amplifier, as shown in the following equations:

$$\Delta T = \frac{n(t_1)}{S} \quad ; \tag{1}$$

$$P_n = \frac{1}{\sqrt{2\pi}.\sigma_n} \exp(-n^2 / 2\sigma_n^2) \quad ; \tag{2}$$

$$P_{\Delta T} = \frac{1}{\sqrt{2\pi}.\frac{\sigma_n}{S}} \exp(-(\Delta T.S)^2 / 2\sigma_n^2) \quad ; \tag{3}$$

$$\sigma_{\Delta T} = \frac{\sigma_n}{S} \quad , \tag{4}$$

where

ΔT = Zero crossing signal jitter,

$n(t_1)$= Instantaneous noise amplitude,

S = Slew-rate,

P_n = Gaussian voltage-noise distribution,

$P_{\Delta T}$ = Signal jitter distribution,

σ_n = Standard deviation for voltage-noise, and

$\sigma_{\Delta T}$= Standard deviation for signal jitter.

A reduction in zero-crossing signal jitter can thus be achieved by increasing the slew rate, as is shown in Figure 5.

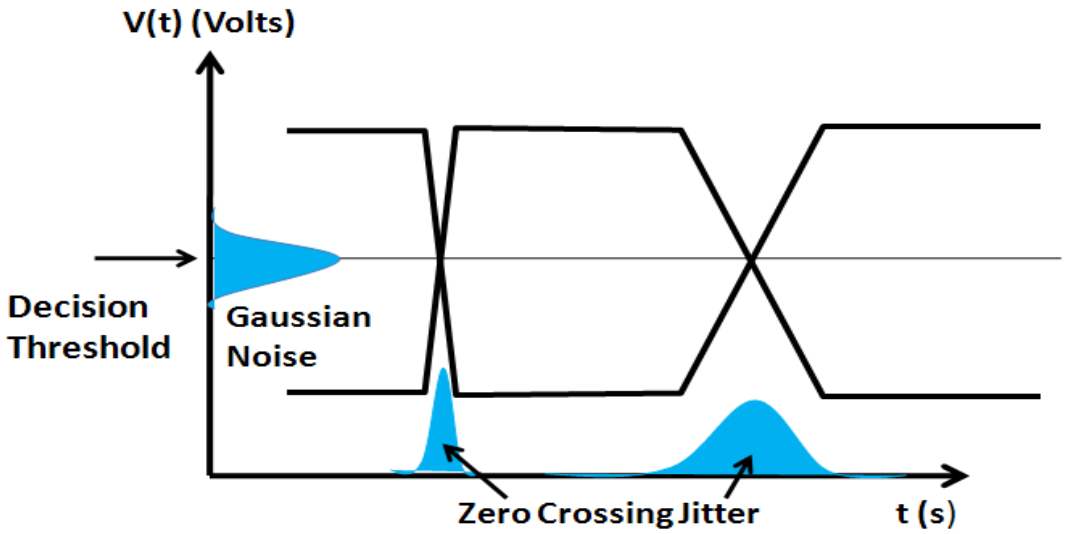


Figure 5. Intuitive representation of the relationship between noise, slew rate and signal jitter.

Thus, a primary constraint in the design of the LA is its edge rate, which is determined from the given noise specification.

To increase the edge rate, the available f_T of the device must be fully utilized. As the peak f_T of a device occurs at high base-to-collector reverse bias voltage, these amplifiers are typically used with 3.3 V supply rails to maximize their speeds. Unfortunately, this large supply voltage requirement increases the power consumption by a significant amount. Furthermore, as most of the other blocks can operate off 2.5 V rails, this leads to the problem of dual supply requirement.

As mentioned earlier, the LA architecture has several advantages over the AGC architecture for very high data rate applications. It was previously mentioned that the LA must have a high edge rate, almost equal to the data rate, to minimize the added signal jitter. The overall aim of this design is to not only have high edge rates, but also to achieve them while consuming as low power as possible. To achieve this end, the supply was fixed at 2.5 V. This, along with the introduction of properly sized peaking inductors, leads to the lowest reported power for a lumped element design having a bandwidth in excess of 60 GHz. The amplifier is

intended to be used as a data buffer for critical internal nodes in the CDR as well as function as the requisite LA after a few minor modifications.

The amplifier consists of three stages with decoupling emitter follower (EF) buffers placed in between each stage, as shown in Figure 6. Each amplifier stage is designed as a modified Cherry-Hooper (C-H) architecture. The amplifier is designed for true differential operation, with a differential input and output. On-chip 50Ω has been used for wide-band matching. A fifth level metal resistor was chosen for this purpose owing to its low parasitic capacitance as compared to a diffusion resistor.

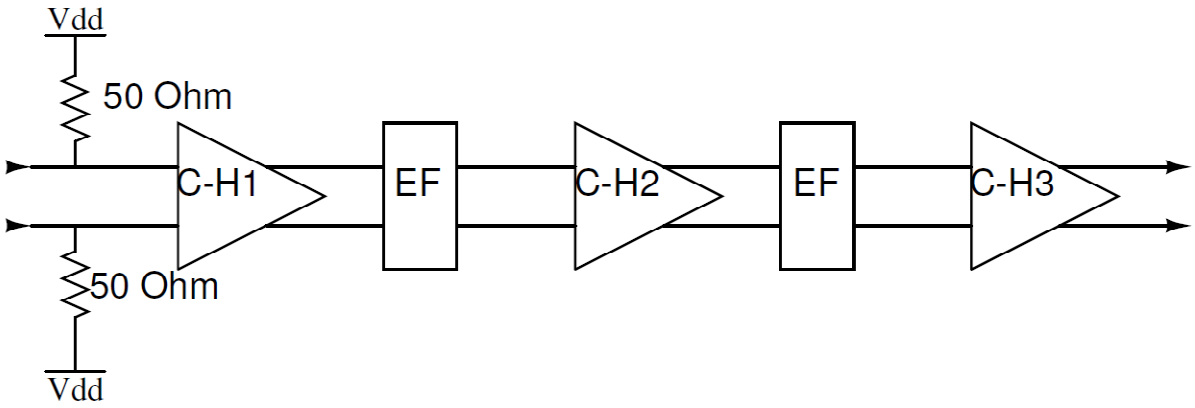


Figure 6. Broadband amplifier block diagram showing the Cherry-Hooper and emitter-follower stages.

2.1 DESIGN TECHNIQUES

Low power consumption is achieved by reducing the supply voltage from 3.3 V to 2.5 V. However, this reduces the headroom of the C-H tail current source. To alleviate this problem, the HBT tail current source is replaced by a high aspect ratio MOS field effect transistor (FET) which has a lower headroom requirement. Also, cascaded emitter-followers, which are typically used to decouple amplifier stages at high frequencies, were replaced by single emitter-followers for reduced power consumption. To achieve the maximum possible bandwidth, the

principle of maximum impedance mismatch has been utilized along with true differential operation and on-chip matching [11]. This mismatch is achieved by alternating trans-admittance (TAS) and trans-impedance (TIS) stages to form the C-H amplifiers. Shunt peaking is used to extend the bandwidth [12]. The peaking inductances were chosen to be greater than that required for maintaining maximally flat bandwidth. The emitter followers were also chosen to have a peaking response. This has been based on the method of active peaking. The response when looking into an emitter follower shows an inductive response for a specific band of frequencies. This can be understood by the simple intuitive diagram shown in Figure 7.

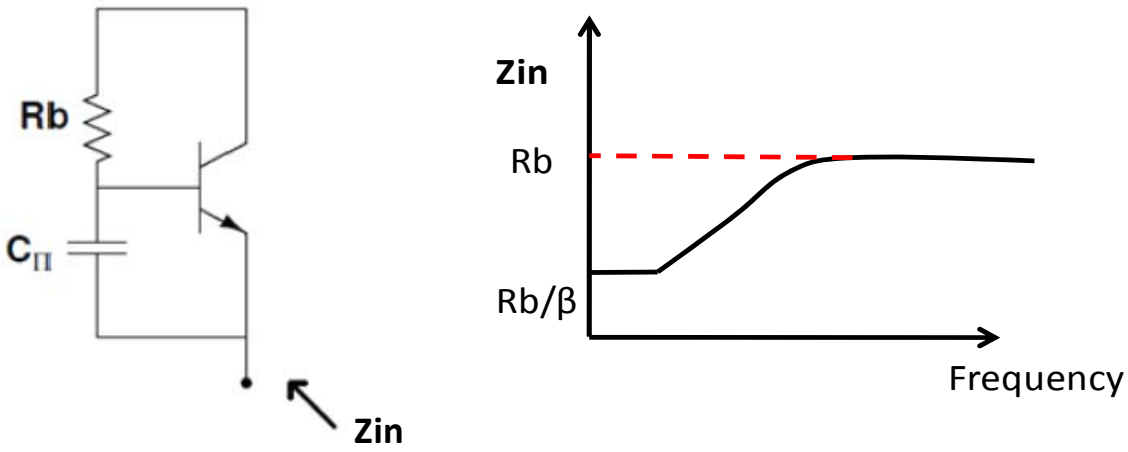


Figure 7. The peaking response of an emitter follower.

At low frequencies the impedance looking into the emitter follower is purely resistive and the value is given by the following expression:

$(r_e + R_e + Rb/\beta)$;

where $r_e = 1/g_m$, R_e = contact resistance of the emitter, Rb= the load resistance of the previous cell, and β=the transistor current gain. In general, the resistance Rb/β dominates so for an

intuitive analysis we can neglect the other two terms. At high frequencies, the capacitor C_{Π} shorts the emitter out, hence only the resistance Rb can be seen. Thus we see that the impedance of the system has gone up with frequency which is the characteristics of an inductor. Thus, the emitter follower can be used as an active peaking cell. Excessive peaking, though, leads to the degradation of the deterministic jitter. This is because excessive peaking distorts a flat group delay response required to keep deterministic jitter to a minimum. To reduce the peaking to an acceptable value, the bias current of the devices were adjusted to provide just enough bandwidth.

2.2 AMPLIFIER ARCHITECTURE

The three-stage amplifier shown in Figure 8 displays each C-H stage along with associated single emitter follower stages [13]. A modified differential Cherry-Hooper architecture was used to implement the amplifier stages, as shown in Figure 9 [14]. The C-H amplifier consists of a TAS and a TIS stage. The cascading of the TAS-TIS stages allows for the maximum mismatch between them and hence enhances the bandwidth.

A concept called "U- shaped" gain taper has been utilized in this implementation. Traditionally, in a multistage amplifier, one of three types of gain taper is used. The types of taper are the forward taper, backward taper or straight taper. In the forward taper, the gain of each stage is progressively increased. This is generally done to avoid having to place a large gain-bandwidth requirement for the first stage, which also has to be low noise. The second method, called the backward taper, is very popular in high speed design. The idea behind this method is to prevent bandwidth loss by cascading. As is known that if two stages of the same bandwidth are cascaded together the resulting bandwidth is $1/(2)^{1/2}$ times the original bandwidth.

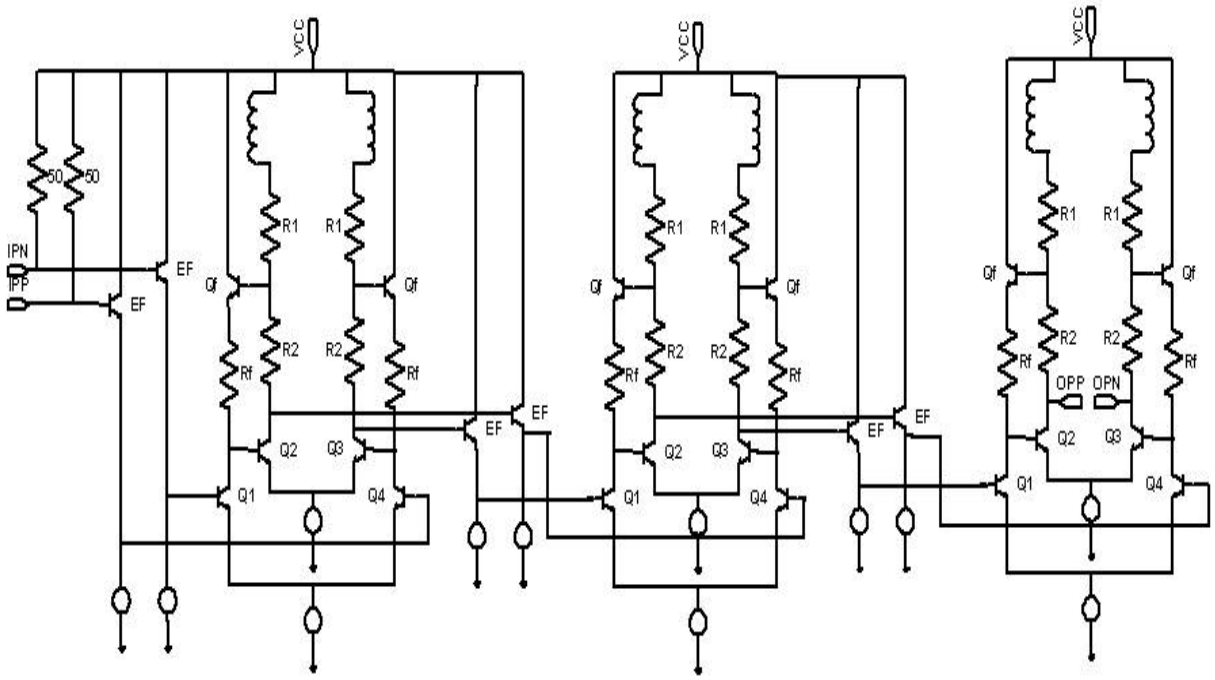


Figure 8. The schematic diagram of the implemented amplifier *(publication [3]).*

To circumvent this problem, each stage is made progressively smaller. Thus the preceding stages always see a diminishing load to drive, thus preserving the bandwidth. The principle drawback of this method is the low gain. The third method or the straight taper is the simplest of the three as it involves just cascading of three similar stages. This is done where the gain-bandwidth and the jitter requirement are not very stringent. This takes the least design and layout cost as it simply repeats the first stage as many times as required.

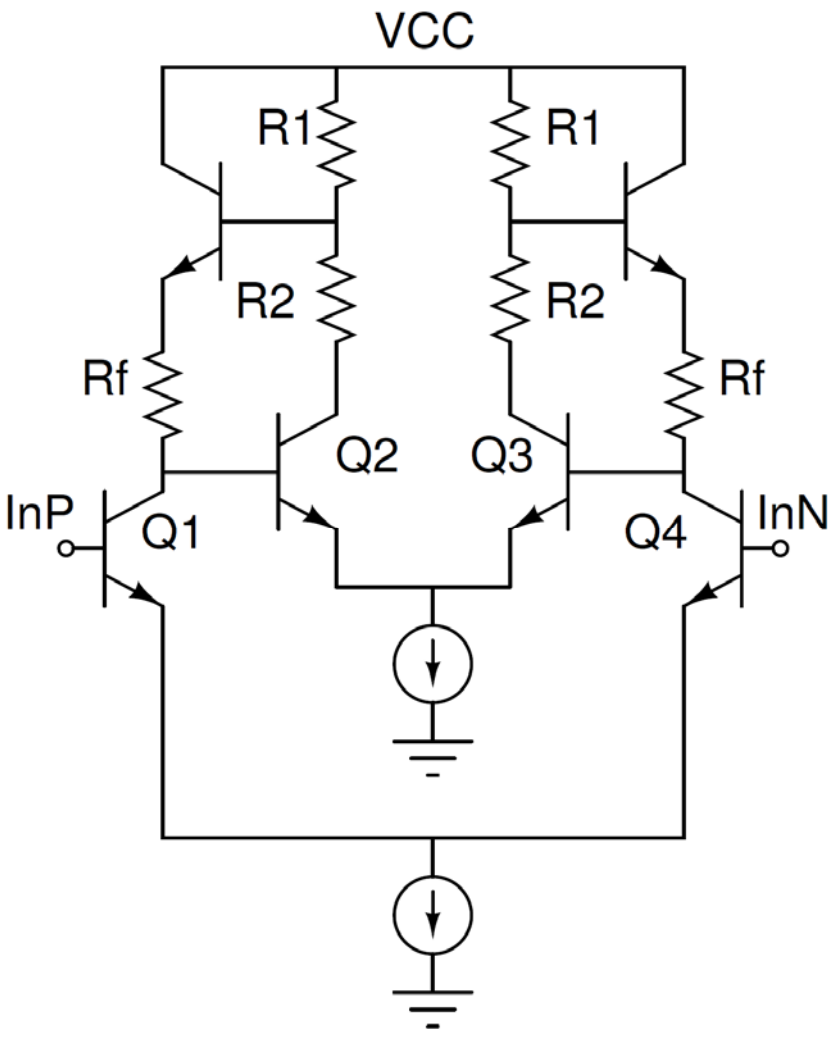


Figure 9. Modified Cherry-Hooper amplifier stage.

We have implemented a hybrid of the forward and backward taper, in essence a "U-shaped" taper. In this method, applied on a three stage architecture, the gain of the first and last stages are high, while the middle stage has a low gain. Looking back at the equations where the relationship between Gaussian voltage noise and time domain jitter was established, it can be noted that the time domain jitter decreases with increase in slew rate. This is the idea that has been utilized in the "U-shaped" taper. Typically, the first stage has a small voltage input, which

is not enough to switch the transistors in the first stage. Thus the first stage is largely linear. The gain of this stage is made larger by using larger inductor peaking for this stage. To further support this gain and yet have larger bandwidth, the second stage was made smaller. The gain of the first stage is set to a value such that the minimum voltage output of the stage is enough to switch the current in the second stage by 90 %. This requires a minimum output swing of about 80 mV for practical operation. Now, the most important point to understand is that the time domain jitter is decided at the first point where large signal switching takes place. Thus, the first stage which is a linear stage amplifies both the signal as well as the noise by the equal transfer function. In the second stage, since it has enough input to switch, would be the stage that would decide Gaussian noise to time domain jitter conversion. Hence, this stage should have the highest possible slew rate. Thus, in this stage the gain has been traded off with the slew rate. The slew rate of the last stage does not affect the jitter by a large amount; hence, here the slew rate is traded off with a larger gain.

The purely resistive feedback of a traditional C-H amplifier has been modified in this design by the inclusion of an emitter-follower in the feedback path. The emitter follower serves to minimize feed-forward effects and also provides inductive peaking, both of which help to increase the overall amplifier bandwidth. In addition, this architecture mitigates the voltage headroom problem in the TAS stage.

The collector resistance has been split into R1 and R2, which boosts the gain by (1+R1/R2) without affecting the circuit bandwidth significantly, provided that $0<R2/R1<2.5$ [14]. Shunt peaking has been utilized in all stages of the amplifier to further enhance the bandwidth [12]. Peaking inductors were implemented with transmission lines with the signal line as the seventh (top) metal layer and the first metal layer as the bottom plane.

We deliberately decided to not include a dedicated output buffer to drive 50 Ω loads, in spite of the resulting low gain. This decision was influenced by the fact that it might be

impossible to accurately de-embed the response of the output buffer and to subsequently be able to accurately characterize the performance of the amplifier itself.

Layout

The chip micrograph is shown in Figure 10. The layout has been made perfectly symmetrical with very short interconnects. All interconnects, including via stacks, have been modeled with Ansoft HFSS. To minimize parasitic elements and keep the signal paths as short as possible, the overlap of the RF and the DC paths have been largely avoided. Although this leads to an extremely compact layout, the tradeoff is that the DC supply must be provided from both sides of the chip. The concept of "U-shaped" gain taper which has been discussed earlier can be clearly observed from the chip diagram, as the top metal layer clearly shows the difference in length going from the first to the second stage.

2.2 MEASUREMENT RESULTS

The simulated DC operating conditions match the measurement results. The total chip draws 50 mA of current from a 2.5 V supply.

S-Parameter Measurements

Single-ended two-port scattering parameter measurements were performed using an Agilent 8510C Network Analyzer with frequency extension modules to increase the measurement range up to 110 GHz.

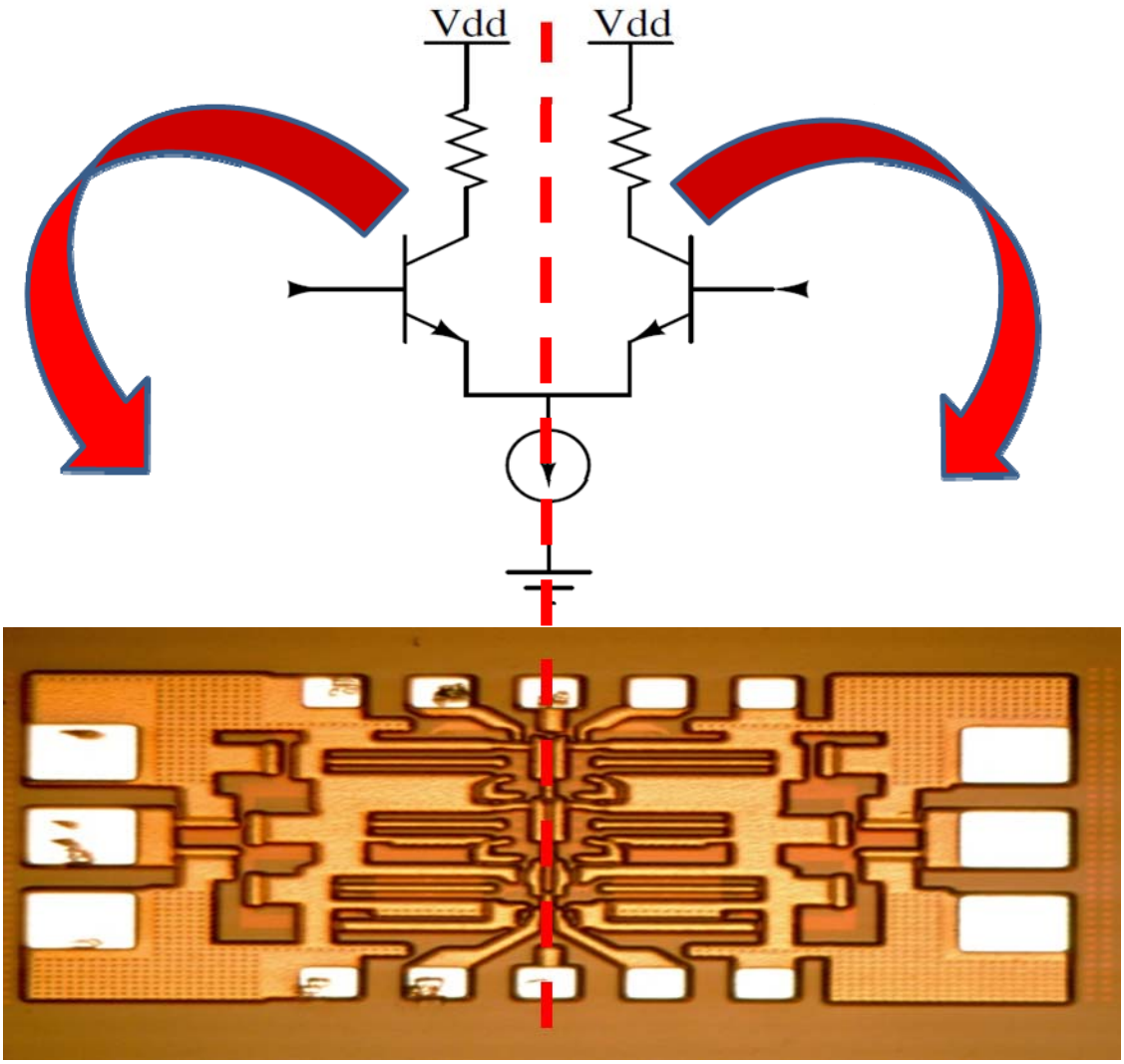
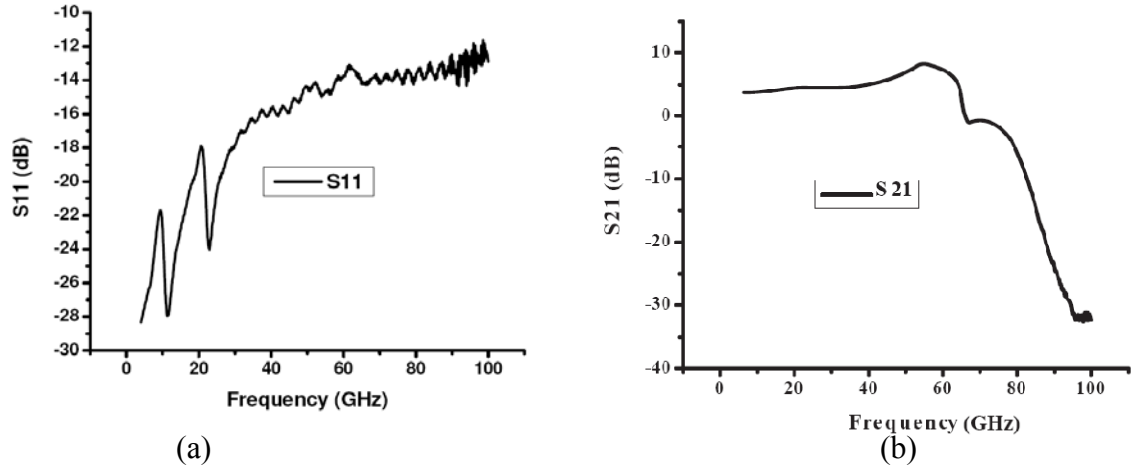


Figure 10. The die-photograph of the LA showing how the differential sections are mapped.

The measured S-parameters from 1-100 GHz, with an input power of -18 dBm, are shown in Figure 11. Figure 11 (a) shows that S_{11} is below -14 dB for the entire band of interest. Figure 11 (b) shows a mid-band gain of 5 dB with a bandwidth in excess of 60 GHz.



(a) (b)

Figure 11. Measurement results: (a) S11 and (b) S21 data.

Since single-ended measurements were performed, 6 dB was added to S_{21} to obtain a mid-band differential gain of approximately 5 dB. This is about 3dB lower than the post-layout extraction simulated gain. There are two possible reasons for this observed difference:

1) To reduce parasitic elements, the layout was made symmetrical and compact by avoiding the crossing of DC and RF paths. Hence to properly bias the chip, the same supply must be provided to both sides of the chip. Because of equipment limitations, the measurement setup provided bias to only one side of the chip resulting in an asymmetric biasing to the two arms of each differential pair; and 2), large MOSFETs were used as tail current sources for the differential pairs to enable low voltage operation. This leads, however, to a degradation of CMRR, which has a lower impact on circuit performance in true differential operation but degrades performance for single-ended operation (S-parameter measurements) which is compounded with the asymmetric biasing condition

Time Domain Measurements

Due to the unavailability of a pattern generator operating above 12.5 Gb/s, we were unable to measure the chip at 100 Gb/s speeds. Hence, shown in Figure 12 is the post-layout extraction simulated eye diagram of the chip operating at 100 Gb/s. This post layout simulation

result is validated by the measured S_{21} result, which shows a bandwidth in excess of 60 GHz, adequate for a data rate of 100 Gb/s.

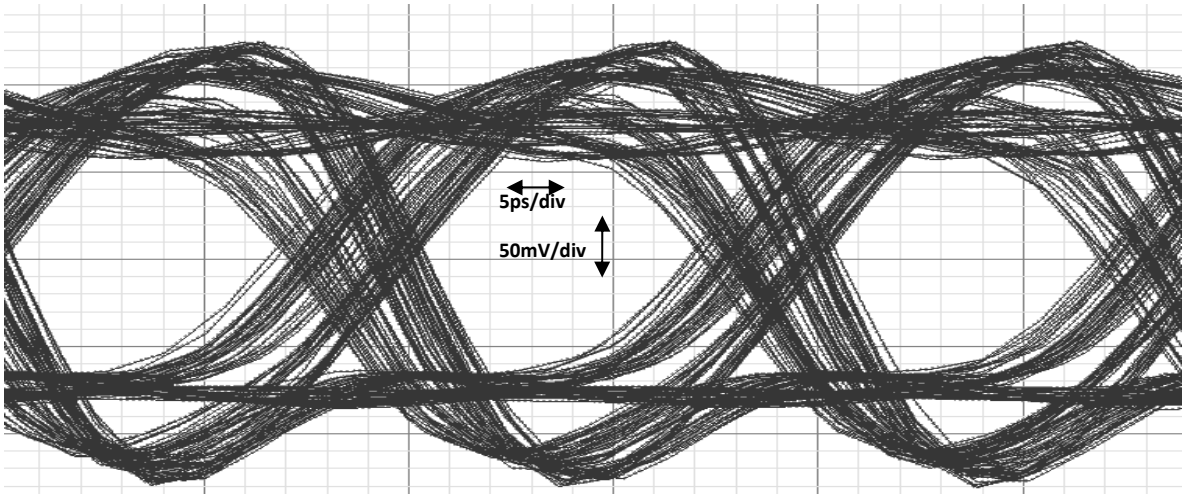


Figure 12. Simulated eye diagram for a data rate of 100 Gb/s.

Summary

A broadband SiGe amplifier designed in a 130 nm, 200 GHz f_T SiGe process is presented for application to 100 Gb/s Ethernet. The amplifier achieves a mid-band differential gain of 5 dB across a bandwidth in excess of 60 GHz, with a power consumption of 50 mA from a 2.5 V supply. To our knowledge, this is the lowest reported power consumption for a 60 GHz broadband amplifier. Table 1 compares this amplifier with some notable work. It can be noted that the present work significantly improves the power and bandwidth performance compared with previously reported results.

Table 1- Comparisons with other broad-band designs.

Author	Results			
	BW [GHz]	Gain [dB]	Supply [V]	PWR [mW]
R. Krithivasan, 2005 [14]	24	42	-5	550
W. Perndl, 2004 [15]	62	16	-5	770
K. Ohhata, 1999 [16]	32.7	19	-7.5	725
This work [13]	62	5	2.5	125

CHAPTER 3

NOVEL, CIRCUIT-LEVEL

SEU HARDENING TECHNIQUE

The problem of single-event upset was first recognized in the early 1960s [18]. In a publication in 1975, anomalies were reported in circuits being used in satellites [19]. The upsets in the circuits were then attributed to cosmic rays. In 1975, another research team reported SEUs in standard very-large-scale-integration (VLSI) circuits, even in terrestrial environments [20]. This was attributed to α-particles emitted by the packaging materials. Even though the purity of packaging materials has been considerably improved since 1975, progressive downscaling of technology still makes SEUs an area of concern [21-22]. Terrestrial cosmic rays have also been shown to cause SEUs even in the absence of α-particles from packaging materials [23-24].

SiGe is inherently tolerant to a large total ionizing dose (TID) of radiation. This built-in total dose hardness, unfortunately, does not translate into improved single-event upset response for high-speed SiGe hetero-junction bipolar HBT digital logic [25]. Hence, substantial research efforts have been aimed at improving SEU immunity at both the circuit and the system level [25-26]. Substantial improvement in SEU response was observed with the implementation of triple-module redundancy (TMR) [26]. Unfortunately, this implementation consumes three times the power of a standard implementation.

3.1 RELATED WORK ON CIRCUIT-LEVEL RADIATION HARDENING

One of the first attempts at SEU mitigation was made by the introduction of the current share hardening (CSH) technique [27]. Figure 13 shows the diagram of a CSH block. This method only shows marginal improvement in overall SEU immunity at the cost of great area penalty [26]. The hardened version of CSH is also slower compared to its unhardened version.

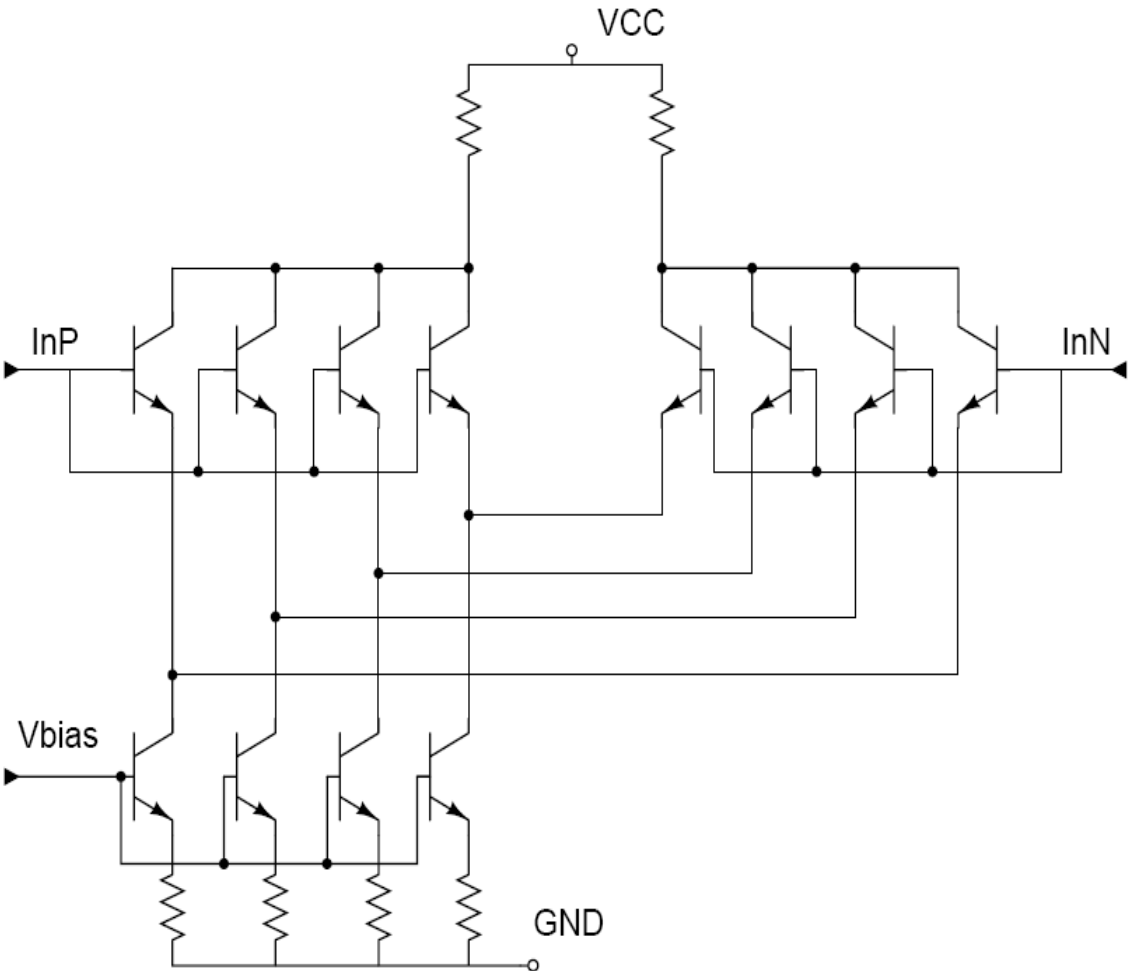


Figure 13. Current shared hardening.

Recently reported hardening techniques like dual-interleaved (DI) and gated-feedback have shown improvement in SEU immunity at the cost of over 100% power and area overhead [25].

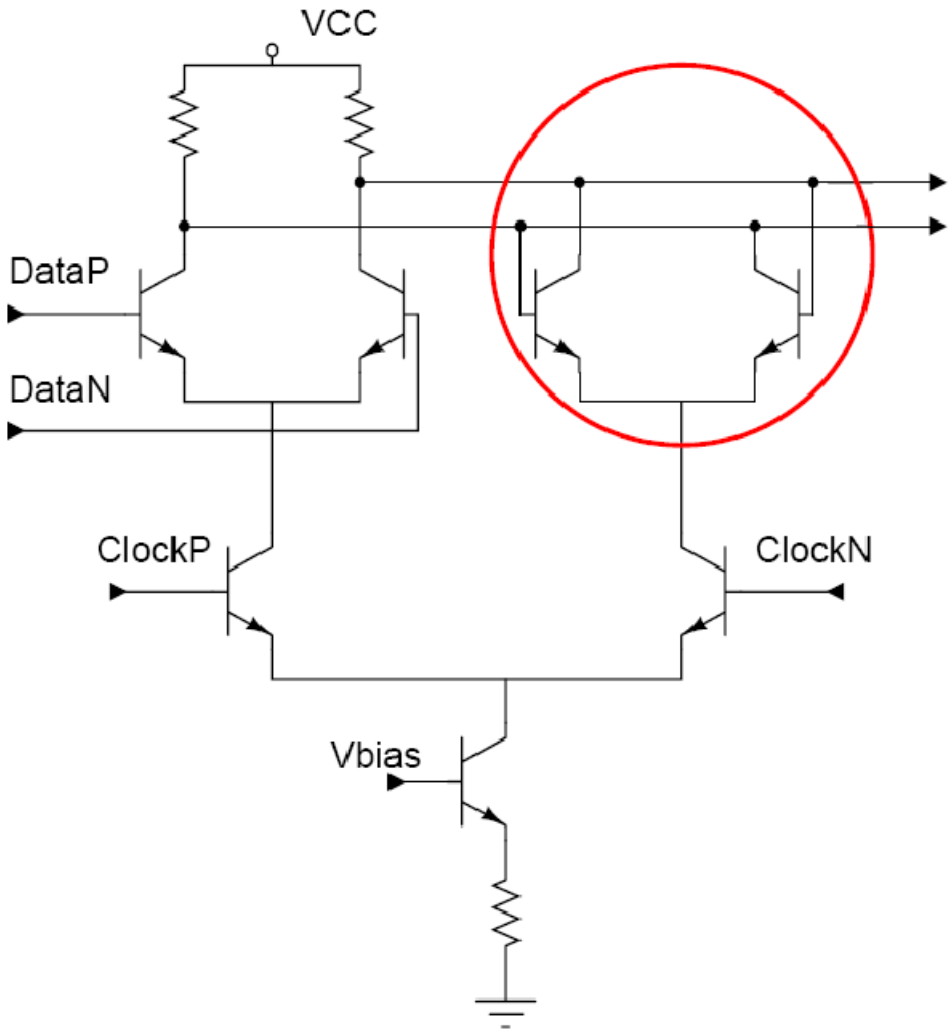


Figure 14. The cross-coupled cell was identified as the most sensitive block of the CML.

A detailed study was previously conducted on the sensitivity of different nodes in a CML to radiation [28]. The result of this study identified the transistor-level cross-coupling present in the CML storage cell to be the most vulnerable node, as shown in Figure 14. In response to this discovery, a new method of SEU mitigation, the DI, was proposed [28]. In the DI method an attempt is made to partially de-couple the storage cell transistors by interleaving two duplicate

logic cells. The partial decoupling weakens the propagation of the effect of a hit on any one transistor to the others. Unfortunately, as shown in Figure 15, the implementation of the DI topology requires duplication of each logic block, leading to twice the power consumption of a single block. The idea explored in the present work is to try to adapt a similar concept at a lower level of abstraction.

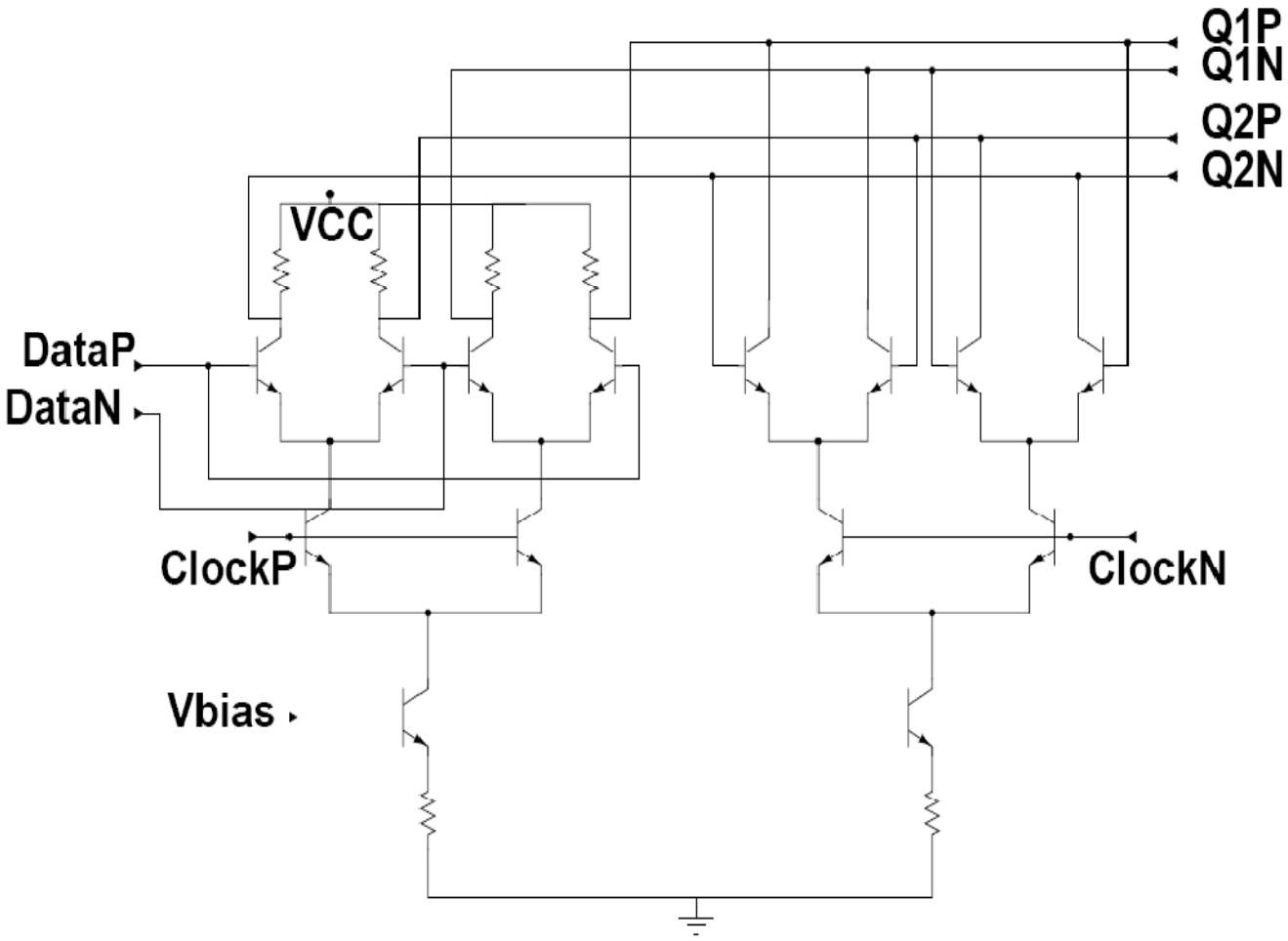


Figure 15. The dual-interleaved architecture.

A novel circuit-level SEU hardening technique has been proposed to mitigate the effect of radiation on SiGe-based circuits. The technique has been applied to both CML and LVL families, with significant improvement over the unhardened versions. The functional validity of the present SiGe SEU-hardening approach has been verified via simulation in state-of-the-art 200 GHz SiGe technology (IBM 8HP) [29], using calibrated 3-D TCAD simulated ion-strike current waveforms. Calibrated 3-D TCAD has been proven to reliably predict SEU occurrences with results matching measurement values [30]. SEU-free operation has been simulated up to data rates as high as 25 Gb/s [31].

3.2 DISCUSSION OF STANDARD AND MODIFIED ARCHITECTURES

Effect of Radiation on Standard Low- Voltage Logic

The standard low-voltage logic latch is depicted in Figure 16. The critical nodes for investigating the SEU tolerance of this circuit are the nodes Q and $\overline{Q}$, as verified via ion strikes on all circuit nodes. An ion strike to either the transistor M1 or the transistor M2 leads to an upset in the latch output over multiple clock cycles. This is a result of the strong positive feedback of the cross-coupled pair, as well as the current steering between the two storage transistors. Assuming that node Q is high and node $\overline{Q}$ is low, prior to an ion strike on M1, almost all of the bias current of the storage cell flows through M2 (since the node $\overline{Q}$ is in the "low" logic state). The ion strike changes the state of Q from a logical high to a logical low**,** causing the base of transistor M2 to be driven to a low state. The tail current is subsequently steered from M2 to M1 (which is in the opposite state), and thus the node $\overline{Q}$ now is forced "high," leading to an upset in the output of the latch – an SEU event.

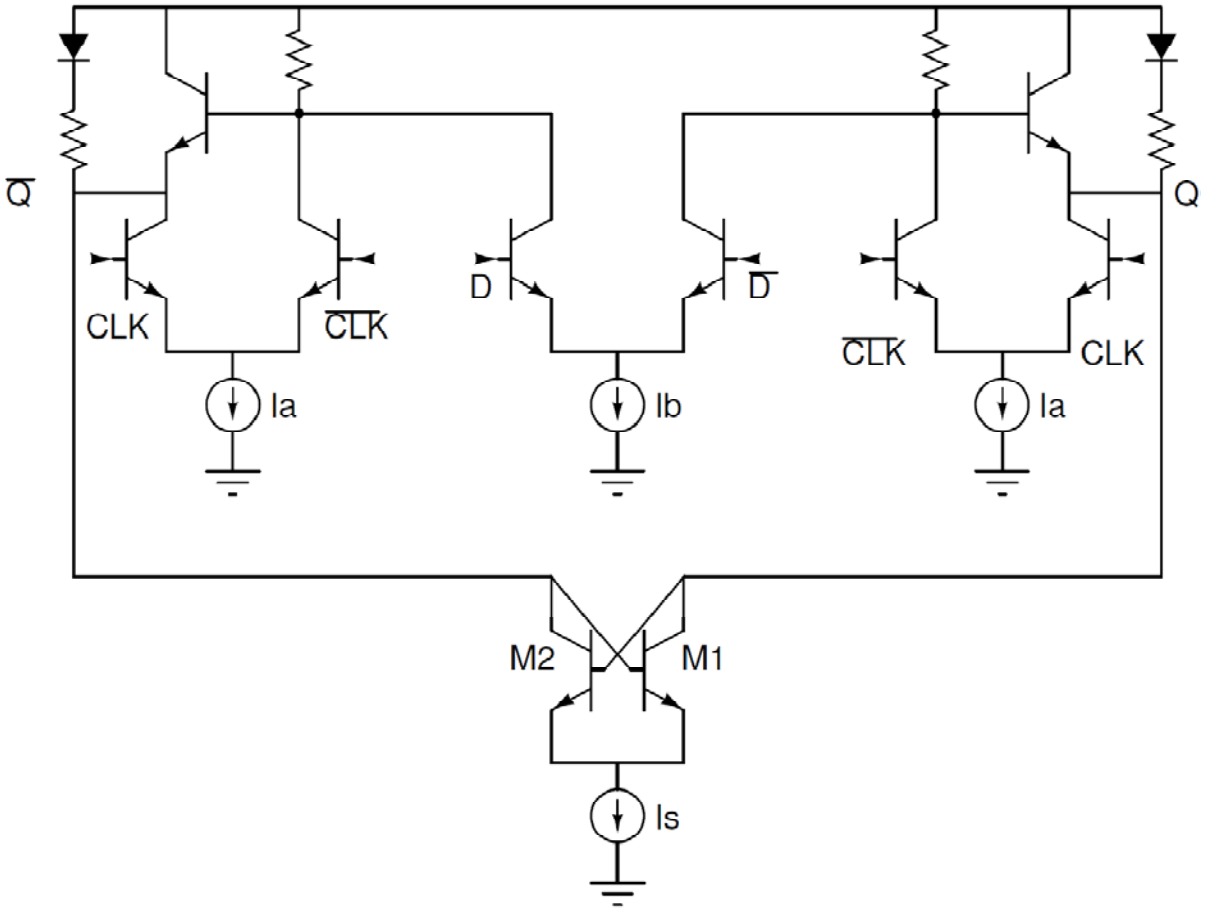


Figure 16. Schematic diagram of low-voltage logic latch.

Effect of Radiation on Standard CML

The standard CML flip-flop is depicted in Figure 17. Prior investigations of this topology have identified the cross-coupled storage cell as the critical node with respect to SEU. The upset mechanism in the storage cell following an ion strike is similar to the mechanism discussed in the case of the LVL topology [32-33]. One important distinction is that, unlike the CML topology, the storage cell in the LVL topology is driven by emitter followers. As a result, the accumulated charge in the device is likely to be dissipated to the power rail much faster in the

case of LVL when compared to CML as a consequence of the very small impedance presented to it by the emitter followers. Moreover, the storage cell in the low-voltage logic is composed of transistors one-third the size of transistors in the pass cell, thus reducing the likelihood of a direct ion hit inside the deep trench (DT) as well as the amount of charge collected in the event one does occur. This can be contrasted to the standard CML implementation in which both the pass and storage cell transistors are of the same size.

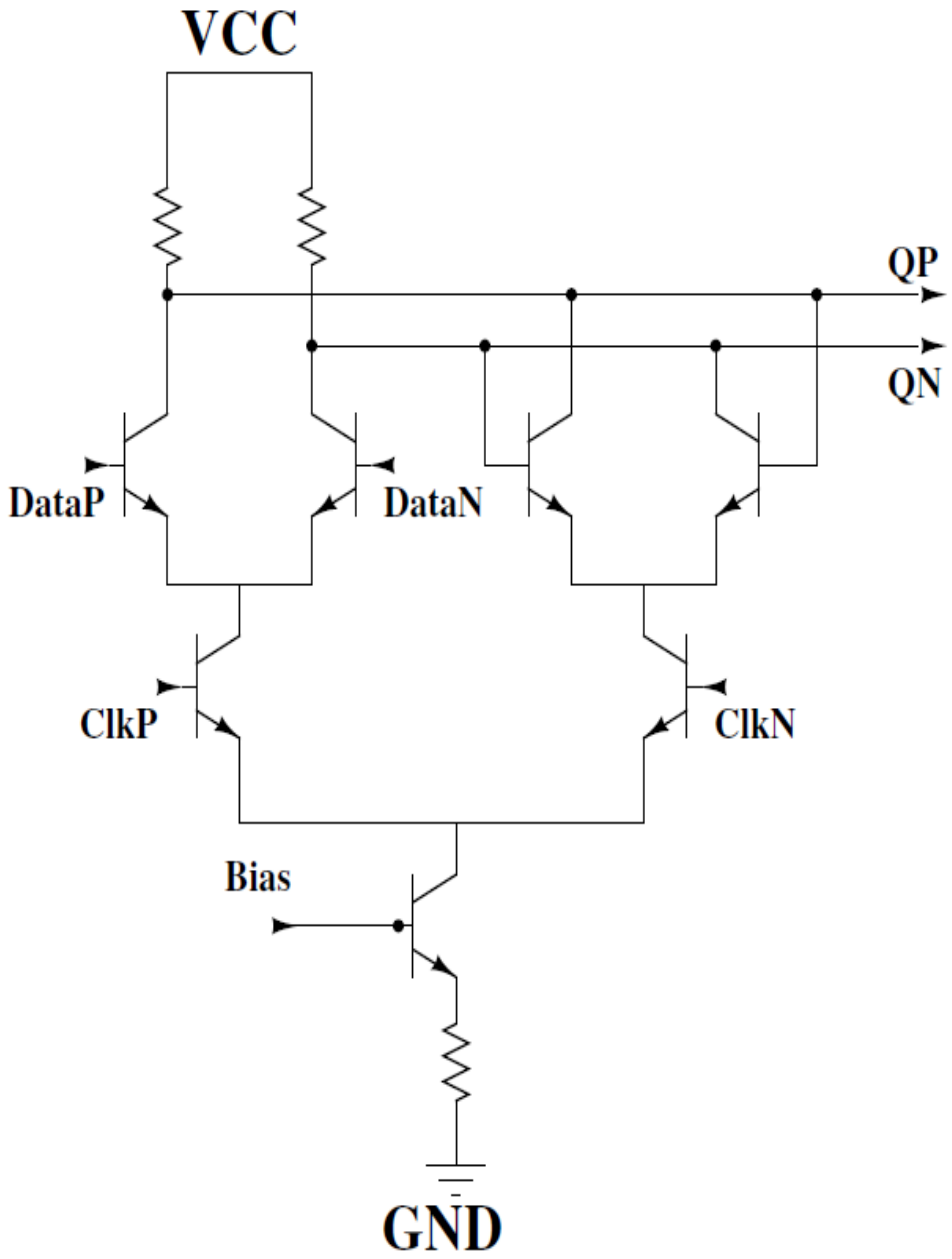


Figure 17. Schematic diagram of a standard CML latch.

Novel SEU-hardened low-voltage logic

The hardened version of the LVL latch is depicted in Figure 18. In the unhardened version, the tail current (I_s = 0.5 mA) of the storage cell is much smaller than that of the pass cell (I_a = 2.5mA and I_b = 1.5mA). Therefore, adding redundancy to the storage cell incurs less power penalty than duplicating the entire latch as in [34], or using CSH or GFC approaches [27,35]. In the modified storage cell, transistors M2 to M7 are used to achieve decoupling.

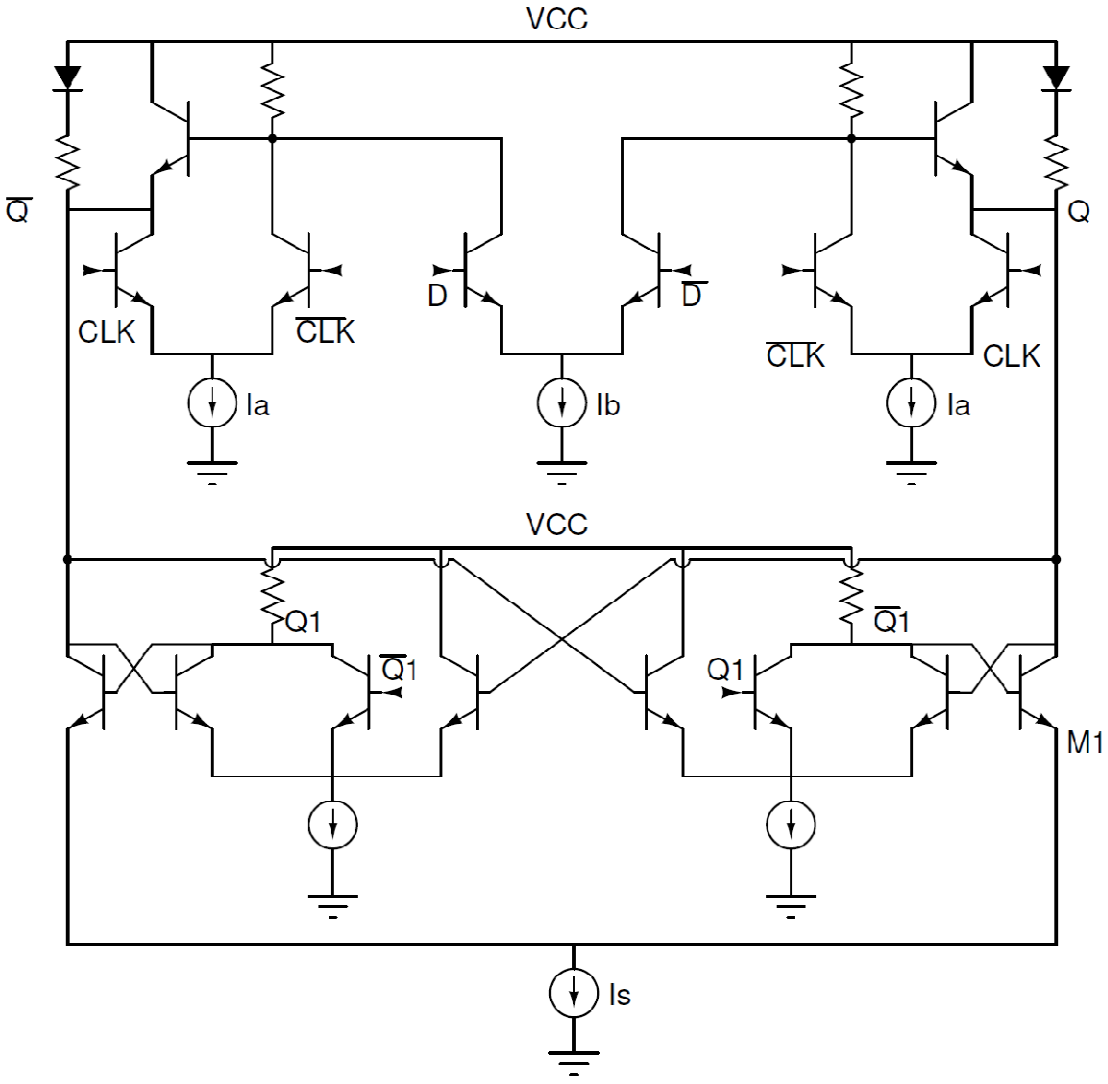


Figure 18. Schematic diagram of SEU hardened low voltage logic.

In the unhardened circuit, an upset is caused when the current is shifted from the node at the low logic state to the node at the high logic state. In the modified storage cell, however, this possibility has been minimized. That is, in the hardened version, we assume that M1 is hit when Q is in the "high" state. Prior to the strike, transistors M2 and M3 are both turned on. The node Q goes low after the hit and turns transistor M2 off. Transistor M3, however, still remains in the low state and sinks all of the I_{s1} current. The current through the resistor connected to M2 and M3 remains the same, holding the state of $\overline{Q}1$ low. The current is transferred to a device in the same state rather than to an opposite state, thus preventing an upset at $\overline{Q}1$ and subsequently at $\overline{Q}$. The result is that the succeeding stage (which is also differential) can reconstruct the data using the difference between Q and $\overline{Q}$. The hardened version of this circuit preserves the reduced transistor stacking of the unhardened version, enabling it to work at low voltages without a speed penalty. The power penalty of this RHBD approach is only 14.3%, compared to 100% in DI and 300% in GFC. The transistor count and layout area are also significantly reduced when compared to current SiGe SEU mitigation techniques.

Application of the method on CML

As previously stated, the same technique can be adopted for a standard CML latch (Figure 19). The hardened circuit shows measurable improvement in SEU compared to the unhardened version, but shows reduced SEU mitigation for moderate LET ion hits compared to LVL.

One possible explanation is that the technique shields one node of the differential data from the effects of an ion hit on the complementary node. Therefore, any succeeding differential stage can easily reconstruct the data. In the low-voltage logic, the voltage at the affected node is quickly pulled up by the emitter followers to a level above the logic '0,' and simultaneously the

SEU hardening network prevents the effects of the hit from propagating to the other node. Thus, the succeeding stages are able to correctly identify the actual data.

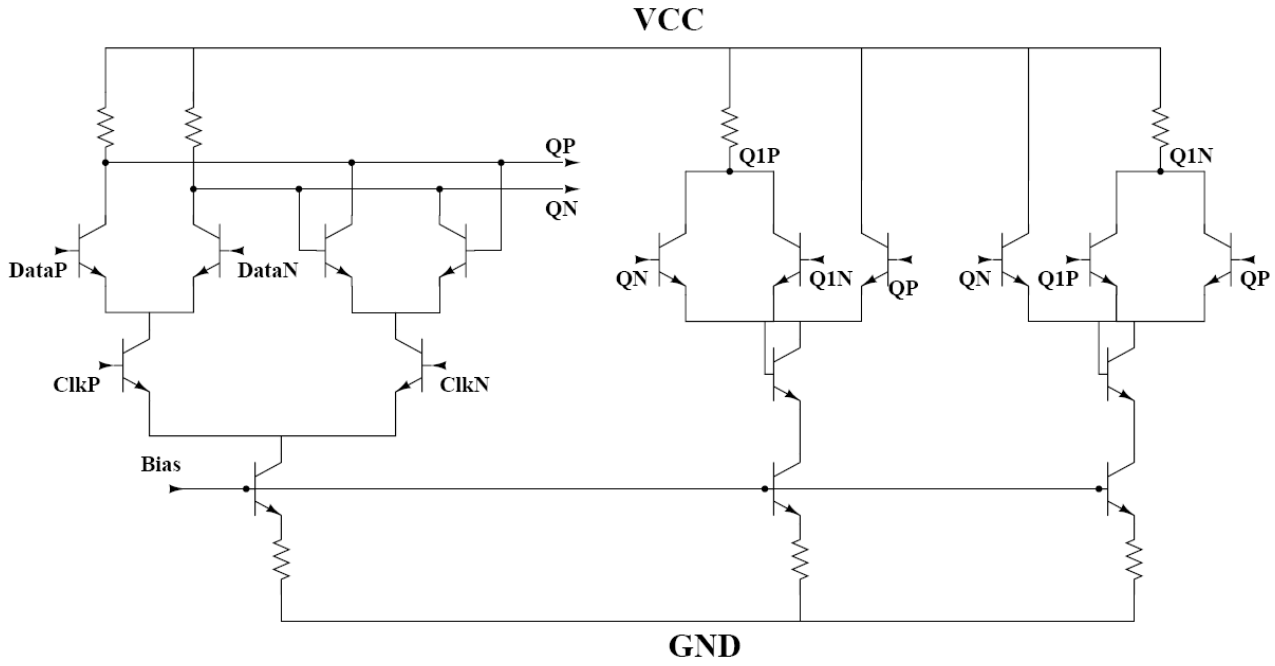


Figure 19. Schematic diagram of CML hardened with the proposed technique**.**

Moreover, the variation of the voltage at the node hit is limited as the node has no other transistor stack below it. However, in case of CML, the voltage variation of the node hit is well below the level of logic '0' for a period of time due to the lack of emitter followers to pull it up. Also, the presence of transistor stacking below it allows a much bigger fall in voltage level. Hence, even though the SEU hardening network does shield the other node from the effects of the hit, the succeeding stage cannot correctly identify the data at this point.

The SEU performance of the hardened CML is still better than the unhardened version. This is because as soon as the voltage level of the node hit returns to a value above logic '0', the next stage can identify the data correctly, as the opposite node still has the correct data. Thus, the difference between the nodes provides the correct logic. In the case of the unhardened CML, the data at the node complementary to the one hit is also reversed because of the strike and it stays

that way until the level at the node that was hit crosses the data threshold. The result is that it takes much longer to correct the SEU.

3.3 RESULTS AND ANALYSIS

To validate the SEU hardening approach, calibrated TCAD simulations were used to obtain the terminal upset currents corresponding to a heavy ion strike at linear energy transfer (LET) values of 0.1 pC/μm, 0.2 pC/μm, and 0.5 pC/μm [34]. These time-domain upset currents were then incorporated into the Spectre simulator in Cadence in a similar fashion to that reported in [35]. Because the LET of 0.1 pC/μm failed to produce any upset even with the CML, the results are not presented here and the LET is designated as a "low LET" ion hit. The LET of 0.2 pC/μm did not cause an upset with the LVL but affected the CML hardened version. This is designated as a "moderate LET" ion hit. The LET of 0.5 pC/μm caused an upset even with the hardened LVL. This is designated as a "high LET" ion hit.

The simulations were performed with a single flip-flop and with an 8-bit shift register, both for the LVL and CML topologies. As no significant differences were observed between the flip-flop-level and register-level upset sensitivity, we will concentrate on register-level upset results.

Moderate LET single-ion hit (LVL and CML)

Figures 20-23 show circuit simulation results of the hardened versus unhardened LVL register at data rates of 12.5 Gb/s, 20 Gb/s, and 25 Gb/s (corresponding to clock rates of 12.5 GHz, 20 GHz, and 25 GHz) and at an LET of 0.2 pC/μm. The ion-strike-induced transient current was triggered in all of the circuits at 5 ns.

The register level simulation results of the hardened vs. unhardened CML at a 6 Gb/s data rate are shown in Figure 20. In order to have a fair comparison, the power dissipation in both the LVL and CML are kept the same. Unfortunately, with the same amount of power as LVL, the

CML topology was limited to a maximum speed of 6 Gb/s data rate. Although the results are not as good as for the low-voltage logic, they are still measurably better.

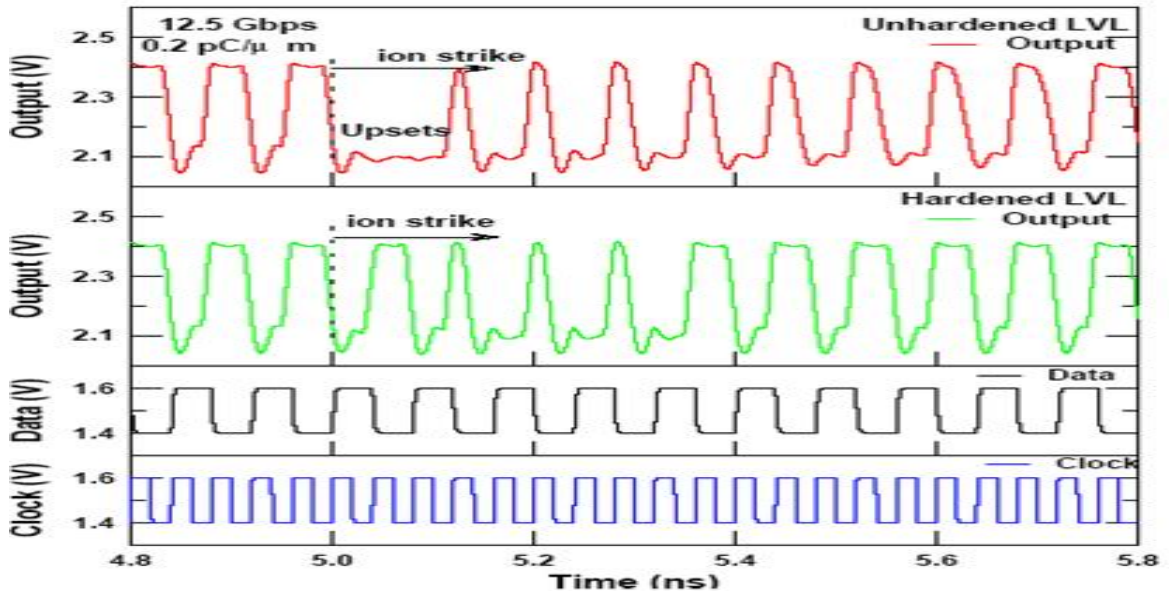


Figure 20. Simulation result of output, data and clock waveforms of unhardened (top) and hardened (2nd from top) LVL circuits at a 12.5 Gb/s data rate (LET = 0.2 pC/µm).

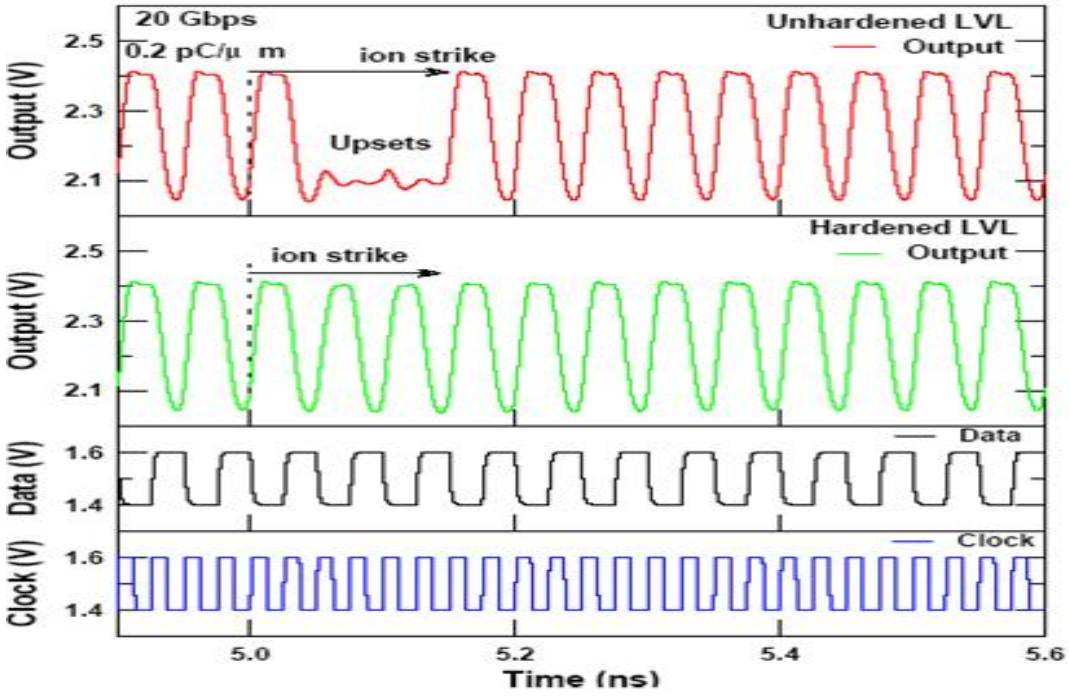


Figure 21. Simulation result of output, data and clock waveforms of unhardened (top) and hardened (2nd from top) LVL circuits at a 20 Gb/s data rate (LET = 0.2 pC/µm).

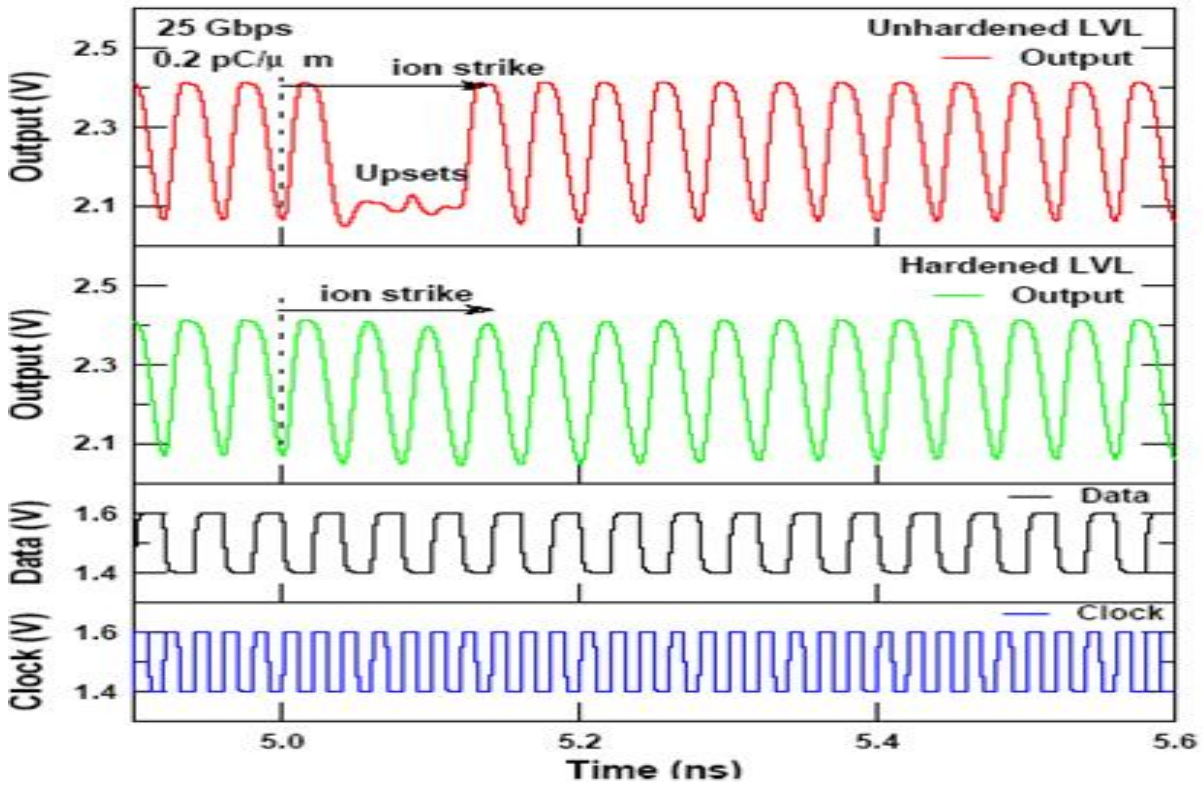


Figure 22. Simulation result of output, data and clock waveforms of unhardened (top) and hardened (2nd from top) LVL circuits at a 25 Gb/s data rate (LET = 0.2 pC/μm).

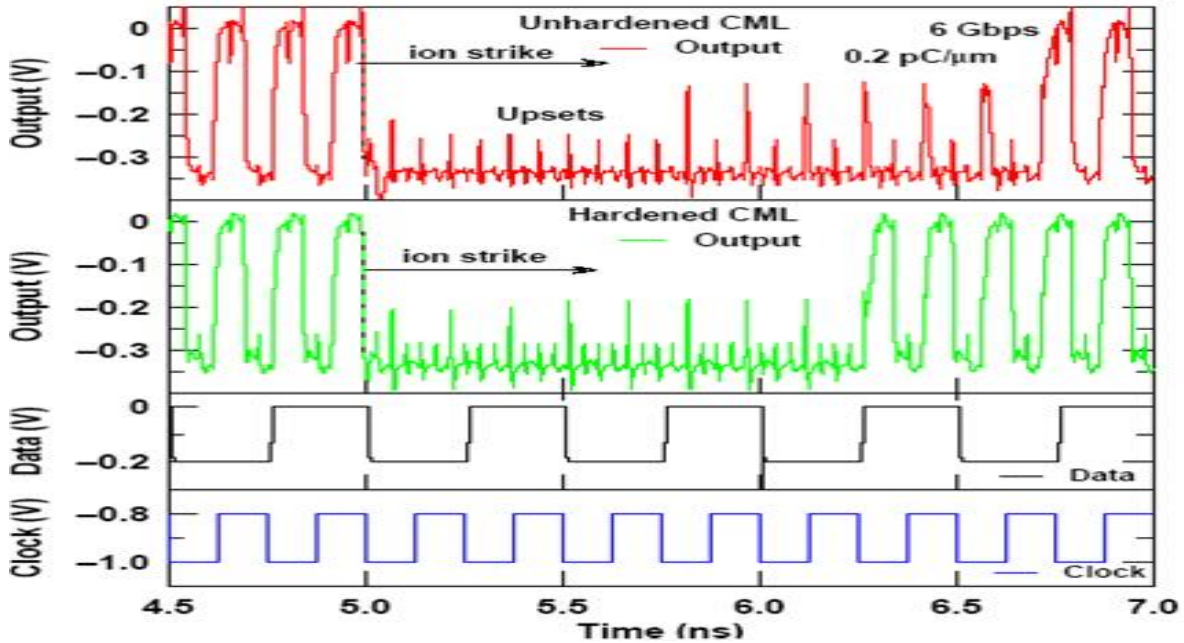


Figure 23. Simulation result of output, data and clock waveforms of unhardened (top) and hardened (2nd from top) CML circuits at 6 Gb/s data rate (LET = 0.2 pC/μm).

High LET single-ion hit (LVL)

The simulation results with the moderate LET ions failed to cause any upset in the LVL hardened version. Hence, the simulation was done with an LET of 0.5 pC/µm. At this LET, the hardened version just starts to show upsets. Moreover, the upsets start only above a data rate of 12.5 Gb/s. The simulation results show only a 2-bit upset at 12.5 Gb/s data rate. The dramatic improvement in SEU over the unhardened version is evident from the simulations (Figure 24).

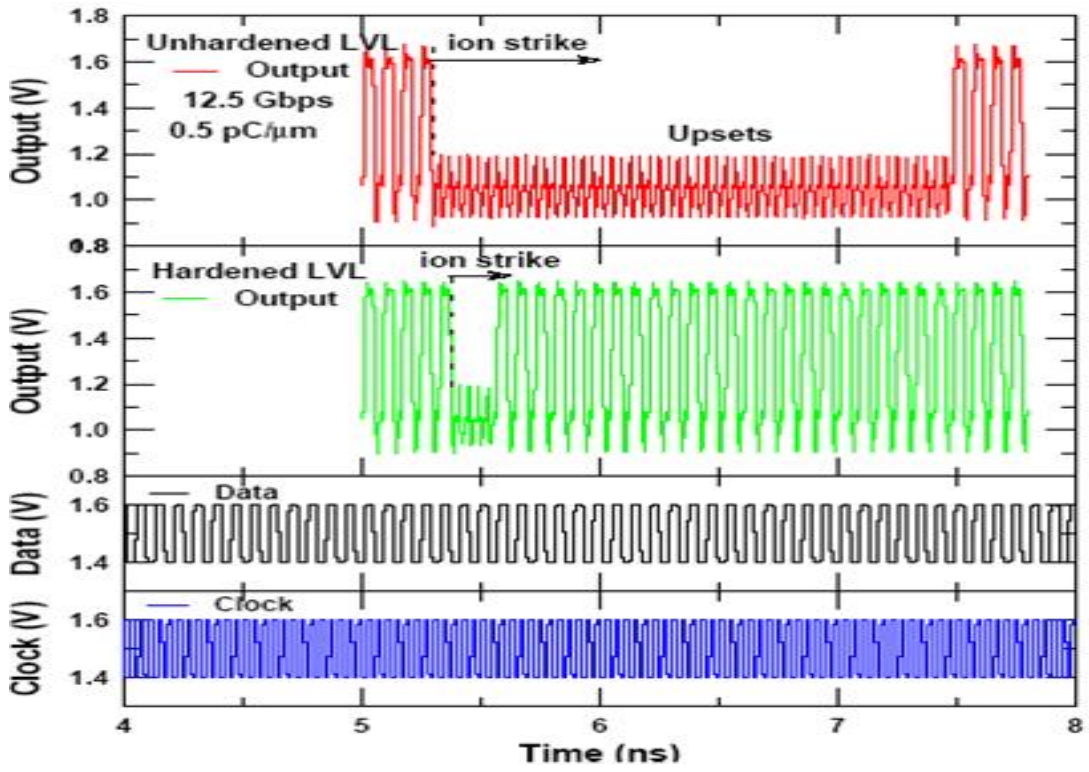


Figure 24. Simulation result of output, data and clock waveforms of unhardened (top) and unhardened (2nd from top) LVL circuits at a 12.5 Gb/s data rate for (LET =0.5 pC/ µm).

Moderate LET multiple-ion hits (LVL)

To obtain further insight into the working and the limitations of the approach, simultaneous hits to multiple transistors of the storage block of both the hardened and unhardened LVL have been simulated with an LET of 0.2 pC/µm.

Figure 25 (a) shows the simulation results of simultaneous hits on both transistors of the cross-coupled cell of the unhardened LVL. As the transient currents are equal in both of the branches, their effect at the output is a common-mode signal, which the succeeding differential stage rejects. Hence the output of the total register remains unperturbed.

Figure 25 (b-d) are the simulation results of two ion hits on the hardened LVL for various combinations of the nodes in the storage cell. Figure 25 (b) shows the results of ion hits to nodes Q and $\overline{Q}$ simultaneously. Again, the same effect observed in the case of unhardened LVL occurs. Thus, we deduce that if there are simultaneous hits to nodes that are complementary to each other in logic, the effect will be rejected by the next stage. Figure 25 (c), which shows the simulation results of hits on nodes Q and $\overline{Q}1$, offers further support of this theory.

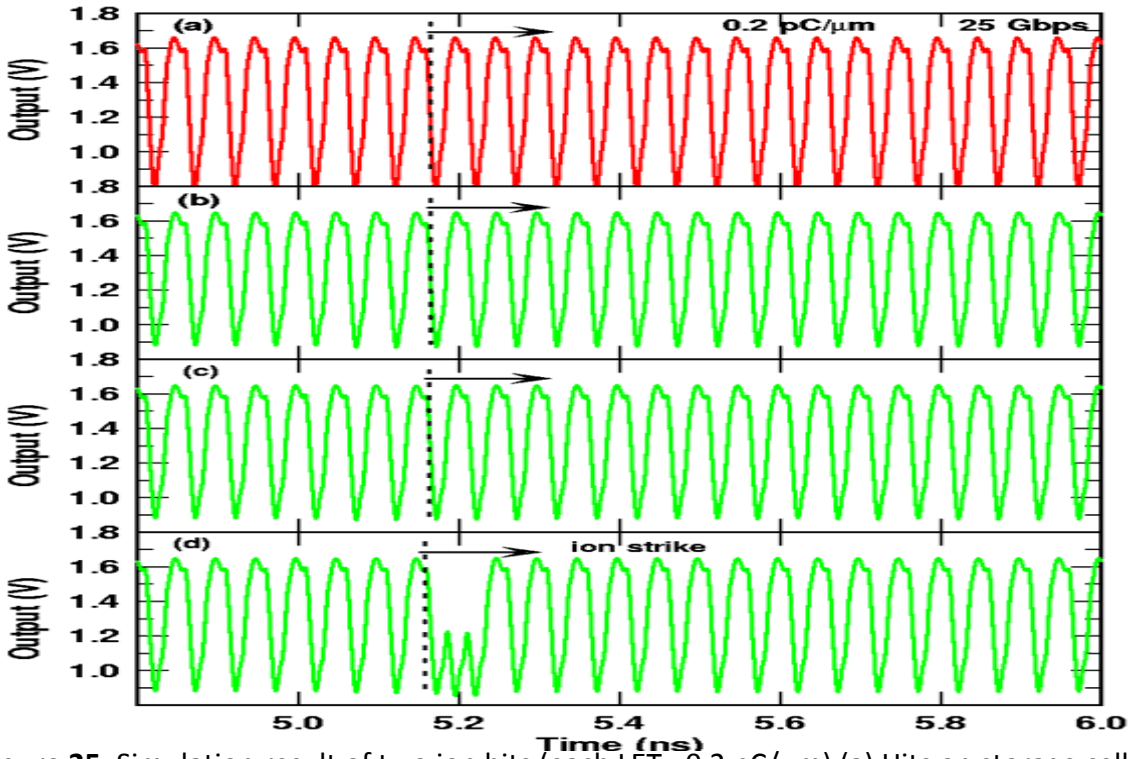


Figure 25. Simulation result of two ion hits (each LET= 0.2 pC/µm) (a) Hits on storage cell transistors of unhardened LVL (b) Hits on the nodes Q and $\overline{Q}$ of hardened LVL (c) Hits on the nodes Q and $\overline{Q}1$ of hardened LVL (d) Hits on the nodes Q and $Q1$ of hardened LVL.

Figure 25 (d) is the simulation result of hits on Q and $Q1$. The hardening network was designed to prevent an upset from occurring in the case of a SEU, which generally is the predominant cause of upsets. The two hits to the two nodes disrupt the corrective action of the network, which needs at least one correct result from either Q or $Q1$. Now both the other two nodes, $\overline{Q}$ and $\overline{Q}1$, suffer bit-flips, leading to an upset.

Figures 26 (a-b) show the simulation result of three and four ion hits to the hardened LVL, respectively. No upset is observed in either case. A probable explanation may be that since from among the three nodes hit at least two are always complementary nodes, the effect of an ion hit to these two is rejected. Thus the three ion hit case becomes almost equivalent to the single ion hit case, which the circuit can effectively mitigate. In the case of the four-ion hit case where all

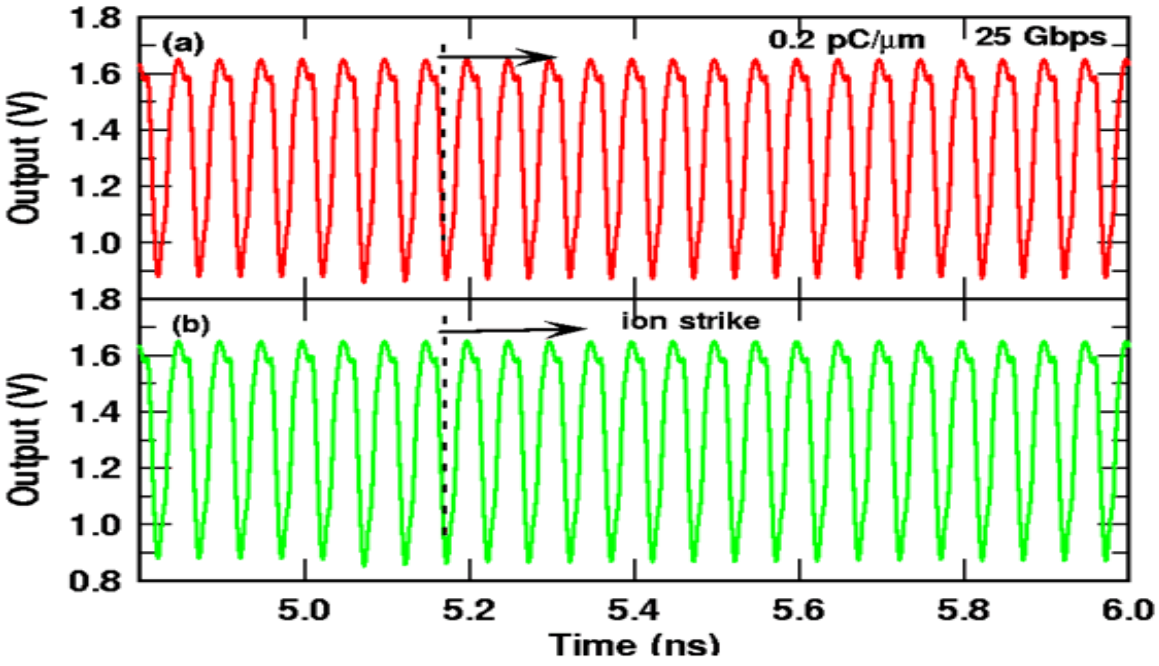


Figure 26. Simulation result of the hardened LVL register for ion hits on (a) Three nodes of the storage cell (b) Four nodes of the storage cell.

nodes of the storage cell of the hardened LVL, i.e. Q, $Q1$, $\overline{Q}$, and $\overline{Q}1$ are hit, the effect of the hit is rejected due to the common mode rejection, as discussed above. The chip micrograph of the radiation hardened LVL is shown in Figure 27, and the radiation hardened CML in Figure 28.

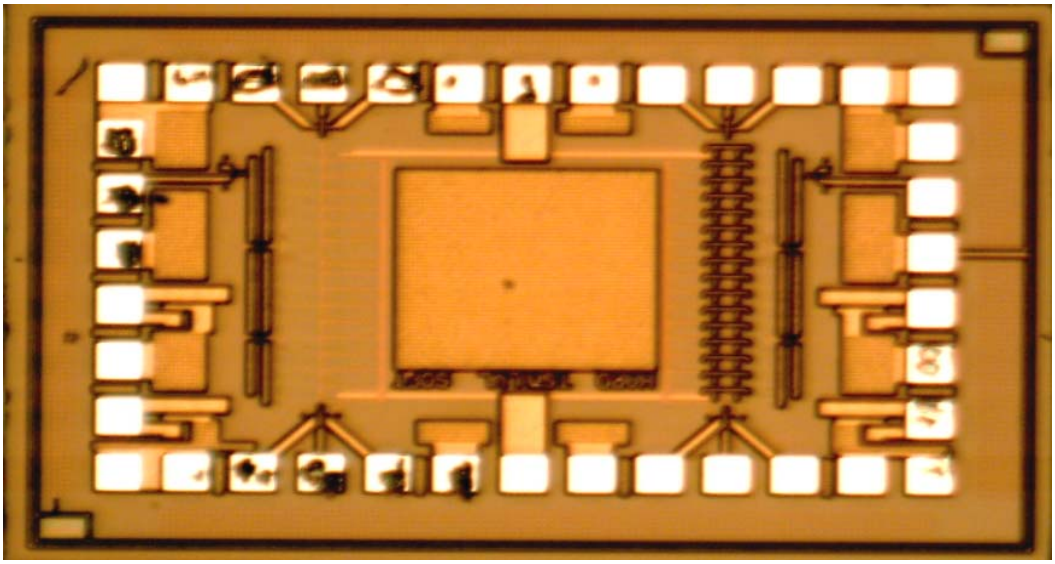


Figure 27. Chip Photograph of the radiation hardened LVL.

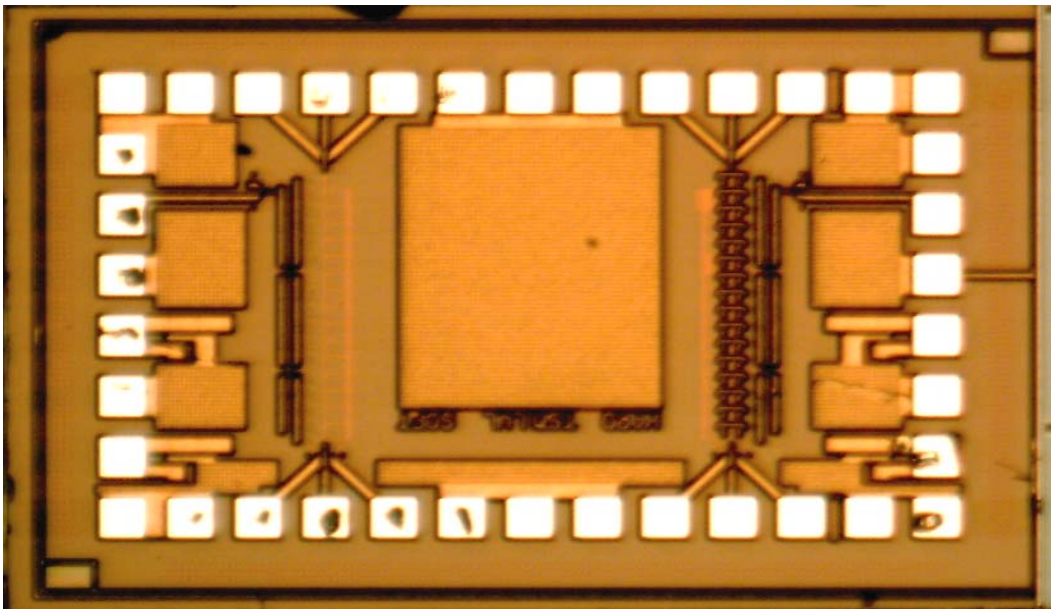


Figure 28. Chip Photograph of the radiation hardened CML.

Analysis of the Results

The simulation results show substantial improvement in the SEU performance of the hardened version compared to the unhardened version in case of the LVL. Figure 29 shows the differential output (Q & Q*) of a latch (LVL) hit and then the output of the latch succeeding it (Q only) for a moderate ion hit. It is evident that Q is distorted when it is hit by an ion but Q* stays at the correct level. The next stage, which needs only 20 mV of difference to identify the data, can then successfully regenerate it. Hence, the Q output of the next stage shows no perceptible effect of SEU.

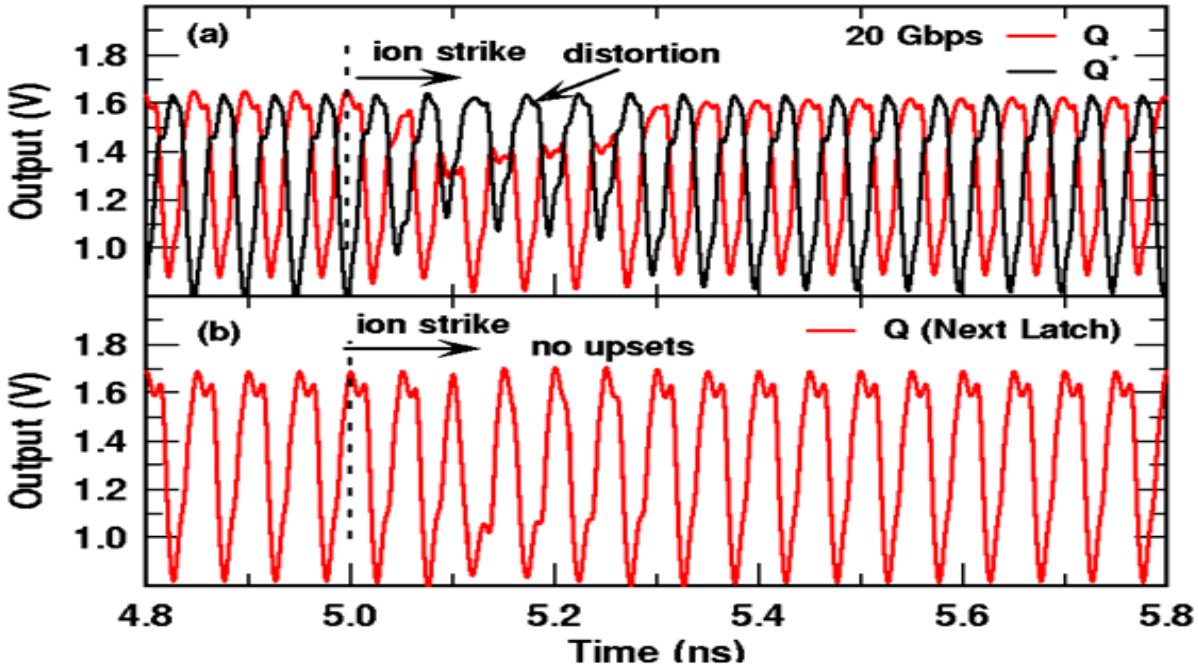


Figure 29. The output waveform of the latch hit (LVL) and the latch succeeding it. The waveforms show how a hit distorts the node hit, but the complementary node is not affected thus allowing the next stage to completely reconstruct the data.

Table 2 compares the different SEU techniques with respect to their power penalty and transistor count compared to their corresponding unhardened versions. The proposed technique has the lowest transistor count penalty with the smallest power penalty.

Summary

The results suggest that the new SEU-hardened low-voltage latch topology is an ideal candidate for use in harsh environments. Not only does it have the capability to operate over a very large bandwidth and support a very high data rate, but it also has the advantage of low-voltage / low-power operation. This SEU hardening technique can also be easily incorporated on existing CML with minimal effort on the part of the designer while providing it with moderate SEU immunity [31].

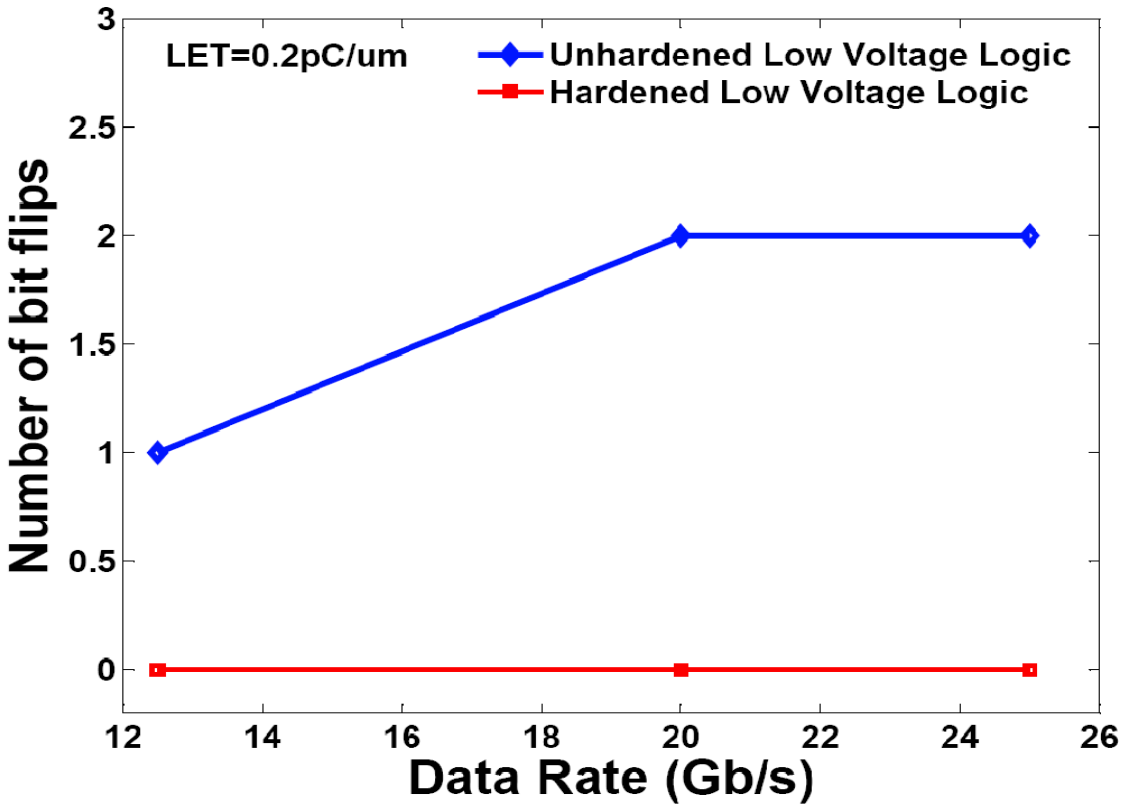


Figure 30. A comparison of number of upsets due to ion strike (0.2 pC/µm) on hardened and unhardened Low Voltage Logic. The data rates are 12.5, 20 and 25 Gb/s.

Table 2– Comparison of different SEU hardening techniques with respect to their incurred penalty over their unhardened versions.

Metric	Dual- Interleaved [24]	Current-Shared [26]	Gated Feedback [24]	This work (For LVL)
Power Penalty	100%	None	300%	14%
Area Penalty	60%	N/A	150%	50%
Penalty in Transistor Count	100%	400%	157%	80%
Supply Voltage (V)	3.3-4.0	3.3-4.0	3.3-4.0	2.0-2.5

CHAPTER 4

STUDY OF INJECTION-LOCKED CLOCK EXTRACTION

4.1 INTRODUCTION TO INJECTION-LOCKING

If a periodic signal of sufficient power is injected into an oscillator, at a frequency close to the natural frequency of oscillation, it is observed that the oscillator frequency locks onto the injected signal [36]. In its locked state, an oscillator exhibits a definite phase and frequency relationship with the injected signal. It is also observed that the frequency of the oscillator under injection-lock is an exact multiple or sub-multiple of the input signal and that the phase shows an inverse sinusoid relation with the power of the injected signal as shown:

$$\Delta f_{lock} = f_{osc} \cdot \frac{I_{inj}}{2 \cdot Q \cdot I_{tail}} \quad ; \tag{5}$$

$$\theta = sin^{-1}\left(\frac{f_{osc} - f_{inj}}{\Delta f_{lock}} \right) \quad , \tag{6}$$

where

Δf_{lock} is the locking range, f_{osc} is the VCO oscillation frequency, I_{inj} is the injected current, I_{tail} is the tail current, Q is the VCO quality factor, and θ is the phase shift of the VCO.

When an external signal is injected into an oscillator, it exhibits three distinct regions of operation, as illustrated in Figure 31. If the injected signal is within the lock range, the VCO output frequency locks perfectly onto to the injected signal [37]. If the input signal is just outside the locking range, then the VCO exhibits a phenomenon known as oscillator-pulling. When oscillator-pulling occurs in a VCO, the VCO output frequency is an interpolation between the

injected signal and the natural frequency of the VCO. If the injected signal is even beyond the pull-in range, then the output of the VCO is a mixing product of the injected signal and the VCO harmonics.

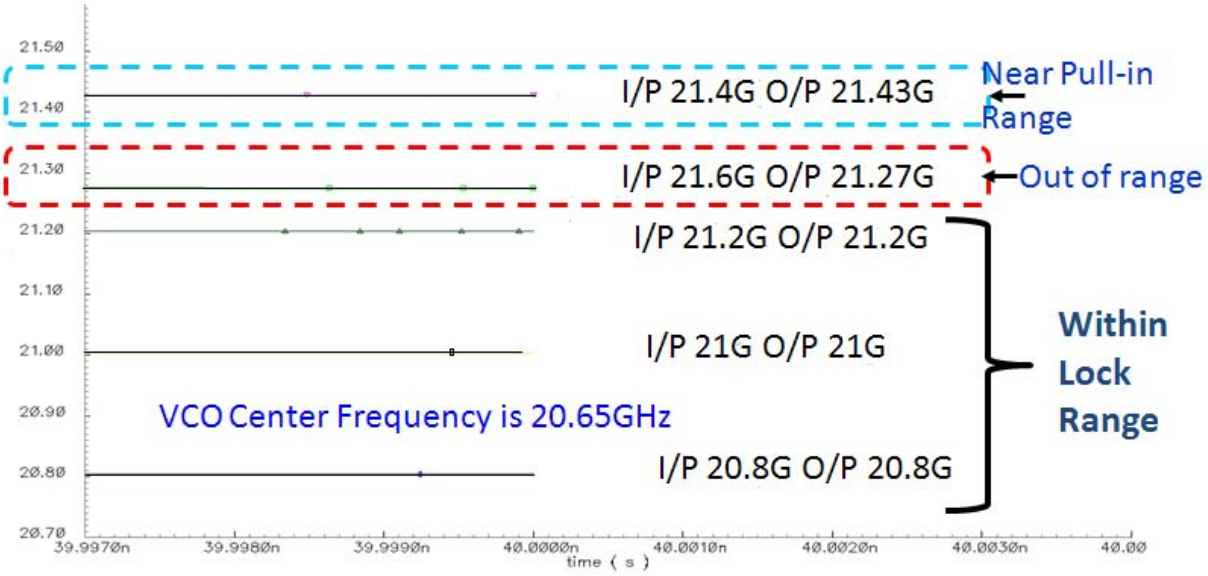


Figure 31. Average output frequency for different injection frequencies (using Cadence).

Due to the simple nature of the injection-locking scheme, a number of efforts have been made to utilize the phenomenon in wire-line CDRs [38]. In wire-line CDR applications, the transmitted data is generally coded in a NRZ format. As shown earlier in Figure 1, the spectrum of a PRBS data stream in NRZ format is the square of the Sinc function. It can be noted that the Sinc function has a null in power at the clock frequency. Hence, directly injecting the received signal into the tank of a VCO would fail to lock the VCO to any frequency. It has been claimed that unintentional electro-magnetic coupling in the circuit gives rise to residual power at the clock frequency, which can be amplified and directly injected into the tank of a VCO for clock extraction [39]. The amplification required to implement this scheme would involve unacceptable power consumption. Therefore, the received data would need to be passed through a non-linear spectrum processing block to generate harmonics of the data rate before trying to injection lock a VCO.

4.2 IMPLEMENTATION OF INJECTION-LOCKING

The easiest method to implement a harmonic generator would be to pass data, along with its delayed replica, through a digital exclusive-or (XOR) logic gate, as shown in Figure 32 [40-41]. The output pulse width generated by this scheme is equal to the delay element. At data rates nearing $f_T/4$ of the device technology, sharp pulses cannot be generated by this method. Hence, analog-based schemes need to be explored [42].

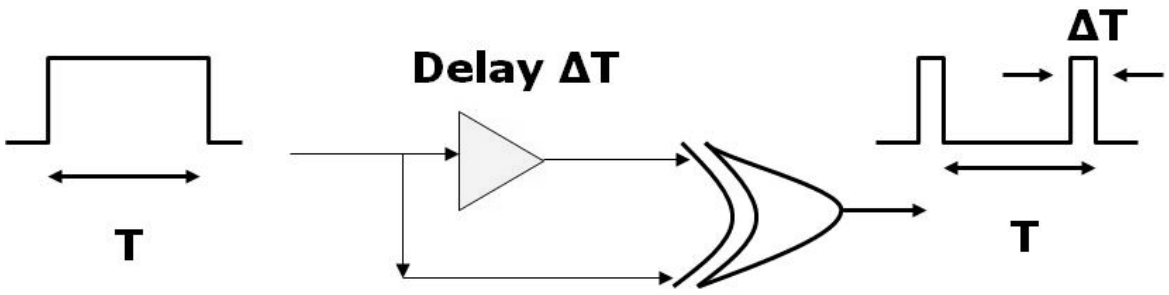


Figure 32. Digital implementation of a harmonic generator.

It has been shown earlier that a VCO can work in three different modes when a periodic signal is injected into it. It has also been shown that a pseudo-random data stream contains a null at the clock frequency and therefore cannot be directly used for clock recovery. Non-linear processing of the input data is the first step towards using injection-locking for clock recovery by injection locking. A non-linear processing block would generate multiple harmonics of the fundamental frequency. The power present in the fundamental frequency and its harmonics serve to generate the same phase-frequency lock condition.

A digital harmonic generator, though easy to implement, is unsuitable for high speed implementations. To alleviate this problem, analog based approaches have been tried in this work. The general analog approach is to first differentiate the data and then rectify it. In the present work, two approaches have been attempted. The first approach utilizes a modified

Gilbert Cell to perform harmonic generation. This cell is inherently differential. Hence, this method is useful for locking to the fundamental frequency or its odd harmonics. This cell, shown in Figure 33, can be directly connected to the tank of the VCO. The lower level switching pair of the cell has been coupled through a capacitor instead of a direct short as in a standard Gilbert Cell. This stage behaves like a differentiator. For a data bit at the input, this stage generates current pulses corresponding to the data edges. The upper stage behaves like a rectifier, and it only allows pulses of a fixed polarity to flow in each branch.

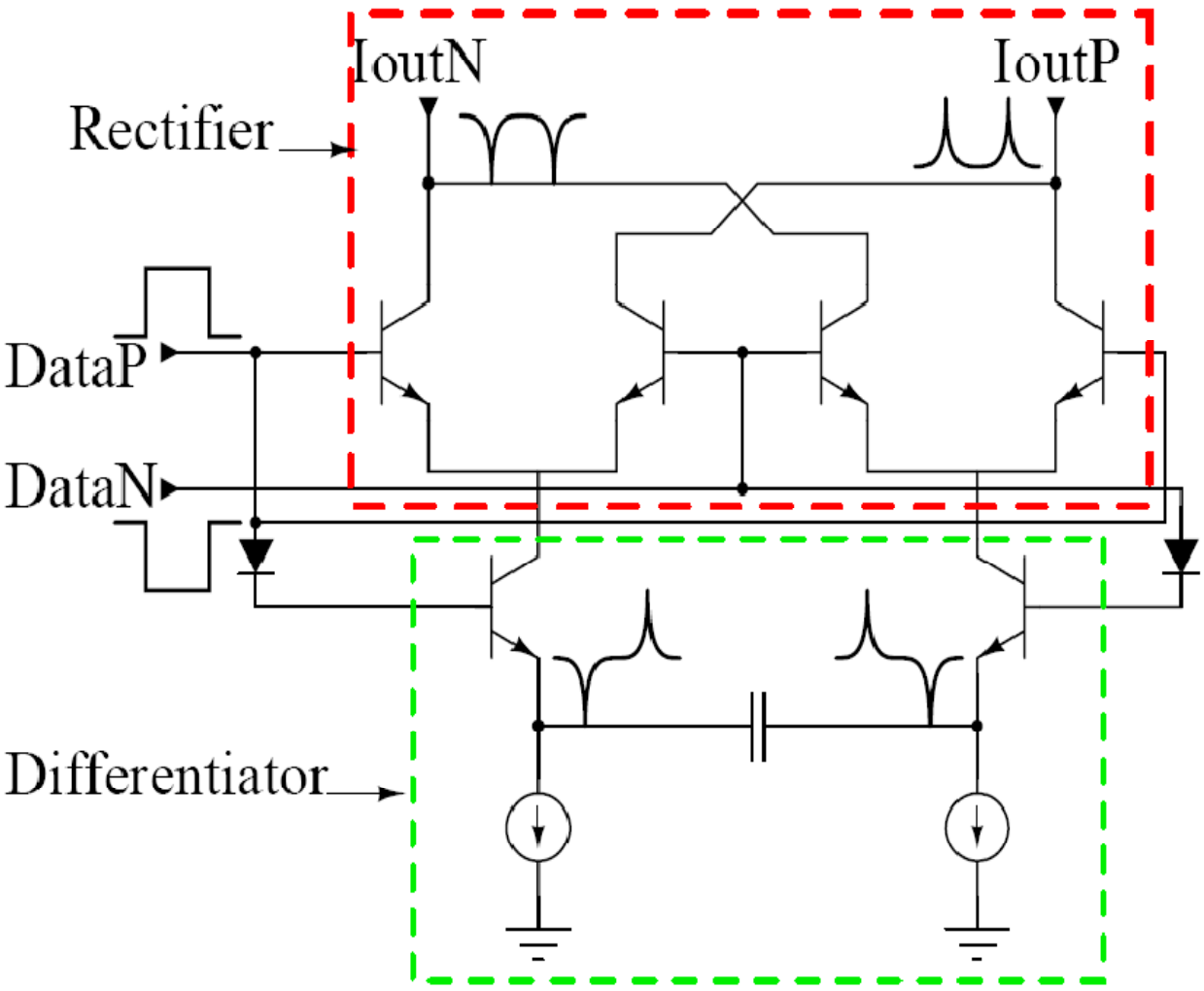


Figure 33. Modified Gilbert Cell harmonic generator.

The second approach for generating harmonics is to use an analog differentiator followed by a wired-or rectifier, as shown in Figure 34. This method generates strong components of the second and other even order harmonics of the fundamental frequency. In a generic cross-coupled VCO, the common-emitter node has a frequency component at twice the VCO oscillation frequency. Therefore, if a strong signal close to the second harmonic frequency of the VCO is injected into the common emitter node, as shown in Figure 34, then the VCO will start to

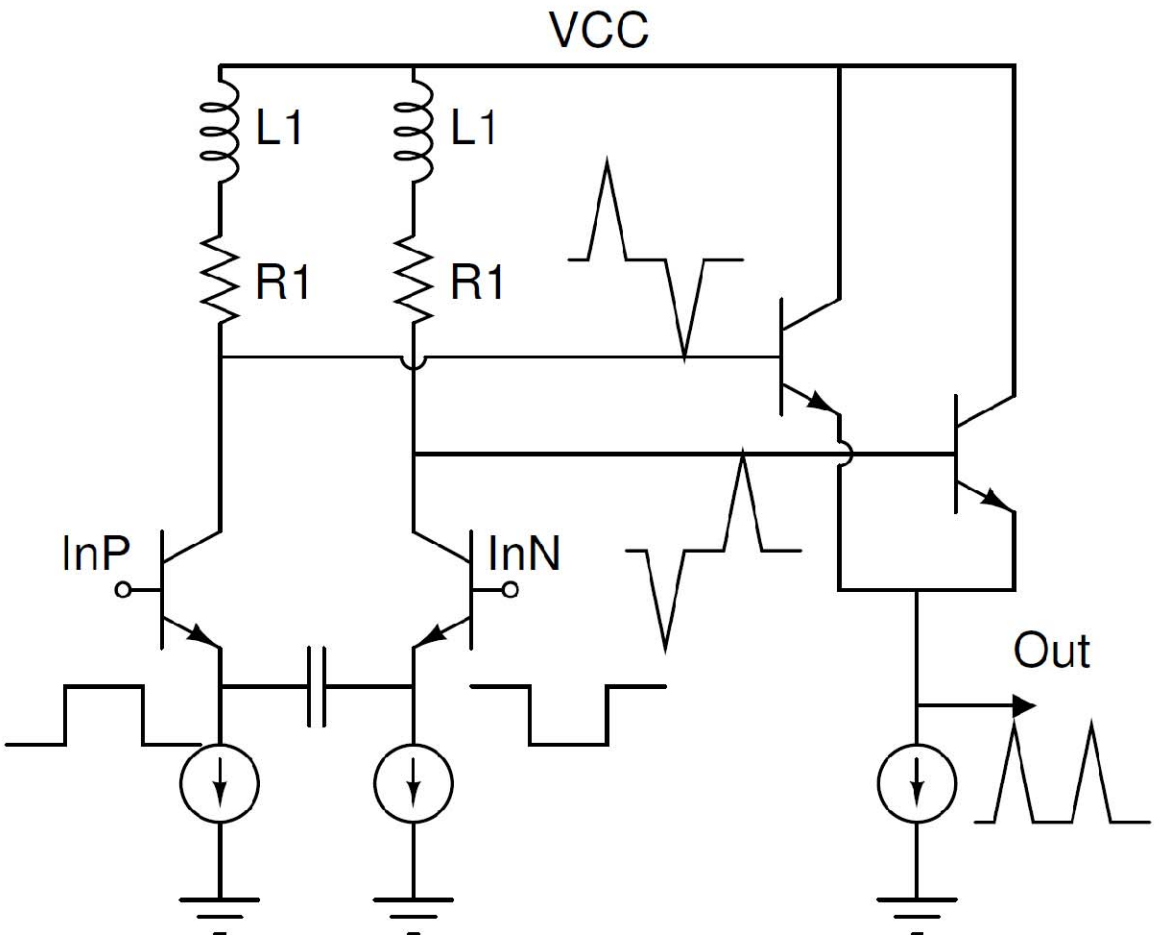


Figure 34. Analog differentiator followed by wired-or rectifier.

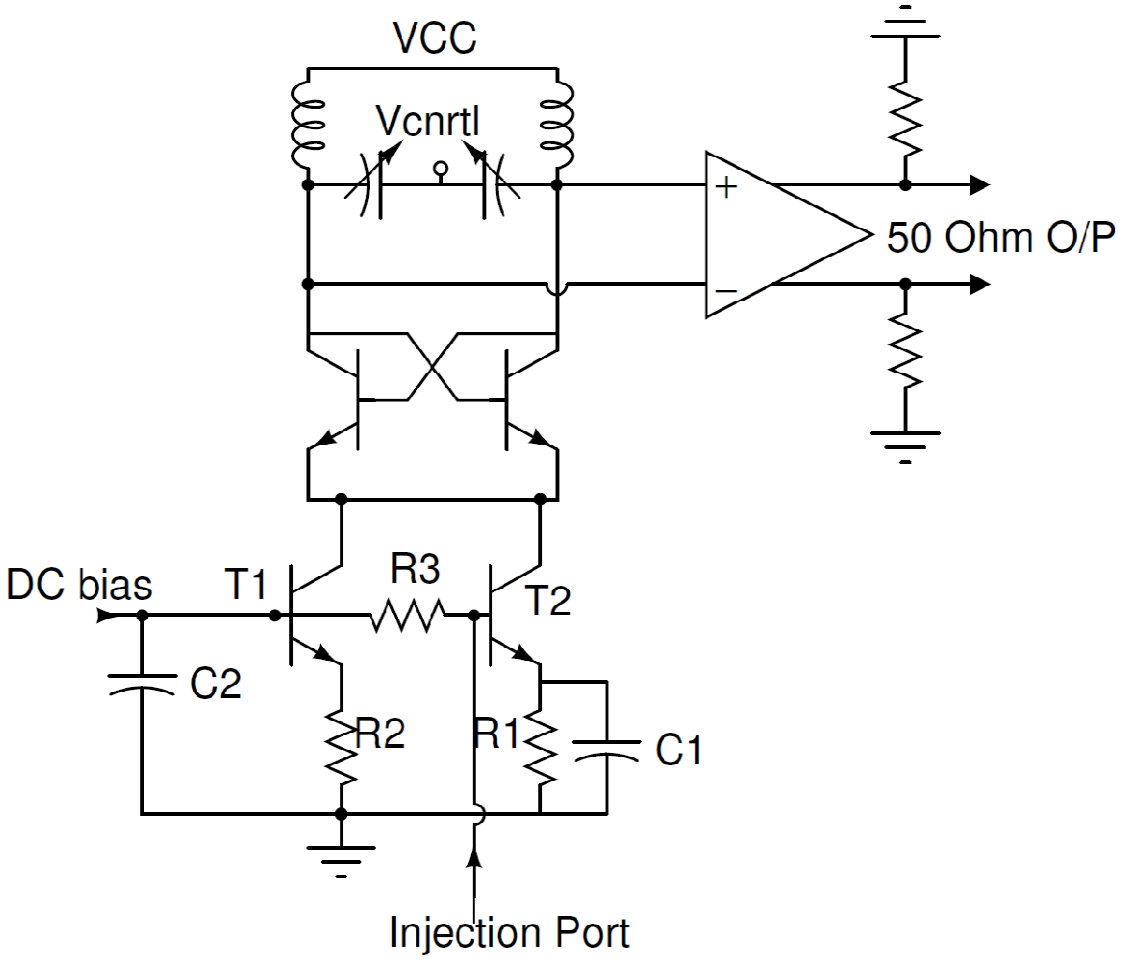


Figure 35. Injection-locked VCO

behave as a precise frequency divider for the injected signal. In this scenario, the analog differentiator using the wired-or approach is useful. High-speed clock routing is a challenge for wire-line systems as the non-deterministic delay in the clock paths lead to significant skew between the different phases at high frequencies. So, at near $f_T/4$ speeds, half-rate architectures are generally preferred. With these tradeoffs in mind, the second approach was selected to generate precise clock extraction at half the input data rate.

The circuit shown in Figure 35 has been specifically modified to suit injection locking. In traditional injection locking by the tail current injection method, the signal is directly injected into the base of the tail current source T1. The tradeoff in this case is necessitated by the degeneration resistor R2. A larger R2 improves the stability and matching of the DC current by negative feedback. At the same time a large R2 reduces the gain of the device with respect to the injected signal. This can be circumvented by connecting a capacitor in parallel with the resistor R2. The device T1 is sized according to the amount of DC current necessary for the VCO. Hence, in most cases using this device leads to larger parasitic at the injection node. Thus the injection gets limited by bandwidth, having very high gain at low frequencies and low gain at the high frequencies. Further, it was observed during simulation that this arrangement gave rise to difficulties in sustaining proper VCO amplitude. This is because whenever a large signal was injected into the device, the device was switching on and off, which led to discontinuities in the current supply to the VCO. To get rid of these tradeoffs, a separate block consisting of transistor T2, resistor R2, and the capacitor C1 is constructed. In this arrangement, the device T2 is designed to sustain only a fraction of the total tail current (less than 10%) by sizing the resistor R1 appropriately. This also sets the g_m of the device. To boost high frequency content, the resistor is bypassed using a capacitor C1. Thus this arrangement lets the RF power injected into the VCO to be set independently of the DC power leading to easier design.

4.2 ANALYSIS OF INJECTION-LOCKING

To study the effect of injected signal on the VCO, data at different rates were transmitted to the system. It was theorized that the response of the VCO to the injected signal would follow the bell shaped curve of its tank impedance. It can be seen from Figure 36 that this is indeed the case, as the peaks of the output spectrum trace out the bell shaped curve from the center frequency. Figure 35 also shows the regions of locking, pulling and out-of-lock.

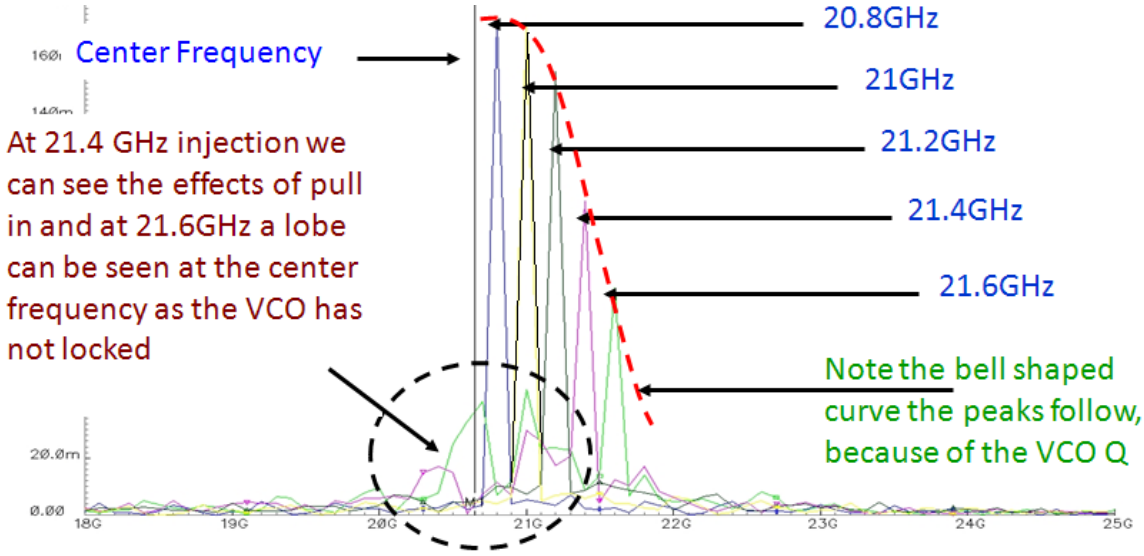


Figure 36. The output spectrum of the VCO for different frequency of injection.

The earlier discussion makes it clear that the effectiveness of injection locking is dependent on the amount of power that can be generated at the clock frequency by the harmonic generator. The harmonic generator transfer function is hence a very critical optimization parameter. Since the transformation of input PRBS to clock spectra requires non-linear operation, it is difficult to formulate an exact analytical expression. To understand the circuit tradeoffs involved, it is necessary to develop a system-level model to provide optimal values for circuit parameters such as inductor lengths and component values of the other passive elements [43]. A block diagram of the simulation model used is shown in Figure 37 (a). In this model, the pseudo-random data signal is passed through the differentiator transfer function to yield a set of alternating pulses. They are then rectified and fed to a periodogram to perform spectral analysis. The signal at the output of periodogram can be written as the following equation:

$$Z(f) = W(|X(f).H(f)|) \quad , \tag{7}$$

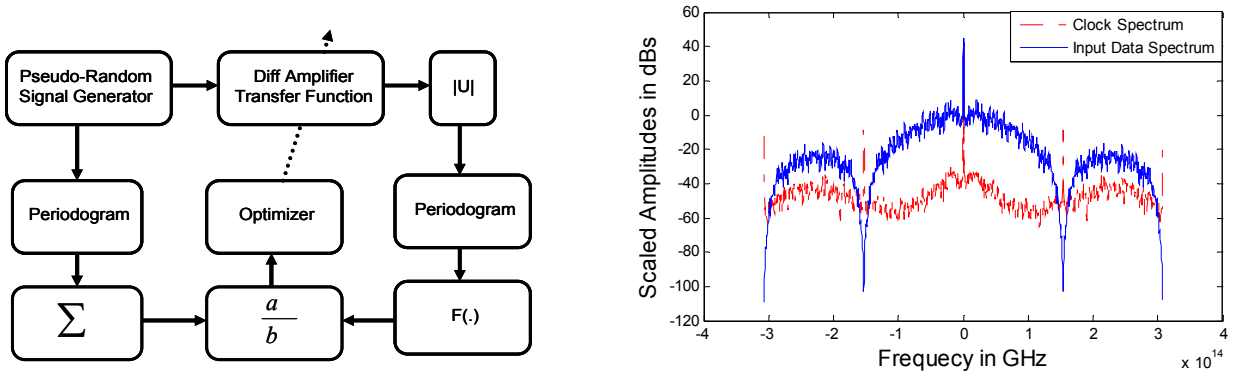
where $W(.)$ is the Kaiser window function to define and extract the finite spectral energy, $H(.)$ is the transfer function for the composite difference amplifier and second order filter, and X is the input signal spectrum. The signal Z is then acted upon by the operator F which extracts the particular index $f=f_{clk}$ from the signal. The output of the block is then used to form an optimality criterion for the CDR system. The criterion is defined by the following relations:

$$O(H) = \frac{\sum W(X(f))}{F(Z)} = \frac{P(signal)}{P(clock)}\ , \tag{8}$$

such that

$$F(Z) = Z(f)\big|_{f=f_{clk}}\ , \tag{9}$$

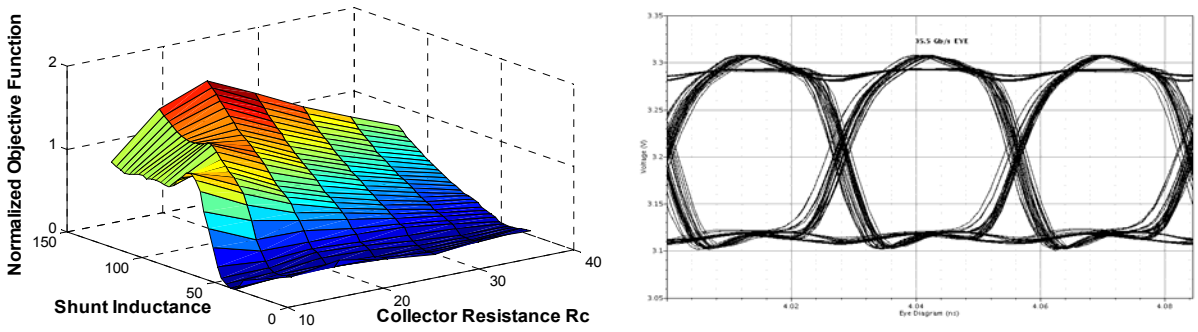
where, O is the optimality criterion based on the ratio of power in the signal and the power in the clock frequency. The limits for the windowing function $W(.)$ can be defined based upon the spectral purity requirement set by the VCO injection and phase noise response. It can be seen that the optimality criterion $O(H)$ is a function of the filter transfer function that itself is the tunable parameter for the entire system model. After defining the optimality criterion, the first task in using the system was to form the spectral line at the desired clock frequency and observe the relative power spectrum. The result of the simulation appears in Figure 37 (b), which shows the overlap of signal and clock spectra. It can be observed that the clock component contains a finite amount of power that would be optimized in the next step. An optimizer was then used to run the model in Simulink (MATLAB) with several component values of the differentiator. The results are plotted in Figure 38 (a) and it demonstrates the optimum component values of the differentiator with regard to the cost function described by Equation 8.



(a) (b)

Figure 37. a) The block diagram of simulation model b) Spectrum of input data and recovered clock

To validate the approach, a 71 Gb/s, half-rate circuit was designed in a 150 GHz f_T commercial SiGe process. The VCO is designed to have a center frequency around 35 GHz. Data at 71 Gb/s was passed through the harmonic generator to generate power at 71 GHz by differentiation and rectification. The signal was then fed into the VCO using tail current injection. The VCO locks onto the signal and the output frequency of the VCO is half of the injected signal which is 35.5 GHz. The output of the VCO can now be used as a half-rate clock. This clock is used to sample the data in the flip-flop (which acts like one of the channels of a 1:2 de-multiplexer). The output of this flip-flop is exactly at half the input data rate, at 35.5 Gb/s. Figure 38 (b) shows an opening in the eye diagram of about 200mV$_{P-P}$ single-ended (400mV differential). It can also be observed that the data rate is now exactly 35.5 Gb/s. This demonstrates that the clock and data are correctly synchronized or otherwise the bit period at the output would have varied and produced a closed eye.



(a) (b)

Figure 38. a) Optimality plot of the harmonic generator b) Clear eye-diagram of the de-multiplexed data at 35.5 Gb/s

Measurement results:

The chip micrograph is shown in Figure 39. To validate the concept of lock, the input frequency to the chip was swept while keeping the power fixed at -18 dBm. The resulting output power is shown in Figure 40. It can be clearly seen that the output power traces roughly a bell shaped curve when the frequency is swept. This validates the injection locking principle and also provides a measure of the locking range of the system.

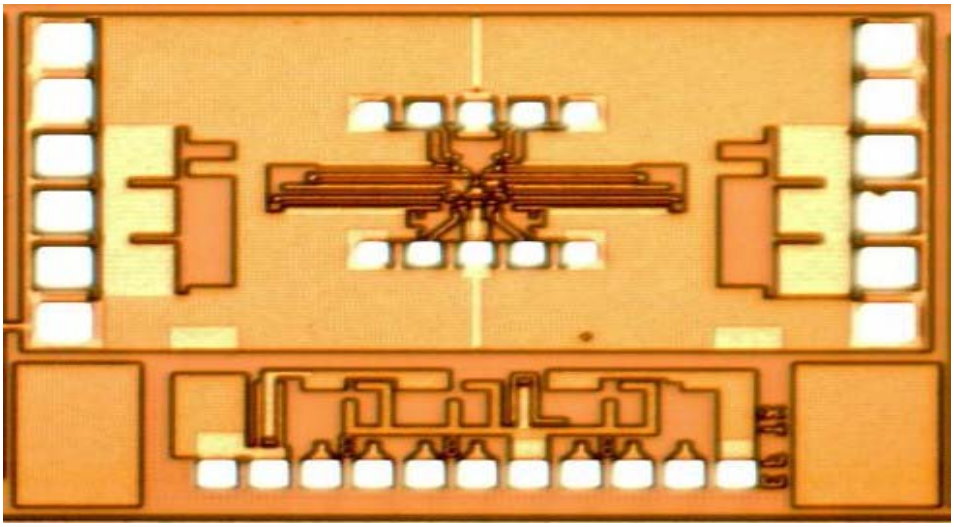


Figure 39. The chip photograph of the injection-locked system

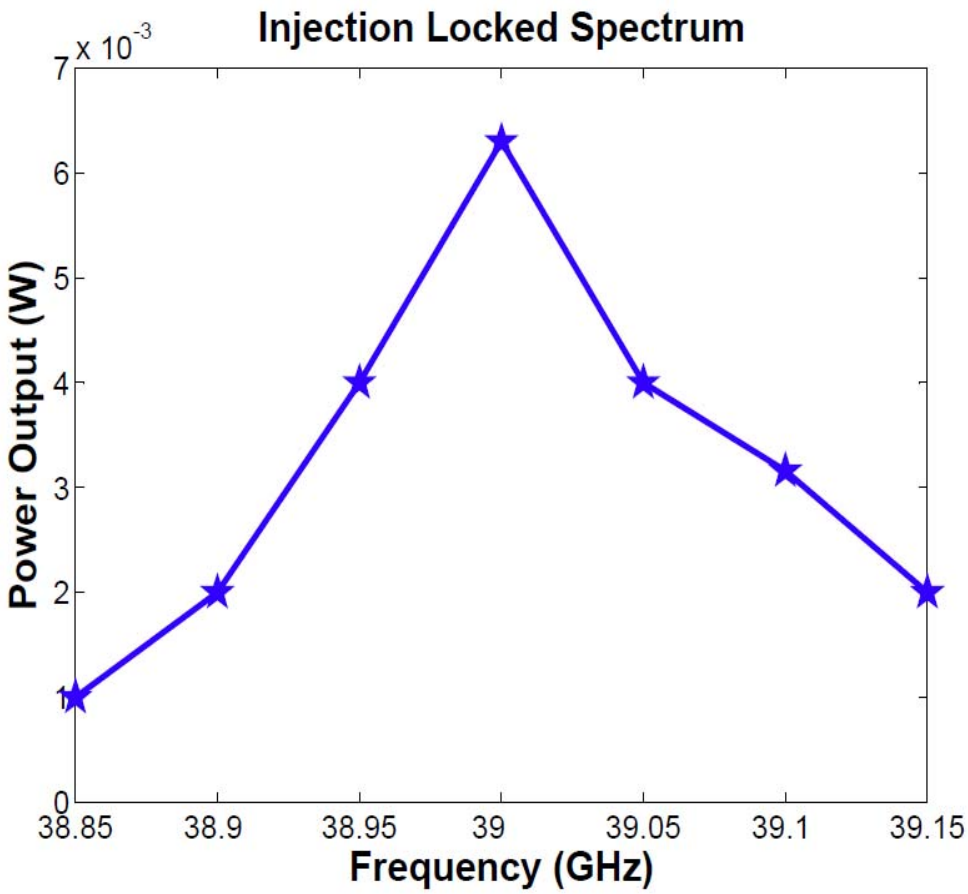


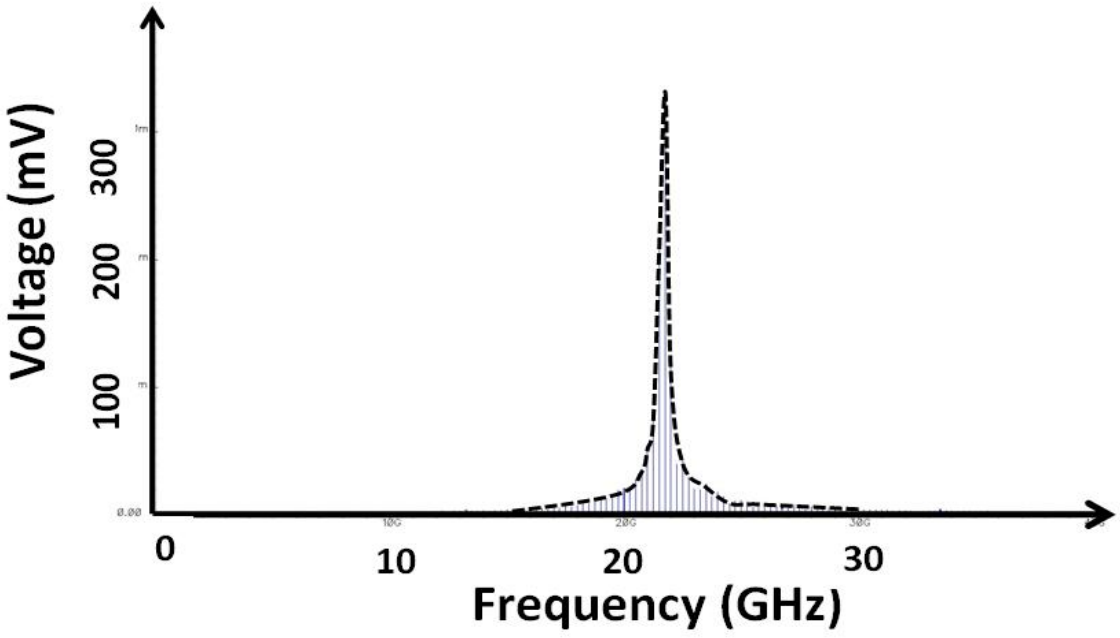
Figure 40. The measured output power when the input frequency is swept while keeping the input power constant at -18 dBm.

Effect of jitter on Injection-Locking

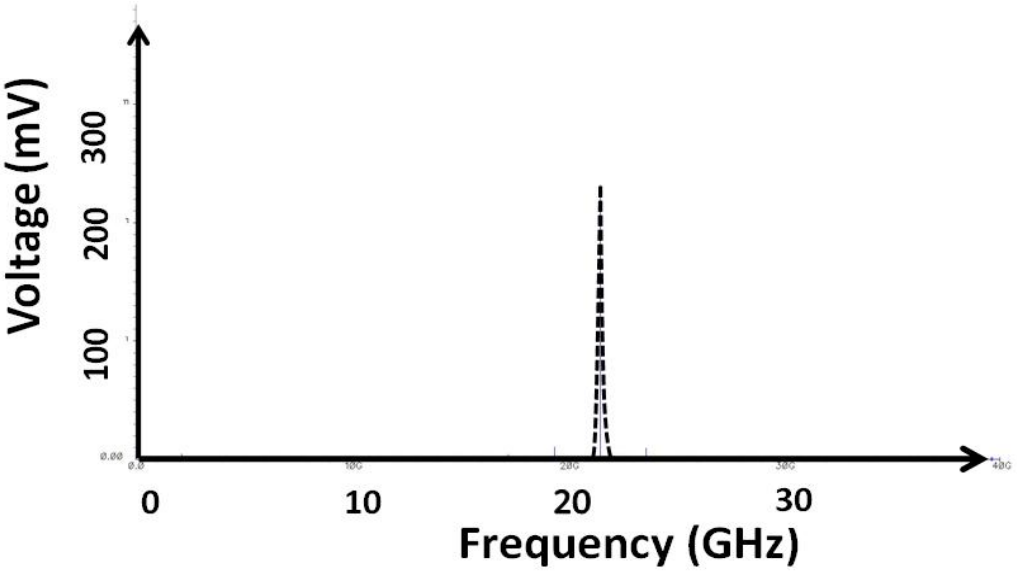
By the above demonstrations, injection locking appears to be a viable alternative to closed loop PLL designs, however, there were some important caveats discovered during the course of research. One of the most important specifications of a CDR is its response to signal jitter. To study the effect of signal jitter on the injection locked system, signal jitter with 0.6 unit interval (UI) duration and 300MHz frequency offset was injected into a VCO with 21.75 GHz center frequency. When a clean 21.5 Gb/s data stream was injected into the system, the VCO locked perfectly onto the signal. Thereafter a 21.3 Gb/s signal with 0.6 UI signal jitter at 300

MHz offset was injected into the oscillator. This time the VCO locked onto 21.6 GHz. The possible explanation of this phenomenon is that the injected signal has powerful side-bands at 21.6 GHz (21.3+0.3) and 21 GHz (21.3-0.3) due to the presence of signal jitter at 300MHz offset. The band at 21.6 GHz has more power under the bell curve of the VCO than the actual data rate at 21.3 Gb/s. Hence, the VCO incorrectly locks to 21.6 GHz.

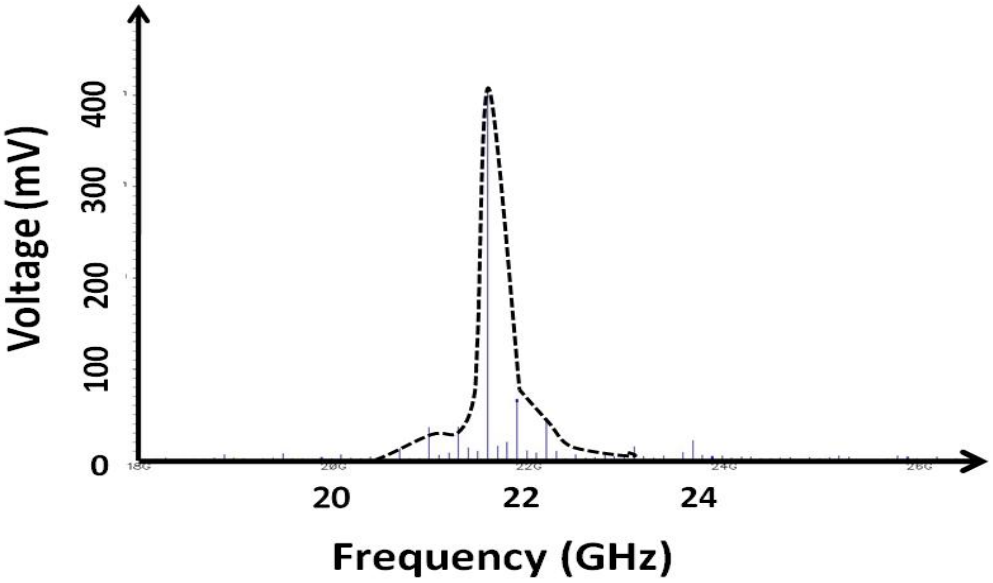
Figure 41 (a) shows the Discrete Fourier Transform (DFT) of the VCO output. The bell curve can be seen centered about 21.75 GHz. The Figure 41 (b) shows the result of the injection of a clean 21.5 Gb/s data stream. As explained earlier, the VCO is prone to lock to a jitter side-band if the relative power in the side-band is greater than the fundamental frequency. This phenomenon is illustrated in Figure 41 (c).



a) Spectrum of the VCO free-running at 21.75 GHz



(b) VCO spectrum when a clean 21.5 Gb/s data stream is injected



(c) Injection of 21.3 Gb/s data with 0.6 UI, 300MHz signal jitter. The VCO locks to 21.6 GHz

Figure 41. a) Spectrum of the VCO free-running at 21.75 GHz (b) VCO spectrum when a clean 21.5 Gb/s data stream is injected (c) Injection of 21.3 Gb/s data with 0.6 UI, 300MHz signal jitter. The VCO locks to 21.6 GHz.

From the result it is clear that the VCO fails to recognize the fundamental component of the data from far-out components of signal jitter. A VCO essentially acts like an adaptable filter, but its resolution is limited to the bell curve. Hence, the injection-locking method cannot be recommended for use in a stand-alone CDR, especially in applications where stringent signal jitter specifications need to be met. However, injection-locking may be used in passive-optical-networks (PON), where signal jitter requirements are low. It also may be utilized as an acquisition aid to improve conventional CDR performance.

CHAPTER 5

FALSE LOCKING OF CDRS

The phenomenon of false locking is a common occurrence in commercially available CDRs. The primary reason is the use of digital logic based rotational phase-frequency detectors (PFDs). A rotational PFD utilizes the relative motion of the data and the VCO output frequency to determine the correct polarity of charge pump current. The digital PFDs have very limited sampling windows, which leads to the PFDs showing pattern dependency [44]. It would seem ideal to replace the digital PFDs by their analog counterparts, as the analog implementation does not suffer from sampling limitations. Unfortunately, analog blocks cannot differentiate between the true clock spectrum and that caused by the superposition of noise and signal jitter.

It has been found that repetitive data patterns, like a K28.5 pattern, force the PLL to an inflection point away from the true minima of the loop. Once the loop enters a point of inflection, the average output of the charge pump is zero. Hence the PLL "false locks" and cannot move toward the correct frequency. An attempt was made at robust lock detection in [45], but it was not geared to catch false-locks, only whether the CDR has acquired lock or not under normal cases. Furthermore, the solution was not really practical as it needed perfect alignment of data and clock.

The Pottbacker PFD is the most common commercially implemented rotational PFD [46]. Therefore, the Pottbacker PFD was chosen to study the phenomenon of false lock.

As a test case, a CDR that used the Pottbacker PFD, was locked under the K28.5 pattern. As shown in Figure 42, the CDR false locked to 19/20 times the data rate. The output of the CDR toggles between two distinct states generating the point of inflection.

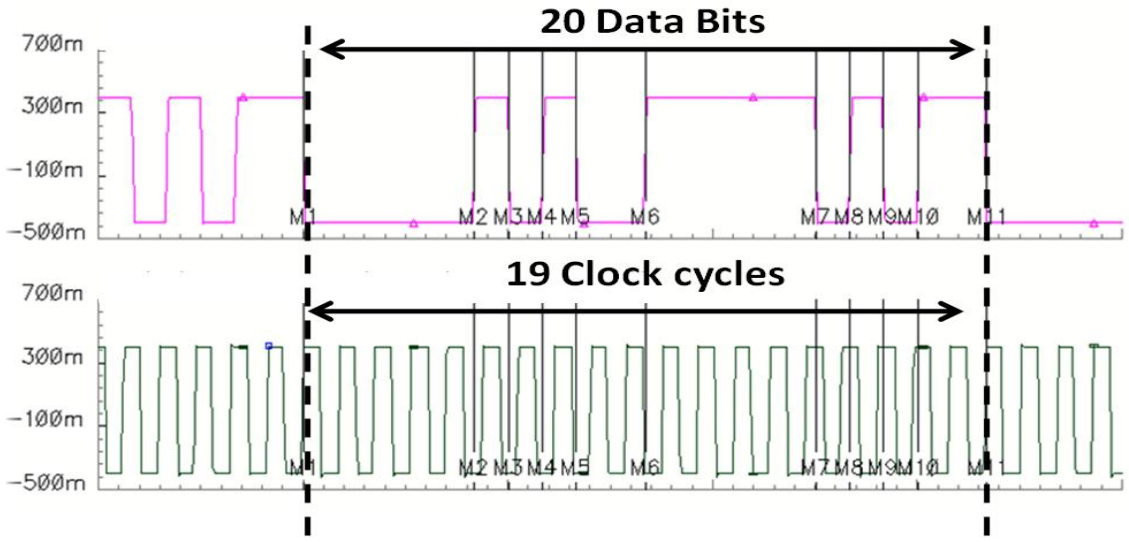
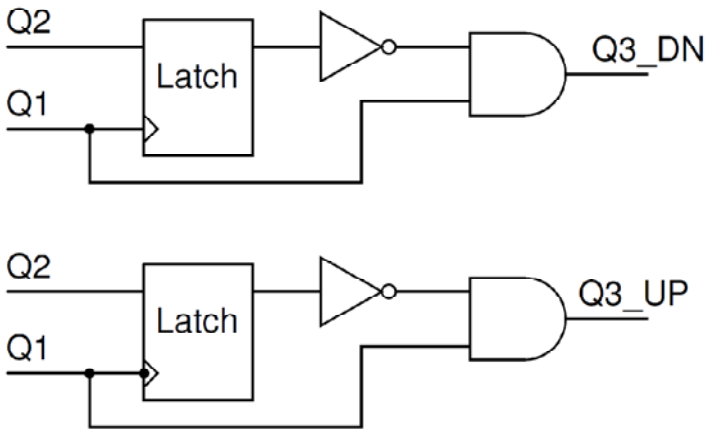


Figure 42. Clock and data pattern for a CDR in false lock with K28.5 pattern

(courtesy: Mr. Arlo Aude, National Semiconductor Corporation)

5.1 STUDY AND ANALYSIS OF FALSE-LOCKING



Q1= Output of I phase detector

Q2= Output of Q phase detector

Q3= Output of Frequency detector

Figure 43. Schematic diagram of the Pottbacker FD

The Pottbacker PFD, which was referred to earlier, utilizes the data edges to sample the clock. The diagram of the Pottbacker FD is shown in Figure 43. In the case of a full-rate PFD, two clock phases at quadrature, called I and Q phases, are required. When the data samples the clock only four different outputs are possible, as shown in Figure 44.

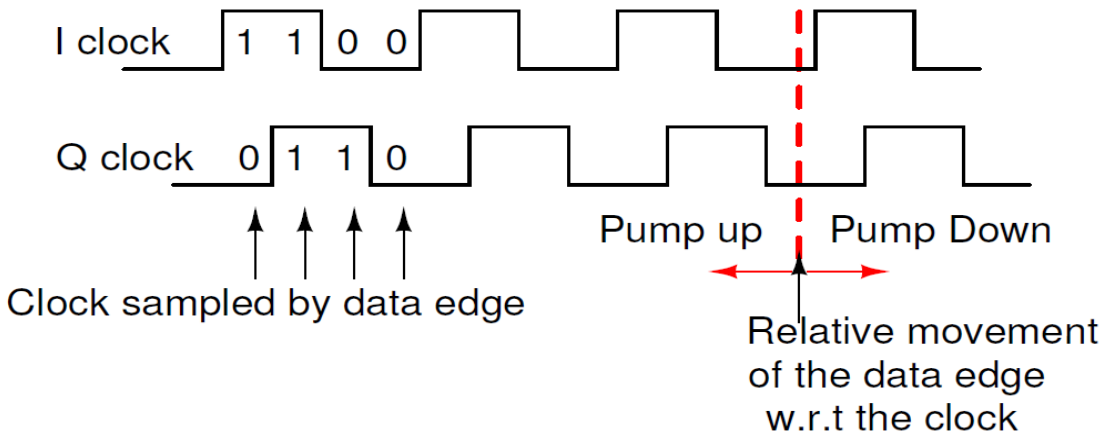


Figure 44. Quadrant generation by the data sampling the clock

Let the result of sampling be denoted by (I,Q). The set (I,Q) therefore consists of (0,0), (1,0), (1,1) and (0,1). The working of a PFD can be better visualized from a signal space mapping shown in Figure 45 (a). If there is a difference in frequency between the data and the clock, then there is a sequential movement in the output of the PFD, i.e. either "00->10->11->01->00," or " 00->01->11->10->00". Such a movement can be mapped to either clockwise or counter-clockwise movement in the signal space. This movement can be decoded to give the correct polarity of the frequency difference. The Pottbacker PFD tries to decode the movement across only one phase boundary. This is done to enable "tri-state" logic functionality. The Pottbacker PFD decodes the (0, 0) to (1, 0) movement as the negative polarity (Down), and the (1, 0) to (0, 0) as the positive polarity (UP) as shown in Figure 45 (b).

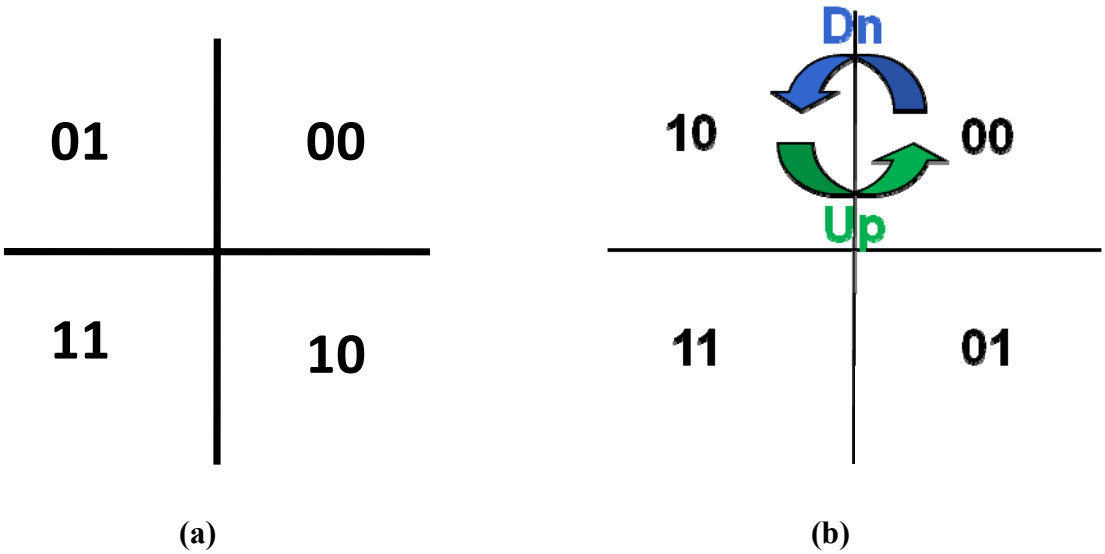


Figure 45. a) The signal-space mapping of a Pottbacker PFD b) Decode sequence of a Pottbacker PFD.

It can be discerned that there are only four distinct quadrants in the signal space, as shown earlier in Figure 45 (a). If the incoming data is assumed to be pseudo-random, there can be long strings of "zeros" or "ones" in the data stream. In this case, if the frequency of data and clock are different, then there are a significant number of cases where the output of the PFD jumps two quadrants, as illustrated in Figure 46 (a).

There are only four distinct states; for any signal jump which spans two states, the resulting direction of rotation in the signal space cannot be determined. This was discovered to be a primary cause of false lock. Since in any two-quadrant jump, both the I and the Q output suffer inversion, an easy solution to prevent any action in this case would be to perform exclusive-or gating on the individual phases I and Q. Unfortunately, it was later discovered that cases of three-quadrant jumps also lead to the same problem, as discussed in the next paragraph. This solution was therefore discarded.

In case of a three-quadrant jump, caused by missing transitions, followed by a correct single-quadrant movement, the output of the PFD is then either an UP followed by a Down or vice-versa. In either case, the average output is zero. This case is illustrated in Figure 46 (b). Even though there is a frequency difference between the clock and the data, the PFD fails to respond correctly.

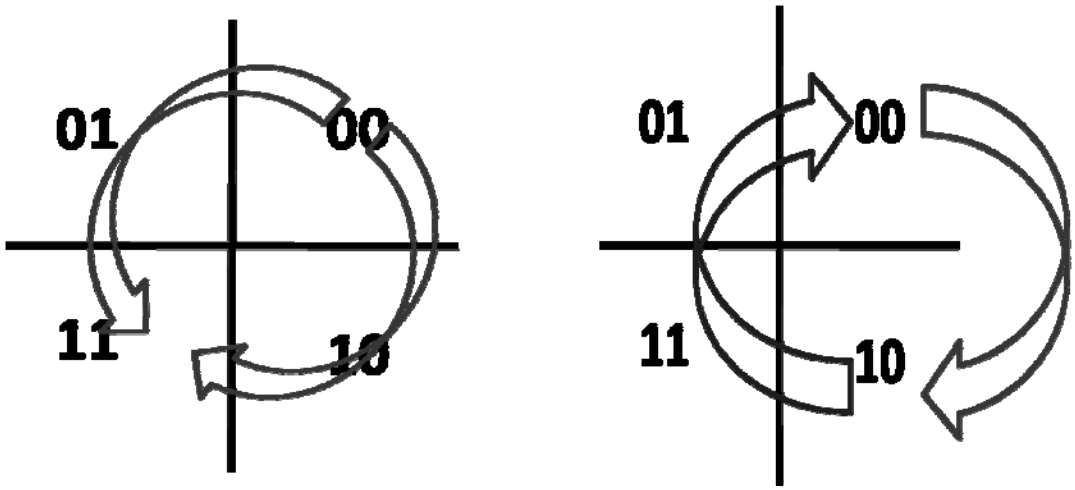


Figure 46. a) Two-quadrant jump b) Three-quadrant jump.

A detailed study of the Pottbacker PFD, that is being used a test case to check false locks, has revealed some interesting facts about its operation, some of which were possibly unintended. The truth-table of the Pottbacker PFD is presented in Table 3**.** In the table, the subscript (n-1) denotes the previous state and the subscript (n) denotes the following state. It can be observed from the table that the transitions which have been high-lighted give rise to a "hold" state in one of the outputs and 0 in the other output. This leads to an ambiguous output. As such, if "hold" is zero in these states, then the systems' output is a "tri-state" even though there might be a phase-frequency discrepancy. This was initially targeted as an area to approach to mitigate false locking in CDRs. The most important approach is still to try and detect false locks from a higher level of abstraction from which a solution will be universally applicable. The proposed false lock detector would be designed to operate up to a data rate of 12.5 Gb/s. This would enable it to be tested with an existing 12.5 Gb/s CDR.

Table 3-Transition states of a Pottbacker PFD.

$I_{(n-1)}$	$Q_{(n-1)}$	I_n	Q_n	Up	Down
0	0	1	0	0	1
1	0	0	0	1	0
0	0	1	1	0	1
1	1	0	0	0	0
0	1	1	1	0	0
1	1	0	1	0	0
1	1	1	0	0	Hold
1	0	1	1	0	Hold
1	0	0	1	1	0
0	1	1	0	0	0
0	0	0	1	Hold	0
0	1	0	0	Hold	0

The study of false-lock raises an important question about trying to mitigate false-locks at the circuit levels itself. It was noticed that the K28.5 pattern generates a unique pump up/pump down pattern that leads to a sum zero charge pump current. This leads us to predict that mitigating the logic conditions that create this for K28.5 might lead to some other pattern creating a false-lock. Thus to avoid these complications, a system-level approach is preferable. The suggested approach would involve a simple yet robust detection scheme combined with a CDR control algorithm to correctly move the CDR out of false-lock.

5.2 PRESENT DETECTORS AND REQUIREMENTS OF THE SOLUTION

In a typical commercial CDR, the VCOs have multiple coarse and fine tune settings to achieve both the correct frequency as well as a large acquisition range. The CDR control algorithm generally controls the switched-capacitor banks which determine the coarse tune settings whereas the fine tune settings are adjusted by the PLL. This is done by analog control of the voltage input to the varactor bank. The charge pump actually either adds or subtracts charge from a capacitive filter to control this analog voltage. The CDR control algorithm sets a certain switched-capacitor setting and then allows the PLL to adjust the correct varactor voltage. To understand how a typical CDR control algorithm works, we assume that the data rate is higher than the starting frequency of the CDR. Furthermore, let us assume that the CDR control algorithm sets the default frequency to the lowest possible value by turning all the capacitors in the tank on. We also assume that the difference in frequency is higher than the fine tune range that can be adjusted by the varactor. In this scenario, the charge pump would continue to pump the voltage up at the varactor node till it is limited by the supply voltage. To detect this, a comparator is generally placed at the varactor control node. The comparator would trip as the voltage is nearing the supply voltage. The CDR control algorithm can thus detect that the

capacitor setting is inadequate and thus switch off some capacitors in the VCO tank (depending on the search algorithm preferred).

If a suitable detector can be designed then the CDR controller can be used to change the capacitor setting to force the VCO frequency to move near to the true lock condition. A suitable implementation in this case would be if we implement a linear search algorithm starting from the lowest possible VCO frequency. Thus, if the false-lock detector detects a false lock, the CDR controller switches the capacitor setting to the next one, which is suitable for a higher frequency. This process would continue till the false-lock frequency becomes out of the fine tune range of the CDR. Thereafter the CDR would move naturally to the correct lock condition.

We have considered various approaches to detect false-lock. One of the methods studied was the edge counting method shown in Figure 47. The edge counting method is widely implemented in commercial CDRs due to its simple design and implementation. The principle of working for the edge counting method is the assumption that for true locking of the CDR, the number of edges in the raw data will equal the number of edges in the retimed data. This is generally true as in the case that the CDR false-locks or is out of lock, the number of edges in the retimed data would be lower (though if the clock frequency, which is re-sampling the data, is significantly higher, then this assumption might not be true). To avoid the case where the clock is significantly faster than the data, the CDR is generally started from the lowest possible frequency by default.

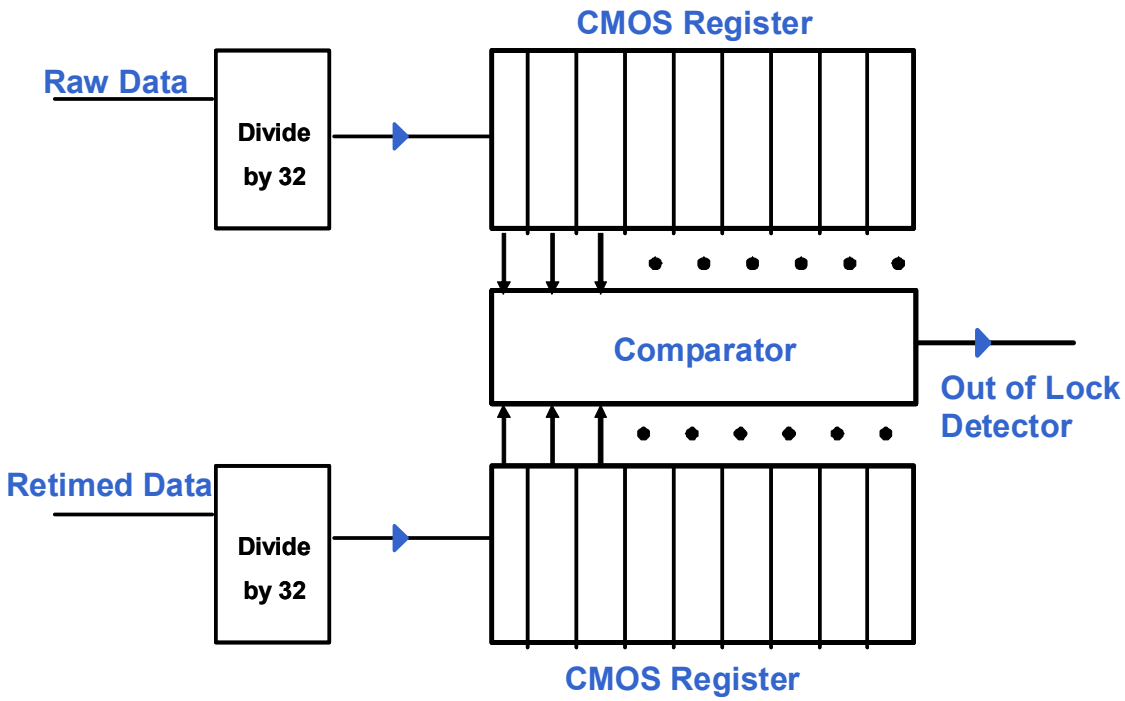


Figure 47. Schematic of the edge counting method of lock detection.

There are two principal drawbacks of this system. First, is the large counter memory required to implement this system. The accuracy of the system is directly proportional to the number of edges that can be stored and compared. Typically, a 32 bit counter is implemented for both the raw and re-timed edges. As a consequence, if the CDR is false-locked or out of lock by less than 1/32 times the data frequency, then the system cannot detect it. This granularity of error can be reduced by implementing larger counters, but at the cost of increasing the die area. Second, the counters are implemented in CMOS to save power consumption and die area. In a SiGe process the BJTs are much faster than CMOS and to implement the counter in CMOS, the data rate must be divided down to a rate compatible with the speed of the CMOS cells in the process. In the SiGe process from National Semiconductor we chose to use, the BJTs have a peak f_T of 100 GHz and the MOSFETs have a peak f_T of 50 GHz. In reality, to save power, the MOSFETs are not used in a CML architecture, but as switches to implement digital logic. So the actual peak speed of the digital counters are nearly 32 times slower than the BJTs. Therefore, the

data edges have to be divided down by 32 before the counters can be implemented. The use of the extra dividers increases the power consumption of this implementation. Moreover, it was found that existing commercial CDRs with this system failed to detect the false-lock caused by repetitive patterns like the K28.5.

Before we discuss the proposed solution, it is also necessary to define the target specifications/operating parameters of any such false-lock detection system. Commercial CDRs need to have a jitter tolerance of at least 0.6 unit interval (UI). Thus, any detection system also needs to have a jitter tolerance of 0.6 UI. It should be able to have this tolerance over process, voltage and temperature variation (PVT). In our case we define the process corners as the BJTs being slow or fast. The voltage variation to be tolerated is defined to be 2.25-2.75 V. The operating range of temperature that is being targeted is the commercial range from -10^{o} C to -85^{o} C ambient. The thermal characteristic of the package (LLP40) is going to be superimposed on this requirement. The system should not only be able to catch false-locks under jitter, but more importantly not show the output as false-lock when the CDR is in true lock, even in the presence of large jitter. It should also be simple to implement and have small area and low power consumption than the brute force edge counting approach outline earlier.

5.3 PROPOSED LOCK DETECTOR

To overcome the problems stated above, a completely new approach is being proposed. If the CDR is in true lock, then the raw data and the re-timed data should be exactly same except for a phase shift between them. In general, CDRs are designed so that the re-timing clock edge falls exactly in the middle of the raw data bit. This gives the system the maximum possible margin before failure to re-time the bit. We can in, in other words, say that the clock edges are generally 0.5 UI away from the data defining points. Thus, in true lock, the raw and re-timed data streams should look exactly the same, except for the re-timed stream being 0.5 UI shifted

from the raw data stream. This feature is the basis of our solution. The relative position of the edges is shown in Figure 48.

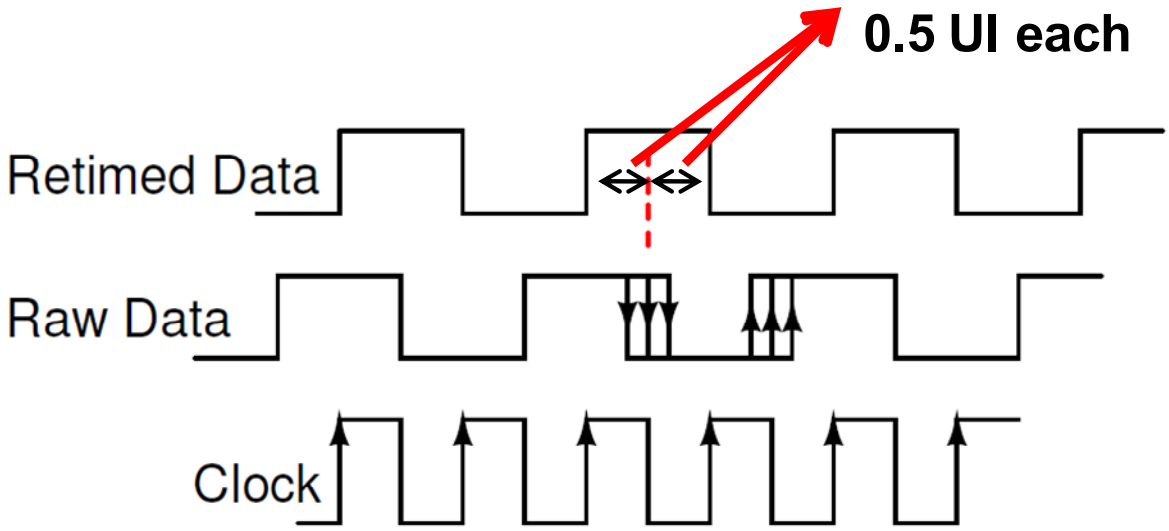


Figure 48. Relative position of raw and re-timed data.

Assuming the facts discussed above, the raw and the re-timed data should have an auto-correlation factor of 1. A system level diagram of a normal reference-less CDR is shown in Figure 49.

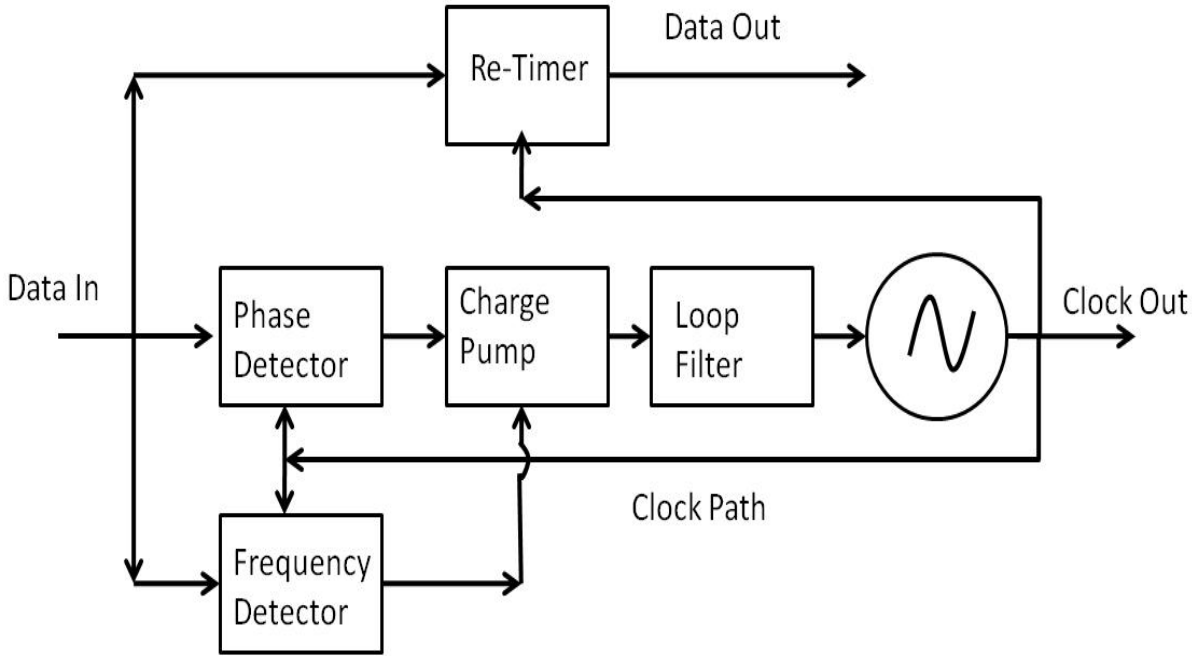


Figure 49. System-level diagram of a traditional CDR.

The proposed system level solution is shown in Figure 50. It can be observed that this block can be used as a simple add on to an existing CDR.

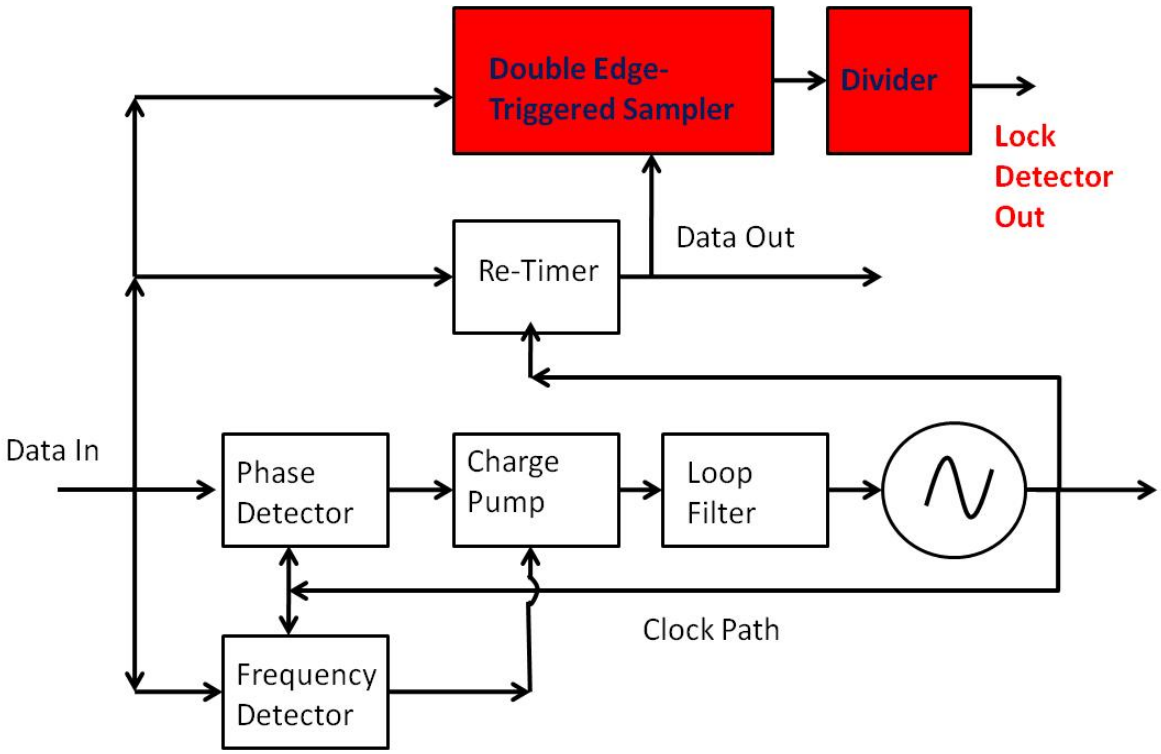


Figure 50. System-level diagram of the proposed solution.

In this proposed solution the re-timed data is sampled by both the rising and the falling edge of the raw data. As can be seen from Figure 48, the rising edge of the data should always sample zero and the falling edge should always sample one. In case the CDR is out of lock the re-timed data is likely to miss some bits. In that case, is a bit zero the raw data would sample a zero instead of a one if a bit one is missed. Thus the output of the sampling system would start to toggle, denoting that the CDR is out of lock. This system is inherently robust and jitter tolerant. As shown in the Figure 46 earlier, the raw edges are in the worst case 0.5 UI away from the re-timed edges. Jitter tolerance can be broken up by the relative frequency of the jitter. The jitter that is within the PLL bandwidth is called close-in jitter and cannot be filtered by the PLL. The jitter that is beyond the PLL bandwidth is attenuated by the PLL filter function and is called far-

out jitter. Since the PLL cannot filter out the close-in jitter, the clock that is recovered by the PLL has the same jitter as the input data. Thus the raw data and the re-timed data have no relative jitter. In this case the proposed lock detector has an infinite theoretical jitter tolerance. Whereas in the far-out jitter case, the system will have a theoretical jitter tolerance of 1 UI, as the raw edge is 0.5 UI away from both the rising and falling edges of the re-timed data. This is the maximum jitter tolerance achievable theoretically for any re-timing system. In reality, the tolerance is limited by the non-zero set-up time and hold-time of the re-timing flip-flops. The schematic diagram if the proposed system is shown in Figure 51.

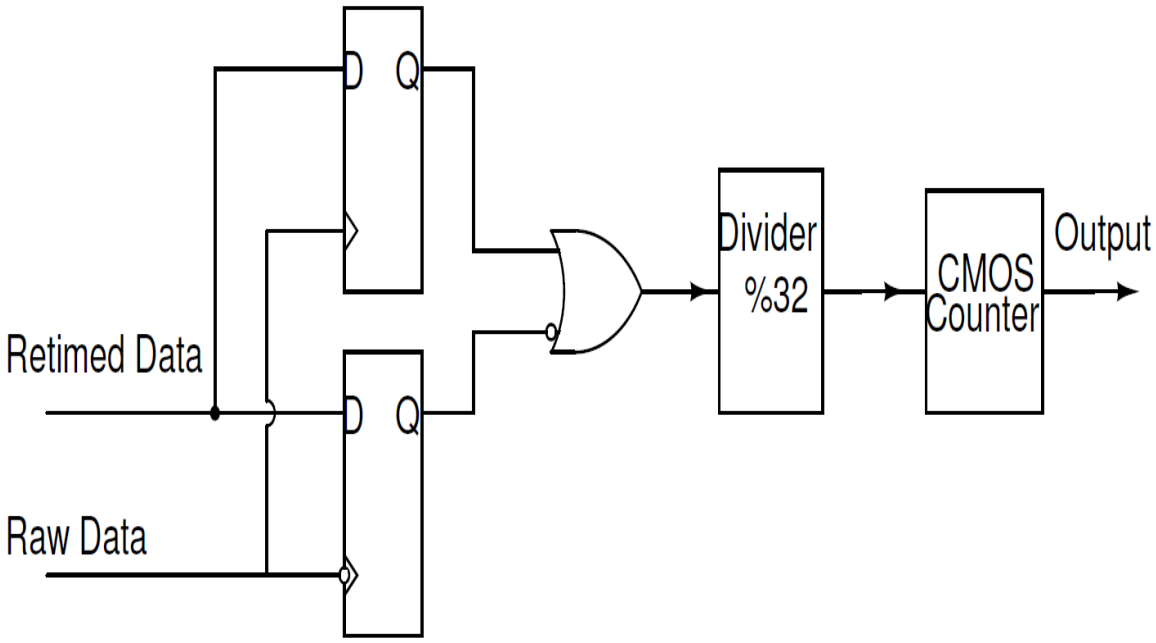


Figure 51. Schematic diagram of the proposed solution.

5.4 MEASUREMENT RESULTS

To validate the method, the system was first implemented by verlogA blocks. The verilogA language allows for implementing latches which are much closer to the actual latches than simply using verilog blocks. This helps us in understanding the robustness of the system before spending time in implementing it in silicon. The complete CDR was implemented in verilogA, including the Pottbacker PFD, to study the effects of false-lock and jitter. When a K28.5 pattern in given as input to the system, the CDR false-locked to a frequency 19/20 times the actual data rate. In this position, the edges of some of the bits were found to be exactly aligned to the clock. If the setup time of the latches were not violated, in some cases, there were no missing edges. Thus under these cases the system would be unable to catch the false-lock if the FD was kept on. This is because it is the FD which maintains the relationship between the edges in case the CDR is false-locked. The PD gives a DC zero because there is a difference in frequency. Therefore, the best solution is to turn the FD off once the lock has been achieved. The PD should be kept on to take care of small frequency and phase drifts in the PLL.

In the case of the verilogA simulation, the sharp edges created by the verilogA model lead to a slight jitter in the PLL which made the false-lock detector catch the false-lock locks even without turning the FD off. When the complete system was simulated with a K28.5, pattern the output of the lock detector started toggling (as discussed above) and hence could catch this false-lock case, as shown in Figure 52.

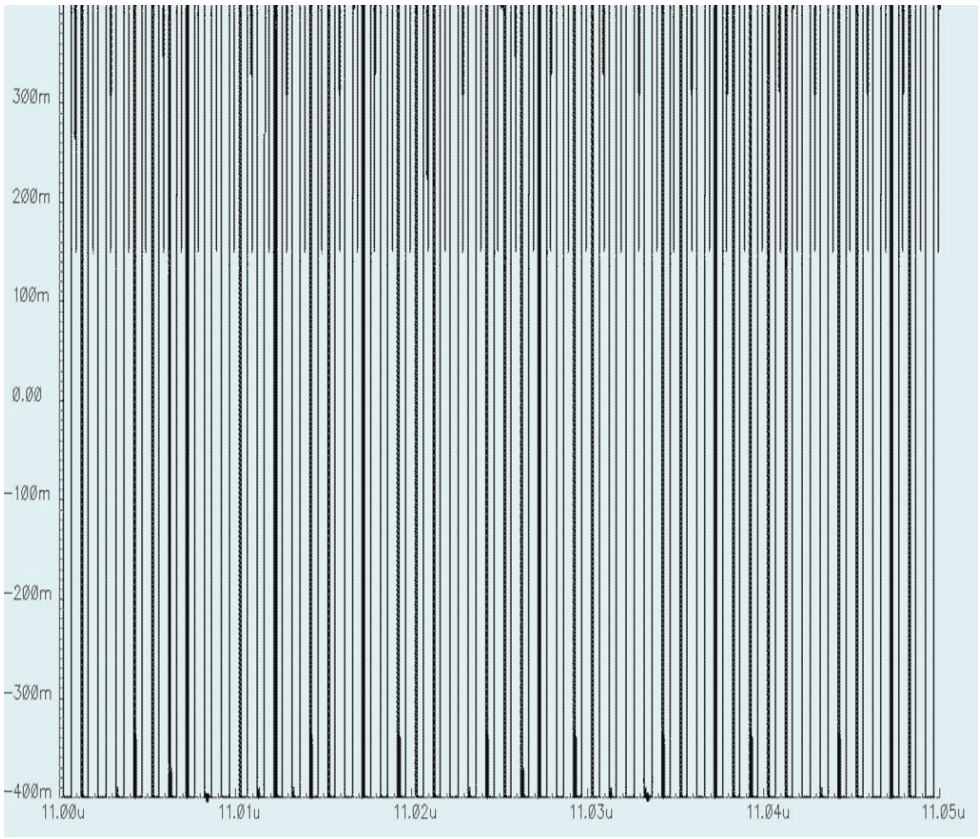


Figure 52. VerilogA simulation result of the detector when K28.5 pattern is used to false-lock the CDR.

As has been mentioned earlier, the system would have no practical value if the system could catch false-locks, but erroneously showed a toggle pattern under high jitter in true-lock. This is the fundamental criterion that the system has to meet. The simulation result of the system, under true lock and in the presence of 300 MHz, 0.6 UI sinusoidal jitter is shown in the Figure 53. As can be seen from the figure, there is no toggle, thus proving its robustness.

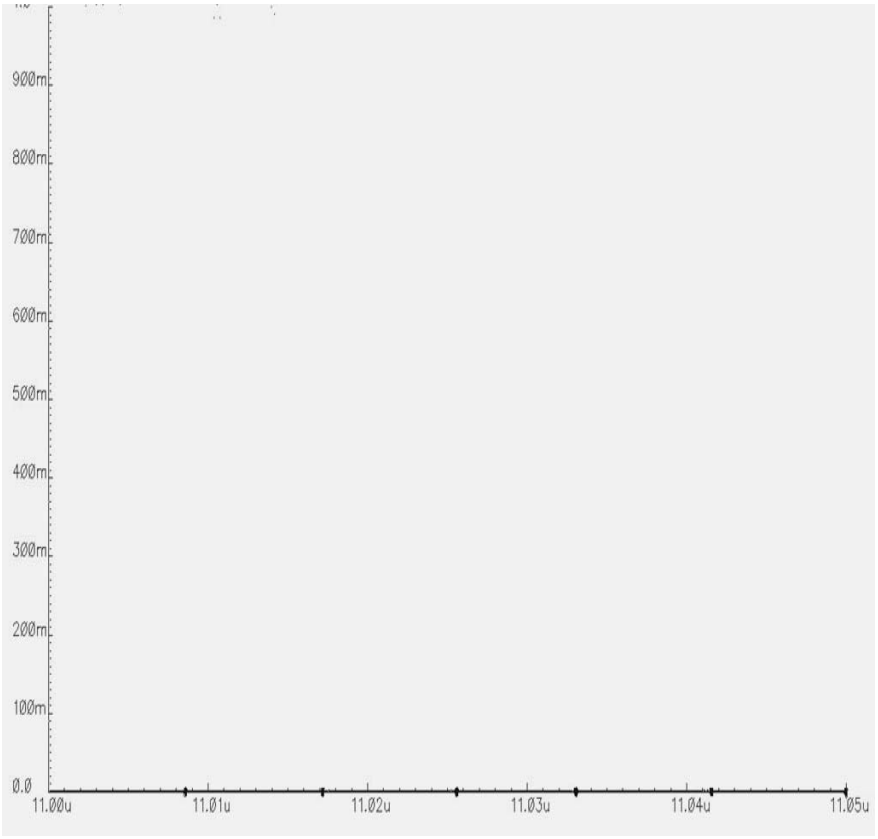


Figure 53. VerilogA simulation result of the detector in the presence of jitter, when the CDR true locks

The circuit was designed and fabricated in a 100 GHz SiGe HBT process from National Semiconductor. An existing 12.5 Gb/s CDR was chosen as the platform to test the system out. The CDR was tested under various known conditions of false lock, to check the functionality of the false-lock detector. Another test comprising the check of the output of the false-lock detector versus the bit error rate tester (BERT) output was done. As the false lock detector should not give an "out-of-lock" signal if the CDR is in lock, even under high input signal jitter conditions, this test was useful in comparing the functionality of the on-chip false-lock detector versus the external BERT. A LLP-40 package from National Semiconductor Corporation was used to package the chips. Even though packaging introduces significant parasitic elements which degrade the performance of a chip, yet for practical applications packaging is necessary. The

12.5 Gb/s board is shown in Figure 54, followed by the snapshot of the measurement setup in Figure 55.

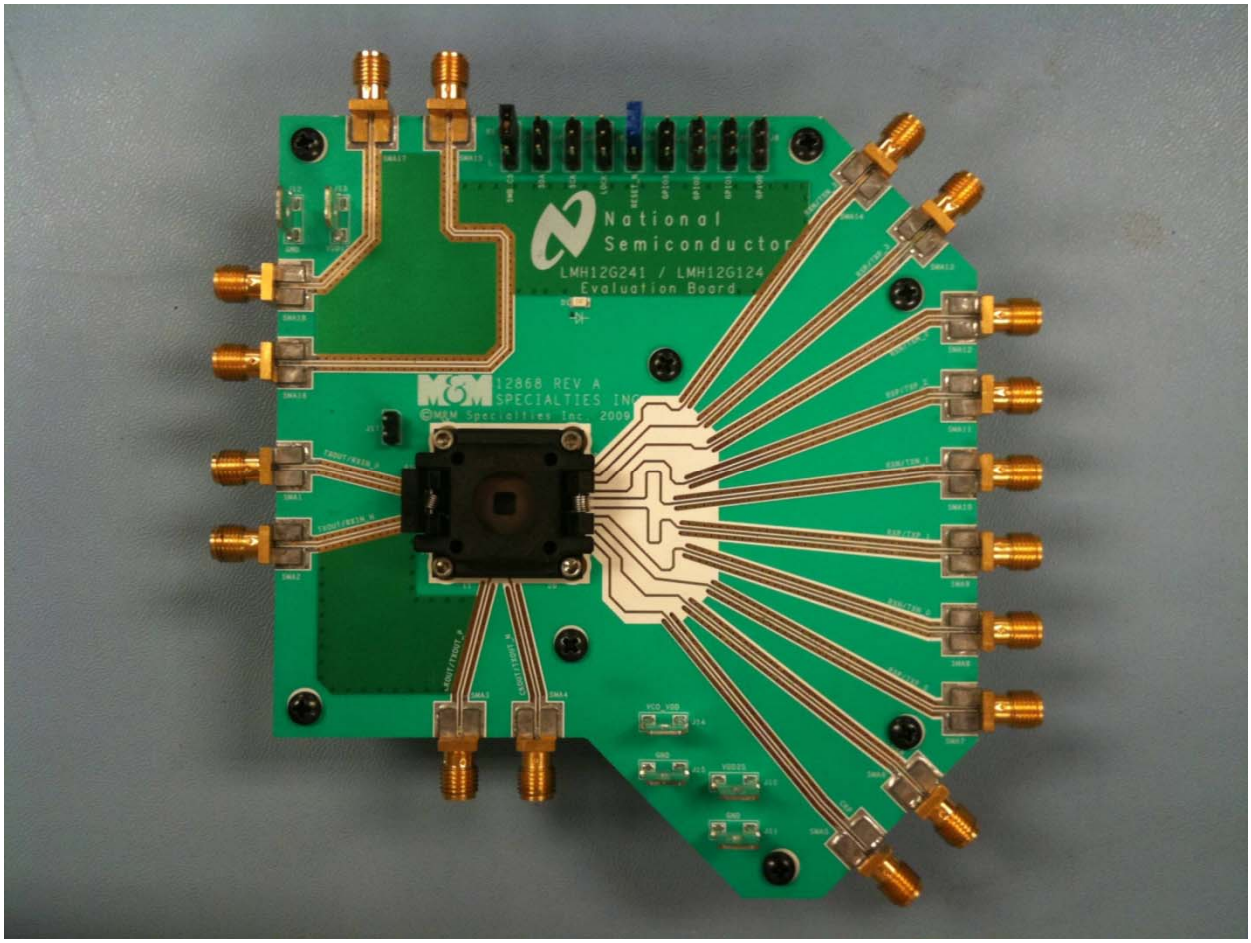


Figure 54. The LMH12G241 board along with the socket (used to test different chips without soldering).

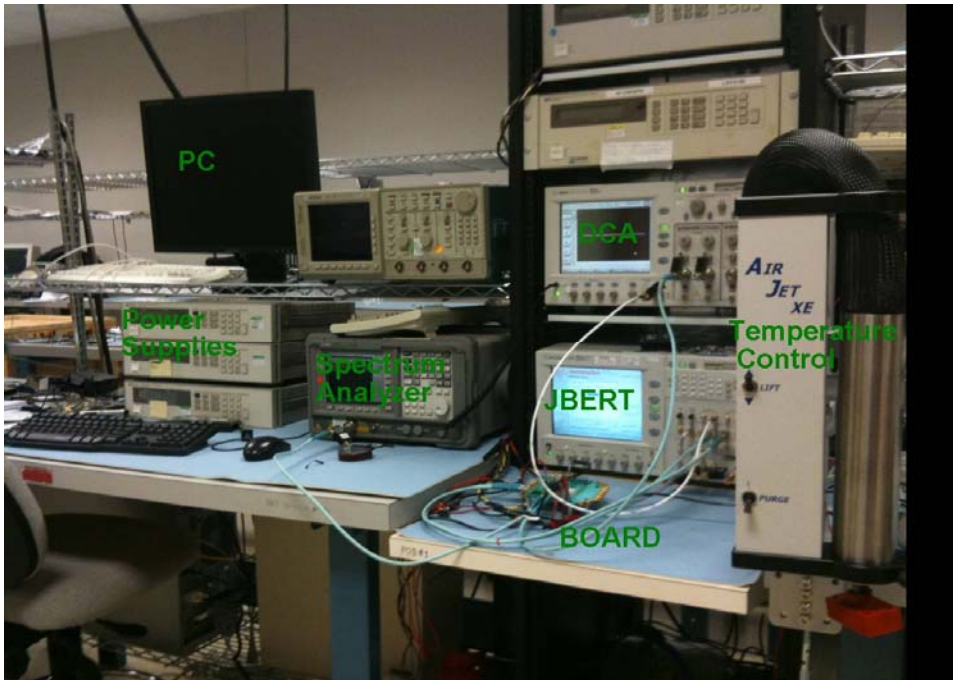


Figure 55. Measurement setup containing the board, the DCA, the spectrum analyzers and the temperature control unit.

The chip was measured for false-lock at 6.25 Gb/s as the system did not false lock for some of the patterns consistently at higher speeds. The clock frequency at the output in this case has been divided down by four to enable speed compatibility with GPIO interface and also the false-lock output has been divided down by 32 to enable CMOS compatibility.

The Figure 56 shows the clock spectrum and the Figure 57 shows the false lock detector output for a true lock. It can be observed that in true lock, the output of the false-lock detector toggles for a brief period when the CDR is acquiring lock, and thereafter remains flat. The testing was done with two different repetitive patterns which were known to cause false-lock issues, the K28.5 and the K27.7. The Figure 58 shows the clock and the Figure 59 shows the output of the false-lock detector for the pattern K28.5. Similarly the Figures 60 and 61 show the clock and the output of the false-lock detector respectively for K27.7. In both these cases the FD was turned off.

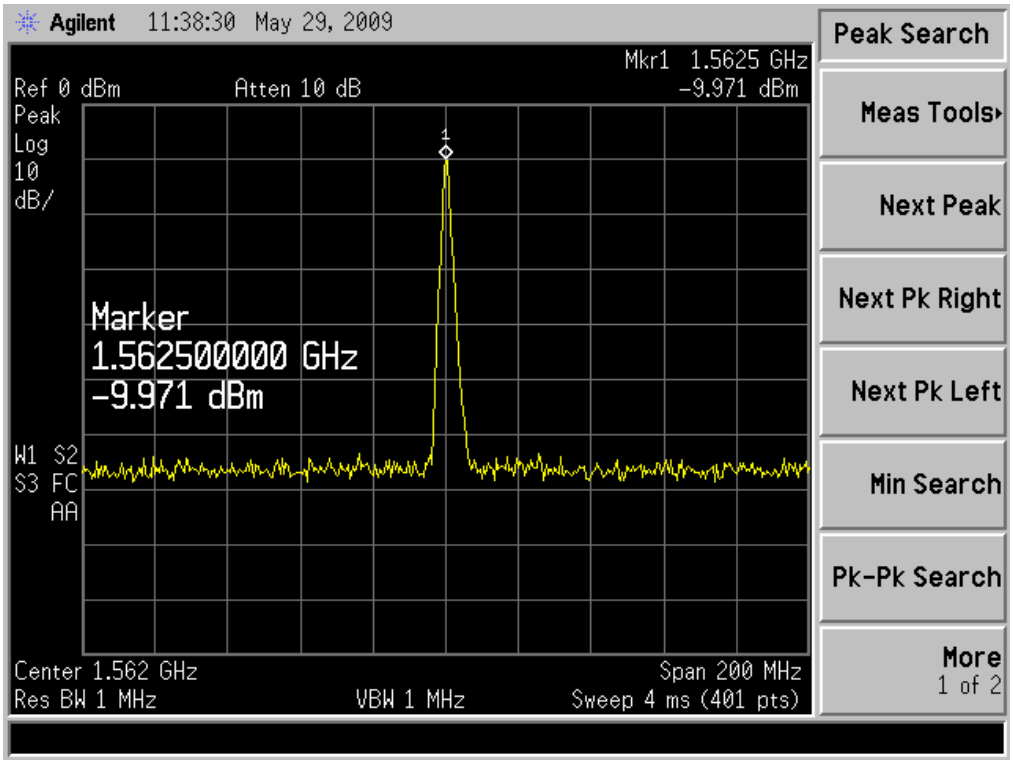


Figure 56. Spectrum at true-lock.

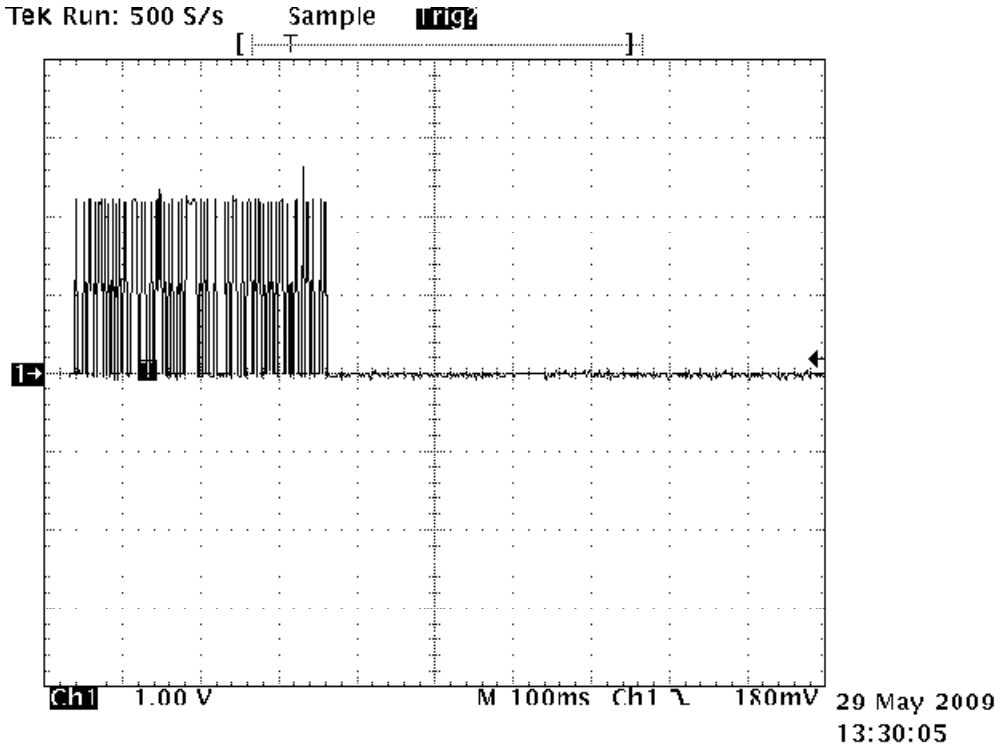


Figure 57. False-lock detector output at true lock. The system toggles initially when the CDR is acquiring lock, and then settles down.

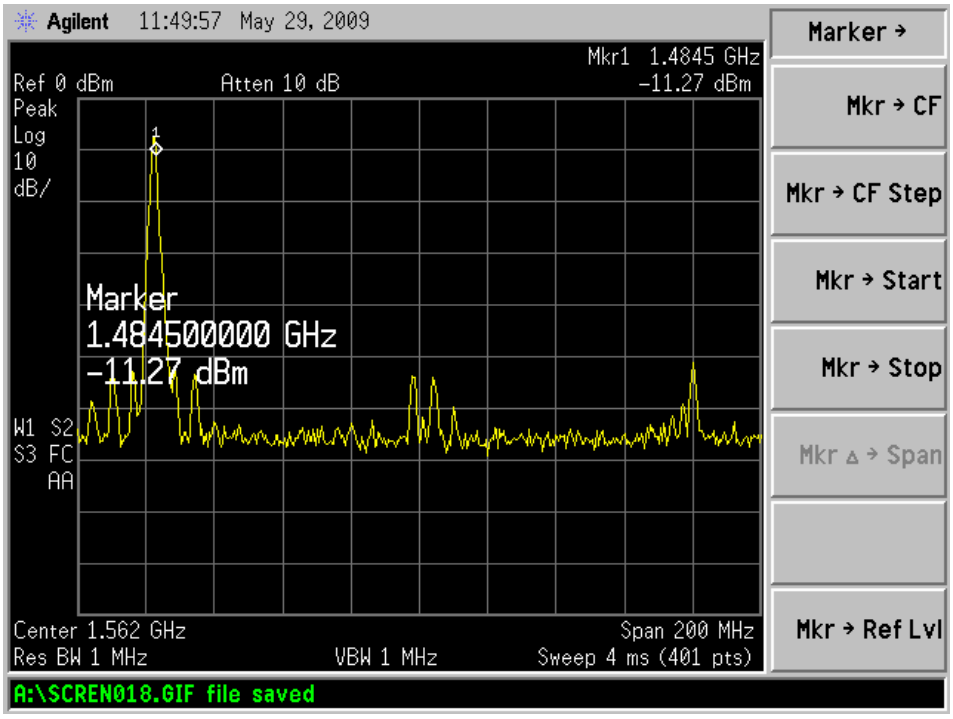


Figure 58. Spectrum at false-lock with K28.5 pattern. Note that the frequency is 19/20 that of true lock.

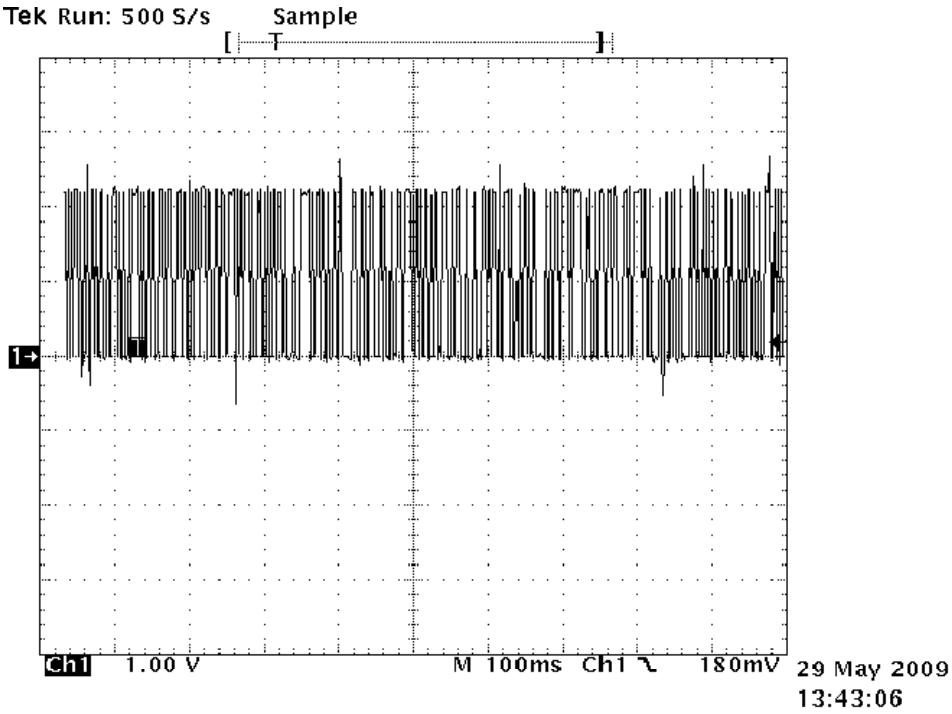


Figure 59. False-lock detector output toggles when the CDR false-locks for K28.5 pattern. This is the first time any reported system has successfully detected false-lock.

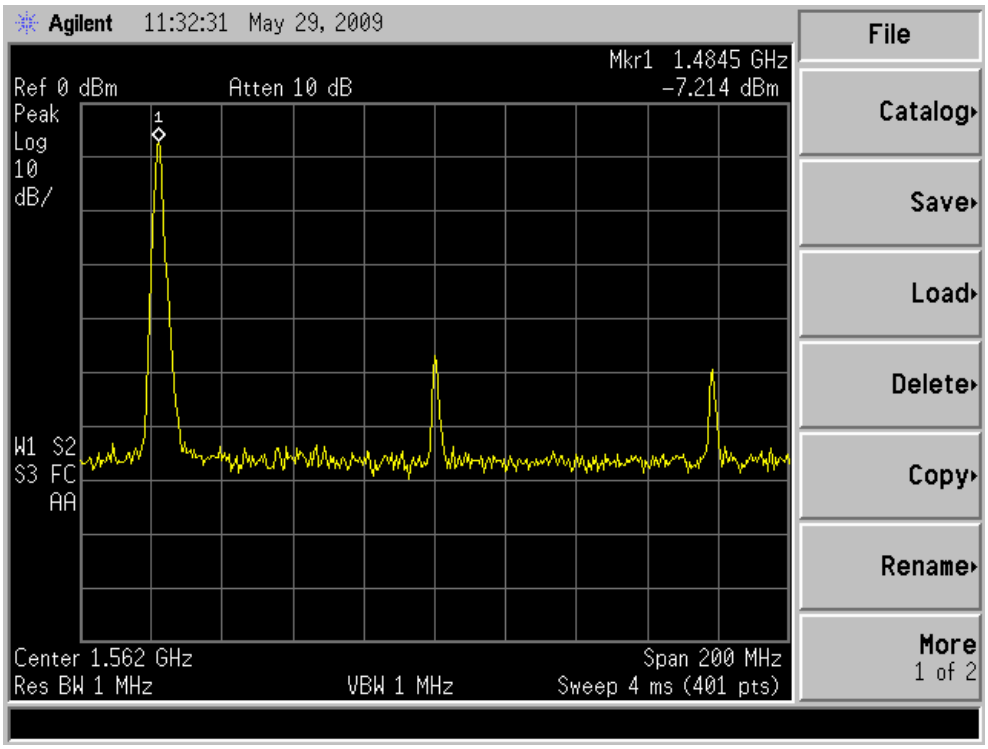


Figure 60. Spectrum at false-lock with K27.7 pattern. Note that the frequency is 19/20 that of true lock.

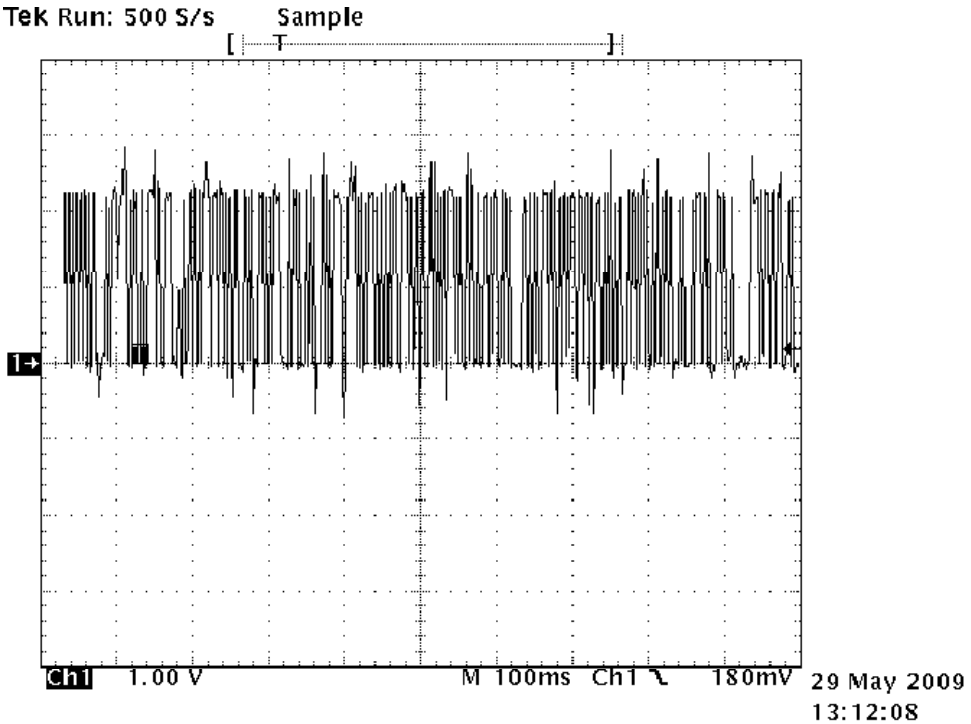


Figure 61. False-lock detector output toggles when the CDR false-locks for K27.7 pattern. This is the first time any reported system has successfully detected false-lock.

The proposed system was tested against a BERT system to ascertain the tolerance limits of the proposed system in catching errors. The results are plotted in Figure 62. As can be seen from the figure, the plots of the BERT and the proposed system are indistinguishable, thus proving the robustness of the system. Furthermore, the plot shows that the system can be used as crude on chip BERT to improve the CDR performance.

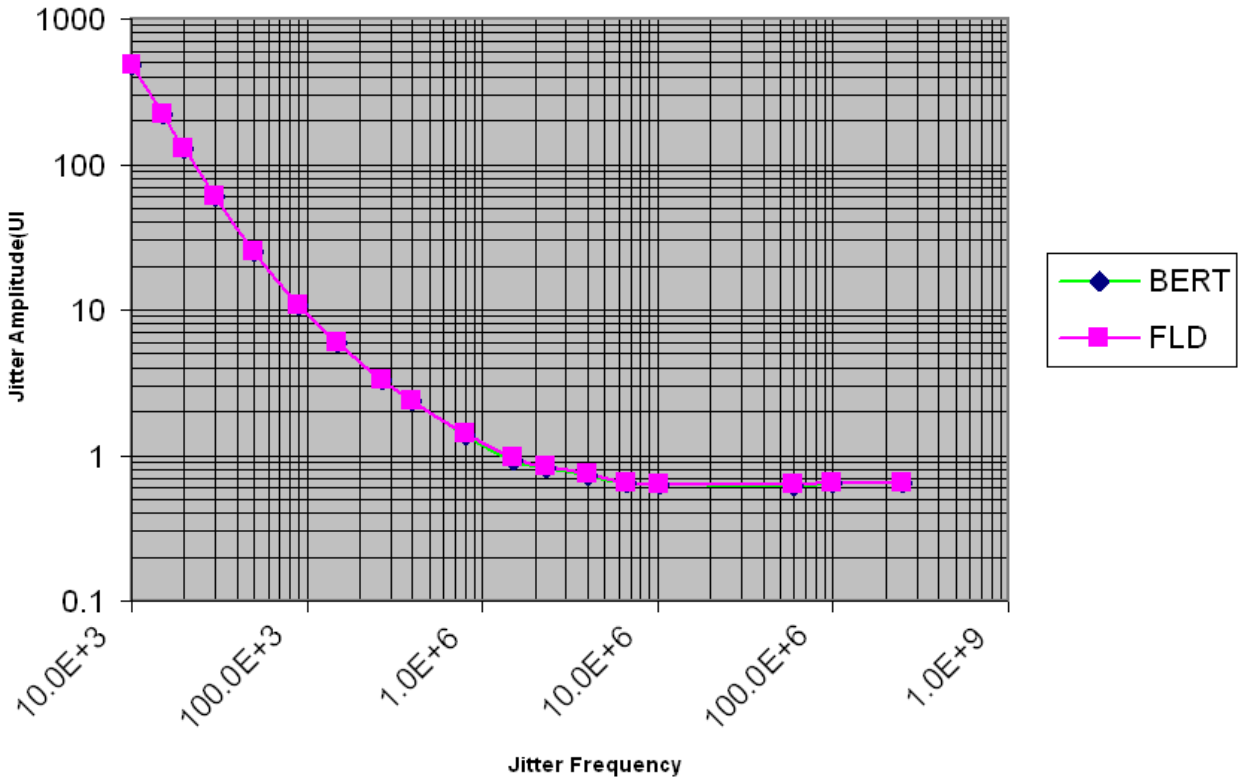


Figure 62. Plot of error detection of the proposed system (FLD) versus the BERT system. The plots are indistinguishable.

CHAPTER 6

VCO LAYOUT OPTIMIZATION

Almost all commercially available CDRs, which form the core of wire-line transceivers, are based on phase-locked loops. The heart of a PLL consists of a VCO with low phase noise. When a random data stream is passed through a CDR, the PLL extracts the fundamental frequency from the incoming data stream. The transfer function, H(s), of a type II, second-order PLL can be approximated as

$$H(s) = \frac{w_n^2(1 + s/w_z)}{s^2 + 2\xi w_n s + w_n^2} \quad , \tag{10}$$

where w_n is the natural frequency, s is the Laplace variable, and ξ is the damping factor.

Thus, it can be observed that the PLL transfer function from the input to the output is a low-pass filter. Furthermore, the transfer function from the VCO to the output is found to be a high-pass filter function Y(s):

$$Y(s) = \frac{s^2}{s^2 + 2\xi w_n s + w_n^2} \quad . \tag{11}$$

Therefore, it is clear that the PLL replaces the incoming signal jitter by the phase noise of the integrated VCO. Hence, generally VCOs integrated into PLLs are designed to have very low phase noise. Inductor-capacitor (L-C) tank-based VCOs are mostly preferred over ring oscillators because of their superior phase noise performance. It was noted in a previous publication that the phase noise of a VCO decreases as a cubic function of its quality factor (Q) [47]. It was further noted in the same publication that the phase noise of a VCO was reduced as a square of its output voltage. The output voltage of a VCO is directly proportional to the size of the inductor [47]. Thus, to reduce phase noise, a large inductor is generally chosen.

A reference-less CDR is a special type of CDR in which no external clock signal is required to perform phase-frequency alignment [44]. Typically, these types of CDRs are designed with a large acquisition range because the exact clock frequency is not known. A standard VCO with low tuning-range specification is generally designed with only variable capacitor (varactor) banks. However, in the case of reference-less CDRs, the internal VCO should also have a large tuning range in order to accommodate the large data acquisition range. Achieving this large tuning range necessitates the use of switched-capacitor banks on top of the varactor bank present in standard VCOs. The presence of switched-capacitor banks and the large inductor generally make the VCO the largest single block on the chip.

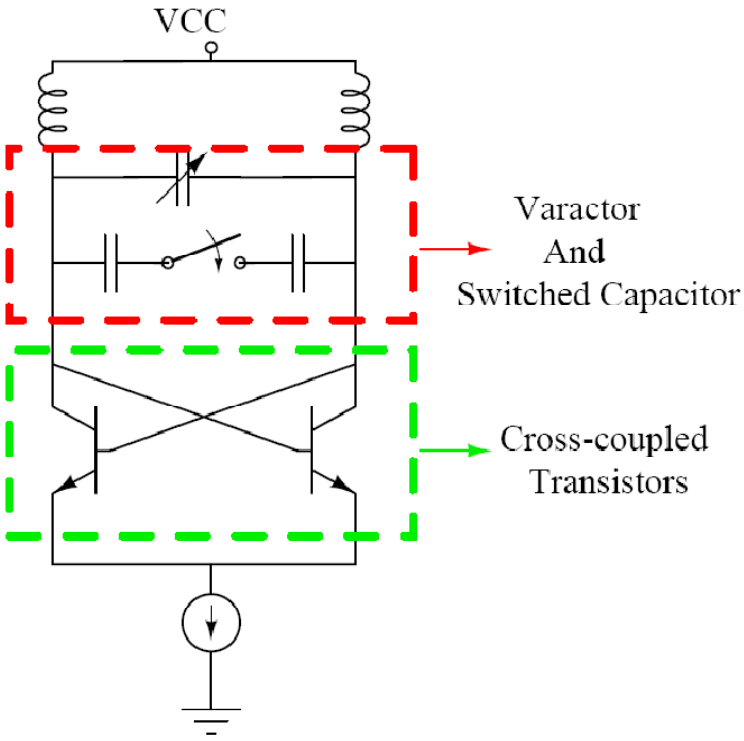


Figure 63. Schematic of a cross-coupled VCO with a varactor and a switched-capacitor.

6.1 NEED FOR A SYSTEMATIC VCO LAYOUT

The layout of the VCO is as critical as the design methodology. This is because a significant change in the effective quality factor of the VCO occurs due to post-layout parasitic elements. For example, long connections to the capacitor bank introduce extra resistance and inductance that reduce the available Q of the VCO tank. Routing varactor banks, capacitor banks, and the tank inductor has to be accomplished while remaining mindful of electromagnetic coupling and parasitic effects. This makes the layout especially challenging. A substantial amount of research material exists on VCO design [47]**.** Unfortunately, only a very small percentage of the previously published reports deal with the issue of VCO layout**.** Even those that deal with layout concentrate mostly on the spiral inductor structure**.** Hence, an urgent need developed to address the issue of an optimized layout for the VCO. It should also be noted that all L-C tank VCOs that require a large tuning range will inevitably have to incorporate the same components in any modern fabrication process. Hence, if a VCO layout technique is optimized for reference-less CDRs, it should be uniformly applicable to all wide-range VCOs.

A floor-plan of a typical VCO layout used in wire-line applications is shown in Figure 64. The noticeable aspect of this layout is the positioning of the varactor bank and the switched-capacitor bank. It can be observed from the figure, that the VCOs are generally laid-out in an interleaved format. The inductor of the VCO must be connected in parallel to both the varactor and the switched capacitor bank. Hence, the "leads" from the inductor are quite long in the traditional interleaved method of layout. In the traditional method of layout it has been found that the length of the leads can be up to 40% of the total inductor length. The lengths of the leads are generally not accounted for in the first pass of VCO design. Consequently, a large number of simulation and optimization iterations are needed to meet the final targets of the design. To somewhat reduce the length of the leads, the varactor and the switched-capacitor banks are physically positioned parallel to the direction of the leads. As maximum electro-magnetic coupling occurs for structures in parallel, the varactors and the switched capacitors have to be

moved a certain distance away from the leads to prevent electro-magnetic coupling. This extra wiring introduces unwanted parasitic elements to the tank of the VCO. If this wiring is made thicker, the Q of the VCO improves, but the extra parasitic capacitance reduces the oscillation frequency. If, on the other hand, the wiring is made thin, then the VCO holds on to its native oscillation frequency, but the Q of the tank is degraded because of parasitic inductance and resistance. In either of the cases, extra power and design time is needed to meet the desired performance parameters.

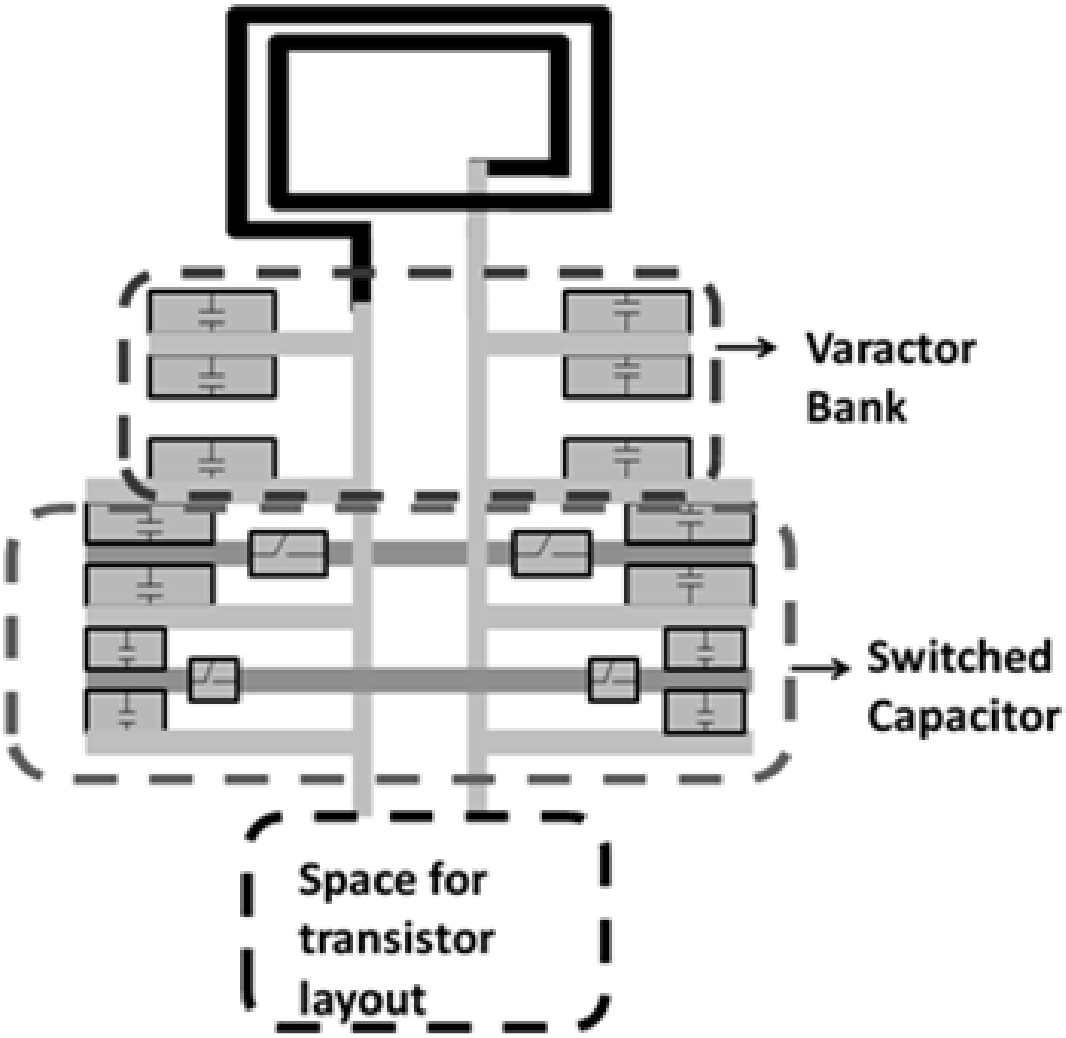


Figure 64. Traditional floor-plan of a VCO.

6.2 NOVEL VCO LAYOUT METHODOLOGY

A novel preliminary floor-plan is being explored as an alternative to the traditional method as shown in Figure 65**.** In this proposed floor plan, the distance between the leads has been slightly widened to accommodate the switched-capacitor bank in between the leads. The differential varactor bank has been positioned on the outer periphery of the leads. In this method, both the varactors as well as the switched-capacitors are physically positioned at right angles to the leads. As a result, the electro-magnetic coupling between the devices and the leads is minimal. Furthermore, now the varactors and switched capacitors can now be directly connected to the leads, without the need for any further wiring.

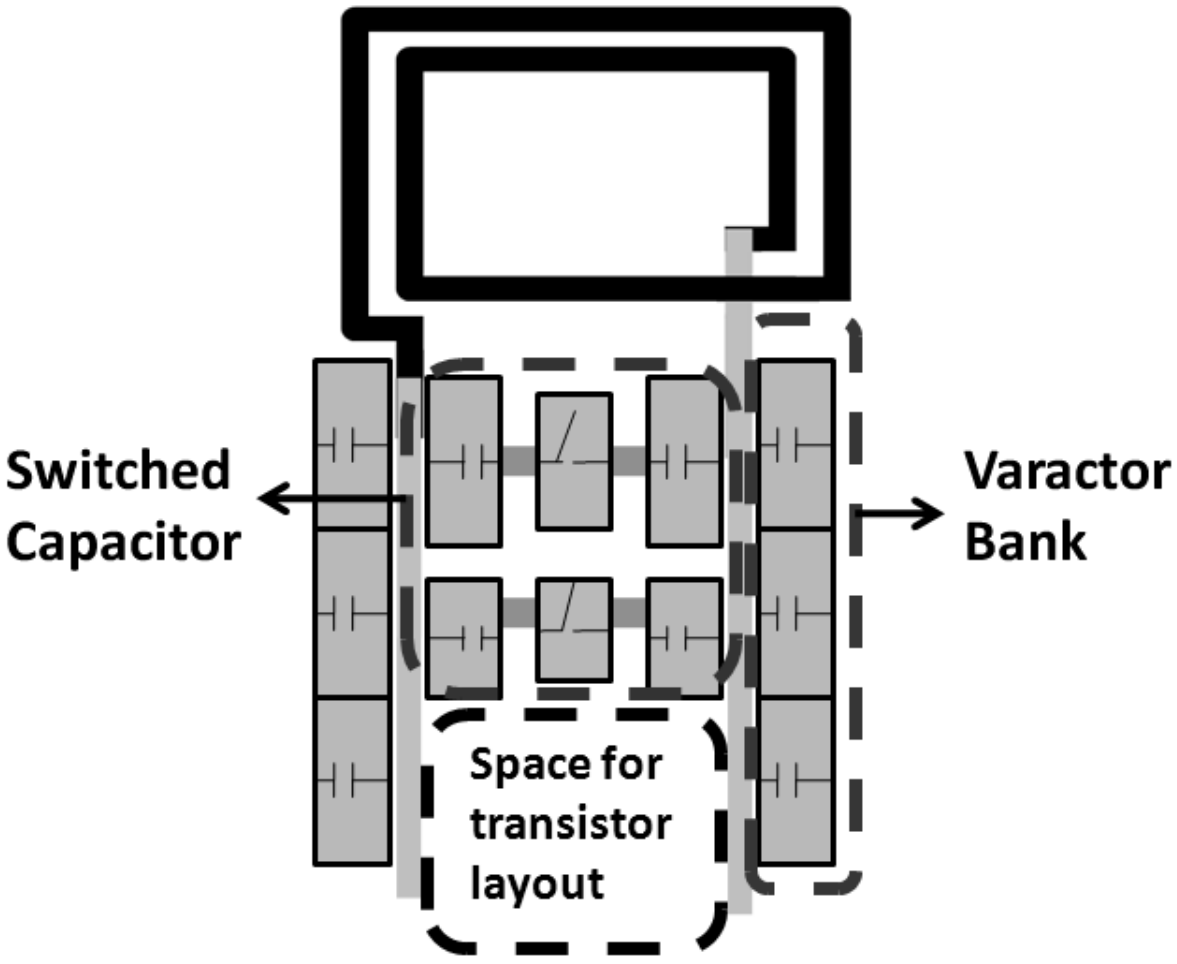


Figure 65. Novel VCO layout.

The advantage of this method is three fold. Firstly, the lengths of the leads are cut by 50%, as the varactor and the switched-capacitor are not stacked. Secondly, the area of the layout decreases dramatically (by almost 70%). Thirdly, the Q of the tank is fully preserved, without any shift in frequency, as there is almost no unaccounted parasitic involved in the layout. The Figure 66 compares the new layout versus an old VCO layout, both targeting the same specifications. The significant area saving (70 % approximately) can be easily noted from the figure.

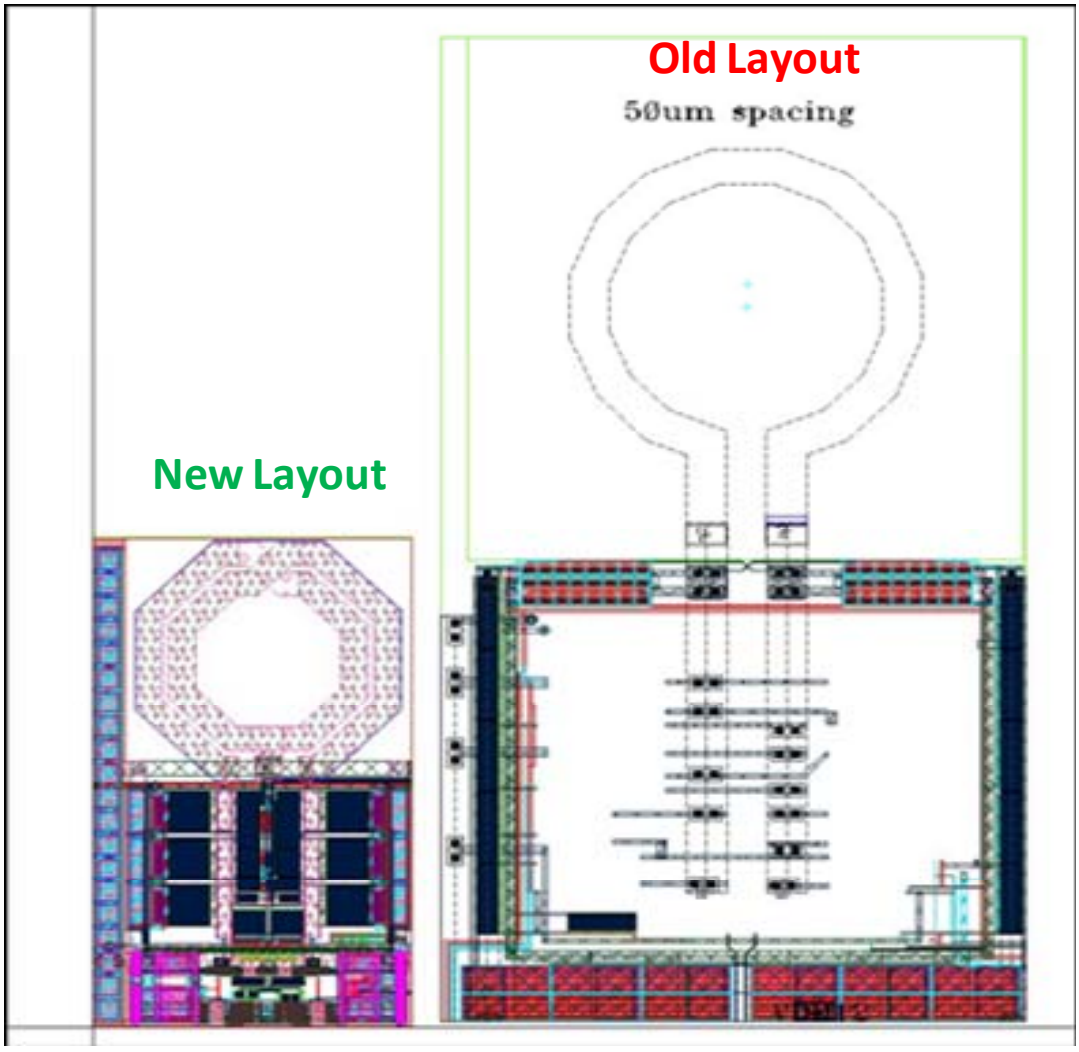


Figure 66. Comparison of the new VCO layout versus the old VCO layout.

The proposed VCO was designed in a 100 GHz f_T SiGe process. The targeted specifications for the VCO are tabulated in Table 4:

Table 4- VCO specifications.

Metric	**Targeted Value**
Frequency Range (cap-DAC)	24-26 GHz
Phase noise	-90dBc/Hz at 1MHz offset
Switched-Capacitor Bank	4-Bit for coarse tuning
Varactor Bank	3-element for fine tune range and high linearity
Supply Voltage	2.5 V
Power Consumption	Less than 20mW

The peak f_T of the process decreases to about 60 GHz at the worst process and temperature corner. Hence, the specified frequency has been chosen to stress the process to its limit as general designs only work up to $f_T/4$ frequencies. Under this condition, the specified performance would not be achievable in this process if the traditional layout was used.

6.3 VCO DESIGN DETAILS

The VCO needs to have both varactors to cover the fine tune range as well as the bank of capacitors to give it the necessary range and coarse tune capability. We chose to use MOS varactors in this implementation due their larger tuning range over comparable junction based

devices. The varactors had a liner range of operation from 0 to 0.6 V bias. In a 2.5 V process, generally the charge pumps would have a range of operation from 0.8 to 2 V (the range where the tail and the top current sources are both in saturation range). Hence, to utilize this complete range, more than one varactor would be necessary. Added to the 1.2 V range (2-0.8) an additional 0.3 V needs to be covered both at the lower end as well as the upper end of the voltage range. This is because the varactor needs to be in the linear range even with a large VCO swing. Otherwise, the non-linear portion of the curve would lead to degradation in the VCO phase noise. Thus the varactors need to have staggered bias ranges. In our case, to cover 1.8 V range (1.2 V+ 0.6 V of additional range) we needed 3 varactors staggered to turn on from 0.6 V, 1.2 V and 1.8 V.

It was also decided to have a 1.5 % range granularity in the capacitor digital to analog (DAC) block and 6% range in the varactor. This was done so that the varactor can access both the upper capacitor as well as the lower capacitor frequency range from any given DAC setting. This ensures redundancy in the VCO range and implies greater robustness.

Using the data outlined in the previous sections, three varactors were chosen, each nominally 122 fFs, and a capacitor DAC of 4 bits starting from the least significant bit (LSB) of about 9 fF. This ensures both high linearity as well as low error when switching ranges. Using the calculated values of capacitor bank and the varactor bank, the proposed VCO was designed and taped-out.

6.4 STATIC DIVIDER

The cost of evaluation boards go up considerably with the maximum frequency they can support. Hence a cost saving can be achieved if the output of the VCO can be divided down before being driven out to the board. To keep the overall power consumption to a minimum the supply voltage has to be limited to 2.5 V. At the specified frequency of 25 GHz, which is near

$f_T/2$, the lowering of supply voltage is a serious handicap. As the available speed of the devices decrease at lower supply rails, the CML blocks cannot be used. In order to achieve 25 GHz at 2.5 V rails, significant topological changes need to be made in the design of frequency divider. A modified version of a low-voltage, low-power logic family is being targeted to achieve the goal (Figure 67).

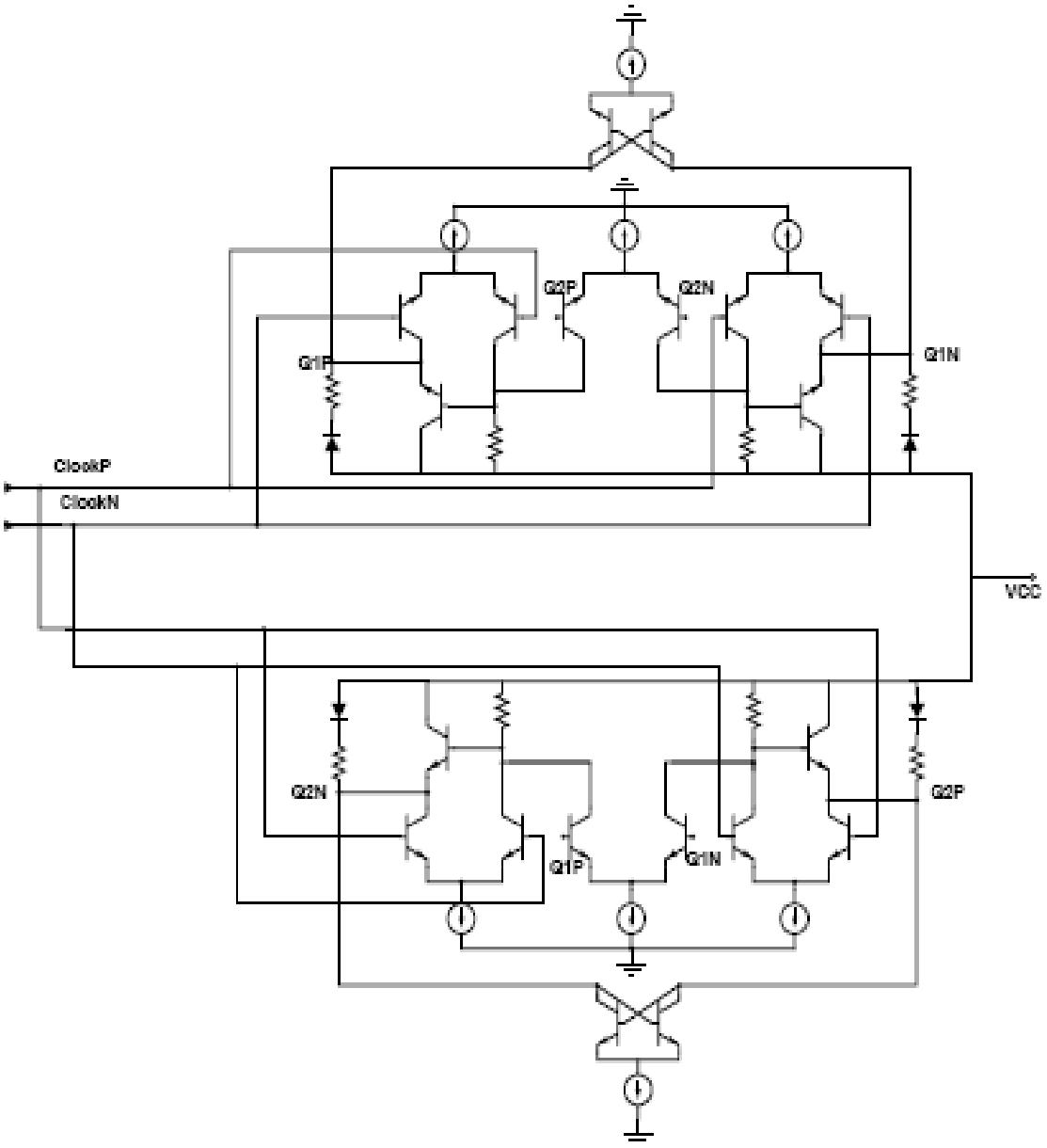


Figure 67. Modified LVL divide-by-2 circuit.

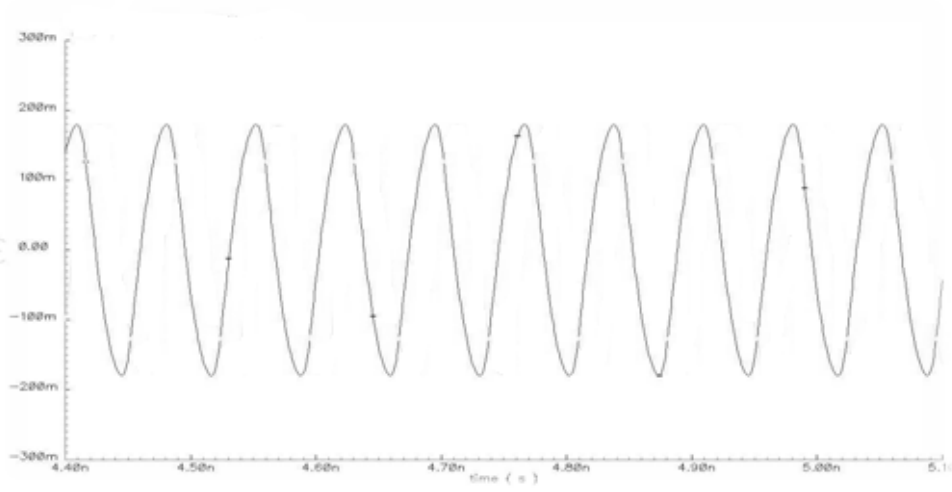


Figure 68. Simulation result of the divide-by-2 at worst process-temperature corner.

The modified LVL is the architecture that is most suited for high speed operations when working from low supply voltages [48]. The primary reason for this is the parallel gating architecture. The traditional CML based logic utilizes a serial gating method. What this means is that the clock logic and the data logic are physically stacked on top of each other to form a series gating. Though this is efficient at low speeds as both the data and the clock share the same bias current, yet at higher frequencies this is a serious handicap (show CML again in fig). The speed issue is compounded at lower supply voltages. The reason for this handicap at higher frequencies can be understood from the following explanation. As can be seen from the diagram, the CML has two signal levels separated by a diode drop. The clock level is exactly one diode drop less than the data level. For a 2.5 V supply, the data level can only be generated from a collector voltage level. Thus, if we assume a 200 mV swing, then when the data is high the corresponding transistor will be on (if the clock is in the sampling mode). Thus the collector would be 200 mV below the base. This base-to-collector forward bias severely limits the speed of the transistor. In

this particular fabrication process, a base-to-collector forward bias brings the f_T of the device down to about 25 GHz from the peak f_T of 100 GHz, at the slow/hot corner (the BJTs are slow and the temperature is 125^o C).

The LVL, on the other hand relies on parallel gating instead of series gating. In this architecture, the clock and the data level are both the same level denoted as "S2" level, which is the collector logic level shifted by one diode drop. The main gating is done by an idea adapted from high speed track-and-hold amplifiers called switched emitter followers. As can be seen from the diagram of the LVL, the output of the cell is driven by an emitter follower that sits on one branch of a differential pair that is being driven by the clock. Thus, depending upon the clock phase, the emitter follower either allows the data to be passed on to the static cross-coupled storage cell or decouples it from the storage cell. This action gives rise to a latch. The main advantage of this architecture is that there is no collector logic which stacks with another collector logic, thus reducing the voltage stacking by one diode drop over the comparable CML block. Further, no transistor, which is operating on a collector logic, goes into base-to-collector forward bias, thus helping each transistor to have it maximum possible speed.

6.5 MEASUREMENT RESULTS

The VCO, along with the divider, were taped out in a 100 GHz SiGe process from National Semiconductor. The Table 5 shows the phase noise of the VCO for different cap-DAC settings with the varactor tuning voltage set to nominal.

Table 5- VCO phase noise at different DAC settings

DAC Setting	Frequency Divided-by-4 (GHz)	Phase noise at 1 MHz offset
0	6.69	-107.56
1	6.64	107.94
2	6.6	107.99
3	6.575	-108.37
4	6.54	-108.08
5	6.5	-108.88
6	6.476	-108.93
7	6.445	-108.15
8	6.412	-109.6
9	6.376	-109.15
10	6.341	-108.55
11	6.313	-109.17
12	6.284	-109.21
13	6.251	-109.85
14	6.225	-110.1
15	6.197	-110.44

From the results, we can see that the VCO achieves a phase noise better than -110dBc/Hz over its range. The measured phase noise of the VCO at nominal DAC setting of seven is shown in Figure 69.

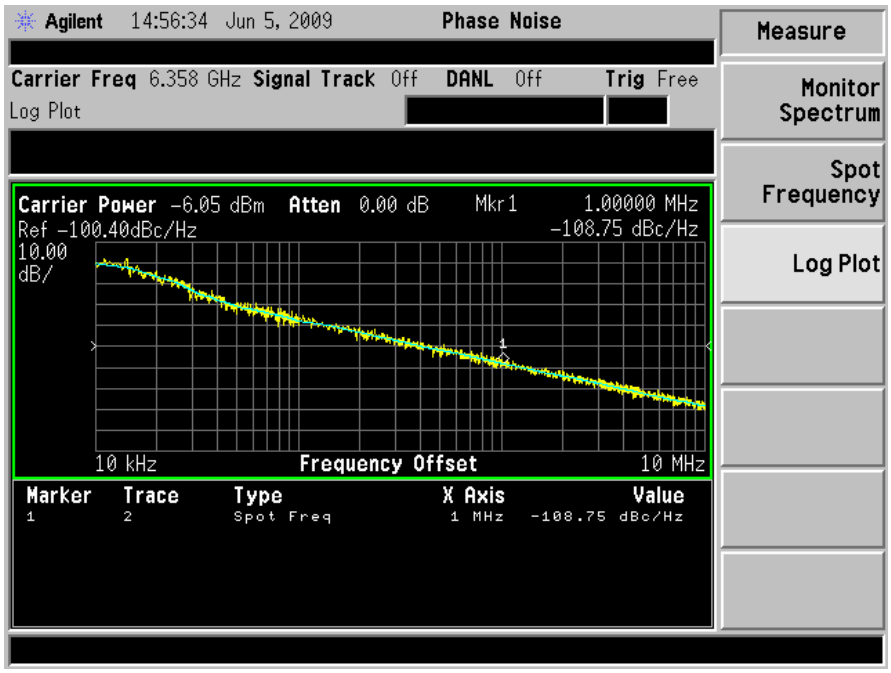


Figure 69. Measured phase-noise at divide-by-four output.

Table 6- Measured VCO specifications

Metric	**Measured Value**
Frequency Range (cap-DAC)	24-28 GHz
Best Phase noise	-110Bc/Hz at 1MHz offset (divide by 4)
Switched-Capacitor Bank	4-Bit for coarse tuning
Varactor Bank	3-element for fine tune range and high linearity
Supply Voltage	2.5 V
Power Consumption	15 mW Maximum

As can be seen from Table 6 that all the specifications that had been met or exceeded. This result includes the modified LVL divider in the path, hence, it also validates the tremendous speed achievable by the LVL topology. Moreover, this design and layout required significantly less number of passes as compared to the traditional method to meet the specifications. Since all the specifications were easily met at greater than $f_T/3$ speeds, it validates our novel layout approach. Traditional approaches would have found it hard to match the results while requiring similar resourses.

6.6 CONCEPT OF A NEW STATIC DIVIDER ARCHITECTURE

The LVL architecture, even though it has significantly improved speed over the CML, consumes much higher power than a CML. This is due to the fact that all the three differential pairs need to be biased at about the same current that a single CML cell needs. The table 7 compares the power consumption, speed and the number of devices necessary for a CML versus a LVL divider in the 100 GHz process from National Semiconductor that we are using when used from a 2.5 V supply. In some applications, this consumption would be unacceptably high despite the speed advantage of the LVL over the CML. Keeping this in mind, an attempt was made to reduce the power consumption of the divider while keeping the speed intact while operating from a 2.5 V supply.

Table 7- LVL versus CML divider

	Power Consumption	**No. of devices**	**Speed (worst corner)**
CML	2 mW	14	18 GHz
LVL	8.5 mW	24	25 GHz

An important distinction between a simple cascading of two latches and using them as a divider is the clock phase supplied to the two latches. A pair of cascaded latches can have a random bit as its input and also the two clocks can be independent of each other. This is not the case when the latches are used as a divider. Then both the clocks are always a phase of ∏ radians away from each other. Further the input and output both are sinusoids of the same frequency. Thus the clocking pair can be shared in between two latches instead of each latch having its own dedicated clocking pair. The concept is shown in Figure 70. A consequence of this is the reduced decoupling from the input of the latch to its output in the hold state. Fortunately, this is not an issue for a divider as because both the input and the output are sinusoids of the same frequency. Thus they can be thought of as two standing waves with a relative phase shift between them. Thus, any leakage does not contribute to jitter. Instead, it only reduces the amplitude of the swing, which can be remedied by increasing the gain of the pass cell.

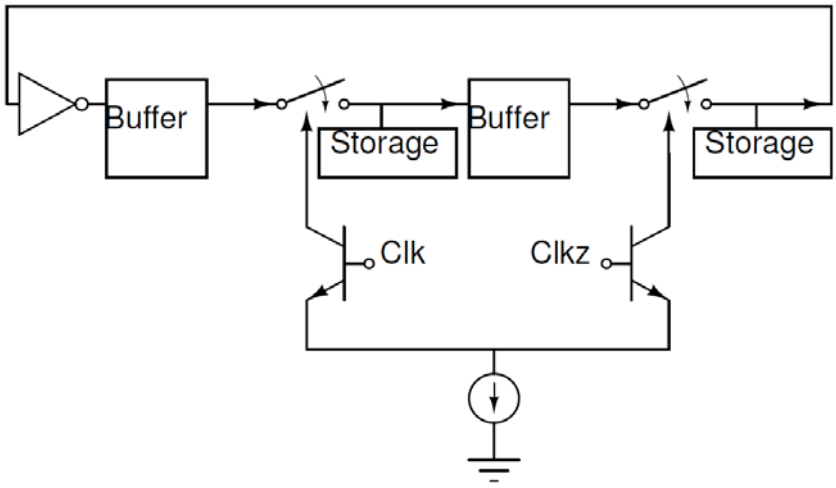


Figure 70. Conceptual representation of a new static divider.

The proposed concept has been applied to an LVL cell, as the LVL has the best speed characteristics when operating from a 2.5 V supply. The Figure 71 shows the new divider. As can be seen from the figure, the new circuit is significantly simpler and smaller than the LVL. It

also needs about 50 % less power than the LVL. The worst maximum speed, number of devices and the total current consumption of the new divider has been compared with the LVL in table 8.

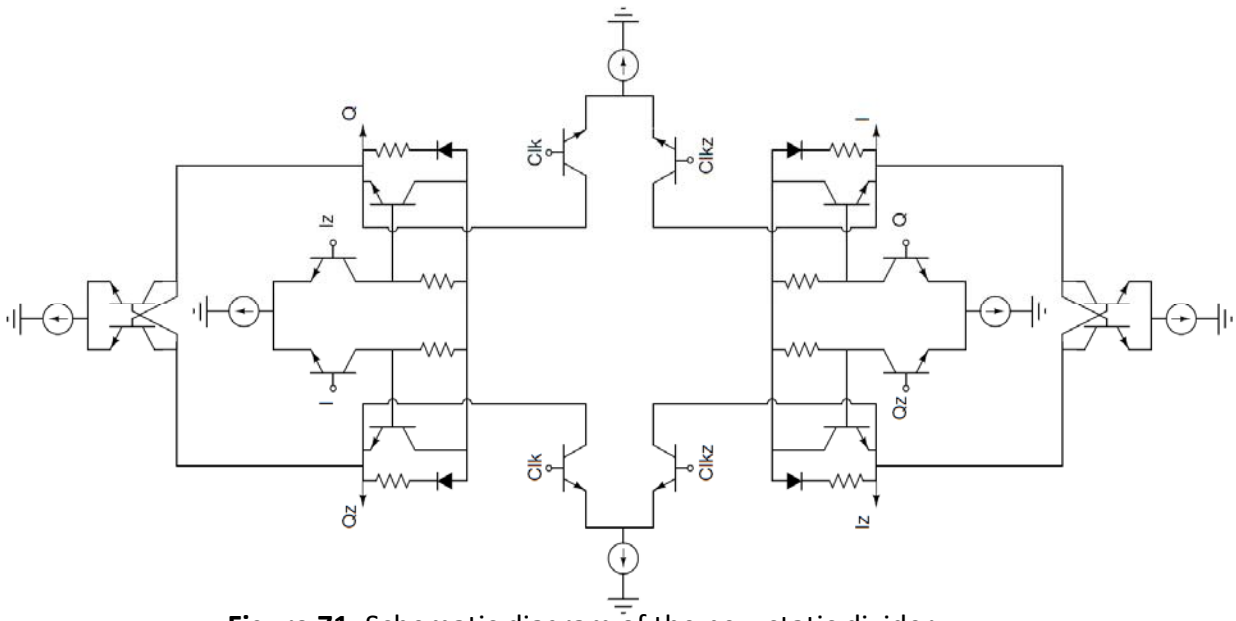


Figure 71. Schematic diagram of the new static divider.

Table 8- LVL versus the new concept

	Power Consumption	**No. of devices**	**Speed (worst corner)**
LVL	8.5 mW	24	25 GHz
New Divider	4.5 mW	20	28 GHz

CHAPTER 7

CONCLUSION

The object of this research is to develop robust wire-line systems which demonstrate high performance while simultaneously consuming low power. Most high performance designs come at the expense of high power consumption, while low power designs typically are not as robust as high power architectures. These problems have retarded the development of multi-gigabit wire-line systems. In this thesis, a holistic approach consisting of system level architecture modification, along with circuit level innovation and optimization has been presented to circumvent the stated problems. In this chapter the contribution of this dissertation has been summarized along with the analysis and prediction of the possible future work.

7.1 CONTRIBUTIONS

In this dissertation the primary focus was developing high performance CDR circuits which are robust and also consume as low power as possible. One way to classify the work would be to partition the work under high performance at low power and the other would be robustness with low cost.

The first topic addressed under the high performance classification is the broadband amplifier. A modified Cherry-Hooper architecture has been implemented. Current sources at the tail have been modified with MOS devices to reduce headroom requirement, also making the circuit a true BiCMOS circuit which utilizes both the HBT as well as the MOS devices present in the process effectively. Gain peaking strategies were implemented using transmission lines leading to more accurate values. A new gain taper strategy has been implemented to optimize bandwidth as well as jitter. The amplifier has achieved a 62 GHz bandwidth while consuming

only 125 mW, the lowest power consumption amongst any amplifier to achieve 60 GHz bandwidth as known by us.

The second topic studied under high performance circuits is the injection locked clock recovery. The literature study and our research of injection locking revealed that it is a very economical method to recover clock from PRBS data and can be utilized to design cost effective CDRs. The simplicity of the method, coupled with the low number of devices and low power would have made it an ideal circuit to implement for very high speed applications. Unfortunately, our research revealed that the injection locking method has jitter tolerance issues for far-out jitter. Also it was found that the method cannot filter the jitter beyond the natural filter curve of the VCO. We therefore, based on our research, do not recommend using injection locking method as a standalone CDR when jitter tolerance limits are imposed.

The third topic addressed under high performance CDR circuits is the VCO layout. Commercially available CDRs with low jitter transfer characteristics generally use L-C tank VCOs. Almost all such VCOs have similar structures, with switched capacitor banks for coarse tune and varactor banks for fine tune. As is known in high speed design, the layout of a VCO is as important as the design steps because the VCO parameters can change by as much as 50 % in post-layout conditions. Typically, this would be tackled by multiple design passes, again assuming that an accurate parasitic characterization is available and even then mostly power is increased to compensate for the parasitics. In this work, a novel and systematic layout technique has been proposed. The method can be generically applicable to any L-C tank VCO for wireline systems. The method was found to reduce the area requirement by 70 % while drastically reducing parasitic elements. Thus multiple design and layout passes could be avoided. The VCO measurement results confirm the potency of the layout method with a speed exceeding f_T /3 while consuming minimal power. A new concept was developed for the design of a static frequency divider that leads to approximately 50 % saving in power over conventional static dividers.

The other classification we targeted is achieving robustness at low power. As it was found that the latch, on account of its cross-coupled storage, is the most sensitive circuit of a CDR with respect to its robustness, hence this was the circuit we targeted. It was also found from literature survey that package radiation and other radiation effects severely affect the BER of a CDR. Thus the aim of this work was to try and reduce data loss from a latch because of radiation and also to do it by purely circuit level techniques. In this work we have proposed a novel method to make SiGe HBT based latch radiation hardened. The technique is based on a systematic response to a single-ended effect. The method tries to route the current and charges in such a way that any SEU has minimal effect while true differential data is passed without any detrimental effect. The technique has been successfully applied to a LVL latch and also to a CML latch with moderate success. The method significantly reduces the penalty to make the latches radiation hardened as compared to other comparable works.

The final topic addressed is the topic of false-lock detection in CDRs and is our most important contribution towards robustness of a CDR. Reference-less CDRs have been gaining ground in the commercial CDR market because it can be easily be targeted at a multi-market design and also because it does away with the need of having a crystal oscillator, which saves cost as well as reduces pin count. Reference-less CDRs are susceptible to false-lock in the presence of a repetitive pattern. For the first time, a robust lock-detection method has been proposed, based on the cross-correlation of raw and re-timed data. The system has been demonstrated to catch false-locks due to various patterns like the K28.5. The system is simple to design and implement and is capable of very high data rates beyond 10 Gb/s. Further, the system is platform and process independent and can be designed into any existing CDR.

7.2 FUTURE WORK

In this section we outline how some of the work presented in this dissertation can be taken forward. The three major blocks which need to be researched further are the injection locked clocked recovery, the radiation hardening and the false-lock detection/ prevention.

The injection locked clock recovery suffers in performance in the presence of jitter. The system always locks to the frequency where the average power is greatest, provided that the injected spectrum is within the VCO bell curve. Furthermore, in case of close-in jitter, the system fails to adequately reject or attenuate it resulting in high jitter transfer. On the other hand the system can lock to incoming data stream almost instantaneously, making it lucrative from the perspective of burst-mode CDR. A direction of research that could be undertaken, then, is to see if a PLL-injection locked hybrid can be designed that can improve the jitter attenuation over the injection locked scheme, while improving the lock time of the PLL based CDR.

The radiation hardening block has primarily been designed for a LVL latch. The LVL latch is not a widely used or a standard latch like a CML. The concept of current routing, so as to prevent logic flip, needs to be refined and adapted for CML and other blocks. The circuits need to tested much more thoroughly under different environmental stresses to understand the drawbacks and overcome them. Furthermore, we would recommend starting a redundancy network from ground up using the concept, instead of trying to fit the same network to different circuits.

The false-lock detector represents the first time any working solution has been demonstrated for this problem at high speeds. The work is a break-through result which can potentially remove the drawbacks of reference-less CDRs vis-à-vis referenced CDRs. The work still needs refining and improvement. The idea that has been explored here is the detection of false-lock followed by a system-level remedy. A possible topic of research, in this regard, should be to investigate if the false-lock can be prevented by improved phase/frequency detector design.

The truth table of the Pottbacker PFD had been presented in this work. We had also identified potential drawbacks in the truth table. Fortunately for us, we could implement and test a robust solution by way of the detector. But, the logic correction of the Pottbacker still needs to be researched.

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