CMOS RF SOC TRANSMITTER FRONT-END, POWER MANGAMENT AND DIGITAL ANALOG INTERFACE

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CMOS RF SOC
TRANSMITTER FRONT-END,
POWER MANGAMENT AND
DIGITAL ANALOG INTERFACE

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

With the growing trend of wireless electronics, frequency spectrum is crowded with different applications. Some commercialized products, such as Bluetooth and Zigbee, operating at 2.4 GHz, can offer data transfer rate in the range of kbps to Mbps. However, with the vast increase in digital media transfer and storage, this data transfer rate will not be feasible due to the time consuming process. High data transfer rate solutions that operate in license-exempt frequency spectrum range are sought. The most promising candidate is the 60 GHz multi-giga bit transfer rate millimeter wave circuit. In order to provide a cost-effective solution, circuits designed in CMOS are implemented in a single SOC.

PAs achieving reasonable performance have been designed; however, design cycle, which eventually increases design cost, is lengthened because no single CAD tool can provide an accurate and efficient way for extremely high frequency simulation in time domain and frequency domain. In this work, a modeling technique created in *Cadence* shows an error of less than 3dB in magnitude and 5° in phase for a single transistor. Additionally, less than 3dB error of power performance for the PA is also verified. At the same time, layout strategies required for millimeter wave front-end circuits are investigated. All of these combined techniques help the design converge to one simulation platform for system level simulation.

Another aspect enabling the design as a single SOC lies in integration. In order to integrate digital and analog circuits together, necessary peripheral circuits must be designed. An on-chip voltage regulator, which steps down the analog power supply

voltage and is compatible with digital circuits, has been designed and has demonstrated an efficiency of 65 percent with the specific area constraint. The overall output voltage ripple generated is about 2 percent.

With the necessary power supply voltage, gate voltage bias circuit designs have been illustrated. They provide feasible solutions in terms of area and power consumption. Temperature and power supply sensitivities are minimized in first two designs. Process variation is further compensated in the third design. The third design demonstrates a powerful solution that each aspect of variations is well within 10%.

As the DC conditions are achieved on-chip for both the digital and analog circuits, digital and analog circuits must be connected together with a DAC. A high speed DAC is designed with special layout techniques. It is verified that the DAC can operate at a speed higher than 3 Gbps from the pulse-shaping FIR filter measurement result.

With all of these integrated elements and modeling techniques, a high data transfer rate CMOS RF SOC operating at 60 GHz is possible.

CHAPTER 1

INTRODUCTION

1.1 Motivation

In recent years, driven by market, personal wireless devices have made a great leap in advancement as shown in current technology, such as Bluetooth, Ultra-Wide Band (UWB) and ZigBee. IEEE 802.15 Task Groups have been specifically established to standardize commercialized products compatible with wireless personal area networks (WPANs). These common standards are indicated in Table 1.1

Table 1.1 Some common commercialized technology standards in WPAN

	Bluetooth 2.1 + EDR (802.15.1)	ZigBee (802.15.4)
Maximum Frequency	2.4 GHz	2.4 GHz
Maximum Data Rate	3 Mbps	250 kbps

However, all the existing standards in WPAN only support low data transfer rate, suitable for applications such as audio or simple remote control. With the highest data transfer rate system in current wireless local area network (WLAN), 802.11n can only support about 250 Mbps operating at 2.4 or 5 GHz. In order to satisfy the number of growing high throughput data transfer and video applications demanding new wireless standards, one such developing standard is 802.15.3c. It focuses on 60 GHz modulation frequency, which promises multi-gigabit data transfer rate that is high enough for real time video streaming applications, such as high-definition television (HDTV), video on

demand (VOD) and XBOX. Currently, frequency spectrum at that range is license-exempt, defined as 57-64 GHz in US by Federal Communications Commission (FCC) 47 CFR 15.255 and 59-66 GHz in Japan. Military applications have already utilized that frequency band using group III-V compound semiconductor, which inherits high cutoff frequency (f_T) and high oscillation frequency (f_{max}) [1]. Those materials are usually used as Heterojunction Bipolar Transistors (HBT) and Pseudomorphic High Electron Mobility Transistors (PHEMT) structure. The main drawbacks are high large-volume cost and lack of digital integration. In addition, heterogeneous integration also introduces many problems, which may make system-on-chip (SOC) impossible with CMOS baseband circuit. Eventually, it increases the size of the chip due to the extra interfacing layers between different materials during fabrication or packaging process.

One solution that is widely used in modern cell phones is separation of components. All the circuitries are assembled on a printed circuit board (PCB), instead of SOC. The electrical performance may not be significantly degraded if it is operated at lower frequency, such as 2-5 GHz. However, once millimeter wave design has to be employed that utilizes transmission line theory, extreme caution must be placed throughout the design and fabrication process for each external wire connection. It is because the dimension of a single wire may introduce extra inductance, capacitance from pad connections and antenna effect through radiation causing significant performance degradation. Eventually, the system will be sensitive to assembly procedures and decrease the yield and throughput of the final product. Additionally, the possibility of mechanical failures, such as thermal coefficient mismatch, during packaging processes also further decreases the yield. This issue has been overseen by market for several

years. Thus, the cell phone industry increases the level of integration by moving on to SOC and stacking for local components. SOC does not only increase the reliability, but also decreases the area and cost.

With the advancement of CMOS into the nanometer regime, a single SOC that integrates the whole transceiver with digital processor is possible. Another attractive attribute from 60 GHz modulation frequency is that propagation characteristic sharply falls with distance and is significantly blocked by human skin, due to oxygen absorption. As a result, this propagation characteristic reduces signal interference, such as echo effect, and hazardous effect towards human.

With this promising solution in terms of applications, fabrication processes and individual circuit blocks, a SOC-based on-off keying (OOK) modulation transceiver chip is constructed. It utilizes direct conversion structure, which is less complex with less power consumption compared with traditional heterodyne or super-heterodyne architecture, as shown in Figure 1.1. The transmitter consists of a pulse-shaping finite impulse response (FIR) filter, digital signal enhancement circuit, up conversion mixer, power amplifier (PA), voltage control oscillator (VCO) and phase lock loop (PLL). The receiver is composed of a low noise amplifier (LNA), amplitude detector, analog-to-digital converter (ADC), clock data recovery (CDR) circuit and output buffers.

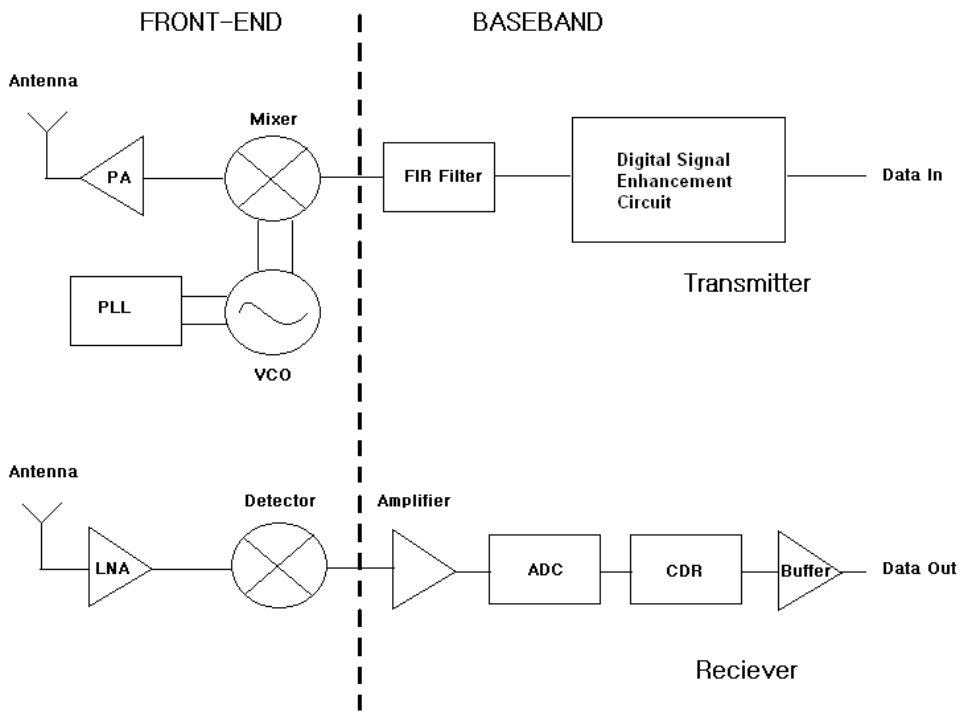

Figure 1.1 OOK SOC with direct conversion topology.

Ideally, each front-end block will work as expected if correct supply voltage and bias voltage are applied. In addition, many IEEE publications also indicate a workable solution at this frequency band for different separated blocks with variations in performance [2-4]. However, another challenge for SOC is to have a compact integrated system. With limited area, no room exists to accommodate all the input and output pads for each bias voltage or supply voltage, especially since one side of the SOC is occupied by antenna pads. In order to solve this problem, associated bias circuits and voltage regulator have to be integrated into the chip.

All of these DC circuitries are essential elements because they govern the power consumption and output signal strength of the system and ensure proper operation.

Hence, a detailed planning from system, design to layout level has to be carried out effectively.

As an example, PA and mixer in the transmitter front-end require DC biases. If there is any incorrect bias voltage, it can lead to a few decibel (dB) losses in signal. In a serious situation, it will significantly distort the signal due to saturation of the PA, and it eventually generates undistinguishable signal when it is transmitted to the receiver.

With the growing trend of digital transmission, digital components will eventually be integrated into the chip for multiple-input and multiple-output (MIMO) to improve communication performance. In order to maximize the compatibility of the radio frequency integrated chip (RFIC) with baseband digital circuits, such as physical layer (PHY) and Medium Access Control (MAC), a compatible digital-to-analog (DAC) circuit, which enhances spectral efficiency with the pulse-shaping FIR filter, will have to be implemented between digital and analog domain.

1.2 Transmitter Front-End Design and Simulation

Power amplifier generally is divided into two modes of operation, and each mode has difference classes. For non-switch mode of operation, it is classified into A, AB, B and C. These classes have the trade-offs among efficiency, linearity and gain. Table 1.2 summarizes the performance of these non-switch mode classes of operation.

Table 1.2. Amplifier performance comparison for non-switch mode of operation[5]

	Class A	Class AB	Class B	Class C
Conduction Angle	$\theta = 360^o$	$180^o < \theta < 360^o$	$\theta = 180^o$	$\theta < 180^o$
Efficiency	$\eta = 50\%$	$50\% < \eta < 78.5\%$	$\eta = 78.5\%$	$\eta > 78.5\%$
Linearity	Best	Fair	Good	Poor
Gain	Large	Moderate	Moderate	Small

Switch mode amplifiers usually utilize switches to charge and discharge a capacitor through combinations of inductor and capacitor networks. This type of amplifier is not feasible in extremely high frequency (EHF) domain, which is from 30 GHz to 300 GHz, because it generally only has small gain and poor linearity. In addition, the switch within the amplifier would not be able to incorporate a control loop that is fast enough in this regime.

Once the topology has been chosen, a detailed investigation on transistor dimension, process and bias voltage are also critical for amplifier operated in EHF. This dimension eventually will govern the parasitic capacitance and resistance within the transistor and affect the overall performance. 90nm RF CMOS technology is specifically chosen for this application. The NMOS in this process inherits a maximum oscillation frequency (f_{max}) of 200 GHz and cutoff or transit frequency (f_T) of 150 GHz [6], which are sufficiently high enough for the 60 GHz operation. As the process scaled down to 65nm and below, f_{max} and f_T are also increased due to the decrease in parasitic elements and gate oxide thickness. However, at the same time, this small feature size technology lowers break down voltages and eventually leads to poor linearity of front-end amplifiers.

In radio frequency (RF) domain, impedance-matching networks are common techniques used to reduce power loss between different stages of PA and high frequency components. The matching networks ensure that the impedance is transformed to be conjugated to the target impedance location for maximizing power transfer. In most of the commercialized RF electronics, reactive lump components are usually deployed. However, it is not realizable in millimeter wave domain due to CMOS low quality factor passive components with limited self-resonant frequency. With additional degeneration

effect from CMOS lossy substrate, transmission lines, such as microstrip and coplanar, have to be employed. In addition, a thick metal layer is also required in order to minimize sheet resistance of the signal line.

Traditionally, all the designs in EHF are based on frequency domain simulators, such as *Agilent Advance Design System* (*ADS*), and measurement result; however, time domain simulation is not accurate and reliable in those platforms relative to other time domain based simulator.

This issue is particularly serious while designing a mixer in this case. The mixer has to interact with digital circuits in system level; however, all of the digital circuit designs are based on time domain simulator, *Cadence*. Hence, a proper model has to be developed in order to perform accurate and reliable system level time domain simulation.

1.3 Voltage Regulator Design

Analog circuits, such as a PA and mixer in this case, usually use a power supply voltage of 1.2V or above to maximize gain and linearity. The gain and linearity performances are more essential in CMOS technology. PA designed with Silicon Germanium (SiGe) or Gallium Arsenide (GaAs) usually has a better performance in terms of gain, power added efficiency (PAE) and linearity [7]. Meanwhile, digital circuitries in 90nm CMOS are operated in 1V power supply. If the power supply voltage is above or below 1V, it will cause transistor breakdown or degrade the performance.

When analog and digital circuits operate with different supply voltages, only a step-up (boost) or step-down (buck) converter can be used as a solution. Buck converter is chosen because digital circuits usually do not consume a large amount of current. As a

result, the efficiency degradation from the converter will be relatively minimized. In addition, all the voltage regulators existed today inherit output voltage ripple. This ripple is more tolerable with digital circuits since those circuits are more insensitive to power supply noise.

Once the architecture is decided, a thorough frequency planning has to be done in order to ensure proper operation. In high power domain, such as power generator or civilian adapter for power outlet, the design is less challenging. The obstacle in on-chip regulator design is the trade-off between area and efficiency. Thus, an overall chip layout has to be taken into account in the design phase. Another problem that makes the design more difficult is the baseband circuits that are operated at 1.728 Gbps, while most of the existing voltage regulators are operated in kHz frequency range. As a result, higher sample rate have to be used in the regulator to avoid possible overshoot in current or voltage.

1.4 Bias Circuit Design

Bias circuit has the same important role as a voltage regulator; however, the magnitude of effect for the bias circuit is large. All the analog amplifiers, buffers and mixed-signal circuits within the chip require a bias voltage in order to ensure transistors are operated under saturation condition. For example, with a slight shift in the bias voltage, the PLL and VCO may not lock into the correct frequency. However, unlike a voltage regulator, this standalone circuit within the chip is self-monitored without any feedback from the load. As a result, it is prone to variation in power supply, temperature

and process. Additionally, those variations are not uniform throughout the chip. As a result, a very robust design is required.

Many techniques have been developed, such as the bandgap referenced, subthreshold operating condition, Complementary To the Absolute Temperature (CTAT) and Proportional To the Absolute Temperature (PTAT) circuits to minimize temperature and power supply fluctuation effects; however, most of the circuits neglect process variation, which is critical in current small feature size IC technology. In addition, those circuits are usually complex and may include an amplifier internally for low supply voltage condition, which makes integration to a large scale system unfeasible in terms of power consumption and process variation.

In order to accommodate the bias circuits for the system as a whole, a system level planning has to be done first, such as area constraint, power consumption and integration scheme.

1.5 Digital-to-Analog Converter

With the necessary voltage regulators and bias circuits designed, external circuits can interact with the chip with less supply voltage and data input and output pads. Meanwhile, internally, digital circuits and analog circuits have to be bridged with a digital-to-analog converter (DAC) for transmitter and analog-to-digital converter (ADC) for receiver system in order to complete the system.

Similar to a bias circuit, the DAC in transmitter should be invariant towards temperature and process. Power supply rejection is not as critical as bias circuit. The reason is because the DAC is integrated into the pulse-shaping FIR filter in this

implementation. If the filter should experience any power supply voltage drop, the DAC should also be outputting the corresponding level according to the digital circuit dynamic range and resolution.

1.6 Summary

This chapter illustrates the high speed performance of the new personal area network technologies by comparing current commercialized standards. With the growing of digital media transmission and the massive increase in digital storage, it is eminent that 60 GHz radio provides a promising solution for future high speed wireless data transfer.

In order to put the solution into production, a low cost system has to be developed, which utilizes CMOS technologies, instead of other high performance high cost material. Additionally, a fully integrated small form-factor system will also reduce packaging cost and enhance reliability. Thus, this fully integrated system brings up the necessity of integrating all the interfacing circuitries, such as bias circuits, voltage regulator and DAC, instead of mounting different separated components on a PCB, which introduces other mechanical and electrical issues that degenerate the system.

However, there is no computer aid (CAD) tool available today that can simulate front-end circuit and baseband circuit accurately operating at EHF. As a result, front-end circuit modeling is important for this 60 GHz millimeter wave CMOS technology design.

CHAPTER 2

POWER AMPLIFIER AND MIXER

2.1 Introduction

The power amplifier (PA) is a key element in every communication device. Its main purpose is to amplifier the signal and be able to drive certain loads at the same time. Most of the elements in a simple direct conversion topology, such as filters and mixers, usually inherit loss due to their passive nature. Although active mixers and filters are implemented in some cases, they generally do not provide the necessary gain and driving capability to the load. For heterodyne or super-heterodyne architectures, the gain can be somewhat increased between different conversion stages; however, the front-end mixer will become the limiting factor. On one hand, active mixer can provide gain or less conversion loss. On the other hand, it has its own 1dB compression point. Thus, gain cannot be significant increased before the front-end mixer. As a result, PA is necessary for any communication electronic design topology. Additionally, a front-end mixer should be designed along with PA because it operates at the same frequency as PA and defines the necessary gain level or output power for the baseband or intermediate frequency (IF) blocks.

Due to the constraint of interference, FCC specifically assigns certain bandwidth of frequency spectrum to certain applications. As wireless technology keeps advancing, the frequency spectrum is crowded. As a result, a higher frequency of operation is sought. This trend opens a new field of microwave engineering, which is based on electromagnetic theory, for RF front-end design.

2.2 Basic Concepts for EHF Front-End Design

Maxwell's equation built the foundation of electromagnetic theory. His equations were developed and evolved into different forms that were used for different applications, such as physics and engineering. These equations view current and voltage as a form of wave. This behavior is not realized in lower frequency range applications, such as ultra high frequency (UHF), which is defined as 300MHz to 3GHz. It is because interconnection length usually is not long enough to experience this effect while radio frequency (RF) engineer trying to minimize the loss using short wire. This waveform behavior of current and voltage in interconnects or transmission lines leads to a non-uniform distribution of impedance as stated in transmission lines theory. Each small segment of transmission line can be represented in Figure 2.1, where R, L, G and C represent resistance, inductance, conductance and capacitance respectively, and z represents any location of a wire at a given time, t.

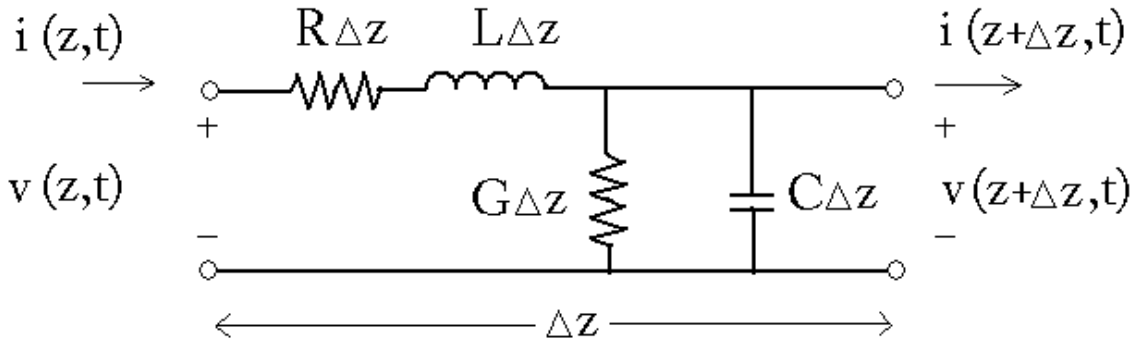

Figure 2.1. Lump components representation of a segment of wire.

With this model, a wave like behavior of current and voltage can be derived with wavelength of

$$\lambda = \frac{2\pi}{\omega\sqrt{LC}} \tag{1}$$

and a phase velocity of

$$\upsilon_p = \frac{1}{\sqrt{LC}} \tag{2}$$

This phenomenon can be illustrated along a transmission line rather than a small segment. Figure 2.2 indicates the current, voltage and impedance along an interconnection that is open-circuited.

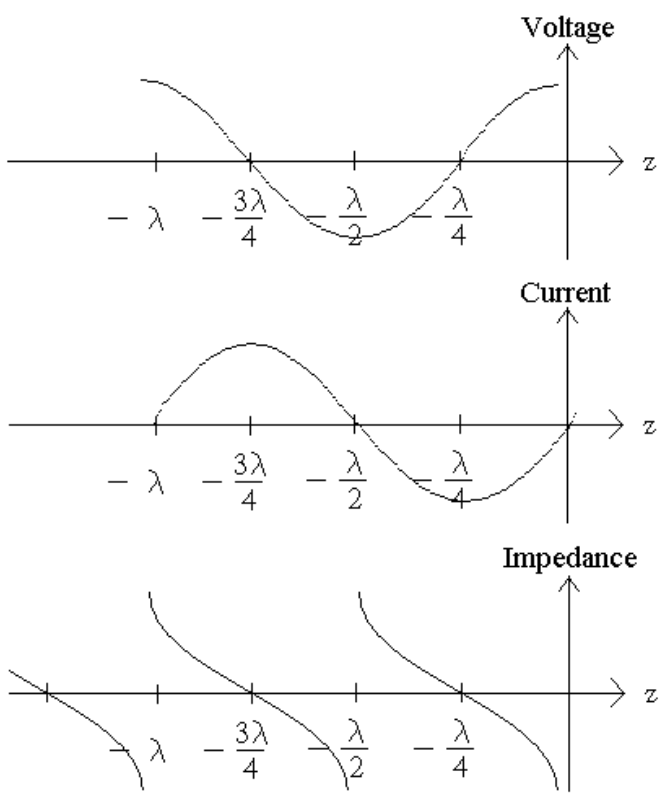

Figure 2.2. Voltage, current and impedance waveform along an open-circuited transmission line.

This model establishes the fundamental of transmission line behavior in this application operating at extremely high frequency (EHF) domain. It is crucial for front-end circuit design. Every wire dimension has to be precisely defined in order to ensure the circuits operate in the desired condition.

In order to maximize power transfer, impedance of the load and the source has to be the same or matched. As indicated in transmission line theory, the impedance is varying along an interconnection. Thus, a matching network is specifically designed to transform the impedance to desired value. Additionally, a matched circuit also enhances signal-to-noise ratio (SNR) and decreases amplitude and phase error [8]. In case of the PA, it is usually matched with 50 Ω at the output. This value is particularly chosen because 33 Ω is the optimal value for power transfer, and 75 Ω is the optimal value for minimum distortion. Thus, industries standardize most of the measurement and interface equipments with an intermediate value, 50 Ω.

Once a circuit is matched, the power or signal reflected back to the source from the load will be minimized. Scattering parameter (s-parameter) is specifically used for this application. It defines the power level that is transferred from one port to another or reflection from its own port. In other words, it can be used to characterize gain and return loss. With additional mathematical manipulation, it can also be used to acquire voltage standing wave ratio (VSWR), reflection coefficient, stability and other important parameters. As a result, EHF measurement usually is done in the form of s-parameter. Additionally, this technique will also be used for modeling, instead of normal small or large signal modeling.

As an example, a PA can be treated as a two-port network, as illustrated in Figure 2.3. Both input and output of the PA are terminated with 50Ω. S-parameter S11 represents the power incident on port one and reflected back to port one. S22 stands for the power incident on port two and reflected back to port two. These two parameters can be used to characterize input and output return loss. S21, on the other hand, shows the power transfer characteristic of power incident at port one while transmitting at port two. Subsequently, these parameters will be the main focus for transistor modeling.

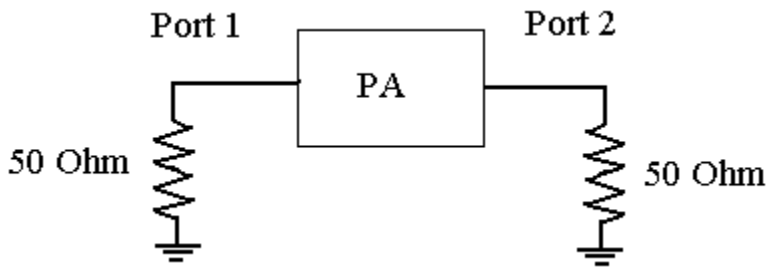

Figure 2.3. Two-port model of a PA.

This port model is not limited to two ports. In the case of a mixer that has differential local oscillator (LO) inputs, differential IF inputs and a RF output, it can have as many as five ports depending on the topology and application.

The matching networks within the circuits also partially serve as interconnections, such as power supply and inter-stage connections. These matching network designs using transmission line usually are implemented in terms of a waveguide. The most common types of waveguides are rectangular, circular and planar. In terms of fabrication aspects, rectangular and circular waveguides are physically impossible due to geometries and sizes. Thus, planar waveguide will be the main focus for the RF front-end layout.

2.3 Power Amplifier Topology Overview

In EHF domain, where millimeter wave circuits have to be used, any signal that is sent through two circuits or separated into two signals is implemented as a coupler or divider. These passive components theoretically will inherit a 3dBm power loss. This technique is widely used in some advance power amplifier operating with lower frequency band. For example, a Doherty amplifier generally boosts output P1dB and is able to output higher power; however, this design usually has a poor gain. With a divider and coupler at the input and output of the amplifier, the power gain will suffer significantly. This aspect is especially important for CMOS design relative to other processes. As a result, main focus is placed on the gain with reasonable P1dB rather than power added efficiency (PAE).

A class A common source amplifier is used as the power stage of the PA. A single transistor has to be used in order to provide the best linearity with the highest achievable P1dB without any boosting techniques. The last stage of the PA consists of a single 60um×0.1um transistor optimally chosen for its 50 Ω driving capability and gain. It consumes about 54mW from 1.5V supply voltage. The first stage employs a cascode structure that provides most of the gain from 1.8V supply voltage. The driver stage is situated between the cascode stage and power stage of the amplifier with 40um×0.1um in size and requires a 1.5V power supply. The design used for modeling is provided in [9] as shown in Figure 2.4.

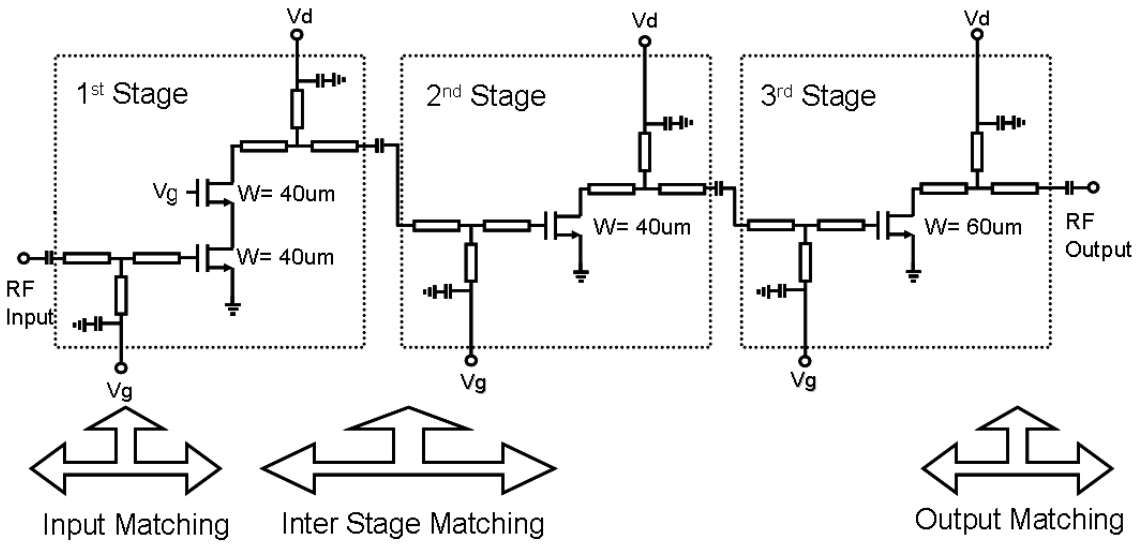

Figure 2.4. 60 GHz PA design schematic [9].

Instead of common inter-stage matching techniques, such as load-pull and source-pull that provide optimal gain, all of the matching network designs are matched with 50 Ω. The reason behind that is because of stability. Usually, as the gain increases, the stability factor decreases. As a result, optimal gain does not always guarantee a stable design without oscillation. Due to its marginal trade-off between stability and gain, 50 Ω matching throughout the design is chosen.

In this design, the PA achieves a gain of 17dB with a P1dB of 5dBm [9]. All of the design procedures are based on measurement result and frequency domain simulator, *ADS*. On the other hand, the layout of the PA, which *ADS* doesn't provide transistor layout model, has to be done in *Cadence*. Furthermore, *Cadence* can also achieve time domain simulation, where PA modeling will be necessary.

2.4 Mixer Topology Overview

Mixers have been used for many years. Most of them were designed using GaAs due to the performance, in terms of less conversion loss and high speed. A mixer can be designed as simple as a single transistor or diode, but this type of mixer requires filters in order to generate a desirable result. Figure 2.5 indicates the output signal frequency spectrum of the mixer. Eventually, only $RF_{desired}$ should remain after filtering.

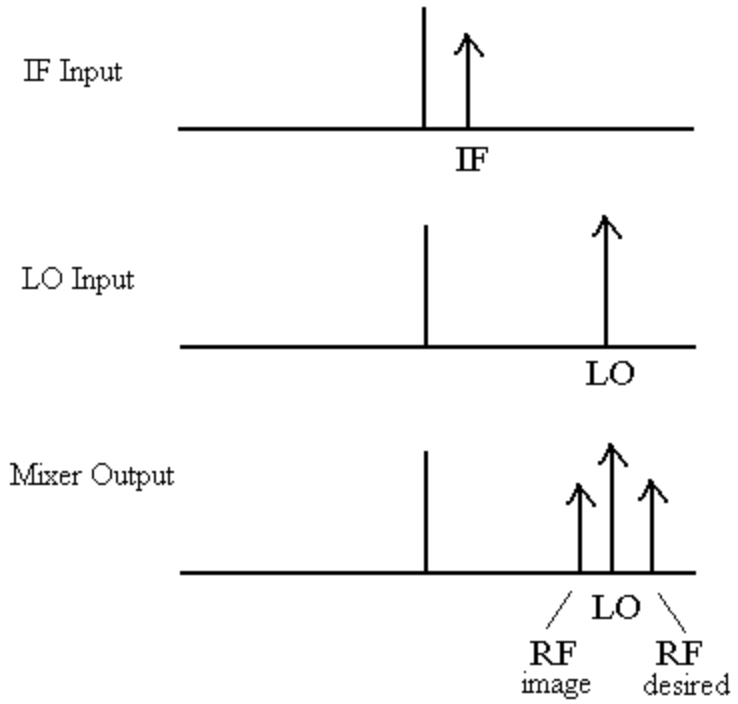

Figure 2.5. Mixer frequency input and output spectrum.

In this application, the frequency of the LO and RF_{image} is extremely close to $RF_{desired}$. Unless a very high quality and high-order filter is used, the LO and RF_{image} signal will also be amplified by the proceeding PA stage.

One of the attractive attributes of millimeter wave design is that matching networks can also act as a filter. Matching network can be specifically tuned for certain bandwidth with the trade-off of reduced gain. Although RF_{image} is significantly degenerated by the matching network, LO signal is still very close to $RF_{desired}$, which is 864 MHz for this application. As a result, LO rejection topology should be deployed. The most common LO rejection architecture is double balance structure, such as Gilbert cell mixer. Additionally, image and LO rejection topology can also be implemented together; however, it is not recommended. The reason is because an image and LO rejection mixer requires additional mixers with a lot of hybrids or phase shifters. These components will significantly increase conversion loss. In addition, a slight 5° mismatched for the hybrids, which is common in EHF design, will cause the frequency rejection scheme to be ineffective. Hence, a simple mixer with LO rejection feature should be the most efficient solution for this application.

On the other hand, the conversion loss is expected to be large for passive mixers because active mixer experience conversion loss instead of gain at 60 GHz. This behavior is mainly due to the frequency dependency of transistor, which is limited by parasitic inductance, capacitance and resistance.

Thus, a simple single gate mixer topology is utilized. The design [10] is shown in Figure 2.6. It employs only a single 40um×0.1um NMOS transistor, which is optimally chosen to minimize conversion loss. This simple mixer inherits a low power consumption feature. Additionally, the open-stub matching network at the IF input port also improves stability and provides LO rejection. Thus, this LO rejection scheme with the use of matching network filters, RF_{image} and LO will be significantly degenerated.

Similar to PA design, matching network designs are based on measurement result and *ADS* simulation. However, unlike PA linear nature, which the performance can be estimated by its gain and P1dB, mixer is a crucial component that interacts with VCO and baseband circuit. In order to verify a correct frequency mixing scheme, time domain simulation must be performed. Thus, the *Cadence*-based model has to be developed for the simulation.

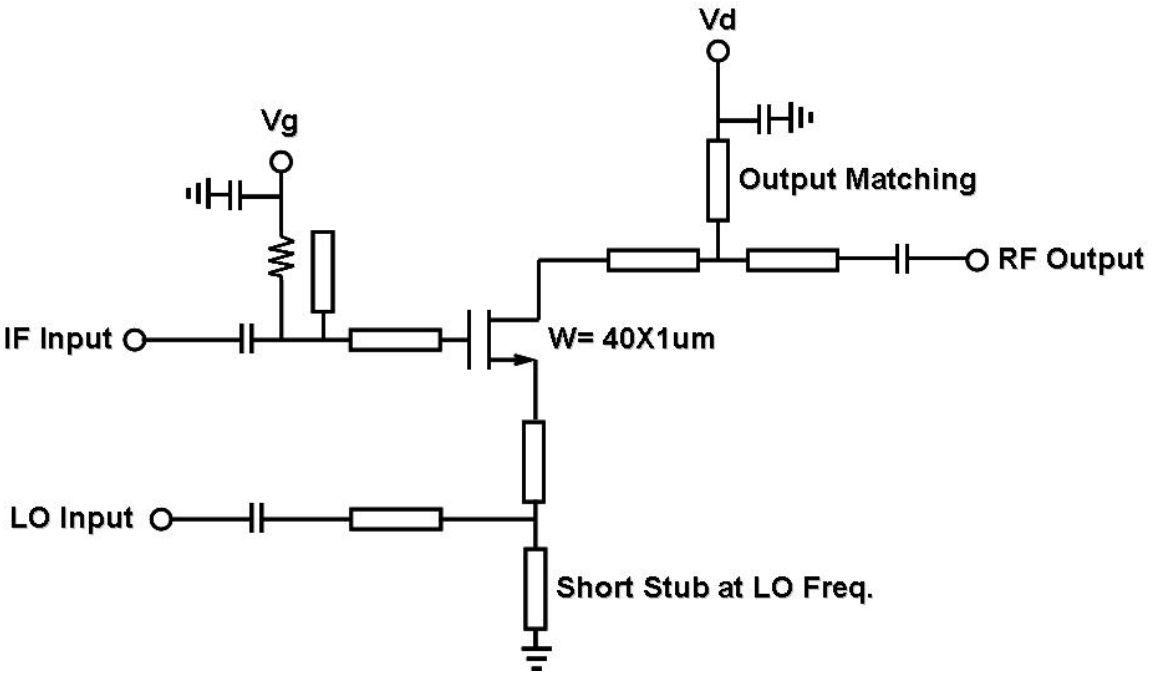

Figure 2.6. 60 GHz mixer design schematic [10].

2.5 Modeling Result and Comparison

All of the EHF designs are based on frequency domain platform, *ADS*. It provides accurate frequency domain simulation result in terms of gain and return loss through s-parameter analysis. Additionally, this simulator can also import measurement data with respect to frequency in the design. Thus, it is a reliable simulator for matching network design.

However, this imported data can only provide frequency response for an unmatched transistor during measurement. It does not offer any indication or analysis beyond its frequency response. As a result, it is not reliable for time domain simulation. Hence, a high frequency specific model has to be developed through the modification of a transistor in other simulation platform.

Cadence is a widely used time domain simulator. It does not only offer RF layout capability for EHF design, but it also offers an accurate low frequency and DC response transistor model. As a result, it provides a perfect system level simulation environment for baseband digital circuits accompanied with RF front-end circuit.

As mentioned, transistor measurement has to be done prior to any data import into *ADS* for matching network design. This measurement result, at the same time, provides a valuable data for transistor level modeling. The modeling technique is based on s-parameter two-port model. Using transistor model in *Cadence* as base, DC and EHF response matching is possible.

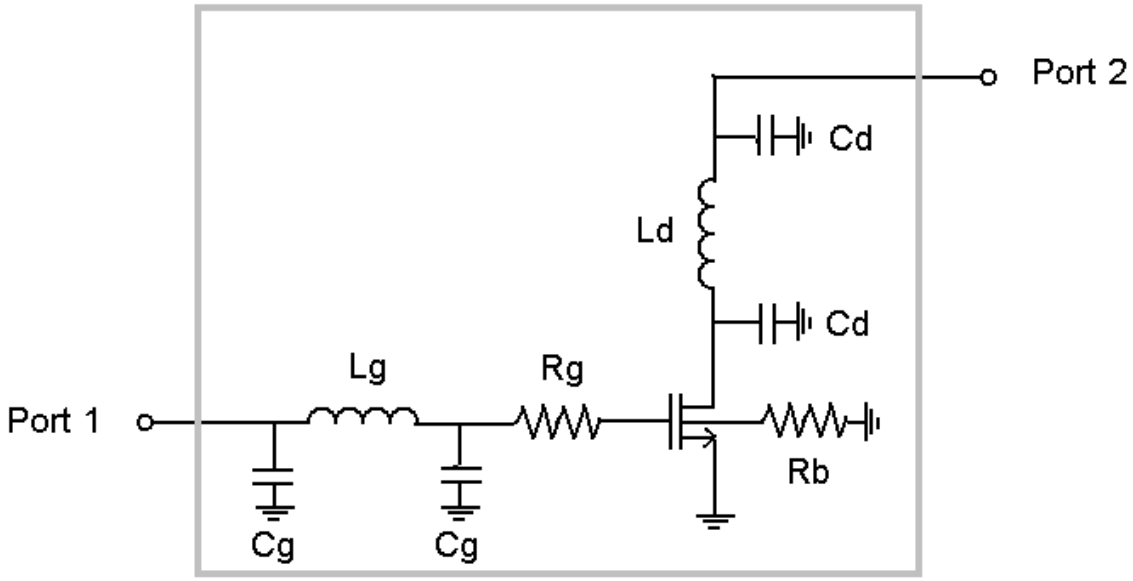

Figure 2.7. Parasitic model for a single transistor.

In the EHF domain, electrical performance is mainly affected by parasitic capacitance, inductance and resistance similar to transmission line theory. Although physically it is different from a transmission line, such as dielectric capacitance between substrate and transmission line instead of gate-to-source capacitance in NMOS device, its behavior essentially is the same. Figure 2.7 shows the parasitic model used for a single transistor model. Two capacitors, Cg, are added to increase parasitic capacitance that the model originally has in EHF domain. Similar to Miller capacitance, these capacitors impose an increase in the gate-to-source capacitance. Additionally, the ground ring surrounding the transistor also contributes partially. The capacitors are identical in order to ensure the parasitic elements are evenly distributed. In order words, the left side and right side of the parasitic network alone should experience the same reactance. Similar network, Cd, is added to the drain of the NMOS. Additionally, inductors, Lg and Ld, are deployed due to electrical behavior. In other words, every interconnection has a small

inductance associated with it as indicated in transmission line theory. Physically, this interconnection represents the waveguide feeding taper to the gate and drain of the NMOS as illustrated in Figure 2.8.

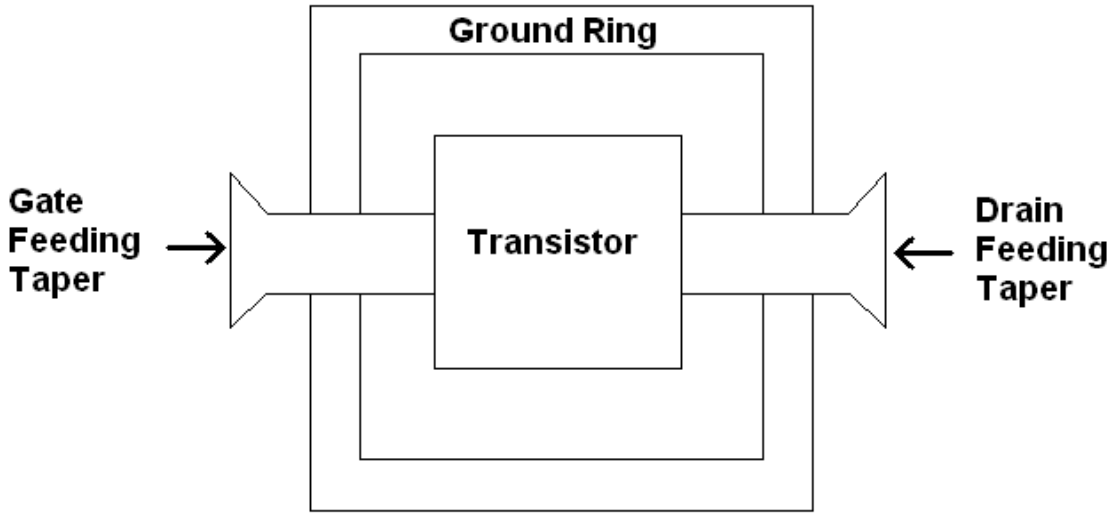

Figure 2.8. RF NMOS transistor layout structure.

Different than the drain parasitic network, an extra resistance, Rg, is purposely added only to the gate of the transistor. The reason is that the gate of NMOS is not electrically conducted, except a small gate oxide leakage current. Thus, it doesn't alter the original *Cadence* DC model, while matching the impedance that the AC signal experience at high frequency. This resistance is usually noted as gate spreading resistance, which is especially crucial for low noise amplifier design. The resistance, Rb, at the bulk is more intuitive that it increases the bulk resistance of normal small signal model without affecting any DC performance. For physical interpretation, this resistance exists laterally between the depletion region and the substrate.

Figure 2.9 to 2.12 graphically indicates the simulation result for the 40um×0.1um NMOS transistor in terms of s-parameters in a two-port model from 40 MHz to 65 GHz.

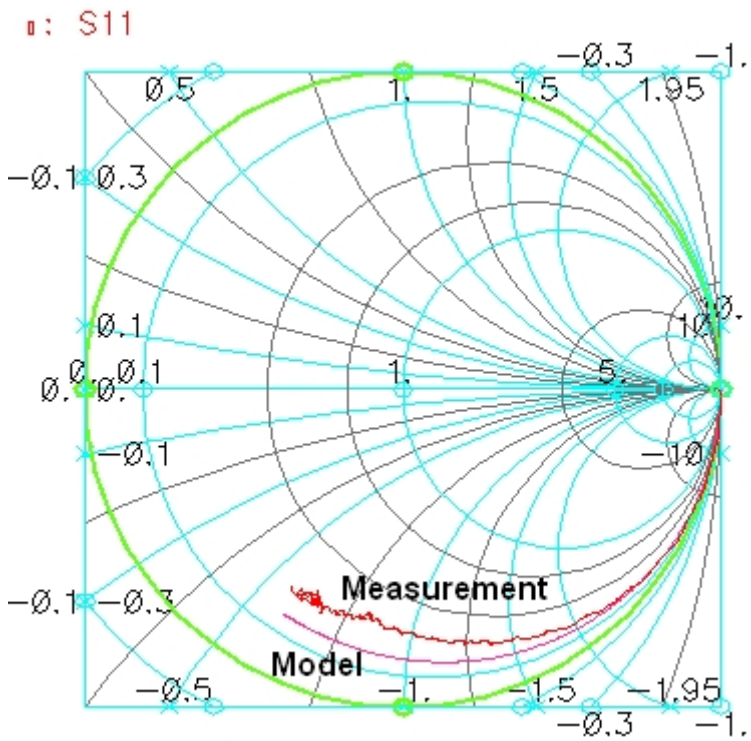

Figure 2.9. S11 Smith chart representation for 40um×0.1um NMOS transistor.

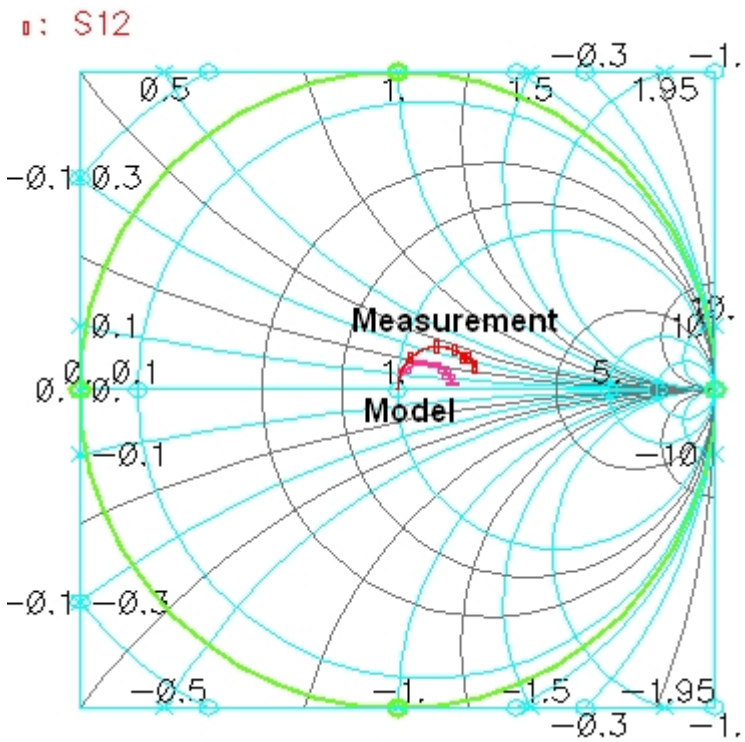

Figure 2.10. S12 Smith chart representation for 40um×0.1um NMOS transistor.

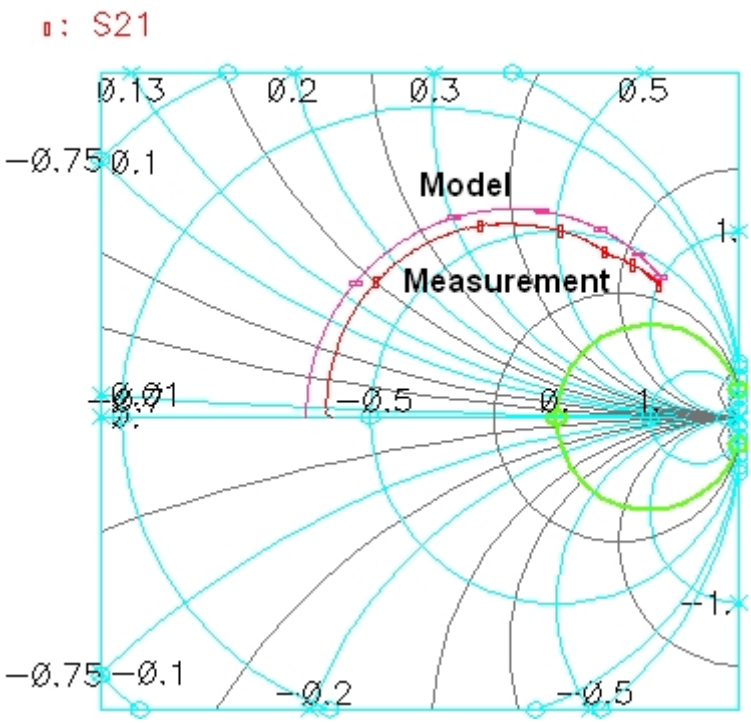

Figure 2.11. S21 Smith chart representation for 40um×0.1um NMOS transistor.

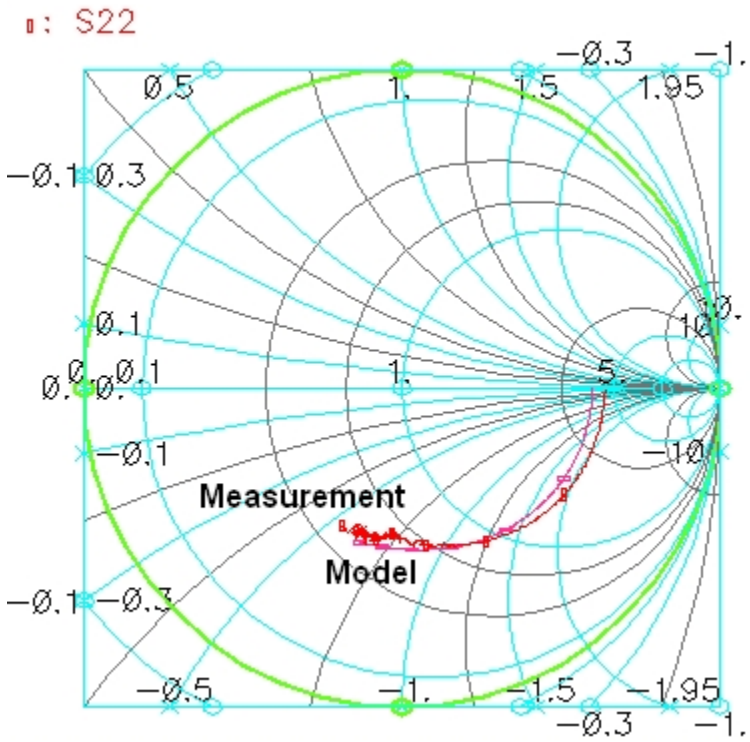

Figure 2.12. S22 Smith chart representation for 40um×0.1um NMOS transistor.

As intended, the focus is placed on S11, S21 and S22. S12 is the signal transfer from the output, port 2, back to the input, port 1. Although it characterizes the isolation quality, it only offers negligible result in the overall design. In other words, once the inter-stage, input and output impedance are matched with desired level, the reflected signal from the output is very small. This small reflection is further attenuated with each stage S12, which will fall into the range of less than -30 dB. This small signal level is not critical in transmitter front-end design; however, caution has to be placed in low noise amplifier design of the receiver front-end. As shown in the result, the single transistor model matched with the measurement in the order of less than 3dB for magnitude and 5° in phase shifted at 60 GHz.

Figure 2.13 to 2.16 graphically indicates the simulation result for the 60um×0.1um NMOS transistor in terms of s-parameters in a two ports model from 60 MHz to 65 GHz.

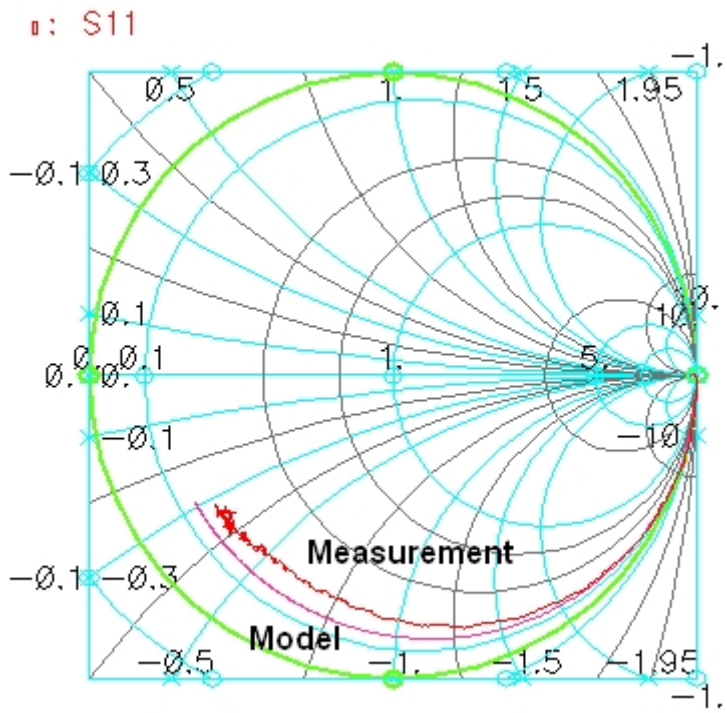

Figure 2.13. S11 Smith chart representation for 60um×0.1um NMOS transistor.

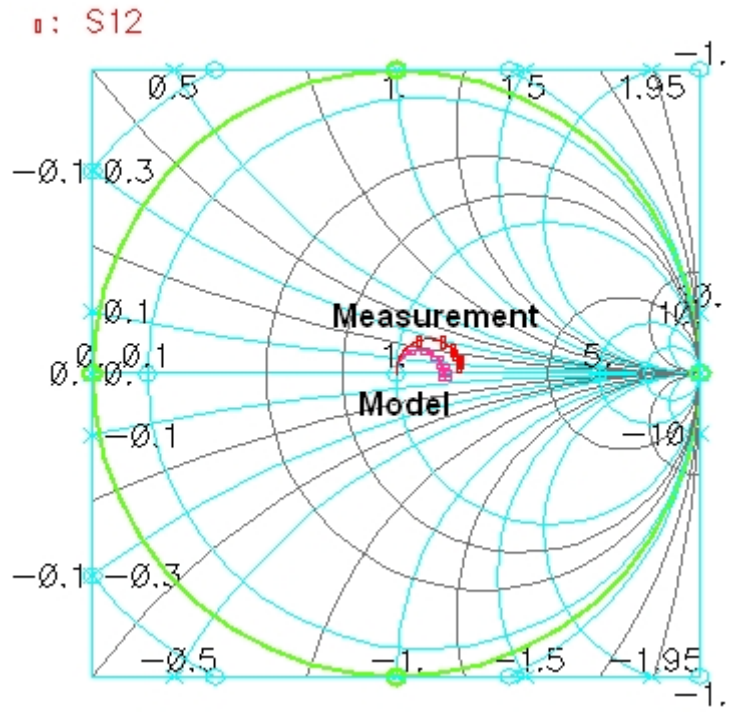

Figure 2.14. S12 Smith chart representation for 60um×0.1um NMOS transistor.

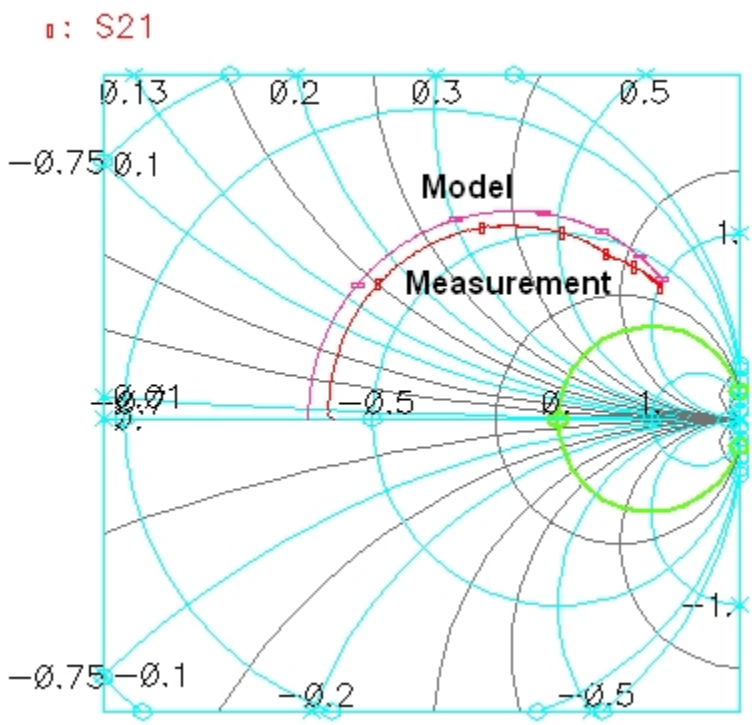

Figure 2.15. S21 Smith chart representation for 60um×0.1um NMOS transistor.

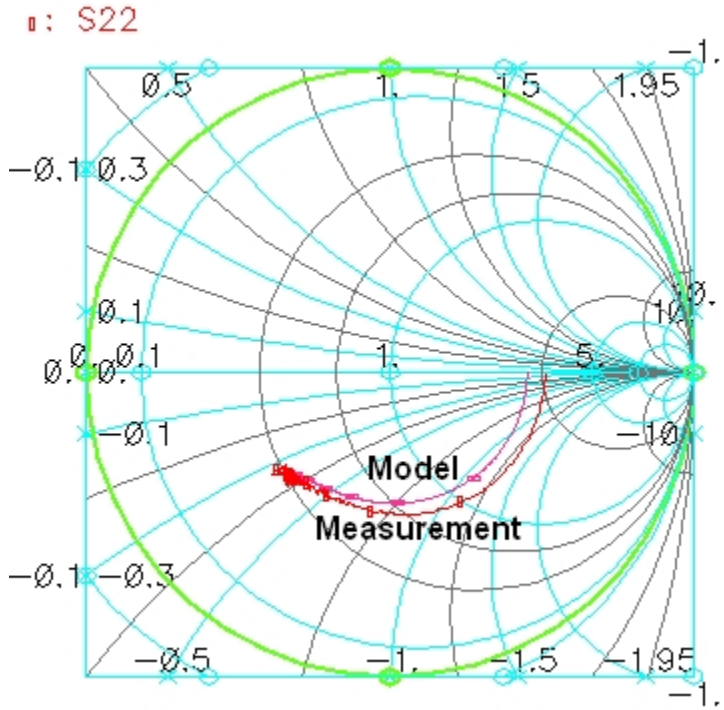

Figure 2.16. S22 Smith chart representation for 60um×0.1um NMOS transistor.

Same as the 40um×0.1um NMOS modeling, the concentration is placed on S11, S21 and S22. As shown in the result, the single transistor model matched with the measurement in the order of less than 3dB for magnitude and 5° in phase shifted at 60 GHz. In addition, all the Smith chart plots demonstrate the frequency response trend is similar between the model and measurement result. Thus, this method is proven to be feasible in any size of transistor modeling.

The remaining modeling required is the PA first stage cascode structure. All of these transistors are composed of 40um×0.1um NMOS. Ideally, similar modeling procedures should be conducted; however, a stacked 40um×0.1um NMOS can also provide a reasonable result without further modeling. In other words, the parasitic networks are left in intact, while the drain is simply connected to the source of another same dimension device. This assumption is only valid when the resistance between the

drain and source of the device is negligibly small, which can be manipulated in a device layout.

After each separate stage of the PA and mixer is modeled, it is connected together with *Cadence* build-in transmission line model, MTLine, which is similar to *ADS* transmission line model. Parameters can be easily calculated and imported to MTLine instead of substrate information in *ADS* platform. Simulation is run and compared with measurement result as illustrated from Figure 2.17 to 2.20, where marker A indicates the measurement result with marker B showing the model result. Additionally, Figure 2.21 to 2.23 indicates the PA power performance.

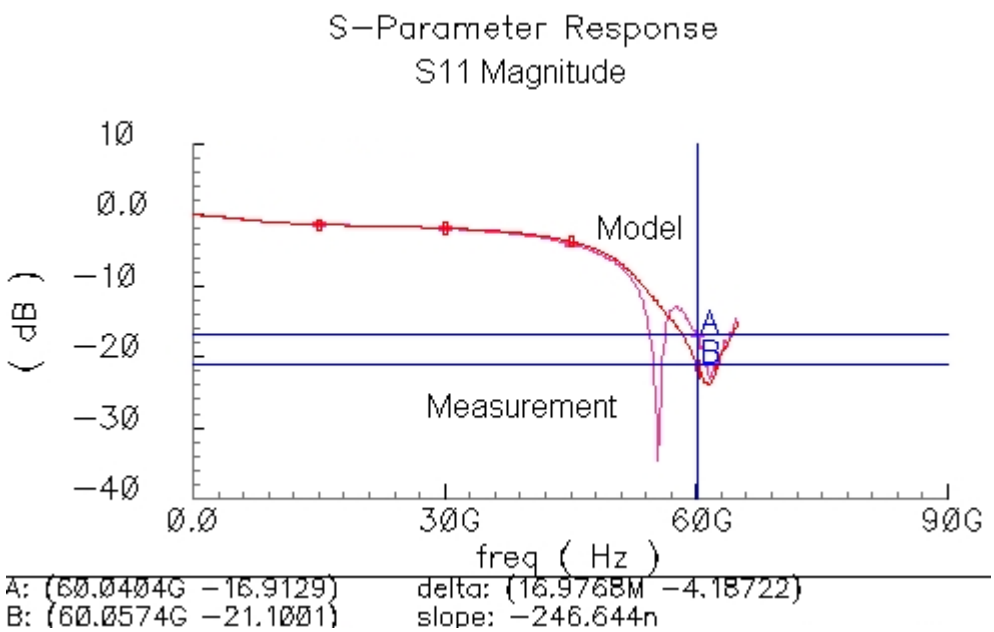

Figure 2.17. S11 magnitude frequency response for the PA.

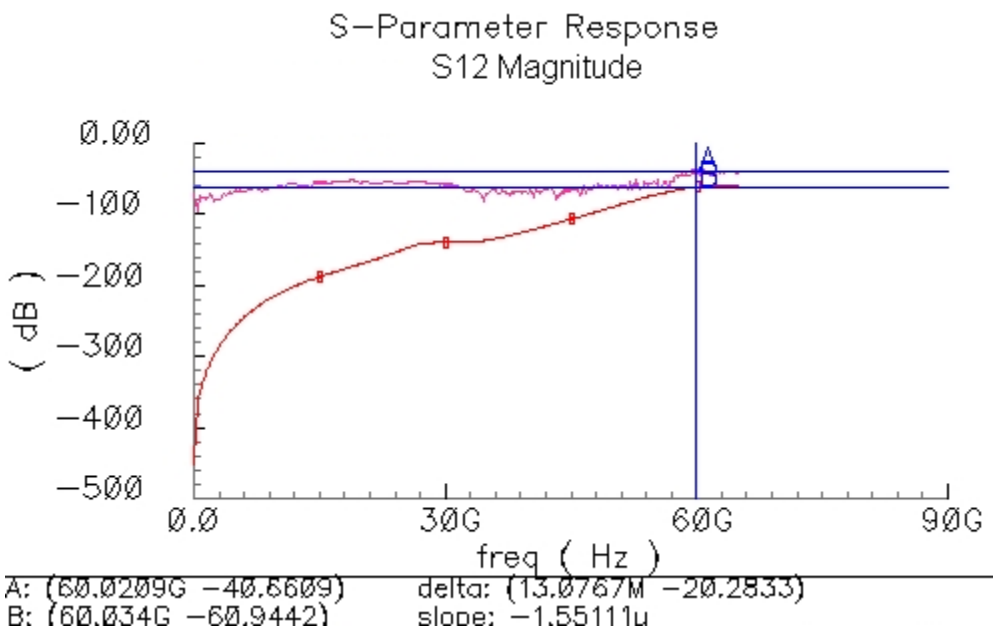

Figure 2.18. S12 magnitude frequency response for the PA.

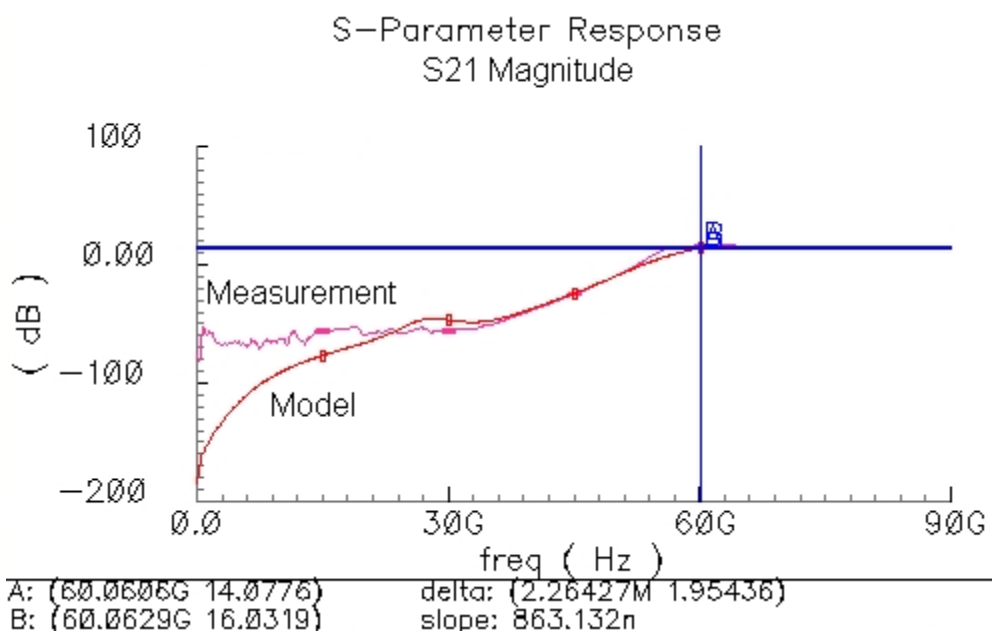

Figure 2.19. S21 magnitude frequency response for the PA.

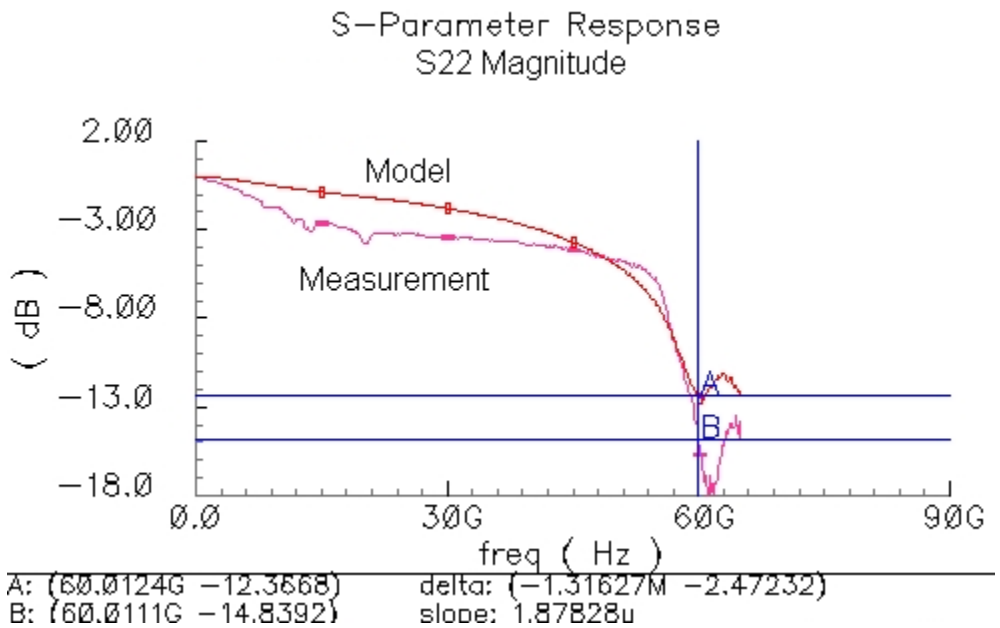

Figure 2.20. S22 magnitude frequency response for the PA.

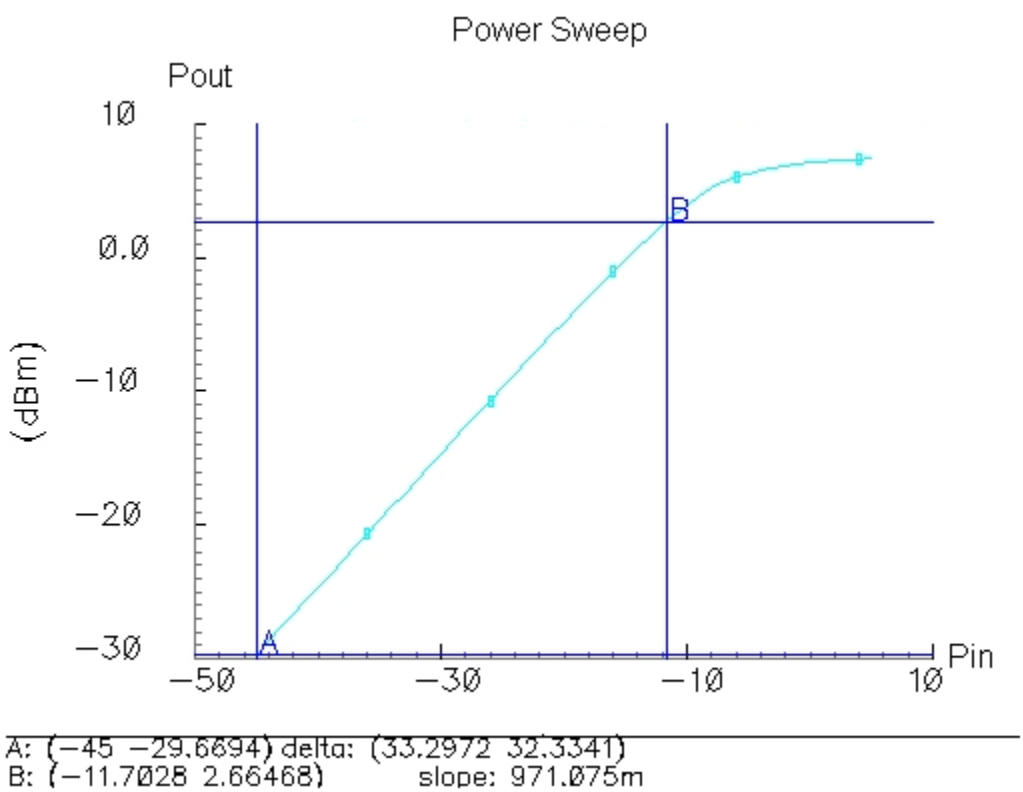

Figure 2.21. Power sweep simulation of the PA showing an output P1dB of 2.66dBm.

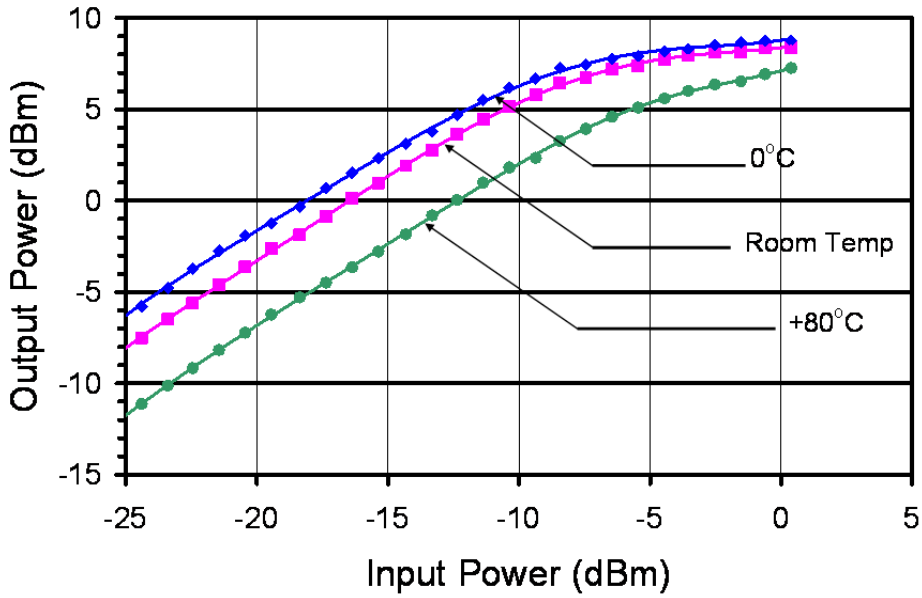

Figure 2.22. Power sweep measurement of the PA showing an output P1dB of 5dBm (use with the courtesy from Dr. Debasis Dawn, GEDC).

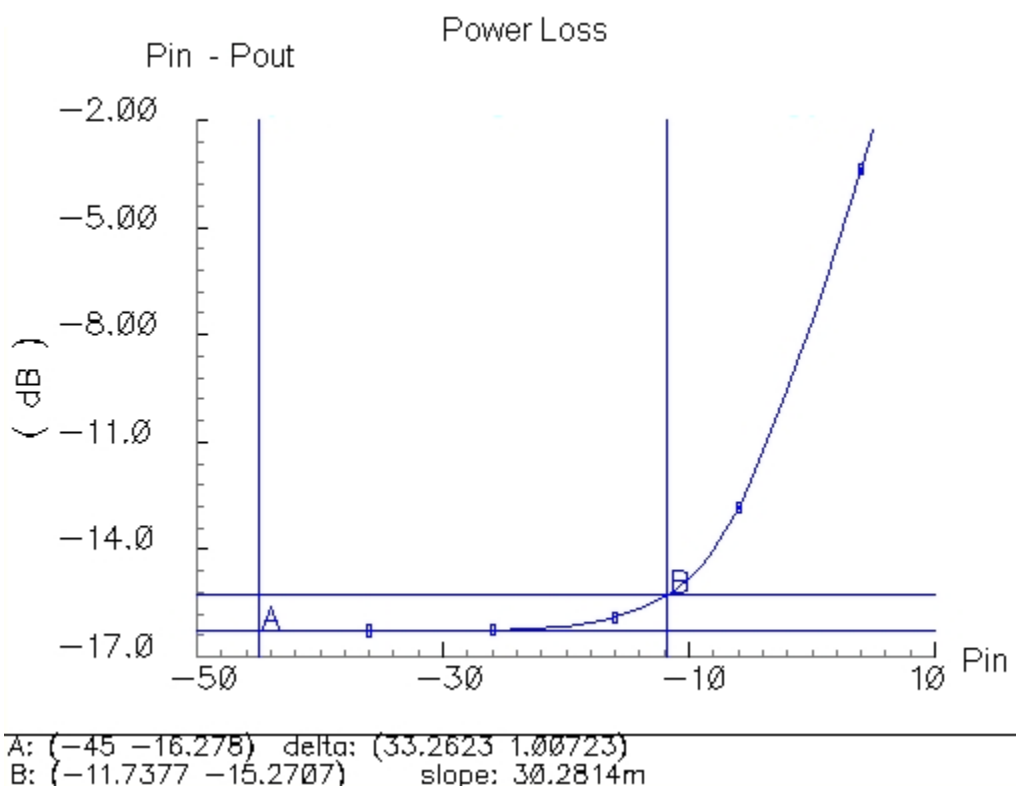

Figure 2.23. Power sweep simulation of the PA showing power gain of 16.28dB.

Table 2.1. PA measurement and model result comparison at 60 GHz

	Measurement	Model	Absolute Error
S11 (dB)	-16.91	-21.10	-4.19
S12 (dB)	-40.66	-60.94	-20.28
S21 (dB)	14.07	16.03	+1.13
S22 (dB)	-12.37	-14.84	-2.47
P1dB (dBm)	5	2.66	-2.34
Gain (dB)	17	16.28	-0.72

Table 2.1 summarizes the PA performance at 60GHz. As predicted, S12 value from the actual measurement is in the range of less than -30dB. As a result, the signal deviation is extremely small when it is converted back to normal scale from dB. Thus, it is not efficient to fine tune this parameter while degrading other s-parameters from modeling. Due to the stacked model in the first cascode stage of the PA, S11 is deviated from the measurement result for more than 3dB, which is more than any absolute error in single transistor modeling. However, the result is still reasonable. As shown in overall design power performance, P1dB and power gain are remained within 3dB absolute error boundary between the measurement and the model.

This transistor modeling creates a very important framework for time domain and system level simulation. It can be further proven with the mixer performance. Figure 2.24 illustrates the output spectrum of the whole transmitter chain simulation without the PA and PLL. Since the PLL is not in place, the VCO experiences a slight shift in frequency; however, the resulting modulated frequency is still within the application bandwidth. Hence, this powerful modeling technique can be applied to not only component level simulation, but also system level simulation.

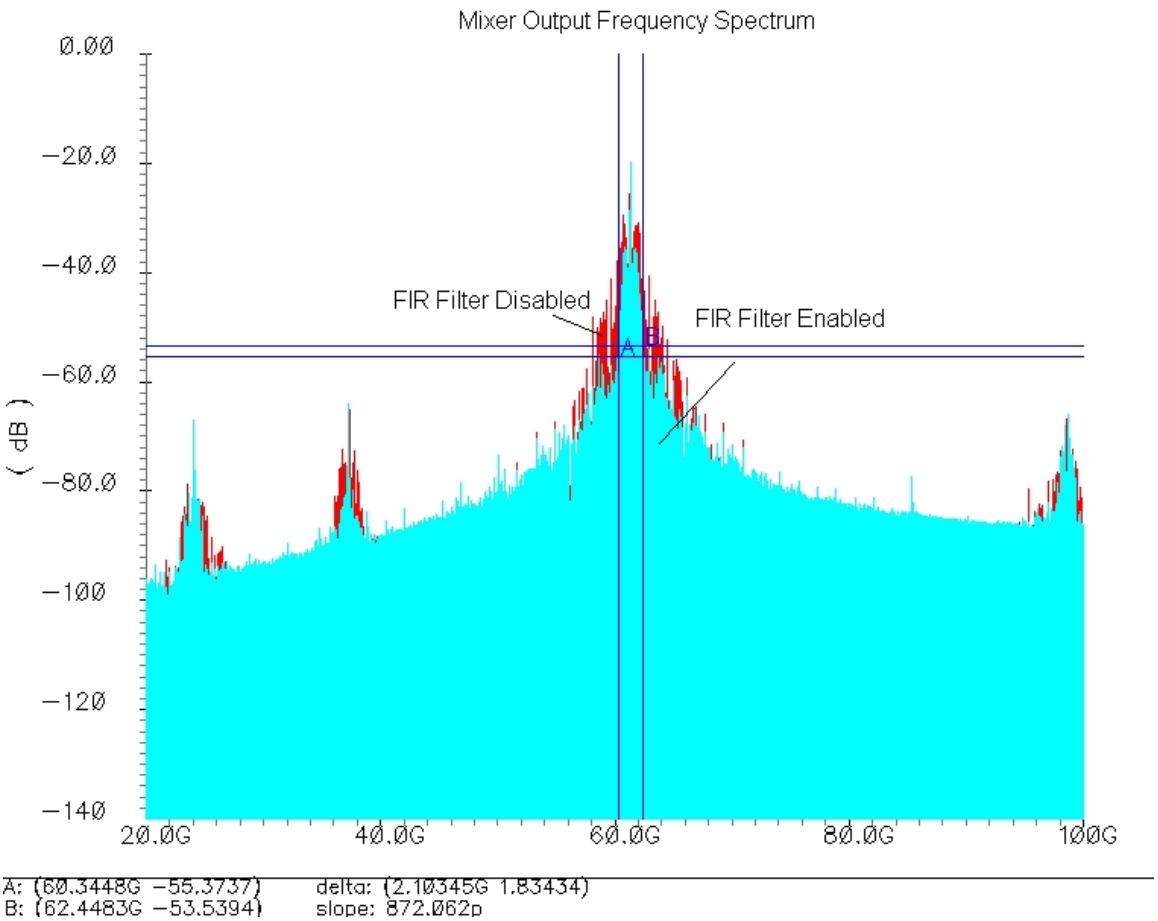

Figure 2.24. Mixer output spectrum with the whole transmitter system chain simulation excluding PA and PLL.

2.6 Layout Strategy

Unlike commercialized standalone components, RF front-end layout has to be compatible with the whole SOC. It is especially important because a lot of constraints are imposed to millimeter wave layout that significantly affect electrical performance. The simplest restrictions are size and orientation. Figure 2.25 shows how the PA and mixer is situation within the OOK chip.

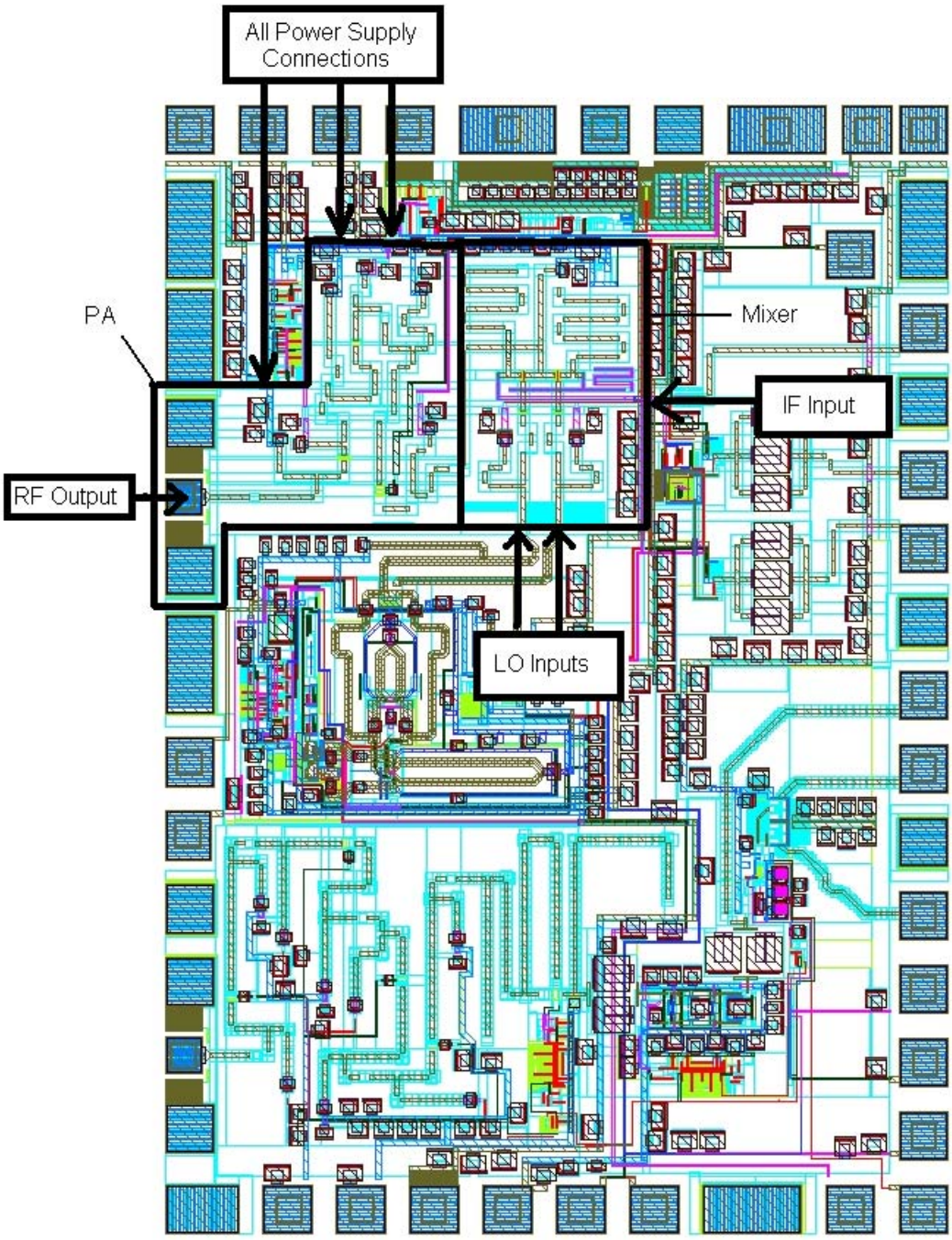

Figure 2.25. OOK chip *Cadence* layout with PA, mixer and all the external and internal connection ports indicated.

Similar to many communication SOC architectures, VCO is usually placed at the center of a chip. For example, heterodyne or super-heterodyne architecture may share the usage of VCO between transmitter and receiver. As a result, LO input feeding ports should be oriented to the center from the mixer. The RF output port from the PA is usually connected to the antenna, which should not have any other components obstructing or interfering with transmission. As a result, there should not be any signal process circuits or external connections, except antenna, resign on the side of RF output pad. In order to evenly distribute an IC mechanical strength, width to length ratio should not be too long. As a result, the power supply should situate on the top side of the PA while minimizing voltage level drop due to wire resistance in case of this chip. Thus, the remaining side will be used as the IF input port for the mixer.

The rules imposed on the simple orientation or integration scheme are mainly due to the use of waveguide for front-end circuits. In order to minimize the area, a microstrip waveguide is chosen over coplanar waveguide. Additionally, it also complies with IC fabrication process. In general, microstrip waveguide consists of a planar transmission line with dielectric and ground plane underneath as shown in Figure 2.26.

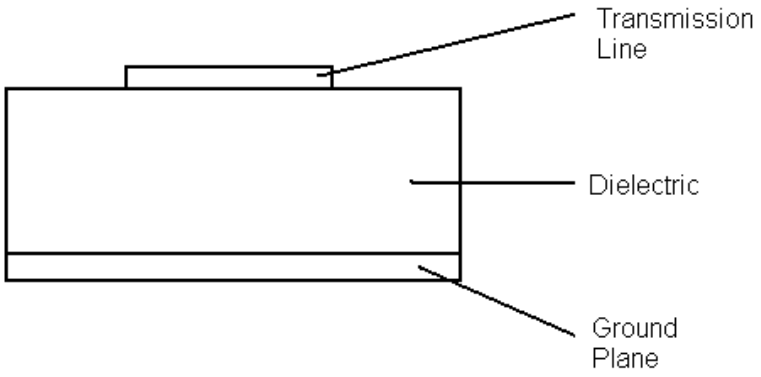

Figure 2.26. Simple microstrip waveguide cross section view.

The highest metal layer is usually used for transmission line, and the lowest metal layer is utilized as ground plane. As a result, the distance between the transmission line and ground plane is maximized, and the distributed capacitance, which affects the electrical performance of high frequency circuit, in transmission line model is minimized. Due to this reason, there should not be any wire going below a transmission line that will create unnecessary capacitance and interference. Thus, the number of inputs and outputs to the front-end circuit is limited.

With the same phenomenon, the transmission lines should not be placed too close to each other. This interference or coupling effect is often called crosstalk, which causes some of the signal propagated to the victim line. Meanwhile, transmission lines bending angle can also increase signal loss. As a result, a 45° angle is used for every waveguide turns, in addition to the 30um spacing between each line. Detailed mathematical analysis can be done towards crosstalk, using Sakurai's model or electromagnetic theory for calculating turn angle loss; however, it is not feasible to perform such calculation for a large structure, such as this communication system chip. *ADS* features momentum simulation, which takes into account of the electromagnetic effects. Using the above specification for transmission line layout, simulation is done for the PA as shown from Figure 2.27 to 2.30 with marker A positioned on the original design value while marker B situated on the momentum simulation result extracted from the actual layout at 60 GHz.

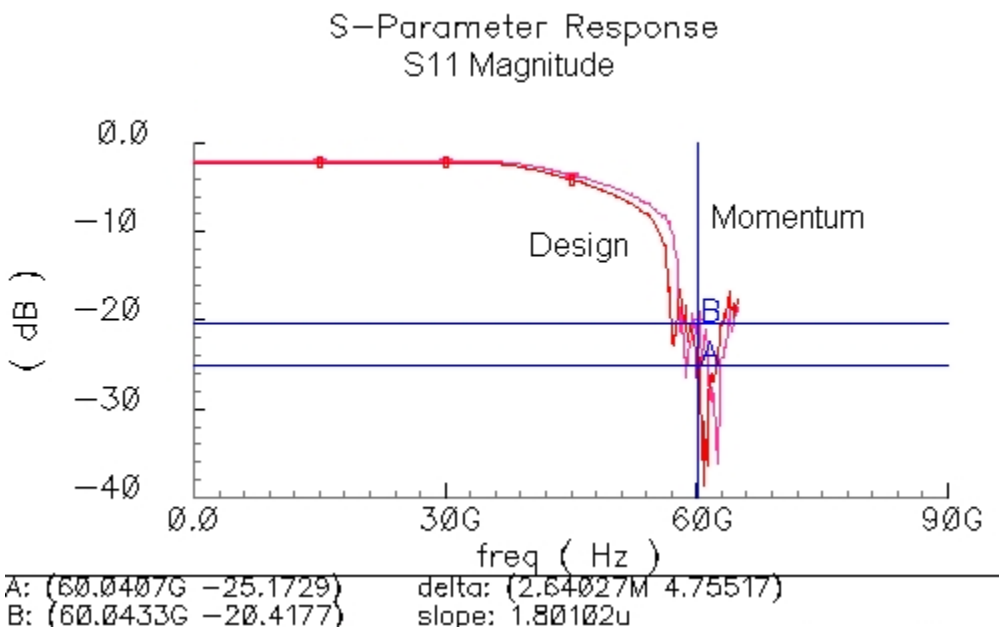

Figure 2.27. PA S11 response comparison between the original design and momentum simulation for the actual layout.

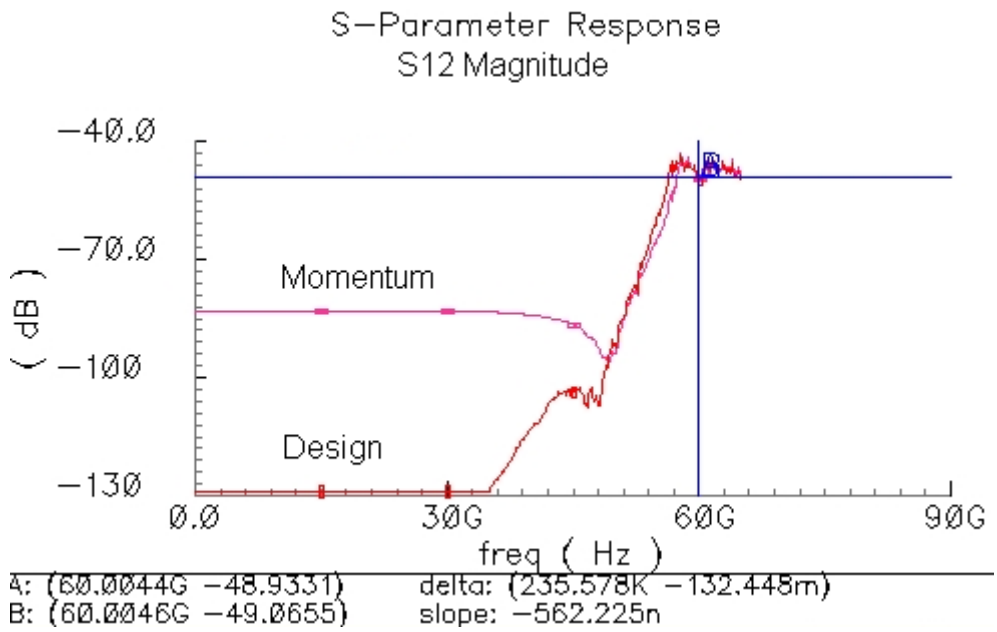

Figure 2.28. PA S12 response comparison between the original design and momentum simulation for the actual layout.

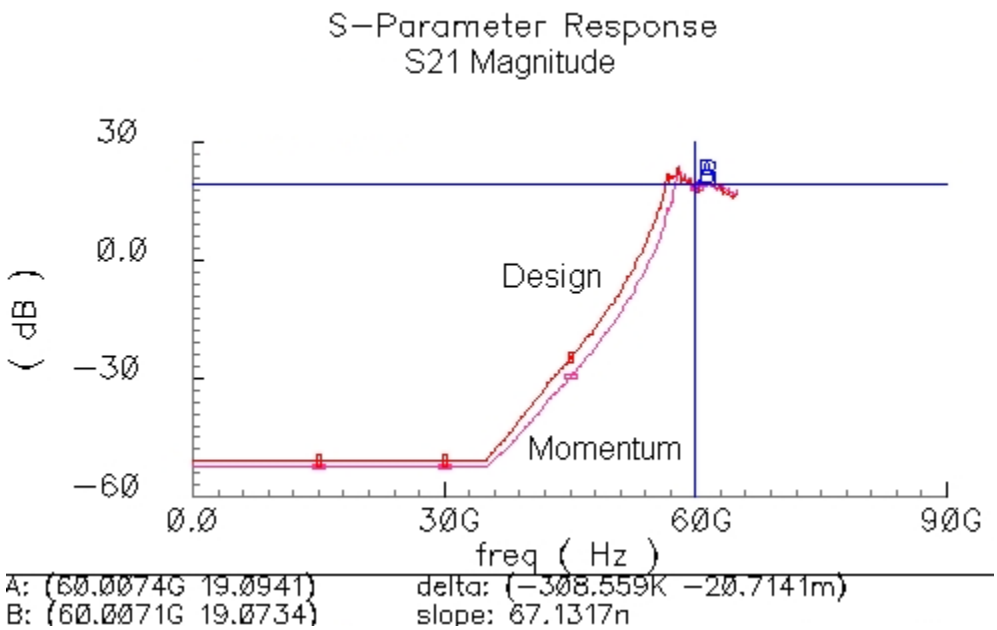

Figure 2.29. PA S21 response comparison between the original design and momentum simulation for the actual layout.

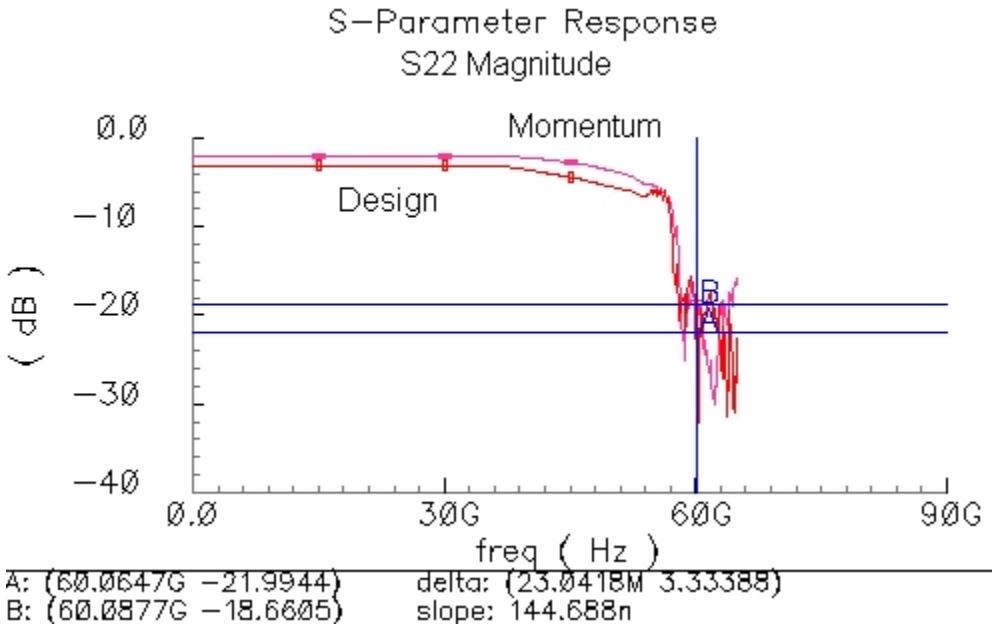

Figure 2.30. PA S22 response comparison between the original design and momentum simulation for the actual layout.

Table 2.2. PA original design and momentum simulation result at 60 GHz

	Design	Momentum	Absolute Error
S11 (dB)	-25.71	-20.42	+4.76
S12 (dB)	-48.93	-49.07	-0.13
S21 (dB)	19.09	19.07	-0.02
S22 (dB)	-21.99	-18.66	+3.33

At the frequency of operation, the result summarized in Table 2.4 clearly shows the electromagnetic effect between ideal design and physical implementation. More detailed investigation also indicates a slight shifted in the bandwidth and matching network performance. Another factor that is contributing to the error is the momentum simulation resolution. It is because the layout has to be imported from *Cadence* to *ADS* for momentum simulation; however, *ADS* does not support high resolution waveguide dimension, which may result in round-off error.

In addition to transmission line implementation, the ground plane is another critical aspect for microstrip structure. In most of the current fabrication process, it usually has a density limit for different metal layers. As a result, the ground plane cannot be fully covered with metal lines connected to ground. Hence, a simple ground plane pattern has to be developed that avoids maximum metal density issue and electromagnetic field induced to the substrate at the same time. This ground plane is not only situated underneath the transmission line, but also the entire chip. The advantage is that the ground plane will be connected to several locations of the ground pads, which are actually connected to signal ground. This ground plane distribution further reduces ground resistance, which may act as a degeneration resistance for most of the amplifiers within the chip.

2.7 Summary

Similar to current commercialized communication electronics, topology chosen is critical with respect to different applications. For EHF domain design, many advance techniques cannot be realized because of physical constraints. Minor details, such as transistor and wire dimension used in low operating frequency circuit design, become critical components for EHF design that eventually hinder proper operation. As demonstrated in PA electromagnetic simulation, the physical signal path does affect the performance to some extent.

As CMOS transistor feature size keeps reducing, high frequency applications are made possible. Thus, many CAD tools were developed to accommodate RF design. The two most common simulators used in industries are *Cadence* and *ADS*. *Cadence* offers advance features in physical layout and time domain simulation with some other basic frequency domain simulation functions while *ADS* provides a well-rounded frequency simulation. As a result, both of them have to be utilized in communication electronics design. In order to ensure bidirectional support, device modeling becomes a crucial step for keeping the integrity of transferring a design to another simulation platform.

The modeling technique proposed not only enables a system level time domain simulation, but also frequency domain simulation in *Cadence*, in case of a mixer. Thus, this technique provides a powerful tool for millimeter wave design that reduces design cycle and eventually the overall cost.

CHAPTER 3

VOLTAGE REGULATOR

3.1 Introduction

DC voltage regulators are widely used in every application, from low power IC level to high power generator level. Their sole purpose is to convert a single power supply voltage to another supply voltage level that consumes current. As indicated in fundamental physics, there is no energy conversion that can achieve 100 percent efficiency. Energy may be lost in the form of thermal energy or extra energy that is required for conversion. The same theory is applied to voltage regulators. Over the decades, power electronics have developed many topologies that improve efficiency or electrical performance; however, the obstacle remains on the physical component itself. For example, a simple power line ideally should transfer necessary voltage and current to the load, but the wire itself inherits some impedance. As a result, voltage at the load may not be the same as the source voltage because power is dissipated through the wire impedance. This kind of voltage drop is realized based on material and length. As a result, substations are usually set up to maintain a standard power level throughout a city. In IC level, wire sheet resistance becomes critical, where the width is around 10um for 90nm technology. For example, the PA power line feeding point for this OOK chip is situated very close to the power connection pad to minimize this voltage drop effect.

On the other hand, a voltage regulator also generates output voltage ripple [11]. This unavoidable ripple is produced during the conversion. In addition, if the load current consumption is varying, which is mostly the case in communication electronics,

the ripple amplitude will further increase. The reason is because the DC resistance along the wire remains the same while the current is varying. As Ohm's law indicated, the voltage at the load will also be changed. With years of development, techniques, such as decoupling capacitor or switch-mode converters, have been introduced to minimize these effects. However, in IC level, more constraints are usually in place, such as area and speed.

In terms of the OOK chip in this research, area is a crucial factor. As most of the IC regulators nowadays required a large capacitor and inductor to conserve power, these lump components are usually forced to be mounted outside of an IC. This is especially true for CMOS process where the quality factor for inductor is usually low. This attributes also translate to a high DC resistance. A simple pulse width modulation (PWM) control scheme voltage regulator having a 120mA rating has been designed with on-chip inductor during the process; however, 30% to 40% of the power is loss on the inductor. Meanwhile, the capacitor is placed off-chip because its size is comparable to the whole chip. Another attractive solution is linear voltage regulator, where all of the components are able to be placed on-chip [12], as shown in Figure 3.1.

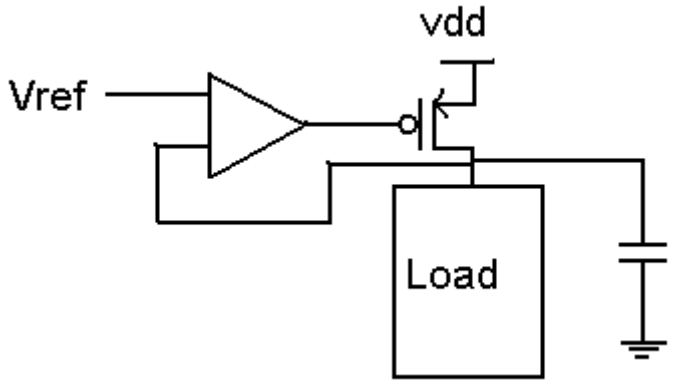

Figure 3.1. Simple linear voltage regulator.

This type of converter can only provide the efficiency limited by the voltage conversion level. In other words, in the case of the OOK chip, power supply voltage 1.8V is converted to 1V for the baseband digital circuits. Meanwhile, the current through the PMOS switch is the same as the current sourcing to the load. As a result, the efficiency is approximated as

$$\eta = \frac{V_{converted}}{V_{supply}} \tag{3}$$

Without considering any loss due to interconnections, the efficiency of the linear voltage regulator is 55%. Thus, switch-mode voltage regulator is the only solution.

A switch-mode voltage regulator is mainly divided into two parts. One is the regulator; another is the DC-DC converter. The most common converters are step-down (buck), step-up (boost), buck-boost, Cuk and full-bridge. Full bridge converters can provide bidirectional power transfer while Cuk can support step-up and step-down conversion. More advance converters, such as zero-voltage switching converters and zero-current switching converters, are also developed to reduce stress experienced for the internal switches. In order to minimize power loss, a buck converter is used. Advance voltage converters usually contain many components that inherit loss and provide functionality that is not necessary to this application. For example, zero-current switching is not required because current consumption is very small compared with large machinery motor drives. Buck converter is chosen over boost converter because digital circuits, which use 1V, do not consumes current constantly as in the case of analog circuits, which use 1.2V or above. As a result, the conduction loss is reduced.

Regulator control scheme is another advance topic. It is mainly divided into continuous-conduction mode and discontinuous-conduction mode. For a continuous-

conduction mode regulator, current through the filter inductor in the converter never stays at zero, as illustrated in Figure 3.2.

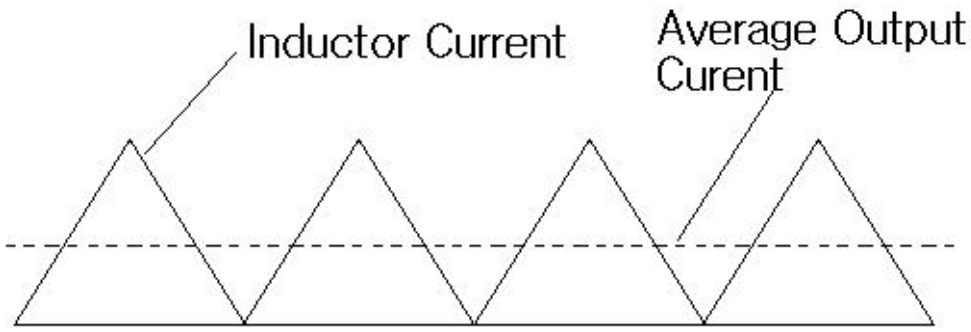

Figure 3.2. Current waveform in the converter using continuous-conduction mode.

This type of control waveform will generate a higher conduction loss over discontinuous-conduction mode. The discontinuous-conduction mode, on the other hand, source current to the inductor in a shorter pulse and causes no conduction to be occurred in the inductor for a period of time during a cycle. Thus, it produces a higher switching loss over continuous-conduction mode. In order to implement either mode of operation, one of the common techniques used is PWM, where current or voltage is sensed at a fixed rate. As a result, the converter internal switch will be on and off to charge the filter capacitor, where it provides a power supply voltage. This control scheme is attractive because the frequency spectrum has a distinct peak, where it interferes with other circuits in a controllable or expected manner. However, caution has to be placed on stability and current or voltage overshoot depending on the load characteristic. As in the case of digital circuits, due to its switching on and off nature, the PWM control should have a higher sampling rate in order to avoid overshoot. One way to solve these problems is to

use hysteretic regulator, where voltage or current is sensed in real time and is only limited by the loop delay and components bandwidth. The only drawback to this control scheme is that it is operating in a dynamic frequency manner, which the interference generated is not critical in digital circuits.

3.2 Hysteretic Voltage-Mode Regulator Design

With the different trade-offs mentioned, hysteretic voltage-mode regulator design is the most suitable topology for this application. Due to its dynamic sensing nature, a constant current load without switching effect should be designed first.

Frequency planning will be the first step for this design. With the constraint on area, off chip components can only have a package size less than 0603 package, in which the sizes are possible for mounting near the chip. 270nH inductor with self-resonant frequency (SRF) of 900 MHz and 1uF capacitor with SRF of about 6.7 MHz is chosen. Thus, the operating frequency should be less than the lowest SRF. Then, maximum specified current rating, which is 20mA in this case, should be used for the initial constant current load design because it will provide the maximum operating frequency for hysteretic regulator topology. The last thing to be considered in system level is pad assignment. The number of pad should be determined so that the pad and wire bond can sustain maximum peak current in desired conduction mode of operation. Next, modeling is done for three main components, which are inductor and capacitor in the converter and wire bond for the chip external connections. Figure 3.3 shows the equivalent model for these components.

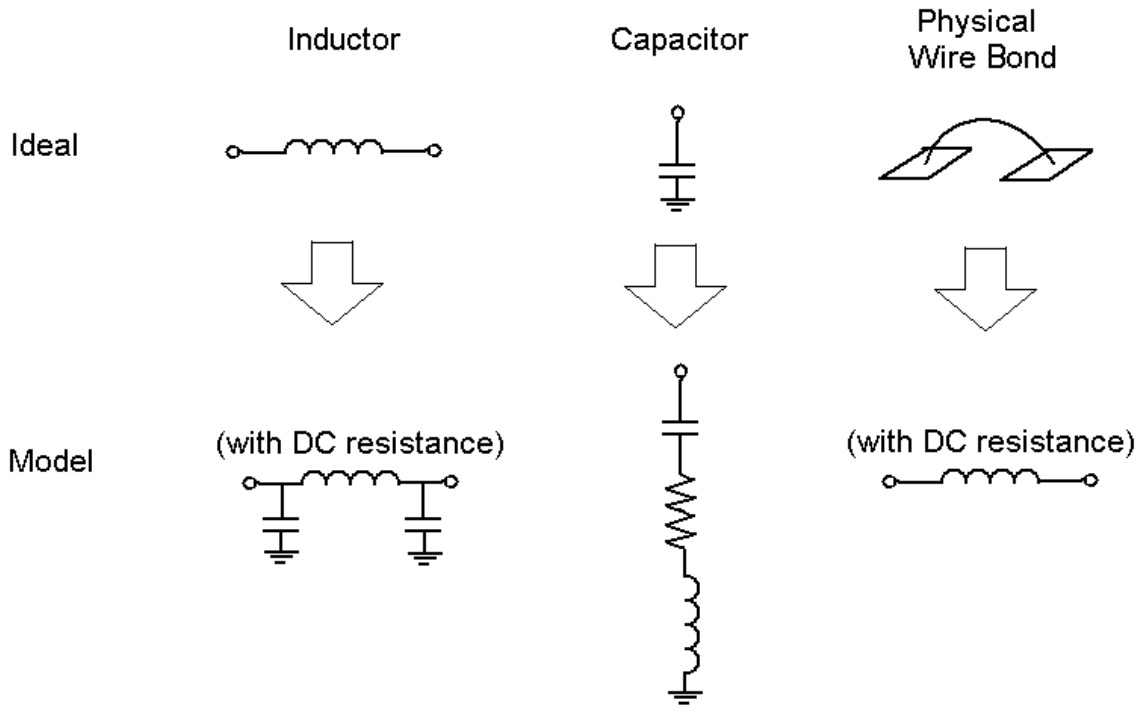

Figure 3.3. Equivalent lump components modeling.

These models can clearly indicate the resonant frequency of each component and performance during switching. With this technique, the inductor inherits two capacitors with value of 110fF each; the capacitor has an effective self resistance (ESR) of 10 mΩ and an effective self inductance (ESL) of 600pH; the wire bond, which is determined by the number of pad, has an inductance of 220pH with DC resistance of 0.5 Ω. Hence, the duty cycle and operating frequency for the design can be correctly determined.

Component level design will be the next step. In buck converter topology, there are two common variations. The first type is using a free-wheeling diode, which allows the current to be flown through the diode to the inductor during the off-state of the switch as shown in Figure 3.4.

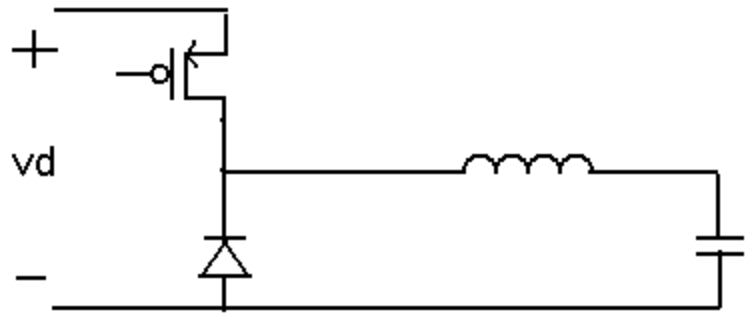

Figure 3.4. Buck converter schematic using free-wheeling diode.

The second type of buck converter is replacing the diode in Figure 3.4 with a NMOS transistor. This type of converter is widely used because it reduces the switching loss through the diode when operating at high frequency. However, additional complex circuits have to be employed in order to ensure that there is enough dead time between the on-off state of the PMOS and NMOS. As a result, there is no occurrence at any time that the PMOS and NMOS are turned on at the same time. Both of the topologies have been tested, but they give similar results in terms of area. In other words, the NMOS switch does provide less loss, but the area of the switch and associated control circuitries is larger than similar performance provided by parallel diodes in 90nm technology. Thus, the circuit in Figure 3.4 is used.

In normal hysteretic regulator design, the output voltage of the converter is feedback to the hysteresis. Then, the voltage output of the hysteresis is sent to a comparator to control the internal switch of DC converter [13]. The ripple generated is mainly determined by the hysteresis opening window; however, if 1% ripple is required when the output voltage of the converter is 1V, the required hysteresis window would be quite small for voltage mode control. In terms of reliability and process variation, this

window may not be realizable for the comparator. As a result, an error amplifier is required.

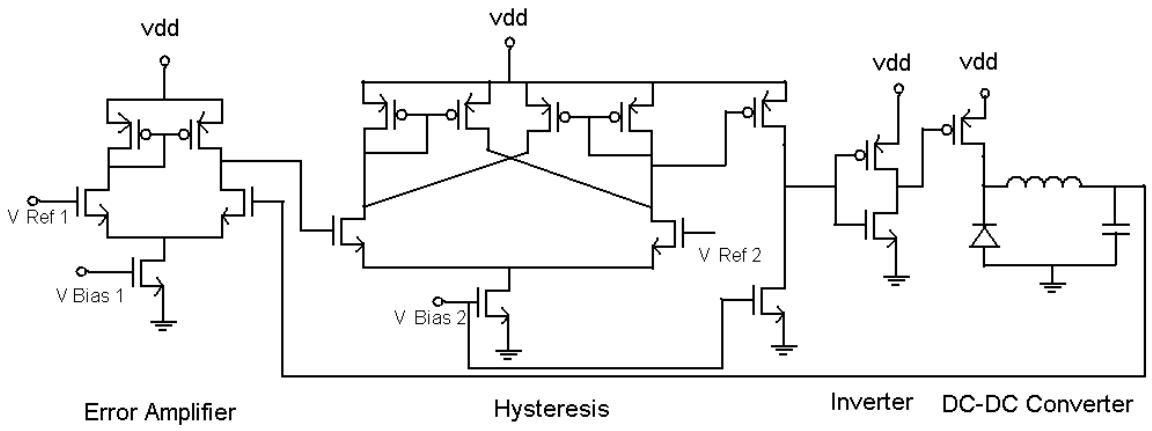

Figure 3.5. Proposed hysteretic voltage-mode regulator schematic.

Figure 3.5 shows the schematic of the proposed voltage-mode regulator. Every stage is operated in DC coupled condition. Thus, a fine tuned design is required. For example, this topology simplifies the design of a comparator by replacing it with a simple inverter. As a result, the output and the opening window of the hysteresis should cover reasonable range of the inverter midpoint crossing. Additionally, a single inverter usually is not enough to drive the large switch, which minimizes on-state loss, in the DC-DC converter. Hence, a chain of inverters with increasing size ratio of 2.7, which provide the optimal driving capability, should be used. This technique also provides a shorter rise and fall time for the converter switch that reduces power loss in transistor transition state.

Once constant current consumption load design is finished, an integration level power distribution scheme has to be setup. For this application, the baseband circuit is operating at 1.728 Gbps. This frequency will cause the load circuits experience large impedance when looking from the load to the converter output. This effect will impose a

larger than original design ripple in addition to the ripple caused by the loop delay and DC offset. The ripple is especially important because there is no capacitor that has a GHz range SRF while supporting the specific current loading. In serious situation, the power supply voltage experienced at the load may have a rail-to-rail fluctuation.

The only technique that can alleviate this effect is to use a decoupling capacitor. The basic function of the decoupling capacitor is to provide charges that are required by the load at a faster time than the charges flowing from the DC-DC converter. In other words, it shortens the current loop. The decoupling capacitor should have a high SRF with reasonably small in size, which is ideal for placing it on-chip. The most effective way is to have distributed elements. This network should have a decoupling capacitor for a certain length of wire. Thus, it decreases the combined effects of the voltage ripple. Ideally, large capacitor for every small segment of wire should be used. However, area remains the biggest challenge for SOC. Thus, an optimization has to be done between the area and acceptable output voltage ripple.

Meanwhile, the DC resistance along the wire can be minimized by stacking more than one layer of metal line. In terms of electrical performance, it is equivalent to placing resistors in parallel. The parallel metal lines do not only reduce the DC resistance, but also increase the capacitance along the power line.

3.3 Simulation Result

Off-chip components are modeled according to existing commercialized packages. The inductor is chosen from *Tyco Electronics Corp*. that has a SRF of 900MHz and DC resistance of 2.1 Ω. Using the modeling techniques, the frequency response is shown in Figure 3.6 with marker A identified the DC resistance and marker B located the SRF. As indicated in the plot, the inductor will have a capacitive response beyond the SRF.

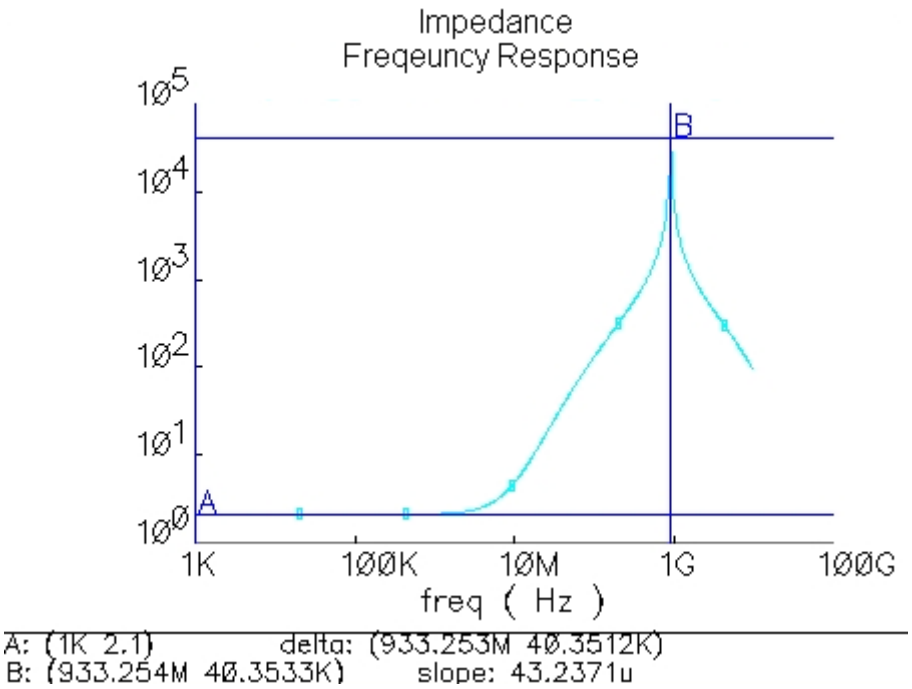

Figure 3.6. Impedance frequency response for the off-chip inductor model.

Employing similar strategy, the remaining off-chip capacitor is modeled. The measurement result [14] for the 1uF 0402 package capacitor is shown in Figure 3.7, and the model result is shown in Figure 3.8.

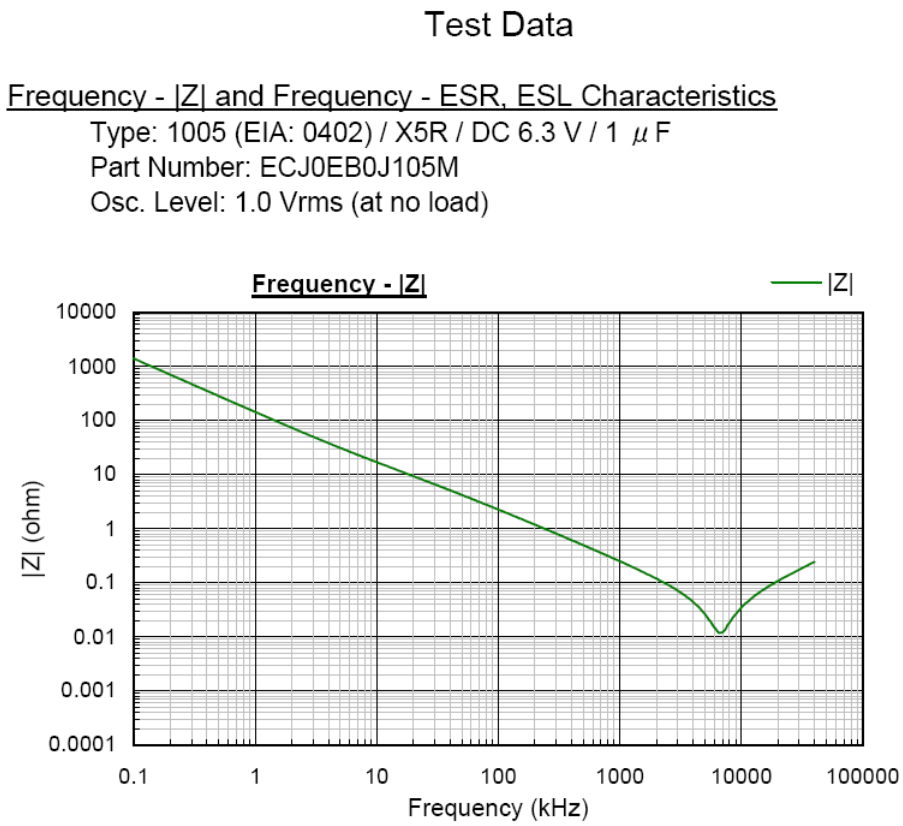

Figure 3.7. 1uF off-chip capacitor measurement result [14] (used with the courtesy from Panasonic Matsushita Electronics Components Co. Ltd).

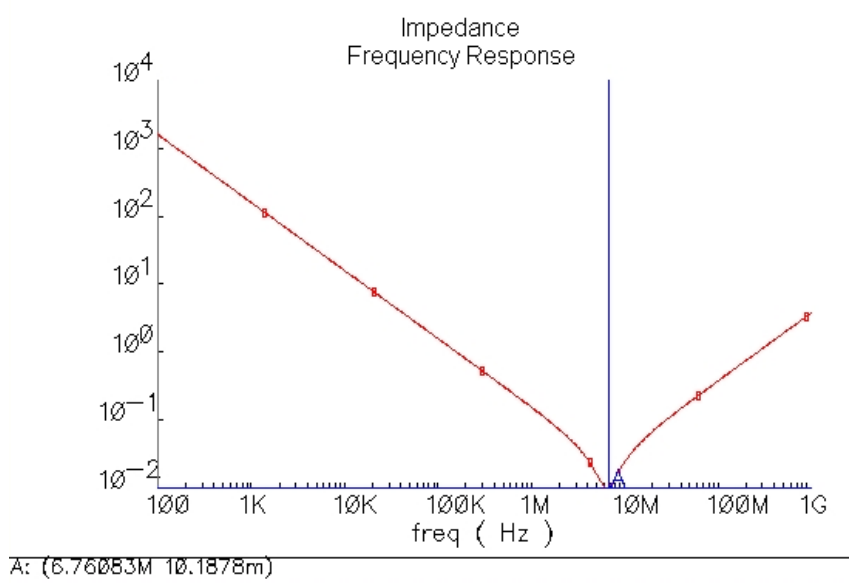

Figure 3.8. 1uF off-chip capacitor model result with respect to frequency.

With these off-chip components correctly modeled, error amplifier and hysteresis tuning is possible. The procedures usually involve the optimization among area, reliability and efficiency. A 20mA loading is chosen that is exceeding the maximum requirement for reliability reason. The design proposed for this application generates an output voltage ripple of 1.2% as shown in Figure 3.9 steady-state output voltage response.

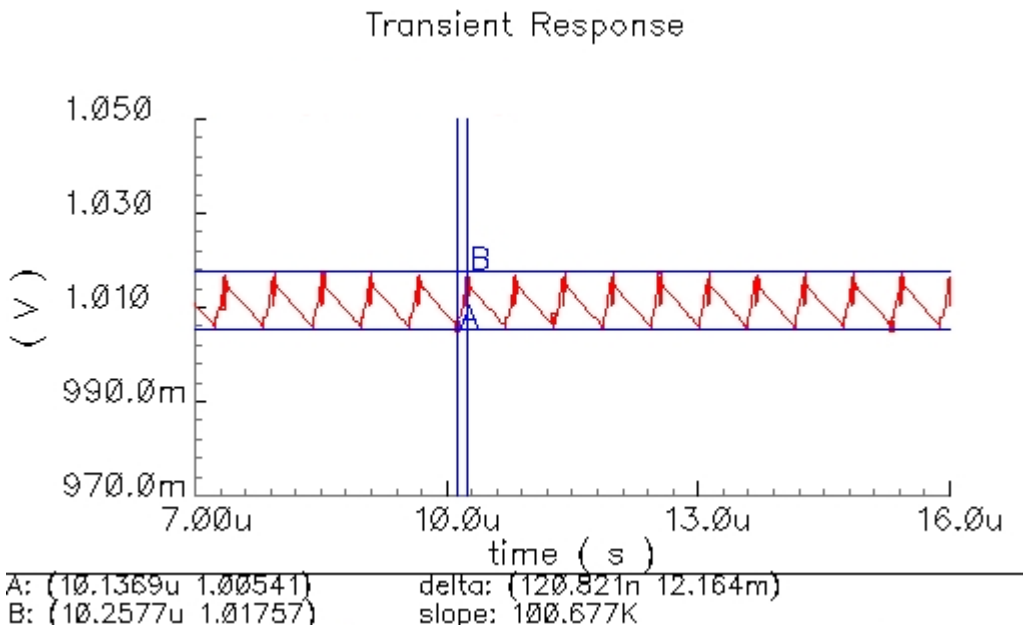

Figure 3.9. Proposed design steady-state output voltage ripple response.

The output voltage ripple can be further minimized by using smaller hysteresis window or larger component value for the DC-DC converter filter; however, caution has to be placed for the hysteresis window in terms of reliability. In the aspect of frequency response, the SRF is expected to be lower for larger off-chip components. Thus, the design cycle may require a feedback loop to the frequency planning phase. Then, off-chip components will have to be remodeled to ensure proper operation.

Figure 3.10 shows the overall output voltage response of the voltage regulator that indicates a worst case startup time of about 4us with 20mA load current. This startup time is mainly dominated by the charging time of the converter capacitor.

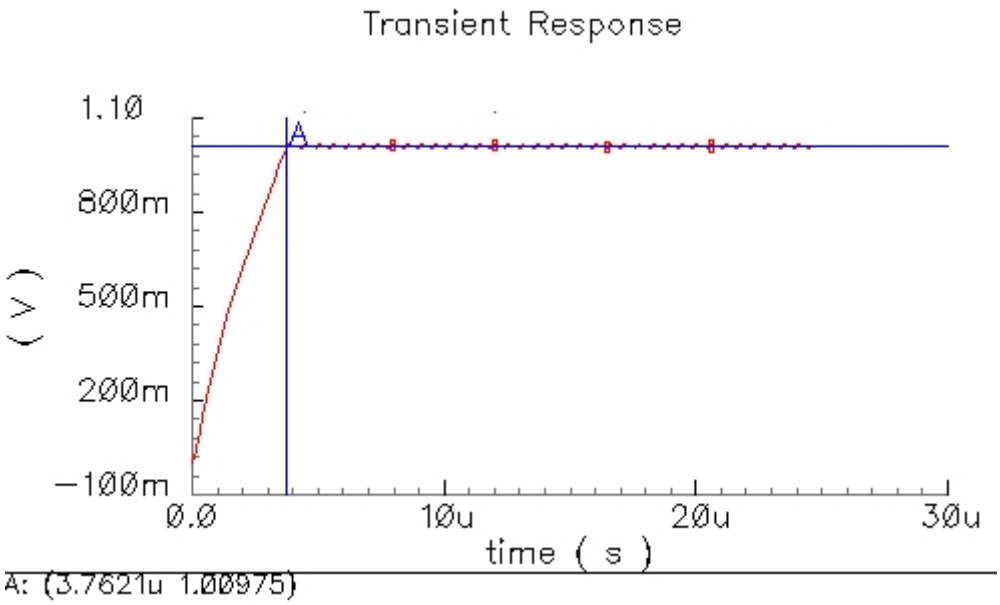

Figure 3.10. Voltage regulator output voltage response including startup phase.

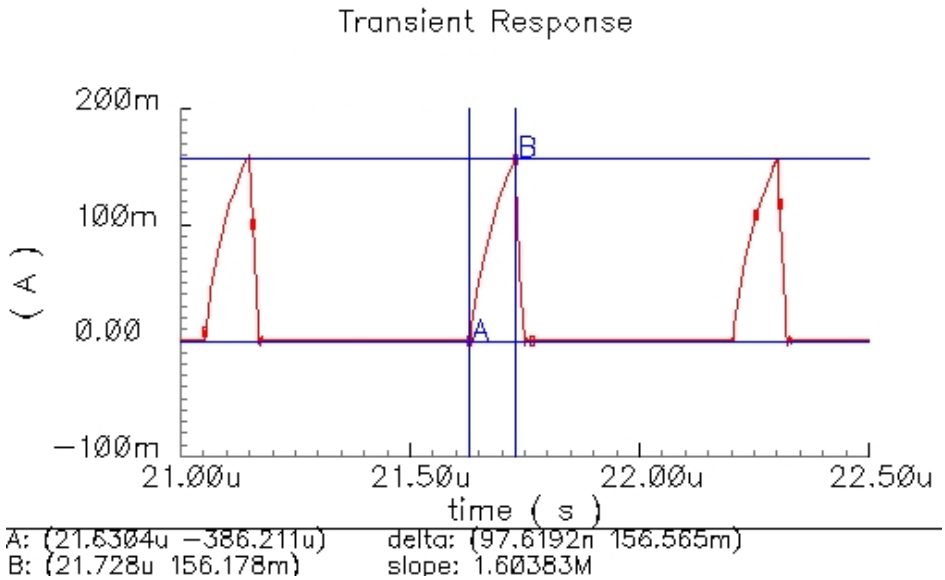

Figure 3.11. Current response through the DC-DC converter filter inductor.

As Figure 3.10 suggested, the regulator is operating below the SRF of off-chip components. Figure 3.11 further shows that the current through the inductor has an operating frequency of about 1.75 MHz, which is four time smaller than the resonant frequency. Additionally, the converter has a duty cycle of about 0.17, where the switch in the converter is turned on as marked by marker A and B. This response also reveals the number of pad and wire bond required to sustain the current rating.

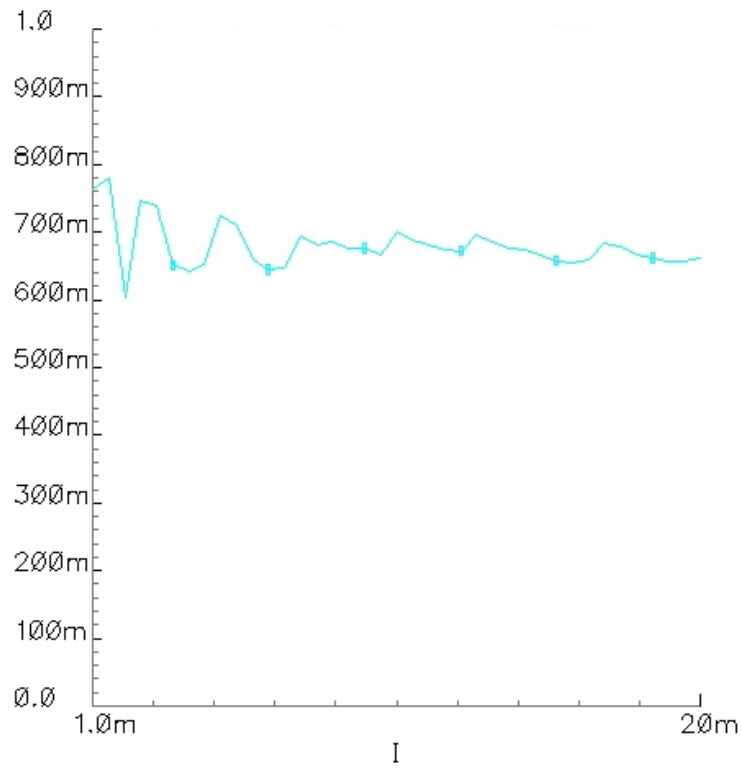

Figure 3.12. Proposed voltage regulator DC-DC converter efficiency.

Figure 3.12 demonstrates the design achieved efficiency between 60% to 80% depending on the load current. The efficiency can be improved if a larger switch, capacitor and inductor are used in the DC-DC converter. As indicated in Table 3.1, the

DC-DC converter filter network and associated wire bond dominate most of the power loss that reduces the efficiency of about 20 percent.

Table 3.1. Power dissipation for each component in the DC-DC converter

	Power Dissipation	Percentage
Power Input	31mW	--
Switch and associated wire bonds	2mW	6.45%
Diode	3mW	9.68%
Filter and associated wire bonds	6mW	19.35%
Power Output	20mW	64.52%

This result may not be able to significantly improve further because of the area constraint. If a larger area is available, more wire bond and pad connection can be used. It will further reduce the DC resistance. Hence, the area has a direct relationship with efficiency. However, this result is still acceptable because its efficiency is still higher than the linear voltage regulator while satisfying the area constraint.

With this constant load design, a power distribution network has to be setup in order to accommodate digital circuit loads. Decoupling capacitor of 2pF for every 150um length of wire is optimally determined with respect to area and performance tolerance. Figure 3.13 shows the significant improvement in terms of wire impedance experienced at the load 1.5mm away from the pad connection. As suggest by basic electrical behavior, the inductive load from the converter inductor and wire bond inductance will increase the impedance with frequency. As a result, the decoupling capacitor acts as temporary charge storage for the instantaneous need of the high speed baseband circuits.

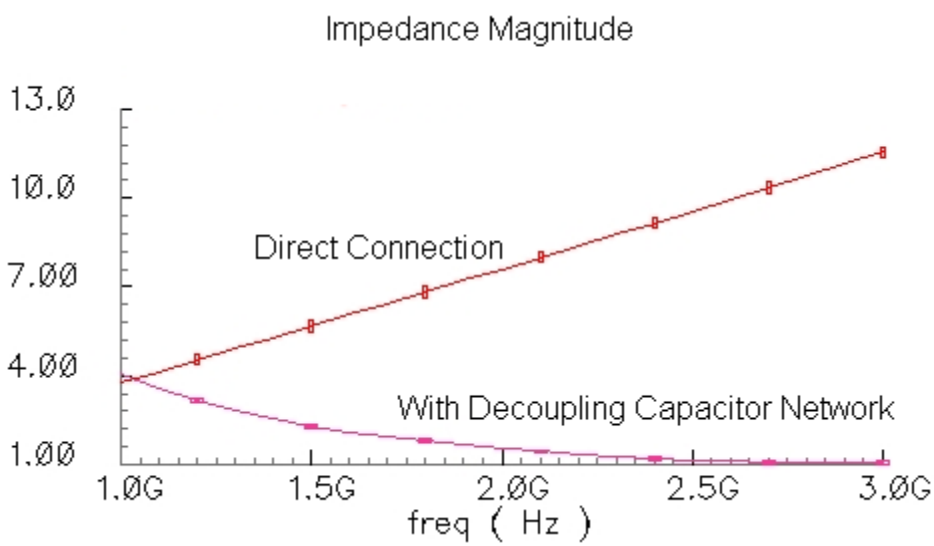

Figure 3.13. Impedance magnitude simulated from the load to the pad and DC-DC converter.

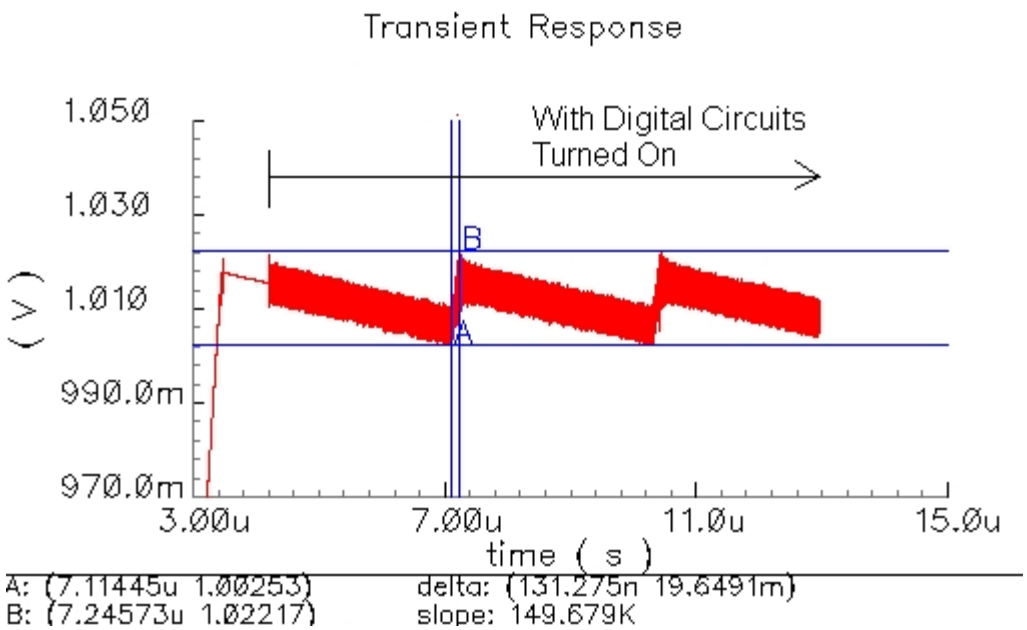

Figure 3.14. Voltage regulator output voltage response with digital circuits turned on at about 4us.

With the power distribution network and the voltage regulator in place, simulation is run with the pulse-shaping FIR filter and digital input signal enhancement circuits, which consumes total average current of 3mA. Figure 3.14 illustrates that an addition of 0.8% voltage ripple is resulted from the digital circuit; however, it is significantly reduced by the decoupling network that may, otherwise, result in a close to 0V to 1V ripple. Hence, the overall voltage ripple with respect to regulator control loop delay, converter filter ripple and digital circuits induced ripple is about 2%. A detailed investigation also suggested the digital circuits induced ripple has a variable frequency and is higher than the baseband operating frequency. However, the waveform shown in Figure 3.14 only indicated a close to constant simultaneous switching noise caused by the digital circuit. The reason is because the power distribution network is not identical in length when connected to all the digital circuits. As a result, a wide frequency spectrum exists at the 1V output voltage node of the converter. This noise is bounded by a certain amplitude is mainly contributed by the decoupling capacitor network as illustrated in Figure 3.13, where the impedance does not further increase for higher frequency.

3.4 Summary

An on-chip voltage regulator design has been demonstrated with reasonable efficiency that satisfies area, current rating and output voltage ripple constraints. The room for improvement remains in the trade-off among different specifications. These limitations are mostly depended upon components performance. However, in the system point of view, the design provides a solution that unifies the power supply requirement between analog and digital circuits, which makes a single SOC integration possible.

CHAPTER 4

BIAS CIRCUIT

4.1 Introduction

A bias voltage is necessary for most of the analog and mixed-signal circuits. This voltage is required as a voltage reference for adjusting transistor operation state. As in the case of simple differential pair, it can be used to adjust necessary gain through the manipulation of the DC current. Voltage bias scheme has been developed for a long time. The oldest and simplest topology, which is still in used in some low-quality electronics or prototype, is resistive divider. It generally generates the necessary voltage by utilizing power supply and/or ground as a reference. This type of bias scheme is simple, but may not be feasible. The voltage that can be generated from this scheme is limited by resistor variation and resolution. Additionally, in most of the case, where power supply inherits its own voltage or current supply ripple, the bias voltage varies. These issues are not critical to circuit using high power supply voltage or solder board mounted prototype because they usually has a higher tolerant in bias voltage shift and can be easily adjusted by changing the resistors.

However, the problems cannot be solved when the bias scheme is implemented into an IC with low power supply voltage and cannot be physically adjusted. Thus, circuits have been developed to provide a precise constant DC current or voltage under all of the variation conditions.

In terms of power supply variation, where the effect is produced from internal regulator output voltage ripple, is usually minimized by using a reference voltage from an

active element relative to ground. The most common ones are BJT base and emitter voltage (V_{BE}) referenced and MOS threshold voltage (V_T) referenced [15]. These voltages do not change a lot due to their operation state characteristic. Figure 4.1 illustrates a simple V_T referenced circuit utilizing M1 threshold voltage.

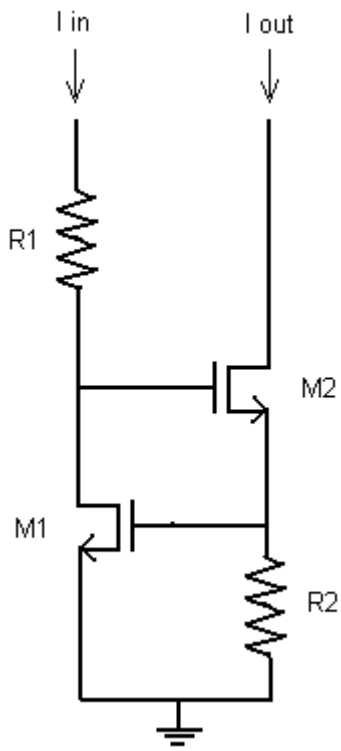

Figure 4.1. Basic threshold referenced current source.

Its output current sensitivity relative to supply voltage is defined as

$$S_{VDD}^{Iout} = \frac{V_{ov1}}{2\left(V_T + V_{ov1}\right)} S_{VDD}^{I_{IN}} \tag{4}$$

where V_{ov} overdrive voltage is

$$\sqrt{2I_{IN} / \left[k'\left(W/L\right)_1\right]} \tag{5}$$

As an approximation for 90nm CMOS technology and assuming sensitivity of $S_{VDD}^{I_{IN}} = 1$, $V_T \approx 0.4V$ and $V_{OV1} \approx 0.05V$, the resulting output current sensitivity will be about 0.055. The result can be improved further by decreasing sensitivity of I_{IN} using current mirror and other bootstrap techniques. Some other advanced methods, such as employing internal error amplifier [16], significantly reduce output current sensitivity with respect to power supply.

However, all these techniques only compensated the variation from other components, such as power supply. The bias circuit itself is also affected by temperature. A V_T referenced current source usually generates a positive temperature coefficient. In other words, the current of V_T referenced circuit increases as the temperature increases. This temperature dependency leads to the use of bandgap referenced, CTAT and PTAT. A bandgap referenced utilizes V_{BE} negative temperature coefficient to cancel the effect of the positive temperature coefficient from V_T current source. With the weighted sum optimized through a summing circuit, the circuit overall response can be adjusted to have a temperature independent region around design specification. This idea is illustrated in Figure 4.2.

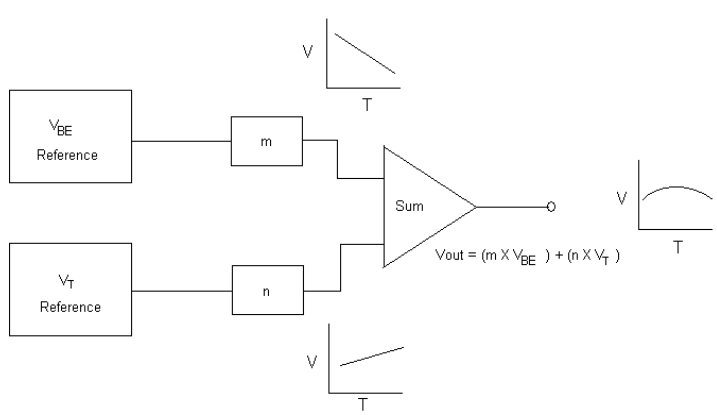

Figure 4.2. Bandgap referenced circuit architecture.

CTAT and PTAT circuits are other topologies that replace the V_{BE} and V_T referenced blocks as a temperature compensation circuit. With these techniques, temperature and power supply variation sensitivity can be minimized. However, as the feature size for CMOS becomes smaller, indicated in the International Technology Roadmap for Semiconductor (ITRS), process variation becomes one of the variations comparable to traditional dominated factors, temperature and power supply variation. This kind of variation does affect the bias circuit sensitivity to some extent. However, there is no mathematical calculation to be performed to compensate this effect because it is based on technology used and fabrication foundries variation specifications. As a result, designs have to be based on tuning instead of mathematical analysis.

Another problem with the bias circuit is the integration scheme. There is no doubt that there are more than one bias points required by a SOC with mixed-signal and RF circuits. Thus, a trade-off has to be made in terms of area and power consumption. Many power supply and temperature invariant circuit utilizes a lot of current mirror or internal amplifier to generate a single stable voltage. Hence, power consumption and area will significantly increase. This increase leads to the development of bias circuit operating in subthreshold region. However, this technique generates noise for RF circuits, and it is usually inherited large process variation due to improper current mirroring to the load.

Focusing on power supply, temperature and process variations, a simple bias circuit that is feasible to SOC with minimal power consumption and reasonable sensitivity should be integrated. Concentration should not be place on a single aspect in order to ensure its robustness.

4.2 Integration Strategy

In order to minimize the area and power consumption, the number of bias circuit cores placed throughout the chip is minimized. This bias core will generated a low sensitivity current towards temperature and power supply. This current is mirrored through a NMOS to the interfaces, which consist of two current mirrors for different loads. This interface utilizes the uniform ground plane from the waveguide for the RF circuits to set the current. As a result, the interface is also independent to power supply voltage. Thus, the power consumption can be reduced by adjusting the transistor sizes in the interface circuits. In term of process variation, the bias core circuit should be fined tune to a point where all the resulting current variations of the load circuits fall into a similar range. In other words, process variation should not be well tuned to one single specific load.

Then, the bias cores should be placed close to the power supply pad to minimize any voltage drop experienced. On the other hand, the interface can be placed in or integrated within the load circuit itself. Hence, this integration scheme reduces final chip integration time by decreasing the number of wire routing to one single bias point.

4.3 V_{BE} Referenced Bias Circuit Design

In this CMOS process, a lateral BJT can be used. As a result, in order to minimize the power supply sensitivity, V_{BE} referenced is deployed. This voltage is referenced to ground, which is uniformly distributed with the entire chip covered with ground plane. On the other hand, the temperature is reduced by the positive coefficient of the resistor and V_T of the MOS transistor. The effect is further compensated at the

diode connected NMOS, which has a positive temperature coefficient, at the output as shown in Figure 4.3.

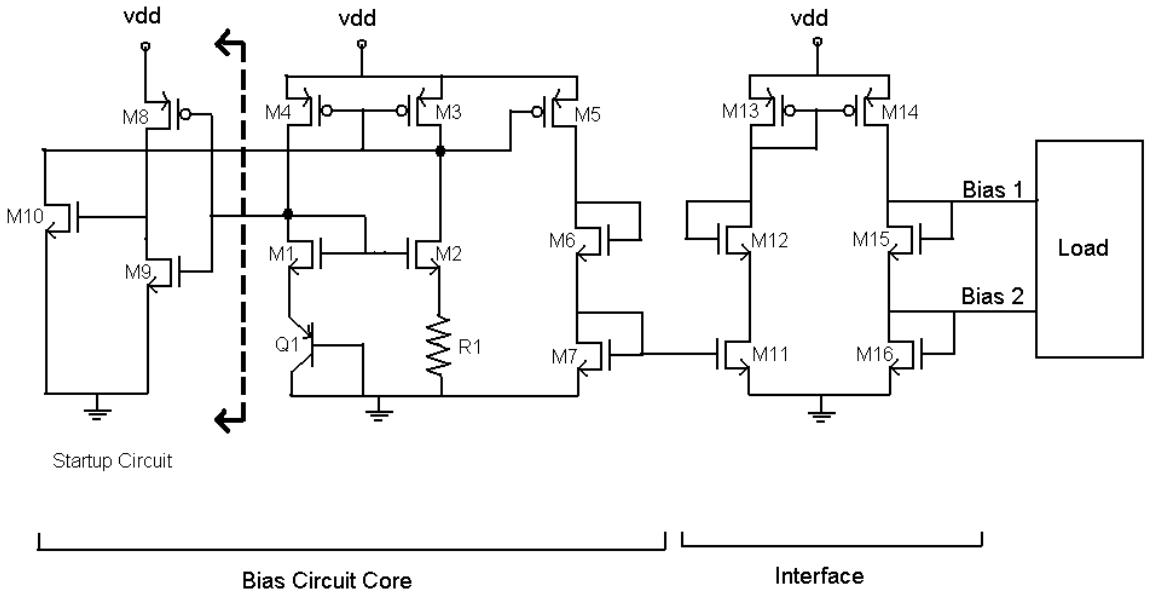

Figure 4.3. V_{BE} referenced bias circuit scheme schematic.

Similar to most bias circuit, stable condition exists at zero-current point for the core. Thus, a startup circuit is required to pull the circuit to another desired stable condition. When there is no current flowing through, the gate voltage at M1 is less than its threshold voltage, which is able to turn on M8, but not M9. As a result, an inverter response is acquired that turns on M10. As M10 is in the on-state, it pulls down the gate voltage of M3 and M4. As a result, current starts to flow through both sides of the core and turns on M9, which partially reduces the current through M10 that may affect the bias core operation. Once it is operational, the voltage generated at the drain of M3 has a small temperature coefficient, which reduces further from the diode connected M6 and

M7. Thus, this simple structure is temperature and power supply sensitivity compensated.

On the other hand, the process variation is minimized by maintaining a similar ratio in the interface circuit transistors, M11, M12 and M13, as the core. Further tuning in the core is achieved for process variation that is average to all the required loads.

This bias scheme is verified through simulation using the first cascode stage of the PA 40um×0.1um NMOS as the load operating with 1.8V power supply voltage. Figure 4.4 illustrates the current sensitivity, which is critical for RF circuit, is about 2.5mA/V. It is translated to 3% variation in current when there is 5.6% variation at the power supply.

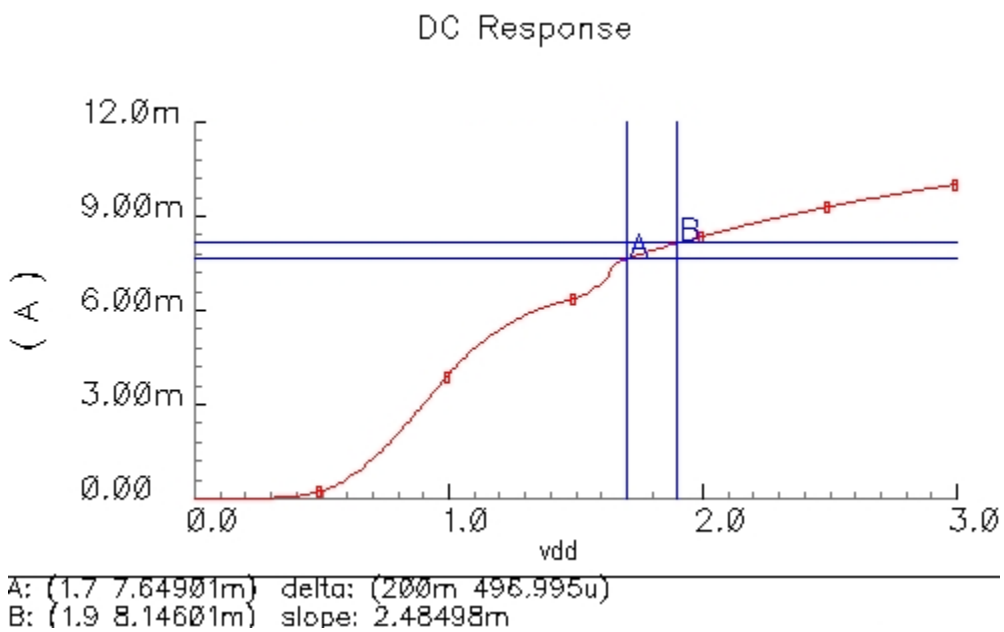

Figure 4.4. Load current response with respect to power supply voltage variation.

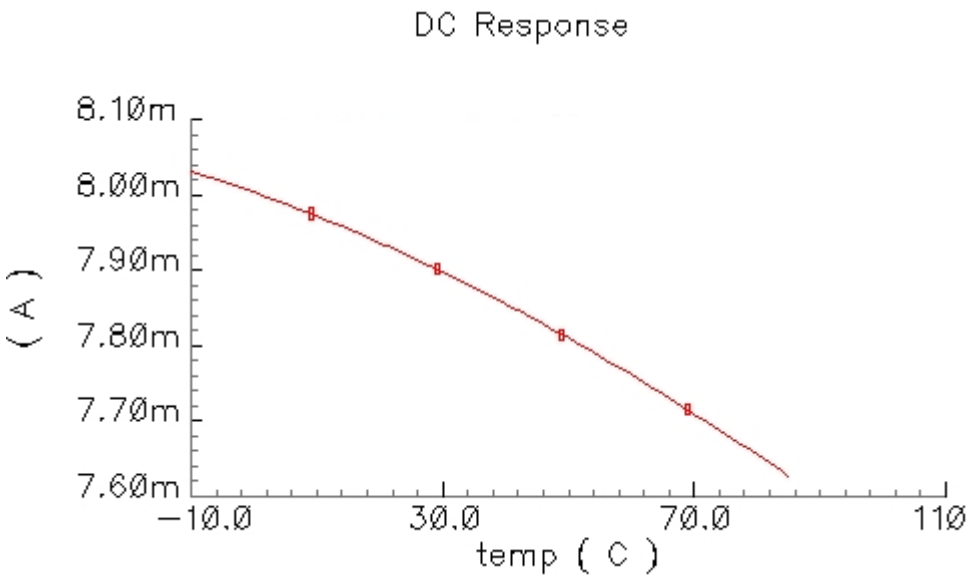

Figure 4.5. Load current response with respect to temperature variation.

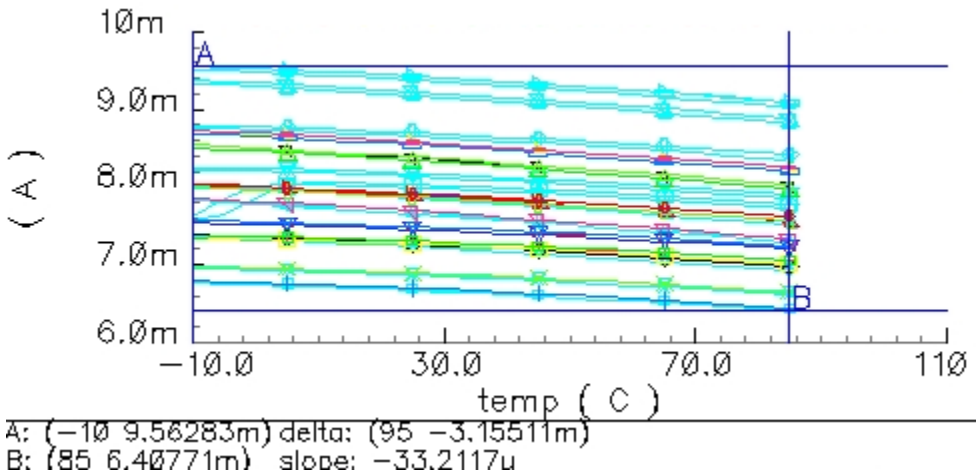

Figure 4.6. Load current response with respect to all process corner combinations and temperature variations with marker A placed on the absolute maximum and marker B situated at the absolute minimum.

As for temperature sensitivity shown in Figure 4.5, the current at the load varies from +1.5% to -3% from the temperature range between -10°C to 85°C. This result is intermediate compared with the well tuned bias circuits with respect temperature or power supply variation existed today; however, attention should not be only placed on these two aspects. As shown in Figure 4.6, the process variation to nowadays small feature technology, 90nm CMOS in this case, is as much as 21%. Additionally, this design has been well tuned to this aspect. Many techniques used today that compensated temperature and power supply variation utilizes amplifier. Thus, their process variations, which is the dominate factor in small feature size IC, will also be amplified to some extent.

4.4 V_T Referenced Bias Circuit Design

As feature size for CMOS technology keeps shrinking, power supply voltage level requirements are also reduced, as indicated in ITRS. The trend urges the usage of lower power supply level for bias circuits also. Thus, a 1V, common voltage used in 90nm CMOS digital circuits, bias circuit is designed.

In this power supply voltage range, V_{BE} referenced circuit is no longer able to be implemented because V_{BE} referenced voltage is generally around 0.8V. As a result, it translates to a 0.2V head room for an additional element, which is PMOS in most of the case. This condition is not able to drive the PMOS into saturation if power supply variation is also taken into account. In other words, for worst case scenario, when the power supply voltage experienced by the core due to voltage drop is -10%, which is

0.9V, there is only 0.1V across the drain and source. Thus, V_{BE} referenced is not practical.

V_T referenced will be the next obvious choice that is about 0.3V to 0.4V in current technology. The basic idea for V_T referenced is illustrated in Figure 4.1. Similar to the proposed V_{BE} referenced circuit, same bias scheme is applied, but with one less NMOS diode connected transistor at the output and in the interface as indicated in Figure 4.7.

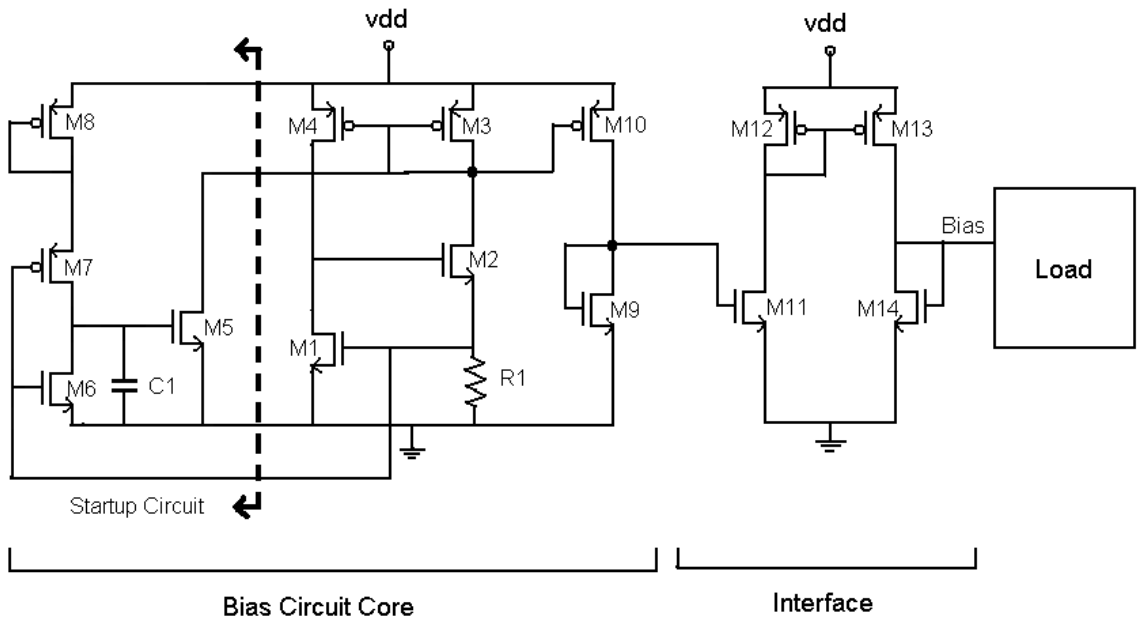

Figure 4.7. V_T referenced bias circuit scheme schematic.

As V_T of M1 sets the voltage across R1, the current is mirrored back to M4 and stabilizes with M2 through a feedback mechanism. Same as the proposed V_{BE} referenced circuit, a startup circuit is required to pull the feedback condition out of zero-current state. However, a diode connected M8 is implemented in the startup circuit in order to

extent the operational power supply voltage to 2V before break down occurs. As a result, the structure for M6, M7 and M8 has to be well tuned for proper operation. Since the power supply voltage is reduced to 1V, M7 and M6 acts as a digital inverter that will be completely turned on and off unlike the case for V_{BE} referenced circuit. This high gain instantaneous switching may cause oscillation in the bias circuit core. Thus, a capacitor, C1, is added to ensure the voltage is ramped up in a reasonable time. The resulting startup response is shown in Figure 4.8 and 4.9 by assuming the gate voltage of M1 is close to 0V, and the gate voltage of M3 is closed to 1V.

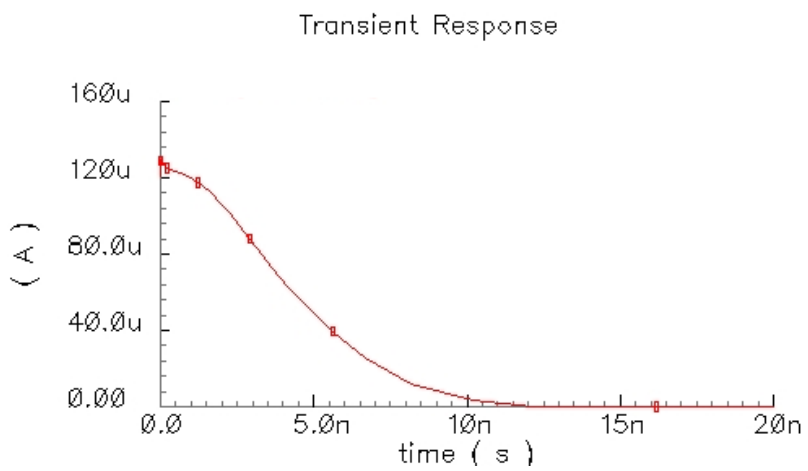

Figure 4.8. Current flow through transistor M5 during the startup state.

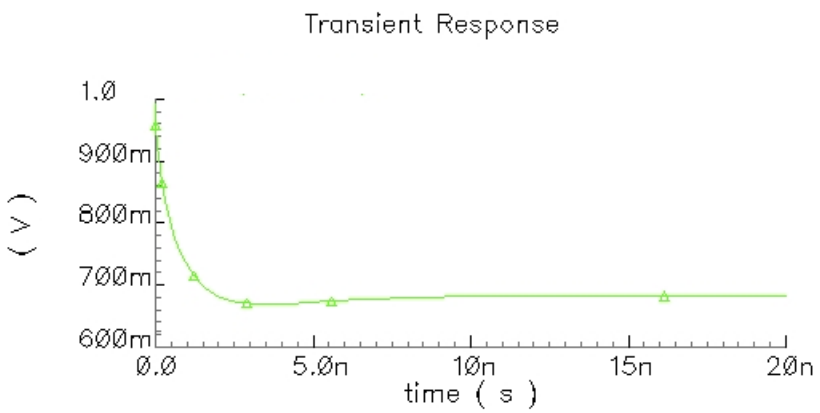

Figure 4.9. Drain voltage of M5 during the startup state.

Similar to other bias circuits, power supply voltage and temperature variation simulation is run. Using the last stage of the PA 60um×0.1um NMOS transistor operating at 1V, current with respect to these variations are illustrated. In Figure 4.10, it shows a sensitivity of 5mA/V around the ±10% power supply voltage operating region. In addition, the plot also indicates a -5.5% to 2% variation for -10% to 10% power supply variation respectively.

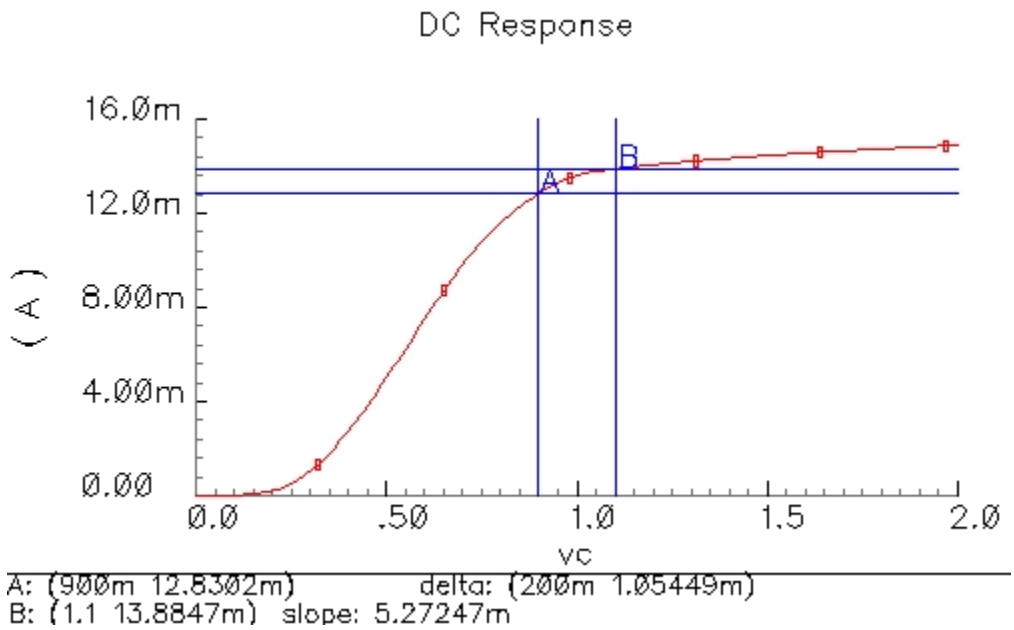

Figure 4.10. Load current response with respect to power supply voltage variation.

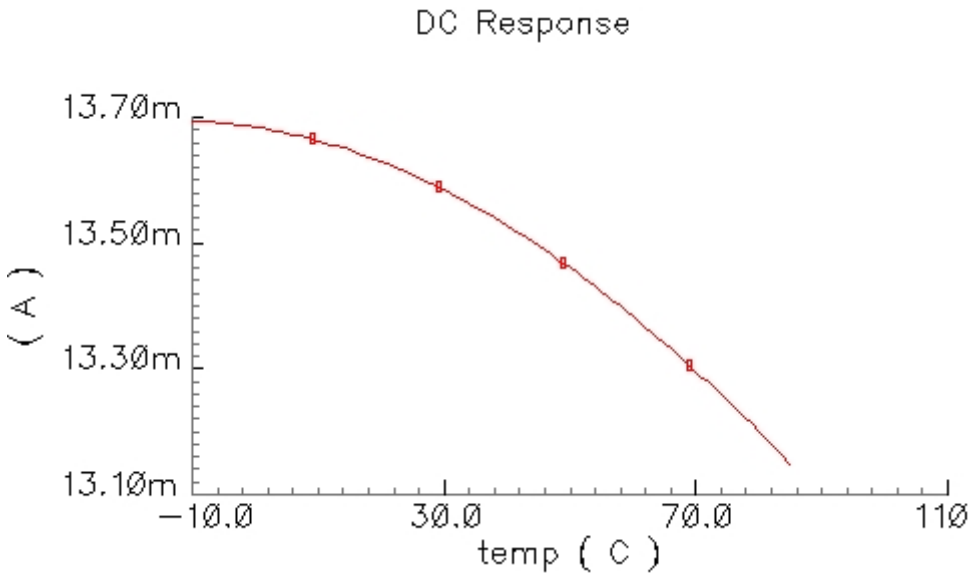

Figure 4.11. Load current response with respect to temperature variation.

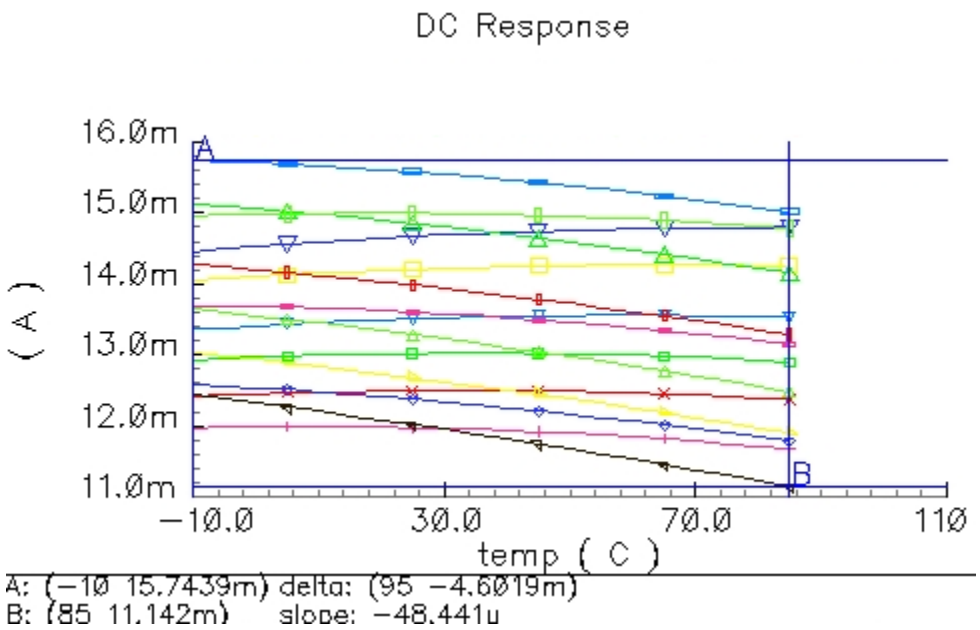

Figure 4.12. Load current response with respect to all process corner combinations and temperature variations with marker A placed on the absolute maximum and marker B situated at the absolute minimum.

Figure 4.11 shows that the current variation, with respect to temperature, is between -3% to 0.7% over the range of -10°C to 85°C. Both of the results are similar to previous proposed V_{BE} referenced bias circuits; however, there is a slight improvement in current variation with respect to process as revealed in Figure 4.12. One observable reason is that only two types of element existed in the bias core. In other words, BJT's process variation is eliminated. As a result, the current variation reduced to the range between -18% to 15%. Overall, the process variation, with respect to transistor and resistor, is still the dominated variation over temperature and power supply voltage.

4.5 Open Loop Process Variation Compensated Bias Circuit Design

As illustrated in V_T referenced circuit, process variation is slightly improved by using one less type of circuit element. This improvement may lead to the assumption that using a bias circuit without a resistor may further reduced process variation. However, eventually, this variation is still around three to five times larger than those induced from temperature and power supply voltage. In order to alleviate the problem effectively, compensation should be employed towards resistor and MOS transistor.

The design is the same as the proposed V_T referenced circuit, but the resistor R1 is replaced by seven resistors and NMOS switches connected to ground in parallel. Caution has to be used with the seven resistors and NMOS dimensions because all of the additional elements alter the sensitivity with respect to temperature and power supply in the original design.

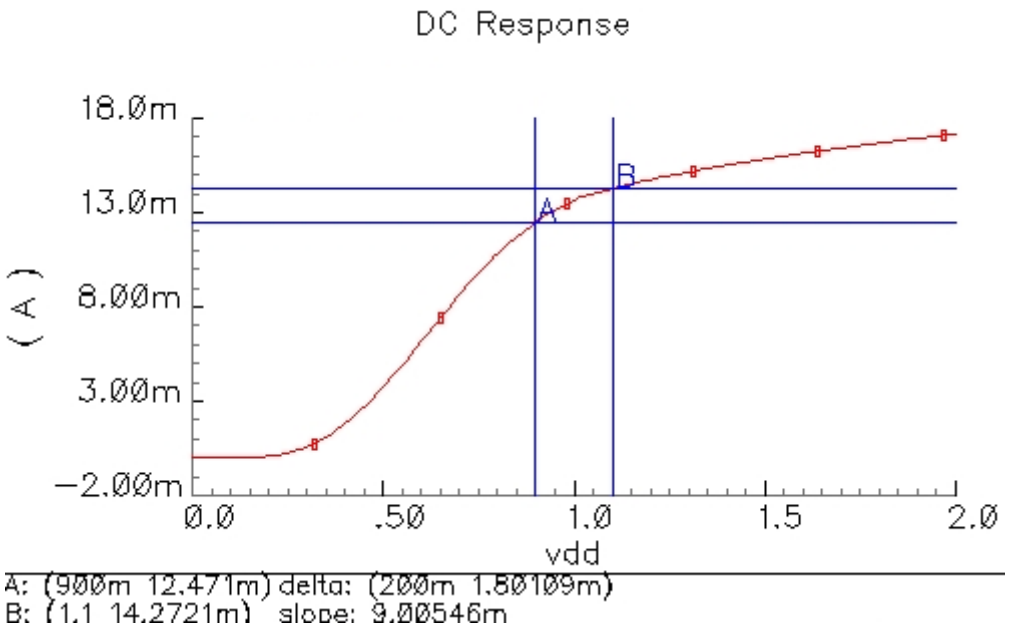

Figure 4.13. Load current response with respect to power supply voltage variation.

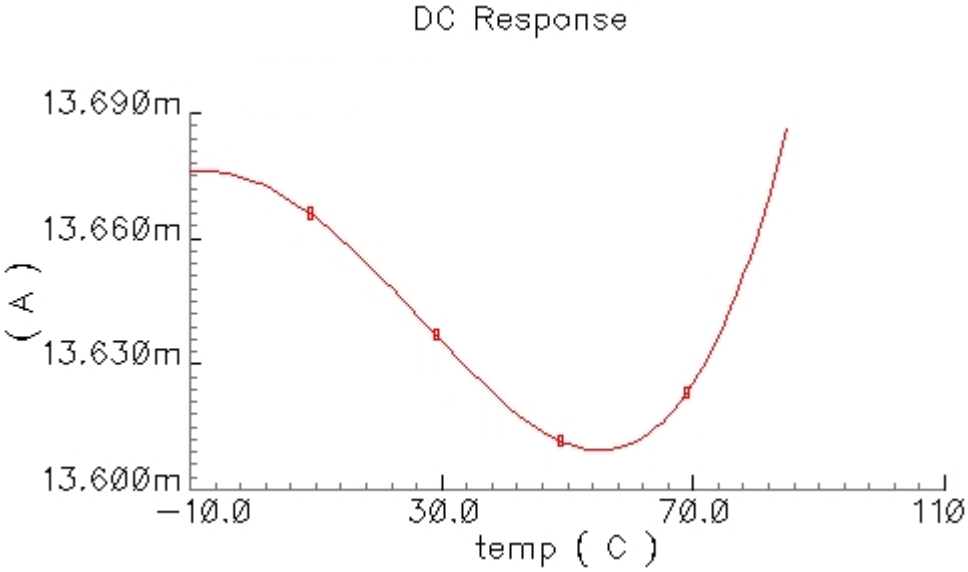

Figure 4.14. Load current response with respect to temperature variation.

As illustrated in Figure 4.13, the power supply sensitivity is increased from 5mA/V to 9mA/V. This response is due to the leakage or subthreshold current through the seven NMOS switches. On the other hand, Figure 4.14 shows the entirely different current variation response with respect to temperature. Although its temperature compensated response is better than the previously proposed V_T referenced circuit, its marginal improvement can be neglected because each process corner combination generates a different temperature response.

All the process corner combinations between the resistors and transistors is compensated with seven resistors and NMOS switches as shown in Figure 4.15 with resulting current variation of ±3%. In terms of integration, the inputs required for this 7-state control can be minimized to 3-bit with a digital controller. Additionally, the number of inputs can be further reduced to one input through a shift register.

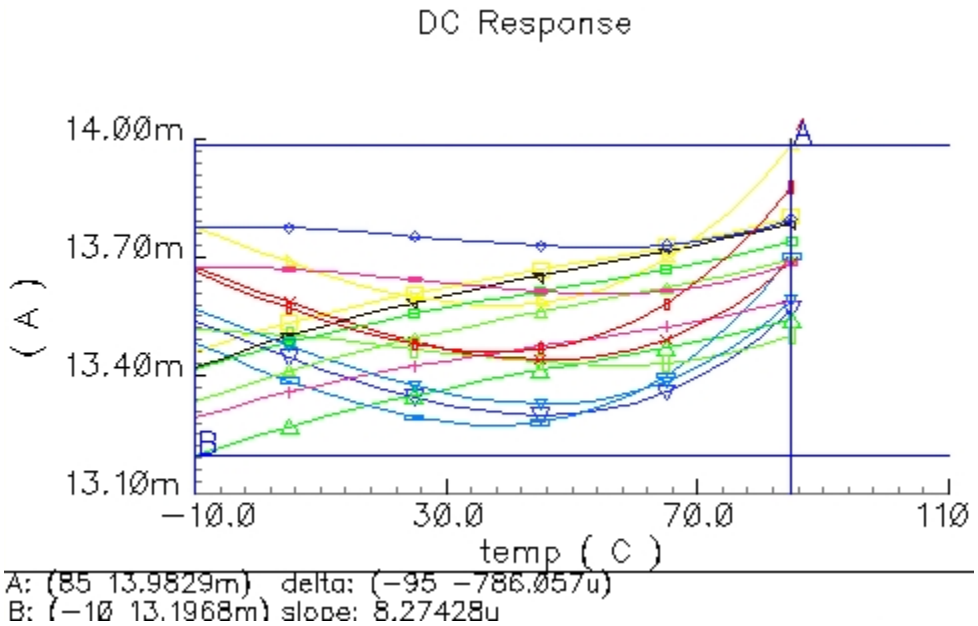

Figure 4.15. Load current response with respect to all process corner combinations and temperature variations with marker A placed on the absolute maximum and marker B situated at the absolute minimum.

Table 4.1. Performance summary of the proposed bias circuits

Variation Factors	V_{BE} referenced circuit	V_T referenced circuit	V_T referenced circuit with process variation compensated
Power supply	2.5mA/V	5mA/V	9mA/V
Temperature	-3% to +1.5%	-3% to +0.7%	-0.2% to +0.2%
Process	-19% to 21%	-18% to 15%	-3% to +3%

4.6 Summary

Bias circuit has been used through every analog circuit that uses BJT and MOS transistors. From simple resistive divider to complex internal amplifier compensated bias circuit. With the growing trend of SOC, bias circuits are also integrated into IC. Unlike automatic gain control circuits, the bias circuit does not have any feedback from the load. Thus, its design has to be robust against all the external and internal generated variation. The most common variations are from temperature and power supply. Many techniques have been employed over years; however, as IC feature size becomes smaller, process variation becomes a main issue as its variation is different from batch-to-batch, process-to-process and technology-to-technology. Simple optimization techniques, such as different load tuning and maintaining transistor ratio, have been used in two designs, but the variation still surpasses that of temperature and power supply compensated result as illustrated in Table 4.1.

Hence, a resistor and transistor specific compensated design is introduced. With a simple structure that is feasible to be integrated into a whole system, this powerful circuit can generate a current with respect to the load that is invariant to temperature, power supply and process. This proposed circuit not only offers a robust solution to bias circuit design, but also increases the reliability of this RF SOC transceiver system.

CHAPTER 5

DIGITAL-TO-ANALOG CONVERTER

5.1 Introduction

The most important element to interface between analog and digital circuits is digital-to-analog converter (DAC) and analog-to-digital converter (ADC). In most transmitter systems, a DAC is usually implemented for conversion. A common type of DAC used in audio systems is sigma-delta over-sampling DAC. The advantage for this DAC is it generates high precision discrete level of output voltages. The entire circuit consists of a subtractor, an integrator, a comparator, a D-latch and a DAC structure. The D-latch, operating at a higher frequency than the signal data, holds and samples data, and allows the other components to determine whether a signal is high or low more accurately. However, in this transceiver system, there is only one clock signal for the input of the pulse-shaping FIR filter. Although frequency doublers are one of the solutions to generate another clock internally for the DAC, sigma-delta DAC is also prone to significant delay due to its feedback loop, which makes it impossible to operate at around 1.728 Gbps.

The binary weighted DAC is attractive for its simplicity and speed that it generates in each distinct level by summing all the current through an operational amplifier. However, this DAC suffers greatly on process variation. The switching capacitive DAC is another common topology; however, it requires large space and generally has a slower speed. Thus, switching capacitive DAC is not feasible for the system.

5.2 R2R DAC Design

One promising solution is the R2R structure DAC. This topology provides a simple and robust solution. The schematic is shown in Figure 5.1. The DAC can be easily analyzed using Thevenin equivalent resistance method to calculate each distinct level. Essentially, it produces a rail-to-rail output. The only exception is the highest output voltage level, which is limited by the resistive drop across the switch. The main design specification for the DAC implemented in the pulse-shaping FIR filter is speed and the number of required distinct output voltage levels.

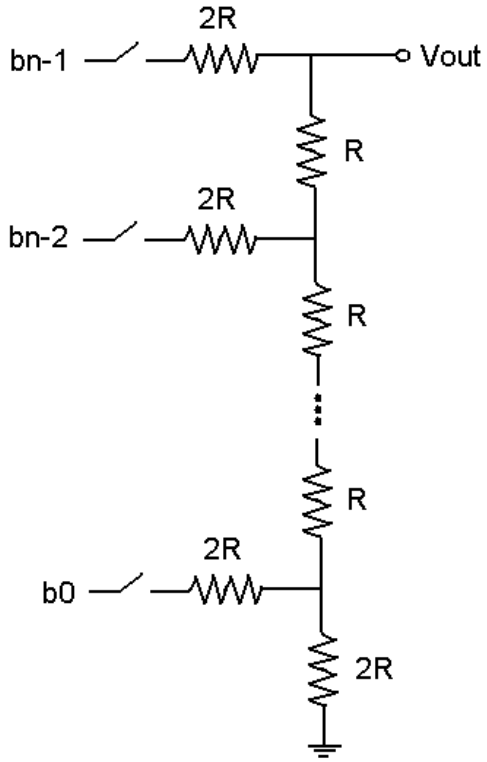

Figure 5.1. R2R DAC schematic.

The speed is mainly governed by the specific load, which is the mixer for the OOK chip. The 40um×0.1um NMOS transistor used in the mixer have a parasitic capacitance of around 100fF to 300fF in GHz range. This gate-to-source capacitance,

combined with the resistive output of the DAC structure, forms a low pass RC network. As a result, this RC network gives a disadvantage in term of speed for this DAC architecture. Thus, resistors have to be chosen between the trade-off of current consumption and speed.

Although the output voltage level for the required 6-bit DAC does not need to be very precise, process variation should be minimized to the point that it is still distinguishable between different levels. In other words, the process variation should not exceed the voltage difference for each distinct output level. One of the advantages for this topology is that the process variation is only slightly affected by the switches DC resistances Most of the IC process variations are varied batch by batch; however, the DAC output voltage is based on ratio rather than the absolute value of a component. Thus, it should provide a very robust solution. Meanwhile, attention should be placed on local process variation, which may affect the resistors ratio. Hence, special layout technique should be deployed to minimize this effect.

5.3 Simulation Result and Implementation

A 6-bit DAC is designed for the pulse-shaping FIR filter to achieve a target roll off factor of 0.3235 for enhancing spectral efficiency. First, a 1 kΩ resistor is used for the R value in the DAC in Figure 5.1. Then, simulation for the process corner variation is run in order to ensure the topology provides a satisfactory result for generating the 64 levels that are distinguishable. Figure 5.2 shows one of the output voltage levels that experiences the most variation among all the process corner for the resistors and transistors, and extreme temperature of -10°C and 85°C combinations.

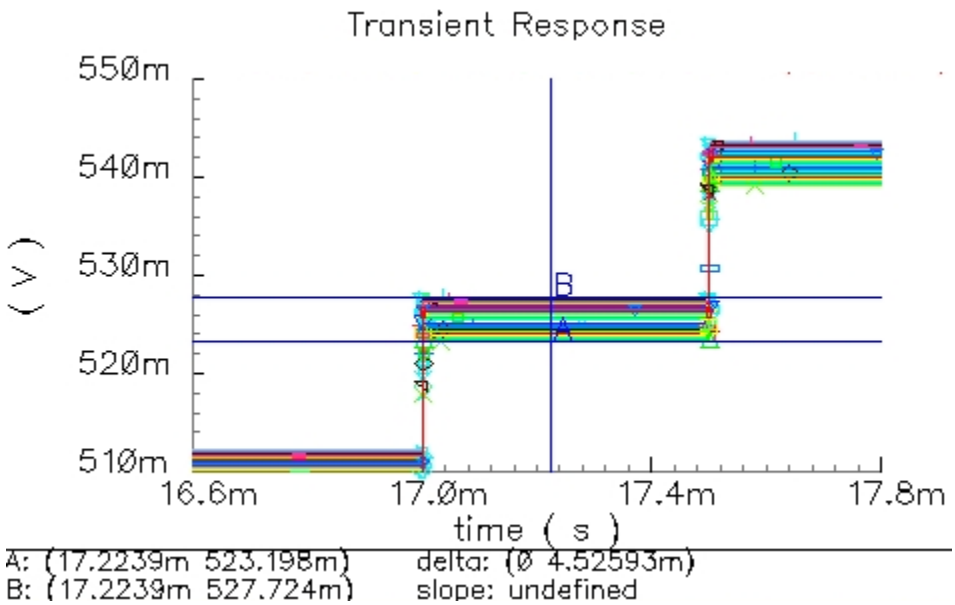

Figure 5.2. One of the 64 output voltage levels of the DAC with all the temperature and process variation combinations.

As indicated in Figure 5.2, the variation can vary between ±2.25mV. This variation is acceptable given that each voltage level output gap is about 15mV. As a result, this error is still within the mid-point level of each step.

In terms of integration, local variation has to be compromised with special resistor network layout. To minimize the effect of local variation, a uniform gradient of variation is assumed. In other words, the left and right, top and bottom resistors should experience the greatest variation relative to resistors close to the centroid of the network. As a result, in order to average out the effect for the extreme resistor values, resistor located at the upper left should be connect to the resistor located at the lower right. Thus, the average value will be similar to those placed at the center. Additionally, the width and length ratio for the resistor network should be close to 1 with all the resistors placed as close as possible. Figure 5.3 illustrates this layout technique implemented for the 6-bit DAC.

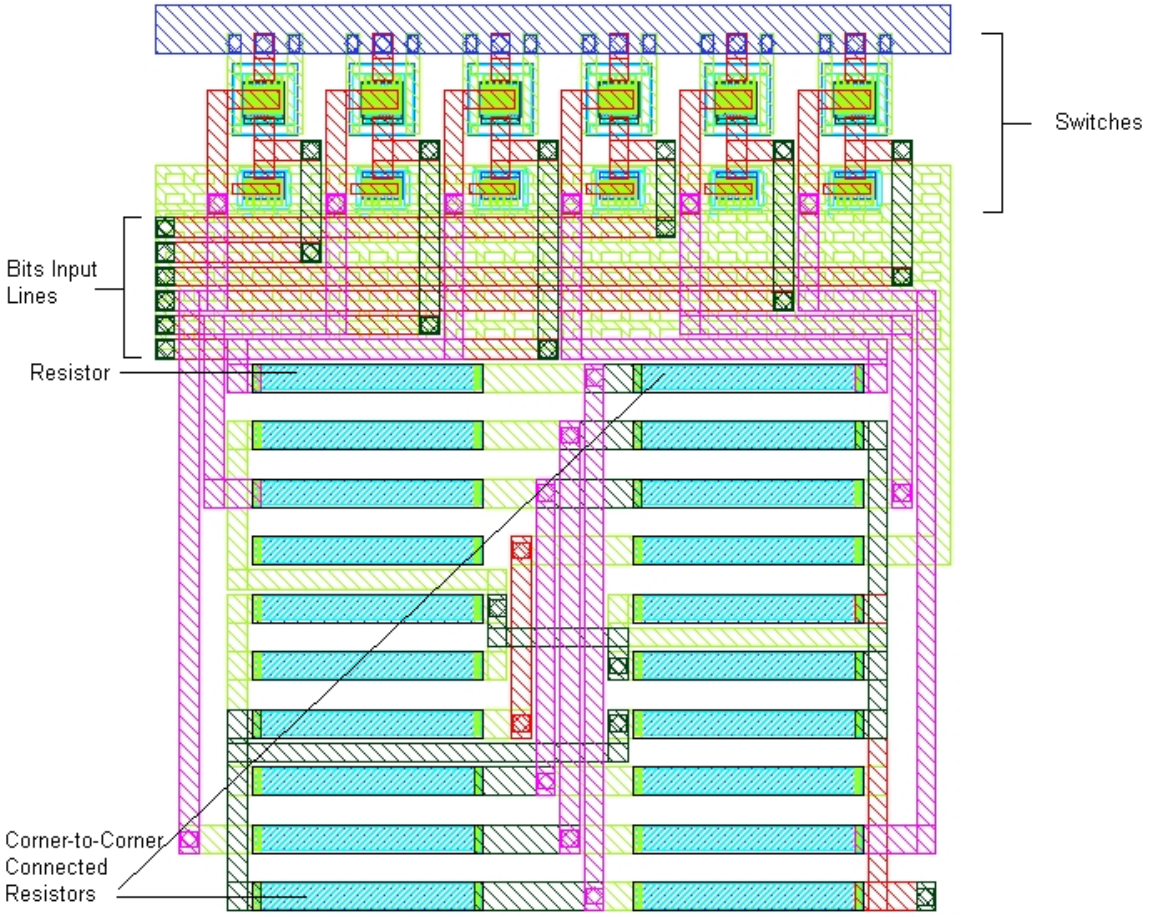

Figure 5.3. Initial 6-bit DAC layout.

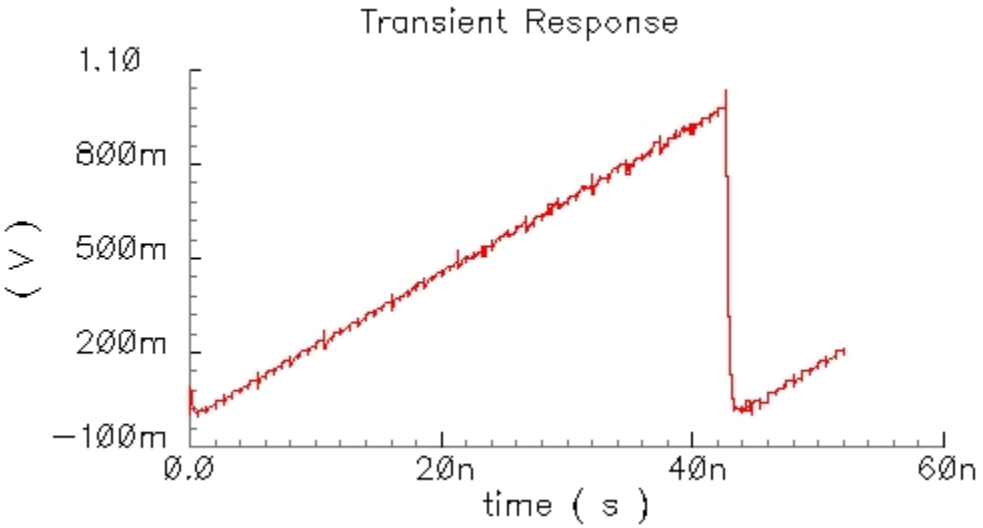

Figure 5.4. Initial 6-bit DAC with 64 distinct voltage output levels.

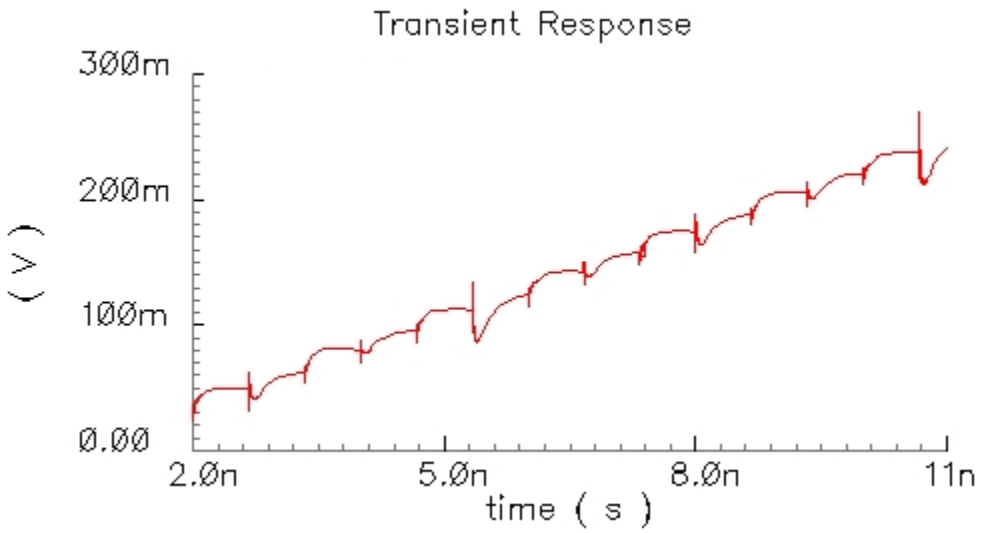

Figure 5.5. Zoom in view of the initial 6-bit DAC voltage output.

A parasitic extracted result, which includes associated capacitance and resistance, from the layout is used for the simulation of the design. Figure 5.4 shows 64 distinct voltage output levels that are generated from the DAC operating at 1.5 Gbps. A zoom in view provided in Figure 5.5 suggested that the DAC is barely operating at 1.5 Gbps with significant parasitic capacitance charging and discharging effect. The effect of the parasitic is reducing the speed from 2 GHz performance considerably.

This problem can be alleviated by optimizing wire width, occurrence of wire overlapping and metal layer chosen at crossing. At the same time, additional dummy resistors, which cause the usable resistors relatively closer to the centroid in the whole resistor network, can also be used as shown in Figure 5.6. These on-chip dummy poly resistors along the edge usually have a different image on the other side of the network.

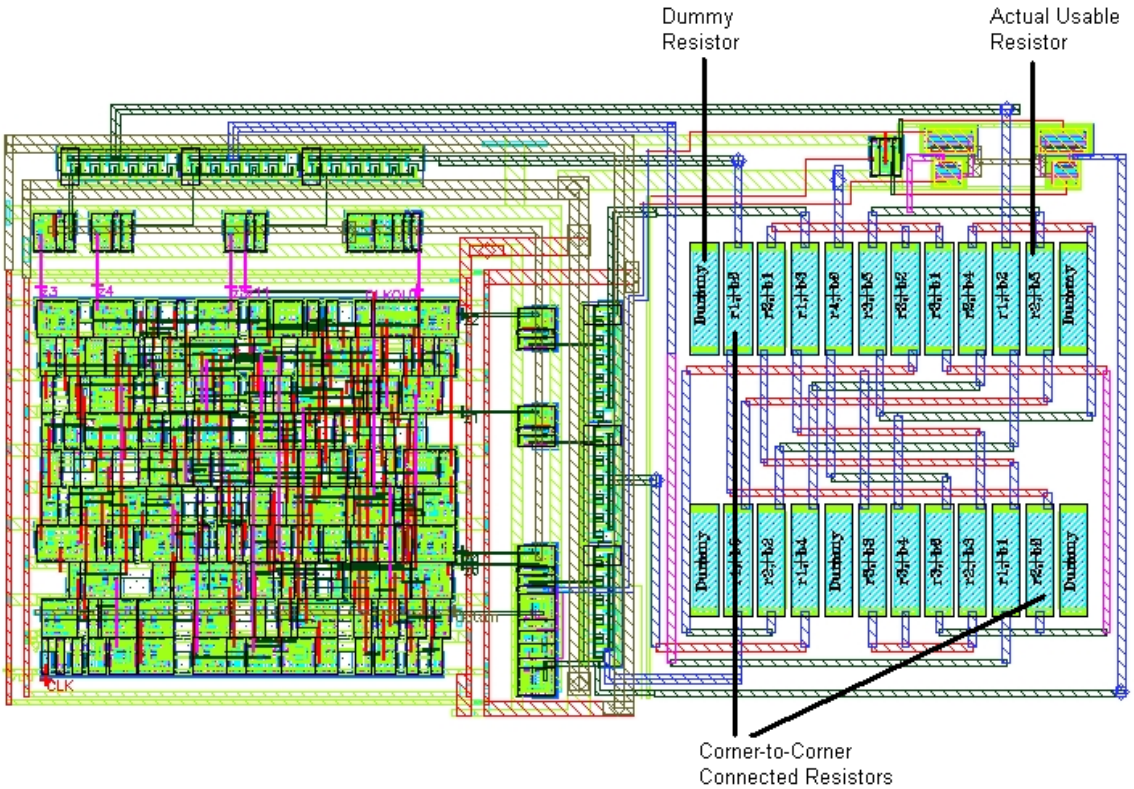

Figure 5.6. Pulse-shaping FIR filter layout (used with the courtesy from Dr. Bevin George Perumana , GEDC) implemented with special DAC layout techniques.

This DAC integrated in the pulse-shaping FIR filter is proven to be able to operate at a much higher frequency than the initial 6-bit DAC. From the measurement and analysis result, the pulse-shaping FIR filter is able to operate beyond 3 Gbps. Since the filter is implemented as a raised cosine pulse-shaping filter with an up sampling ratio of two, the DAC is capable of operating above 6 Gbps.

5.4 Summary

This basic R2R architecture with special layout techniques is proven to be able to operate at frequency up to GHz range. Its simplicity, performance and robustness against process variations show promising solution among other DAC topologies. This DAC

also lays an important fundamental framework towards analog and digital interface. Thus, transmitter front-end and digital circuit integration for a single SOC with CMOS process is possible.

CHAPTER 6

CONCLUSION

With the modeling techniques illustrated, a bidirectional support between well-round frequency domain simulator, *ADS*, and the industrial widely used time domain simulator, *Cadence*, is possible. From the s-parameter simulation, the models developed have been verified with different sizes of transistors, the power performance of the PA and the frequency response of the mixer. In other words, this powerful modeling technique is capable of performing accurate simulation from transistor level, component level to system level. It builds the fundamental design strategy for EHF domain design.

In addition to this bidirectional enabling technique for the front-end circuits, peripheral circuits, such as voltage regulator, bias circuits and DAC, have also illustrated a reasonable and robust solution for the 60 GHz on-off keying SOC CMOS transceiver. As for the regulator, with small on-chip size and off-chip component package size, a step-down power supply voltage is realized for digital circuits with reasonable efficiency. On the other hand, three solutions of bias circuits have been introduced. All of the solutions are proven to be insensitive to temperature and power supply voltage variations. Additionally, the third solution further improves the process insensitivity, which is the dominated variation factor for small feature size technology. Meanwhile, the DAC has also provided the necessary speed for operating between the digital filter and analog mixer. All of the combined factors reduce cost and design cycle.

This CMOS transceiver chip paves a road to future communication electronics that promises multi-giga bit transfer rate, such as wireless real time video streaming, in a low cost and small form-factor package.

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