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Low-voltage C_{60} organic field-effect transistors with high mobility and low contact resistance

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State-of-the-art C_{60} organic transistors are reported here by engineering the essential electrode/semiconductor and dielectric/semiconductor interfaces. By using calcium (Ca) as the source and drain electrodes, the width-normalized contact resistance ($R_C W$) at the electrode/semiconductor interface could be reduced to a constant value of 2 $k\Omega$ cm at a gate-source voltage (V_{GS}) of 2.6 V, for devices with channel lengths ranging from 25 to 200 μm. Channel transconductance is observed to follow channel length scaling, and charge mobility average value of 2.5 cm^2/Vs at $V_{GS}<5$ V is found independent of channel length within the studied range. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2993349]

Driven by the demands for low-cost, large-area flexible electronics with low processing temperatures, low-power organic field-effect transistors (OFETs) are of great interest. To date, a major challenge has been to improve the discrete device performance of *n*-channel OFETs. Electron mobilities as high as 4.9 and 6 cm^2/Vs have been reported by Itaka[1] and Anthopoulos[2] in C_{60} devices when operated at high voltage (>60 V). However, in the former report the on/off current ratio was inevitably reduced by the use of a pentacene (a well-known *p*-type semiconductor) layer at the dielectric/semiconductor interface. In the latter report, C_{60} was deposited by hot wall epitaxy requiring deposition temperatures as high as 250 °C. Recently, low-voltage C_{60} OFETs were demonstrated with a triple layer gate insulator of SiO_2/ZSO/SiO_2 (ZSO: zirconium-silicon oxide) with low level of hysteresis.[3] However, the threshold voltage of 1.9 V was high compared with the applied voltage of 5 V.

The electrical characteristics of OFETs are governed not only by the properties of the semiconductor material but also by the boundary conditions imposed by the device architecture. The most important factors related to above mentioned conditions to look at are the contacts and the interfaces. For example, the low electron mobility measured from *n*-channel OFETs is often due to the contact resistance imposed by the injection barrier between the organic semiconductor and the source/drain electrodes, sometimes *s*-shaped output curves are also reported due to the high injection barrier in *n*-type OFETs.[4] The issue of contact resistance in *n*-channel OFETs, which is far more serious than that of *p*-channel OFETs, has not yet been widely studied. On the other hand, electron trapping at the interface from carbonyl, hydroxyl, and silanol groups has been confirmed as a primary limiting factor for *n*-channel conduction and a major contribution to large threshold voltage.[4,5]

In this letter, state-of-the-art *n*-channel transistors with commercially available C_{60} are reported by engineering the essential electrode/semiconductor and dielectric/semiconductor interfaces. The width-normalized contact resistance ($R_c W$) has been reduced to a constant value of 2 $k\Omega$ cm at a gate-source voltage (V_{GS}) of 2.6 V for the channel lengths ranging from 200 down to 25 μm by using a low work function metal (Ca) as the source/drain electrode, leading to excellent electrical characteristics. Besides high electron mobility with an average value of 2.5 cm^2/V s, overall high electrical performance and stability at low operating voltages are demonstrated by using a combination of Al_2O_3:BCB (gate dielectric)/C_{60} (semiconductor)/Ca (source/drain electrodes) in the device architecture. It not only enables higher performance parameter in a wide range of channel lengths at a low operating voltage, but also significantly improves the electrical stability and reproducibility.[6] The active C_{60} layers were formed using physical vapor deposition (PVD) with the substrates kept at room temperature, which would enable the fabrication of C_{60} devices and circuits on plastic substrates. The combined operating properties of these OFETs are comparable to the best reported *p*-channel OFETs (Ref. 7) and outperform amorphous silicon thin-film transistors (TFTs).

OFETs were fabricated on heavily *n*-doped silicon substrates (also serve as gate electrodes) with a top-contact geometry. A 100 nm thick layer of Al_2O_3 as a gate insulator was formed by atomic layer deposition: a deposition technique that allows for the deposition of highly conformal, defect-free dielectric layers at lower temperature.[8,9] To better control the interfacial properties at the dielectric and C_{60}, the Al_2O_3 dielectric surface was passivated with a thin buffer layer of BCB (Cyclotene™, Dow Chemicals). Crosslinkable BCB can provide a high-quality hydroxyl-free interface to the organic semiconductor with a high dielectric breakdown strength exceeding 3 MV/cm.[6,10] The total capacitance density (C_{OX}) measured from parallel-plate capacitors with 12 varying contact areas was 50 nF/cm^2. The leakage current density through the gate dielectrics was negligible (below 10^{-8} A/cm^2) under an applied field of 2 MV cm^{-1}. Sublimed grade C_{60} (Alfa Aesar) was purified using gradient zone sublimation prior to deposition. A 50 nm thick film of C_{60} was deposited at a rate of 0.6 Å/s using PVD at a constant pressure of 5×10^{-8} Torr while the substrates were held at room temperature. Subsequently, without breaking vacuum, the deposition of 150 nm thick top source/drain electrodes was done through a shadow mask containing the

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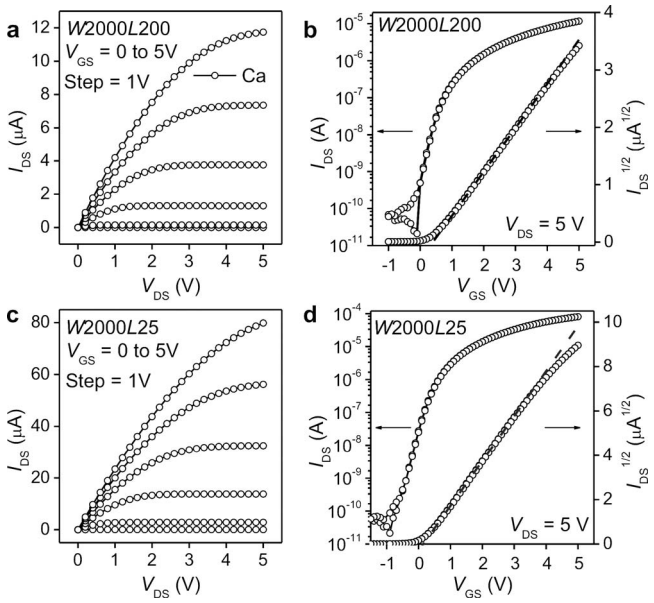

FIG. 1. Comparison of output and hysteretic transfer characteristics of [(a) and (b)] long-channel (L=200 μm/W=2000 μm) and [(c) and (d)] short-channel (L=25 μm/W=2000 μm) C_{60} OFETs.

desired patterns. Devices had a wide range of width versus length ratios, between 2.5 and 80, with channel lengths ranging from L=25 to 200 μm and channel widths ranging from W=500 to 2000 μm. With a low work function of 2.9 eV, Ca was chosen for the source/drain electrodes to facilitate electron injection into the lowest unoccupied molecular orbital (LUMO) (3.6 eV) level of C_{60} (Refs. 11 and 12) since there is no barrier (Φ_B) between the C_{60} LUMO level and the Ca Fermi level (E_F) according to the conventional Mott–Schottky model. The electrical measurements were performed in a N_2-filled glovebox (O_2, H_2O<0.1 ppm) at normal pressure (1 atm) in the dark using an Agilent E5272A source/monitor unit.

Representative output and hysteretic transfer characteristics are compared in Fig. 1 for both long-channel devices (L=200 μm) [Figs. 1(a) and 1(b)] and short-channel devices (L=25 μm) [Figs. 1(c) and 1(d)] with the same channel width W=2000 μm. The electrical parameters: field-effective mobility (μ), threshold voltage (V_T), subthreshold slope (S), and on/off current ratio ($I_{on/off}$), are summarized and compared in Table I. In this work, the maximum mobility values from the dependence of gate bias in the saturation regime were used to characterize C_{60} OFETs. The threshold voltage V_T was determined at the maximum of the second derivative of I_{DS} with respect to V_{GS} in the linear regime

TABLE I. Summary of the electrical parameters for C_{60} transistors with L=200 or 25 μm and W=2000 μm. Each data point represents the mean value and the error bars represent the s.d. calculated from two identical devices. μ is the field-effect mobility, V_T is the threshold voltage, S is the subthreshold slope, and $I_{on/off}$ is the on/off current ratio.

	μ (cm^2/V s)	V_T (V)	S (V/decade)	$I_{on/off}$ ($\times 10^6$)
W=2000, L=200 (W/L=10)	2.3±0.2	0.2±0.1	0.1±0.04	1.0±0.3
W=2000, L=25 (W/L=80)	2.3±0.1	0.1±0.1	0.3±0.03	4.0±0.3

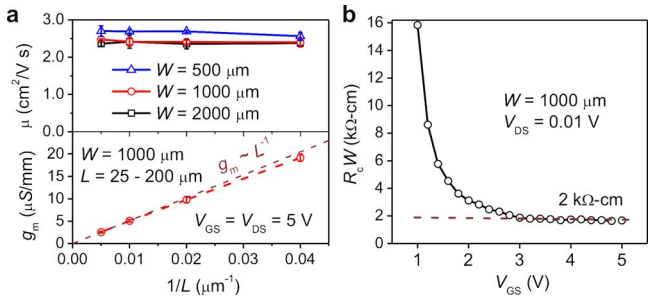

FIG. 2. (Color online) (a) Effect of channel scaling on mobility μ, transconductance g_m in n-channel C_{60} OFETs. Each data point represents the mean value and the error bars represent the s.d. calculated from two to four identical devices (two for W=2000 μm and four for W=500 and 1000 μm). (b) Contact resistance analysis for n-channel C_{60} OFETs with a channel width W=1000 μm and a channel length L ranging from 25 to 200 μm. Width-normalized contact resistance R_CW is shown as a function of gate-source voltage V_{GS} for a drain-source voltage V_{DS}=0.01 V.

where V_{GS} (5 V) is much larger than V_{DS} (0.05 V).[13] Subthreshold slopes (S) and on/off current ratios ($I_{on/off}$) are also extracted from the transfer characteristics. For each type of transistors, two to four devices with identical geometry were measured to obtain a mean value and standard deviation (s.d.). As shown Figs. 1(b) and 1(d), the devices show no hysteresis in the transfer characteristics. As detailed in the previous report,[6] with BCB at the interface, C_{60} OFETs also show excellent electrical stability under both repeated and continuous dc stress. For long-channel devices (W=2000 μm/L=200 μm) as shown in Figs. 1(a) and 1(b), devices show excellent performance with a high mobility of 2.3±0.2 cm^2/V s, V_T close to zero, subthreshold slope S around 0.1 V/decade. When the channel length is scaled down to 25 μm, devices start to show short-channel effects, such as a less pronounced saturation of I_{DS}, earlier turn-on and higher subthreshold voltage,[14] as shown in Fig. 1(d). However, unlike in most n-channel OFETs, the mobility of the devices with Ca contacts remains unaffected with maximum I_{DS} increased by almost eight times.

To investigate the dependence of mobility on channel length, field-effect mobilities of devices with channel width W=500, 1000, and 2000 μm are statistically plotted over the inverse of channel length (L^{-1}) in Fig. 2(a). The transconductance g_m, calculated in the saturation regime as a function of the inverse of channel length (L^{-1}) is also plotted in Fig. 2(a), where a g_m larger than 15 μS/mm was achieved for the short-channel devices with L=25 μm. With no Schottky barrier between Ca source/drain electrodes and C_{60}, the mobility for devices with Ca becomes independent of channel length in the range of L=200 μm down to 25 μm, as seen in Fig. 2(a). Hence, devices with Ca as source/drain contacts show channel scaling as in metal-oxide-semiconductor FET (MOSFET)–like characteristics where g_m becomes proportional to L^{-1}.

To gain a better understanding of the contact effect on the mobility, the width-normalized contact resistance (R_CW) of C_{60} transistors with Ca contacts was extracted using a transmission line method, as shown in Fig. 2(b). The contact resistance was calculated at a low drain-source voltage (V_{DS}) of 0.01 V for V_{GS} values ranging from 1 to 5 V. In general, there are two contributions to contact resistance in top-contact OFETs: the resistance of the metal contact/organic interface and the resistance of organic film itself from the

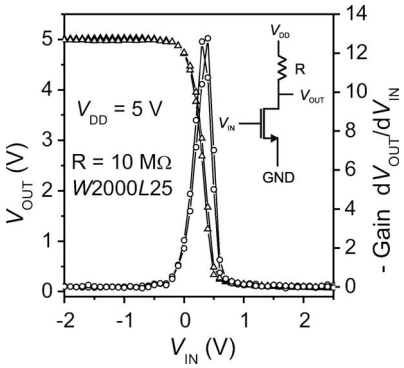

FIG. 3. Voltage transfer characteristics and dc gain of a resistance-load inverter operated under a supply voltage V_{DD} of 5 V with a C_{60} OFET (W=2000 μm/L=25 μm) and a resistor (R=10 MΩ).

metal to the channel. The former can be reduced by tuning the Fermi level (E_F) of the metal with V_{GS} to lower the injection barrier and the latter can be reduced by induced charge density in the accumulation regime with V_{GS}. In the case of Ca, the contact resistance drops drastically and rapidly reaches a constant value of 2 kΩ cm by applying only 2.6 V, which is in contrast to the tens of volts needed for most OFETs. The residual contact resistance (which is no longer modulated by the gate bias) could be governed by the intrinsic conductivity of C_{60} films. The low residual contact resistance achieved at extremely low V_{GS} is attributed to the combination of a low injection barrier between C_{60} and Ca and a high intrinsic mobility of C_{60} (therefore high conductivity).

Figure 3 exhibits the static behavior of resistive-load inverters along with a scheme of the device (inset), which is composed of C_{60} OFET and a load resistor (load resistance R=10 MΩ). With a low threshold voltage, the inverter operates at a low supply voltage V_{DD} of 5 V and the inverter shows an almost ideal transfer curve with a sharp output voltage switching between 5 ("high") and 0 V ("low"). No hysteresis was observed during the inverter action, reflecting excellent threshold voltage stability in our OFETs. The measured voltage gain $-dV_{out}/dV_{in}$, an important parameter for subsequent stage switching, was as large as 13. This gain obtained at low supply voltage directly benefits from low threshold voltage and high bias current resultant from high mobility and low contact resistance in our C_{60} OFETs. The parameter exhibits real potential of our OFETs for logic circuits operating at low voltage.

In summary, we have fabricated high-performance n-channel C_{60}-based OFETs with MOSFET-like electrical characteristics, high electron mobilities of 2.3 $cm^2/V\,s$, threshold voltages near zero (V_T<1 V), low subthreshold slopes (S<0.3 V/decade), on/off current ratios larger than 10^6, and maximum transconductance g_m larger than 15 μS/mm. This overall excellent performance was obtained by engineering the dielectric/organic semiconductor interface and by reducing the contact resistance at the metal contact/organic semiconductor interface. Finally, a simple resistive load organic inverter operating at low voltages (~5 V) was also demonstrated with a high dc gain and without hysteresis in its transfer curve.

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