LOW-VOLTAGE SOFT-SWITCHING SOLID-STATE TRANSFORMER (S4T) ENABLED BY THE SYNCHRONOUS REVERSE BLOCKING SWITCH

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LOW-VOLTAGE SOFT-SWITCHING SOLID-STATE TRANSFORMER (S4T) ENABLED BY THE SYNCHRONOUS REVERSE BLOCKING SWITCH

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"Human influence on the climate system is clear, and recent anthropogenic emissions of greenhouse gases are the highest in history. Recent climate changes have had widespread impacts on human and natural systems. Warming of the climate system is unequivocal, and since the 1950s, many of the observed changes are unprecedented over decades to millennia. The atmosphere and ocean have warmed, the amounts of snow and ice have diminished, and sea level has risen."

Intergovernmental Panel on Climate Change

"To truly transform our economy, protect our security, and save our planet from the ravages of climate change, we need to ultimately make clean, renewable energy the profitable kind of energy"

Barack Obama

To my parents and sister

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SUMMARY

The objective of this research is to demonstrate a high-efficiency, low-voltage Soft-Switching Solid-State Transformer (S4T) enabled by the Synchronous Reverse Blocking (RB) Switch, a patent-pending method to seamlessly integrate dual-active-switch structures into the S4T topology to minimize conduction losses in low-voltage, high-current applications. The S4T is a universal converter with the ability to interface single-phase, three-phase, and DC sources, and features bidirectional power transfer, buck-boost functionality, high-frequency isolation, low electromagnetic interference (EMI) through controlled dv/dt, and zero-voltage switching (ZVS) operation for all main devices over the entire load range to minimize switching losses. Significant success has been achieved in applying the S4T to industrial voltages (600 VAC and 1000 VDC) and medium voltage AC and DC (MVDC and MVAC) through the use of 3.3 kV silicon-carbide (SiC) devices and series connection of multiple S4T modules.

However, applying the topology to interface with low-voltage, high-current sources and loads has been challenging due to the high conduction losses associated with conventional reverse blocking switch structures composed of one active switching device, such as an IGBT or a MOSFET, in series with a diode, usually a SiC Schottky diode. Replacing the conventional RB switch structure with a dual-active-switch configuration, specifically one composed of two low-$R_{DS(ON)}$ N-channel MOSFETs, presents an opportunity to significantly reduce semiconductor conduction losses and increase converter efficiency. However, as the PN-junction MOSFET body diode replaces the series SiC Schottky diode of conventional RB structures, body diode reverse recovery must be mitigated to prevent large device voltage stresses, increased device losses, additional EMI, and reduced converter reliability.

This thesis first presents the device-level validation of the Synchronous Reverse Blocking Switch within the S4T, showcasing the ability of the method to significantly reduce conduction losses while also evidencing benign reverse recovery behavior. Key contribu-

tions include the design of a simple and robust gate control method and the characterization of the switching dynamics of the underlying dual-MOSFET RB switch structure within the unique switching environment of the S4T. Then, the patent-pending Synchronous RB Switch is introduced, pairing the dual-MOSFET RB switch structure with custom gate drive and protection circuitry that leverages the S4T switching environment to eliminate parasitic body diode reverse recovery, mitigate the complexity of controlling the two active switch gates, and enable simple fault protection through dedicated hardware at the gate driver level. Experimental results are presented to demonstrate that the Synchronous RB Switch enables the conduction loss reduction of the dual-MOSFET structure to be exploited with minimal additional cost and no additional control complexity when compared to a conventional RB switch structure. This analysis has been published in the proceedings of the 2020 IEEE Energy Conversion Congress and Exposition (ECCE).

System-level validation of the Synchronous RB Switch is conducted through the design and performance analysis of a low-voltage, high-current S4T bridge intended to interface with a variety of low-voltage sources, including lithium batteries, photovoltaic (PV) panels, and fuel cells. The low-voltage S4T bridge is critical in enabling the S4T topology to address upcoming low-voltage power conversion needs, representing large technology and market opportunities.

Two specific low-voltage S4T applications unlocked by the Synchronous RB Switch are presented and analyzed. The first application, referred to as the AC Cube, is a single-stage multi-port structure that converts power from two low-voltage DC sources, PV and a 48 VDC battery, into a 120 VAC single-phase output, with intended use in rapid deployment AC power sources following grid contingencies. Due to the current-source nature of the topology, parallelization on the 120 VAC side enables the construction of modular microgrids. An arbitrarily scalable microgrid based on AC Cube modular building blocks represents a large opportunity to deliver electricity solutions to off-grid and poor-grid communities, and is a key avenue of future work.

The second low-voltage S4T application converts power from a single DC input, a 48 VDC battery, and produces a three-phase 480 VAC output, enabling a radical, touch-safe, modular electric vehicle (EV) powertrain. Due to the bidirectional power flow capability of the topology, the second low-voltage S4T variant can also be used for power delivery applications in data centers and upcoming 5G access points. The design of this second low-voltage S4T variant has been published in the proceedings of the 2020 IEEE Transportation Electrification Conference & Expo (ITEC).

CHAPTER 1
INTRODUCTION AND BACKGROUND

As the world's nations grow to more fully embrace the impacts of climate change and the inherent non-sustainability of certain ways of modern life, there is a significant trend towards technologies that enable more sustainable generation and consumption of energy. Large changes are occurring across practically every social and economic cross section, with critical examples including the push to increase electrification of transportation, the reduction of carbon intensity of manufacturing, increased grid penetration of renewable energy technologies, a growing realization of the need to reduce the greenhouse gas intensity of conventional agricultural techniques, and an increased focus on residential and commercial building energy efficiency. These shifts in technology are rooted in science and economics, underpinned by the growing body of unequivocal evidence linking human activity to the observed degradation of the Earth's natural atmospheric and ecological systems [1] and the improving cost-effectiveness of renewable energy resources and high-efficiency end-use technologies [2, 3]. Importantly, the technology shifts also stem from a uniquely human desire to unlock pathways of human life that are sustainable not only for our foreseeable posterity, but are sustainable on the order of centuries to millennia, with the potential to allow human civilization to grow and flourish indefinitely.

The field of power electronics is a key enabler of the push towards a sustainable energy future. The past 60 years have produced tremendous technical achievements, including the invention and refinement of efficient power semiconductor devices, deep explorations into numerous power converter topologies and an evaluation of their trade-offs, and significant growth in the grid integration of low-cost renewable energy technologies whose prices continue to decrease [4]. As the field of power electronics matures and as converter topologies reach their practically achievable efficiency limits, new research directions include investi-

gations of increasingly integrated conversion functionalities, minimization of converter cost to enable ubiquitous market uptake, a broader consideration of converter mission profiles for system-level performance optimization, and an embrace of wide-bandgap semiconductor technologies, namely gallium nitride (GaN) and silicon-carbide (SiC), that promise to extend the field of power electronics past the switching frequency and breakdown voltage limitations of the industry's current workhorse, silicon (Si).

Within the field of power electronics, one specific area of growth has been the low-voltage power conversion market, which has seen significant expansion due to the exponential growth of both residential and utility-scale photovoltaic systems [5, 6]. Between 2009 and 2019, the total installed capacity of PV systems in the United States increased from 1.2 GW to 74.8 GW, representing more than a 60-fold increase in just one decade. Over the same time period, the cumulative capacity of US residential solar has grown from 422 MW to 15.4 GW, a 36-fold increase [7]. In addition, the decreasing costs of lithium-ion batteries have increased the cost-effectiveness of pairing PV installations with energy storage to enable backup power, peak-load shifting, and electricity price arbitrage functions. Market forecasts from Wood Mackenzie estimate that by 2025, more than one-third of new residential solar systems and more than one-quarter of new non-residential solar systems will be paired with energy storage [8]. Key products related to this effort on the utility scale include the Tesla Powerpack and Megapack and the Fluence Gridstack, while product offerings at the residential level include the Tesla Powerwall, the Sonnen ecoLinx, and the Panasonic EverVolt.

As the limits of performance, power density, and cost of existing power converter designs related to photovoltaic and energy storage applications are reached, there exists a growing market opportunity for increasingly integrated and feature-rich converter topologies. For instance, the concept of a high-efficiency, isolated, multi-port power converter for the upcoming shift to a ubiquitous 48 VDC bus voltage, with the ability to interface both standard residential AC voltages (120 or 240 VAC) and touch-safe low-voltage (<60 VDC)

sources, such as commonly available photovoltaic panels and lead or lithium batteries, is absent from current market offerings.

To demonstrate the market need and opportunity for such a power converter, consider the following power conversion applications requiring low-voltage interfaces. Upcoming 5G telecommunications infrastructure and data centers require conversion between 480 VAC and 48 VDC, and may additionally utilize 48 VDC batteries for backup power and fault ride-through capabilities [9]. Mild hybrid vehicles, featuring engine quick-start to reduce idling fuel consumption and regenerative breaking to recuperate kinetic energy, have emerged as low-cost modifications to vehicle designs that can improve fuel economy by 10% [10]. This functionality requires conversion from 48 VDC, often from a lithium-ion battery, to 480 VAC to drive the hybrid traction motor. Some automotive suppliers such as Continental are considering 48 VDC systems for standard and plug-in hybrid applications rated at 30 kW [11]. Furthermore, a modular, high efficiency 48 VDC to 480 VAC power converter would enable the realization of an intrinsically safe, low-voltage EV powertrain that could mitigate the critical risk of high voltage DC shock pervading all current and planned EV designs [12].

In addition to the power conversion needs mentioned above, the need for modular, rapid-deployment AC power sources has been evidenced by the forced grid outages following the 2019 wildfires in California [13] and the widespread, long-duration ($>$120 days) loss of electricity in Puerto Rico due to Hurricane Maria in 2017 [14]. These examples particularly evidence the need for conversion from easily procurable low-voltage sources (photovoltaic panels and batteries) to standard mains voltage levels (120 VAC or 240 VAC). Given that the severity and frequency of extreme weather events and the related risks of grid contingencies will increase until global carbon emissions abate [1, 15], this need will be further pronounced in the years to come.

The Soft-Switching Solid-State Transformer (S4T), initially proposed in 2016 [16], is an isolated, multi-port, buck-boost converter that can address many of the aforementioned

needs for highly integrated, efficient, and feature-rich power conversion. The S4T is a universal converter with the ability to interface single-phase, three-phase, and DC sources, and features bidirectional power transfer, buck-boost functionality, high-frequency isolation, low electromagnetic interference (EMI) through controlled dv/dt, and zero-voltage switching (ZVS) for all main devices over the entire load range. Significant success has been achieved in applying the S4T to industrial power conversion applications at 600 VAC and 1000 VDC, and to medium voltage AC and DC (MVDC and MVAC) applications, such as grid power flow controllers and medium voltage solid-state transformers, through the use of 3.3 kV SiC devices and series stacking of modules [17–22]. However, applying the topology to interface with low-voltage, high-current sources and loads has been challenging due to the high conduction losses of conventional reverse blocking (RB) switch structures, required due to the current-source nature of the topology. This challenge has thus far prevented the S4T from being applied to address the growing market need for highly integrated, efficient, and feature-rich power converters with low-voltage interfaces.

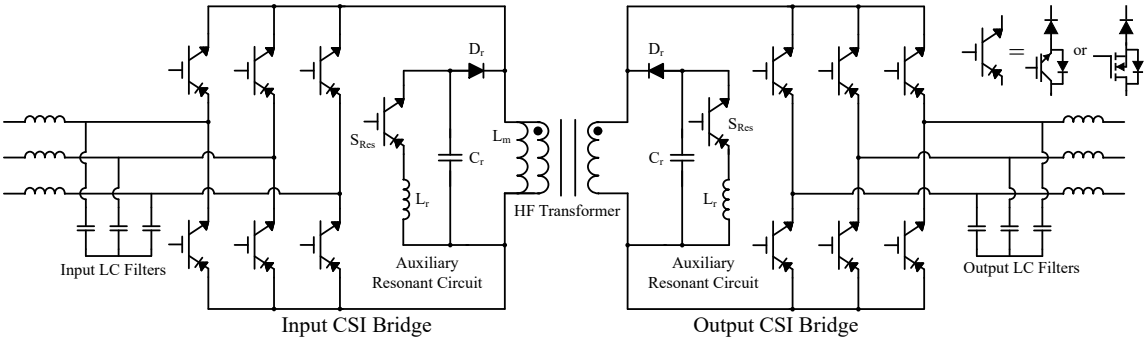


Figure 1.1: Standard 3-phase to 3-phase bidirectional configuration of the S4T.

To illustrate the challenge of achieving high efficiency in low-voltage S4T applications, consider the standard 3-phase to 3-phase AC configuration of the S4T topology presented in Fig. 1.1. Conventionally, each RB switch is formed by the series combination of an active switching device (an IGBT or MOSFET) and a diode, generally a SiC Schottky diode due to minimal reverse recovery charge. In applications where the channel voltage drop of a MOSFET is significantly smaller than a diode voltage drop, significant converter losses

originate from the conduction loss of the series diodes. This scenario is especially common in low-voltage, high-current applications where silicon MOSFETs exhibit a voltage drop an order of magnitude lower than similarly rated diodes. To reduce the conduction loss, the series diode of conventional RB switch structures can be replaced by a second MOSFET, yielding a dual-MOSFET RB switch.

While the steady-state conduction loss reduction from the dual-MOSFET structure is apparent, all negative consequences of the structure must be mitigated to have a truly viable alternative to the robust conventional RB switch structures. Importantly, since the PN-junction body diode of the MOSFET replaces the series SiC Schottky diode of conventional RB structures, the reverse recovery of the body diode must be mitigated to avoid reverse recovery induced device voltage stresses, additional EMI, and converter reliability degradation. A novel, patent-pending gate control methodology for dual-active-switch structures that uniquely leverages the switching environment of the S4T has been designed and validated to address the trade-offs stemming from the dual-MOSFET RB switch structure. Referred to as the Synchronous Reverse Blocking Switch, the gate control methodology is implemented within a dedicated, low-cost gate driver and enables significant conduction loss reduction, mitigation of body diode reverse recovery, and simplification of the control requirements to enable a single-gate-signal interface per RB switch position and integration into standard power module designs. The Synchronous RB Switch enables a seamless integration of dual-active-switch structures into the S4T topology, making the S4T a competitive option to address upcoming low-voltage power conversion opportunities.

This work presents the device-level validation of the gating principles and switching dynamics of the Synchronous Reverse Blocking Switch, and system-level validation of a high-efficiency, low-voltage S4T bridge enabled by the novel, dual-active-switch gating technique. An overview of the following chapters is presented as follows. Chapter 2 introduces the concept of the low-voltage S4T and presents the trade-offs of the use of the Synchronous RB Switch built around an RB switch structure composed of two N-channel

MOSFETs. Chapter 3 presents the device-level experimental validation of the Synchronous RB Switch, demonstrating reverse recovery mitigation within a switching environment that emulates true S4T operation. Chapter 4 presents the experimental validation and performance measurement of a low-voltage S4T bridge built to verify the conduction loss reduction and benign reverse recovery properties of the Synchronous RB Switch. The design of an integrated, low-cost, and single-gate-signal driver circuit specifically suited to the S4T is also presented. Lastly, Chapter 5 presents the conclusion and directions for future work.

CHAPTER 2

LOW-VOLTAGE SOFT-SWITCHING SOLID-STATE TRANSFORMER (S4T)

2.1 Introduction & Challenges

The Soft-Switching Solid-State Transformer (S4T) introduced in [16] proposed a unique, single-stage, and self-contained soft-switching current-source topology with attractive features including high-frequency isolation, zero-voltage switching across the entire load range with controlled dv/dt, flexible AC/DC inputs and outputs, voltage buck-boost conversion capabilities, and bi-directional power flow. To realize the three-quadrant reverse blocking (RB) switch necessary due to the current-source nature of the topology, the switch positions in the S4T typically consist of the series connection of an active switch, in the form of a Si IGBT or SiC MOSFET, and a SiC Schottky diode, preferred over traditional Si diodes due to their characteristic of zero reverse recovery charge. These conventional RB structures are shown in Fig. 2.1(a).

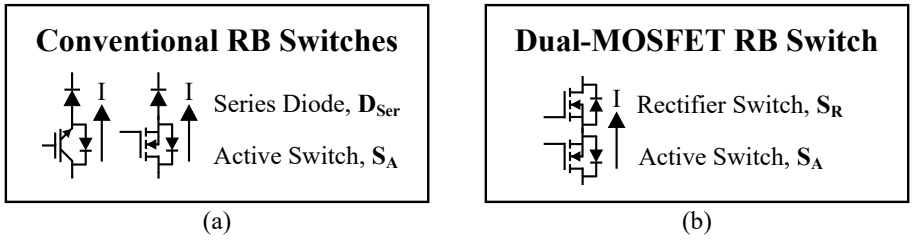


Figure 2.1: (a) Conventional RB switch structures, where the series diode is often a SiC Schottky diode. (b) Dual-MOSFET RB switch structure, showing the direction of current flow through the structure, and the active and rectifier switch designations.

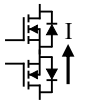
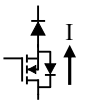
Despite the apparent conduction loss penalty caused by the series connection of two devices per switch position, common to all current-source converter topologies, the virtual elimination of switching losses in the S4T and the removal of the device in series with the transformer in the original S4T configuration [22] yield excellent efficiency levels, comparable to or exceeding efficiencies of traditional voltage-source converter counterparts in the

voltage ranges considered thus far.

The S4T topology is now being considered for high-current, low-voltage applications, to interface with touch-safe 48 VDC sources (lithium batteries and photovoltaic panels) and to address upcoming low-voltage power conversion needs. Some examples include 48 VDC hybrid vehicle systems, intrinsically safe low-voltage modular electric vehicle (EV) powertrains [12], power delivery for 5G wireless access points and data centers [9], and rapid deployment AC power sources for use after grid contingencies and in scalable, modular microgrids.

In this new application space, ultra-low $R_{DS(ON)}$ Si MOSFETs are routinely available at competitive price-points from multiple vendors and in appropriately high-current ratings. They can replace the Si IGBT to significantly reduce the voltage drop across the active device. However, the forward voltage drop of the series low-voltage diode remains, similar to that of the higher-voltage class diodes used in S4T applications thus far, and is responsible for most of the conduction loss in the switch position. The conduction loss of the MOSFET plus series diode RB structure is quantified in Table 2.1, scaled appropriately for a 3 kW 48 VDC S4T bridge. For this target application, the device current and voltage ratings are 100 A and 100 V, respectively. At 100 A of current conduction, and considering a commercially-available 1.3 mΩ Si MOSFET, the conduction voltage drop of the MOSFET is a mere 0.13 V while the forward voltage of the series SiC diode is 1.45 V at the lowest. The total conduction losses of the MOSFET plus series diode RB structure translate into a 5.3% efficiency loss in the 48 VDC bridge alone, with over 92% of these losses taking place in the series diode. This is a well-known challenge in high-current, low-voltage applications and has motivated the development of synchronous rectifier configurations in conventional voltage-source converters [23], and more recently, similar structures for standard current-source inverters [24–28], all with the objective of eliminating the conduction loss of the series diode.

Table 2.1: Comparison of a Conventional MOSFET Plus Series Diode Reverse Blocking Switch and the Dual-MOSFET Reverse Blocking Switch

RB Switch Configuration	Circuit Symbol	Forward Conduction Voltage Drop @ 100A	Conduction Loss @100A	Voltage Blocking Capability	Reverse Recovery Charge
Dual-MOSFET Infineon IAUT300N10S5N015		$2 \times 1.3\text{m}\Omega \times 100\text{A}$ **= 0.26V**	**26W**	100V	166nC
MOSFET and Series Diode Cree CVFD20065A		SiC Schottky: 1.45-1.95V MOSFET: $1.3\text{m}\Omega \times 100\text{A} = 0.13\text{V}$ Combined: **1.58-2.08V**	**158W**	100V	SiC Schottky: 0nC

In this work, a dual-MOSFET RB switch structure, composed of two N-channel MOSFETs in a common-source configuration as shown in Fig. 2.1(b), is paired with a robust and simple gate drive methodology that uniquely leverages the operating principles and switching environment of the S4T topology to exploit the conduction loss reduction of the dual-MOSFET structure while mitigating the concerns of reverse recovery and sensitivity to shoot-through faults that typically plague this kind of structure.

In the dual-MOSFET RB switch configuration, the body diode of the rectifier switch, S_R, acts as the series diode of the conventional RB switch. To reduce conduction loss, the general philosophy is to turn the MOSFET channel of switch S_R on to minimize the conduction time of the body diode. The critical trade-off in replacing the series SiC Schottky diode of conventional RB structures with a Si MOSFET lies in the reverse recovery inherent to the Si MOSFET's PN-junction body diode. Inadequate mitigation of body diode reverse recovery would lead to large device voltage stresses, increased device losses, additional EMI, and reduced converter reliability.

The patent-pending Synchronous Reverse Blocking Switch combines the dual-MOSFET RB structure with a dedicated, low-cost gate driver and protection circuitry designed to enable significant conduction loss reduction, mitigation of the reverse recovery of the S_R body diode, and simplification of the control requirements to enable a single-gate-signal interface per RB switch position and integration into standard power module designs. This work presents the theory of operation and experimental validation of the Synchronous RB Switch

and demonstrates its potential to unlock a high-efficiency S4T for wide scale application in upcoming low-voltage power conversion needs. Key low-voltage S4T topology examples unlocked by the novel, dual-active-switch gating technique are presented in the following section.

2.2 Topology Examples

2.2.1 Rapid Deployment AC Power Sources

The growing risk of climate change induced grid contingencies has increased the market need for rapid deployment AC power sources that can interface with low-voltage, touch-safe, and commonly available DC power sources [13–15]. The Synchronous RB Switch enables a low-voltage S4T variant that can be applied to address this market need. The topology, referred to as the AC Cube, is presented in Fig. 2.2. The implementation shown features two DC ports, one for PV and another for a battery, both at 48 VDC. The AC bridge depicted is rated at 120 VAC single-phase, although the rating can be easily increased to 240 VAC through selection of AC bridge devices with appropriate breakdown voltage. The AC bridge can similarly be adapted to produce three-phase voltages (208, 240, or 480 VAC).

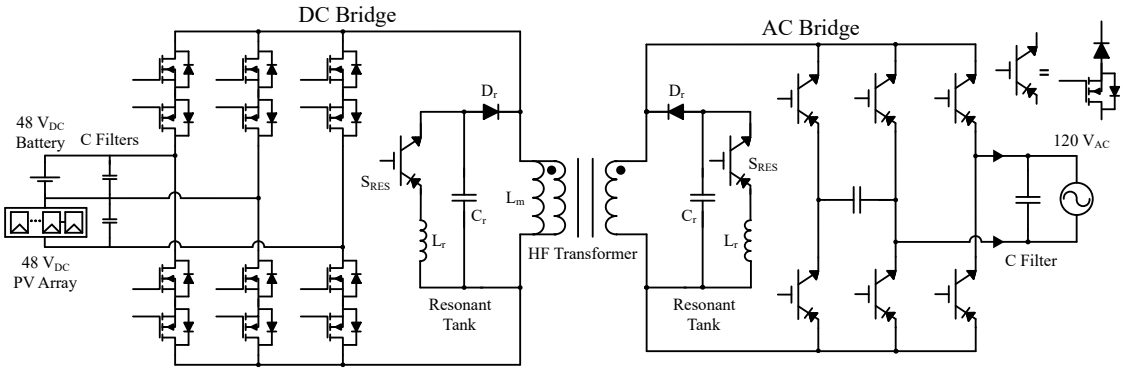


Figure 2.2: 1 kW, 48 VDC (dual DC Port) to 120 VAC S4T with intended use as a rapid deployment AC power source following grid contingencies.

Due to the bidirectional power flow capability of the AC Cube, several operating modes exist. For instance, after a grid contingency, easily obtainable photovoltaic panels can be connected to the PV port to charge the batteries. When needing to serve an AC load, the two DC sources are both used to produce the 120 VAC output. During periods of stable grid operation, the AC port can be plugged into a standard residential wall outlet to charge the battery, acting as a backup power source. In addition, AC Cube modules can easily be connected in parallel on the AC bridge due to the current-source nature of the converter, allowing for a scalable modular microgrid installation. While not shown in Fig. 2.2, an additional battery port on the DC bridge can be added to utilize a large, low-cost battery in addition to the power-dense lithium battery integrated into the AC Cube module.

2.2.2 Modular Electric Vehicle Powertrains

With electric vehicles estimated to represent 30% of new passenger vehicle sales by 2030 [29], and given that EV manufacturers are pushing system voltages from 400 VDC to 800 VDC to further increase power density and reduce vehicle charging times [30, 31], there exists a growing concern about the risk of high-voltage DC shock to passengers, first-responders, and maintenance workers following EV accidents [32]. While the touch-safety of low-voltage motor drives is well understood, scaling low-voltage motor drives to the current EV power levels of 100-200 kW has challenged existing technology. Recently, Continental introduced a 48 VDC, 30 kW hybrid powertrain which requires 625 A of battery current at full power, increasing the complexity of the power distribution system as well as the power converter [11].

The Synchronous RB Switch enables another low-voltage S4T variant that directly and efficiently converts 48 VDC to three-phase 480 VAC to drive an EV traction motor. Additionally, the ease of parallelization on the 480 VAC bridge lends itself to a modular, low-voltage powertrain architecture, where the highest voltage present in the vehicle when parked or at rest is 48 VDC. This low-voltage S4T variant is referred to as the AC Cube

modular drive unit, and is pictured in Fig. 2.3. With module power ratings of 3 kW continuous and 6 kW peak, and with module energy storage ratings of 3 kWh, 33 modules could be connected in parallel to meet the performance and range requirements of most planned EVs today. In addition, with three additional bridge legs on the AC bridge, the topology enables a multi-distribution capable vehicle fast charging port, allowing charging from flexible available AC or DC sources, while maintaining compatibility with current DC fast charging stations and isolating the traction battery from the grid and third party converters and interfaces. The additional weight and volume of the high-frequency transformer is traded off with the fact that the single-stage S4T replaces a DC/DC converter, inverter with low-pass and EMI filters, an on-board charger, and a universal fast charger. In addition, the design flexibility of the battery pack is increased, and the utilization of a mixed chemistry battery pack, consisting of modules with energy dense batteries for extended range and modules with power dense batteries for peak power, enables system-level performance and range optimization.

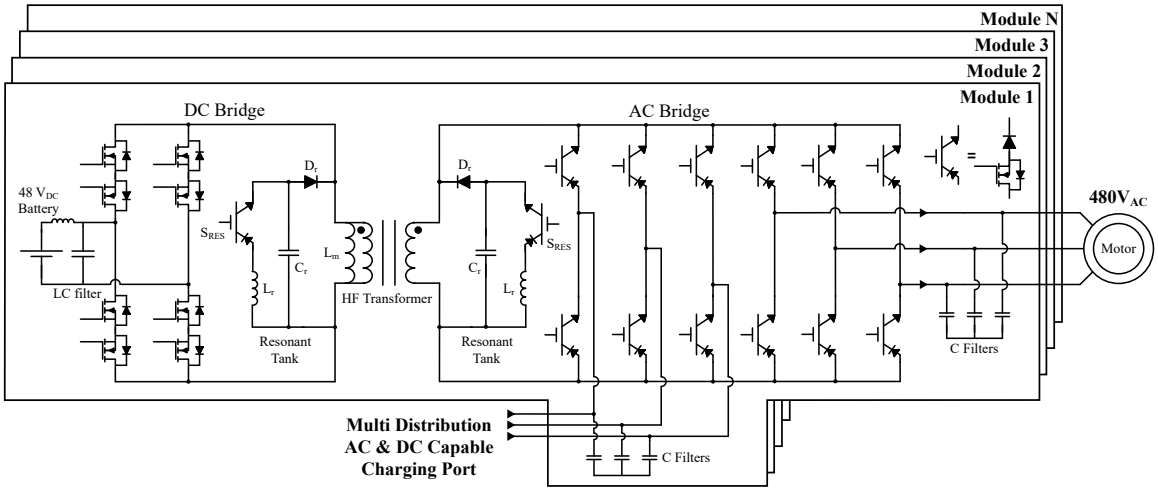


Figure 2.3: Modular, low-voltage EV powertrain built around a low-voltage S4T building block that converts power from a 48 VDC battery to produce a three-phase 480 VAC output used to drive an EV traction motor. Three additional bridge legs on the 480 VAC bridge enable compatibility with single-phase AC, three-phase AC, and DC vehicle fast charging technologies.

2.3 Principle of Operation of the Low-Voltage S4T

The operating principles of the low-voltage S4T follow the initial derivation presented in [16, 17], and are briefly summarized here. On a switching cycle basis, the transformer magnetizing inductance is used as an energy storage element to transfer power between the AC and DC bridges with isolation. Thus, the bridge sourcing energy charges the magnetizing inductance for a portion of the cycle by applying a series of positive voltages called active vectors across the transformer. The bridge sinking energy to the load subsequently discharges the magnetizing inductance via the application of active vectors with negative voltage across the transformer. To maintain a constant switching frequency, the rest of the cycle is padded with a freewheeling state where both transformer windings are shorted by turning a full leg per bridge on. The operating principle of the S4T, specifically applied to the 48 VDC to 480 VAC conversion in the AC Cube modular drive unit, is depicted in Fig. 2.4 where the magnetizing current is charged by the application of the battery voltage, V_{Bat}, and is discharged using two negative active vectors, V_{AC1} and V_{AC2}, corresponding to two motor phase-to-phase voltages.

The soft-switching operation of the converter is enabled by the two resonant tanks connected across the transformer windings as shown in Figs. 2.2 and 2.3. By appropriately sorting the active vectors so that the voltage levels applied to the transformer decrease continuously throughout the cycle, it is possible to leverage the discharge of the resonant capacitors by the magnetizing current during the transition period between the active vectors to achieve ZVS operation. At the end of the cycle, the resonant switches S_{RES} are gated on to initiate a resonance between the resonant capacitor C_r and resonant inductor L_r and flip the capacitor voltage so that a new switching cycle can begin. This process is explained in detail in [16, 17], and all switching states are shown in Fig. 2.5.

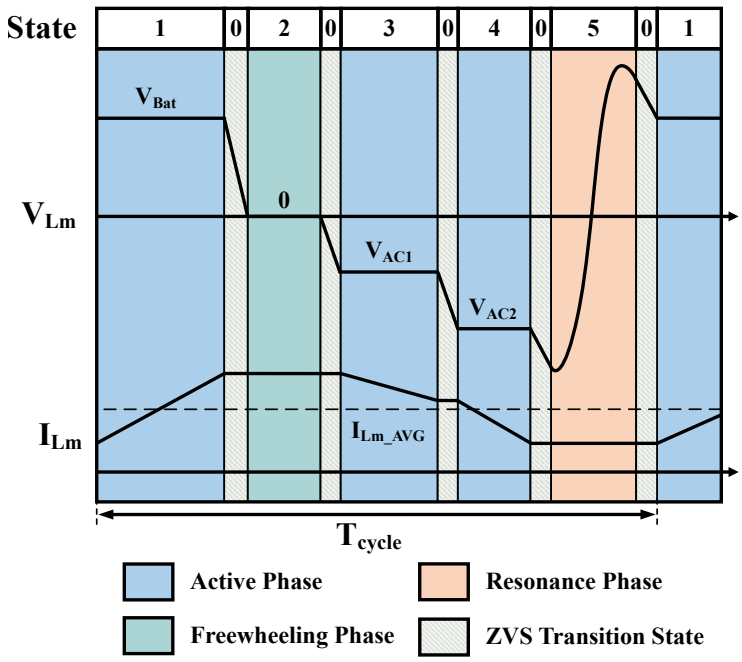


Figure 2.4: Operating principle of the AC Cube modular drive unit showing the voltage across and the current through the magnetizing inductance, L_m.

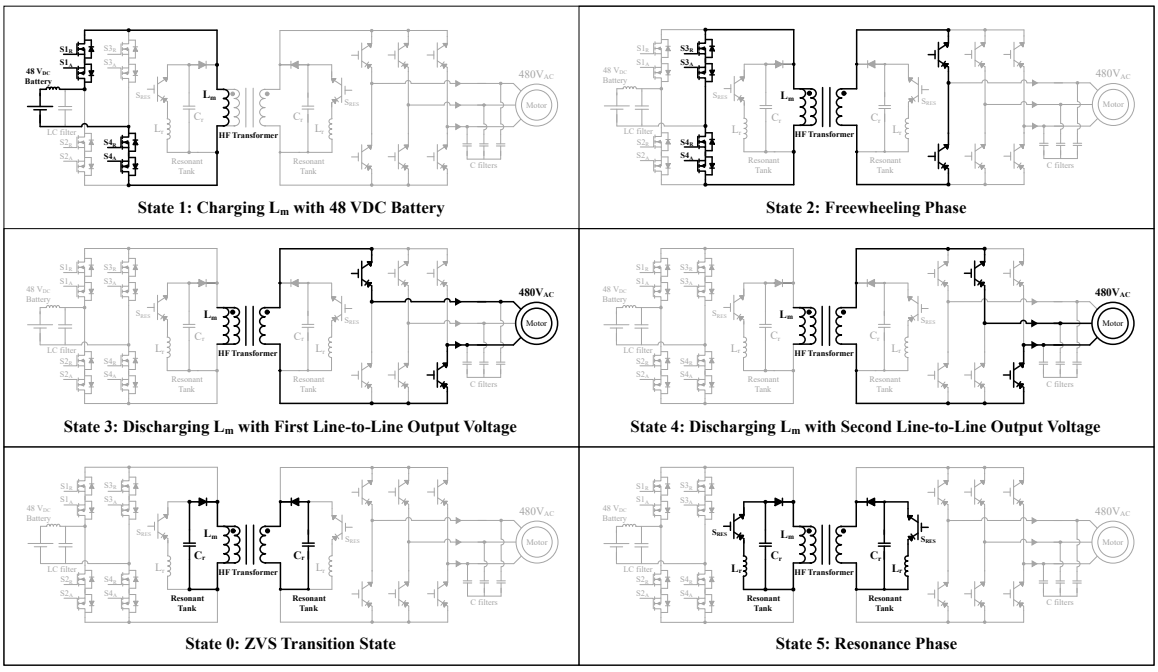


Figure 2.5: Switching states of the AC Cube modular drive unit, pictured without the multi-distribution fast charging port for simplicity. The switching states correspond to those labeled in Fig. 2.4. States 1, 3, and 4 are the active vectors in which power transfer occurs.

2.4 Competing Approaches to Improve Efficiency in Low-Voltage Current-Source Converters

Due to their improved performance and robustness, novel gallium-nitride (GaN) and silicon-carbide (SiC) power device structures present new opportunities to enable high-efficiency low-voltage current-source converters to address the aforementioned needs for highly efficient low-voltage interfaces. Several device structures have been proposed to realize 3-quadrant reverse blocking switches and 4-quadrant fully bidirectional (BD) switches. Key examples are monolithic bidirectional GaN switches based on high-electron-mobility transistors (HEMTs) [24, 25] and bidirectional SiC structures based on MOSFETs with integrated junction barrier Schottky (JBS) diodes [26], both of which boast lower conduction losses than their discrete-device-based counterparts.

While GaN and SiC RB and BD structures do offer strong promise in reducing conduction losses in low-voltage current-source converters and simplifying semiconductor packaging, significant converter-level tradeoffs must still be managed. For instance, the difficulty in the control of a 4-quadrant switch in conventional current-source topologies, particularly during the switching transitions, was detailed in [33]. Using a systematic approach, the author showed that a safe commutation between any two switch positions was only possible through a complex gating scheme requiring constant knowledge of both the switched current direction and the blocked voltage polarity. In addition, due to the relatively high reverse conduction voltage drops of SiC and GaN structures as compared to Si devices, the required commutation dead-times lead to lossy third-quadrant conduction, diminishing the advantage of reduced forward conduction loss [34]. Furthermore, the faster switching dynamics of wide bandgap structures as compared to Si devices increase the sensitivity to shoot-through, requiring precise and coordinated control of device gates and dedicated high-speed protection circuits, increasing control cost and complexity.

In [27, 28], a dual-MOSFET RB switch based on discrete SiC MOSFETs was pro-

posed to reduce conduction losses in a standard three-phase current-source inverter. While conduction loss reduction was achieved, the topology mandates another multi-step gating sequence during the switching transitions in which body diode conduction is required. This leads to lower conduction loss reduction and importantly, does not eliminate reverse recovery losses and associated voltage stresses, especially when standard Si devices are used.

Lastly, the practical performance metrics of available SiC and GaN devices for low-voltage current-source converter applications are lower than those of Si MOSFETs with appropriate voltage ratings. With respect to SiC MOSFETs and SiC Schottky diodes, the lowest available voltage class is 650 V, and while SiC devices have faster switching dynamics and lower on-resistances than Si counterparts of the same voltage rating, lower voltage class Si MOSFETs offer significantly lower on-resistances than 650 V Si MOSFETs. As an example, the Wolfspeed C3M0015065K 650 V SiC MOSFET features an $R_{DS(ON)}$ of 15 mΩ (Wolfspeed's lowest on-resistance discrete SiC MOSFET), while the Infineon IAUT300N10S5N015 100 V Si MOSFET features an $R_{DS(ON)}$ of 1.3 mΩ, that too, at a fraction of the cost. While SiC MOSFETs can be connected in parallel to reduce the effective on-resistance, a further cost penalty must be paid. On the other hand, GaN HEMTs are offered in lower voltage classes, but their usefulness in soft-switching low-voltage current-source converters, whose losses are dominated by conduction losses, is less than that of Si MOSFETs. For example the lowest on-resistance GaN HEMT from Efficient Power Conversion (EPC) in the 100 V category is the EPC2022, which has an $R_{DS(ON)}$ of 3.2 mΩ, more than double of that of the mentioned Si MOSFET. Indeed, GaN HEMTs also present a cost premium over Si MOSFETs of the same voltage class.

CHAPTER 3
DEVICE-LEVEL VALIDATION OF THE SYNCHRONOUS REVERSE BLOCKING SWITCH

3.1 Introduction

Specifically adapted for use in the S4T and its variants, the Synchronous Reverse Blocking Switch leverages the unique switching environment of the topology to enable utilization of dual-active-switch structures to significantly reduce conduction losses while minimizing or eliminating reverse recovery losses. The approach relies on simple control principles implemented at the gate driver level, enabling single-gate-signal control of the structure, and reducing the control complexity to the requirements of a standard RB switch with a series diode. This is in stark contrast to the devices and methods presented in Section 2.4 that require separate and tightly coordinated drivers for both switches in a dual-active-switch structure, and do not eliminate reverse recovery. In addition, the Synchronous RB Switch enables these benefits in all device technologies, from low-cost, legacy silicon devices to the newest wide bandgap switches.

3.2 Principle of Operation of the Synchronous Reverse Blocking Switch

The principle of operation of the Synchronous Reverse Blocking Switch is detailed by analyzing the operation of a high-current 48 VDC S4T bridge, depicted in Fig. 3.1, which allows for the application of all S4T switching states, while abstracting the high-voltage S4T bridge to focus the analysis on the gating and dynamics of the dual-MOSFET structure. In the 48 VDC bridge, the current in the inductor L_m, I_{Lm}, is regulated on a switching cycle basis through the application of positive active vectors (shown as State 1 in Fig. 3.1) to charge the inductor current, and the application of negative active vectors (State

3) to discharge the inductor current. A freewheeling state (State 2) is added to maintain a constant switching frequency. By applying the active vectors in order of descending voltage, the resonant capacitor, C_r, can be discharged by I_{Lm} during the transition periods between the active vectors, enabling ZVS operation (State 0). At the end of the cycle, the resonant switch S_{RES} is gated on to initiate a resonance between C_r and the resonant inductor, L_r, flipping the capacitor voltage to begin the next switching cycle (State 4).

As seen in Fig. 3.1, for any Synchronous RB Switch, the S_R MOSFET blocks a positive voltage (the body diode is reverse-biased) for the portion of the switching cycle before the switch position is activated, and does not block a voltage (the body diode is forward-biased) for the rest of the switching cycle until the resonance phase. This is true for any switch position in the bridge under all normal operating conditions of the S4T due to the modulation scheme used to enable the soft-switching feature of the topology [16, 17].

During the ZVS transition preceding the turn-on of a switch position (State 0), the voltage across S_R of the corresponding Synchronous RB Switch decreases with a controlled dv/dt until it reaches zero and the body diode of S_R starts conducting, signaling the end of the transition and the beginning of the conduction phase of the active vector. At this point, switch S_A of the Synchronous RB Switch must be turned on, and switch S_R can be safely gated on to shift from body diode conduction to MOSFET channel conduction and to reduce the conduction voltage drop. This is achieved by synchronizing the gate turn-on signal of switch S_A with the turn-on signal generated by the controller for the switch position, and by delaying the gate turn-on signal of switch S_R by a fixed delay t_{dON} with respect to the controller signal, as shown in Fig. 3.1.

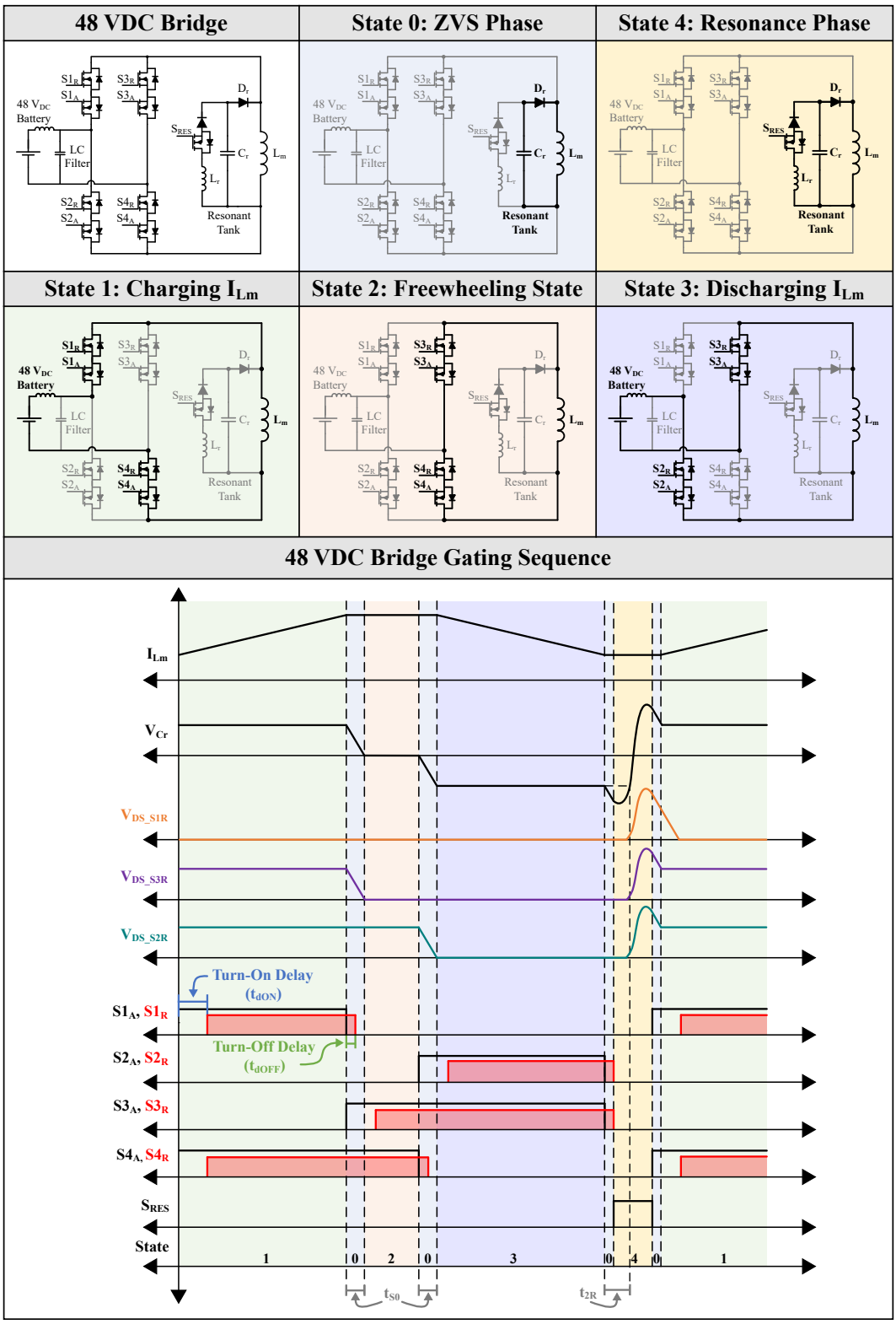


Figure 3.1: Switching states, converter waveforms, and gating signals for one switching cycle of the 48 VDC S4T bridge, showing circulation of a regulated current through L_m. For each Synchronous Reverse Blocking Switch, gating signals for the rectifier switches (S_R) are given in red and those for the active switches (S_A) are given in black.

From the above analysis, to ensure a proper ZVS turn-on of the switch position, the turn-on delay t_{dON} must be such that:

$$t_{dON} > t_{S0} \tag{3.1}$$

with t_{S0} being the duration of the ZVS transition to the active vector (State 0). To maximize the conduction loss reduction of the structure, t_{dON} should be minimized, which is possible because the duration of State 0, t_{S0}, is typically $< 1\%$ of the active state duration. In the case where condition (3.1) is not met ($t_{dON} \leq t_{S0}$), the ZVS transition to the active vector will be aborted and a hard-switching transition event will occur. This does not result in a catastrophic failure mode or possible shoot-through condition, making the above gating scheme robust and simple to implement in terms of possible delay slack.

At the end of the active state, signaled by the controller, switch S_A of the corresponding Synchronous RB Switch must be gated off to trigger the ZVS transition to the next active state. Thus, the gate turn-off of S_A is synchronized with the turn-off signal generated by the controller for the switch position. During the ZVS transition that follows, the voltage across switch S_A increases with a controlled dv/dt until it reaches the input voltage, 48 VDC in this case. Simultaneously, the voltage across switch S_R remains at zero during the transition, and until the resonance phase, as explained above. This enables a unique mechanism for preventing reverse recovery of the body diode of switch S_R. By delaying the turn-off gate signal of S_R with respect to the controller turn-off signal by a fixed delay, t_{dOFF}, it is possible to ensure that the body diode of the S_R MOSFET only conducts for the few initial instants at the active switch turn on, and does not conduct again when the active switch S_A is turned off to break the current. This in turn ensures that the reverse recovery of the body diode of S_R is minimized, if not eliminated, when the switch starts blocking a voltage again during the resonance phase. The maximum applicable t_{dOFF} is determined by the minimum time-to-resonance, t_{2R}, defined as the time between the turn-off of the last

active state and the point at which the resonant capacitor voltage, V_{Cr}, equals the voltage of the last active vector (while still in the resonance phase), as shown in Fig. 3.1. Thus, t_{dOFF} must be such that:

$$t_{dOFF} < t_{2R} \tag{3.2}$$

Extensive device characterization has been conducted to determine the minimum t_{dOFF} required to effectively minimize reverse recovery in standard Si MOSFETs. This was found to be well below the upper limit set by condition (3.2) for the devices tested considering typical S4T resonant tank dynamics and design tradeoffs [35].

The proposed method of gating the Synchronous RB Switch utilizes the resonant capacitor in the S4T topology to provide a path for the inductor current during state transitions, allowing the outgoing S_R MOSFET channel to remain gated on during the transition and eliminating conduction and reverse recovery of the S_R MOSFET body diode. If this technique were to be used in standard current-source inverters, hazardous short-circuit conditions would arise, making the performance gains of the Synchronous RB Switch unique to the S4T and its variants.

The S4T topology is intrinsically immune to shoot-through conditions when using the conventional 3-quadrant RB switch presented in [16, 17]. However, the Synchronous RB Switch is capable of 4-quadrant operation and introduces a risk for shoot-through conditions, under abnormal converter operation, where the sources or loads could produce a short circuit through two Synchronous RB Switches in the same switching cell. To eliminate these potential shoot-through conditions, a simple fault protection logic can be implemented at the gate driver level to block the 4th quadrant operation of the switch structure.

3.3 Experimental Apparatus

Device-level experimental validation of the Synchronous RB Switch was conducted to demonstrate the feasibility of the proposed dual-active-switch gating technique, particularly in terms of timing requirements to achieve the desired reverse recovery mitigation while meeting conditions (3.1) and (3.2). The test apparatus, shown in Fig. 3.2(a), consisted of a full-bridge square wave generator, the device under test (DUT), and an isolated gate driver. Since only the rectifier switch, S_R, of any Synchronous RB Switch undergoes 3rd quadrant conduction and potential reverse recovery, the test apparatus was designed to apply onto the DUT the voltage profile faced by the S_R switch during S4T operation. An FPGA clocked at 50 MHz was used to control the gates of the full-bridge MOSFETs and the DUT. The measured quantities included DUT drain-source voltage, V_{DS}, DUT gate-source voltage, V_{GS}, DUT source-drain current, I_{SD}, and full-bridge output voltage, V_{Square}. I_{SD} was measured using a CWT Ultra-mini 30 MHz Rogowski coil, and voltage measurements were conducted using 120 MHz Teledyne HVD3106 isolated probes. Table 3.1 lists the set of MOSFET and diodes tested.

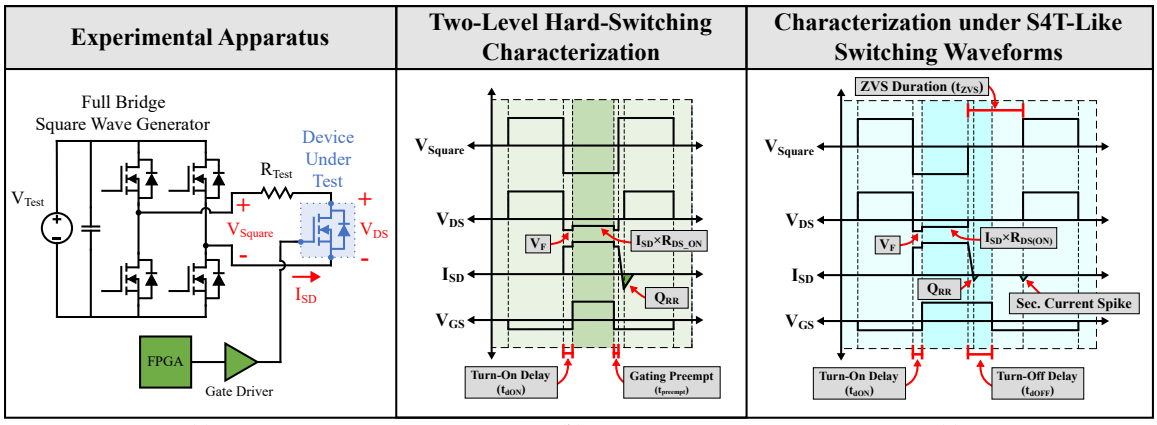


Figure 3.2: (a) Rectifier switch S_R reverse recovery study experimental apparatus, consisting of a full-bridge, an isolated gate driver circuit, and the device under test. (b) Hard-switching characterization of the S_R MOSFET with active gating, leading to MOSFET channel conduction. (c) Characterization of the S_R MOSFET under S4T-like switching waveforms. Note that the gate signal can remain asserted into the zero-voltage segment duration, t_{ZVS}, with a gate turn-off delay of t_{dOFF}.

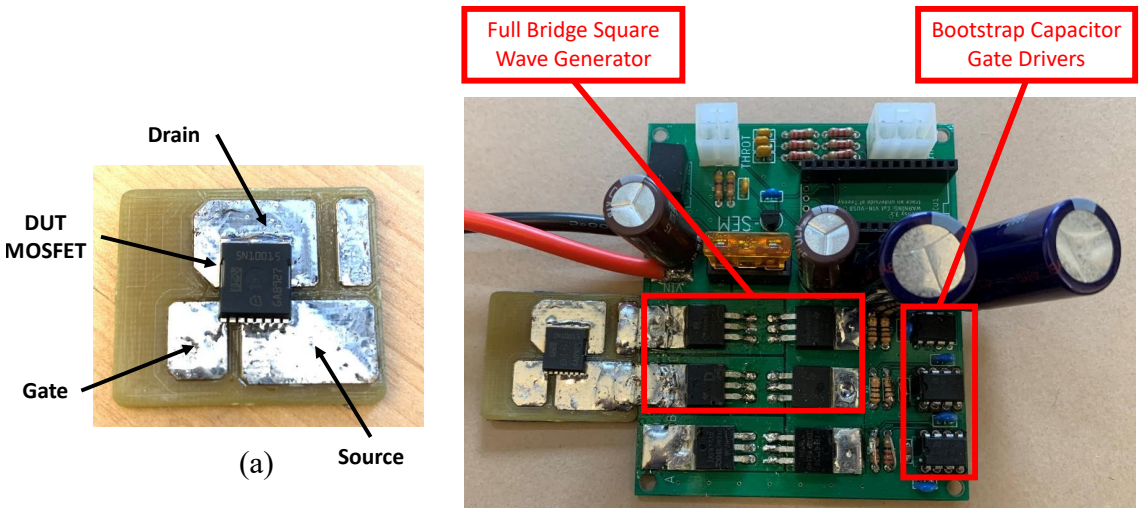


Figure 3.3: Picture of the S_R reverse recovery study experimental apparatus, showing (a) the DUT mounting board, and (b) the full-bridge based on the EasyController2 [36]. An additional picture of the experimental setup is given in Appendix A.

Table 3.1: List of Si MOSFETs and Si PN-Junction Fast-Recovery Diodes Characterized in the S_R Reverse Recovery Experiment

MOSFET Name	**Breakdown Voltage (V)**	**Current Rating (A)**	**$R_{DS(ON)}$ @ 25 C (mΩ)**
IAUT300N10S5N015	100	300	1.3
FCH023N65S3	650	75	23
Diode Name	**Breakdown Voltage (V)**	**Current Rating (A)**	**V_F @ I_{F_Rated}, 25 C (V)**
VS-EPU6006-N3	600	60	1.2
APT75DQ120BG	1200	75	2.8

3.4 Two-Level Hard-Switching Characterization

To establish a baseline reverse recovery level, the devices considered were first tested under a standard two-level hard-switching configuration, similar to the conditions the rectifier switch would face in a standard current-source inverter. The hard-switching characterization of the rectifier switch follows the gating sequence depicted in Fig. 3.2(b), and an example trial is given in Fig. 3.4. In the hard-switching characterization trials, the full-bridge was configured to output a square wave, V_{Square}, with a voltage magnitude below the DUT breakdown voltage and a period of 6 μs at 50% duty cycle. When V_{Square} switched

from positive to negative, the body diode of the DUT became forward-biased, resulting in the buildup of device source-drain current. After a turn on delay of t_{dON}, the MOSFET channel was gated, as shown in the green trace in Fig. 3.4, forcing the current to commutate to the MOSFET channel. The gate was held high until a period $t_{preempt}$ before the reversal of polarity of V_{Square}.

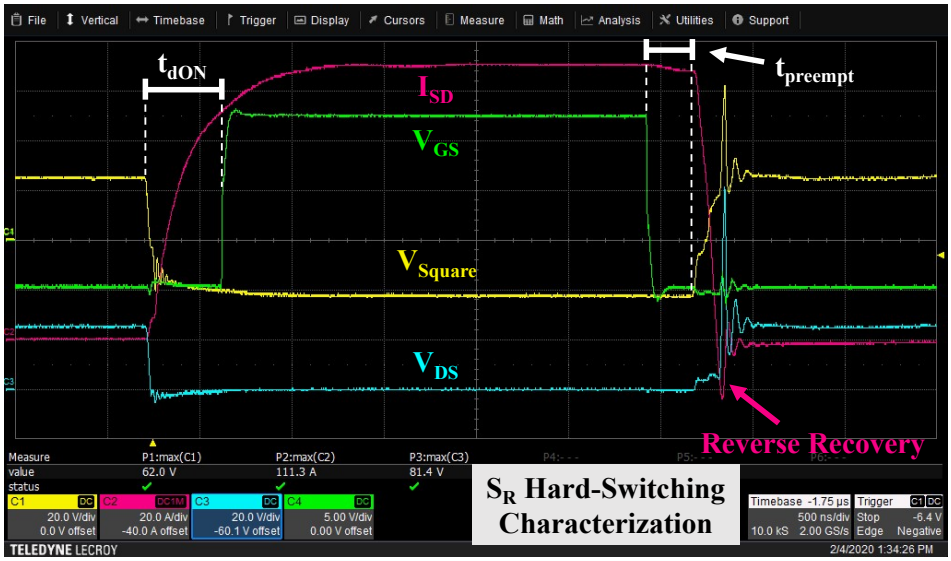


Figure 3.4: Hard-switching reverse recovery trial of rectifier switch, S_R using the 100 V, 1.3 mΩ MOSFET. The square wave voltage magnitude was 25 V, the peak device source-drain current was 111.3 A, and the gating preempt, $t_{preempt}$, was -200 ns.

Three switching performance criteria were quantified as functions of the gating preempt, $t_{preempt}$, including peak reverse recovery current, I_{RR_Peak}, total charge, Q_{Total}, and turn-off energy, E_{OFF}. Fig. 3.5 shows the results of the hard-switching S_R characterization using the 100 V, 1.3 mΩ MOSFET from Table 3.1 at varying V_{Square} and I_{SD}. While all switching performance metrics improved as $t_{preempt}$ increased from -300 ns to 0 ns, gating preempts greater than 0 ns caused shoot-through conditions of the full-bridge in the hard-switching case, as expected. This is shown in Fig. 3.5 by the sudden increase of the measured I_{RR_Peak} corresponding to a 4th quadrant conduction of a reverse polarity current through the RB switch position during shoot-through. It should be noted that E_{OFF} and Q_{Total} were not computed for the experimental conditions producing shoot-through, as they

would not have had any physical meaning.

These results corroborate previous study results demonstrating a reduction in I_{RR_Peak} and Q_{RR} with reduced dead times in synchronous rectifier configurations [23], and importantly, demonstrate the critical difficulty of optimizing commutation dead-times across wide operating ranges in standard hard-switching current-source converters. While conservative gating preempts do not maximize MOSFET channel conduction, narrowly optimized gating preempts (minimized $t_{preempt}$) may present shoot-through hazards at other operating points, especially with variable and unknown propagation delays in the control chain.

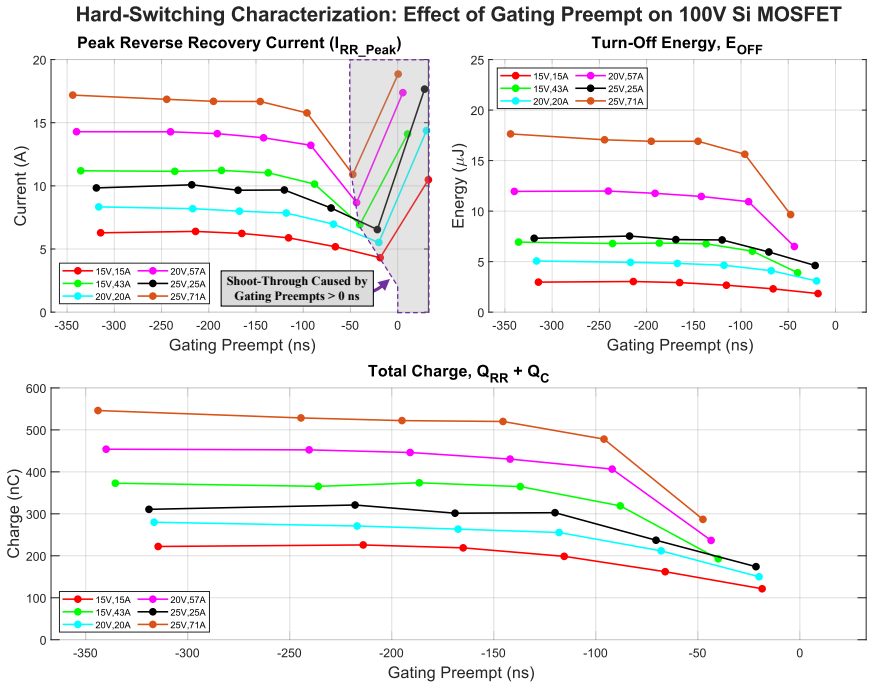


Figure 3.5: Hard-switching S_R characterization using the 100 V, 1.3 mΩ MOSFET, showing switching performance metrics improving as gating preempts near 0 ns. I_{RR_Peak} increases after 0 ns, representing a shoot-through condition.

3.5 Characterization under S4T-Like Switching Waveforms

3.5.1 100 V Si MOSFET (Infineon IAUT300N10S5N015)

The rectifier switch of the Synchronous RB Switch was then tested under conditions representative of the switching environment of the S4T. The same three switching performance criteria were quantified. However, the full-bridge output voltage V_{Square} was modified to include a zero-voltage segment, as shown in Fig. 3.2. The positive and negative V_{Square} segment durations were 2 μs each, and the zero-voltage segment duration, t_{ZVS}, was varied between 0 and 1 μs. As opposed to the standard hard-switching case, V_{GS} can be safely held high into the zero-voltage segment with a varying gate turn-off delay, t_{dOFF}, which is bounded by t_{ZVS} (after which a shoot-through would occur similar to the hard-switching case). A positive turn-off delay corresponds to the condition in which the MOSFET channel, and not the body diode, carries the full I_{SD} as the current is interrupted.

An example experimental trial of the 100 V, 1.3 mΩ MOSFET under S4T-like switching waveforms is shown in Fig. 3.6, where t_{ZVS} was 550 ns and t_{dOFF} was 350 ns. Additional experimental trials for this device are given in Fig. B.1 of Appendix B. The gate turn-on delay, t_{dON}, was fixed at a typical S4T ZVS transition time of 300 ns to closely match the turn-on of the rectifier switch. As observed in Fig. 3.6, the voltage applied to the DUT emulates the drain-source voltage of the S_R switch during S4T operation, as previously presented in Fig. 3.1. The DUT blocks a positive voltage (+50 V segment of V_{Square}) before it is activated (-50 V segment of V_{Square}) and does not block a voltage for the remainder of the switching cycle (0 V segment of V_{Square}). When the square wave reached -50 V, a source-drain current of 94.7 A was developed in the DUT. When the square wave voltage increased to 0 V, a minimal reverse recovery induced current spike was observed. When the square wave voltage increased further to +50 V, a secondary current spike was observed, as noted in Fig. 3.6. The nature of this secondary current spike was investigated by integrating the spike charge at varying blocked voltages and conducted currents as shown in Fig. 3.7.

The charge of the secondary current spike was a weak function of conducted current but a strong function of blocked voltage, evidencing the hypothesis that the secondary current spike was capacitive in nature and was caused by the charging of the MOSFET output source capacitance, C_{OSS}.

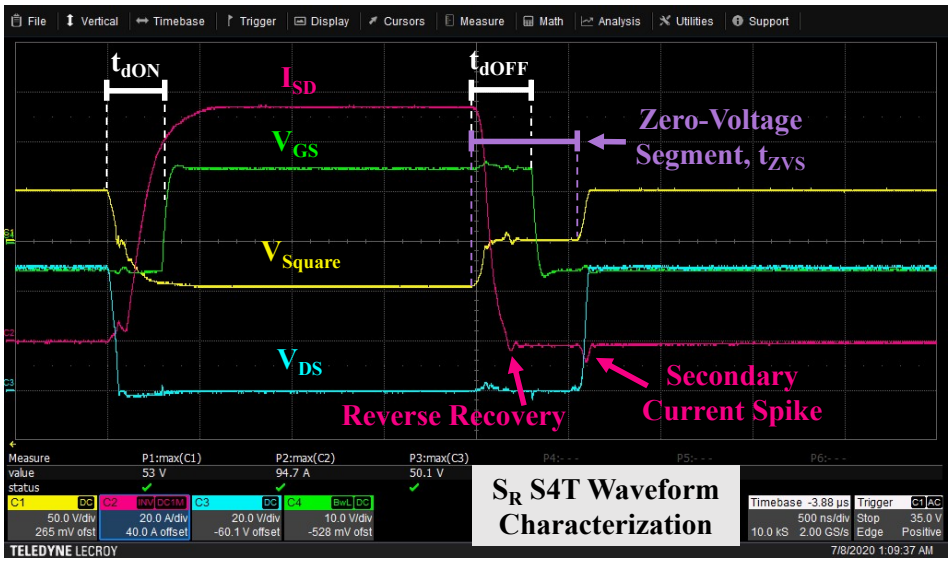


Figure 3.6: S4T-like switching waveform characterization of S_R using the 100 V, 1.3 mΩ MOSFET. The square wave voltage magnitude was 50 V, the peak device source-drain current was 94.7 A, the zero-voltage segment duration, t_{ZVS}, was 550 ns, and the gate turn-off delay, t_{dOFF}, was 350 ns.

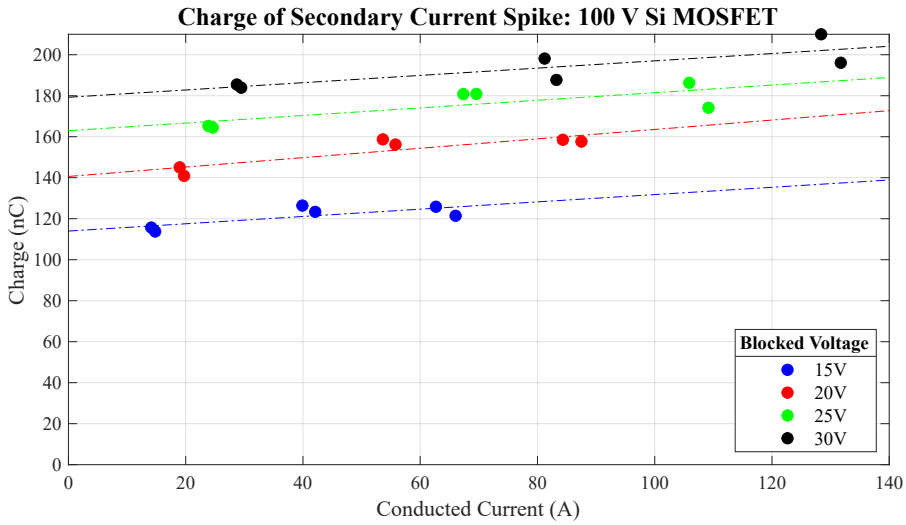


Figure 3.7: Integrated charge under the secondary current spike from S_R characterization trials under S4T-like switching waveforms for the 100 V, 1.3 mΩ MOSFET. Secondary spike charge is a weak function of current, but a strong function of voltage.

Figs. 3.8 and 3.9 present the results of the S4T-like switching waveform characterization of the 100 V, 1.3 mΩ MOSFET as functions of zero-voltage segment duration, t_{ZVS}, and gate turn-off delay, t_{dOFF}, respectively. As shown in Fig. 3.8, a t_{ZVS} of roughly 200 ns is sufficient to reduce all three switching performance criteria to their baseline levels, regardless of t_{dOFF}. Specifically, as reverse recovery charge is eliminated, total charge extracted at turn-off is reduced by 42.8%, reaching the baseline set by the device C_{OSS}. Similarly, the peak reverse recovery current and turn-off energy were reduced to 33.0% of the maximum values recorded under two-level hard-switching characterization (t_{ZVS} = 0 ns). From Fig. 3.9, it is apparent that gate turn-off delay does have a large influence in reducing device stresses with t_{ZVS} below 200 ns, which agrees with the hard-switching characterization results from the previous section. Importantly, a small t_{dOFF} delay, around 100 ns for this device, together with a t_{ZVS} of around 100 ns yields the same reduction in switching metrics as a t_{ZVS} of 200 ns alone with no turn-off delay. This seems to indicate that the turn-off delay helps achieve the same reverse recovery reduction at smaller zero-voltage segment durations.

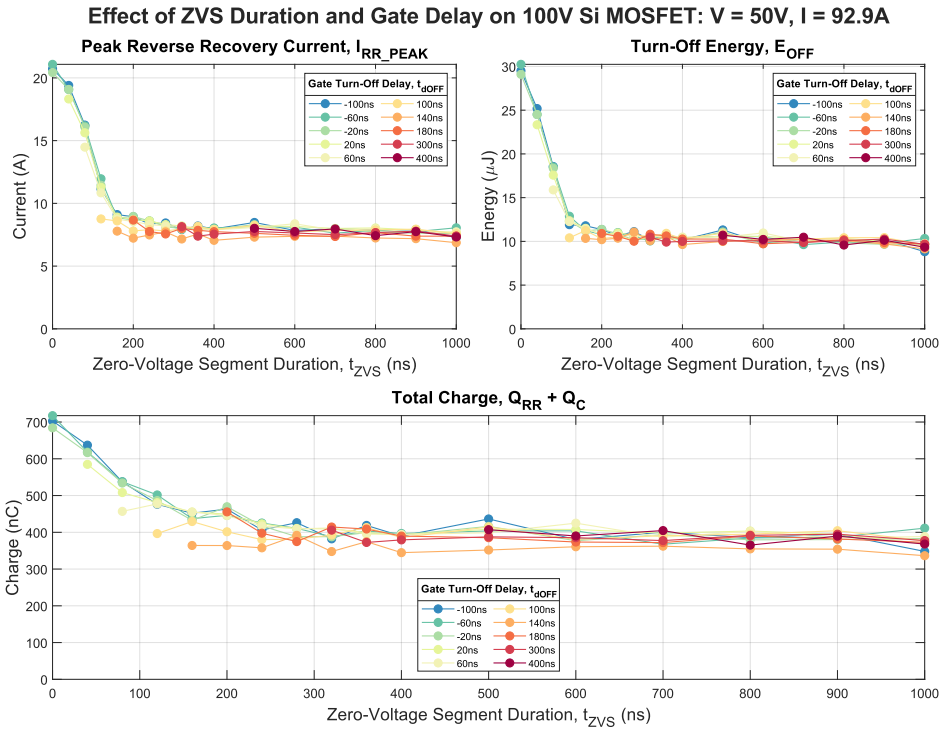


Figure 3.8: S4T-like switching waveform characterization of S_R using the 100 V, 1.3 mΩ Si MOSFET (IAUT300N10S5N015). The x-axis represents zero-voltage segment duration, and the plots are parameterized by gate turn-off delay.

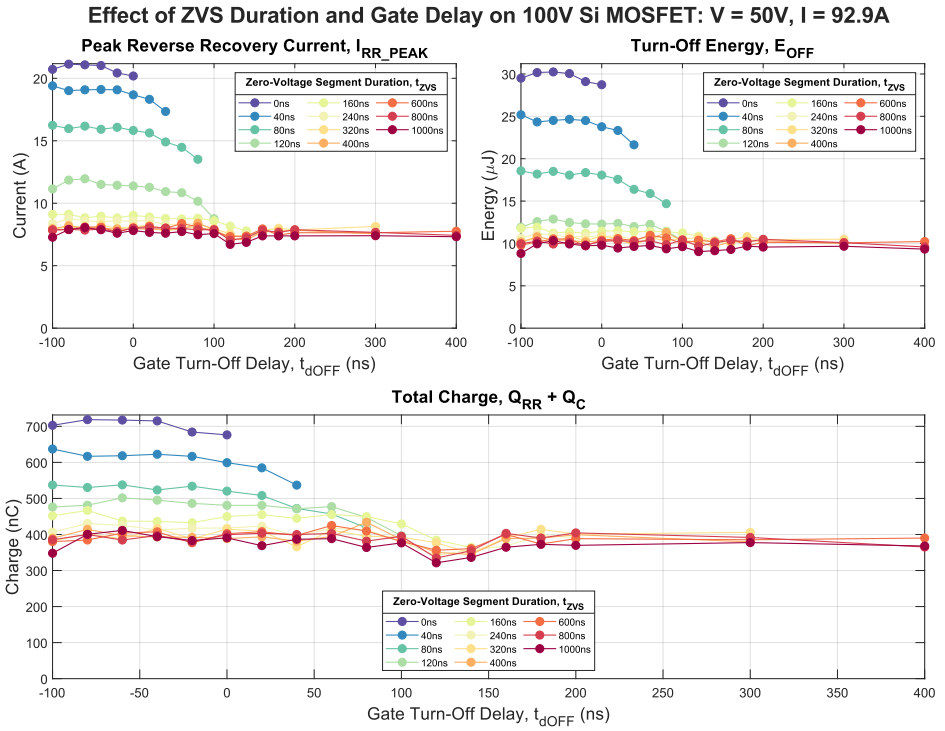


Figure 3.9: S4T-like switching waveform characterization of S_R using the 100 V, 1.3 mΩ Si MOSFET (IAUT300N10S5N015). The x-axis represents gate turn-off delay, and the plots are parameterized by zero-voltage segment duration.

3.5.2 650 V Si MOSFET (ON Semiconductor FCH023N65S3)

The 650 V, 23 mΩ Si MOSFET was then characterized to investigate if the reverse recovery mitigation technique scaled to higher voltage devices. For conciseness, experimental trials for this device are given in Fig. B.2 of Appendix B. The results of the rectifier switch characterization experiments of the 650 V MOSFET under S4T-like switching waveforms are given in Fig. 3.10 and 3.11. These results elucidate the relative magnitudes of the effects of gate turn-off delay and zero-voltage segment duration. As observed in Fig. 3.10, a zero-voltage segment duration of 1 μs alone is not able to reduce reverse recovery current and charge to their baseline values. Instead, a gate turn-off delay of slightly more than 120 ns can minimize all switching performance metrics, for t_{ZVS} as low as 200ns. The charge at turn-off was thus reduced by 68.8%, while the reverse recovery current and turn-off energy were reduced by more than 35.0% in this device. Put together, these results suggest that the effect of gate turn-off delay, which ensures the absence of minority carriers in the PN-junction of the body diode at turn off, is stronger than the effect of the zero-voltage segment duration, which likely relies on recombination to mitigate reverse recovery. This trend seems to be stronger as the voltage rating of the device increases. It should be noted that the 650 V MOSFET features a significantly larger C_{OSS}, especially at low-voltage, causing a larger level of minimum total charge (capacitive charge) than the 100 V MOSFET.

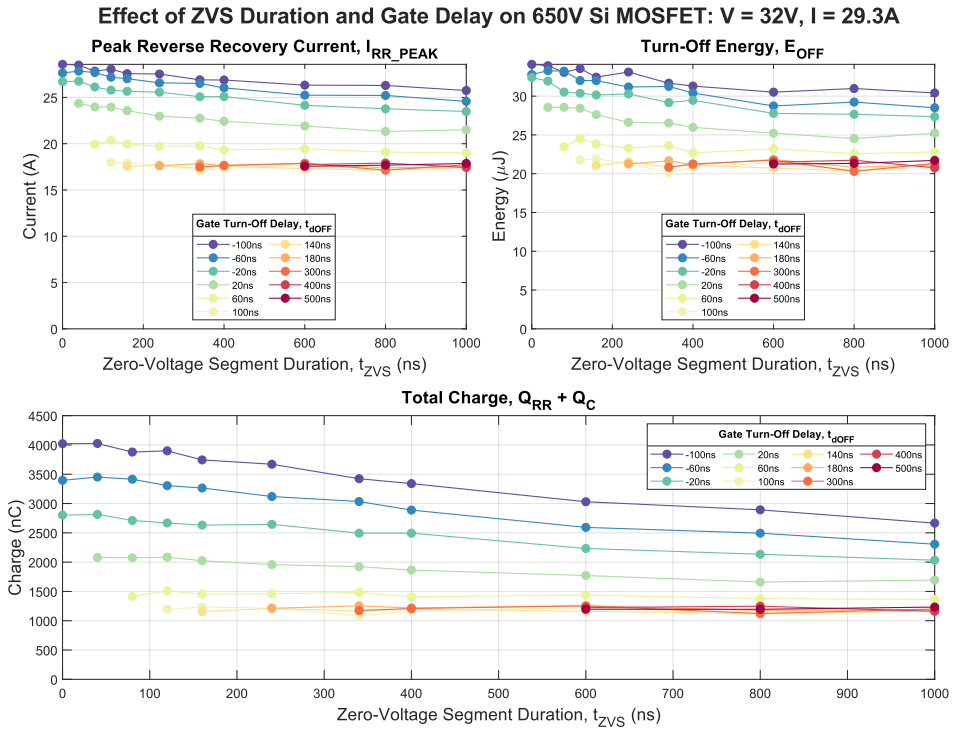


Figure 3.10: S4T-like switching waveform characterization of S_R using the 650 V, 23 mΩ Si MOSFET (FCH023N65S3). The x-axis represents zero-voltage segment duration, and the plots are parameterized by gate turn-off delay.

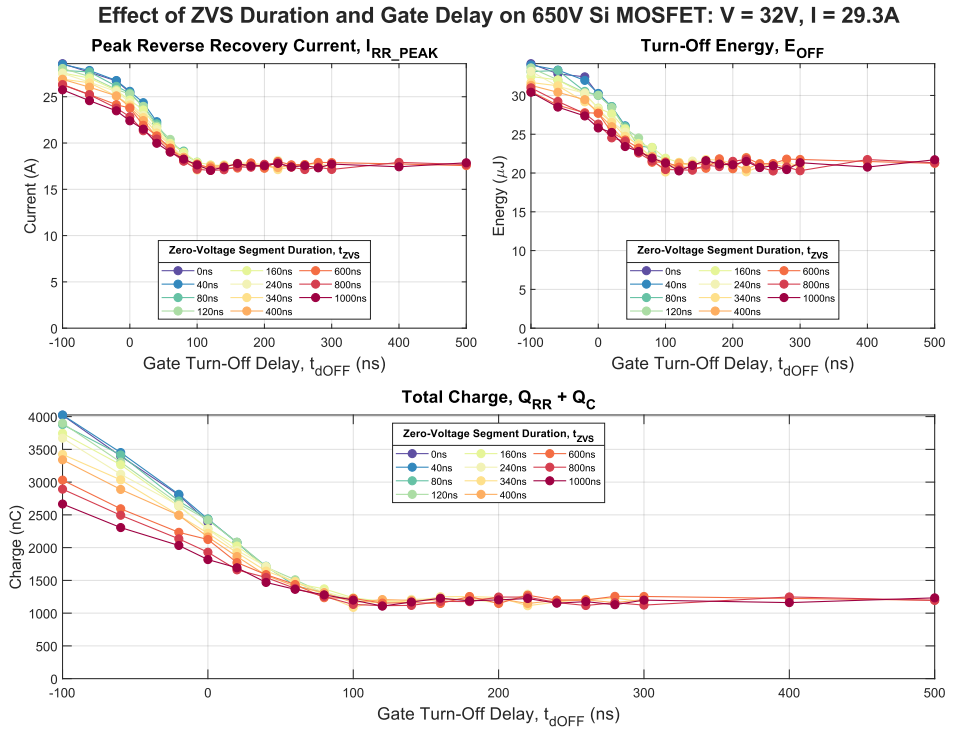
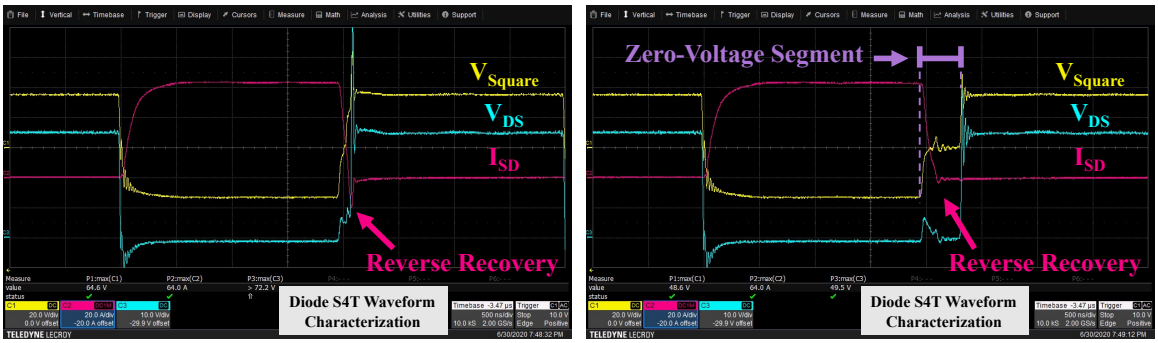


Figure 3.11: S4T-like switching waveform characterization of S_R using the 650 V, 23 mΩ Si MOSFET (FCH023N65S3). The x-axis represents gate turn-off delay, and the plots are parameterized by zero-voltage segment duration.

3.6 Mitigation of Reverse Recovery of Silicon PN Junction Diodes under S4T-Like Switching Waveforms

The hypothesis that a zero-voltage segment can mitigate reverse recovery in Si fast-recovery PN-junction diodes was tested on the diodes listed in Table 3.1. The zero-voltage segment duration was varied between 0 and 1 μs as in the S4T-like switching waveform characterization experiments, but no active gating was possible given that the DUTs were diodes. The same three switching performance criteria were quantified. Without the influence of active gating, the results of the diode characterization trials can help compare different diodes based on the speed of their recombination dynamics.

Two experimental trials of the 600 V, 60 A Si fast-recovery diode (VS-EPU6006-N3) are given in Fig. 3.12. The full results from the characterization of both the 600 V and 1200 V diodes are presented in Fig. 3.13, with the key takeaway being that a zero voltage segment duration of roughly 250 ns was sufficient to minimize all switching performance metrics to their baseline values. Additionally, due to the relatively small device capacitance as compared to the previously tested MOSFETs, a secondary current spike was not observed at the end of the zero-voltage segment. These results evidence the opportunity to use fast-recovery Si diodes to replace the SiC Schottky series diodes of conventional RB structures in cost-critical S4T applications.



(a) (b)

Figure 3.12: S4T-like switching waveform characterization of the 600 V, 60 A Si fast-recovery diode (VS-EPU6006-N3). The switching waveforms emulate the switching conditions of the series SiC Schottky diode in conventional RB switch structures. The square wave voltage magnitude was 35 V, the peak device current was 64.0 A. The zero-voltage segment duration, t_{ZVS}, was 0 ns in (a) and 500 ns in (b).

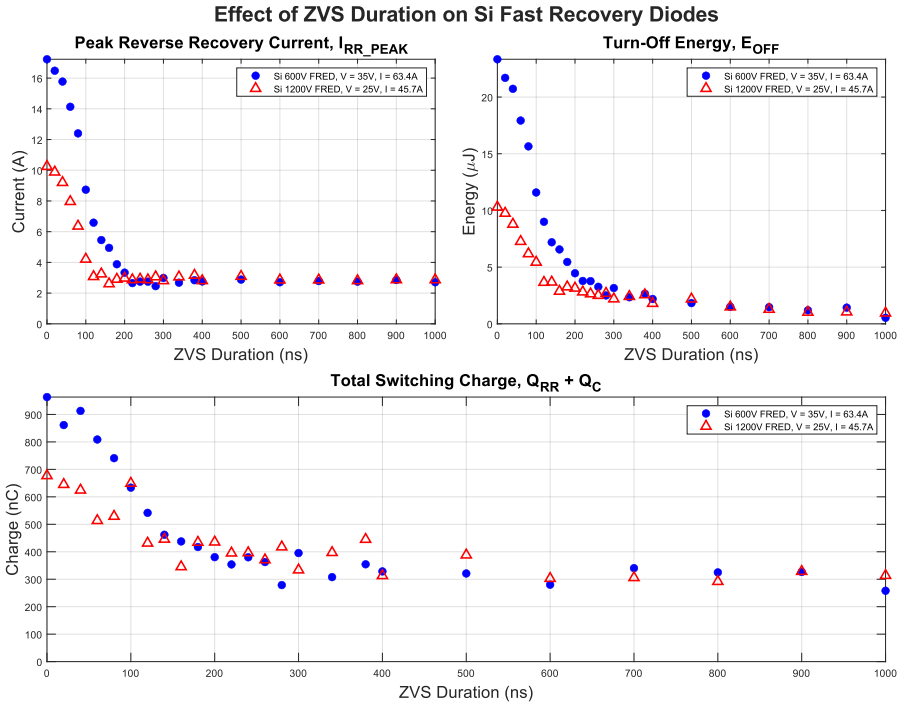


Figure 3.13: S4T-like switching waveform reverse recovery study of the 600 V, 60 A (VS-EPU6006-N3) and 1200 V, 75 A (APT75DQ120BG) Si PN-junction fast-recovery diodes showing switching performance metrics as a function of zero-voltage segment duration.

3.7 Conclusion

The experimental results presented in this chapter evidence the alignment between the gate control timing requirements of the Synchronous Reverse Blocking Switch and the inherent dynamics and operating principles of the S4T. Specifically, during S4T operation, the smallest t_{ZVS} throughout the switching cycle is the time-to-resonance t_{2R}, and is well above 500 ns in typical resonant tank designs [35]. Thus, for the MOSFETs tested, the reverse recovery phenomenon of the anti-parallel body diodes can be effectively mitigated with t_{ZVS} as low as 200 ns and t_{dOFF} slightly above 120 ns. This is well aligned with condition (3.2) from Section 3.2 (requiring that the turn-off delay be less than the time-to-resonance) and validates the applicability of the proposed Synchronous RB Switch gate control and reverse recovery mitigation methods to the S4T topology. In addition, since a t_{ZVS} of 200 ns alone mitigated reverse recovery in the 100 V, 1.3 mΩ MOSFET, this device is a particularly good candidate for a robust, low-cost, and module-integrated Synchronous RB Switch with a passive delay generation circuit. This device has been used to build a 48 VDC S4T bridge based on Synchronous RB Switches as detailed in the following chapter.

CHAPTER 4
DESIGN AND PERFORMANCE ANALYSIS OF A LOW-VOLTAGE, HIGH-CURRENT S4T BRIDGE

4.1 Introduction & Hardware Design

Following the verification of the fundamental principles of the Synchronous Reverse Blocking Switch at the device-level, system-level experiments were conducted to measure the impact on converter operation and conduction loss. The 48 VDC S4T bridge, analyzed in Chapter 2, was built around Synchronous RB Switches composed of the previously tested 100 V, 1.3 mΩ MOSFETs. The component specifications of the 48 VDC bridge are given in Table 4.1, the circuit schematic and built PCB are shown in Fig. 4.1, and the experimental apparatus is shown in Fig. 4.2. The design documents of the 48 VDC bridge are given in Appendix C, and the design documents of the isolated, +15 V / -5 V dual-MOSFET RB switch gate drivers are given in Appendix D. With this gate driver design, t_{dON} and t_{dOFF} were programmed into the upstream FPGA controller, allowing for testing of multiple gate delay options. An updated gate driver with a simplified control interface and integrated rectifier switch delay generation was also designed and is presented in Section 4.4. Appendix F presents an additional image of the experimental apparatus, showing the custom FPGA/DSP-based controller used to control the DC bridge.

Conduction loss through the DC bridge was measured at voltages from 10 V to 50 V and currents up to 30 A. Power was circulated through the bridge by applying the S4T switching states described in Fig. 3.1 of Chapter 3, and total power loss was measured as the input power from the DC power supply. In addition, each power loss component of DC bridge operation was calculated analytically, including losses due to dual-MOSFET RB switch conduction, the main inductor L_m (DC, AC, and core loss), the resonant inductor

L_r (DC and AC loss), auxiliary resonant switch conduction, and PCB trace resistance. The measured loss from the DC supply was used to validate the analytical loss calculations.

Table 4.1: Component Specifications of the 48 VDC S4T Bridge

Power Semiconductors Devices	
Synchronous RB Switch Semiconductor Device	100 V, 1.3 mΩ Si MOSFET (IAUT300N10S5N015)
Resonant Switch Diode	650 V, 30 A SiC Schottky Diode (2 × FFSB3065B-F085)
Passive Power Components	
Resonant Inductor, L_r	160 nH Air Core Solenoid
Resonant Capacitor, C_r	544 nF Film Capacitor (8 × B32621A3683J000)
Main Inductor, L_m	72 µH Nanocrystalline Core Inductor

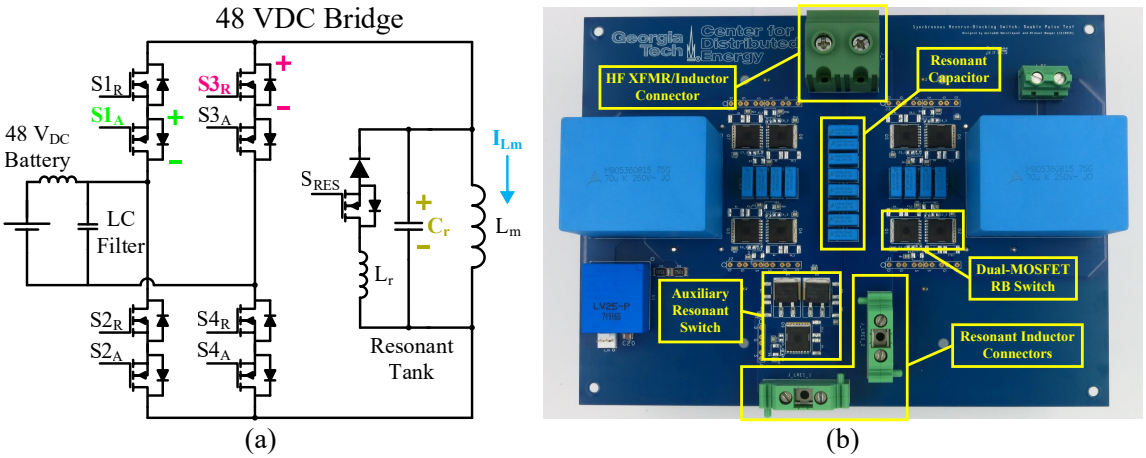


Figure 4.1: Schematic (a) and built PCB (b) of the high-current, 48 VDC S4T bridge circuit built around Synchronous RB Switches composed of two 100 V, 1.3 mΩ MOSFETs.

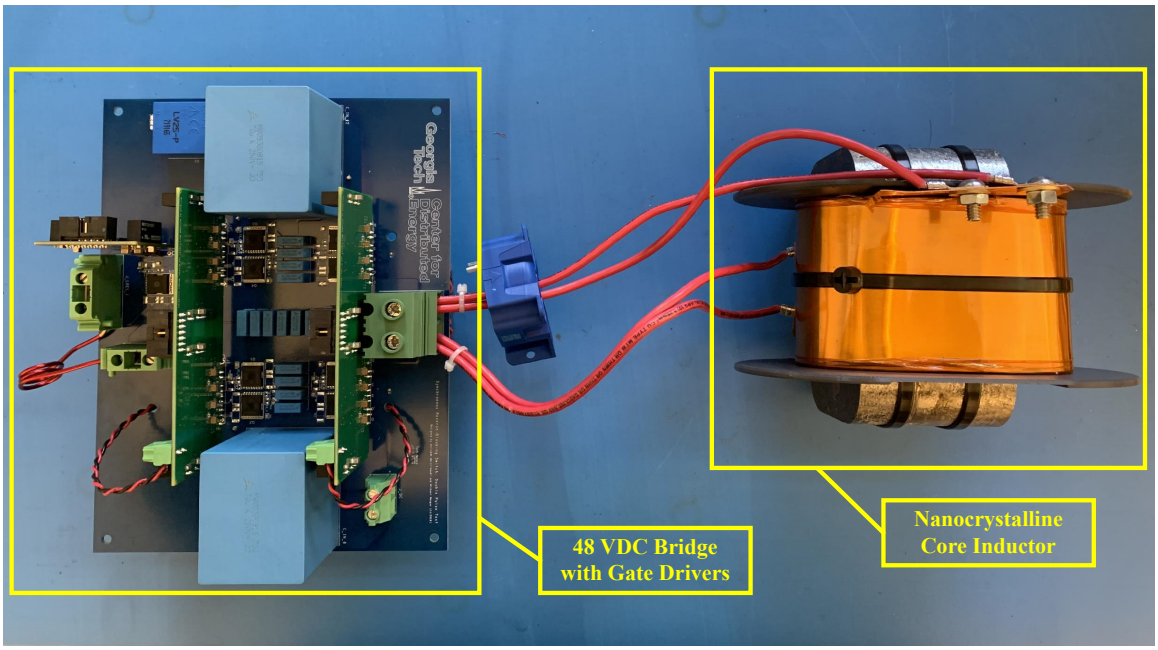


Figure 4.2: Experimental apparatus of the high-current 48 VDC S4T bridge showing the resonant inductor, gate drivers, and nanocrystalline core inductor. An extended picture of the experimental apparatus is given in Appendix F.

4.2 Experimental Validation

4.2.1 Results from Continuous Operation at 10 V, 10 A

The 48 VDC bridge was first tested using a DC input voltage of 10 V, and by circulating 10 A through L_m. Assuming that half of the switching period could be used to deliver power to the output bridge, this 10 V, 10 A operating point represented a 50 W power circulation level. An oscillogram of the 48 VDC bridge under continuous operation at the 50 W power circulation level is given in Fig. 4.3, and the measured electrical and thermal operating conditions are given in Table 4.2. Table 4.3 presents the itemized power loss components within the bridge, calculated using the operating conditions from Table 4.2. The last row of Table 4.3 shows a comparison between the measured loss and the sum of the calculated loss components.

Table 4.4 contains the results of a pair of tests at 10 V, 10 A. For the first test, switch S_R in each Synchronous Reverse Blocking Switch was not gated, leading to complete conduction through the devices' body diodes, and falling back to the conventional RB switch configuration traditionally used in the S4T. In the second test, the S_R switches were gated with a t_{dON} of 1.2 μs and a t_{dOFF} of 330 ns, leading to MOSFET channel conduction, and allowing for a direct evaluation of the impact of the novel Synchronous Reverse Blocking Switch in terms of conduction loss reduction. As shown in Table 4.4, total semiconductor conduction loss was decreased by more than an order magnitude, from 13.99 W to 0.47 W with the gating of the S_R switches. This represents a 29.8-fold reduction in semiconductor conduction loss, increasing the efficiency of power circulation through the DC bridge from 66.6% to 94.3% at the 10 V, 10 A operating point.

Figure 4.3: Experimental waveforms of the 48 VDC S4T bridge operating at 10 V, 10 A (50 W power circulation level). The rectifier switches were gated with appropriate t_{dON} and t_{dOFF}.

Table 4.2: Operating Conditions of the DC Bridge at the 10 V, 10 A (50 W Power Circulation) Operating Point

MOSFET Parameters			
$R_{DS\,(ON)}$ @ T_{op}	$V_{F\,Si\ BD}$ @ 29.75 A		$T_{op\ MOSFET}$
1.42 mΩ	0.80 V		30 °C
Main Inductor (L_m) Parameters			
$R_{Lm\ DC}$	$R_{Lm\ AC}$ @ 15kHz	$I_{Lm\ AVG}$	$I_{Lm\ RIPPLE\ \ RMS}$
2.20 mΩ	42.00 mΩ	9.55 A	0.97 A
Resonant Circuit Parameters			
$I_{Lr_{pk}}$	$V_{F_{SiC\ Schottky}}$ @ 47.55 A (Note: 2 diodes in parallel)	t_{RES}	$R_{Lr_{DC}}$
95.10 A	1.88 V	1.33 µs	0.98 mΩ
$I_{Lr_{RMS}}$	$R_{Lr_{AC}}$ @ 500 kHz	$T_{op\ DIODE}$	
9.48 A	8.82 mΩ	30 °C	
PCB Parameters			
R_{TRACE}		$T_{op\ PCB}$	
1.85 mΩ		30 °C	

Table 4.3: Comparison of the Calculated DC Bridge Loss Components to the Measured Loss at the 10 V, 10 A (50 W Power Circulation) Operating Point

	Loss Calculation Method	Loss	Component Total
$\mathbf{P_{MOSFET_{cond}}}$	$4 \times \left(I^2_{Lm\ AVG} \times R_{DS\,(ON)}\right)$	0.47 W	0.47 W
$\mathbf{P_{Lm_{DC}}}$	$\left(I^2_{Lm\ AVG} \times R_{Lm\ DC}\right)$	0.20 W	0.28 W
$\mathbf{P_{Lm_{AC}}}$	$\left(I^2_{Lm\ RIPPLE\ \ RMS} \times R_{Lm\ AC}\right)$	0.04 W	
$\mathbf{P_{Lm_{Core}}}$	$[8 \times (F_{sw})^{1.62} \times (\Delta B)^{1.98}] \times \text{Volume}_{core}$	0.04 W	
$\mathbf{P_{Lr_{DC}}}$	$\frac{t_{RES}}{T_{SW}}\left[\begin{matrix} I_{Lr_{pk}} \times V_{F_{SiC\ Schottky}} \\ + \\ I^2_{Lr_{pk}} \times R_{DS\,(ON)} \end{matrix}\right]$	1.54 W	2.04 W
$\mathbf{P_{Lr_{AC}}}$	$I^2_{Lr_{RMS}} \times R_{Lr_{AC}}$	0.50 W	
$\mathbf{P_{PCB\ TRACE}}$	$R_{TRACE} = \frac{\rho L}{TW}\left(1 + \alpha_{Cu}\left(T_{op} - 25°C\right)\right)$ $I^2_{Lm_{AVG}} \times R_{TRACE}$	0.15 W	0.15 W
Measured $\mathbf{P_{DC_{Supply}}}$	**2.70 W**	**Total Calculated**	**2.94 W**

Table 4.4: Efficiency of the DC bridge test circuit quantified in a pair of experiments at 10 V, 10 A (50 W power circulation level). In the first experiment, the rectifier switch of each Synchronous Reverse Blocking Switch was left un-gated (left, blue), and in the second experiment, the rectifier switches were gated with appropriate t_{dON} and t_{dOFF} (right, green), yielding a 29.8X reduction in semiconductor loss.

50 W Power Circulation $I_{Lm_{AVG}}$ = 9.55 A V_{DC} = 10 V	**S_R Body Diode Conduction Only (S_R Not Gated)**	**S_R MOSFET Channel Conduction (S_R Gated)**
Body Diode Conduction Loss	13.75 W	0
MOSFET Conduction Loss	0.24 W	0.47W
Inductor L_m Loss	0.28 W	
PCB Trace Loss	0.15 W	
Resonant Tank Loss	2.04 W	
Calculated Loss	16.46 W	2.94W
Measured Loss	16.00 W	2.70W
Efficiency	66.6 %	94.3%

4.2.2 Results from Continuous Operation at 50 V, 30 A

After the 10 V, 10 A experiment evidenced the efficacy of the Synchronous Reverse Blocking Switch in reducing conduction loss, the DC bridge test circuit was then characterized at 50 V, 30 A, corresponding to a power deliver level of 750 W in the S4T. The experimental waveforms are given in Fig. 4.4. The operating conditions are given in Table 4.5, and the itemized power loss components are given in Table 4.6. It is important to note that leaving the S_R switches ungated at the 50 V, 30 A operating point would have yielded a total semiconductor conduction power loss of 51.49 W, with 48.84 W of loss shared between two S_R switch body diodes per switching state.

To avoid thermal damage to the test apparatus, the Synchronous Reverse Blocking Switches were only tested with appropriate gating of the S_R switches at the 50V, 30A operating point, with t_{dON} and t_{dOFF} set to 1.45 μs and 330 ns, respectively. Even without this direct experimental comparison, however, the fact that the total loss measured from the DC source (16.94 W) was less than the theoretical semiconductor loss calculated for the case in which S_R switches are left ungated evidences the efficacy of the Synchronous Reverse Blocking Switch in significantly reducing conduction losses. At the 750 W power circulation level, gating the S_R switches resulted in a 9.7-fold reduction in semiconductor conduction loss, increasing the DC bridge efficiency from 91.7% to 97.8% as shown in Table 4.7. Lastly, given that the 5.29 W of semiconductor conduction loss occurs through 4 individual MOSFETs in any switching state, the results from the usage of the Synchronous RB Switch at the 50 V, 30 A operating point evidence the viability of a passively cooled design, allowing for tightly integrated and power dense low-voltage S4T bridges.

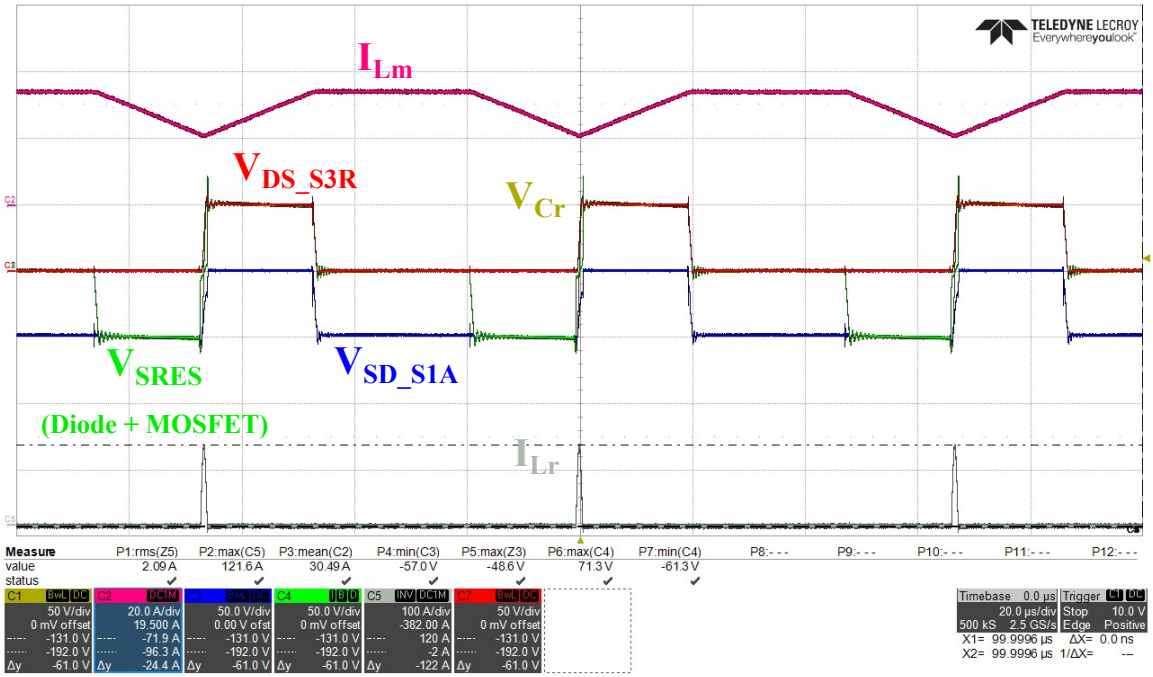


Figure 4.4: Experimental waveforms of the 48 VDC S4T bridge operating at 50 V, 30 A (750 W power circulation level). The rectifier switches were gated with appropriate t_{dON} and t_{dOFF}. The waveforms are void of reverse recovery induced device voltage stresses.

Table 4.5: Operating Conditions of the DC Bridge at the 50 V, 30 A (750 W Power Circulation) Operating Point

MOSFET Parameters			
$R_{DS\,(ON)}$ @ T_{op}		$T_{op\ MOSFET}$	
1.42 mΩ		50 °C	
Main Inductor (L_m) Parameters			
$R_{Lm\ DC}$	$R_{Lm\ AC}$ @ 15kHz	$I_{Lm\ AVG}$	$I_{Lm\ RIPPLE\ RMS}$
2.20 mΩ	42.00 mΩ	30.53 A	4.38 A
Resonant Circuit Parameters			
$I_{Lr_{pk}}$	$V_{F_{SiC\ Schottky}}$ @ 61.3 A (Note: 2 diodes in parallel)	t_{RES}	$R_{Lr_{DC}}$
122.60 A	2.13 V	1.20 µs	0.98 mΩ
$I_{Lr_{RMS}}$	$R_{Lr_{AC}}$ @ 500 kHz	$T_{op\ DIODE}$	
11.43 A	8.82 mΩ	70 °C	
PCB Parameters			
R_{TRACE}		$T_{op\ PCB}$	
1.91 mΩ		65 °C	

Table 4.6: Comparison of the Calculated DC Bridge Loss Components to the Measured Loss at the 50 V, 30 A (750 W Power Circulation) Operating Point

	Loss Calculation Method	Loss	Component Total
$P_{MOSFET_{cond}}$	$4 \times \left(I^2_{Lm\ AVG} \times R_{DS\,(ON)}\right)$	5.29 W	5.29 W
$P_{Lm_{DC}}$	$\left(I^2_{Lm\ AVG} \times R_{Lm\ DC}\right)$	2.05 W	3.60 W
$P_{Lm_{AC}}$	$\left(I^2_{Lm\ RIPPLE\ \ RMS} \times R_{Lm\ AC}\right)$	0.81 W	
$P_{Lm_{Core}}$	$[8 \times (F_{sw})^{1.62} \times (\Delta B)^{1.98}] \times Volume_{\,core}$	0.74 W	
$P_{Lr_{DC}}$	$\frac{t_{RES}}{T_{SW}}\left[\begin{matrix} I_{Lr_{pk}} \times V_{F_{SiC\ Schottky}} \\ + \\ I^2_{Lr_{pk}} \times R_{DS\,(ON)} \end{matrix}\right]$	5.06 W	6.21 W
$P_{Lr_{AC}}$	$I^2_{Lr_{RMS}} \times R_{Lr_{AC}}$	1.15 W	
$P_{PCB\ TRACE}$	$R_{TRACE} = \frac{\rho L}{TW}\left(1 + \alpha_{Cu}\left(T_{op} - 25°C\right)\right)$ $I^2_{Lm_{AVG}} \times R_{TRACE}$	1.78 W	1.78 W
Measured $P_{DC_{Supply}}$	**16.94 W**	**Total Calculated**	**16.88 W**

Table 4.7: Efficiency of the DC bridge test circuit at 50 V, 30 A (750 W power circulation level). Total semiconductor loss with the rectifier switches gated appropriately was calculated as 5.29 W, 9.7X lower than the loss calculated for the case in which the rectifier switches were left ungated (body diode conduction only).

750 W Power Circulation $I_{Lm_{AVG}}$ = 30.53 A V_{DC} = 50 V	**S_R Body Diode Conduction Only (S_R Not Gated)**	**S_R MOSFET Channel Conduction (S_R Gated)**
Body Diode Conduction Loss	48.84 W	0
MOSFET Conduction Loss	2.65 W	5.29 W
Inductor L_m Loss	3.60 W	
PCB Trace Loss	1.78 W	
Resonant Tank Loss	6.21 W	
Calculated Loss	63.07 W	16.88 W
Measured Loss		16.94 W
Efficiency	91.7 %	97.8 %

A zoomed view of one switching cycle observed experimentally is given in Fig. 4.5, showing that the drain-source voltage across switch $S3_R$, V_{DS_S3R}, matches the derivations from Fig. 3.1 in Chapter 3. As seen in both Fig. 4.4 and Fig. 4.5, the converter waveforms are void of reverse recovery related current spikes and resultant device voltage stresses, evidencing the ability of the Synchronous Reverse Blocking Switch to offer significant conduction loss reduction while maintaining benign reverse recovery behavior.

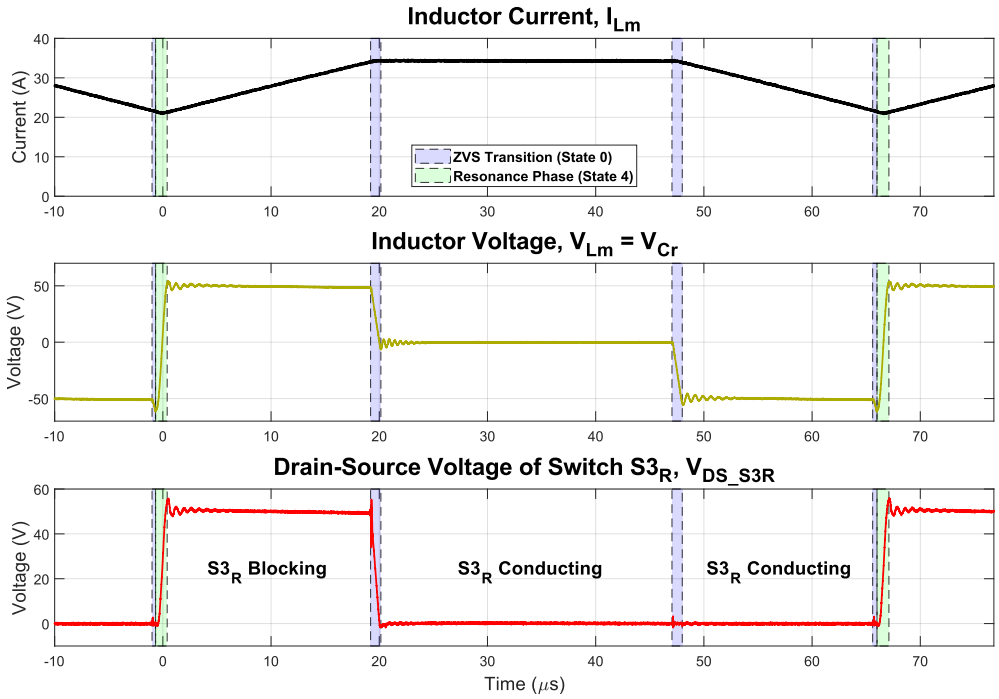


Figure 4.5: Zoomed experimental waveforms of the 48 VDC bridge operating at 50 V, 30 A (750 W power circulation level), confirming that the drain-source voltage of $S3_R$ matches the analysis from Chapter 3.

4.3 System-Level Impacts

4.3.1 1 kW, 48 VDC to 120 VAC AC Cube

The system-level impacts of the conduction loss reduction enabled by the Synchronous RB Switch in the S4T are considered by analyzing the AC Cube, previously presented in Fig. 2.2 in Chapter 2. Fig. 4.6 presents the impact of the Synchronous RB Switch on projected converter efficiency of the AC Cube. By replacing the conventional MOSFET and SiC Schottky RB structure with the Synchronous RB Switch on the 48 VDC bridge, converter efficiency is improved by 9.6% at full load. Additionally, by utilizing Synchronous RB Switches on both the 48 VDC and the 120 VAC bridges, a further 1.5% efficiency increase can be unlocked.

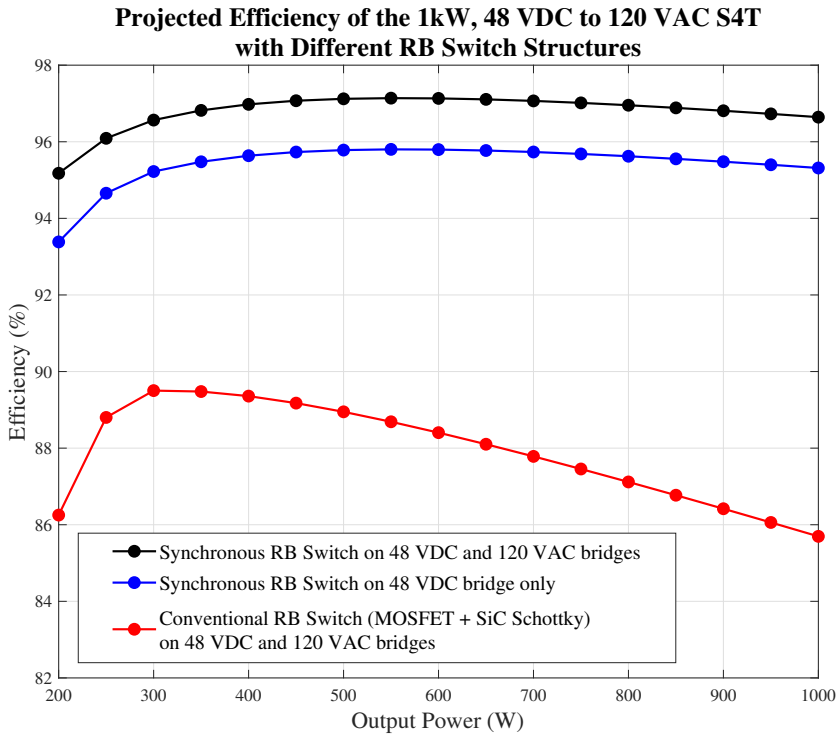


Figure 4.6: Projected efficiency of the 48 VDC to 120 VAC application of the S4T. The Synchronous RB Switch enables an 11.1% increase in efficiency at full load when compared to the case in which a conventional RB switch is used.

4.3.2 3 kW, 48 VDC to 480 VAC AC Cube Modular Drive Unit

The system-level impacts of the Synchronous RB Switch are also analyzed in the case of the AC Cube modular drive unit, previously presented in Fig. 2.3 in Chapter 2. To demonstrate the ability of the Synchronous RB Switch to enable high efficiency in the AC Cube modular drive unit, a 3 kW, 48 VDC to 480 VAC system has been modeled and simulated using the parameters given in Table 4.8. As seen in Fig. 4.7(a) below, the magnetizing current is controlled on a switching cycle basis and the switching dv/dt is under 500 V/μs at 3 kW and rated voltage stresses, demonstrating the soft-switching operation at full power and maximum voltage boost. As shown in Fig. 4.7(b), the magnetizing current, I_m, is regulated to the reference value of 140 ADC (referred to the 48 VDC bridge) throughout the simulation with a controlled soft-start (no inrush current), thus validating the controllability of the structure across the load and voltage boost range required. At the rated output power, the output waveforms have low harmonic content, with THD $< 4\%$ and $< 2.5\%$ for the voltages and currents, respectively. Similarly, the battery current THD is controlled under 7% at full power. Losses are low, with an estimated efficiency of 96.5% at rated power, increasing to 98.2% at partial load levels, as shown in the red curve of Fig. 4.7(c). This includes losses in the devices, transformer, and filters and compares with DC/DC converter and inverter losses in comparable high-voltage EV powertrains. Extension of the dual-MOSFET RB switch structure and the gating principles of the Synchronous RB Switch to 1200 V SiC MOSFETs for the 480 VAC bridge can enable further improvements in efficiency, as shown in the black curve of Fig. 4.7(c).

Table 4.8: Simulation Parameters of the 48 VDC to 480 VAC AC Cube Modular Drive Unit

f_{sw}	L_m	C_{in}	C_{out}	I_m (48 VDC Bridge / 480 VAC Bridge)	P_{rated}	Transformer Ratio	Rated Input Voltage	Rated Output Voltage	Rated Output Frequency
15 kHz	25 µH	140 µF	4.7 µF	140 A / 11.7 A	3 kW	1:12	48 VDC	480 V_{LL_RMS}	60 Hz

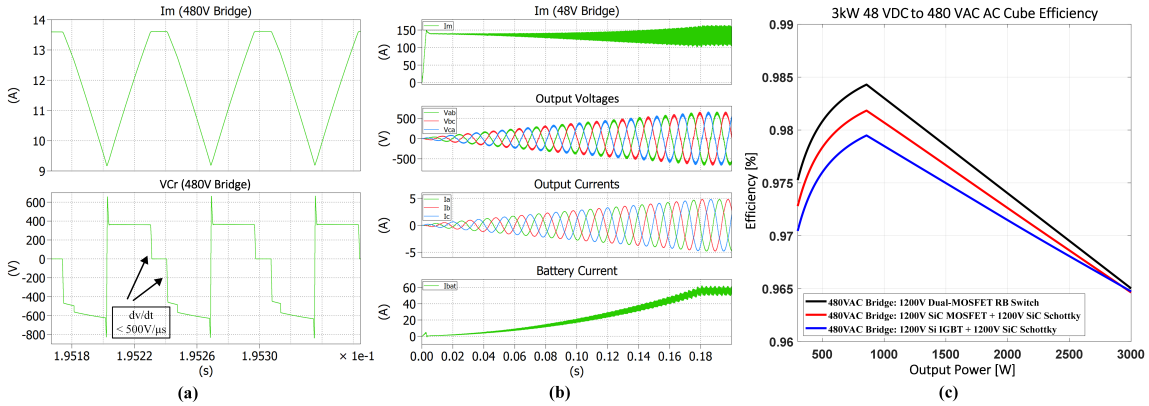


Figure 4.7: (a) Soft-switching waveforms of the AC Cube modular drive unit at 3 kW showing the magnetizing current, I_m, and resonant capacitor voltage, V_{Cr}, both referenced to the 480 VAC bridge. (b) 200 ms simulation of the AC Cube modular drive unit showing output waveforms, battery current, and magnetizing inductance current. (c) Efficiency over the converter operating range for different configurations of the reverse blocking switches used on the 480 VAC bridge.

4.4 Prototype of the Synchronous RB Switch Gate Driver with Integrated Delay Generation

The rectifier switch gate delay generation strategy of the Synchronous Reverse Blocking Switch, validated in the device-level experiments in Chapter 3 and in the system-level tests of this chapter, is simple enough to be implemented with a dedicated and cost-effective hardware solution. The delay generation mechanism is integrated into the gate driver controlling the dual-MOSFET RB structure to form the proposed Synchronous Reverse Blocking Switch as shown in Fig. 4.8(a). The implementation shown features an "Enable Signal" in addition to the single control signal generated by the controller. This allows for both normally on and normally off versions of the gate driver circuit, but may not be needed in all applications. As shown in Fig. 4.8(a), the single control signal is directly used to control switch S_A. A fixed delay generator is used to delay the control signal by t_{dON} and t_{dOFF}, at turn on and turn off, respectively. This delayed signal is then fed into an AND gate together with the fault protection signal and the result is used to drive switch S_R. The fault protection signal is generated within the fault detection block by sensing the voltage across switch S_R, V_{DS_SR}, as described in Chapter 3. A single, isolated power supply is used to control both

MOSFETs owing to the common source configuration. As previously mentioned, a further reduction in cost and an implementation compatible with standard power module packaging techniques can be achieved using a simplified, passive S_R delay generation circuit, as shown in Fig. 4.8(b), in this case without the V_{DS_SR} measurement circuitry.

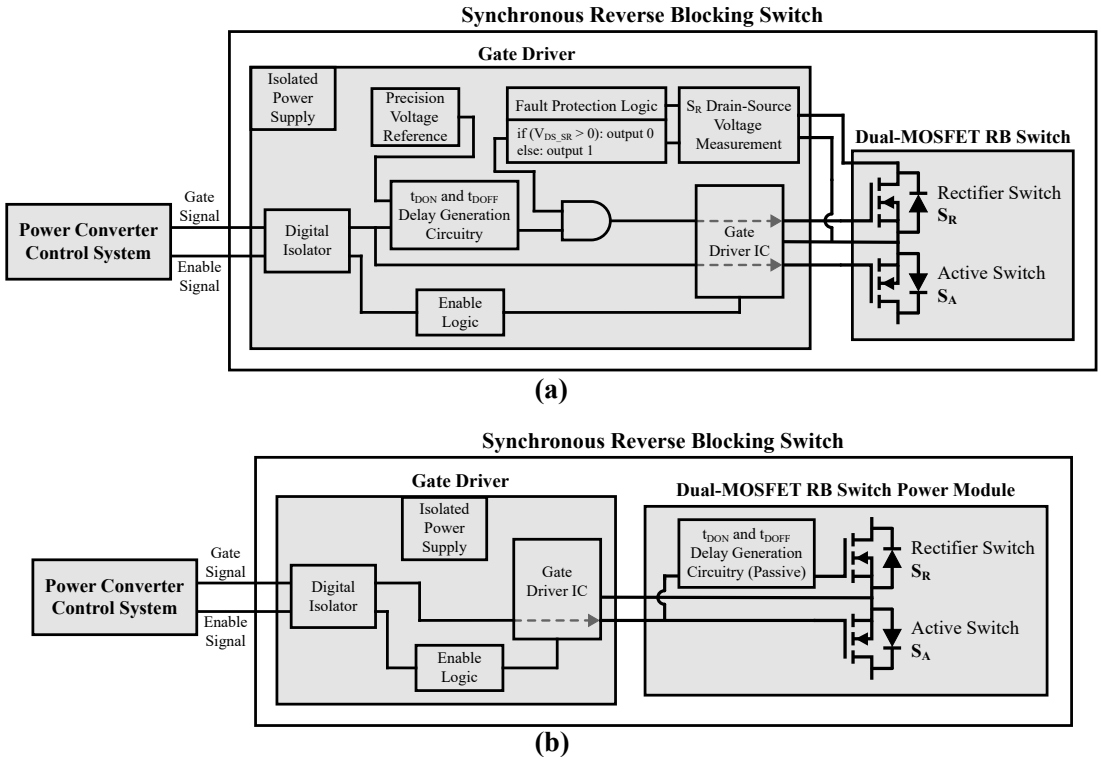


Figure 4.8: (a) Block diagram of the Synchronous RB Switch, showing the gate driver with integrated delay generation for the rectifier switch and fault protection through measurement of the rectifier switch drain-source voltage. (b) Low-cost, power module compatible implementation of the Synchronous RB Switch.

A prototype of the Synchronous RB Switch gate driver with integrated delay generation has been constructed, and the design documents are given in Appendix E. As the required turn-on delay t_{dON} is larger than the turn-off delay t_{dOFF}, one implementation is to use an RC circuit in combination with a comparator with hysteresis, as shown in Fig. 4.9. This method yields a compact and easily re-configurable delay circuit, while also presenting an extremely economical design. The analysis of the RC delay generation stage is given on the following page. Validation of converter operation using the Synchronous RB Switch gate driver with integrated delay generation is a significant direction for future work.

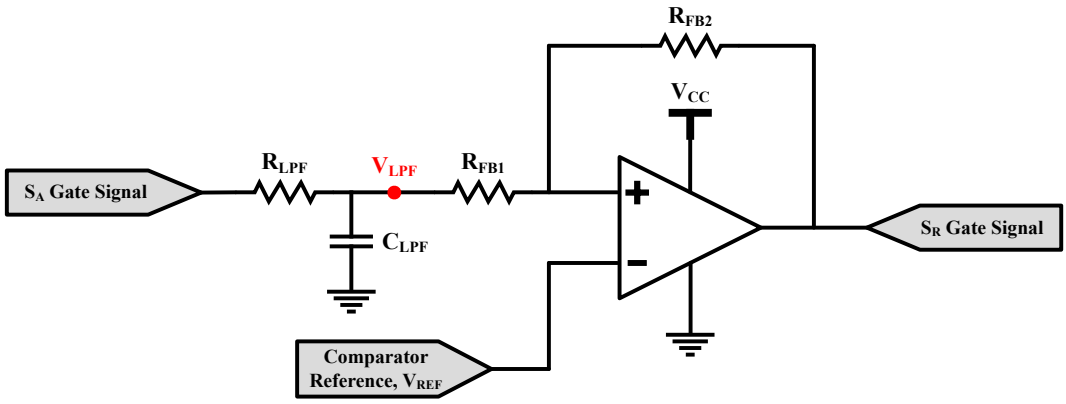


Figure 4.9: S_R gate delay generation method using an RC circuit and a comparator with hysteresis.

The gate delay timings, t_{dON} and t_{dOFF}, can be calculated using the formulas

$$V_{LPF}(t) = V_{CC} \times \left(1 - e^{\frac{-t}{R_{LPF}C_{LPF}}}\right) \tag{4.1}$$

$$V_{THRES_{HI}} = V_{REF} \times \left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}}\right) + V_{COMP_{offset}} \tag{4.2}$$

$$V_{THRES_{LO}} = V_{REF} \times \left(\frac{R_{FB1} + R_{FB2} - (R_{FB1} \times V_{CC})}{R_{FB2}}\right) + V_{COMP_{offset}} \tag{4.3}$$

$$t_{dON} = -R_{LPF}C_{LPF} \times \log\left(1 - \frac{V_{THRES_{HI}}}{V_{CC}}\right) + t_{COMP_{delay}} \tag{4.4}$$

$$t_{dOFF} = -R_{LPF}C_{LPF} \times \log\left(\frac{V_{THRES_{LO}}}{V_{LPF}(t_{duty})}\right) + t_{COMP_{delay}} \tag{4.5}$$

where

V_{LPF} is the voltage at the node following the RC delay circuit

V_{CC} is the comparator supply voltage

R_{LPF}, C_{LPF} are the RC delay resistor and capacitor

R_{FB1}, R_{FB2} are the comparator feedback resistors, as shown in Fig. 4.9

$V_{THRES_{HI}}$ is the upper level of the hysteresis band of the comparator

$V_{THRES_{LO}}$ is the lower level of the hysteresis band of the comparator

$t_{COMP_{delay}}$ is the propagation delay of the comparator

$V_{COMP_{offset}}$ is the comparator input offset voltage

t_{duty} is the duty time of the switch position, as determined by the system controller

4.5 Conclusion

The experimental results presented in this chapter demonstrate that the Synchronous RB Switch can unlock significant conduction loss reduction under true S4T operation while also mitigating the reverse recovery of the S_R body diode in the dual-MOSFET RB switch structure, preventing large device voltage stresses, additional device losses, and increased EMI. In the 1 kW, 48 VDC to 120 VAC AC Cube, the Synchronous RB Switch enables an 11.1% efficiency improvement over conventional RB switch structures. In the case of the AC Cube modular drive unit, the Synchronous RB Switch enables a peak system efficiency of 98.4%. While not shown in Fig. 4.7(c), usage of the conventional MOSFET plus series SiC Schottky diode RB structure on both the 48 VDC and 480 VAC bridges would have yielded a peak efficiency of only 91.6%, decreasing to less than 80% at full load. Furthermore, each conventional RB switch position on the 48 VDC bridge would require three SiC Schottky diodes in parallel to reach this subpar efficiency, significantly increasing cost, cooling requirements, and converter size. Put together, these results evidence the ability of the Synchronous RB Switch to open application areas for the S4T previously rendered impractical due to the high conduction losses of conventional RB switch structures.

CHAPTER 5
CONCLUSIONS

The Synchronous Reverse Blocking Switch proposed and validated in this work offers a seamless method to integrate dual-active-switch structures into the S4T topology to enable high-efficiency low-voltage applications to address the growing market need for efficient, highly integrated, and feature rich low-voltage power interfaces. Together with the integrated gate driver and protection circuitry, the method is agnostic to the higher-level control architecture, applies to all variants of the S4T, and significantly reduces converter conduction losses by replacing diode conduction with MOSFET channel conduction. The control method leverages the unique switching environment of the S4T topology to virtually eliminate reverse recovery and the associated voltage stress and loss when standard silicon devices are used.

Compared to the use of dual-active-switch configurations in hard-switching current-source topologies, the Synchronous RB Switch within the S4T relies on simple and robust control principles, and yields a rugged and cost-effective solution applicable to all power device technologies, including newer silicon-carbide and gallium-nitride devices to scale in voltage and current. Device-level experiments have demonstrated the ability of the Synchronous RB Switch to mitigate the reverse recovery phenomenon of the body diodes of 100 V and 650 V Si MOSFETs and Si PN-junction fast-recovery diodes.

System-level experiments evidenced the alignment of the gate signal timing requirements of the Synchronous RB Switch to the inherent dynamics of the S4T. In a 750 W 48 VDC bridge power circulation experiment, the Synchronous RB Switch demonstrated conduction loss savings of 46.20 W, a 90% reduction, and in an example 1 kW 48 VDC to 120 VAC S4T, the Synchronous RB Switch offers an 11.1% efficiency improvement at full power when compared to conventional RB switch structures. For these reasons, the novel

Synchronous RB Switch is seen as a unique drop-in replacement solution for S4T converters to unlock ubiquitous, high-efficiency low-voltage power conversion applications.

5.1 Contributions and Directions for Future Work

The analysis presented in this thesis has produced two conference papers. The experimental validation of the switching dynamics of the dual-MOSFET RB structure and the gating principles of the Synchronous RB Switch have been published in the proceedings of the 2020 IEEE Energy Conversion Congress and Exposition (ECCE) [37]. In addition, the design and impact of the AC Cube modular drive unit, featuring a parallel stack of 48 VDC to 480 VAC low-voltage S4T modules and enabling a mixed-chemistry battery pack for system-level performance and range optimization, have been published in the proceedings of the 2020 IEEE Transportation Electrification Conference & Expo (ITEC) [12].

Future work will explore the characterization of Synchronous RB Switches at higher voltages and composed of wide-bandgap semiconductors, the simple and integrated fault protection mechanism preventing converter failure in case of transients or faults, the design and analysis of a low-cost and high efficiency low-voltage S4T converter using the Synchronous RB Switch gating technique, and the verification of benign interconnection dynamics in massively output-parallel low-voltage S4T based systems. One example of a modular AC Cube based system is presented in Fig. 5.1, targeted towards scalable, touch-safe, and low-cost electricity solutions for off-grid and poor-grid communities.

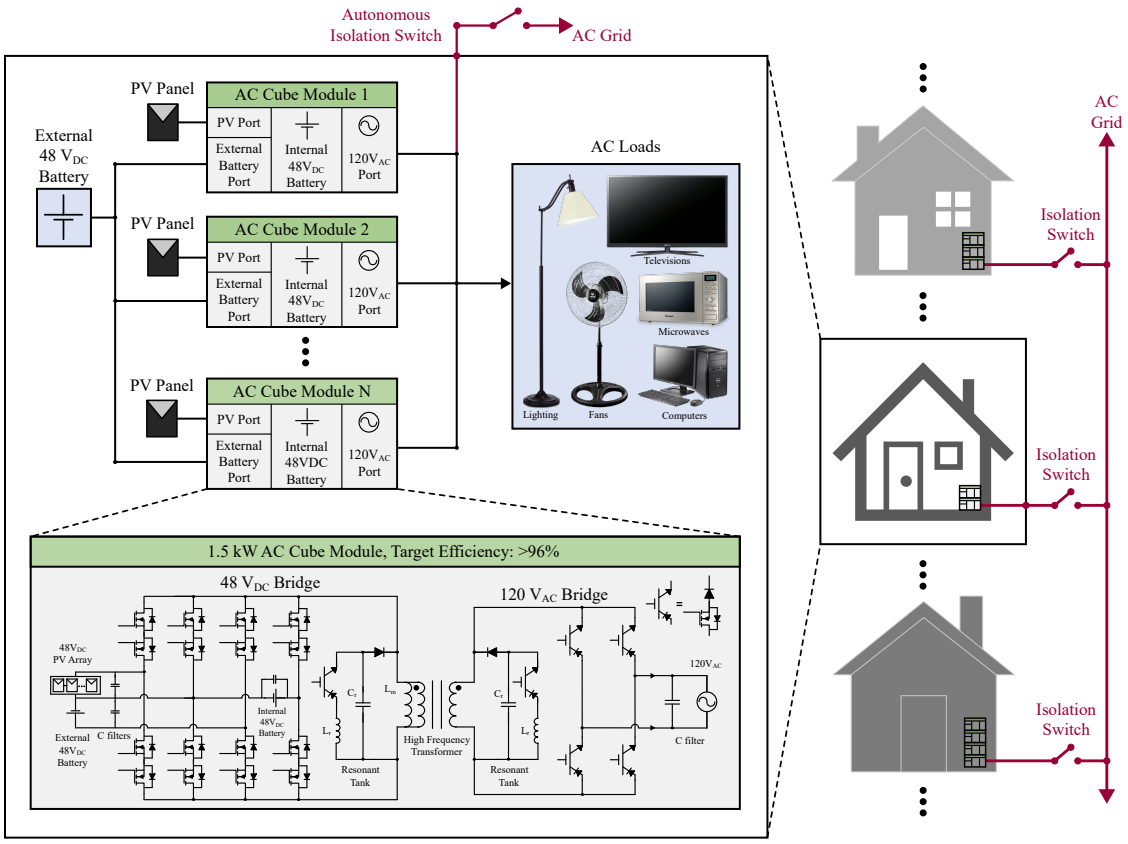


Figure 5.1: System-level diagram of an ad-hoc, multi-home microgrid based on the AC Cube 48 VDC to 120 VAC building block. Multiple AC Cubes can be interconnected to form a larger power subsystem to serve a single home. Multiple subsystems can be interconnected to form a larger multi-user system, enabling a scalable, modular microgrid architecture.

Appendices

APPENDIX A

ADDITIONAL IMAGE OF THE S_R REVERSE RECOVERY TEST APPARATUS

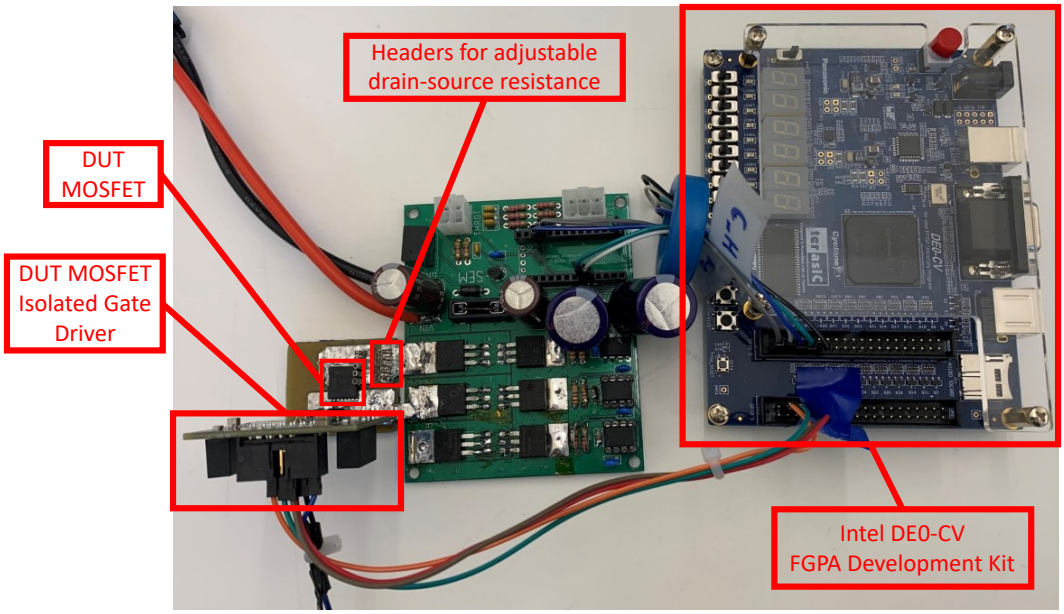


Figure A.1: S_R reverse recovery test apparatus showing the modified full-bridge based on the EasyController2 [36] in green, 50 MHz FPGA, DUT mounting board, and isolated DUT gate driver. Device drain-source current, I_{SD}, was varied by adjusting the value of resistor placed across the drain-source headers and by varying the full-bridge DC input voltage.

APPENDIX B

ADDITIONAL S_R REVERSE RECOVERY EXPERIMENT WAVEFORMS

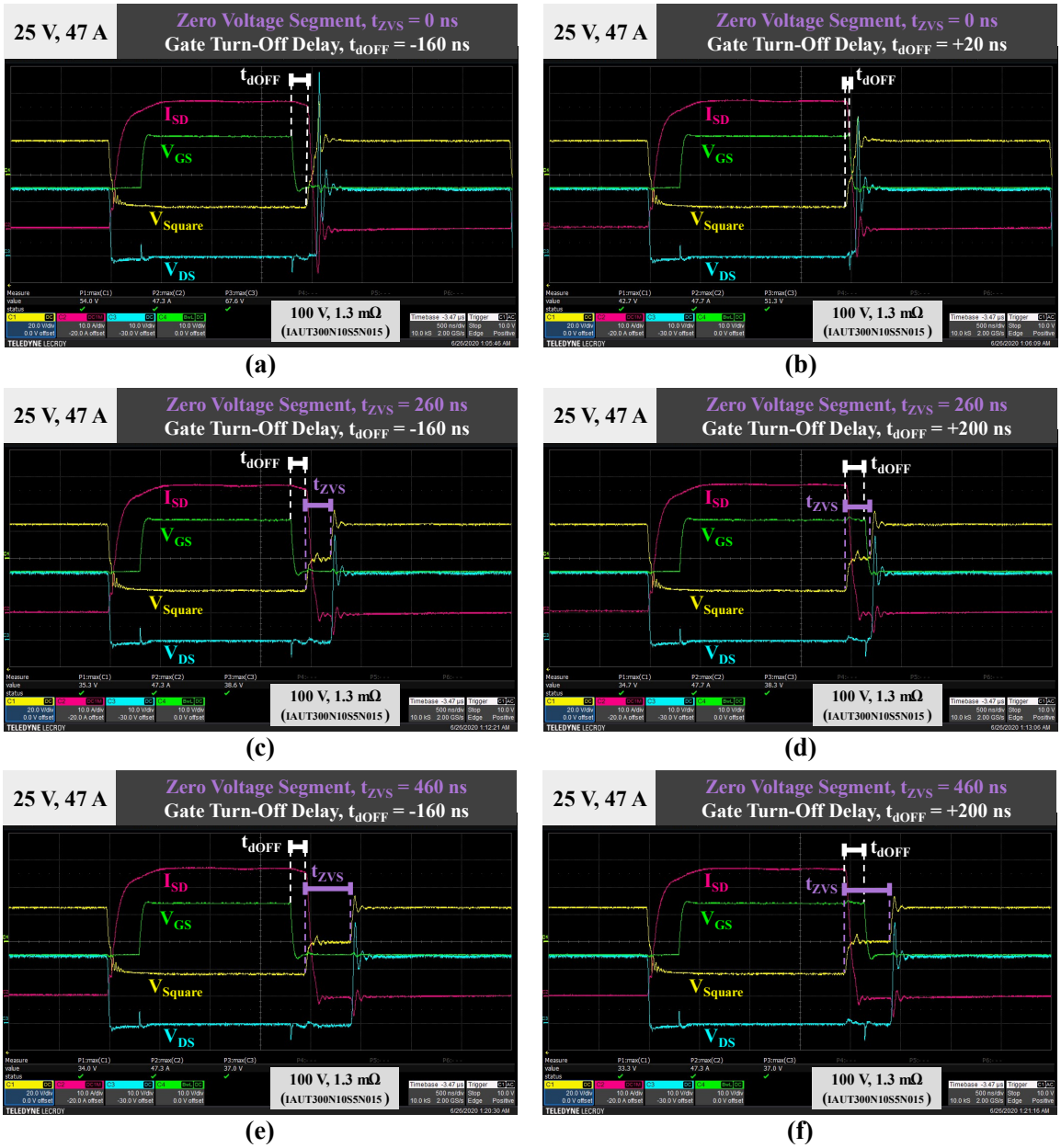


Figure B.1: Additional S_R characterization trials of the 100 V, 1.3 mΩ MOSFET (IAUT300N10S5N015). The oscillograms in (a) and (b) stem from trials with t_{ZVS} of 0 ns (hard-switching characterization). The oscillograms in (c), (d), (e), and (f) stem from trials with non zero t_{ZVS}, representing characterization under S4T-like switching waveforms. In each row, the left-side trial features negative or insufficient gate turn-off delay, t_{dOFF}, while the right-side trial features a positive t_{dOFF}.

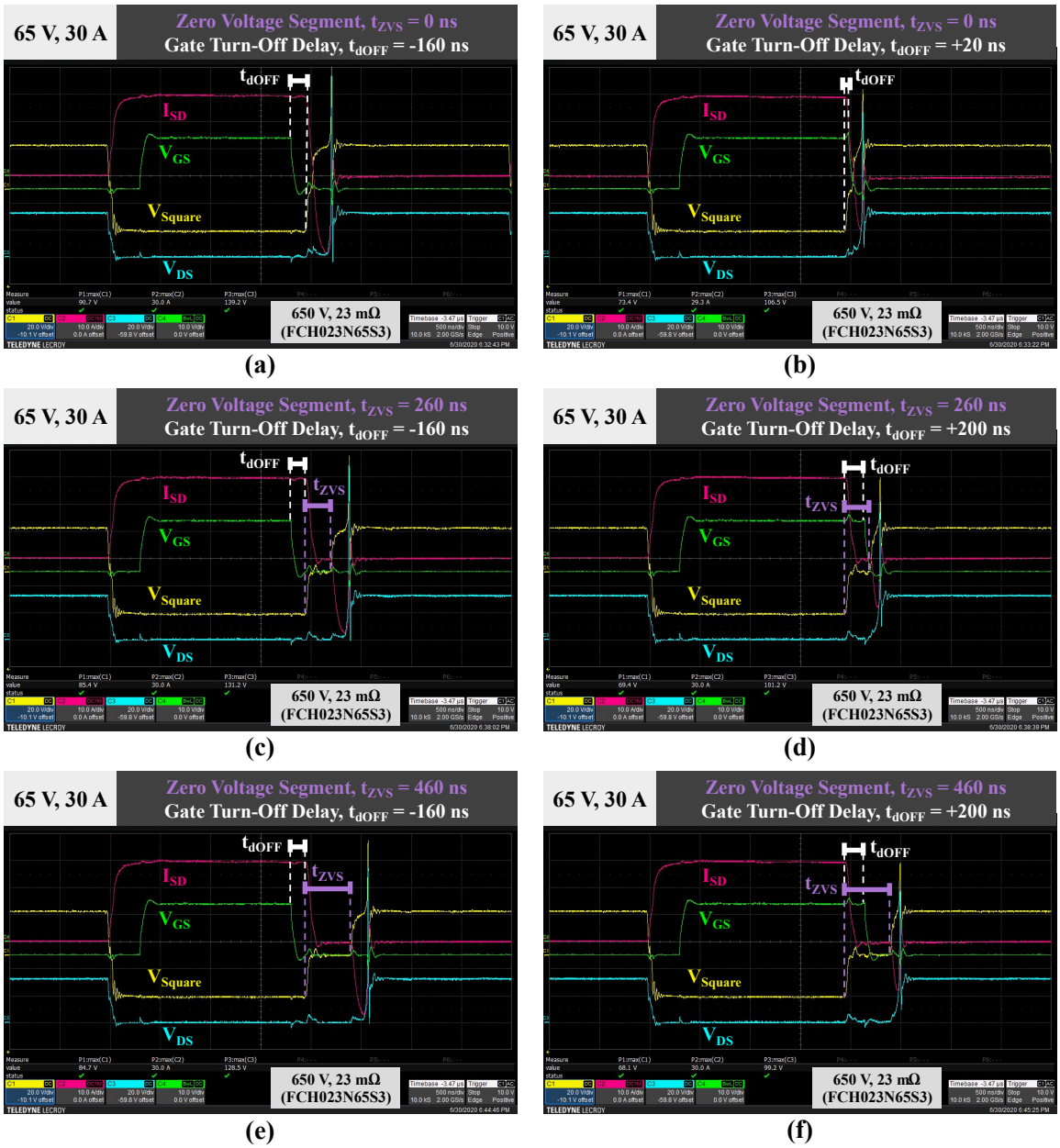


Figure B.2: Additional S_R characterization trials of the 650 V, 23 mΩ MOSFET (FCH02-3N65S3). The oscillograms in (a) and (b) stem from trials with t_{ZVS} of 0 ns (hard-switching characterization). The oscillograms in (c), (d), (e), and (f) stem from trials with non zero t_{ZVS}, representing characterization under S4T-like switching waveforms. In each row, the left-side trial features negative or insufficient gate turn-off delay, t_{dOFF}, while the right-side trial features a positive t_{dOFF}.

APPENDIX C

48 VDC S4T BRIDGE SCHEMATICS AND PCB DESIGN

C.1 48 VDC Bridge Schematic

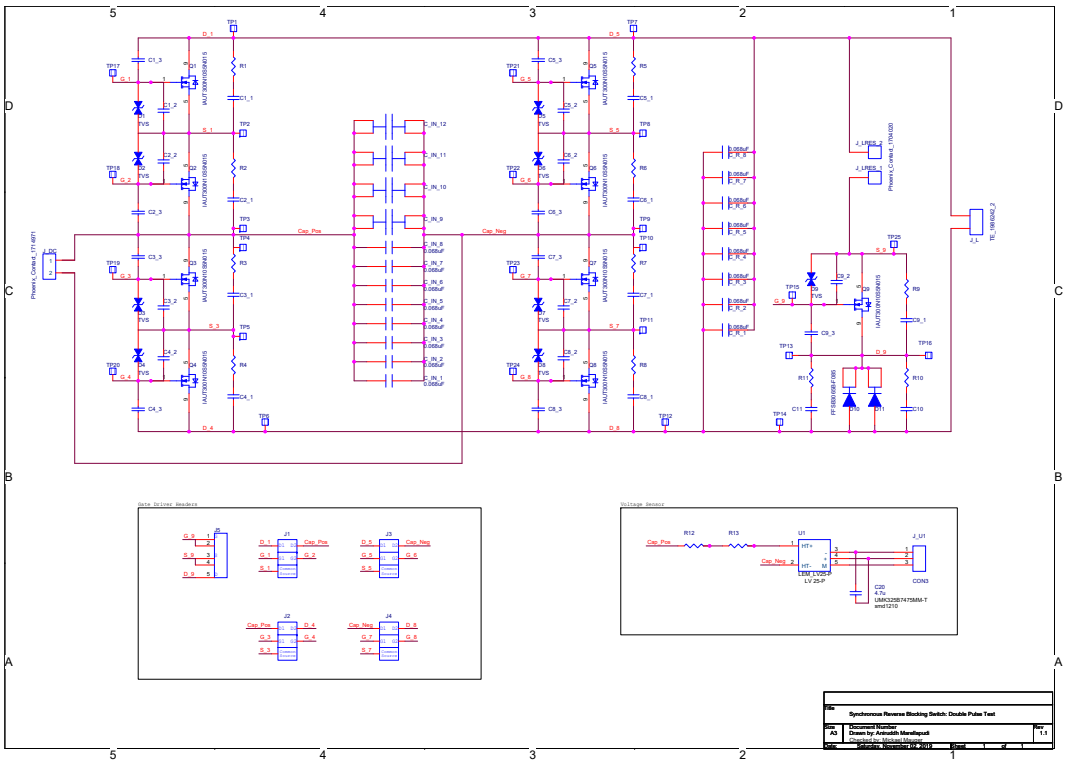


Figure C.1: High-current, 48 VDC S4T bridge circuit schematic drawn in OrCAD Capture CIS.

C.2 48 VDC Bridge PCB Design

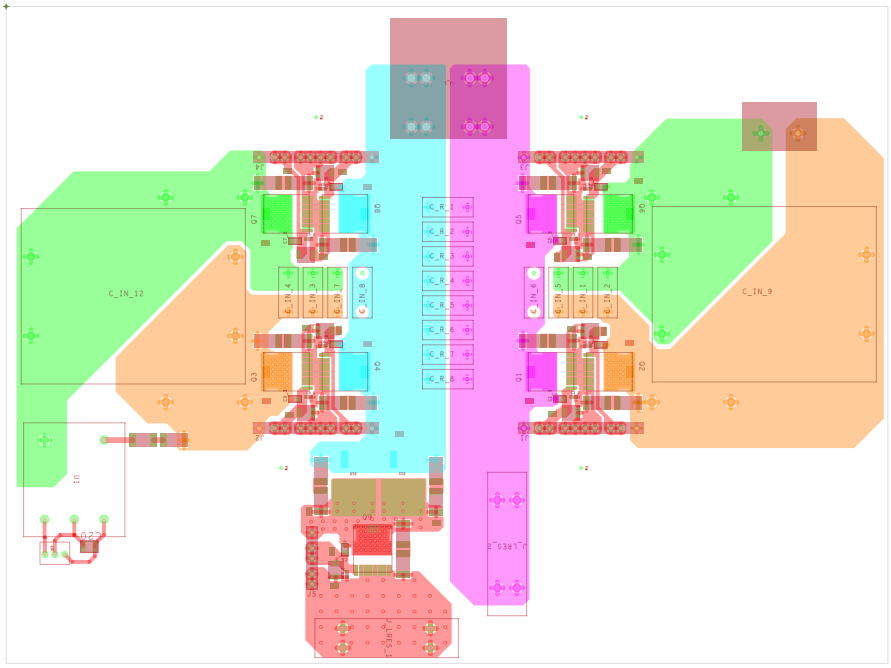


Figure C.2: Low-inductance PCB design of the 48 VDC S4T bridge, showing the top copper layer (layer 1 of 2).

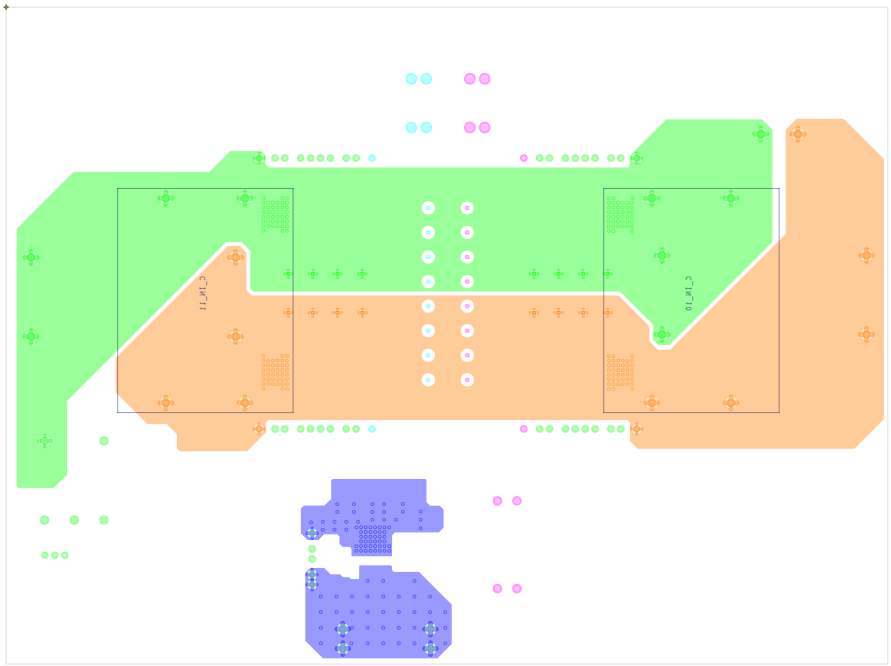


Figure C.3: Low-inductance PCB design of the 48 VDC S4T bridge, showing the bottom copper layer (layer 2 of 2).

C.3 48 VDC Bridge Built PCB Images

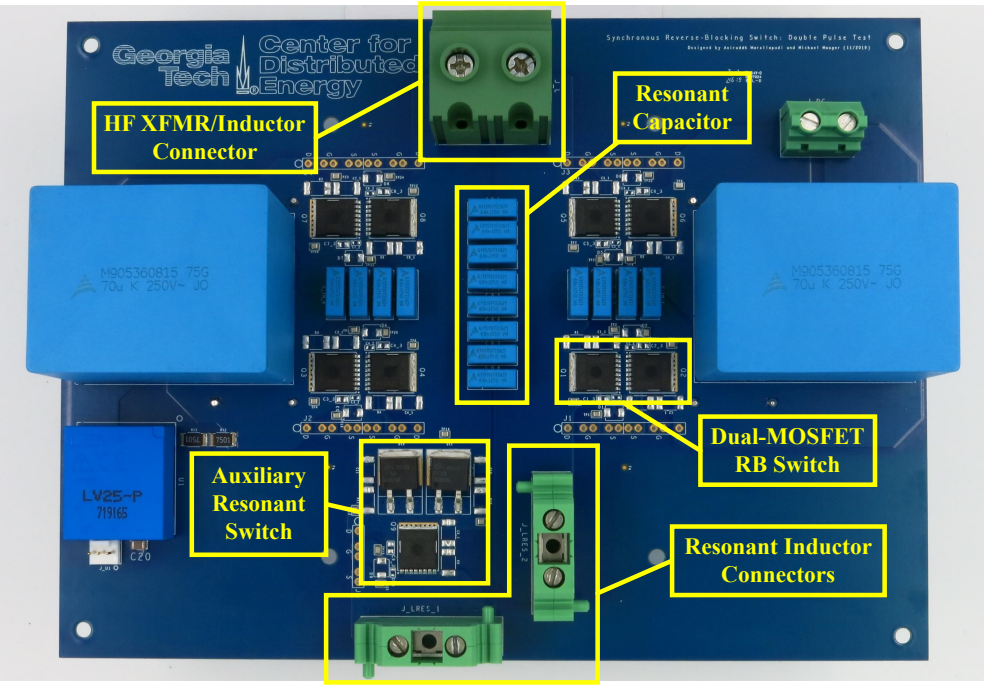


Figure C.4: High resolution picture of the built PCB of the 48 VDC S4T bridge. One dual-MOSFET RB switch, the auxiliary resonant switch, the resonant capacitors, and the L_m and L_r connectors are labelled.

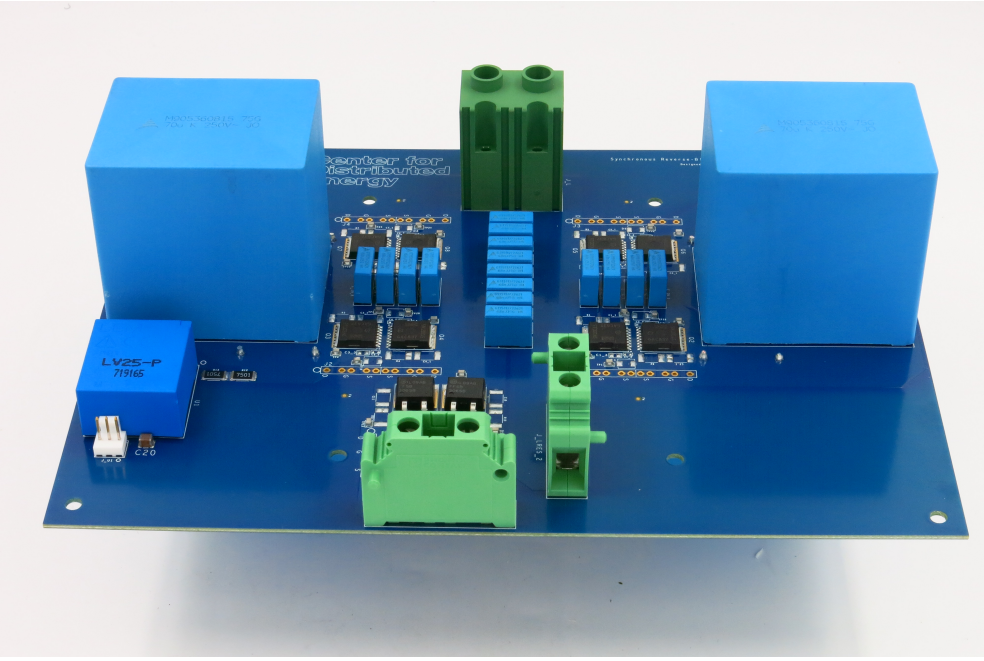


Figure C.5: High resolution side-view picture of the built PCB of the 48 VDC S4T bridge.

APPENDIX D

48 VDC BRIDGE GATE DRIVER SCHEMATICS AND PCB DESIGN

D.1 Gate Driver Schematics

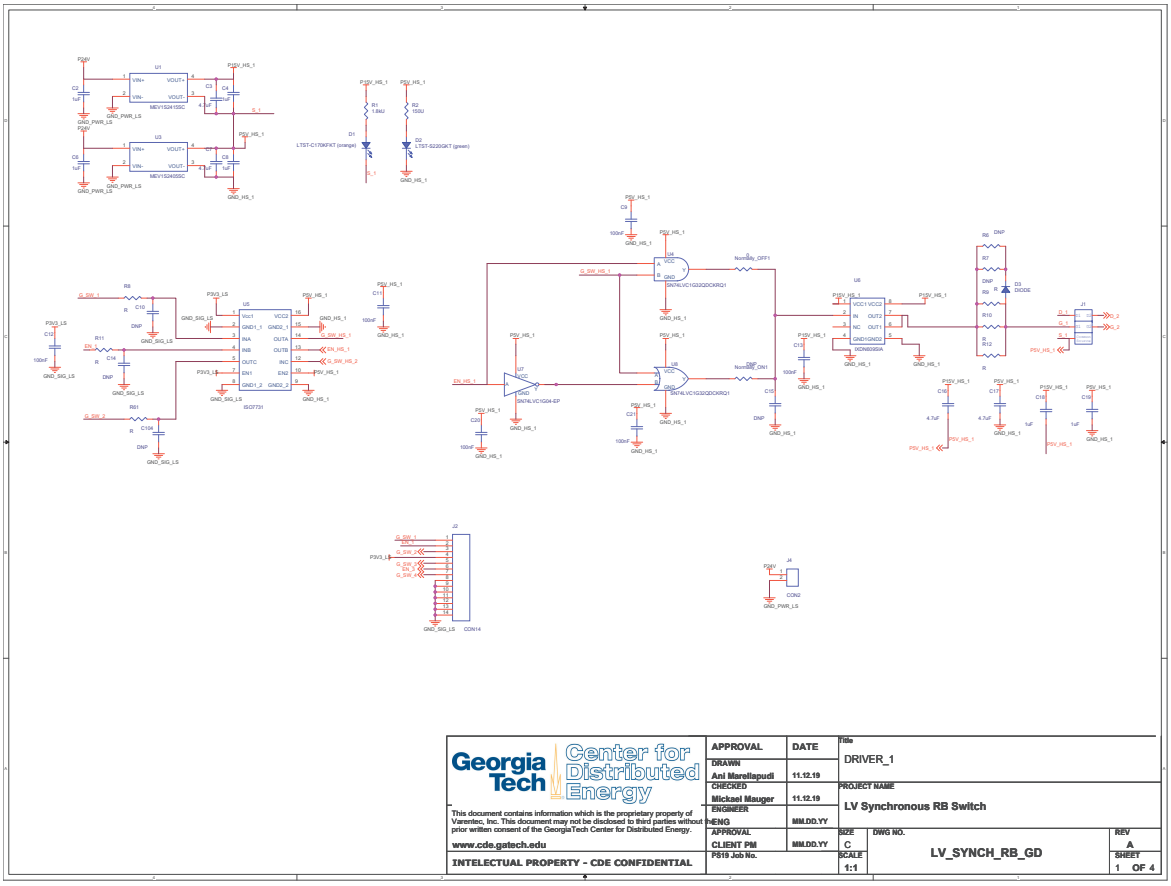


Figure D.1: Circuit schematic of the isolated +15 V / -5 V gate driver for the dual-MOSFET RB switch. Gating delays t_{dON} and t_{dOFF} are implemented in an upstream FPGA. Shown is page 1 of a single gate drive channel (corresponding to one dual-MOSFET RB structure).

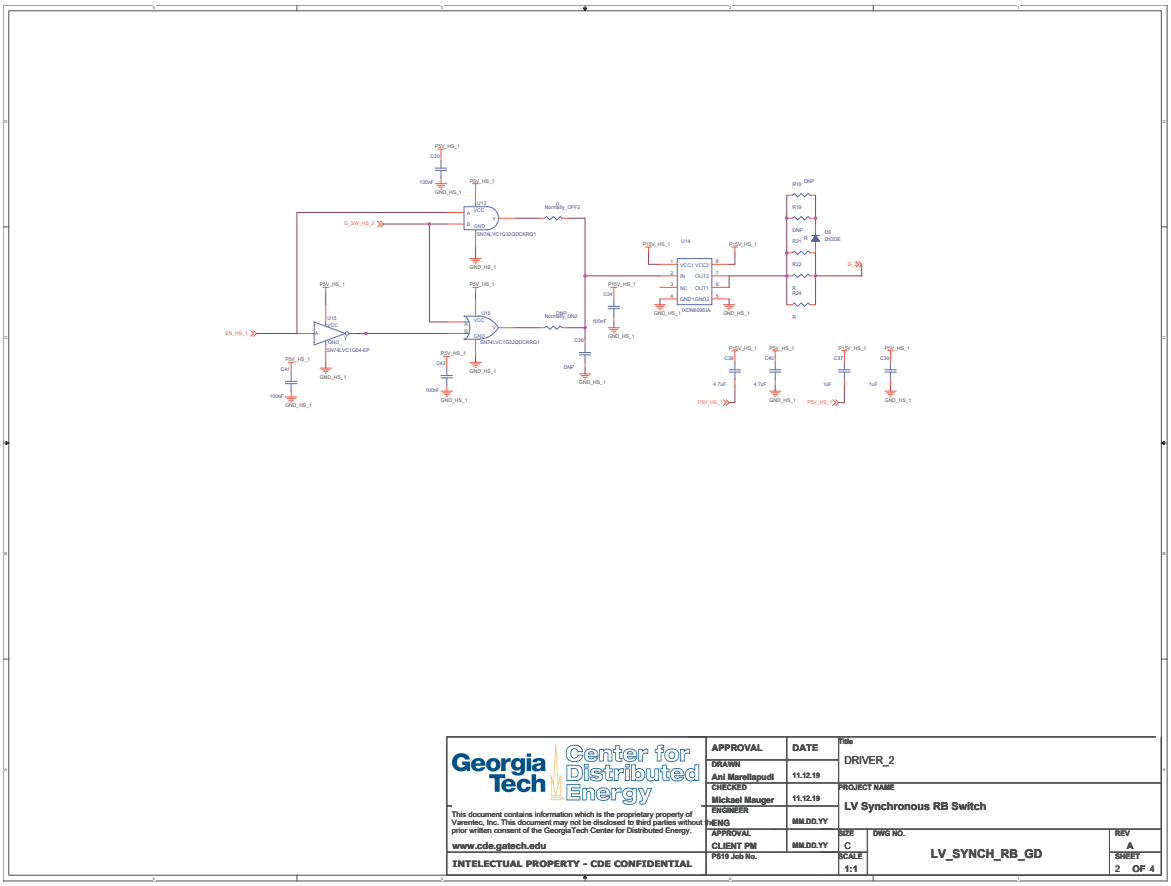


Figure D.2: Circuit schematic of the isolated +15 V / -5 V gate driver for the dual-MOSFET RB switch. Shown is page 2 of a single gate drive channel (corresponding to one dual-MOSFET RB structure).

D.2 Gate Driver PCB Design

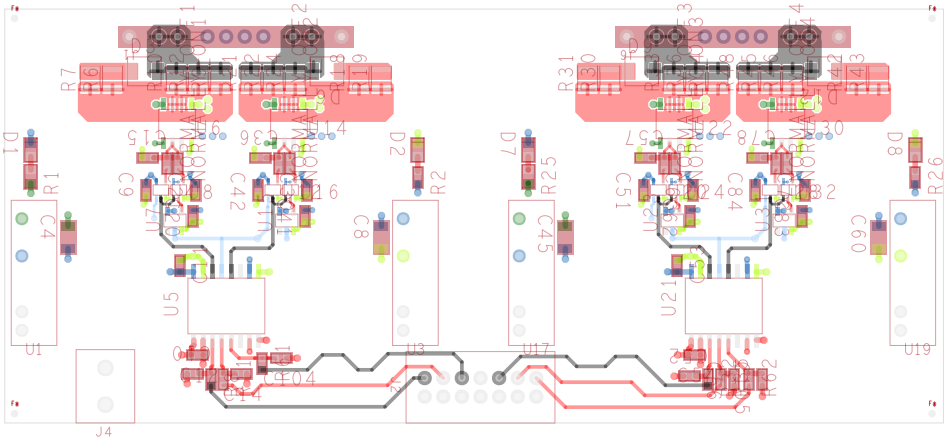


Figure D.3: PCB design of the 48 VDC S4T bridge gate driver, showing the top copper layer (layer 1 of 4).

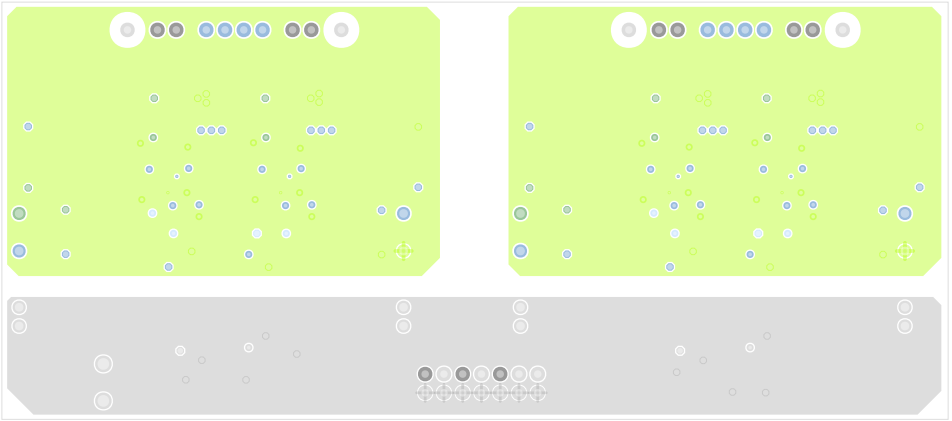


Figure D.4: PCB design of the 48 VDC S4T bridge gate driver, showing the second copper layer (layer 2 of 4).

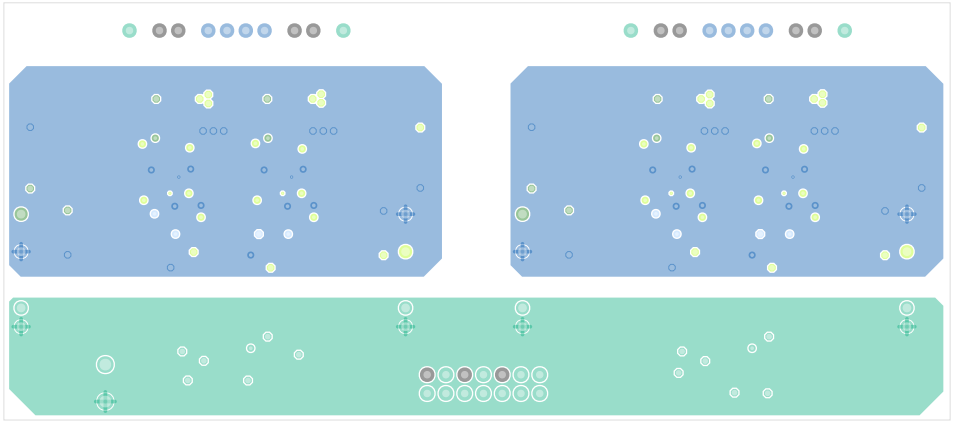


Figure D.5: PCB design of the 48 VDC S4T bridge gate driver, showing the third copper layer (layer 3 of 4).

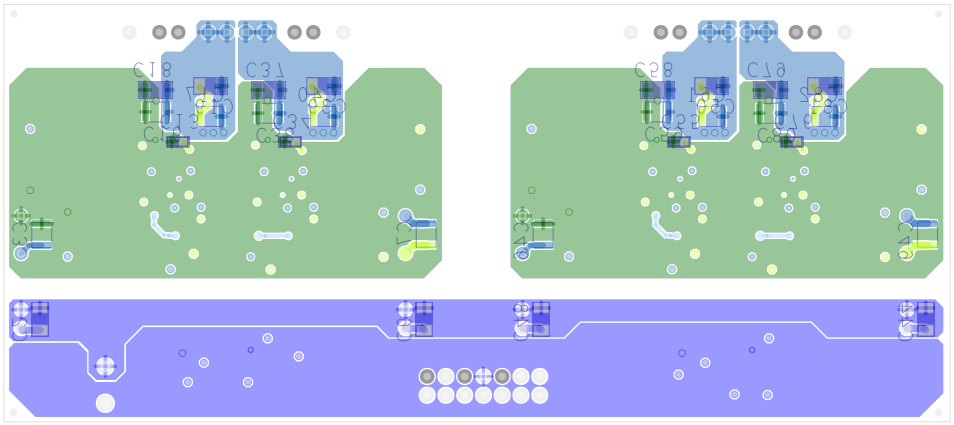


Figure D.6: PCB design of the 48 VDC S4T bridge gate driver, showing the fourth copper layer (layer 4 of 4).

D.3 Gate Driver Built PCB Image

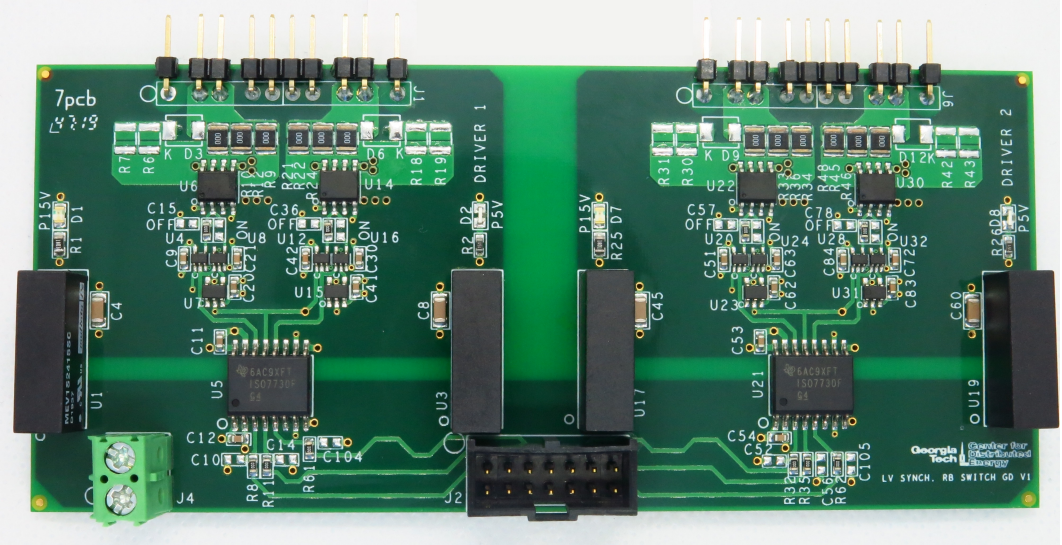


Figure D.7: High resolution picture of the built PCB of the 48 VDC S4T bridge gate driver. The gate driver mounts in a perpendicular manner to the power stage using the pin headers at the top of the PCB.

APPENDIX E

PROTOTYPE SYNCHRONOUS RB SWITCH GATE DRIVER DESIGN

E.1 Prototype Synchronous RB Switch Gate Driver Schematic

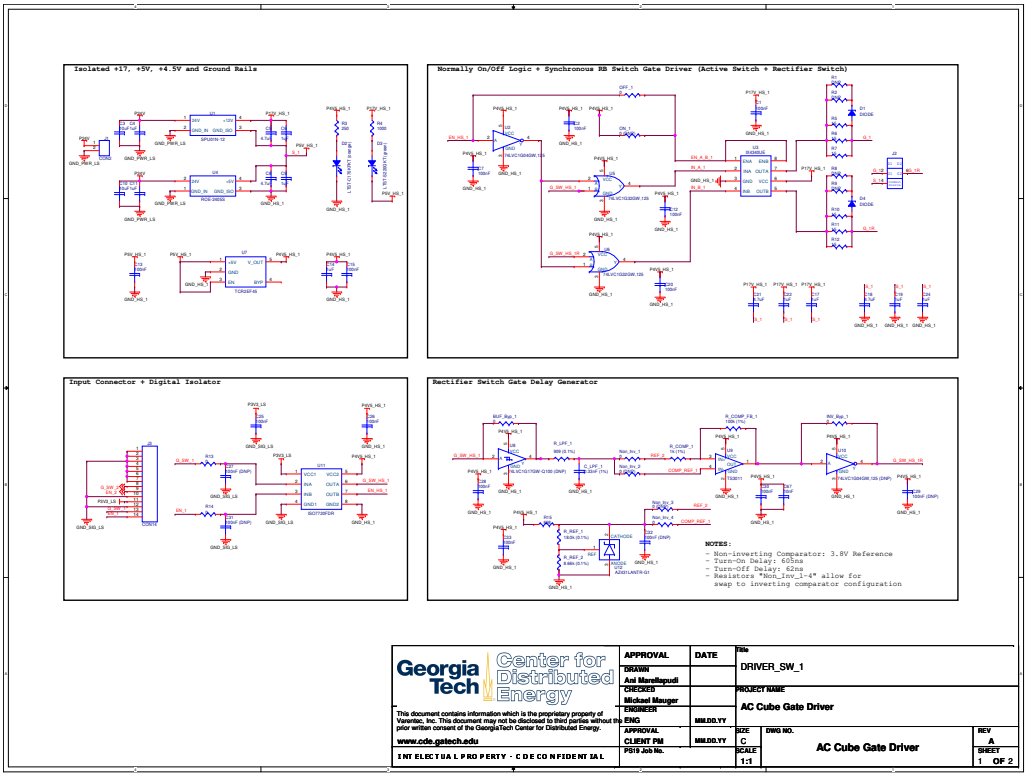


Figure E.1: Circuit schematic of the isolated +12 V / -5 V Synchronous RB Switch gate driver with integrated delay generation for the rectifier switch S_R. Shown is a single gate drive channel corresponding to one dual-MOSFET RB structure. The gate signal for the active switch S_A is provided by the upstream FPGA, while the gate delay timings t_{dON} and t_{dOFF} for S_R are implemented on board using the RC circuit plus comparator with hysteresis analyzed in Chapter 4.

E.2 Prototype Synchronous RB Switch Gate Driver PCB Design

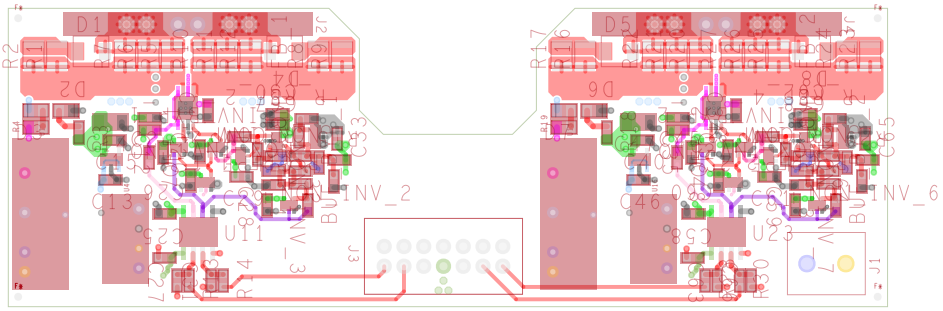


Figure E.2: PCB design of the prototype Synchronous RB Switch gate driver, showing the top copper layer (layer 1 of 4).

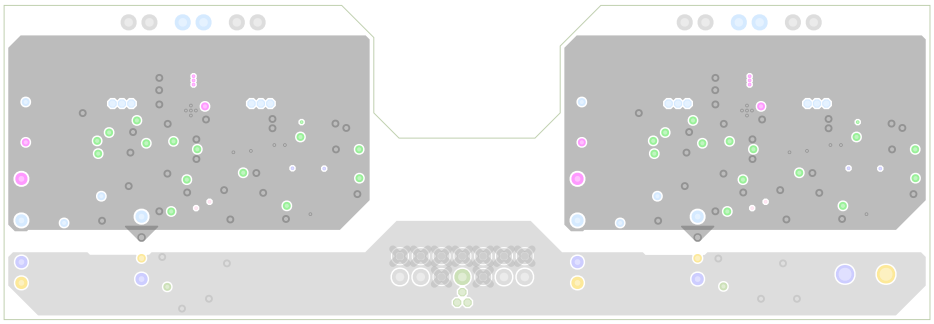


Figure E.3: PCB design of the prototype Synchronous RB Switch gate driver, showing the second copper layer (layer 2 of 4).

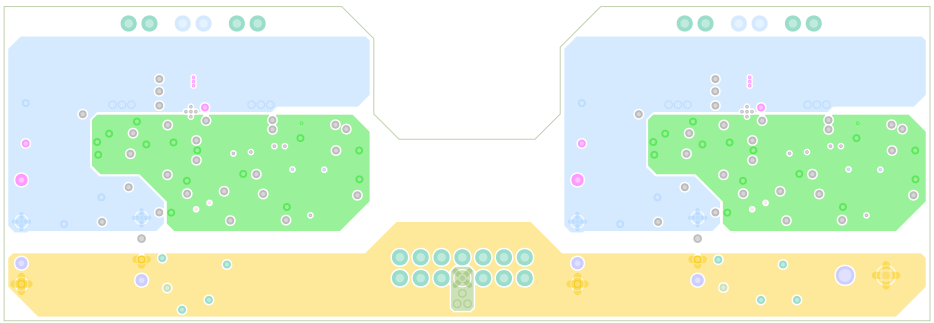


Figure E.4: PCB design of the prototype Synchronous RB Switch gate driver, showing the third copper layer (layer 3 of 4).

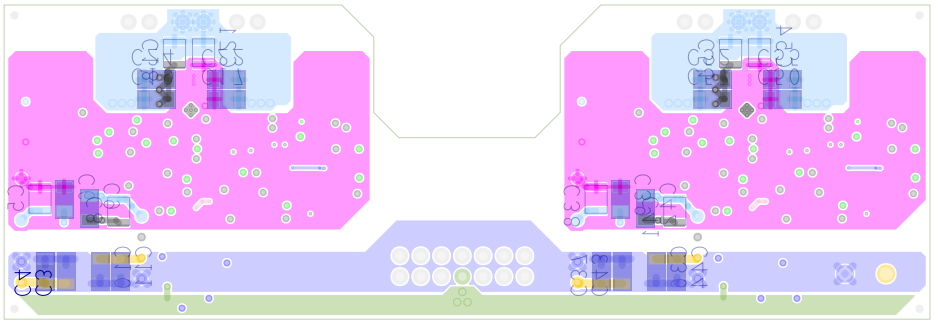


Figure E.5: PCB design of the prototype Synchronous RB Switch gate driver, showing the fourth copper layer (layer 4 of 4).

E.3 Prototype Synchronous RB Switch Gate Driver Built PCB Image

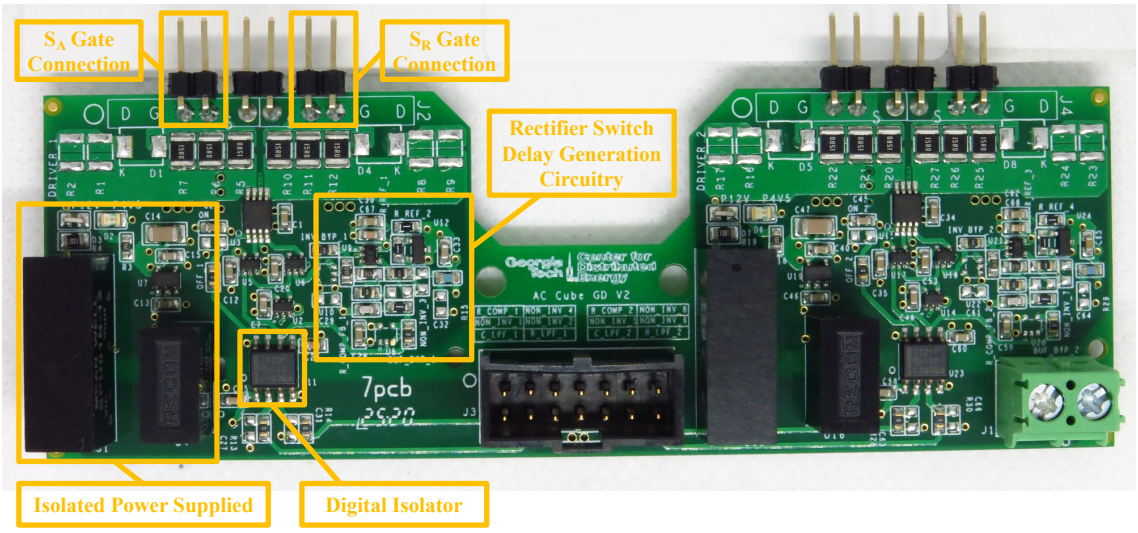


Figure E.6: High resolution picture of the built PCB of the prototype Synchronous RB Switch gate driver.

APPENDIX F

ADDITIONAL IMAGE OF THE 48 VDC S4T BRIDGE EXPERIMENTAL APPARATUS

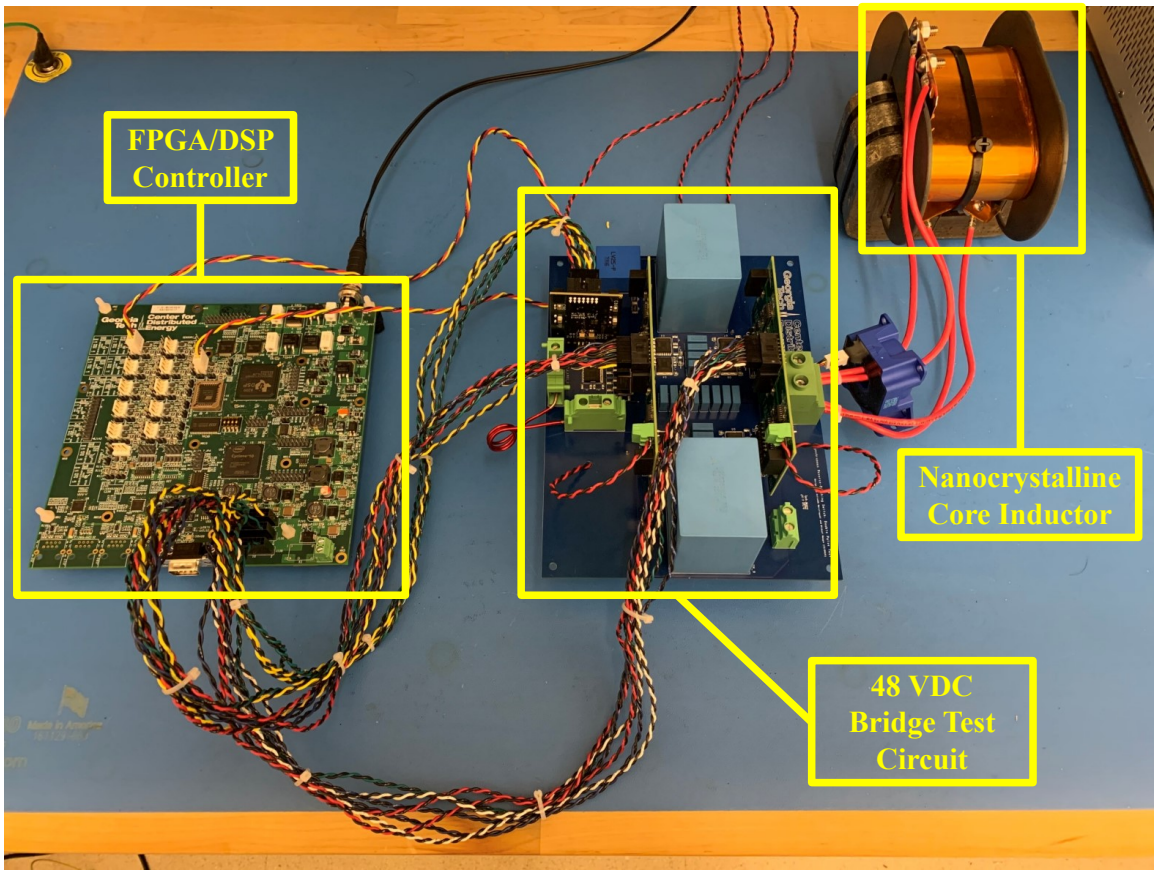


Figure F.1: Additional image of the experimental apparatus of the 48 VDC S4T bridge, pictured with the FPGA/DSP controller, gate drivers, the 72 μH nanocrystalline core inductor, and the 160 nH resonant inductor.

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