MACHINE LEARNING FOR AUTOMATING MILIMETER-WAVE ELECTROMAGNETIC DESIGNS

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MACHINE LEARNING FOR AUTOMATING MILIMETER-WAVE ELECTROMAGNETIC DESIGNS

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To the students at the Georgia Institute of Technology

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LIST OF SYMBOLS AND ABBREVIATIONS

EM   Electromagnetic

ML   Machine Learning

PA   Power Amplifiers

PBO   Power Back Off

SUMMARY

This dissertation proposes a general class of solution and Machine Learning (ML) techniques to support the designs of several critical Electromagnetic (EM) structures at mm-wave frequency ranges, for which the main applications are to directly address the emerging power and efficiency challenges of the next generation of wireless communication. Starting from the coupled line theory, we theoretically propose a common solution for Impedance Transforming Baluns, Power Combiners, Out-Phasing circuits, and Doherty networks, which we refer to as the BCOD structure. The main contribution of this dissertation is to develop Machine Learning techniques that, within the computational time of seconds, can fully automate EM designs of the BCOD network on various on-chip metal stacks for a wide range of electrical specifications. Training neural networks that accurately learn the physical-electrical relationship, we show that our ML models can accurately predict the electrical properties from physical dimensions, reducing the need for time-consuming full-wave EM simulations. From that, we formulate multiple ML algorithms for automating mm-wave designs, which drastically reduce design time from days-weeks-months to seconds, considerably improve the reliability of EM designs, and systematically accomplish the lowest metal loss. Notably, optimizing for the lowest metal loss is a challenging problem, and to the best of our knowledge, we are not aware of any prior techniques that can systematically do so.

Importantly, the application of our proposed ML approaches can go beyond the task of automating EM structures. Serving as a new tool for bigger optimization loops, the ML techniques can theoretically answer several challenging, abstract, and high-level questions

for mm-wave designs, such as the calculation of the optimum transistor sizes, or the derivation of the rule of thumb between device sizes and mm-wave frequencies.

CHAPTER 1.   INTRODUCTION

The next generation of wireless communication is moving toward mm-wave frequency ranges and above. With GHz channel bandwidth and Gsym/s modulation rates, mm-wave communication systems promise to deliver 100 to 1000 times higher channel capacity and data throughput than the current radiofrequency (RF) systems. This extreme data rate will allow life-changing experiences on various applications, such as the fifth generation (5G) wireless network, virtual reality (VR), augmented reality (AR), cloud computing, radar, and driverless automobiles. The next generation of wireless communication will transform our entire infrastructure for extreme indoor/outdoor conditions, remote control, aviation, robotic, ultra-broadband communication (>10Gb/s), object tracking, critical infrastructure protection and control, smart grid, smart homes/building cities, and smart wearable devices. With this premise, enhanced mobile broadband could achieve faster and more uniform user experiences, massive internet of things could have more efficient communication with a deeper coverage, and mission-critical control could accomplish ultra-low latency and high reliability.

With the next wave of technology, researchers have focused on designing robust and efficient mm-wave systems to pave the way for future generations of mm-wave wireless communication. On one hand, the fundamental drawback is that mm-wave ranges are close to the cut-off frequencies of transistors where the active devices exhibit inferior performance. On the other hand, the major challenges are centered on the power and efficiency of mm-wave systems, which the power challenge implies designing mm-wave systems with adequate output power to overcome extreme mm-wave path loss, and the

efficiency challenge involves improving the average efficiency of the entire mm-wave system when transmitting modulated signals.

The development of mm-wave circuits has been driven by the innovation of electromagnetic (EM) or passive structures. Mm-wave designs have two complementary parts: active circuits and passive structures. Limited innovations in the last two decades were on the side of active circuits. Because active devices exhibit similar functionalities in both the RF and mm-wave frequencies, researchers still employ conventional techniques at RF bands to design active circuits at mm-wave frequency ranges. At the same time, over the last two decades, researchers have extensively explored various novel EM structures to design numerous mm-wave tasks, where the clear shift in design paradigms are from lumped EM structures at RF frequencies to distributed EM structures at mm-wave ranges.

Challenges

Designing novel EM structures is the central research approach to resolve the emerging mm-Wave challenges. For example, the major research direction to resolve the power challenge at mm-wave frequencies has been to design efficient mm-wave EM structures that can combine power from as many active devices as possible. Additionally, the main direction to improve mm-wave efficiencies when transmitting modulated signals has been to explore Out-Phasing circuits or Doherty networks. The current bottleneck of those efficiency solutions is the realization of EM structures for the output networks of Out-Phasing and Doherty structures. Numerous attempts have been directed to design Power Combiners, Out-Phasing circuits, and Doherty networks, but all those designs appear to be separate topics. Additionally, most of the solutions proposed in the literature have been for

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single-ended active cores, and to systematically design those EM structures for differential active circuits remains a major challenge.

Furthermore, a full EM design includes a physical realization of a theoretical EM structure. Conventionally, this full EM design is often achieved by iteratively updating physical dimensions obtained from simulated results of commercial EM solvers, which engineers and researchers often take many iteration steps to complete a single EM design. The current approach to physically realize EM structures exhibits several major drawbacks. The computational time of commercial EM simulators is slow, such that the overall EM design often consumes a large amount of time and labor. Also, the iterative process, which involves manual updates of design parameters, often exhibits a high variance in the quality of designs, as these updates can be highly random and subjective to the experiences and impromptu decisions of circuit designers.

The drawbacks of time consuming, labor intensive, and high variance of the current approach to design EM structures motivates us to brainstorm a new approach. Particularly, we see value in adding the new dimension of Machine Learning (ML) to existing EM methods, and from that we formulate ML techniques that can resolve many drawbacks of the current approaches used to design mm-wave EM structures.

Approaches and Contributions

In this dissertation, we develop theoretical and Machine Learning techniques to design mm-wave EM structures that resolve various challenges of the next generation of wireless communication. The first contribution of the thesis is to propose a class of solutions for mm-wave EM structures that can answer both the power and efficiency mm-wave

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challenges. We apply theoretical analysis to develop a unified design element for a variety of mm-wave design tasks, including Impedance Transforming Baluns, Combiners, Out-Phasing circuits, and Doherty networks, which we refer to as the BCOD structure. Moreover, the main contribution of this thesis is our proposed automation techniques that break the fundamental bottlenecks of the current approaches to design EM structures. Adding a Machine Learning (ML) dimension to the existing EM approaches, we present a technique to train ML models that can accurately predict electrical labels, and from that we develop various automation architectures that can drastically reduce the design time, decrease the variance, and improve the EM design quality.

Combining our BCOD theoretical solutions and our proposed automation pipeline with Machine Learning techniques, we illustrate various pipelines that can fully automate the EM designs of critical mm-wave structures, such as Directional Couplers, Impedance Transforming Baluns, Power Combiners, Out-Phasing circuits, and Doherty networks. With our proposed approaches, the full EM structures that resolve the mm-wave power and efficiency challenges can be accurately designed within a matter of seconds. Notably, our techniques can directly optimize EM circuits for the lowest metal loss. To the best of our knowledge, we are not aware of any prior work that can systematically resolve the lowest metal loss specifications.

From the Machine Learning models we built, interestingly, we have a tool to answer many challenging, abstract, and high-level circuit questions. For example, the critical question when working with a new process at a new frequency is to select the optimum device size that maximizes power or efficiency, but how to address this high-level question is a challenge. Additionally, the well-known rule of thumb for mm-wave designers is that

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the size of transistors decreases as the mm-wave frequency goes up, but how to quantify this relationship remains elusive. We will apply the Machine Learning approaches we built to answer those high-level questions.

In section 1.1, we begin our dissertation by reviewing the literature on recent efforts to design mm-wave architectures and EM structures that can address various emerging mm-wave challenges. We then review several prior works that apply Machine Learning techniques to design EM circuits in section 1.2. Lastly, we discuss the problem scope and the organization of this dissertation in section 1.3.

1.1 Literature Survey on EM Structures for Mm-Wave Designs

Various prior publications have explored techniques to resolve the fundamental challenges of mm-wave designs, which includes designing Power Combiners to boost the mm-wave output power and implementing the Out-Phasing circuits and Doherty networks to improve mm-wave average efficiencies when transmitting modulated signals. We summarize the latest techniques in this literature survey.

Power Combiner Techniques
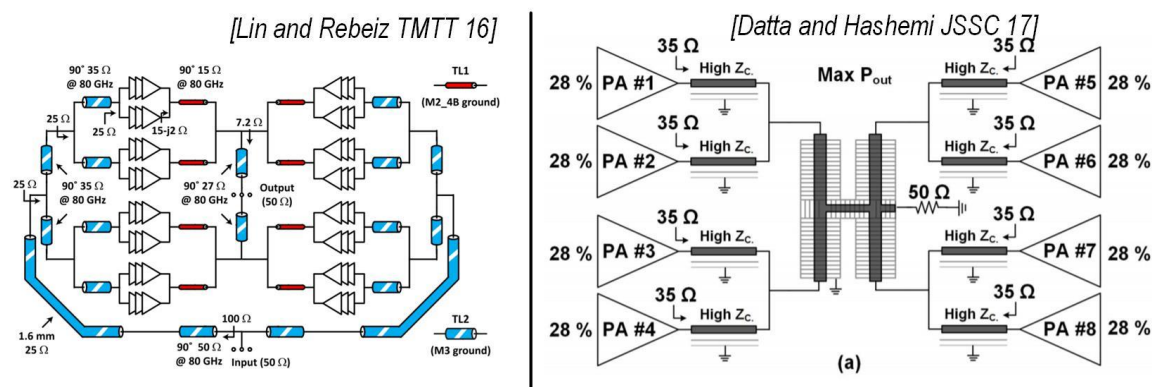
Figure 1.1 Examples of T-Line combiners in the literature.

Viewed as the key to boost the output power of transmitter systems, Power Combiners at mm-wave have been a major topic of research in the last two decades. Particularly, researchers have regularly revisited two major directions: Parallel-connected (or T-Line) and series-connected (or Distributed Active Transformers) combiners. Figure 1.1 depicts the T-Line combiners in several state-of-the-art mm-wave circuits. The T-Line structures, which combine signals at T-junctions, can efficiently support a wide range of impedance transformation and effectively combine power from many cells. For example, recent publications have demonstrated 1-to-8, 1-to-16, or 1-to-32 power combiners with the T-line structure [1]-[8]. Although scalable and easy to use, the structure can only combine power from single-ended ports. Additionally, a design might exhibit an excessive amount of passive loss when T-Line traces are lengthened to increase the number of combined cells. Isolation between power cells is not necessary, but if imposed, one direction is to design an isolation resistor as commonly used in Wilkinson power dividers/combiners.
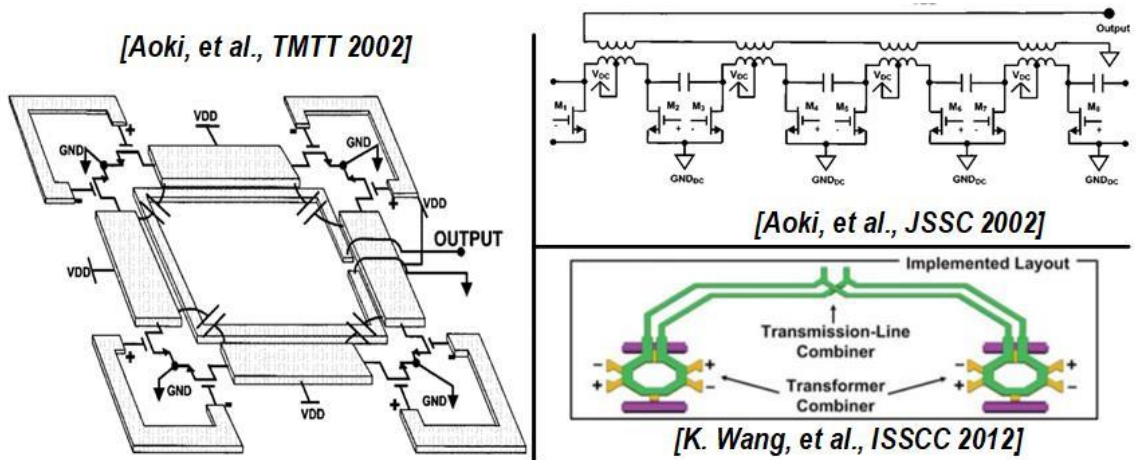
Figure 1.2 Examples of series-connected Power Combiners from the literature.

Furthermore, Fig. 1.2 illustrates the series-connected power combiners that have continuously drawn attention from researchers ever since the publications from California Institute of Technology demonstrated the first >1W CMOS Power Amplifier (PA) at RF frequency (2GHz) in the early 2000s [9][10]. Named as Distributed Active Transformers in one specific layout, the structure can be viewed as the default choice when designing transmitters at RF frequencies by both academic and industrial designs. However, the usage of this network at mm-wave has always been a topic of debate over the last two decades [11][12]. Most publications criticize the capacitive coupling for distorting impedances seen by active cells and causing the structure not to work in mm-wave frequency ranges.

Efficiency Techniques: Out-Phasing and Doherty Circuits

To efficiently transmit modulated signals with large Peak-to-Average Power Ratios (PAPR), such as 64-QAM or OFDM, mm-wave transmitters must be efficient at both peak power and deep Power Back-Off (PBO). This goal motivates mm-wave circuit designers to explore various advanced techniques, such as Out-Phasing or Doherty circuits, rather than the conventional class-AB amplifiers to construct a mm-wave system with an additional efficiency peak at deep PBO. The common insights of those techniques are to actively modulate the output load, so that the impedance seen by PA cells can increase to meet the load-pull condition at lower output power, subsequently creating an additional efficiency peak at PBO. Invented in the early 1930s, both Out-phasing and Doherty architectures are still the major directions in recent research efforts to solve the efficiency challenges when transmitting modulated signals [14]-[29].

Out-Phasing Techniques

Invented earlier was the Out-Phasing architecture that utilizes Out-Phasing circuits together with Chirex compensation on the Out-Phasing inputs between 2 signal paths to accomplish the second efficiency peak at PBO (see Fig. 1.3) [13]. However, researchers often criticize the generation of Out-Phasing signals that involves substantial digital pre-distortion and baseband overhead for being the major bottleneck when deploying Out-Phasing systems in practice.
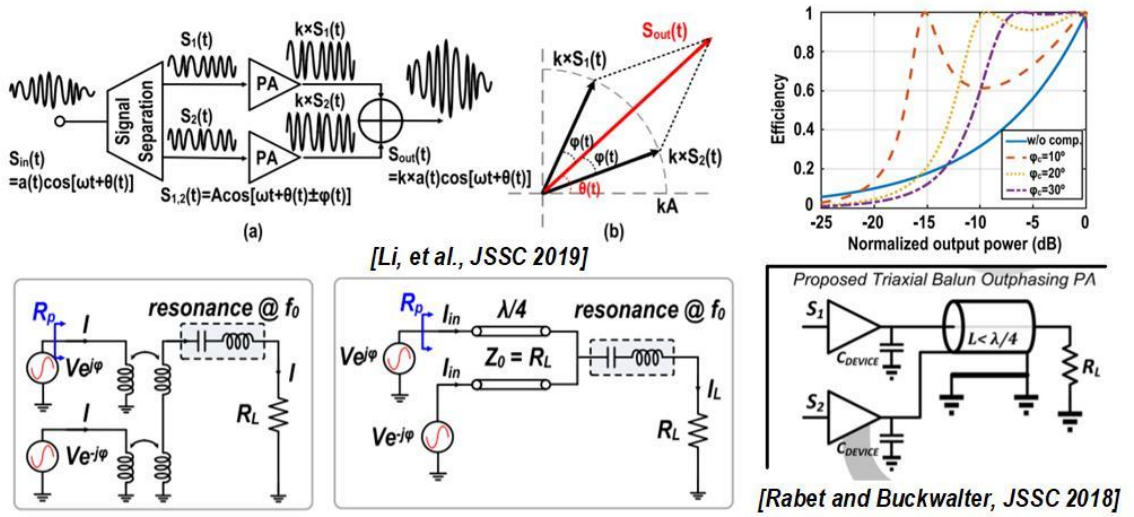
Figure 1.3 Conceptual drawing of the Out-Phasing system and the Out-Phasing network as a non-isolating power combiner.

Although Out-Phasing architectures might look complex in appearance, after working out the math, the key to design is essentially a non-isolating power combiner that sums the input voltages (see Fig. 1.3). Researchers have actively focused on proposing novel electromagnetic (EM) structures to design these non-isolating circuits in recent years [14]-[19]. For example, [18] presents a triaxial balun Out-Phasing PA, while [19] illustrates an

on-antenna Out-Phasing network. Both papers agree that implementing an efficient Out-Phasing combiner is the major challenge when designing Out-Phasing architectures.

Doherty Techniques
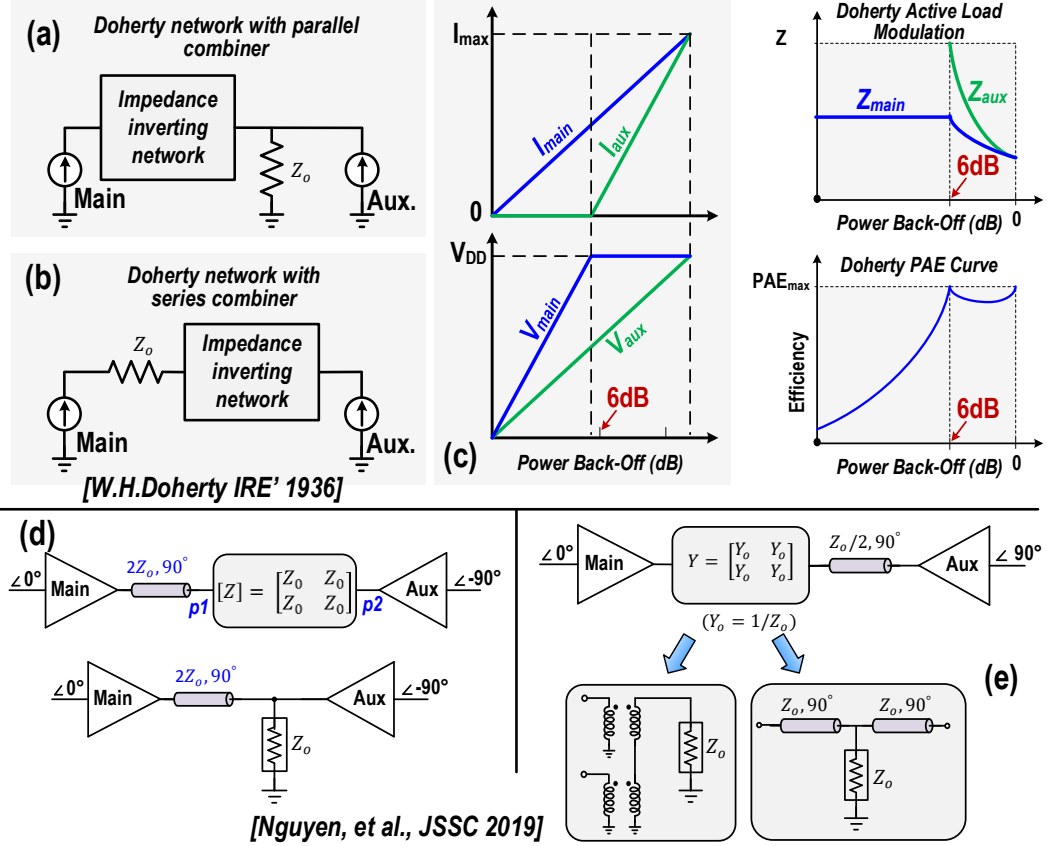
Figure 1.4 Conceptual drawing of the Doherty architecture with parallel and series combiners, the theoretical efficiency curve, and the Microwave network realization.

Willian Henry Doherty, who invented the architecture named after him in 1936 [20], introduced a novel scheme with Main and Auxiliary PAs that actively modulate the loads to enhance efficiency at 6dB PBO (see Fig. 1.4). Intrinsically demanding low baseband digital signal processing overhead and instantaneously supporting wideband modulation, the circuits proposed by Doherty remain a primary and popular choice of architectures to

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enhance efficiency at PBO almost a century after the original invention. These days, researchers still actively develop Doherty architectures for numerous electronic processes and at various frequency bands [21]-[29].

Two major challenges that researchers and engineers must overcome when designing Doherty systems are to accurately synchronize the operation of Main-Auxiliary PAs and to efficiently design Doherty output networks that actively modulate output loads. Synchronizing between PAs can be done by employing adaptive biasing circuits but designing an efficient Doherty output network remains a major challenge at high mm-wave frequency ranges.

1.2   Machine Learning for EM Designs

TABLE I
ERROR COMPARISON BETWEEN THE ANN MODEL AND EM SIMULATIONS FOR THE CPW SYMMETRIC T-JUNCTION. INPUT BRANCHLINE PORT IS PORT 1 AND THE OUTPUT PORTS ON THE MAIN LINE ARE PORTS 2 AND 3

	$|S_{11}|$	$\angle S_{11}$	$|S_{13}|$	$\angle S_{13}$	$|S_{23}|$	$\angle S_{23}$	$|S_{33}|$	$\angle S_{33}$
Training								
Average Error	0.00150	0.754	0.00071	0.176	0.00084	0.246	0.00106	0.633
Std. Deviation	0.00128	0.696	0.00058	0.172	0.00097	0.237	0.00109	0.546
Testing								
Average Error	0.00345	0.782	0.00088	0.141	0.00126	0.177	0.00083	0.838
Std. Deviation	0.00337	0.674	0.00085	0.125	0.00105	0.129	0.00068	0.717

Figure 1.5 Examples of EM design with Machine Learning (a) from [34], (b) from [37].

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Before coming back to the topic of mm-wave EM designs, we make a detour to review Machine Learning (ML) and its application to EM designs. Arguably one of the most active areas of research today, Machine Learning attempts to solve the fundamental problem of learning the relationship between inputs and outputs. Depending on various topics and fields of studies, the definition of inputs and outputs can be relatively abstract. For example, inputs can be the properties of a house, such as locations, areas, and furniture, and outputs can be the prices of houses. In Computer Vision, inputs can be images and outputs can be what objects are inside and where they are located, while in Natural Language Processing, inputs can be an English sentence and outputs can be a French sentence with the same meaning. In Human Computer Interaction, inputs can be a time-series signals from several sensors inside an iPhone, and outputs can be the actions the owners of these iPhone make. Substantial training data plus advancements in ML techniques allow a high level of accuracy when making these input-output predictions, leading to many ML models today even surpassing human's predictions.

In EM designs, we can apply Machine Learning to learn various input and output relationships (see Fig. 1.5) that are either computationally expensive or hard to compute. After "squeezing" the input-output information into a compact ML model, we can directly utilize optimization techniques to design Microwave circuits. For example, [34] builds a ML model to learn the performance of a CPW Symmetric T-Junction that achieves a very close result with EM simulation, and then uses this ML model instead of an EM simulator to optimize a CPW folded double-stub filter. The ML model has a much faster running time compared to the EM simulator, which allows the direct usage of gradient descent to optimize EM dimensions. Also, the ML model in [34] learns the large-signal behaviors of

a MESFET to design a 3 stage MMIC amplifier. [35] builds ML models to design spiral inductors, 4-pole, and 6-pole filters, while [36] presents a novel eigenmode-based ML model to automate the design of a microstrip Bandpass filter. In a different approach, [37] utilizes the latest development in Deep Reinforcement Learning to design patch antennas with improved antenna gain. General agreements are that many behaviors of passive/active components/circuits can be accurately learned by ML models. The computation time of ML models is much faster than running EM experiments from scratch, and the knowledge learnt by ML models can be directly applied to the related engineering tasks without the repetition of re-running full-wave EM experiments.

Applying Machine Learning techniques to solve mm-wave problems remains a rarely explored area. Mm-wave designs entail several key EM structures that are repeatedly used in many building mm-wave blocks. If some can spare an effort to collect data and train ML models that learn how to design these structures accurately and efficiently, the collected data and models would be useful for the entire community.

1.3 Problem Scope and Organization of The Dissertation

The last decade witnessed many active research activities in mm-wave designs. The deployment of the next generation of wireless communication has drawn researchers and engineers together at this frequency band. While RF circuit design often utilizes inductors and transformers, mm-wave design increasingly employs Microwave circuits. Driven by emerging mm-wave challenges, various microwave topics have emerged, and numerous microwave solutions have been proposed to resolve mm-wave challenges.

In this thesis, starting from the theory of coupled lines, we develop a common class of solutions for mm-wave EM designs that can resolve many emerging mm-wave challenges, which include Impedance Transforming Baluns, Power Combiners, Out-phasing circuits, and Doherty networks. We refer to the common solution as the BCOD structure, for which we will first formulate a general theory and then build various Machine Learning techniques to automate full EM designs of this class of solution. Interestingly, the Machine Learning approaches we develop can advance beyond the BCOD applications and serve as a new tool to help answer many high-level and abstract questions arising in mm-wave designs.

The organization this dissertation is as follows:

Chapter 2 discuss the theory of the proposed BCOD structure. We begin by defining an electrical specification, which involves output impedance Z_L, device optimum impedance Z_S, and device parasitic capacitance $Z_C = Z_S/Q$, for various critical EM structures such as baluns, combiners, Out-Phasing circuits, and Doherty networks. We then mathematically and numerically design the BCOD structure when given a mm-wave design task and a specification of Z_L, Z_S, and Q. Our derivation proves that theoretically the proposed BCOD structure has a broad design space that contains solutions for many emerging mm-wave challenges.

Chapter 3 employs Machine Learning models to accurately compute electrical properties of mm-wave circuits from physical dimensions, which the computation is conventionally done by commercial EM solvers. To build the ML models, we sample the physical dimensions from a continuous design space and simulate the EM structure to

collect data, extract electrical labels from simulated S-parameter files, and train neural networks to learn the relationship between the outputs as extracted electrical labels and the inputs as physical dimensions. Collecting data and training physical-electrical ML models for coupled lines and vanilla baluns, we employ the K-fold validation techniques to evaluate those ML models, where the validation results demonstrate the excellent accuracy of the prediction from ML models.

Chapter 4 and 5 propose several automation algorithms to fully automate the design of various EM structures, which includes Directional Couplers, Impedance Transforming Baluns, Power Combiners, Out-Phasing circuits, and Doherty networks. The proposed automation algorithms utilize the theoretical derivation in Chapter 2 to convert from high-level to mid-level electrical specifications and employ the pre-trained ML models in Chapter 3 to compute mid-level parameters from physical dimensions. With multiple initializations of physical dimensions and gradient descent, the algorithm gradually optimizes physical parameters to achieve the electrical specifications with the lowest loss. Chapter 4 demonstrates a number of automation algorithms that employ the ML models for coupled lines, while Chapter 5 shows several automation algorithms that use the ML models for vanilla baluns. Verified for numerous electrical specifications and dielectric thicknesses, the proposed algorithms can accurately automate EM structures for various EM design tasks within the design time of seconds.

Chapter 6 expands the Machine Learning approach to address several abstract and high-level questions concerning mm-wave designs. One of the challenges is to compute the optimum device size that results in highest efficiency when given the process and the frequency of operation. Another challenge is to qualify the relationship between device

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sizes and mm-wave frequencies, where the rule of thumb is to reduce the device sizes when operating at higher frequencies. Additionally, we also apply the Machine Learning technique to study the implementable range of electrical specifications for the BCOD structure. From the results in Chapter 6, we see that the ML approaches have opened doors and served as a new tool to understand many bigger pictures associated with mm-wave designs.

Chapter 7 concludes the dissertation and discusses several major directions for future research.

CHAPTER 2.   THE BCOD STRUCTURE: A THEORETICAL PERSPECTIVE

In this chapter, we develop a common class of solutions that can be utilized in a variety of mm-wave design tasks, including Impedance Transforming *B*aluns, Power *C*ombiners, *O*ut-Phasing circuits, and *D*oherty networks, which we refer to as the BCOD structure. As an extension of a Marchand balun with shorter electrical lengths and two lumped capacitors, the BCOD structure transfers power between differential active cores and a single-ended load to support the operation of a differential mm-wave architecture.

To develop a common theory for the BCOD structure in mm-wave designs that often involve strong parasitic capacitance, we redefine all design tasks into a common specification that includes a load impedance Z_L, an optimum source impedance Z_S (or R_{in}), and a device parasitic capacitance $Z_C = Z_S/Q$. From the theory of coupled lines and our mathematical analysis, we develop a numerical approach to theoretically solve the BCOD structure for arbitrary values of Z_L, Z_S, Q, which represents a wide range of electrical specifications in various scenarios of mm-wave designs. The theoretical analysis proves that the proposed BCOD structure has a broad design space that contains solutions for many emerging mm-wave challenges.

2.1   The BCOD Structure

In this dissertation, for many mm-wave design tasks, we develop a common class of solutions that involves Impedance Transforming *B*aluns, Power *C*ombiners, *O*ut-Phasing circuits, and *D*oherty networks. We call the common solution the "BCOD structure" to

annotate various applications of our proposed approaches. We confine the analysis of our proposed BCOD design in this dissertation to two basic structures: the vanilla coupler-based balun and the series-connected coupler-based balun (see Fig. 2.1), which presents an extension of the Marchand balun with shorter electrical lengths and several lumped capacitors. These structures, while simple in appearance, can resolve many emerging mm-wave challenges.
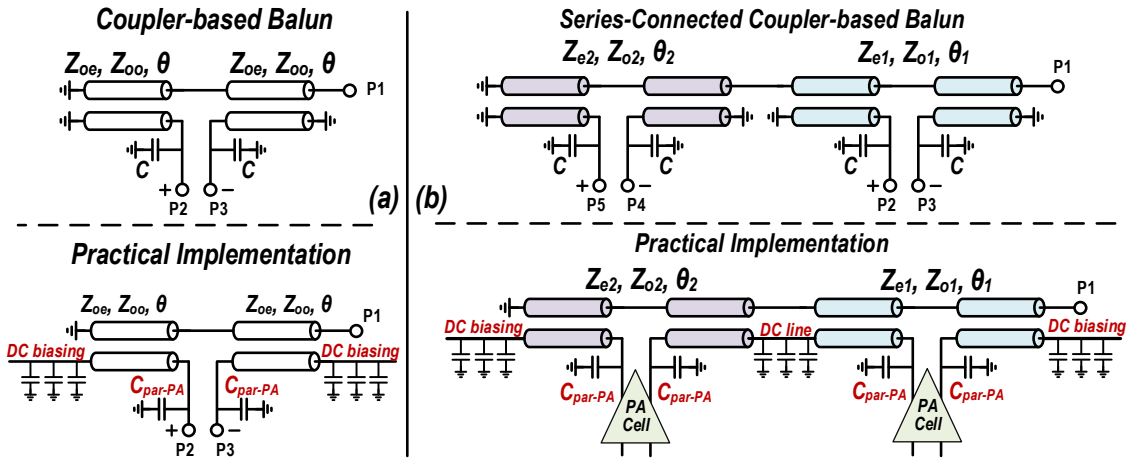
Figure 2.1 (a) The vanilla coupler-based balun and its practical implementation (b) The series-connected coupler-based balun and its practical implementation.

Figure 2.1a illustrates the *vanilla coupler-based balun*, which consists of two distributed coupled lines and two lumped capacitors. The balun property of the structure comes from the blocking of the even-mode transmission, as theoretically presented in [30]. In practical implementation, we utilize two AC short-circuited terminations to provide DC biasing without a choke and employ the lumped capacitors to naturally absorb the device parasitic capacitance of the PA core. The design space of the vanilla coupler-based balun includes 4 intrinsic design parameters Z_{oe}, Z_{oo}, θ, and C.

Depicted in Fig. 2.1b, the second structure we want to employ is the *series-connected coupler-based balun*, which extends the ideas of the vanilla coupler-based balun by cascading two coupler-based baluns in series. For simplicity, we constrain the design to use the same lumped C and Z_S for the two coupler sections. Compared to the vanilla coupler-based balun, the series-connected balun has *3 additional design dimensions: Z_{e2}, Z_{o2}, θ_2*. The combination of both structures can lead to solutions for designing many advanced mm-wave circuit architectures.

From the definition of the BCOD structure, section 2.2 redefines all design tasks into a common specification with a load impedance Z_L and differential active cores that with a load impedance Z_S and a parasitic capacitance $Z_C = Z_S/Q$. Section 2.3 mathematically derives solutions for Impedance Transforming Baluns, and sections 2.4 and 2.5 propose the solutions for Out-Phasing circuits and Doherty networks, respectively. We present several theoretical solutions for Power Combiners in section 2.6 and conclude the theoretical analysis in section 2.7.

2.2 Common Specifications for the BCOD Designs

The BCOD applications, including Impedance Transforming *B*aluns, Power *C*ombiners, *O*ut-Phasing circuits, and *D*oherty networks, might seem to be separate topics, but all share the similar design specifications and mechanisms. All applications require a transfer of power between a single-ended load with an impedance Z_L and differential active cores that inherently exhibit an optimum load Z_S with a device parasitic capacitance $Z_C = Z_S/Q$. To develop a common specification for those applications, in this section, we will define the BCOD design from an electrical specification of 3 parameters: Z_L, Z_S, and $Z_C = Z_S/Q$.

2.2.1 Impedance Transforming Baluns
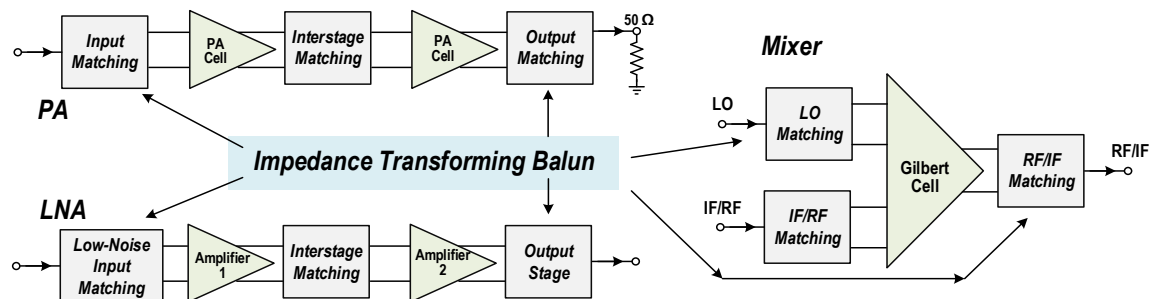
Figure 2.2 Examples of the use of Impedance Transforming Baluns in several mm-wave blocks.

The first structure we want to design is Impedance Transforming Baluns. Employed everywhere in mm-wave systems, Impedance Transforming Baluns match impedances from sources to loads, resonate out device parasitics, and convert differential to single-ended signals and vice versa (see Fig. 2.2). The Impedance Transforming Baluns at the output network of PA designs play a crucial role in determining the efficiency of entire mm-wave transmitter systems, because improving the loss of this output balun by 0.5dB increases the efficiency of the transmitter system by 10%. When used at the inputs in differential LNAs, the balun becomes critical for the overall Noise Figure of receiver systems, since an improvement of 1dB in the loss of an input balun boosts the Noise Figure of the receiver systems by 1dB. In balanced mixers, the mm-wave impedance transforming baluns are employed for matching at both RF and LO paths. The broadband design of PAs, LNAs, Mixers, and Phase Shifters requires broadband baluns that maintain the same transformation ratio over a broad bandwidth. Advancing the techniques used to design Impedance Transforming Baluns will assist the designs of all those mm-wave blocks.
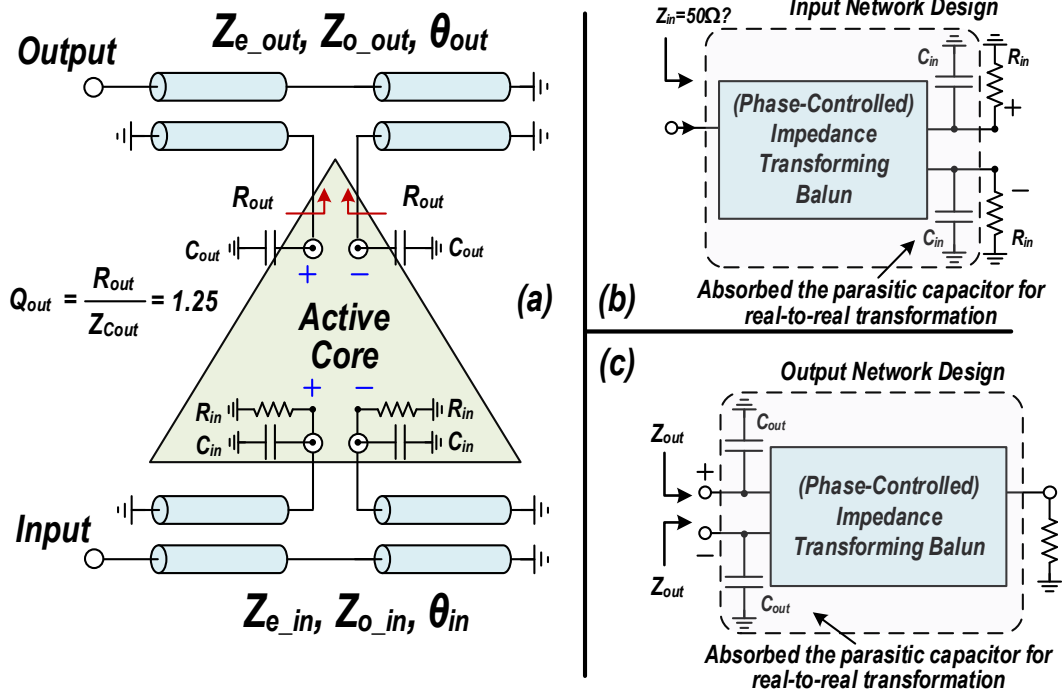
Figure 2.3 (a) Schematic of vanilla coupler at the input and output network. (b) An input network with C_{in} and (c) an output network with C_{out} absorbed inside the impedance transforming balun.

Regardless of the applications in PAs, LNAs, Mixers, etc., all differential cores have an input impedance R_{in}, a parasitic capacitance C_{in}, a parasitic capacitance C_{out}, and a desirable output load R_{out} (see Fig. 2.3a). While baluns in Microwave circuits and discrete components often work with standard 50Ω loads at both inputs and output, baluns in mm-wave designs must additionally resonate out the device parasitic impedance Z_C and perform impedance matching from Z_L (typically 50Ω) to a desirable impedance Z_S at the differential transistor cells (see Fig. 2.3a).

In mathematical terms, we want to develop an Impedance Transforming Balun that transforms from the load impedance Z_L to the source impedance $Z_S = QZ_C$ and resonates out the device parasitic capacitance $Z_C = Z_S/Q$ for arbitrary values of Z_L, Z_S, and Q.

2.2.2 Power Combiners

Always the fundamental problem of any wireless communication system, generating more output power is often achieved by employing Power Combiner structures, since this approach can boost the output power without trading off linearity performance. At mm-wave frequencies, generating power is even harder because the mm-wave range is close to the cut-off frequency of transistors. T-Line parallel combiners are the prevalent choice, but to design series-connected power combiners at mm-wave frequencies remains a major challenge.
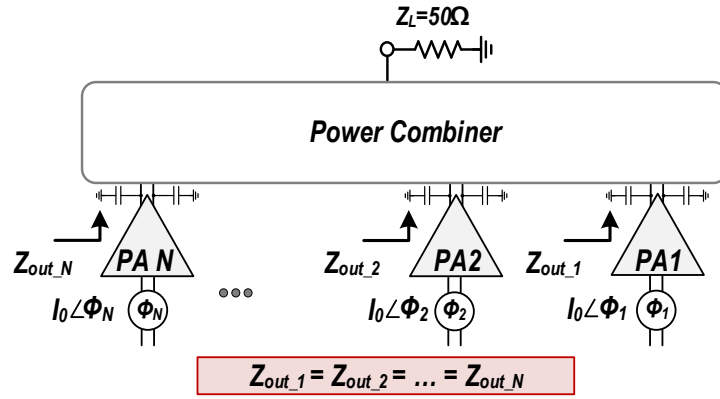
Figure 2.4 Design specifications for mm-wave Power Combiners.

Compared to Impedance Transforming Baluns, Power Combiners also absorb the parasitic capacitance of active devices but must deal with more than one active cores, as shown in Fig. 2.4. For simplicity, we assume that all the active cores are identical in the design of Power Combiners. Given the same active cores, the condition for Power Combiners is that all active devices must see the same conditions. In mathematical terms, we want to design a Power Combiner that works with N active differential cores, transforms from the load impedance Z_L to N source impedances, each of which is $Z_S =$

QZ_C, and resonates out N device parasitic impedances $Z_C = Z_S/Q$. The critical parameters in a power combiner are the loss and impedance transformation ratio Z_L/Z_S and the number of combined cells.

2.2.3 Out-Phasing Circuits
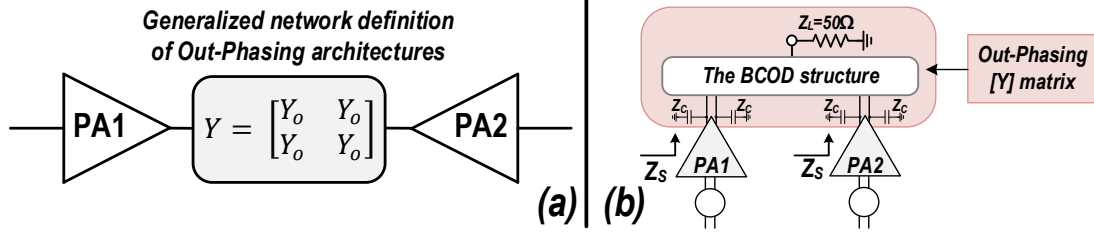
Figure 2.5 (a) Derived microwave network definition of Out-Phasing EM networks (b) Design specifications for mm-wave Out-Phasing circuits.

One of the key solutions for improving the efficiency for transmitting modulated signals, Out-phasing architectures utilize Out-Phasing EM structures together with Chriex compensation to actively modulate the load and boost the efficiency at Power-Back Off (PBO). To a certain extent, an Out-Phasing EM structure without Chirex compensation is a special case of a Power Combiner with an additional constraint of satisfying a [Y] matrix as shown in Fig. 2.5a.

In mathematical terms, we want to design an Out-Phasing EM structure that works on two differential pairs, each having an optimum impedance of Z_S, a device parasitic impedance of $Z_C=Z_S/Q$, and an output impedance of Z_L. The [Y] matrix of the structure when absorbing the parasitic capacitance Z_C must be of the form:

$$[Y] = \begin{bmatrix} jY_0 & jY_0 \\ jY_0 & jY_0 \end{bmatrix}$$

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2.2.4 Doherty Networks

Among all the architectures for transmitting modulated signals, Doherty architectures, which feature wideband modulation with no additional digital-signal-processing overhead, have been a popular and primary choice for RF/Mm-wave circuits when enhanced PBO efficiency is needed. Actively modulating the loads to create an additional efficiency peak at 6dB PBO, Doherty EM networks must also resonate out a parasitic device capacitance Z_C. At 0dB PBO, the circuit transforms an output load Z_L to an optimum load $Z_S = Z_C Q$ seen by both the Main and Auxiliary PAs (see Fig. 2.6a). At 6dB PBO, the circuit transforms the output load to $2Z_S$ seen by the Main PA when the Auxiliary PA is turned off by imposing an open-circuited termination (see Fig. 2.6b).
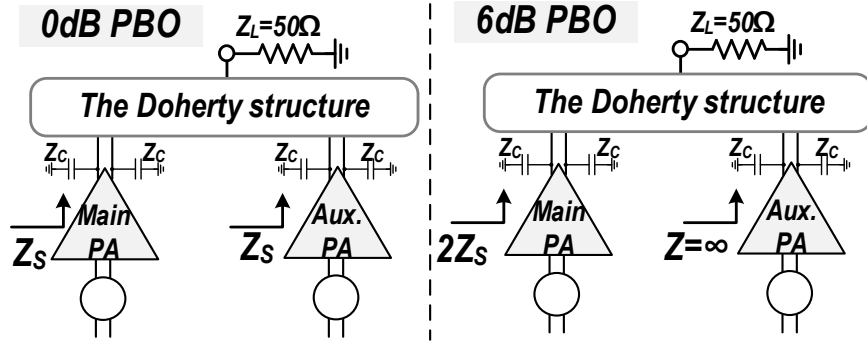
Figure 2.6 Design specifications for Doherty architectures (a) at 0dB PBO and (b) at 6dB PBO.

2.3 The BCOD Designs for Impedance Transforming Baluns

2.3.1 Theoretical Derivations

The proposed BCOD structure can be an excellent candidate to design mm-wave impedance transforming baluns for several major reasons. First, the structure inherently includes lumped capacitors to absorb device parasitic capacitance of mm-wave active

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cores. Second, the short-circuited terminations instantaneously provide low-impedance nodes for DC biasing without any additional overhead (see Fig. 2.3). More importantly, the structure can support a wide range of impedance transformation ratios and phase delays, as will be shown in this section.

Mathematical Equations for Transformation Ratio and Phase Delay

To mathematically solve for the phase-controlled impedance transforming balun parameters, we begin with the derived [Y] matrix of the vanilla coupler-based balun [31]:

$$\begin{bmatrix} I_S \\ I_L \end{bmatrix} = \begin{bmatrix} jY_c - jY_p cot(\theta) & jY_m csc(\theta)/2 \\ jY_m csc(\theta) & -jY_p cot(2\theta) \end{bmatrix} \begin{bmatrix} V_S \\ V_L \end{bmatrix}$$

$$where\ Y_p = \frac{Y_e + Y_o}{2}, Y_m = \frac{Y_o - Y_e}{2}, Y_e = \frac{1}{Z_e}, Y_o = \frac{1}{Z_o},$$

$$Y_c\ is\ the\ admittance\ of\ the\ lumped\ capacitor\ C.$$

From the [Y] matrix of the vanilla baluns, we terminate the source (balanced) ports with a resistance Z_S and a capacitive impedance Z_C to calculate the impedance seen by the load. With the help of Mathematica software, we derive the complex transformation ratio and the phase delay of the vanilla coupler-based balun as follows:

$$Transformation\ Ratio\ = \frac{2i}{2Y_{ps}\ cot(2\theta) - \dfrac{C^2 Y_{ps}^2\ csc^2(\theta)}{-Q + Y_{ps}\ cot(\theta) + i}}$$

$$Phase\ Delay\ = Phase\left(\frac{CY_{ps}\ csc(\theta)}{-2Q + 2Y_{ps}\ cot(\theta) + 2i}\right)$$

$$where\ Y_{ps} = Y_p Z_S\ , C\ = \frac{Z_e - Z_o}{Z_e + Z_o}, Q\ = \frac{Z_S}{Z_C}$$

Designing Impedance Transforming Baluns

From the derived formula, designing an impedance transforming balun with the BCOD structure requires us to solve the equation:

$$Transformation\ Ratio\ = \frac{Z_L}{Z_S} + 0j$$

The design space of the vanilla coupler-based balun includes 3 design parameters Z_e, Z_o, and θ, but the design of impedance transforming baluns involves only 2 equations for real and imaginary values of the transformation ratio, so we have one extra degree of freedom. If the condition of phase control is imposed, we can utilize the extra degree of freedom to control the phase delay:

$$Phase\left(\frac{CY_{pS}\ csc(\theta)}{-2Q + 2Y_{pS}\ cot(\theta) + 2i}\right) = Desirable\ Delay$$

In a broadband design, we can utilize the extra dimension to solve for the transformation ratio with the maximum ripple, or if the design goal is for the lowest loss, we can optimize several coupler parameters and select the one with the lowest loss.

2.3.2   Designing Impedance Transforming Baluns

As the equations to compute transformation ratio and phase delay are nonconvex, we must use numerical solvers to derive the electrical parameters of coupled lines (Z_e, Z_o, θ) that satisfy a real transformation ratio and possibly phase delay. The initial values of electrical parameters of coupled lines are critical to ensure that the optimizer can converge. In this work, we propose to use the following initial values:

$$Y_{pS} = Q \tan(\theta)$$

$$C = \frac{\cos(\theta)}{Q} \sqrt{\frac{2}{Ratio}}$$

When substituting these parameters into the transformation ratio equation, we get:

$$Transformation\ Ratio = \frac{Ratio}{1 - i\,Q\,\tan(\theta)\cot(2\theta)\,Ratio}$$

which is close enough to the desirable ratio, except for the imaginary part of the denominator. From the proposed initialization values, we numerically solve for the theoretical coupled line parameters from the specifications of baluns. Examples of theoretical solutions are presented for various values of Q in section 2.2.3.

2.3.3   Examples of the Proposed Solutions over Various Values of Q

We apply our proposed approach to determine the BCOD structure for various practical scenarios of impedance transformation baluns. Particularly, the baluns often have distinct specifications when employed at the output networks as compared to the inputs networks of high impedance devices such as CMOS or GaN and the input networks of low impedance devices such as SiGe or InP. A desirable output impedance R_{out} of mm-wave PAs is around 15-35Ω to deliver a substantial amount of power, while an input impedance for CMOS is around 150-500Ω and an input impedance for SiGe is much lower at 10-30Ω.

For a given process, one critical constraint is that the ratio $Q = \frac{R}{Z_c} = 2\pi f C R$ remains relatively constant. The reason is that when we increase the size of the device the parasitic capacitance C goes up and the optimum impedance goes down, leading to the product RC

remaining relatively the same. In various practical scenarios of impedance transformation

baluns, the loaded Q at the output stage is about $Q_{out} \sim 1 - 2$ while the loaded Q at the

input stage is about $Q_{in} \sim 3 - 6$ for CMOS and $Q_{in} \sim 0.2 - 0.5$ for SiGe. In this section,

we apply our proposed approach to numerically solve for impedance transforming baluns

with various values of Q.

[Q = 1-2] Output Networks
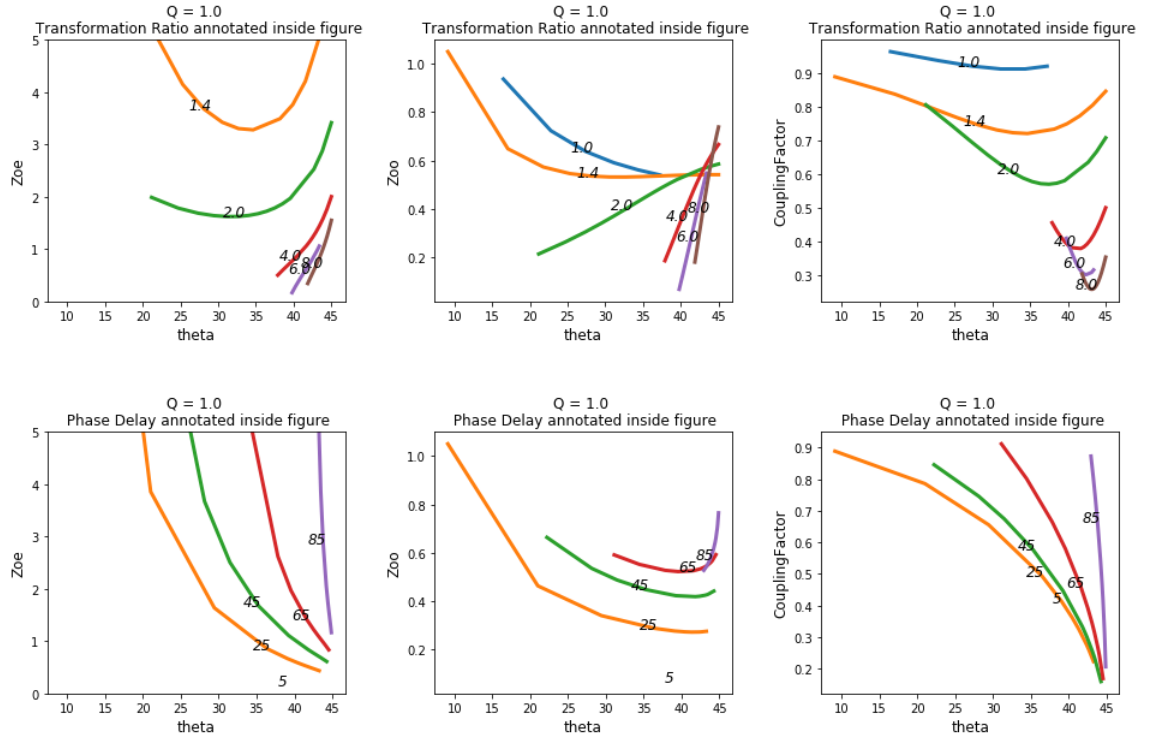
Figure 2.7 Numerical solutions for Phase-Controlled Impedance Transforming Balun with Q=1.

Typically, at the output network of mm-wave circuits, we transform from Z_L=50Ω

impedance to the optimum impedance seen by the PA of Z_S=15-35Ω and we resonate out

a device parasitic capacitance of 60-300fF, resulting in Q values ranging from 1-2 with a

transformation ratio Z_L/Z_S=1.2-3.5. To demonstrate designs of the BCOD structure for

output networks, we representatively solve for two cases of $Q = 1$ and $Q = 1.75$. For example, Fig. 2.7 illustrates our theoretical analysis for the impedance transformation ratio and phase delay of the BCOD structure for Q=1. The structure supports an impedance transformation ratio from 1.4-10.0, where a higher transformation ratio typically requires the electrical length to approach 45°, and delivers a wide range of phase delays from 5°-90°, where a greater electrical length results in a higher phase delay. The BCOD structure also supports a broad range of transformation ratios from 0.6-4.0 and phase delay from 5°-90° for Q=1.75, as shown in Fig. 2.8.
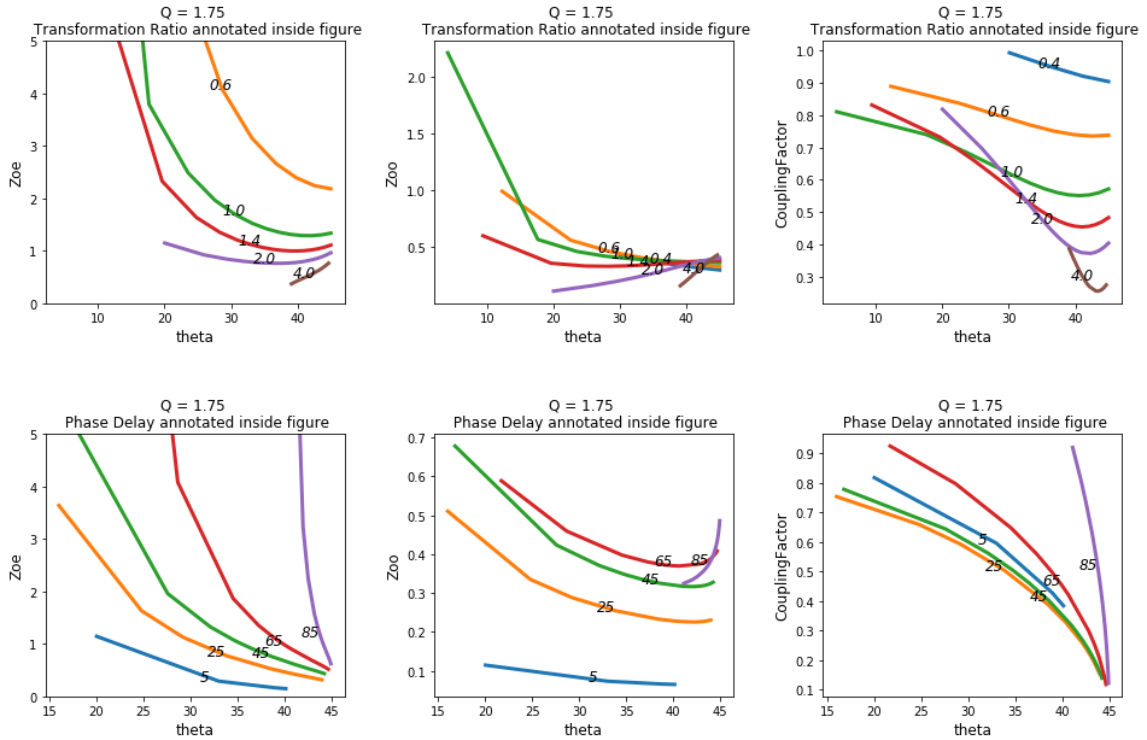
Figure 2.8 Numerical solutions for Phase-Controlled Impedance Transforming Balun with Q=1.75.

[Q = 2.5-6] Typical Values for CMOS Input Networks

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Frequently, at the input network of mm-wave circuits for CMOS processes, we transform from the Z_L=50Ω impedance to the optimum impedance seen by the PA of Z_S=120-350 Ω and we resonate out a device parasitic capacitance of 60-250fF, resulting in Q values ranging from 2.5-6 with a transformation ratio Z_L/Z_S=0.15-0.4. As an illustration, we numerically solve the BCOD equations for $Q = 3$ and $Q = 6$ over various transformation ratios and electrical lengths of coupled lines and depict the results in Fig. 2.9 and Fig. 2.10. From the theoretical solutions, we see that the BCOD structure supports transformation ratios of 0.2-2.0 for Q=3 and transformation ratios of 0.1-1.6 for Q=6, demonstrating that the proposed BCOD structure can support the requirements of transformation ratios Z_L/Z_S=0.15-0.4 of mm-wave CMOS input matching.
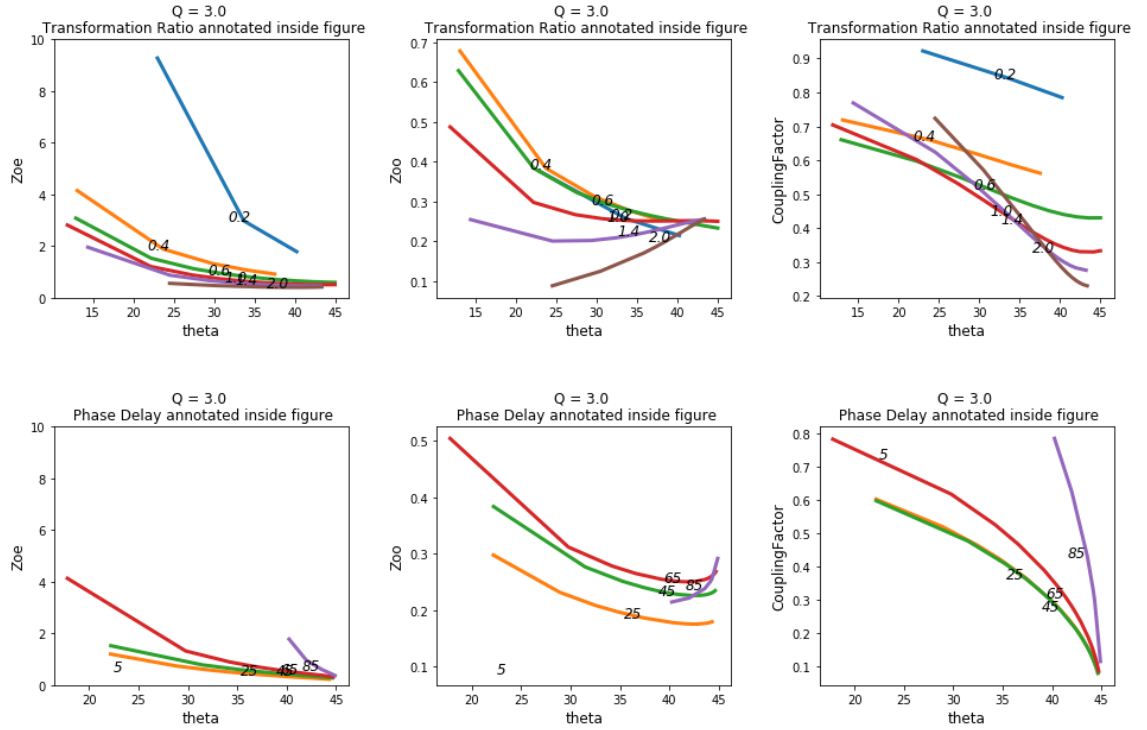
Figure 2.9 Numerical solutions for Phase-Controlled Impedance Transforming Balun with Q=3.
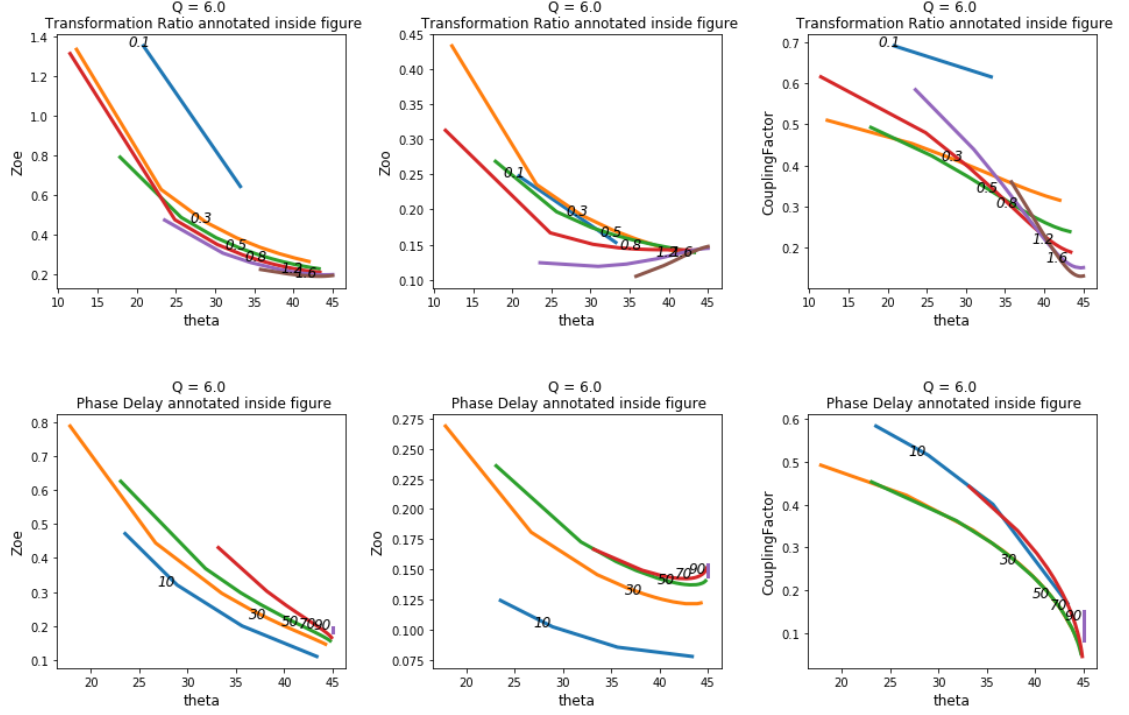
Figure 2.10. Numerical solutions for Phase-Controlled Impedance Transforming Balun with Q=6.

[Q = 0.4-0.8] Typical Values for SiGe Input Networks

At the input network of mm-wave circuits for SiGe processes, we transform from the $Z_L=50\Omega$ impedance to the optimum impedance seen by the PA of $Z_S=10\text{-}25\ \Omega$ and we resonate out a device parasitic capacitance of 60-250fF, resulting in Q values ranging from 0.4-0.8 with a transformation ratio $Z_L/Z_S=2\text{-}5$. To demonstrate the BCOD design for input networks of SiGe processes, we numerically solve for impedance transforming baluns with $Q = 0.5$ and $Q = 0.8$ over various transformation ratios and electrical lengths of coupled lines, as shown in Fig. 2.11 and Fig. 2.12. From the theoretical solutions, we see that the BCOD structure supports transformation ratios of 2.0-8.0 for Q=0.5 and transformation ratios of 1.6-9.0 for Q=0.8, demonstrating that the proposed BCOD structure can cover the requirements of transformation ratio from 2-5 of mm-wave SiGe input networks.

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Figure 2.11 Numerical solutions for Phase-Controlled Impedance Transforming Balun with Q=0.5.

Figure 2.12 Numerical solutions for Phase-Controlled Impedance Transforming Balun with Q=0.8.

2.3.4   Analysis

In this section, we developed a general theory for designing impedance transforming balun with the BCOD structure. Mathematically deriving the transformation ratio and phase delay, we transform from the commonly used electrical parameters of Z_e, Z_o to the new variables of Y_{ps} and C, such that we can greatly simplify the formulas. We proposed initial values for those parameters that significantly improved the convergence to the desirable solutions.

We analyzed the baluns for various values of Q for numerous transformation ratios and illustrate the designs for three common cases: at the output networks, at the input networks of high impedance devices, and at the input networks of low impedance designs. The BCOD structure was shown to have solutions for all those practical scenarios.

2.4   The BCOD Designs for Out-Phasing Circuits

We are aware of no publication that proposes an efficient Out-Phasing network for differential architectures at high mm-wave frequencies. For examples, Out-Phasing structures at lower frequencies often employ a series-connected transformer [14], but the strong capacitive coupling at high mm-wave frequencies distorts the characteristic of this structure [11]. Meanwhile, [18] points out that designing an Out-Phasing network is the major challenge for an Out-Phasing system, and the work proposes a tri-axial network that works only with single-ended architectures. In another attempt, [19] designs an Out-Phasing network for a differential active core, but the network is designed on an antenna, while many systems require the Out-Phasing architectures to deliver power to a 50Ω load rather than directly radiate the output power.

Figure 2.13 (a) High-level architectures of Out-Phasing EM structures (b) Proposed BCOD design for Out-Phasing EM structures.

In this section, with two identical impedance transforming baluns, we propose the BCOD design for Out-Phasing circuits that theoretically supports arbitrary values of Z_L, Z_S, and Q, as shown in Fig. 2.13. Note that we do not depict the Chirex compensation for simplicity. The baluns employed in the proposed Out-Phasing circuits have a phase delay of 90° from inputs to outputs and transform from Z_S to $2Z_L$, in which the factor of two is due to the parallel combination of two PA paths. With the phase-shift of 90°, the baluns invert the impedance [31], leading to a desirable [Y] matrix of Out-Phasing networks. We then apply the analysis we develop in section 2.2 to convert from balun specifications to coupler parameters. Given the design specification of Z_L, Z_S, $Z_C = Z_S/Q$, we drive the unique solution for this Out-Phasing structure as follows:

$$Y_O = QY_S + \sqrt{\frac{1}{2}Y_SY_L} \; ; \; Y_e = QY_S - \sqrt{\frac{1}{2}Y_SY_L}.$$

Following this solution, the proposed BCOD structure can be used to design theoretical Out-Phasing circuits for arbitrary values of Z_L, Z_S, and Q. As an illustration, we show a theoretical BCOD structure for an Out-Phasing network with an electrical specification of $Z_L=50\Omega$, $Z_S=30\Omega$, Q=1. From the design equation, we choose coupled lines with the

electrical parameters of Z_e=66.33Ω, Z_o=19.38 Ω, and θ=45° and illustrate the Out-Phasing

load modulation curves of our proposed structure and compare the results with the idealistic

Out-Phasing response in in Fig. 2.14, where the idealistic Out-Phasing load seen by the

device depending on the Out-Phasing angle ϕ is as follows:

$$R_p = \frac{Z_S}{cos^2(\phi)}$$

Shown in Fig. 2.14, the Out-Phasing load modulation curves of the design overlap with

the idealistic response, proving the effectiveness of the proposed designs.
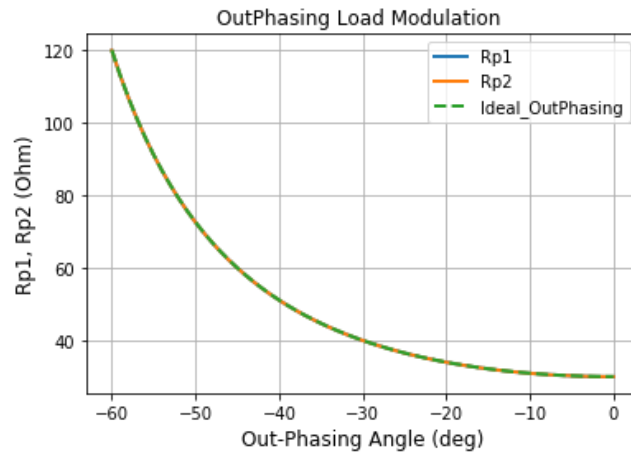
Figure 2.14 Out-phasing load modulation of the proposed Out-Phasing theoretical structure.

2.5   The BCOD Designs for Doherty Networks

In this section, we show theoretically that the proposed BCOD structure has solutions

for the Doherty networks for an arbitrary value of Z_L, Z_S, and Q. Described in Fig. 2.15,

we can apply the design of two impedance transforming baluns to construct an EM

structure for a Doherty network as in [31]. The Main PA requires a balun that transforms

from $2Z_L$ to Z_S with a phase delay of 90°, and the Auxiliary PA necessitates a balun that transforms from $2Z_L$ to Z_S with a phase delay of 0°/180°. We then apply the theoretical analysis in section 2.2 to solve for the coupled line parameters, and to ease the design of the Auxiliary balun, we add a quarter-wavelength T-line to transform from Z_L to Z_S. From that, giving an output load Z_L, device parasitic Z_C, and optimum impedance $Z_S=Z_CQ$, we drive a closed-form BCOD solution for the proposed Doherty output network shown as follows:

$$Y_{o1} = \left(Q + \sqrt{\frac{1}{2}} \right) Y_S, Y_{e1} = \left(Q - \sqrt{\frac{1}{2}} \right) Y_S,$$

$$Y_{o2} = 5QY_S, Y_{e2} = \frac{Q}{2} Y_S;$$

$$and\ Y_T = \sqrt{Y_S Y_L}$$
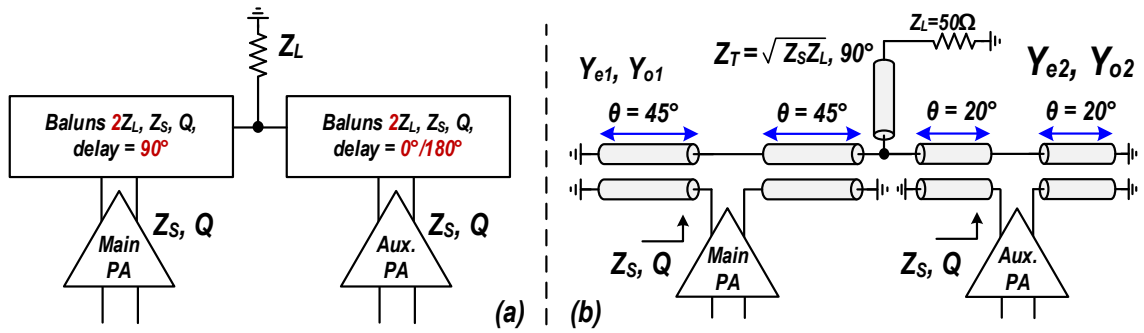
Figure 2.15 (a) High-level architectures of Doherty EM structures (b) One of the closed-form solutions for mm-wave Doherty output networks.

As an illustration, we show a theoretical BCOD structure for an Out-Phasing network with an electrical specification of $Z_L=50\Omega$, $Z_S=30\Omega$, $Q=1$. Following the design equation,

we choose coupled lines with the electrical parameters of Z_{e1}=102.4Ω, Z_o=17.57Ω, and θ_1=45° for the Main balun, Z_{e2}=60Ω, Z_o=6Ω, and θ_1=20° for the Auxiliary balun, and a quarter-wavelength with a characteristic impedance Z_T=38.73Ω. With those parameters, we build the theoretical BCOD circuit for Doherty networks, demonstrate the active load modulation results, and compare those with the idealistic Doherty response in Fig. 2.16. The load modulation of the BCOD structure tracks closely to the ideal Doherty behaviors, which verifies our proposed formulas and proves that the BCOD structure acts as Doherty EM networks.
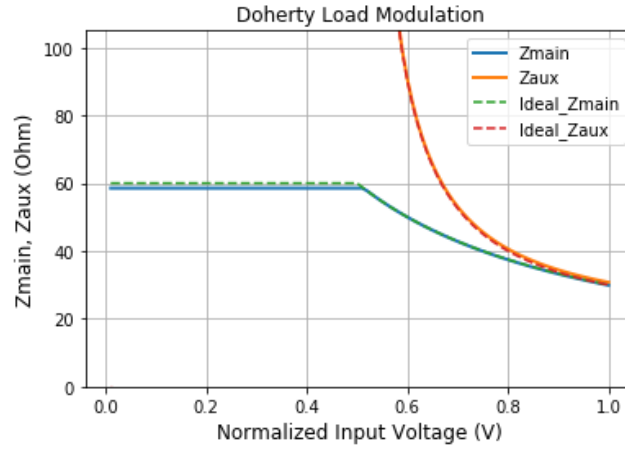
Figure 2.16 Doherty load modulation results of the proposed theoretical BCOD structure.

2.6 The BCOD Solutions for Power Combiners

The proposed BCOD structure can also be an excellent candidate for Power Combiners, as depicted with parallel-connected and series-connected structures in Fig. 2.17. On one hand, the parallel-connected Power Combiners are relatively easier to implement; we can simply design an impedance Transforming balun with an electrical specification of NZ_L, Z_S, Q and parallelly connect N identical baluns together at the single-ended node, as shown

in Fig. 2.17a. On the other hand, the series-connected Power Combiners are relatively more challenging to design; we must employ coupled lines with different characteristic impedances with phase shifted inputs and utilize numerical method to solve for the design parameters.
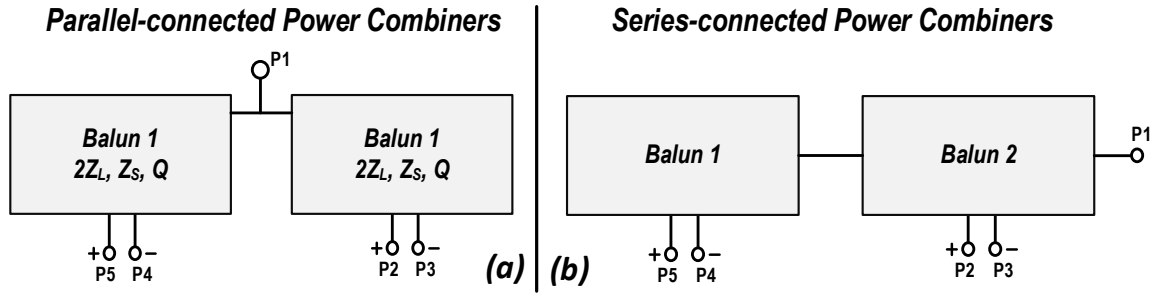
Figure 2.17 Power Combiners for two active differential cores with the proposed BCOD structure (a) Parallel-connected structures (b) Series-connected structures.
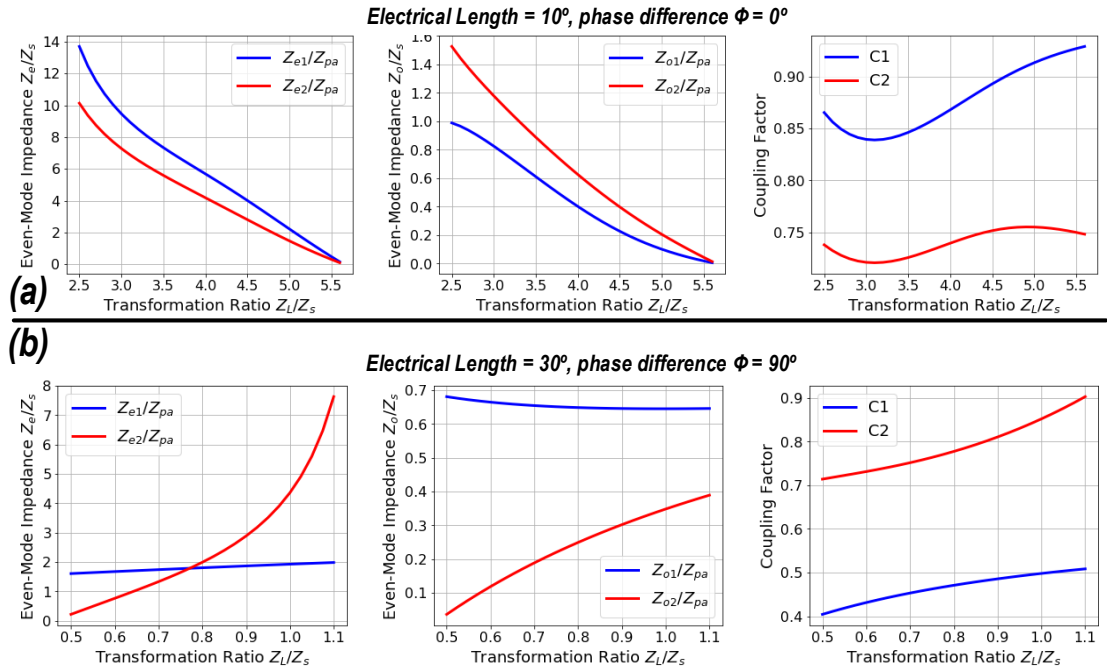
Figure 2.18 Numerical solutions for series-connected Power Combiners with series-connected coupler-based structure.

As an example, we numerically solve the series-connected coupler for $Q=Z_S/Z_C=1.25$, a typical value for the output network of a silicon process at high mm-wave frequencies. Described in Fig. 2.18a, when the electrical length of both baluns equals 10° and the phase difference between two active cores is 0°, the BCOD structure supports a wide range of transformation ratios Z_L/Z_S from 2.5-5.5. Shown in Fig. 2.18b, when the electrical length equals 30° and the phase difference equals 90º, the BCOD structure supports impedance transformation ratios from 0.5-1.1. Overall, we show that the design space for the BCOD structure is broad enough to support the designs of series-connected Power Combiners with various transformation ratios.

2.7   Conclusion

In this chapter, we present the theoretical aspects of the proposed BCOD structure. We first define the common electrical specification for all BCOD design tasks. Moreover, based on the coupled line theory, we mathematically derive the BCOD equations and propose a numerical approach to convert from electrical baluns to the parameters of coupled lines. We show that the BCOD equations have theoretical solutions for various Impedance Transforming Baluns at the output networks and the input networks of high and low impedance devices. We further advance the concept and apply our results for impedance transforming baluns with control of phase delays to produce theoretical solutions for both Out-Phasing and Doherty networks, where we demonstrate that the BCOD structure can theoretically design Out-Phasing and Doherty circuits with arbitrary electrical specifications. The BCOD structure can also support the design of series-connected Power Combiners, where we have illustrated various design curves.

Overall, we show that the BCOD structure has a broad design space that contains solutions for many emerging mm-wave challenges. The next step is to develop a framework that can fully automate the EM design of the BCOD structure when given a mm-wave task and an electrical specification.

CHAPTER 3. DEVELOPING PHYSICAL-ELECTRICAL MACHINE LEARNING MODELS

To develop automation algorithms for mm-wave EM structures, we must first build several Machine Learning models that can predict the electrical properties of mm-wave circuits from physical dimensions. Conventionally, engineers solve this physical-electrical conversion by utilizing commercial EM simulators, such as the High Frequency Structure Simulator (HFSS) [38], which might require a slow computational time of minutes-hours to complete a full-wave simulation. In this chapter, we present an approach to compute the physical-electrical relationship with Machine Learning techniques, which in our approach includes sampling a continuous design space to collecting data, extracting electrical labels from S-parameter files, and training a neural network to predict electrical properties. Note that because the ground truth as the outputs of Machine Learning models are often referred as labels, we define electrical labels as an equivalent term for the "ground-truth" electrical properties of EM structures. Verifying with the K-fold validation technique, we show that our ML models can equivalently determine electrical properties from physical parameters as accurately as commercial EM solvers but our models drastically reduce computational time from minutes-hours to a fraction of seconds.

With the complete knowledge about the entire design space of the EM structures, our pre-trained ML models can help automate various critical mm-wave EM blocks as will be presented in Chapters 4-5. The models can also serve as a new tool for mm-wave designers to answer many challenging and abstract questions as will be shown in Chapter 6.

3.1 Motivations for Developing Physical-Electrical Machine Learning Models

3.1.1 Drawbacks of Current EM-Design Techniques
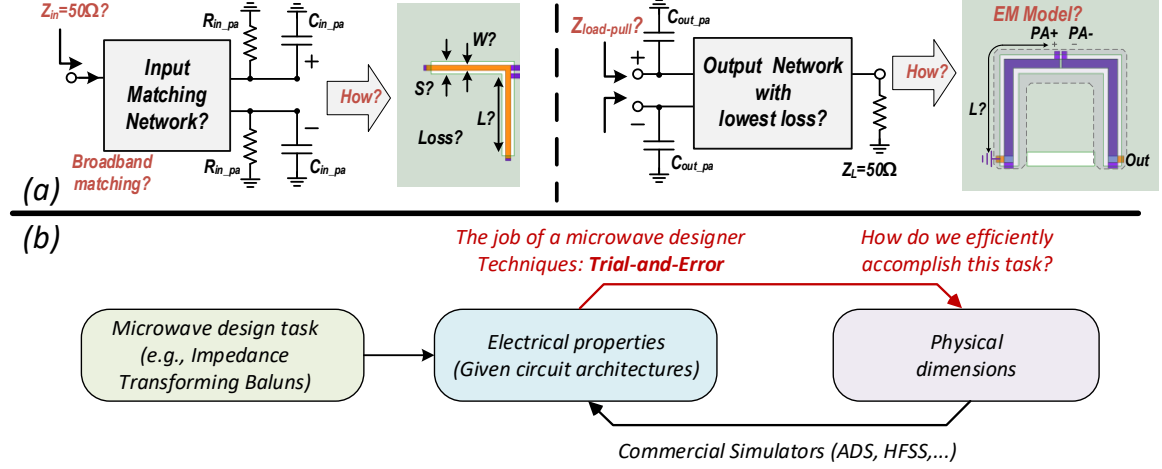
Figure 3.1 (a) The task of designing Impedance Transformation Baluns (b) A typical design flow.

The current approach to design EM circuits heavily relies on trial-and-error. To physically realize an EM structure, engineers must repeatedly run EM simulators to calculate electrical properties and keep updating physical parameters until all electrical specifications are met. As an illustration, Fig.5.1a details the task of designing impedance transforming baluns. The specification is to design an input/output balun that resonates out the parasitic capacitance Z_c and matches from a load impedance of Z_L to a source impedance of Z_S. The goal is to design a full EM structure with proper physical dimensions (see Fig. 3.1.a) that performs the balun operation and desirable impedance transformations. Figure 3.1b illustrates a typical design flow. The first step is to decide a circuit architecture for the design task, which the BCOD structure we proposed can be an excellent candidate. The second step to realize the physical dimensions is heavily based on trial-and-error. First, engineers make an educated guess with a high level of randomness to initialize the first-try

physical dimensions. Many times, engineers tend to stay at a local optimum solution due to a poor initialization. Then, they use commercial EM simulators, such as the High Frequency Structure Simulator (HFSS) [38], to predict the electrical properties. Based on the differences between the predicted outputs and actual specifications, engineers decide how to update physical parameters, which also involves a high level of uncertainty, and then keep running the EM simulators to tune various physical dimensions. Depending on the experience of designers and sometimes impromptu decisions, the design time can vary from days to weeks or even months, and the design quality can drastically change over various design attempts.

The current design approach is time-consuming and labor-intensive because EM simulators are normally slow to run and the number of EM iteration steps are typically large. This approach to design EM structures involves a high variance in the design quality because the approach heavily depends on the first random initialization and the experience and impromptu decisions of circuit designers when updating physical dimensions. Given the same electrical specifications, even the same circuit designers might generate different EM structures with varying design quality when attempting to design the tasks several times.

3.1.2 Why We Need Machine Learning

We must be able to compute electrical properties from physical dimensions to properly design an EM structure. For example, in the task of designing coupled lines, we must calculate the even-/odd-mode impedances, electrical length, and losses when given the physical dimensions of coupled lines. In the design of baluns or combiners, we need to

calculate the resistive and reactive impedances Z_S and Z_C seen by device given the load impedance Z_L and all EM physical parameters.

Figure 3.2 describes various approaches to compute the physical-electrical relationship. In one approach, we look for closed-form mathematical equations that explicitly yield electrical parameters as functions of all physical dimensions. If such mathematical equations exist, we can accurately calculate the electrical properties over the entire design space of physical parameters and from that efficiently optimize the physical dimensions for the design task. However, mathematically deriving the closed-form equations is extremely challenging. The mapping from even-/odd-mode impedances and electrical length to the width and the length of the EM traces can be relatively monotonic, but the mapping between loss and EM dimensions is much more complicated to compute. As the EM structures grow more complex, solving such structures must demand approximate and computational techniques.
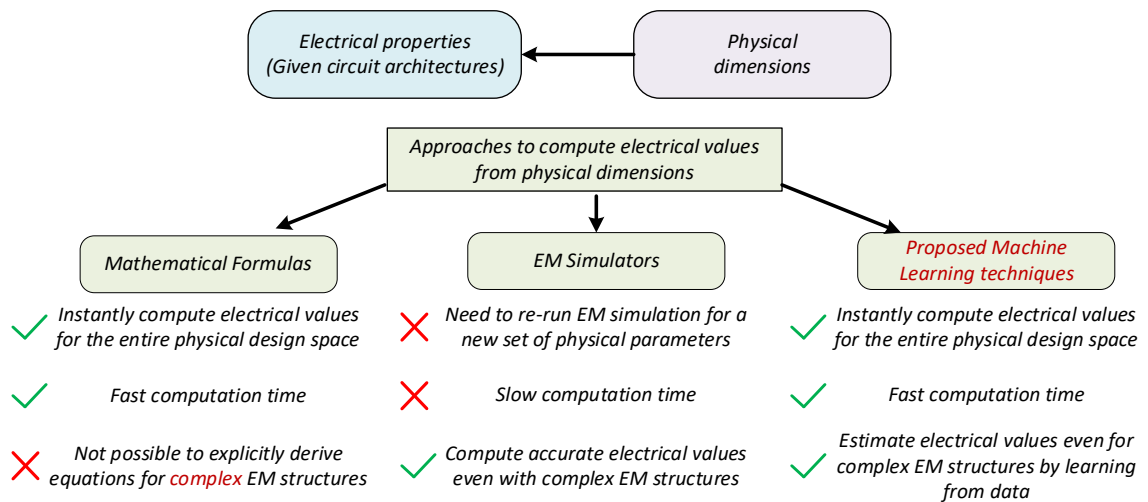
Figure 3.2 Comparison among various techniques to calculate electrical properties from physical dimensions.

In another approach, engineers commonly utilize commercial EM simulators to compute electrical parameters from physical dimensions. Although the EM solver can accurately predict the electrical performance, the solver can only reveal the physical-electrical conversion for specific physical parameters. We need to re-run the full-wave simulator again to evaluate the circuit performance when physical dimensions changes. The computation time is often slow, the update of physical dimension is manual over a large number of iteration steps, and as a result, we confront the drawbacks of time-consuming, labor-intensive approaches with a high variance in quality when designing EM structures, as discussed in section 3.1.1.

Adding Machine Learning techniques to the existing EM methods can resolve these challenges. If we can develop ML models that accurately learn the physical-electrical relationships over the entire design space of physical dimensions, then the resulting ML models are equivalent to the closed-form mathematical equations that derive electrical properties from physical parameters, since both have the same inputs and similar outputs. Practically, we can train those ML models by continuously sampling data from the entire design space of physical parameters and applying various ML models to learn the input-output relationships. The trained ML models allow us to effectively navigate over the entire design space, accurately predict the electrical properties, and efficiently run numerous iteration steps to optimize EM designs.

3.1.3   *Applications of Machine Learning Models*

We can apply the ML models to automate various Mm-wave design tasks. The theoretical analysis in chapter 2 shows that the design space of the BCOD structure is broad

enough to contain solutions for many challenging mm-wave tasks. By collecting EM simulated results for coupled lines and vanilla baluns and by learning from data, we can develop an ML model that fully learns the entire design space of those structures. Together with automation architectures with multiple initializations and gradient descent, the ML models can allow us to automate EM design tasks and reduce design time from weeks-months to seconds, as will be presented in Chapters 4-5. Additionally, the ML models can also reveal the bigger pictures about the design problems we are dealing with and can advance our understanding of the topic to the next level, as will be discussed in Chapter 6.

3.2   The Physical Design Space of the BCOD Structure

Machine Learning models build from data, and the BCOD structures we use to design critical mm-wave blocks such as Baluns, Combiners, Out-Phasing, and Doherty circuits build from coupled lines. To begin the developments of Machine Learning models for the BCOD, we first define the on-chip structures of coupled lines in this section, before we present the design space of physical dimensions and demonstrate our method to collect data to train physical-electrical ML models for both coupled lines and vanilla baluns in the next sections.

3.2.1   On-Chip Implementation

Without a loss of generalization, we automate the BCOD structure with an assumption of on-chip implementation. On-chip metal stacks typically share a common 250µm silicon substrate but differ in (t_m) metal and (t_d) dielectric thicknesses, as illustrated in Fig. 3.3a. On one hand, due to the strong skin effect at mm-wave, a metal thickness t_m greater than 1.5 µm tends to have less effect on the loss performance, thus we set t_m=3µm as the metal

thickness in this work to follow the metal stack of the GlobalFoundries 45nm CMOS SOI process. On the other hand, the dielectric thickness (t_d) can strongly affect the coupled-line parameters, such as length, width, or spacing. On silicon processes with multiple metal layers, we can "discretely" vary the dielectric thickness by moving the signal traces from one metal layer to another, thus representing the option of changing metal layers by including dielectric thickness as one of the design parameters.
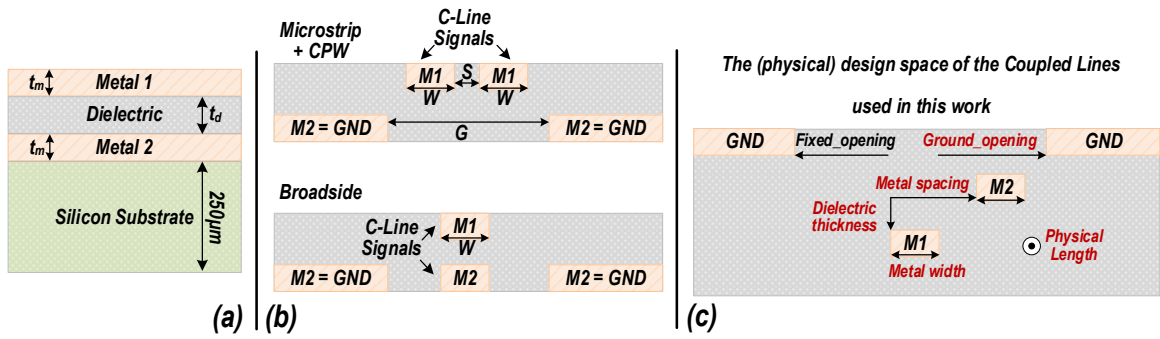
Figure 3.3 (a) A generalized Silicon process (b) Microstrip, CPW, and broadside coupled lines technologies (c) Physical design space of coupled lines structures used in this work. Design dimensions include physical length, metal width, metal spacing, ground opening, and dielectric thickness.

To physically implement coupled lines on chips, engineers commonly employ the microstrip, broadside, and co-planar waveguide (CPW) structures, as shown in Fig. 3.3b. Two electrical signals can remain parallel as in microstrip designs or stack vertically as in broadside configurations. The ground plane near the signal areas can also be opened to control the even-mode impedance as in the CPW implementations. In this work, we combine the characteristics of microstrip, broadside, and CPW to a common implementation of coupled lines as in Fig. 3.3c. The design parameters for the implementation includes the physical length of coupled lines, the metal width of both

coupled-line signals, the metal spacing of two traces, and the ground opening at the ground layer, as shown in Fig. 3.3c.

3.2.2 Examples of Physically Implemented BCOD Structures

From the physical implementation presented in Fig 3.3c, we can construct various EM structures for the BCOD with examples as shown in Fig. 3.4. A design example of Impedance Transforming Baluns that includes two identical coupled lines that transfer power between a differential core and an output load is illustrated in Fig. 3.4a. An example for Power Combiners consists of two impedance transforming baluns connected in series as shown in Fig. 3.4b, while examples of Out-Phasing circuits and Doherty networks are depicted in Fig. 3.4c and 3.4d, respectively.
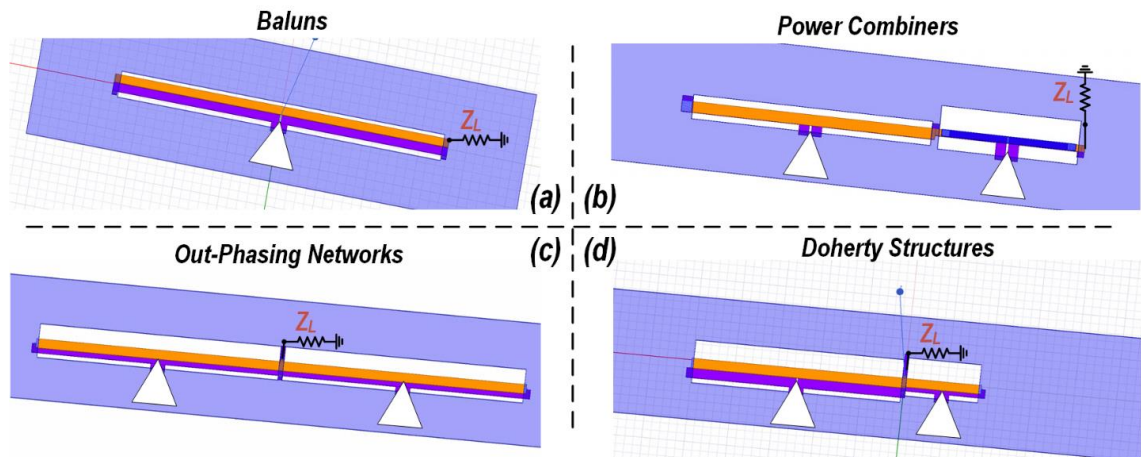
Figure 3.4 Examples of EM implementations for (a) Baluns, (b) Combiners, (c) Out-Phasing networks, and (d) Doherty circuits.

3.3 The Physical-Electrical Machine Learning Model for Coupled Lines

After defining the physical design space for the coupled lines, we then develop various physical-electrical ML models, where in this section, we first build a ML model for coupled lines.

3.3.1 Data Collection

ML models build from data, where the data in this physical-electrical ML model for coupled line comes from the EM simulated results of coupled structures. Because the data we collect must represent the true distribution of the physical design space, we must continuously and randomly sample various sets of physical dimensions of coupled lines, where the parameters for random sampling include the dielectric thickness, physical length, metal width, spacing, and ground opening. Next, we build the HFSS model for coupled lines to simulate the S-parameters of each set of randomly sampled physical dimensions. Fig. 3.5a demonstrates several examples of HFSS models of randomly generated coupled lines with different physical dimensions, and Fig. 3.5b shows the sampling range of physical parameters for each model. In total, we sample 3350 HFSS designs of coupled lines to train the ML models. The dielectric thickness ranges from $0.1\mu m - 7.9\mu m$, the physical length ranges from $40\mu m - 799\mu m$, the spacing ranges from $-14\mu m - 60\mu m$, the ground gap ranges from $5\mu m - 80\mu m$, and the width ranges from $2\mu m - 50\mu m$, as shown in Fig.3.5b.
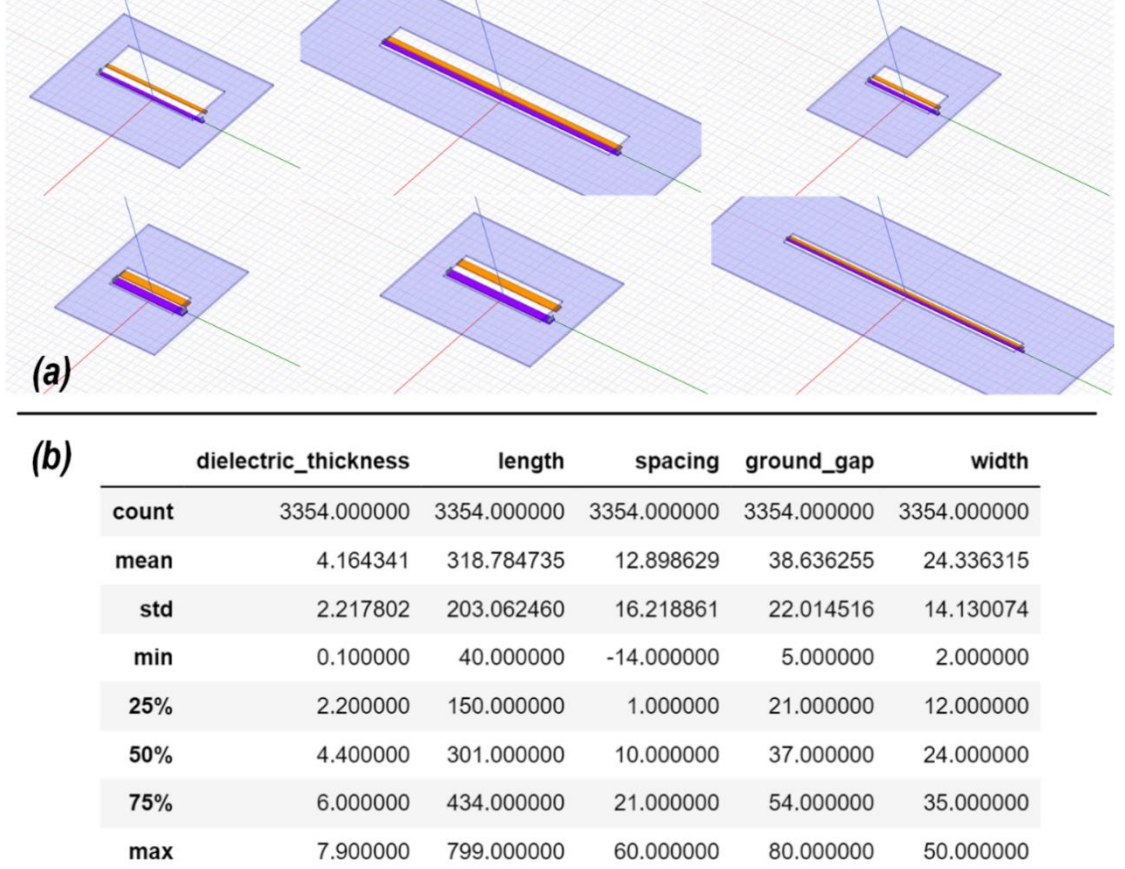
Figure 3.5 (a) Examples of randomly generated coupled-line structures (b) Statistical analysis of all the collected data for various design parameters.

3.3.2 *Extracting Electrical Labels from S-Parameter Files*

Because the ground truth as the outputs of Machine Learning models are often referred as labels, we define electrical labels as an equivalent term for the "ground-truth" electrical properties of EM structures. From the simulated S-parameters of EM structure, we develop an extraction pipeline to mathematically compute the electrical labels, and we will employ those labels to train the physical-electrical ML models.

Mathematical Analysis

We first solve several subproblems to prepare for the extraction process.

Sub-problem 1: Given a [Z] matrix for a transmission line, calculate the characteristic impedance Zo and electrical length theta

The Z matrix for a 2-port transmission line is as follows:

$$\mathbf{Z} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{12} & Z_{22} \end{pmatrix} = \begin{pmatrix} -iZ_o/tan(\theta) & -iZ_o/sin(\theta) \\ -iZ_o/sin(\theta) & -iZ_o/tan(\theta) \end{pmatrix}$$

Given Z_{11} and Z_{12}, we derive the characteristic impedance and electrical length as follows:

$$Z_o = -i\sqrt{-Z_{11}^2 + Z_{12}^2}$$

$$\theta = arctan(Z_{11}/Z_{12})$$

Sub-Problem 2: Given a [Y/Z] matrix for a two-port network, compute the conjugate matching (resistive and capacitive) input impedance, loss, and phase delay of the network (see Fig. 3.6).
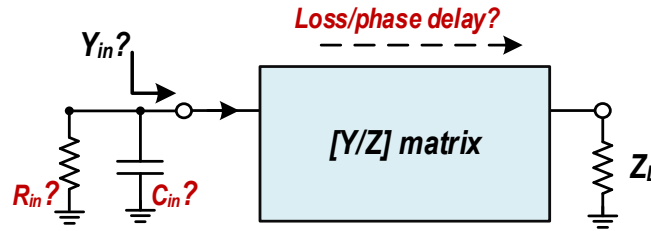
Figure 3.6 The sub-problem of calculating conjugate matching impedance, passive efficiency, and phase delay.

First, we calculate the resistive and capacitive input impedance when given the [Y/Z] matrix of network and output impedance Z_L. The input admittance can be computed from either the [Z] or [Y] matrix as follows:

$$Y_{in} = -\frac{-Z_{22} - Z_L}{-Z_{12}^2 + Z_{11}Z_{22} + Z_{11}Z_L}$$

$$Y_{in} = -\frac{-Y_{11} + Y_{12}^2 Z_L - Y_{11}Y_{22}Z_L}{1 + Y_{22}Z_L}$$

From the above equations, we derive the resistive and capacitive impedance as follows:

$$R_{in} = 1/real(Y_{in})$$

$$C_{in} = imag(Y_{in})/2\pi f$$

Second, we compute the passive efficiency and phase delay of the network by exciting 1V at the inputs. The power deliver to the network is:

$$P_{in} = V_{in}^2/R_{in} = 1/R_{in}$$

The output voltage at the output can be calculated from either the [Y] or [Z] matrix is:

$$V_{out} = \frac{Z_{12}Z_L}{-Z_{12}^2 + Z_{11}Z_{22} + Z_{11}Z_L}$$

$$V_{out} = -\frac{-Y_{12}Z_L}{1 + Y_{22}Z_L}$$

The passive efficiency (loss) and phase delay from input to output are as follows:

$$loss = P_{out}/P_{in} = V_{out}^2 R_{in}/Z_L$$

$$phase\ delay = phase(V_{out})$$

Extract Coupled Line Parameters

The critical electrical parameters that characterize a coupled line are the characteristic impedances, electrical length, and propagation loss of both even and odd modes. Given the simulated [Z] matrix of the 4-port coupled lines, we first excite the circuit in either even or odd mode and convert the 4-port network to 2-port sub-circuits (see Fig. 3.7).

The equations to extract the *even mode* [Z] matrix are as follows:

$$Z_{11\_even} = (Z_{11} + Z_{13} + Z_{33} + Z_{31})/2$$

$$Z_{12\_even} = (Z_{12} + Z_{14} + Z_{34} + Z_{32})/2$$

$$Z_{22\_even} = (Z_{22} + Z_{24} + Z_{44} + Z_{42})/2$$

The equations to extract the *odd mode* [Z] matrix are as follows:

$$Z_{11\_odd} = (Z_{11} - Z_{13} + Z_{33} - Z_{31})/2$$

$$Z_{12\_odd} = (Z_{12} - Z_{14} + Z_{34} - Z_{32})/2$$

$$Z_{22\_odd} = (Z_{22} - Z_{24} + Z_{44} - Z_{42})/2$$

Next, we apply the mathematical derivation in the subproblem 1 to calculate the characteristic impedance and electrical length of both even-/odd-modes. Terminating the even-/odd-lines with the even-/odd-mode characteristic impedance, we employ the formulas derived from the subproblem 2 to compute the propagation loss of both even-/odd-modes. We depict the derived electrical length and propagation loss over frequencies and compare to the simulation results from the Advanced Design Systems (ADS) simulator

[39] as shown in Fig. 3.7. The overlapping of the extracted and simulated curves demonstrates the accuracy of the proposed extraction process.
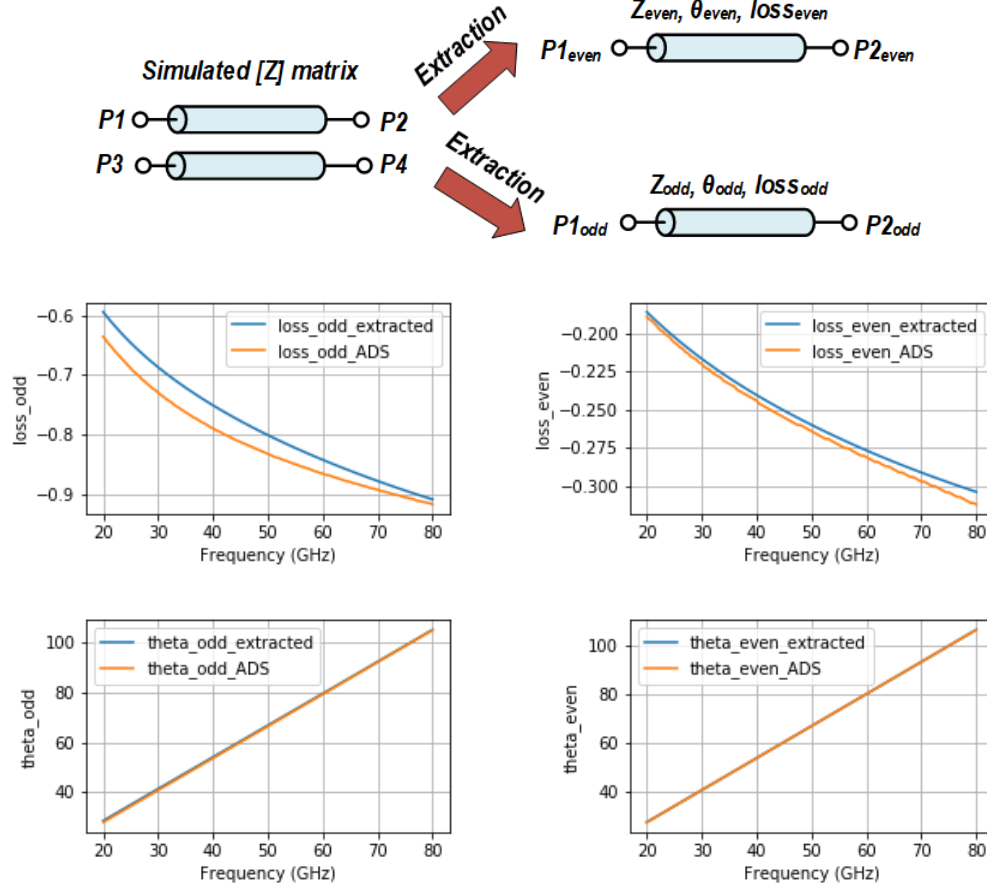
Figure 3.7 The extraction of electrical labels of coupled lines and comparison between mathematically extracted and ADS simulated results.

3.3.3 Training Neural Networks

From the physical dimensions defined in section 3.2 and the electrical labels extracted in section 3.3.2, we build a database that consists of physical dimensions and electrical labels for coupled lines. The database spans the entire design space of physical dimensions of proposed EM structures. We seek to develop an ML model that can generalize all data

points in our database or generalize the entire design space of the physical parameters. As discussed in section 3.1.2, building such an ML model is equivalent to explicitly deriving closed-form mathematical formulas that map from physical dimensions to electrical properties.

The Machine Learning community has developed several major techniques to generalize a model from data, such as Neural Networks, Support Vector Machines, or Tree-Based techniques. Among those, we choose the Neural Network techniques (see Fig. 3.8), because with this approach, we can compute gradients of outputs with respect to inputs, which subsequently we can apply gradient descent to optimize input values.
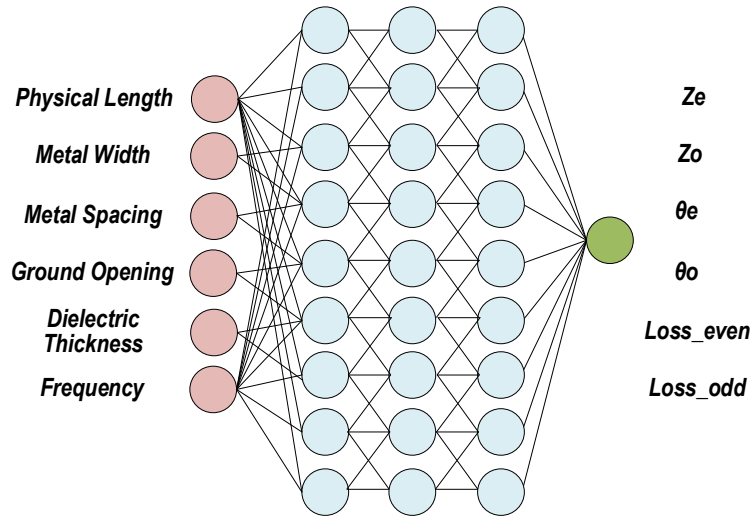
Figure 3.8 Neural Networks for the physical-electrical ML models for coupled lines.

Applying to the task of developing physical-electrical ML models for coupled lines, we design neural networks with 3 hidden layers, each of which has 64 neurons. The input dimension of the coupled-line ML model equals 6, which represents the dielectric thickness, physical length, signal width, signal spacing, ground gap, and frequency. The

outputs have a dimension of 1 that indicates the electrical label we want to predict. We build separate coupled-line ML models to learn the characteristic impedances, electrical length, and most importantly, propagation loss values of both the even and odd modes. From the physical-electrical database, we train our neural networks with a batch size of 128, a learning rate of 0.001, and the loss of mean absolute error. We use Keras [40] to build our ML models and employ Adam optimizers [41] to update the learnable weights of the models over 10 epochs.

3.3.4   *Evaluating Machine Learning Models*

We use the K-fold validation technique (see Fig. 3.9a) to evaluate the generalization score of ML models. We split the data into 5 random portions, take 4 portions as training sets and the remaining as testing sets, and report mean absolute loss over various training and evaluating data in Fig. 3.9b. The models can predict the electrical length of both the even and odd modes with an average error of 1-2° and predict the loss with an average error of less than -0.02dB for even-mode loss and -0.035dB for odd-mode loss. The models also can learn the even-mode impedance with an error of less than 5Ω (for an average even-mode impedance of 70Ω), and odd-mode impedance with an error of less than 0.7Ω (for an average odd-mode impedance of 15Ω). Depicted in the second row of Fig. 3.9b, the mean values of relative percentage errors are all less than 10% for all electrical labels, indicating that the ML models accurately predict the electrical values within the range of 0.9-1.1 times the actual values. Overall, the K-fold scores are similar for both training and evaluating sets, and the error values are small, demonstrating that the ML models for the coupled lines well match the physical-electrical relationships.
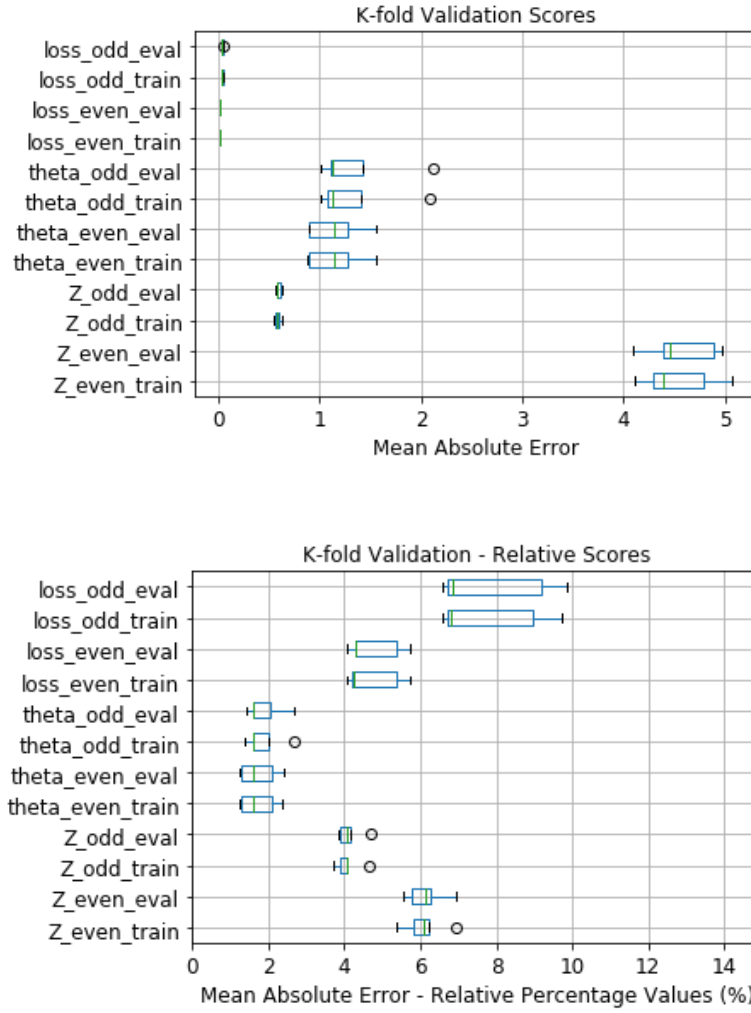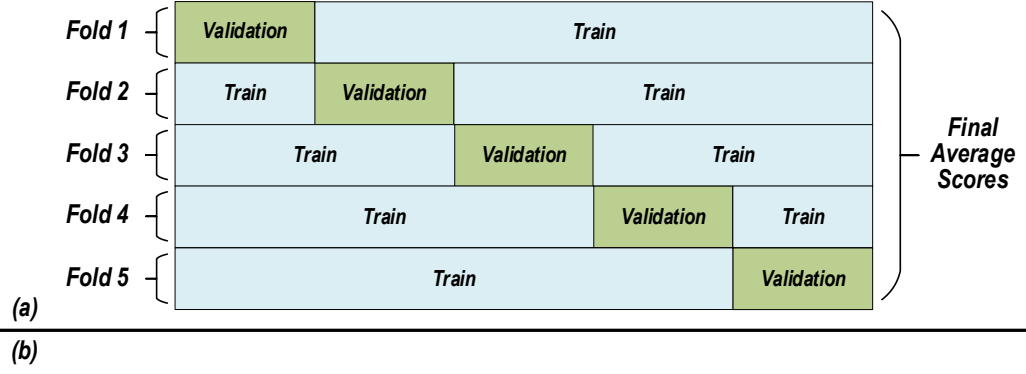
Figure 3.9 (a) K-fold validation concepts (b) K-fold scores for the physical-electrical ML models for coupled lines with mean absolute errors in the first row and mean relative errors in the second row. The relative errors of less than 10% indicate that the ML models accurately predict electrical properties within the range of 0.9-1.1 times the ground-truth values.

3.4 The Physical-Electrical Machine Learning Model for Vanilla Baluns

In this section, we develop the physical-electrical Machine Learning models for vanilla baluns, which is the fundamental building block for our proposed BCOD structure. Section 3.4.1 describes the data collection process, section 3.4.2 shows the extraction of electrical parameters, section 3.4.1 illustrates the training of neural networks, and section 3.4.2 demonstrates the K-fold validation results.

3.4.1 Data Collection

	dielectric_thickness	length	spacing	ground_gap	width
count	2089.000000	2089.000000	2089.000000	2089.000000	2089.000000
mean	4.090378	195.570129	7.323121	34.650072	25.216850
std	2.248000	100.275215	16.367998	20.664989	14.090919
min	0.100000	30.000000	-14.000000	1.000000	2.000000
25%	2.200000	104.000000	-5.000000	18.000000	12.000000
50%	4.100000	182.000000	4.000000	33.000000	25.000000
75%	6.000000	273.000000	18.000000	46.000000	37.000000
max	7.900000	783.000000	60.000000	80.000000	50.000000

Figure 3.10 (a) Examples of HFSS models of randomly generated vanilla-balun structures (b) Statistical analysis of the sampled data.

We connect two identical coupled lines together to construct vanilla baluns. To build a physical-electrical ML model for baluns, we also sample from a continuous design space of physical dimensions, simulate balun structures with EM solvers, and record simulated S-parameters files for further extraction. Fig. 5.6a shows examples of HFSS models of randomly generated vanilla baluns, and Fig. 5.6b illustrates the statistical analysis of the data collection, where the range of the physical dimensions we collect for the vanilla baluns are the same as those of coupled lines. In total, we sample 2089 different designs of vanilla baluns to train our ML models.

3.4.2   Extracting Electrical Labels from S-Parameter Files

Given the physical dimensions of vanilla baluns, we want to build the physical-electrical ML models for baluns that can predict the source impedance Z_S (or R_{in}), the capacitive (C_{in}) impedance seen by the device, the loss of baluns, and the phase delay between inputs and outputs. To prepare the data for those ML models, in this sub-section, we extract the electrical labels by applying the mathematical analysis from section 3.3.2 to the simulated S-parameters files of HFSS models for baluns.

As the balun is a 3-port network, we first differentially excite the balun to transform the 3-port network to a 2-port structure:

$$Y_{11\_diff} = (Y_{11} - Y_{12})/2$$

$$Y_{12\_diff} = Y_{13}$$

$$Y_{22\_diff} = Y_{33}$$

We subsequently follow the results of sub-problem 2 in section 3.3.2 to calculate the input impedance, loss, and phase delay of the networks. Fig. 3.11 compares the extracted results to the simulated data from ADS, both of which are similar, indicating the accuracy of the proposed extraction process.
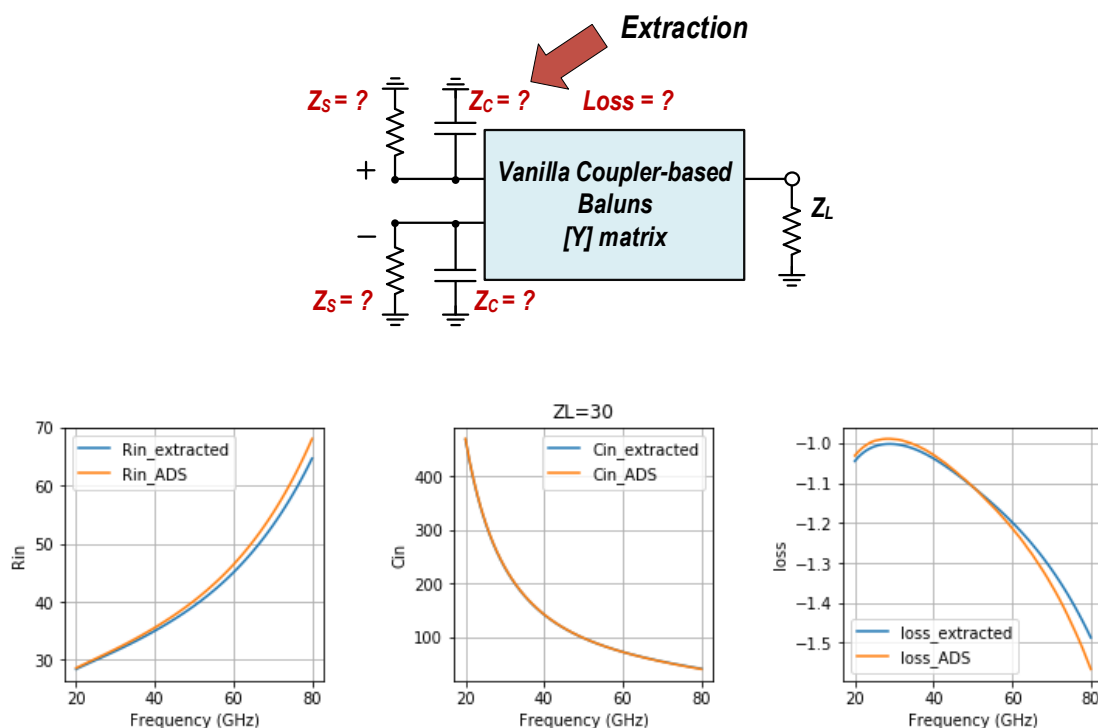
Figure 3.11 Extracting electrical labels of the vanilla baluns and comparison between mathematically extracted and ADS simulated results

3.4.3 Training Neural Networks

Compared to the ML models for coupled lines, we add the output load Z_L as an additional dimension for inputs, since we must know Z_L in advance to compute Z_S (or R_{in}), C_{in}, $Q = Z_S/Z_C$, and passive loss. From all the simulated baluns that are continuously sampled from the physical design space, we also randomly sample various values of Z_L in

the range from 10-150Ω and mathematically apply our extraction technique in sub-section 3.4.2 to develop our database for baluns.
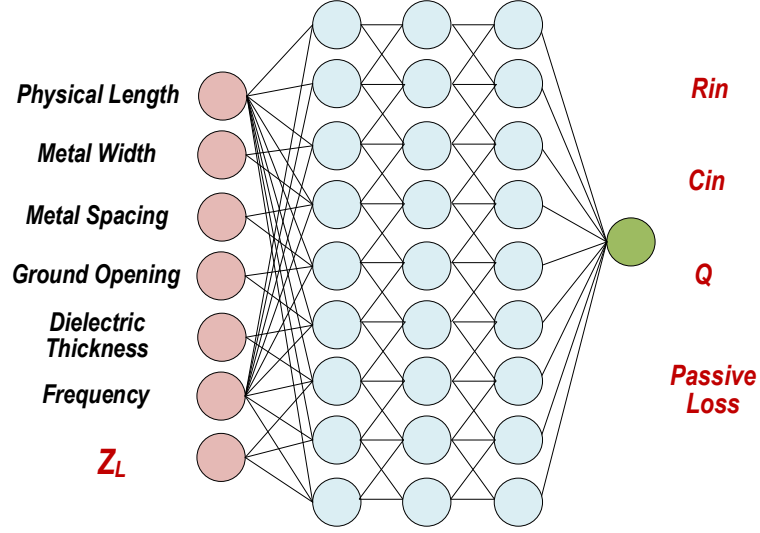
Figure 3.12 Neural Networks for the physical-electrical ML models for vanilla baluns.

Resolving the task of developing physical-electrical ML models for coupled lines, we design neural networks with 3 hidden layers with hidden dimensions of 128, 128, and 64, respectively. The input dimension of the ML model for vanilla baluns is 7, which equals the input dimensions of the ML models for coupled lines plus one for the additional dimension of an output load Z_L. The outputs have a dimension of 1 that indicates the electrical label we want to predict. We build separate coupled-line ML models to learn the source impedance Z_S (or R_{in}), the resonated parasitic capacitor C_{in}, the loaded $Q = Z_S/Z_C$ of the network, and the passive loss of the baluns, as shown in Fig. 3.12. From the physical-electrical database, we train our neural networks with a batch size of 128, a learning rate of 0.001, and the loss of mean absolute error, and we employ Adam optimizers to update the learnable weights of the models over 10 epochs.

3.4.4 Evaluating Machine Learning Models
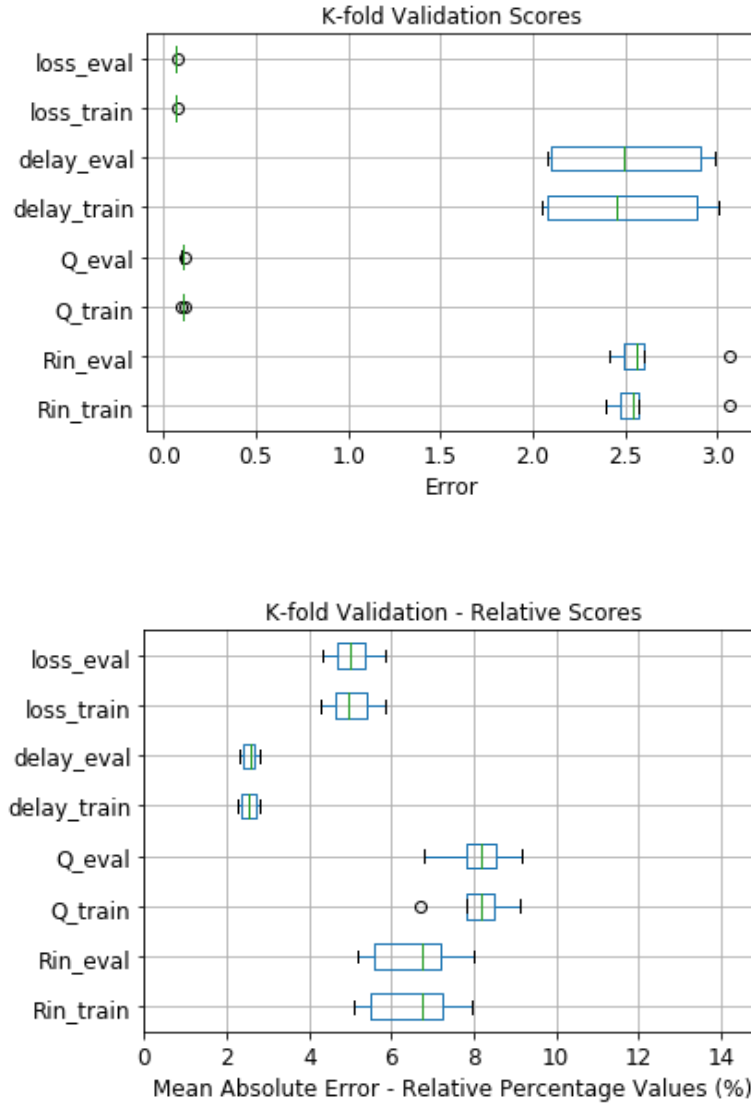
Figure 3.13 K-Fold Validation Scores for the ML models for baluns. The first row is absolute errors, and

the second row is relative errors. The relative errors of less than 10% indicate that the ML models

accurately predict electrical properties within the range of 0.9-1.1 times the ground-truth values.

We also apply the K-fold validation technique to evaluate the performance of ML models for baluns by splitting the data into 5 random portions following techniques in subsection 3.3.4. The validation shows that the ML models can predict the passive loss

with an average error of less than -0.07dB and compute the phase delay from inputs to outputs with an average error of 2-3º. The models also can learn the quality factor Q with an error of less than 0.1 (for an average Q of 3), and the input impedance Z_S (or R_{in}) of 2-3Ω (for an average input impedance of 70Ω). Demonstrated in the second row of Fig. 3.9b, the mean values of relative percentage errors for passive loss and phase delay are all less than 6%, and those for Q and R_{in} are less than 9%. Note that a relative error of less than 10% indicates that the ML models accurately predict the electrical values within the range of 0.9-1.1 times the ground-truth values. From the K-fold validation results, the error is small and identical between the training set and the validation set, which indicates that the ML models can accurately match the physical-electrical relationship for baluns.

3.5   The Physical-Electrical Machine Learning Models for Other EM Blocks
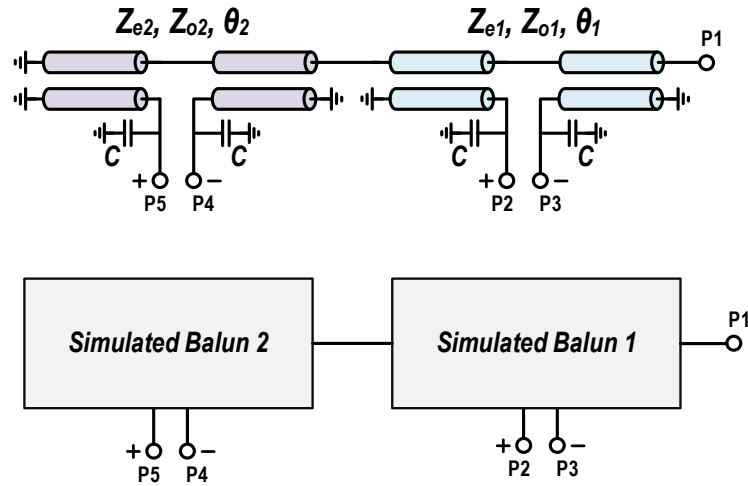
Figure 3.14 Example of generating training data for series-connected baluns without re-running HFSS

simulation

The framework shown in section 3.3 and 3.4 for coupled lines and vanilla baluns is generic, such that we can apply the same framework to build ML models for other EM

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blocks by sampling from a continuous design space, extracting electrical labels, training ML models, and evaluating with K-fold validation.

However, with the existing data that we have collected, we can simultaneously generate new training data for the new EM blocks without rerunning EM solvers to simulate EM structures. For example, Fig. 3.14 illustrates the schematic for the series-connected baluns. Conventionally, we need to build an HFSS model with two baluns connected in series, then continuously sample various values for physical dimensions of those baluns. Equivalently, we might ignore the minor effect of the connection between 2 baluns, sample two simulated baluns directly from our database, and connect two S-parameters files in series to construct S-parameters for a series-connected balun. Similar to the LEGO concepts, where we reuse previous designs to immediately build a new one, we can reuse the existing simulated S-parameter files to develop new S-parameters for new EM blocks.

After generating new data by "LEGO"-ing the existing data, we can apply mathematical extraction and train ML models for new EM blocks. While developing ML models for other EM blocks are not so challenging, those tasks are beyond the topics we want to explore in this thesis.

CHAPTER 4. MACHINE LEARNING FOR AUTOMATING MM-WAVE DESIGNS - PART 1

The current approach to design EM structures is heavily based on trial-and-error, such that the quality of EM design exhibits high variance, and the overall design process consumes a large amount of time and engineering effort. To resolve this problem, we propose in this chapter an automation technique that can drastically reduce the design time from days-weeks-months to seconds while maintaining the high quality of EM designs. Utilizing the BCOD theory presented in Chapter 2 and our pre-trained ML models developed in Chapter 3, our proposed approach can fully automate the mm-wave EM designs to achieve the lowest loss for numerous mm-wave design tasks. Notably, optimizing physical dimensions for the lowest metal loss is a challenging problem, and to the best of our knowledge, we are not aware of any prior techniques that can systematically address the specification of the lowest metal loss for mm-wave EM designs.

The automation pipeline we propose in this chapter is generic, and we can apply the same principle to automate various mm-wave design tasks, including Directional Couplers, Impedance Transforming Baluns, Series-Connected Power Combiners, Out-Phasing circuits, and Doherty networks. From a specification of the output load impedance Z_L, the optimum load impedance Z_S (or R_{in}), and the parasitic capacitance of active device $Z_C = Z_S/Q$, numerous automation examples over a wide range of mm-wave tasks verify that our proposed approach can both accurately design various electrical specifications for many mm-wave EM structures and efficiently complete all those tasks within a computational time of seconds.

4.1 The Proposed Approach to Automate Mm-Wave EM Designs

The current approach to design EM circuits, as shown in Fig. 4.1a, heavily relies on trial-and-error. Engineers must keep running EM simulators to calculate electrical properties and keep updating physical parameters for many iterations until all electrical specifications are met. As a result, the design process consumes a large amount of time and labor, and the outcome of the process often exhibits high variance in terms of the final quality (see section 3.1).
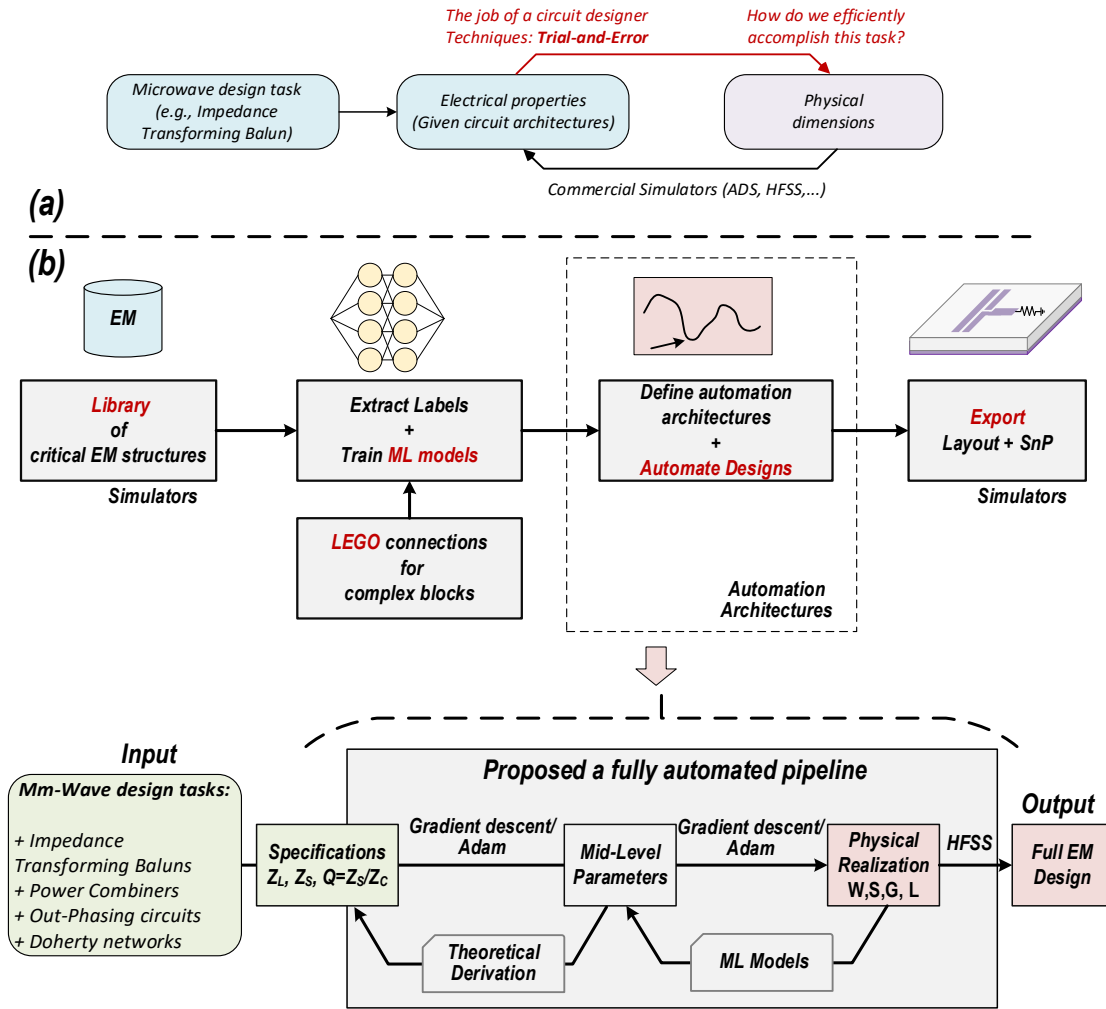
Figure 4.1 (a) Current approach of designing EM structures (b) Proposed pipeline to design EM structures.

In this dissertation, we propose an automation approach that leverages Machine Learning techniques to resolve the drawbacks of the current approach to design EM structures. Described in Fig. 4.1b, the proposed approach includes developing a database or library of critical EM structures, training ML models from extracted electrical labels, applying an automation algorithm, and exporting the final designs and their S-parameter files. We present our approach to build a database for EM structures by sampling physical parameters from a continuous design space and training ML models utilizing neural networks with extracted electrical labels. In Chapter 3, the K-fold validation results show that ML techniques can accurately compute electrical parameters from physical dimensions. In this chapter, we demonstrate the automation algorithm with various automation architectures to fully design numerous mm-wave tasks, including Directional Couplers, Impedance Transforming Baluns, series-connected Power Combiners, Out-Phasing circuits, and Doherty networks. Given a design task and a specification for an output load Z_L, an optimum impedance Z_S, and a parasitic capacitance $Z_C = Q/Z_S$ of a device, the pipeline automatically calculates the optimum physical dimension and generates a full EM design that satisfies all electrical specifications.

Compared to the current approach to design mm-wave EM structures, our approach is drastically faster, because we can use ML approaches to effectively compute electrical properties within a small fraction of seconds while the current approach takes minutes-hours to complete an EM simulation. Our technique is also more reliable than the current technique because our automation algorithm does not depend on subjective judgements to update the EM parameters while the current technique heavily relies on the experience of circuit designers to make an update. Additionally, the proposed approach directly optimizes

for the lowest metal loss, whereas the current technique might not have a systematic way to fully address the loss specifications.

In this chapter, we start from the automation architectures of fundamental blocks, such as Directional Couplers or Impedance Transformation Baluns, and leverage those automations to design more complex structures, such as Series-Connected Power Combiners, Out-Phasing circuits, or Doherty networks. We present the architectures that use the ML model for coupled lines in this chapter and illustrate those that use the ML model for vanilla baluns in Chapter 5.

The organization of this chapter is as follows: Section 4.2 demonstrates the architecture for designing Directional Couplers, section 4.3 illustrates the indirect approach to automate Impedance Transforming Baluns, and section 4.4 outlines the technique used to implement Power Combiners. In Chapter 5, we will automate the design of Baluns, Out-Phasing circuits, and Doherty networks.

4.2 Automating the Design of Directional Couplers

The first EM design we automate is that of Directional Couplers, which utilize coupled lines to couple the power from the input to the coupled port with a 90° phase shift. In practical application, this automated technique can assist EM designs in many critical Mm-wave blocks, such as the inputs and outputs of Balanced Amplifiers, IQ phase shifters, Balanced Low Noise Amplifiers, or inputs of Doherty architectures. To demonstrate our proposed approach, we mathematically formalize the automation problem and outline our algorithm in subsection 4.2.1. We then verify the effectiveness of the proposed technique by presenting design examples with 50Ω characteristic impedance for various coupling

factors of -3dB, -10dB, and -20dB in subsections 4.2.2, 4.2.3, and 4.2.4, respectively. Notably, the proposed algorithm can complete all design specifications within a design time of seconds.

4.2.1   Automation Problems and Algorithms

Automation Problem: *Given the coupling factor C in dB, characteristic impedance Zo of the termination impedance, and the frequency of operation, automate a full EM design of directional coupler with the lowest loss.*

Among many ways of computing the overall loss, we define the loss to be minimized in this automation problem as the sum the even-mode and odd-mode loss.

Approaches
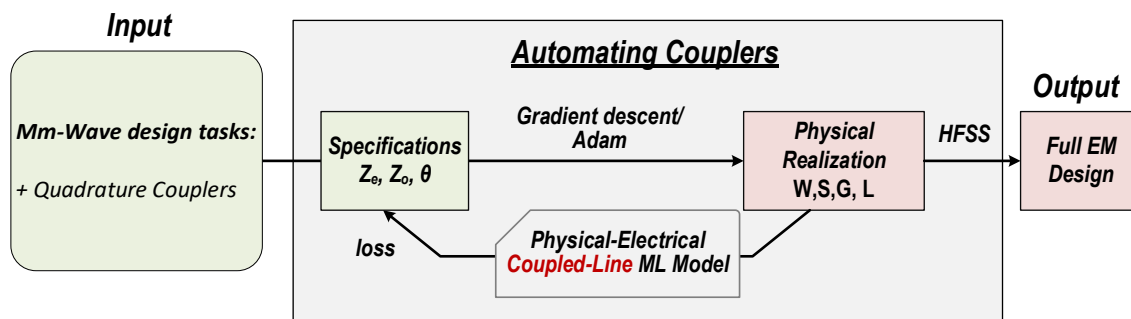
Figure 4.2 Proposed automation architecture for designing Directional Couplers.

Figure 4.2 depicts our automation architecture for designing couplers. From the coupling factor and characteristic impedance, we compute the even- and odd-mode impedances of the coupler, utilize our pre-trained physical-electrical ML model for coupled lines and gradient descent to optimize for physical dimensions, and then use HFSS [38] to

generate and simulate a full EM design. To start the automation loop, we must initialize

the random physical dimensions for the coupled line and employ gradient descent to update

those parameters toward the design goal. Conventionally, we only choose one initialization

point for the optimization. In this work, to make the automation process less sensitive to

the initialization, we initialize N sets of physical dimensions, which is equivalent to

attempting to design the coupler N times, where the value of N is typically from 20-100.

Among those N attempts, we select the design with the lowest loss.

Loss Functions

For all the physical dimensions, we compute the characteristic impedance, electrical

length, and loss of the even and odd modes. The optimization loss is computed as the

weighted mean absolute error between the predicted outputs and the desirable electrical

labels, where the weights are inversely proportional to the values of electrical labels:

$$optimization\ loss\ = \sum_k \frac{|y_{pred} - y_{true}|}{|y_{true}|},$$

The ground truth value y_{true} includes the characteristic impedances Z_e, Z_o for the even

and odd modes and the electrical lengths $\theta_{even} = \theta$, $\theta_{odd} = \theta$. The metal loss is computed as

the sum of the losses for the even and odd modes, as defined in the automation problem,

and the final loss is the sum of the optimization loss and the metal loss:

$$metal\ loss\ = \sum_k |loss_{even}| + |loss_{odd}|,$$

$$loss\ =\ optimization\ loss\ +\ metal\ loss$$

Subsequently, we compute the gradient of the loss with respect to all physical parameters and apply gradient descent with Adam optimizers to update the physical dimensions to minimize the loss. Repeating the loop for 2000 iterations, we finalize the physical dimensions for N designs, select the one that has optimization loss below a certain threshold (typically 0.5) with the lowest metal loss, and use HFSS to generate a full EM design and simulate the performance of this final design.

Algorithms

Overall, the algorithm for automating coupler designs is as follows:

Algorithm for Automating the Design of Couplers

Compute Ze, Zo, θ from electrical specifications

Randomly initialize N sets of physical dimensions for N coupled lines as an N×4 vector

Fix the dielectric thickness and frequency to initialize an N×6 input vector for the ML models

Load the physical-electrical ML models for coupled-lines

For step = 1, M do

Predict the impedance, electrical length, and loss of both even and odd modes

Compute the optimization loss as the weighted mean absolute error between predicted outputs and desirable electrical labels. The weights are inversely proportional to the values of electrical labels.

Sum the optimization loss and metal loss as the final loss

Compute the gradient of the loss with respect to each physical parameter

Update N sets of physical dimensions by gradient descent with Adam update rules

Select the dimensions with the lowest metal loss which have optimization loss less than threshold

Simulate the selected dimensions with HFSS and generate S-parameters

4.2.2 Design Examples for -3dB Couplers

-3dB Directional Couplers

$t_d = 1.6\mu m$

$t_d = 3.2\mu m$

$t_d = 4.8\mu m$

$600\mu m$

$t_d = 6.4\mu m$

Figure 4.3 HFSS models of automated EM designs for -3dB couplers over various dielectric thicknesses.

We apply the automation pipeline to design directional couplers with a -3dB coupling factor for 50Ω characteristic impedances over several dielectric thicknesses of 1.6μm, 3.2 μm, 4.8 μm, and 6.4 μm. Those values of dielectric thicknesses represent various possible

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cases for on-chip metal options. Taking less than 20 seconds for the entire design process, the proposed algorithm automatically generates an EM design for -3dB directional couplers as shown in Fig. 4.3. As all couplers have the same electrical length, the algorithm also constructs couplers with similar physical lengths. Because the coupling factors are the same over all dielectric thicknesses, the algorithm learns to widen the metal width as the dielectric thickness increases to maintain a constant coupling factor. Shown in Fig. 4.4, the HFSS results from those automated designs verify that all generate -3dB coupled power and satisfy all other design specifications.
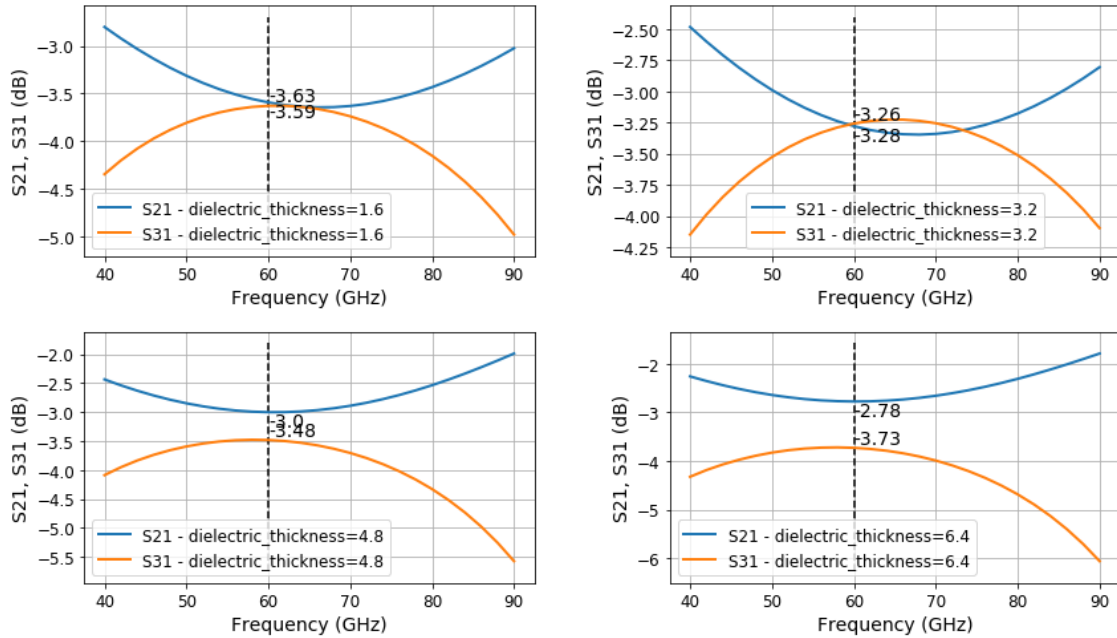
Figure 4.4 Simulated results for automated designs of -3dB couplers over various dielectric thicknesses.

4.2.3 Design Examples for -10dB Couplers

Another example is to design -10dB couplers for 50Ω characteristic termination impedances over several dielectric thicknesses of 1.6µm, 3.2 µm, 4.8 µm, and 6.4 µm.

With a total design time for all dielectric thicknesses of less than 20 seconds, the proposed algorithm automatically constructs EM structures for -10dB directional couplers as shown in Fig. 4.5. The automated pipeline produces lines with similar physical length for all designs to achieve the same electrical length and narrows down the metal spacing as the dielectric thickness goes up to maintain constant coupling factors. Depicted in Fig. 4.6, the simulated results demonstrate that all automated designs exhibit -10dB coupling across all dielectric thicknesses, confirming the accuracy of the proposed approach.
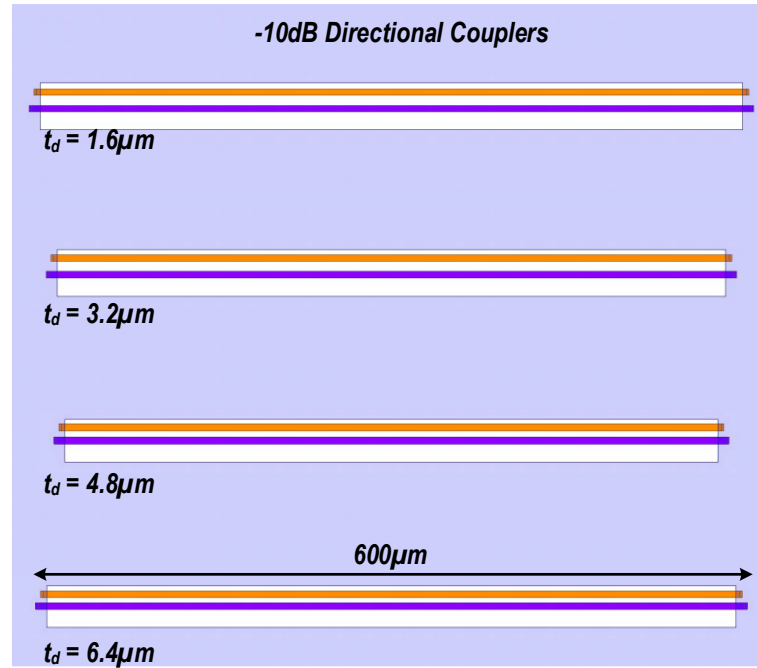
Figure 4.5 HFSS models of automated EM designs for -10dB couplers over various dielectric thicknesses.
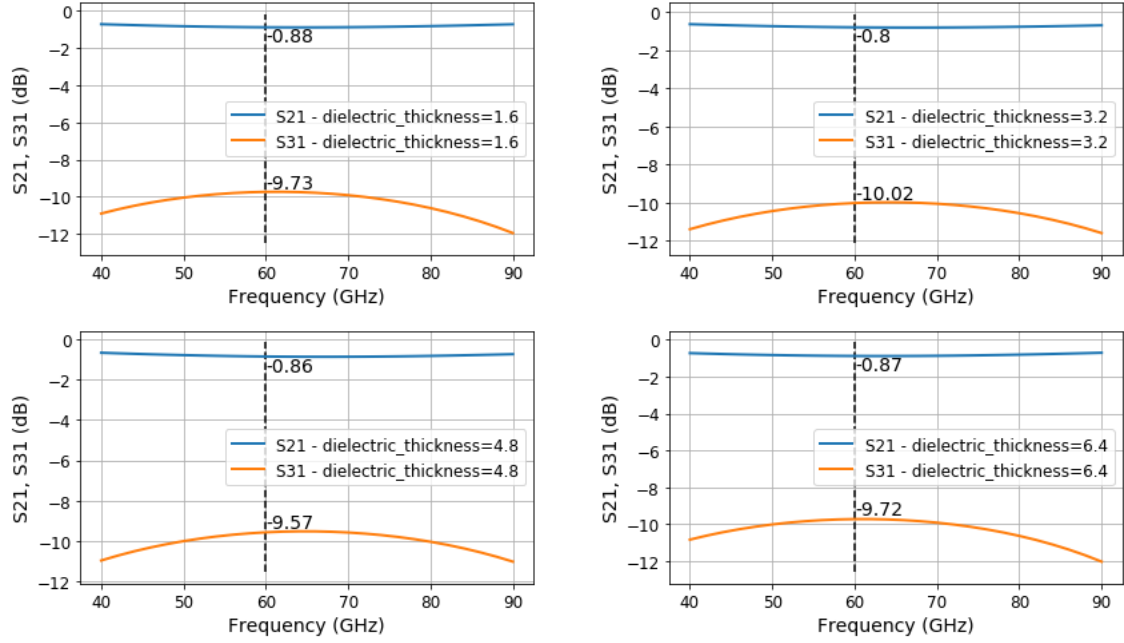
Figure 4.6 Simulated results for automated designs of -10dB couplers over various dielectric thicknesses.

4.2.4   Design Examples for -20dB Couplers

We also automate the design of -20dB couplers for 50Ω characteristic termination impedances over various dielectric thicknesses of 1.6µm, 3.2 µm, 4.8 µm, and 6.4 µm. Completing all design tasks in less than 20 seconds, the pipeline automatically generates full EM designs for -20dB directional couplers as illustrated in Fig. 4.7. As a -20dB coupling factor implies only a limited amount of power is coupled, all the automated designs have the ground plane underneath the coupled signals to reduce the coupled power. The spacing between two metal traces is relatively large, leading to the dielectric thickness having an insignificant effect on the coupling factor. Consequently, the automation algorithm generates similar geometries for all designs. Simulated with HFSS, all automated designs exhibit approximately -20dB coupling factors for all dielectric thicknesses, as illustrated in in Fig. 4.8, which demonstrates the effectiveness of the proposed technique.

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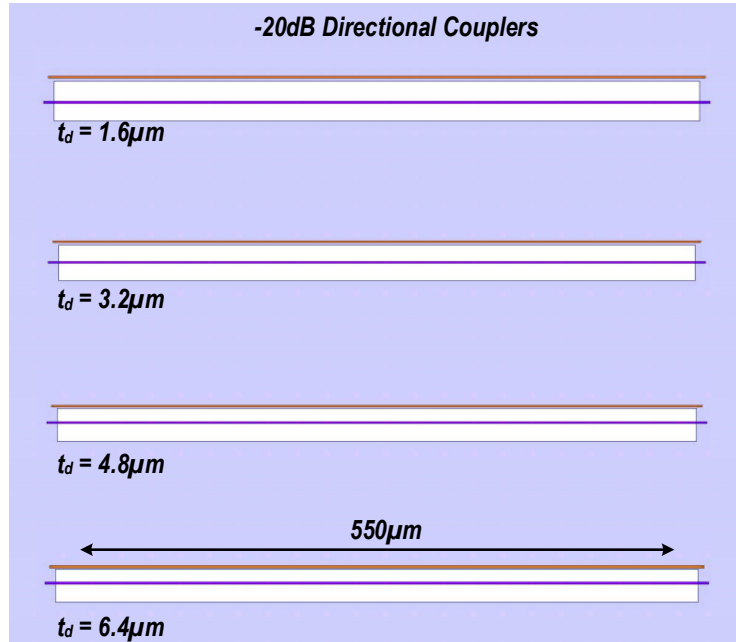
Figure 4.7 HFSS models of automated EM designs for -20dB couplers over various dielectric thicknesses.
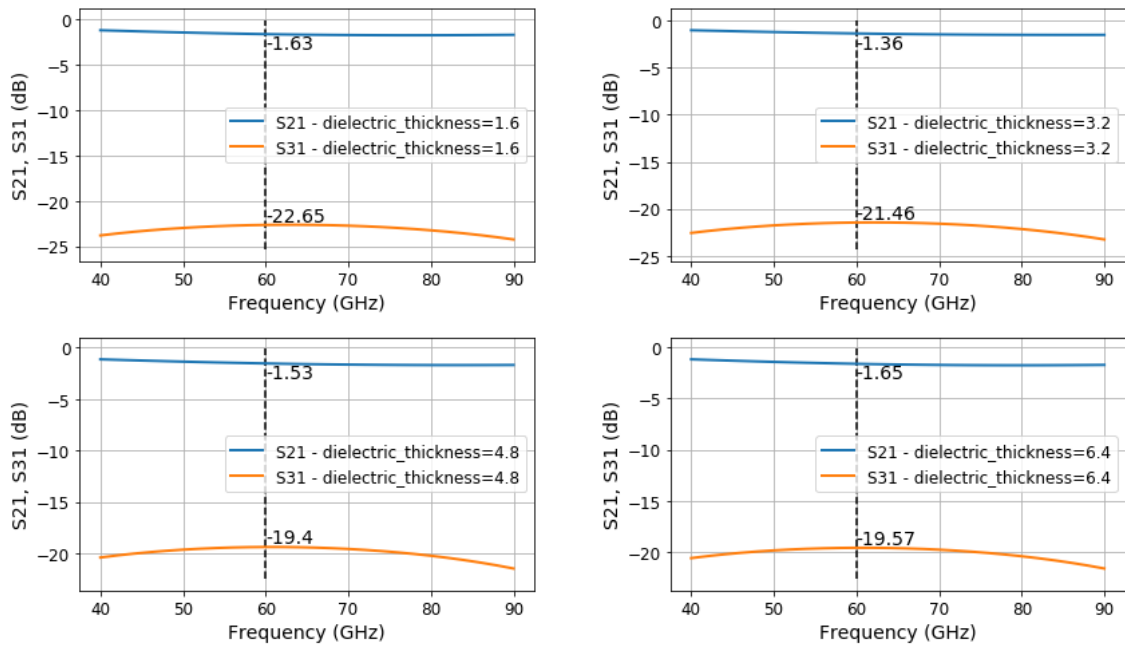
Figure 4.8 Simulated results for automated designs of -20dB couplers over various dielectric thicknesses.

4.3 Automating the Design of Impedance Transforming Baluns – The Indirect Approach

The second EM design we automate is that of Impedance Transforming Baluns, which transform the output load Z_L to the source impedance Z_S and resonate out a device parasitic capacitance $Z_C = Z_S/Q$. To generate physical dimensions for baluns, in this section, we introduce an intermediate step of computing coupled-line parameters based on the lossless theory developed in Chapter 2, and subsequently, we call this technique the "indirect" approach.

This automation pipeline can support all the blocks in mm-wave systems involving differential pairs, e.g., PAs, LNAs, Mixers, and Phase Shifters. The designs of Impedance Transforming Baluns are highly critical at the output network of Power Amplifiers, where the requirement for minimizing the passive loss of the baluns is exceptionally stringent. For example, an improvement of 0.5dB in the loss of balun can boost the efficiency of an entire transmitter system by 10%. We also utilize baluns at the input stages for differential signal generation and impedance matching. In this functionality, Impedance Transforming Baluns generally have two distinct specifications for two different type of active devices: high impedance devices, such as CMOS, GaN, and low impedance devices, such as SiGe or InP.

To present our approach, we define the automation problems in mathematical terms and our proposed algorithm in subsection 4.3.1. As the specification for baluns can vary over several applications, we demonstrate three examples of baluns: (1) for mm-wave output networks in subsection 4.3.2, (2) for mm-wave CMOS (high impedance devices) input

networks in subsection 4.3.3, and (3) for mm-wave SiGe (low impedance devices) input networks in subsection 4.3.4.

4.3.1   *Automation Problems and Algorithms*

Automation Problem: *Given the Z_L as the load impedance, Z_S as an optimum impedance seen by device, and the loaded Q of the network, automate a full EM design of an impedance transformation with the lowest loss at the frequency of operation.*
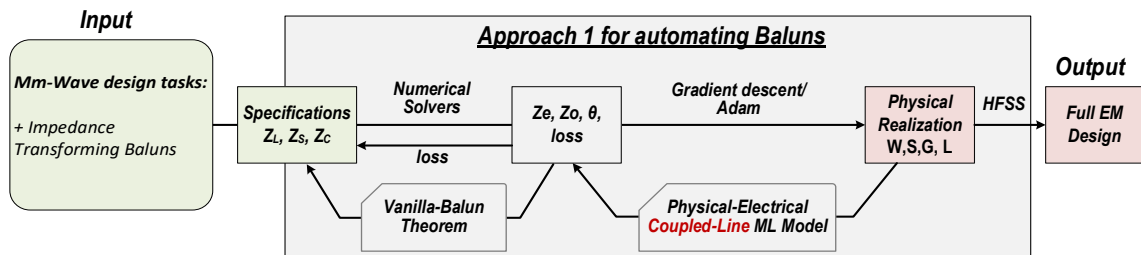
Approaches

Figure 4.9 Proposed indirect approach to automate the design of Impedance Transforming Baluns.

Depicted in Fig. 4.9, our proposed approach to indirectly automate the design of Impedance Transforming Baluns is formulated by the theorem of vanilla baluns developed in Chapter 2 and the physical-electrical coupled-line ML model built in Chapter 3. Given the electrical specifications, the first step is to compute the electrical parameters of coupled lines (Ze, Zo, θ), and the second step is to convert from electrical properties to physical dimensions, which we resolve by leveraging the automation pipeline for couplers as shown in section 4.2.

This indirect approach mimics how an engineer often designs the Microwave circuits: gradually transform from top-level specifications to low-level electrical parameters and utilize EM simulators to iteratively realize the structure's physical dimensions. In this design task for baluns, we can have many solutions for Z_e, Z_o, θ which all can satisfy the impedance transformation ratio and lead to good designs. As a result, we sweep values of θ from 5° to 45° in 2° incremental steps, solve the theoretical coupled line parameters numerically for each value of θ, and automate the physical dimensions for all. Among many possible coupled line parameters, we choose the design with the lowest loss when evaluating the physical-electrical ML models for vanilla baluns.

Loss functions

The numerical solver can compute exact values of Z_e, Z_o, θ that satisfy the specification of baluns by following the lossless assumption of coupled lines. The step of obtaining physical dimensions has the same loss as the automation pipeline for couplers.

Algorithms

Overall, the algorithm to indirectly automate the Impedance Transforming Baluns is as follows:

Algorithm for Indirectly Automating the Design of Impedance Transforming Baluns

For θ = 5°, 7°, 9°, …, 45° do:

Follow the technique in section 2.2 to numerically solve Ze, Zo, θ

Generate a list of all possible theoretical solutions and follow the automation pipeline for coupler designs to convert to a list of possible physical dimensions

Employ the ML model for vanilla baluns to select designs with the lowest loss

Simulate the selected parameters with HFSS and generate the S-parameter files

Design Examples

We frequently design Impedance Transformation Baluns for use in output networks, CMOS input networks with high Z_S, and SiGe input networks for low Z_S. To evaluate the effectiveness of the proposed approach, we present three design examples for those commonly used cases.

Design Specifications: *Design an impedance transforming balun at 60GHz for three different sets of specifications*

(1) Output networks: $Z_L=50\Omega$, $Z_S=30\Omega$, Q=1.2

(2) CMOS input networks: $Z_L=50\Omega$, $Z_S=200\Omega$, Q=6

(3) SiGe input networks: $Z_L=50\Omega$, $Z_S=20\Omega$, Q=0.5

The thickness of the metal can be 1.6μm, 3.2μm, 4.8μm, 6.4μm.

4.3.2 Design Examples for Output Baluns

The first design example evaluates the algorithm on the specification of $Z_L=50\Omega$, $Z_S=30\Omega$, Q=1.2, which is typically the specification for an output balun at 60GHz. Following the steps presented in subsection 4.3.1, the algorithm first derives the theoretical values of coupled lines over various values of theta, as shown in the blue curves in the top

row of Fig. 4.10, and then utilizes the physical optimizer to generate the physical dimensions of those coupled lines, where the extracted electrical parameters of those physical implementations are depicted in the yellow curves in the top row of Fig. 4.10. The theoretical solutions exist for θ=10-50°, as in the blue curves in the top row of Fig. 4.10, but not all those theoretical values can be physically realized on-chip. Shown as the yellow curves in the top row of Fig. 4.10, the physical optimizer can only design a physical realization for θ=20-46°. One of the critical design insights that the algorithm yields is that coupled lines with an even-mode impedance greater than 100Ω or with a coupling factor greater than 0.8 are typically challenging to implement on-chip.
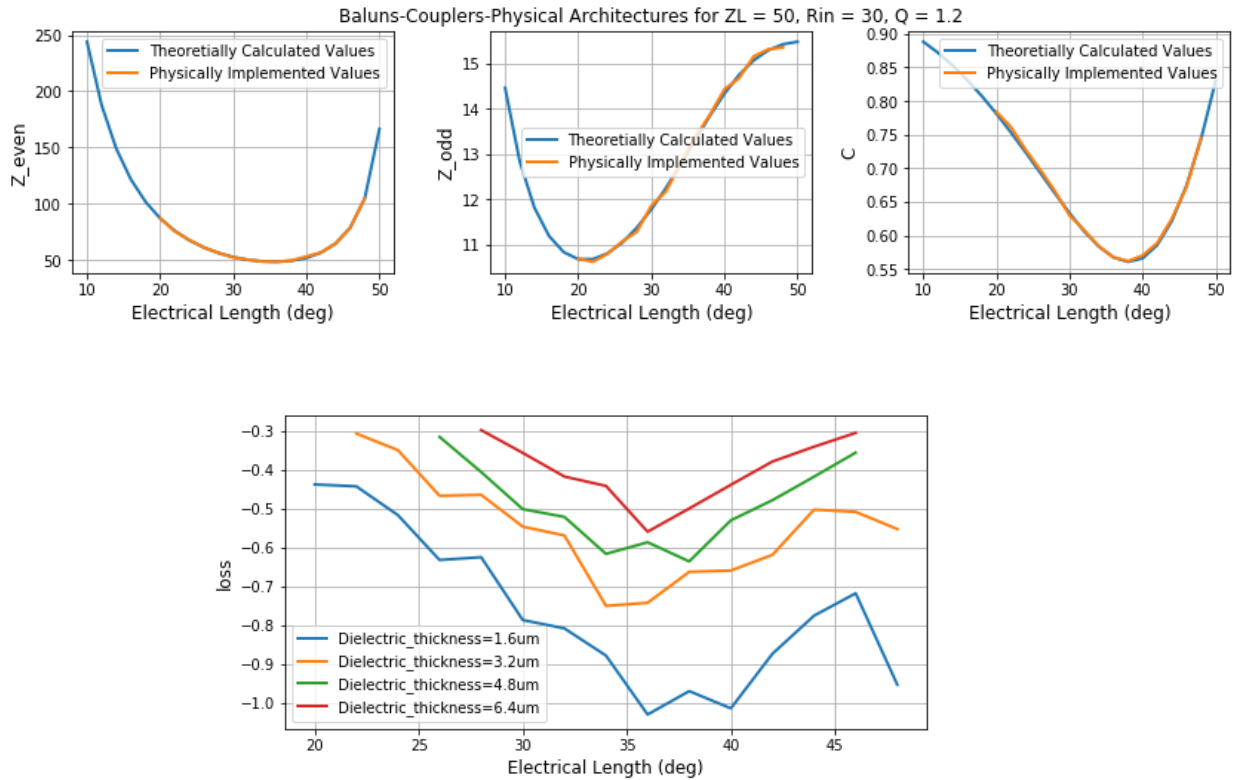
Figure 4.10 Theoretical values and physically implemented values for the coupled lines that result in impedance transforming baluns with Z_L=50Ω, Z_S=30Ω, and Q=1.2 (the first row), and predicted loss for various implementation of the automation algorithm (the second row).

Figure 4.11 HFSS models of automated designs with the indirect approach for impedance transforming

baluns with Z_L=50Ω, Z_S=30Ω, and Q=1.2.

We employ the vanilla balun ML model to compute the loss for all the coupled lines that are possible to be realized on chip and illustrate the results in the second row of Fig. 4.10b. From the loss curves, we select the designs with the lowest loss as the final EM designs and show the automated Impedance Transforming Baluns for various thicknesses in Fig. 4.11. Among all realizable values, in this design example, the lowest possible electrical length also minimizes the loss. Additionally, Fig. 4.11 demonstrates the strategy the algorithm adopts when working with various dielectric thicknesses. The coupling factor should stay relatively constant over all dielectric thicknesses, and the algorithm maintains this coupling factor by widening the metal traces as the dielectric thickness increases.

The results also inform us about the trade-off when choosing the metal layers to implement the baluns. On one hand, when two metal layers are close to each other with a smaller dielectric thickness, they can achieve tighter coupling factors, so we can realize a wider range of electrical parameters. As an example, the dielectric thickness of 1.6µm supports the implementation of input baluns with electrical lengths from 20°-48°, but the dielectric thickness of 6.4µm only realize the range from 28° to 46°. On the other hand, higher dielectric thicknesses often result in lower loss. The second row of Fig. 4.10 illustrates that the loss curve gradually increases as the dielectric thickness goes up from 1.6µm to 6.4µm.
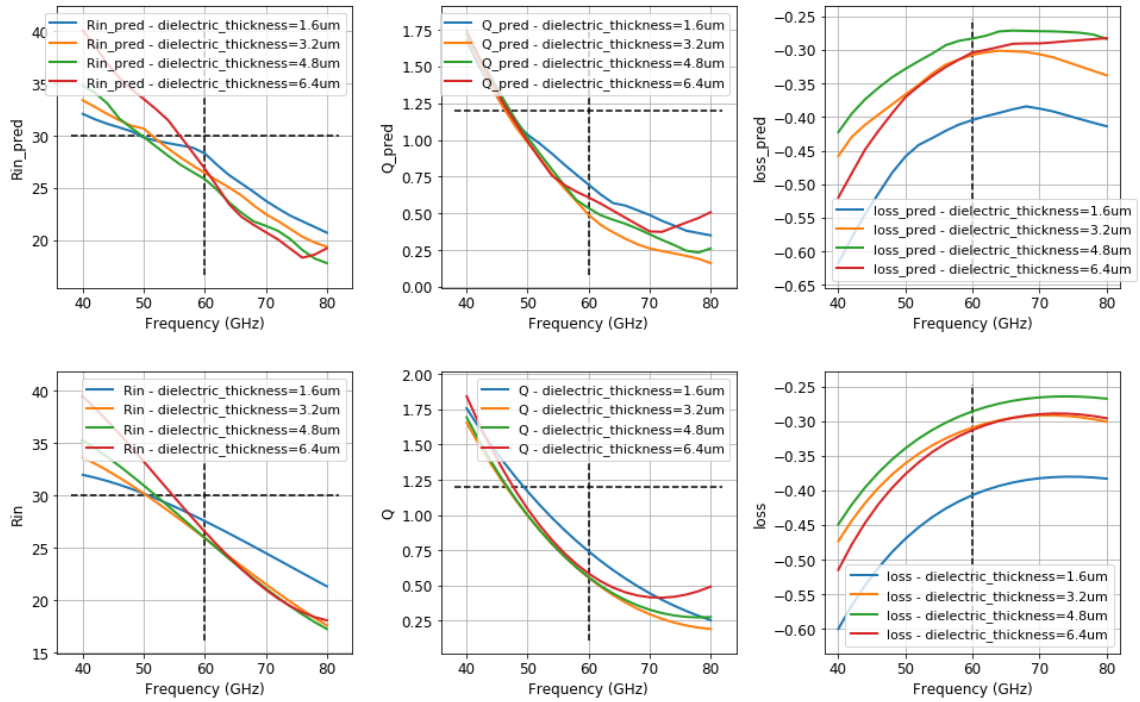
Figure 4.12 Automated results for impedance transforming baluns with Z_L=50Ω, Z_S=30Ω, and Q=1.2. The first row describes the predicted specification by the physical-electrical ML models, and the second row shows the actual physical-electrical values obtained from HFSS.

Finally, the algorithm selects the design with the lowest predicted loss, builds the HFSS model, and simulates the S-parameters files. From HFSS simulated files, we terminate the output load with Z_L=50Ω and utilize ADS software to compute the Z_S (R_{in}), Q, and loss in the bottom row of Fig. 4.11. The predicted electrical label shown in the top row closely agrees with the actual results from HFSS and ADS, demonstrating that our pre-trained ML models can accurately compute electrical parameters over all frequencies and design cases. Note that the HFSS software takes several hours to simulate the results, but the ML models take less than a second to compute the prediction. Guided by the lossless coupled line models, the automated designs achieve Z_S (or R_{in}) from 25-28Ω, Q from 0.5-0.75, and passive loss from -0.85dB to -0.78dB across many dielectric thicknesses, which are relatively close to the design specifications. We further improve the automation pipeline with the direct approach and present the results in section 5.1.

4.3.3   Design Examples for CMOS Input Baluns

As the second illustration, we automate the design of CMOS input baluns with Z_L=50Ω, Z_S=200Ω, and Q=6 at 60GHz. Following the steps presented in subsection 4.3.1, the algorithm first computes the theoretical values for coupled lines, as shown in the blue curves in the first row of Fig. 4.13, where the theoretical solutions exist for θ=10-50°. Among those solutions, the algorithm physically realizes the coupled lines with electrical length θ in the range of 24-50°, as shown in the yellow curves in the first row of Fig. 4.13. The constraint here is that the even-mode impedance Ze must be less than 120Ω and the odd-mode impedance Zo must be less than 45Ω. The pipeline then utilizes the vanilla balun ML model to evaluate the loss of all physical realizations, in which we depict the results in the second row of Fig. 4.13. The optimum electrical length for this design specification is

approximately θ=32°. The final physical dimensions are shown in Fig. 4.14, where one critical observation is that the algorithm moves two lines closer to each other as the dielectric thickness increases, so that the coupling factor remains constant across various thicknesses.
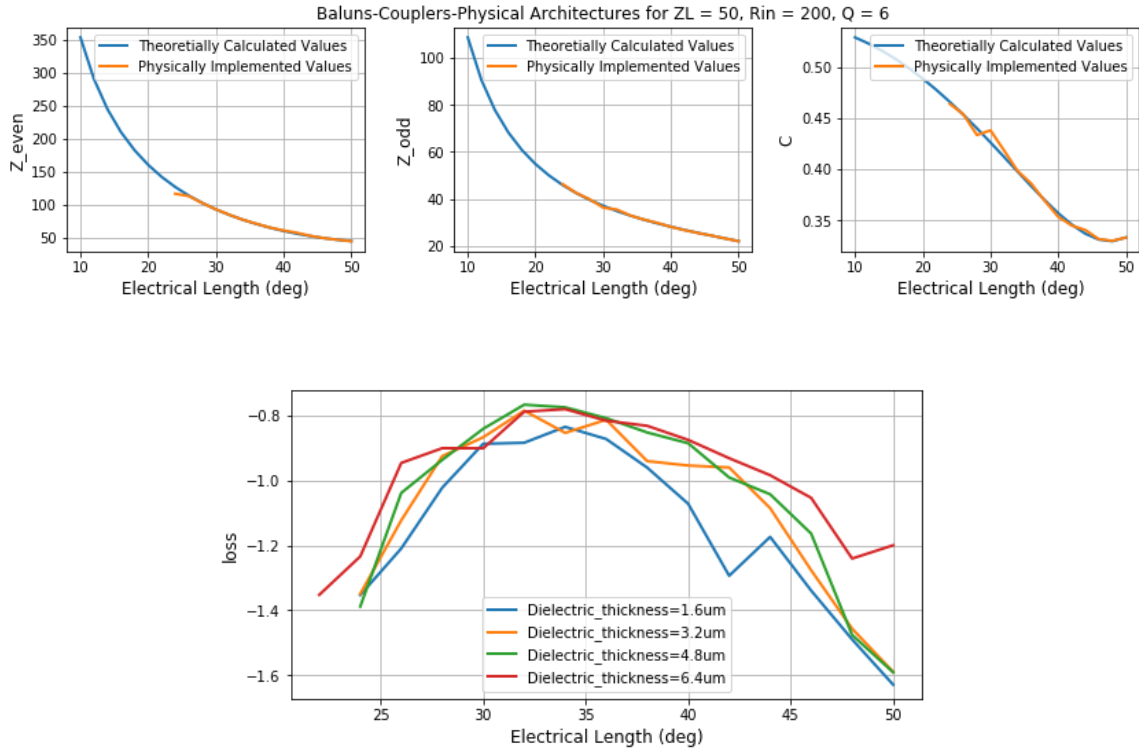
Figure 4.13 Theoretical calculated values and physically implemented values for the electrical properties of coupled lines that lead to impedance transforming baluns with Z_L=50Ω, Z_S=200Ω, and Q=6 (the first row) and predicted loss for various automated EM design from the automation algorithm (the second row).

From the simulated S-parameter files generated by HFSS, we terminate the output load with Z_L=50Ω and utilize the ADS software to evaluate the Z_S (or Rin), Q, and passive loss of the automated EM designs, as shown in the second row of Fig. 4.15. The predicted values using our vanilla balun models for Z_S (or Rin), Q, and passive loss, as depicted in the first row of Fig. 4.15, exhibit good agreement with the actual results by commercial

simulators, demonstrating the accuracy of our ML models. Based on the lossless coupled line models, the automated designs accomplish Z_S (or R_{in}) from 125-145Ω, Q from 4.0-4.5, and passive loss from -0.85dB to -0.78dB across many dielectric thicknesses, compared to the specification of Z_L=50Ω, Z_S=200Ω, Q=6.
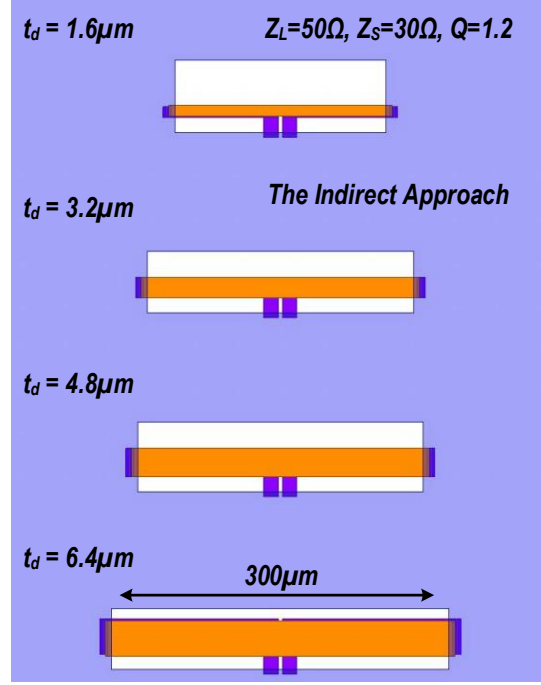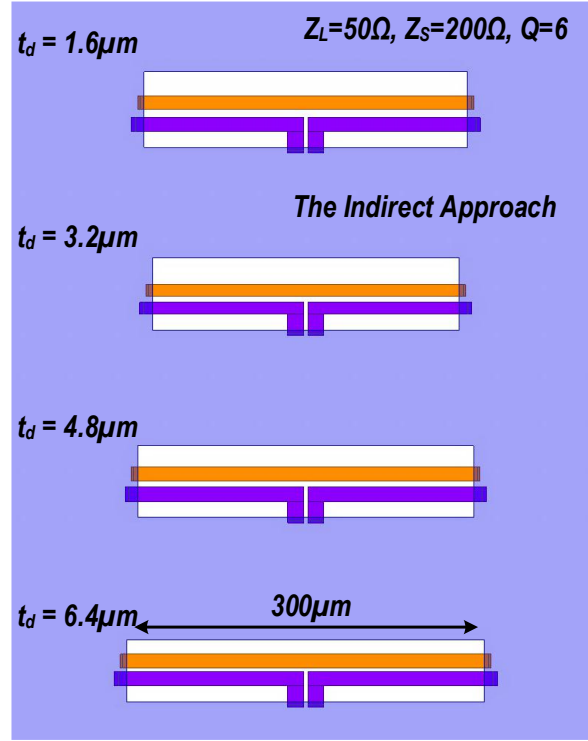

Figure 4.14 HFSS models of automated designs with the indirect approach for impedance transforming

baluns with Z_L=50Ω, Z_S=200Ω, and Q=6.
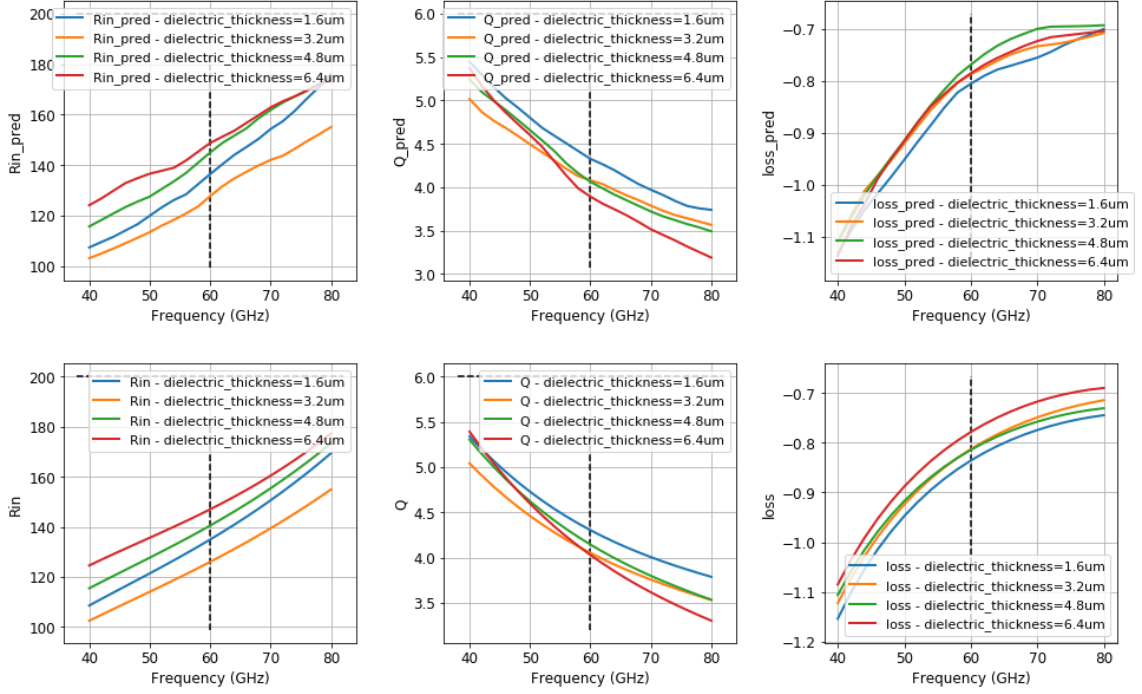
Figure 4.15 Automated results for impedance transforming baluns with Z_L=50Ω, Z_S=200Ω, and Q=6. The first row describes the predicted specification by the physical-electrical ML models, and the second row shows the actual physical-electrical results from commercial simulators.

4.3.4 Design Examples for SiGe Input Baluns

As the third illustration, we automate the design of SiGe input baluns with Z_L=50Ω, Z_S=20Ω, and Q=0.5. The algorithm initially evaluates the theoretical parameters for coupled lines, where the solutions exists for values of θ=30-40°, as shown in the blue curves in Fig. 4.16. Transferring those values to physical dimensions, the automaton pipeline for couplers can physically realize a range of electrical length θ=30-38°, where the constraint is that the even-mode impedance Ze must be less than 110Ω and the coupling factor must be less than 0.8 (see the yellow curves in Fig. 4.16). Among all the possible dimensions, we utilize our pre-trained ML model to compute the passive loss of all

automated designs and illustrate the results in the second row of Fig. 4.16. The optimum electrical length for this design specification is approximately θ=35°. Increasing the dielectric thickness leads to lower passive loss, with the highest loss occurring with 1.6µm and the lowest losses with 4.8µm and 6.4µm.
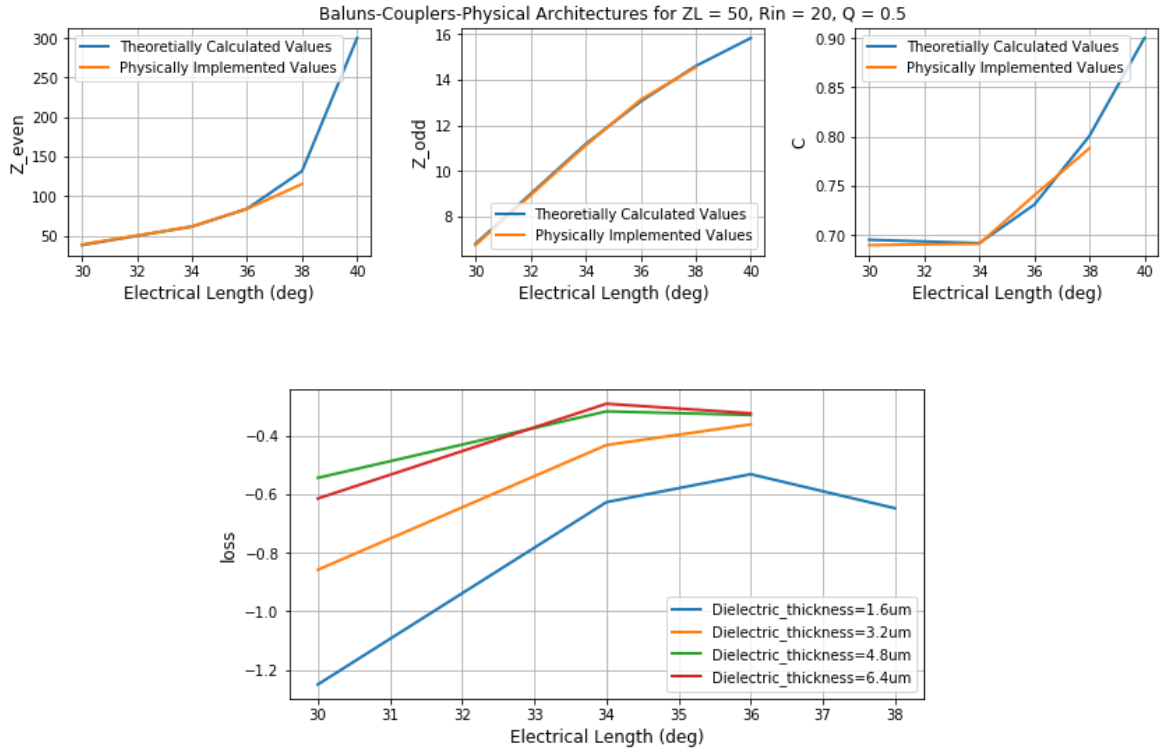
Figure 4.16 Theoretical calculated values and physically implemented values for the electrical properties of coupled lines that lead to impedance transforming baluns with Z_L=50Ω, Z_S=20Ω, and Q=0.5 (the first row) and predicted loss for various automated EM design from the automation algorithm (the second row).

Show in Fig. 4.17, the final automated designs illustrate several strategies the algorithm uses to maintain the same coupling factor over various dielectric thicknesses. At t_d=3.2µm, two metals stack directly on top of each other. When t_d increases to 4.8µm or 6.4µm, the algorithm widens the metal traces to compensate for the higher value of thickness.

However, when t_d reduces to 1.6 µm, the algorithm learns to keep a similar line width but moves the lines further away from each other to retain the same coupling strength.
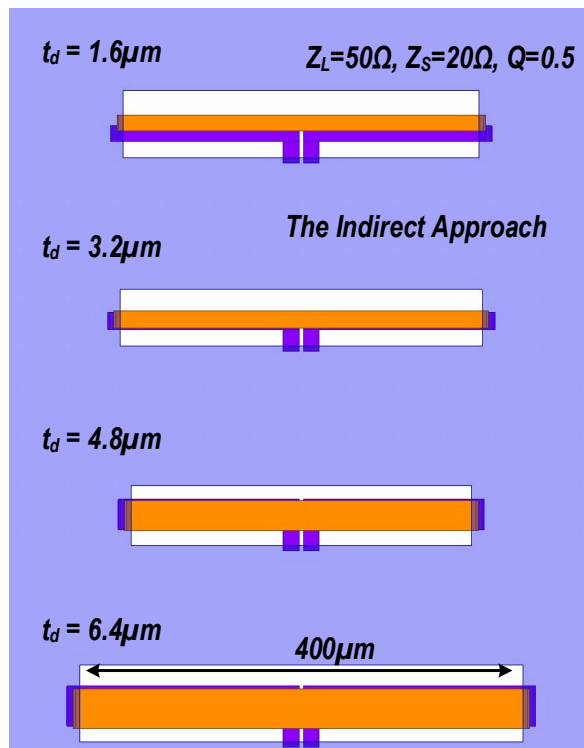
Figure 4.17 HFSS models of automated designs with the indirect approach for impedance transforming baluns with $Z_L=50\Omega$, $Z_S=20\Omega$, and Q=0.5.

We utilize the simulated S-parameters with HFSS and terminate the output load with $Z_L=50\Omega$ to evaluate the Z_S (or R_{in}), Q, and passive loss of the automated EM designs. The predicted values using our vanilla balun models for Z_S (or Rin), Q, and passive loss are shown in the first row, and the actual results by commercial simulators are illustrated in the second row of Fig. 4.18. Over the entire frequency range from 40-80GHz, the ML model predictions match closely with the actual results by commercial simulators. Note that the HFSS software takes several hours to compute the results, but the ML models take a fraction of a second to complete the prediction. Guided by the lossless coupled line

models, within the design time of seconds, the automated designs exhibit Z_S (or R_{in}) from 20-27Ω, Q from 0.25-0.6, and passive loss from -0.5dB to -0.3dB across many dielectric thicknesses, compared to the specification of Z_L=50Ω, Z_S=20Ω, and Q=0.5.
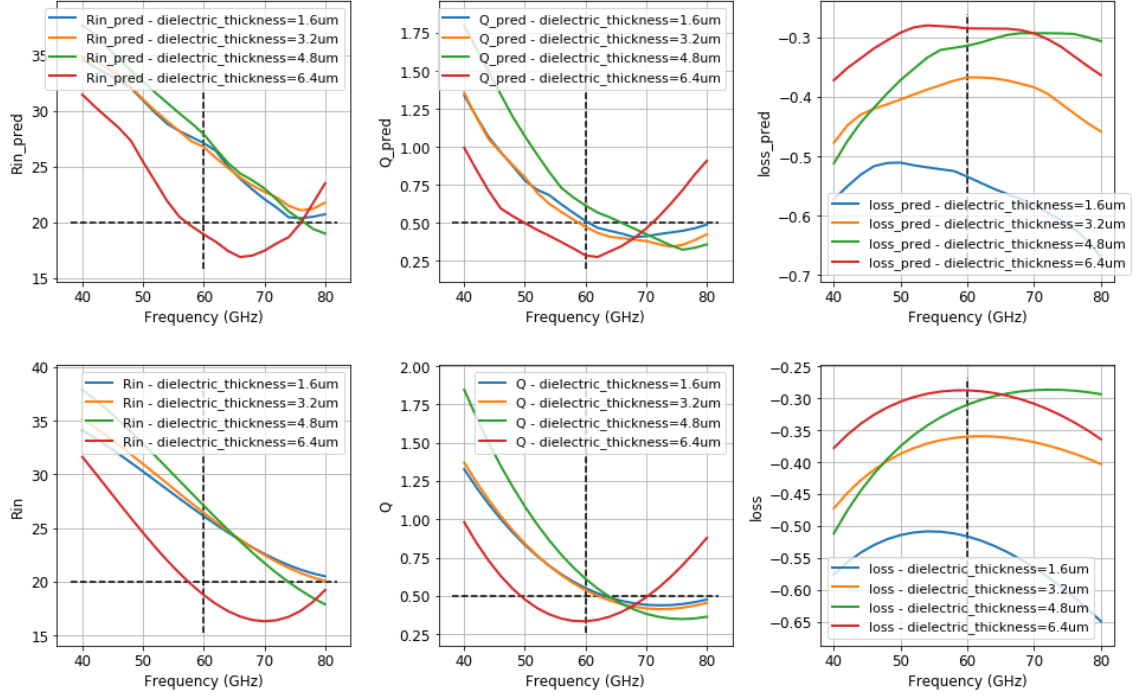
Figure 4.18 Automated results for impedance transforming baluns with Z_L=50Ω, Z_S=20Ω, and Q=0.5. The first row describes the predicted specification by the physical-electrical ML models, and the second row shows the actual physical-electrical results from commercial simulators.

4.3.5   Analysis

Developed from the lossless model of coupled lines, the indirect approach allows us to optimize physical dimensions for Impedance Transformation Baluns that achieve results that are close to desirable specifications. Demonstrated on multiple cases of baluns on various dielectric thicknesses, we verify that the proposed pipeline can effectively automate design tasks within the design time of seconds. Also, by comparing between the

predicted and actual results, we show that our pre-trained ML models can accurately predict the electrical performance over various ranges of frequency and design specifications. The approach also informs us about the realizable range of coupled lines when implementing on-chip. The low loss solution typically has even mode impedance less than 120Ω and the coupling factor less than 0.8.

Although we can leverage the theoretical analysis to automate EM structures in this indirect approach, the inherent drawback of this approach is the assumption of a lossless model, while the coupled lines undoubtedly exhibit metal loss when physically implemented on chips.

4.4   Automating the Design of Series-Connected Power Combiners

Having been the common and popular choice of designs to combine power at RF frequencies, series-connected Power Combiners have been frequently revisited at mm-wave ranges. However, researchers find it difficult to implement this structure at mm-wave bands, where much of the criticism is directed at the strong mm-wave capacitive coupling that distorts the impedance seen by active cores. Analyzing this structure in Chapter 2, we have showed that designs for series-connected power combiners exist at mm-wave frequency ranges, given that we must design the coupled lines asymmetrically and add phase-shifts at the inputs.

Advancing from the theoretical study, we will apply Machine Learning techniques and build automation algorithms to physically implement the design of series-connected Power Combiners in this section, where subsection 4.4.1 illustrates the automation problems and

our proposed solutions, and subsection 4.4.2 shows a design example of automating series-connected power combiners.

4.4.1 Automation Problems and Algorithms

Automation Problem: *Given the Z_L as the load impedance, Z_S as an optimum impedance seen by device, the loaded Q of the network, and the number of active cells (N_baluns) from which we want to combine the power, automate a full EM design of a Power Combiner with the lowest loss at the frequency of operation.*

Approaches
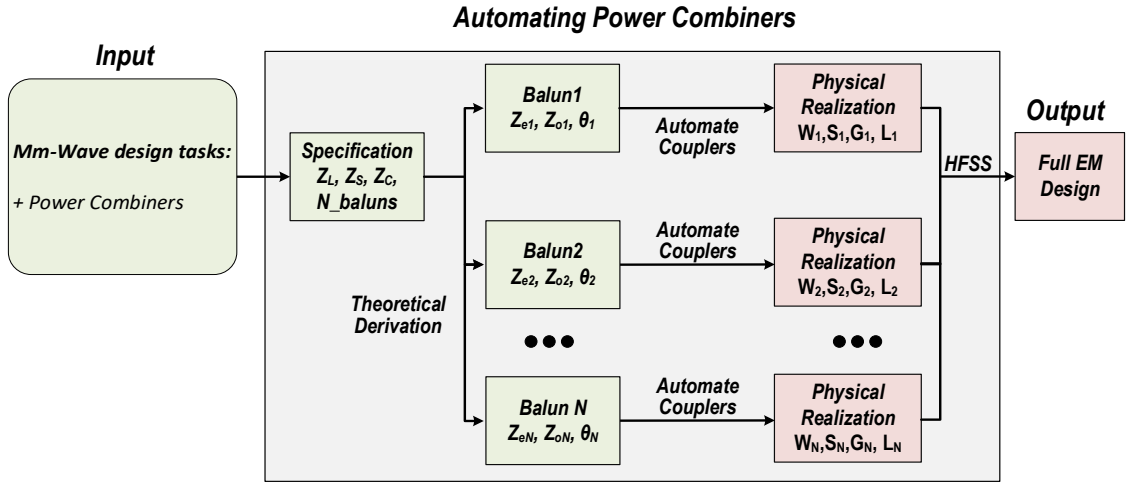
Figure 4.19 Proposed architectures to automate the design of Series-Connected Power Combiners.

Given the electrical specifications, we apply the theoretical analysis to compute the electrical parameters of all coupled lines (Z_e, Z_o, θ) for all active cells. We then convert from electrical properties to physical dimensions by the automation pipeline for couplers as presented in section 4.2. Among many sets of automated design, we select the design

that minimize the overall loss defined as the sum of the even-mode and odd-mode loss of all coupled lines.

Algorithms

Algorithm for Automating the Design of Series-Connected Power Combiners

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Compute N sets of coupled lines parameters that satisfy the specification of Power Combiners

Follow the pipeline for coupler design to convert to a list of possible physical dimensions

Select the design that minimizes the sum of even- and odd-mode losses for all coupled lines

Simulate the selected parameters with HFSS and generate S-parameters

4.4.2 Design Examples
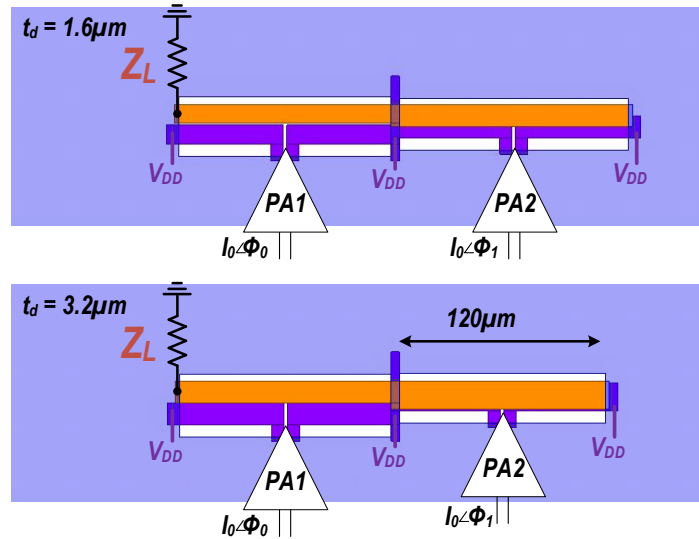
Figure 4.20 HFSS models for automated Power Combiners with two baluns, $Z_L=25\Omega$, $Z_S=30\Omega$, and Q=1.2.

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We demonstrate a design example for the case when $Z_L=25\Omega$, $Z_S=30\Omega$, Q=1.2, and

N_baluns=2. Numerical methods from Chapter 2 are used to extract the electrical

specification of two baluns, both of which have the same electrical length of 30°. With an

input phase difference of 90°, we calculate the electrical parameters of coupled lines as

$Z_{e1}=55.7\Omega$, $Z_{o1}=19.9\Omega$, $Z_{e2}=55.7\Omega$, and $Z_{o2}=7.11\Omega$. We then apply the physical optimizer

for the coupled line design to physically realize those values and select the design with the

lowest loss defined as the sum of the even-mode and odd-mode propagation loss for both

baluns. We depict the automated designs for the Power Combiners in Fig. 4.20 and the

electrical properties of those in Fig. 4.21. Generally, both differential cores see a resistive

impedance close to the desirable value of 30Ω and a series imaginary impedance close to

the desirable value of 0Ω, as we already absorb the parasitic capacitance inside the network.
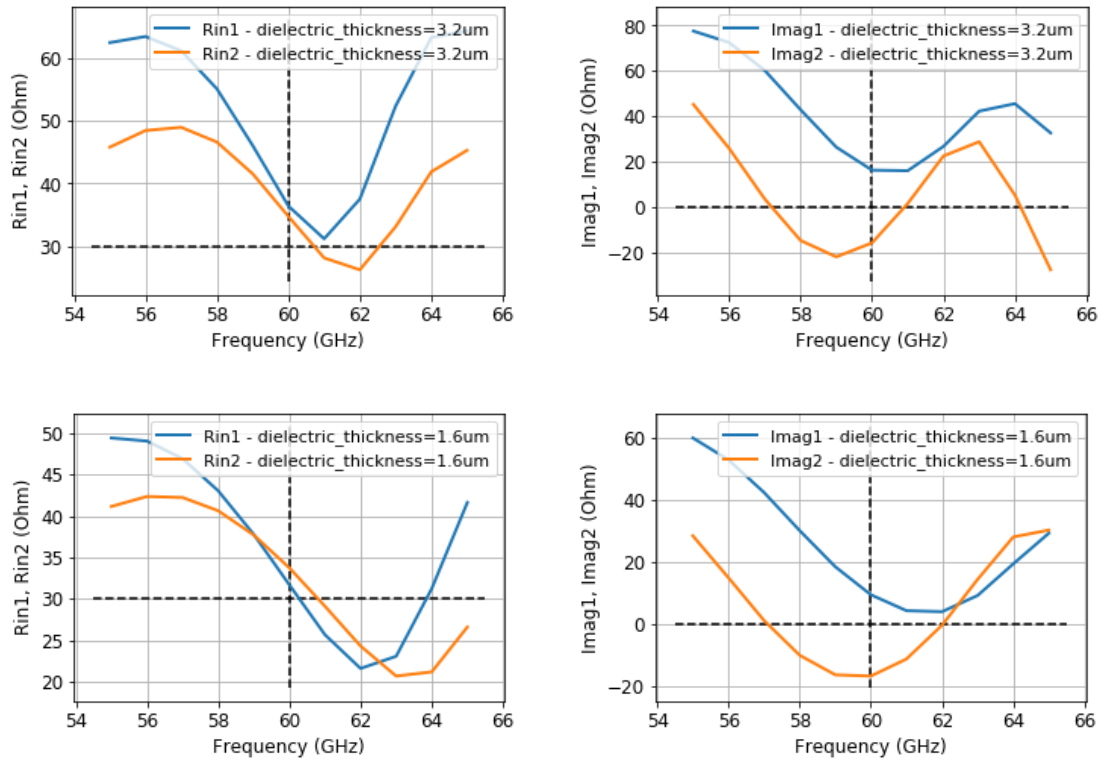
Figure 4.21 Automated results for Power Combiners with 2 baluns, $Z_L=25\Omega$, $Z_S=30\Omega$, and Q=1.2.

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4.5   Analysis

In this chapter, we made an assumption that the coupled lines are lossless such that we can mathematically convert from high-level electrical specifications to mid-level parameters of coupled lines and apply our physical optimizer for couplers to automate various design tasks. Indeed, this is the pipeline that engineers often use to design EM structures, and we follow a similar path but build new tools to reduce the design time to seconds. The automated results are encouraging, producing EM designs close to electrical specifications, but the mismatches still show the limitation of both the lossless assumptions and the typical pipeline that engineers often use to design EM structures.

To remove this lossless assumption, we will build more comprehensive ML models that learn electrical properties of actual simulated metal traces to account for all non-ideal effects. We will present the results of the approach without the lossless assumption in Chapter 5.

CHAPTER 5.   MACHINE LEARNING FOR AUTOMATING MM-WAVE DESIGNS – PART 2

In the previous chapter, we proposed several algorithms that employed the physical-electrical ML models for coupled lines to fully automate several mm-wave EM design tasks, such as Directional Couplers, Impedance Transforming Baluns, and Power Combiners. The major drawback is that the previous approaches assumed that coupled lines are lossless to compute mid-level electrical parameters from the high-level electrical specifications, which at times leads to automated solutions with marginal accuracies.

To resolve this challenge, in this chapter, we develop automation algorithms that leverage the physical-electrical ML models for baluns while incorporating actual metal loss in our optimization algorithm. We demonstrate that even without an intermediate step of mathematically analyzing EM structures, ML algorithms that can directly design Impedance Transforming Baluns, Out-Phasing circuits, and Doherty networks with both high accuracies and seconds-level design time. Overall, we complete the ML algorithms to fully automate all BCOD design tasks.

5.1   Automating the Design of Impedance Transforming Baluns – The Direct Approach

This section revisits the design of Impedance Transforming Baluns, but we apply the physical-electrical Machine Learning models for baluns to automate the design process in the "direct" approach. Unlike the "indirect" approach investigated in Chapter 4, the direct

approach incorporates loss in the coupled line models. To the best of our knowledge, this is the first work that comprehensively analyzes the loss of the on-chip baluns. We present our proposed algorithm in subsection 5.1.1 and demonstrate various automated examples for output baluns, input baluns for high-impedance devices, and input baluns for low-impedance devices in subsections 5.1.2-5.1.3 to verify the effectiveness of our proposed approach.

5.1.1   Automation Problems and Algorithms

Automation Problem: *Given the Z_L, Zs, Q as the load impedance, optimum impedance seen by device, and loaded Q of the network, automate a full EM design of an impedance transformation with the lowest loss at the frequency of operation.*
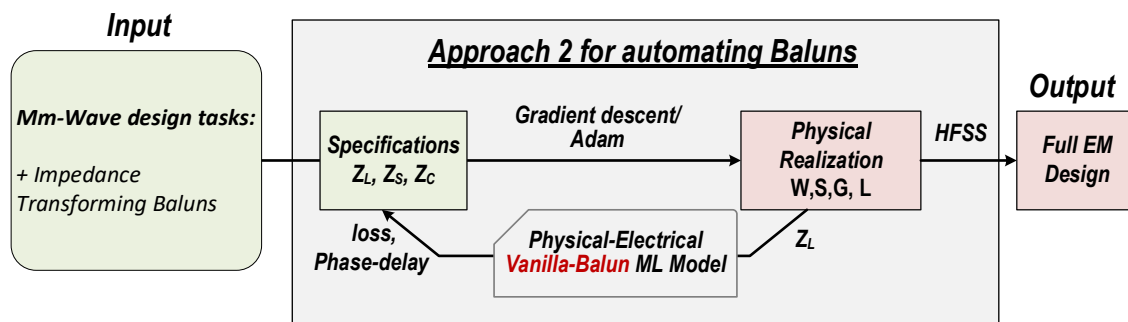
Approaches

Figure 5.1 Proposed direct approach to automate the design of Impedance Transforming Baluns.

Figure 5.1. illustrates our proposed approach to directly automate the design of an Impedance Transforming Baluns. Given a specification of an output load Z_L and the frequency of operation, we initialize multiple physical dimensions to formulate the input vectors for the balun ML models and from that compute the resulting Z_S (or R_{in}), C, Q, and

loss of those physical parameters. Subsequently, we compute the loss function, apply gradient descent and Adam optimizers to obtain the physical dimensions, and select the design with the lowest loss.

Loss Functions

For all the physical dimensions, the output impedance Z_L, and the frequency of operation, we compute the resistive impedance Z_S (or R_{in}) seen by the source, the capacitor C_{in} that the network resonates out, the quality factor Q of the baluns, and the passive loss associated with the path from inputs to outputs. The optimization loss is computed as the weighted mean absolute error between the predicted outputs and the desirable electrical labels, where the weights are inversely proportional to the values of electrical labels:

$$optimization\ loss\ =\ \sum_k \frac{|y_{pred} - y_{true}|}{|y_{true}|},$$

The ground truth value y_{true} includes the Z_S, C_{in}, and Q. The metal loss is computed as simply the passive loss of the structure:

$$metal\ loss\ =\ passive\ loss,$$

$$loss\ =\ optimization\ loss\ +\ metal\ loss$$

From the overall loss as the sum of optimization loss and the metal loss, we compute the gradient of the overall loss with respect to all physical parameters and apply gradient descent with Adam optimizers to update the physical dimensions to minimize the loss. Repeating the loop for 2000 iterations, we finalize the physical dimensions for N designs, select the one that has optimization loss below a certain threshold (typically 0.5) with the

lowest metal loss, and use HFSS to generate a full EM design and simulate the performance of the final design. The typical value for N is from 20-100, which is equivalent to attempting to design the baluns 20-100 times to select the structure with the lowest loss.

Algorithms

Overall, the algorithm to directly automate the design of Impedance Transforming Baluns is as follows:

Algorithm for Directly Automating the Design of Impedance Transforming Baluns

---

Randomly initialize N set of physical dimensions for N coupled lines as an N×4 vector

For step = 1, M do

Predict the Z_S, C_{in}, Q, and passive loss of the Impedance Transforming Baluns

Compute the optimization loss as the weighted mean absolute error between predicted outputs and desirable electrical labels. The weights are inversely proportional to the values of electrical labels.

Compute the gradient of the loss with respect to each physical parameter

Update N sets of physical dimensions by gradient descent with Adam update rules

Select the dimensions that have optimization loss less than threshold and achieves the lowest metal loss

Simulate the selected dimensions with HFSS and generate S-parameters

As discussed in Chapter 2, we need impedance transformation baluns in three common cases: at output networks, at input networks of high impedance devices (CMOS), and at input networks of low impedance devices (SiGe). To evaluate the effectiveness of this direct approach, we demonstrate three design examples as follows:

Design Specifications: *Design an impedance transforming balun at 60GHz for three different sets of specifications*

(1) *Output networks: $Z_L=50\Omega$, $Z_S=30\Omega$, Q=1.2*

(2) *CMOS input networks: $Z_L=50\Omega$, $Z_S=200\Omega$, Q=6*

(3) *SiGe input networks: $Z_L=50\Omega$, $Z_S=20\Omega$, Q=0.5*

The thickness of the metal can be 1.6μm, 3.2μm, 4.8μm, 6.4μm.

5.1.2   Design Examples for Output Baluns

The first example automates the design of Impedance Transforming Baluns for use at an output network with a specification of $Z_L=50\Omega$, $Z_S=30\Omega$, Q=1.2. Given the specification, we solve the physical dimensions over various physical lengths of the coupled lines and show the results in Fig. 5.2 with the Z_S (or R_{in}) and Q in the first row and the passive loss in the second row. The direct approach illustrates an excellent optimization loss, where both automated values for R_{in} and Q are close to the desirable specifications, with R_{in} ranging from 28-34Ω and Q ranging from 1.1-1.25 when the physical length ranges from 50-250μm. The passive loss curve in the second row of Fig. 5.2 demonstrates that the optimum physical length over various dielectric thicknesses for this design problem is approximately 80-110μm. Fig. 5.3 shows HFSS models with the optimum physical dimensions for the design tasks at various dielectric thickness. A common trend is that the

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automated algorithm widens the metal traces as the dielectric thickness increases to maintain the same coupling factor over various designs.

Figure 5.2 Automation results for the direct approach to design Impedance Transforming Baluns with Z_L=50Ω, Z_S=30Ω, and Q=1.2 over numerous physical lengths of baluns.

Next, the automation pipeline simulates the design with the lowest predicted passive loss with the HFSS software to obtain S-parameters files. In Fig. 5.4, we depict the predicted results from our pre-trained physical-electrical ML models for baluns in the first row and illustrate the actual results from commercial EM simulators in the second row. Both results are well correlated across the entire frequency range, demonstrating the

prediction accuracy of our ML models. The results show R_{in}=30-35Ω, Q=1.25-1.3 when Z_L=50Ω, which are identical to desirable electrical values. Overall, in a design time of less than 15 seconds, our proposed algorithms can fully automate EM designs of output baluns that both meet the specifications and achieve the lowest possible loss over various dielectric thicknesses.

Figure 5.3 HFSS models of automated EM designs with the direct approach for baluns with Z_L=50Ω, Z_S=30Ω, and Q=1.2.

Figure 5.4 Automated results for impedance transforming baluns with $Z_L=50\Omega$, $Z_S=30\Omega$, and Q=1.2. The first row describes the predicted specification by the physical-electrical ML models, and the second row shows the actual physical-electrical results from commercial simulators.

5.1.3   Design Examples for CMOS Input Baluns

The second example automates the design of Impedance Transforming Baluns for use at an input network of high impedance devices with a specification of $Z_L=50\Omega$, $Z_S=200\Omega$, Q=6. Figure 5.5 presents the results of the automation algorithm over various physical length of the coupled lines, all of which demonstrate automated baluns with R_{in} and Q close to the desirable values, with R_{in} ranging from 182-200Ω and Q ranging from 5-6 when the physical length ranges from 120-180µm. The realizable range for physical length in this design is much narrower than in the previous design example. Additionally, the smallest electrical lengths do not imply the lowest passive loss in this design example. As shown in

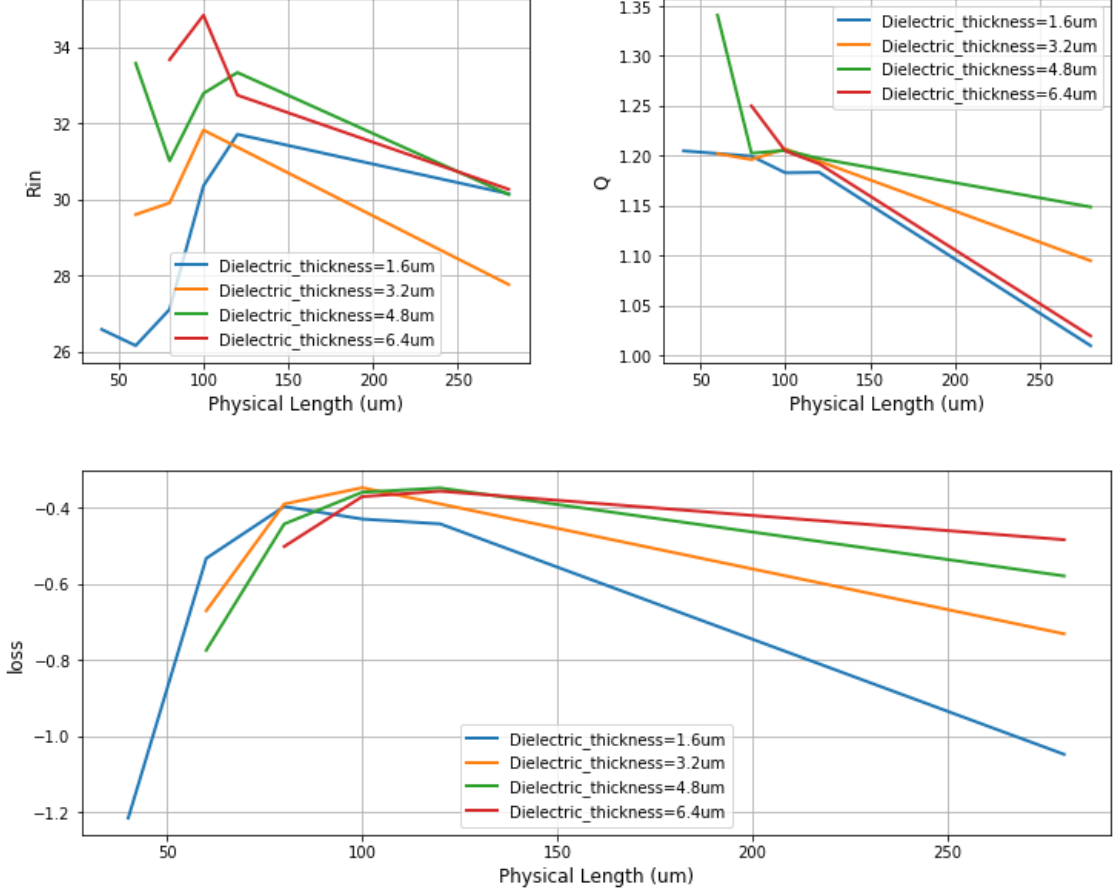the second row of Fig. 5.5, passive loss peaks at the highest physical length of the realizable ranges.
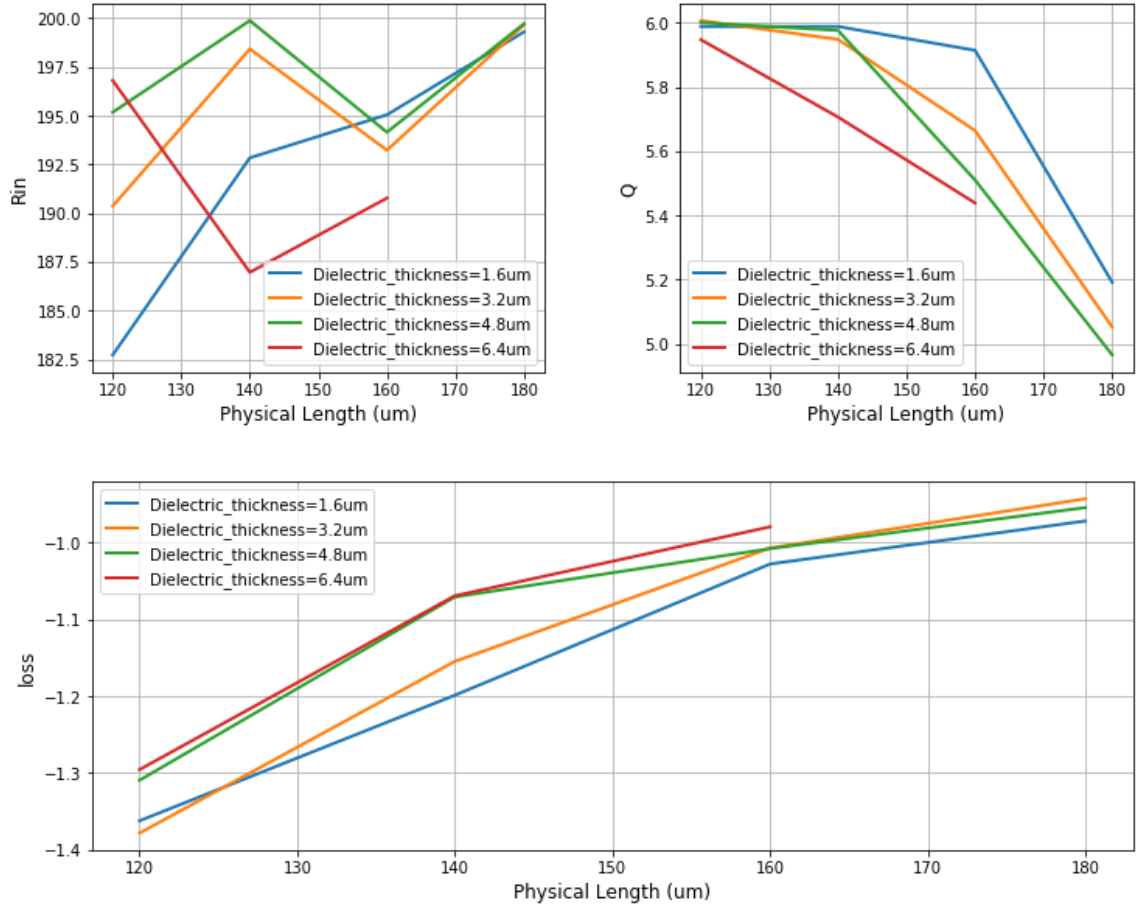
Figure 5.5 Automation results for the direct approach to design Impedance Transforming Baluns with $Z_L=50\Omega$, $Z_S=200\Omega$, and Q=6 over numerous physical lengths of baluns.
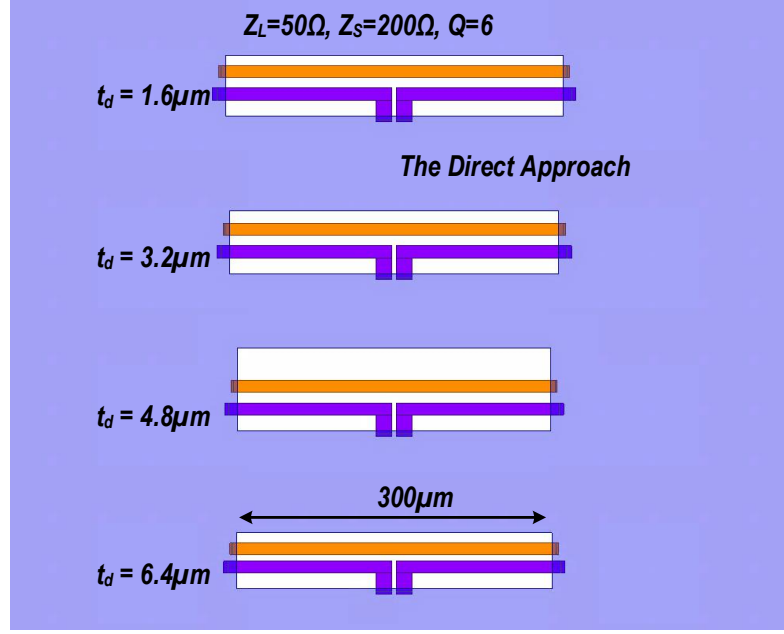
Figure 5.6 HFSS models of automated EM designs with the direct approach for baluns with $Z_L=50\Omega$, $Z_S=200\Omega$, and Q=6.

Figure 5.6 shows HFSS models with the optimum physical dimensions for the design tasks at various dielectric thicknesses. A common trend is that the automated algorithm moves two metal traces closer to each other as the dielectric thickness increases, so that the coupling factor over various designs can remain the same. Figure 5.7 depicts the predicted results from our ML models in the first row and the simulated results from commercial EM simulators in the second row. Both results are similar across the frequency bands, illustrating the high prediction accuracy of our ML models. The results demonstrate R_{in}=190-200Ω, Q=5.6-6 when $Z_L=50\Omega$, both of which are identical to the desirable values. Overall, within a design time of less than 15 seconds, the direct approach fully automates various high-quality input baluns for high impedance devices with both accurate electrical specifications and the lowest passive loss.
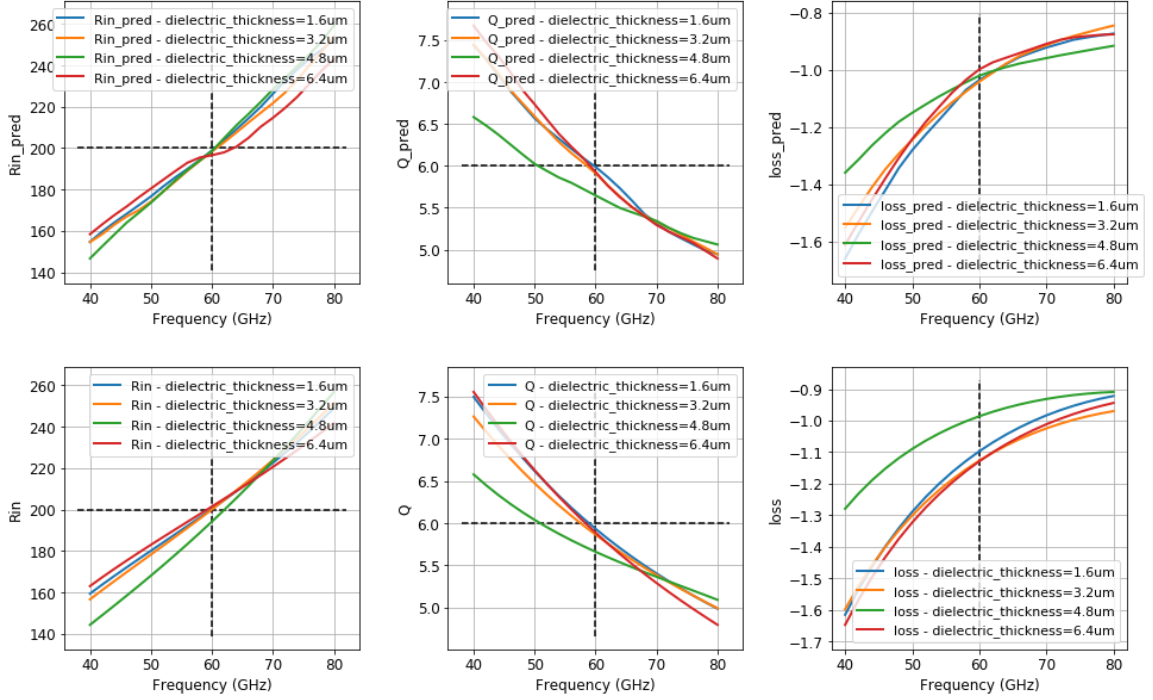
Figure 5.7 Automated results for impedance transforming baluns with $Z_L=50\Omega$, $Z_S=200\Omega$, and Q=6. The first row describes the predicted specification by the physical-electrical ML models, and the second row shows the actual physical-electrical results from commercial simulators.

5.1.4   Design Examples for SiGe Input Baluns

The third example automates the design of Impedance Transforming Baluns for use at an input network of low impedance devices, such as SiGe, with a specification of $Z_L=50\Omega$, $Z_S=20\Omega$, Q=0.5. Figure 5.8 details the results of the proposed algorithm when we fix various values of physical lengths, all of which illustrate automated baluns with R_{in} and Q close to the desirable values, with R_{in} ranging from 20-24Ω and Q ranging from 0.48-0.54 when the physical length ranges from 50-250µm.
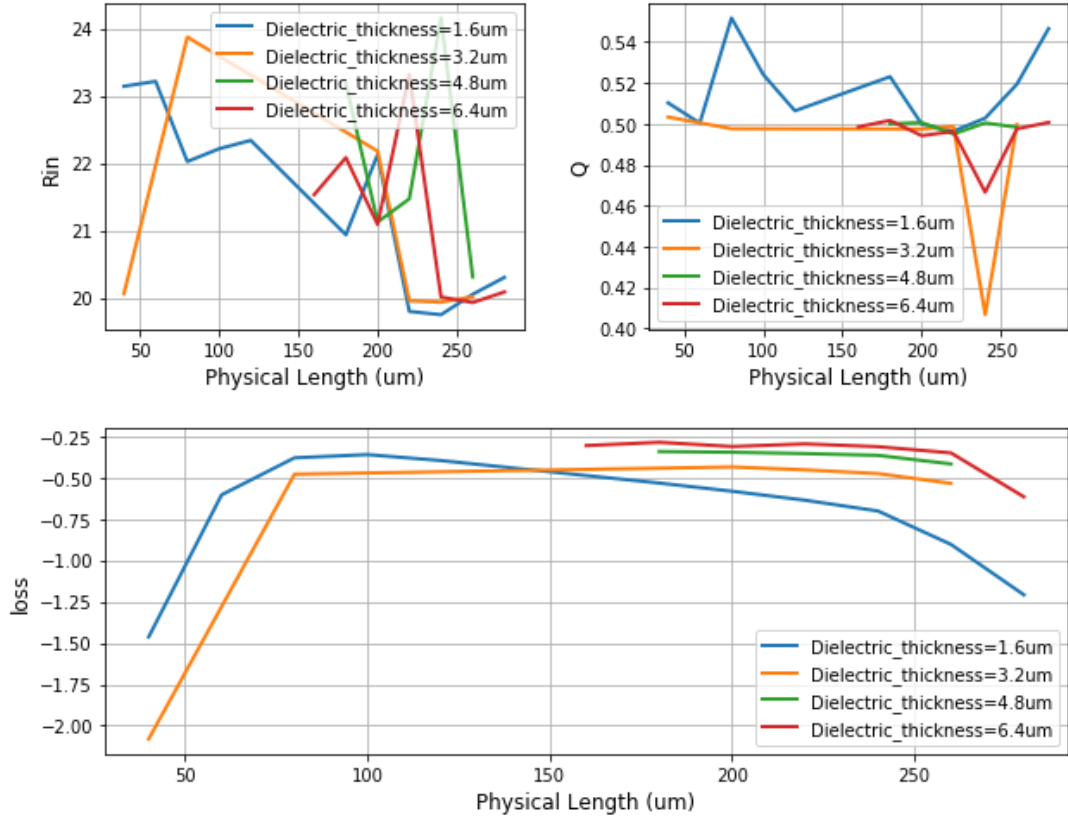
Figure 5.8 Automation results for the direct approach to design Impedance Transforming Baluns with $Z_L=50\Omega$, $Z_S=20\Omega$, and Q=0.5 over numerous physical lengths of baluns.

Interestingly, in this design of input baluns for low-impedance devices, we see two distinct modes, one for short physical lengths less than 100µm where solutions exist for dielectric thicknesses of 1.6µm and 3.2µm, and another for long physical lengths greater than 150µm where solutions exist for dielectric thicknesses from 3.2-6.4µm. The optimum physical dimensions shown in Fig. 5.9 illustrate these two modes. At a dielectric thickness of 1.6µm, the algorithm selects the short physical length, while at dielectric thicknesses from 3.2-6.4µm, the pipeline generates designs with longer physical lengths.
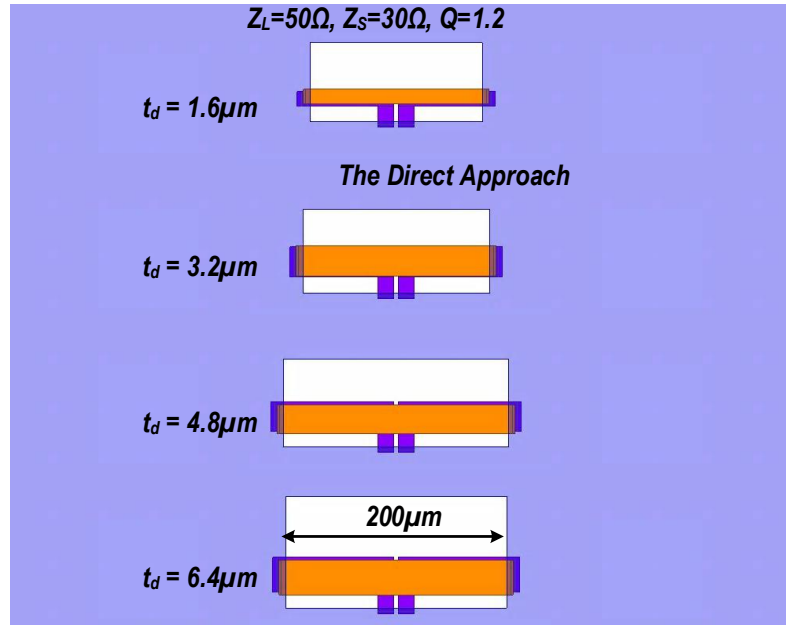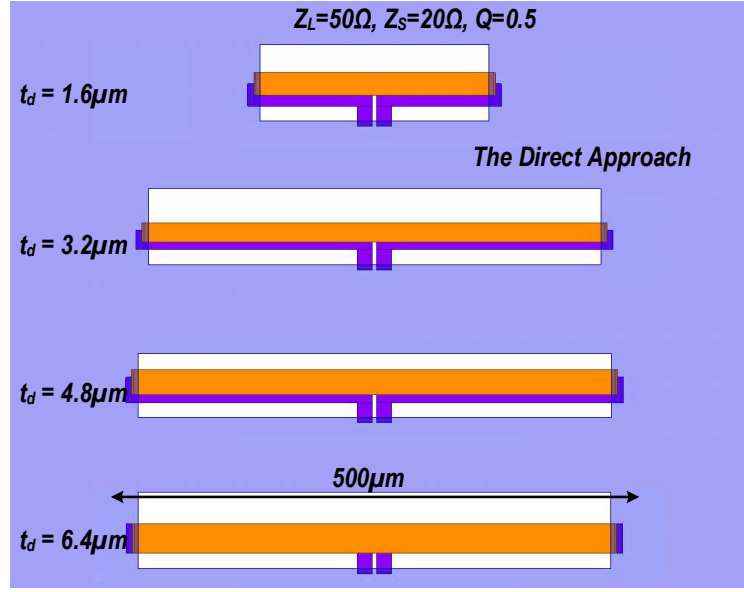
Figure 5.9 HFSS models of automated EM designs with the direct approach for baluns with $Z_L=50\Omega$, $Z_S=20\Omega$, and Q=0.5.
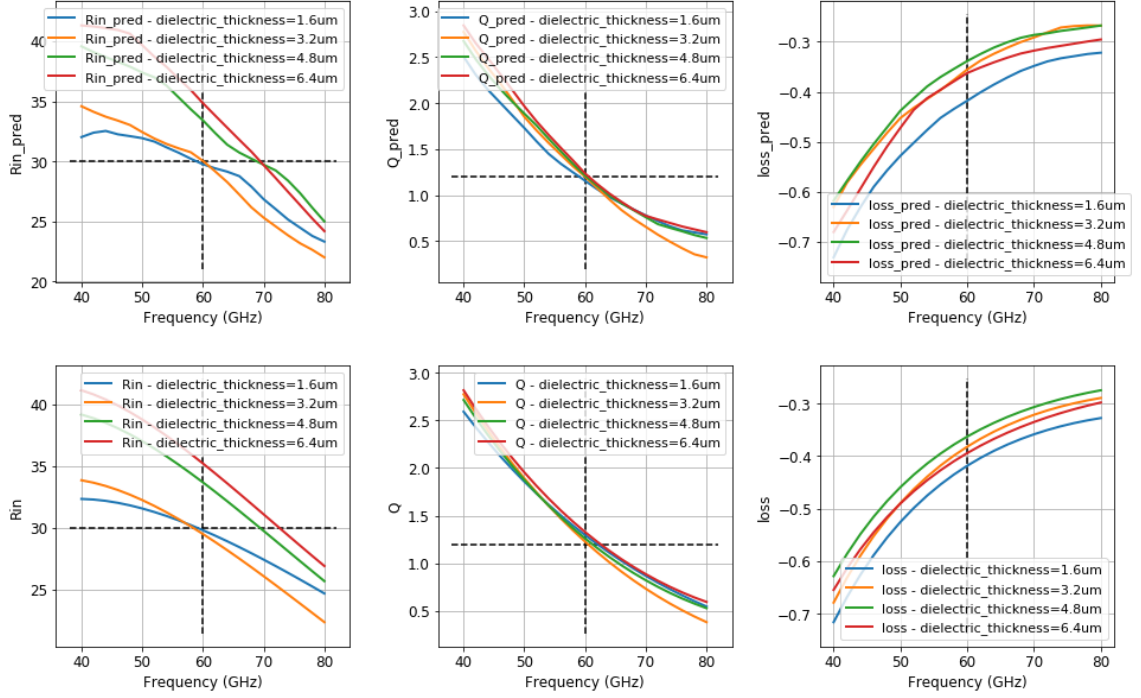
Describes in Fig. 5.10, both the predicted results from our ML models shown in the first row and the simulated results from commercial EM simulators illustrated in the second row exhibits similar responses over the entire frequency range, illustrating the high prediction accuracy of our ML models. We also see two distinct patterns of the response for two models. The results show R_{in}=20-24Ω, Q=0.5, both of which are close to the desirable specifications of R_{in}=20Ω, Q=0.5. Overall, within a design time of under 15 seconds, the proposed algorithm generates full EM designs that both fulfill the electrical specifications of various input baluns for low-impedance devices and achieve the lowest passive loss.
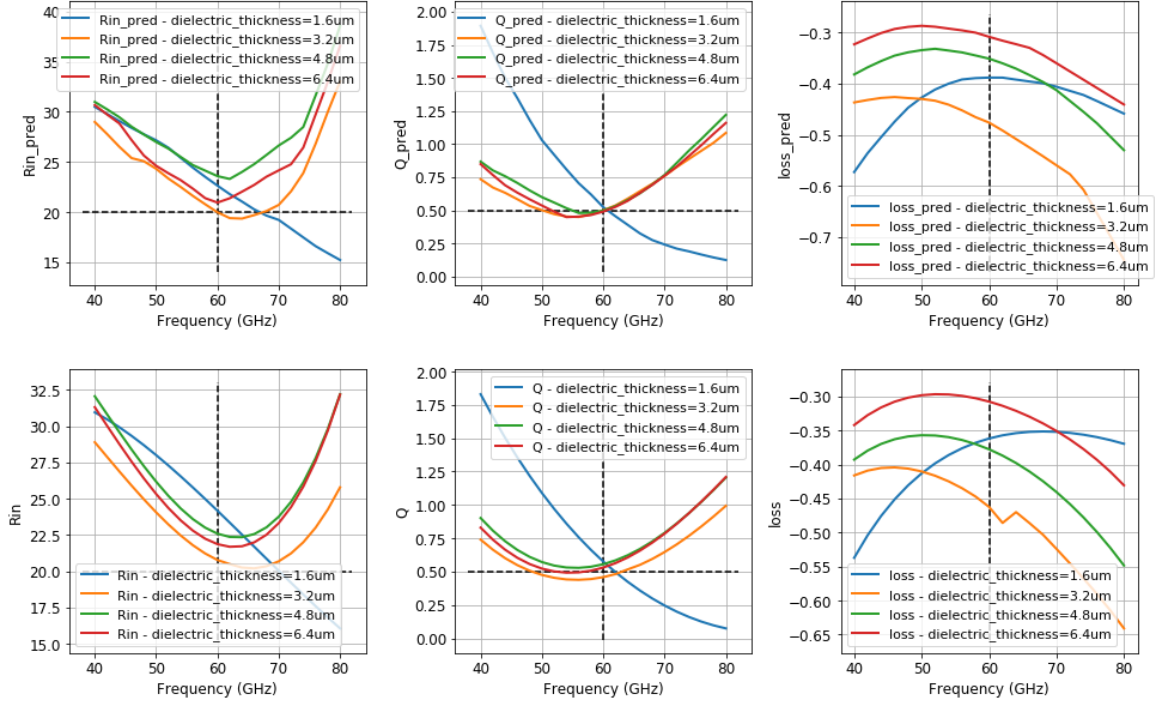
Figure 5.10 Automated results for impedance transforming baluns with $Z_L=50\Omega$, $Z_S=20\Omega$, and Q=0.5. The first row describes the predicted specification by the physical-electrical ML models, and the second row shows the actual physical-electrical results from commercial simulators.

5.1.5   Analysis

Several design examples with various electrical specifications and dielectric thicknesses verify the effectiveness of the ML approach. Within the design time of seconds, the algorithm generates full EM designs that yield electrical properties almost identical to the desirable specifications while demonstrating the lowest passive loss. Without effective ML models that accurately learn the physical-electrical relationships of baluns, those results might not be achievable.

We end this section with a thought about the automation algorithm. When gradually receiving more example S-parameter files for baluns, the learning algorithm eventually

understands the entire design space, and from that the algorithm can navigate directly from problems to solutions, or from the electrical specifications to physical dimensions, without any intermediate steps of analyzing what is actually inside the circuits. In other words, without any explicit analysis of the design space, the learning algorithm can still become a mastermind by just observing enough of discrete behaviors of this design space. We find this fact both interesting and fascinating.

5.2   Automating the Design of Out-Phasing and Doherty Networks

To improve the average mm-wave efficiency when transmitting modulated signals, researchers and engineers commonly use advanced mm-wave architectures, such as Out-Phasing circuits or Doherty networks. The current challenges to implement those architectures are still the Out-Phasing and Doherty EM structures that can actively modulate the load. In this thesis, not only have we proposed the theoretical solutions for the Out-Phasing and Doherty EM designs in Chapter 2, but we will also develop an automation algorithm that can physically realize those EM structures within a computational time of seconds. We first present the automation problem and our proposed algorithm in subsection 5.2.1 and then demonstrate automated design examples for Out-Phasing circuits in subsection 5.2.2 and Doherty network in subsection 5.2.3.

5.2.1   *Automation Problems and Algorithms*

Automation Problem: *Given the Z_L, Z_s, Q as the load impedance, optimum impedance seen by device, and loaded Q of the network, automate a full EM design of an Out-Phasing or Doherty EM network with the lowest loss at the frequency of operation.*
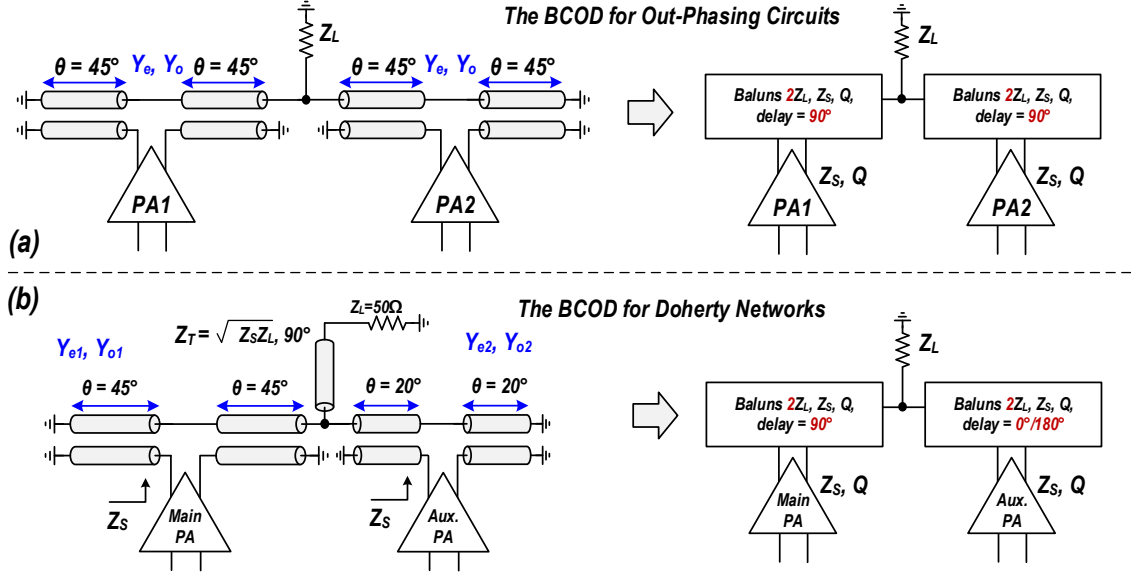
Figure 5.11 The BCOD structures for (a) Out-Phasing circuits (b) Doherty networks.

Approaches

In chapter 2, we theoretically solved the BCOD structure for Out-Phasing circuits and Doherty networks and proposed explicit parameters for theoretical EM circuits that satisfy the design specifications for arbitrary values of Z_L, Z_S, and Q. One possible way to automate the EM designs is to follow the indirect approach presented in Chapter 4, by assuming that the coupled lines are relatively lossless, utilizing mathematical analysis to convert electrical specifications to mid-level parameters, and leveraging the ML models for coupled lines to indirectly compute physical dimensions.

Interestingly, given more comprehensive ML models of vanilla baluns, we can directly automate the Out-Phasing and Doherty networks without explicitly analyzing mid-level parameters of coupled lines inside the baluns. As demonstrated in Fig. 5.11, we only need to automate two baluns, one with $2Z_L$, Z_S, Q, and phase delay=90°, and another with $2Z_L$,

Z_S, Q, and phase delay=0°/90°, to construct the full EM designs of Out-Phasing and Doherty EM networks. We visualize our proposed approach to automate the designs tasks as in Fig. 5.12.
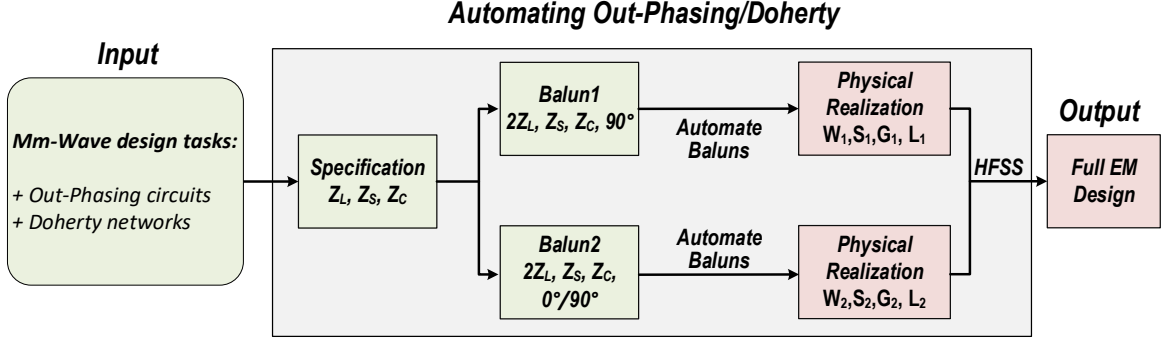
Figure 5.12 Proposed architectures to automate the design of Out-Phasing circuits and Doherty networks.

Loss Functions

Both balun 1 and 2 in Fig. 5.12 have optimization loss and metal loss:

$$optimization\ loss_{1,2} \ = \ \sum_{k,\{1/2\}} \frac{\left|y_{pred} - y_{true}\right|}{\left|y_{true}\right|},$$

$$metal\ loss_{1,2} = passive\ loss_{1,2},$$

The overall loss is the sum of the optimization loss and the metal loss:

$$loss_{1,2} = optimization\ loss_{1,2} + metal\ loss_{1,2}$$

In common with the previous automation algorithms, we employ the multi-initialization for the physical dimensions, which is equivalent to attempting to design the structure multiple times. Among all the generated designs, we choose those with optimization loss

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smaller than a certain threshold, which typically we set to 0.6, and select the remaining design with the lowest metal loss.

Algorithms

Overall, the algorithm to fully automate the design of Out-Phasing circuits and Doherty networks is as follows:

Algorithm for automating the Design of Out-Phasing Circuits and Doherty Networks

Automate the design of balun1 with the specification $2Z_L$, Z_S, Q, and phase delay = 90°

If designing Doherty structures:

Automate the design of balun2 with $2Z_L$, Z_S, Q and the phase delay = 0°/180°

Else if designing Out-Phasing structures:

Keep balun2 the same as balun1

Utilize the balun automation to design balun1 and balun2

Simulate the selected parameters with HFSS and generate S-parameters

5.2.2 Design Examples for Out-Phasing Circuits

This subsection presents an example of designing an Out-Phasing network for a specification Z_L=50Ω, Z_S=30Ω, and Q=1. Applying the automation algorithm presented in subsection 5.2.1, we automate the Out-Phasing EM structures over various dielectric thicknesses and show the finalized HFSS models of those automated designs in Fig. 5.13.

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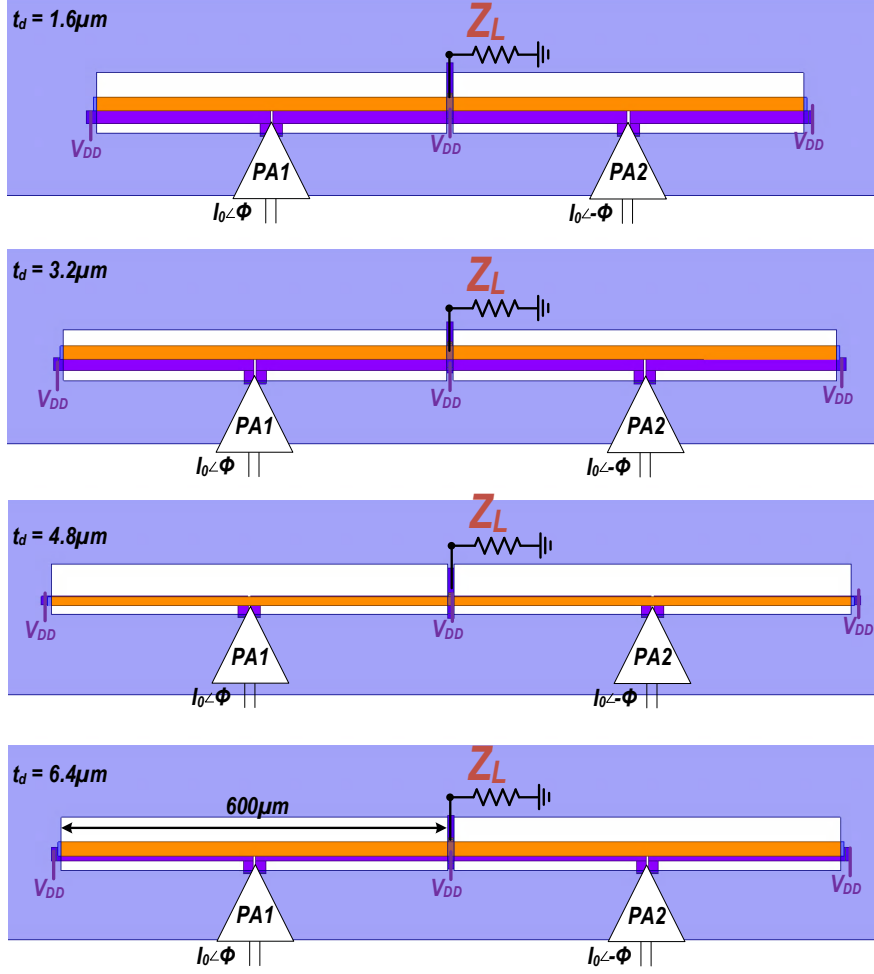
Figure 5.13. Automated designs for Out-Phasing circuits with specifications Z_L=50Ω, Z_S=30Ω, and Q=1 over various dielectric thicknesses. The Chirex compensation is not included for simplicity.

Ideally, the active load modulation curves of Out-Phasing should follow:

$$R_p = \frac{Z_S}{cos^2(\phi)}$$

where ϕ is the Out-Phasing angle. From the simulated HFSS results, we apply the Out-Phasing input signals to our automated design, plot the active load modulation curves as functions of Out-Phasing angles, and compare with the idealistic Out-Phasing response in Fig. 5.14. The Out-Phasing active load modulation curves for our automated design closely

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track the idealistic response, demonstrating that we accurately generate EM designs for Out-Phasing circuits over various dielectric thicknesses. We also depict the passive loss of the automated designs in Fig. 5.15, where the best Out-Phasing design exhibits a small loss from -0.9dB to -0.5dB across all Out-Phasing angles.
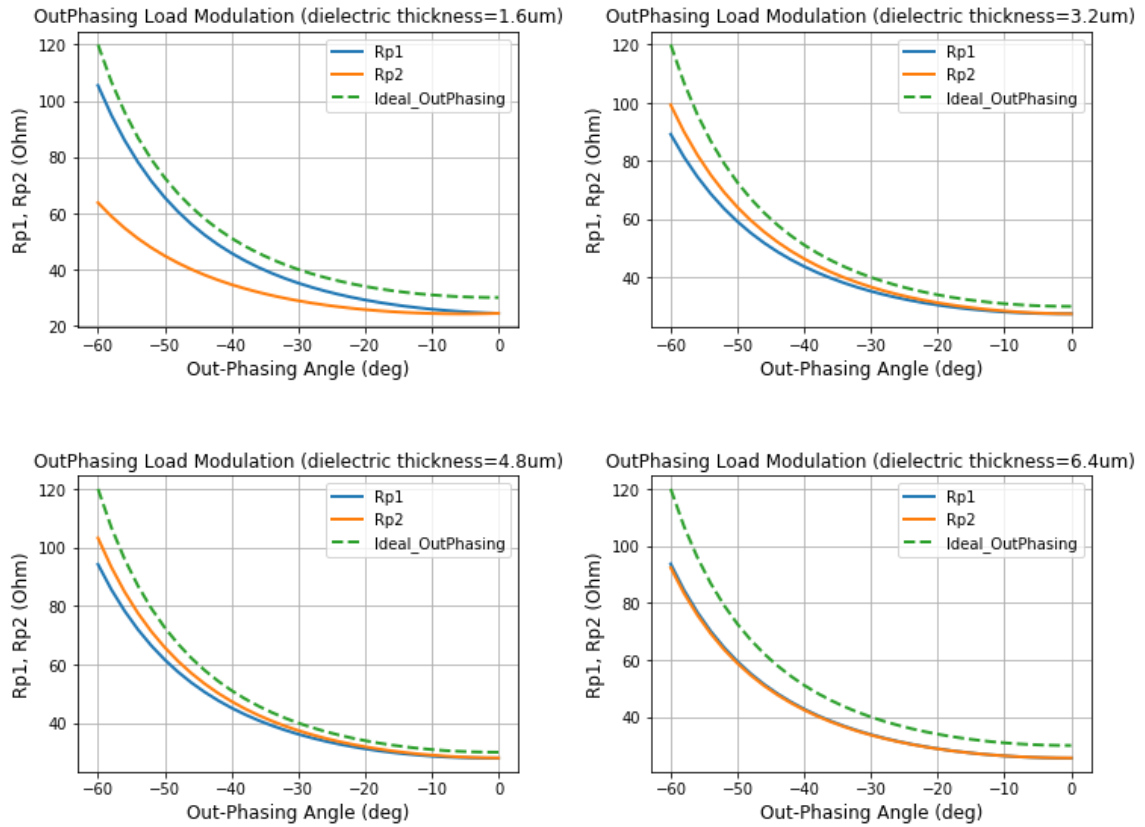
Figure 5.14 Active Load Modulation curves for the automated Out-Phasing designs over various dielectric thicknesses.
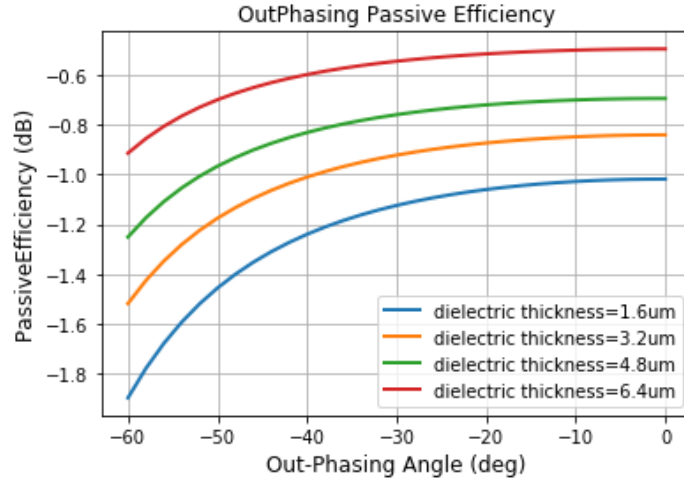
Figure 5.15 Passive Efficiency curves for the automated Out-Phasing designs over various dielectric thicknesses.

5.2.3   Design Examples for Doherty Networks
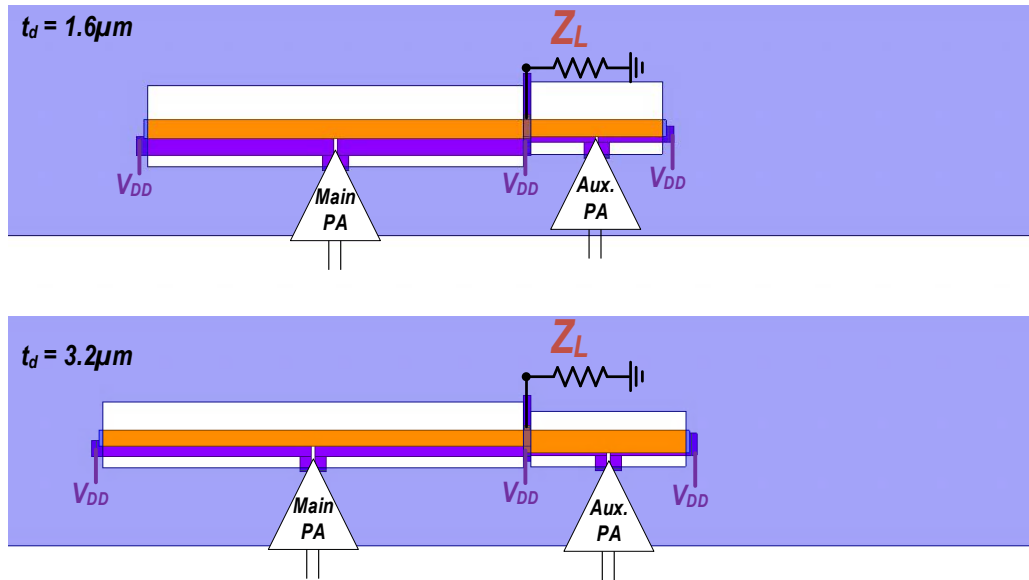
Figure 5.16 Automated designs for Doherty circuits with specifications Z_L=30Ω, Z_S=30Ω, and Q=1.

Next, we present an example of designing a Doherty network with $Z_L=30\Omega$, $Z_S=30\Omega$, and Q=1. For simplicity, we assume that we implement both Main and Auxiliary baluns on the same dielectric thickness. Employing the algorithm presented in subsection 5.2.1, within a design time of less than 15 seconds, we complete the automated EM designs of Doherty structures and display the HFSS models of those automated Doherty networks in Fig. 5.16. For this electrical specification, balun 2 requires a strong coupling factor, such that the solutions only exist at dielectric thicknesses of 1.6-3.2μm.

From the simulated S-parameters of HFSS models, we plot the active load modulation curves of the automated Doherty design in Fig. 5.17 and the passive loss over normalized input voltage in Fig. 5.18. The automated EM structures also exhibit low passive loss from -0.9dB to -0.5dB for a 3.2μm dielectric thickness over the entire Doherty operation. Additionally, the active load modulation curves shown in Fig. 5.17 closely track the idealistic Doherty response, demonstrating the Doherty functionality of the automated designs and the effectiveness of our proposed algorithm.
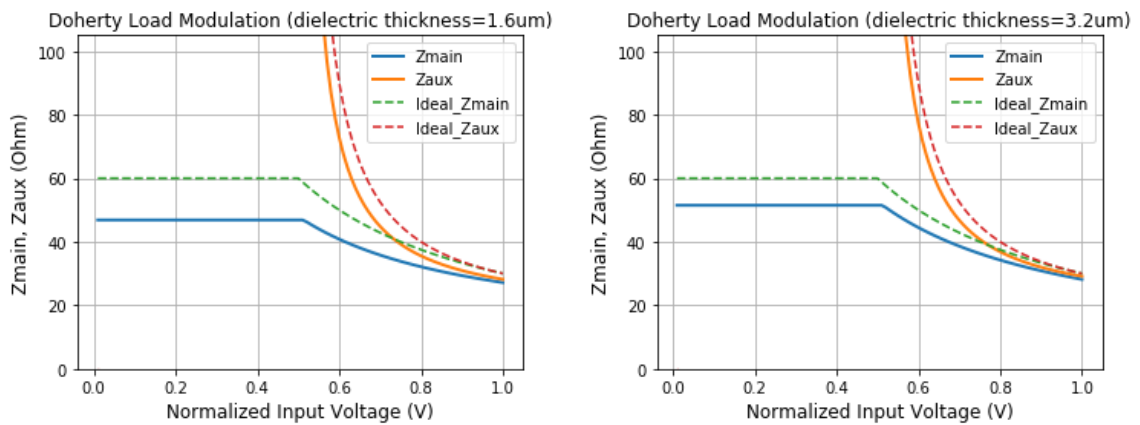
Figure 5.17 Active Load Modulation curves for the automated Doherty designs over various dielectric thicknesses.
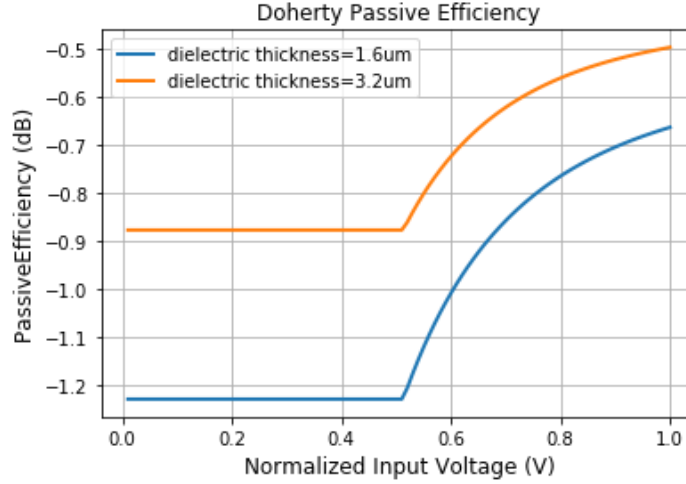
Figure 5.18 Passive Efficiency curves for the automated Doherty designs over various dielectric
thicknesses.

5.3 Analysis

Chapter 4-5 presents our proposed Machine Learning approach to fully automate EM designs for the BCOD tasks. From a number of design examples for many critical EM structures, we verify that our proposed automation algorithm can both generate EM designs that fulfill the electrical specifications with the lowest loss and can complete all design tasks within a computational time of seconds. Notably, we directly optimize all EM structures for the lowest metal loss. We are not aware of any existing approach that can systematically optimize this critical parameter.

The main motivation to develop automated algorithms is to resolve the drawbacks of the current approach used to design EM structures, which is time-consuming, labor intensive, and involves high variance in the quality of designs. While the current approach is effective if the designers have enough experience to complete the design within a small

number of iterations, we believe that adding the Machine Learning dimension to existing EM methods can lead to fruitful results.

Current Approach to design EM   **Proposed Approach to design EM**

✓ *Good: if designers have enough of experience to get the design Done within few iterations*

? *Somebody has to collect + share the data*

✗ *Time Consuming + Labor Intensive*

✓ *(Super) Fast*

✗ *High Variance in Design Quality*

✓ *Reliable*

✓ *Has the answer for metal loss*

✓ *Is a tool for bigger optimization loop/ higher level questions*

Figure 5.19 Comparison between the current and our proposed approach to design EM structures.

We compare the current and our proposed approach to design EM structures in Fig. 5.19. Obviously, someone must collect and share the data used to train ML models, but the rest of our automated algorithm is generic and can be readily applied to any new automation problems. First, the proposed approach to design EM structures can be super-fast, where we have drastically reduced the design time from days-weeks-months to seconds. Second, the automated algorithm can be ultra-reliable because it does not depend on any subjective judgements to update physical parameters. The current approach might lead to EM structures with varying qualities over various attempts to design, but our proposed approach can compute similar optimum solutions every time we run the algorithm. Third, the Machine Learning approach to design EM allows the incorporation of the metal loss, which is arguably one of the most critical parameters for EM designs, and we are not aware

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of any other approaches that can address the metal-loss challenge. Lastly, we find both interesting and fascinating that our proposed Machine Learning techniques can be a tool for bigger optimization loops to resolve higher level mm-wave questions, which we will analyze in Chapter 6.

CHAPTER 6.   MACHINE LEARNING REVEALS BIGGER PICTURES

In previous chapters, we develop the Machine Learning models that accurately predict electrical properties from physical dimensions and formulate various algorithms that can fully automate EM designs for numerous mm-wave EM design tasks. To further advance the concepts, in this chapter, we will apply our Machine Learning techniques as a tool for more general optimization problems and from that present our answers for several challenging, abstract, high-level questions of mm-wave designs.

6.1   Introduction

A Machine Learning model that both accurately, reliably, and quickly computes electrical properties from physical dimensions can be highly useful even beyond the application of automating EM structures. In this chapter, we will apply the ML approach to resolve several high-level and abstract questions of mm-wave designs.

First, one of the major questions for mm-wave engineers when working on a new process at a new frequency band is to select the optimum size for the mm-wave transistors at the last stages of transmitter chains. The reason is that knowing this optimum size can help evaluate the upper limits of electrical performance, such as power or efficiency, of the entire mm-Wave system at a particular frequency. We present our approach to address this question in section 6.2.

Second, the well-known rule of thumb in mm-wave designs is that we must use a smaller device for a higher mm-wave frequency, but to the best of our knowledge, the relationship

between device and frequency remains abstract, and none of the existing publications can quantify this relationship. Utilizing the ML approach, we attempt to answer this high-level question in section 6.3.

Third, not all electrical specifications for the BCOD structure can be physically realized on chip, even when the theoretical Microwave circuits for those specifications exist. To evaluate the practicality of realizing the theoretical solutions, we use the ML algorithms to study the implementable specifications of several BCOD designs in section 6.4.

6.2   The Optimum Transistor Size

One of the critical questions for mm-wave designers is to choose an optimum size for mm-wave devices for a given process. We pay special attention to the devices at the last stage of Power Amplifiers since those devices determine the overall power and efficiency of the entire transmitter systems. Also, we define the concept of "optimum" as the value that results in the highest power or efficiency performance. The optimum value of device sizes is an abstract question for mm-wave designs, for which engineers frequently employ the trial-and-error technique to resolve but often does not have a conclusive answer. Interestingly, the Machine Learning techniques we propose can mathematically quantify this abstract question with an assumption that we work with differential mm-wave architectures.

All mm-wave devices exhibit a device parasitic capacitance C and a load-pull impedance R_{in}. When we double the device size, the parasitic capacitance C doubles while the load-pull impedance R_{in} reduces by half, thus the quality factor $Q = 2\pi f C R_{in}$ remains relatively constant. If the given device size has a parasitic capacitance C, the optimum

impedance would be $R_{in} = Q/2\pi f C$. With the assumption of differential architectures, we must design an impedance transforming balun that transforms from Z_L to R_{in} and resonates out this parasitic C. We utilize the proposed ML algorithm developed in previous chapters to optimally automate baluns with the electrical specification of Z_L, R_{in}, and C. By comparing the performance of those automated balun designs, we can deduce the optimum value of parasitic capacitance C, or in other words, the optimum size for mm-wave devices.
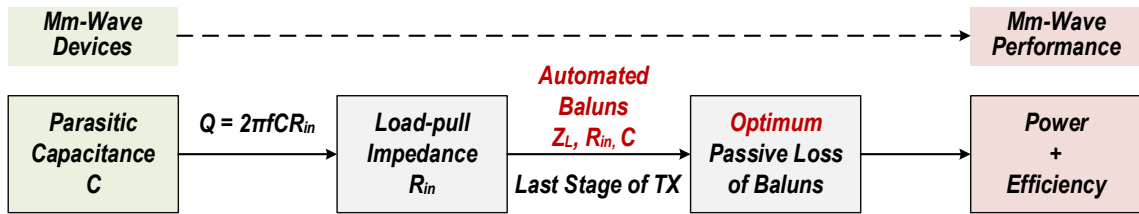
Figure 6.1 Computational process from the transistor device with a parasitic capacitance C to the high-level mm-wave power and efficiency performance. The proposed ML approach allows us to directly evaluate mm-wave performance when given the size of mm-wave devices.

We summarize the computational process that can answer the high-level question of the optimum device size in Fig. 6.1. As an illustration, we mathematically solve this abstract question on a metal stack that supports dielectric thickness ranging from 1.6µm-6.4µm, an on-chip process with a loaded Q=1, an output load of 50Ω, and a frequency of operation of 60GHz. Without any assumption on the size of transistors, we study all possible sizes of on-chip devices. Particularly, we sweep the parasitic capacitance C from 5fF-300fF with 5fF incremental steps, which represents various transistor sizes, automate the optimum impedance transformation balun for each value of C, and describe the results of optimum baluns in Fig. 6.2. The left column illustrates the passive loss, while the right column shows the optimum physical dimensions for length and width of metal traces.
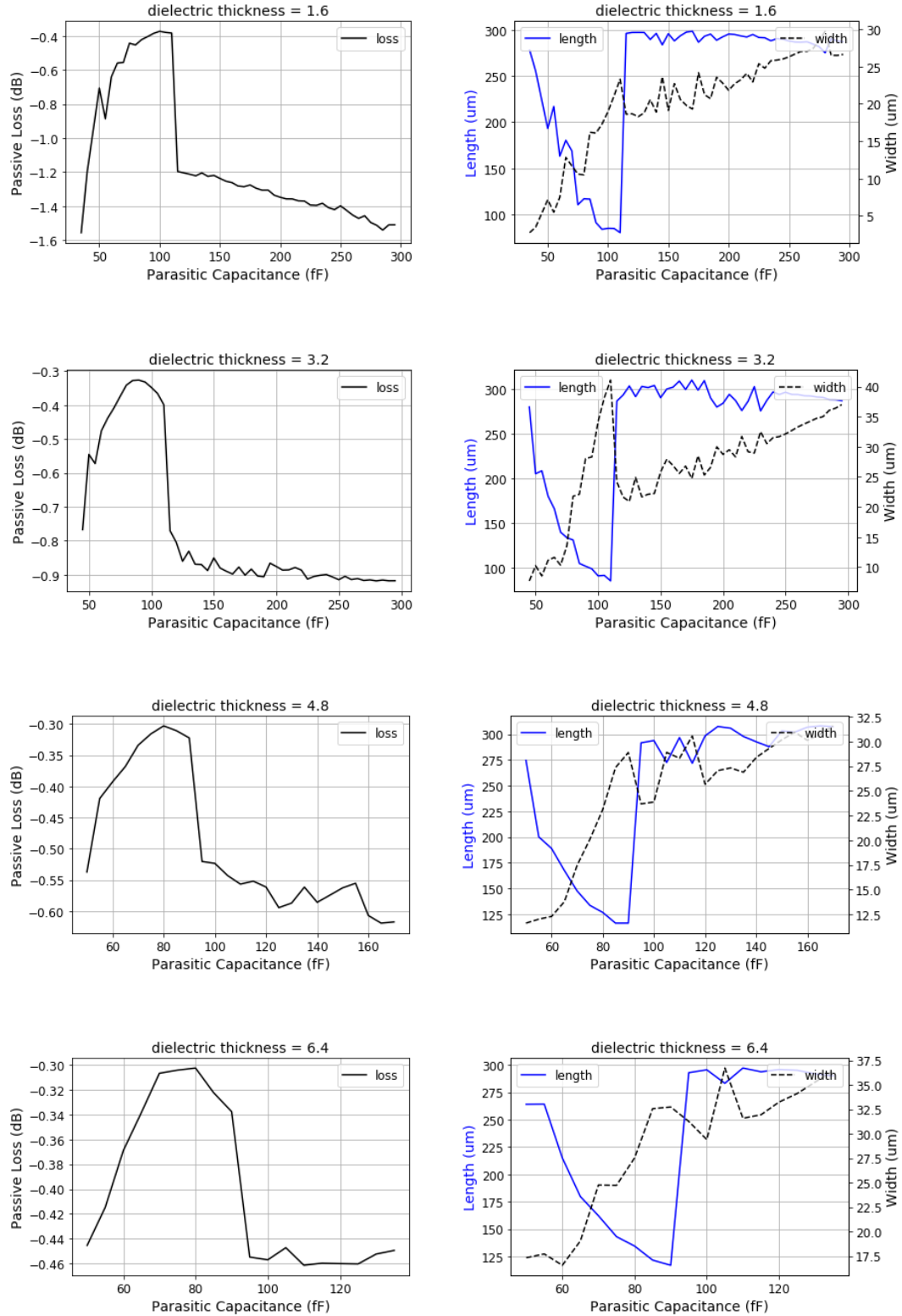
Figure 6.2 Performance of the optimum output baluns at 60GHz over the values of parasitic capacitance for

a process with loaded Q=1 over several dielectric thicknesses.

Following the current approach to design EM structures, we might not be able to compute the best dimensions for each parasitic capacitance value. The reason is that the current approach involves high variance in the final quality of design and provides no systematic evidence about achieving the optimum physical dimensions even for a single device size. However, the proposed ML algorithms can reliably complete the optimum EM parameters within a computational time of seconds for each value of C, consequently allowing us to efficiently resolve the bigger optimization questions. Demonstrated by the optimization results in Fig. 6.2, we learn that in order to design mm-wave systems with highest efficiency at 60GHz, the optimum device size has a parasitic capacitance ranging from 80fF-100fF because those devices allow the output baluns to exhibit the lowest passive loss.

We also analyze the results in Fig. 6.2 in several other aspects. First, after running the ML algorithm, we see the curves exhibit sharp changes at C=120fF or 90fF for dielectric thickness 1.6µm-3.2µm or 4.8µm-6.4µm. This sharp change illustrates the strategy that the ML algorithm thinks is optimum. At a low value of parasitic capacitance C, the strategy to design an optimum balun is to reduce the physical length and widen the metal width when the value of parasitic capacitance C increases. When the value of C exceeds certain thresholds, this strategy no longer yields solutions, and the next strategy is to set the physical length to around 300µm or 45°electrical length to optimally design baluns for higher ranges of parasitic capacitance C.

Second, the results again illustrate a trade-off when selecting the metal layers, or the dielectric thickness, to implement the EM structures. Smaller values of dielectric thickness can support EM solutions for a wider range of mm-wave devices, while higher values of

dielectric thickness often imply lower loss. For example, the dielectric thickness of 1.6µm exhibits the best loss of -0.4dB and can support mm-wave devices with 45fF-300fF parasitic capacitance, while the dielectric thickness of 6.4µm exhibits the best loss of -0.3dB and can support mm-wave devices with 50fF-135fF parasitic capacitance, as shown in the first and last row of Fig. 6.2.

6.3   The Rule of Thumb between Device Sizes and Frequencies

The rule of thumb in mm-wave designs is to use smaller mm-wave devices for higher mm-wave frequencies. However, how to express this rule of thumb in mathematical values remains an elusive question for the mm-wave community. To the best of our knowledge, we are not aware of any prior works can answer this fundamental relationship.

To a certain extent, this rule of thumb is an advanced version of the optimum device question addressed in section 6.2, which we expand from a single frequency as considered in section 6.2 to the entire mm-Wave frequency ranges in this section. With an assumption of a differential architecture, at each frequency, we calculate the optimum device size over various values of the loaded Q and the metal stack size and plot the results over the mm-Wave frequencies ranging from 25-80GHz in Fig. 6.3. The left column depicts the mm-wave device parasitic capacitance and frequencies, and the right column shows the best passive loss when we design baluns at various frequencies. We mathematically compute the high-level and abstract relationship between device size and frequencies, and the computation demonstrates the inverse relationship in all the cases as shown in Fig. 6.3. Interestingly, the ML approach also reveals the trade-off between power and efficiency,

because higher loaded Q values support larger device sizes to increase output power but results in higher passive loss or decreased efficiency, and vice versa.
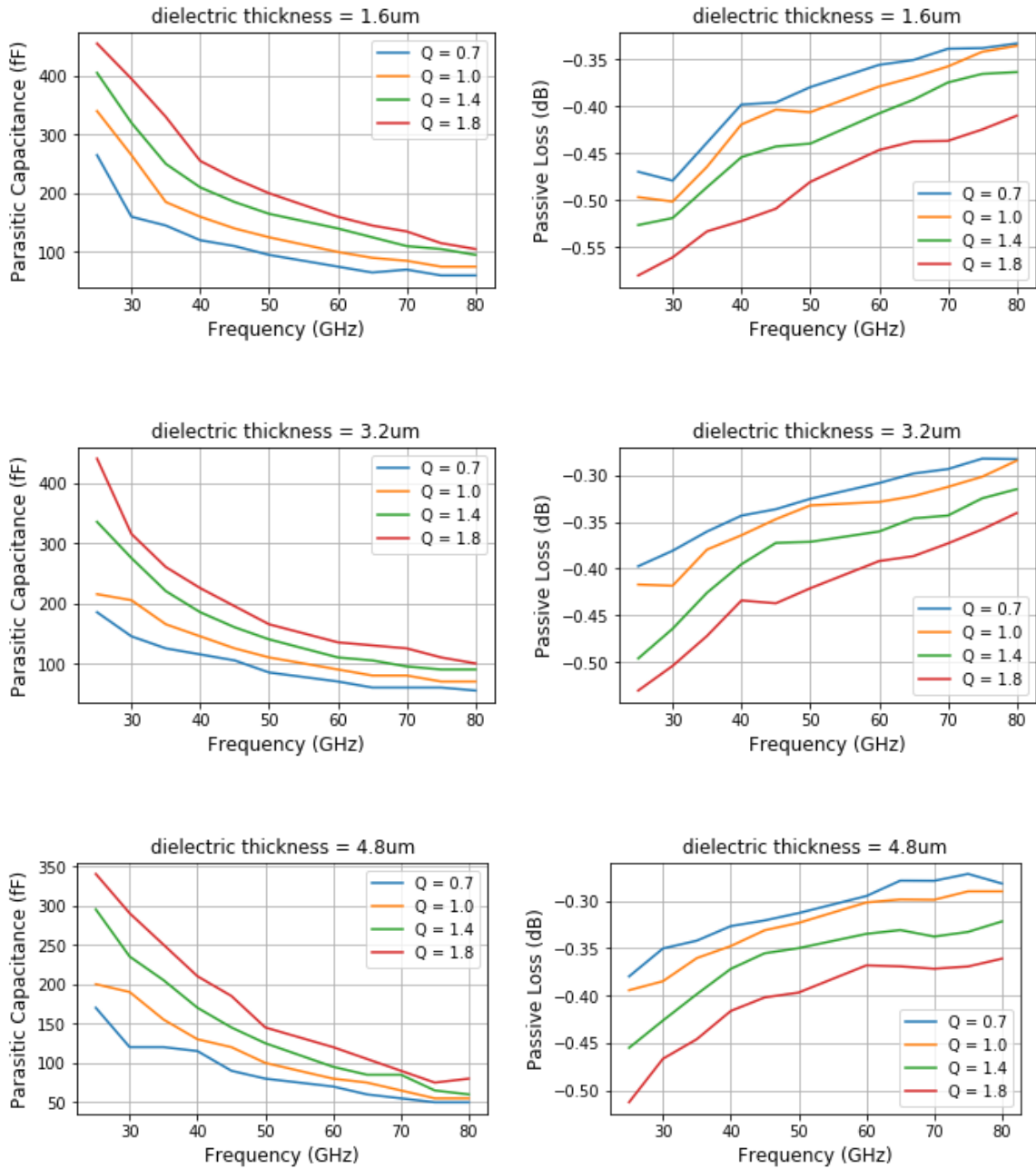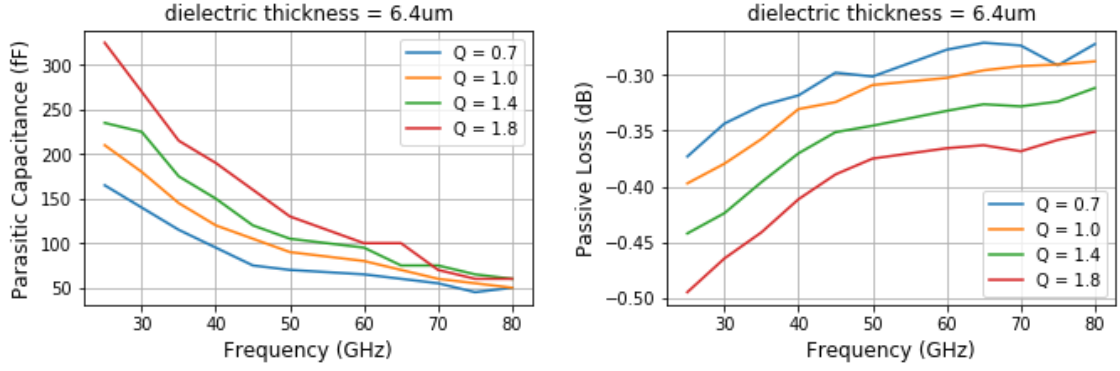
Figure 6.3 The high-level relationship between the optimum mm-wave device size/passive loss and mm-wave frequencies, as calculated by our proposed Machine Learning approaches. The plots verify the rule of thumb that the optimum mm-wave device size reduces as the frequency increases.

6.4 The Implementable Specifications for the BCOD Tasks

In Chapter 2, we theoretically analyze the BCOD structure with the assumptions of lossless coupled lines and infinite realizable ranges for even and odd mode characteristic impedances. Without the Machine Learning approaches, we only have the coupled line theory as the mathematical tool to calculate mid-level coupled line parameters, and as a result, we can only design the BCOD structure with ideal Microwave schematics. Advancing from the designs of theoretical circuits, we developed the Machine Learning techniques in this thesis as a new tool that allow us progress to the next level of fully designing the physical EM structures, where we demonstrated that we can accurately realize physical-level EM networks for the BCOD circuits within a computational time of seconds. Importantly, employing the ML techniques does not require the assumptions of lossless couplers and infinite realizable ranges of Z_e and Z_o that we must adopt in the theoretical methods (see Fig. 6.4).
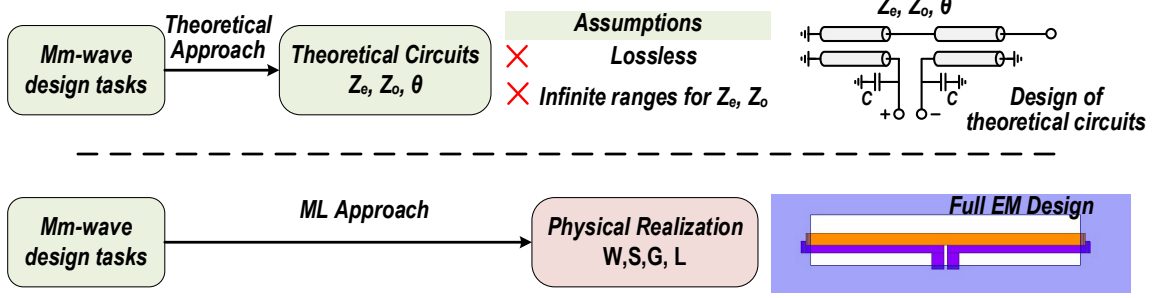
Figure 6.4 Comparison between the theoretical approach and the ML approach. The theoretical approach assumes lossless coupled lines and infinite ranges for Z_e and Z_o and can only produce designs of theoretical circuits, while the ML approach can analyze the design tasks without those assumptions and produce physical realization of EM structures.

The theoretical solutions for the BCOD structure exist for various specifications of Z_L, Z_S, and Q, as shown in Chapter 2, but those solutions are still theoretical and might not be implementable. To evaluate the practicality of those theoretical solutions, in this section, we leverage our ML approaches to revisit several mm-wave design tasks to evaluate the range of electrical specifications that is implementable by our ML techniques. On one hand, this section shows the limitation that our ML algorithms cannot overcome. Also, note that this limitation might also be the inherent limit of the on-chip implementation as well. On the other hand, the results from this section can assist engineers to make high-level design choices when designing mm-Wave systems that involve the BCOD networks.

6.4.1 Impedance Transforming Baluns

Not all the electrical specifications of Impedance Transforming Baluns with an output load Z_L, a device with capacitive impedance Z_C, and the optimum impedance $Z_S = QZ_C$ can be implementable on-chip. For output baluns with Q from 0.7-1.8, we have intensively studied the implementable ranges of electrical specifications in sections 6.2-6.3 over many

mm-wave frequencies and dielectric thicknesses of metal stacks. For example, results from Fig. 6.2 show that on a metal stack with dielectric thickness of 1.6μm, the implementable specifications at 60GHz for Q = 1 and Z_L = 50Ω require that the parasitic capacitance C be from 40-300fF, for which the optimum range is from 50-120fF. For input baluns, we can apply the same technique to study the implementable range. For example, in Fig. 6.5, we illustrate input baluns at 60GHz with Z_L= 50Ω for high impedance devices with Q=6 in the first row, and for low impedance devices with Q=0.6 in the second row. Generally, the implementable specifications for parasitic capacitance is from 40-350fF, where the optimum range for high and low impedance device is from 60-250fF and 60-80fF, respectively.
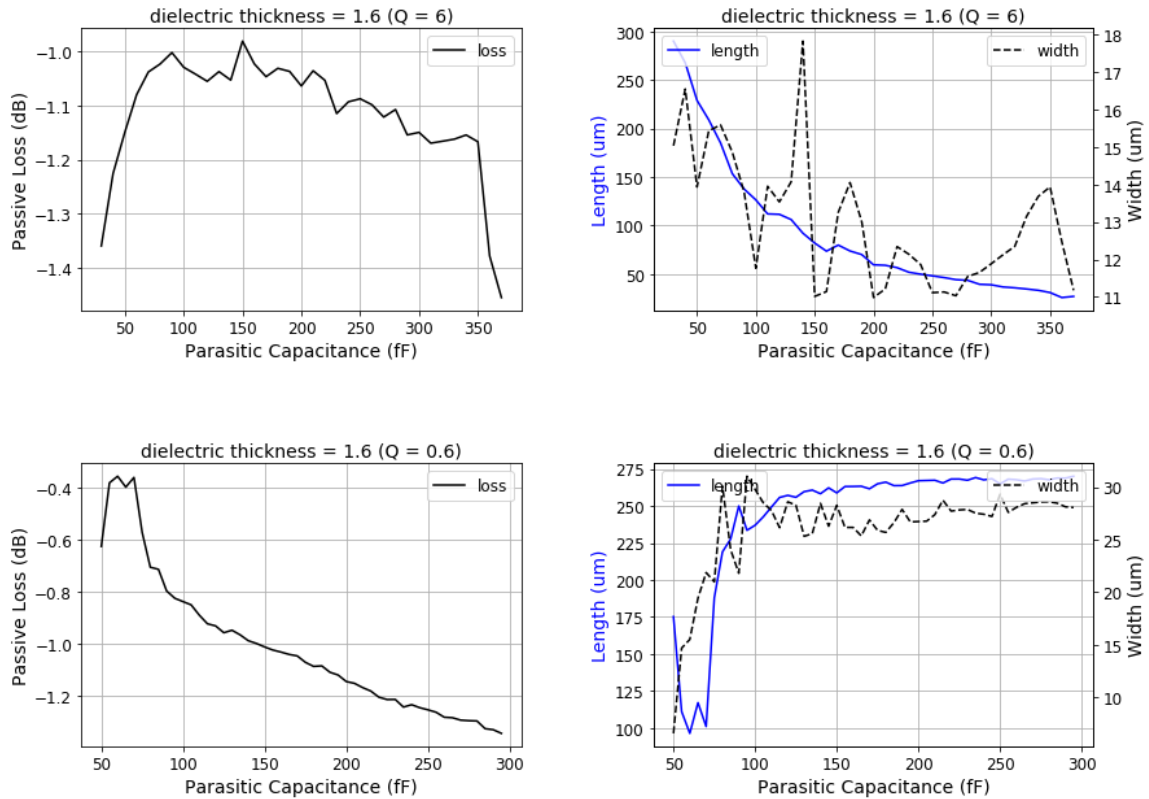
Figure 6.5 The implementable range for input baluns at 60GHz with high impedance devices (high Q) in the first row and with low impedance devices (low Q) in the second row.

6.4.2 Out-Phasing Circuits

The proposed BCOD structure has theoretical solutions for Out-Phasing circuits for arbitrary values of Z_L, Z_S, and $Q = Z_S/Z_C$, as shown in section 2.4, but not all those values might be physically realized on-chip. To understand the limitation, we leverage the ML algorithms to study the implementable range of the theoretical solutions for Out-Phasing circuits in this subsection. Compared to a typical Impedance Transforming Baluns with specifications of Z_L, Z_S, and Q, our proposed Out-Phasing network has two identical baluns with specifications of $2Z_L$, Z_S, and Q, but additionally requires a phase delay of 90° from inputs to outputs. Note that the specification changes from Z_L to $2Z_L$ due to parallel combiners, but we can compensate for this ratio by adding an impedance transformation network.
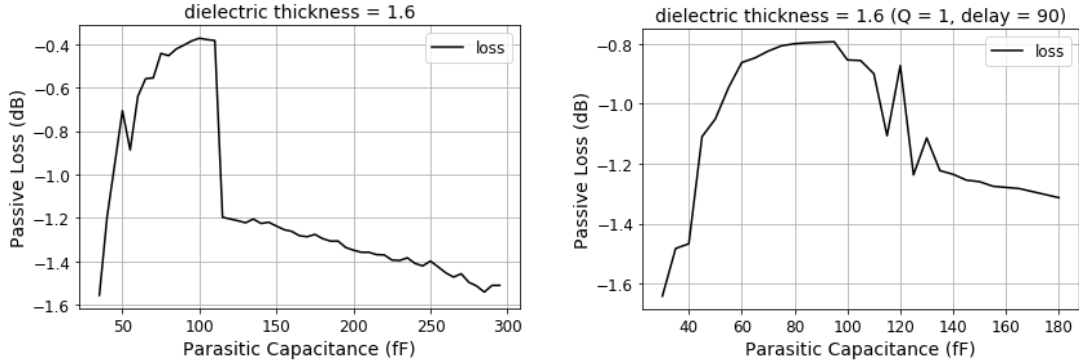
Figure 6.6 The optimum passive loss and implementable range for typical baluns on the left column and for Out-Phasing circuits with phase delay = 90° on the right column. Both have the specifications of Z_L=50Ω, Q=1, and dielectric thickness=1.6µm.

To illustrate the effect of adding the phase-controlled dimension, we describe the optimum passive loss for $Z_L = 50Ω$ and $Q = 1$ over a wide range parasitic capacitance without phase control in the left column of Fig. 6.6 and with phase delay of 90° in the right

column of Fig. 6.6. The ML algorithm yields several critical insights about designing Out-Phasing circuits. On one hand, we can only physically realize Out-Phasing networks with a limited range of specifications. For example, Fig. 6.6 shows that both Out-Phasing circuits and typical baluns have an optimum parasitic capacitance in the range from 60-110fF for the given settings. On the other hand, the optimum passive loss of the Out-Phasing circuits is worse than those of baluns over the range from 60-110fF, which is mainly due to the additional constraint of the phase delay of 90° for Out-Phasing circuits. In this example, the best passive loss for Out-Phasing circuits is -0.8dB, while that for typical baluns is -0.4dB. For other specifications, we can apply a similar procedure to reveal the high-level pictures and trade-offs of Out-Phasing designs.

6.4.3 Doherty Networks
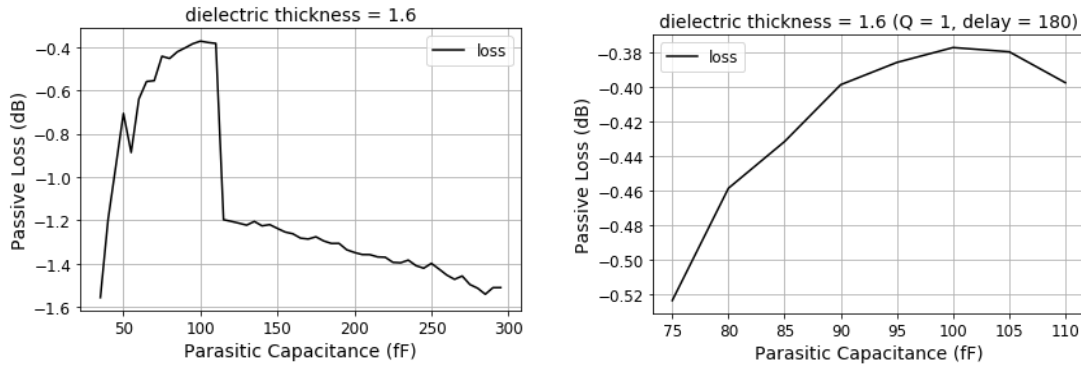
Figure 6.7 The optimum passive loss and implementable range for typical baluns on the left column and for the Auxiliary side of Doherty networks with phase delay = 0°/180° on the right column. Both have the specifications of $Z_L=50\Omega$, Q=1, and dielectric thickness=1.6μm.

The implementable range of electrical specifications for on-chip Doherty networks is also limited, and we can utilize the ML algorithms as a tool to study this range. Compared to the design of Out-Phasing circuits, the design specifications for Doherty networks is

even more stringent, because Doherty EM structures require a phase delay of both 90° for Main PAs and 0°/180° for Auxiliary PAs. Because we presented the high-level picture for a 90° phase delay in subsection 6.4.2, we only show the analysis by the ML algorithms for 0°/180° phase delays in this subsection. Depicted in the right column of Fig. 6.7, the optimum passive loss of Impedance Transforming Baluns in the range from 75-110fF is approximately identical to those of the Auxiliary side of Doherty networks that requires 0°/180° phase delay, indicating that this delay also results in the lowest passive loss. Moreover, the study shows that the implementable range for parasitic capacitance of the Auxiliary side of 60GHz Doherty structures with Z_L=50Ω, Q=1, and dielectric thickness=1.6µm is from 75-110fF. We can also apply similar techniques to understand the implementable ranges for other specifications of Doherty designs.

6.5   Analysis

Going beyond the original motivation of automating the BCOD structure, in this chapter, we leveraged the ML techniques to add theoretical interpretations for several aspects of mm-wave designs. For example, we employed the ML approaches to reveal high-level insights about the optimum transistor sizes, the rule of thumb between device sizes and mm-Wave frequencies, or the implementable range of electrical specifications. Without the ML algorithms that can accurately, reliably, and quickly transfer from problems (electrical specifications) to optimum solutions (physical dimensions), we might not be able to answer those high-level questions.

CHAPTER 7.   CONCLUSIONS

In this dissertation, we develop Machine Learning techniques for automating mm-wave EM designs. Starting from the emerging mm-wave power and efficiency challenges, we theoretically propose the BCOD structure with a broad design space that has solutions for Impedance Transforming Baluns, Power Combiners, Out-Phasing circuits, and Doherty networks. Following that, the main contribution of the dissertation is to formulate Machine Learning techniques that can fully automate EM designs for the BCOD structures. To build various physical-electrical Machine Learning models, we randomly sample physical dimensions from a continuous design space, extract electrical labels from S-parameter files, train neural networks to learn the physical-electrical relationships, and evaluate the ML models with K-fold validation. The results demonstrate that our ML models can accurately predict electrical properties from physical dimensions, reducing the need for time consuming full-wave EM simulations.

From our pre-trained ML models for couplers and baluns, we propose several automation algorithms that can fully generate EM designs for BCOD structures within a computational time of seconds. We demonstrated design examples for Directional Couplers, Impedance Transforming Baluns, Out-Phasing Circuits, and Doherty networks over a wide range of electrical specifications, all of which exhibit the electrical properties closely matched with desirable values. Notably, our automation algorithms can optimize for the lowest metal loss, and to the best of our knowledge, we are not aware of any prior techniques that can systematically do so for mm-wave designs. From a higher-level

perspective, we show that adding the Machine Learning dimension to existing EM methods can resolve many drawbacks of the current design approach. The time to design an EM structure could be reduced from days-weeks-months to seconds, the quality of design could be more reliable and exhibit less variance, and the condition of the lowest metal loss could be systematically guaranteed.

The Learning Algorithm
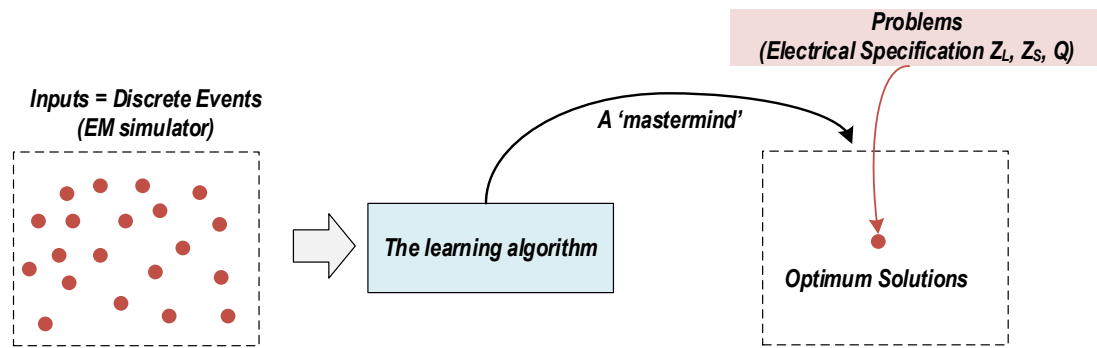
Figure 7.1 A conceptual drawing of the learning algorithm presented in this dissertation.

Observing enough discrete events (EM simulated results) of the design space, the learning algorithm eventually becomes a "mastermind" that can directly know the optimum solutions (full EM designs) when given the problems (electrical specifications), as described a conceptual drawing in Figure 7.1. The critical requirement of the proposed learning algorithm is to collect enough data to understand the design space. On one hand, we might need to extensively run full-wave EM simulations to collect the data if we are not able to "LEGO" previous EM results to construct the desirable EM results, as discussed in section 3.5. On the other hand, we need to intensively simulate EM experiments only once, or we can even leverage the existing EM data collected by other engineers or

researchers, and from that we could immediately formulate the learning algorithm that helps directly navigate from problems to optimum solutions.

When the EM structures get more complex and involve many design parameters, making the right decision when updating the physical dimensions from simulated results can be highly challenging for engineers if following the current technique to design EM circuits. The reason is that the circuit analysis might be too complicated for engineers to manually make a meaningful choice of amending physical dimensions. At the same time, the learning algorithm still works because the gradient of the loss with respect to the design parameters will serve as a circuit-analysis tool to guide the update of EM parameters. After training the ML models that accurately learn the physical-electrical relationship of the design space, in the computational time of seconds, the learning algorithm could still generate the optimum EM designs even with the high complexity of the EM structures.

In Chapter 6, we demonstrated that the application of the proposed Machine Learning techniques can go beyond just automating specific EM designs. We see that the ML models can serve as a new tool for bigger optimization questions, and we used our proposed techniques to answer several challenging, abstract, and high-level questions, such as the calculation of the optimum transistor size, the derivation of the rule of thumb between the device size and mm-wave frequencies.

New Tools for Designing EM Structures

During the last several decades, computational EM and commercial EM solvers such as ADS or HFSS have been the major driving force that moved EM designs forward. The capability of the software to predict the electrical properties of complex EM structures with

a very high level of accuracy has allowed electrical engineers to realize many advanced wireless systems. Engineers spend considerable time tuning EM designs, and the results have been fruitful, but many designs are still based heavily on trial-and-error. Looking forward to the next decades, we see the importance of developing new tools to not only verify that certain EM designs achieve all specifications but also help automating EM circuits and exploring novel EM structures. The new tools will creatively design circuits rather than simply compute circuits. For example, those should help us to search in a wide variety of design spaces, explore repeated patterns, and from that invent novel structures [42][43]. We think Machine Learning will play an important role in building such tools, and we are looking forward to the future.

REFERENCES

[1] H. C. Lin, G. M. Rebeiz, "A 70–80-GHz SiGe Amplifier with Peak Output Power of 27.3 dBm," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 7, pp. 2039-2049, July 2016.

[2] E. Wagner and G. M. Rebeiz, "Single and Power-Combined Linear E-Band Power Amplifiers in 0.12- μ m SiGe With 19-dBm Average Power 1-GBaud 64-QAM Modulated Waveforms," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 4, pp. 1531-1543, April 2019.

[3] Y. Hsiao, Z. Tsai, H. Liao, J. Kao and H. Wang, "Millimeter-Wave CMOS Power Amplifiers with High Output Power and Wideband Performances," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4520-4533, Dec. 2013.

[4] A. Chakrabarti and H. Krishnaswamy, "High-Power High-Efficiency Class-E-Like Stacked mmWave PAs in SOI and Bulk CMOS: Theory and Implementation," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 8, pp. 1686-1704, Aug. 2014.

[5] R. Bhat, A. Chakrabarti, and H. Krishnaswamy, "Large-scale power combining and mixed-signal linearizing architectures for watt-class mmWave CMOS power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 703–718, Feb. 2015.

[6] K. Datta and H. Hashemi, "Watt-level mm-wave power amplification with dynamic load modulation in a SiGe HBT digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 371–388, Feb. 2017.

[7] K. Datta, H. Hashemi, "High-Breakdown High-fmax Multiport Stacked-Transistor Topologies for the W-band Power Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1305-1319, May 2017.

[8] W. Tai, L. R. Carley and D. S. Ricketts, "A 0.7W fully integrated 42GHz power amplifier with 10% PAE in 0.13µm SiGe BiCMOS," *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, 2013, pp. 142-143.

[9] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully integrated CMOS Power Amplifier Design Using the Distributed Active-Transformer Architecture" *IEEE J. Solid-State Circuits*, vol.37, no. 3, Mar. 2002.

[10] I. Aoki, S.D. Kee, D. B. Rutledge, A. Hajimiri, "Distributed active transformer-a new power-combining and impedance-transformation technique", *IEEE Trans. Microw. Theory Techn.,* vol. 50, no. 1, pp. 316-331, Jan. 2002.

[11] U. R. Pfeiffer and D. Goren, "A 23-dBm 60-GHz Distributed Active Transformer in a Silicon Process Technology," in *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 5, pp. 857-865, May 2007.

[12] K. Wang, et al., "A 1V 19.3dBm 79GHz Power Amplifier in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers,* Feb. 2012.

[13] H. Chireix, "High power outphasing modulation," in *Proc. IRE*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.

[14] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. A. El-Tanani and K. Soumyanath, "A Flip-Chip-Packaged 25.3 dBm Class-D Outphasing Power Amplifier in 32 nm CMOS for WLAN Application," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1596-1605, July 2011.

[15] T. W. Barton, A. S. Jurkov, P. Pednekar, and D. J. Perreault, "Multi-Way Lossless Outphasing System Based on an All-Transmission-Line Combiner," *IEEE Trans Microw Theory Tech.,* vol. 64, pp. 1313–1326, Apr. 2016.

[16] D. Zhao, S. Kulkarni, P. Reynaert, "A 60-GHz Outphasing Transmitter in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3145–3183, Dec. 2012.

[17] M. Mehrjoo, J. Buckwalter, "A microwave injection-locking outphasing modulator with 30dB dynamic range and 22% system efficiency in 45nm CMOS SOI," *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, Feb. 2016.

[18] B. Rabet and J. Buckwalter, "A high-efficiency 28GHz outphasing PA with 23dBm output power using a triaxial balun combiner," *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, 2018, pp. 174-176.

[19] S. Li, T. Chi, J. Park, H. T. Nguyen and H. Wang, "A 28-GHz Flip-Chip Packaged Chireix Transmitter With On-Antenna Outphasing Active Load Modulation," *in IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1243-1253, May 2019.

[20] W. H. Doherty, "A new high efficiency power amplifier for modulated waves", *Proc. IRE*, vol. 24, no. 9, pp. 1163-1182, Sep. 1936.

[21] N. Rostomyan, M. Özen, P. Asbeck, "28 GHz doherty amplifier in CMOS SOI with 28% back-off PAE," *IEEE Microw. Wireless Compon. Lett.,* vol. 28, no. 5, pp. 446-448, May 2018.

[22] M. Özen, K. Andersson and C. Fager, "Symmetrical Doherty Power Amplifier with Extended Efficiency Range," *in IEEE Transactions on Microwave Theory and Techniques,* vol. 64, no. 4, pp. 1273-1284, April 2016.

[23] M. Özen, N. Rostomyan, K. Aufinger, C. Fager, "Efficient millimeter wave Doherty PA design based on a low-loss combiner synthesis technique", *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 12, pp. 1143-1145, Dec. 2017.

[24] S. Hu, F. Wang, and H. Wang, "A 28GHz/37GHz/39GHz Multiband Linear Doherty Power Amplifier for 5G Massive MIMO Applications," *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, Feb. 2017.

[25] K. Greene, A. Sarkar, and B. Floyd, "A 60-GHz dual-vector Doherty beamformer," in *IEEE J. Solid-State Circuits,* vol. 52, no. 5, pp. 1373–1386, May 2017.

[26] E. Kaymaksut et al., "Transformer-Based Doherty Power Amplifiers for mm-wave Applications in 40-nm CMOS," *IEEE Trans. Microwave Theory and Techniques,* vol. 63, no. 4, pp. 1186-1192, Apr. 2015.

[27] H. T. Nguyen, S. Li and H. Wang, "4.6 A mm-wave 3-Way Linear Doherty Radiator with Multi Antenna Coupling and On-Antenna Current-Scaling Series Combiner for Deep Power Back-Off Efficiency Enhancement," *2019 IEEE International Solid- State Circuits Conference (ISSCC),* San Francisco, CA, USA, 2019, pp. 84-86.

[28] H. T. Nguyen, T. Chi, S. Li, and H. Wang, "A 62-to-68GHz linear 6Gb/s 64QAM CMOS Doherty radiator with 27.5%/20.1% PAE at peak/6dB-back-off output power leveraging high-efficiency multi-feed antenna-based active load modulation," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* Feb. 2018, pp. 402–403.

[29] H. T. Nguyen, T. Chi, S. Li and H. Wang, "A Linear High-Efficiency Millimeter-Wave CMOS Doherty Radiator Leveraging Multi-Feed On-Antenna Active Load Modulation," *in IEEE Journal of Solid-State Circuits,* vol. 53, no. 12, pp. 3587-3598, Dec. 2018.

[30] Kian Sen Ang, Yoke Choy Leong, and Chee How Lee, "Analysis and design of miniaturized lumped-distributed impedance-transforming baluns," *in IEEE Transactions on Microwave Theory and Techniques,* vol. 51, no. 3, pp. 1009-1017, March 2003.

[31] H. T. Nguyen and H. Wang, "A Coupler-Based Differential Doherty Power Amplifier with Built-In Baluns for High Mm-wave Linear-Yet-Efficient Gbit/s Amplifications," *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC),* Boston, MA, 2019.

[32] H. T. Nguyen and H. Wang, "A Coupler-Based Differential Mm-wave Doherty Power Amplifier with Impedance Inverting and Scaling Baluns," *in IEEE Journal of Solid-State Circuits,* vol. 55, no. 5, pp. 1212-1223, May 2020.

[33] H. T. Nguyen, D. Jung and H. Wang, "4.9 A 60GHz CMOS Power Amplifier with Cascaded Asymmetric Distributed-Active-Transformer Achieving Watt-Level Peak Output Power with 20.8% PAE and Supporting 2Gsym/s 64-QAM Modulation," *2019 IEEE International Solid- State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2019, pp. 90-92.

[34] Qi-Jun Zhang, K. C. Gupta and V. K. Devabhaktuni, "Artificial neural networks for RF and microwave design - from theory to practice," *in IEEE Transactions on Microwave Theory and Techniques,* vol. 51, no. 4, pp. 1339-1350, April 2003.

[35] H. Kabir, Y. Wang, M. Yu, and Q. Zhang, "Neural Network Inverse Modeling and Applications to Microwave Filter Design," *in IEEE Transactions on Microwave Theory and Techniques,* vol. 56, no. 4, pp. 867-879, April 2008.

[36] M. Ohira, A. Yamashita, Z. Ma and X. Wang, "Automated Microstrip Bandpass Filter Design Using Feedforward and Inverse Models of Neural Network," *2018 Asia-Pacific Microwave Conference (APMC),* Kyoto, 2018, pp. 1292-1294.

[37] Jie Liu, et. al, "Microwave Integrated Circuits Design with Relational Induction Neural Network," *arXiv* 1901.02069.

[38] High Frequency Structure Simulator , https://www.ansys.com/products/electronics/ansys-hfss

[39] Advanced Design System, https://www.keysight.com/us/en/products/software/pathwave-design-software/pathwave-advanced-design-system.html

[40] Chollet, F., & others. (2015). Keras. GitHub. Retrieved from https://github.com/fchollet/keras.

[41] Diederik P. Kingma and Jimmy Ba, "Adam: A Method for Stochastic Optimization," *International Conference on Learning Representations,* San Diego, CA, USA, 2015.

[42] Zoph, B. & Le, Q. V. (2016), "Neural Architecture Search with Reinforcement Learning," *arxiv* 1611.01578.

[43] Gaier, A. & Ha, D. (2019), "Weight Agnostic Neural Networks," *Neural Information Processing Systems*, pp. 5365-5379, Dec 2019.