ULTRA THIN ULTRAFINE-PITCH CHIP-PACKAGE INTERCONNECTIONS FOR EMBEDDED CHIP LAST APPROACH

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ULTRA THIN ULTRAFINE-PITCH CHIP-PACKAGE INTERCONNECTIONS FOR EMBEDDED CHIP LAST APPROACH

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SUMMARY

Ever growing demands for portability and functionality have always governed the electronic technology innovations. IC downscaling with Moore's law and system miniaturization with System-On-Package (SOP) paradigm has resulted and will continue to result in ultraminiaturized systems with unprecedented functionality at reduced cost. The trend towards 3D silicon system integration is expected to downscale IC I/O pad pitches from 40μm to 1- 5 μm in future. Device- to- system board interconnections are typically accomplished today with either wire bonding or solders. Both of these are incremental and run into either electrical or mechanical barriers as they are extended to higher density of interconnections. Downscaling traditional solder bump interconnect will not satisfy the thermo-mechanical reliability requirements at very fine pitches of the order of 30 microns and less. Alternate interconnection approaches such as compliant interconnects typically require lengthy connections and are therefore limited in terms of electrical properties, although expected to meet the mechanical requirements. Furthermore, according to International Technology Roadmap for Semiconductors (ITRS-2006), the supply current in high performance microprocessors is expected to increase to 220 A by 2012. At such supply current, the current density will exceed the maximum allowable current density of solders. The intrinsic delay and electromigration in solders are other daunting issues that become critical at nanometer size technology nodes. In addition, formation of intermetallics is also a bottleneck that poses significant mechanical issues.

Recently, many research groups have investigated various techniques for copper-copper direct bonding. Typically, bonding is carried out at 400oC for 30 min followed by annealing for 30 min. High thermal budget in such process makes it less attractive for integrated systems because of the associated process incompatibilities. In the present study, copper-copper bonding at ultra fine-pitch using advanced nano-conductive and non-conductive adhesives is evaluated. The proposed copper-copper based interconnects using advanced conductive and non-conductive adhesives will be a new fundamental and comprehensive paradigm to solve all the four barriers: 1) I/O pitch 2) Electrical performance 3) Reliability and 4) Cost. This thesis investigates the mechanical integrity and reliability of copper-copper bonding using advanced adhesives through test vehicle fabrication and reliability testing. Test vehicles were fabricated using low cost electro-deposition techniques and assembled onto glass carrier. Experimental results show that proposed copper-copper bonding using advanced adhesives could potentially meet all the system performance requirements for the emerging micro/nano-systems.

1. INTRODUCTION

This chapter begins with a brief introduction of the current trend towards convergent and multi-functional mixed signal micro-systems with integrated functions. Seamless integration of chip to package enabled by ultrahigh package wiring density, coupled with ultra-fine pitch chip-package interconnections are identified as the key cornerstones for SoP. Various challenges associated with providing ultra-fine pitch and short interconnections that can support high bandwidth with miniaturization and integration, are identified and the current approaches to address these issues are presented. Need for advances in interconnections, assembly, and module reliability technology in future high-speed multifunctional systems are reviewed. A novel approach of cu-cu bonding using advanced nano-conductive and non-conductive adhesives to address the ultra-fine pitch/high I/O requirements of future are then presented as the objectives of the current study.

Microelectronic products in the past have been discrete systems with different systems providing different functions. Recently, there is a new and emerging trend towards convergent micro-systems that bring together existing digital and RF technologies as well as newer technologies like optoelectronics, Micro-Electro Mechanical Systems and bio-sensors. In the past, driven by Moore's law, the integration efforts were focused predominantly on silicon using CMOS technology. While Silicon is best suited for integration of transistors, it does not lend itself to integration of RF and

Optoelectronic circuits in a cost-effective manner. The System-on-Chip (SoC) concept seeks to integrate numerous system functions on one silicon platform horizontally, namely the chip. This approach of integrating functionalities on a single chip is beset with several fundamental and practical barriers like high cost, several photolithography steps, low yield and licensing and Intellectual Property (IP) issues [1]. Most systems consist of many non-silicon components, such as passive components, sensors, antennas, connectors, etc. that have limited performance when integrated on silicon. Currently, System-in-Package (SIP) approach of vertical stacking of bare and packaged ICs is pursued by several packaging companies for integration of functions at module and subsystem levels. SIP extends silicon integration in 3D but is still limited by CMOS capabilities. A new paradigm that overcomes the shortcomings of SoC, SiP, and traditional packaging, therefore, is necessary.

To overcome the limitations of SoC approach, System-on-Package (SoP) approach was proposed by Prof. Rao Tummala at the Packaging Research Center in 1994. SoP enables heterogeneous integration of RF/digital/opto/bio-sensing functions by system-centric IC-package co-design and functional optimization with 3D integration of thin film components on the package. Most system companies are pursuing SoP to answer the market demand for highly-miniaturized, high-performance, low-cost systems for the era of ambient intelligence characterized by smart electronic portable devices. A schematic SoP cross-section is shown in Figure 1.1. The underlying benefit of System-on-Package (SoP) technology is its ability to support highly integrated systems or subsystems with optimized cost, size, and performance while simultaneously reducing the

time to market. With this fundamentally new paradigm, the SoP methodology overcomes the barriers of SoC leading to cheaper and faster convergent Microsystems [2].

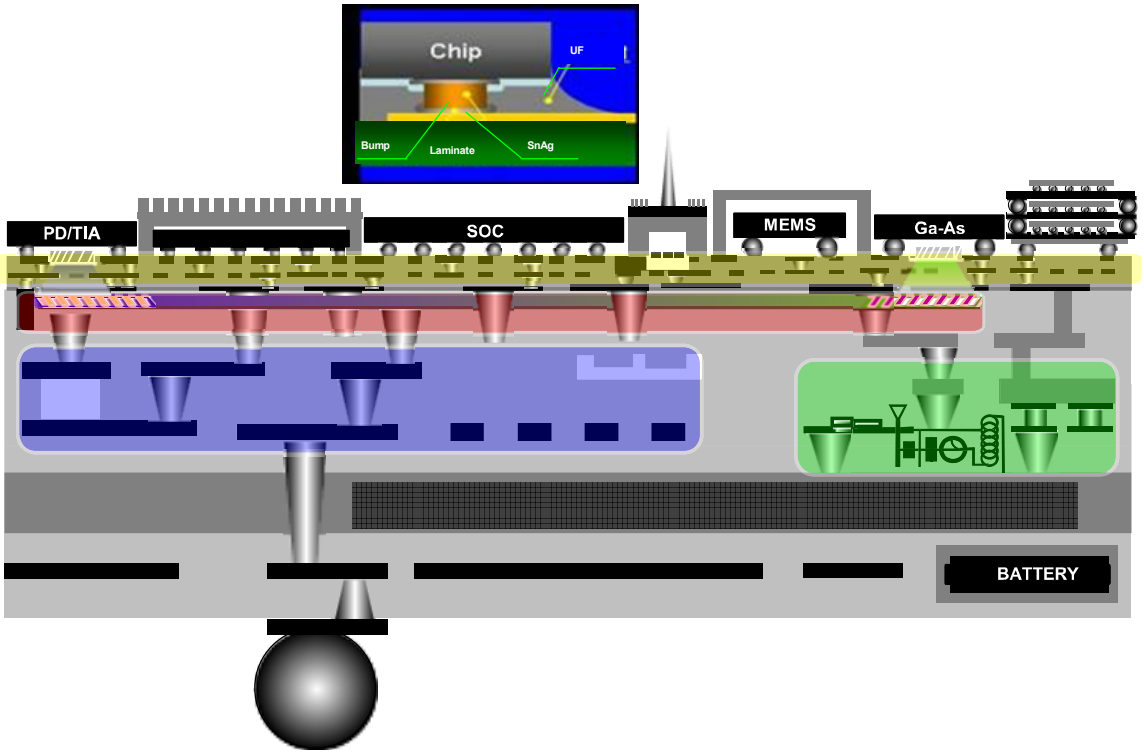


Figure 1.1 A schematic of SOP highlighting the chip-package interconnections.

The system-on-package (SoP) is a system concept with this package integration, in contrast to SiP, a module concept. The SoP, a System-centric technology, is based on embedded thin film components in organic boards or packages, and together with SiP modules, SoC devices, battery and user interface, leads to multi-functional systems in the short term and mega–function systems in the long run. It seeks to integrate disparate technologies to achieve multiple system functions into a single package, while providing ultra-small form factor.

Along with mixed signal electronic systems, SoP is also becoming critical for neuroscience applications such as wireless implantable micro-systems. Neural implants have a 3-D array of electrodes that interface with the tissue, thus creating the much significant neuro-electronic interfaces. These micro-systems support electronics for signal processing and for wireless communication with the outside world. [3]. The most significant challenges in packaging these arrays are keeping the feature sizes small in order to keep the low profile of the package.

1.1 Major enablers for SoP

SoP relies on embedded thin film components and high density packaging for system integration. Three enabling technologies of SoP permit applications such as a single-chip module interconnection or multi-chip integration of heterogeneous semiconductor chips to provide a system on a package. They are – high density chip-package interconnections, high substrate wiring densities, and embedded actives.

1.1.1 High density substrate wiring

The escalating I/O densities in ICs are driven by the need for the highest system performance such as by multicore processors, aggregately providing data rates in TByte/s. Back End of Line (BEOL) wiring refers to the formation of local and global interconnections wiring that interconnects various transistor circuit elements on the chip. In the 65 nm node IC technology, the BEOL interconnect lines vary from 200 nm (metal layer 1) to 1100 nm (metal layer 8). These interconnections have a thickness-to-width ratio of 1.8 with low-k inter layer dielectric material. On the other hand, the coarse I/O

pitches of even the most advanced package substrate interconnection technologies are still around 100 μm with line and spaces around 25-30 microns. This is in huge contrast to IC I/O pad pitches which are as small as 40μm for state-of-the-art technologies and will reduce to 1- 20 μm in future. It is clear that a large interconnect gap exists between the on-chip interconnect technologies and off chip organic substrate technologies.

SOP on a silicon substrate offers a solution to the above IC-Package gap. The main contributor to this solution is the silicon wafer itself. Unlike organic packages or boards, silicon wafer is flat and smooth and amenable therefore for ultrahigh density wiring with ultra fine pitch. Standard silicon wiring ground rules can be used on the Si system substrate to lower the mismatch between the interconnect pitches on-chip and off-chip to support system integration with active and passive components. Submicron Back End Of Line (BEOL) geometries can be achieved by leveraging the current and previous generation semiconductor processing tools to achieve dense wiring and meet the future I/O pitch needs.

1.1.2 Embedded Actives

Embedded Actives have been proposed and realized, to some exent, as a promising package technology to achieve ultra miniturized form factor as well as better electrical performance. It accomplishes these by burying active chip components directly into an HDI (High Density Interconnect) substrate. While embedded active approaches with chip-first technology can give many advantages such as small form factor and better electrical performance, they also have many other concerns such as: (1) Serial chip-to-build-up processes accumulate yield losses associated with each process, leading to lower

yield and higher cost. (2) Defective chips cannot be reworked in an embedded package structure. This needs 100% KGDs (Known Good Die). (3) The interconnections in chip-first approach which are direct metallurgical contacts can fatigue due to thermal stress. (4) Thermal manangement issues are also evident since the chip is totally embedded within polymer materials of substrate or build-up layers.

It is expected that the chip-last approach has many advantages and a few disadvantages, compared to chip-first or chip-middle technologies from the viewpoints of process, yield, reworkable interconnections and thermal management.

1. Process and yield: Lower loss accumulation and higher process yield are expected for mutichip applications, since all the processes for substrate, build-up layers, cavity and embedding the chip are carried out in two parallel operations—substrate and chip. In addition, no complex processes are needed after the chip is embedded, which could otherwise damage the chip.
2. Reworkability: Defective chips can be replaced by the use of reworkable interconnects and appropriate selection and processing of underfill and encapsulation materials after electrical testing.
3. Interconnections: Short interconnections can give rise to electrical performance as good as direct metallurgical contacts of chip-first embedding active technology. Nano-structured materials with not only high electrical conductivity but also excellent mechanical strength, toughness and fatigue resistance can provide mechanically reliable interconnects even with low profile.

4. Thermal management: Since the backside of embedded chip is directly exposed to air or bonded to a layer of heatsink with highest thermal conductivity, thermal management becomes easier and many possible solutions for cooling can be applied.

1.1.3 Ultrafine pitch chip-package interconnection

Ultrafine pitch chip-package interconnection is a key cornerstone for SoP. The need for ultrafine pitch interconnection is multifold as discussed below.

A) WLSOP needs ultrafine pitch interconnections

WLSOP, defined here as SOP with a silicon substrate, closes the IC-to-board I/O gap by means of ultra fine pitch wiring and interconnection pitch that cannot be achieved with traditional organic substrate and board technologies. The trend towards 3D silicon system integration is expected to further downscale IC I/O pad pitches from 40μm to 1- 5 μm in future.

B) Device downscaling

In the past two decades, there have been rapid advances in integrated circuit (IC) fabrication and their applications with faster, lighter, smaller, and yet less expensive electronic products. The semiconductor industry crossed the historic transition – nano chips with less than 65 nm nodes. Some of these chips will have more than a billion transistors which require I/Os in excess of 10,000 and power in excess of 150 watts, providing computing speed at terabits per second. ITRS Roadmap calls for the IC feature size down to 32 nm and the I/O pitch down to 20 μm.

Figure 1.2 displays ITRS trends for first level interconnections. With such downscaling of the feature size signal integrity, interconnection delay, parasitics, mechanical stability of the interconnections and electromigration become utmost important. The IC packaging that is used to provide I/O connections from the chip to the rest of the system is typically bulky, costly, and limits both the performance and the reliability of the IC it packages. Systems packaging involving interconnection of components on a system level board are similarly bulky and costly, with poor electrical and mechanical performance.

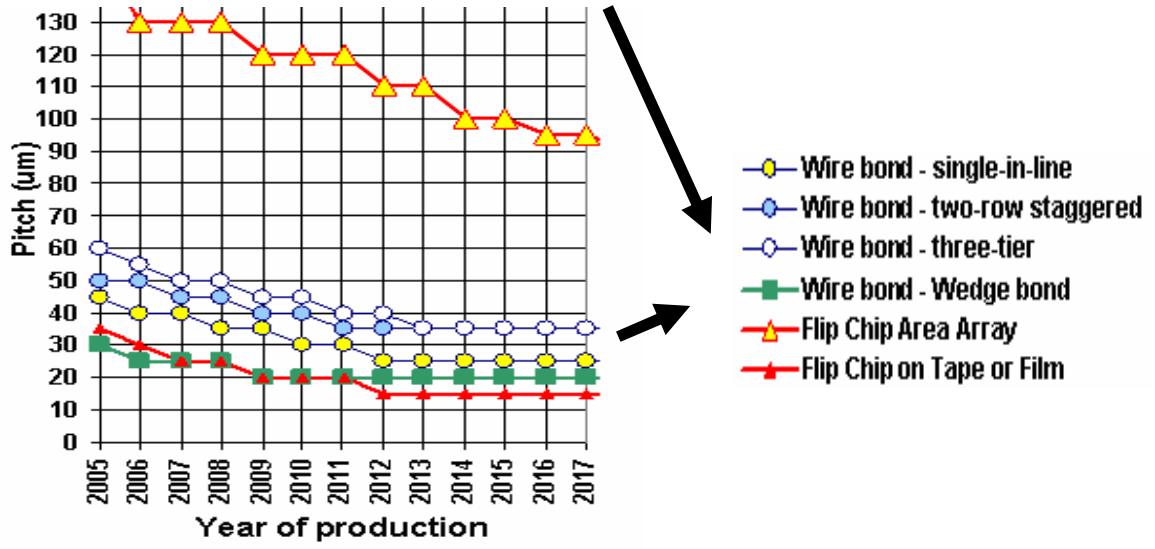


Figure 1.2 Chronological trend in transition in electronic technology

C) TSV Bonding

The concept of silicon chip carrier was developed in IBM in 1972 [4], wherein a Si substrate was used as a chip carrier instead of organic or ceramic substrates. Initially, the chips were connected to the chip carrier by perimeter connections such as wire

bonding. Later, the connections were replaced by flip chip connections. Lately, TSVs have replaced both. The TSVs help to develop a much higher density interconnection from the chip to the carrier and from the carrier to the board. Presently silicon chip carrier technology involves through-silicon vias (TSVs), ultra high density wiring, fine pitch chip-to-carrier interconnections, and integrated actives and passives. Figure 1.3 shows the cross-section view of a Si chip carrier and the process steps involved in developing such a Si chip carrier with TSVs [5]. The chips are flip chip bonded to the chip carrier either by Cu-Cu bonding or solder bumping. The TSV development is carried out by via-first approach. The TSVs supply the signal and power from the board to the top side of the chip carrier. High-speed and high density wiring on the chip carrier distributes the signal and power to the chip.

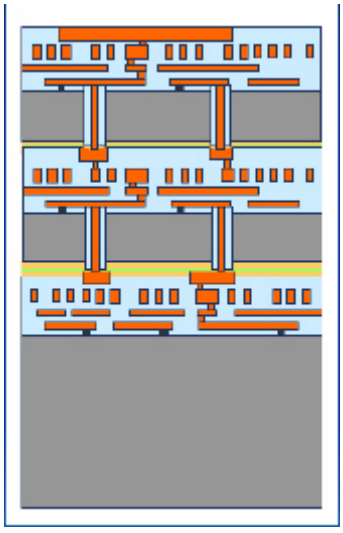


Figure 1.3 Cross-section view of a Si chip carrier with TSVs (Courtesy: IMEC)

D) Multicore architectures

A reduction in the power dissipation and increase in the total bandwidth is achievable using the multi core approach. The multi-core approach would need an

extremely high number of I/O's and interconnects to support bandwidths of the order of 1 TByte/s for communications between IC's. The escalating I/O densities are therefore driven by the need for computer and communication technology for highest system performance, not by the operating frequency of a single processor but by multi-core processors, aggregately providing highest data rates at lowest power.

E) Low-cost RF modules

In the WLSOP concept, redistribution layers may not be necessary as the package wiring geometries match that of the chip I/Os and the IC-packages are co-designed and fabricated for impedance-matched, high data rate interconnections with the lowest interconnection distances. However, the traditional wafer level packaging constituted redistribution of peripheral bonding pads designed for wirebond to area array interconnections with coarser pitch as well as, stress buffering or stress redistribution features. Multilevel thin film redistribution layers enlarge the wafer pitch to match that of the organic packages with a rerouting process. Such redistribution layers also enhance passivation and partially relieve the WLP stresses leading to better assembly reliability. However, low cost RF modules are driving RF IC manufacturers to eliminate the redistribution steps and assemble at pitches less than 30 microns using ultrafine pitch peripheral I/Os (Figure 1.4).

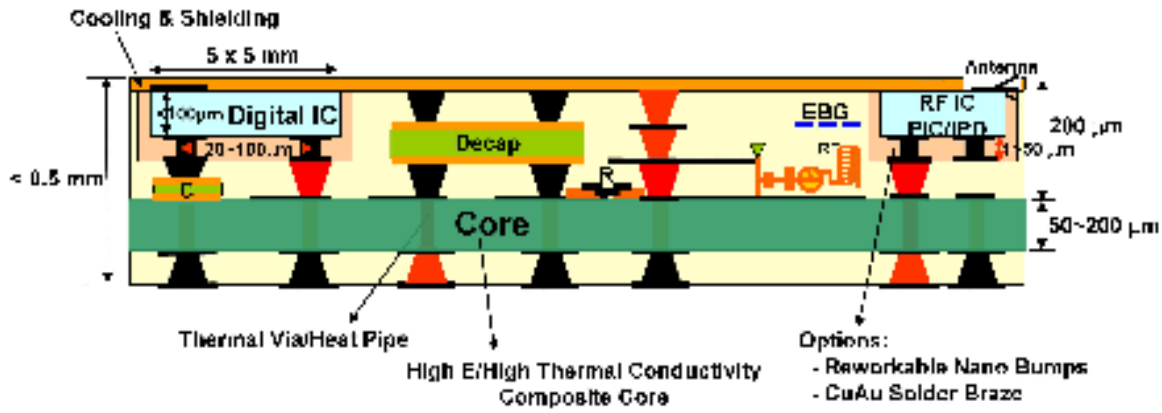


Figure 1.4 Cross section of low cost RF modules with embedded actives and passives (Georgia Tech, PRC)

1.2 Current Approaches for Device-Package Interconnections

Electrical interconnections rely heavily on multi-functional materials that must serve as electrical conductors and be able to withstand complex, sustained and cyclic thermo-mechanical loads. In addition, the materials must be environmentally-friendly, corrosion resistant, thermally stable over a long time, and resistant to electro-migration. A major challenge is also to develop economic processes that can be integrated into back end of the wafer foundry, i.e. with wafer level packaging.

Device- to- system board interconnections today are typically accomplished with either wire-bonding or solders. Both of these are incremental and run into either electrical or mechanical barriers as they are extended to higher density of interconnections. Downscaling traditional solder bump interconnect will not satisfy the thermo-mechanical reliability requirements at very fine pitches even of the order of 30 microns and less. Alternate interconnection approaches such as compliant interconnects typically require

lengthy connections and are therefore limited in terms of electrical properties, although expected to meet the mechanical requirements. Solder technology imposes several pitch, processability and cost restrictions at such fine pitches. Furthermore, according to International Technology Roadmap for Semiconductors (ITRS-2006), the supply current in high performance microprocessors is expected to increase to 220 A by 2012. At such supply current, the current density will exceed the maximum allowable current density of solders. The intrinsic delay and electromigration in solders are other daunting issues that become critical at nanometer size technology nodes. In addition, formation of intermetallics is also a bottleneck that poses significant mechanical issues.

Being able to provide several fold increase in the chip-to-package vertical interconnect density is essential for garnering the true benefits of nanotechnology that will utilize nano-scale devices. Major interconnection and their enabling technologies along with the current roadblocks are outlined below.

1.2.1 Ultra-fine pitch wire bonding

Today, one of the most widely-used interconnect technology is thermo-sonic Au wire bonding. Using this low-cost method, pitches of 40μm can currently be achieved. This technology however results in long interconnect wires, fanning out from the small on-chip I/O pitch to a coarse package level pitch of typically 200μm or more. Besides the difficult manufacturability and the reliability issues associated with these long and narrow pitched wires, electrical parasitic effects become important. Moreover, wire bonding technology is mostly limited to peripheral array interconnections.

1.2.2 Flip-chip Solder Bumping

One way to overcome the parasitic effects related to wire bonding is the use of flip-chip bumping technology. This technology is especially suitable for high speed, high frequency or high I/O count applications. However, downscaling traditional solder bump interconnects to very fine pitches of the order of 50 microns or less is not expected to satisfy the thermo-mechanical reliability requirements. A brief discussion on various solutions offered in response to the above needs is as follows.

1.2.3 Compliant Interconnects

Compliant Wafer Level Packages have offered a solution to the shortcomings of underfill and flip chip technologies. They do a better job than most technologies at satisfying the mechanical requirements of high performance micron sized interconnects. However, this mechanical reliability comes at the cost of electrical performance which is again compromised due to lengthy connections as in the case of wire bonds.

1.2.4 Stud Bumping

Stud bumping or ball bumping is done by transferring the bump onto a bonding pad from a wire using a modified wire bonding process. In a typical wire bonding process, a gold ball is forced down and thermo-sonically bonded to a die bond pad to form the first connection in a wire bond. With the ball connected, the wire is then fed out and attached to a second surface to complete the connection. The ball bumping process is a variation of this wire bonding operation. In the ball bumping process, the wire is snapped off after the ball is initially connected to the die. The resulting gold bump (also known as a stud), is firmly connected to the first surface. Because of the maturity of the wire

bonding process, the reliability of these bump connections is well established and documented. Stud bumping, however, has several shortcomings. It is not a wafer level process and as the number of I/Os increase, the cost of gold stud bumping increases. The coplanarity of the bumps across the whole die is a problem in case of stud bumping and additional steps are required to fix the problem. The bumps are not flat and the shape of the bumps cannot be controlled. A separate coining machine and additional step to flatten the bump may be required.

1.2.5 Underfills

Undefills are typically used to increase the reliability of flip-chip packages. Although with a decreasing pitch and consequently a decreasing ball size, the joint gap between the substrate and the die decreases to the point that it may become very difficult to flow underfill completely under the die. At 100 μm pitch, the gap between the die and substrate could be significantly less than 25 μm, the limit of underfill flow. For these very fine-pitch applications, an alternative underfill technique will need to be developed or flow under the chip will not be possible. One alternative would be to deposit the underfill material on the wafer immediately after flip-chip solder bumping. Achieving high filler loading witn no-flow underfills is critical to achieve the optimum CTE and modulus. New nanocomposite underfill materials and processes are being developed to implement this process. Use of underfill can also exert significant peeling stresses on the die, bump and package substrate. These peeling stresses are a concern for chips using low-k dielectrics. In general, low-k dielectrics are softer and have weaker adhesion properties than oxide, so they are more prone to delamination.

1.3 Copper interconnect proposal for chip-last and 3D packaging technologies

As discussed above, solder has been the traditional choice for SMT and flip chip interconnections in spite of its poor mechanical properties and electrical performance-mechanical properties trade-offs and process constraints. Compliant leads made of solder or other materials solve the mechanical reliability but with higher parasitics. With the trend towards shorter interconnections, fine pitch and higher I/O density, there is a need for more innovative interconnect solutions to overcome the limitations of solder bumps. This gap between future requirements and current technologies is succinctly illustrated in Figure 1.5.

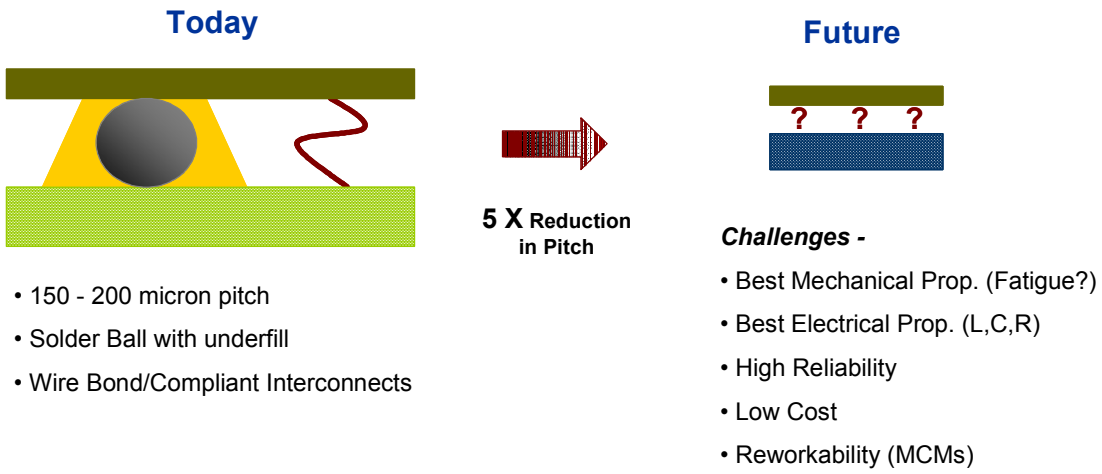


Figure 1.5 ***Current area-array interconnect technologies and future requirements.***

In order to address these issues with chip-first and chip-last, GT-PRC has proposed a chip-last embedded active approach [6]. Here the chips are embedded after all the build-up layer processes are finished. For the interconnections, ultra-fine pitch Cu-Cu bonding using advanced nano-conductive and non-conductive adhesives are used to enable shortest interconnect with the best electrical and thermo-mechanical properties. To

minimize the processability and reliability problems associated with solder based flip chip assembly at fine-pitch, Copper interconnections with nano-conductive adhesives and non-conductive adhesives have the potential as a candidate for replacement of solder. This approach has several advantages such as:

1) Low modulus adhesive can accommodate strains and thus improves reliability at ultra-fine pitch.
2) No bridging problems because of the non-reflowable metal post.
3) Lower bump temperature, uniform current distribution and thick UBM that helps in the electro-migration aspect.
4) Ultra-fine pitch assembly with adhesive serving as underfill as well.
5) Sintering of nano-filler particles at the curing temperature enables a reliable metallurgical connection with stable contact resistance.
6) Flexibility of bumping with various shapes and sizes; thus enhancing the performance of the flip chip assembly.

The proposed copper-copper based interconnects using advanced conductive and non-conductive adhesives will be a new fundamental and comprehensive paradigm to solve all the four barriers: 1) I/O pitch 2) Electrical performance 3) Reliability and 4) Cost. The new approach involves the use of fine-grained copper based interconnections for high fatigue resistance compared to solders, ultrahigh current carrying capabilities and lowest electrical parasitics.

The I/O pitch challenge is being accomplished by fabricating these interconnects at a pitch of 30 microns. The high electrical performance is obtained from the lowest capacitance, resistance and inductance of the interconnections that can be shortened as required. The high reliability comes about by low modulus adhesive that accommodates strains. It also comes about from better fatigue resistance and strength of fine-grained copper. Low cost comes from wafer level packaging—a process by which the entire wafer is deposited with copper interconnections with a few lithographic steps. This thesis develops and demonstrates low-cost nanoadhesive based bonding layers for ultrafine pitch interconnections of 30 micron pitch.

1.4 Objective and organization of thesis

The objective of this research, guided by the trends and the challenges described above is to explore the potential on providing extremely large number of interconnections between ICs in a system by means of ultrafine-pitch copper interconnections using advanced adhesives. The final goals of this research are 1) to explore ultrathin interconnections (8-10 microns height) at ultrafine-pitch (30 microns) using electroplated copper bump and advanced conductive and non-conductive adhesives, and 2) to demonstrate reliability and processability enhancement with Cu bumps at fine-pitch compared to existing conventional solder bumps. In this approach, the best electrical properties come from the ultra-small interconnections enabling ultra-high speed signal transmission. The mechanical integrity and reliability come from the low modulus adhesive that accommodates strains. It also comes about from better fatigue resistance and strength of fine-grained copper compared to existing conventional solder bumps.

Wafer level packaging of ICs is expected to be cost effective since copper interconnections are deposited on the entire 300 mm wafer with thousands and possibly millions of connections.

The approach is to fabricate ultrafine-pitch copper interconnections using fine-grained copper electroplating to get flat, smooth and coplanar copper bumps and to assemble those onto glass substrates to evaluate their reliability by subjecting them to Highly Accelerated Stress Test (HAST) and High Temperature Storage (HTS). Failure analysis is carried out to determine the failure locations and failure mechanisms and to compare and contrast NCF and nano-ACF as a potential candidate for ultrafine-pitch flip chip binding.

Chapter 2 provides a discussion on various issues discussed in literature with regards to the work described in this thesis. This starts with the challenges associated with next-generation-chip to package interconnections; discussed both in terms of materials and process challenges. Long term R&D challenges from roadmaps emphasizing the need for reduction in pitch and increase in I/O count are presented in detail. Limitations of solders as we go to finer pitches and justification of copper as an interconnection material is discussed and compared with solders in terms of electrical and mechanical performance, wafer process compatibility, electromigration resistance, cost, and fine pitch compatibility. State of the art copper pillar/post/bump technology and emerging direct copper-copper bonding have been discussed in light of the need for high I/O density and trend towards 3-D packaging. The chapter concludes with with a

discussion on advanced conductive adhesives as a promising candidate for fine-pitch interconnections.

Chapter 3 presents test vehicle design for the 30 micron pitch interconnections. The chip layouts for the 3 mm x 3 mm, 30 micron pitch peripheral array of copper interconnections and the substrate layouts for matching glass substrate are presented.

Chapter 4 describes the advanced materials and processing techniques that were used to fabricate the 30 micron pitch interconnection test vehicles. The chapter begins with the description of photolithographic processes, followed by a discussion on plating bath composition used to deposit the fine-grained copper for interconnection formation. The chapter concludes with a description of fabrication process used for making the matching glass substrates for the dies in order to assemble the test vehicles for reliability characterization.

Chapter 5 covers the results and discussion based on the experimental techniques discussed in chapter 4. It shows the fabrication results for chips and substrates at 30 micron pitch. This is followed by description of assembly processes with advanced conductive adhesives and assembly process optimization at ultrafine-pitch of 30 microns using NCF and n-ACF. HAST and HTS reliability results and failure analysis are presented followed by appropriate discussion based on the results.

Chapter 6 summarizes the work and makes final conclusions followed by suggestions on areas in which future work can be carried out in order to further explore the concept and to examine the viability of using advanced conductive adhesives for next-generation micro-systems packaging.

2. LITERATURE REVIEW

This chapter discusses the material and process challenges as we move towards finer pitch chip-package interconnections. The chapter begins with a thorough review of long term R&D challenges from roadmaps emphasizing the need for reduction in pitch and increase in I/O count. Further discussion reveals the limitations of solders as we go to finer pitches and justifies the need for new interconnection materials. Copper as an interconnection material is discussed and compared with solders in terms of electrical and mechanical performance, wafer process compatibility, electromigration resistance, cost, and fine pitch compatibility. State of the art copper pillar/post/bump technology is then reviewed in detail. Emerging direct copper-copper bonding has been discussed in light of the need for high I/O density and trend towards 3-D packaging. Most direct Cu-Cu bonding techniques are high thermal budget, high temperature processes which are not compatible with other packaging processes and thinned-down dies for embedded actives. The chapter concludes with a discussion on advanced conductive adhesives as a promising candidate for fine-pitch interconnections.

2.1 Long Term R&D challenges from Roadmaps

The semiconductor industry closely follows the International Technology Roadmap for Semiconductors (ITRS) that projects the need for several technology generations. The package interconnections must be capable of overcoming these projections if these technologies have to be successful because these roadmaps are now perceived to be conservative projections. This section discusses different challenges that

will be faced by any new WLP (Wafer Level Package) technology in terms of meeting the requirements of the ITRS roadmap [7] Different technology markets will have varying needs in terms of these issues. High performance applications have the highest I/O requirement of all the markets. The size of the die is assumed to be the size of WLPs. Minimum pitches are used to calculate the number of I/Os supported by a particular WLP technology. The predictions of ITRS roadmap in terms of interconnect pitch for three main interconnection technologies in use today are tabulated in Table 2.1. The ITRS 2006 Assembly and Packaging roadmap summarizes their picture of challenges and issues in Table 2.2.

Table 2.1 2006 ITRS Roadmap for Interconnect Pitch (µm)

Year	***2008***	***2009***	***2010***	***2015***	***2020***
Wire bond	35	35	30	25	25
Area Array Flip Chip	130	130	120	100	85
Peripheral Flip Chip	25	20	20	15	15

Table 2.2 Assembly and packaging difficult challenges beyond 2010 (re-written table 93b from ITRS 2006 Assembly and Packaging roadmap) [7].

Difficult challenges beyond 2010	**Summary of Issues**
Package cost does not follow the die cost reduction curve	Margin in packaging inadequate to support investment required to reduce cost

Table 2.2 continued	
Small die with high pad count, High power density, and/or high frequency	Current density, operating temperature, etc for these devices exceed the capabilities of current assembly and packaging technology
High frequency die	Substrate wiring density to support >20 lines/mm; Lower loss dielectrics—skin effect above 10 GHz;
Close gaps between substrate technology and the chip	Silicon I/O density increasing faster than the package substrate technology. Production techniques will require silicon-like production and process technologies.
System-level design capability to integrated chips, passives, and substrates	Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. Embedded passives may be integrated into the "bumps" as well as the substrates.
New device types (organic, nanostructures, biological) that require new packaging technologies	Organic device packaging requirements not yet defined; Biological interfaces will require new interface types; Bumpless area array technologies will be needed during this period. Face to face packages and other

Table 2.2 continued	
	3D packages are examples. High frequency, low power and low profile are driving forces.

ITRS 2006 table 93b comments that "Production techniques will require silicon-like production and process technologies after 2005". A challenge and an opportunity exist here to find ways around this bottleneck, avoiding involving the more expensive silicon-like production and process technologies. An obvious challenge is that new device types (organic, nanostructures, biological) put different requirements on packaging technologies and especially on the temperature and chemical environment excursions during processing. Especially biological, but also organic materials with interesting properties cannot be involved in many of today's processes. Process-design and process compatibility will therefore be much more important in the future. New processes need to avoid high temperatures and probably often exclude also vacuum steps for both compatibility and cost reasons. Organic materials that are specifically designed to avoid out-gassing and degradation under these circumstances will find more use in future [8].

2.2 Fine Pitch Interconnection Trends and Challenges

Miniaturization at system and component level is plagued with myriads of electrical challenges. Integration of over a billion transistors on high end microprocessors witnesses interconnection scaling challenges that include issues related to degradation of resistivity, material integration, planarity control, high aspect ratio via and wire coverage,

and reliability problems due to electrical, thermal and mechanical stresses in a multilevel wire stack [7].

According to the International Technology Roadmap for Semiconductors (ITRS 2006), the transition in electronic industry will cause nanochips with less than 32 nm nodes, in excess of 10000 I/Os and pitch down to 20 μm [7, 9]. An evolution of packaging technology in last four decades is shown in Figure 2.1. With such downscaling of the feature size, signal integrity, interconnection delay, parasitics, mechanical stability of the interconnections and electromigration become utmost important.

SIP technology has shown potential to address abovementioned issues by enabling vertical integration of devices and allowing significant reduction in interconnect length and thus high packing density [10, 11]. Heterogeneous device integration (e.g., logic, memory, analog, sensors, microfluidics, and power sources) at wafer-scale will push the interconnection pitch to 2-10 microns and terabit bandwidth. The ITRS roadmaps are believed to be more conservative in this regard.

Table 2.3 compares intrinsic interconnection delay with transistor switching delay at different technology nodes [G8]. As the nodes become smaller, evidently interconnection delay becomes more prominent. At 35 nm node, the intrinsic delay surprisingly becomes two order magnitudes higher than the transistor delay. SIP technology has shown potential to address abovementioned issues by enabling vertical integration of devices and allowing significant reduction in interconnect length and thus

high packing density [10, 11]. Heterogeneous device integration (e.g., logic, memory, analog, sensors, microfluidics, and power sources) at wafer-scale will push the interconnection pitch to 2-10 microns and terabit bandwidth.

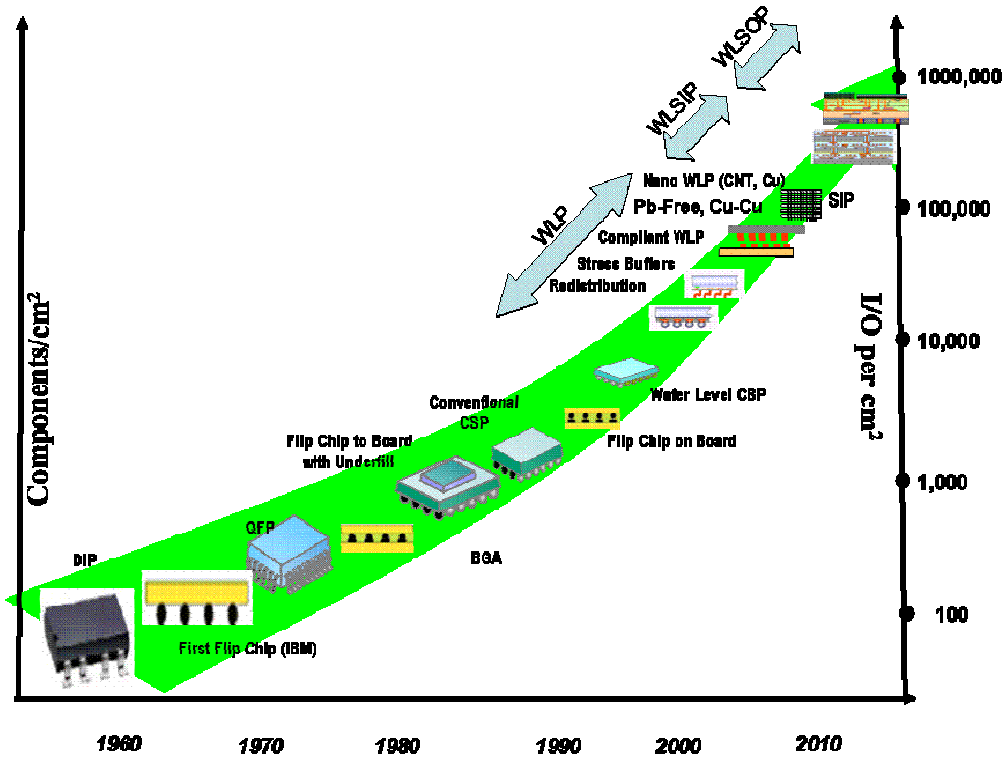


Figure 2.1 Evolution of IC packaging [9]

Table 2.3 Transistor and interconnect delay at different technology nodes [12]

Technology Node	MOSFET Switching delay (ps)	Intrinsic delay of minimum scaled 1mm interconnect (ps)	Intrinsic delay of reverse scaled 1mm interconnect (ps)
1.0 µm (Al, SiO_2)	20	5	5
0.1 µm (Al, SiO_2)	5	30	5
35 nm (Cu, low K)	2.5	250	5

The trend in flip-chip interconnect pitch indicates that the current 150 μm pitch for area-array packages will shrink to 90 μm by 2010. The driving force for this pitch shrink is to satisfy the requirements for high-performance silicon devices. These requirements include a dramatic increase in the number of I/Os due to increase in the number of signal lines and power requirements. Higher power devices require more signal and ground lines and, to limit point sources of heat, the power and ground interconnects should be spread evenly across the area array.

2.3 Traditional interconnection approaches, limitations and the need for copper-based interconnections

Solder interconnection based assembly was introduced three decades ago by IBM as the C4 technology. Since then, the success of flip chip technology (assembly with the active die facing the substrate) resulted in several advances in the solder bump assembly. Solders are well-characterized and well-qualified materials for power consuming digital applications that use high current densities and large dies (1-2 cm^2). They are more forgiving towards nonplanar substrates and are therefore ideal for organic packages. The solder pitch has shrunk to less than 150 microns pitch, and is expected to move to even smaller pitches.

2.3.1 Eutectic Sn/Pb Fine-Pitch Solder bumping at 50 micron Pitch

Some of the latest advances in fine pitch solder interconnections are covered here where high-density packaging and interconnection of IC's are achieved through controlled design and manipulation of flip-chip solder bumps and IC orientations.

MCNC (Research Triangle Park, NC, now RTI International) has developed a fine-pitch Sn/Pb solder bumping process that is capable of reliably fabricating 25µm bumps on 50µm pitch, as well as flip-chip assembly methods that allow the construction of multi-chip modules of sensor – readout circuit pairs [13]. Their process relies on an electroplating method to form the solder bumps, which gives tremendous flexibility in processing conditions and excellent wafer-level uniformity (Figure 2.2). The very nature of fine pitch flip chip assembly creates several issues associated with flux residue removal after reflow. This problem was completely eliminated here by the use of Plasma Assisted Dry Soldering (PADS) process during assembly. PADS is a plasma treatment process that reacts with the Sn oxides on the surface of Sn-bearing solders. The Sn oxides are converted into a compound that breaks up as the solder melts during reflow, exposing unoxidized solder to the bond pad, allowing full solder wetting to occur. Reflow is done in a conventional nitrogen-inerted belt furnace that prevents the reoxidation of the solder during the bonding process.

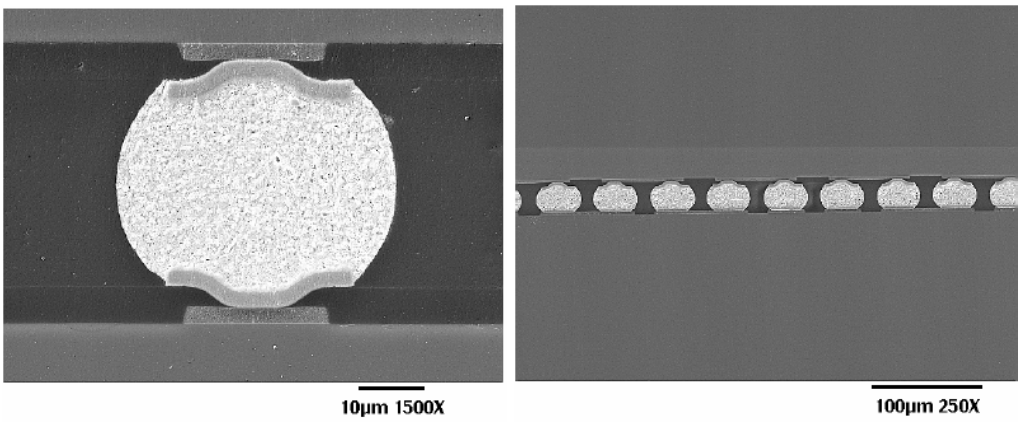


Figure 2.2 Cross-Section of Joined 25µm Bumps.

There are a number of materials and processing challenges associated with finer pitches. As the pitch shrinks, the methods to deposit the solder become more limited.

Solder paste is very difficult to deposit using a silk-screen method at pitches below 150 μm due to rheological limitations of forcing a semi-solid (paste) into small holes (silk screen). Evaporation is difficult because developing a metal screen mask with the required tolerances is prohibitively expensive. Solder plating is still a good option, but the solder must be very uniform across each die and current electroplating chemistries for binary and ternary solder alloys do not provide a tight control on plated alloy compositions. Solder ball uniformity is also critical because large variations between die could result in electrical opens for small balls and shorts for large balls. (Figure 2.3).

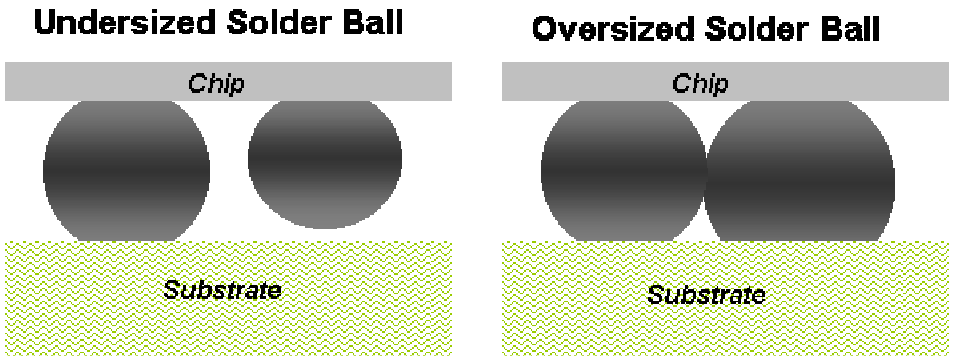


Figure 2.3 The uniformity of ball size on the flip chip is important. (a) If the ball is undersized, electrical opens occur. (b) If the ball is oversized, electrical shorting is possible.

An additional issue with a decrease in ball size is the stand-off height between the substrate and the die decreases to the point that it may become very difficult to flow underfill completely under the die. At 100 μm pitch, the gap between the die and substrate could be significantly less than 45 μm, limiting the flow of underfill. For these very fine-pitch applications, an alternative underfill technique will need to be developed or flow under the chip will not be possible. One alternative would be to deposit the underfill material on the wafer immediately after flip-chip solder bumping. New underfill materials and processes would have to be developed to implement this process.

2.3.2 Stress-relief with solders

Flip Chip Technologies has developed a unique stress-relief structures to enhance the solder joint reliability. Only one technique, reinforcing polymer structure that surrounds the solder ball neck at the die surface, called Polymer Collar, is discussed here. Their intent was to improve the board level reliability by reinforcing the interface between the solder ball and UBM surface. This technology is believed to be highly compatible with high volume manufacturing with a minimal cost adder. Due to this significant improvement in board level reliability, the Ultra CSP™ Polymer Collar™ enhancement is expected to become a standard part of FCT's RDL and Bump technology. Figure 2.4 provides a visual comparison between FCT's standard Ultra CSP™ bump and a bump with Polymer Collar [14].

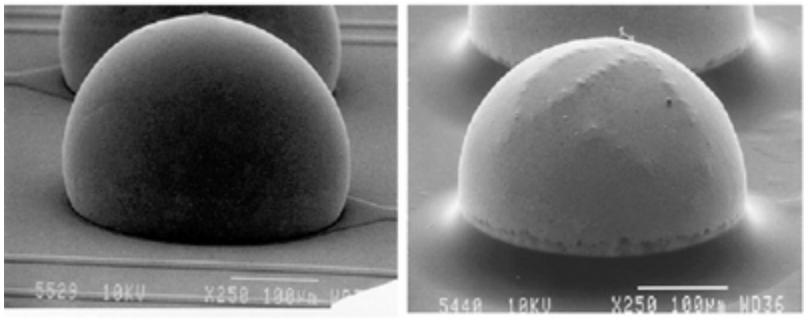


Figure 2.4 FCT's Standard vs Polymer Collar Ultra CSP.

Much emphasis is being put on attaining finer pitch interconnections. However, some novel advances presented here offer unique solutions to the IC interconnect challenges. Newly available commercial materials offer the required processing advantages to solve a host of limitations for fine pitch interconnections. The materials of thick photo-resists improve efficiency for solder bumping and wafer thinning by accomplishing the required thickness with only one coat. Together these improvements

translate to fine pitch interconnections at lower process costs. An approach to achieving the bumping of wafers thinned to 100 microns has also been shown. Design ideas for controlled variable height solder bumps, buried bumps and on-edge 3D chip assembly have resulted in some unique solutions to advanced packaging interconnect challenges.

2.3.3 Micro C-4 Interconnections

An increase in the area array density of interconnections demands has driven a constant decrease in the pitch/diameter of the solder bumps. IBM had recently demonstrated semiconductor test chips and silicon carrier test vehicles with 50µm µ-C4 diameters on a 100µm pitch and 25µm micro-bump diameters on a 50µm pitch compared with typical industry standards of 100µm solder bumps on 200µm or 225µm pitches (Figure 2.5). This advance using µ-C4 interconnection represents a 16 times improvement in I/O area density over a standard flip-chip array with 200µm pitch. A range of solder and various ball-limiting metallurgies (BLMs) were explored, including high melt solder, PbSn (97/3), eutectic PbSn (37/63), Pb-free solder (Sn/Ag/Cu family of solders), and gold–tin [AuSn (80/20)]. Ball-limiting metallurgies included compositions such as TiW/CrCu/Cu/Ni/Au, Cr/CrCu/Cu/Au, Ti/Cu/Ni/Au, Ti/Ni/Au, Ti/Cu, Cr/Cu/Cu/Ni/Au, and others considered to be dependent on the solder interconnection. [15]

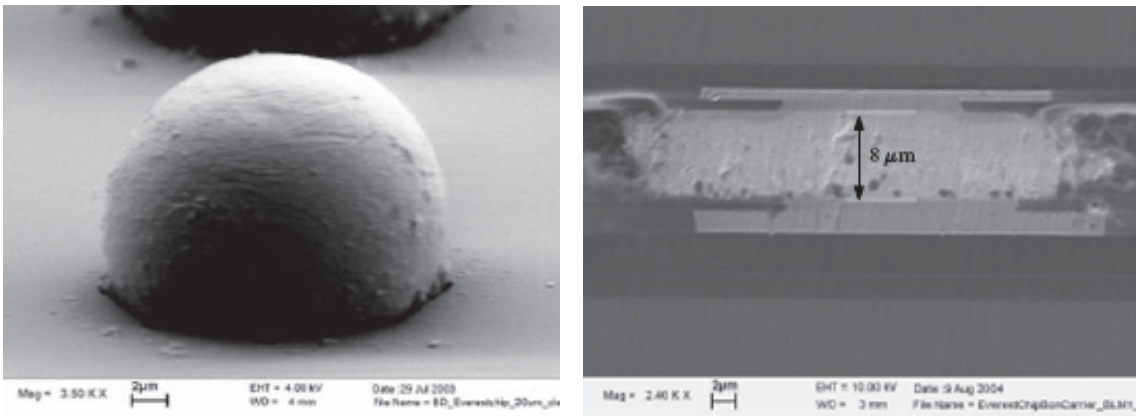


Figure 2.5 (a) Examples of microsolder bumps in which microbumps are approximately 25 µm in diameter on a 50µm pitch, (b) Cross sections of silicon on silicon at 50µm pitch with multiple solder connections (left) and one 25 µm wide solder connection.

2.3.4 Ultra-thin Soldered Flip Chip Interconnections on Flexible Substrates

Flip chip assembly of silicon IC´s on flexible substrates has gained more interest in the last years. Fraunhoffer recently demonstrated an immersion soldering process (a cost effective maskless bumping process) for thin solder layers on flip chips with assembly on thin flexible substrates (Figure 2.6). Test chips were bumped using immersion solder bumping technology to create thin solder caps down to 40 µm pitch. Thermode bonding was shown as a promising fast flip chip technology for thin soldered contacts on flexible substrates. They studied two different solder materials in combination with no-flow underfill materials for flip chip contacts of less than 10 µm height. Since the reliability of thin solder joints is a key issue, the failure mechanisms and the ageing behavior were described. They showed that the inter-metallic phase formation has a large influence on joint reliability because the intermetallics consume the majority of the solder alloy. [16]

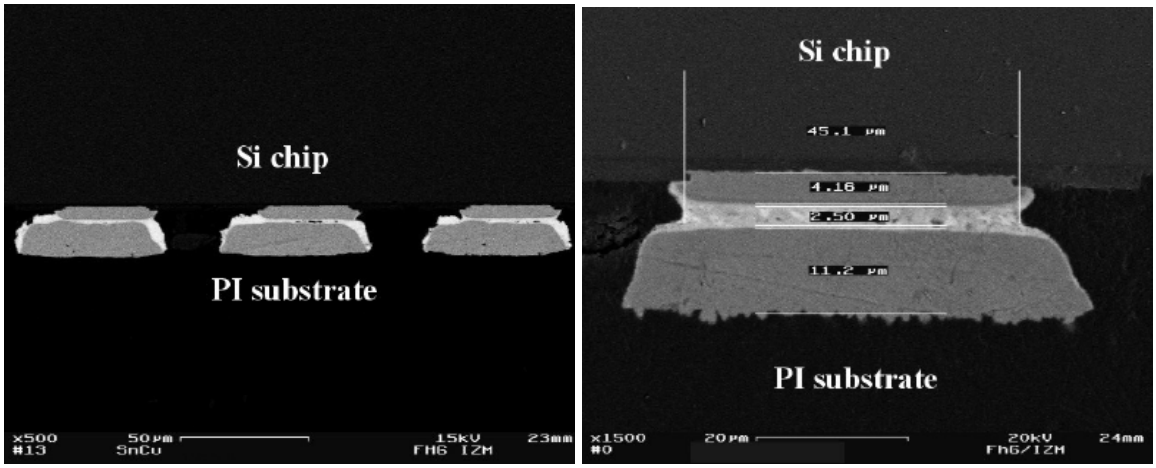


Figure 2.6 SEM picture of SnCu soldered interconnections 60 µm test vehicle in initial state after thermode bonding.

2.3.5 3D Embedded Components in Organic Packages

Shinko has shown embedding of ultra-thin silicon components into the organic substrates using a "chip-middle" approach. Their embedded package uses low cost manufacturing process with the conventional build-up substrate process and materials (Figure 2.7). They have demonstrated two kinds of chip mounting processes (face-up mounting, flip-chip mounting) in the substrate, and have studied the key technologies (simulation of stress, wafer thinning, interconnection of embedded chip) for the manufacturing of such packages. They showed that thinner and smaller chip is suitable for embedding the chips in organic substrates, since the thin chip becomes flexible, and the stress in the interconnect joints is relaxed. [17]

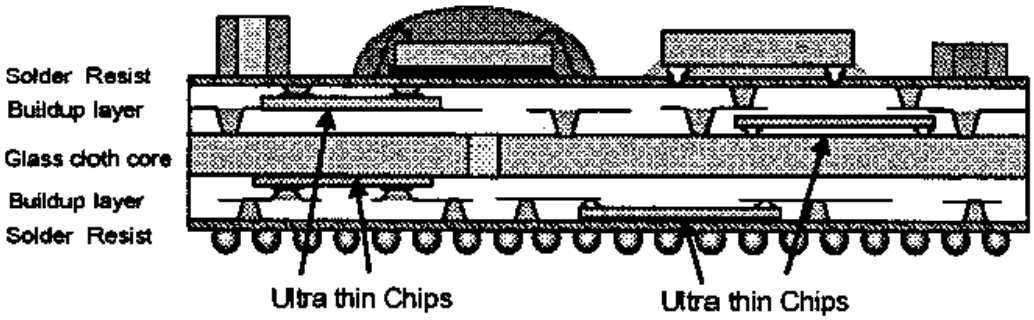


Figure 2.7 Structure of Shinko's embedded organic package.

2.4 Limitations of Solders and the Need for Novel Interconnection Materials

Solder has been the most prevalent choice for SMT and flipchip interconnections for more than two decades. This is due to several reasons such as low- temperature processing, low material and process cost, excellent wettability to metals and alloys, corrosion resistance, self-alignment, among others. But the emerging applications and environmental concerns are forcing the industry to consider other interconnection materials, processes and structures. One such application is the new need for computer and communication technology for highest system performance not by the operating frequency of a single processor but by multicore processors, aggregately providing highest data rates at lowest power. These multi-core architectures are pushing the I/O density to more than 10,000/cm^2 and pitch to less than 50 microns. Decreasing I/O pitch is, in fact, one of the key technological barriers identified by the 2006 International Technology Roadmap for Semiconductors (ITRS) [7]. The other application driving a different need for off-chip interconnection is for ultra thin and small RF modules with embedded actives and passives, not requiring any stand-off height. These and other

applications, on one hand, and packaging at wafer-level, on the other hand, offer new interconnection opportunities.

Current solder-based approaches for chip-to-package interconnections either limit the pitch or result in electrical performance-mechanical reliability trade-off in properties. Compliant leads made of solder or other materials solve the mechanical reliability but at the expense of electrical performance. The electrical and miniaturization requirements with today's embedded active and 3D technologies dictate that the interconnect height be lowered from today's 100 microns to less than 25 microns over the next few years. While the electrical performance dictates shorter interconnections, the fatigue life of a flip chip solder interconnection is proportional to the vertical stand-off height (interconnection height) between the chip and the substrate. For low-strength and low fatigue resistance materials such as solders, taller and bulky bumps are required to keep the solder strains low. The trend towards lead-free solders aggravates the stresses in the solders because of their higher reflow temperatures. The increased tendency for intermetallic formation with lead-free solders leading to poorer mechanical properties is only worsened with electro-migration assisted mass transport, leading to several reliability issues at fine pitch.

The interconnect signal delay between the IC and the package and the thermomechanical reliability depends strongly on the interconnect material used. Materials with lowest resistivity that are processable and manufacturable, and yet maintain superior mechanical properties at assembly and operating temperatures become a logical choice for the interconnect system.

The stress-strain behavior of solders is compared with copper in Figure 2.8. Figure 2.9 compares the stress-strain behavior of micro-copper and nano-copper. (Shubhra et al). Solders are weaker materials with much lower yield stress, leading to much higher plastic strains for the same stress. The strength of solders is ~40 MPa compared to micro- and nano-copper which are 4-10 times stronger.

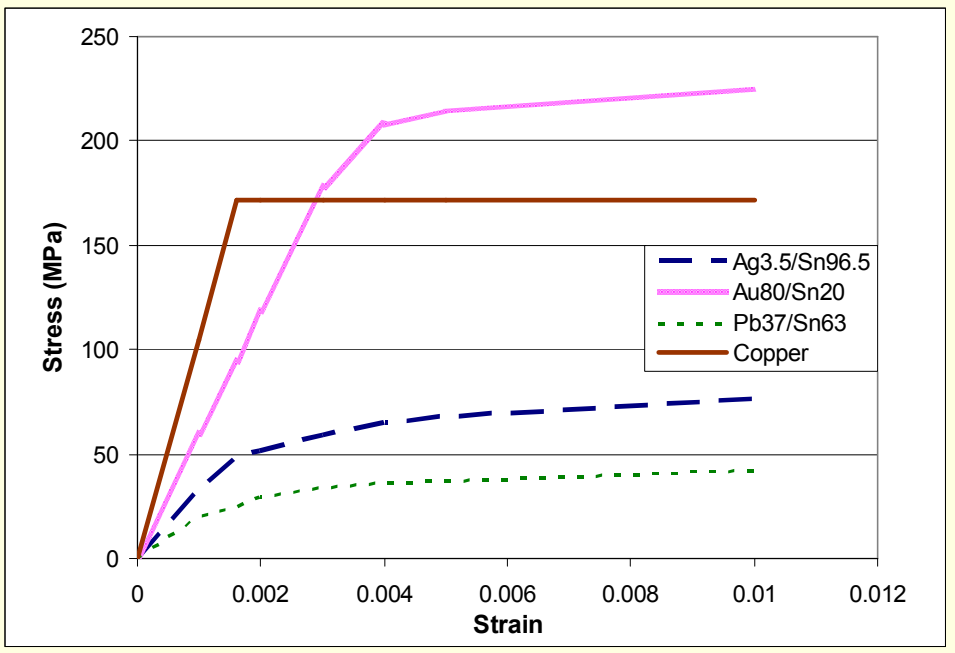


Figure 2.8 Stress-strain curves for solders, copper and Au-Sn braze. [18]

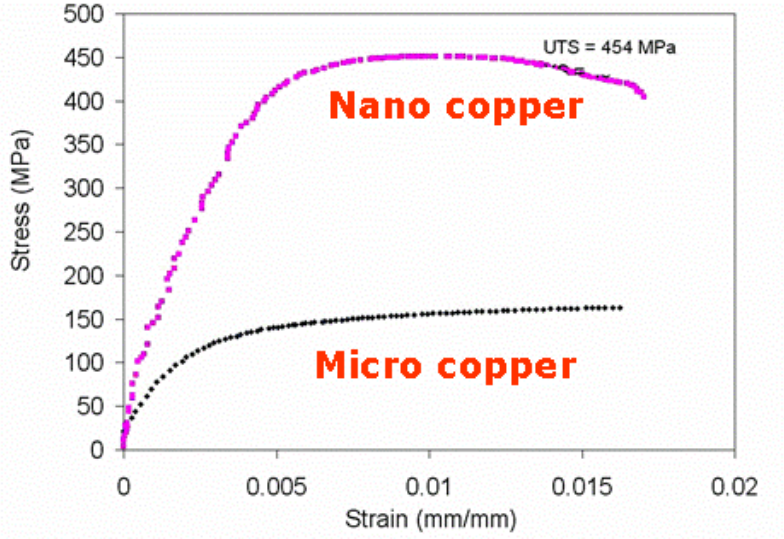


Figure 2.9 Stress-strain curves for solders, copper (Shubhra et al)

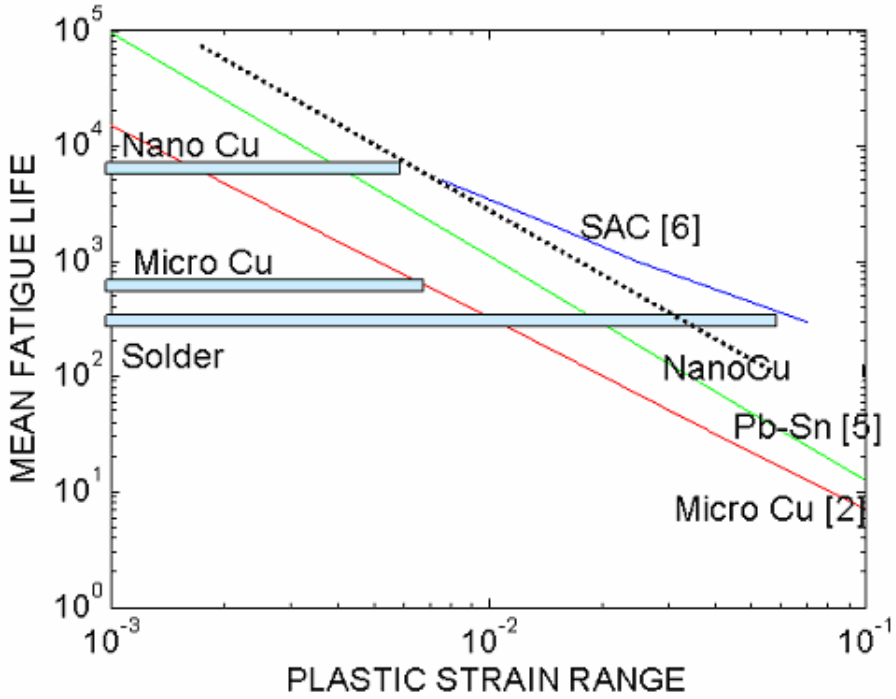


Figure 2.10 Mean fatigue life vs. plastic strain range for solders and copper. The strain values are chosen from literature sources for solders and are rough estimates for copper.

The plot for fatigue life vs. plastic strain range using literature data (except for nano-copper) is shown in Figure 2.10. The strain range for copper is expected to be lower because of its higher yield stress compared to solder, leading to improved fatigue life as seen from the figure. The inferior mechanical properties of solders are also compared with copper through the dynamic fatigue or crack growth rate behavior. Coffin-Manson-type equation, derived using experimental data for electroplated copper [19] and eutectic solders are summarized in Table 2.4.

Table 2.4 Coffin-Manson fatigue models for plated copper, eutectic (Pb-Sn) and lead-free solders.

Copper	$N_f^{-0.6} \; X \; E_f^{0.75} = \Delta E_p$	N_f: Mean cycles to failure ΔE_p: Plastic strain range E_f: Fatigue ductility coefficient The fatigue ductility coefficient for copper was reported to vary from 0.15 to 0.3 [20].
Eutectic solder	$Nf = 0.146\ \Delta E^{-1.94}$	N_f Mean fatigue life; ΔE: Plastic strain range; [21]
SnAgCu solder	$N_f^m \; X \; \Delta \; E_p = C$	Data obtained from Pang et al. [22]

Advantage of copper as a good electrical conductor is undisputed. Conductivity of pure copper is 5.96 x 10^7 $Ohm^{-1}.m^{-1}$ as compared to a conductivity of 6.9 x10^6 $Ohm^{-1}.m^{-1}$

for Pb-Sn eutectic solders. In addition, copper has good electro-migration stability that renders high current carrying capability to the interconnects.

Electro-deposition of copper is one of the methods most generally employed to obtain metallic films of adequate thickness, porosity-free structure and good adhesion [23-25]. Electrodeposited copper films have been widely investigated with respect to their morphological characteristics, electrical properties and corrosion resistance [26, 27]. By controlling variables such as current density, applied current signal, temperature, bath composition, etc., a variety of films with different characteristics can be achieved, thus allowing to tailor the mechanical characteristics of the films for specific applications. It is well known that one of the ways to control the structure of the electrodeposits is to adjust the current density during dc plating or to apply a periodically changing current signal. In the first case, films of different grain sizes can be achieved, even in the nanometer range if sufficiently high current densities are applied. In the case of a periodically changing current, i.e., periodic electrolysis, different morphologies can be obtained. It has been established that this kind of electro-deposition technique leads to beneficial morphological effects such as smoother, more uniform and more compact deposits [28-30]. This being the case, if different structures showing suitable morphologies can be formed, different and maybe better mechanical properties can be tailored.

It can be concluded from the above discussion that copper is an excellent candidate material for next generation of chip-package interconnections because of its high electrical and thermal conductivities, good mechanical properties at assembly and

operating temperatures and well-established infrastructure to integrate with back-end processes with electroplating technology downscalable to nanoscale. This technology can also accommodate the increasing I/O density of future microprocessors with the best electrical and mechanical performance. In addition, embedment of active components with chip-last approach being proposed by Georgia Tech PRC can also be realized with the shortest interconnections resulting in performance and miniaturization comparable to chip-first approach. There is an increasing trend to replace solders with copper because of these advantages.

2.5 State of the art Copper pillar/post/bump technology

Due to the fine-pitch limitations of solder bumps, companies and universities worldwide are exploring copper pillars or posts as a potential solder bump replacement. The Microsystems packaging research center at GaTech (GT-PRC) has been spearheading a comprehensive research in the area of copper pillar/post/bump interconnect technology by bringing new concepts and technologies to achieve ultra fine pitch wafer level packaging. Figure 2.11 shows a schematic drawing of the PRC strategy for the interconnect paradigm change for the wafer level packaging from the current 150-225 micron pitch assembly towards finer pitch in the range of 20 μm to 50 μm with more than 10,000 I/Os [31].

Next generation IC-package interconnect requires a technology that is low cost, reworkable, possesses good electrical properties, good reliability, and is easily testable at

the wafer level with good co-planarity. Downscaling traditional solder bump interconnect to very fine pitches of the order of 30 microns and less will not easily satisfy the thermo-mechanical reliability requirements. To achieve the requirements of very fine pitch (as projected by ITRS) with conventional interconnections and materials, we have to accept a trade-off in electrical and mechanical performance and possibly cost.

Table *2.5* below summarizes the advantages of copper pillar over solder and compliant interconnections.

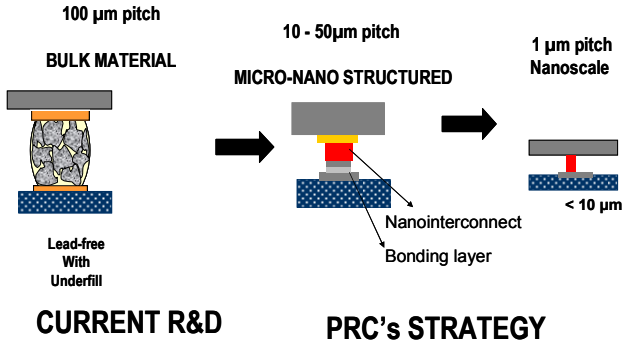


Figure 2.11 PRC's vision of Copper Interconnection strategy.

Table 2.5 Advantages of copper pillar over solder and compliant interconnections.

Properties	Solder	Compliant	Nano Interconnect
Best Electrical	✓	X	✓
Best Mechanical	X	✓	✓
Manufacturability	X	X	✓
Reworkability	✓	X	✓

Copper Pillar Bump offers performance and process advantages to the flip chip interconnection system. Most semiconductor foundries are now equipped with advanced copper electroplating systems that can be easily integrated with the back-end processes. In addition, the flexibility that the bumps can be manufactured in various shapes and

sizes further increases the current and heat capacities. As only solder is reflowed to create the joint, a consistent standoff can be maintained through the non-meltable copper portion, which further enables the downstream processes of flip chip packaging. For example, it can provide a wider window for underfilling process, and also a maskless substrate can be used.

Electromigration in solder bumps was discovered to be one of the key reliability issues in flip chip technology. As the power continues to increase, the electrical current through the bump increases leading to higher bump temperature. The bump temperature is reaching a level where electromigration is becoming a severe concern. Joule heating is dependent on the material resistance. It has been studied that the failure of solder bumps is induced by rapid dissolution of the UBM, and the effect of current crowding causing assymetrical UBM dissolution. The effect of electromigration can be improved with copper pillar Bumps.

Copper is first deposited on the metal pad of semiconductor chip, which provides a consistent standoff for the flip chip interconnection system. One way to bond copper is by solid state bonding of copper to copper as Suga et al. has reported [32]. This technology requires a very high degree of planarity and smoothness. In the short term, lower melting point solder alloy can be deposited on the free end of the copper post to provide an electrical joint to the next interconnection level. The tall and slim structure of copper pillar bumps enable fine pitch solder interconnections with good reliability performance. Conventional solder bump has a limitation to fine pitch due to the shape of

solder after reflow. There will be a drawback on the standoff height, and thus reliability performance, in order to reduce the solder bridging.

Heinen et al., as early as 1989, demonstrated solder capped copper bumps for multichip module application [33]. In Fujitsu's *Super*CSP [34], the interconnect standoff and, thus, the compliance was enhanced by adding a copper post under the solder bump, which together with an encapsulant layer with CTE close to that of the mother board, effectively reduced the strain induced in the solder joint. To increase the compliance further and eliminate the use of underfill, Liao et al. reported a modified copper-column-based interconnect called multi-copper column (MCC) interconnect which consists of multiple copper columns in parallel and supporting a solder bump [35]. Based on a simple analytical model, correlating the interconnect geometry and the thermal fatigue life, MCC interconnections were predicted to have higher compliance and thus higher thermo-mechanical reliability, while the associated electrical parasitics at dc and moderate frequencies were still kept low. Charles et al. demonstrated the use of electroplated copper pillars for first and second level interconnections in 3D stackable packages [36].

Park et al. compared the thermo-mechanical behavior of copper column grid array (CuCGA) and conventional ceramic tin-lead column grid arrays (CCGA). Although accumulated plastic deformation per cycle was bigger in tin-lead columns compared to copper columns, CuCGA failed first because the crack propagation in the CuCGA package was along the copper-solder interface while tin-lead column had failure in the

solder column itself. They concluded that the fatigue resistance of the lead-free solder fillet, used to bond copper column to substrate, is inferior to that of the copper column itself and the Cu-Sn intermetallic is weaker and brittle compared to Pb-Sn solder [37]. Based on a FEM study, Yamada et al. found [38] that the maximum strain region in the copper column based solder bump was distributed at the edge of the copper column. Furthermore, the thermal fatigue lifetime of copper column based solder bump increased the flip-chip interconnection reliability and indicates equal or longer reliability than that of non-copper column based solder bump. This was also confirmed by the reliability tests. In a FEM study on copper column-lead-free solder interconnect by Kacker et al [39], failure was found to occur in copper interconnections on the die side.

Lin et al. reported a WLCSP design with a double-pad structure (DPS-WLCSP) and used copper columns as the electro-mechanical interconnections between the two pads as they provided a good compliance to solder joints and also held a thicker stress buffer layer [40].

A laser assisted bump transfer approach has been reported where copper bumps with gold bonding layers and intermediate nickel barriers, fabricated by UV lithography and electroplating on quartz wafers with pre-deposited polyimide layers, were thermosonically bonded to their respective chips and then released from the carrier by laser machining of the polyimide layer, using laser light incident through the carrier [41]. Zhang et al. demonstrated a similar bump transfer technique [42].

Copper pillar/post/bump fabrication processes can be classified into two major categories: spin-on photoresist process and dry-film photoresist process. These are described in detail below.

2.5.1 Spin-on Photoresist Process

Copper interconnection fabrication process is based on photolithography and an electroplating process which is compatible with conventional integrated circuit (IC) fabrication integration into wafer-level processing as batch process. The baseline process flow is shown in Figure 2.12. Incoming wafer is first sputtered with UBM layers comprising of Titanium and Cu. Titanium is served as an adhesion layer while Cu is the seeding layer for the electroplating of Cu Pillar. Photo-Resist is then coated onto the sputtered wafer using spin coating process. The coated photo resist material is then exposed and developed to open up the area for bumping. A plasma descum process is also necessary to clean away the photo resist residue left behind during the developing process. Cu followed by nickel barrier and solder are then electroplated onto the resist opening to form Cu Pillar bumps. After the two metals are deposited, the resist is stripped away using appropriate solvents and sputtered Ti/Cu seed layers are etched away using metal etchants. The wafer is finally reflowed under forced convection reflow oven to give solder a hemispherical shape.

For high aspect ratio copper post interconnections, Aggarwal et al. in PRC at Georgia Tech fabricated the interconnections in a single photolithographic step using the SU-8 Series 2000^{TM} (MicroChem Corp.) photoresist. In this work, test dies with 10 mm x 10 mm size and interconnections with 20 microns diameter, 100 microns height and 40

micron pitch were fabricated on silicon test wafers. SU-8 has very high optical transparency which makes it ideally suited for imaging near vertical sidewalls in very thick films, and is near UV (350-400nm) and e-beam imageable. Resist thickness ranging from 50 µm to 200µms can be achieved with single spin coat process. Besides, it has superb chemical resistance that makes it suitable for a variety of electrolytic plating bath chemistries.

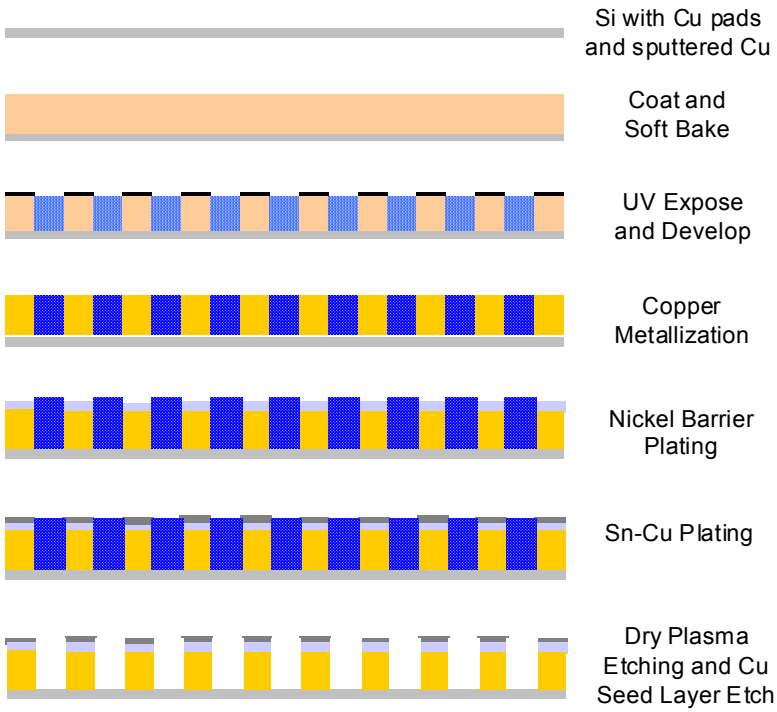


Figure 2.12 Baseline process for fabrication of high aspect ratio copper posts.

The copper pillar technology has been further extended to no-flow Underfill (NFU) technology. Traditionally, NFU has no Silica filler causing CTE mismatch to the solder bumps. As a result, Flip Chip using NFU had encountered reliability problems especially for large die. On the other hand, if Silica fillers were to be added into the NFU, it would have Silica entrapment problem thus reducing the assembly yield. A Thermal

Compression Bonding (TCB) process was used to interconnect the large die onto BT substrate together using NFU with Silica fillers. During the bonding process, compressive force was used to push the Silica filler aside and ensure all bumps were connected to the bond pads. A local reflow was performed to create the interconnection between the Cu Pillar Bumps and bond pads, during which the wicking of molten solder over the pad helped to push the Silica filler away from interconnection area (Figure 2.13). In addition, the bottom pads of the BT substrate were deposited with solder forming solder caps on the pads. This created a rolling effect on Silica fillers during the compression process, which further minimized the Silica entrapment. This process is called Thermal Compression Bond (TCB) with Twin Reflow Tip. APS has demonstrated this process using a 10x10 mm die with 1600 I/Os on a single layer BT substrate. Solder was deposited onto the pads using conventional printing and reflow processes to form the solder cap. TCB process was performed using Pansert FC2 Flip Chip Bonder. After the bonding, post cure of the underfill was performed in a batch curing oven. Electrical connectivity were then tested. CSAM was also used to inspect the void level and detect possible delamination between the layers. The assembly had passed Moisture Sensitivity Level 3 test with 3x reflows at 260C. With MSL3 preconditioning, the assembly had futher passed 1000 cycles of Thermal Cycling from –55C to 125C.

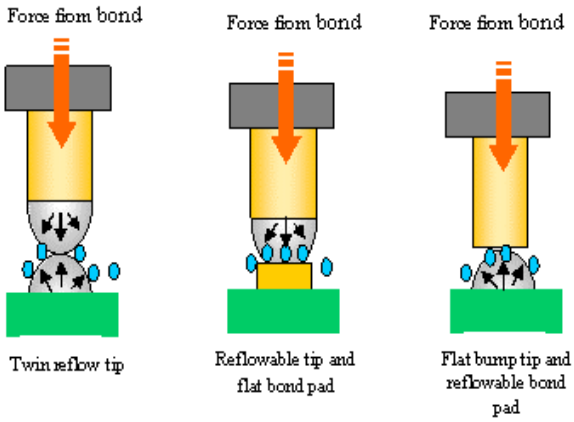


Figure 2.13 Schematic representation of the 'Twin Reflow Tip' and single reflow tip.

2.5.2 Dry film Process

The bed of nails process (BON) is an alternative low cost robust copper post interconnection fabrication proces. In this process, rather than using a spin on photoresist material, high aspect ratio Cu pillar interconnections were fabricated using a negative working dryfilm photoresist material.

The Cu interconnections fabrication process cost using spin on photoresist is high since the 90% of resist material is wasted during spin coating and it also needs multiple coatings to obtain high aspect ratio interconnections. Conventional dryfilm photoresist is used for the lager feature sizes with low aspect ratio structures. Obtaining the high aspect ratio (> 2) and high density (11.6×10^5) openings on 8 inch wafer with development through out the wafer during photo lithography is the biggest challenge in this process. Another challenge is uniform plating throughout the wafer with co-planarity of ± 5µm and without missing any of the bumps.

In the BON process (Figure 2.14), dryfilm has an excellent resolution, uniform thickness, ease of processing, and it can be easily stripped in diluted alkaline (potassium hydroxide) solution. It is also a low cost resist material compared to spin on resist materials. Dryfilm thickness layers of 80µm and 120µm can be achieved in single lamination, and it has a very good adhesion with copper and excellent chemical resistance to acid electroplating baths such as copper sulphate and solder fluoborate (tin/lead, tin), acid cleaners, ammonium persulfate, dilute sulfuric acid. Electroplating was carried out in copper sulphate electrolyte bath. The patterned wafer is descumed using O_2 plasma before electroplating to clean the bottom of the mould and to activate the resist moulds for copper plating. The wafer is also dipped for 5 min into a cleaner solution which contains surfactants at 40^0C to improve the wettability of high aspect ratio openings. The current density of 0.02 A/cm^2 was used to plate the copper interconnections.

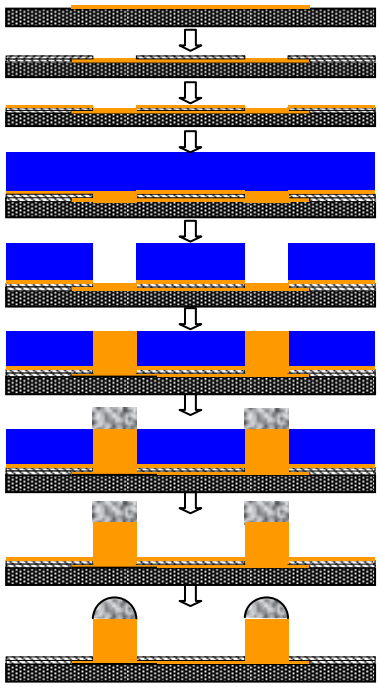


Figure 2.14 Fabrication process flow of copper column interconnections using BON process

Cu column interconnection fabrication process was demonstrated on 8 inch wafers with 50μm diameter, 120μm height, and 100μm pitch. High density copper column interconnections of 36,481 I/Os on 20mm × 20mm die were fabricated.

2.6 Emerging direct metal-metal bonding trends

Due to limitations of solders at fine pitch such as extra processing steps, barriers to control intermetallics, there is an increasing to trend to direct pad-to-pad bonding without using solders. Trend towards 3-D packaging has been a major impetus for direct pad-to-pad bonding. It holds promise for meeting the high I/O count and ultrafine pitch needs of the future. Some of the recent pad-to-pad bonding technologies are discussed below.

2.6.1 Transient Liquid Phase bonding

This three-dimensional (3D) chip stacking technology has been developed by ASET to realize a high-density and high-performance System-in-Package (SiP). A 20-pm-pitch low impedance vertical interconnection through Cu through-via (TV) within thin chips plays the following roles: the wide signal bus and very short electrical path for high-frequency signal transmission, the strong power supplies and stable ground lines. The vertical interconnection is fabricated by Inter Chip Connection (ICC) process, which includes Copper Bump Bonding (CBB) utilizing Cu-Sn diffusion for connecting Cu TVs without the formation of bumps on the chip back surface and encapsulating micro thin gap between chips (Figure 2.15).

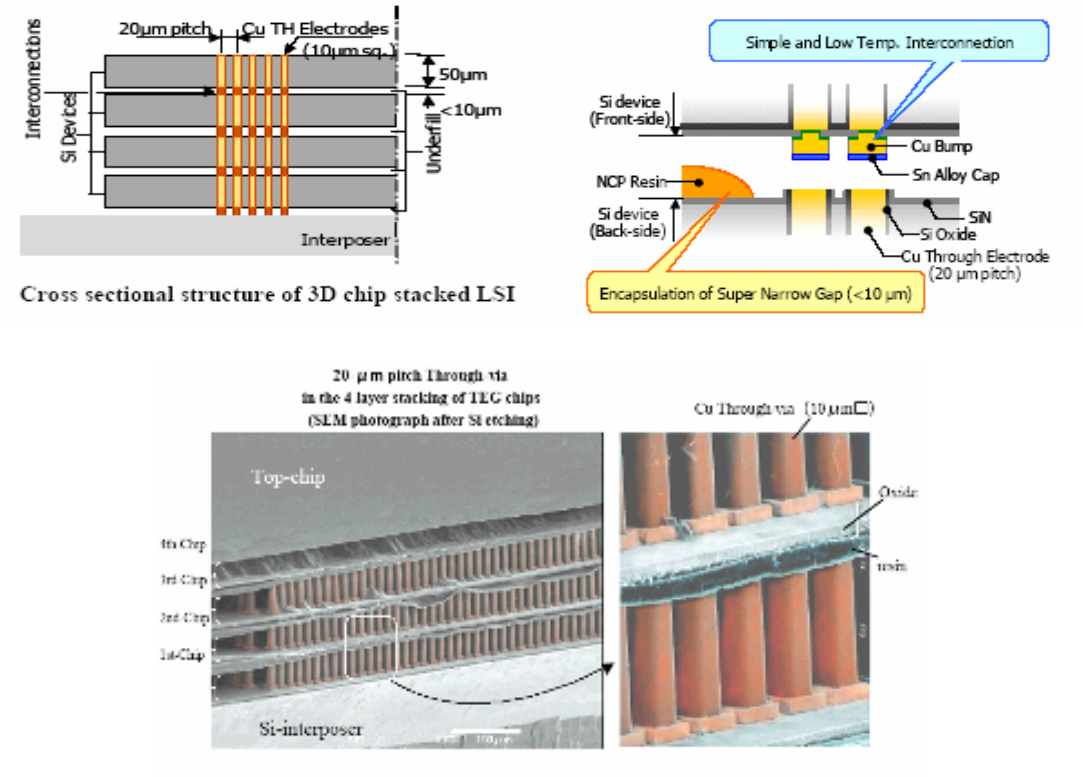


Figure 2.15 20 μm-pitch vertical interconnection is formed in through chips.

The temperature cycling test (TCT) was on Chip on Chip (CoC) and 3D chip stacking structure fabricated by ICC process, and over 1,000 cycles reliability was demonstrated. The vertical interconnection with Cu TV and ICC demonstrated the excellent capability of high performance interconnection on 3D chip stacking package. The vertical interconnection that was established by TVs and inter-chip connection (ICC) is able to realize high-speed data transmission between devices to prevent signal delay. As shown in the figure, the 20-pm-pitch vertical interconnection is formed in through chips, which is fabricated by the Cu TV fabrication in chip and the inter chip connection (ICC) process [36].

2.6.2 Cu-Cu Thermocompression bonding

The impressive bonding property using Cu thermo-compression holds tremendous promise for 3-D IC integration and has the potential to find its way through in large scale assembly of copper based chip-to-package interconnections. Need for reduction in I/O pitch and trend towards 3-D packaging have given huge impetus to the emerging copper-to-copper direct bonding. There has been several reported works that discuss approaches to carry out copper to copper direct bonding. Copper to copper direct bonding using thermo-compression method is most attractive in this regards. The bonding is carried out by thermally induced diffusion. Several research groups including Veer, Kolster et al. [43], Ward and Carroll [44], and Iijima, Wakabayashi et al. [45] have studied the diffusion characteristics of copper in copper silicon systems that includes the inter diffusion coefficient and vacancy assisted self diffusion coefficient. Though the reported values of temperatures are higher than the bonding temperature of interest, the above mentioned works give the basic understanding of the diffusional process that is crucial for thermo-compression bonding. The pioneering work on actual demonstration of copper to copper direct bonding has been done by Fan et al [46] and Chen et al [47,48-57]. Fan et al demonstrated copper to copper face to face bonding at 450 C for 30 min. followed by 30 min nitrogen annealing at same temperature range. The thickness of evaporated copper, which was used in the process, was 300 nm. They reported good quality bonding with their processes. However, in absence of quantitative bond strength measurement bonding at different process parameters could not be comprehensively compared. In addition, it was found that the presence of diffusion layer (Ta) did not affect the bonding at the bonding temperature of interest. From this finding it can be safely concluded that

the bonding doesn't involve copper – silicon diffusion that is only interlayer copper self diffusion across the bonding interface is only important. This is an important understanding because the diffusional work done in copper silicon systems reveals very fast diffusion kinetics of copper in silicon [58-60]. Since copper is a deep-level trap for carriers, a diffusion barrier is indispensable [46].

Further work by Chen et al developed methods to carry out bonding at 400 C at 4000 mbar pressure. Also, studies on microstructural evolution at the interface and other bonding locations during the bonding process suggest several phenomena including copper self diffusion, recrystallization and grain growth acting together to form a strong metallurgical bond some time free of any identifiable interfacial region (Figure 2.16). However, the bonding interfaces may take several forms including indistinguishable interface, zigzag interface and distinct interface.

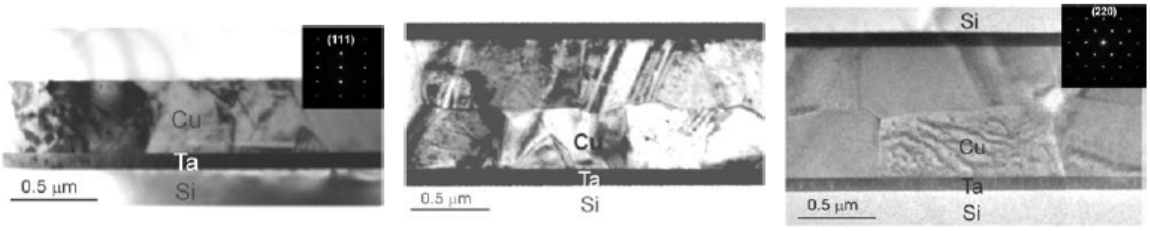


Figure 2.16 XTEM images of the Cu-Cu bonded layer and the major diffraction pattern of single grains for selective area: (a) before bonding (b) after 30 min bonding (c) after 30 min bonding and annealing [46].

2.6.3 Surface-Activated Bonding

Suga et al [97] developed over the past 10 years, a method for joining dissimilar materials at room temperature, called Surface Activated Bonding (SAB). This method is

based on the reactivity of atomically clean surfaces of solids and the formation of chemical bonds in contact between the clean and activated surfaces. The bonding consists of cleaning the surfaces by ion or radical beam irradiation and contact in an ultrahigh vacuum or in an inert gas, depending on the materials combination and the characteristics required by the bonding. The key items are the surface-activating process and the alignment and manipulation of the chip. So far, several surface-activated pieces of equipment have been developed, including a cold-rolling machine for manufacturing metal laminates and a bonding machine for wafers up to 200 mm [61]. Figure 2.17 shows a high precision SAB flip-chip bonder.

SAB represents a new type of interconnection technology that reaches into the area of design rules and on-chip interconnects. It is performed at room temperature versus the higher temperatures of traditional bonding methods. Al-Al laminates fabricated by SAB have been put into practical applications for a part of the safety vent for the Li-ion battery. SAB addresses the challenges to establish a method for smart disassembly of electronic products by using reverse engineering.

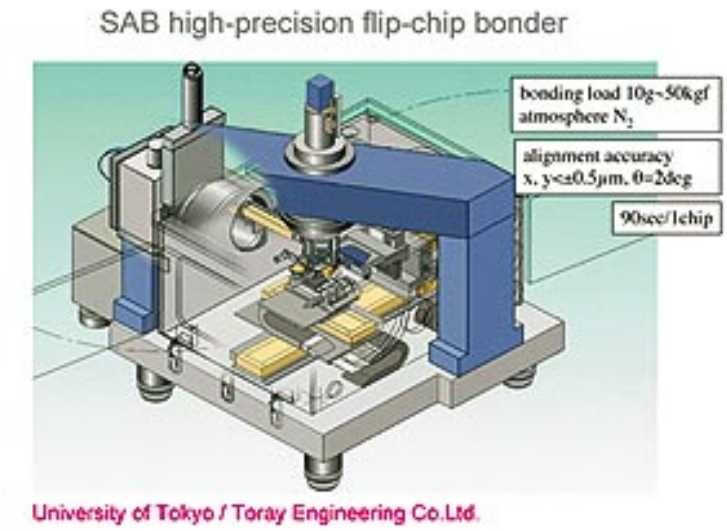


Figure 2.17 A SAB high-precision flip-chip bonder.

Direct copper-copper bonding is a high thermal budget process which is not compatible with other packaging processes. Most of them also need very high pressures which is not compatible with thinned-down embedded dies. Hence, there is a need for low-temperature, relatively lower pressure, reworkable, environment-friendly interconnection process for fine-pitch interconnections.

2.7 Conductive adhesives for fine pitch interconnections

Flip chip assembly using Non-Conductive Adhesives (NCA) and Anisotropic Conductive Adhesives (ACAs) has been gaining attention for its simple and lead-free processing, in addition to being a cost-effective packaging method. The ACAs do not need additional underfill and can potentially be processed much faster than the conventional solder/underfill method. They are already being successfully implemented as package methods for chip-on-glass, chip-on-film for flat panel displays, and chip-on-board for mobile electronics [62-65].

Non Conductive Film (NCF) is an epoxy film that holds the chip and the substrate together, enabling a mechanical contact between the bumps and the corresponding bond pads while also acting as an underfill. Isotropic Conductive Adhesive (ICA) is an epoxy consisting of dispersed metallic filler particles with the loading level above the percolation limit. Typical Anisotropic Conductive Film (ACF) is an adhesive film consisting of dispersed, microscopic, electrically conductive particles 3-15 μm in diameter and an insulating adhesive film 15-35 μm thick. Figure 2.18 shows cross sections of flip chips assembled with ICA and ACA. Various kinds of conductive particles, such as carbon fiber, metal (Ni, solder), and metal (Ni/Au)-coated plastic balls, and types of adhesive materials, such as thermoplastic (SBR: styrene butadiene rubber, polyvinyl butylene), thermosetting (epoxy resin, polyurethane, acrylic resin), and mixed thermoplastic and thermosetting materials, have been proposed. Thermosetting adhesive film with metal-coated plastic particles is the most popular type. In general, the normal bonding conditions, as well as an adhesive temperature of about 180˚C, a bonding time of about 20 seconds, and a bonding pressure of about 20 kg/cm^2 are recommended [66]. The latter three key parameters depend on the type of ACF, the capability of the process equipment, and the required process time.

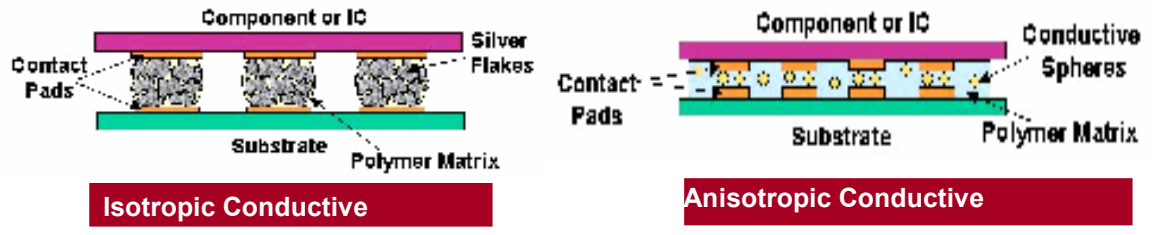


Figure 2.18 Cross sections of flip chips assembled with ICA and ACA

The anisotropic electrical conductivity of these materials comes from the trapped conductive particles between conductive bumps on the flip chip IC and the corresponding pads on the substrate, and from conductive particles not connecting electrically between pads. In general, these materials are poor thermal conductors due to their thermally insulated polymer matrix and low content of conductive filler.

The continuous downscaling of structural profiles and increase in interconnection density in flip chip packaging using ACAs has given rise to another problem: as the bump size is reduced, the current density through bump increases. Increased current density causes new failure mechanisms such as interface degradation, and adhesive swelling caused by high current stressing. This is a particular issue in the high current carrying joint of ACA flip chip assembly where high junction temperature enhances such failure mechanisms. Therefore, it is necessary for the ACA to be a thermally conductive medium that allows effective heat dissipation from the ACA flip chip joint through adhesive resin to the substrate for the flip chip package. This will improve the lifetime of the ACA flip chip joint by reducing the interface and adhesive degradation caused by high current density and heat accumulation.

ACAs have been used mostly with gold stud bumps on glass or flexible substrates. Gold stud bumping is a relatively mature technology that has promising attributes for fine pitch applications. Gold bumping can be grouped into two categories - thermocompression gold to gold bonding without any adhesive layer and thermocompression bonding using adhesive layer such as Anisotropic Conductive Fillers (ACF) and Nonconductive Filler (NCF). Details of gold stud bumping technology can be

found out in the research paper of Miessner et al [67]. Gold stud bumping, typically, involves bonding of gold wire to the substrate, which is induced by thermal and ultrasonic energy coupled with pressure, followed by shearing off the wire from the formed ball to leave a stud bump [68]. Direct gold to gold bonding using thermocompression technique can be useful to lower the bonding temperature and achieve high bond reliability. However, planarity and the bump shape are important issues that are deterrent to the effectiveness of such process. Majeed et al has studied the reliability issues in gold bump technology for flip chip applications [68]. Reliability concerns can be addressed using conductive film adhesives. Oh et al has reported a thermoplastic conducting polymer bumping approach that uses thick film photoresist to achieve high planarity bumps [69]. Such process can decrease the bonding temperature and eliminate the need of adhesive. A notably low contact resistance and high degree of planarity have been reported. However, this technology involves added process steps and low pitch resolution. Similar approach by Johanson et al uses an epoxy perform and aligns it on the die which is then aligned to the substrate and bonded by simultaneous application of pressure and temperature [70]. This approach needs very high degree of alignment resolution. Gold stud bumping and bonding using Anisotropic Conductive Film (ACF), Isotropic Conductive Film (ICF) and Nonconductive Film (NCF) have been understood to be more attractive. This polymeric adhesive can eliminate some of the problems associated with the earlier bonding approaches. Recently, Ankur et al. has demonstrated that micro ACF and NCF passed the thermal cycling (-40 to 125 C) test with 200 micron pitch peripheral PB8 bumps [71]. However, the HAST (Highly accerlerated stress test) and HTS (high temperature storage) tests were not conducted. For

micro ACF, the number of particles trapped between a bump and the corresponding bond pad will be very less causing higher contact resistances and unstable resistances under humidity-assisted swelling. Typical ACAs with micron sized fillers are inadequate for ultra fine-pitch applications as they can cause shorts due to very small gaps between two adjacent bumps. Nano ACF enables particle sintering at lower bonding temperatures and can also prevent the lateral conduction better by preventing electromigration. This results in improved contact resistance stability. This study uses a nano-conductive adhesive film (n-ACF) with nano-sized silver particles, recently developed by Georgia Tech, for ultra fine-pitch applications [72]. Low temperature bonding, simple processing steps, fine pitch capability and high reliability make these attractive candidates for next generation packaging applications and will be main focus of this thesis.

3.30μm Pitch Chip and Substrate Layout

This chapter describes the test vehicle design for the 30 micron pitch interconnections. The chip layout for the 3 mm x 3 mm, 30 micron pitch peripheral array of copper interconnections to assess the mechanical reliability is described. This is followed by a description of the matching glass substrate design at 30 μm pitch.

3.1 Chip Layout

Each wafer has a total of fifty-two 3 x 3 mm dies and each die consists of one-row peripheral array of interconnects at a pitch of 30μm. A few pairs of adjacent bumps were left unconnected through die-side or substrate side traces (dog-bones) to enable insulation resistance measurement of n-ACF and NCF at 30 micron pitch. Two types of alignment marks were incorporated for each die to aid with the alignment process during sequential lithography steps. All the masks were designed on AutoCAD drawing tool. Table 3.1 tabulates the ground rules for designing the chip at 30 micron pitch. The wafer fabrication involves a two-mask process. The first mask defines the chip-side die-pads to form the daisy chain. Electroplated Copper interconnects are fabricated onto a 4" wafer using the second mask where each die pad footprint matches the substrate for subsequent assembly.

Table 3.1 Ground Rules for Chip Design at 30 micron pitch

Interconnect Pitch	30 microns
No. of I/Os	356
Die Size	3mm x 3mm
Interconnect Height	8-10 microns
Distance from Die Edge	250 microns
Pad Impression on Chip	20 microns

Each individual die on the wafer has been designed to assess the reliability of the interconnections in HAST and HTS tests. To monitor the reliability performance, daisy chains have been incorporated on all four sides of the die. Figure 3.1 displays a schematic of the mask used to fabricate the first layer of interconnect structures. Figure 3.2 displays AutoCAD snapshots of the complete chip design for the daisy-chained die.

Figure 3.3 illustrates the daisy chain design on the chip side and the dimensions of die pads and interconnect pitch.

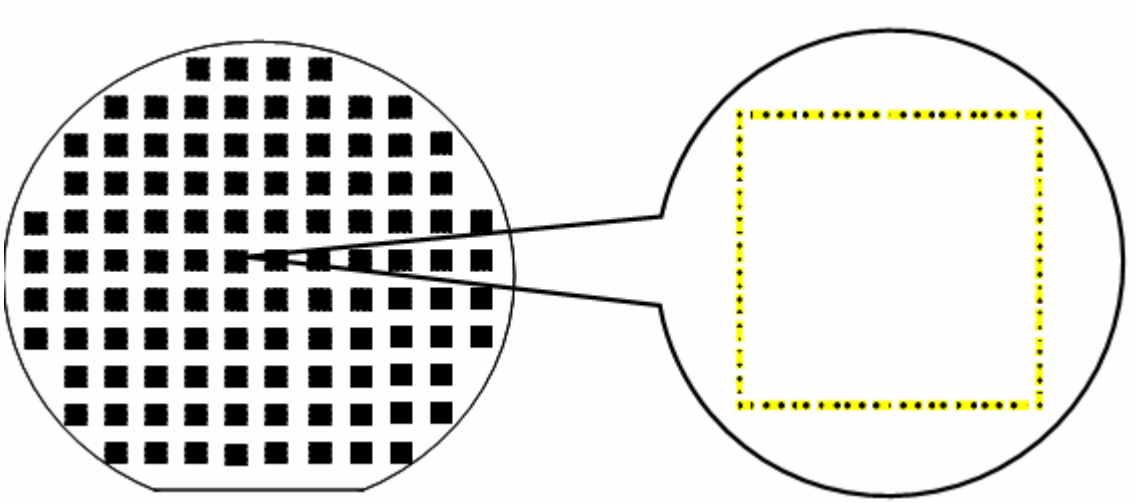


Figure 3.1 Wafer fabricated with the first layer of interconnect structures

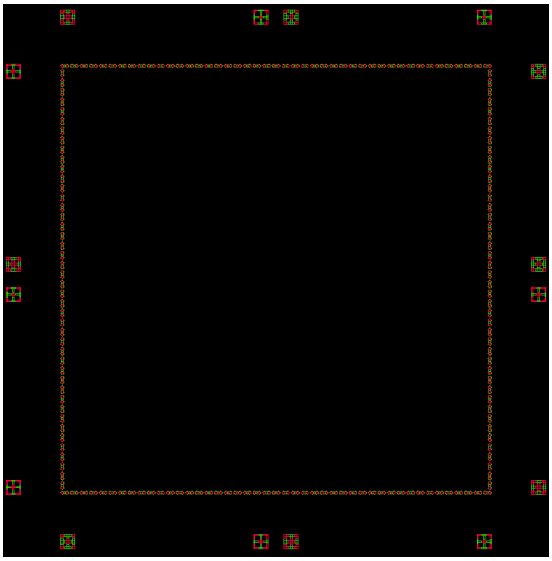


Figure 3.2 30 micron pitch daisy-chained chip with alignment marks.

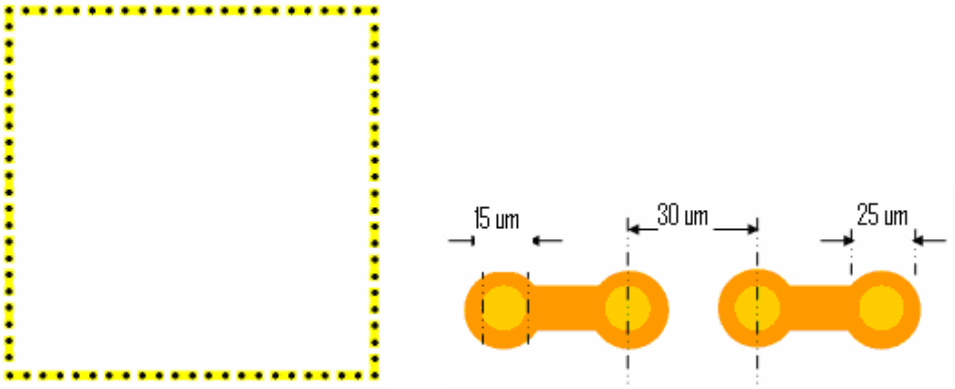


Figure 3.3 Die pad layout and dimensional illustration of die pads with passivation openings.

The definition and fabrication of the copper interconnects comprises of a two mask process. The first mask layer defines the die pads, and the second mask defines the photoresist openings for plating the interconnections.

Two types of alignment marks, with 7 microns and 15 microns wide features respectively, were designed around each die to aid in the alignment of the next mask process. The alignment marks were deliberately removed from the dies while dicing the wafer else they might prevent good assembly.

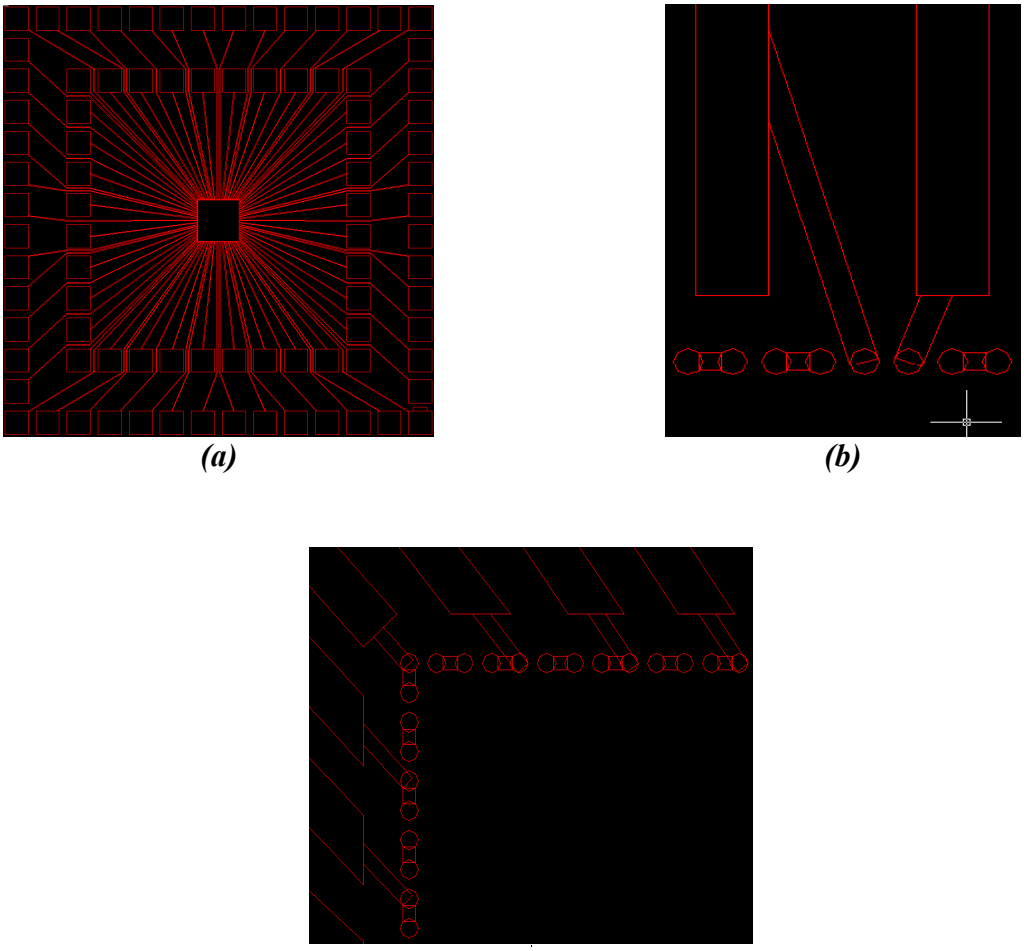
To fabricate the 30 micron pitch Copper interconnect structures on the silicon wafer, 5" x 5" bright field glass masks which are transparent to UV light were used. The glass mask comprises of an absorber pattern metal (~800 Å thick chromium) layer that defines the features of the interconnect structures. The mask is placed in direct contact with the photoresist-coated surface and subsequently exposed to UV light. The chromium

pattern on the photomask is opaque to UV light, whereas the glass is transparent to UV light which subsequently photo-patterns the photoresist.

3.2 Substrate Layout

After the wafer is singulated into individual 3 mm x 3 mm peripheral-array 30 μm pitch copper interconnects, they are ready to be assembled onto a substrate which in this study is a glass carrier. Figure 3.4 displays snapshots of the substrates layout.

The substrate is designed for manually probing the reliability of the interconnections. The daisy chain was probed at every fourth bump to monitor failure locations and failure statistics of the die more accurately. Probe pads are included around the periphery of die in order to narrow down the failure location. Every fourth bump was routed to a probe pad of dimensions 1.5mm x 1.5 mm through 15-50 micron wide traces. These narrow (50 microns), extremely thin (0.63 μm) and long (1 – 1.5 mm) traces have high resistances of 6-14 Ohms.



(a) *(b)* *(c)*

Figure 3.4 a) Substrate coupon for the daisy-chained die, b) a pair of adjacent bumps being probed for insulation resistance measurement, c) tracing fanning out of every fourth bump on the daisy-chain.

4. EXPERIMENTAL PROCEDURES - ADVANCED FABRICATION AND PROCESSING TECHNIQUES

This chapter describes the advanced materials and processing techniques that were used to fabricate the 30 micron pitch interconnection test vehicles. The chapter begins with the description of photolithographic processes, followed by a discussion on plating bath composition used to deposit the fine-grained copper for interconnection formation. The chapter concludes with a description of fabrication process used for making the matching glass substrates for the dies in order to assemble the test vehicles for mechanical and electrical characterization.

4.1 Fabrication of electroplated Copper bumps at 30 micron pitch

Photolithography is the most widely used form of lithography where patterns are transferred from masks onto thin films. The fabrication of 30 micron pitch electroplated copper interconnects utilizes photolithography to build specific structures with pre-designed dimensions. The design of the 30 micron pitch test vehicles was described in detail in chapter 3. In this section, the micro-fabrication details are presented in detail. Various materials used, their properties, and processing conditions are thoroughly described. The fabrication results obtained from these processing techniques will be shown in chapter 5 followed by appropriate discussions including electrical and mechanical characterizations.

The interconnects are fabricated on 4” silicon wafers where each die pad footprint matches the substrate, which in this study is a glass carrier, to which each singulated die will subsequently be assembled onto. The baseline process for fabrication is shown in Figure 4.1. The fabrication process consists of various processes that include wafer oxidation, die pads deposition, passivation, seed layer sputtering, photoresist spin-coating, lithography, and electrolytic plating followed by photoresist stripping process and seed layer etching. All these steps are outlined in detail as follows.

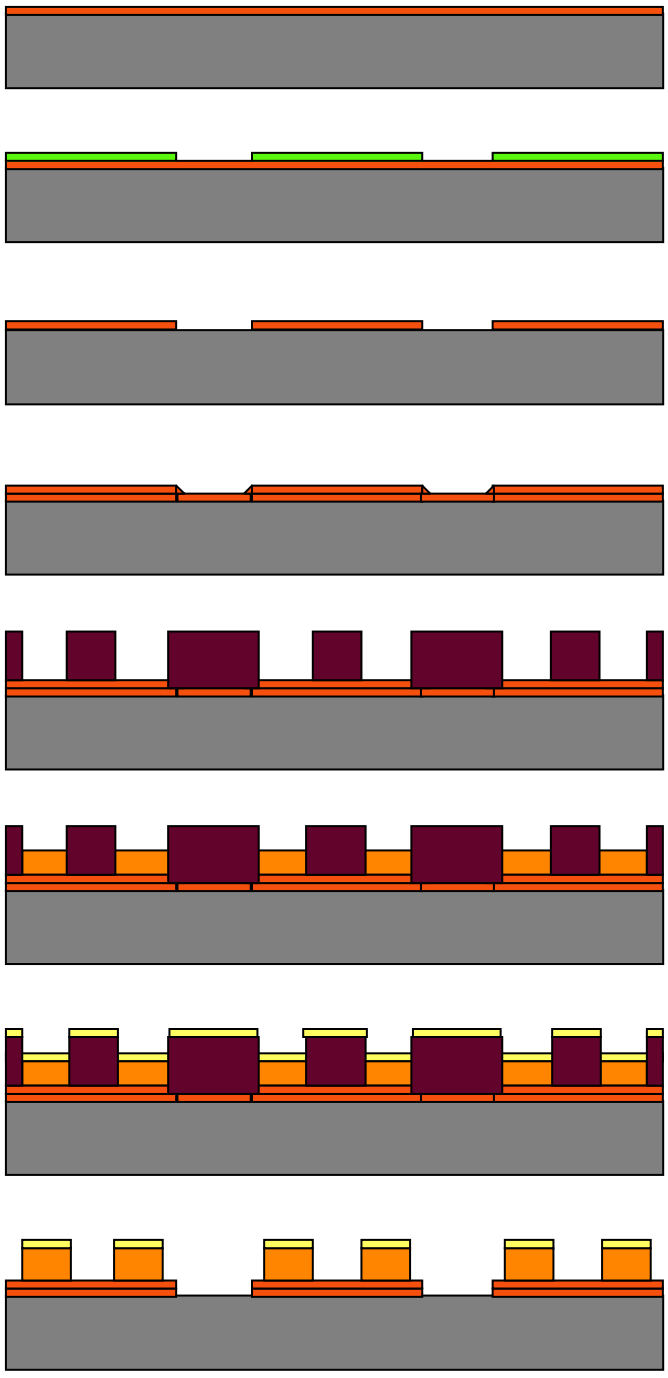


Figure 4.1 Baseline process for fabrication of electroplated Copper interconnections.

4.1.1 Wafer Oxidation

The silicon wafer is first cleaned with acetone, methanol, iso-propanol, and deionized (DI) water (in this order) to remove any contaminants that may be present on the surface of the wafer. The wafer is subsequently exposed to oxygen plasma for a few minutes to get rid of any organic traces left from the clean process. Following cleaning, a thin layer (approximately 1.5µm) of PECVD oxide is deposited on the wafer in order to passivate the silicon surface. The conditions used to deposit the PECVD oxide are listed in Table 4.1. It takes approximately 30 minutes to deposit a 1.5µm film of silicon oxide.

Table 4.1 PECVD Conditions for Oxide Deposition

Temperature	(250 °C)
Gases	SiH4 (2% in N2) - 400 sccm
N2O	900 sccm
Pressure	900 mTorr
Power	25 W
Deposition Rate	500 Å/min

4.1.2 Die Pad Deposition

Post oxidation, the wafer is thoroughly washed and dried using nitrogen (N_2) gas and placed into a 95°C oven for 10 minutes to fully dehydrate the wafer. Thereafter, a

layer of Titanium (Ti) and Copper (Cu) is deposited on the wafer using a CVC DC sputterer. Here, Ti serves as an adhesion layer between silicon oxide and the copper layer that forms the conducting traces on the die side. Copper as such does not have a very good adhesion with silicon/silicon oxide and hence such an adhesion layer is very critical. Thicknesses of the two metals deposited using sputtering are Ti: 300 Å and Cu: 0.6 μm. Initially, Cu layer as thick as 1.8 μm was tried but it resulted in significant undercut during the etch-back process (described on below) to form the die-pads. Considering extremely small dimensions of the die-pads, an undercut of about 1.8 μm was unacceptable and hence 0.6 μm thick Copper was used for die-pads.

Table 4.2 Photoresist processing conditions for die pads masking

Spin Coating	4000 RPM/500RPM Ramp Rate/40 Seconds
Soft Bake	107˚C
Exposure	405 nm wavelength; 8 seconds at an intensity of 20 mW/cm^2
Developer	MF-319 for 1 minute, agitation
Rinse	Rinse in water for 2 minutes

The die side metallization was patterned with an etch back process using a thin layer of SC 1813 photoresist (Shipley Chemicals). SC1813 is a positive tone photoresist and it replicates the mask design on to the wafer i.e. the dark features similar to the ones on mask are transferred on to the wafer. Therefore, the photoresist selectively protects the copper film on the wafer. The processing conditions used for this are shown is Table 4.2.

Thereafter, the copper and titanium films are selectively etched using Cu and Ti metal etchants. The composition of the etchants and the etching time is shown below in Table 4.3.

Table 4.3: Metal Etchant Compositions and etch times

Etchant	Composition	Etch Time
Copper Etchant	1:1:50 H_2SO_4:H_2O_2:H_2O	30 seconds
Titanium Etchant	1:20 HF:H_2O	5 seconds

Once the copper and titanium layers are selectively etched, the photoresist mask is removed by dissolving in acetone, and the wafer is cleaned thoroughly using DI water followed by drying with a Nitrogen gun.

4.1.3 Electroplating Seed Layer Deposition

Followed by die-pad deposition, the wafer was sputtered with a layer of Ti/Cu that serves as a seed layer for the electroplating step. Before sputtering, the wafer was dipped in a 10% H_2SO_4 solution to remove any copper oxide formed on the surface during the polyimide curing process. This step is extremely critical in order to maintain a clean conducting path for interconnects, and thus the wafer must be transferred to the sputterer as soon as the oxide cleaning step is finished in order to minimize the copper oxidation from air. The sputtered seed layer comprises of 2500Å each of titanium and copper. Topographical contrast was enough to be used for alignment in the next lithography step.

4.1.4 Photoresist processing

Photoresists from Rohm and Haas (Shipley), Clariant, Futurrex, Microchem Corp and other companies are eligible to meet the 15 micron opening requirements. Shipley photoresists have low viscosity and typically give thinner films. Futurrex photoresist is chosen because of its compatibility with various plating chemistries, and its capability to give thicker films ranging from 10-30 microns in a single coating step. It can be stripped off with a simple liquid remover and does not need reactive ion etching unlike SU8 photoresist. A negative working, cyclohexane based aqueous processable liquid photoresist, NR5-8000 (Futurrex Inc.) is used as the electroplating mold in this application. This photoresist has been developed by Futurrex for various electroplating applications, and is compatible with most of the acidic plating baths. This photoresist has a strong heat resistance and an excellent resolution capability, facilitating future down-scaling requirements. The resist requires short bakes and short resist development time, which in conjunction with short exposures boosts throughput of lithographic process. The resist also has a superior film thickness uniformity and exhibits very straight sidewalls when used with suitable exposure tools and fixtures. It has a very good adhesion during copper plating. Very little or no bubbling is observed in the photoresist films which is very typical of liquid photo-resists.

To ensure a good adhesion between the seed layer and the photoresist, the surface must be free of any kind of organic contamination. Cleaning immediately prior to spin coating is helpful in removing surface particles and avoiding recontamination. Table 4.3

describes the conditions used for spin-coating and patterning a 15-17 microns thick coating of the NR5-8000 photoresist on silicon substrate.

Table 4.3 Photoresist Processing Conditions for Electroplating Mold on Silicon

Spin Coat	1000 RPM/300 Ramp/40 Seconds
Soft Bake	150˚C for 90 seconds on a hot-plate
Exposure	80 seconds; Intensity of 6.1 mW/cm^2 [i-line] using Karl Suss MA6 mask aligner (additional optical filter used which decreased the intensity).
PEB	100˚C for 90 seconds
Develop	RD-6 for 30-50 seconds

During the initial soft baking at 150°C the solvent within the photoresist evaporates out of the film, to improve the coating fidelity, reduced edge beads, adhesion to substrate, and bubbles within the film. The PEB is performed to selectively cross-link the exposed portions of the film. Precise control of PEB is critical in determining the subsequent development time. Another reason that PEB is desired is because the reactions initiated during exposure might not have run to completion. Adjusting the amount of exposure and PEB process conditions can control the amount of cross linking.

The NR5-8000 resist is very sensitive to soft bake and post exposure bake temperatures/time, and care has to be taken to maintain the accuracy of these temperatures.

To maximize the resolution, a hard contact and high intensity light source was used. An i-line long pass filter was used between the photoresist and the exposure lamp for reasons discussed earlier. For a photoresist thickness of 15 microns, the exposure time was 80 seconds at a lamp intensity of 365nm wavelength was 6.1 mW/cm^2 with an optical filter that reduced the actual intensity to about 3.5 mW/cm^2.

Once the photoresist is exposed, the resist development is done using the RD-6 developer (Futurrex, Inc.). The resist is developed with agitation in a puddle for 30-50 seconds with continuous agitation. At such fine feature sizes, the development time is a very critical parameter and it needs to be controlled very carefully. Any over development of the resist will lead to delamination of the photoresist film. Any underdevelopment will leave undeveloped photoresist at the bottom of the opening that will prevent electroplating. The wafer has to be examined under an optical microscope during the development process to prevent any over-development and delamination. This process leads to very clean openings with little photoresist residue at the bottom of the trench. The wafer is then thoroughly rinsed with DI water for a few minutes.

After the wafer is washed thoroughly after developing, there is some organic residue left at the resist/Cu interface in the photoresist openings that will prevent the electroplating through the opening. It is important to remove this residue, and this is done

using a plasma assisted descum process. The plasma conditions used for this are shown in Table 4.4.

Table 4.4 Dry Plasma Conditions for Organic Descum Process

RF Power	250W
Chamber Pressure	300mTorr
O_2 Flow Rate	50 SCCM
CHF_3 Flow Rate	7 SCCM
Descum Time	30 seconds

4.1.5 Electrolytic plating of fine-grained copper

Once the photoresist process is complete, the next step in the process flow is to electroplate the copper interconnects. The details of the electroplating bath will be discussed in the later sections of this chapter.

Prior to placing the wafer in the electroplating bath, it is dipped in 10% sulfuric acid for 30 seconds and rinsed with DI water for one minute. If this is not done, the thin copper oxide layer will provide poor adhesion, or possibly no electroplating between the interconnect and the copper pad. The total plating area on the wafer is approximately 10 cm^2. A plating current of 35mA is used which translates to a current density of 3.5mA/cm^2. The plating time to deposit about 10 microns of copper was about 3 hours

with a deposition rate of approximately 3.5μm/hour. To avoid over plating, the wafer is taken out and inspected periodically with a profilometer and microscope. Since the actual features are too small to be measured with a stylus type profilometer, some bigger features need to be incorporated on the wafer just to monitor the plating rate. Another way is to have a ring of exposed copper around the perimeter of the wafer where profilometer measurements can be done. The results of the copper electroplating will be discussed in the next chapter.

4.1.6 Gold protection evaporation and lift-off

Copper oxidation needs to be prevented during assembly for better long term reliability of the interconnections. Thin layer of evaporated gold was used for this purpose. The total photoresist thickness was 15-17 microns to begin with. After plating 8-9 microns of copper, and before stripping off the photoresist, a 300-500 nm thick protective gold layer was evaporated using a CVC electron beam evaporator. The copper plated wafer was thoroughly cleaned with 10% H_2SO_4, to remove any oxide at the surface of the copper bumps, before evaporating gold on top. This step is very critical because the copper oxide at the top surface of the bumps may cause poor adhesion of gold to copper. It may also prevent any electrical connections depending on the thickness of the oxide formed. The wafer was transferred to the e-beam evaporator right after cleaning without any delay. 0.3-0.5 μm Au was evaporated onto the wafer.

4.1.7 Photoresist release and seed layer etch

Followed by copper electroplating and gold deposition, the photoresist is stripped using the RR-4 resist remover (Futurrex Inc.). The lift-off is carried out in ultrasonicator

to help the stripper solution reach the fine features. It is a fairly easy stripping solution to use and the whole process doesn't take more than a few minutes. Next, the seed layers are removed where very mild copper etchant is used to first remove the copper seed layer. The copper interconnections should not be exposed to the seed layer etchant for a longer period of time. Since the bumps are ultra-thin and very fine-pitch, significant amount of copper can be etched from the bumps if the etching process is not optimized. Very dilute copper etchant should be used and the wafer should be taken out as soon as the seed layer is etched. Next, the titanium seed layer is removed with a very mild HF solution. A strong HF solution will cause significant undercut and decrease the area of the bump at the base which can significantly affect the reliability. Once the etching process is complete, the wafer is thoroughly washed with DI water to remove any acidic residues. The wafer is subsequently singulated into individual dies to be assembled on to the glass/silicon substrates.

4.2 Electrolytic plating of fine-grained copper

In a copper plating solution, the copper ions from the solution are deposited onto the surface of the wafer. Two main components of a copper plating bath are copper sulfate and sulfuric acid. At the anode side, oxidation of the copper metal generates copper ions which are transferred through the bath onto the wafer. To agitate the system, a stirrer or pump that provides ample flow through the system is used to provide good uniformity through the system. Conductivity of the solution is controlled by hydrogen ions that are provided by water and sulfuric acid. The high conductivity of the plating solution is critical in achieving a uniform film thickness on the cathode substrate.

Electrical contact is made to the seed layer, and current is passed such that the reaction $Cu^{2+} + 2e^{-} \rightarrow Cu$ occurs at the cathode surface. In case of copper plating, all Cu ions removed from the solution at the cathode are replaced by dissolution of a solid copper anode. The set-up for a copper sulfate electrolytic plating bath is shown in Figure 4.2.

In the absence of a secondary reaction, the current delivered to a conductive surface during electroplating is directly proportional to the quantity of metal deposited (Faraday's law of electrolysis). Using this relationship, the mass deposited on the substrate can be readily controlled through variations of plating current and time.

In electroplating, the composition of plating solution plays a major factor in obtaining high-quality plated structures. With specialized plating solution, modification of other operating conditions (temperature, plating current density, etc) can improve the electroplating results.

Copper Gleam 125-EX is a high acid copper electroplating chemistry (Rohm and Haas Electronic Chemicals) that that was used for plating the nano-structured copper interconnects. This chemistry produces ultra-fine grained equiaxed deposits of copper. Typical characteristics of a copper deposit obtained from this bath are shown in Table 4.5.

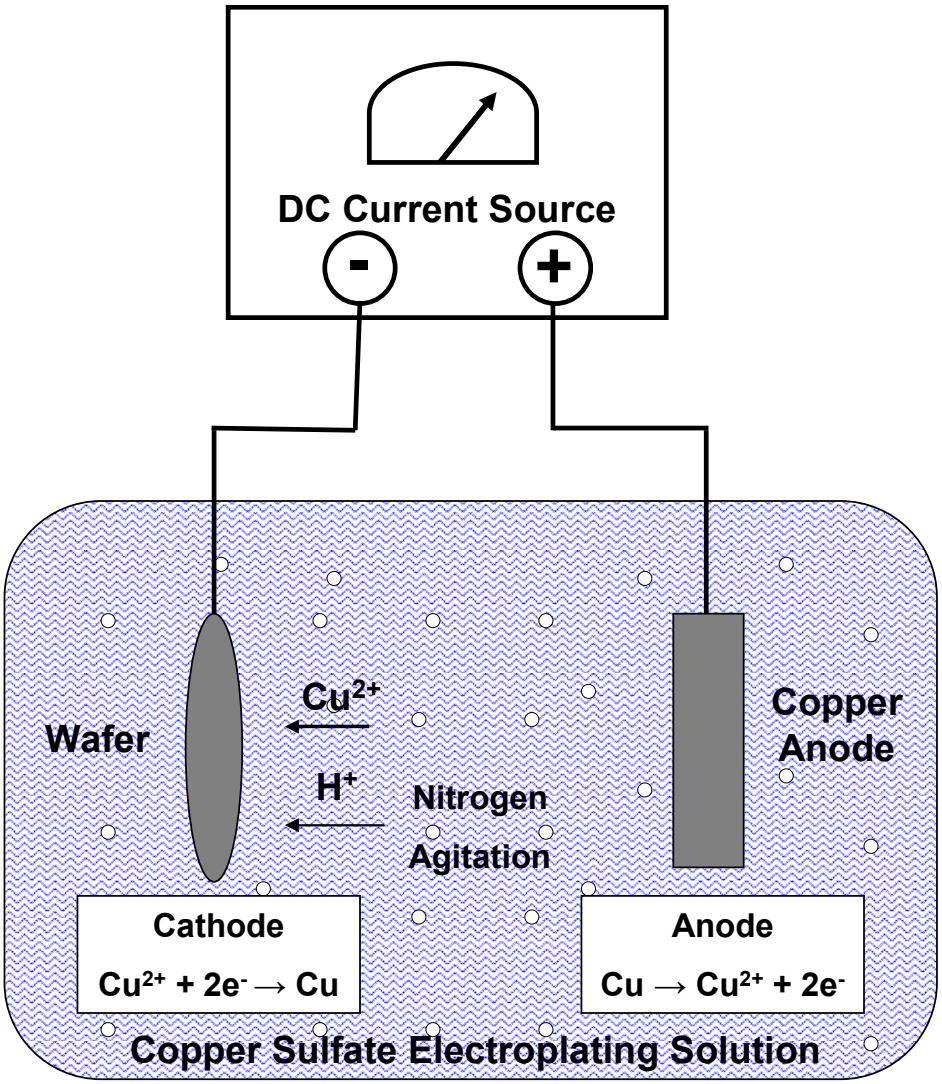


Figure 4.2 Copper Electrolytic Plating Setup.

Table 4.5 Electrodeposited Copper Properties

Density	8.9 g/cc
Conductivity	0.59 micromho/cm
Elongation	20 – 30%
Tensile Strength	280 – 350 N/mm^2 (40 – 50 KPSI)

Table 4.6 Copper Plating Bath Make-up Chemistry

Chemical	Make-up Quantity [Total 6000ml]
DI Water	4866 ml
Sulfuric Acid (50 %)	599 ml
Copper Sulfate Pentahydrate	443 gms
Copper Gleam 125 EX Carrier	61 ml
Copper Gleam 125 EX Additive	31 ml

The copper plating bath make up chemistry is shown in table Table 4.6 and the operating parameters are tabulated in Table 4.7. To make-up the plating bath, the polypropylene tank is first cleaned thoroughly using DI water. The tank is then filled to approximately 1/3rd of the final bath volume with de-ionized water, and the copper sulfate is added to the water. Sulfuric acid is then slowly added to the solution with thorough mixing. A dilute form of sulfuric acid (50%) was used to minimize the heat build-up in the tank. The bath agitation (N_2) should be turned on and the tank should be allowed to cool down to 38˚C (100˚F) or below. The 125-EX carrier is then added and dummy plating is done at 0.50 A/dm^2 for 2 hours followed by dummy plating at 1.0 A/dm^2 for another 2 hours. Thereafter, copper gleam 125-EX additive is added to the bath followed by another dummy plate for at least 3 hours at 1.0 A/dm^2 to 1.5 A/dm^2 anode current density.

Table 4.7 Operating Parameters for Copper Plating

Anode	Copper Bar
Temperature	21 – 29˚C
Current Density	0.75 – 3.0 A/dm^2
Anode to Cathode Distance	20 cm

The copper gleam 125-EX additive contains the active grain refiners. The copper gleam 125-EX carrier contains surface active agents that are also referred to as "wetters" or "suppressors". Nitrogen purging based agitation of copper plating bath is done for reducing the porosity in the electroplating cell and for the impacting of electrolyte jets on the surface of the wafer for deposition. It can result in the limiting current density the current efficiency, and a decrease in the concentration of polarization in acid sulfate solutions.

Current density during electroplating has a large impact on the deposition rate. Insufficient current will result in poor coverage of recesses or vias and a low general plating rate, while the presence of excessive current does not necessarily result in increased plating rate and is likely to create dull, burnt plating with impurities.

4.3 Glass substrate fabrication

Glass was chosen as a substrate material for this work because of its flatness and transparency that can assist in measuring the die-substrate misalignment. An ultra-flat substrate was desired to eliminate the warpage of the substrate and thus eliminate any yield or reliability issues arising due to non-coplanar substrate. At such fine pitch with a non self-aligning bonding layer, alignment is very challenging. Due to extremely thin metallizations on both the chip and the substrate and ultra-thin bumps, it is very difficult to look at the alignment using the X-ray. Hence, it was decided to use a transparent substrate where the alignment can be looked at from the back side of the substrate.

To get a very good thin planar metallization, electron-beam evaporation and lift-off was used. The baseline process for fabrication is shown in Figure 4.3 . The borosilicate glass is first cleaned with Acetone, methanol, iso-propanol and DI water. NR5-8000 photoresist is then spin-coated, soft-baked, exposed, post-baked and developed on the cleaned glass substrate. The lithography conditions are tabulated in Table 4.8 . Since the thermal conductivity of glass is much less compared to silicon, the soft-bake and post exposure bake times are higher in case of glass as compared to those on silicon.

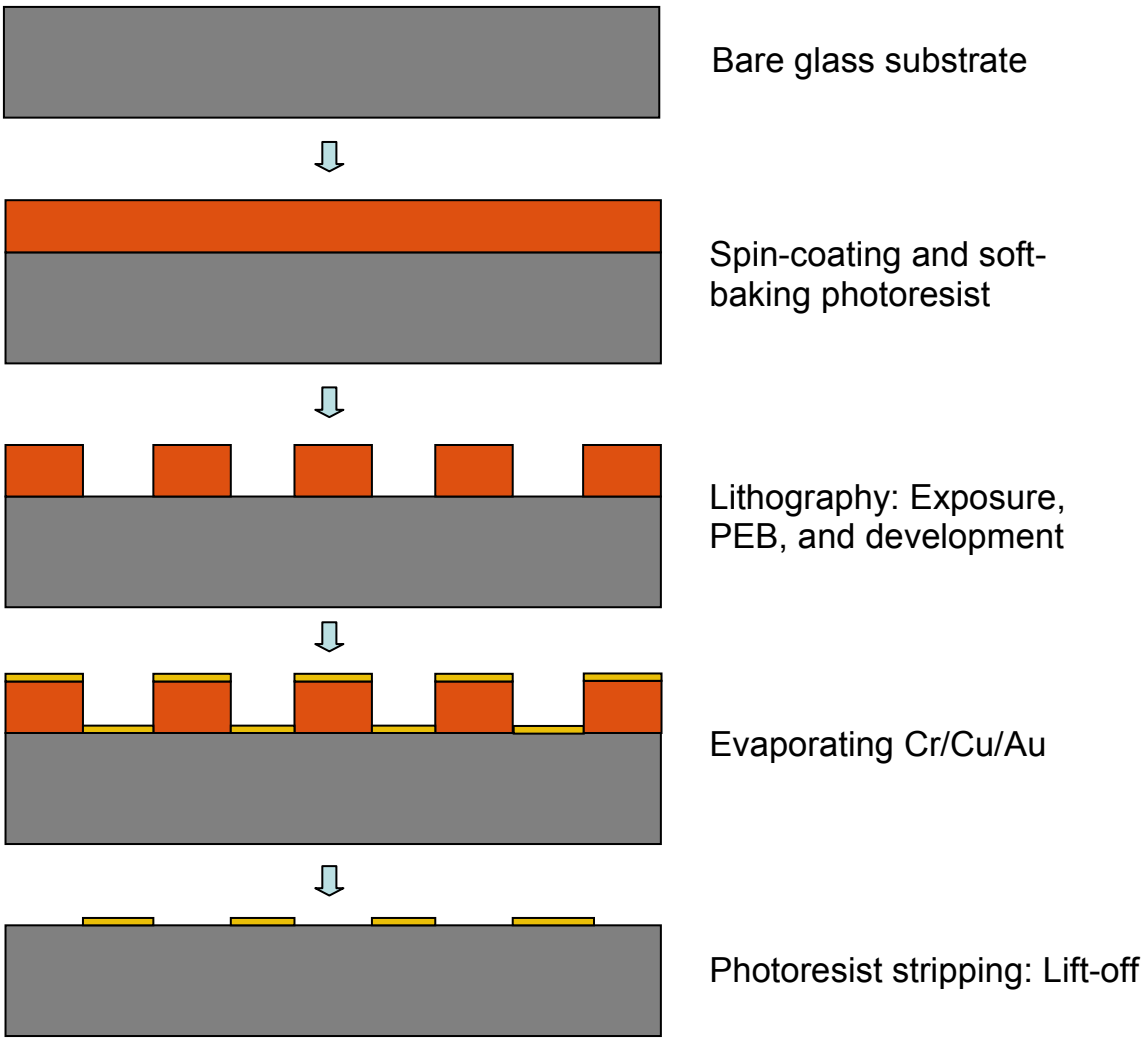


Figure 4.3 Baseline process flow for fabrication of glass substrate.

Table 4.8 Photoresist Processing Conditions for Electroplating Mold on Glass

Spin Coat	1000 RPM/300 Ramp/40 Seconds
Soft Bake	150˚C for 180 seconds on a hot-plate
Exposure	80 seconds; Intensity of 6.1 mW/cm^2 [i-line] using Karl Suss MA6 mask aligner (additional optical filter used

Table 4.8 continued	
	which decreased the intensity).
PEB	100˚C for 180 seconds
Develop	RD-6 for 35 seconds

As mentioned earlier, the NR5-8000 resist is very sensitive to soft bake and post exposure bake temperatures/time, and care has to be taken to maintain the accuracy of these temperatures.

To maximize the resolution, a hard contact and the same high intensity light source was used. The same i-line long pass filter was used here also between the photoresist and the exposure lamp for reasons discussed earlier.

Once the photoresist is exposed and post exposure baked, the resist development is done using the RD-6 developer (Futurrex, Inc.). The resist is developed with agitation in a puddle for 30-50 seconds with continuous agitation. As discussed earlier, at such fine feature sizes it is very important to control the development time very carefully. Any over development of the resist will lead to delamination of the photoresist film. Any underdevelopment will leave undeveloped photoresist at the bottom of the opening that will drastically reduce the adhesion of the metallization to the glass substrate. A bit of over-development is preferred here because it will only help later during the lift-off process. This process leads to very clean openings with little photoresist residue at the

bottom of the trench. The substrate is then thoroughly rinsed with DI water for a few minutes.

After the wafer is washed thoroughly after developing, there is some organic residue left at the resist/Cu interface in the photoresist openings that will drastically decrease the adhesion strength of the metallization to the glass substrate. It is important to remove this residue, and this is done using a plasma assisted descum process. The plasma conditions were same as used for the silicon wafer (Table 4.11). The glass substrate is then transferred to the e-beam evaporator where Cr (400 A), Cu (0.4-1.2 μm), and Au (0.1-0.3 μm) are successively evaporated onto the patterened glass substrate.

Followed by gold evaporation, the photoresist is lifted-off using the RR-4 resist remover (Futurrex Inc.). The lift-off is carried out in ultrasonicator to help the stripper solution reach the fine features. Once the stripping process is complete, the substrate is thoroughly washed with DI water to remove any acidic residues.

5. RESULTS AND DISCUSSION

This chapter discusses the results based on the synthesis methods and test vehicle fabrication described in chapter 4. The chapter begins with the results of electroplated copper bump fabrication at 30 μm pitch. This is followed by a brief discussion on results of glass substrate fabrication by electron beam evaporation and lift-off process. Assembly process development with NCF and n-ACF at 30 micron pitch are then discussed in detail. Insulation resistance comparison and reliability evaluation of ultrafine-pitch copper bumps with NCF and n-ACF are discussed followed by failure analysis of HAST failed samples.

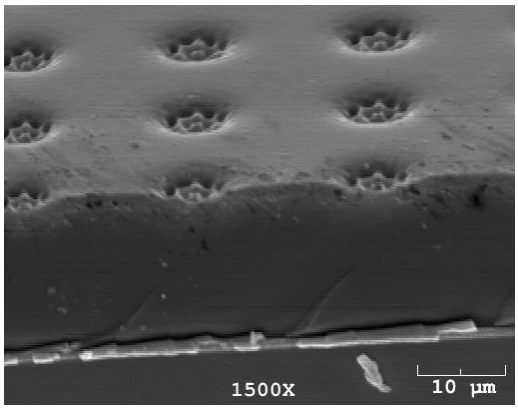
5.1 Fabrication of copper interconnections at 30 micron pitch

Fine-grained copper interconnections were fabricated at 30 micron pitch using the NR5-8000 photoresist. The fabrication steps were described in detail in chapter 4. Like any other electroplating photoresist mold, even in this case the develop cycle is extremely critical. While an improperly or incompletely developed resist opening might lead to no plating through the photoresist opening, over developing the photoresist can cause de-lamination of the photoresist film from the silicon substrate. Since these interconnections are fabricated at ultrafine pitch, even a little overdeveloping of the resist leads to the undercutting and local film delamination, while enough development has to be allowed in order to have clean resist opening and near vertical side-walls. Exposure time is also a critical parameter at such fine pitch. Figure 5.1 shows the effects of these parameters on the opening size, shape and delamination on a 20 micron pitch area-array mold. Figure

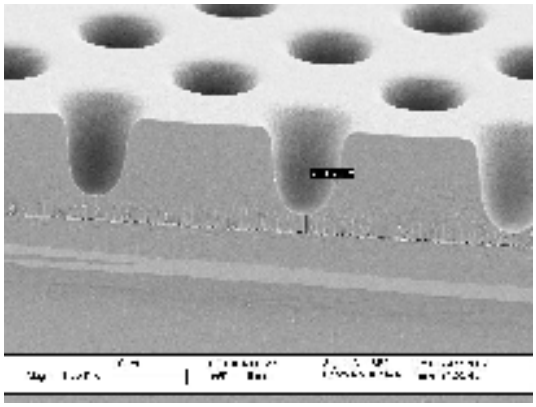
5.1(a) shows an over exposed photoresist which eventually could not be developed; Figure 5.1(b) shows an underdeveloped opening which will prevent any plating through the mold; Figure 5.1(c) shows a completely developed opening that has started delaminating from the base and may not be acceptable if having near-vertical side-walls is critical for the particular application; Figure 5.1(d) displays a clear opening, with no residue and no delamination, obtained by an ideal development cycle; Figure 5.1(e) shows copper interconnects plated through a highly delaminated mold causing underplating.

Once the photoresist development is complete, copper is plated through the photoresist openings to a thickness of 8-9 μm. The photoresist mold is then removed, followed by seed layer etching to yield copper interconnections at 30 μm pitch. SEM pictures of the interconnections fabricated using the above described processes are shown in Figure 5.2. Figure 5.3 shows some optical micrographs of the copper interconnections.

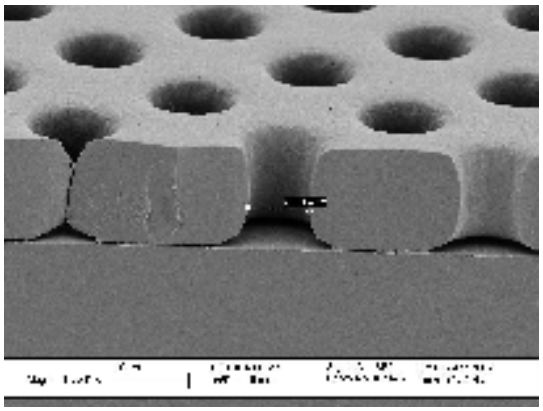
Interconnections with 15 microns diameter 8.5 microns height and 30 micron pitch were fabricated as shown below. The fabricated chips are assembled on to glass substrate, and these assembly experiments will be discussed in detail in later sections.



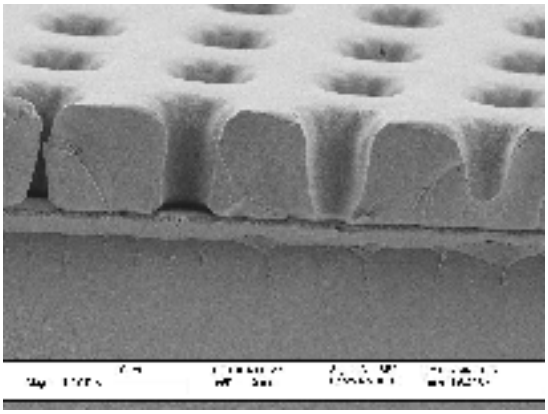
(a)



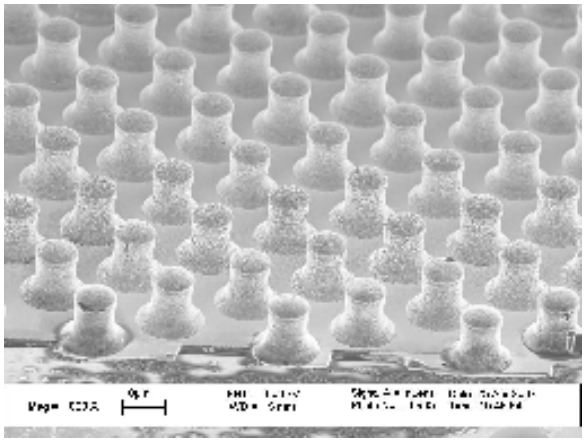
(b)



(c)



(d)



(e)

Figure 5.1 (a) An over-exposed photoresist opening, (b) an under-developed photoresist opening, (c) a completely developed opening that has starting delaminating, (d) a clear opening obtained by an ideal development cycle, (e) copper interconnects plated in a highly delaminated photoresist mold causing underplating.

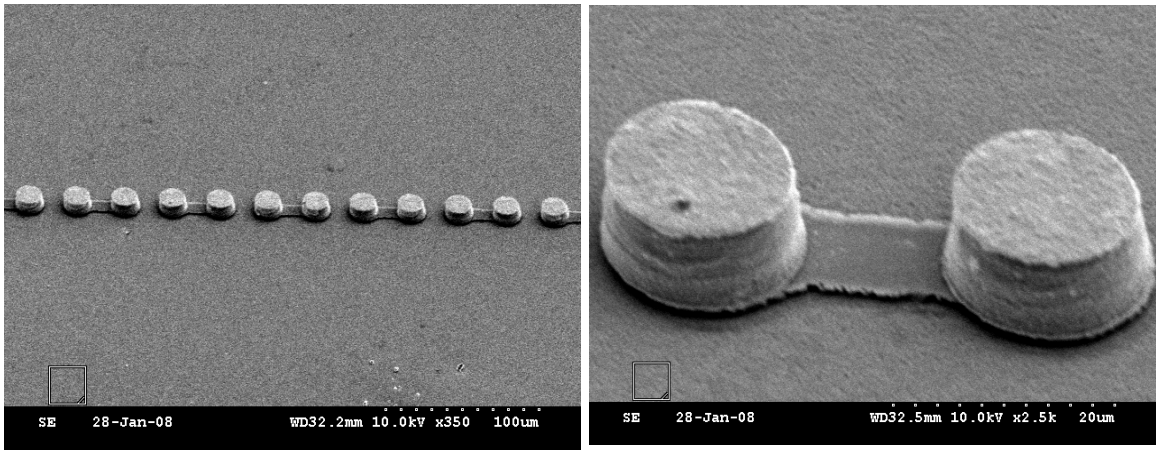
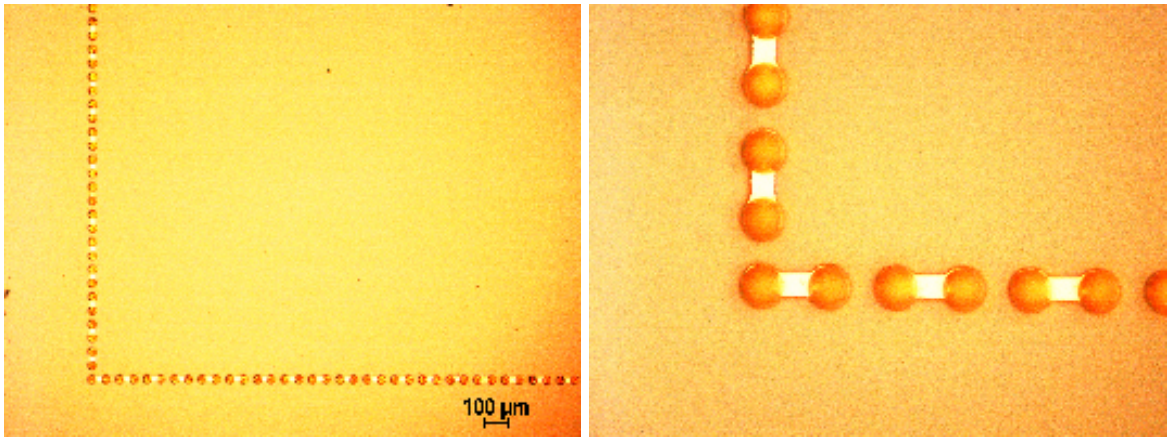


Figure 5.2 Electroplated copper interconnects with 0.5 μm evaporated gold at 30 micron pitch.



(a) ***(b)***

Figure 5.3 (a)&(b) Optical micrographs of electroplated copper bumps with evaporated gold protection at the top.

Assembly of these copper interconnections with nano-ACF or NCF requires very good coplanarity of the bumps. The more the non-coplanarity, the higher the required force will be to yield all the interconnections. In typical micro-ACF, the filler particles are micron-sized, soft elastic particles that can compensate for the non-coplanarity of the bumps. They also compensate for the hygroscopic expansion of the epoxy during the HAST testing. Since there are no micron-sized, soft particles in the nano-ACF/NCF, the

bump material has to deform to compensate for the non-coplanarity. Typically, adhesive materials have been used with gold bumps with chip-on-flex kind of applications. Since, gold is a softer material; it can easily deform and compensate for non-coplanarity. Use of copper as an interconnection material (which is harder than gold) coupled with the non-elastic particles demand very high level of coplanarity in the copper bumps.

Coplanarity measurements were performed on the 30 micron pitch copper bumps to ensure that the coplanarity requirement is met before assembling these bumps onto glass substrate with n-ACF/NCF. SEM was used to measure the bump heights of dies from different locations on a wafer. Figure 5.4 shows a plot of bump height versus frequency. Table 5.1 shows the height variation statistics for the electroplated copper bumps. Figure 5.5 shows SEM pictures of a few copper bumps on which the height measurements were carried out. SEM is not the best method to carry out coplanarity measurements but it can be used for a relatively small sample size.

SEM measurements reveal good coplanarity of the bumps. The average height of the bumps was 8.34 μm. Al the bumps were within 2 standard deviations. As seen from Figure 5.4, there are a few fall-outs (7.6 μm and 8.9 μm) that may cause problems for assembly. These fall-outs could be easily seen at 500X magnification in the optical microscope. This is because at such large magnification, the depth of field is very small and even a few microns variation in height can be quantitatively estimated. The SEM measurements were correlated with the optical microscopy examination of the bumps and the good dies were chosen based on the optical inspection at high magnification.

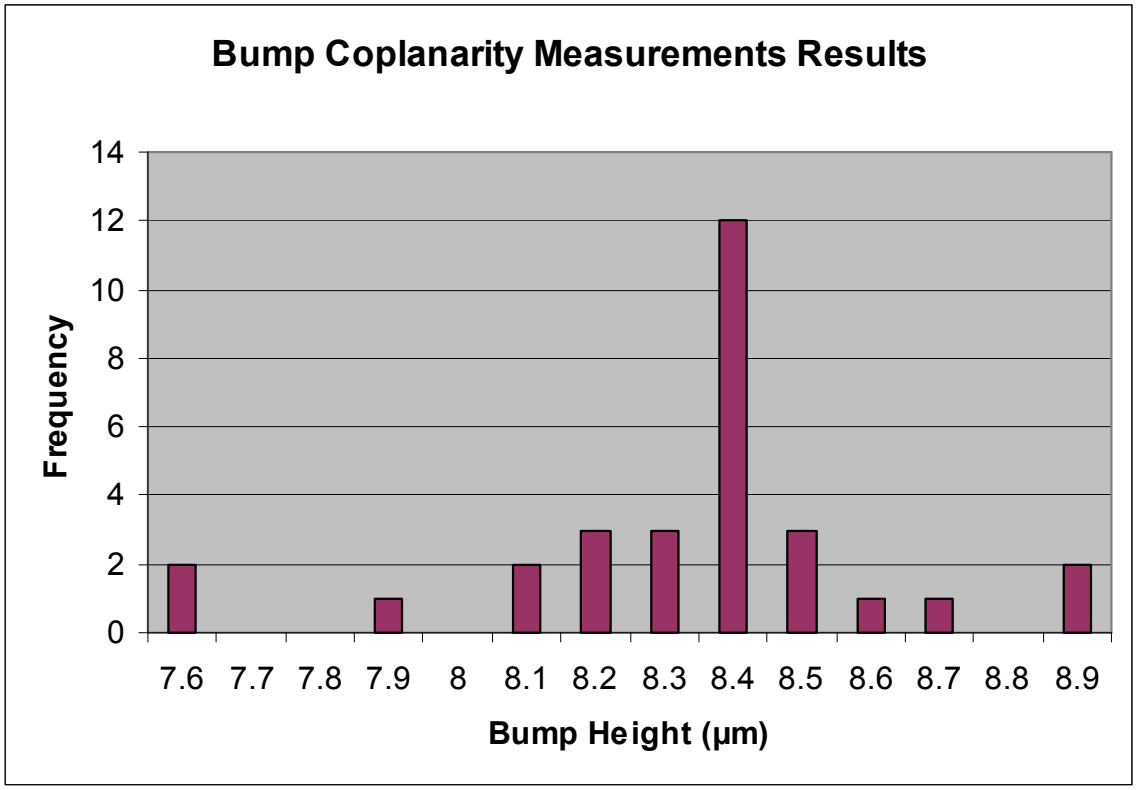


Figure 5.4 Electroplated copper bump coplanarity measurements results.

Table 5.1 Height variation statistics of electroplated copper bumps.

Average	8.34 μm
Minimum	7.6 μm
Maximum	8.9 μm

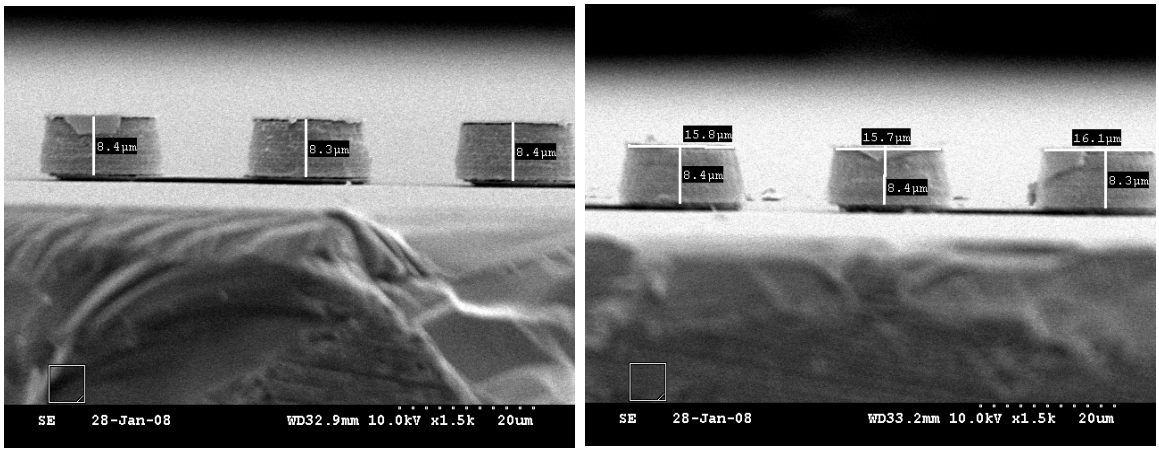


Figure 5.5 SEMs of height measurement of electroplated copper bumps.

5.2 Fabrication of glass substrate at 30 micron pitch

As described earlier, glass substrate was chosen for its flatness and transparency which will assist in measuring the chip-substrate misalignment. To get a very good planar metallization, electron-beam evaporation and lift-off was used. NR5-8000, aqueous processiable photoresist, developed by Futurrex was used. The photoresist processing conditions were described earlier. The photoresist was slightly over-developed to make the lift-off process easy. Since the features are extremely fine and the gap between two adjacent bond-pads is only 10 microns, too much over-development could cause shorts. Lift-off with resist remover RR4 was carried out in ultrasonicator. It was observed that a slight over-development obviates the use of ultrasonicator. Chrome was found to have very good adhesion on the glass surface. No additional metal finish was required since the substrate metallization had a top layer of evaporated gold for protection from oxidation during assembly process.

Substrate test structure consists of a single metal layer with bonding pads of 20 μm diameter and 20 μm lines for escape routing the daisy-chain test structures. The final diameter of the bond-pads after lift-off was around 18 μm. The escape lines were designed to be 20 microns where they start at the bond-pads for a length of about 100 μm after which they were widened to 50 microns to increase the yield of the lines and to decrease their DC resistance. The final widths after lift-off were around 18 μm and 48 μm. Figure 5.6 displays optical micrographs of die-side bond pads and escape routing lines for the daisy-chain test structure. Figure 5.7 shows high density substrate fabricated on glass.

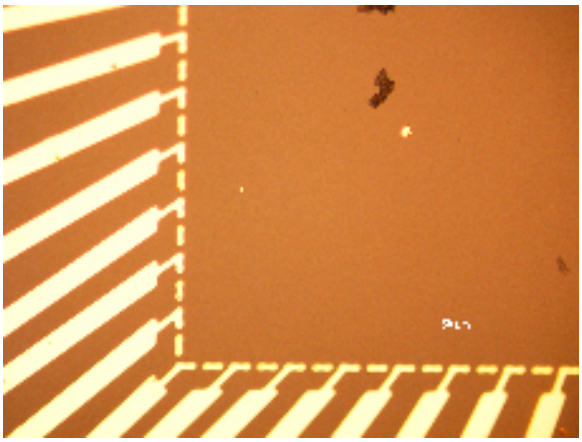


Figure 5.6 Die-side bond pads and escape routing lines for the daisy-chain test structure.

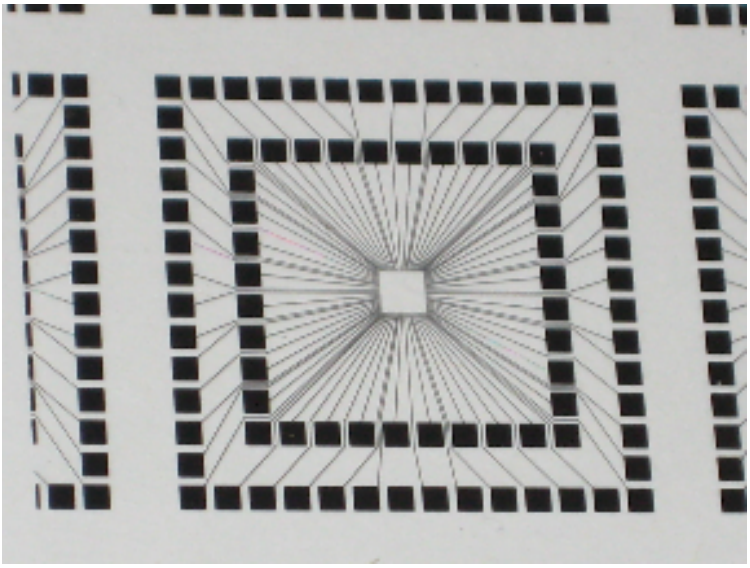


Figure 5.7 High density substrate fabricated on glass

5.3 Assembly processes using advanced adhesives

Electroplated Copper interconnections at 30 micron pitch have been assembled on to glass carrier using Non Conductive Films (NCF) and nano-Anisotropic Conductive Films (n-ACF). The assembly processes and conditions are described in this section.

Non conductive anisotropic conductive film, commonly known as ACF, is a lead-free and environmentally-friendly epoxy system that has been used for almost 30 years in the flat panel display industry to make the electrical and mechanical connections from the device electronics to the glass substrates of the displays. ACF works by trapping conductive particles between the corresponding conductive pads on the IC and the substrate. Typical ACF consists of a very stable matrix of 3-5μm polymer spheres, each nickel-gold plated and then coated with a final insulating layer that protects them against

shorting through contact with a neighboring particle. The insulated particles are distributed in such a way that their incidental contacts in the X and Y axes are low.

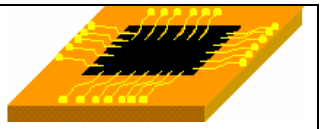
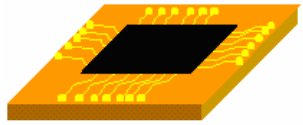
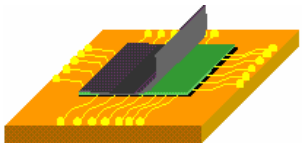
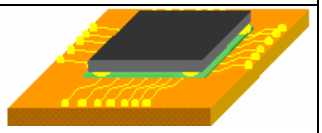
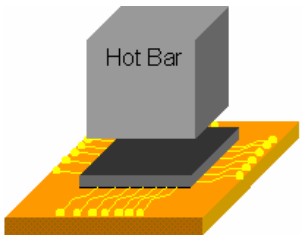
During the bonding process, the insulation layer in the Z-axis where the balls are trapped is pushed away, allowing the metal layer on the particle to form an electrically conductive path between the IC and the substrate, while not shorting in the X and Y directions. The epoxy cures, locking the particles in this compressed state. The elasticity of the compressed trapped particles causes them to constantly press outward on both contact points, helping to maintain electrical connections through a wide range of environmental conditions.

Typical ACF was not appropriate for such fine pitch as used in this study. This is because the gap between two adjacent bumps is only 15 microns and 2-3 microns metallic particles could cause electrical shorts. Also, because of the relatively small bump diameter, there won't be enough particles between each bump and corresponding bond-pad. A novel nano-scale conductive film developed by Wong et. al [72] which combines the advantages of both traditional anisotropic conductive adhesives/films (ACAs/ACFs) and nonconductive adhesives/films (NCAs/NCFs) was used. This film was introduced and developed for next generation high performance ultra-fine pitch packaging applications. This novel interconnection film possesses the properties of electrical conduction along the Z-direction with relatively low bonding pressure (ACF-like) and the ultra-fine pitch (< 100 μm) capability (NCF-like). Unlike typical ACF which requires 1-5 vol% of conductive fillers, the novel nano-scale conductive film only needs less than 0.1

vol% conductive fillers to achieve good electrical conductance in the z direction. The nano-scale conductive film also allows a lower bonding pressure than NCF to achieve a much lower joint resistance (over two orders of magnitude lower than typical ACF joints) and higher current carrying capability. With low temperature sintering of nanosilver fillers, the joint resistance of the nano-scale conductive film could be as low as 10^{-5} Ohms, even lower than the NCF and lead-free solder joints. The insertion loss of nano-scale joints are almost the same as the standard ACF or NCF joints, suggesting that the nano-ACF joints are suitable for reliable high-frequency adhesive joints in microelectronics packaging. In this nano-ACF, the Silver nano fillers are passivated/ protected with Self-assembled molecular wires (SAM) to help reduce silver migration and maintain a good insulation/dielectric property in the x-y plane. Epoxy film without any filler particles (NCF) was also used for comparison.

Assembly with n-ACF/NCF was carried out using Fineplacer assembly tool. The n-ACF/NCF film was applied onto the substrate. The chip and substrate were then aligned and pre-heated at 80^{o}C to decrease the viscosity of the epoxy. Followed by this, the chip and substrate were pressed together and heated upto 180 ^{o}C for 10 minutes to ensure complete curing of the epoxy and to give enough time for sintering of Ag nanoparticles. During the curing process, the epoxy shrinks and holds the chip and substrate together enabling a mechanical contact in case of NCF and a metallurgical contact in case of nano-ACF due to the sintering of nano-Silver particles to the substrate metallization and bump surface. Table 5.2 give detailed steps for n-ACF/NCF assembly process.

Table 5.2 Steps for n-ACF/NCF assembly process

Step 1: Prepare the substrate. The substrate in this case was glass carrier with Cr/Cu/Au metallization.	
Step 2: Laminate the ACF to the substrate. This is done by cutting a length of ACF from a reel of ACF pre-slit to the required width. The ACF is laid in place over the bonding area and is heated for 3-5 seconds at 80°C for it to adhere to the glass substrate well. No heavy load needs to be applied to the n-ACF/NCF film in this step.	
Step 3: n-ACF/NCF has a release liner on its rear surface to prevent it from adhering to anything else during the lamination procedure. This must be removed without damaging the ACF layer or causing any delamination within the bonding area.	
Step 4: IC is then aligned to the substrate. Alignment is done through the ACF by looking at the reflective gold beneath it.	
Step 5: The substrate is then heated to 80°C to decrease the viscosity of the polymer. The IC is brought in contact with the substrate. The final process subjects the ACF to high temperature and pressure, permanently curing the epoxy and attaching the IC to the substrate. The bonding profile used is 180°C and a load of approximately 300 MPa for 10 minutes.	

Once the bonding process is complete using the above steps, the continuity of the daisy chains are verified using a multi-meter, and the resistances of various daisy chains are measured. Due to the fine pitch and very thin and narrow traces, bond-pads and probe pads, the resistance of the traces itself is quite high (20-40 Ohms depending on the actual position and hence length of the particular trace.) The bump resistance and contact resistance are very small values compared to the trace resistances and hence if the flip chip assembly has successfully bonded the resistance measured must be very close the resistance of the corresponding traces. If resistance measurement is high or resistance is increasing it means that the epoxy has not already set i.e., bonding is not complete. In such a case, the final curing step is repeated for a few more minutes followed by electrical continuity verification with the multimeter.

5.4 Assembly process optimization at 30 micron pitch

Assembly process optimization was a major challenge faced during this study. Adhesives being non-self aligning coupled with ultrafine-pitch and ultrathin interconnections made the process highly unforgiving towards parameters like non-coplanarity and tilt. Unlike solders, adhesives are not self-aligning and therefore need much better alignment accuracy during assembly. This situation is worsened by the ultrafine-pitch and ultrashort interconnections. At 30 μm pitch and 15 μm bump diameter with 18 μm substrate bond-pads, the alignment accuracy is less than 1.5 μm.

Two types of assembly tools were tried – one with a vertical movement of bond-head (CB5 flip-chip bonder from RD Automations) and another with a swinging arm type

movement (Fineplacer from Finetech). The alignment accuracy of the CB5 was about 5 μm and there was erratic misalignment depending upon the lowering speed of bond-head (which could not be controlled quantitatively). Finetech claims to have alignment accuracy of 1 μm and after careful calibration and tweaking of optics, perfect alignment with around 1 μm accuracy was achieved. However, fineplacer being a swinging arm type tool, the tool length also comes into picture. Figure 5.8 schematically (profile view from the left side of the tool) shows the effect of tool length on the die tilt after assembly. Figure 5.8 (a) shows the three situations (snapshots of the machine before assembly) where the length of the tool is less than, greater than, and approximately equal to 22 mm respectively. Figure 5.8 (b) shows the same three situations after assembly resulting in tilted die in the first and third situations and perfectly horizontal die in the second situation where the tool length was perfect.

According to the machine geometries, the sum of the tool head length and die thickness has to be 22 mm. Based on the calculations on machine geometries, a 50 μm error in the total tool length was expected to give a tilt of 1 μm across a 3 mm die. Since the bumps were only 8.5 μm thick, even a couple of microns of tilt could prevent the die from yielding completely on all 4 sides. The length of the tool used was 21 mm and the wafer thickness was around 500 μm. The typical die-map for assemblies obtained from this tool configuration is shown in Figure 5.9 (a). The green color of pad means connection and red color means an open. The total tool length was still 500 μm short of the required 22 mm. Spacers with 400 μm and 500 μm thicknesses were tried to increase the total length to the required 22mm. Figure 5.9 (b) and (c) display die-maps for

assemblies obtained with 400 μm and 500 μm spacers respectively. Figure 5.10 shows a plot of connection frequency versus probe pad number for 8 different assemblies carried out without spacer. Connection frequency tells us in how many dies a particular probe pad was connected. The probe pads were numbered according to the position of the die during the assembly process. Table 5.3 shows which probe pads belong to which side of the die.

As can be clearly seen from Figure 5.8, tool length less than 22 mm is expected to cause only the bottom side of the die to make connections. This was verified from Figure 5.9 (a) where typically only the bottom side and a few bumps on the left and right side that are adjacent to the bottom side are connected. Figure 5.10 statistically corroborates the same thing by showing that the bottom side (probe pads 23-43) (Table 5.3) and a few adjacent bumps are connected in most of the dies assembled without spacer.

With the incorporation of a 400 μm spacer, the die is expected to land on the substrate more horizontally that without any spacer. This hypothesis is verified by Figure 5.9 (b) where the number of bumps connected on the left and right side increased after incorporation of 400 μm compared to the situation before although the die is still not completely connected. With the incorporation of a 500 μm spacer, the die is expected to land nearly horizontal onto the substrate. Figure 5.9 (c) represents this scenario and thus proves the hypothesis.

One of the tilted assemblies was cross-sectioned and the tilt was measured using SEM. The gaps between the chip and substrate were measured at two ends and there was around 7 μm tilt across the die. This completely explains the hypothesis of die-tilt.

Chips were assembled onto glass substrates with this optimized assembly process and reliability tests were carried out on these optimized assemblies. Figure 5.12 displays a 30 micron pitch 3 mm x 3 mm die assembled onto a high density glass substrate. Figure 5.13 shows optical micrographs of as-assembles samples as seen from the back side of transparent glass substrate. Figure 5.14 shows optical and SEM micrographs of cross sections of as-assembled chips bonded with n-ACF on glass substrates. Permanent deformation and barreling can be clearly seen on the copper bumps. The lighter region between the bump and substrate pad is the Au of the chip and the substrate side. The cross sections of as-assembled samples also reveal that the pressure used was enough to squeeze out all the epoxy between bumps and substrate bond pads.

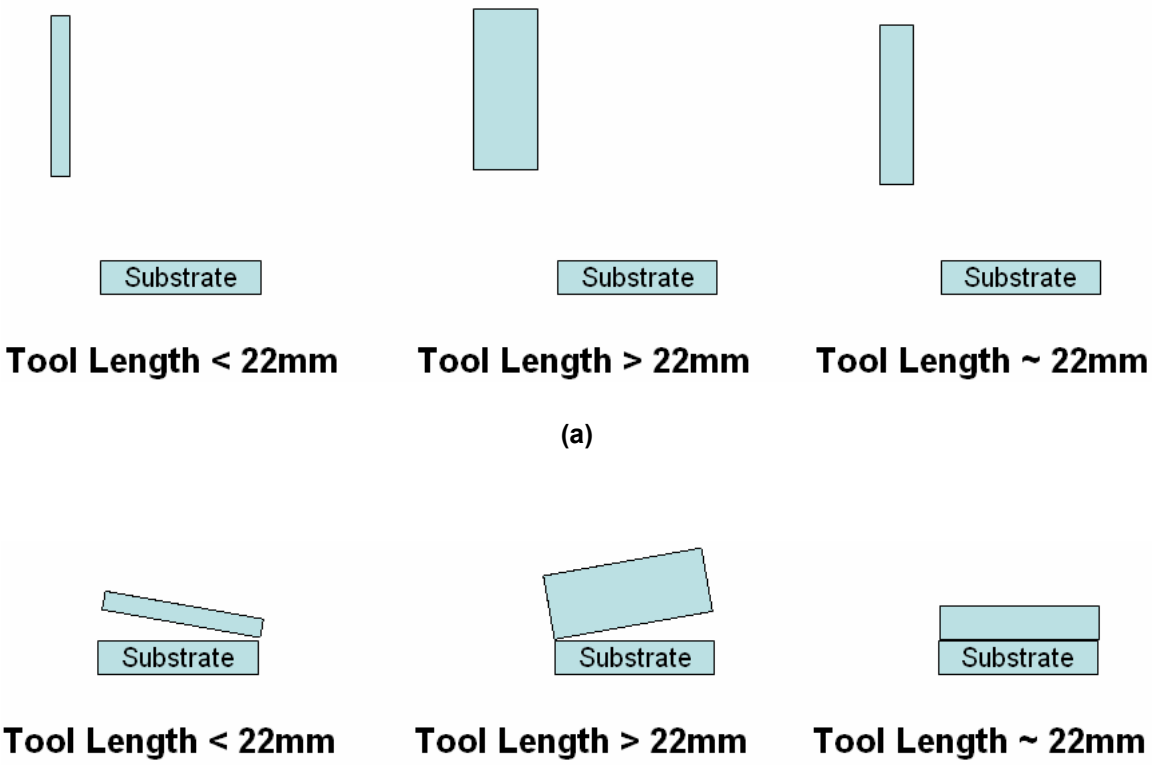


Figure 5.8 Schematic representation of the effect of tool length on die tilt after assembly.

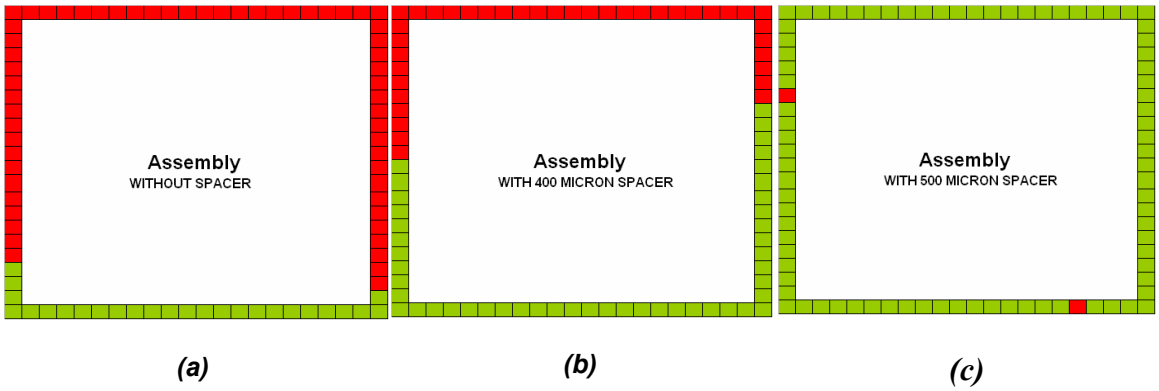


Figure 5.9 Typical die-maps for assembly (a) without spacer, (b) with 400 μm spacer, (c) with 500 μm spacer.

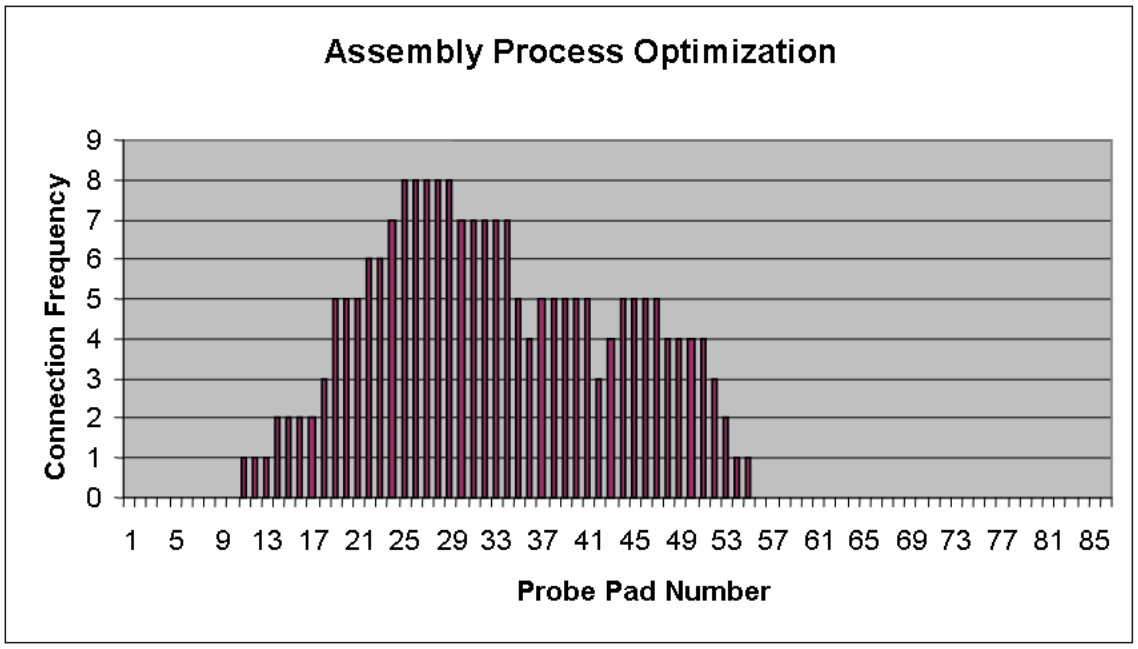


Figure 5.10 Plot of connection frequency versus probe pad number for 8 different assemblies carried out without spacer.

Table 5.3 Probe pad numbering according to die-sides.

Probe Pad #	**Die Edge**
1-22	Right
23-43	**Bottom**
44-65	Left
66-86	Top

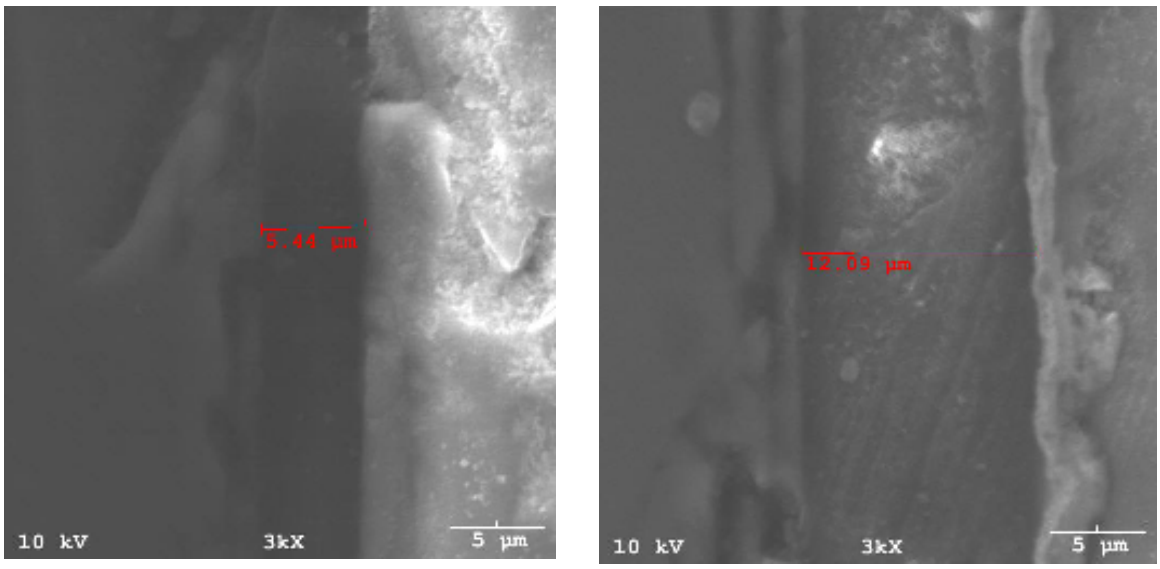


Figure 5.11 Cross section of tilted die for measurement of die tilt.

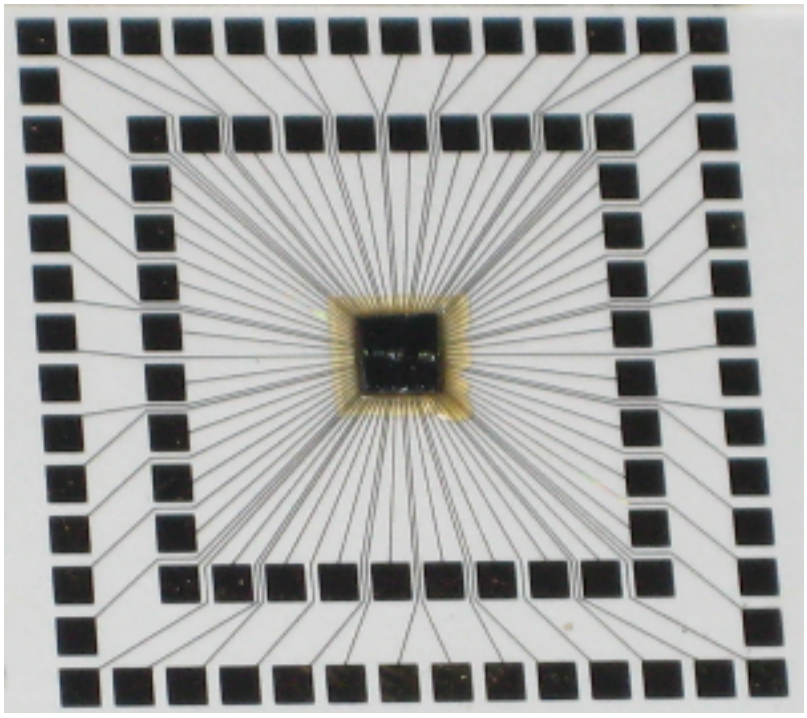


Figure 5.12 30 micron pitch 3 mm x 3 mm chip assembled onto a high density glass substrate

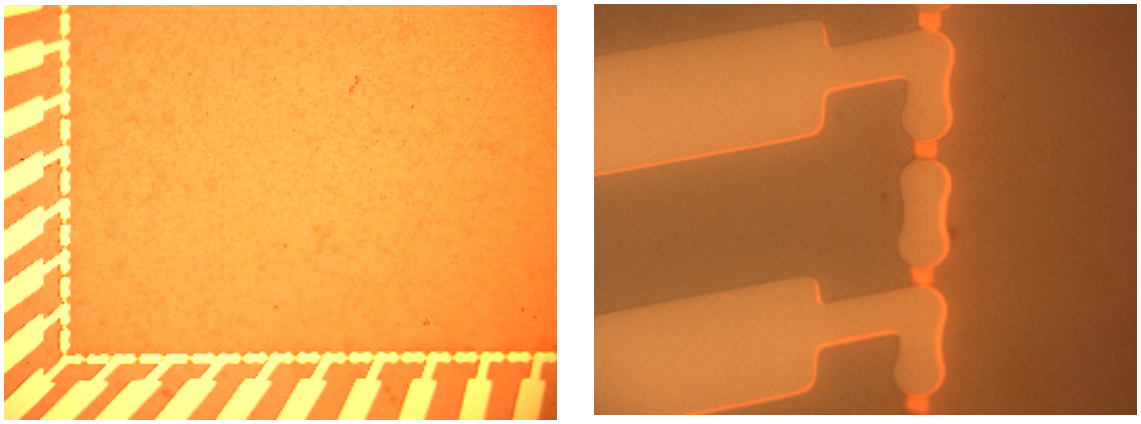


Figure 5.13 Optical micrographs of as-assembled samples as seen from the back side of transparent glass substrate.

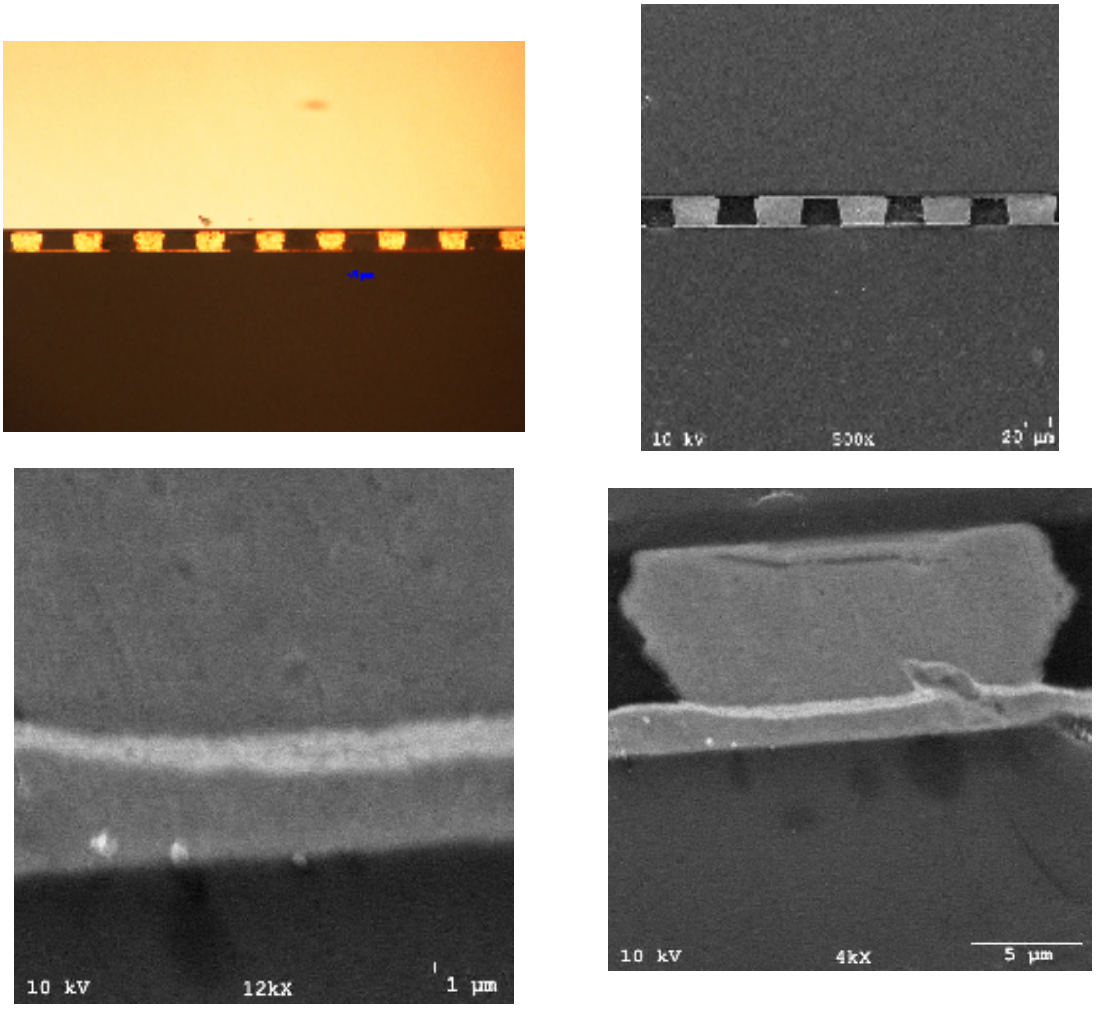


Figure 5.14 Optical and SEM micrographs of cross sections of as-assembled chips on glass substrates

5.5 Insulation resistance comparison of n-ACF and NCF at 30 micron pitch

At ultrafine pitch of 30 μm, the gap between the two adjacent pads is only 15 μm. Leakage current or lateral conductance has to meet certain specifications and at such fine pitch with dispersed metallic particles, it could be a major concern. As described earlier, six pairs of adjacent bumps were deliberately left unconnected through chip or substrate side traces to enable insulation resistance measurement. Figure 5.15 shows the I-V curves for the insulation resistance of n-ACF and NCF. The average insulation resistances at 30 μm pitch for NCF and n-ACF were 7.82E+11 Ohms and 4.69E+11 Ohms respectively. The currents measured were in picoAmps range at 0-2 Volts for both n-ACF and NCF. These measurements clearly indicate that incorporation of 0.1% Ag nano-fillers doesn't change the insulation resistance and leakage current values between two adjacent bumps.

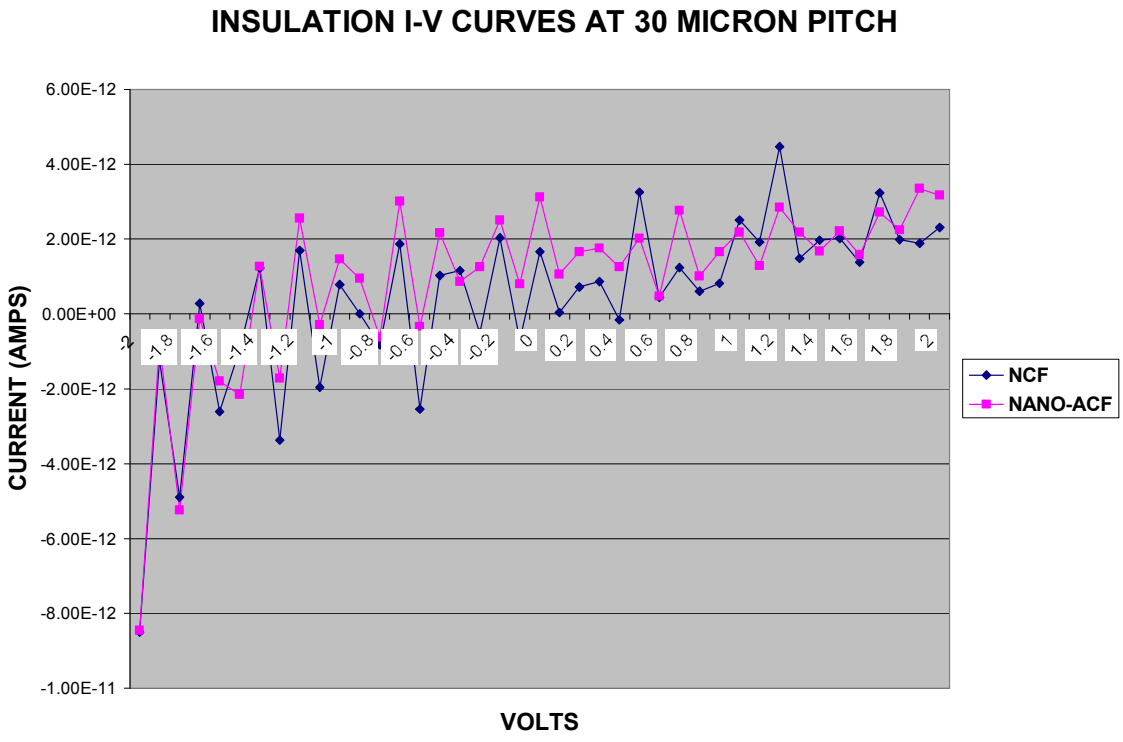


Figure 5.15 I-V curves for the insulation resistance of n-ACF and NCF

5.6 Reliability evaluation of 30 micron pitch copper bump with advanced adhesives

Package qualification strategies require aggressive reliability tests to ensure that the package exceeds minimum reliability test requirements. Therefore, choosing a correct qualification test is necessary. Humidity and temperature assisted swelling called hygroscopic expansion is the most dominant failure mechanism in conductive and non-conductive adhesives. To asses the reliability of the 30 micron pitch copper interconnections, the optimized assemblies with both n-ACF and NCF were put through rigorous HAST (Highly Accelerated Stress Testing) testing. HTS (High Temperature storage) was also performed on assemblies with both n-ACF and NCF

Following the assembly using various bonding interfaces, the samples were electrically tested for their initial contact resistance and integrity of the daisy chained contacts. Subsequently, they were subjected to HAST (unbiased 130C/85%H) until failure and HTS (175 C bake in air in a convection oven) for 72 hours Based on the results obtained, additional electrical continuity tests were performed. Figure 5.16 schematically shows the reliability tests carried out on the optimized assemblies. The failure analysis of various failed components is presented in the following sections.

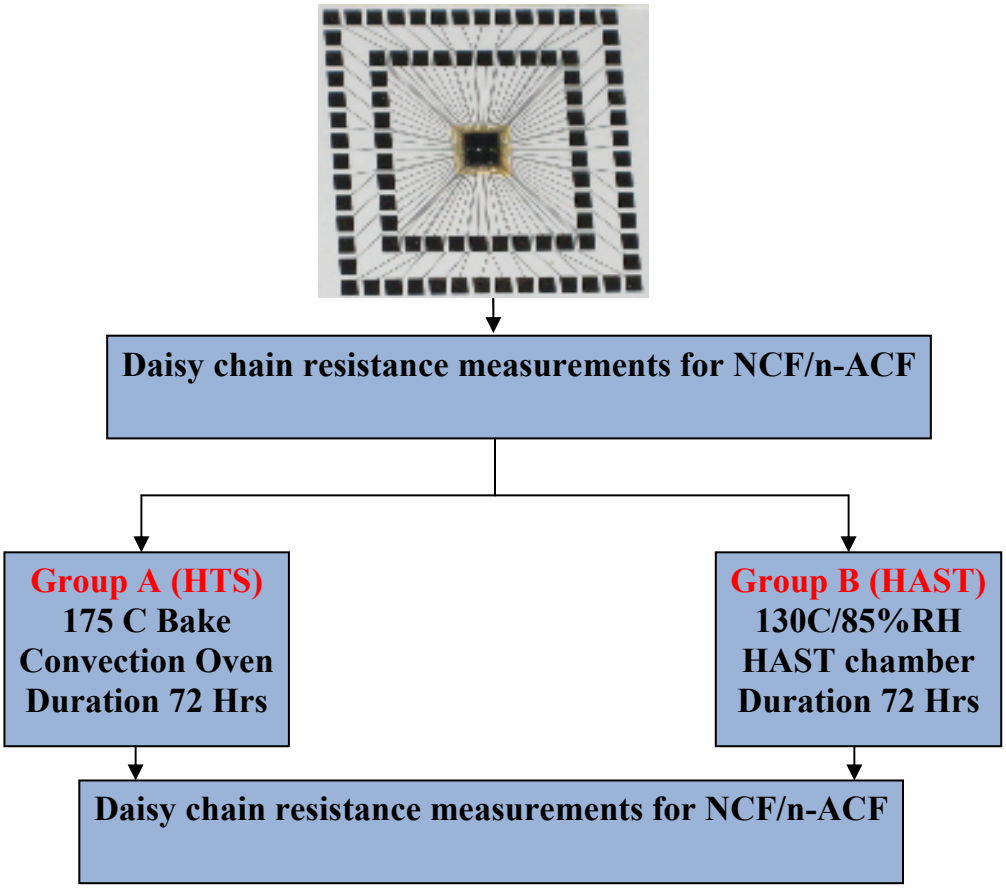


Figure 5.16 Schematic representation of reliability test conditions carried out on optimized assemblies

5.6.1 Reliability of 30 micron pitch Copper bump in HTS

As mentioned earlier, optimized assemblies were subjected to High Temperature Storage (HTS) at 175 °C for 72 Hours. Samples were taken out after every 12 hours for first few times and after every 24 hours later on and daisy-chain resistances were measured. The change in DC resistance, with time of HTS, daisy-chains for samples bonded with NCF and n-ACF is shown in Figure 5.17. To normalize the effect of variations in the resistances of the traces from sample to sample, normalized average resistances were also plotted to get a better comparison. Figure 5.18 shows normalized average change in DC resistance during HTS at 175 °C for samples bonded with NCF and n-ACF. No failures were observed in any of the NCF or n-ACF samples during HTS testing.

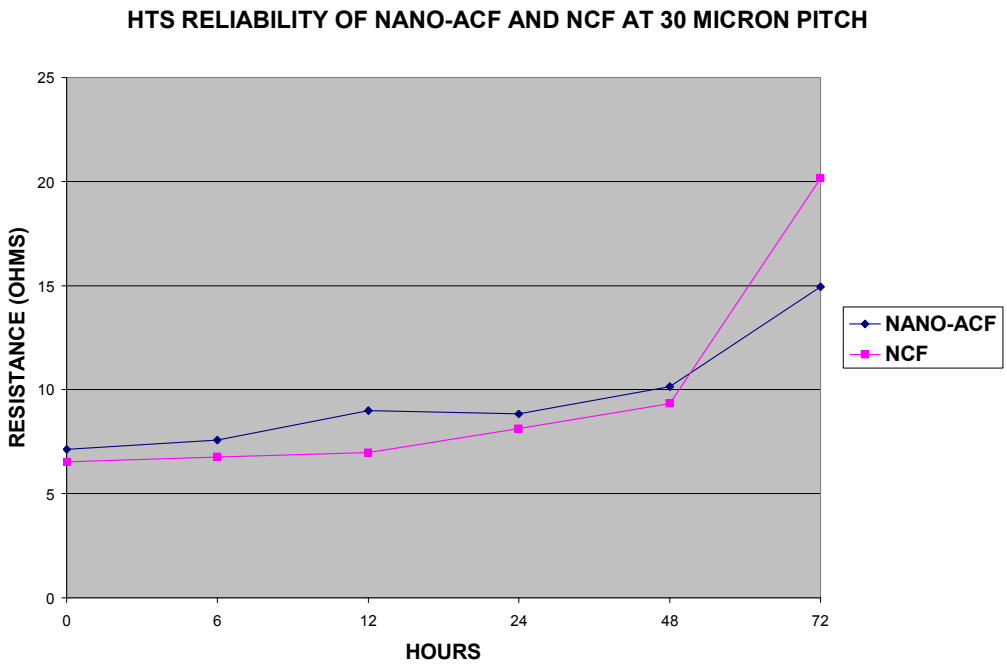


Figure 5.17 Change in DC resistance during HTS at 175 °C for samples bonded with NCF and n-ACF

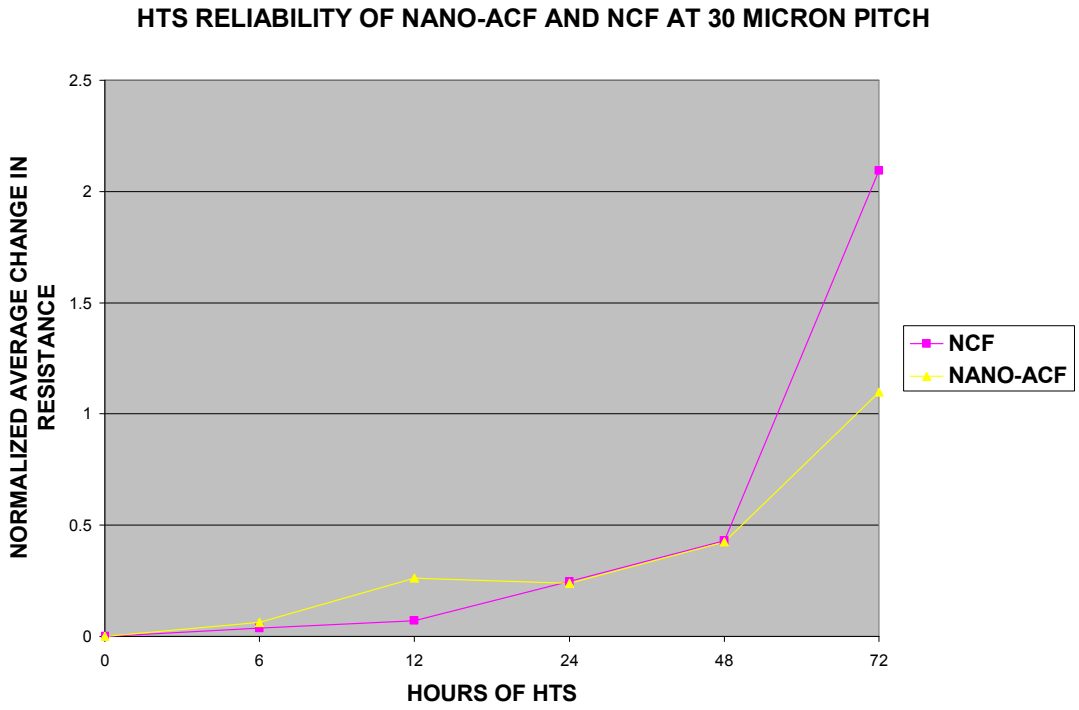
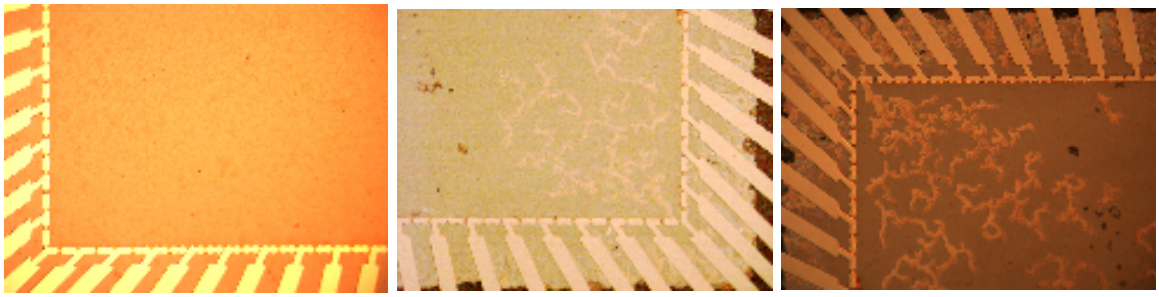


Figure 5.18 Normalized average change in DC resistance during HTS at 175 °C for samples bonded with NCF and n-ACF

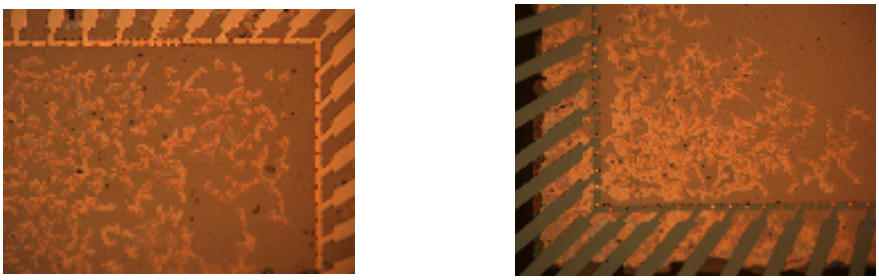
5.6.2 Reliability of 30 micron pitch Copper bump in HAST

Optimized assemblies, bonded with both NCF and n-ACF, were subjected to HAST (130°C/85%RH) until failure. Very early failures were observed during HAST with both NCF and n-ACF. Use of transparent glass substrate enabled visual inspection of samples for any traces of moisture ingression or other changes during the HAST testing. Figure 5.19 shows optical micrographs, from the back side of the transparent glass substrate, of as-assembled sample and sample after 1 hr, 2 hr, 3 hr, and 5 hr of HAST. Moisture ingression can be clearly seen in all the micrographs except the as-assembled one which looks perfectly clean. Moreover, moisture content keeps on increasing with the duration of HAST. Also, as seen from the micrographs, moisture

seems to be seeping-in from the edges and migrating to the center with time. This seems to be causing local hygroscopic swelling of the adhesive due to moisture retention. This swelling seems to be pulling the chip and substrate apart by increasing the gap between them, resulting in a decrease of contact area between the bump and substrate bond pad, which in turn results in the increase in contact resistance ultimately leading to failure.



(a) As Assembled *(b) After 1 Hr HAST* *(c) After 2 Hr HAST*

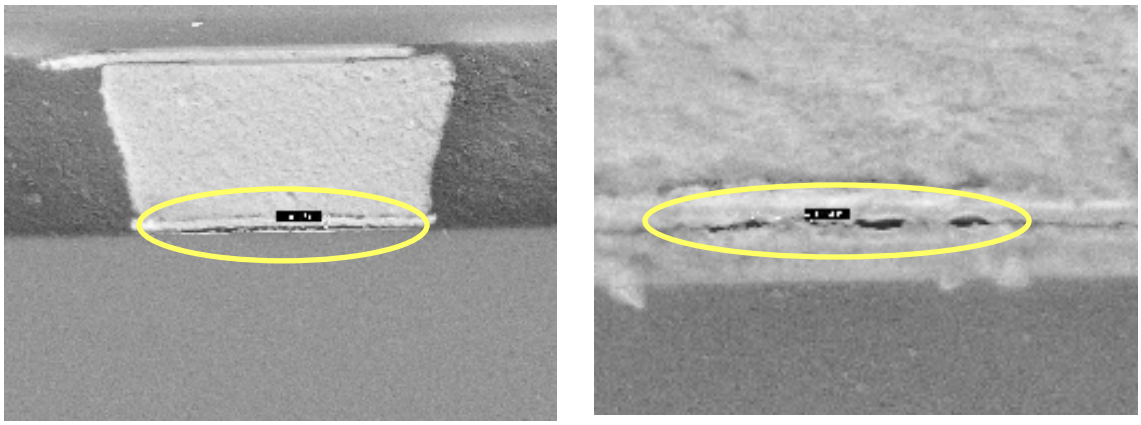


(d) After 3 Hr HAST *(e) After 5 Hrs HAST*

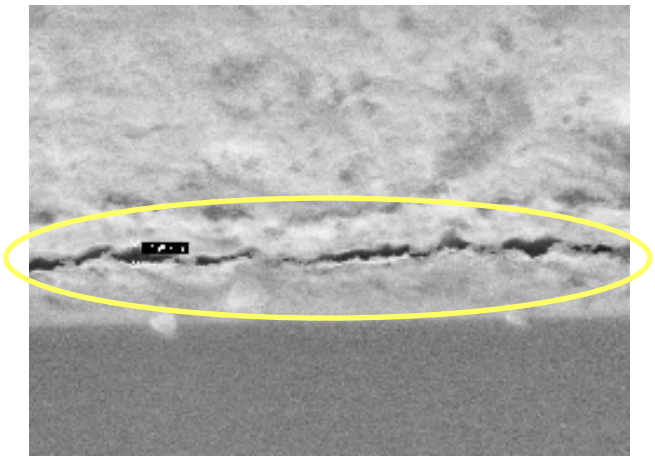
Figure 5.19 Optical micrographs, from the back side of the transparent glass substrate, of as-assembled sample and samples after 1 hr, 2 hr, 3 hr, and 5 hr of HAST

Figure 5.20 shows SEM images of samples failed during HAST. Cracks can be seen along the bump and substrate bond pad interface. It should be noticed that the crack is between the gold-gold interface, i.e. between the gold on bump side and the gold on the substrate bond pad. It is clearly evident that moisture ingression and resulting hygroscopic swelling caused expansion in the epoxy material in the z-direction resulting

in crack generation and propagation along the bump-side gold – substrate bond pad-side gold.



(a) *(b)*



(c)

Figure 5.20 SEM images of cross sections of samples failed during HAST

Based on the cross sections of the failed samples, the reason for early increase in resistance and failures is expected to be hygroscopic swelling and expansion of epoxy material causing pulling apart of chip and substrate. Such early failures could have been caused by poor adhesion of epoxy to glass resulting in moisture ingression through the

epoxy-glass interface. An adhesion promoter, in this case, could significantly improve the reliability. Sintering of Ag nano-particles is expected to result in a metallurgical bond between the chip and substrate side gold layers. Oxidation of Ag nano-particles might have prevented or decreased the amount of sintering that would have happened otherwise. Higher temperatures and times of bonding might also help increase the amount of sintering of Ag nano-particles to the chip and substrate side gold layers, providing a more reliable metallurgical bond that can withstand some expansion of the epoxy.

As mentioned earlier, it seems that the moisture penetration occurred along the interface between glass and epoxy. This could be due to poor adhesion of epoxy to glass per se. Local delamination of the epoxy from glass, providing path for moisture, could also be due CTE mismatch between glass and epoxy which causes high interfacial stresses. Incorporation of low CTE fillers in the epoxy can reduce the CTE mismatch and is believed to improve the reliability. Changing the chemistry of the epoxy itself by adding moisture scavengers can possibly help reduce moisture absorption resulting in better reliability. Since adhesive interconnections are shown to be thermo-mechanically very reliable, incorporating the above suggestions can make nano-adhesive an extremely reliable interconnection technology at ultrafine-pitch.

6. CONCLUSIONS AND OPPORTUNITIES FOR FUTURE WORK

This chapter is divided into two sections. First section summarizes the work done and contains conclusions that can be drawn from it. Second section explores the scope of future work in order to explore this work further.

6.1 Conclusions

Unceasing demands for better performance, higher functionality, portability and low cost has driven the Moore's law and System-On-Package technology. Short and reliable interconnections are becoming very critical both for next generation micro-systems packaging. Ultrafine pitch chip-package interconnection is a key cornerstone for SoP and the need for ultrafine pitch interconnections is multifold. WLSOP needs ultrafine-pitch interconnections to close the IC-to-board I/O gap. Device downscaling demands interconnections with extremely high electrical and mechanical performance. Multicore architectures and low-cost RF modules are emerging applications that are driving high density packaging with ultrafine-pitch chip-package interconnection. TSV bonding has also provided a major thrust to fin-pitch interconnection research. These applications will drive the need for less than 20 micron pitch interconnections in the next few years.

Using lead free solders, 50 micron pitch has been demonstrated recently by IBM. On the other hand, for high end microprocessors, companies such as Intel have announced copper bump technologies combined with solders to address the electro-migration and reliability issues at fine pitch. While there is a general opinion that lead-free solders may not withstand the high stresses and strains at fine pitch, there is no ideal replacement for fine pitch interconnections that can address bonding and assembly at low temperatures and low cost while providing the required reliability. This problem is further complicated because of the difficulty in underfilling at fine pitches for larger die size.

Pad-to-pad bonding (mostly Cu-Cu) holds lot of promise for ultrafine-pitch bonding. However, high melting temperature makes copper to copper bonding highly thermal intensive making it incompatible for 3D silicon or organic packaging. Recently, several works have been done to carry out bonding at 400^0C. However, the bonding duration and annealing time are still higher.

In the present work, copper-copper bonding using advanced nano-conductive and non-conductive adhesives was explored. Nano-Anisotropically Conductive Adhesive, recently developed by Georgia Tech, is a promising candidate for ultrafine-pitch applications. Daisy-chain test vehicles at 30 micron pitch were fabricated using lithography and electroplating processes and matching high-density glass substrates were fabricated using lift-off process. Assembly challenges at ultrafine-pitch were overcome and 30 micron pitch electroplated copper gold protected interconnections were assembled

onto the glass substrates which also had a top protective gold layer. Optimized assemblies were subjected to HAST (130˚C/85%RH) and HTS (175˚C bake for 72 hours) to evaluate their reliability and to determine the failure locations and failure mechanisms. DC resistances of the daisy-chains were measured before stress testing and after regular time intervals during the testing. Insulation resistance of n-ACF in the lateral direction between two adjacent bumps, which was expected to be a concern at ultrafine-pitch, was measure to be of the order of 10^{11} Ohms and the leakage current values were in picoAmps. These values were close to the values for NCF. Hence, it was shown that n-ACF has very high lateral resistance even at such fine pitch.

Very early failures were seen during the HAST with both NCF and n-ACF. Optical inspection showed moisture ingress and retention causing hygroscopic expansion of the epoxy resulting in decreased contact area between bumps and substrate bond pads. SEM pictures revealed pulling apart of the bump and substrate side gold layers due to hygroscopic expansion of the epoxy. It is believed that moisture seeped-in along the adhesive-glass interface. Assemblies with both NCF and n-ACF passed the HTS test. Resistances increased but no failures were observed even after 72 hours of testing.

Earlier works have shown that ACF has very good thermo-mechanical reliability and the dominant failure mechanism is temperature and humidity assisted swelling of the epoxy. Addition of adhesion promoters, low CTE fillers (to reduce CTE mismatch between glass/silicon and adhesive) and moisture scavengers are expected to improve the reliability significantly.

6.2 Future Recommendations

This work evaluated advanced nano-anisotropic conductive adhesives as a candidate material for ultrafine-pitch chip-package interconnection. There is a need to carry out further studies to examine the effects of different parameters on the HAST reliability. Some of the recommendations for future work are as follows.

1) Moisture penetration was believed to be along the glass-adhesive interface as a result of poor adhesion between the two materials. It would be beneficial to add adhesion promoters to the epoxy to see the effect on reliability.
2) CTE mismatch between glass and epoxy is also expected to assist delamination of the adhesive from the glass surface. Incorporation of low CTE fillers to reduce the CTE of the epoxy is expected to help improve reliability.
3) Hermetically encapsulating the whole package is another way to prevent moisture ingress to improve the reliability of the package.

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