DESIGN OF SWITCH-LESS SILICON-GERMANIUM BI-DIRECTIONAL AMPLIFIER FOR LOSS COMPENSATION IN PASSIVE TRANSMIT/RECEIVE MODULES

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DESIGN OF SWICH-LESS SILICON-GERMANIUM BI-DIRECTIONAL AMPLIFIER FOR LOSS COMPENSATION IN PASSIVE TRANSMIT/RECEIVE MODULES

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SUMMARY

This thesis presented an investigation of the design of switch-less bi-directional amplifier (BDA) for loss compensation in passive transmit/receive (T/R) modules, using Silicon-Germanium (SiGe) BiCMOS technology. We have demonstrated an X-band six-bit high-pass (HP)/low-pass (LP) switched-type phase shifter with embedded inter-stage switch-less SiGe BDA cores. The incorporation of single-ended cascode BDA cores in the phase shifter effectively compensated the insertion loss of passive components, while preserving the bi-directionality of the building block. To further explore the potential of SiGe BDAs in passive T/R loss compensation, this thesis investigated differential topology for switch-less SiGe BDA design.

Chapter 1 presents the motivation of this research, focusing on the needs of loss compensation for passive T/R modules. The fundamentals of phased-array, the advantages and disadvantages of passive T/R modules, and the benefits of SiGe HBTs are briefly discussed as well.

Chapter 2 discusses the application of BDA in passive T/R module loss compensation and conventional switchless BDA design. An X-band six-bit HP/ LP switched-type phase shifter design is discussed in detail. This work was presented on *2017 IEEE Radio Frequency Integrated Circuits Symposium* [1].

Y. Gong, M.K. Cho and J.D. Cressler, "A bi-directional, X-band, 6-bit phase shifter for phased array antennas using an active DPDT switch," in *Proc. 2017 IEEE RFIC Symposium,* Honolulu, HI, 2017, pp. 288-291.

Chapter 3 first surveys the concerns and techniques for millimeter-wave circuit design using differential topology with transformers. The latter half of this chapter shows the design, analysis, and characterization of a switch-less differential BDA using anti-parallel cross-coupled common-emitter pairs. The work presented in this chapter has been submitted to *IEEE Microwave and Wireless Components Letters* and is currently under review.

Chapter 4 provides concluding remarks and discusses some ideas for potential future work.

CHAPTER 1. INTRODUCTION

1.1 Motivation

Phased-arrays are a technique that is well understood and frequently deployed in Radar and commutation applications by scientists and engineers for many decades. With 5th generation (5G) standards expected to be rolled out in 2020, interests in efficient phased-array systems for mobile communication applications are ramping up again in industry and academia. Phased-arrays consist of arrays of radiating elements that leverage constructive and destructive interferences of electro-magnetic waves in free space to enable beam forming and steering [2]. In mobile communication applications, phased-arrays are essential achieve high data rate and reliable link in modern communication systems.

Figure 1 shows a typical block diagram of a phased-array antenna. Although, depending specific applications and system requirements, phased-array system designs vary, they all contain three basic sub-blocks. The array of antenna elements are responsible for radiating and receiving signal to and from free space. The power divider/ combiner building block that distributes and combine power to and from the array. Front-end transmit/receive (T/R) modules are what enables beam steering for phased-arrays as they are responsible for providing phase and amplitude control of signal transmitted and received from each channel. There are many variations of T/R module architecture tailored for specific needs of different applications. Though different, they share similar features. A block diagram of a typical T/R module is shown in Figure 2. The front-end low noise

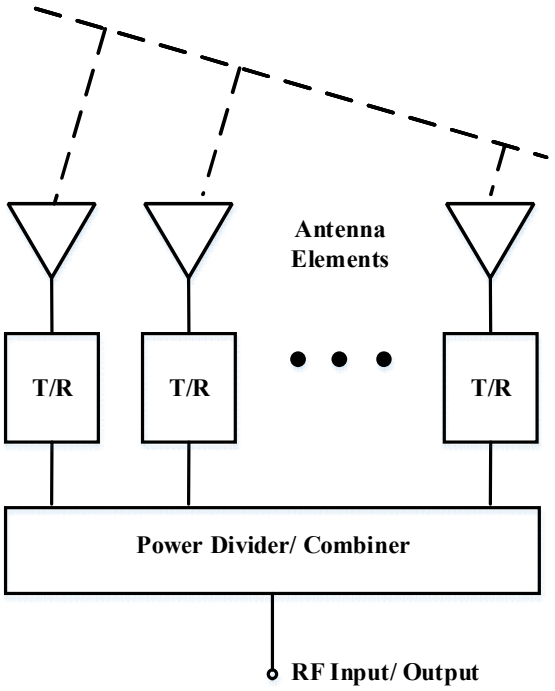

Figure 1: A typical block diagram of a phased-array antenna.

amplifier (LNA) is usually included to amplifier the received signal and suppress signal to noise ratio (SNR). Power amplifiers (PA) are placed close to the antenna elements to boost transmitted power to the required level. The attenuator and the phase shifter provide a certain degree of control on the amplitude and phase of the received and transmitted signal, a control that is essential to beam forming.

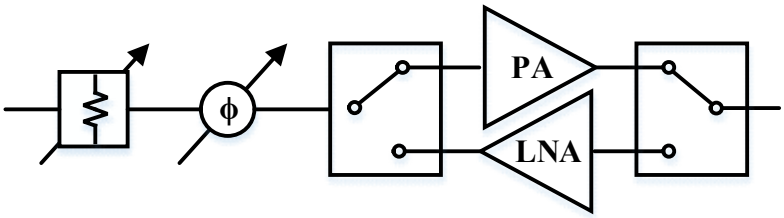

Figure 2: A typical block diagram of a T/R module.

T/R modules design for phased-array antennas is a highly complex subject. A typical T/R module consists of many sub-blocks, each of which requires detailed discussions for a comprehensive understanding of the block. This thesis by no means aims to discuss on every detail of each component. Instead, this thesis attempts to address one of the issues for one of the many potential T/R module architectures. The goal of this thesis is to investigate the use of switch-less SiGe bi-directional amplifier for loss compensation in T/R modules with passive attenuator and phase shifters.

1.2 T/R Modules

Signal amplitude and phase control are important functions of T/R modules. Depending on system level requirements, the approach to amplitude and phase control can be implemented in several different ways.

1.2.1 Signal Amplitude Control

Signal amplitude control in phased-array is important as it allows adjustable beam width and sidelobe level of the radiation pattern of the array. It also provides compensation for the gain variation of the phase shifter under different phase states. Intuitively, signal amplitude control can be achieved through introducing controllable gain or loss on the signal path. This intuition naturally leads to two popular approach: variable gain amplifiers (VGAs) and programable attenuators. A typical VGA approach bases on the bias-dependent characteristic of the transistor's transconductance to vary the gain of the amplifier. K. Hettak and G.A. Morin demonstrated a typical VGA design in [3] which achieves adjustable gain to the amplifier though changing the bias of the *gm* transistor, while keeping the rest of the bias levels constant. The simplified VGA schematic of their

design is shown in Figure 3 (after [3]). Programmable attenuators utilize passive networks with embedded CMOS switches. As an example, Figure 4 shows the schematic of a 6-bit digital attenuator designed by J. Zhao *et al.* [4]. Attenuation control is achieved by toggling the series and shunt CMOS switches and changing the effective passive network of each attenuation bit.

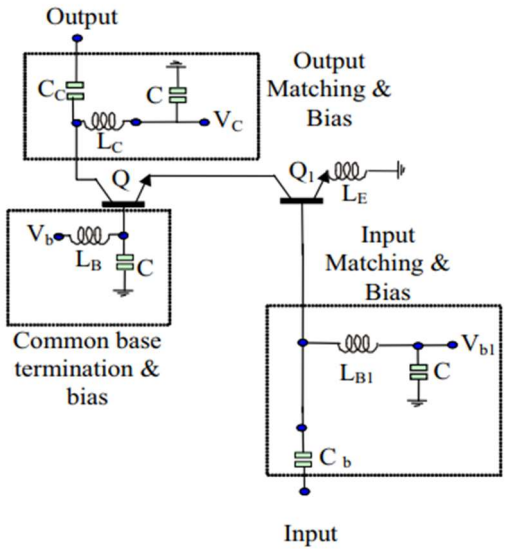

Figure 3: Simplified schematic of a typical VGA design (after [3]).

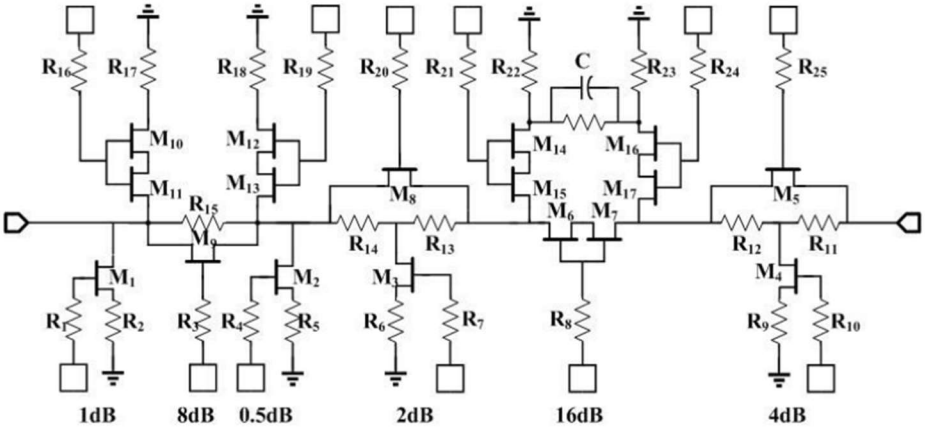

Figure 4: Schematic of a 6-bit digital attenuator by J. Zhao *et al.* (after [4]).

Apart for the two approaches discussed above, researchers also proposed to remove the need for a dedicated VGA or attenuator, but instead integrate the gain control functionality into the front-end LNA. Y. Wu *et al.* demonstrated a four-channel 60-GHz antenna phased-array receiver by using variable-gain LNA and phase shifter [5]. However, doing so enable signal amplitude control on the receiver only but not the transmit signal path. Therefore, this approach will not be discussed here.

1.2.2 Phase Shifters

Signal phase control is normally achieved by dedicated building blocks called phase shifters, also known as phase rotators. Digital phase shifters are gaining more popularity in recent years as compared to analog phase shifters due to their tolerance in control signal noise and temperature variation. There have been many well-established methods to introduce phase shift to signal. Well-designed vector-sum based active phase shifter can achieve low phase error and provide decent signal amplification [6], [7]. Although implementation strategies vary from design to design, the basic operating principle of vector-sum based phase shifter relies on the weighted sum of the orthogonal in-phase and quadrature (I/Q) copies of the input signal to create a phase-shifted copy of the signal at the output. The basic operating principle is illustrated in Figure 5, where the I/Q generator creates a pair of 90-degree out of phase copy of the input signal and the two VGAs control the weight of the I and Q signals. This phase shifter is also called a phase interpolator since an interpolation is performed between the in-phase and 90-degree components. This phase shifter topology is sometimes also referred to as a polar modulator or a cartesian combiner [8].

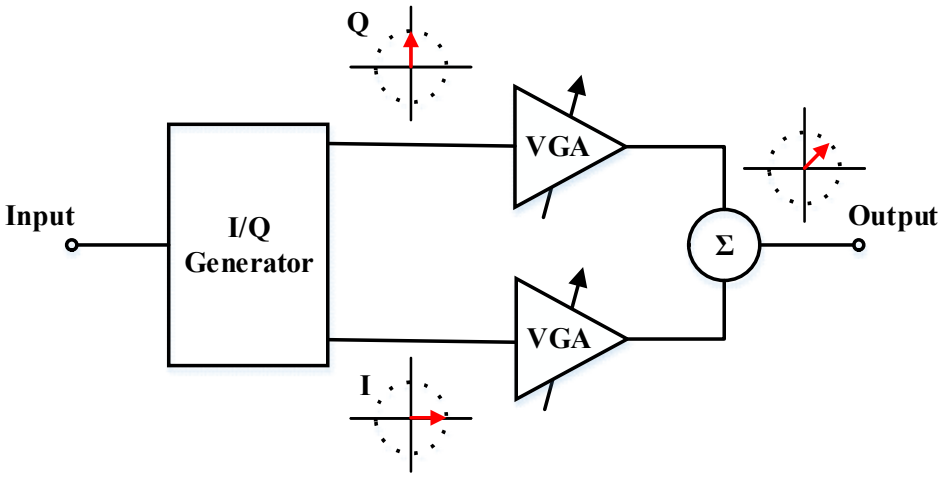

Figure 5: A simplified block diagram of vector-sum based phase shifter.

Another main category of phase shifters is passive phase shifters. There are many architectures for passive phase shifters such as switched-line, loaded lines, switched high-pass/ low-pass (HP/ LP), and reflective-type. One important thing in common among all these types of passive phase shifter is that they introduce phase shift to the signal through reconfiguring or tuning the passive network on the signal path. The basic principle of switched-line type phase shifter relies two single-pole double-throw (SPDT) switches to select between the reference and delay path transmission lines of different electrical length, and thus obtain the required phase difference (shown in Figure 6). Arguably, the simplicity of this architecture is one of the main reason for its popularity across applications and technology platforms: Y.Du *et al.* demonstrated an X-band switched-line phase shifter on PCB using RF MEMS multi-throw switches in [9], and M. T. Gul *et al.* designed a 60 GHz switched-line phase shifter using 130-nm CMOS technology [10]. However, despite of its simplicity, the switched-line architecture is not often used by engineers in millimeter-wave on-chip phase shifter design for two main reasons: transmission lines usually takes up a lot

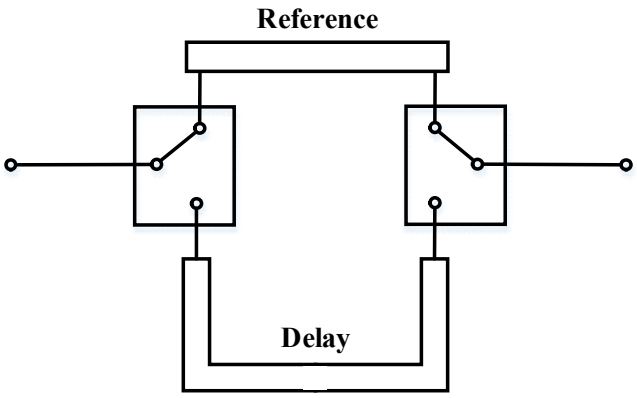

Figure 6: Operation principle of switched-line phase shifter.

of chip area, and extra attention needs to be paid to compensate the loss difference between the two transmission lines. Instead of using transmission lines with different electrical lengths, switched HP/ LP phase shifters switch signal between phase-leading high-pass filter and phase-lagging low pass filter of same loss to achieve phase shift. Comparing to switched-line phase shifters, switched HP/ LP phase shifters tend to lead to less amplitude variation between the phase states, and they potentially occupy less chip area due to the use of discrete inductors and capacitors in the filter synthesis. More detailed discussion on switched HP/ LP phase shifters will be presented in Chapter 2. Reflective-type phase shifter is another type of notable passive phase shifter. A conventional reflective-type phase shifter consists of a 90-degree coupler and two tunable reflective loads, normally implemented using C-L-C pi-network (as shown in Figure 7). The conventional single-ended reflective-type phase shifter have limited phase shifting range normally below 180 degrees. To achieve 360-degree phase shifting range, two such phase shifters could be cascaded. Alternatively, T. W. Li and H. Wang demonstrated a fully differential reflective-type phase shifter using transformer-based coupler and reflective loads in [11], that achieves a full

360-degree phase shifting range. Loaded-line phase shifter achieves phase shift by switching the loads at the ends of a transmission line section. However, to save chip area, the transmission line in the conventional loaded-line architecture is normally replaced by discrete component synthesized artificial transmission line, and the resulting circuit is a cascade of varactor loaded C-L-C pi-networks. The phase delay of the artificial transmission line changes as the varactor capacitance changes. At the same time, however, the characteristic impedance of the artificial transmission line changes too. Therefore, the useful phase shifting range of the loaded-line architecture is limited by the quality factor and tuning range of the varactor, as well as the acceptable return loss. To alleviate this problem, S. Shamsadini *et al.* proposed a loaded-line phase shifter with transformer-based tunable inductor [12].

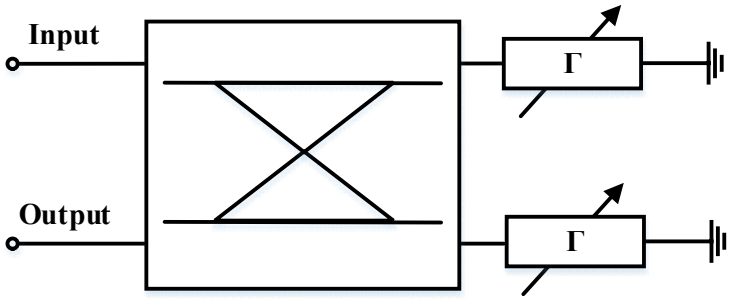

Figure 7: Conventional single-ended reflective-type phase shifter.

1.2.3 Active and Passive T/R Modules

Most of the T/R modules used in modern phased-array antennas contain front-end LNAs and PAs that are undoubtedly active circuit components. However, the architecture for signal amplitude and phase control can be active, passive, or a hybrid of the two. For

simplicity, the author will loosely (and inaccurately) refer to T/R modules as only the amplitude and phase control building blocks, excluding the front-end LNA and PA (as in Figure 1). T/R modules with passive attenuators and passive phase shifters are referred to as passive T/R modules, and T/R modules with any other combinations are referred to as active phase shifter.

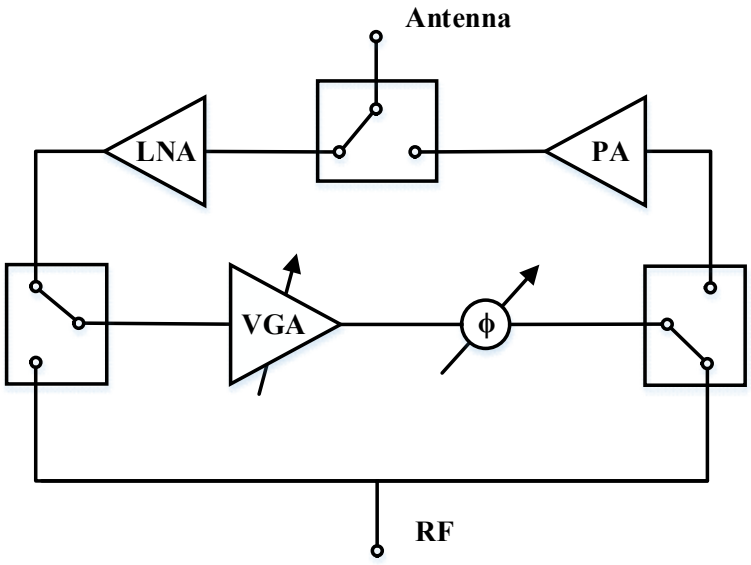

Figure 8: T/R module with VGA and phase shifter on the common-leg.

In term of amplitude and phase tuning range and accuracy, there is no clear winner between active and passive T/R modules. Since active T/R modules contain VGAs along the signal path, they face all the design trade-offs amplifiers normally face such as: bandwidth, gain, linearity and power consumption. On the other hand, passive T/R modules does not consume any DC power and can potentially have wider bandwidth (especially in the VGA vs. passive attenuator case), but passive T/R modules presents significant loss on the system level. Another main difference between active and passive phase shifters is that active phase shifters only allow uni-directional operation because of the presence of uni-

directional amplifiers. However, a T/R module need to provide amplitude and phase control to both receiving and transmitting signals, and therefore the system configuration shown in Figure 1 cannot be used in this case. To solve the problem created by the uni-directionality of active T/R modules, the common-leg configuration, shown in Figure 8, is usually adopted. The resulting additional SPDT switch and signal routing increases T/R module loss and system integration complexity. Other than the common-leg configuration, another commonly used solution is to dedicate separate amplitude and phase control units for both the receiving and transmitting paths as demonstrated by K. Kibaroglu *et al.* in [13].

From a system integration perspective, passive T/R modules that support bi-directional operation are more advantageous. However, the high insertion loss from the passive structures must be dealt with

1.3 SiGe BiCMOS Technology

The development history of silicon-germanium technology can be dated back to 1940s when William Shockley proposed the idea of using silicon-germanium alloy in BJT design to create superior semiconductor devices [14]. The SiGe HBT was first demonstrated in 1987 and manufacturing was first available in 1992 [15].

Both silicon (Si) and germanium (Ge) have the same lattice structure with Ge having a lattice constant 4.18% larger than that of Si. Because of this difference in lattice constant, Ge has a smaller bandgap (0.66 eV) than that of Si (1.12 eV). For every 10% of Ge introduced to Si lattice, the associated compressive strain results in an approximately 75 meV of decrease in bandgap [16]. By depositing Ge into the base of a transistor, an effective band offset could be observed pronominally in the balance band. Therefore, by

carefully optimizing the Ge profile across the base of the transistor, a bipolar transistor with enhanced performance could be engineered. The amount of Ge content introduced to the transistor base typically increases across the width of the base as shown in Figure 9, and this results in a gradual reduction of bandgap across the base. As a result, the HBT has higher current gain and early voltage.

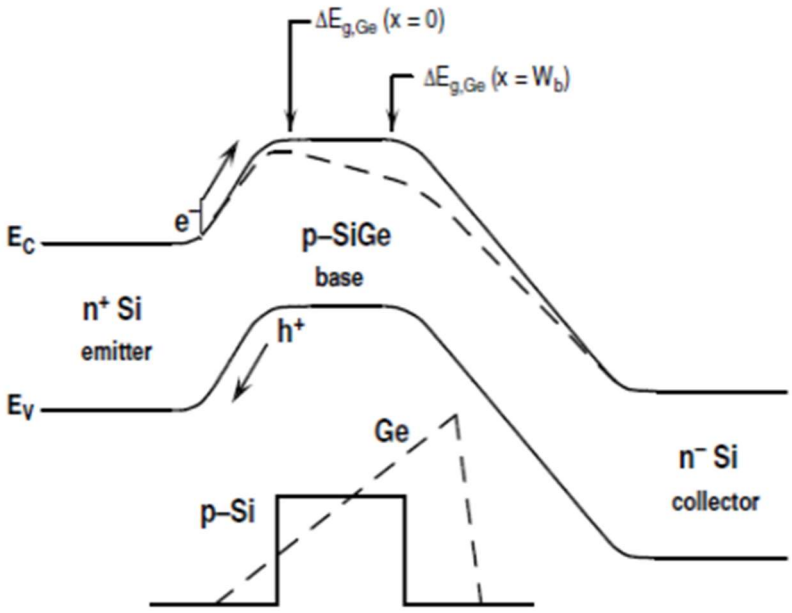

Figure 9: Graded-base SiGe HBT and resultant energy band diagram (after [16]).

The two main figures of merit used to benchmark high frequency performance of transistors are the unity gain cut-off frequency (f_T), which is the frequency when short circuit current gain becomes unity, and the maximum oscillation frequency (f_{MAX}), the frequency when power gain of the transistor under matched condition equals to one. Thanks to bandgap engineering, SiGe HBTs shows far more superior f_T and f_{MAX} than CMOS devices at similar technology node. Figure 10 shows the advance of SiGe HBT f_T

and f_{MAX} over generations [17]. The III-V like performance and CMOS process fabrication compatibility make SiGe a very attractive technology for highly integrated RF circuits and systems design.

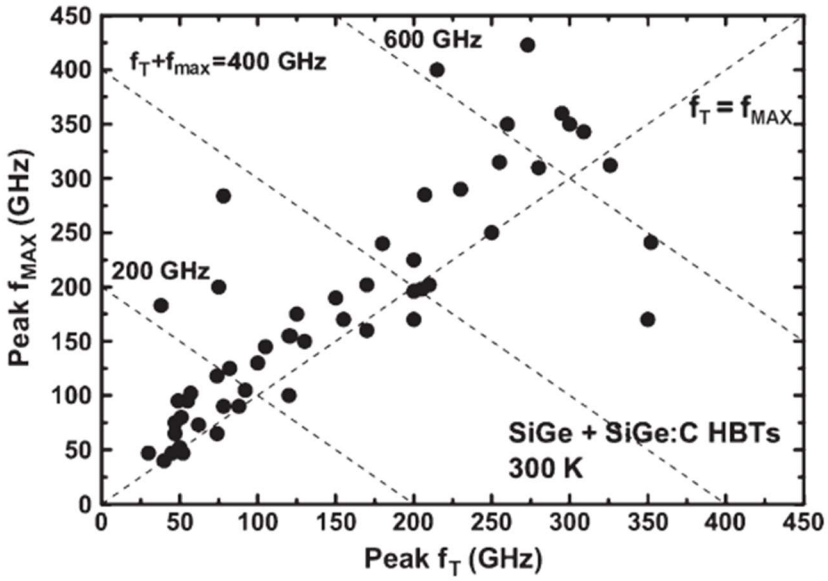

Figure 10: Measured f_{MAX} versus f_T of various SiGe and SiGe:C HBTs.

Even though advanced CMOS technology can achieve above 300 GHz f_T and f_{MAX}, the aggressive lateral scaling of lithography creates many other design challenges and concerns. As a direct result of scaling, the physical terminals of CMOS devices are closer together, and this lead to a more serious parasitic effect due to interconnections. R. L. Schmid *et al.* showed in [18] that the RF performance degradation worsens as technology node scale down. Moreover, due to the close proximity of drain and source nodes in advanced CMOS technology, the resultant significant drain-source capacitance leads to an additional stability concern to implementation of the popular cascode topology pointed out by S. V. Thyagarajan in [19]. On the other hand, the performance of SiGe HBTs relies

more on the vertical scaling and bandgap engineering. The current commercially available SiGe HBTs can reach an f_T and f_{MAX} above 300 GHz with moderate lateral scaling. In other words, technology scaling presents for potential enhancement to SiGe HBTs than potential penalties. This makes SiGe HBT technology an ideal choice for high performance mm-wave circuit and system design.

CHAPTER 2. APPLICATION OF BDA IN PASSIVE T/R MODULE LOSS COMPENSATION

As discussed in Chapter 1.2, the high linearity, zero DC power consumption and bi-directionality of passive T/R modules present great advantages in terms of system robustness, power efficiency and system simplicity. However, pure passive component based T/R modules suffer high passive lost. This chapter will briefly survey the existing solutions to for loss compensation in passive T/R modules. An X-band 6-bit phase shifter with active DPDT switches will be discussed in detail to examine the benefits and disadvantages of using single-ended BDAs for loss compensation in passive T/R modules.

2.1 Loss Optimization

The first and most apparent step to alleviate the high passive loss is to optimize the passive structure to achieve the intended performance with minimal loss.

2.1.1 Choice of Technology

One of the main loss mechanism in bulk silicon process is due to RF signal coupling thought he low-resistivity silicon substrate. Signal coupling through substrate not only introduces loss but also results in poor linearity to circuits design such as switches. Though design techniques might help to alleviate this problem, loss through silicon substrate is a process technology related fundamental issue that cannot be completely mitigated. Historically, to achieve high-performance circuit component, particularly high linearity, low loss, and high isolation RF switches, III-V process or silicon-on-sapphire technologies [20] are employed. Although these technologies deliver transistors with superior

performance as compared to most of processes on bulk silicon, their expensive substrate and low integration capability make them less favourable in high-integration and low-cost system design.

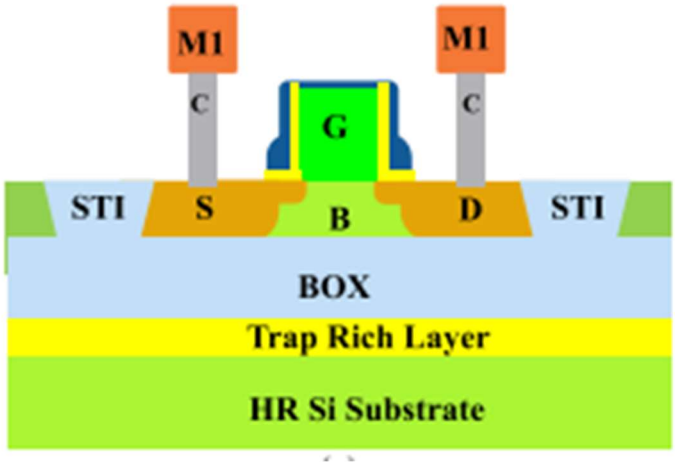

Figure 11: Schematic of an SOI NMOS with a trap-rich layer.

In recent years, high-resistivity silicon-on-insulator (HR SOI) technology has been gaining popularity in high-performance RF circuit design due to its reduced parasitic capacitance and substrate loss [21]. However, the fixed charges within the oxide of HR SOI technology attract free carries near the Si/SiO_2 interface, and these fixed charges results in parasitic surface conduction. To solve this problem, researchers have proposed and demonstrated introduction of a trap-rich layer between the buried oxide layer and HR Si substrate, as shown in Figure 11, to capture the free carriers near the Si/SiO_2 interface [22], [23].

However, despite the plethora of high-performance technology platforms that feature low loss substrate, the freedom to choose which ever technology best suited for

each building block is often a luxury to engineers because of the integration and cost concerns.

2.1.2 Design Techniques

Other than choosing the best suited technology, many design techniques and alternative circuit topologies from conventional approach have been devised to lower the loss of passive designs.

Body-floating technique with triple-well process were reported in [24] and [25] to enhance linearity and reduce loss of the MOS switch design. These techniques address the high passive loss issue by reducing the RF signal loss to substrate.

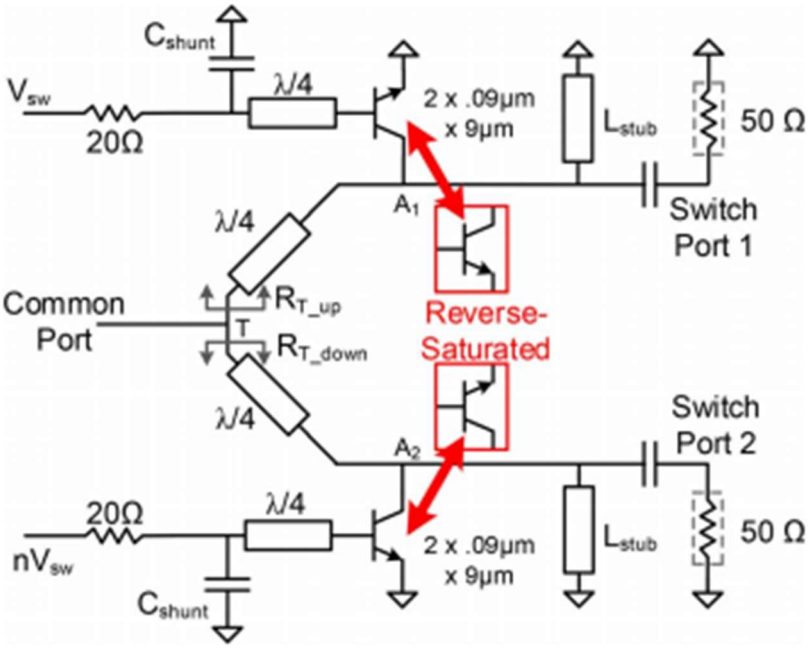

Figure 12: Using reverse-saturated HBTs instead of saturated HBTs in quarter-wave shunt switches (after [26]).

One significant loss contributor in passive T/R modules is the switch. R. L. Schmid *et al.* proposed in [26] the use of reverse-saturated SiGe HBTs in place of the conventional saturated HBTs in quarter-wave shunt switch topology, as shown in Figure 12. By using the emitter at the RF output node, the proposed topology takes advantage of the higher emitter doping and improves isolation from the bulk substrate and hence reduces loss of the switch.

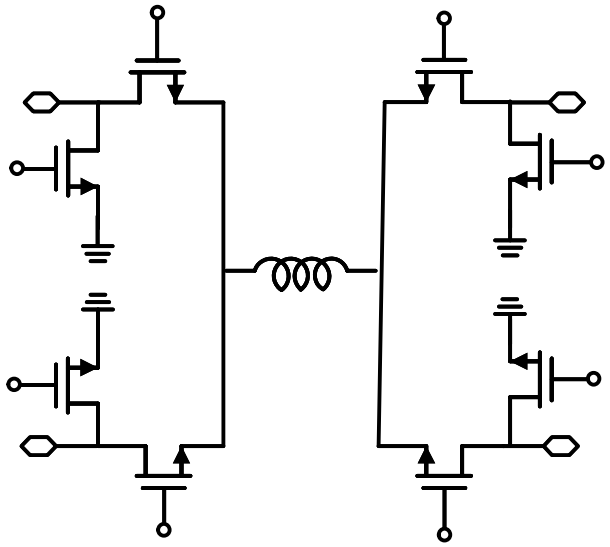

Figure 13: Simplified schematic of conventional DPDT design.

At lower frequencies, the conventional series-shunt FET switches are often used, and the ON resistance is one of the major loss contributor in passive T/R modules. One natural strategy to reduce loss is to reduce the number series transistors on the RF signal path. The conventional double-pole double-throw (DPDT) switch consists of two head-to-head single-pole double-throw (SPDT) switches with inter-stage matching as shown in Figure 13. Regardless of which two ports are selected as through, there are always two series FET on the signal path. M.-K. Cho *et al.* presented a passive DPDT design in place

of the conventional back-to-back SPDT topology to optimize the loss of passive DPDT by reducing the number of series transistors on the signal path [27], as shown in Figure 14. This topology ensures only one ON transistor on the signal path.

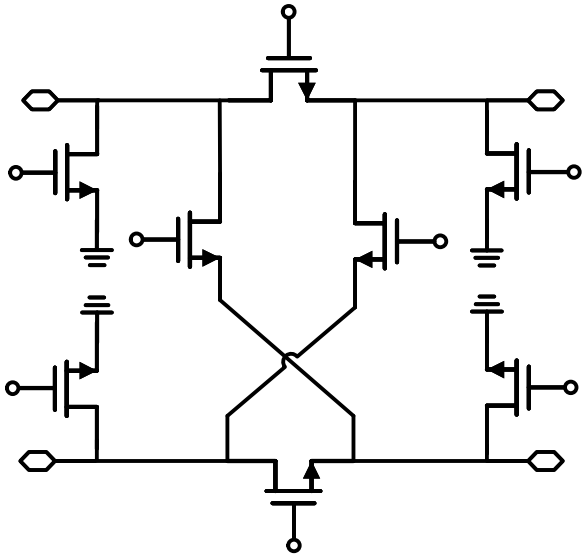

Figure 14: Simplified schematic of DPDT switch proposed by M.-K. Cho *et al.*

2.2 Compensation with High Performance Front-End LNA and PA

Despite of the effectiveness of loss reduction techniques discussed above, the high loss problem of passive T/R modules persists. The purpose of optimization is to alleviate the issue, maybe to a point when the loss of the resultant T/R modules can be tolerated at the system level. On the other hand, although passive T/R modules are known for their high passive loss, it does not necessarily mean the loss is the limiting factor at the system level. U. Kodak and G. M. Rebeiz demonstrated a 28 GHz bi-directional phased-array with passive T/R modules in [28]. As shown in Figure 15 (after [28]), the 4-bit attenuator and 6-bit passive shifter together show a passive loss of 12 dB. High-performance PA and LNA, implemented in GaAs technology on a separate die, are used to compensate such

high loss. In this case, the system is limited by the linearity of the passive T/R module instead of its loss.

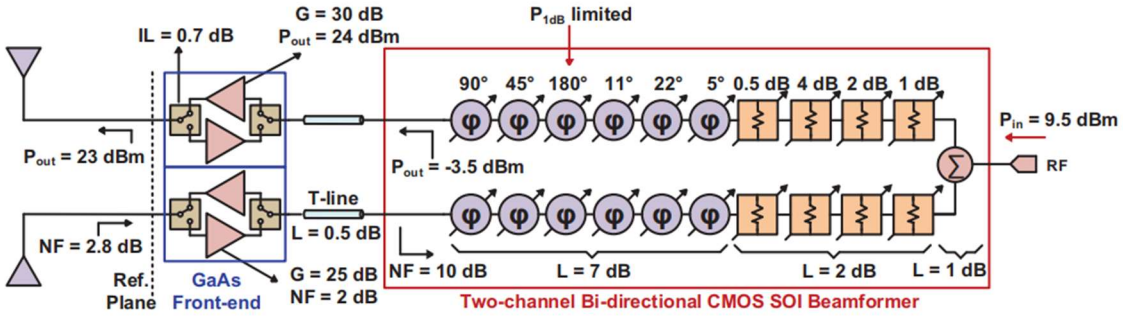

Figure 15: Passive T/R module with GaAs front-end PA and LNA (after [28]).

Note that this approach completely moves the loss compensation burden to the front-end PA and LNA. The PA needs high gain and efficiency to guarantee enough power delivered to the antenna at limited input drive power, and the LNA need enough gain and low noise figure to suppress the SNR degradation caused by the high loss of the passive beam-forming elements. The stringent requirement on the performance of PA and LNA make the single-chip integrated design challenging. While the beam forming elements in the design by U. Kodak and G. M. Rebeiz are realized using 45 nm CMOS SOI technology, the front-end PA, LNA and switches are designed using III-V technology, as shown in Figure 15, for its superior power handling capability, better LNA noise figure and lower switch loss.

2.3 Loss Compensation Using Bi-Directional Amplifiers

For base station applications that requires large transmit power per elements to achieve high EIRP, the use of high performance III-V technology together with CMOS

chipsets is justifiable as most CMOS and SiGe designs can only transmit relatively low power. However, for end-user applications, highly integrated and low-cost system on chip solutions are favored. In this case, the high loss of passive T/R modules are more likely to be the limiting factor in the system and loss compensation is more desired with-in the system other than relying solely on the front-end LNAs and PAs.

C. Liu *et al.* proposed a loss-compensated 5-bit X-band phase shifter with wideband distributed inter-stage amplifier for loss compensation [29]. The block diagram of the compensated phase shifter is shown in Figure 16. Although this approach effectively compensates for the loss of the passive components in the T/R modules, the use of uni-directional loss compensation amplifiers (LCAs) forsake the bi-directionality of the passive T/R modules and hence a common-leg approach like that shown in Figure 8 is adopted in this scenario. The author would argue that a better loss compensation approach is to use bi-directional amplifiers in the system to compensate the passive loss while still reserve the bi-directionality of the building block.

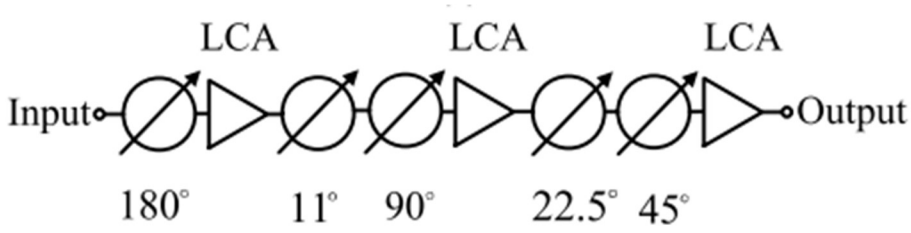

Figure 16: Block diagram of the compensated X-band 5-bit phase shifter by C. Liu *et al.* (after [29]).

In fact, the use of BDAs for loss compensation in T/R modules have been practiced by many engineers over decades. Several topologies of the BDAs have been reported in

the literature. J. M. Yang *et al.* presented a switchless BDA using common-source topology in [30], as shown in Figure 17, and J. W. Archer used common-gate topology in [31]. Both designs use multi-stage single-ended amplifier core and their direction of operation are directly controlled via DC biases on the forward and backward branches. Due the symmetricity of the topology, the two input and output matching networks (M.N.) are usually identical.

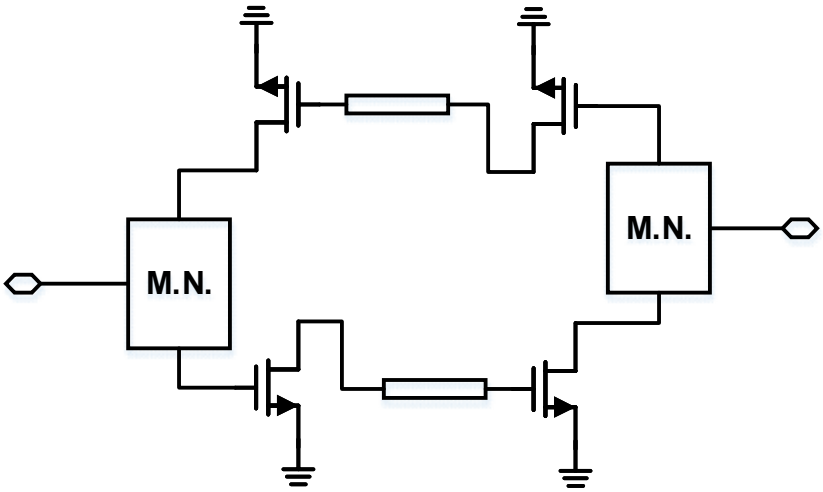

Figure 17: Simplified common-source BDA schematic.

Since the matching networks need to match the input impedance and output impedance of the active amplifier branch, the network design can be challenging and is usually narrow-band. To solve this problem, the distributed technique can be adopted to realize broadband distributed BDA. However, since gain of the stages of distributed amplifier add instead of multiply, the distributed BDAs display low gain and low efficiency. S. -H. Weng *et al.* proposed a BDA using a g_m-bandwidth extension technique to enhance the gain of BDA in [32]. Another problem with distributed topology is that the circuit

component normally takes up a lot of chip area for artificial transmission line synthesis. To achieve a compact design, S. Sim *et al.* used a single-stage BDA in [33] to compensate the loss from the passive components in the passive T/R module. A simplified schematic of the single-stage BDA is illustrated in Figure 18. Strictly speaking, even though the design follows the distributed amplifier technique, since the amplifier only has one stage, this circuit topology cannot be referred to as a distributed amplifier. Rather, this topology is a single stage BDA with resistive input and output matching network. The use of resistive matching network trade the gain of the amplifier with wider and easier input and output matching. It is fair to say that one of the main reasons the author of [33] could achieve near identical performance for forward and backward operation is because of the resistive termination that greatly lowered the Q factor of the input and output matching networks The BDA core consists of a single-ended anti-parallel cascode stage for both forward and backward operations. The direction of operation is determined through the gate DC bias on the common-gate transistor. The voltage supply is fed through RF choking inductors.

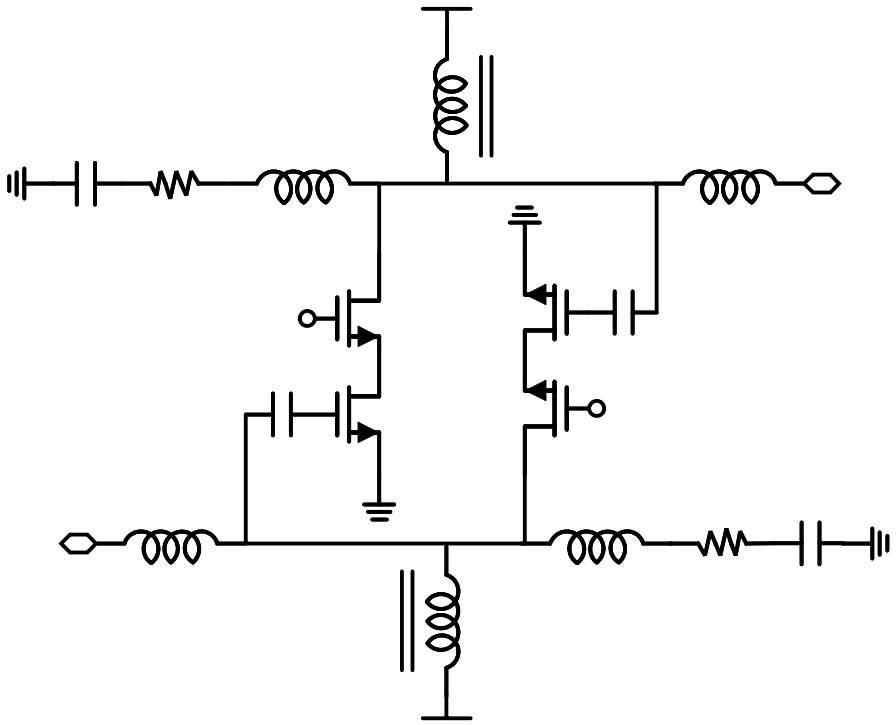

Figure 18: Simplified schematic of single-stage distributed BDA.

The designs in [30]- [32] are implemented in III-V platform that enables each stage to have high gain. The design demonstrated in [33] is implemented using a 130 nm CMOS technology. Even though the author did not specifically mention the rationale behind the choice of amplifier core topology, it is reasonable to assume that cascode topology is chosen in [33] because it provides high single-stage gain and good reverse isolation for stability. In fact, cascode topology is a very popular choice to implement BDAs. Besides it high gain and good isolation, additional current steering transistors parallel to the cascode transistor can be conveniently incorporated in the design to give the BDA a variable gain, as demonstrated by S. Afroz and K. -J. Koh in their design of a 94 GHz bi-directional variable gain amplifier [34].

2.4 A Bi-Directional X-Band 6-Bit Phase Shifter Using Active DPDT Switches

As discussed in the previous sections, to mitigate the high loss in passive T/R modules, techniques can be applied to minimize the passive loss from switches, and BDAs can be incorporated in the RF signal path for compensation. In practice, these two approaches are usually used in conjuncture. In this section, a bi-directional X-band 6-bit phase shifter will be described in detail as an example to demonstrate the loss mitigation in passive T/R modules. Part of the content in this section is taken from the publication by the author in [1].

2.4.1 Circuit Overview

Switched HP/ LP topology is chosen for the phase shifter design presented in [1]. The block diagram of the phase shifter is shown in Figure 19 (after [1]). Two passive series-shunt SPDT switches are used in the phase shifter at the two ends of the phase shifter. Optimal transistor sizing, resistive body-floating, and biased triple-well are employed to minimize insertion loss and improve isolation. The insertion loss of the two SPDT switches and passive networks are compensated using four active DPDT switches, which will be discussed in detail in the following subsection. Three additional tuning bits are included in the design to enhance the phase shifting performance of the design. The four active switches draw 65 mA of DC current from a 3 V supply.

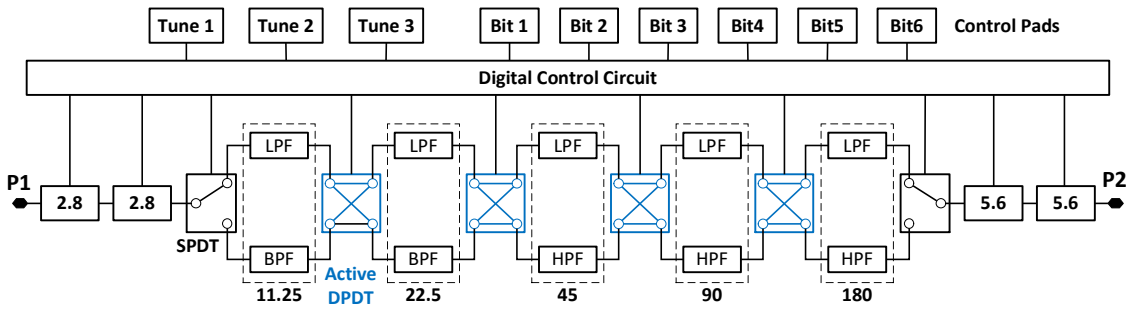

Figure 19: Block diagram of presented switched HP/ LP 6-bit phase shifter using active DPDT switches (after [1]).

2.4.2 Active Bi-Directional DPDT Switch

Building on the single-stage BDA presented by S. Sim *et al.* in [33], M. -K. Cho *et al.* proposed an active DPDT switch in [35] that uses a similar BDA design topology with an addition of four series-shunt switches on to achieve bi-directional four-way signal switching. The schematic of the proposed bi-directional DPDT is shown in Figure 20. The core of the active DPDT switch consists of a single-stage bi-directional amplifier, consisting of a pair of anti-parallel cascode amplifiers. The core topology is similar to the BDA core proposed in [33] and matching networks are also implemented with resistive input and output termination resistor R_T. The direction of operation is determined by selectively biasing the forward (Q_1 and Q_2) or backward (Q_3 and Q_4) cascode gain stage. Different from the MOSFET BDA design in [33] that have termination resistors fixed at the two ends of the input and output artificial transmission line, the active DPDT uses four series-shunt SPST switches to choose the terminals that need to be terminated. Port selection is also achieved by the four SPDT switches.

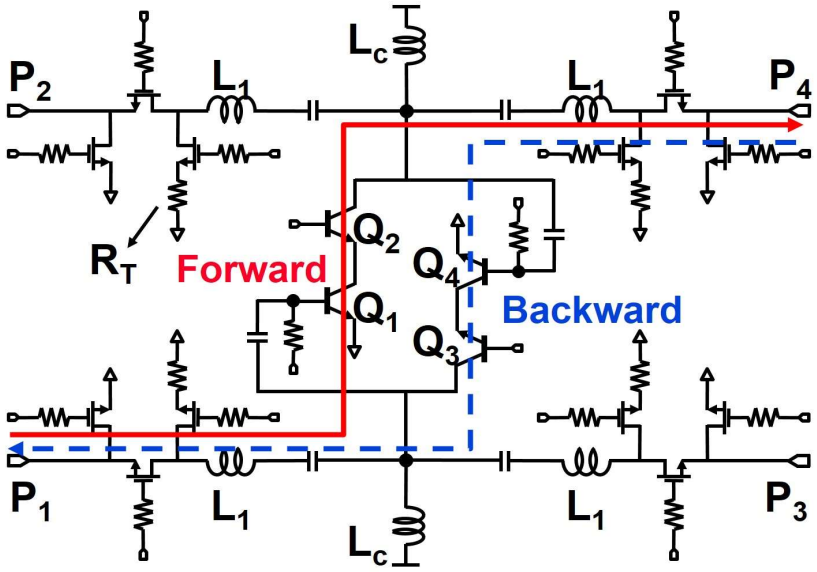

Figure 20: Schematics of active bi-directional DPDT switch (after [1]).

The effective circuit for P1 to P4 signal flow configuration is illustrated in Figure 21. To choose the forward operation, bias is applied to the base of transistor Q_2 and therefore turning on the forward cascode amplifier Q_1 and Q_2. At the same time, the base of transistor Q_3 is grounded and thus render the backward amplifier Q_3 and Q_4 inactive. Only one of the anti-parallel amplifier branch is turned on at a time to ensure the stability of the circuit. Since P1 and P4 are configured as the through ports, the series FET transistors in the switches at P1 and P4 are turn on. The switches at P2 and P3 are switched to the terminating resistors. Additional shunt transistors at the four ports are added to increase port to port isolation. In addition to the use of BDA in the switch for loss compensation, body-floating and triple-well techniques are also employed in the design of the four SPDT switches for loss reduction and linearity enhancement.

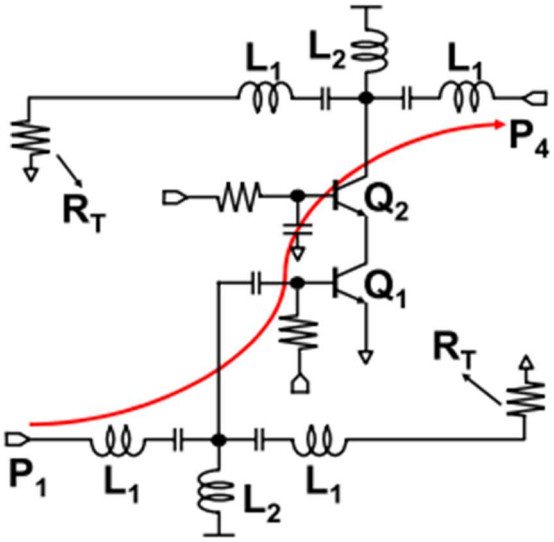

Figure 21: Effective circuit when signal configured to flow from P1 to P4 (after [35]).

2.4.3 Phase Shifting Elements

A switched HP/ LP topology is used for this phase shifter. To save chip area, band-pass filters are also used for lower phase shifting bits. The 11.25º, 22.5º, 45º, 90º and 180º bits are implemented with LPF and HPF/ BPF networks, as shown in Figure 22. The inductances and capacitances are chosen following the methodology described by Q. Xiao in [36] to achieve flat phase response and low amplitude error across the bandwidth. The 5.6º least significant bit (LSB) and the additional three tuning bits (two 2.8º bits and one 5.6º bit) are designed together with the SPDT switches using the topology shown in Figure 23 instead of filter networks to save chip area and reduce circuit complexity. By turning the one or both the shunt transistors on and off, a small phase difference is introduced. Because of the topology, the 2.8º bits and 5.6º bits show monotonically increasing phase shift with increasing frequency instead of a flat phase response across the bandwidth.

However, such undesired phase response is negligible when compared to phase errors from the other major states, and therefore the design tradeoff is justified.

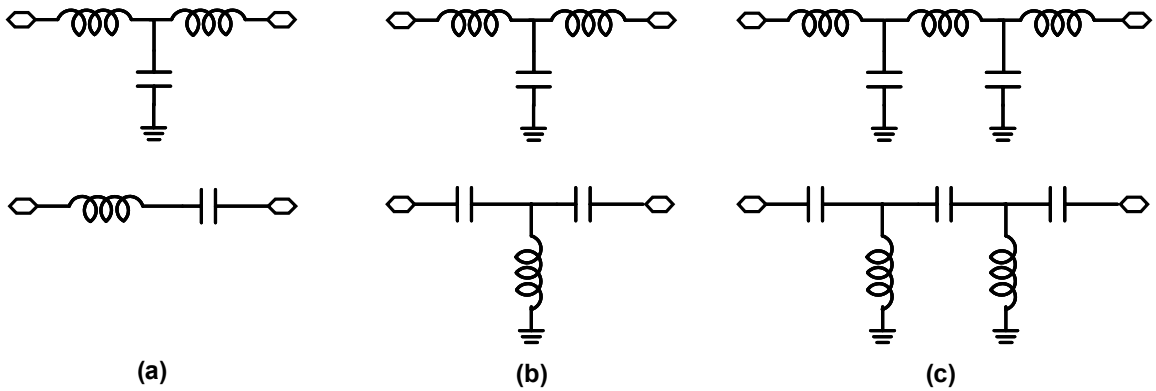

Figure 22: Filter networks used for (a) 11.25º and 22.5º bits, (b) 45º and 90º bits, and (c) 180º bit.

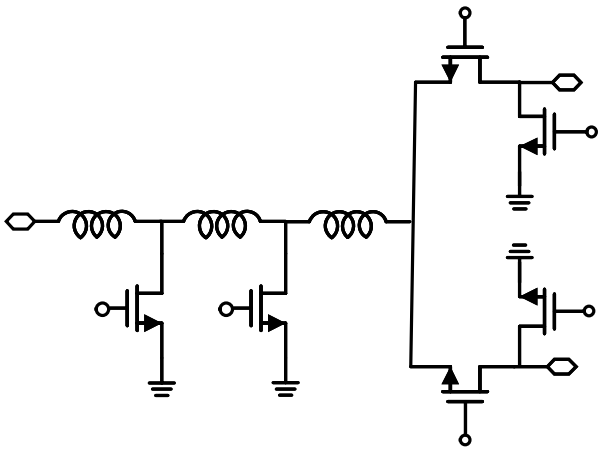

Figure 23: LSB and tuning bit design with SPDT switch.

2.4.4 Measurement Results and Discussions

The X-band 6-bit phase shifter is implemented in a 130 nm SiGe BiCMOS technology, featuring f_T/f_{MAX} of 200/280 GHz (GlobalFoundries 8HP technology). A

microphotograph of the fabricated phase shifter is shown in Figure 24. The four active DPDT switches are placed closely next to each other and the high-pass and low-pass filter are placed between the DPDT switches. The circuit has dimensions of 2.6 × 1.5 mm^2, including pads. The phase states are controlled using an on-chip switch control circuitry implemented using simple logic gates. A standard 2-port SOLT calibration was performed for on-die s-parameter characterization. The bi-directional operation is verified by measuring and comparing the s-parameters under left-to-right and right-to-left bias conditions. Figure 25 shows that the input and output matching, and gain of the reference states of operation. Results are reasonably matched for both directions

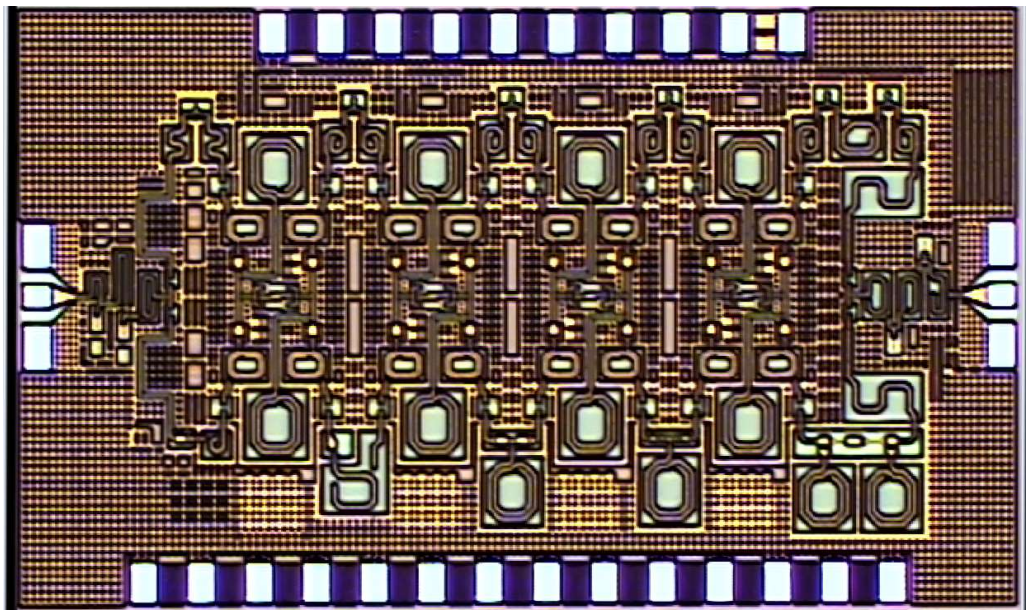

Figure 24: Microphotograph of the X-band 6-bit phase shifter (after [1]).

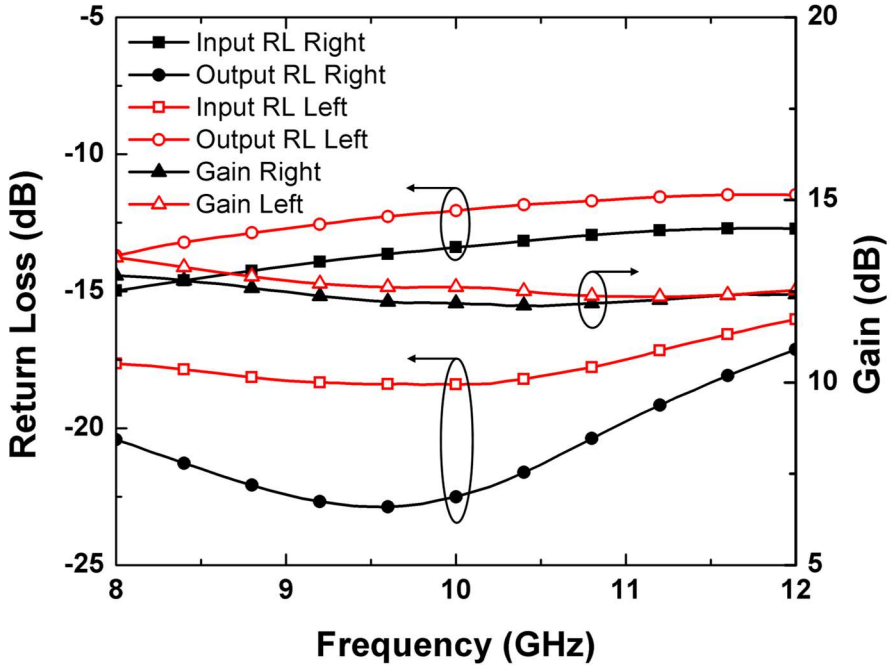

Figure 25: Input and output return loss and gain of the reference state in the forward and backward operations (after [1]).

Although all states under both the forward and backward operations are measured, only data from the major states of the forward operation are plotted to obtain a clear and less confusing plots. The input and output matching and gain are plotted in Figure 26. The input and output return loss are greater than 10 dB for all the 6 major states, and the gain under all 6 major states is greater than 11. 5 dB across the desired frequency band (8 – 12 GHz). An undesired gap is observed between the gain plots of the 6 major states. This is likely caused by imperfect loss matching between the HPF and LPF design. However, despite of the existence of this amplitude error, the RMS amplitude error is still less than 0.9 dB, as shown in Figure 28.

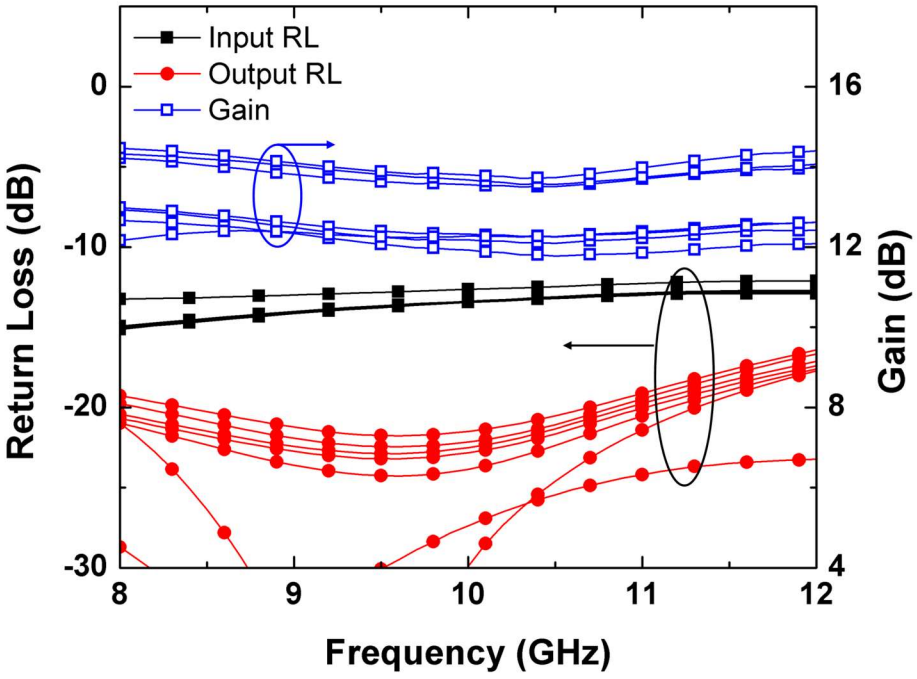

Figure 26: Input and output return loss and gain of the major states for the forward operation (after [1]).

The phase performance of the 6 major states are plotted in Figure 27. The black solid line are the reference relative phase shift curves that are used to benchmark the measured phase performance of the phase shifter. The blue curved shows the relative phase shift of the design without any bit tuning. Due to the finite order of filter networks used in the design, the flatness of each in-band phase states is limited. The first five bits of the phase shifter element show close matching to the intended relative phase states with relatively low phase error. The phase error of the MSB shows an average of 10-degree phase error as shown in the plot. This is probably resulted from inaccuracy in electromagnetic simulation during the design. The significant absolute phase error from the MSB also results in high mean and RMS phase errors. However, this error can be minimized through using the three tuning bits. By tying the control signals of the three

tuning bits together with the control signal of the MSB, the 10-degree gap of the MSB is effectively closed. Consequently, as shown in Figure 28, the mean phase error is decreased to -2.4 degrees at the centre frequency and the RMS phase error is decreased to less than 2.2 degrees across the design frequency.

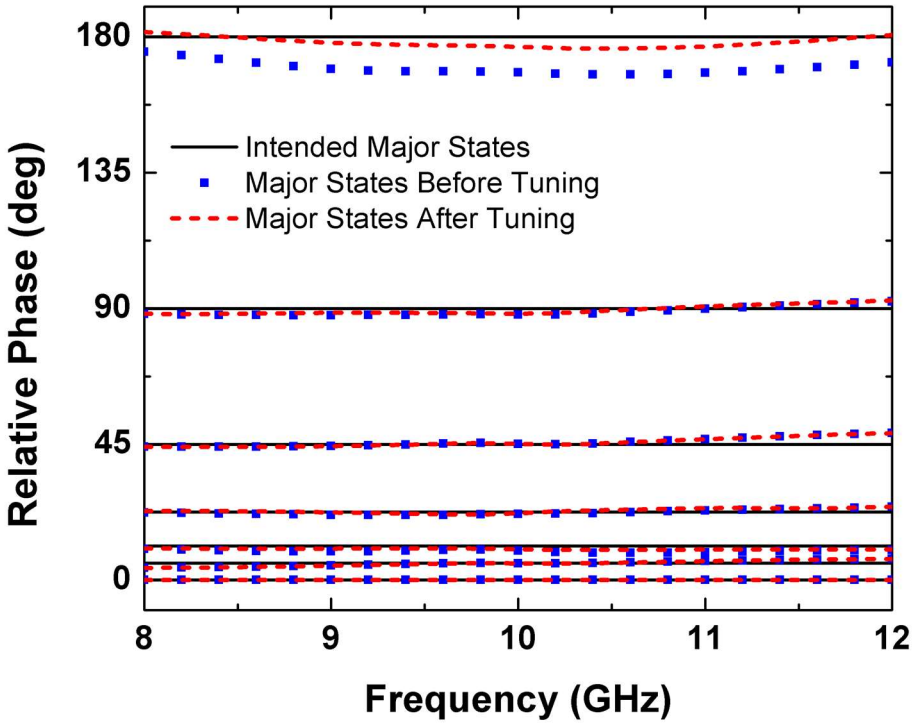

Figure 27: Reference phase and measured major relative phase before and after bit tuning (after [1]).

One big advantage of passive T/R modules is their high linearity. The input-referred 1-dB compression (IP1dB) of the reference state under forward operation is measured and plotted in Figure 29. An unimpressive -15 dBm IP1dB is measured. Since the passive filters and switches should inherently have high linearity, the P1dB of the phase shifter is likely limited by the cascade of the four active DPDT switches.

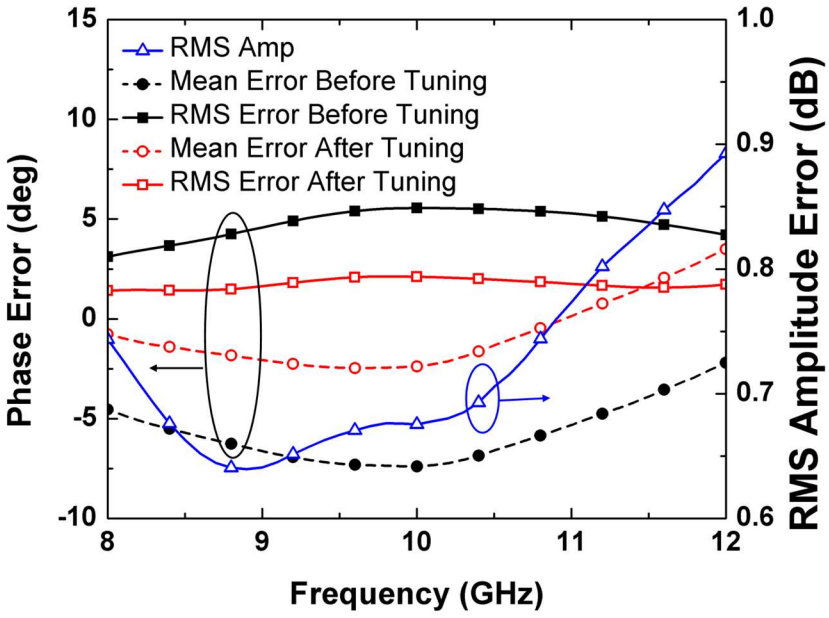

Figure 28: Mean and RMS phase error before and after bit tuning, and RMS amplitude error (after [1]).

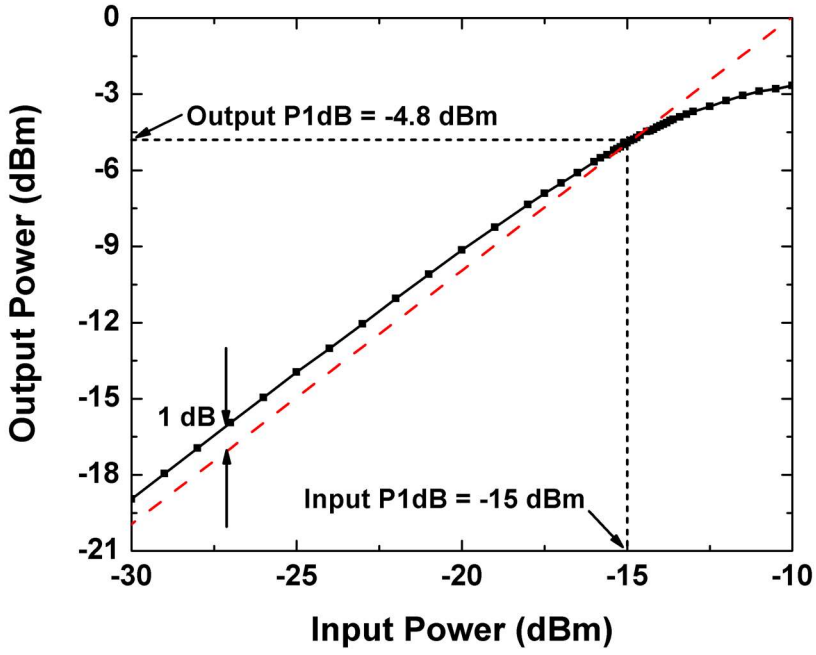

Figure 29: Input-referred 1 dB compression point of the phase shifter (after [1]).

The performance of the X-band 6-bit phase shifter is benchmarked versus similar phase shifter in Table 1.

Table 1 Performance Comparison of Phase Shifters

	Bits	Freq (GHz)	Gain (dB)	RMS Amp Err (dB)	RMS Phi Err (deg)	Input P1dB (dBm)	P_{DC} (mW)	Size (mm^2)
[28]	5	6-18	16.5-19.5	< 1.1	< 5.6	-	61.7	1.2×0.75
[7]	6	8-12	< -2.5	< 2	< 6.4	-11	110	1.87×0.88
[37]*	5	8-10.7	11	< 0.6	< 8	-	33	13.3
[27]	5	8-12	< -10.8	< 0.5	< 6.5	9.3	0	1.14×0.78
[29]*	5	9-11	25	1.2	3.8	-19**	352	15.6
[1]	**6**	**8-12**	**> 11.5**	**< 0.9**	**< 2.2**	**-15**	**195**	**2.6×1.5**

** Circuit specifications of received path in a T/R module including front-end LNA,*
*** Calculated from output P1dB and gain.*

In summary, the X-band 6-bit bi-directional phase shifter show greater than 11.5 dB gain across the desired bandwidth through the incorporation of active di-directional DPDT switches. The phase shifter shows good input and output matching. Due to the switched HP/ LP topology, the phase shifter shows less than 0.9 dB RMS amplitude error and a RMS phase error less than 2.2 degrees. However, the used of multiple single-ended anti-parallel cascode amplifiers significantly limits the linearity of the T/R module.

2.5 Summary

In this chapter, we investigated different choices and techniques to reduce and compensate the loss in passive T/R modules. We proposed the used of BDA in the passive

T/R modules for loss compensation and we demonstrated this concept in a 6-bit X-band switched high-pass/ low-pass phase shifter design.

The phase shifter presented shows a greater than 11.5 dB gain across the design bandwidth. The choice of topology results in a low RMS phase error and a low RMS amplitude error. The incorporation of active DPDT switches in the design proves effective in loss compensation. However, due to the four cascaded active stages, the resultant overall input referred P1dB compression point is an unsatisfactory -15 dBm. In other words, the proposed design implies a significant trade-off between the loss compensation and linearity. Although this trade-off may be justifiable for certain applications, it is in general undesirable.

CHAPTER 3. DIFFERENTIAL BDA DESIGN USING SIGE HBTS

3.1 Introduction

The use of bi-directional amplifiers (BDAs) is seen in various applications including front-end PA/ LNA, active circulator [38], and loss compensation in passive beam-forming elements. In this thesis, we focus the application of BDAs in passive T/R modules for loss compensation purposes.

In the previous chapter, we demonstrated the use of BDAs with single-ended anti-parallel cascode amplifier pairs in a switched-type phase shifter for loss compensation. The rationale behind the choice of cascode topology for amplifier core is mainly two-fold. It is important to have an amplifier with high single-stage gain to avoid bulky distributed amplifier structure. The more important reason is the high reverse isolation of cascode structure, which is critical to ensure the stability of the circuit. For cascode amplifier, the P1dB is restricted by the upper common-base transistor which has large voltage swing across the base and collector nodes. While the proposed BDA is effective in loss compensation, it limits the overall linearity of the phase shifter. As a result, by using the BDA described in Chapter 2, loss compensation and bi-directionality conservation are achieved at the expense of the linearity of the phase shifter, which is one of the main advantages of passive phase shifters. Therefore, to realize more effective loss compensation using BDAs, alternative BDA designs that can achieve higher output swing are desired.

A natural intuition to the limited P1dB problem is to explore differential BDA topologies, which in theory promise 3 dB higher output power, and thus higher dynamic range. In this chapter, we survey the benefits and designed concerns of differential amplifiers at high frequency. A design of differential anti-parallel cross-coupled common-emitter bi-directional amplifier using SiGe HBTs is presented in this chapter. This design is submitted to *IEEE Microwave and Wireless Components Letters* and is currently under review.

3.2 Differential Amplifiers

Differential amplifiers are widely used in analog and RF circuit for many reasons. Differential topologies provide good common mode rejection at the input and is less prone to supply noise. At millimeter-wave, the supply noise rejection is still applicable for non-linear and time-variant circuit but less important for amplifiers due to the high millimeter-wave band and baseband frequency isolation [8]. Differential topologies are still very relevant at millimeter-wave design for many other benefits. One advantage of differential circuits is the virtual ground nodes which make good low-impedance physical ground connection less challenging. Another advantage of differential amplifier is the higher output swing as compared to its single-ended counterpart. This is the advantage the proposed BDA explores to enable higher P1dB.

Differential topologies also bring many properties and design techniques that can help improve the efficiency and performance of the design. It is well known that symmetrical inductors, when driven differentially, show higher Q factor as compared to single-ended inductors, and thus resulting in higher power efficiently when used for

impedance matching. This phenomenon is explained by B. Razavi in his textbook [39]. Efficient output impedance transformation and power combining using symmetrical inductor based transformer is technique extensively used in RF and millimeter-wave circuit design, as demonstrated in [40] by D. Zhao and P. Reynaert. Another advantage of using differentially driven symmetric inductors is that the center tap of the inductor is a virtual AC signal ground, a convenient node for bias supply without the need for additional large RF choking inductors (as shown in Figure 30). A very useful technique for differential circuit is capacitive neutralization. This technique is used in most of modern high-performance amplifier design, especially power amplifier, to increase stability and output power. This technique will be discussed more in detail in latter section of this chapter.

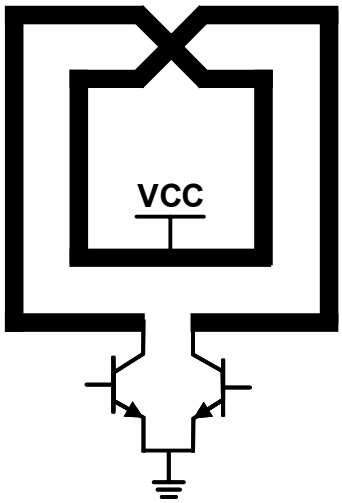

Figure 30: Symmetric inductor in a differential circuit using center tap for bias.

3.2.1 Differential Mode Stability Analysis

Rollett's K-factor analysis [41] and the μ-factor test are the two most frequently used for stability analysis on two-port networks by designers. Due to the finite reverse

isolation of two-port amplifiers, the impedance looking into/ out of the input/ output terminals of the two-port network depend on the loading conditions at the ports. The two-port network is unconditionally stable if the K-factor is greater than one and the determinant of the s-parameter matrix is less than one. These conditions are equivalent of saying that the network is unconditionally stable if the real part of the network impedances looking into the input and output ports are always positive under all possible passive loading conditions. The K-factor analysis provides a binary decision on whether the two-port network is unconditionally stable, but greater K-factor value does not necessarily indicate the two-port has greater stability. The μ-factor test, on the other hand, provides indication on how far the amplifier is from the boundary of stability [42].

Although, K-factor and μ-factor tests are good indicators to the stability of a two-port network, they treat the two-port network as a black box and do not provide information on whether any internal nodes of the two-port network are likely to oscillate. To test the stability at internal nodes of a two-port system, an alternative method called the S-probe analysis was introduced by Texas Instruments in [43]. A succinct S-probe testing procedure could be found in the Master's thesis by R. L. Schmid [44]. To test if a node is likely to subject oscillation, a S-probe is inserted at the node. The product of the reflection coefficient seen from the two sides of the probe is computed and the result is plotted on a Nyquist plot. The S-probe circuit model for an arbitrary node in the network and an example resultant Nyquist plot were shown in Figure 31 (after [44]). The node is stable if the point (1,0) is not encircled by the resultant plot.

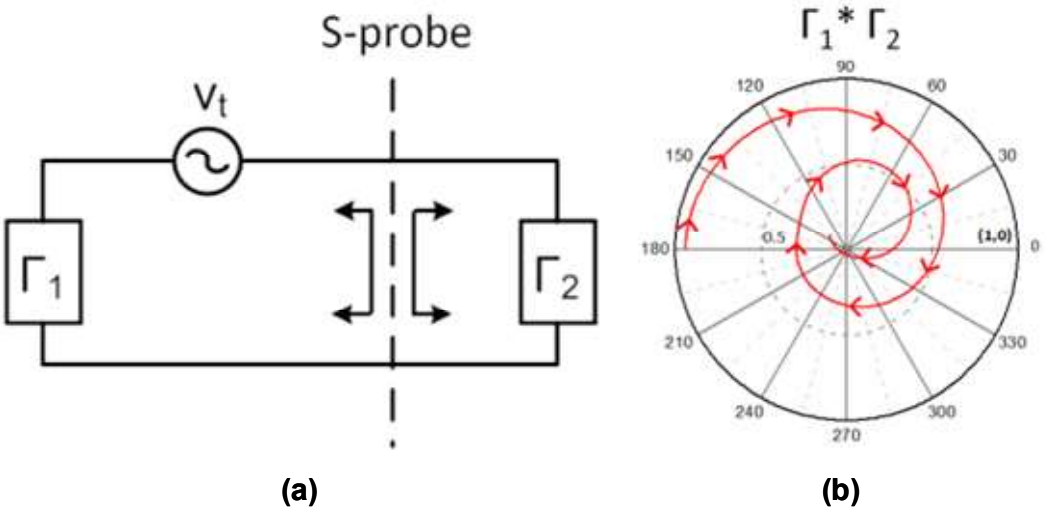

Figure 31: (a) S-probe circuit model for an arbitrary node, (b) example Nyquist plot (after [44]).

3.2.2 A Differential 77 GHz Low Noise Amplifier Design

The author designed a 77 GHz low noise amplifier (LNA) with three cascaded cascode stage using GlobalFoundries 90 nm BiCMOS 9HP technology. At millimeter-wave frequency, the parasitic capacitance from transistors and the parasitic inductance from signal routing become significant, causing various gain degradation and stability issues that are less relevant at lower frequency. The base node of the upper cascode transistor is known to be prone to oscillation. The parasitic capacitance at the collector of the lower common-emitter transistor and the emitter of the common-base transistor provide capacitive degeneration to the cascode transistor. This capacitive degeneration results in a negative real part of the impedance looking into the base of the upper cascode transistor, and therefore small amount of parasitic inductance of the bias line at the upper base can easily result in oscillation. The design was simulated and laid out with considerations for

differential mode stability. The Cadence layout view of the three-stage LNA design is shown in Figure 32. The design adopts pseudo-differential topology with transformer based baluns and inter-stage matching. Inductive degeneration is used for each stage to achieve simultaneous noise and power matching.

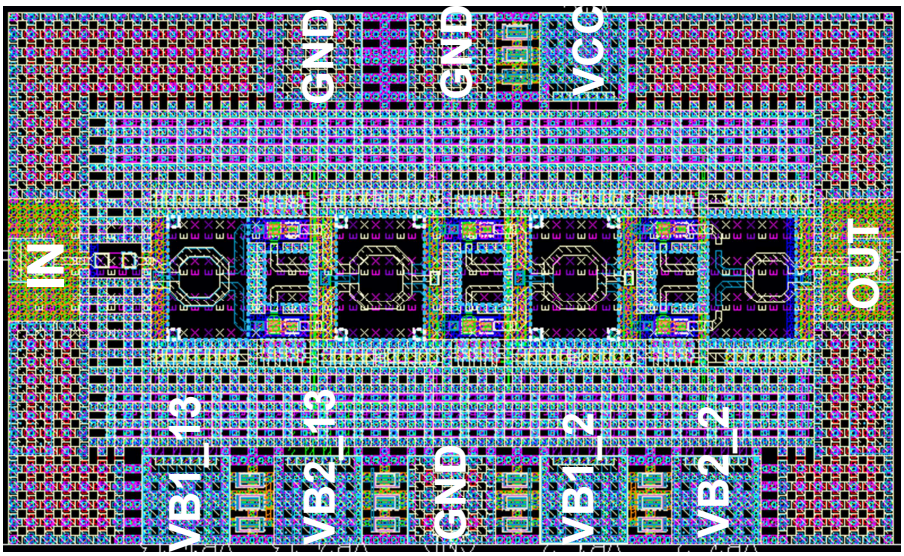

Figure 32: Cadence layout view of the three-stage differential cascode LNA.

The design simulation was primarily conducted using Keysight ADS. Differential mode stability was checked using the standard K-factor and μ-factor test, and the results are shown in Figure 33. The K-factor and the μ-factor tests indicate that the two-port network shows good stability. With concerns for internal node stability, S-probes was placed at the cascode base nodes at each stage as well as center taps of each transformer. The products of the reflection coefficients looking into both side of each S-probe are plotted in Figure 34, and results indicate good stability at sensitive internal nodes.

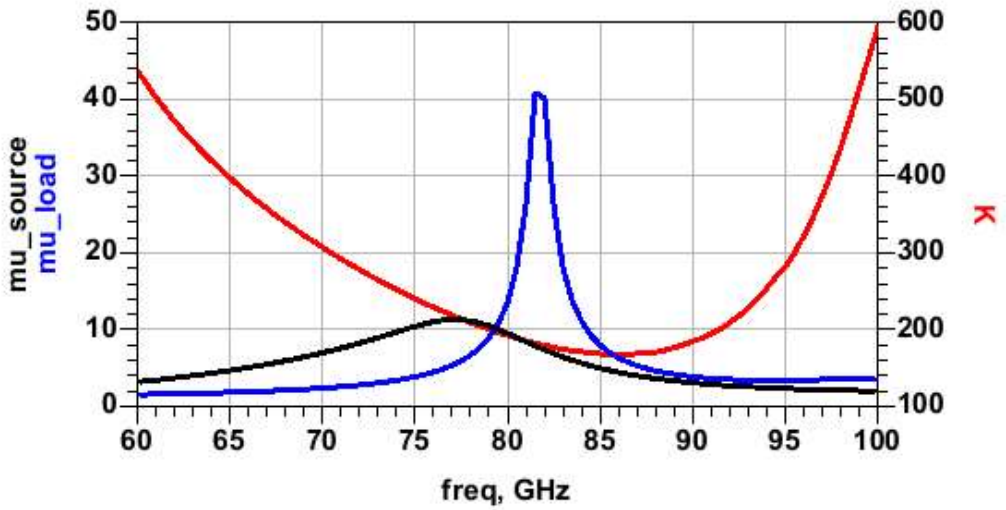

Figure 33: K- and μ-factor tests of the three-stage differential LNA.

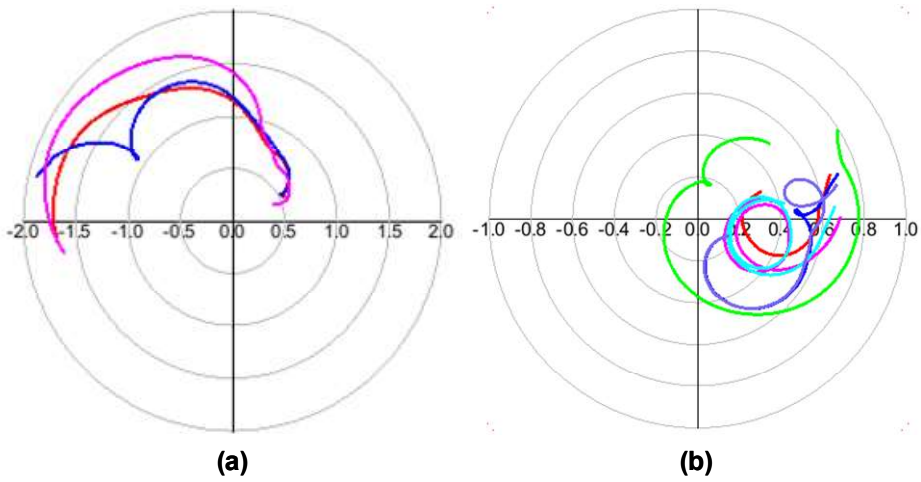

Figure 34: Nyquist plots of the three-stage differential LNA at (a) cascode base nodes and (b) transformer center taps.

3.2.3 Common Mode Gain of Differential LNA

Despite of the indication of good stability as simulated in the previous section, a strong tone was observed from a wide band s-parameter characterization of the design, as

shown in Figure 35. A strong out-of-band signal was observed at 34 GHz that heavily saturated the amplifier. The out-of-band signal is a clear indication that the amplifier design has serious common mode issue which the author failed to capture during the design process, even though the S-probe tests suggests that the center taps of transformers are stable.

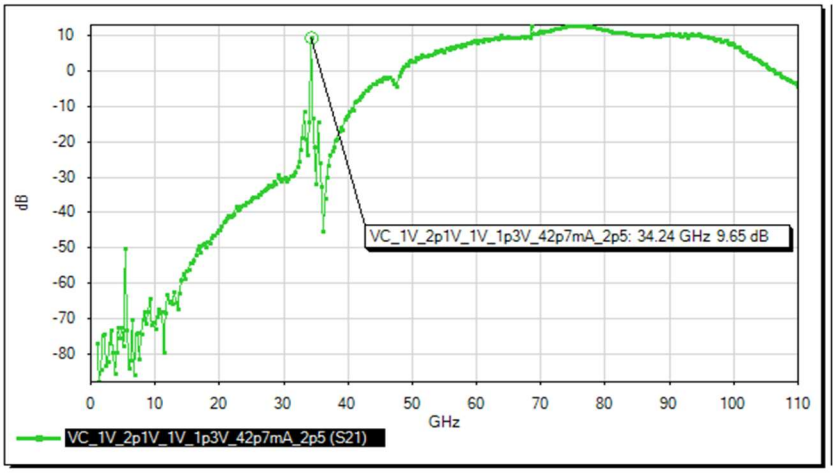

Figure 35: S-parameter characterization of the 77 GHz differential LNA from DC to 110 GHz, showing oscillation at 34 GHz.

With the conclusion drawn from the measurement result, the author revisited the schematic design and tested for common mode gain of the multi-stage amplifier. A small common mode signal is injected at the base of the common-emitter transistor pairs at the first stage and the common mode gain is checked at the collectors of the cascode transistor pairs at the last stage. The common mode S21 is plotted in Figure 36, and the frequency of the peak in the common mode gain curve coincide with the frequency of the strong tone observed in the measurement.

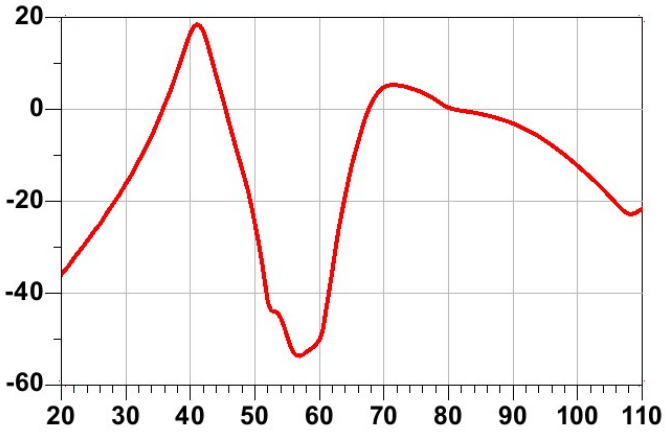

Figure 36: Common mode gain of the 77 GHz differential LNA.

One of the downside of differential and balanced circuits is the need to operate with differential signals. Most of the test equipment and many of the components in a T/R module are designed to operate with single-ended input and output. To convert between single-ended and balanced signals, engineers often design on-chip baluns to achieve this task. Due to the amplitude and phase imbalance of the input signal, a common mode signal can develop at the input of the differential pair. In millimetre-wave differential amplifier design, tail current source or tail resistors are rarely used due to various concerns such as additional layout complexity, additional noise and additional parasitics. Without the degeneration from the common tail, the common mode gain of each stage can be high, especially at lower frequency when the transistor gain is much higher compared to the gain at higher frequency. In addition, the signal imbalance contributed by layout parasitics effects also lead to less ideal common mode signal rejection. In the case of this differential circuit design case, the common mode signal is amplified to a great amplitude enough to saturate the whole circuit.

An easy way to lower the common mode gain is to introduce more loss to the common mode signal that is unseen by the differential signal. In this 77 GHz differential amplifier design with transformer balun and inter-stage matching, the most convenient way to introduce loss to common mode signal is to put a small series resistance at the center taps of the transformers, which appear as virtual ground nodes by differential signal. Small series resistor of 10 Ω are placed at each center tap nodes of the transformers to introduce common mode loss. Note that for this 77 GHz differential LNA design, transformer center taps are also used to supply DC bias to the circuit, and therefore series resistors at the center taps will also lead to bias voltage drops and DC power dissipation. For LNAs with low DC current bias, a small series resistor at VCC supply only causes a small voltage drop. However, extra consideration is needed if the amplifier consumes large DC current, as even a small resistor at the DC current will cause serious amplifier efficiency degradation. The modification was applied to the three-stage amplifier design and the common mode gain was plotted again as shown in Figure 37. The common mode gain is effectively suppressed.

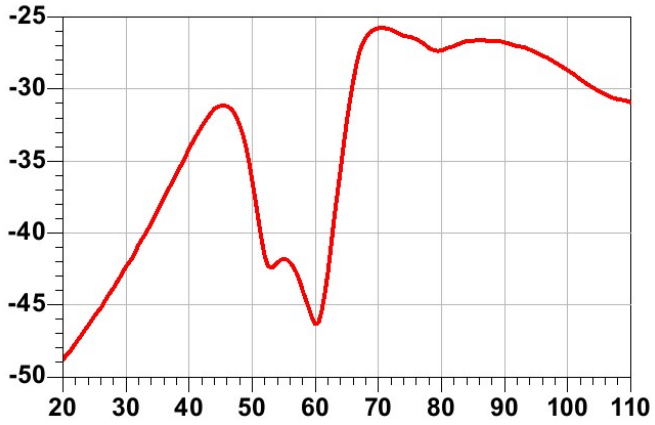

Figure 37: Common mode gain of the 77 GHz differential LNA with small resistors at transformer center taps.

To verify the effectiveness of the solution, a two-stage 77 GHz differential amplifier (Figure 38) was designed using GlobalFoundries 130 nm 8HP technology, which has a faster turn-around time. The s-parameter was measured and no out-of-band tone was observed as shown in Figure 39.

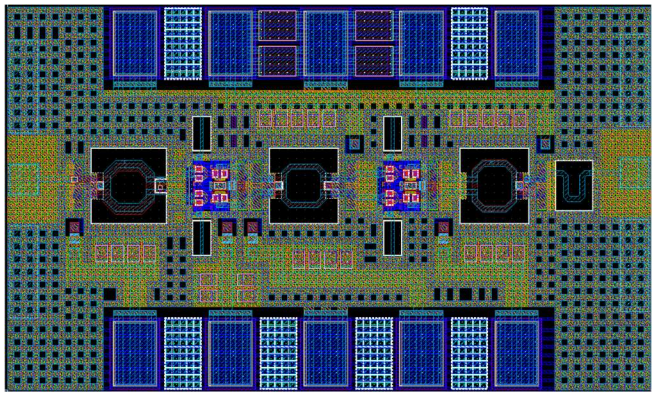

Figure 38: Cadence layout view of two-stage 77 GHz differential LNA in 8HP.

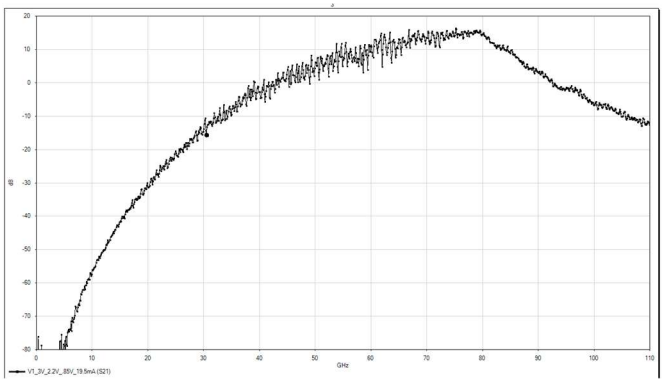

Figure 39: S-parameter characterization of the two-stage LNA from DC to 110 GHz

3.2.4 Capacitive Neutralization

The collector-base junction capacitance (C_{CB}) of the transistors creates an undesirable negative feedback path for common-emitter amplifiers. This feedback reduces

the amplifier gain and results in poor isolation between the input and output of the amplifier stage. One of the main reason for the popularity of cascode topology in amplifier design is because the common-base transistor mitigates the Miller effect and thus enabling high reverse isolation, better stability and simplified input and output matching when compared to common-emitter amplifiers.

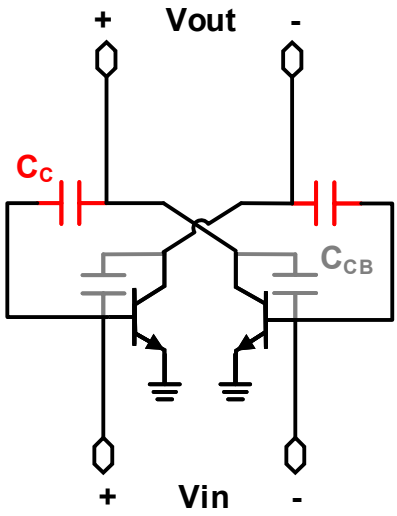

Figure 40: Simplified common-emitter pair illustrating capacitive neutralization.

For a differential amplifier design, however, the undesirable feedback from C_{CB} can be easily compensated for by using a pair of cross-coupled capacitors between the base and collector terminals. This technique is called capacitive neutralization and is vastly used in differential amplifier design to increase reverse isolation of the amplifier stage [45], [46]. As shown in Figure 40, a pair of small capacitors C_C are cross coupled between the input and output terminals with the same polarity, thus providing a compensating current to cancel the undesired feedback due to the junction capacitance C_{CB}. Although neutralization technique does not provide complete uni-lateralization due to the existence of other

feedback mechanisms, this technique significantly improves the reverse isolation of differential amplifier stage. Various works have studied and showed the reverse isolation improvement of the differential pair with neutralization technique. For example, W. L. Chan and J. R. Long as shown a greater than 10 dB improvement of reverse isolation when neutralization technique is applied to differential common-source amplifier stage, as illustrated in Figure 41 (after [5]). Because of the mitigation of Miller effect, higher output power is obtained and the circuit stability is improved. However, it is worth noting that neutralization is in fact partially cancelling the negative feedback due to C_{CB} with positive feedback through C_C. Therefore, while it is important to ensure that the choice of C_C is big enough to provide sufficient cancellation, it is essential to ensure the choice of C_C does not cause oscillation itself. In practice, a small capacitance value comparable to the C_{CB} of the transistor used is sufficient.

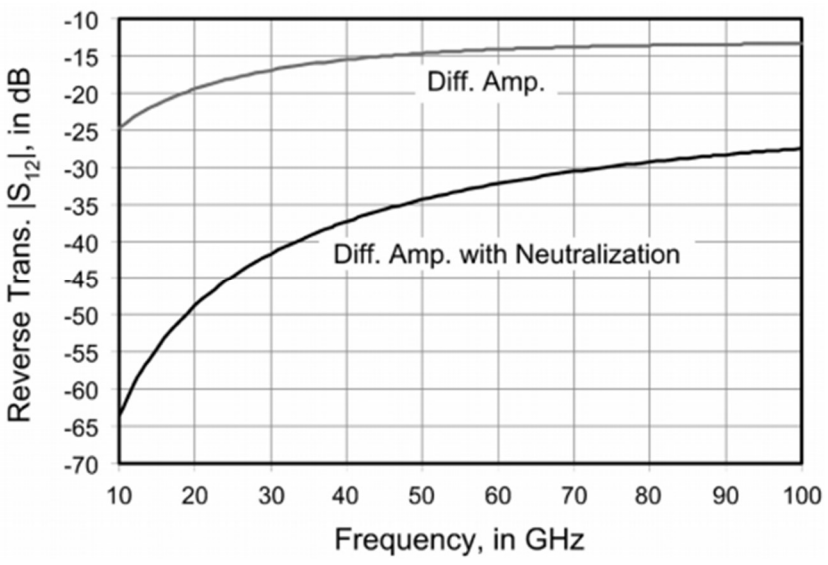

Figure 41: Reverse isolation improvement of common-source differential amplifier using neutralization technique (after [45]).

Although the neutralization technique we discussed so far in this section applies to differential common-emitter or common-source amplifiers, the application of neutralization is not limited to the topology we discussed above. S. V. Thyagarajan *et al.* have demonstrated the use of neutralization technique in cascode amplifier implemented in 28 nm CMOS technology to mitigate the parasitic coupling between the source and drain nodes [19].

3.3 A 28 GHz Differential BDA Design Using SiGe HBTs

A 28 GHz switchless differential BDA design using GlobalFoundries 130 nm SiGe BiCMOS technology is presented in this section. The design adopts differential topology in attempt to deliver more output power and achieve improved P1dB as compared to the single-ended cascode BDA presented in Chapter 2. Two anti-parallel cross-coupled common-emitter pairs are used for forward and backward signal amplification. Operation direction is controlled though base bias on the two pairs. The forward and backward gain are 10 dB and 8.6 dB, with noise figure (NF) of 3.9 dB and 4.2 dB, respectively, at 28 GHz. The input-referred 1 dB compression point at 28 GHz for forward and backward operations are -2.4 dBm and -0.4 dBm, respectively. The BDA consumes 26.9 mW of power with a 1.6 V VCC at a V_{BE} bias of 0.86 V. The circuit has dimensions of 0.71×0.90 mm^2 including bondpads. The circuit design and measurement results will be discussed in the following sub-sections. Contents in this section are taken from the original work by the author *et al.* "A 28-GHz switchless, SiGe bi-directional amplifier using neutralized common-emitter differential pair." [47] This work has been submitted to *IEEE Microwave and Wireless Components Letters* and is currently under review.

3.3.1 Circuit Design

The schematic of the proposed switchless differential BDA core is illustrated in Figure 42. The differential BDA consists of two cross-coupled differential common-emitter pairs ($Q_{1,2}$ and $Q_{3,4}$) with equal transistor size, for forward and backward amplification respectively. A common VCC bias is applied to the collectors of both differential pairs through the center-tap of the secondary coils of the two input/output transformer baluns. DC blocking capacitors are used to decouple the collector and base biases. The sizing of the transistor and the choice of emitter degeneration inductance follow standard LNA design procedures for simultaneous gain and noise matching to ensure modest noise figure. However, the transistors are biased close to peak f_T/f_{MAX} current density for high linearity. The component values used for the design are also listed in Figure 42. Transformer balun are used at the input and output for on-die single ended characterization.

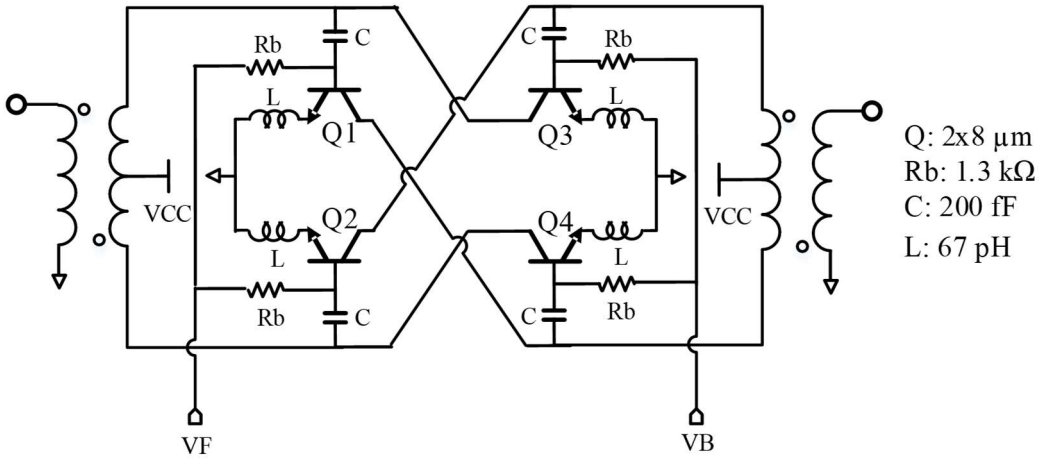

Figure 42: Schematic of the proposed differential BDA (after [47]).

To select forward operation, $Q_{1,2}$ are biased in forward-active region while $Q_{3,4}$ are turned off. The bias resistors, base-emitter junction capacitance, and degeneration inductance of $Q_{3,4}$ help to de-Q the output impedance and make output matching network design easier. The bases and collectors of differential pair $Q_{1,2}$ are cross-coupled with the collector-base (CB) junctions of $Q_{3,4}$ for capacitive neutralization. Since all transistors are equally sized, the capacitances of reverse biased $Q_{3,4}$ CB junctions are comparable to C_{CB} of $Q_{1,2}$, and therefore the CB junctions of $Q_{3,4}$ are suitable for providing capacitive neutralization for $Q_{1,2}$.

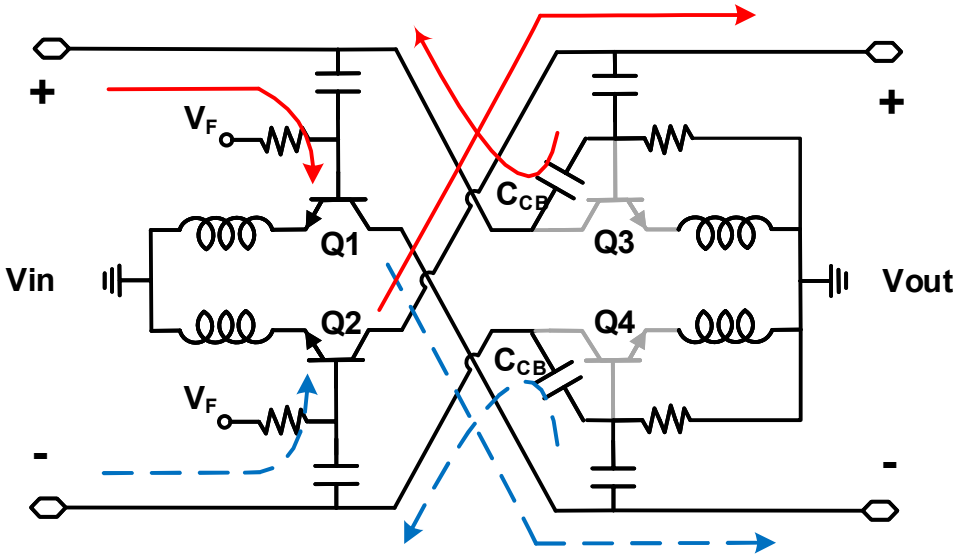

Figure 43: Simplified equivalent circuit of the differential BDA core under forward operation.

The forward operation of the proposed BDA core is illustrated in Figure 43 with solid arrows representing positive signal flow and dotted arrows representing inverted signal flow. Unlike the anti-parallel cascode BDA presented in Chapter 2 where the parasitics of the OFF amplifier does not contribute to the circuit performance, if not

creating additional undesirable signal feedback path, the proposed differential topology takes advantage of the parasitics of the OFF amplifier to enhance the performance of the ON amplifier..

3.3.2 Measurement Results and Discussions

Figure 44 shows a microphotograph of the fabricated differential BDA. The dimensions of the BDA are 0.71 × 0.90 mm^2 including bondpads. The two sets of the DC pads on the north and south sides are internally connected, and the circuit can be fully biased through either set of DC pads. A 1.6 V VCC is applied to the collectors of the transistors with a 0.91 V base bias for the active differential pair (the actual V_{BE} is 0.86 V from simulation). The circuit draws 16.8 mA of DC current.

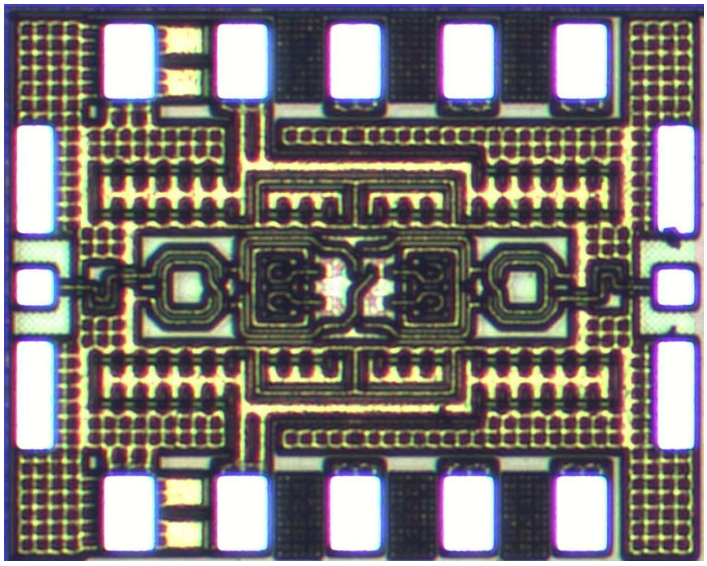

Figure 44: Microphotograph of the 28 GHz switchless differential BDA (after [47]).

A standard two-port SOLT calibration was performed for on-die s-parameter characterization. Both the forward and backward operation are characterized and

compared. Figure 45 shows the measured and simulated return loss under both modes of operation. S11 and S22 of both operational modes are under -10 dB between 26.5 GHz and 29.5 GHz. The simulated and measured forward and backward gain are plotted in Figure 46. The measured forward operational gain is 10 dB, and the gain for backward operation is 8.6 dB, at 28 GHz. The measured gain characteristics show a close match with simulation results, with maximum of 0.6 dB difference. The 1.4 dB gain difference between the forward and backward operations is a result of the asymmetric cross-coupling routing between the two differential pairs. The measured results show 10 GHz 3-dB bandwidth from 22 GHz to 32 GHz for the two operational modes.

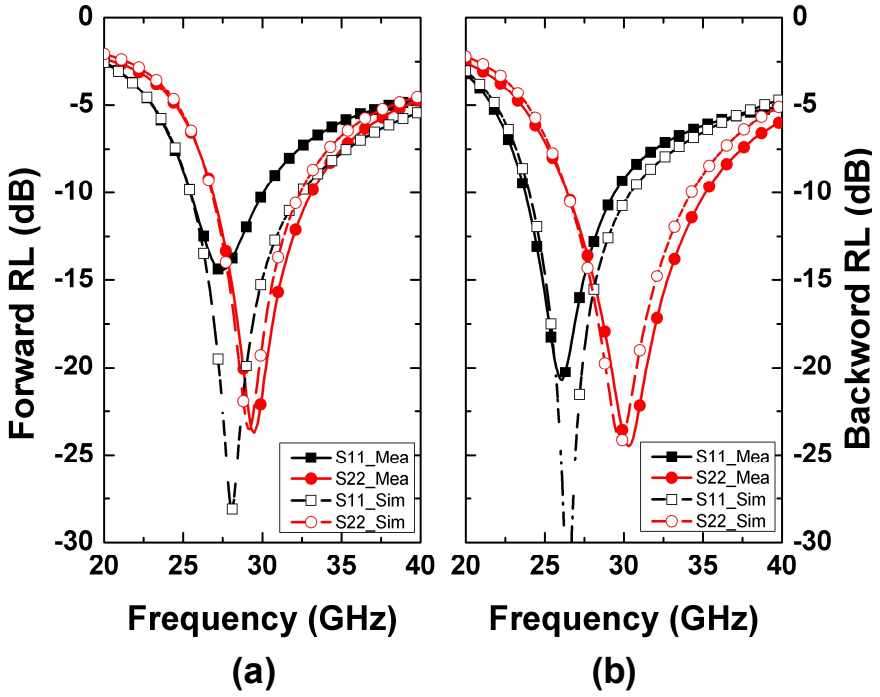

Figure 45: Simulated and measured return loss of the differential BDA under (a) forward and (b) backward operations (after [47]).

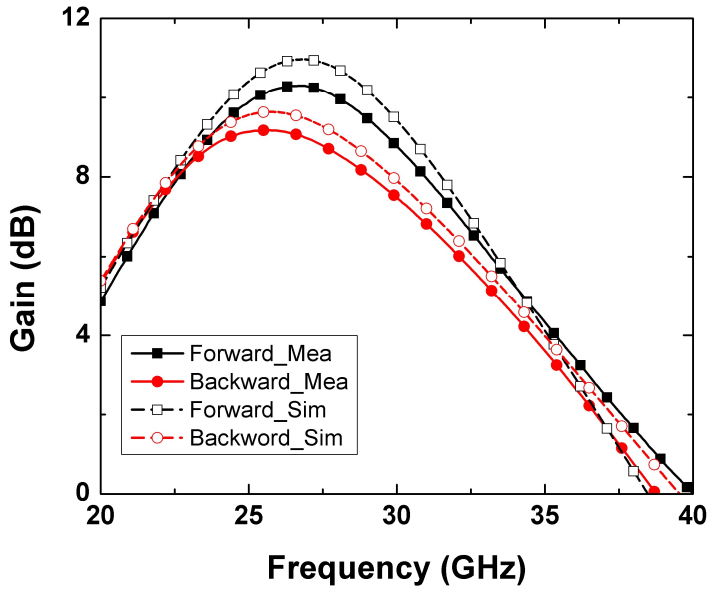

Figure 46: Simulated and measured of the differential BDA under forward and backward operations (after [47]).

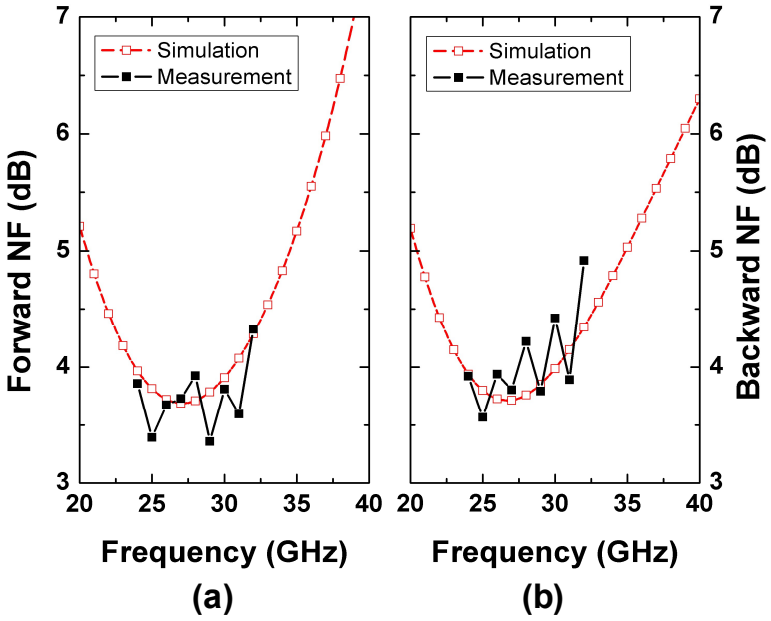

Figure 47: Simulated and measured noise figure of the differential BDA under (a) forward operation and (b) backward operation (after [47]).

The noise figures of the two operational modes were measured and plotted in Figure 47. Forward operation shows 3.9 dB NF at 28 GHz, and the NF of backward operation at 28 GHz is 4.2 dB. Figure 48 shows the P1dB measurement of forward and backward operation. The measured input-referred P1dB of forward operation is -2.4 dBm, and that of backward operation is -0.4 dBm.

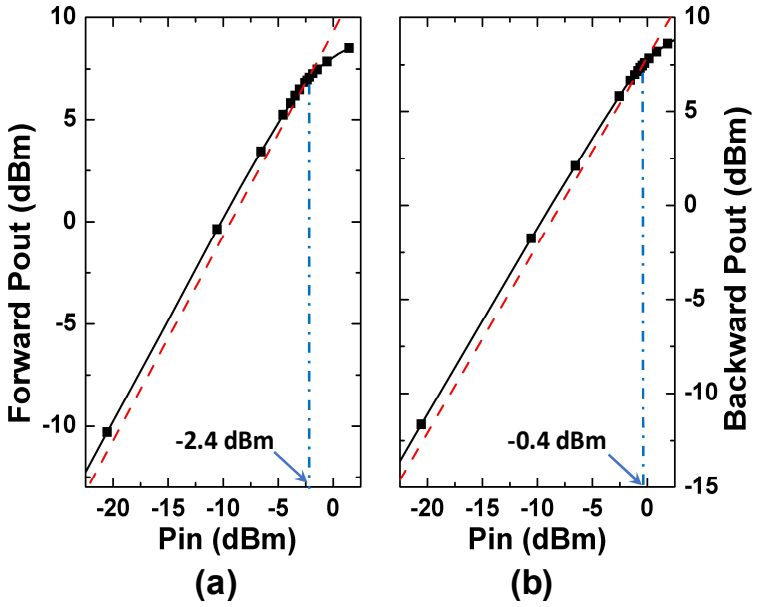

Figure 48: Measured P_{OUT} *vs.* P_{IN} of the differential BDA under (a) forward operation and (b) backward operation (after [47]).

The performance of the proposed differential BDA is compared with the performance of other switchless BDAs presented in the literature in Table 2. A differential BDA core, that takes advantage of the parasitics of the OFF amplifier to achieve performance enhancement, has been demonstrated. The proposed BDA shows competitive performance in gain, NF and P1dB with modest DC power consumption.

Table 2 Performance Comparison of Switchless BDAs

Ref	Tech	Freq (GHz)	Gain (dB)	RL (dB)	OP1dB (dBm)	NF (dB)	P_{DC} (mW)	Size (mm^2)
[48]	65nm CMOS	55-66	-4.3 – 8.6	-	-2.0	6.9 (sim)	27.6	0.80×0.60 (core)
[33]	130nm CMOS	8.5 – 10.5	> 6.2	> 11	> 7.4	< 6.1	43	0.39×0.58
[49]	130nm CMOS	3 – 20	> 10	> 9	> 8	3.2 – 6.5	68	0.96×0.85
[47]	**130nm SiGe**	**26.5 – 29.5***	**10/ 8.6****	**> 10**	**6.9/ 7.5****	**3.9/ 4.2****	**26.9**	**0.71×0.90**

** Frequency range where RL is > 10 dB. The 3dB BW is 22 – 32 GHz.*
*** Forward / backward operation measured at 28 GHz.*

3.4 Summary

In this chapter, the advantages and design concerns of differential amplifier design have been briefly discussed. Taking into consideration of the design concerns and techniques, the author successfully designed and demonstrated a differential anti-parallel cross-coupled common-emitter BDA.

The proposed BDA shows comparable gain with the active DPDT design discussed in Chapter 2 but demonstrates much better linearity. Note in the active DPDT design described in Chapter 2 that resistive termination is used to simplify input and output matching as well as extend the bandwidth of the design. The same resistive matching technique could be applied to the proposed differential BDA design if a higher bandwidth is desired. Doing so would lead to gain degradation, but the resultant bandwidth and P1dB would expect to see a significant improvement.

CHAPTER 4. CONCLUSION

This work has demonstrated the use of compact bi-directional amplifiers in passive T/R modules for loss compensation while preserving the bi-directionality of the module. A compact switchless BDA using differential topology has been described in this work as a potential solution to linearity limitation posed by single-ended anti-parallel cascode BDA topology. The differential BDA composes of two anti-parallel cross-couple common-emitter differential pair, where the circuit parasitics of the OFF pair is used in advantage to improve the linearity, gain and stability of the ON differential pair. Although the resultant circuit has much narrower fractional bandwidth as compared to the single-ended anti-parallel cascode BDA with resistive matching network, larger bandwidth can be easily traded for lower gain by incorporating resistive matching in the input and output.

4.1 Future Work

The presented work was design as a proof of concept to demonstrate the potential of using differential topology in BDA design. The author identifies the imbalance in the forward and backward operation performances. This is caused by cross-over in signal routing and is not easily avoidable. Further attempts in layout optimization could be made that might lead to less performance difference. However, this imbalance could also be intentionally enhanced to tailor to different performance requirement of the signal transmit and receive paths.

This work only presented a differential bi-directional amplifier without demonstrating its application in loss compensation for passive T/R modules. More work

could be done to optimize and incorporate the proposed design in a system to achieve the task this BDA is intended to do. However, the application of differential BDA is not necessarily limited to loss compensation in beam forming elements in the T/R modules. The author sees a potential of using the differential BDA for a front-end quasi-circulator circuit. Further investigation of other differential BDA topologies other than cross-coupled common-emitter pair could also be beneficial.

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