MODELING, DESIGN AND FABRICATION OF MINIATURIZED, HIGH PERFORMANCE AND INTEGRATED PASSIVE COMPONENTS FOR 5G AND MM-WAVE APPLICATIONS

A Dissertation
Presented to
The Academic Faculty

By

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology

December 2020

MODELING, DESIGN AND FABRICATION OF MINIATURIZED, HIGH PERFORMANCE AND INTEGRATED PASSIVE COMPONENTS FOR 5G AND MM-WAVE APPLICATIONS

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[Quran 55:13]

Arabic: Fabi'ayyi 'Ālā'i Rabbikumā Tukadhdhibān.

<u>Translation</u>: *"So which of the favors of your Lord would you deny?"*

To my parents, *Akbar* and *Yasmin*,

my brother, *Faizan*,

my wife, *Amna*,

and my newborn daughter, *Anaya*,

whose unconditional love, countless sacrifices and unwavering support have granted

reason to my efforts and meaning to my existense.

This is for *You!*

the pillars supporting various research programs at GT-PRC. I have the honor of working with Yoichiro Sato (AGC), Masahiro Karakawa (Ajinomoto), Andrew Ketterson (Qorvo), Deep Dumka (Qorvo), Aayush Thapa (Northrop Grumman), Kaysar Rahim (Northrop Grumman), Christian Hoffman (Qualcomm), Jeremy Dunworth (Qualcomm), Ravi Shenoy (Qualcomm), Ali Tassoudji (Qualcomm), Dan Oh (Samsung) and Urmi Ray (iNEMI). I hope the industry consortium at GT-PRC continues to push the boundaries and make strides in advancing the field of electronic packaging. The administrative staff of PRC also deserves my gratitude for their consistent help and support: Christopher White, Lila Dahal, Brian McGlade, Shari Tavares and Carol Mills.

To my friends and family, thank you for your tremendous support and your faith in me to get through the challenges of work and life on the other side of the world. I am grateful for the sacrifices and prayers of my parents. It would not have been possible without their firm belief in me.

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SUMMARY

The objective of this research is to model, design, fabricate and characterize integrated passive components for 5G and mm-wave applications on advanced substrates such as ultra-thin laminated glass. These passive components include filters, power dividers, antenna arrays, diplexers and their integrated versions. The target frequency range of these passive components are the 5G new radio (NR) bands: 28 and 39 GHz and the bands of interest are in the Frequency range 2 (FR2) as defined by 3GPP: n257, n258 and n260.

Both circuit-level simulation and full-wave electromagnetic (EM) simulation are employed to design these passive components for 5G and mm-wave applications. Glass substrate is emerging as an ideal candidate to realize mm-wave technologies. This is mainly because of its low loss, superior dimensional stability, ability to form fine-pitch through-vias, stability to temperature and humidity, matched coefficient of thermal expansion (CTE) with devices, and availability in large-area, low-cost panels. Passive components such as filters, power dividers, antenna arrays and diplexers can benefit from the aforementioned advantages of glass substrates along with precision redistribution layers (RDL) to enable miniaturization. These components can be designed and fabricated to achieve dimensions of less than twice the free space wavelength corresponding to the operating frequency and can be integrated in electronic packages such as RF front-end modules (FEM), as integrated passive devices (IPD). Precision linespace capabilities also empower the designer to opt for higher-impedance structures for filters, reducing the footprint. The demonstrated filters exhibit low loss, low standing wave ratio (VSWR) and high selectivity. Similarly, the power dividers are designed and fabricated in two-, three- and four-way equal-split ratios, and they can used in low-power on-device antenna-to-chip chain to provide power to corresponding antenna array configurations. Moreover, they utilize minimal matching techniques to efficiently cover the entire 28 GHz 5G band and exhibit low VSWR as well as minimal phase shift variation between the output ports. Yagi-Uda antennas are used to

demonstrate antenna arrays utilizing the designed power dividers.

The diplexers are designed using the filters for 5G NR bands and they exhibit low insertion loss, high stopband rejection, high selectivity, ease-of-integration in packages as well as small footprint. The diplexers are also integrated with couplers to emulate a power detection and control circuitry in a modern RF power amplifier (PA) FEM. The coupler covers the entire 5G mm-wave bands: from 24.25 GHz to 40 GHz. Using this integrated passive component block as an example, a system performance analysis using a co-simulation technique is presented to quantify the distortion in amplitude and phase produced by the fabricated passive component block. Moreover, the scalability of this approach to compare similar passive components based on their specifications and evaluation of their signature using a system-level performance metric such as error vector magnitude (EVM) is discussed.

For the fabrication of these passive components, semi-additive patterning (SAP) process is utilized using a glass substrate as a core. Unlike subtractive patterning process, where a thick copper foil is etched off from the undesired areas to form circuit patterns, SAP yields better dimensional and copper sidewall control. Finally, dimensional analysis is performed to find the discrepancy between desired and obtained feature dimensions. All of the demonstrated passive components have a footprint which is a fraction of the unit free-space wavelength of their operating frequencies. It is observed that the feature dimensions do not vary by more than 5%, resulting in an excellent model-to-hardware correlation of fabricated passive components. Thus, the superiority of glass based IPDs for RF FEMs is demonstrated.

CHAPTER 1

INTRODUCTION

1.1 What is 5G?

The pursuit of seamless global connectivity and the need to access boundless amount of data has driven advances in wireless networks to increase data rates and improve spectrum efficiency while reducing energy per bit as demand for data continues to grows exponentially. Fifth generation wireless network, abbreviated as 5G, is the new global telecommunications standard for RF networks beyond its predecessors: 4G, long term evolution (LTE) and LTE-Advanced (LTE-A) networks. This standard expands the scope of 4G and LTE from consumer-centric approach to a connectivity fabric that virtually includes everything: devices, machines and objects, by offering and enabling use-cases such as massive enhanced mobile broadband (eMBB), ultra-reliable low latency communication (URLLC) and massive machine type communication (mMTC). This standard is designed to reliably deliver multi-gigabit per second (Gbps) peak data rates, massive network capacity, ultra-low latency and high fidelity to give a uniform experience to its users. Moreover, the 5G standard expands its reach by utilizing available spectrum in millimeter-wave (mm-wave) frequency range in addition to utilizing and expanding the spectrum used by LTE-A below 7 GHz.

In this regard, 5G air interface is revolutionary as the focus is shifted from only providing higher data rates to the consumer to serve other applications covered by the three primary use-cases. The leap to realize 5G is considered equivalent to jumping from 1G to 4G in view of the advances promised by 5G wireless communication networks. That is why the term "new radio (NR)" is coined for 5G as it addresses and supports the use-cases required by the ever-growing demand of connected devices. It is estimated that over

World Population	6.3 Billion	6.8 Billion	7.2 Billion	7.6 Billion
Connected Devices	500 Million	12.5 Billion	25 Billion	50 Billion

Connected Devices Per Person	0.08	More connected devices than people	1.84	3.47	6.58

| 2003 | 2010 | 2015 | 2020 |
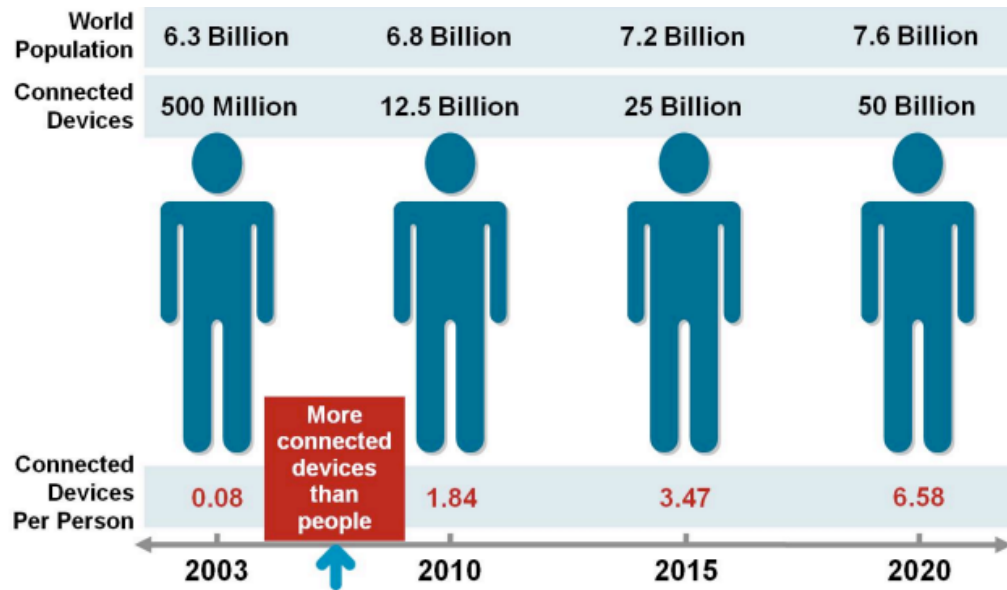
Figure 1.1: Projected number of connected devices.
(Source: Cisco)

50 billion devices will be connected to the wireless networks by the end of 2020 which requires high capacity networks with high fidelity. Unlike 4G and LTE, which are limited by the frequency range and technology to support such an enormous amount of connected devices, 5G promises massive communication networks to realize a world connecting not only humans through cell phones but sensors and other devices across the spectrum, as shown in Figure 1.1 [1]. From the economic standpoint, 5G will enable $13.2 trillion of global economic output with its value chain generating $3.6 trillion and supporting 22.3 million jobs as shown in Figure 1.2. Moreover, the investment in 5G and its deployment will result in sustainable long-term returns to global GDP in 2020-2035 [2].

1.1.1 Evolution of Wireless Networks

Wireless connectivity is established with a range of communication standards. Reliable connectivity is the foundation of mobile experience. Global system for mobile (GSM), wireless local area network (WLAN), infrared (IR), Bluetooth and global positioning system (GPS) are some of the traditional wireless connectivity networks.

It started with first generation (1G) cellular networks in the second half of 20th cen-
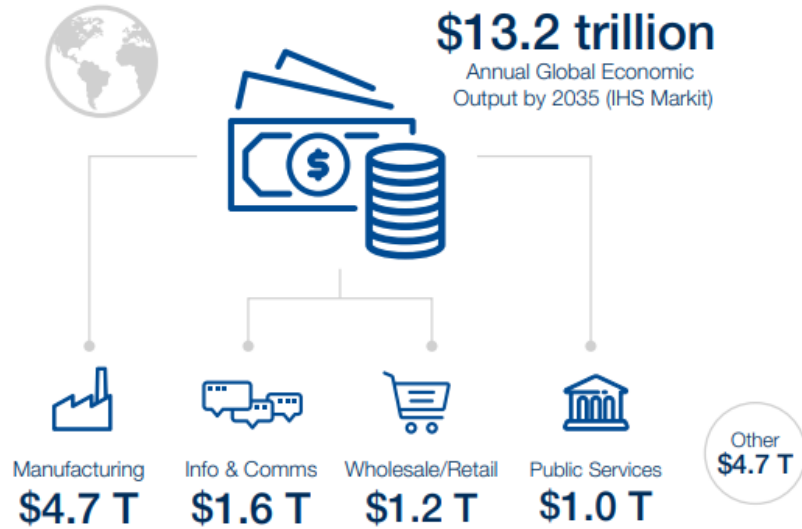
Figure 1.2: Projected socio-economic value of 5G [3].
(Source: World Economic Forum)

tury. Limitations in terms of high cost, poor coverage and low quality of service led to the second generation of mobile networks. The 2G standard was named GSM by ETSI and it had digital voice, improved coverage and capacity along with availability of text and multimedia messages using general packet radio service (GPRS). 2G evolved into EDGE (2.5G) where the data rate was doubled to 500 kbps and supported more than one user per channel by the use of time division multiple access (TDMA). Due to the scalability of 2.5G networks, it received much wider adoption and revolutionized the wireless network landscape. However, TDMA required large gaps in frequency to mitigate interference.

3G started in 2001, as the first packet-switched network utilizing code division multiple access (CDMA), four times as fast as 2G at the launch, with the aim to standardize network protocols between vendors. It included data along with voice and international roaming. Essentially, it was the start of wireless network of internet age where video calls, mobile TV and digital networking came into service and started to evolve continuously. The data rate increased significantly to support these services: up to 63 Mbps peak data rate for high speed packet access (HSPA) downlink three-carrier aggregation (CA) bands. With the advent of iPhone in 2007, the network capability was pushed to its limits. Finally, 4G
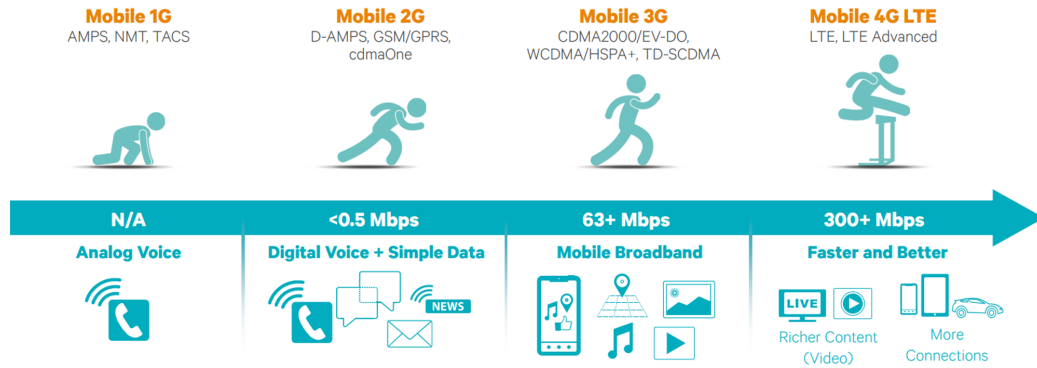
Figure 1.3: Evolution of mobile networks: 1G to 4G [4].
(Source: Qualcomm)

started in 2009 with the LTE standard to make high-quality video streaming a world-wide reality for consumers. The data rates jumped up to 300+ Mbps for LTE-A with 2x20 MHz downlink channels and continued to increase as more and more bands were licensed by FCC [4]. A total of 56 frequency division duplex (FDD) and time division duplex (TDD) are operating bands in 4G LTE [5]. Over 200 CA combinations of these bands are utilized to increase the speed for consumers with LTE. The summary of evolution of networks is depicted in Figure 1.3. Ten years after the advent of 4G, 5G is starting to become a reality despite the fact that 4G coverage is not ubiquitous. But 5G standard is not only built to provide blazing fast data rates of more than 20 Gbps, it is designed to realize the vision of IoT where billions of devices are connected and real-time communication with ultra-low latency (<1-ms) is the norm. In the US, low-band 5G using 600 MHz spectrum (band n71) was launched in December, 2019 and several 5G-enabled devices are available to early adopters [6–8].

1.1.2   Comparison of 4G/LTE/LTE-A and 5G

The main difference between current generation networks and 5G is that it supports new internet-of-things (IoT) and mission critical communication use-cases beyond the scope of simply improving data rate as is the case of current LTE network. Unlike LTE which is an evolutionary measure, 5G is revolutionary as it is an entire new network with a broad

range of applications and use-cases [9]. Some of the improvements in 5G in comparison to current LTE-A networks are listed in Table 1.1.

Table 1.1: Improvements in 5G Technology compared to LTE-A.

Parameter	5G	Improvement compared to LTE-A
Device/km^2	10^6 devices/km^2	10-100X
Latency	<1 ms	10X
Data Rate	10-20 Gbps	10-20X
Frequency Range	600 MHz to mm-Wave	600 MHz to 5.925 GHz
Channel Bandwidth	100 MHz for <7 GHz and 400 MHz for mm-wave	5X-20X

1.1.3   5G Frequency Range

The 3rd Generation Partnership Project (3GPP) unites seven telecommunications standard development organizational partners in six countries and provides their members with a stable environment to produce the reports and specifications that cover cellular telecommunications technologies. 3GPP has defined two frequency range designations: Frequency Range 1 (FR1) and Frequency Range 2 (FR2). FR1 covers low- and mid-frequency bands whereas FR2 is solely for mm-wave bands. The frequency range of FR1 and FR2 are defined below:

- FR1: 450 MHz - 6000 MHz (3GPP Rel. 15 V15.4.0 [10]), 410 MHz - 7125 MHz (3GPP Rel. 15 V15.5.0 [11])

- FR2: 24250 MHz - 52600 MHz

Till 3GPP Release 15 V15.4.0 [10], the maximum frequency range of FR1 was 6000 MHz hence the name "sub-6 GHz" became a norm but it was changed to 7125 MHz in

3GPP Release 15 v15.5.0. FR2 has remained the same till the latest report (3GPP Release 16 v16.3.0) [12]. The 5G spectrum is also defined as low-, mid- and high-bands. They are defined below:

- Low-band: <1 GHz

- Mid-band: sub-7 GHz (1 GHz - 7.125 GHz)

- High-band: mm-wave (above 24 GHz)

In the US, Federal Communications Commission (FCC) regulates the communications by radio, television, wire, satellite, and cable. FCC has its own categorization of 5G spectrum for low-, mid- and high-bands licensed in the US [13]. 5G mm-wave bands with their fractional bandwidths (FBW) are also listed below:

- n257: 26.5-29.5 GHz (FBW = 10.71%)

- n258: 24.25-27.5 GHz (FBW = 12.6%)

- n260: 37-40 GHz (FBW = 7.8%)

- n261: 27.5-28.35 (FBW = 3.04%)

1.1.4   Non-standalone vs. Standalone 5G

With the rapid need of 5G roll-out, two approaches to it are given by 3GPP: non-standalone (NSA) and standalone (SA). NSA is the early version of 5G NR as it uses LTE radio access network (RAN) and core with the addition of support for 5G low- and mid-bands (sub-7 GHz). This variant is for fast-to-launch approach favored by many carriers throughout the world. On the other hand, the long-term variant, SA has advantages in terms of simplicity and improved efficiency of 5G next gen core, lower costs, steady improvement of performance in the entire network while enabling URLLC and mMTC use-cases. To be precise,

SA gives 5G NR the ability of independent deployment as it is an end-to-end solution providing solid basis to unleash its full potential. However, it has multiple time-consuming and cost-demanding challenges associated with it such as building 5G infrastructure. A comparison of these two approaches to realizing 5G is shown in Figure 1.4 [14].
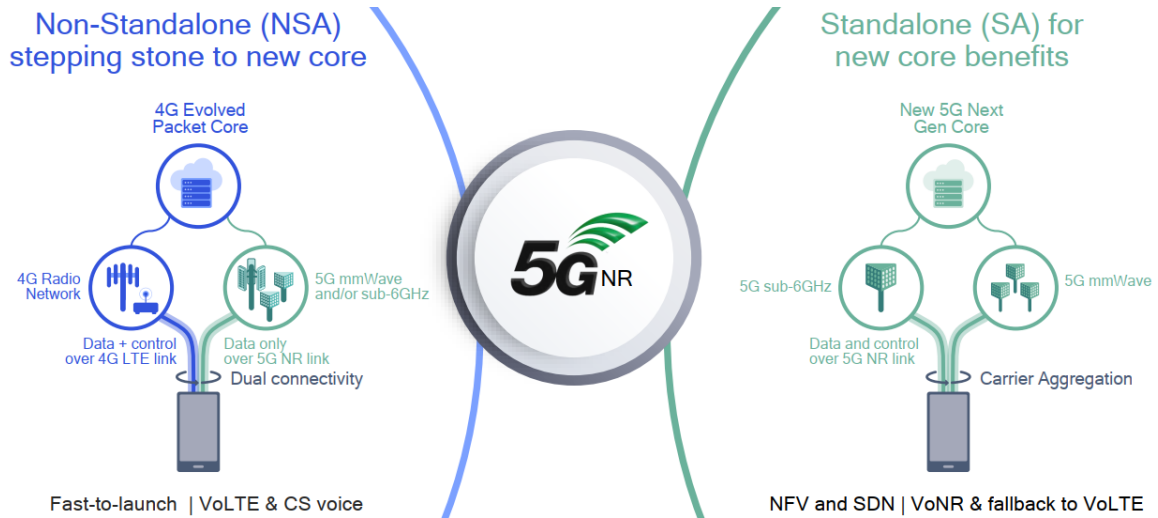
Figure 1.4: Non-standalone vs. standalone approach to realize 5G reality.
(Source: Qualcomm)

As an inference from the two methods to approach 5G, it can be asserted that NSA 5G requires more incremental improvements over its SA counterpart. In the context of FR2, the dynamics of system drivers shift towards pushing the envelope in an interdisciplinary fashion as the challenges span multiple fields requiring simultaneous innovation [15, 16]. This stems from the wide array of requirements for developing networks which can support mm-wave communication by normalizing advanced radio to support all of the use-cases of 5G.

1.1.5 5G Use-Cases

eMBB, URLLC and mMTC are the three use-cases of 5G air interface as shown in Figure 1.5. The focus of eMBB is to support the human-centric need of ever-increasing demand of higher data rates by increasing system capacity [17]. This is achieved by pushing the envelope of current limitations of the frequency spectrum, the primary being available band-
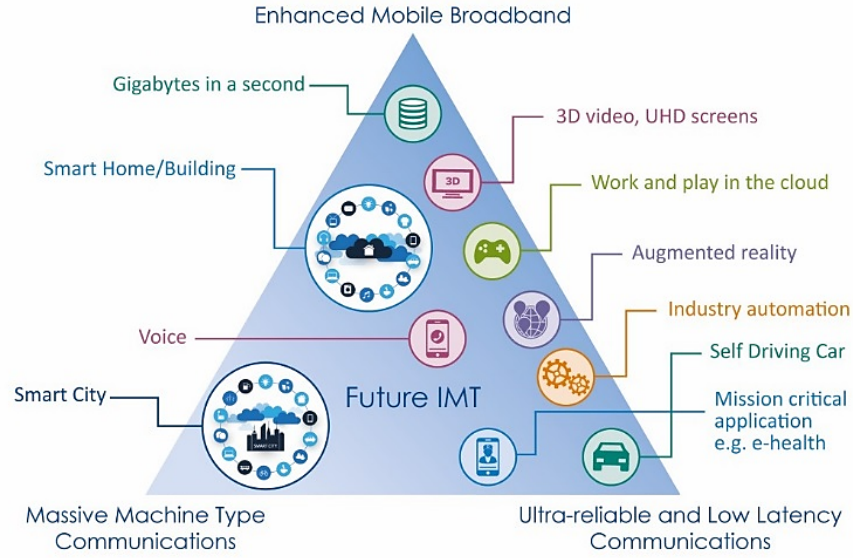
Figure 1.5: Three main use-cases of 5G.
(Source: 3GPP)

width. This limitation is overcome by licensing available bandwidth in sub-10 GHz range as well as opening up millimeter-wave (mm-wave) frequencies where wide bandwidth can be easily allocated. Antenna arrays with multiple antenna elements enable massive multiple input multiple output (MIMO) and beamforming, which multiplies the capacity of a network by exploiting multipath propagation. eMBB is the initial phase and face of 5G deployment and it is helping to develop modern broadband use-cases such as UltraHD and 360° streaming, and emerging AR/VR media and its applications [18].

The ability to process and harmonize various inputs for fast response falls under the domain of URLLC. It provides ultra-response connections with <1-ms latency and 99.9999% availability of connection along with support of high-speed mobility for mission critical services (MCS) [19]. Some of the use-cases of URLLC services include security, vehicle-to-vehicle (V2V) and vehicle-to-everything (V2X) applications, healthcare, utilities, cloud and real-time monitoring situations. The primary advantage of URLLC is not speed but its unfettered reliability to support robust and autonomous real-time decision making [20].

Finally, mMTC service targets robust and cost-sensitive connection of billions of de-

vices with long time availability and low power consumption. As the name suggests, is primarily for machine-to-machine (M2M) applications with negligible human interaction. This service takes into account IoT with low power consumption and low data rate for a large number of connected devices such as sensors with long range, low maintenance times [21, 22]. Essentially, mMTC entails a large mesh of low-cost, densely connected devices.

1.2 State-of-the-Art RF Front-End Module Packaging Technologies and Passive Components

The purpose of this section is to establish the critical role of miniaturized, high performance and integrated passive components for 5G and mm-wave applications.

Wireless communication systems have been key enablers for the ubiquity of smartphones and advancements in these systems will play a prominent role in realizing the true form of IoT, automotive electronics for vehicle-to vehicle (V2V) and vehicle-to-everything (V2X) connectivity for self-driving cars and seamless communication using a variety of communication standards for a range of applications. The massive number of devices to be connected along with the aforementioned applications have driven major breakthroughs in electronics and packaging innovation for multi-band multi-standard (MBMS) communications with GSM, WLAN, Bluetooth, 4G and LTE, GPS and mm-wave. All these technologies need to coexist in a single system while maintaining excellent quality of service (QoS). The major challenges in hardware design and development are in the advancing system-level integration technologies that could effectively integrate multiple standards of communication in parallel with meeting all the modern product quality standards. 5G wireless systems will use mm-wave frequencies as a means to provide blazing fast data rate in Gbps to the end-users in metropolitan areas. This goal translates to advancements in electronics for communication and requires higher density of integration than current technologies. Miniaturized, individual integrated components and modules with increased functional density, maximum electromagnetic isolation and reduced footprint are essential to

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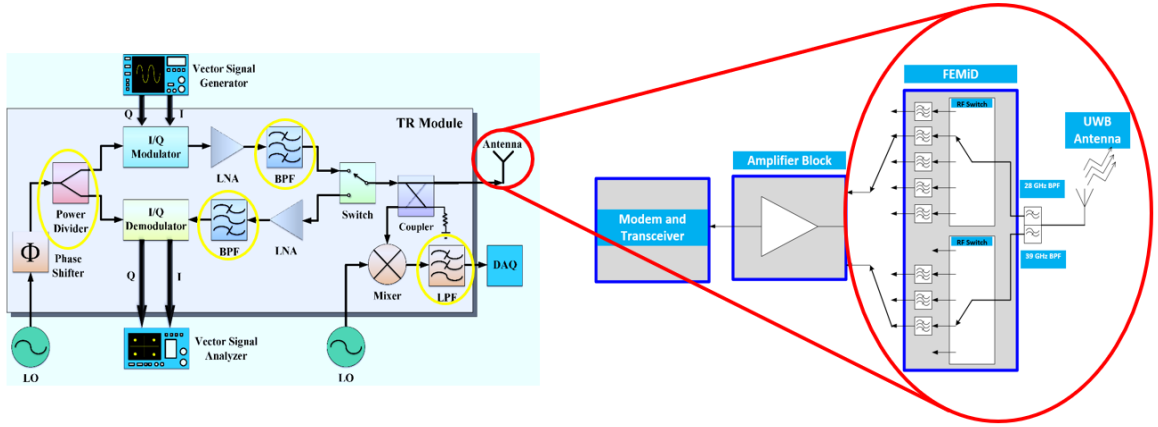
Figure 1.6: Block diagram of a typical 5G module with interconnected active and passive devices.

meet the growing demand for smart communication devices and systems for 5G networks, especially for mm-wave band infrastructure such as small-cells.

In modern RF modules, separately-packaged active and passive devices are interconnected to perform front-end modules (FEM) functionality. The discrete devices are assembled in their individual packages and then they are combined on substrates or printed circuit boards (PCB). A block diagram of a typical 5G RF FEM is shown in Figure 1.6. As the number of frequency bands been considerably increased for 4G LTE and continues to increase for 5G, the FEM has now transformed into FEM with integrated duplexer (FEMiD) with a filter bank connected with a switch, band-select filters and an ultra-wideband antenna.

Passive components play a key role in wireless system implementations as there is a need to provide matching impedances for components such as PAs and LNAs, filtering, tuning and biasing [23]. Passive components also make up functions such as couplers, baluns, power combiners and dividers, filters, phase shifters, circulators and isolators, and duplexers are usually paired with RF ICs for their nominal operation on the system level. It is typically estimated that passive components account for 90% of the component count, 80% of the size and 70% of the cost [24]. RF components have evolved significantly over time as technologies have advanced to achieve better electrical performance at high

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frequencies, especially at sub-7 GHz. RF passives in planar type show their advantages in high-frequency and wideband operation capability, flexibility as either discrete surface mount device (SMD) components or embedded passives in substrates, and low-cost manufacturability. They are typically implemented in the form of distributed circuits or discrete lumped elements. Distributed circuits are usually constructed by transmission lines and waveguides, and they tend to give high quality factors in microwave and mm-wave frequency range. Lumped elements are zero-dimensional, and they work exceptionally well at low RF frequencies such as below 10 GHz. Since the distributed components are proportional to wavelength, they are not recommended for cellular operations due to their large footprint requirements. They are widely used in applications which require high power and are not strictly limited by space.

Traditional RF passive components and substrates are based on low temperature cofired ceramics (LTCC) technology which involves fabrication with multiple layers of ceramic such as glass-alumina and a conductor such as copper. This technology has matured over the past few decades and is commonly used in industry for passive components and RF FEMs. Particularly for FEMs, LTCC is advantageous as it can provide functional density due to multiple layers by enabling complex signal and power delivery interconnections, and embedding of passive devices between the layers as depicted in Figure 1.7a and 1.7b. However, due to limitations in thickness reduction and scalability to panel-level, LTCC technology is subsequently taken over by multilayer organic laminate substrate technology. This has not completely outdated LTCC: as the substrate technologies have evolved, improvements have been made, giving rise to customized performance metrics, form-factors and design rules for specific passive components and module substrates.

Multilayered organic laminate-based packaging technologies proliferated due to their low-cost, ease-of-processing and large panel manufacturing. For 5G applications, antenna-in-package approach (AiP) is most sought out because the antenna array can be integrated in package rather than on board due to the small size of antenna at mm-wave frequencies.

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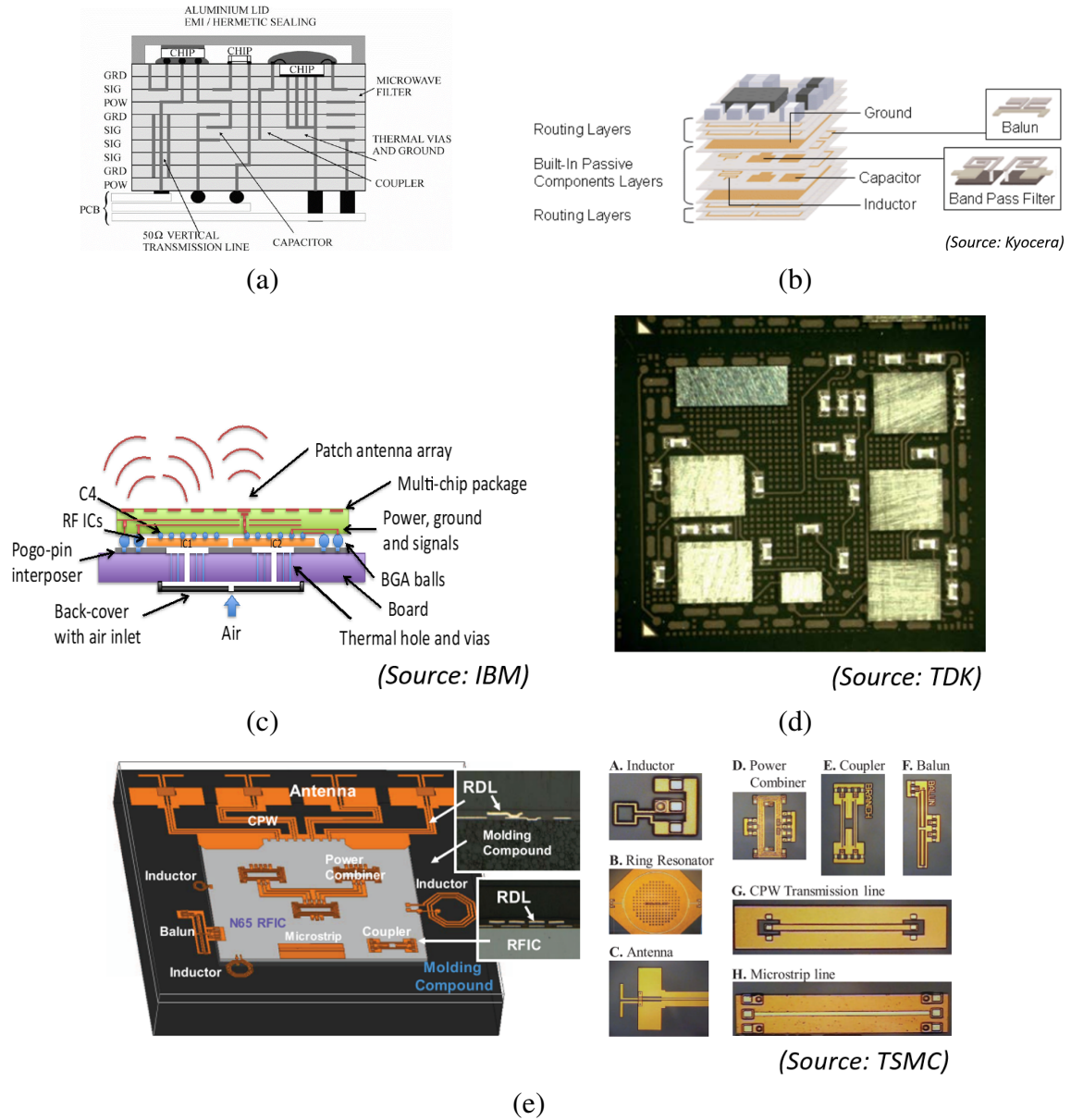
Figure 1.7: (a) An example cross-section of LTCC, (b) LTCC cross-section with embedded passives from Kyocera, (c) An example organic laminate AiP cross-section from IBM, (d) A multilayer multi-chip module organic laminate from TDK, and (e) mm-wave RF IC and passive components on InFO RDL.

A cross-section of an AiP is shown in Figure 1.7c. Another reason for popularity of organic laminates is the integration of multiple chips in the same package which increases functional density and performance while reducing cost. This approach is considered 2D if the ICs are assembled side-by-side as shown in Figure 1.7d [25]. However, the form-factor and performance limitations of organic laminates, particularly for 3D architectures, fall

short of meeting the miniaturization requirements for emerging electronics. This leads to the evolution of technologies to integrate passive components in the same package as their active counterparts. The passive components in this case are termed as integrated passive devices (IPDs). IPDs can be realized on LTCC substrates, organic laminates, silicon wafer and glass substrates. The complexity of integration brings new challenges in terms of performance, design, fabrication and miniaturization but given the functionality and footprint requirements of modern RF components and modules, industry as well as academia have invested in finding intelligent solutions to these challenges.

The ultimate goal of passive components is to serve active devices to provide system-level functionality. It is important to both miniaturize the passive components and to integrate them closer to the active devices to reduce interconnection parasitics. This has led to 3D and embedded modules in which the primary focus is to reduce form factor and shorten the interconnection length for improved electrical performance. Moreover, heterogeneous integration allows for complete integration of various devices and components in one package. The thickness of module is reduced by embedding active devices in substrates. Fan-out technologies have recently become mainstream either as wafer-level or panel-level packaging. Integrated fan-out (InFO) is a wafer-level packaging technology with low-loss dielectrics, fine-pitch and thick-copper redistribution layers (RDL). As shown in Figure 1.7e, several passive components such as inductors, ring resonators, antenna array, power combiner, coupler, balun and, microstrip and CPW transmission lines are integrated with an RF IC are demonstrated on InFO RDL [26]. Georgia Tech has advanced the concept of chip-first and chip-last approach, particularly the chip-last embedded and fan-out power and RF modules in which core and buildup layers are used to embed ICs in cavities, and interconnects and thin-film passive components are realized in RDL [27]. Figure 1.8 shows the evolution of RF packaging technologies for passive components [28].

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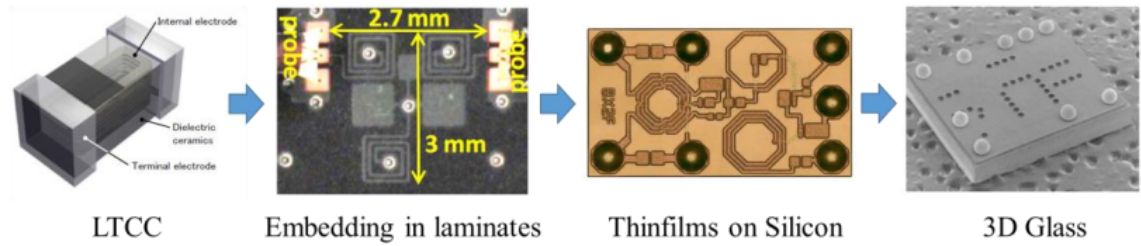
Figure 1.8: Evolution of RF passives.

1.3 Laminated Glass-based Passive Components

Glass is an ideal core material for mm-wave 5G modules and IPDs since it combines the benefits of ceramics for high-frequency electrical performance, laminates for large-area panel processing for low cost, and silicon for its dimensional stability and precision patterning, which is essential for mm-wave circuits. Some of the key features of glass substrate are:

1. Low-loss and high-resistivity.

2. Silicon-like dimensional stability.

3. Tailorable coefficient of thermal expansion (CTE) for improved reliability and warpage reduction.

4. Panel-level processing and manufacturing comparable to organic laminates.

5. Low-loss through-glass via (TGV) enabled double-side component integration.

This empowers the realization of compact and low loss passive components which can be either embedded as thin films into the package or prefabricated as standalone IPDs that can be embedded into a 3D module. A cross-section of a modern 5G module with broadband and/or end-fire antennas is shown in Figure 1.9. This stackup serves as the motivation for this research as its variations are used for demonstration of passive components.
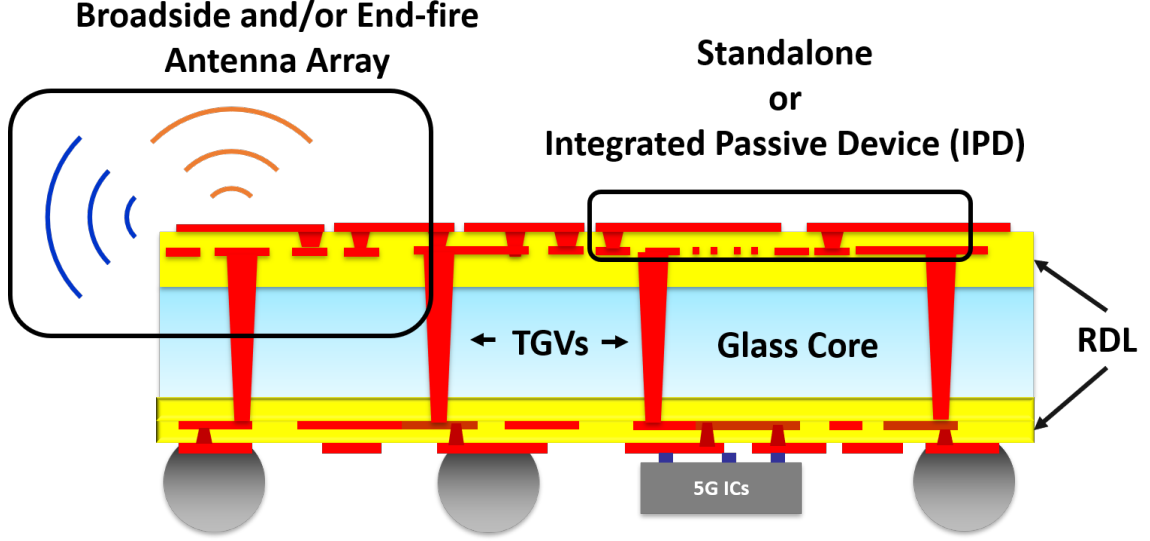
Figure 1.9: Cross-section of a state-of-the-art laminated glass-based 5G module with integrated active and passive components.

Heterogeneously integrated active and passive components along with high density layers for digital routing and low-loss, seamless interconnects are key features of this module. Traditionally, mm-wave components are designed on-chip to take advantage of tight process control. However, this can consume expensive IC real estate and also lead to high component insertion loss. Traditional package integration with thick components can lead to large interconnect loss and prevent design flexibility. Package integration with ultra-thin 3D architectures can address the limitations of both on-chip and off-chip approaches and it gives the best performance of both. Semi-additive patterning (SAP) process enables the realization of precision circuitry on ultra-thin materials such as glass and is superior

Table 1.2: Comparison of filter realization platforms.

Filter Platform	Insertion Loss	Interconnect Loss	Footprint	Thickness
On-Chip	4 dB	0.1 dB/mm	Very Small $(<4\lambda_0{}^2)$	Very Small $(<500\mu m)$
Traditional Off-Chip	2 dB	0.5 dB/mm	Small-Med. $(\sim4\lambda_0{}^2)$	Med.-Large $(\sim500\mu m)$
On-Package – 3D Module	2.5 dB	0.2 dB/mm	Very Small $(<4\lambda_0{}^2)$	Small $(<500\mu m)$

λ_0: Free-space wavelength

to conventional processes such as wet etching in which feature profile and dimensions are difficult to control when high precision (on the order of few micrometers) is required [29, 30]. For example, given the tight process control of processing RDL on glass, a comparison is drawn for filters realized as on-chip, off-chip and on-package in terms of insertion loss, interconnect loss, footprint and thickness of stackup as shown in Table 1.2. Laminated glass-based realization takes the best of other two approaches in terms of both performance and footprint.

1.4 Research Objectives, Challenges and Tasks

1.4.1 Research Objectives

The objective of the proposed research is to model, design, fabricate and characterize integrated passive components for 5G and mm-wave applications on advanced substrates, enabled by design and precise process of low-loss thin-film passives on laminated ultra-thin glass substrates for RF FEMs. The research objectives for filters, power dividers, diplexers and integrated passive components are given in Table 1.3.

The integration of passive components is an extension of this research in which two of the passive components: diplexers and couplers, are combined. They are also co-simulated with active components in a RF transmitter chain to analyze their performance in a system. In addition to the passive component integration, a co-simulation methodology is introduced and applied to characterize integrated passive components for 5G NR bands, to evaluate their system performance metric signature using higher-order modulation schemes and the scalability of this approach to compare various passive components for 5G and mm-wave applications is discussed. The selected modulation schemes are differential quadrature phase shift keying (DQPSK) and 64-state quadrature amplitude modulation (64-QAM). The latter modulation scheme is utilized very commonly in 4G LTE systems under low degradation channel conditions and is expected to be the used in early phases of 5G deployment. The performance of a digital communication system is typically

Table 1.3: Objectives, prior art and challenges in proposed research.

Topics	Metrics	Objectives	Prior Art	Challenges
Filters	Performance	• IL (in-band) < 2.6-dB • IL (out-of-band) > 30-dB • RL > 20-dB	• IL (in-band) < 4-dB • IL (out-of-band) > 20-dB RL > 15-dB	• High-Q resonators are required to achieve low insertion loss • Stopband attenuation objectives can append the need for additional notches to suppress harmonic responses • Trade-off between performance and footprint • Package-integrated design
	Miniaturization	• Footprint: < $2\lambda_0 \times 2\lambda_0$	• Footprint: > $2\lambda_0 \times 2\lambda_0$	
Power Dividers	Performance	• IL < 3.82-dB for two-way, < 5.57-dB for three-way, < 6.82-dB for four-way • RL > 20-dB	• Passband as high as 1.5-2 dB added insertion loss above theoretical	• Design power dividers to achieve required insertion loss. Optimize designs with design-for-fabrication considerations • Investigate designs on ultra-thin RDL (<50-μm) and implement techniques to maintain insertion loss over wide bandwidth • Package-integrated design
	Miniaturization	• Footprint: < $\lambda_0 \times \lambda_0$	• Footprint: > $\lambda_0 \times \lambda_0$	
Diplexers	Performance	• Filter Design: Doubly terminated • IL < 3-dB • RL > 15-dB	• Filter Design: Singly terminated	• Design doubly terminated filters and configure them as diplexers • Characterization of multi-port networks • Precise line/space features required for excellent model-to-hardware correlation
	Miniaturization	• Footprint: < $2\lambda_0 \times 2\lambda_0$	• Footprint: > $2\lambda_0 \times 2\lambda_0$	
Integrated Passive Components	System Performance Analysis	• EVM < 17.5% for QPSK • EVM < 8% for 64-QAM (Defined by 3GPP for 5G)	• Component-level EVM signatures for passive components are only evaluated at sub-6 GHz frequencies using lower order modulated schemes	• Extract EVM for the integrated passive component block in a RF transmitter chain. • Appropriate selection of active components and co-simulation methodology

IL: Insertion Loss (dB(S2,1))
RL: Return Loss (dB(S1,1))
λ_0: Free-space wavelength
EVM: Error Vector Magnitude

estimated with bit error rate (BER), signal-to-noise ratio (SNR) and error vector magnitude (EVM) [31]. The choice of system performance metric is EVM, which is the magnitude of difference between a complex transmitted data symbol and its ideal counterpart, defined by Equation (1.1) and depicted in Figure 1.10. The complex data symbol has an in-phase (I)
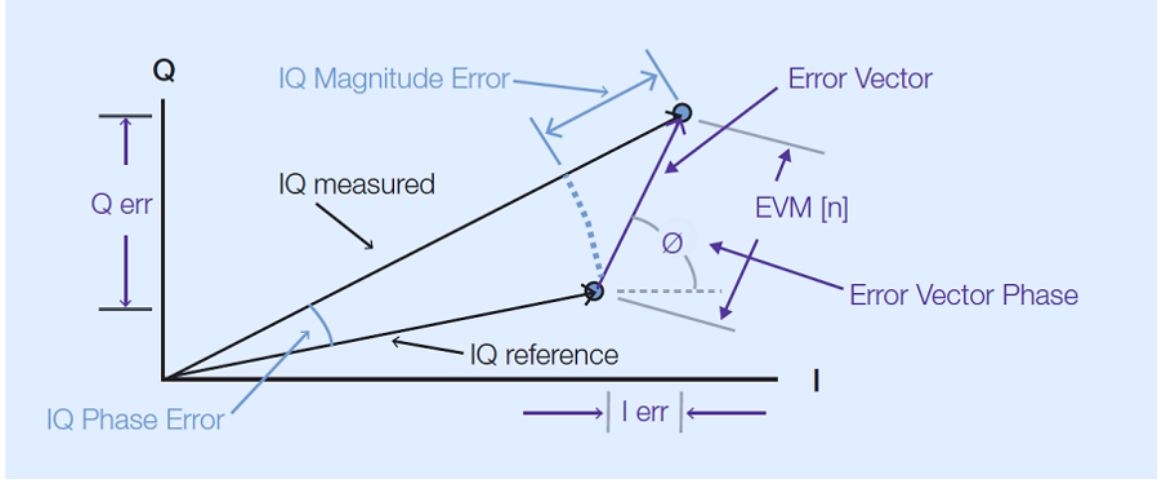
Figure 1.10: Visualization of EVM.
(Source: Keysight)

and a quadrature (Q) component. EVM is a figure of merit of modulation accuracy and is primarily a quantity of concern in link budget analysis of transceivers [32, 33]. 3GPP has defined EVM levels for 5G communications with various modulation schemes at different power levels [12, 34]. For QPSK and 64-QAM, EVM levels are defined as 17.5% and 8%, respectively.

$$EVM(\%) = \frac{\sqrt{\frac{1}{N} \sum_{0}^{N-1} I_{err}[n]^2 + Q_{err}[n]^2}}{Constellation\ Maximum} \tag{1.1}$$

where:

n = symbol index

N = number of symbols

$I_{err} = I_{Ref.} - I_{Meas.}$

$Q_{err} = Q_{Ref.} - Q_{Meas.}$

The frequency at which these passive components operate covers both 5G New Radio (NR) mm-wave bands:

- US 28 GHz (24.5-29.5 GHz), and

- EU 39 GHz (37.0-43.5 GHz)

Moreover, mm-wave specific 5G bands (n257, n258 and n260) are also a focus of this research.

1.4.2 Technical Challenges

Key challenges in electrical design and substrate fabrication need to be addressed to realize low loss and miniaturization targets for glass-based passive components.

Filters

The key performance metrics of filters are insertion loss, passband ripple, return loss, bandwidth, stopband attenuation, roll-off factor, group delay and repetition frequency of spurious passband. One of the common trade-offs in filter design is passband insertion loss vs. roll-off. The roll-off of a higher order filter will be sharp but at the cost of higher passband insertion loss. Moreover, a higher order filter will have a physically larger footprint. Therefore, a trade-off needs to be made between insertion loss, selectivity and footprint. The choice of transmission line: microstrip, stripling, coplanar waveguide (CPW) and conductor-backed CPW (CBCPW) for realizing planar filters also contributes to the insertion loss based on the Q-factor of resonator.

The current major limitation with 4G and LTE networks is the total usable fractional bandwidth (FBW). The same FBW at mm-wave frequencies provides much higher bandwidth, and thus, ability to provide the end-user with higher data-rates. This translates to increased complexity of electronics, which in turn, drives platform integration. One of the ongoing challenge of MBMS RF solutions for smart phones, essentially CA, requires the addition of more bands within the same physical space of user-equipment (UE) [35]. The requirement to use mm-waves for communications leads to complex filtering challenges such as low in-band insertion loss and high out-of-band rejection: a daunting task beyond 20 GHz. Small-cell FEMs will also deploy advanced filtering technologies to isolate the

communication bands from nearby interferers [36]. To address this issue, designers have resorted to either connecting standalone filters to one antenna accessed by a switch, often called a CA switch, or they resort to using multiplexers with very high Q filters [37, 38]. Another challenge is in the domain of optimal power levels for mm-wave frequencies for 5G and concerns regarding close proximity of mm-wave equipment with end-user. Models have been developed to present the efficacy of mm-wave bands and determine their path loss in typical scenarios [39, 40]. A filter performance related example is the trade-off of insertion loss in the passband when designing a filter. As evident in Figure 1.11, the insertion loss variation in-band is significant whereas return loss is more than 20-dB. In filter specifications, insertion loss needs to be uniform and it is often defined in conjunction with an acceptable ripple level. It is imperative to maintain low variation in insertion loss otherwise the frequency components of the signals passing through the filter will be attenuated differently causing distortion and signal-integrity issues.
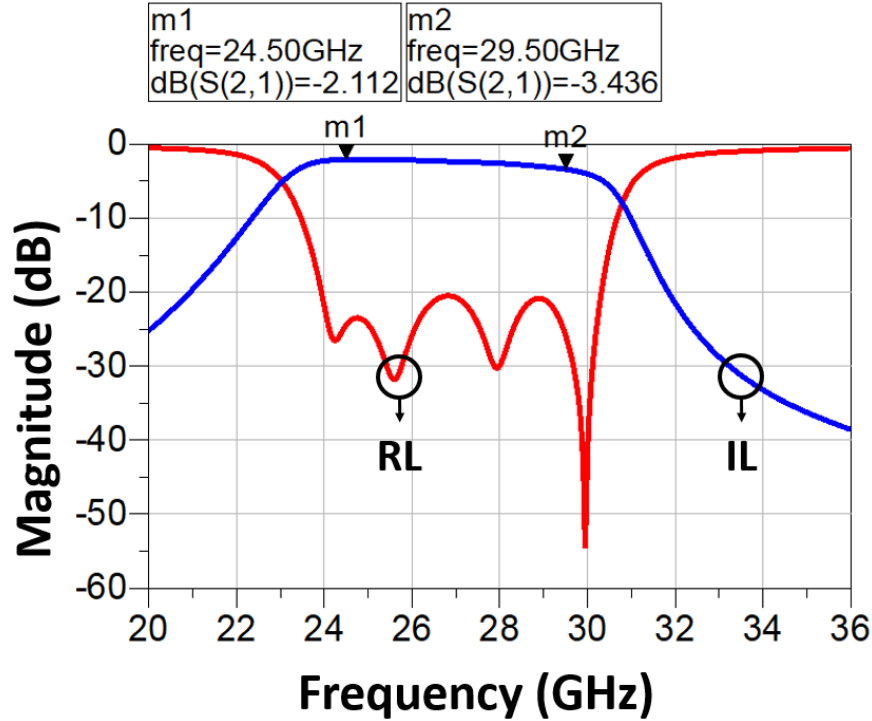
Figure 1.11: Challenges in design: A well-matched (RL >20-dB) 28 GHz band filter with significant variation in IL.

Similarly, infrastructure-side mm-wave FEMs, specifically in small-cells for short-range communication, require advancements in component design in terms of low cost, high performance and reliability. Sub-6 GHz communication filtering is dominated by acoustic wave technologies such as SAW and BAW filters [41]. However, these technologies do not scale to mm-wave frequencies and a new approach is required to design and fabricate high-performance filters for mm-wave bands of 5G communication systems. In addition to delivering higher performance, form-factor also governs the use of a particular filter in a specific application. Meeting the requirements of wide bandwidth, sharp-rejection and compact size is often subjected to certain trade-offs. For techniques involving coupled lines, the fabrication becomes challenging for wide bandwidth requirements due to stringent linespace requirements [42]. Also, process-induced variations can severely affect the filter response and all of them cannot be thoroughly modeled in simulations. For example, variations in linewidth affect can be induced due to various reasons as shown in Figure 1.12. Such variations can be mitigated by process optimization and by exercising process control measures.
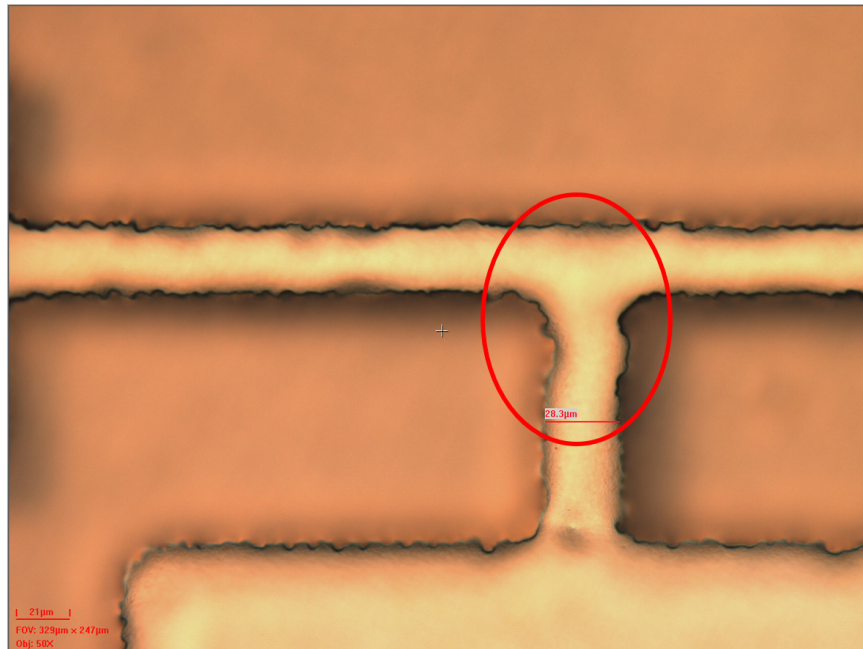
Figure 1.12: Process-induced variations in linewidth.

Power Dividers

The key electrical performance metrics of power dividers are added insertion loss, VSWR, split ratio, amplitude and phase balance as well as isolation and phase shift between the output ports. From the fabrication perspective, the power divider design needs to be flexible enough to accommodate the package requirements while maintaining excellent electrical performance. Due to higher free-space loss of mm-waves, high directivity and beam-steering of antennas becomes an inevitable requirement to enable a stronger and reliable wireless 5G connection. With the trend shifting towards package-integrated antennas, integrating a power dividing network with the antenna array in a package becomes extremely important as the power delivery to antennas operating at different bandwidths need to have minimal phase-shift [10]. Generally, power dividers can be integrated either in the same metal layer or in the metal layer underneath the antenna array, depending primarily upon the complexity of the system as well as the chosen structure for power divider. Typical structures are based on microstrip, CBCPW and stripline transmission lines [43].

One of the major challenges in demonstration of power dividers is to maintain constant, low added insertion loss over the entire operational bandwidth. The added insertion loss can be systematically reduced by using advanced materials and processes to maintain rectangular conductor profiles along with low surface roughness. For ultra-wideband operations, there are techniques in literature to maintain the insertion loss within a tight tolerance over multiple octaves of bandwidth [44]. Another challenge is the complexity of matching network between the input and output legs of the power dividers. Depending upon the split-ratio and bandwidth of operation, the complexity of matching network can increase.

Diplexers

The key performance metrics for diplexers are insertion loss, stopband attenuation return loss, cross-over point of filters and isolation between two bands. One of the challenges

in diplexer design comes from the frequency spacing between bands. Usually, singly-terminated filters (filters with characteristic impedance at one port and zero or infinite impedance at the other) are utilized to design both types of diplexers: contiguous and non-contiguous [45]. It is to be noted that singly-terminated filters cannot be characterized individually unlike doubly-terminated filters. Contiguous diplexers have both band filters intersecting at 3-dB passband insertion loss where non-contiguous diplexers have frequency-spaced bands and thus the cross-over point of filters is at a much higher insertion loss.

Doubly-terminated filters, on the other hand, have same characteristic impedance at both ports and they can be utilized to design non-contiguous diplexers using T-junction networks. This approach has some limitations as to what bandwidth filters are being combined to form a diplexer. Higher bandwidth filters can have mismatch and low isolation between bands due to the limited bandwidth characteristics of the designed T-junction. Another aspect is characterization of diplexers on two-port test equipment as they are three-port networks. This challenge will be addressed in detail in Chapter 4.

Integrated Passive Components

There are two primary challenges in integration of passive components. The first challenge is to characterize multiport networks with more than three ports and how this influences design stage. The second challenge is to evaluate system performance of the integrated passive component block when it is co-packaged with other active and passive components in an output power control circuitry in a RF transmitter chain. In addition to system performance, extracting the EVM signature of the passive component block using various higher-order modulation schemes requires appropriate selection of active and passive devices in the RF chain. Moreover, relating component parameters such as the bandwidth, ripple and roll-off factor of a filter, to a system performance metric such as EVM is a challenging task [46]. Finally, the approach needs to be scalable to give system architects the

ability to discriminate between various passive components.

<u>1.4.3 Research Tasks</u>

The common research tasks to address challenges in filters, power dividers and diplexers are: 1) to incorporate design-for-fabrication and design-for-characterization considerations in the design phase, 2) to develop and optimize the fabrication process of precision redistribution layers on ultra-thin laminated glass substrates with 100-μm thickness, and 3) to perform a model-to-hardware correlation study to identify potential design improvements and mitigation of process-induced variations to obtain excellent correlation between simulated and measured results.

Filters

The research tasks to address challenges in filter design and demonstration are given in Table 1.4. From the design perspective, the objective is to focus on high performance filter design by evaluating various high-Q resonator structures to obtain lower insertion loss and high out-of-band rejection. The focus will be on lowpass filter (LPF) and bandpass filter

Table 1.4: Research tasks to address challenges in demonstration of filters.

Topics	Metrics	Objectives	Challenges	Tasks
Filters	Performance	• IL (in-band) < 2.6-dB • IL (out-of-band) > 30-dB • RL > 20-dB	• High-Q resonators are required to achieve low insertion loss • Stopband attenuation objectives can append the need for additional notches to suppress harmonic responses • Trade-off between performance and footprint • Package-integrated design	• Design filters to achieve lower in-band insertion loss and higher out-of-band rejection using advanced structures and high-Q resonators • Achieve optimum trade-off between filter performance and footprint in simulation. Optimize for package integration • Fabricate and characterize filters to perform model-to-hardware correlation study
	Miniaturization	• Footprint: < $2\lambda_0 \times 2\lambda_0$		

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(BPF) structures. To address the trade-off of electrical performance vs. footprint, several thin-film polymer dielectrics are evaluated based on their electrical properties as well as processability and the one which features excellent electrical performance with process compatibility is selected for this demonstration.

Power Dividers

The research tasks to address challenges in power divider design and demonstration are given in Table 1.5. One of the tasks for demonstration of power dividers is to evaluate high performance RDL with $<50\text{-}\mu$m thickness to miniaturize the power dividers. However, this miniaturization is limited by the distance between arms of power divider as they are designed to be configured as antenna arrays using Yagi-Uda antenna elements for 28 GHz 5G mm-wave band. This leads to focus on achieving optimum trade-off between performance and footprint of power dividers as well as corresponding antenna arrays.

Table 1.5: Research tasks to address challenges in demonstration of power dividers.

Topics	Metrics	Objectives	Challenges	Tasks
Power Dividers	Performance	• IL: < 3.82-dB for two-way, < 5.57-dB for three-way, < 6.82-dB for four-way • RL > 20-dB	• Passband as high as 1.5-2 dB added insertion loss above theoretical • Optimize power dividers for antenna arrays • Package-integrated design	• Design power dividers to achieve low added insertion loss. Investigate designs on ultra-thin RDL (<50 µm) and implement techniques to maintain insertion loss over wide bandwidth • Fabricate and characterize splitters and combiners as standalone components and as antenna arrays. Optimize for package integration • Achieve optimum tradeoff between process capability, footprint and performance
	Miniaturization	• Footprint $< \lambda_0 \times \lambda_0$		

Table 1.6: Research tasks to address challenges in demonstration of diplexers.

Topics	Metrics	Objectives	Challenges	Tasks
Diplexers	Performance	• Filter design: doubly terminated • IL < 3-dB • RL > 20-dB • Isolation > 40-dB	• Filter design: singly terminated • Minimize loading effect of filters on each other when configured as a diplexer	• Design doubly terminated filters and configure them as diplexers • Characterization of multi-port networks • Precise line/space features required for excellent model-to-hardware correlation
	Miniaturization	• Footprint: $< 2\lambda_0 \times 2\lambda_0$		

Diplexers

The research tasks to address challenges in diplexer design and demonstration are given in Table 1.6. These diplexers cover 5G NR bands n257, n258 and 260. For the design of non-contiguous diplexers, doubly terminated filters are to utilized and they are combined using T-junctions. The design of T-junction is critical as a properly designed structure can isolate both filters significantly, that is, it reduces the loading effect of filters on each other, while adding very low insertion loss to the individual bands. The characterization of three-port diplexers such as diplexers also requires planning in the design phase if the characterization equipment is limited to two-ports.

Integrated Passive Components

The research tasks to address challenges in intergrated passive component design and demonstration are given in Table 1.7. A five port network is designed: diplexer covering bands n257 and n260, and a coupler covering the entirety of 5G NR bands are integrated and characterized. Using the characterization results of this block, a co-simulation is setup to evaluate the performance of integrated passive component block using higher order modulation schemes and to extract its EVM signature.

Table 1.7: Research tasks to address challenges in demonstration of integrated passive components.

Topics	Metrics	Objectives	Challenges	Tasks
Integrated Passive Components	System Performance Analysis	• EVM < 17.5% for QPSK • EVM < 8% for 64-QAM (Defined by 3GPP for 5G)	• Component-level EVM signatures for passive components are only evaluated at sub-6 GHz frequencies using lower order modulated schemes	• Extract EVM for the integrated passive component block in a RF transmitter chain. • Appropriate selection of active components and co-simulation methodology

1.5 Organization of Dissertation

The proposed research tasks are carried out with details presented in the following chapters: Chapter 2 summarizes the literature survey of RF passive component technologies with focus on filters, power dividers and antenna arrays. Chapter 3 describes the design and demonstration of the aforementioned passive components. Chapter 4 covers the design and demonstration of diplexers, integrated passive components and their system-level performance analysis. Finally, research summary, novelty of research and suggestions for future work are compiled in Chapter 5.

CHAPTER 2

LITERATURE REVIEW

This chapter reviews various building block technologies for 5G applications, with focus on passive components. A typical 5G system along with its components is briefly discussed, followed by a review of key technological advances in transistors, interconnects, antennas and passives. The significance of passive components in such a system is presented through several examples from current and emerging technologies.

A highly-integrated 5G substrate system architecture along with traditional discrete module is shown in Figure 2.1. Following system components are an integral part of a 5G substrate system:

- Systems: Integrated Circuits (ICs)

- Transmission Lines

- Interconnects
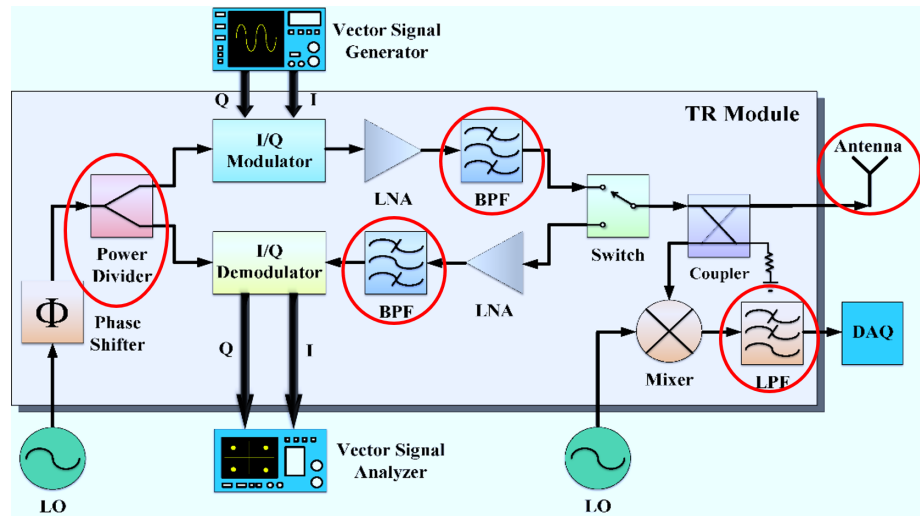
Figure 2.1: Microwave/mm-wave transceiver system for 5G with highlighted passive components.

- Passives: RLC, Filters, Power Dividers, Couplers, Baluns etc.

The key advances in these system components are briefly reviewed in the following sections.

2.1 5G Components and Systems

A conceptual 5G substrate system is depicted in Figure 2.2 along with its cross-section. The system has parts ranging from individual components such as resistors, filters to ICs which are wire-bonded or assembled in a flip-chip configuration on the package.

Each of these components serve a unique purpose: active components aid in amplifying a weak signal and antennas help in transmitting and receiving radio signals for processing. The system components are discussed in the following section. However, this research work is primarily focused on passive components for 5G and mm-wave applications and thus those components are presented in detail.
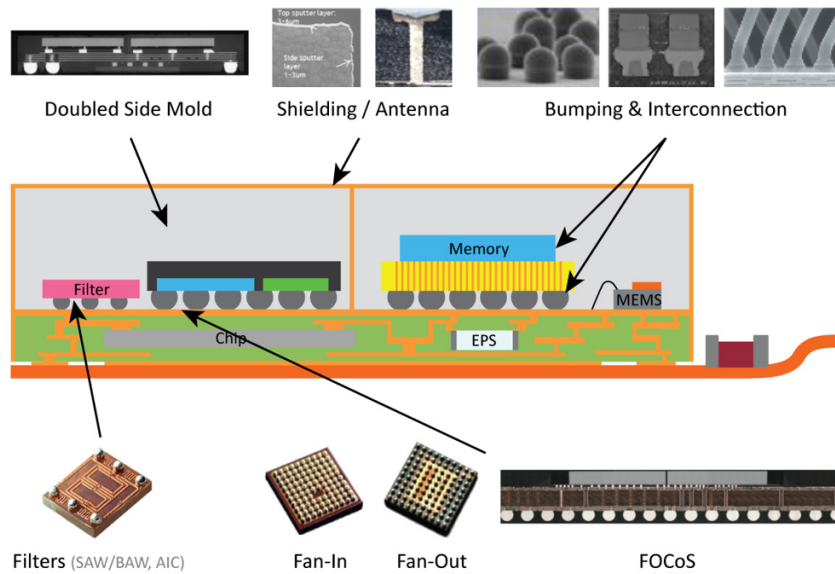
Figure 2.2: Conceptual 5G substrate system with prominent subsystems and components.

2.1.1   Integrated Circuits (ICs)

Several advanced transistor technologies come into play for mm-wave applications and are thus suitable options for 5G systems. The majority of mm-wave circuits have been implemented in Indium Phosphide (InP)-based or Gallium Arsenide (GaAs)-based transistor technologies. High Electron Mobility Transistors (HEMTs) have been historically used for high-speed applications because of their relatively higher current gain cut-off frequency and maximum oscillation frequency. In recent years, InP-based heterojunction bipolar transistors (HBTs) are developed to deliver superior performance to any other transistors. However, Silicon Germanium (SiGe) and BiCMOS (bipolar junction transistor and CMOS transistor integrated in a single device) have the ability to integrate high degree of functionality in a single chip and are thus considered as alternatives to InP-based transistors for mm-wave markets [47, 48]. After the year 2000, silicon-based technologies gradually took over GaAs-technologies. This is because they have much better integration capabilities as compared to GaAs. It is easier to integrate the baseband digital circuits into a single chip with mm-wave circuits in Si-based technologies rather than that in GaAs-based technologies [49]. Infineon technologies has proposed a SiGe BiCMOS for automotive radar solutions in 76-81 GHz [50]. This radar is based on Monolithic Microwave Integrated Circuit (MMIC) technology. Better performance of the SiGe HBTs is needed to improve performance as this technology has cutoff frequencies in the range of 200-300 GHz, which is only a factor of 3 higher than the application frequency, resulting in lower margin for RF design. Infineon's SiGe BiCMOS technology can improve the RF performance and address the limitations in SiGe HBTs.

Systems with 5G standards have been challenging leading device companies to mass-produce low-cost ICs. Qualcomm, a leading organization in the world of communication electronics, recently announced its 28 GHz 5G Chip [51]. It is a modem operating at 28 GHz and will be used for testing pre-standard 5G cellular trials by Verizon and Korea Telecom. This indicates the roll-out speed of some vendors to push 5G standard even

closer in time. The Snapdragon X50 has the capability to deliver 5 gigabits per second (Gbps) downlinks and multiple gigabit uplinks for mobile and fixed-wireless networks. It also has a separate LTE connection as an anchor for control signals, whereas the 28 GHz link can deliver higher data rates over tens to hundreds of meters. It features eight 100 MHz channels, a 2×2 MIMO antenna array, adaptive beamforming techniques and 64-QAM to achieve a 90-dB link budget. It is compatible with other Qualcomm chips such as SDR05x mm-wave transceiver and PMX50 power management chip. These transceivers have evolved over time to achieve higher data rates and excellent power management. With the advancements in technology, most of the supporting passives are also included in ICs to save package real-estate and utilize it for some other purpose such as heat management or to increase density of components on it. This brings a very interesting perspective in the 5G substrates domain. Since the integration at circuit level is advancing with components being moved from package to IC itself, the main purpose of package has moved from supporting external components to provide high fidelity and low-loss interconnects to effectively route IOs of the IC.

2.1.2   Transmission Lines

For 5G packages, typical transmission lines such as microstrip, stripline and conductor-backed coplanar waveguide (CBCPW) are common. Stripline is usually avoided due to its higher loss. CBCPW and its ground-less variant, CPW, are profusely deployed due to their inherent shielding features and comparative losses to that of a microstrip transmission line. The cross-sections of these transmission lines are shown in Figure 2.3. In case of multilayered packages with less or no shielding between the layers, CPW is the line of choice. Usually, high-power signals in the system are routed through CBCPW lines to avoid any coupling with adjacent lines and compromising the signal integrity.

Above 30 GHz and at mm-wave frequencies, microstrip suffers from increased radiation loss and problems with spurious propagation modes which are undesired to maintain

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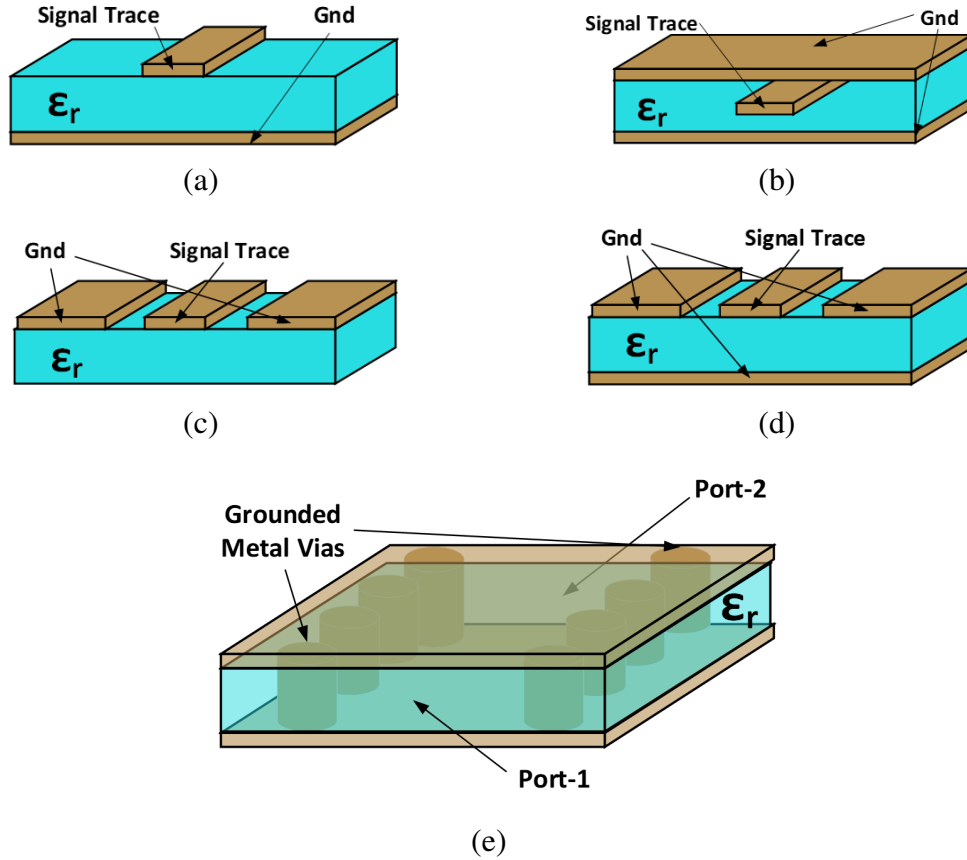
Figure 2.3: Different types of transmission Lines (a) Microstrip (b) Stripline (c) CPW (d) CBCPW (e) SIW.

signal integrity. Often, the designers choose to transition from microstrip to CBCPW as soon as physically possible to avoid radiation loss and benefit from minimal spurious mode propagation. Another advantage of using microstrip and CBCPW is their exposure which helps in assembling SMDs on them. These transmission lines also provide ease of testing along with lower fabrication cost.

Striplines become unattractive due to its small dimensions, higher losses and difficulty in routing using vias. Moreover, it is difficult to fabricate as compared to microstrip and CPW, and usually avoided at mm-wave frequencies. Achieving close-to-ideal transitions from stripline to coaxial or any other transmission line is also a challenge. However, stripline is not a lost art as it can be used at mm-wave frequencies when paired with the appropriate materials. Suspended Stripline structures can be a suitable option for two-layered

substrate systems but it has limited applications in 5G systems.

Substrate Integrated Waveguide (SIW) is an embedded waveguide within a substrate. Essentially, it is a dielectric-filled rectangular waveguide with reduced height, leading to thinner substrates. The side-walls of this waveguide are created with arrays of plated via holes. It is shown in Figure 2.3e. This makes it a very attractive option for passive devices and signal routing, given that it is less costly to fabricate. Moreover, it has the same characteristics as a conventional rectangular waveguide. SIW is a relatively new transmission line as compared to its counterparts and many innovative techniques to develop passive components using it have been published, especially filters because of its inherent structural flexibility in coupling design and topological arrangement [52].

2.1.3 Device-to-Package Interconnections

Interconnects serve as streets and highways of the IC, connecting external elements to the IC and interfacing it with the outside world. Interconnect design can vary depending upon the complexity of the IC. For 5G and mm-wave, interconnects need to be ultra-small, low-loss and should be cost effective to be commercialized in a fabrication process. Fabricating these intricate structures, interconnects and adjoining vias, is one of the most process-intensive and cost-sensitive portions of chip manufacturing. A few interconnect types are shown in Figure 2.4.

Since the interconnect length is comparable to the wavelength of the operating system at mm-wave frequencies, parasitics becomes a serious concern. This drives the designers to opt for even shorter transmission distance to reduce the loss other than on PCB or cable-connected board. Interconnects from chip to antenna feeding line is demonstrated to have 0.7-dB loss in a study by Tsai *et al.* [53]. This study revolves around a 4×4 antenna array integrated with RF chip using integrated fan-out wafer level packaging (InFO-WLP) technology. The array operates in 57-64 GHz range with a 11.6% fractional bandwidth and boasts a gain of 14.7-dBi in a small form factor of $10 \times 10 \times 0.5$ mm^3. Interconnect
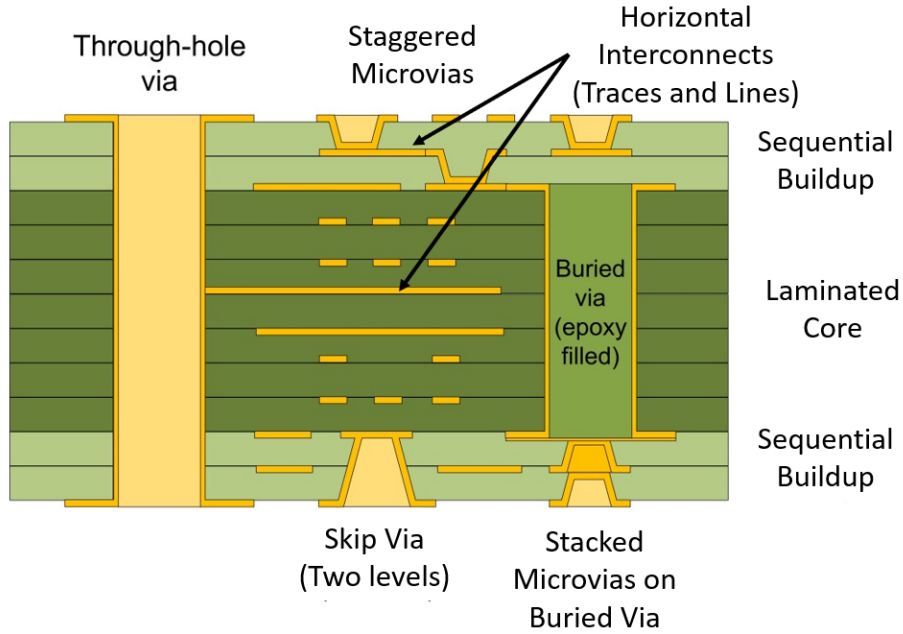
Figure 2.4: Types of interconnection technologies.

loss study is also performed using a 1600-μm long CPW transmission line. This loss is compared with chip pad to antenna port through C4 bump on LTCC substrate and though solder balls on LTCC substrates. In these cases, the loss is 1.6-dB and 4.9-dB, respectively, at 60 GHz. This can save 19% higher power amplifier output power compared with that of a flip-chip package. The insertion loss of these interconnect types is graphically shown in Figure 2.5.

Various types of interconnect techniques are depicted in Figure 2.6. These techniques have evolved over time with the advancements in microelectronics. The most popular techniques for 5G applications are fan-out, ball-grid array (BGA) and their variants. Wire-bonding is a very popular technique for RF applications to connect a die to its lead-frame but it has several limitations at mm-wave frequencies, of which increased loss and higher coupling are the prominent ones. Fan-out and its variants have become popular in the recent years due to their substrate thinness, lowest parasitics, ease of fabrication, low cost, scalability for high integration level and greater number of interconnections. It provides a smaller package footprint with higher IOs along with improved thermal and electrical
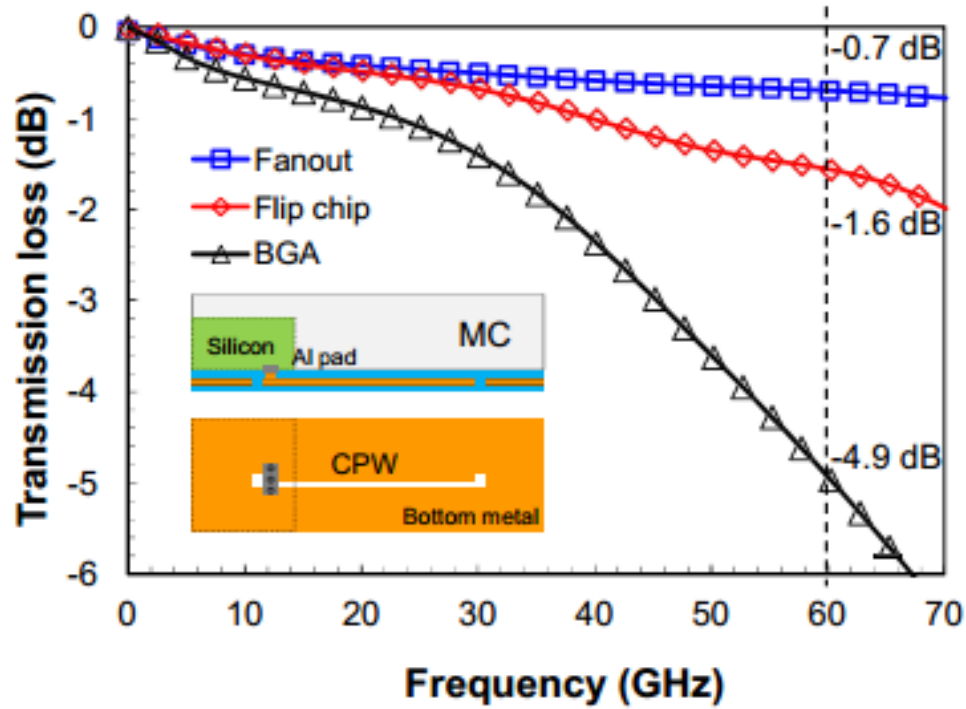
Figure 2.5: Transmission loss in fan-out, flip-chip and BGA interconnect structures.
(Source: C.H Tsai et. al. TSMC Ltd.)

performance. It takes individual die and embeds them in a low-cost material such as epoxy mold compound with space allocated between each die for additional IOs, avoiding the use of relatively expensive real estate of the substrate.

2.1.4   Passive Components and Devices

Passive components such as resistors, capacitors and inductors are universally found in every electronic device. Initially, larger size through-hole passive components were used in circuit boards but with the advancement in technology to using higher frequencies for circuits, passive components have evolved as well. Once the operating wavelength of the system becomes comparable to size of the components, several parasitics come into play. A resistor might depict capacitive properties due to its enclosure, causing unnecessary capacitance in the system. To avoid these parasitics, component size is made smaller than $\lambda/10$ of the operating frequency. Since the components at RF frequencies (upto 20 GHz) are
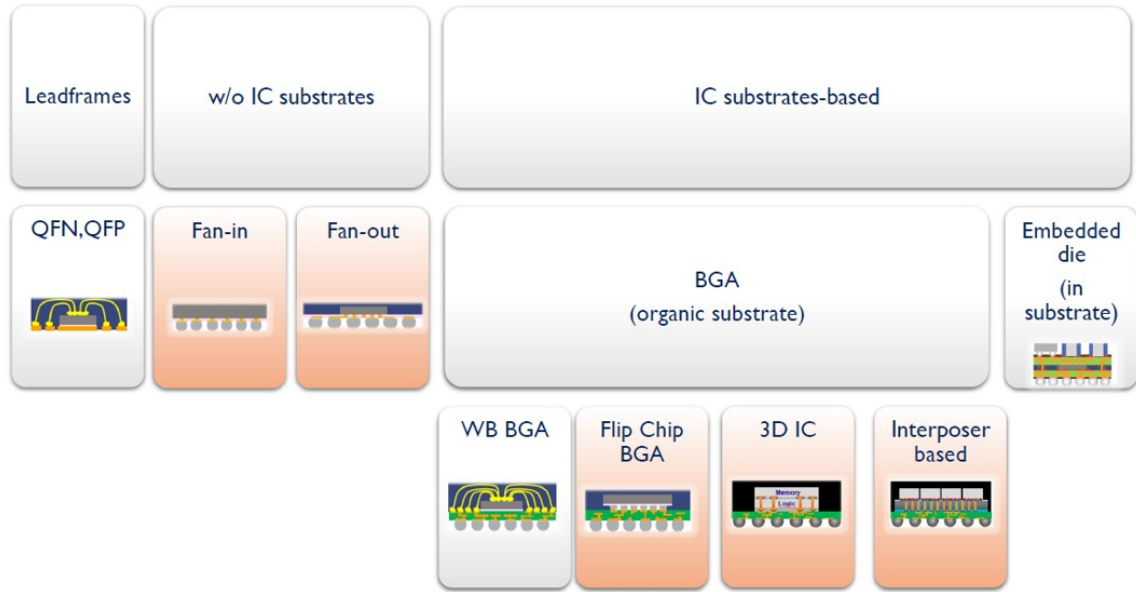
Figure 2.6: Types of fan-out packages.

very small, through-hole technology is no longer suitable for them. Surface Mount Technology (SMT) is the method of producing electronic components in which the components are directly mounted onto the surface of PCBs. The passive SMT components fall in the category of surface mount devices (SMDs).

The process of reflow soldering is used to mount SMDs on a PCB. Since SMDs are suitable for high-volume production at a low cost, they are very popular among PCB designers as the cost of assembly also decreases with the increased production volume of these devices. At mm-wave frequencies, even SMT falls short as the parasitics overwhelm the actual properties of the component. A capacitor can behave as an inductor at higher operating frequencies. At mm-wave frequencies, usually passive components are realized using active devices such as a diode-connected transistor acting as a resistor. Another approach is embedded passives where the passive components are made using conductor patterns and are embedded in a multilayered package. Figure 2.7 depicts the concept of embedded passives for a LTCC package.

Embedded passives have the following advantages [44]:

ALUMINIUM LID
EMI / HERMETIC SEALING

CHIP   CHIP

CHIP

GRD
SIG   MICROWAVE
POW   FILTER
GRD
SIG
SIG   THERMAL VIAS
SIG   AND GROUND
GRD
POW   COUPLER

PCB

50Ω VERTICAL
TRANSMISSION LINE   CAPACITOR
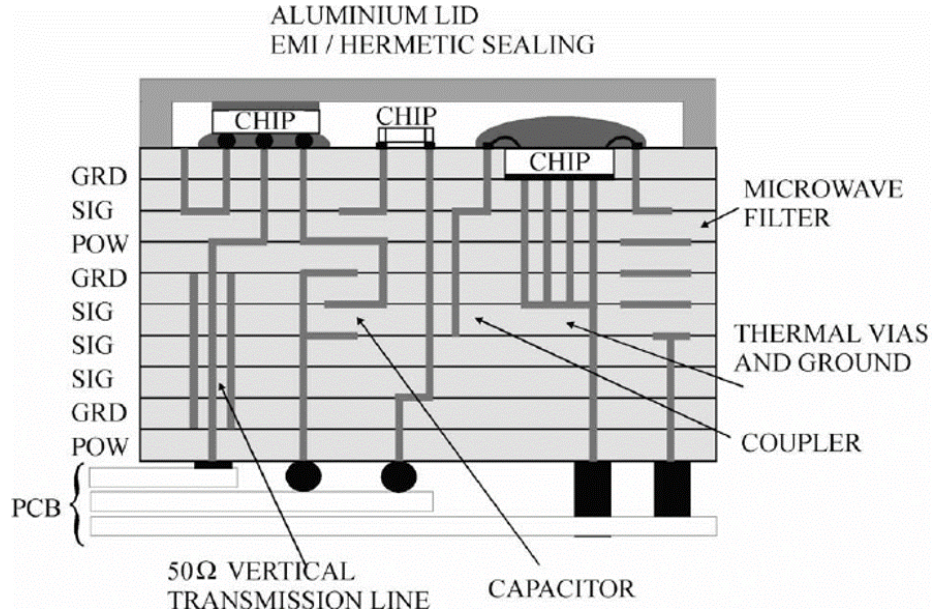
Figure 2.7: LTCC cross-section as an illustration of embedded passives.

- Increased circuit density by saving real-estate on the substrate.

- Decreased product weight.

- Improved electrical properties through additional termination and filtering opportunities, and shortening electrical connections.

- Cost reduction through increased manufacturing automation.

- Increased product quality through elimination of incorrectly attached devices.

- Improved reliability through the elimination of solder joints.

Embedded passives, however, have a disadvantage in terms of the quality factor of the component, which is mathematically defined as:

$$Q = \frac{f_r}{\Delta f} \tag{2.1}$$

where f_r is the resonant frequency and Δf is the resonance width or bandwidth of the system. An ideal passive component has infinite Q-factor.

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Embedded passives, especially inductors, suffer from poor Q-factor at RF frequencies and, therefore, are avoided by circuit designers when frequency of operation is over 20 GHz. Capacitors, on the other hand, can be embedded and made to have higher Q-factor. Typical embedded capacitor structure is of a parallel-plate capacitor. As shown in Figure 2.7, embedded passives not only refers to resistors, capacitors or inductors, but also transmission lines, filters, couplers and others.

Tong *et al.* of PRC Georgia Tech have reported SIW in glass interposers using through-package-vias (TPVs) [54]. The SIW was designed at an operating frequency of 20 GHz with a 100% fractional bandwidth and 0.67 dB/cm insertion loss on a 130-μm glass. The diameter of vias, denoted by d, is set at 120-μm. The study also showed that the insertion loss in dB/cm decreases with increasing substrate height as shown in Figure 2.8. Moreover, insertion loss variation of less than 1% is observed when via pitch was changed from 100 to 480-μm, indicating that radiation loss in minimized due to the relatively small via diameter. This study indicates that glass is a potential substrate for mm-wave systems.

2.1.5   Discrete Lumped Components and Circuits

The evolution of passive components started with low temperature co-fired ceramic (LTCC), which became very popular as the surface mount technology (SMT) components for resistors, inductors and capacitors. These SMD components are adapted due to their electrical performance, small-footprint, low tolerance and ease-of-use. As technologies evolved, their operation at higher frequencies (upto 10 GHz) also became possible due to reduction in parasitic effects by physical design. To date, passive SMDs are the most commonly found components in electronic systems. Thick- and thin-film technologies have revolutionized the chip passive component market by enabling a wide variety of high-precision, low-tolerance and low-cost components. A comparison of five different substrate technologies for passive components in terms of performance, thickness, size and some other parameters is given in Figure 2.9 [28]. As the substrate technologies have evolved, improvements
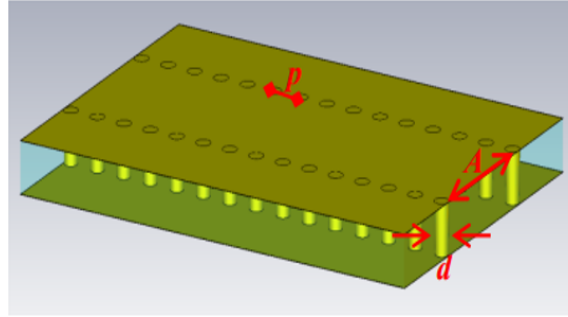
(a)
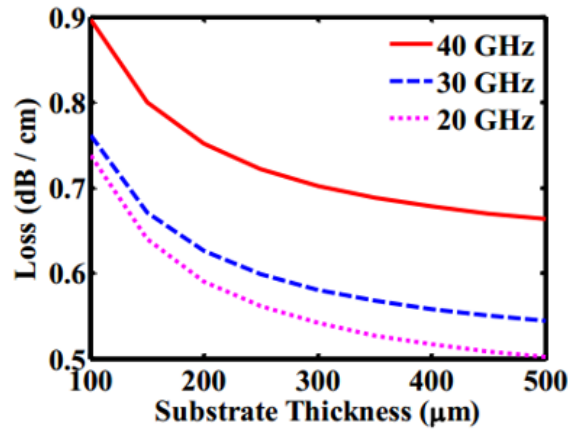
(b)

Figure 2.8: (a) Designed SIW (b) Loss in dB/mm vs. substrate thickness.

have been made in each performance metric giving rise to differences in use-cases of each substrate technology for passive components.

Over the past few decades, several theoretical advancements have been made in de-

	LTCC	Laminate	Silicon	Acoustic Wave	3D Glass
Performance	Low loss	Substrate loss	Substrate loss	High selectivity	Low loss
Thickness	Thick	Thin	Thin	Thin	Thin
Size	Small footprint	Moderate footprint	Moderate footprint	Small footprint	Small footprint
Density	Low density	Moderate density	Moderate density	High density	High density
Frequency	Low - high	Low - moderate	Low - moderate	Low	Low - high
Cost	Mass production	Less in demand	High	High	Not in market

Figure 2.9: Summary of RF passive component technologies.
(Source: Zihan Wu, Finisar Corporation)

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sign and fabrication of passive components such as filters, power dividers, diplexers and couplers. These components have experienced reduction in size while maintaining and improving performance metrics as the processes to fabricate them have advanced. A brief review of prior art of these components is given below.

2.2 Prior Art: Filters

2.2.1 Sub-7 GHz Filters

The sub-7 GHz frequency domain has seen advances in filter technologies driven by the proliferation of wireless networks throughout the world. Given the different telecommunication standards in geographical regions throughout the world, these filter technologies have been adapted to accommodate for the needs of communication systems. In this section, the discussion is focused on planar filter technologies for sub-7 GHz frequency range.

Filters using Discrete Inductor-Capacitor (LC) Components

LC filters are low-cost structures depicting moderate performance and size. They are designed by combining the correct values of discrete inductors and capacitors to obtain the desired response. SMD inductors and capacitors are assembled on a board with connecting traces to form a filter. Since these components are designed using using LTCC technology, tolerance in the desired value of the component and parasitics play a very important role in their high frequency operation. The reduction of parasitics is the differentiating factor between low and high operating frequency LC components. There are four different types of SMD inductors: winding, stacked, thin-film and woven/knit-type. Similarly, the capacitors can be classified into the following categories: multilayer ceramic, thin-film, electrolytic and tantalum.

For example, inductors can be designed in vertical solenoid configuration to fully exploit the advantages of multilayer ceramics in LTCC. These inductors feature high Q factors and are available in a variety of values because of controllable inductance density per unit

Internal electrode

Dielectric
ceramics

Terminal electrode

Connecting
terminal

Ceramic layers
(dielectric)

Electrode

Coating

Connecting
terminal

(a)   (b)
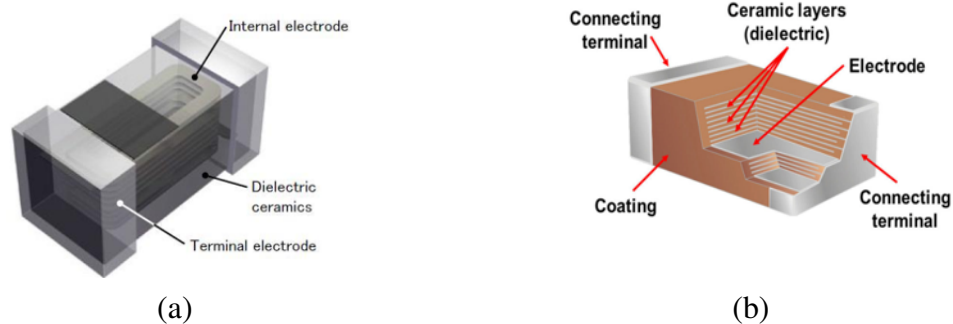
Figure 2.10: SMD components based on LTCC technology (a) vertical solenoid inductor, and (b) thin-film capacitor.

area. On the other hand, ceramic capacitors also take advantage of LTCC technology to achieve high capacitance density per unit area to realize high value, high Q capacitors. An inductor and capacitor based on LTCC technology are shown in Figure 2.10.

The performance of these filters is dependent on three main factors: 1) Q-factor of the discrete component, 2) frequency of operation, and 3) value of inductance or capacitance vs. frequency. Q-factor is also a frequency-dependent quantity. For the inductors, another important factor is self-resonant frequency (SRF) which is a frequency as a result of inductance of the inductor itself and the parasitic capacitance between the terminals of its package. SRF needs to be sufficiently higher than the operating frequency for best performance. Similarly, for the capacitors, effective series resistance (ESR) is the important factor. Ideally, ESR should be zero but practically, it varies with the frequency. This resistance is the characteristic of the conducting electrodes and dielectric material. Typical value of ESR for high frequency capacitors is below 0.2-Ω at 2 GHz. Another important metric is loss tangent of the dielectric material which plays a key role in overall losses contributed by the capacitor. The frequency-dependent Q-factor of inductors and capacitors by Johanson Technology of 0402 footprint is given in Figure 2.11a and 2.11b, respectively [55, 56].

The LC components can be arranged in different filtering circuits to obtain the desired
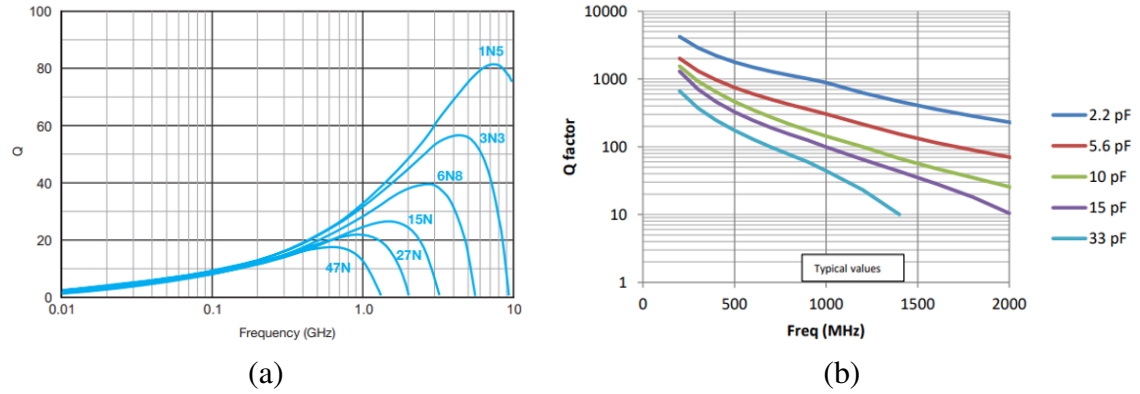
Figure 2.11: Q-factor vs. frequency of 0402 size components (a) RF ceramic chip inductors, and (b) multi-layer high-Q capacitors.
(Source: Johanson Technology)

response. An example layout of LC realization of a lowpass filter is shown in Figure 2.12. The shunt elements are SMD capacitors whereas the series elements are inductors. Since SMD components are available in standard values, they can be combined in series or parallel to obtain custom required values. As evident from Figure 2.12, series elements or inductors are combined to obtain the required value. This type of implementation is known as ladder network structure. Some applications of discrete LC filters are wireless LAN, Bluetooth, GPS, PCS and GSM. Since SMD components can be designed with very low tolerance values (less than 2%), repeatability of designs is guaranteed and given the small footprint of these components, the circuit is highly miniaturized as compared to its distributed version. From the implementation perspective, the layout of the pads for assembly of passive components needs to be optimized to ensure desired RF behavior after reflow
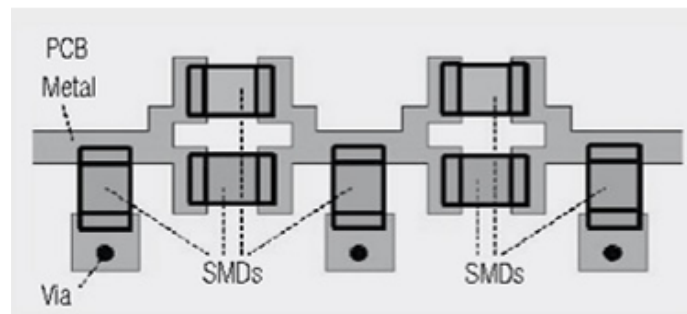
Figure 2.12: Layout of LC realization of a lowpass filter using discrete components.

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processes. For example, non-optimal landing pad sizes can lead to additional parasitic capacitances which can cause undesired behavior in the filter response.

Filters as Integrated Passive Devices (IPDs)

IPDs are composed of inductors and capacitors interconnected in a single packaged substrate laterally or vertically. LTCC substrates can aid in realizing high-performance IPDs as the number of layers can be changed depending upon the complexity of the design. For example, an ultra-compact, high-rejection, balanced filter on LTCC is reported by Yatsenko *et al.* [57]. The filter uses 16 low dielectric constant LTCC layers and features 2.2-dB insertion loss at the center frequency with 2.7-dB insertion loss at band edges, and has more than 30-dB rejection in the lower and upper stopband. The size of filter is just 1.2-mm^3 with overall height less than 0.3-mm. The 3D layout and transmission characteristics of this filter are shown in Figure 2.13. Similarly, a high performance fifth order LTCC wideband BPF based on coupled lines has been demonstrated by Feng *et al.* [58]. It uses 9 LTCC layers, has a center frequency of 3 GHz and 23% fractional bandwidth (FBW) with less than 2-dB insertion loss and more than 20-dB rejection. Commercially fabricated filters on LTCC technology are also reported by Johanson Technology [59, 60], Murata [61] and

(a)   (b)
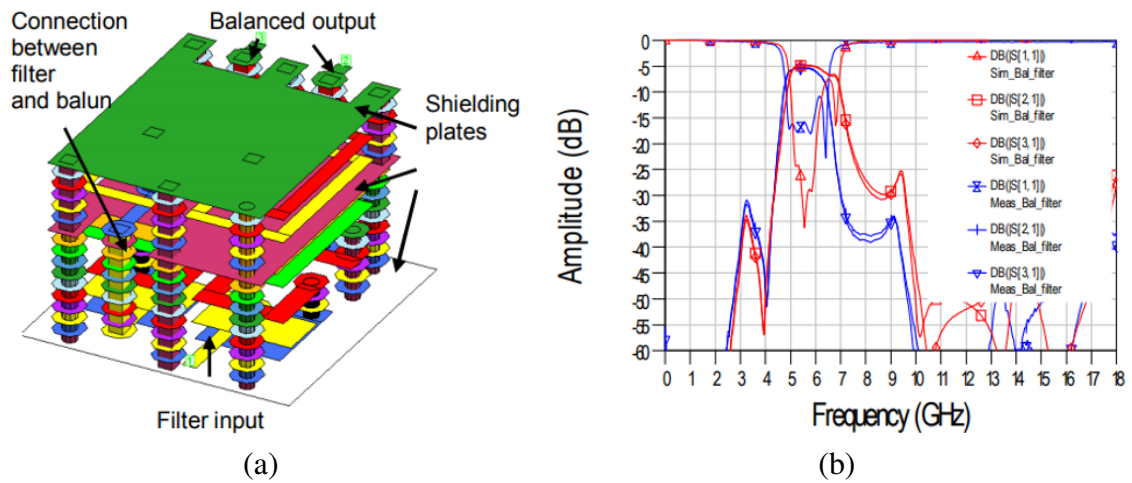
Figure 2.13: LTCC IPD example: balanced filter (a) 3D layout, and (b) response.

others [62] for sub-7 GHz operation.

Moreover, diplexers can also be implemented with compact size on LTCC. A SHF-band diplexer with 400 MHz bandwidth at 3.6 GHz and 1000 MHz bandwidth at 5.5 GHz is reported in [63]. The diplexer is composed of two fourth order cross-coupled Chebyshev filters. It has an insertion loss of less than 2-dB, better than 30-dB out-of-band rejection and its size is $4 \times 10 \times 2$ mm^3. The diplexer is shown in Figure 2.14 along with its response. TDK-EPCOS has demonstrated various compact WLAN diplexers on LTCC substrates with design innovations. [57, 64].

Some of the challenges of building high-performance IPDs on LTCC substrates are reduction in thickness, smaller linespace requirements as well as high-density integration into a miniaturized RF module. One approach to reduce thickness is to reduce the high count of LTCC layers but it results in performance degradation. Moreover, these components need to be integrated on PCBs with external interconnections which can be lossy, leading to limited use-cases of such components.

The challenges in LTCC IPDs, primarily thickness reduction and smaller feature requirements has driven the development of laminate-based passive component. Using an organic laminate core with laminated film RDL, LTCC-like higher component density can be achieved. The film thickness can be controlled to reduce the overall thickness of the component [65]. Georgia Tech has reported compact, 2.4 and 5 GHz filters on low-loss
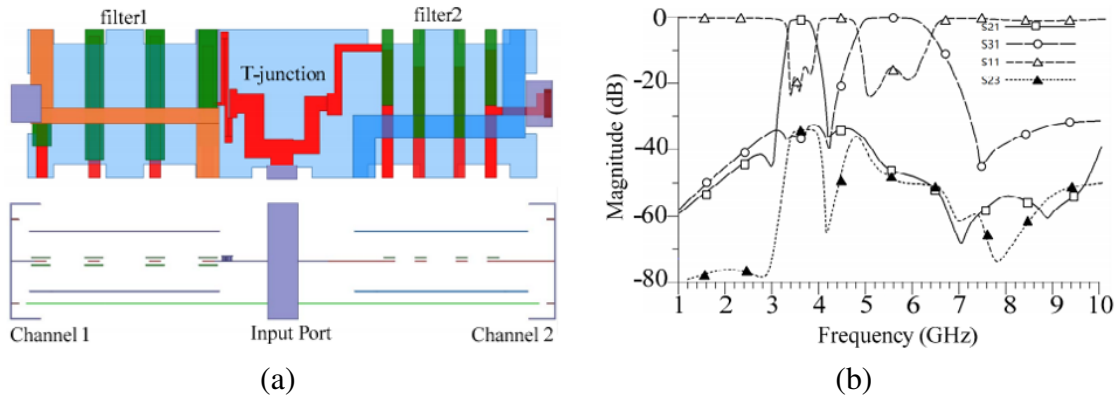
Figure 2.14: LTCC IPD example: diplexer (a) top view, and (b) response.

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RXP substrates with transmission zeros (TZ) around the passband to improve stopband rejection [66]. The size of one of the 2.4 GHz filters is $3.6 \times 2.4 \times 0.2$ mm^3. Thin-film LC components such as spiral inductor and metal-insulator-metal (MIM) capacitors enable miniaturized IPDs and they can be integrated on glass or silicon. Glass has an advantage of realizing 3D passive filters due to its low loss and silicon-like dimensional stability. Extensive work on glass-based thin-film IPDs has been reported in [28, 67, 68].

Acoustic Wave Filters

Acoustic wave filters have dominated the filter market in sub-7 GHz low power wireless equipment due to their small-size, unmatched performance and low cost for complex filtering requirements. These filters operate under the fundamental principle of piezoelectric effect which is essentially the concept of electromechanical resonance [69]. RF is converted to mechanical or acoustic energy using interdigital transducers and that energy is carried by the piezoelectric substrate, and then converted back to RF. The piezoelectric substrate can be quartz, lithium tantalite (LiTaO$_3$) or lithium niobate (LiNbO$_3$). The dimensions of transducers correspond to the wavelength of incoming RF signal. The decay or filtering happens in the substrate itself due to its special properties, resulting in in-band and out-of-band insertion loss. The process of conversion of electrical energy to acoustic energy and vice versa is highly efficient, and the unwanted energy is significantly decayed. This results in much higher Q factor (>2000 at 2 GHz) of the designed filters, making this technology the most widely adopted one for cellular applications. As can be expected from the type of energy, the traveling speed of the electrical wave is reduced to 3000-12000 m/s (compared to 300,000,000 m/s of light in free-space) when it is converted to acoustic wave. As indicated by the name, the acoustic wave travels at the surface of the substrate for surface acoustic wave (SAW) filters. They suffer from degradation of selectivity above 1 GHz but operate well upto 3 GHz. A simple SAW filter is shown in Figure 2.15a. Since the transducer lines are patterned using photolithography, high frequency operation becomes

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(a)	(b)
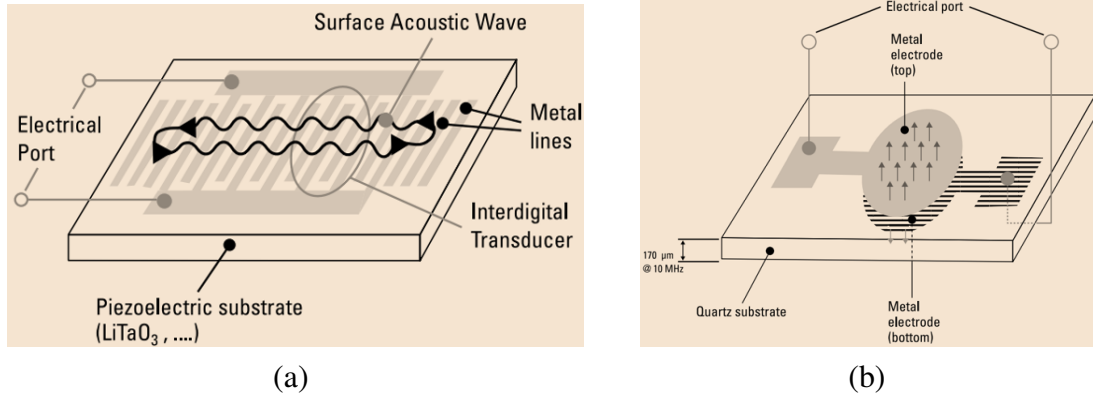
Figure 2.15: Basic acoustic wave filters (a) SAW, and (b) BAW.

challenging due to process limitations, limiting the frequency range of operation. Also, SAW filters suffer from drift in specifications due to changes in ambient temperature [70]. To mitigate the shift in filter response due to change in temperature, low/zero temperature coefficient of frequency (TCF) are introduced. It is predicted that for smartphone markets, the competition will be between SAW and BAW filtering technologies for the next five to ten years [71].

Bulk acoustic wave (BAW) filter, unlike SAW, have the acoustic wave propagate vertically in the substrate. As a result, it is possible to design narrowband filters with exceptionally steep skirts and excellent rejection. BAW filters have become popular due to increased CA requirements for 4G and LTE networks to support more bands in cellular devices, and they have evolved to support additional sub-7 GHz in 5G NR as well [72]. As mentioned earlier, the energy travels vertically in the substrate thus transducers are placed at the top and bottom of the quartz substrate rather than on one side as is the case of SAW filters. The resonance frequency is determined by the thickness of substrate and the mass of the electrodes [73]. As a result of this approach, BAW filters operate in sub-7 GHz range with ease and they can go higher up to 9 GHz. A simple BAW filter is shown in Figure 2.15b. The thickness of piezoelectric layer at higher frequency is only a few micrometers, thus BAW takes full advantage of film deposition techniques to achieve precise thickness [41]. An acoustic Bragg reflector can be created by stacking thin layers of materials with alter-

nating stiffness and density, and this approach can help in keeping the wave from leaking into the substrate. This approach is called a solidly mounted resonator BAW (BAW-SMR). Alternatively, a more popular approach is to have the material layers replaces by an etched air-filled cavity, resulting in suspended membranes. This results in film bulk acoustic wave resonators (FBAR) which have a very high Q factor, leading to filters with excellent electrical performance.

The superiority of SAW and BAW filters is in their low insertion loss, high selectivity and highest Q-factor among similar footprint filter realization technologies. Since their realization is compatible with modern-day processes: flip-chip and wafer-level packaging technologies, it results in design flexibility, improved performance, lower costs and faster manufacturing time. They can also be seamlessly integrated with other components, particularly with PAs, switches and other RF FEM components. However, acoustic wave filters are hindered by narrowband of operation due to electromechanical coupling coefficient which is determined by the selection of materials and design topologies [74]. BAW filters become costlier as the frequency of operation increases due to tighter precision tolerance and complex processing steps such as the requirement of multiple masks. An infographic depicting the use-cases of SAW and BAW filters for various 4G and LTE bands is shown in Figure 2.16.

Planar Transmission Line Filters

Planar filters are based on transmission line structures discussed in Section 2.1.2. They are also known as distributed filters as the lumped LC components are realized using transmission lines. Generally, they have a lower Q-factor than their acoustic wave counterparts and are larger in size. In current and next generation radios for communication systems which have complex circuitry to support a range of functionalities, significant need exists for planar filters. They are popular due to their low profile and ability to be heterogeneously integrated in packages and boards. Regarding filter specifications, insertion loss can be
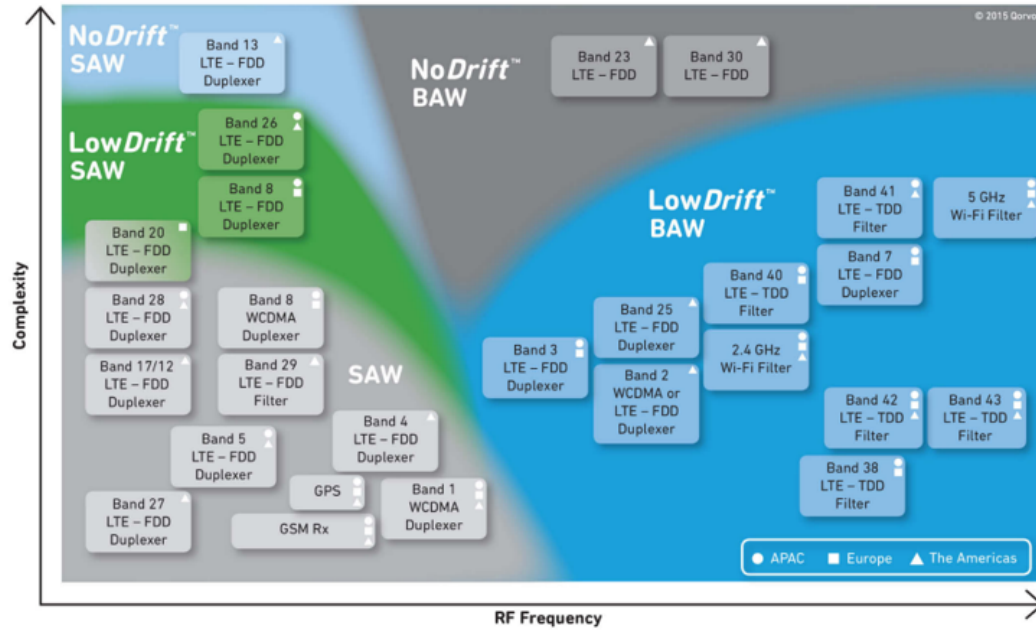
Figure 2.16: Use-cases of SAW and BAW filters for 4G and LTE bands.
(Source: Qorvo)

compensated in a system by means of tuning the amplifier stages but passband flatness and sharp rejection require high-Q resonators. The materials required for high-Q resonators increase the manufacturing cost of these filters. However, techniques such as lossy and predistorted design theory can improve flatness in passband as well as provide desired rejection, avoiding the use of high-Q materials. The filtering specifications become more challenging when flexibility in operational bandwidth and reconfigurability is required. A detailed review of advances in planar filters is presented by Hong [75].

The following research topics have attracted the research community in planar filters [76–78]:

- Multi-band bandpass, bandstop and multiplexers for receivers.

- Reflection-less or absorptive filters to mitigate generation of out-of-band reflections.

- Filters with multi-functional and co-integration capabilities: antenna-integrated filters, filtering power dividers and couplers, filtering impedance transformers and others.

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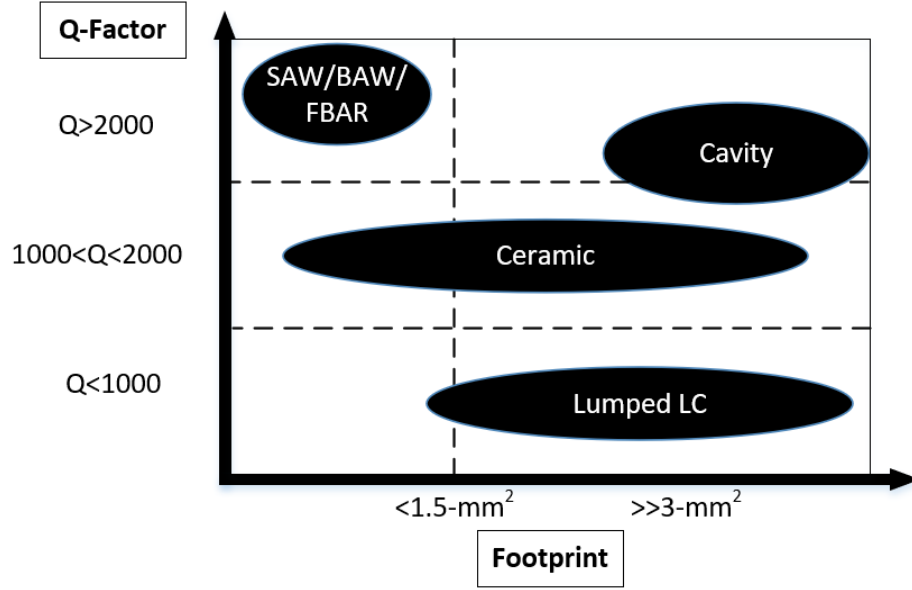
Figure 2.17: Comparison of various filter technologies at 1 GHz in terms of performance (Q-factor) and footprint.

- Reconfigurable filters.

A comparison of filter performance (Q-factor) vs. footprint is given in Figure 2.17. Acoustic wave technologies have surpassed the typical lumped and distributed LC networks in sub-7 GHz range in realizing high performance filters, resonators, oscillators and delay lines, and have found many applications in 4G and LTE networks.

2.2.2 Millimeter-Wave Planar Transmission Line Filters

Over the past few decades, several theoretical advancements have been made in the design and fabrication of planar filters with their evolution in terms of reduction in size while improving performance metrics [79]. Planar filters are constructed using transmission lines, some of which are microstrip, stripline and SIW. They can be broadly classified into following categories: on-chip, on-package and off-chip. The on-chip technologies include gallium-arsenide (GaAs), silicon-germanium (SiGe), complementary metal oxide semiconductor (CMOS) and bipolar CMOS (BiCMOS). For on-package and traditional off-chip variants, the technologies are LTCC, organic laminates, state-of-the-art integrated fan-out

wafer-level packaging (InFO WLP) and ultra-thin laminated glass for passive components realization. A brief review of prior art of these components is this section.

On-Chip Filters

On-chip filters are popular due to their compatibility with the existing semiconductor processes, giving designers the freedom to integrate filters with other circuitry directly by taking advantage of short interconnects and precision fabrication of dimensional features. The classification of these filters is shown in Figure 2.18. Some of the on-chip filters for mm-wave applications are discussed below.

A novel mm-wave 35 GHz BPF using half-wavelength CPW resonators on 0.18-μm standard CMOS process is reported by Yeh *et al.* [81]. A transmission zero (TZ) using series LC resonators is created at 58 GHz and with the parasitic effect, another TZ is created at 80 GHz. Furthermore, a TZ is created at 66 GHz using a shorter conductor-backed resonator, resulting in improved filter selectivity. The capacitively loaded CPW lines are implemented using metal-insulator-metal capacitors, which also aid in miniaturization. The insertion loss of this filter is less than 4.5-dB and its return loss is higher than 12-dB. The size of this filter is 0.225×0.55 mm^2. Compared with a conventional combline filter, the size reduction is up to 63.4% at the operating frequency of 35 GHz. The substrate and layout of this filter along with its measured results are shown in Figure 2.19.

Another on-chip mm-wave BPF using 0.13-μm SiGe BiCMOS technology utilizes a
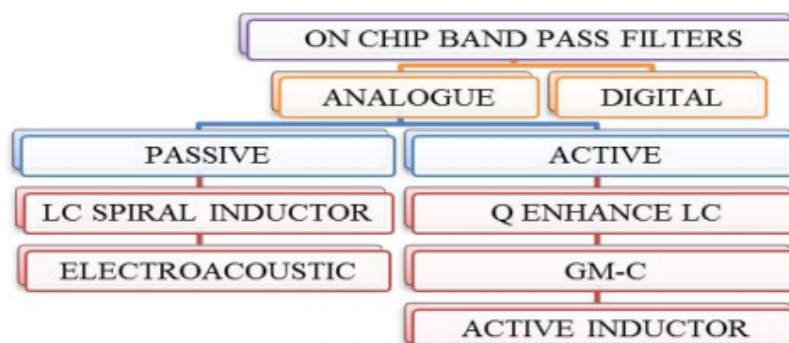
Figure 2.18: Classification of on-chip filters [80].
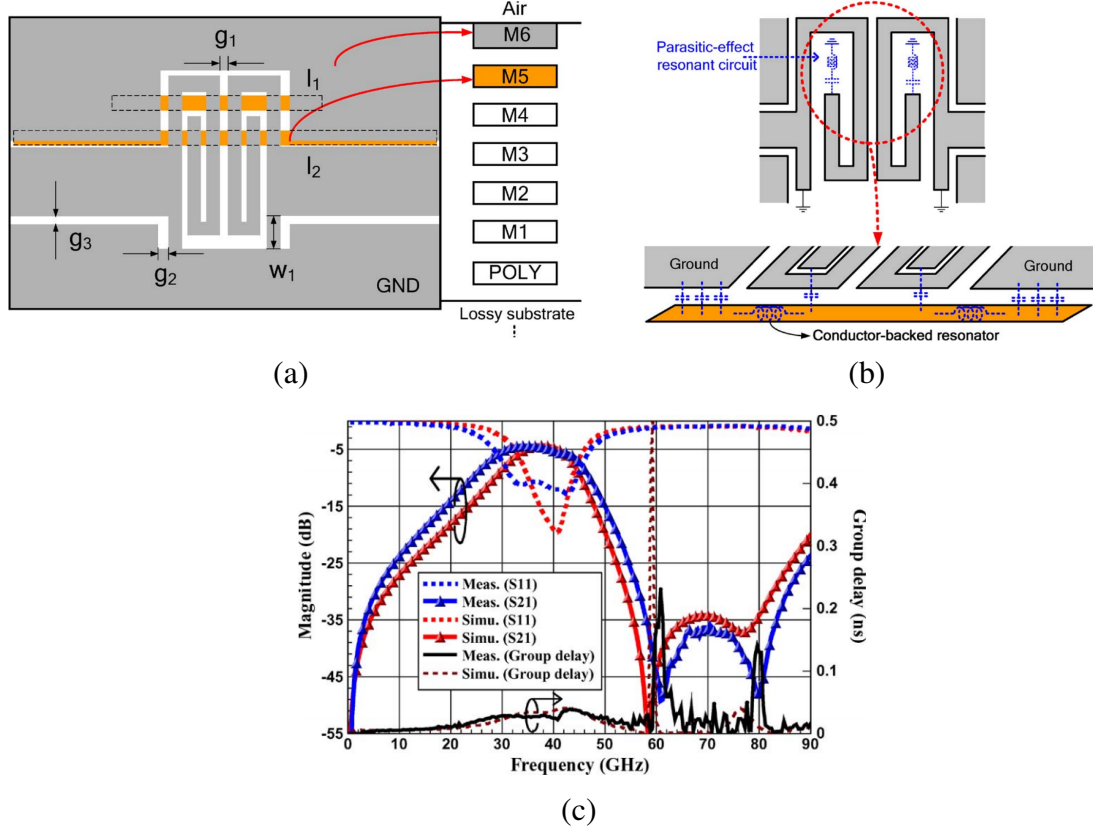
Figure 2.19: An on-chip CPW CMOS mm-wave BPF using conductor-backed resonators (a) stackup layers and top view, (b) 3D layout and (c) comparison of simulated and measured response [81].

novel design methodology for TZ generation based on multilayer patterned ground (MPG) element, inspired by defected ground structures (DGS) principles, is presented by Sun *et al.* [82]. The technique discussed by the authors is suitable for miniaturization and it provides a simple way to introduce a TZ at the upper stopband without significantly affecting response of the filter. Three version of the filters with second-order response are designed to show the capability of this technique. The material stackup consists of five metal layers on a substrate with MIM layers in-between to realize the capacitors. A behavioral model using LC components is also presented for the EM structure. The third BPF design achieves a minimum insertion loss of 2.7 dB at 31 GHz and it has 17.5% FBW. It features suppression of more than 25-dB in lower and upper stopbands. The size of the three designs are: 0.06×0.284 mm^2, 0.09×0.286 mm^2 and 0.154×0.288 mm^2. The material stackup and

layout of this filter along with its response are shown in Figure 2.20. Similar BPFs are also reported in [83, 84].

(a)

(b)

(c)
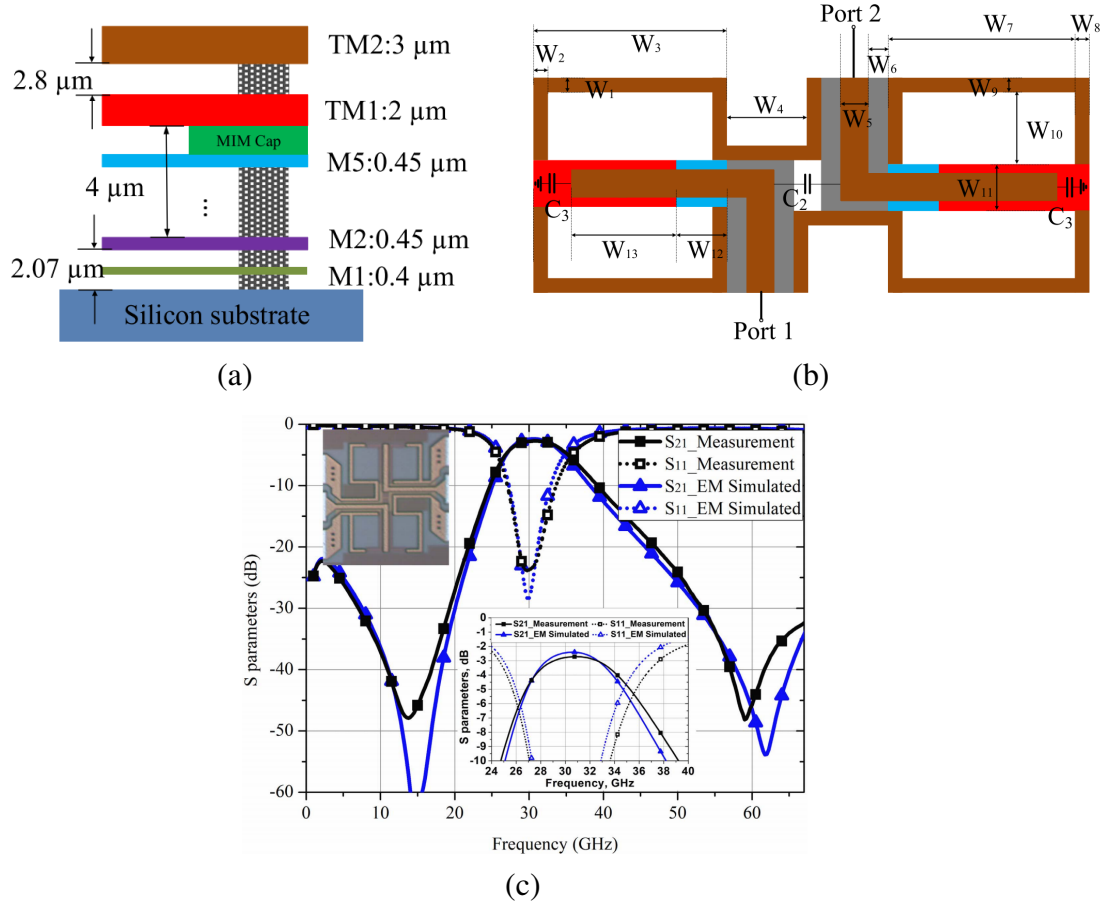
Figure 2.20: An on-chip BiCMOS mm-wave BPF using MPG elements (a) stackup layers and top view, (b) 3D layout and (c) comparison of simulated and measured response [82].

Two BPFs for 28 GHz 5G mm-wave on GaAs technology with high selectivity BPFs using coupled, dual-behavior, open and shorted stub resonators are reported by Feng *et al.* [85]. Two on-chip BPFs with two and three out-of-band TZs are presented. The insertion loss of both filters is less than 2.2-dB and they have FBWs of 11.1% and 8.9% for two and three TZs, respectively. Their out-of-band rejection is more than 20-dB. The footprint of the designed filters is 2.556×1.23 mm^2 and 3.155×1.47 mm^2, respectively. The material stackup, layout and response of the filters is shown in Figure 2.21. Similar BPFs on GaAs and CMOS are reported in [86, 87]. Another Ka-band BPF with asymmetrical compact
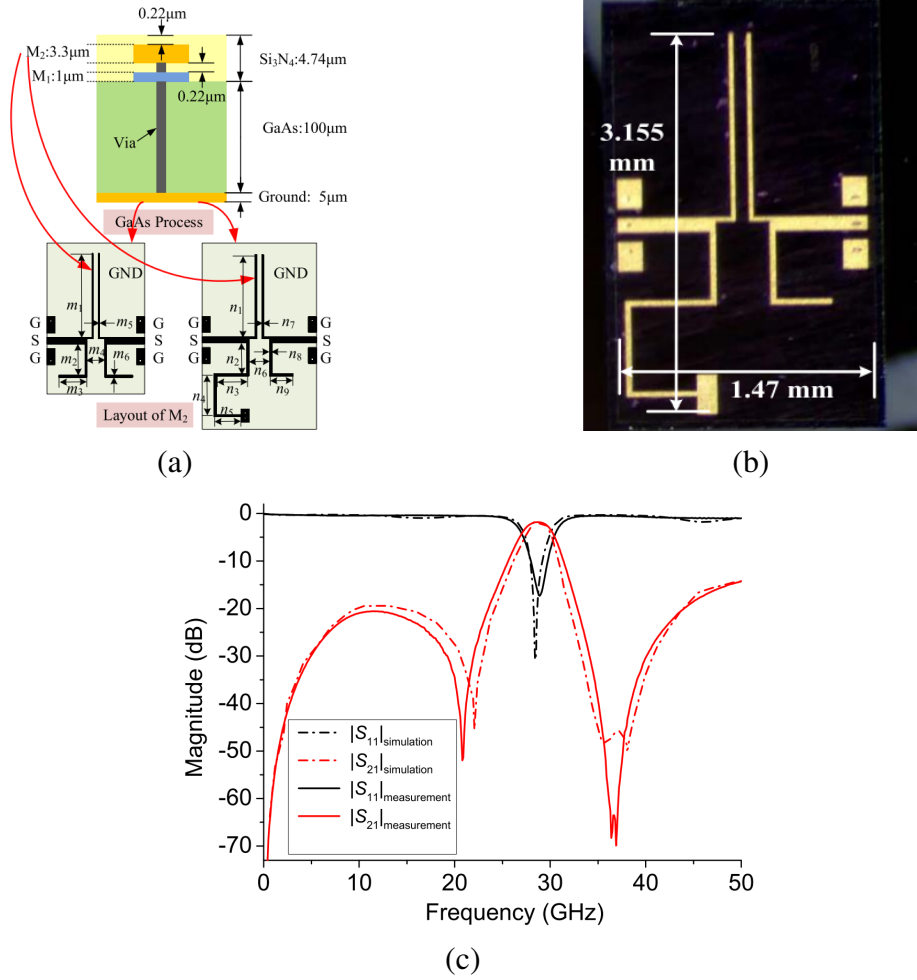
Figure 2.21: On-chip BPFs using GaAs technology for 28 GHz 5G mm-wave applications (a) material stackup and layout of two filters, (b) fabricated second filter, and (c) measured response [85].

resonator using 0.15-μm GaAs fabrication technology is presented by Yang *et al.* [88]. This filter features a minimum insertion loss of less than 3.2-dB at the center frequency of 34 GHz with 14.8% FBW. The out-of-band attenuation is greater than 25-dB and 50-dB due to TZs located at 15 and 43 GHz, respectively. The size of this filter is $0.288{\times}0.257$ mm^2.

As evident from the literature review of on-chip filters for mm-wave applications presented in this section, they have advantages of low interconnect loss, tighter integration and process compatibility. However, they suffer in terms of electrical performance with high passband insertion loss ($\sim$3-dB and higher) as well as poor selectivity as compared to their

traditional off-chip counterparts.

Off-Chip Filters

The technologies for planar off-chip filter fabrication are LTCC and organic laminates, and to some extent liquid crystal polymer (LCP). A brief overview of planar on-package filters for mm-wave applications is given in this section.

LTCC facilitated initial advances in mm-wave distributed filters because of its ability to integrate complex 3D multilayered conductor patterns with through and blind vias. A 4-pole dual-mode resonator filter on LTCC for 30 GHz center frequency with FBW of 4.67% and an insertion loss of 2.95-dB using two TZs is reported by Ahn *et al.* [89]. It uses a five metal layer stackup with filter footprint of 11×8 mm^2. Another four-pole quasi-elliptic waveguide filters using multilayer LTCC is reported by Shen *et al.* [90]. The filter has a center frequency of 29.87 GHz with 3-dB FBW of 13.02%. Its passband insertion loss is 3.3-dB and two attenuation poles at 26.2 and 34.6 GHz help in improved selectivity. The size of this filter without the vertical transition is $3.67\times2.79\times0.8$ mm^3. The material stackup, 3D layout and response of the filters is shown in Figure 2.22.

Similarly, two system-on-package (SoP) based two-stage SIW single cavity filters with embedded planar resonators on LTCC are reported for 5G applications by Showail *et al.* [91]. The filter with stripline ring around the cavity has a center frequency of 28.21 GHz with 13% FBW and an insertion loss of 0.82-dB. In parallel, a 0.53-dB insertion loss filter with center frequency of 28.12 GHz and 15% bandwidth has a design that feeds at the middle of a stripline resonator. Its dimensions are $7.55\times4.44\times0.47$ mm^3. The final filters is fabricated on a stackup with five layers of LTCC, four layers for the cavity and one layer to feed the filter [92]. The exploded view of the latter filter along with its s-parameters are shown in Figure 2.23.

Although LTCC became a very attractive option for fabricating microwave and mm-wave passive components for a couple of decades, challenges such as complexity and

(a)

(b)

(c)
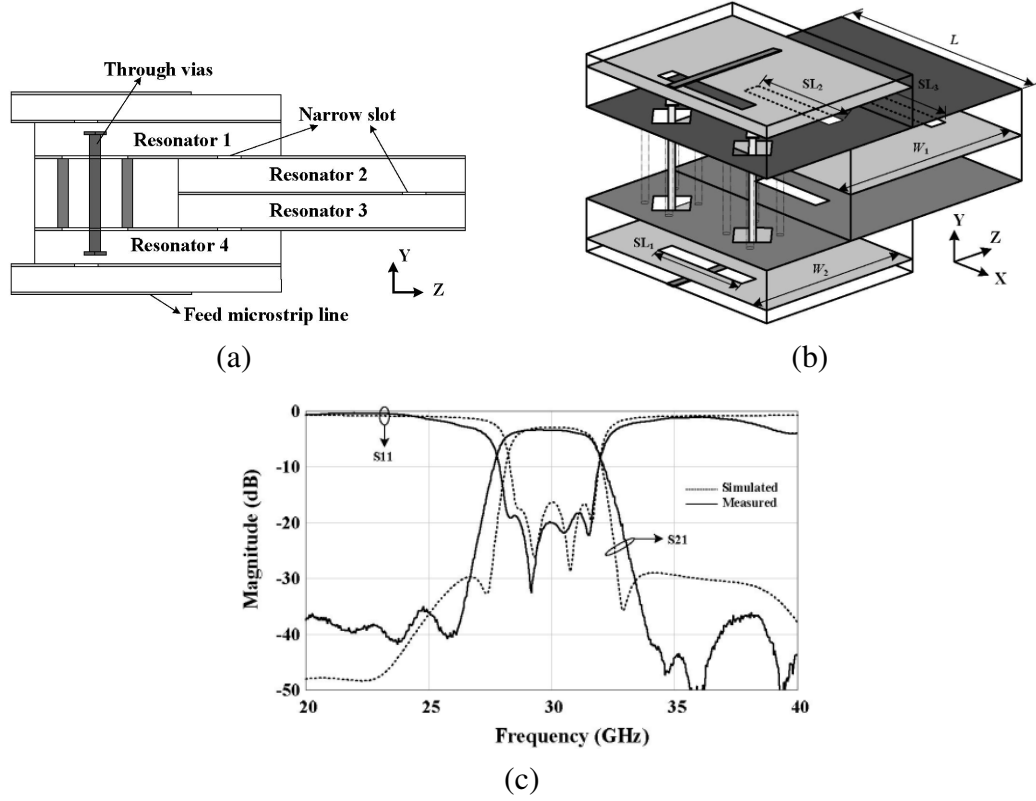
Figure 2.22: Off-chip four-pole BPF on LTCC (a) material stackup, (b) 3D layout, and (c) response [90].

cost of fabrication due to high number of layers, loss at mm-wave frequencies and surface roughness led to developments in the wake of relatively new planar organic substrates with stable electrical properties and ease of fabrication. Filters in organic laminates are typically designed with larger footprints and feature lower insertion loss. X-P CHen et al., have reported Ka-band four-degree BPFs on SIW having asymmetric frequency response for diplexer applications for high rejection between neighboring channels [93]. The filters are fabricated on Rogers RT/duroid 6002 substrate with thickness of 0.508 mm by using a low-cost PCB process and have TZs on either side of the passband as shown in Figure 2.24. The center frequency of these filters is 35 GHz with 3.7% FBW and insertion loss of 1.25 dB. The dimensions of these filters are $11 \times 11 \times 0.508$ mm^3.

Another work presents microstrip coupled-line BPFs for mm-wave frequency applications [94]. The attenuation poles at the high and low passband edges are suitably inserted
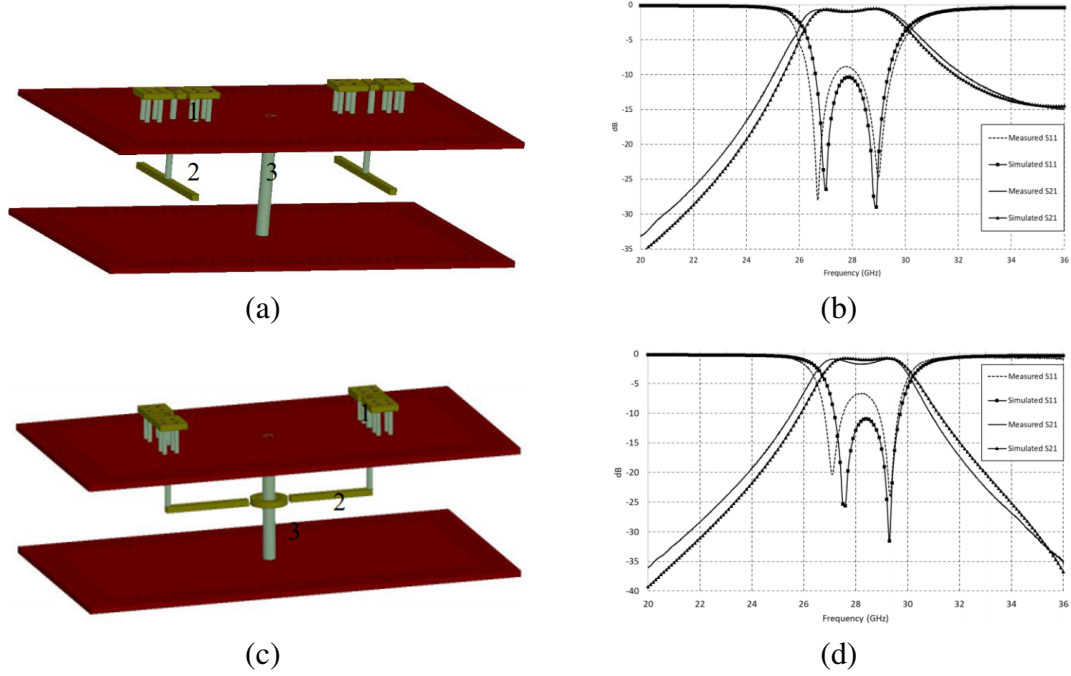
Figure 2.23: SIW cavity filters on LTCC (a) exploded view of the filter with center fed stripline resonator (vias hidden), and (b) its response, (c) exploded view of the filter with stripline ring around the cavity's center post, and (d) its response [91].

in an edge-coupled structure by adding a capacitively coupled gap and tapped open stubs. The filters are fabricated on Teflon and Alumina. The fabricated filter on Teflon depicts an insertion loss of 4-dB and 4.67% FBW centered at 27.85 GHz whereas the filter fabricated on Alumina shows 3-dB insertion loss and 7.8% FBW centered at 38.5 GHz.

Moreover, a miniaturized mm-wave BPF based on SIW incorporating stepped-impedance slot-resonator (SI-SR), also known as complementary split ring resonators (CSRR), is presented for 5G mm-wave communication by Wang *et al.* [95]. The center frequency is controlled by adjusting the size of SI-SR and the coupling coefficients are altered by changing their position and inter-resonator spacing. The authors have demonstrated three structures: one second order and two third order filters. The substrate is Rogers RT/duroid 5880 with 0.254 mm thickness and the filters are fabricated using standard PCB process. The two-pole filter has a center frequency of 29 GHz with 14.18% FBW. Its measured passband insertion loss is 2.2-dB. Similarly, three-pole filters have insertion loss of 2.51-
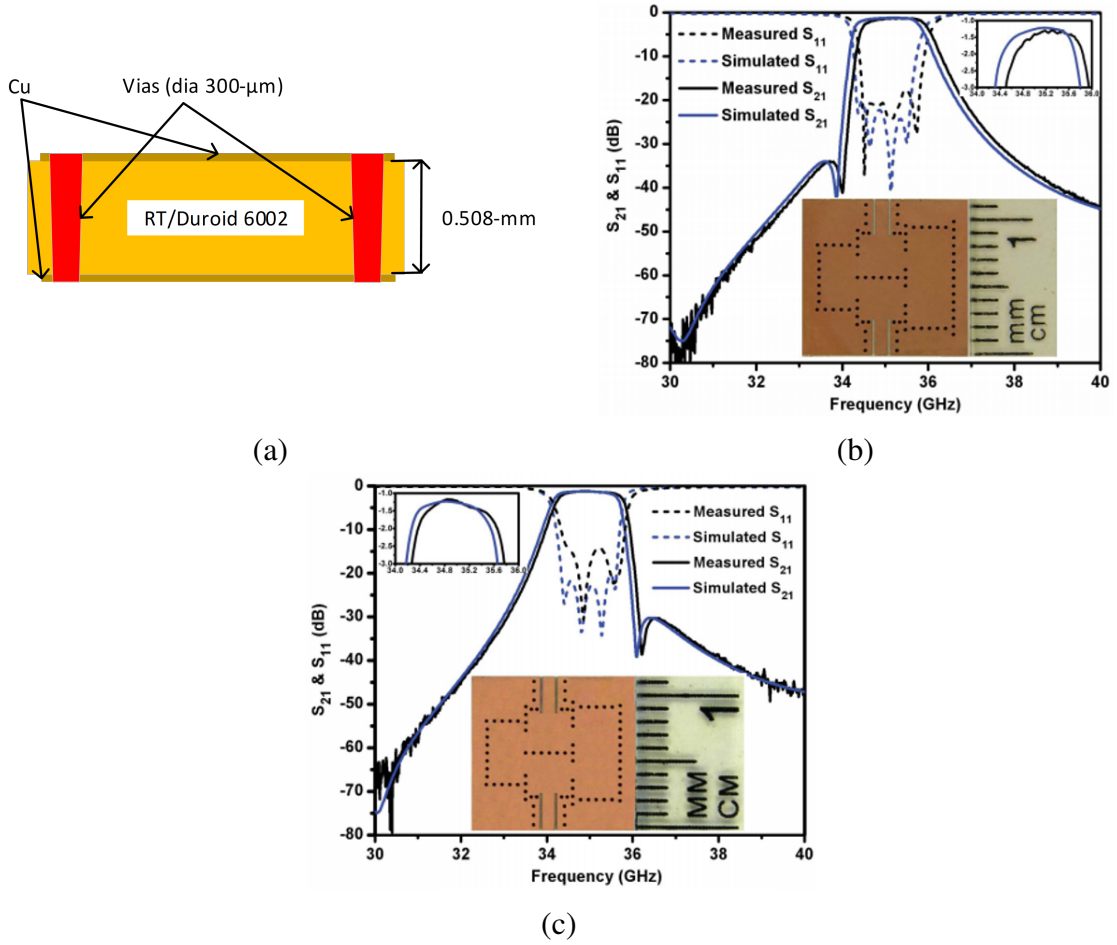
Figure 2.24: Ka-band four-pole SIW filter on organic laminate (a) stackup, (b) TZ on left of passband, and (c) TZ on right of passband [93].

dB and 2.3-dB with FBWs of 12.39% and 14.39%, respectively. The second three-pole filter has additional vias at the center to improve attenuation at the upper stopband. The layout and response of these filters is shown in Figure 2.25.

For filters in the mm-wave range with operating frequencies more than 40 GHz, Lee *et al.*, report several mm-wave passive components using 3D LTCC system-on-package (SOP) technology [96]. His work reports slotted-patch resonator as a filter, duplexer at 41/61 GHz, three- and five-resonator BPF at 60 GHz and a 40 GHz directional filter. Another work by Aryanfar *et al.*, reports a compact mm-wave filter using capacitively loaded CPW resonators at W-band [97]. They used the method of loading a CPW line with multiple capacitive loads along the length of the transmission line to increase its capacitance. They

Figure 2.25: Miniaturized SIW BPFs with SI0SRs for mm-wave applications (a) stackup, (b) layout of three-pole filter with additional vias, (c) response of three-pole filter, and (d) response of three-pole filter with additional vias, depicting improved upper stopband performance [95].

also provide a hybrid method of simulation by combining method of moments (MOM) and circuit simulations which facilitates a systematic approach for filter design at mm-wave frequencies. Hao *et al.* have reported development of a low-cost W-band CQ BPF integrated with fine-line SIW-waveguide transitions on an organic laminate (Rogers RT/duroid RO5880) with loss tangent of 0.0009 at 10 GHz [98]. It is a coupling structure with a fractional bandwidth of 2.5% centered at 80 GHz. This demonstration reveals that low-cost commercially available substrates can be used for the fabrication of mm-wave passive devices.

Similarly, a mode suppression technique for microwave and mm-wave LTCC filters using discriminating coupling is reported in [99]. The author proposes a new discriminating coupling mechanism, which is realized by choosing suitable coupling region between the

feeding lines and resonators, and it suppresses the unwanted resonance modes without affecting the desirable operating modes. This methodology is used to propose a microwave and a mm-wave frequency filter. The filters have wide stopband since the third and fifth harmonics are suppressed by the discriminating coupling technique. The filters utilize upto 10 metal layers with ceramic sheet between two metal layers. The mm-wave frequency filter operating at 60 GHz is designed to be oversize to avoid fabrication difficulties and this is achieved by utilizing high-order resonance modes rather than the fundamental mode for the BPF designs. The number of layers is reduced to three for this filter to avoid any parasitic effects at mm-wave operating frequencies. The author reports a minimum insertion loss of 2.8 dB with fractional bandwidth (FBW) of 6.6%.

2.3   Prior Art: Millimeter-Wave Power Dividers and Antenna Arrays

The mm-wave packaging technologies along with embedded antenna-in-package (AiP) is one of the vital contributors for the realization of high data-rate wireless communication. Package-integrated phased-array antennas and passive components, with single- or multi-chip transceiver solutions are the key enabling technologies for the next generation of radio solutions [100–102]. Millimeter-wave beam-forming is one of the most active areas in pursuit of compact, efficient and low-cost end-user devices as it is one of the key enabling technologies for 5G infrastructure such as UE, small-cell and base-stations [25, 103]. With the trend shifting towards package-integrated antennas, integrating a power dividing network with the antenna array in a package becomes extremely important as the power delivery to antennas operating at different bandwidths need to have minimal phase-shift [104].

To overcome the challenge of increased path loss with the use of 5G new radio (NR) bands, while providing Gb/s data rates with low latency, the 5G base-stations and UE will have to rely on directed communications [105, 106]. System-level implementation challenges can be translated to IC- and package-level requirements which are vital for mm-wave 5G hardware and software co-design [107]. Some of the circuit and phased-array IC level

challenges are to have reasonable spatial isolation between the links provided by beam-forming, support for dual polarization and finer resolution in phase shifter. Since antenna is the largest element in an AiP and essentially governs its size, the antenna (or antenna array) needs to be wideband with equal-length feeding lines, support dual-polarization with low cross-polarization distortion and have the tunability to support multiple beamforming and beam steering algorithms [108, 109]. Similarly, the package needs to support heterogeneous integration of multiple RFICs for scalability, seamless routing and interconnects, high thermal efficiency as well as multiple-functionality passive components [110].

A power divider splits a signal into two or more outputs in equal or unequal split ratio. If the input and output ports are switched, then the power divider becomes a power combiner, for combining multiple signals into one. A basic power divider is a three-port network and as per the nature of three-port networks, it cannot be simultaneously loss-less, matched at all ports and reciprocal. Power dividers with different performance metrics are broadly used in a range of applications and are selected based on the requirements. Extensive work has been done on power dividers in the past few decades for numerous low, medium and high-power applications. The innovation in these power dividers lies in performance breakthroughs, physical configurations and functional integrations [111]. Functionally-integrated power dividers have evolved as the need of multiple functionality in the same footprint has risen as communication systems have advanced. Power dividers are key components in realizing antenna arrays as they form the basis of dividing the input signal to be fed to multiple antennas. As mentioned earlier in Section 1.4.2, the key performance metrics of power dividers are:

- Splitting ratio

- Insertion loss

- Return loss

- Isolation
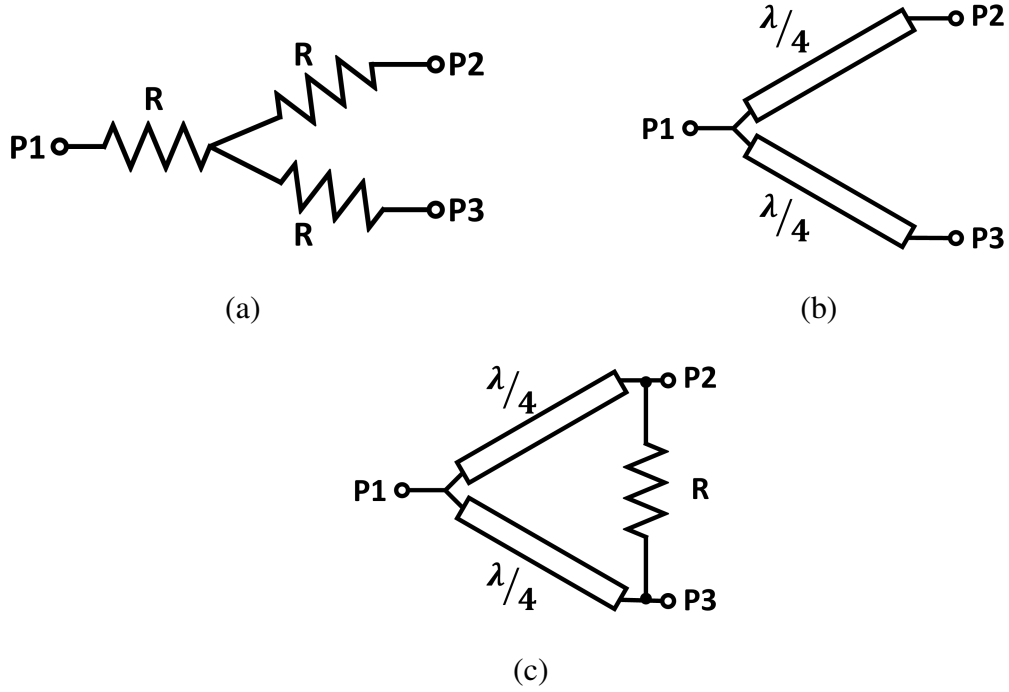
Figure 2.26: Schematic of three different types of power dividers (a) resistive, (b) T-junction, and (c) Wilkinson.

- Relative phase shift

- Amplitude balance and ripple

- Phase balance and ripple

The three different types of power dividers are: resistive, T-junction and Wilkinson. Their schematic is shown in Figure 2.26 and they are compared based on different performance metrics in Table 2.1 [112, 113]. A few planar power dividers in the 5G mm-wave frequency range realized on various technologies are discussed in this section.

On-chip power dividers are mostly realized on CMOS technology. An ultra-wideband low-loss mm-wave Wilkinson power divider covering DC-67 GHz has been developed on a 0.18-μm SiGe BiCMOS process [114]. It has an insertion loss of less than 1-dB from DC-61 GHz and its isolation is better than 15-dB in 37-67 GHz range. The die-size of this power divider is 0.15×0.525 mm^2. Another new on-chip dual-band Wilkinson power divider, designed at 28/60 GHz using GaAs IPD process is reported by Chu *et al.* [115]. It

Table 2.1: Comparison of three different types of power dividers.

Metrics	Resistive Power Divider	T-Junction / Wilkinson Power Divider
Physics of Operation	Resistive voltage divider circuit	Quarter-wave transformer separating even and odd mode signals with / without isolation resistor
Operation Frequency Range	DC - 10s of GHz	100s of MHz - 10s of GHz
Insertion Loss	6-dB (assuming two outputs)	10log(N) N = number of output ports
Split Ratio	6-dB for equal power split	3-dB for equal power split
Isolation	6-dB	None / 20-dB (typical)
Output Phase Shift	In-phase (0°)	In-phase (0°)

uses composite right/left-handed lines in microstrip form to achieve its dual band property. The added insertion loss of this power divider is 0.9-dB. The FBW of this power divider at 28 and 60 GHz bands is 20.4% and 20.3%, respectively. The isolation is better than 19-dB in both bands and it has a footprint of 0.7×0.71 mm^2. The layout, comparison of simulated and measured response, and comparison of simulated and measured amplitude and phase imbalance is shown in Figure 2.27. A similar but higher split-ratio (16-way) power divider using 0.18-μm BiCMOS process for K and V bands is reported in [116]. One of the smallest normalized chip area (0.035 mm^2, 1.7×10^{-4} λ_0^2) for mm-wave (Ka band, 33 GHz) power divider based on coupled-lines is reported in [117].

Off-chip planar power dividers are realized on LTCC, organic laminates and InFO technologies. For example, a Ka-band in-phase high isolation planar six-way power divider on LTCC is reported by Zhang *et al.* [118]. It is realized using ten layer of FerroA6M LTCC substrate in the frequency range of 34-36 GHz. The average insertion loss of this power divider is 8.38-dB with a maximum phase difference of 6° between the output ports. The
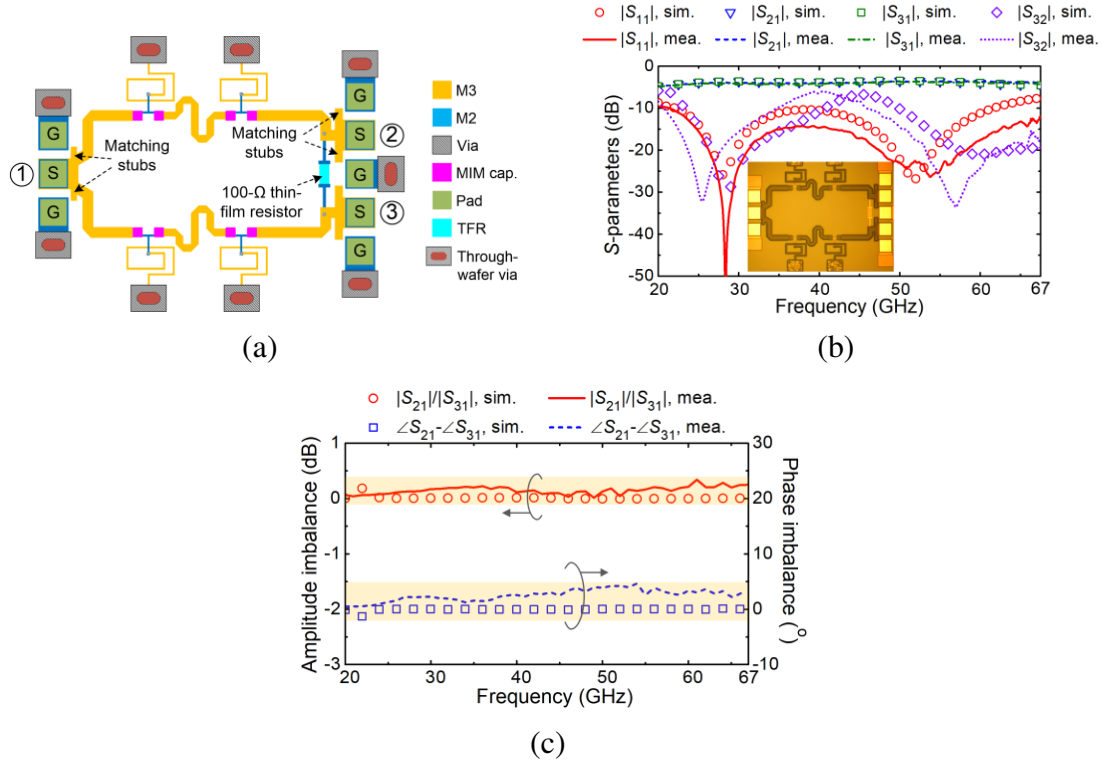
Figure 2.27: On-chip dual-band Wilkinson power divider (a) layout, (b) comparison of simulated and measured s-parameters, and (c) comparison of simulated and measured amplitude and phase imbalance [115].

dimensions of this power divider are 40×13 mm^2. Another SIW-based balanced power divider in mm-wave SoP applications on LTCC is presented by [119]. The power divider consists of a multilayer transition which is essentially two waveguides lying on different layers and connected through a longitudinal slot. It is fabricated on a six layer DuPont 9K7 LTCC substrate stackup. The operating frequency range of this power divider is from 32 to 38 GHz. Since it is a balanced structure, the phase shift between the output ports is $182° \pm 0.7°$.

A variable power divider for 28 GHz 5G mobile systems using a modified Wilkinson structure is reported by Abbas *et al.* [120]. It consists of a conventional Wilkinson power divider with input T-junctions replaced by coupled-lines. A varactor is placed placed between each coupled-line to tune the coupling factor. The power division in this design varies from 1:1 to 1:2 in the 27-29 GHz frequency range. It is realized on Rogers RT/duroid 5880 lam-
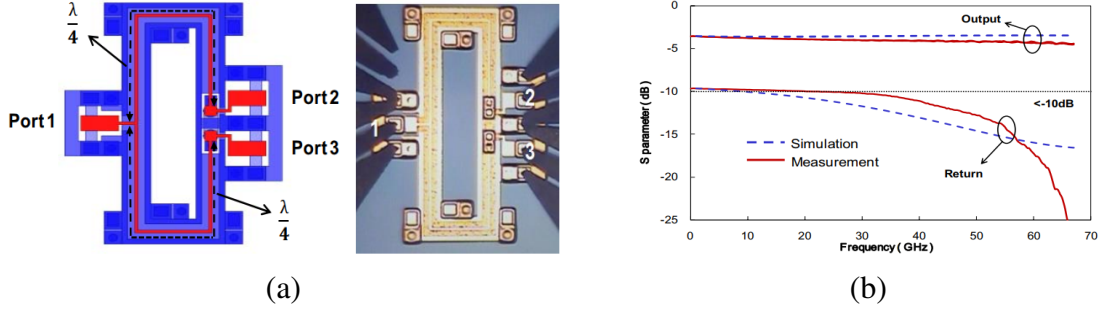
Figure 2.28: CPW power divider on InFO RDL (a) design schematic and fabricated layout (b) s-parameters [43].

inate with thickness of 0.127-mm. It has a footprint of 10×10 mm^2. The power divider has a phase imbalance of 22.5° which can be significantly higher for some applications. One of the most recent advances was presented by Hsu *et al.*, is an equal-split ultra-miniaturized CPW power divider on integrated fanout InFO RDL with excellent ground shielding capability. The power divider exhibits a -10-dB return loss from DC-67 GHz with an insertion loss of -4.3-dB from 30-67 GHz [43]. The layout of the power divider is shown in Figure 2.28 with its s-parameters.

Several antenna array structures are also demonstrated in literature using T-junction and Wilkinson power dividers for various applications [122–125]. A 28/38 GHz dual-band mm-wave SIW antenna array with electronic band-gap (EBG) structures for 5G applications on Rogers RT/duroid 5880 with 0.254-mm thickness is presented by Ashraf *et al.* [121]. Based on Wilkinson power divider, a four-way structure is realized, which then feeds the dual-band SIW antennas. The FBW covered by this antenna is 1.14% and 5% at 28 and 39 GHz, respectively. The antenna array gain at these frequency bands is 11.9-dBi and 11.2 dBi. The size of the power divider is 27.5×20 mm^2. The substrate stackup, layout, response and radiation pattern of this antenna array is shown in Figure 2.29. Similarly, Juo-Sheng *et al.* have reported a 2×2 stacked patch antenna array on a six-layer LTCC stackup with opposite-side feeding structure covering 10.1% bandwidth (26.75-29.6 GHz) [126].
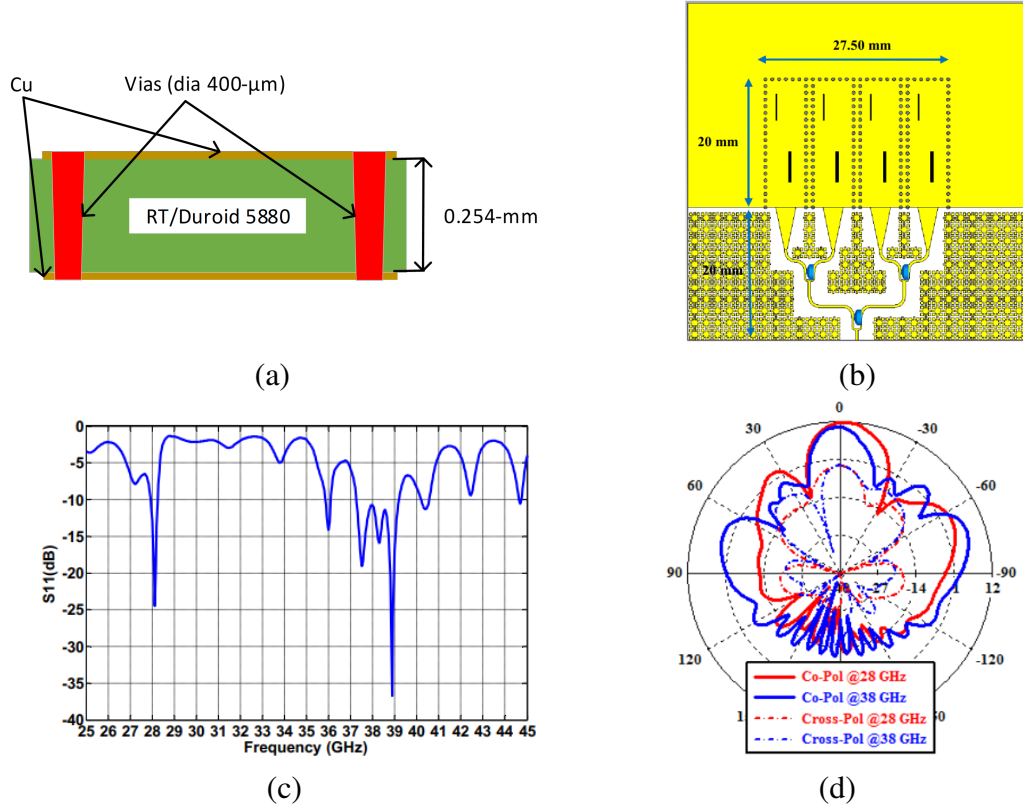
Figure 2.29: A 28/38 GHz dual-band mm-wave SIW antenna array (1×4) with EBG structures (a) substrate, (b) layout, (c) response, and (d) E-plane radiation pattern at 28 and 38 GHz [121].

2.4   Prior Art: Millimeter-Wave Diplexers

A diplexer is the simplest form of a multiplexer, which splits signals from one common port into different paths. It is essentially a frequency-selective power divider as opposed to T-junction and Wilkinson power dividers, which divide on the basis of power-level of the signal. A diplexer is a three-port device. If the roles of input and output ports are reversed, a diplexer can combine two signals at different frequencies onto the common port. Diplexers and multiplexers are most commonly used in communication systems, especially in FEMs where different frequency signals are combined into one line to feed an antenna. Their application in cellular systems boomed with the advent of carrier aggregation (CA) since multiple bands are required to support higher data rates to the end-user. The schematic of

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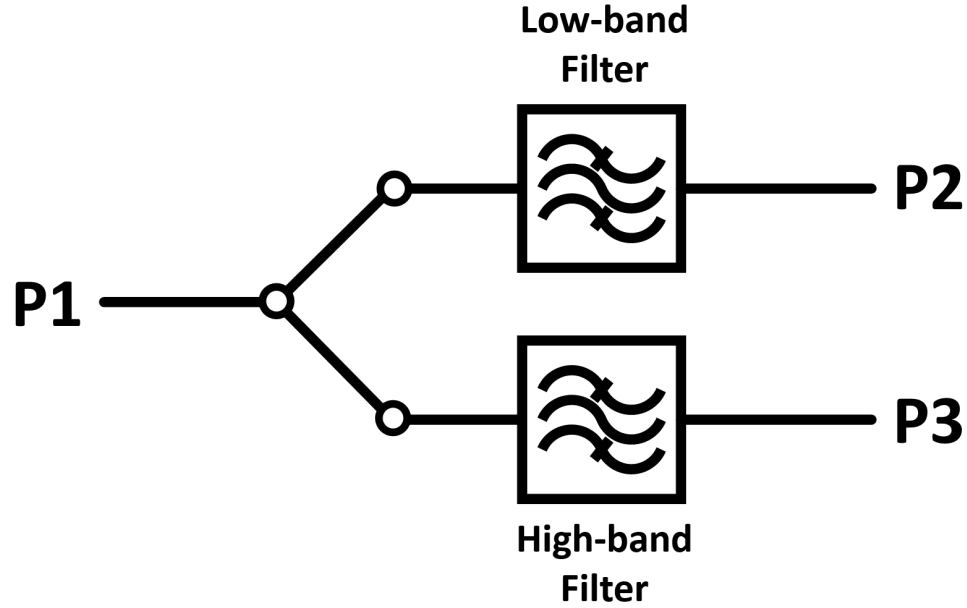
Figure 2.30: Schematic of a diplexer.

a diplexer is shown in Figure 2.30.

A diplexer can be constructed using a lowpass and a highpass filter or using two BPFs, depending upon the requirements. Contiguous diplexers have the common cut-off at 3-dB insertion loss whereas any other common insertion loss value diplexers fall under the category of non-contiguous diplexers. Singly-terminated filters with different source and load impedances are commonly used for contiguous diplexers. They can also be used for non-contiguous diplexers. Standard or classic doubly-terminated filters with same characteristic impedance at both ports are used to realize diplexers if frequency-spacing between two filters is enough to prevent them from loading each other.

The performance metrics of a diplexer are its insertion loss, return loss, out-of-band rejection and isolation between two channels. A comparison of different technologies used to design planar RF diplexers is given in Table 2.2 [127]. A few planar diplexers reported in literature for 5G mm-wave frequency range on various technologies are discussed in this section.

A novel high-performance mm-wave planar diplexer based on complementary charac-

Table 2.2: Comparison of different technologies used to design planar RF diplexers.

Metrics	Planar Diplexers	Quasi-Planar Diplexers	SAW/BAW Diplexers	SIW Diplexers
Frequency	0.5-100 GHz	5-100 GHz	10 GHz	0.5-100 GHz
Q-factor	Low	High	Very High	High
Size	Small	Large	Small	Moderate
Power Handling	Low	High	Moderate	Low
Reproducibility	Excellent	Requires Tuning	Excellent	Requires Tuning

teristics of SIW dual-mode filters with circular and elliptic cavities by making trade-offs between isolation, insertion loss and selectivity, is reported by Tang *et al.* [128]. Based on complementary response of cavities, a high performance diplexer is designed with upper and lower passbands at the center frequency of 25 and 26 GHz. The proposed diplexer is fabricated using standard PCB process on Rogers RT/duroid 5880 with 0.5-mm thickness. The FBW at the upper and lower passband frequency is 5.2% and 5.4%, respectively. The measured insertion loss of this diplexer in these bands is 1.95 and 2.09-dB with isolation more than 50-dB. Another ultra-broadband contiguous planar DC-35-65 GHz diplexer using suspended stripline technology is presented by Ashiq *et al.* [129]. The diplexer has two channels: lowpass channel covers DC-35 GHz whereas highpass channel covers 35-65 GHz frequency range. The substrate for the fabrication of this diplexer is Rogers RT/duroid 5880. The insertion loss of this diplexer is 1.3-dB at 65 GHz and the cross-over point of the filters is at 5-dB. The stackup, response and fabricated coupons of this diplexer are shown in Figure 2.31.

Another work using stripline substrates compact mm-wave diplexer with two modified hairpin filters is presented by Nan *et al.* [130]. The second order hairpin filters are modified to reduce their footprint as well as produce a transmission zero on lower and upper side of the passband. The utilized substrate has a dielectric constant of 2.6 with a 0.32-mm
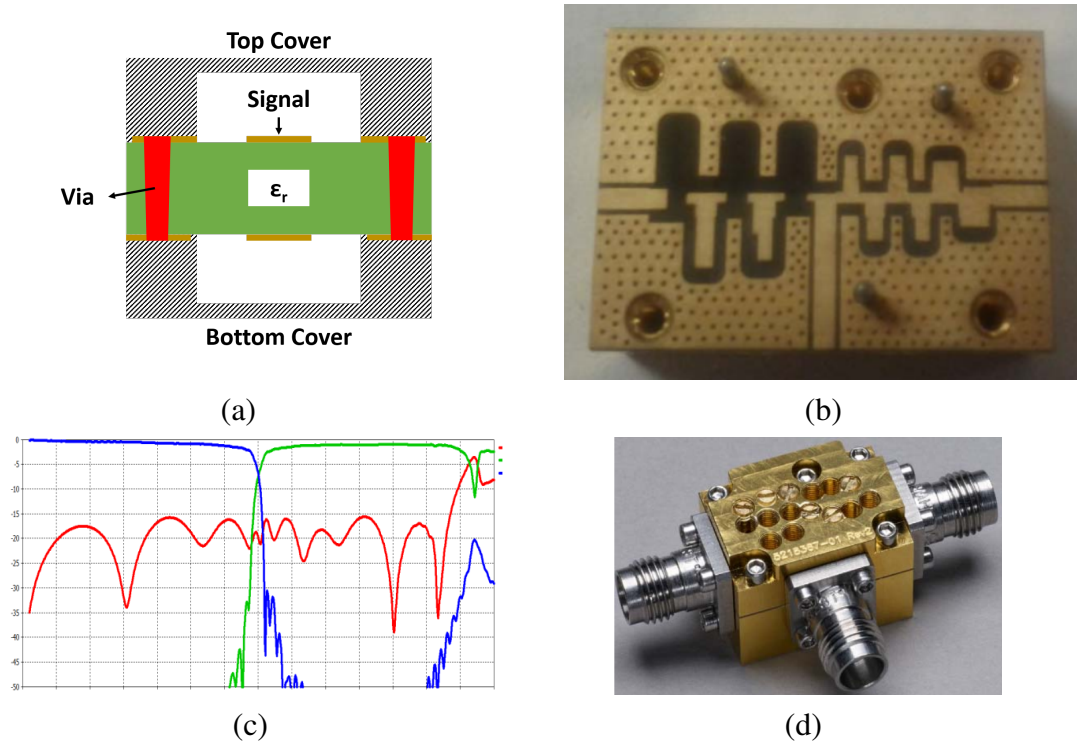
Figure 2.31: A LPF-HPF contiguous diplexer on suspended stripline (a) stackup, (b) fabricated diplexer, (c) response, and (d) assembled diplexer [129].

thickness. The center frequency of lower and upper band is 26.5 and 40.5 GHz with FBW of 6.6% and 5.6%, respectively. Both bands have insertion loss less than 1.5-dB with better than 30-dB isolation. The size of this diplexer is smaller than 2.73×3.06 mm^2. Similarly, a mm-wave microstrip diplexer using elliptical open-loop ring resonators (OLRR) for 14/28 GHz bands is reported by Shaman *et al.* [131]. This diplexer consists of 14 and 28 GHz BPFs utilizing elliptical OLRRs which couple two microstrip lines acting as input and output ports. The geometry of OLRRs can be easily configured to achieve desired center frequency and bandwidth. This diplexer is fabricated on Rogers RT/duroid 5880 substrates with thickness of 0.127-mm. The authors report insertion loss of 1.9 and 4.7-dB at 14.5 and 28.2 GHz, respectively.

Finally, large frequency ratio dual-/tri-band BPFs and diplexers to support the coexistence of microwave and mm-wave technologies is reported in Zheng *et al.* [132]. The authors have explored the use of a new aperture coupling mechanism to combine two band-

pass elements for dual- and tri-band operation with large frequency ratio without significant difference in physical size of the filters. The selected substrate for this demonstration is Rogers RT/duroid with 0.508-mm thickness. First, a combined third-order LPF and second-order $\lambda/4$ single-inline resonator-based BPF is presented which achieves a very wide stopband. The impedance ratio of $\lambda/4$ SIR BPF is adjusted in such a way to achieve a wide stopband and it is further enhanced by combining a LPF with it in series. The center frequency of BPF is 2.36 GHz with FBW of 17.8%. The combined filter has a stopband upto 14.8×center frequency of the BPF with 22-dB out-of-band attenuation. Now the third order mm-wave BPF based on air-filled SIW with circular cavities is designed. This filter has a center frequency of 30 GHz with 6% FBW. The physical designs of these filters: microstrip for microwave filter and air-filled SIW for mm-wave, enables stacking of mi-
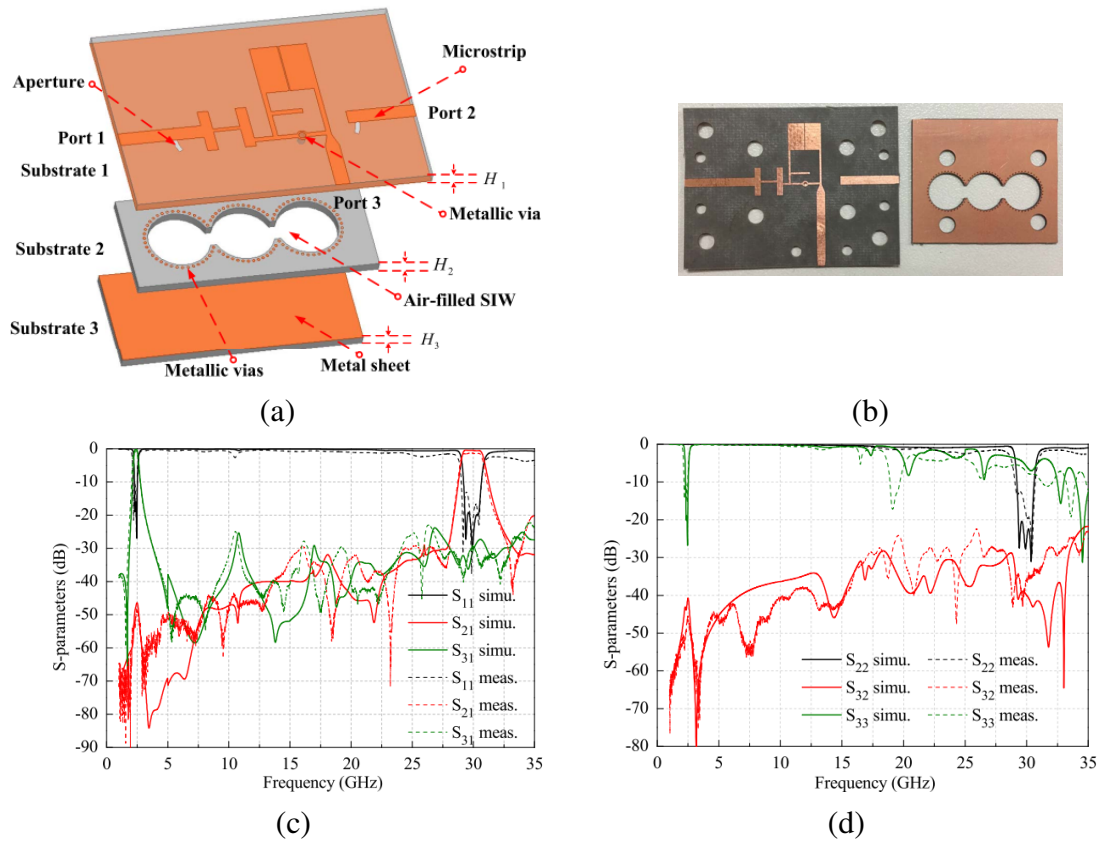
Figure 2.32: A novel diplexer with large frequency ratio (a) 3D layout, (b) fabricated diplexer, (c) and (d) response [132].

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crowave filter on top of the mm-wave filter, thus reducing footprint. The measured center frequencies of low- and high-band are 2.35 and 29.87 GHz with 19.15% and 6.29% FBW, respectively. Owing to the large frequency ratio of these filters, they have almost negligible effect on each other, resulting in a diplexer with large frequency ratio (29.87/2.35 = 12.71), low insertion loss (0.94 for low-band and 1.32 for high-band), better than 22-dB isolation and 39.59×29.26 mm^2 is achieved. The significance of this approach is its scalability to tri-band operation as the low-band filter can be replaced with a dual-band filter to achieve the desired performance. The diplexer is shown in Figure 2.32 along with its response. Some advancements using single/multiple-band coupled-line filtering section for RF diplexers, bandpass/bandstop filters and filtering couplers are detailed in [76].

2.5 Summary

A detailed literature review of filters, power dividers and diplexers is presented in this chapter. It is observed that with enhanced communication systems as a driver and advancements in technologies as a support, profound progress has been made in these passive components in terms of electrical performance, miniaturization and functional integration. Several challenges are overcome by adapting the designs and fabrication processes to meet the needs of various equipment used in a communication system: from base stations to user equipment. However, some challenges still remain as each technology has its trade-offs: for example, existing solutions of filtering components with on-chip integration have merits in terms of low interconnect loss and ease-of-integration but they suffer with poor electrical performance, burdening other system components such as amplifiers to compensate for their loss and thus limiting the efficiency. Innovative passive component design, fabrication and integration with co-development of material technologies is the way forward to meet the stringent performance requirements of 5G and beyond systems.

CHAPTER 3

DESIGN AND DEMONSTRATION OF MINIATURIZED FILTERS AND POWER DIVIDERS

This chapter presents the design and demonstration of miniaturized filters and power dividers along with corresponding antenna arrays. The objective is to model, design, fabricate and characterize filters and power dividers for 5G and mm-wave applications on advanced substrates, enabled by design and technology advances in precision low-loss thin-film passives on laminated ultra-thin glass. These components can be either fabricated as standalone components or integrated in packages as IPDs.

The first half of this chapter presents modeling and design of miniaturized lowpass and bandpass filters. The electrical design procedure and fabrication process are discussed in detail. This is followed by an elaborate fabrication process with required considerations and optimization of each step to ensure excellent model-to-hardware correlation. Next, characterization methodology is presented and model-to-hardware correlations are studied. Dimensional analysis is also performed to extract electrical dimensions from physical dimensions. Finally, the filters are compared with prior art in terms of their electrical performance and footprint to show their superiority in both.

The second half of this chapter adopts the same pattern to discuss power dividers. They are also configured as antenna arrays. The miniaturization objective is limited by the required spacing between the output ports of the power dividers since they are designed to be configured as antenna arrays.

3.1 5G Filters

An RF filter belongs to one of the classifications of electronic filters and it is designed to pass desired frequencies while blocking the undesired ones. A filter is one of the key

passive components in an RF system in both transmitters and receivers. It is also used as a building block to realize multiplexers. There are four basic types of filters:

- Lowpass filter (LPF): allows frequencies below the cut-off frequency

- Highpass filter (HPF): allows frequencies above the cut-off frequency

- Bandpass filter (BPF): allows a desired band of frequencies

- Bandstop filter (BSF): blocks a desired band of frequencies

Their response is shown in Figure 3.1. In this research, the focus is on LPFs and BPFs only.

There are several technologies to fabricate filters. Some of them are listed below:

- Crystal resonators

- Acoustic Wave: SAW, BAW, BAW-SMR and FBAR

- Discrete LC or Lumped elements
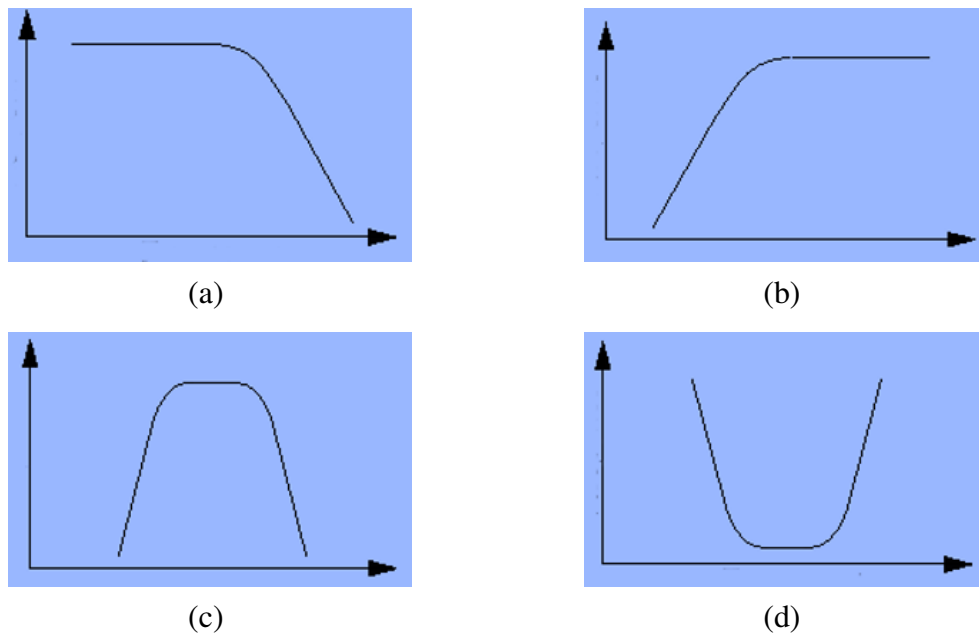
Figure 3.1: Types of filters (a) lowpass, (b) highpass, (c) bandpass, and (d) bandstop
Magnitude (Y-axis) vs. Frequency (X-axis)

- LTCC

- Organic laminates

- Cavity

- Waveguide

Another important aspect of filters is their electrical performance and how it is used to discriminate between filters. The figure of merit of filters are listed as follows:

- Insertion loss

- Return loss/VSWR

- Bandwidth

    - Passband

    - Stopband

- Order

- Stopband attenuation/rejection

- Roll-off factor/selectivity

- Amplitude Ripple

- Cut-off Point

- Q-factor

- Temperature Stability

- Group Delay

The technical challenges and tasks to address the technical challenges for 5G filters have been discussed in detail in Chapter 1. The objectives of 5G filters research task is to model, design, fabricate and characterize filters covering 5G mm-wave bands with less than 2.6-dB insertion loss, more than 30-dB out-of-band attenuation and to achieve a footprint smaller than $2\lambda_0 \times 2\lambda_0$, where λ_0 corresponds to the free-space wavelength corresponding to the 28 and 39 GHz band frequencies. The frequency range and FBW of the 5G mm-wave bands is given below:

- US 28 GHz: 24.5-29.5 GHz (FBW = 18.52%)

- EU 39 GHz: 37.0-43.5 GHz (FBW = 16.15%)

The filters discussed in this section cover the entire 28 and 39 GHz bands. All of the filters are designed using microstrip transmission line structures.

3.1.1 Material Stackup

In this section, the material stackup for 5G filters is discussed. The material stackup is shown in Figure 3.2. For this demonstration, the core substrate is 150×150 mm^2 EN-A1, 100-μm thick glass substrate from Asahi Glass Company (AGC). A 72.5-μm thick epoxy film from Ajinomoto (ABF GL102) is chosen as buildup dielectric for filter structures. The electrical properties of these materials are given in Table 3.1. For a test panel, the glass substrate was replaced by 200-μm thick BT laminate. The polymer film is laminated on both sides of the panel to avoid warpage. The thickness of conductor (copper) is selected to be 8-μm, which is sufficiently thicker than five times the skin depth at frequencies as high as 50 GHz. The skin depth at 50 GHz is 0.3-μm.

Finally, conformal blind via diameter is chosen to be the industry standard of 60-μm, which gives an aspect ratio (substrate thickness/via diameter) of 1.2 for plating. The minimum center-to-center via pitch is twice the via diameter (120-μm). This material stackup is
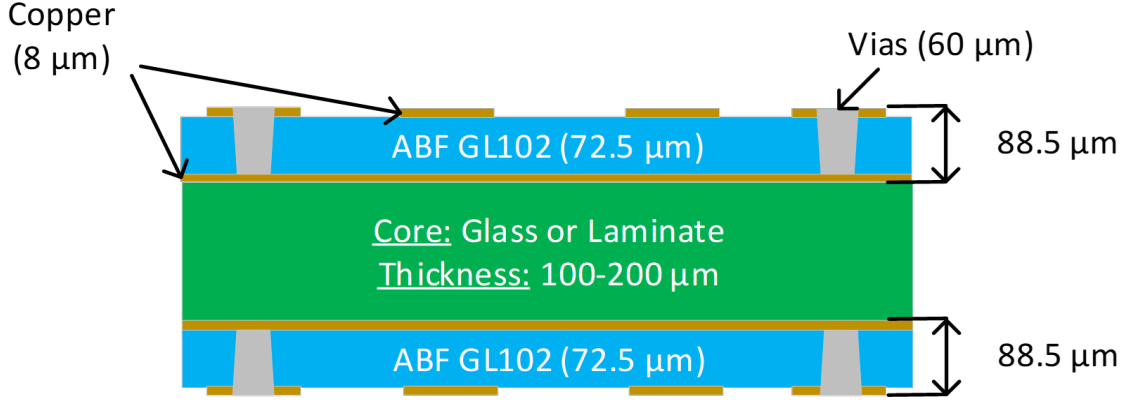
Figure 3.2: Material stackup for 5G filters.

used in simulation using Keysight PathWave Advanced Design System (ADS) for all filters
in this demonstration [133].

3.1.2   Design of Lowpass Filters

The transfer function of a two-port network such as a filter describes its response character-
istics. The numerator and denominator of this transfer function translate to zeros and poles
on the complex plane and for a passive network such as filter to be stable, these poles need
to be on the left half of the plane. Different types of transfer function responses are given
below:

- Butterworth or Maximally Flat response

- Chebyshev response

- Elliptic Function response

Table 3.1: Electrical properties of materials in 5G filters stackup.

Material	Dielectric Permittivity (ε_r / Dk)	Loss Tangent (tan δ / Df)	Characterization Frequency
AGC EN-A1	5.4	0.0056	10 GHz
ABF GL102	3.3	0.0044	5.8 GHz

- Gaussian or Maximally Flat Group-Delay Response

- All-pass response

We will consider the first three types: Butterworth, Chebyshev and elliptic. The low-
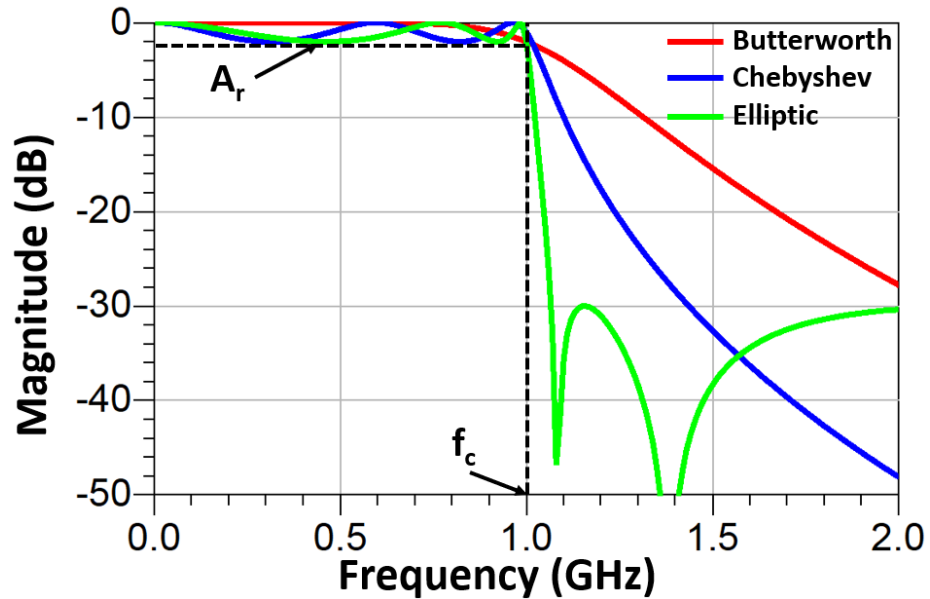
(a)
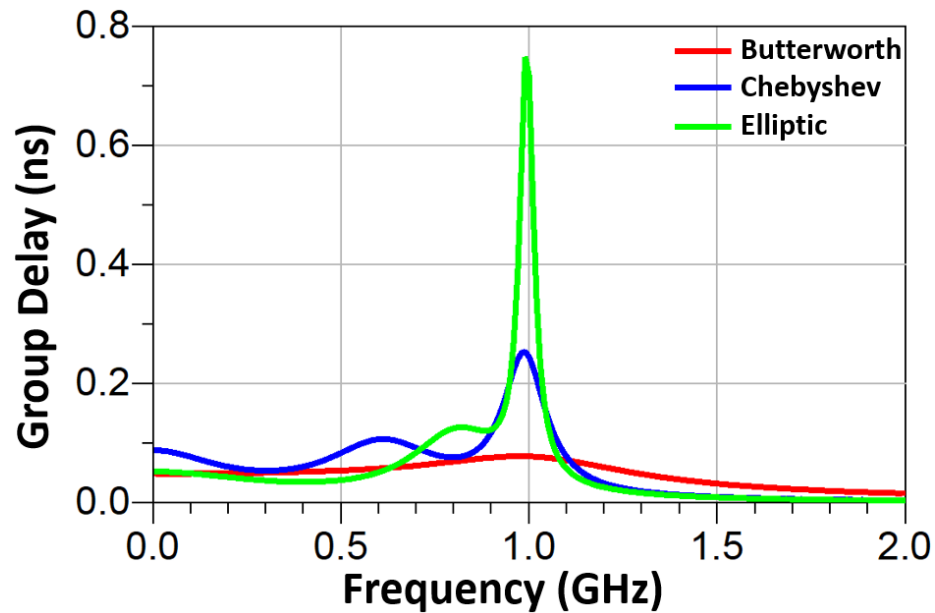
(b)

Figure 3.3: Different types of lowpass filter responses: (a) Butterworth, Chebyshev and elliptic, and (b) their group delay.

pass transfer function of the first three types of transfer function responses along with their group delay are plotted in Figure 3.3. Butterworth response is also referred as maximally flat response because it is flat in the passband as well as in the stopband. The amplitude of insertion loss at cut-off frequency (f_c) of 1 GHz is 3.01-dB. Notice that the negative sign is omitted as the amplitude is linked to insertion loss, which has a maximum value of 1 in linear scale or 0-dB in log-scale. All of the zeros of this response are located at infinity whereas the poles are distributed in a semi-circular pattern on the left half of complex plane. The Chebyshev response exhibits equal-ripple in the passband and has a maximally-flat stopband. The amplitude of ripple is denoted by A_r in Figure 3.3a. Similar to maximally-flat response, zeros of Chebyshev response are located at infinity whereas poles are located on left-half of complex plane along the major axis of a semi-ellipse. The elliptic function response has equal-ripple in both passband and stopband. Unlike maximally flat and Chebyshev responses, these filters have zeros at finite frequencies. Comparing the roll-off of these three responses in Figure 3.3a, the elliptic response has the sharpest roll-off. But it comes at the cost of increased group delay as shown in Figure 3.4b. To summarize, the roll-off sharpens from maximally-flat to elliptic response for the same order but the trade-off is amplitude ripple as well as increased group delay.

Lowpass Filter Prototype for All-Pole Response

To realize the aforementioned all-pole response, the resultant network is a so-called low-pass prototype filter [134]. Its values are normalized to source resistance of 1-Ω, denoted by $g_0 = 1$, and the cut-off angular frequency, measured in rad/s, is also set to be unity. Further elements in this network are denoted by g_i for $i = 1$ to n where n corresponds to the order of the filter. The ladder network is shown in Figure 3.4a. represents a lowpass prototype to realize Butterworth and Chebyshev filters. Its dual network is shown in Figure 3.4b. g_i represents either a shunt capacitor (C) or a series inductor (L) since the networks are equivalent to each other and will give the same response. The most basic form of LPFs
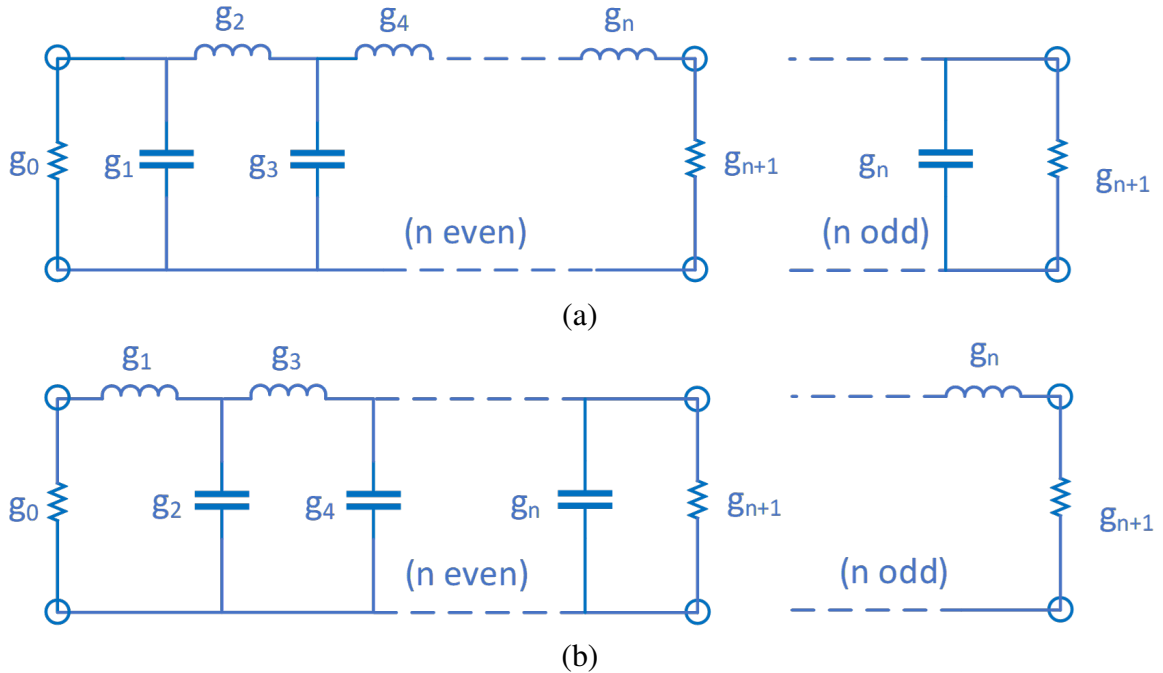
Figure 3.4: Lowpass prototype filters to realize all-pole filter responses: (a) a ladder network, and (b) its dual.

using LC discrete components can be designed using these networks.

Lowpass Filter Prototype for Elliptic Response

The response selected for lowpass filters for 5G is elliptic transfer function response. The reason for this selection is that steepest roll-off factor is provided by this transfer function as compared to maximally flat and Chebyshev types. The passband ripple can be minimized to meet certain specification and stopband ripple can be designed in such a way that it is below a specified level. The structures chosen for lowpass filter are elliptic/semi-lumped with finite-frequency infinite-attenuation poles. A n-th order lumped element lowpass prototype of elliptic function LPFs is shown in Figure 3.5. The procedure to design these lowpass filter structures is summarized below:

1. Find filter order (n) based off desired attenuation in stopband.

2. Select g-values for the desired order. g-values are unity-impedance unity-frequency values for a lowpass filter prototype.
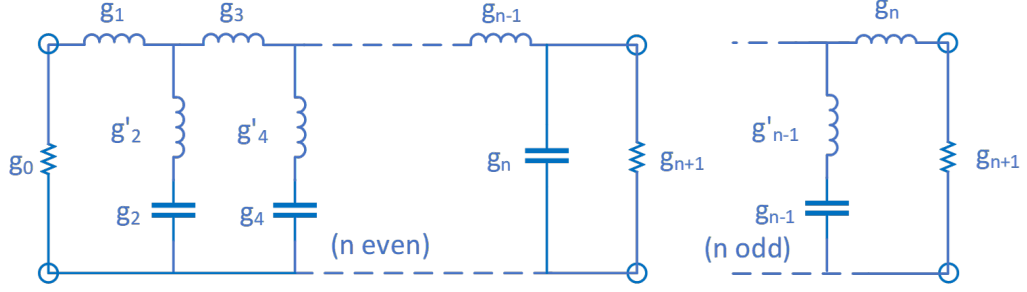
Figure 3.5: A nth-order elliptic lumped-element lowpass prototype filter with series parallel-resonant branches.

3. Scale g-values to desired impedance and frequency to find L & C values using Equation (3.1).

$$L_i = \frac{1}{2\pi f_c} Z_0 g_{Li}$$
$$C_i = \frac{1}{2\pi f_c} \frac{1}{Z_0} g_{Ci}$$

(3.1)

where, f_c = cut-off frequency of lowpass filter,

Z_0 = characteristic impedance (usually 50-Ω),

Z_{Li} =g-values of the filter corresponding to inductors,

Z_{Ci} = g-values of the filter corresponding to capacitors.

4. Equation (3.2) can be used to find physical length corresponding to each lumped L & C for microstrip structure.

$$l_{Li} = \frac{\lambda_{gL}(f_c)}{2\pi} \arcsin(2\pi f_c \frac{L_i}{Z_{0L}})$$
$$l_{Ci} = \frac{\lambda_{gC}(f_c)}{2\pi} \arcsin(2\pi f_c Z_{0C} C_i)$$

(3.2)

where, $\lambda_{gL}(f_c)$ and $\lambda_{gC}(f_c)$ are guide wavelengths corresponding to L and C at the cut-off frequency,

Z_{0L} = characteristic impedance of the inductor ($> Z_0$),

Z_{0C} = characteristic impedance of the capacitor ($< Z_0$),

Z_{0L} and Z_{0C} are the choice of designer as they physically correspond to width of transmission lines (microstrip) to be fabricated.

5. Apply required compensations for unwanted reactance/susceptance at the junction of inductive line elements as shown in Figure 3.6b.

6. Simulate and optimize in Keysight PathWave ADS Schematic and Momentum.

7. Finalize layout: Add ground pads (GSG) for testing, connect GSG ground planes through a rectangular path and make a boundary to define filter size.

Using this method, the following LPFs are modeled, simulated and optimized:

- 28 GHz band (f_c = 29.5 GHz): 5th, 7th and 9th order.

- 39 GHz band (f_c = 43.5 GHz): 5th, 7th and 9th order.

As an example, the circuit schematic of a fifth-order semi-lumped LPF along with its microstrip realization is shown in Figure 3.6. The design procedure of LPF for 28 GHz 5G band is described here. The process starts with g-values which can be obtained from [135, Chapter 3]. The g-values are for A_r = 0.1-dB and stopband insertion loss (L_{As}) of 39.5947-dB at 1.4085 times the cut-off frequency. The ratio of stopband attenuation
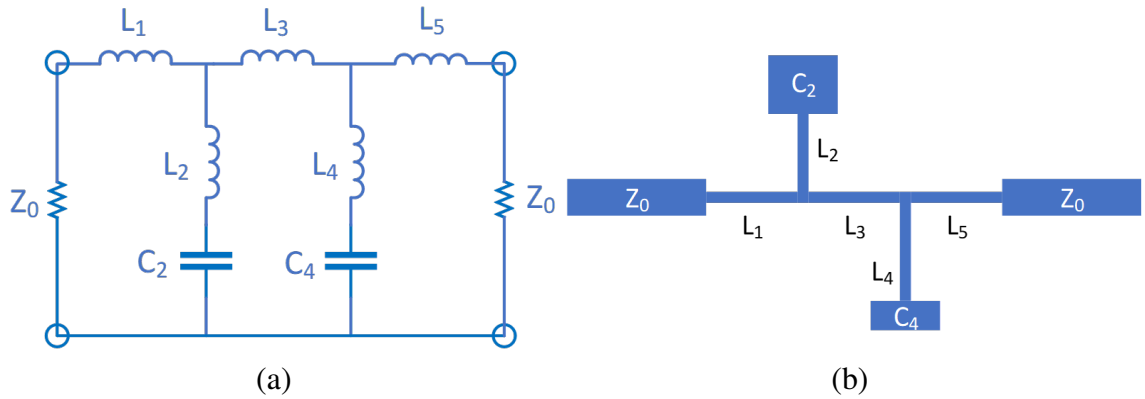
Figure 3.6: A fifth-order elliptic LPF (a) lumped-element prototype, (b) its microstrip realization.

Table 3.2: Scaled g-values of fifth-order elliptic LPF.

g-value	g-value (referred to Z, L or C)	Scaled Z, L or C
$g_0 = g_6$	$Z_0 = 1$	50-Ω
g_1	$L_1 = 1.0058$	0.2713-nH
g_2	$C_2 = 1.1862$	0.128-pF
g_2'	$L_2 = 0.1816$	0.049-nH
g_3	$L_3 = 1.5771$	0.4254-nH
g_4	$C_4 = 0.8638$	0.0932-pF
g_4'	$L_4 = 0.5436$	0.1466-nH
g_5	$L_5 = 0.7578$	0.2044-nH

frequency to cut-off frequency is denoted as Ω_s. The g-values are listed in Table 3.2. They are also scaled to characteristic impedance of 50-Ω and cut-off frequency of 29.5-GHz using Equation (3.1) to obtain L & C values for the circuit shown in Figure 3.6a. The simulated response of the circuit using LC values given in this Table 3.2 is shown in Figure 3.7.

As evident from Figure 3.7, the response of LC network is as expected but needs fine
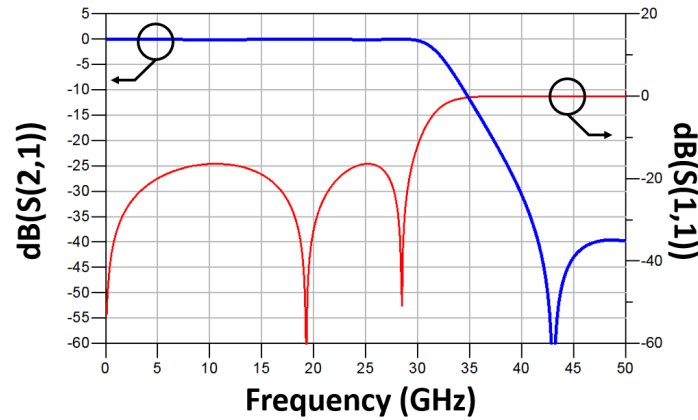
Figure 3.7: Simulated response of LC circuit of fifth-order elliptic LPF for 28 GHz 5G band.

tuning to further improve the return loss. Instead of optimization at this stage, the filter is first converted to a detailed model in ADS which primarily captures the microstrip junction effects as well as open-ended transmission line effects of capacitors. The L & C values are transformed to microstrip by using Equation (3.2): Z_{0L} and Z_{0C} are appropriately selected and line lengths are evaluated corresponding to each L & C. The microstrip realization of this LPF is shown in Figure 3.6b. Selection of Z_{0L} is more critical since its approximates inductors and it is the smallest line width. However, selecting a higher Z_{0L} translates to thinner lines which can be difficult to process during fabrication as well as testing because of smaller width. The power handling of thinner lines is also lower. The

Table 3.3: Optimized design parameters of fifth-order LPF for 28 GHz 5G band.

Parameter	Value
Cut-off Frequency	29.5 GHz
Insertion loss at cut-off frequency	$<$2-dB
Highest impedance: Inductor (Z_{0L})	100.53-Ω
Line Width: Inductor (W_{0L})	35.90-μm
Lowest impedance: Capacitor (Z_{0C})	27.20-Ω
Line Width: Capacitor (W_{0C})	399.80-μm
Line Width: 50-Ω	162.34-μm
Line Length: 50-Ω	1000-μm
Line Length: L_1	328-μm
Line Length: C_2	358.1-μm
Line Length: L_2	228.1-μm
Line Length: L_3	812.6-μm
Line Length: C_4	282.6-μm
Line Length: L_4	363.4-μm
Line Length: L_5	303.9-μm
Filter dimensions (Physical)	3.44 $\times$ 1.35 mm^2

model is then simulated in Momentum and optimized to obtain the desired filter response. Since detailed Momentum simulations can give close-to-practical results, optimization is performed meticulously to meet the specifications. The optimized design parameters of fifth-order LPF for 28 GHz 5G band are given in Table 3.3. The simulation layout of the final filter is shown in Figure 3.8a and the optimized response from Momentum simulations is shown in Figure 3.8.

The simulated insertion loss at the cut-off frequency is 1.43-dB and return loss is more than 20-dB for a large fraction of filter bandwidth. The 30-dB attenuation point to band-

(a)

(b)
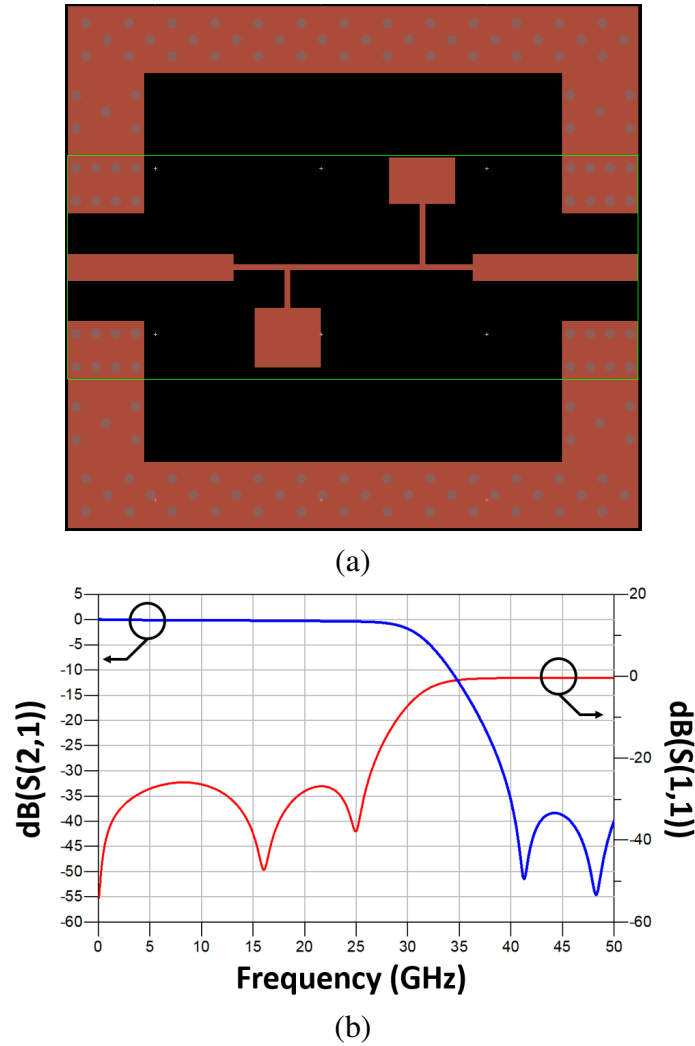
Figure 3.8: A fifth-order LPF for 28 GHz 5G band (a) layout, and (b) simulation results after optimization.

edge ratio is 1.33 and 40-dB attenuation point to band-edge ratio is 1.37 (achieved Ω_s). For this design, the selected g-values have Ω_s of 1.4085 with L_{As} of 39.5947. By comparing the ratios, it is clear that this filter meets the stopband attenuation specification by a margin of more than 1 GHz. The same process is repeated to design seventh- and ninth-order LPFs for 28 GHz 5G band. The layout of seventh- and ninth-order LPFs for 28 GHz 5G bands are shown in Figure 3.9a and 3.9b, respectively. For 39 GHz 5G band with 43.5 GHz cut-off frequency, similar filters are designed. The layout and response of a ninth-order LPF are depicted in Figure 3.10.

The optimized simulated response for all three LPFs for 28 GHz 5G bands is plotted

(a)   (b)

(c)
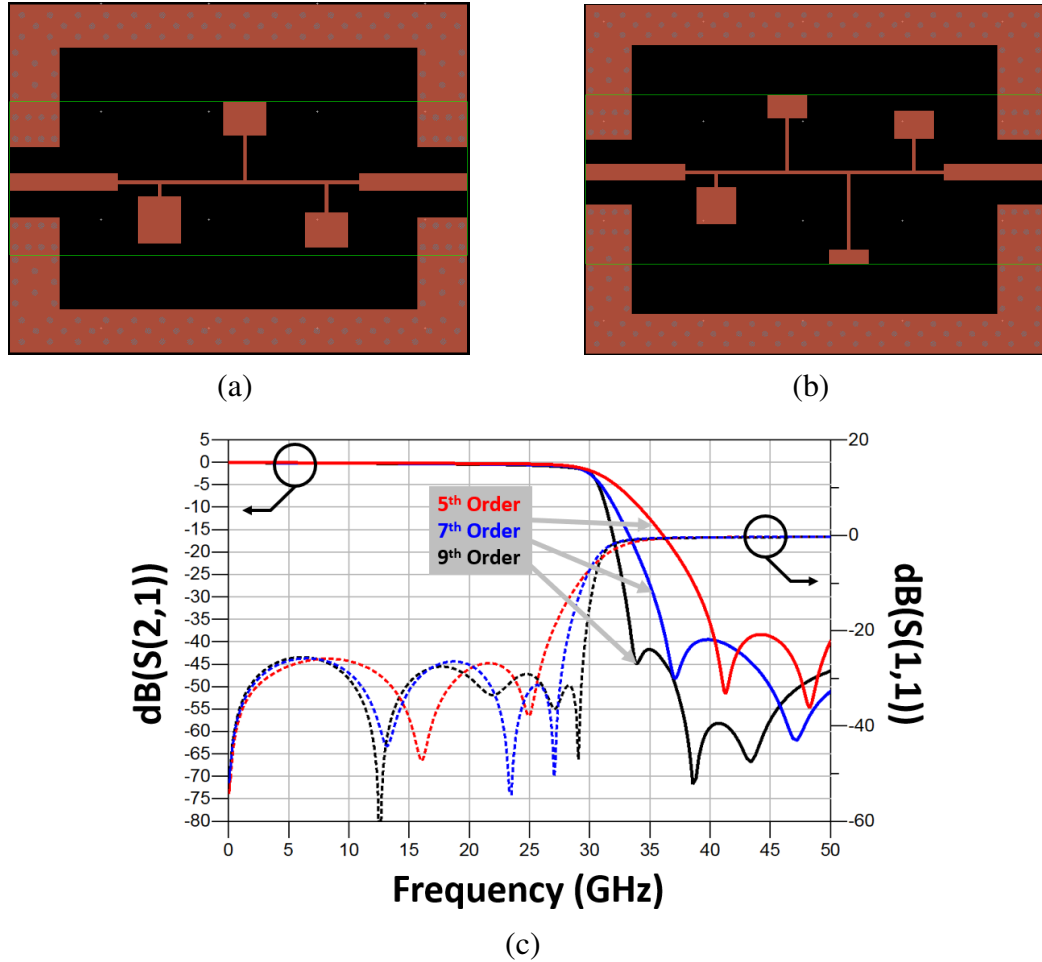
Figure 3.9: Layout of LPFs for 28 GHz 5G band, (b) seventh-order, and (b) ninth-order. (c) Combined simulation results of fifth-, seventh- and ninth-order LPFs after optimization.

84

(a)

(b)
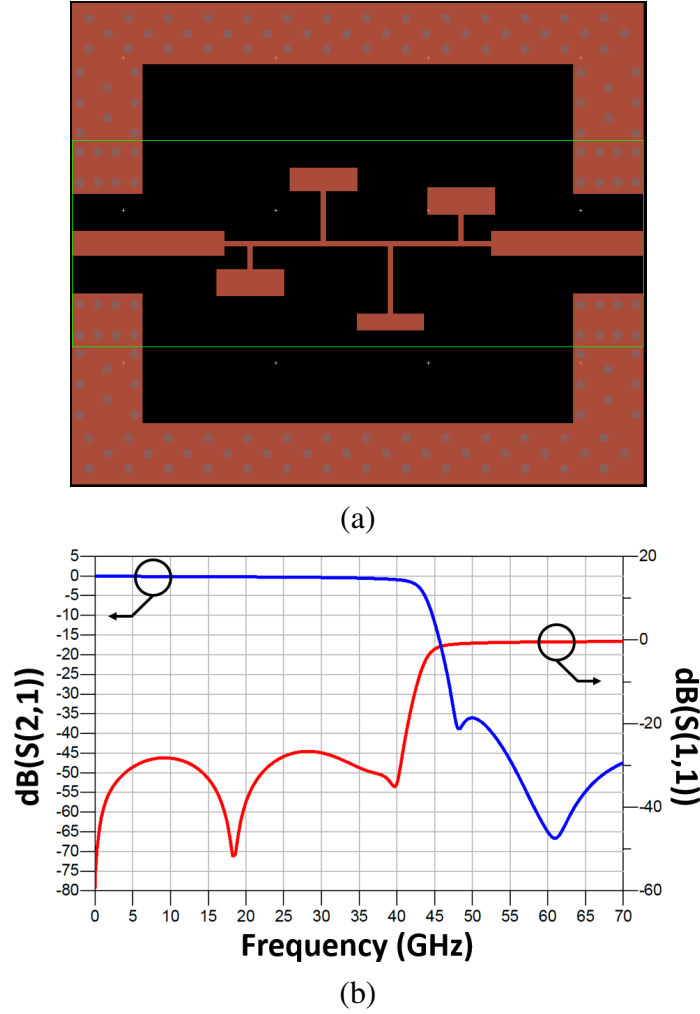
Figure 3.10: A ninth-order LPF for 39 GHz 5G band (a) layout, and (b) simulation results after optimization.

in Figure 3.9c for comparison. As expected, roll-off skirt of the filter increases sharply as filter order is increased.

3.1.3   Design of Bandpass Filters

For the bandpass filters, interdigital and hairpin structures are selected for 28 and 39 GHz bands. Hairpin bandpass filters use parallel-coupled half-wavelength ($\lambda/2$) open resonators, whereas interdigital filters use quarter-wavelength ($\lambda/4$) short resonators, making these structures an ideal choice for small-footprint. The design process of both these filters is given in detail in [134, 135]. A relatively modern technique with explicit design equa-

tions for interdigital filters is given in [136]. It is to be noted that resonators for hairpin and interdigital filters have fixed width, and spacing between resonators is adjusted to obtain the desired response. Both interdigital and hairpin filters have tapped input and output resonators for feeding and are designed using Chebyshev polynomial g-values with 0.1-dB ripple. The following filters are designed for this demonstration:

- Hairpin for 28 and 39 GHz bands

    - Third-order

    - Fifth-order

- Interdigital for 28 and 39 GHz bands

    - Third-order

    - Fifth-order

The process of designing a hairpin BPF summarized here. It starts with the specifications of filter: center frequency, ripple, FBW and order. The specifications of the filter is to be designed for 28 GHz band are: FBW of 18.52%, 0.1-dB ripple and third-order response. The g-values of lowpass prototype can be obtained from [135, Chapter 3]. These values are: $g_0 = g_4 = 1$, $g_1 = g_3 = 1.0316$ and $g_2 = 1.1474$. Using these values, the bandpass filter design parameters can be calculated from the following equations:

$$Q_{e1} = \frac{g_0 g_1}{FBW} \tag{3.3}$$

$$Q_{en} = \frac{g_n g_{n+1}}{FBW} \tag{3.4}$$

$$M_{i,i+1} = \frac{FBW}{\sqrt{g_i g_{i+1}}} \quad \text{for } i = 1 \text{ to } n - 1 \tag{3.5}$$

where Q_{e1} and Q_{en} are the external quality factors of the input and output resonators and $M_{i,i+1}$ is the coupling coefficient between adjacent resonators. A design equation to estimate the tapping point location (t) for the terminal resonators is as follows:

$$t = \frac{2L}{\pi} \arcsin \left(\sqrt{\frac{\pi}{2} \frac{Z_0/Z_r}{Q_e}} \right) \tag{3.6}$$

where Z_r is the characteristic impedance of the hairpin resonator and L is approximately quarter guide-wavelength ($\lambda_{g0}/4$) corresponding to the center frequency (f_0) of the filter. The layout of a third-order hairpin BPF is shown in Figure 3.11.

Using the Equations (3.3)−(3.5), external Q-factors and coupling coefficients are calculated. The values are: $Q_{e1} = Q_{e3} = 5.158$ and $M_{12} = M_{12} = 0.1622$. These values can now be used in full-wave EM simulations to extract physical dimensions against computed parameters using parameter extraction technique given in [135, Chapter 8]. Q_e can be computed against t and generally Q_e increases as t decreases. Similarly, $M_{i,i+1}$ can be used to compute spacing between resonators to achieve the desired coupling. This methodology is an approximation for a decent starting point. However, iterative optimization of various parameters is still required as the initial filter response needs improvement. The first-pass
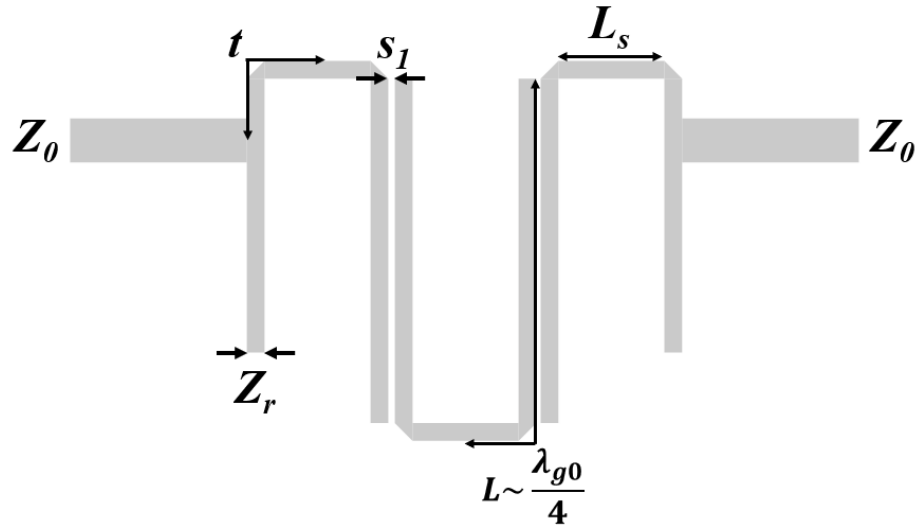
Figure 3.11: Layout of a third-order hairpin BPF with labeled geometry features.

Table 3.4: Design parameters of third-order hairpin BPF for 28 GHz 5G band.

Parameter	Value
Cut-off Frequency	24.5 and 29.5 GHz
Insertion loss at cut-off frequency	$<$2-dB
Z_r	85-Ω
W_r	51.5-Ω
Z_0	50-Ω
L_s	380-μm
L	1840-μm
s	31.5-μm
t	428-μm
Filter dimensions (Physical)	3.26×2.15 mm^2

optimized parameters of third-order hairpin BPF for 28 GHz 5G band are given in Table 3.4. These parameters are then rigorously optimized to obtain the desired filter response which meets the specifications. The layout of this filter along with its simulated response is given in Figure 3.12. Its simulated passband insertion loss is less than 1.5-dB and return loss is more than 20-dB.
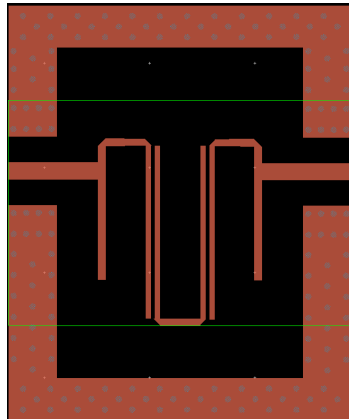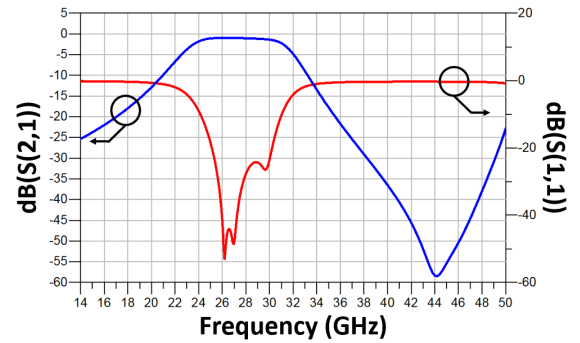
(a)   (b)

Figure 3.12: A third-order hairpin bandpass filter for 28 GHz 5G band (a) layout, and (b) simulation results after optimization.
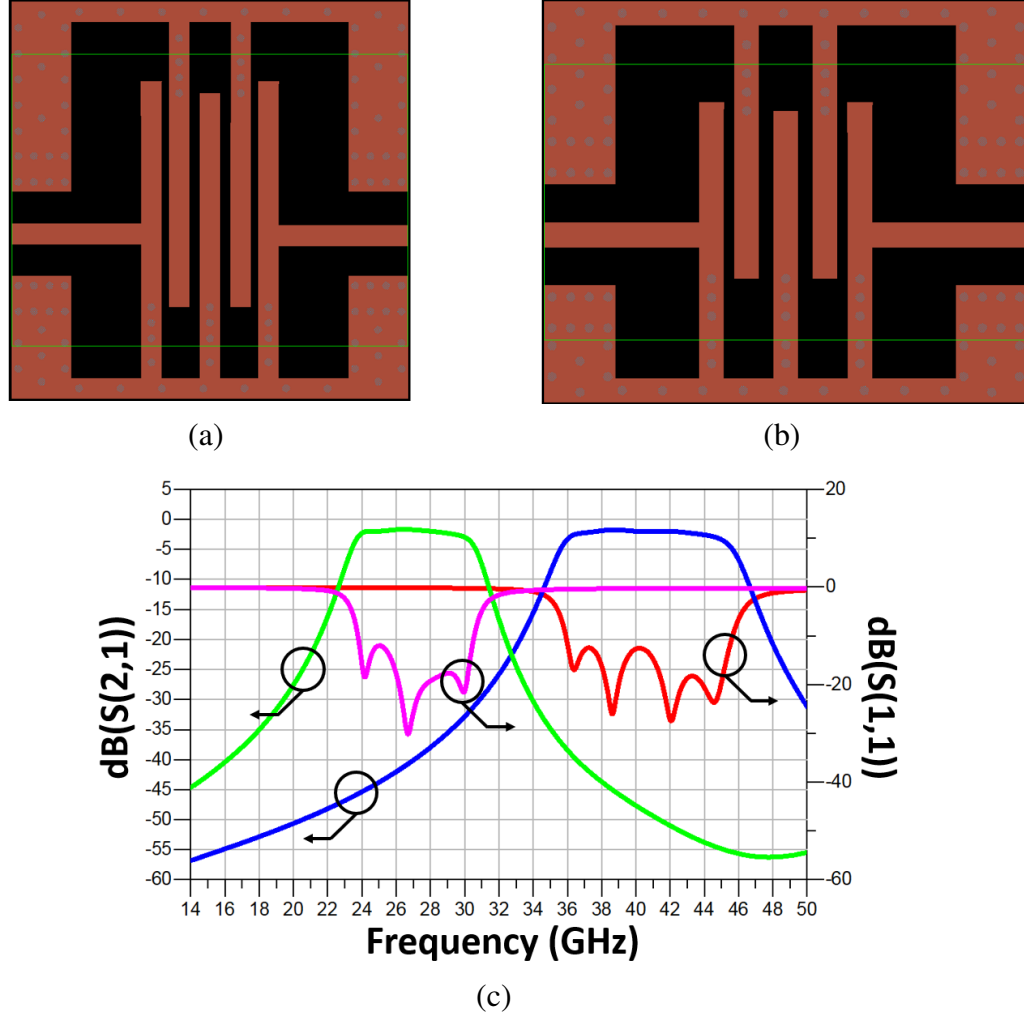
Figure 3.13: Layout of designed fifth-order interdigital BPFs (a) for 28 GHz 5G band, and (b) for 39 GHz 5G band. (c) Combined simulation results of these filters.

Similarly, fixed-resonator width interdigital filters with third- and fifth-order response are designed for 28 and 39 GHz bands. The layout of fifth-order interdigital BPFs for 28 and 39 GHz bands is presented in Figure 3.13a and 3.13b, respectively. Moreover, their simulated response is shown in Figure 3.13c. The simulated passband insertion loss for both filters is less than 2.5-dB with return loss more than 12-dB.

3.1.4 Fabrication Process

The fabrication process utilizes the semi-additive patterning (SAP) process to pattern the copper structures. Figure 3.14 illustrates the SAP process through schematic cross-sections
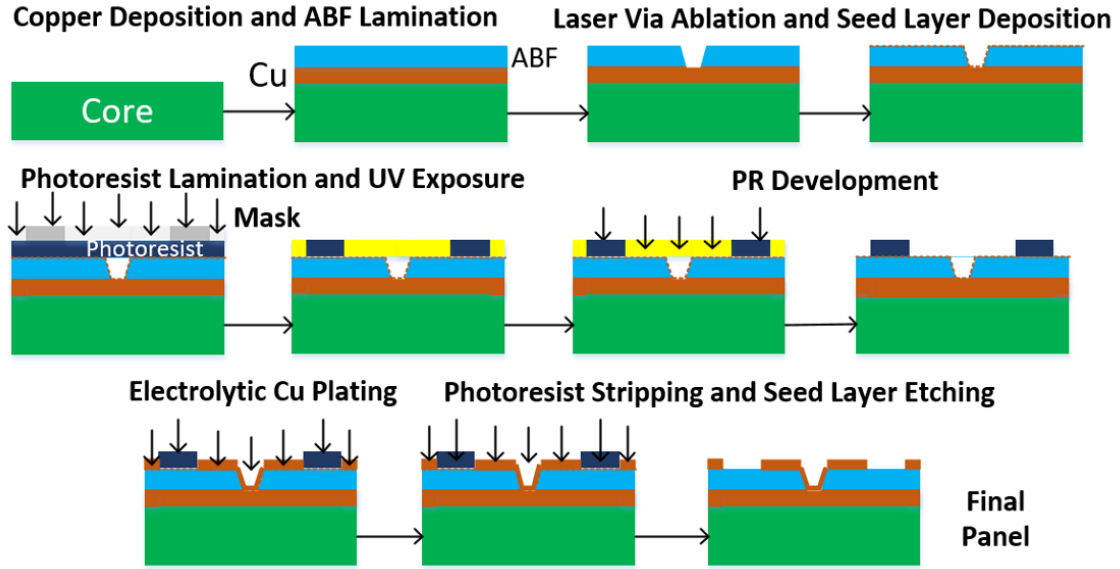
Figure 3.14: Illustration of SAP for fabrication of 5G filters with step-by-step cross sections.

of each step. The process starts with a bare glass panel on which copper is electrolytically deposited. If a copper-clad substrate is used as the core, then the panel is cleaned using O_2 plasma and then its surface is treated by Novabond wet process by Atotech [137]. It is a five step chemical treatment process which improves adhesion of copper to ABF dry-film both chemically and mechanically by forming nano-anchor structures to lock the polymer film. Next, the dielectric film is laminated using a vacuum laminator. This stage also serves as a pre-cure for the film and after lamination, another curing process step is performed in a nitrogen oven. Blind vias are then ablated using a UV laser. This step is very critical as non-optimal laser ablation conditions can damage copper underneath the film, thus affecting electrical performance. The surface roughness at the dielectric-copper interface is very important as the fields are concentrated in that region for microstrip structures.

After via ablation, another plasma step is performed to clean the vias. The process continues to seed layer deposition which involves the setup of chemical desmear and electroless copper plating solutions. The desired seed layer thickness is 0.2-0.4 μm. The first step, chemical desmear, removes residues of polymer left after via-drilling process. The

removal of this residue is necessary as it can affect the quality of copper plating. Secondly, it also roughens the walls of surface of ABF film to enhance copper bond strength. The measured seed layer thickness after this procedure is 0.2-μm with $\pm$0.02 μm variation across the panel. Uniformity of electroless copper deposition ensures uniformness of electrolytically-deposited copper. Similar to lamination of ABF dry-film, a 15-μm dry-film negative photoresist from Hitachi Chemicals is vacuum-laminated on the panel. It is photolithographically patterned using a mylar mask on an exposure tool. The exposure time needs to be optimized carefully to obtain dimensionally-accurate feature size. After exposure, it is advised to settle the panel down for some time before developing. This to ensure proper cross-linking to realize accurate feature size. The developing of photoresist gets rid of unnecessary photoresist. The development speed also needs optimization to support precision features. After photoresist development, the panel is subjected to O$_2$ plasma to remove photoresist residue and improve the wettability of electrolyte on copper. The metalization of traces is performed using electroplating. SAP on a dimensionally-stable core provides excellent dimensional control when a fine feature size is required, such as in this application, which helps in maintaining the rectangular profile of lines as opposed to convex profile achieved after subtractive etching procedures. Moreover, the dimensional control is the result of avoiding long etching intervals and lateral undercuts usually prevalent in subtractive etching. The target copper thickness is 8.2-μm, considering that etching seed layer at the end of the process will lead to target thickness of 8-μm.

Finally, photoresist is removed using a stripper solvent, and seed layer is differentially-etched away to obtain the desired circuit patterns. After fabrication process, the measured copper thickness is 8.5$\pm$0.5 μm. The fabricated panel for 5G filters is depicted in Figure 3.15. Three of the fabricated filters are shown in Figure 3.16.
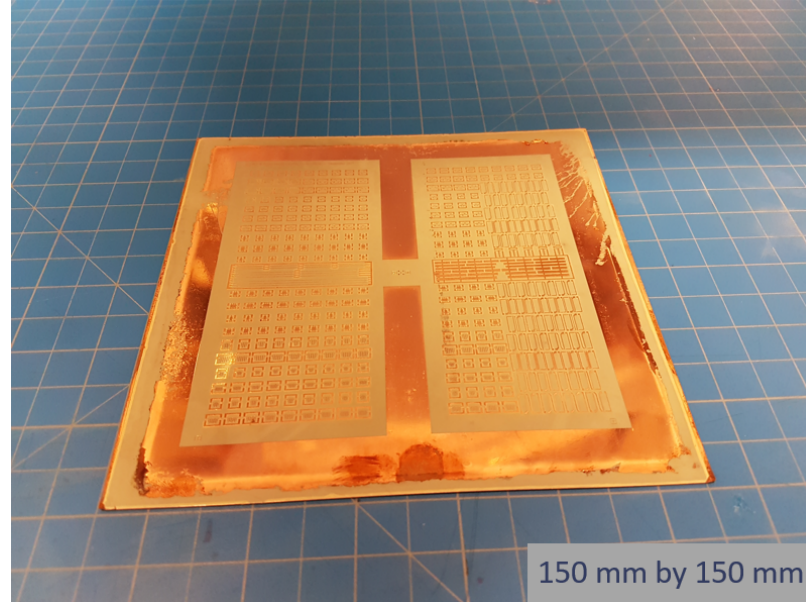
Figure 3.15: Fabricated panel for 5G filters.
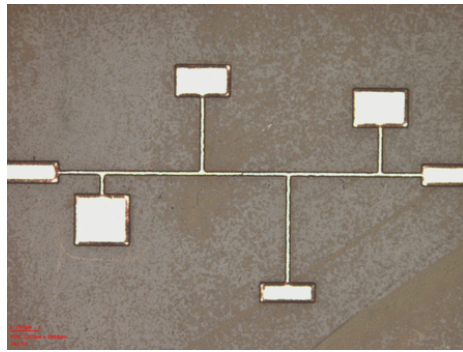
(a)
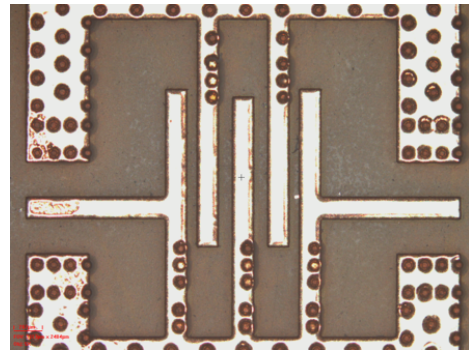
(b)
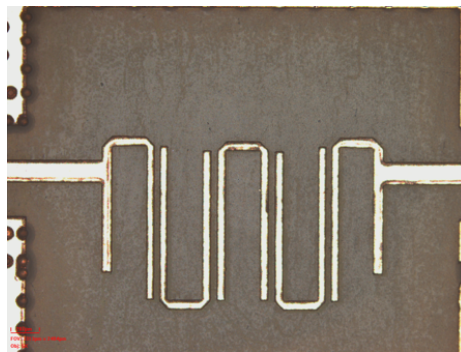
(c)

Figure 3.16: Fabricated filters for 5G mm-wave bands (a) ninth-order LPF for 28 GHz band, (b) fifth-order interdigital BPF for 28 GHz band, and (c) fifth-order hairpin BPF for 39 GHz band.

3.1.5   Characterization Results

In this section, the characterization results of fabricated filters are discussed in detail. The measurements are performed using Keysight E8361C PNA in the frequency range of 14-50 GHz using 500-μm pitch ACP50 GSG probes and short-open-load-through (SOLT) calibration. The measurement results are compared with simulation results to perform a model-to-hardware correlation study.

Lowpass Filters

The measurement results of fabricated fifth-, seventh- and ninth-order LPFs for 28 and 39 GHz bands is shown in Figure 3.17a and Figure 3.17b, respectively. Their simulated results are also plotted to evaluate model-to-hardware correlation. As evident from the Figure 3.17, excellent model-to-hardware correlation is achieved for LPFs operating in both 28 and 39 GHz 5G bands, indicating the accuracy of fabrication process with very strict tolerance.

The measured response of 28 GHz band LPFs shows <2-dB insertion loss at the f_c of 29.5 GHz. The return loss is also more than 20-dB, corresponding to VSWR of less than 1.22, indicating an outstanding impedance match. The ratio of 30-dB attenuation point to band-edge for fifth-, seventh- and ninth-order LPFs is 1.33, 1.2 and 1.16, respectively. For 39 GHz band LPFs with f_c of 43.5 GHz, the lower order filters cannot be fully characterized due to the limitation of available GSG probes as they operate well only up to 50 GHz. The stopband behavior of fifth- and seventh- order filters is not completely characterized but we can see the first transmission zero of ninth-order filter. When compared with simulation, the measured roll-off skirt of all filter closely follows the simulated results. The insertion loss at 43.5 GHz for fifth- and seventh-order LPFs is less than 1.6-dB. For the ninth-order filter, it is designed to have more around 4-dB insertion loss at f_c and as evident from Figure 3.17b, it achieves that result. All LPFs have better than 20-dB return loss in a large fraction of bandwidth. The 30-dB attenuation point to band-edge ratio for fifth-, seventh- and ninth-order LPFs is 1.36, 1.19 and 1.09, respectively. For fifth- and seventh-

order filters, since the 30-dB attenuation points cannot be measured due to upper limit of measurement frequency, the ratios are calculated using simulated results since the measured results track very closely with them.

(a)

(b)
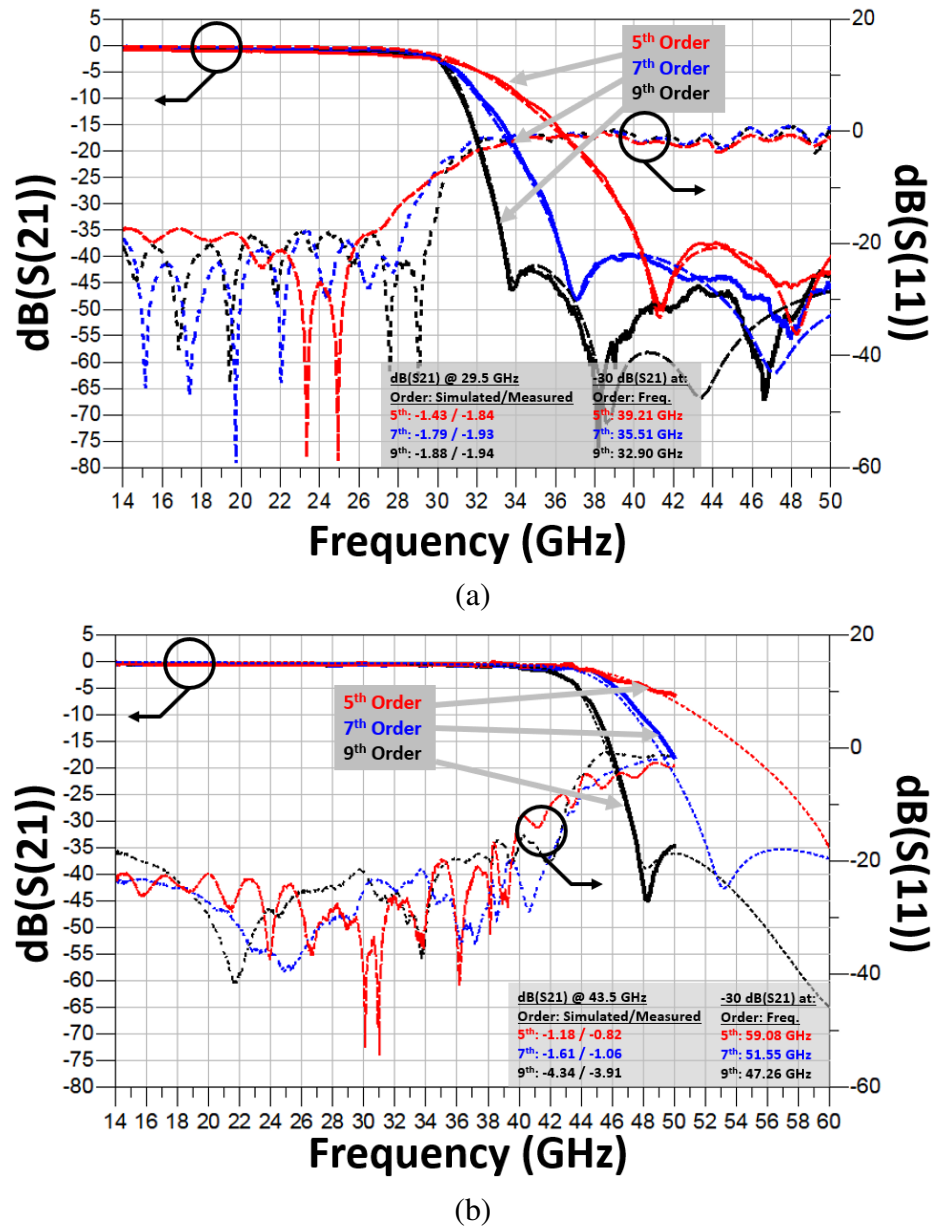
Figure 3.17: Comparison of simulated and measured fifth-, seventh- and ninth-order LPFs (a) for 28 GHz band, and (b) for 39 GHz band.

Results: Bandpass Filters

The comparison of simulated and measured results of fabricated third- and fifth-order interdigital BPFs are depicted in Figure 3.19a and 3.19b, respectively. As evident from these figures, filters exhibit more bandwidth than their simulated versions and are slightly shifted in frequency. This is attributed to slight increase in resonator width during exposure in the photolithography step. The dose time is optimized for small line widths only. Due to this optimization, the wider resonator traces such as in interdigital filters, are affected and spacing between the resonators decreases resulting in a slightly wider bandwidth. However, despite this effect, the fabricated third-order filters show a midband insertion loss of 1.32- and 1.80-dB for 28 and 39 GHz bands, respectively. The fifth-order interdigital BPF for 28 GHz band depicts a mid-band insertion loss of 2.6-dB, has 30-dB attenuation point to band-edge ratio of 1.16 and a VSWR better than 1.25. Similarly, the fabricated fifth order interdigital BPF for 39 GHz band depicts a mid-band insertion loss of 2.6-dB, has 30-dB attenuation point to band-edge ratio of 1.16 and a VSWR below 1.79.

Hairpin bandpass filters of third- and fifth-order for both 28 and 39 GHz bands are modeled, designed, optimized, fabricated and characterized. Similar to interdigital bandpass filters, they depict a slightly higher bandwidth but are not shifted in frequency as shown in

(a)   (b)
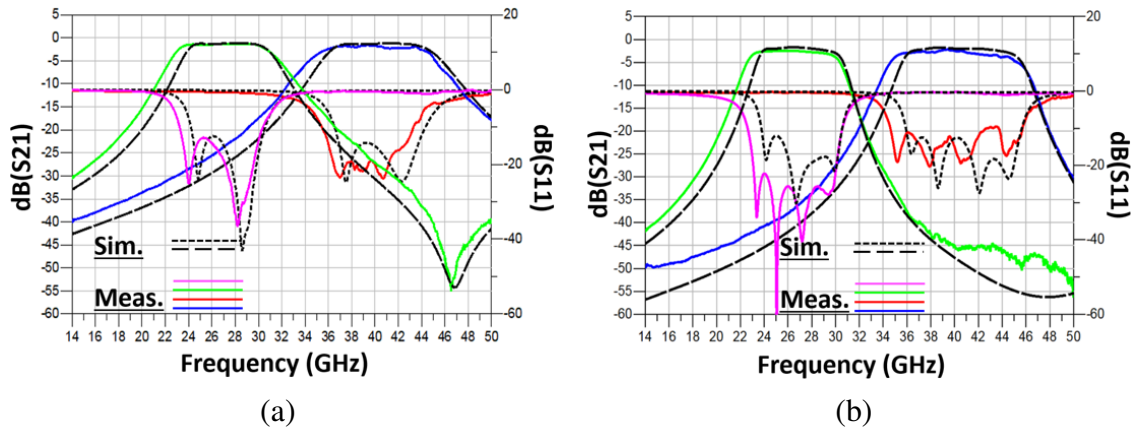
Figure 3.18: Comparison of simulated and measured results of fabricated interdigital BPFs for 28 and 39 GHz bands (a) third- and (b) fifth-order.
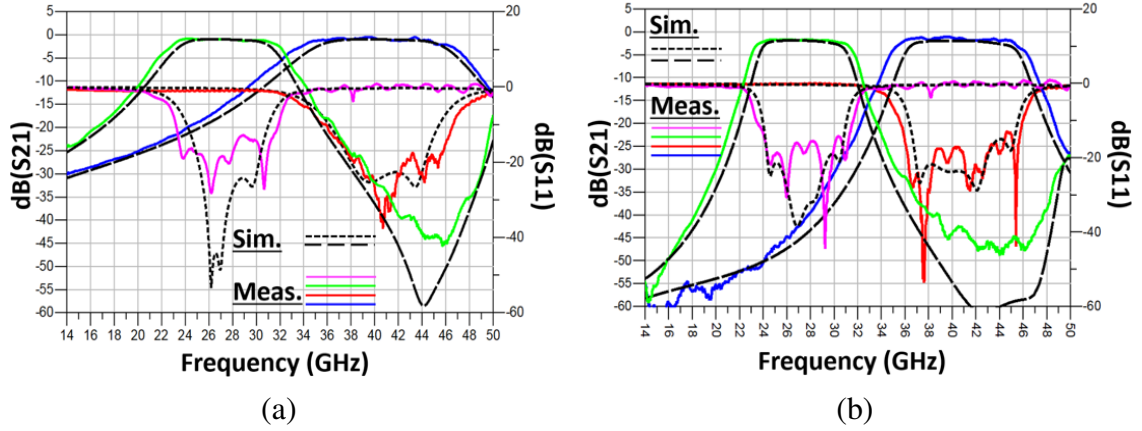
Figure 3.19: Comparison of simulated and measured results of fabricated hairpin BPFs for 28 and 39 GHz bands (a) third- and (b) fifth-order.

Figure 3.18a and 3.18b. The third-order hairpin BPFs have an insertion loss of 0.99- and 0.95-dB for 28 and 39 GHz bands, respectively. For the fifth-order hairpin BPF for 28 GHz band, the midband insertion loss is 1.8-dB, 30-dB attenuation point to band-edge ratio is 1.18 and VSWR is better than 1.5. Similarly, the fifth-order hairpin BPF for 39 GHz band has a measured insertion loss of 1.43-dB, 30-dB attenuation point to band-edge ratio of 1.19 and has VSWR below 1.6.

Despite the slightly increased bandwidth in both hairpin and interdigital filters, the model-to-hardware correlation is excellent. The midband insertion loss and rejection in the other band of 28 and 39 GHz BPFs is summarized in Table 3.5 and Table 3.6, respectively. As expected, rejection in the other band increases as the filter order increases. For example,

Table 3.5: Insertion loss and out-of-band rejection of 28 GHz BPFs.

Filter	Order	Midband Insertion Loss (dB)	Rejection in 39 GHz band (dB)		
		27.0 GHz	37.0 GHz	40.25 GHz	43.5 GHz
Interdigital BPF @ 28 GHz	3	1.32	20.37	27.69	34.76
	5	2.60	39.94	45.45	45.50
Hairpin BPF @ 28 GHz	3	0.99	21.85	32.42	40.25
	5	1.80	36.78	43.65	47.06

Table 3.6: Insertion loss and out-of-band rejection of 39 GHz BPFs.

Filter	Order	Midband Insertion Loss (dB)	Rejection in 28 GHz band (dB)		
		40.25 GHz	24.5 GHz	27.0 GHz	29.5 GHz
Interdigital BPF @ 39 GHz	3	1.80	27.80	23.76	18.68
	5	2.58	40.19	35.85	29.21
Hairpin BPF @ 39 GHz	3	0.95	18.53	15.76	10.76
	5	1.43	48.47	42.39	33.00

on comparing fifth-order interdigital and hairpin filters for 28 GHz band, rejection in 39 GHz band is within a difference of 2-dB. This also indicates that the Q-factor of interdigital and hairpin resonators is fairly close in this frequency range [138].

3.1.6   Dimensional Analysis and Comparison with Recent Prior Art

The dimensional analysis of all fabricated filters is performed to find the discrepancy between desired and obtained resonator widths and spacings along with physical measurements of filter size to translate it into electrical size. It was observed that resonator widths for BPFs are affected by a nominal variation of 3-4 μm whereas variation in high impedance lines in fabricated LPFs is only 1-1.5 μm. The overall variation in dimensions of fabricated features is less than 5%.

The physical dimensions along with corresponding electrical dimensions in terms of free-space wavelength (λ_0) corresponding to band frequency of each fabricated filter is given in Table 3.7. The physical dimensions of 28 GHz band filters are normalized by corresponding free-space wavelength of 28 GHz: 10.71-mm, and the physical dimensions of 39 GHz filters are normalized by corresponding free-space wavelength of 39 GHz: 7.69-mm. As evident from the electrical dimensions of the filters given in Table 3.7, all filters are smaller than $0.5\lambda_0 \times 0.5\lambda_0$ with z-height of 188.5-μm.

A performance comparison between the fabricated filters and other similar structures reported in literature is presented in Table 3.8. The fabricated filters in this work are the

Table 3.7: Dimensional analysis of fabricated 5G filters.

Filter	Order	Physical Dimensions (mm^3)	Electrical Dimensions (λ_0^3)
LPF @ 29.5 GHz	5	3.44×1.35×0.1885	0.32×0.13×0.018
	7	4.23×1.42×0.1885	0.39×0.13×0.018
	9	4.59×1.70×0.1885	0.43×0.16× 0.018
LPF @ 43.5 GHz	5	2.91×1.35×0.1885	0.38×0.18×0.025
	7	3.29×1.35×0.1885	0.43×0.18×0.025
	9	3.75×1.35×0.1885	0.49×0.18×0.025
Interdigital BPF @ 28 GHz	3	2.60×2.25×0.1885	0.24×0.21×0.018
	5	3.06×2.25×0.1885	0.29×0.21× 0.018
Interdigital BPF @ 39 GHz	3	2.63×1.79×0.1885	0.34×0.23×0.025
	5	3.12×1.77×0.1885	0.41×0.23×0.025
Hairpin BPF @ 28 GHz	3	3.26×2.15×0.1885	0.30×0.20×0.018
	5	4.65×2.12×0.1885	0.43×0.19×0.018
Hairpin BPF @ 39 GHz	3	3.18×1.67×0.1885	0.41×0.22×0.025
	5	3.85×1.66×0.1885	0.50×0.22×0.025

smallest in terms of footprint and z-height in addition to depicting superior performance in terms of passband insertion loss, return loss, out-of-band rejection and compact size. Moreover, these filters can be easily integrated in the top layer of RF FEMs in the same layer as antennas with ultra-short interconnects to reduce overall end-to-end loss, making them ideal for 5G and mm-wave applications.

To further reduce the insertion loss of these filters, another fabrication is performed using a low-loss polymer from Taiyo Ink Mfg., Co., Ltd. (Zaristo) for some of the filter structures. Its electrical properties are: ε_r = 3.3, tan δ = 0.0025, characterized at 10 GHz. The thickness of this dry-film is 71-μm. Since its electrical properties and thickness of Taiyo Zaristo are similar to that of ABF GL102, the designs are not re-optimized for this stackup. Since tan δ of Taiyo Zaristo is less than ABF GL102, a reduction in insertion loss

Table 3.8: Comparison of filters using various substrate technologies for mm-wave applications

Ref.	Substrate / Structure	Order	IL (dB)	f_c (GHz)	BW (GHz)	Size {(L×W)×H} (mm³)
[91]	LTCC / SIW	2	0.53	28.12	4.22	7.55×4.44×0.47
[91]	LTCC / SIW	2	0.82	28.21	3.72	7.55×4.44×0.47
[92]	LTCC / SIW	4	2.66	27.45	0.98	(43.5)[1]×0.84
[89]	LTCC / SIW Cavity	4	2.95	30	1.4	11×8×0.47
[139]	LTCC / Stacked SIW	4	2.8	27.95	1.03	6.12×3.24×0.4
[93]	Rogers Laminate / SIW	4	1.25	35	1.3	11×11×0.508
[140]	Rogers Laminate / SIW	4	3.6	29.375	3.75	9×9×0.3
[94]	Alumina / Microstrip	3	3	38.5	3	(7.1)[1]×0.254
[141]	Rogers Laminate / Air-filled SIW	4	3.9	21	0.23	68.1×10.954×1.524
[95]	Rogers Laminate / SIW	2	2.2	29	4.35	2.9×3.38×0.254
[95]	Rogers Laminate / SIW	3	2.51	29.39	3.64	3.78×3.38×0.254
[95]	Rogers Laminate / SIW	3	2.3	29.05	4.18	3.78×3.38×0.254
[142]	Alumina / CHSR[2]	2	4	29.85	0.293	23.9×12.7×0.2
This Work	Laminated Glass / Microstrip	3	1.32	27	5	2.60×2.25×0.1885
This Work	Laminated Glass / Microstrip	3	0.95	40.25	6.5	3.18×1.67×0.1885
This Work	Laminated Glass / Microstrip	5	2.6	27	5	3.06×2.25×0.1885
This Work	Laminated Glass / Microstrip	5	1.43	40.25	6.5	3.85×1.66×0.1885

[1]L and W are not explicitly mentioned in the reference.
[2]CHSR = Coplanar type H-slot resonator.

is expected.
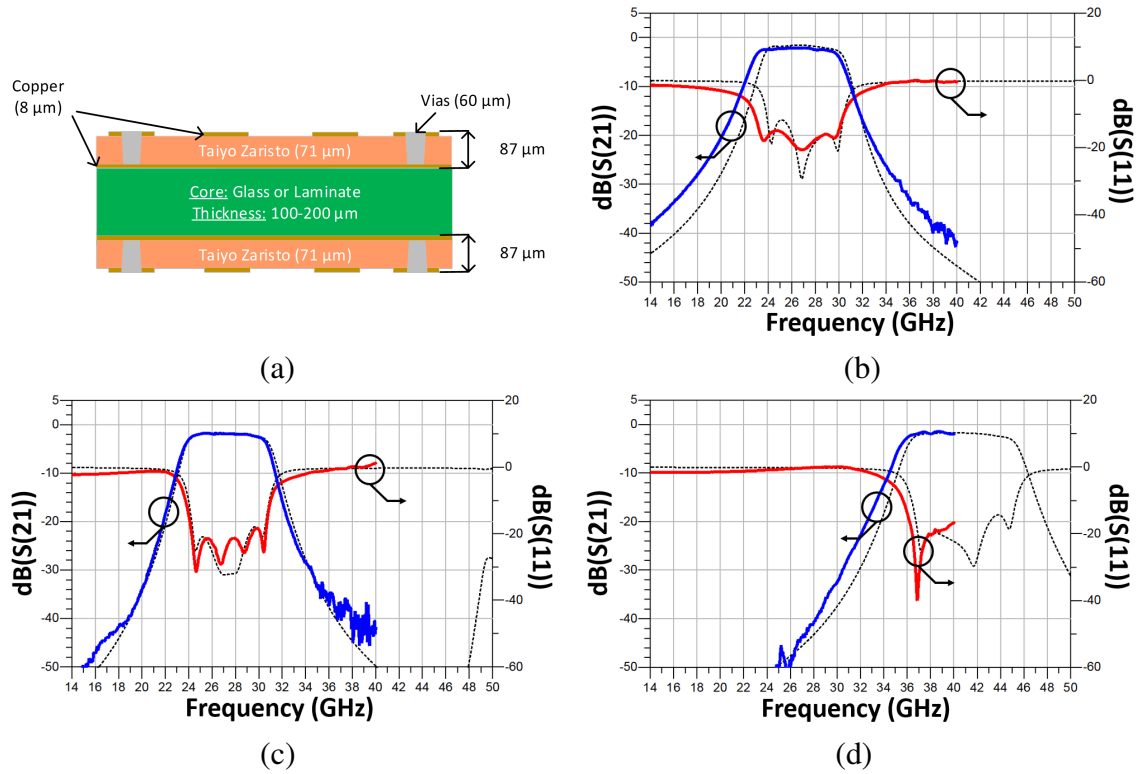
Figure 3.20: Fabricated fifth-order BPFs on stackup using Taiyo Zaristo for 5G mm-wave (a) stackup, (b) interdigital for 28 GHz band, (c) hairpin for 28 GHz band, and (d) hairpin for 39 GHz band.

The comparison of simulated and measured response of three of the fabricated BPFs is shown in Figure 3.20. The characterization equipment is limited to the frequency range of 14-40 GHz for these measurements. The 39 GHz band filters suffer from this limitation as their response cannot be measured completely. The mid-band insertion loss of fabricated filters is given in Table 3.9. The most significant improvement is in the insertion loss of fifth-order filters, which reduced to about 2-dB from 2.6-dB, reported earlier using ABF GL102. As evident from Figure 3.20, the return loss of these filters is more than 15-dB and excellent model-to-hardware correlation is achieved using Taiyo Zaristo as well.

Table 3.9: Midband insertion loss of 5G filters fabricated using Taiyo Zaristo dry-film.

Filter	Order	Midband Insertion Loss (dB)
		@ 27.0 GHz
Hairpin BPF @ 28 GHz	3	1.05
	5	1.87
Interdigital BPF @ 28 GHz	3	1.19
	5	2.09
		@ 40.25 GHz
Hairpin BPF @ 39 GHz	3	1.18
	5	2
Interdigital BPF @ 39 GHz	3	1.43

3.2 5G Power Dividers and Antenna Arrays

The focus of this research topic is to design and demonstrate package-integrated power dividers with footprint smaller than unit free-space wavelength corresponding to the operating frequency of 28 GHz band for 5G Antenna-in-Package (AiP), by utilizing precision low-loss redistribution layers (RDL) on glass substrates for highly integrated mixed-signal systems. Three configurations of power dividers with two-, three- and four-way equal power split are modeled, designed and fabricated on glass substrates with thin film build-up layers. This approach combines the benefits of ceramic and low-loss polymers for electrical performance, and silicon-like dimensional stability of glass for precision panel-scale patterning. Multilayered RDL with sub-20 μm features are utilized to design innovative power divider topologies with benefits in terms of low added insertion loss (<0.8-dB) and minimal phase-shift between the output ports, due to high precision of distributed transmission lines and through panel vias (TPVs).
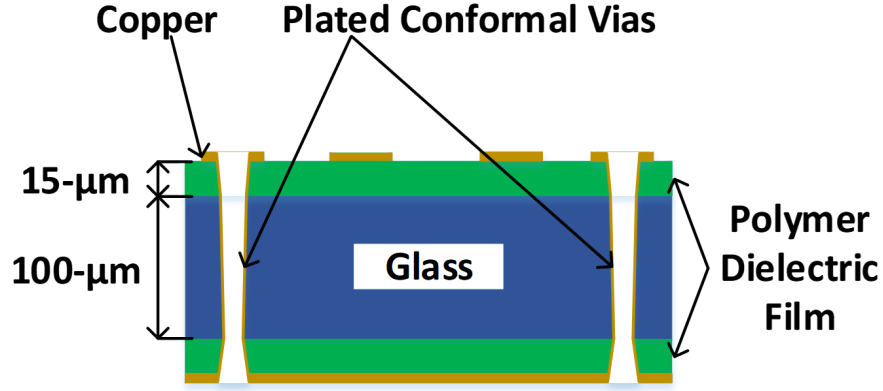
Figure 3.21: Material stackup for power dividers and antenna arrays.

3.2.1 Material Stackup

In this section, the material stackup and design procedure of power dividers is discussed. The microstrip structure is selected for power dividers with the intent of integrating them into a module on top metal layer, along with antennas. The material stackup is shown in Figure 3.21. The glass substrate has ε_r of 5.4 and tan δ of 0.005 and Zaristo film depicts ε_r of 3.3 and tan δ of 0.0025, characterized at 10 GHz. The size of glass panel is 150×150 mm^2. The desired copper thickness is set to 8-μm which is more than five times the skin-depth at the highest operating frequency of 29.5 GHz. The skin-depth at 29.5 GHz is 0.38-μm. The design rules are also set at the modeling stage and are listed below:

- Critical dimension (min. width) and linespace: 35-μm

- Through-glass via (TGV) and via-in-via Diameter: 100-μm

- Via pitch: 450-μm

3.2.2 Design of Power Dividers and Antenna Arrays

A power divider splits or divides an input signal into two or more output signals, regardless of the frequency of the incoming signal. It is a three-port network in its basic form, that is, two-way power divider and usually it is designed with an equal-split ratio. Power dividers

with unequal split can also be designed but in this research, we will focus on equal-split structures. A power divider is a reciprocal structure: if the roles of input and output ports is reversed, it acts as a power combiner which combines two or more input signals into a single output. They are commonly used in RF transceivers with multiple amplifiers or multiple antenna arrays to combine the signals coming from the amplifier block into one line then divide it again for multiple antennas in an antenna array.

The electrical performance of power dividers is based on several figures of merit. They are listed as follows:

- Splitting ratio

- Insertion loss

- Return loss

- Isolation

- Relative phase shift

- Amplitude balance and ripple

- Phase balance and ripple

Splitting ratio is the ratio of output to input power. A 2:1 power divider is considered as an equal-split power divider: it splits the power into half for each output port. Similarly, a 3:1 two-way power divider allows 33.33% of the power to pass through one port and remaining 66.67% to the other port. The insertion loss of the power divider refers to additional loss other than split-ratio. It is also known as added insertion loss. Ideally, this loss would be zero for a loss-less power divider but in practice, this can go as high as 1.5-2 dB. This is due to the combination of impedance mismatch, conductor and radiation losses, and dielectric absorption. The return loss metric refers to matching of the power divider to the source and load impedance. For nominal operation, it is imperative to maintain matching

to characteristic impedance (50-Ω) over the desired frequency band. Isolation in a power divider refers to mutual isolation of output ports. This translates to leakage of power from one output port to another. Isolating the output ports becomes challenging when bandwidth of the power divider is fairly large. Usually, better than 20-dB isolation can be achieved. Relative phase shift refers to the difference in phase between the output ports. Power dividers can be designed to have output power in-phase (0°), quadrature phase (90°) and out-of-phase/differential (180°). In-phase power dividers are most commonly found in RF transceivers and are the focus of this research. Amplitude balance is the measure of difference in amplitude between the output ports and ideally, it should be zero. Practically, the achievable amplitude balance is typically less than 0.25-dB. Amplitude ripple is the measure of flatness of divided power over a specified bandwidth. Similarly, phase balance and ripple are the measure of differential phase shift and phase flatness between the output legs of the power divider, respectively. Careful design, fabrication and packaging techniques can help to maintain accurate phase balance and ripple.

The following equal-split power dividers are designed for this demonstration and are also configured as antenna arrays:

- Two-way

- Three-way

- Four-way

The power dividers are designed to cover the frequency range of 24.25 to 29.5 GHz (19.53% FBW), which is the combined range of 5G bands n257, n258 and n261.

Depending upon the position in the system, the selection of power divider structure can be decided. For example, as shown in Figure 3.22, two locations can have power dividers, one after amplifier block and one for the ultra-wideband (UWB) antenna array. The power divider near the amplifier block requires isolation whereas the antenna array power divider can be used without isolation requirements if the antenna array is only transmitting power.
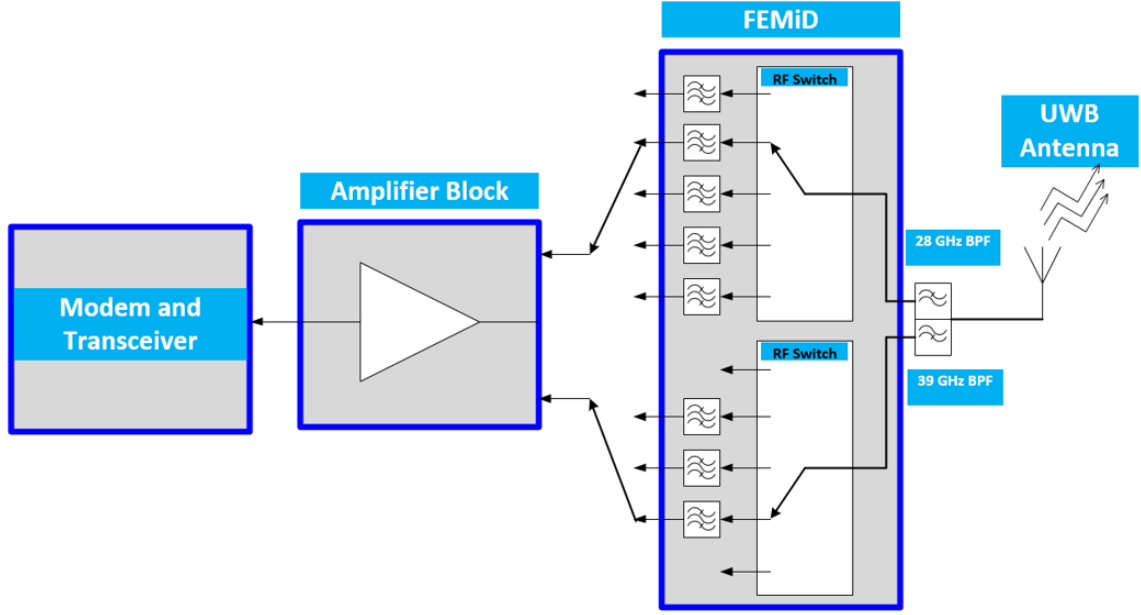
Figure 3.22: An example RF FEM with integrated duplexer (FEMiD).

T-Junction is the basis of transmission line modeling of the equal-split, microstrip power dividers, as shown in Figure 3.23. Alternatively, a reciprocal and matched (at all ports) power divider, commonly known as Wilkinson power divider is frequently used as it provides isolation between output ports. For small-footprint applications, Wilkinson power divider can be disadvantageous as it requires a lumped resistor between the output legs of the power divider. Moreover, as power division ratio is increased to more than two-way split, Wilkinson power divider implementation becomes complex and it can require a multi-layer stackup [113]. Looking into the junction in Figure 3.23, total admittance (Y_{in}) is seen as the sum of admittance of the output legs in combination with stored energy at the junction:

$$Y_{in} = jB + \frac{1}{Z_2} + \frac{1}{Z_3} + ...$$ (3.7)

where jB represents the sored energy as the lumped susceptance (B) and Z_n ($n = 2, 3, 4...$) are impedances of the output legs. Generally, there can be fringing fields in a T-junction and higher-order modes are associated with discontinuity at the junction of

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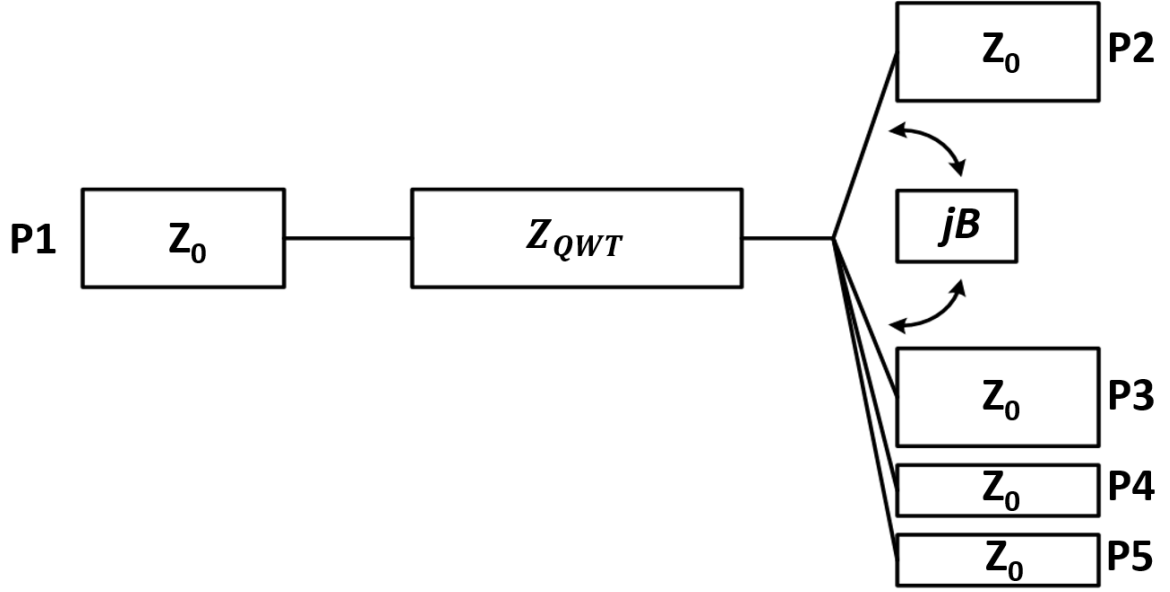
Figure 3.23: Circuit schematic for designing power dividers.

three or more transmission lines, leading to the stored energy jB. This susceptance in Equation (3.7) can be neutralized either by discontinuity compensation or by a reactive tuning element and it is non-zero in practice. For the power dividers in this demonstration, matching between input and output ports is performed using a single-section quarter wave transformer. The transformer can also aid in neutralizing jB but as split-ratio increases, jB starts dominating and can limit bandwidth of the structure. This effect can compound with bandwidth limitations of impedance transformer. Yagi-Uda antenna elements designed for 28 GHz n257 and n258 5G NR bands with 4-dBi realized gain are then used to configure the designed power dividers as antenna arrays [143].

Before starting the modeling and design of power dividers, it is important to calculate effective ε_r of the substrate stackup shown in Figure 3.21. The glass substrate has ε_r of 5.4 whereas Taiyo Zaristo dry-film laminated on both sides of glass substrate has ε_r of 3.3. The dielectric constants of each layer are donated by ε_n where n is the number of layers ($n = 1, 2, 3, ...$). It is expressed using the following set of equations in which $h_n, h_{n-1}, ..., h_1$ represent the height of individual layer starting from the top and ε_n, $\varepsilon_{n-1}, ...\varepsilon_1$ correspond

to the complex relative permittivity of the respective dielectric layer [144, 145]:

$$\varepsilon_{rc} = \frac{\mid d_1 \mid + \mid d_2 \mid + \mid d_3 \mid}{\mid \frac{d_1}{\varepsilon_1} \mid + \mid \frac{d_2}{\varepsilon_2} \mid + \mid \frac{d_3}{\varepsilon_3} \mid} \tag{3.8}$$

for $h_n + h_{n-1} + ... + h_1 \simeq \lambda/10$.

$$d_1 = \frac{K(k_1)}{K'(k_1)} \tag{3.9}$$

$$d_2 = \frac{K(k_2)}{K'(k_2)} - \frac{K(k_1)}{K'(k_1)} \tag{3.10}$$

$$d_3 = \frac{K(k_3)}{K'(k_3)} - \frac{K(k_2)}{K'(k_2)} - \frac{K(k_1)}{K'(k_1)} \tag{3.11}$$

$$d_n = \frac{K(k_n)}{K'(k_n)} - \frac{K(k_n - 1)}{K'(k_n - 1)} - ... - \frac{K(k_1)}{K'(k_1)} \tag{3.12}$$

Generally, k_n is defined as [146]:

$$k_n = \frac{1}{cosh(\frac{w\pi}{h_n+h_{n-1}+...+h_1})} \text{ for n=1, 2, 3,...} \tag{3.13}$$

The value of $\frac{K()}{K'()}$ is given by:

$$\frac{K(k_n)}{K'(k_n)} = \frac{1}{\pi}ln(2\frac{1 + \sqrt{k_n}}{1 - \sqrt{k_n}}) \text{ for } 0.7 \leq k_n \leq 1 \tag{3.14}$$

The frequency-independent relative dielectric constant of the multilayer substrate is obtained using Equation (3.8)−(3.14). After obtaining this parameter, the next objective is to find frequency-dependent behavior of the material stackup. The concept transforms to a single substrate with permittivity ε_{rc} and thickness of $h = h_n + h_{n-1} + ... + h_1$ and it is

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discussed in detail in [147, 148]. It is assumed in this model that total substrate thickness is approximately equal to $\lambda_0/10$ to obtain quasi-TEM characteristics.

Although calculating frequency-dependent behavior of the multilayer stackup is not absolutely critical below 100 GHz, the frequency-independent ε_{rc} is important as it helps in calculating width of the transmission line corresponding to characteristic impedance of 50-Ω. The frequency-dependent behavior of the multilayer stackup is useful in accurately finding electrical length associated with physical length of transmission line. Moreover, ε_{rc} can also be estimated intuitively by looking at the contribution of each dielectric to the stackup based on the thickness of individual layer. In this specific case, ε_1 and ε_3 both equal to ε_r of Taiyo Zaristo which makes 30-μm of the total stackup height. The remaining 100-μm is the ε_r of glass substrate. Using this data, ε_r of the entire stackup can be estimated to be slightly less than the ε_r of glass substrate. Utilizing this technique, width of the microstrip transmission line corresponding to the characteristic impedance of 50-Ω is calculated.

The schematic and microstrip realization of a two-way power divider is shown in Figure 3.24. Looking into transmission line junction of the two-way network, two 50-Ω impedances are seen in parallel, making an effective impedance of 25-Ω. The input transmission line has an impedance of 50-Ω which is matched to 25-Ω impedance using a quarter-wave transformer. This transformer also helps in countering the lumped suscep-tance jB at the junction of power divider. The distance between output ports is adjusted in reference to dimensions of Yagi-Uda antennas and required spacing between them for antenna arrays. The spacing between array elements is usually half of the free-space wave-length. Ansoft HFSS is utilized to simulate power dividers and corresponding antenna arrays in the frequency range of 20-32 GHz. The layout of this divider along with its sim-ulated response is shown in Figure 3.25. As evident from this figure, the power divider has a flat insertion loss in the frequency range of 24.25-29.5 GHz. The ideal insertion loss of this power divider is 3.01-dB, marked by horizontal dashed line in Figure 3.25.

$$Z_{QWT} = \sqrt{Z_0^2/2}$$
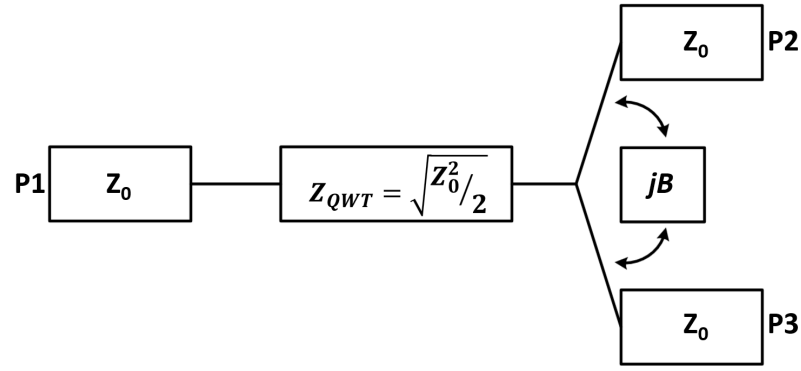
(a)
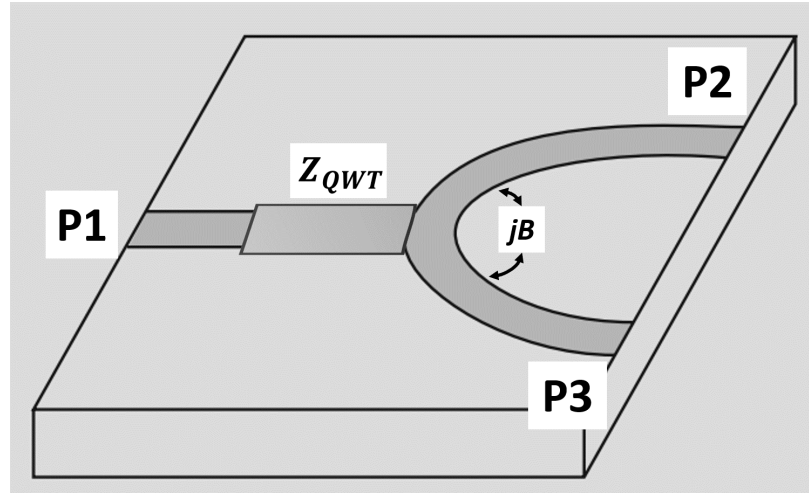
(b)

Figure 3.24: A two-way T-junction power divider with a matching quarter-wave transformer (a) schematic, and (b) an example microstrip realization.

The next step is to configure the two-way power as a 2×1 Yagi-Uda antenna array. The layout of 2×1 YagiUda antenna array is shown as an example in Figure 3.26 and its key parameters are given in Table 3.10. As evident from the figure, TGVs are utilized to connect top and bottom ground planes for measurements using GSG probes.

Similarly, three-way and four-way power dividers, and corresponding 3×1 and 4×1 Yagi-Uda antenna arrays are designed for 24.25-29.5 GHz frequency range. As stated earlier, junction susceptance reduces bandwidth of operation if more transmission lines are connected to it. This effect was observed in four-way power divider design in which direct split led to slightly reduced bandwidth (18%) as compared to target (19.53%). Since

(a)   (b)
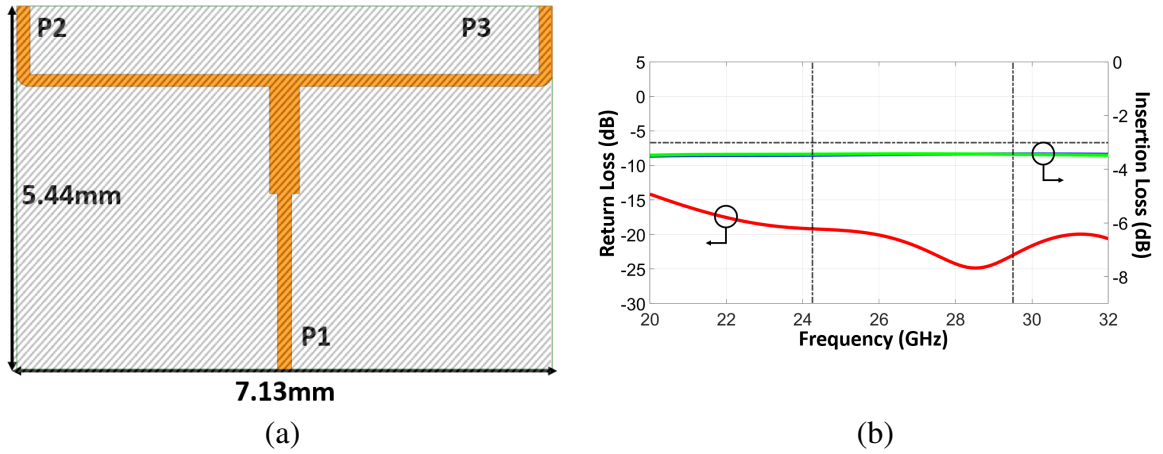
Figure 3.25: A designed two-way power divider (a) layout in HFSS, (b) simulated results
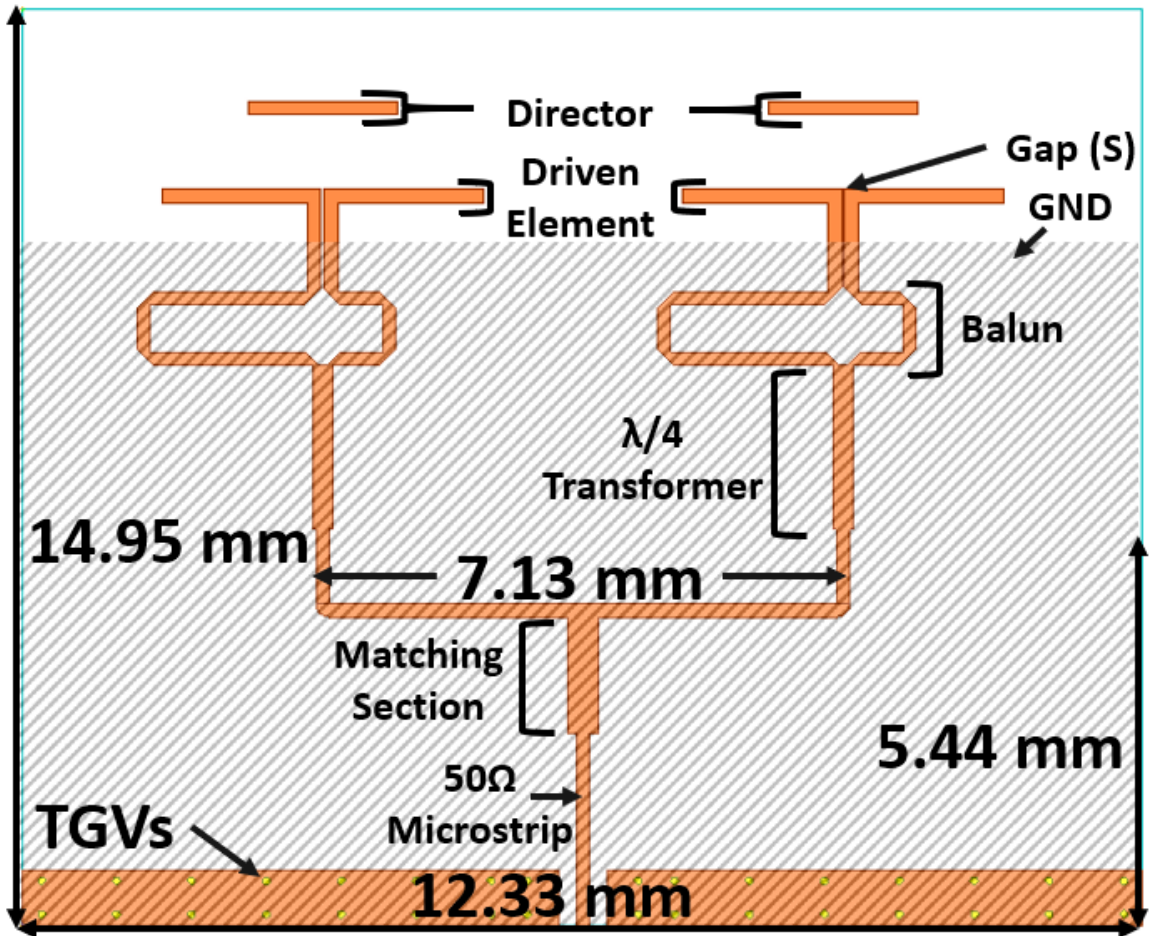
Figure 3.26: Layout of 2×1 Yagi-Uda antenna array.

Table 3.10: Key Parameters of Yagi-Uda antenna element and two-way power divider.

Structure	Dimension	Value (mm)
Director	L	2
	W	0.18
Driven Element	L	4.3
	W	0.18
Balun	L	3.46
	S	0.04
$\lambda/4$ Transformer	L	2.2
	W	0.25
Matching Section	L	1.57
	W	0.4
50 Ω Microstrip	W	0.18

bandwidth is a critical performance parameter, four-way power divider was implemented using three two-way power dividers as an alternative. Two- and three-way power dividers have reduced effects from jB and are thus more wideband than their four-way counterpart. The finalized design of all power dividers fulfill the bandwidth requirements and cover 24.25 to 29.50 GHz frequency range.,

3.2.3 Fabrication Process

The fabrication process for power dividers also utilizes SAP process to pattern the copper structures. Figure 3.27 illustrates the SAP process through schematic cross-sections of each step. This process is fairly similar to the fabrication process of 5G filters discussed in Section 3.1.4.

Proper handling procedures are advised to administer glass fabrication process to address its fragility and brittleness. Polymer lamination on glass addresses the challenge of
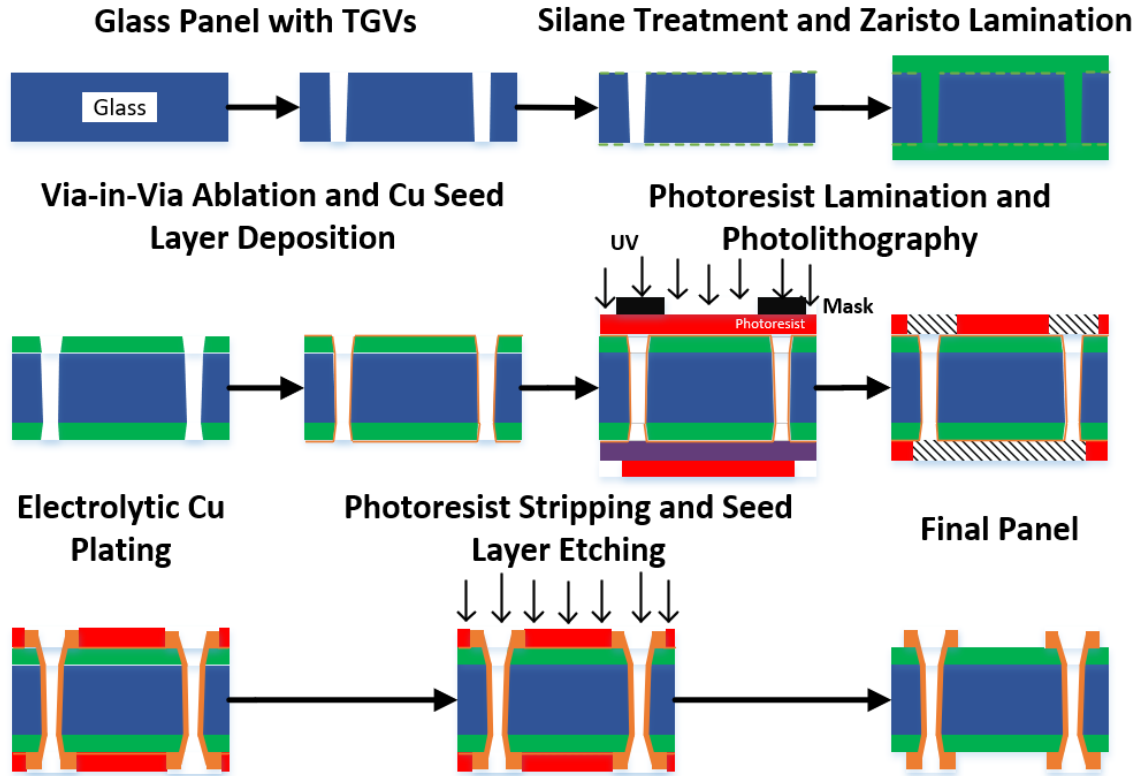
Figure 3.27: Illustration of SAP process for power divider fabrication with step-by-step cross sections.

glass handling and acts a buffer layer that reduces the effect of high CTE copper on glass. It also enables metallization as well as prevents copper migration to glass surface under high electrical voltage during plating. TGVs of 100-μm diameter are drilled by AGC. The glass panels are treated with silane to promote adhesion to polymers and mitigate delamination during the entire fabrication process. Polymer lamination is performed on both sides of glass panel using a roll laminator and 15-μm Taiyo Zaristo. This step is followed by polymer curing. The fabrication process continues to via-in-via ablation. The power, power density and number of repetitions are optimized for the UV laser to drill vias in the polymer. This step is performed on both sides of the panel. Next, a 0.2-μm copper seed layer is deposited uniformly on the polymer using electroless plating method. The electroless plating method has a surface roughening step utilizing a permanganate etch which creates mechanical anchor sites on the polymer to enable latching of copper particles. It also helps

in removal of residual polymer left after via-in-via ablation.

Afterwards, both sides of the panel are laminated with a 15-μm dry-film negative photoresist. The panel is photolithographically patterned with optimized dose time for the critical feature in the design. Followed by photoresist development, the panel is subjected to O_2 plasma which removes photoresist residue and improves surface conditions for copper plating. The metallization of traces and vias is performed using electrolytic plating. SAP yields better dimensions and sidewall control of deposited copper unlike subtractive etching techniques which have limited control. The target copper thickness after fabrication process is 8-μm so the authors strive to achieve plated copper thickness of 8.2-μm to account for removal of copper seed layer. After electrolytic plating, photoresist is stripped off using a stripper solvent and seed layer etching is performed. The measured copper thickness after fabrication process is 8.5$\pm$0.5μm. The fabricated power dividers and antenna arrays are shown in Figure 3.28.

3.2.4 Characterization Results

In this section, characterization results of fabricated power dividers and antenna arrays are discussed in detail. The return loss measurements are performed using an Anritsu VNA in the frequency range of 20-32 GHz using ACP50 GSG probes and Short-Open-Load-Through (SOLT) calibration. For radiation pattern measurements, 2.92-mm edge-mount connectors are soldered onto coupons as shown in Figure 3.29. The radiation pattern measurement setup consists of a two-port VNA, two known antennas and antenna-under-test (AUT). After characterizing path loss using two known antennas, one of them is replaced with AUT, and its gain and radiation pattern are measured. The measurements are performed on four, three and two coupons of 2$\times$1, 3$\times$1 and 4$\times$1 antenna arrays, respectively. The measurement results are compared with simulation results to perform a model-to-hardware correlation.

(a)

(b)

(c)
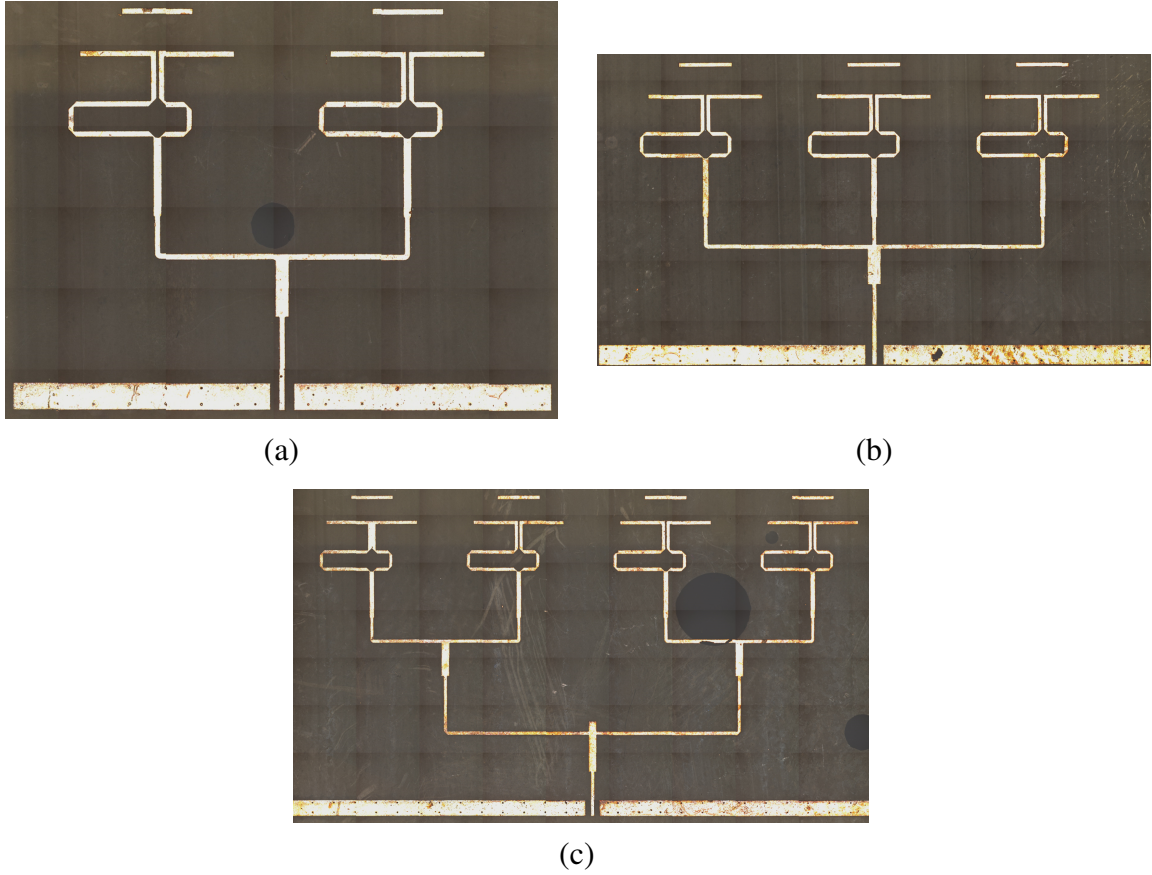
Figure 3.28: Fabricated coupons of Yagi-Uda antenna arrays: (a) 2×1, (b) 3×1 and (c) 4×1.
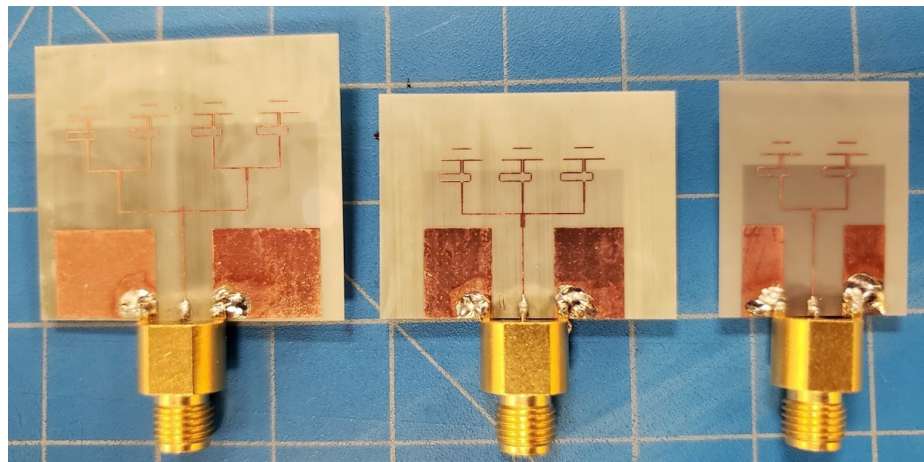
Figure 3.29: Fabricated power dividers and corresponding antenna arrays (right-to-left): 2×1, 3×1 and 4×1 with soldered 2.92-mm connectors for radiation pattern measurements.

Two-, Three- and Four-way Power Dividers

The s-parameters of two-, three, and four-way power dividers are shown in Figure 3.30a, 3.31a and 3.32a. The two-way power divider has a maximum insertion loss of 3.41-dB, three-way power divider has a maximum insertion loss of 5.37-dB and four-way power divider has a maximum insertion loss of 6.88-dB. Compared to the ideal insertion loss of these power dividers, the added insertion loss is: 0.4-dB for two-way, 0.6-dB for three-way and 0.86-dB for four-way power divider. The in-band VSWR is less than 1.92 for the demonstrated power dividers.

2×1, 3×1 and 4×1 Yagi-Uda Antenna Arrays

The comparison of measured return loss of multiple coupons of 2×1, 3×1 and 4×1 Yagi-Uda antenna arrays with the simulation is shown in Figure 3.30b, 3.31b and 3.32b, respectively. As evident from these figures, an excellent correlation is observed between simulated and measured results, as well as between coupons of the same antenna arrays.

The model-to-hardware correlation of two-, three- and four-way power dividers and corresponding antenna arrays is excellent as depicted in the figures. The discrepancies can be attributed to many factors in simulation, fabrication and characterization [149]. Maximum discrepancy is observed between the simulated and measured results for 4×1 antenna array. For this array, a post-characterization simulation is performed to correlate model with hardware and understand the variation between the initial simulation (Simulation-1) and measured return loss. The dimensions of critical features such as gap in balun and matching sections for all three two-way power dividers in a 4×1 antenna array are measured using an optical profilometer and that data is utilized to run a simulation in HFSS. As a result, the new simulation (Simulation-2) captures the effects of small dimensional variations for 4×1 antenna array and correlates better with hardware as compared to Simulation-1 as evident in Figure 3.32b. The realized gain and efficiency of these antenna array structures is given in Table 3.11. Their normalized radiation patterns are measured at 27 GHz and compared
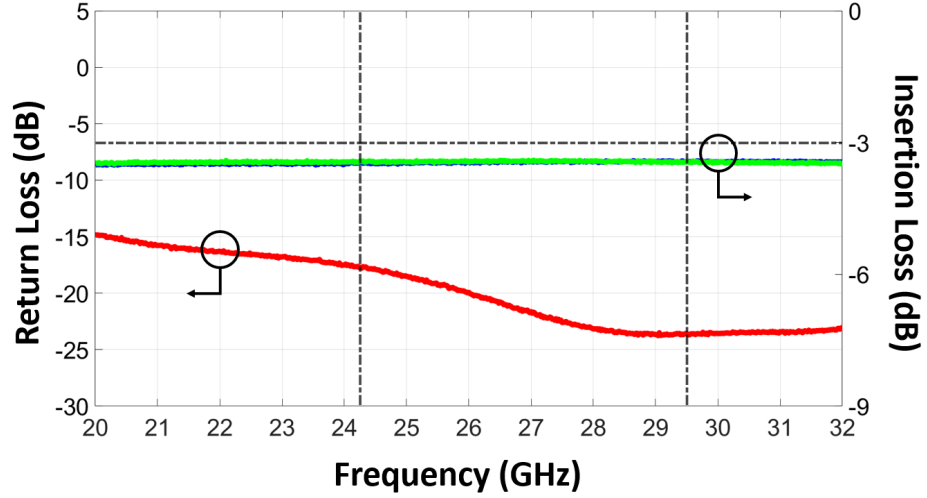
(a)
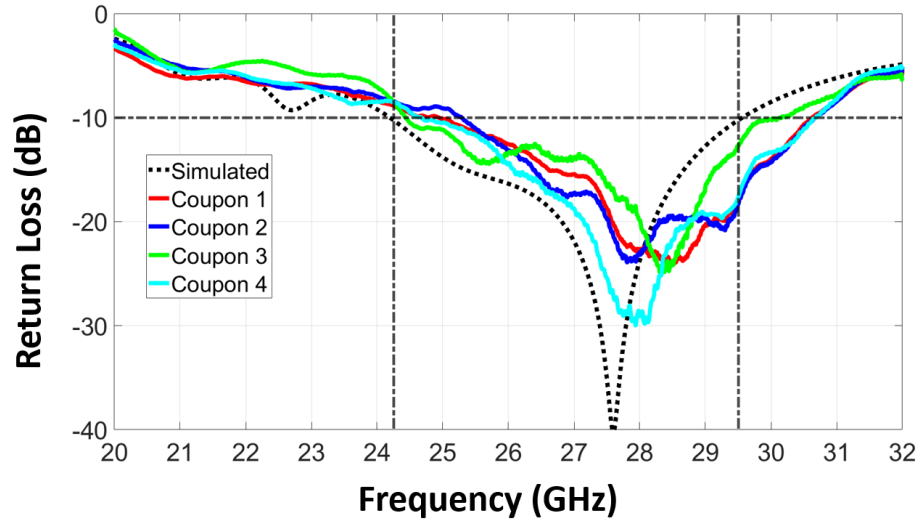
(b)

Figure 3.30: S-parameters (a) two-way power divider, and (b) 2×1 Yagi-Uda antenna array.

with simulation in Figure 3.33. It is to be noted that the realized gain of a Yagi-Uda antenna element is 4-dBi in the 24.25-29.50 GHz frequency range.

3.2.5   Dimensional Analysis and Comparison with Recent Prior Art

The dimensional analysis of all fabricated power dividers is performed to extract the electrical lengths from physical lengths. The physical dimensions are normalized with free-space wavelength (λ_0) corresponding to center frequency (f_c) of 28 GHz 5G bands. The f_c of
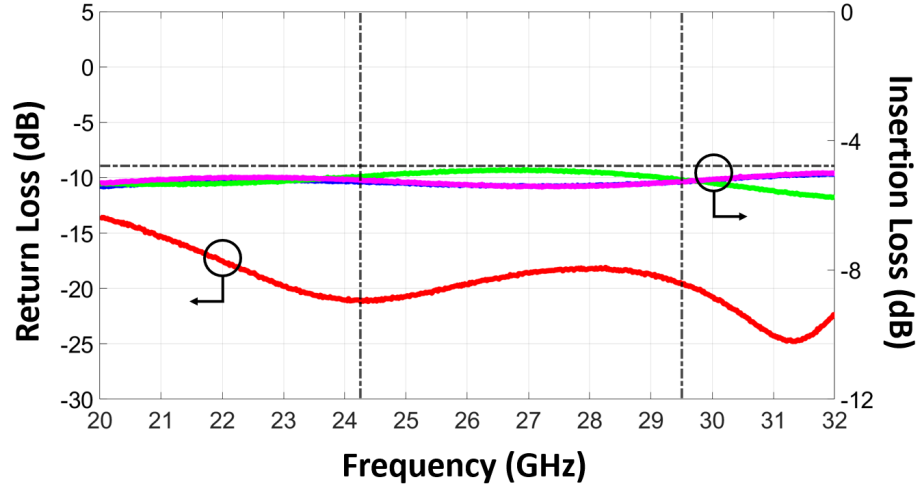
(a)
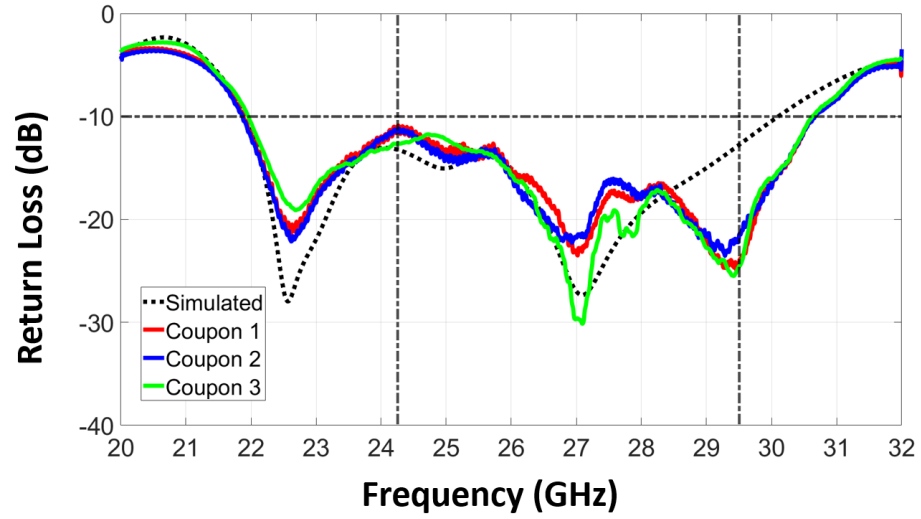
(b)

Figure 3.31: S-parameters (a) three-way power divider, and (b) 3×1 Yagi-Uda antenna array.

Table 3.11: Realized gain and efficiency of demonstrated antenna arrays.

Structure	Realized Gain (dBi)	Efficiency
2×1 Yagi-Uda Antenna Array	6.96	80%
3×1 Yagi-Uda Antenna Array	8.24	85%
4×1 Yagi-Uda Antenna Array	9.51	82%
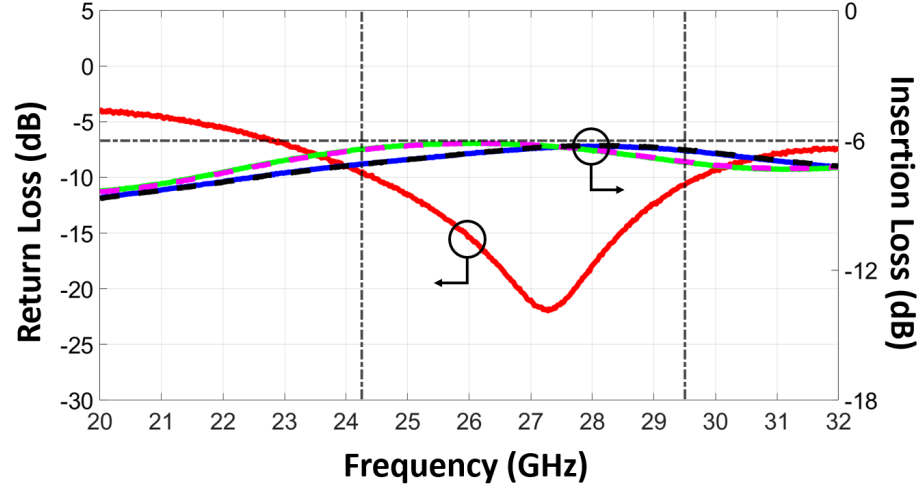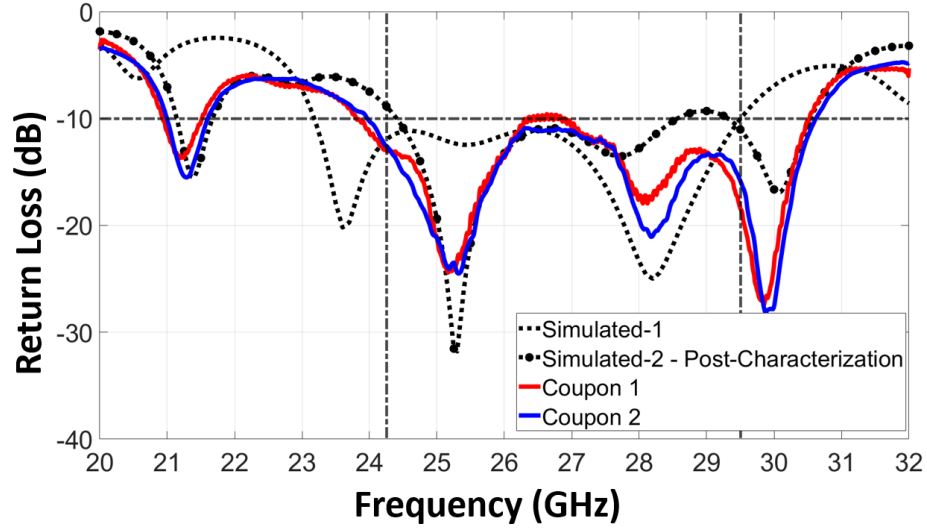
Figure 3.32: S-parameters (a) four-way power divider, and (b) 4×1 Yagi-Uda antenna array.

24.25-29.50 GHz range is 26.875 GHz and the corresponding λ_0 is 11.16-mm. The calculated electrical dimensions of power dividers and antenna arrays are given in Table 3.12.

A comparison of dimensions of the demonstrated power dividers with recent prior art is given in Table 3.13, in which electrical dimensions are calculated by normalizing physical dimensions by λ_0 corresponding to the band frequency. It can be observed that demonstrated two- and three-way power dividers are smaller than unit λ_0^2. Additionally, four-way power divider has a footprint of $1.64\lambda_0^2$. All fabricated structures have a z-height of 147-
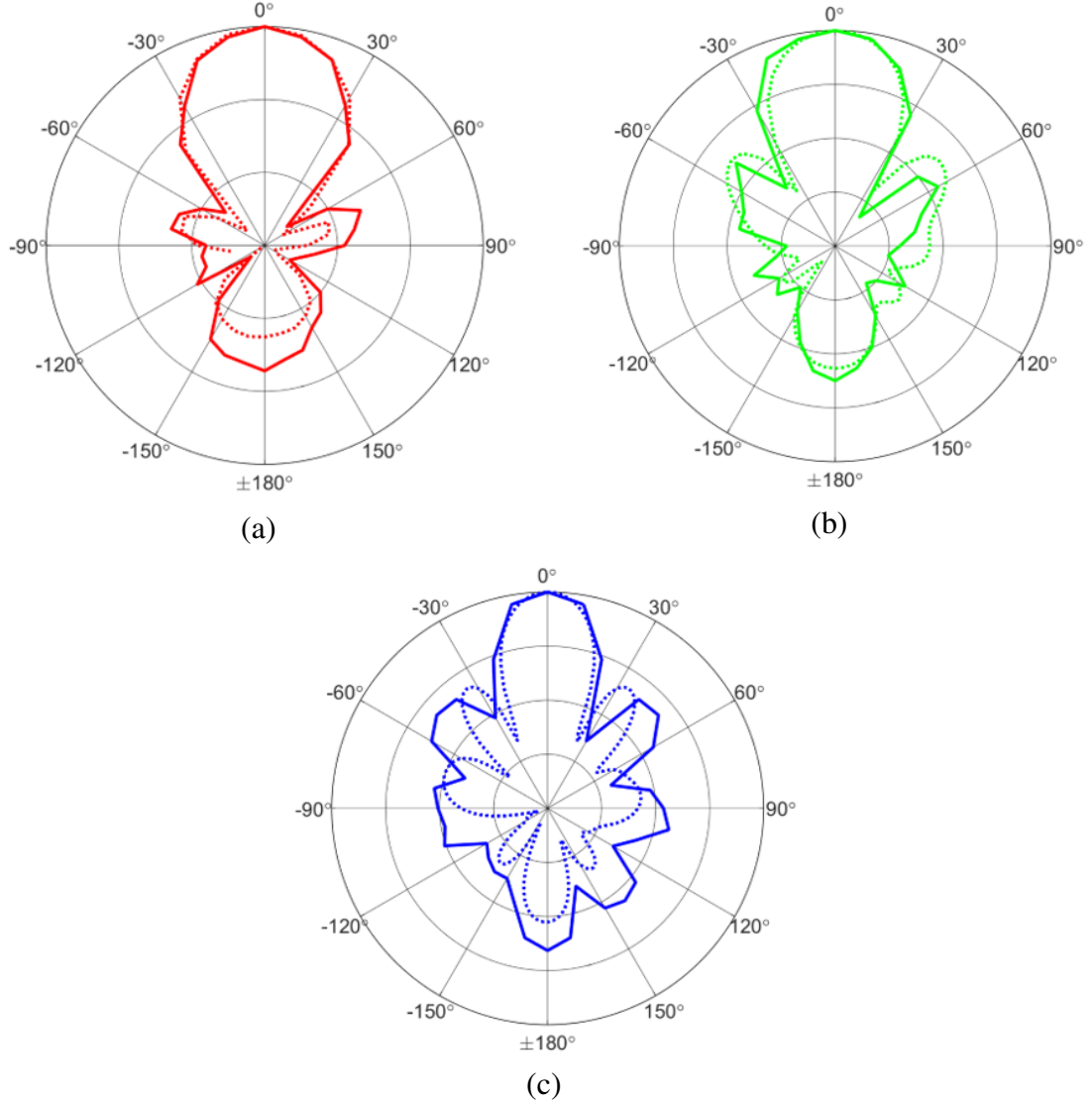
Figure 3.33: Normalized measured radiation pattern of Yagi-Uda antenna arrays at 27 GHz compared with simulation (dashed -simulated, solid - measured) (a) 2×1, (b) 3×1, and (c) 4×1.

μm. Since the power dividers are designed to be configured as antenna arrays, their footprint is governed by the physical spacing between adjacent antenna elements. However, their footprint can be further reduced depending upon the application.

Table 3.12: Physical and electrical dimensions of demonstrated power dividers and antenna arrays.

Structure	Physical Dimensions ($mm^2 \times 0.147mm$)	Electrical Dimensions ($\lambda_0^2 \times 0.013\lambda_0$)
Two-way Power Divider	7.13×5.44	0.64×0.49
2×1 Yagi-Uda Antenna Array	14.95×12.33	1.34×1.1
Three-way Power Divider	12.74×5.5	1.14×0.49
3×1 Yagi-Uda Antenna Array	20.6×12.5	1.85×1.12
Four-way Power Divider	21×9.7	1.88×0.87
4×1 Yagi-Uda Antenna Array	28.9×16.7	2.59×1.5

Table 3.13: Comparison with similar power dividers in literature.

Ref.	Structure	f_0 (GHz) & FBW	Phyiscal Dimensions (mm^3)	Electrical Dimensions (λ_0^3)
[120]	Two-way, Tunable	28 & 7.14%	10×10×0.127	0.93×0.93×0.012
[150]	Two-way	27.5 & 91%	2.2×10.1×0.254	0.2×0.93×0.023
[151]	Four-way	28.2 & 5%	22.7×5.6×0.13	2.13×0.53×0.012
[121]	Four-way, Dual-band	28, 39 & 1.14, 5%	27.5×20×0.254	3.07×2.23×0.028
This Work	Two-way	26.875 & 19.53%	7.13×5.4×0.147	0.64×0.49×0.013
This Work	Three-way	26.875 & 19.53%	12.7×5.5×0.147	1.14×0.49×0.013
This Work	Four-way	26.875 & 19.53%	21×9.7×0.147	1.88×0.87×0.013

3.3 Summary

In this chapter, high-performance and miniaturized filters and power dividers are presented for the first time on ultra-thin laminated glass substrates. Key performance and miniaturization attributes of filters and power dividers are given in Table 3.14 and Table 3.15, respectively.

Miniaturized high-performance filters with footprint less than half the free-space wavelength at the operating frequency of 28 and 39 GHz bands are demonstrated on ultra-thin laminated glass substrates for 5G and mm-wave applications. Two filter types, with three topologies in total are modeled, designed, fabricated and characterized. The filters are fabricated using SAP fabrication process to meet the dimensional accuracy requirements of these networks. The total height of the fabricated filters is 188.5-μm. The characterization results have shown excellent model-to-hardware correlation. The filters exhibit low insertion loss, low VSWR and high out-of-band rejection. Given the introduction of on-package fabrication approach of these filters, they are ideal for integration in glass-based RF FEMs either as standalone devices or as IPDs. Along with their superior performance, these are the smallest reported filters on ultra-thin laminated glass.

Table 3.14: Comparison of objectives and accomplishments for filters.

Topics	Metrics	Objectives	Accomplishment
Filters	Performance	• IL (in-band) < 2.6-dB • IL (out-of-band) > 30-dB • RL > 20-dB	• IL (in-band) ~2.6-dB using ABF GL102, ~2-dB using Taiyo Zaristo • IL (out-of-band) > 30-dB • RL > 20-dB in large fraction of bandwidth, Min. RL > 15-dB
	Miniaturization	• Footprint: < $2\lambda_0 \times 2\lambda_0$	• Footprint: < $0.5\lambda_0 \times 0.5\lambda_0$ with z-height of 188.5-μm

Table 3.15: Comparison of objectives and accomplishments for power dividers.

Topics	Metrics	Objectives	Accomplishments
Power Dividers	Performance	• IL: < 3.82-dB for two-way, < 5.57-dB for three-way, < 6.82-dB for four-way • RL > 20-dB	• IL: < 3.4-dB for two-way, < 5.37-dB for three-way, < 6.88-dB for four-way • RL > 20-dB for a large fraction of bandwidth
	Miniaturization	• Footprint < $\lambda_0 \times \lambda_0$	• Footprint: $0.64\lambda_0 \times 0.49\lambda_0$ for two-way, $1.14\lambda_0 \times 0.49\lambda_0$ for three-way, $1.88\lambda_0 \times 0.87\lambda_0$ for three-way with a z-height of 147-μm

Similarly, package-integrated ultra-thin power dividers with footprint smaller than unit free-space wavelength are presented for 28 GHz 5G NR n257 and n258 bands. Three equal-split power dividers are modeled, designed, fabricated and characterized on a 147-μm thick laminated glass stackup. SAP process is optimized to fabricate these power dividers. TGVs are utilized to connect top and bottom ground planes for characterization. Moreover, these power dividers are also configured as antenna arrays using Yagi-Uda antenna elements. The characterization of these networks reveal their low added insertion loss and minimal phase shift between the output ports with excellent model-to-hardware correlation. Given the integration capability of these power dividers along with their small footprint and z-height, they are ideal candidates for 5G and mm-wave FEMs.

CHAPTER 4

DESIGN AND DEMONSTRATION OF DIPLEXERS AND INTEGRATED PASSIVE COMPONENTS

RF FEMs typically include a combination of active devices such as power amplifiers (PA), low noise amplifier (LNA), switches, and passive components such as filters, diplexers and couplers. In this chapter, the focus will be on design and demonstration of diplexers for 5G mm-wave NR bands and how these diplexers, along with broadband couplers, can be used in an output power control circuitry commonly found in PA FEMs. System performance analysis of this passive component block of diplexer and coupler when co-packaged with other active and passive components is also presented. Using higher modulation schemes for 5G communication systems, a co-simulation methodology is introduced to evaluate system-level performance signature of passive components and how this methodology can aid in comparing various passive components is discussed.

The first part of this chapter focuses on design and demonstration of miniaturized, non-contiguous, planar diplexers for 5G NR mm-wave bands along with their characterization at frequencies upto 40 GHz. In the second half, integration of diplexers and broadband couplers and their characterization is discussed, and then the focus shifts towards evaluating system-level performance metric of this block in a complete RF transmitter chain. The scalability of this approach to discriminate between similar passive components is also explored in detail.

4.1 5G Diplexers

A diplexer is a three-port passive component which separates incoming signal on the basis of their frequency characteristics. It is the simplest form of a multiplexer and essentially can be referred to as a frequency-selective power divider. If the input and output ports are

reversed, a diplexer can combine two signals with different frequencies onto the common port. Diplexers are commonly found in RF FEMs, especially near the antennas. With the advent of carrier aggregation (CA) in 4G and LTE networks, diplexers and multiplexers have been extensively utilized to combine multiple bands to support higher data-rates to the end-user.

Diplexers can be broadly classified into two types based on the cross-over point of filters:

- Contiguous diplexers

- Non-contiguous diplexers

Contiguous diplexers have the cross-over point at 3-dB whereas non-contiguous diplexers have the cross-over point at any higher value of insertion loss. They can be either constructed with lowpass-highpass or bandpass-bandpass filters, as shown in Figure 4.1.

Singly-terminated filters are commonly utilized to design both contiguous and non-contiguous diplexers. Unlike classic doubly-terminated filters, these filters do not have resistor terminations on both ends, rather only one end is matched to the characteristic
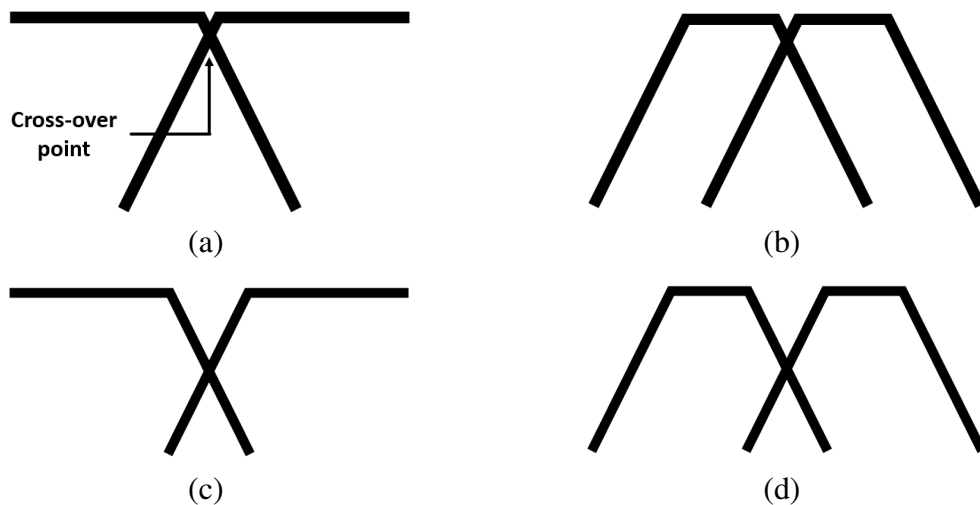
Figure 4.1: Types of diplexers: contiguous (a) lowpass-highpass, (b) bandpass-bandpass, and non-contiguous (c) lowpass-highpass, and (d) bandpass-bandpass

impedance. The other end has zero or ∞ impedance as it is assumed to be driven by a zero internal impedance voltage generator or an infinite internal impedance current generator, respectively. The g-value of this end is ∞ [134]. The advantage of using singly-terminated filters is their seamless combination with the common port to realize a diplexer. However, these filters cannot be characterized individually. Doubly-terminated filters can also be used to design diplexers under the condition that the frequency bands have a guard band between them. This is to ensure that the filters do not load each other once combined at a junction.

The electrical performance metrics of a diplexer are listed as follows:

- Insertion loss

- Return loss

- Stopband rejection

- Isolation

For a well-designed diplexer, the insertion loss will be very close to that of originally designed filters with the addition of insertion loss of the common port network. The stopband rejection of diplexer depends upon its filters so it is more related to the filter design itself. The isolation of a diplexer refers to common-mode rejection of the diplexer and it can be more than 50-dB for an excellent design. For this demonstration, non-contiguous planar diplexers are designed to combine 28 and 39 GHz 5G NR bands. Their frequency range along with FBWs are given below:

- n257: 26.5-29.5 GHz (FBW = 10.71%)

- n258: 24.25-27.5 GHz (FBW = 12.6%)

- n260: 37-40 GHz (FBW = 7.8%)

The diplexers are designed to combine band n257 or n258 with band n260 for this demonstration. All diplexers are realized using microstrip transmission lines.

4.1.1 Material Stackup

A four-metal layer material stackup is chosen for this demonstration as shown in Figure 4.2. The core material is a 150×150 mm^2, 100-μm thick glass substrate (EN-A1) panel from AGC and it has dielectric permittivity (ε_r) of 5.4 and loss tangent (tan δ) of 0.005 at 10 GHz. The polymer dielectric is a low-loss epoxy film from Taiyo Ink. Mfg. Co. (Zaristo$^{\text{TM}}$) with 15-μm and 71-μm thickness. It has ε_r of 3.3 and tan δ of 0.0025 at 10 GHz. The 15-μm thick Taiyo Zaristo is laminated onto bare glass panel, onto which metal layers M2 and M3 are patterned followed by lamination of 71-μm Zaristo on which M1 and M4 are patterned. M2 and M3 act as ground planes to microstrip integrated passive components on M1 and M4. The stackup is double-sided to avoid panel warpage during the fabrication process. The thickness of copper is set to 8-μm which is sufficiently higher than five times of skin depth at the operating frequency of 40 GHz. The total thickness of this stackup is 202-μm.

The design rules are also set at the modeling stage and are listed below:

- Critical linespace: 25/25-μm
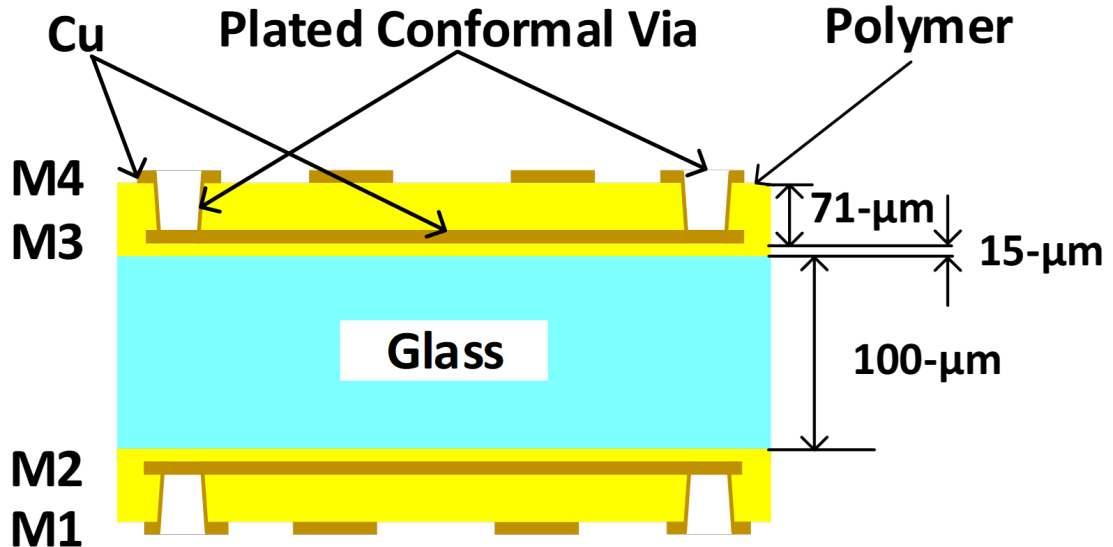
Figure 4.2: Material stackup for Diplexers.

- Blind via diameter: 71-μm

- Blind via pitch: 142-μm

4.1.2 Filter Design for Diplexers

The selection of bandpass filters for diplexers is based on the type of resonators. Hairpin and interdigital filters are selected as candidates for diplexer realization which are extensively discussed in Chapter 3. Moreover, parallel- or edge-coupled filters, which are formed using parallel-coupled $\lambda/2$ resonators are also considered for diplexers. Both hairpin and interdigital filters are designed using 0.043-dB Chebyshev equal-ripple response with fifth order g-values and edge-coupled filters are designed using fourth order g-values. Their order is selected based on acceptable passband insertion loss and stopband attenuation of more than 30-dB. Hairpin and interdigital filters are designed for bands n257, n258 and n260 whereas edge-coupled filters are designed for combined bands n257 and n258 (24.25-29.5 GHz), and band n260. The layout of a microstrip structure of a fourth-order edge-coupled filter is shown in Figure 4.3.

The design of an edge-coupled BPF starts with selection of g-values for lowpass filter prototype [134, 135]. In this case, fourth-order g-values are selected. This filter has $n + 1$
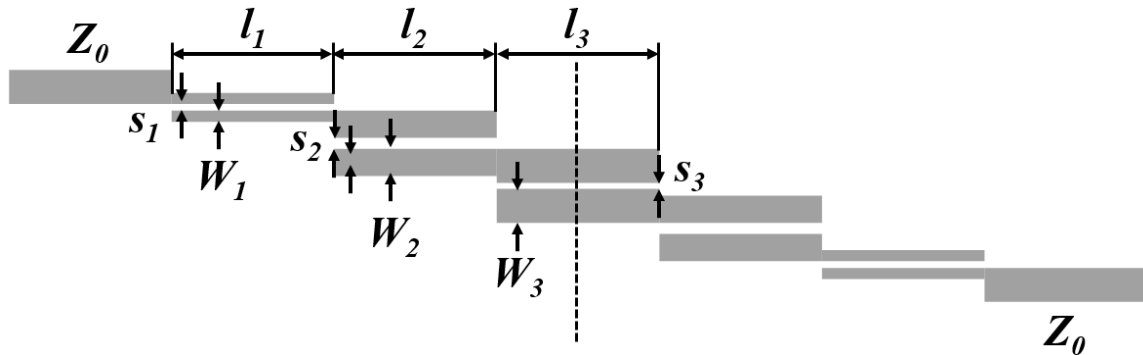
Figure 4.3: Structure of a fourth-order edge-coupled microstrip BPF.

or five coupled-line sections. The design process is summarized here:

$$\frac{J_{01}}{Y_0} = \sqrt{\frac{\pi}{2}\frac{FBW}{g_0g_1}} \tag{4.1}$$

$$\frac{J_{j,j+1}}{Y_0} = \frac{\pi FBW}{2}\frac{1}{\sqrt{g_jg_{j+1}}} \quad for\ j = 1\ to\ n-1 \tag{4.2}$$

$$\frac{J_{n,n+1}}{Y_0} = \sqrt{\frac{\pi}{2}\frac{FBW}{g_ng_{n+1}}} \tag{4.3}$$

where $Y_0 = 1/Z_0$ and $Z_0 = 50$-Ω. The J-inverters are realized by obtaining even- and odd-mode characteristic impedances of the coupled microstrip line resonators. They can be obtained by the following equations:

$$(Z_{0e})_{j,j+1} = \frac{1}{Y_0}\left[1 + \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right] \quad j = 0\ to\ n \tag{4.4}$$

$$(Z_{0o})_{j,j+1} = \frac{1}{Y_0}\left[1 - \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right] \quad j = 0\ to\ n \tag{4.5}$$

The width and spacing of coupled-sections can be found from Z_{0e} and Z_{0o} using Line-Calc tool in Keysight PathWave ADS. The length of the resonators is determines the center frequency of the filter.

Using the technique mentioned above, edge-coupled BPFs for combined bands n257 and n258, and band n260 are designed. The design process of edge-coupled BPF starts with selecting 0.043-dB equal-ripple Chebyshev values for the lowpass filter prototype and calculating $J_{j,j+1}/Y_0$. From these values, even- and odd-mode impedances of coupled sections are calculated. These values are given in Table 4.1. It is to be noted that due to even-order filter, the last g-value is not the same as the first one, resulting in asymmetric even- and odd-impedance values. However, it can be noted that Z_{0e} and Z_{0o} for the first and the last g-value are very close to each other and this difference can be accommodated

Table 4.1: Computed design parameters for fourth-order edge-coupled BPF for band n260.

j	g_j	$J_{j,j+1}/Y_0$	$(Z_{0e})_{j,j+1}$	$(Z_{0o})_{j,j+1}$
0	1	0.5148	88.9925	37.5110
1	0.9305	0.2249	63.7774	41.2827
2	1.2917	0.1728	60.1346	42.8522
3	1.5764	0.2249	63.7774	41.2827
4	0.7624	0.5148	88.9944	37.5110
5	1.2204	-	81.6231	37.6837

while tuning the filter.

For 8% FBW, the response after simulation showed an even smaller bandwidth so the next iteration is started with a higher FBW value. Next, Z_{0e} and Z_{0o} are converted into widths, spacing and lengths of coupled-line sections for microstrip realization. To maintain structural symmetry, terminal coupled sections are assumed to have same widths and spacings and their lengths are optimized to obtain 38.5 GHz center frequency. The initial set of values for microstrip realization of band n260 edge-coupled BPF are given in Table 4.2

Although the response of the filter depicted decent electrical performance, it failed one critical design rule: spacing of the terminal coupled-line sections. For reliable fabrication

Table 4.2: Microstrip realization parameters of fourth-order edge-coupled BPF for band n260.

j	W_j (μm)	s_j (μm)	L_j (μm)
1, 5	90.25	14.6	1232
2, 4	140.92	41.08	1163
3	148.67	57.744	1192

Table 4.3: Optimized microstrip realization parameters of fourth-order edge-coupled BPF for band n260.

j	W_j (μm)	s_j (μm)	L_j (μm)
1, 5	43.33	30.12	1243
2, 4	113.91	37.45	1213
3	124.394	52.8	1182

process with high yield, the spacing of this coupled line sections is fixed to about 30-μm and re-optimization of the entire structure is performed, resulting in values given in Table 4.3. Due to fixing the spacing of first and last line-section, other parameters are optimized to maintain the desired response. The most significant changes are in the widths: $W_{1,5}$ and $W_{2,4}$, whereas the rest of parameters do not require substantial tuning. These simulations are performed in the frequency range of 14-50 GHz in both Schematic and Momentum simulators in Keysight PathWave ADS.

A total of eight filter structures are designed for demonstration of diplexers. The response of a few of them are shown in the following figures: Figure 4.4a shows the response of hairpin filter for band n257, Figure 4.4b depicts the response of interdigital filter for band n258 and for edge-coupled filter for band n260 discussed in this section, its layout and response are presented in Figure 4.5.

4.1.3   Design of Diplexers

The proposed non-contiguous diplexer schematic is shown in Figure 4.6. It consists of two doubly-terminated bandpass filters connected through a T-junction. The T-junction has special properties in terms of different arm lengths corresponding to the center frequency of the filters. The arm lengths are complementary to each other: $\lambda_1/4$ corresponds to guided wavelength of the center frequency of lower frequency filter and $\lambda_2/4$ corresponds
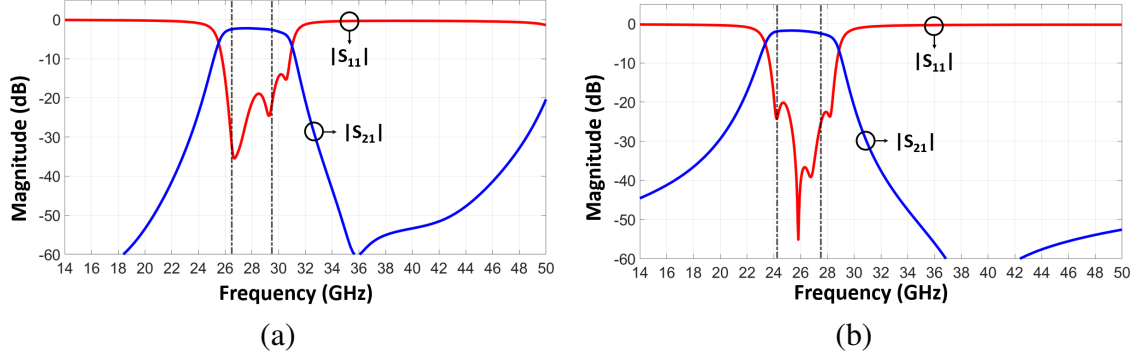
Figure 4.4: Simulated response of designed BPFs for diplexer demonstration (a) hairpin for band n257, and (b) interdigital BPF for band n258.

(a)

(b)
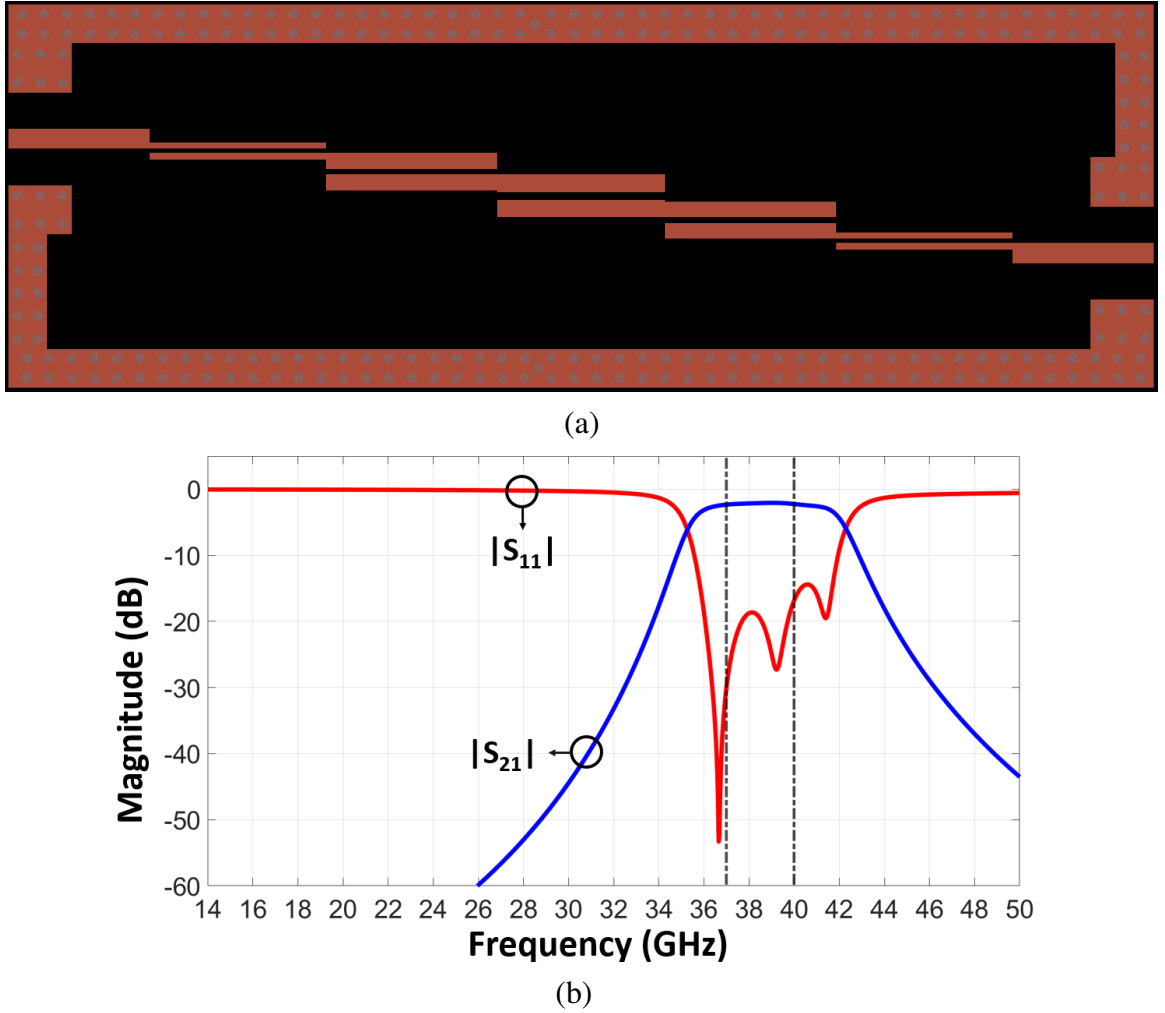
Figure 4.5: A fourth-order BPF for 5G NR band n260 (a) layout, and (b) simulation results after optimization.

131
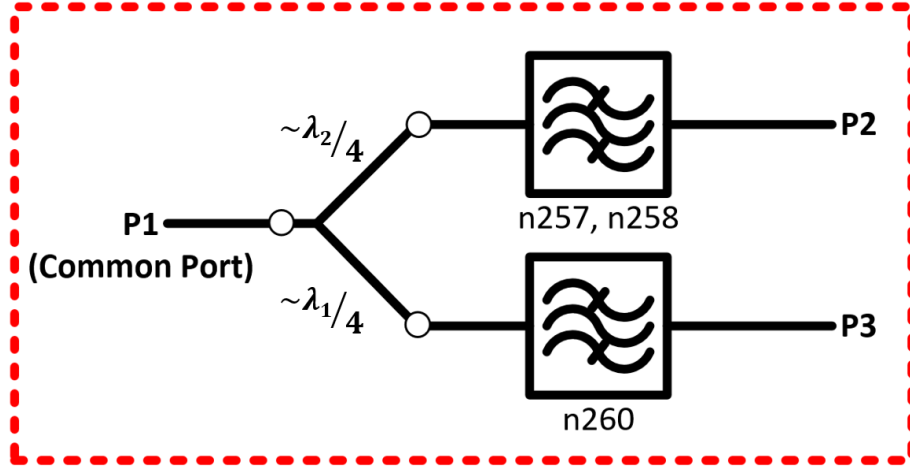
Figure 4.6: Schematic of a diplexer.
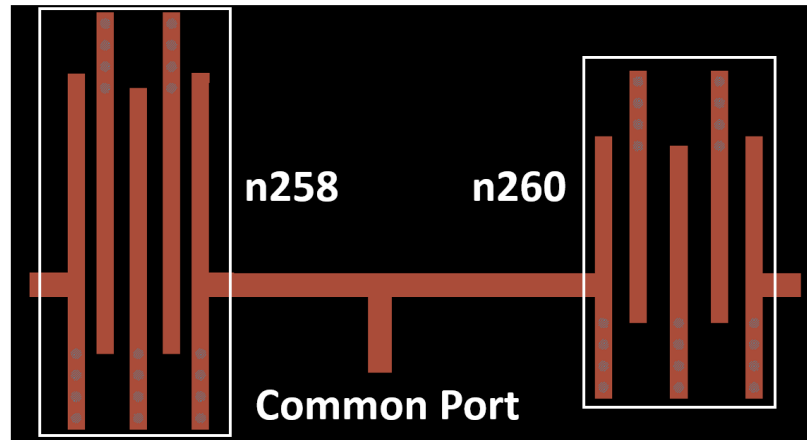
(a)
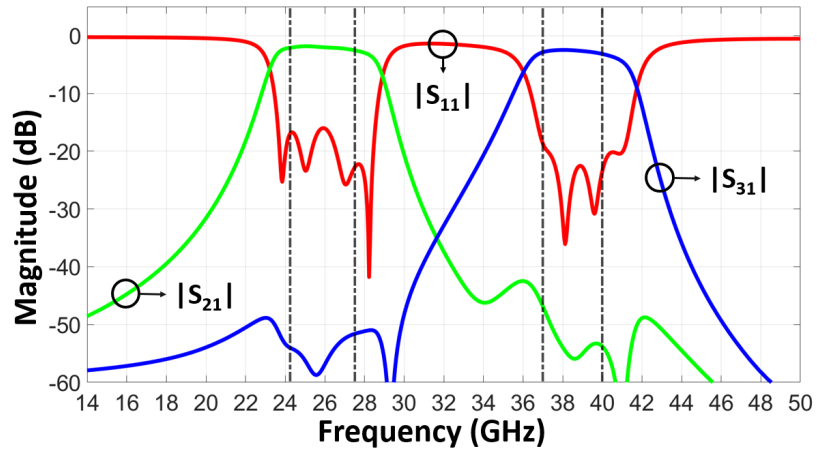
(b)

Figure 4.7: An interdigital diplexer for band n258 and n260 (a) its layout, and (b) its simulated results.

to guided wavelength of the center frequency of the higher frequency filter. In this way, the non-contiguous filters do not load each other, or more precisely, they appear as if they are "open" in the frequency range of other filter. The advantage of this approach is that filters can be tested individually as they have the same characteristic impedance on both ports, unlike the approach which utilizes singly-terminated filters. The lengths of quarter-wave sections usually needs slight optimization to improve the common-port return loss. The line widths, however, can also be tuned to improve the s-parameters but it is often unnecessary to do so. Using this method, following non-contiguous diplexers are designed:

- Hairpin diplexer for band n257 and n260

- Hairpin diplexer for band n258 and n260

- Interdigital diplexer for band n257 and n260

- Interdigital diplexer for band n258 and n260

- Edge-coupled diplexer for combined bands n257 and n258, and n260

The simulated response of an interdigital diplexer for band n258 and n260 is shown with its layout in Figure 4.7.

4.1.4 Fabrication Process

The fabrication is performed using SAP process to pattern fine-line metallization on polymer dielectric films. SAP enables fabrication of sub-10-μm features with exceptional tolerance. The process starts with silane treatment of 100-μm glass core to promote the adhesion of polymers to it and mitigate delamination during the entire fabrication process. Proper handling procedures are advised as fragility and brittleness of glass comes into play during fabrication. The silane treatment is followed by lamination of 15-μm Zaristo dielectric film on both sides of the glass panel using a vacuum laminator. The dielectric film is then cured and a 450-nm copper seed layer is deposited on it using electroless plating process. The

seed layer is patterned using a negative photoresist, followed by photolithography and photoresist development. The exposed seed layer is plated using electrolytic plating process. The target thickness of copper is 8 ± 0.5-μm. After plating, the photoresist is chemically stripped and the seed layer is etched using a differential etcher solution. This completes the patterning of M2 and M3 layers which will act as ground planes for structures on M1 and M4.

To pattern M1 and M4, the surface of the panel with M2 and M3 is treated using Novabond wet process by Atotech, which enhances the adhesion strength of the dielectric film to be bonded. Next, 71-μm Zaristo dielectric film is laminated in two steps: first 56-μm film is laminated on both sides followed by the double-sided lamination of 15-μm film.
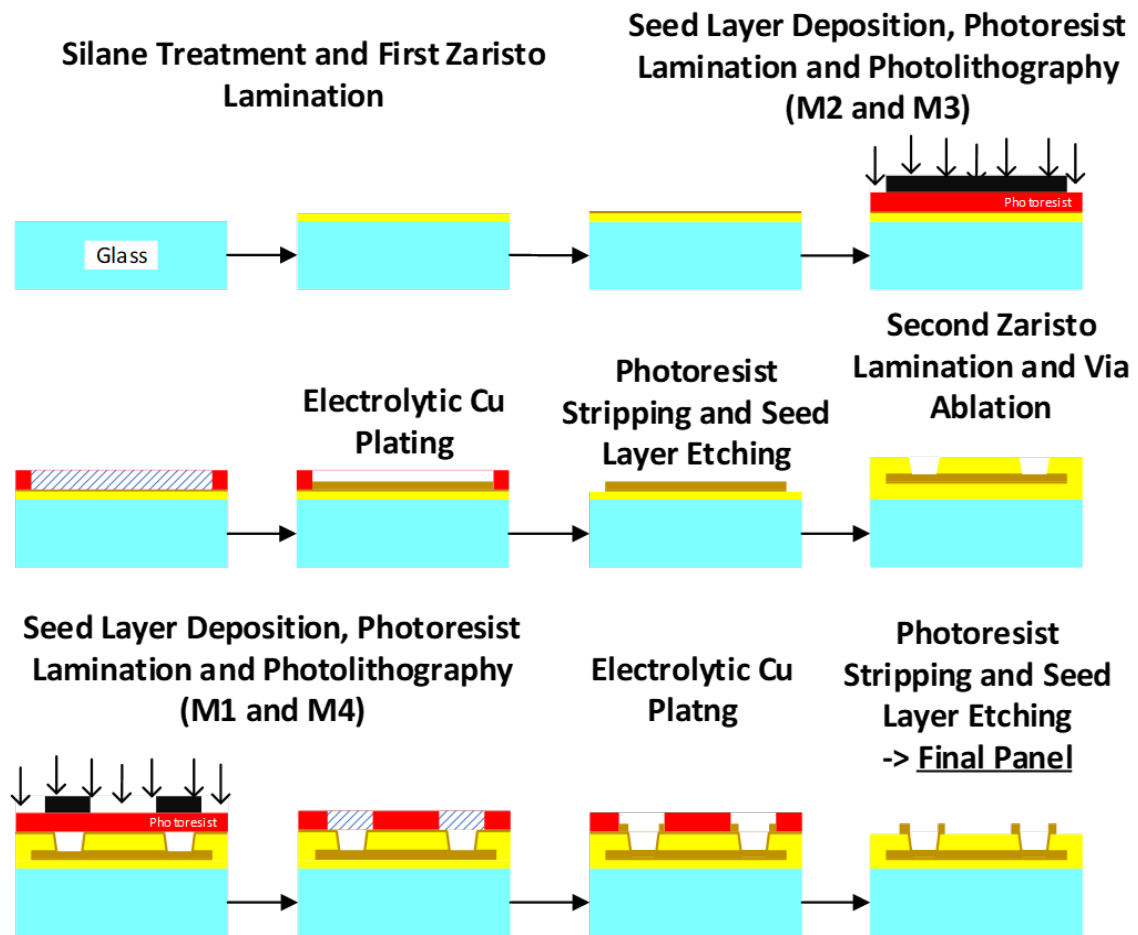
Figure 4.8: Illustration of SAP process for fabrication of diplexers with step-by-step cross sections.
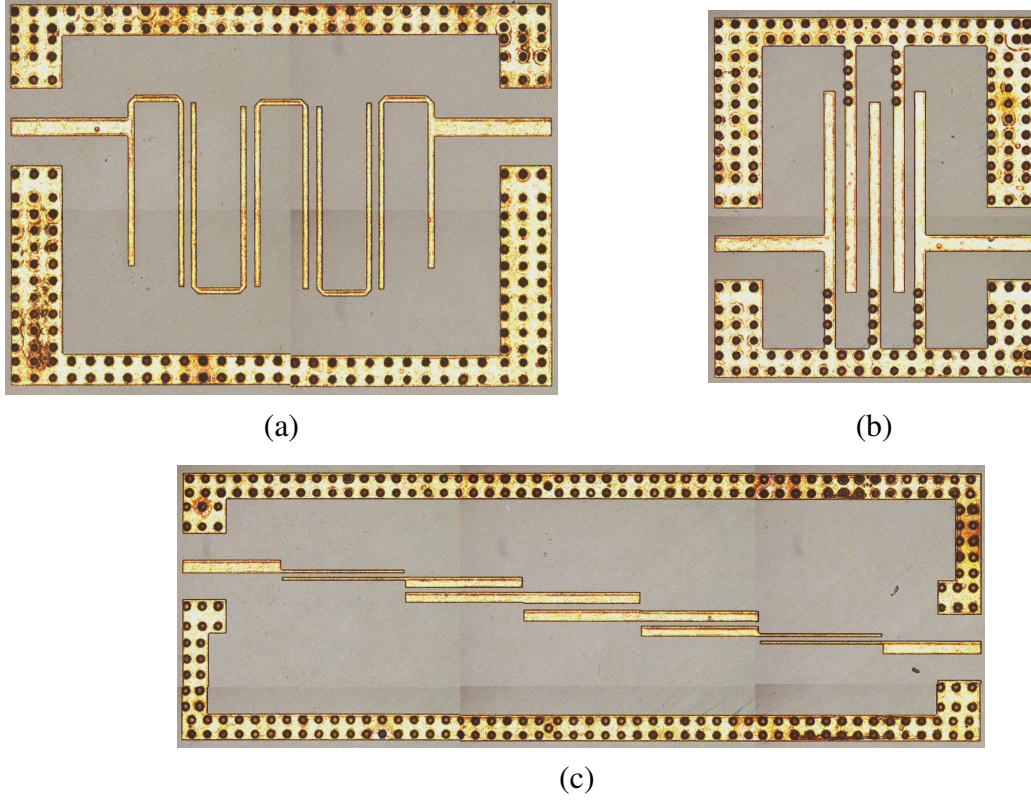
Figure 4.9: Fabricated filter coupons: (a) hairpin for band n257, (b) interdigital for band n258, and (c) edge-coupled for band n260.

The curing is performed after each lamination step. Blind via ablation is carried out using a UV laser. This process is critical as optimization is required in terms of laser power, power density and number of repetitions to ensure desired depth of vias without damaging the copper on M2 and M3. A desmear process is performed to clean the vias as well as improve the adhesion of electroless copper to polymer by roughening using a permanganate chemical etch and then the seed layer is deposited. The remaining processes are similar to those used for the patterning of M2 and M3 layers. They are repeated in order to realize M1 and M4. The measured copper thickness after patterning of all metal layers is 7.8±0.5 μm. Step-by-step cross-sections of various sub-processes of SAP are illustrated in Figure 4.8. Three of the fabricated filters for diplexer demonstration are shown in Figure 4.9. Also, some of the fabricated diplexer coupons are presented in Figure 4.10.
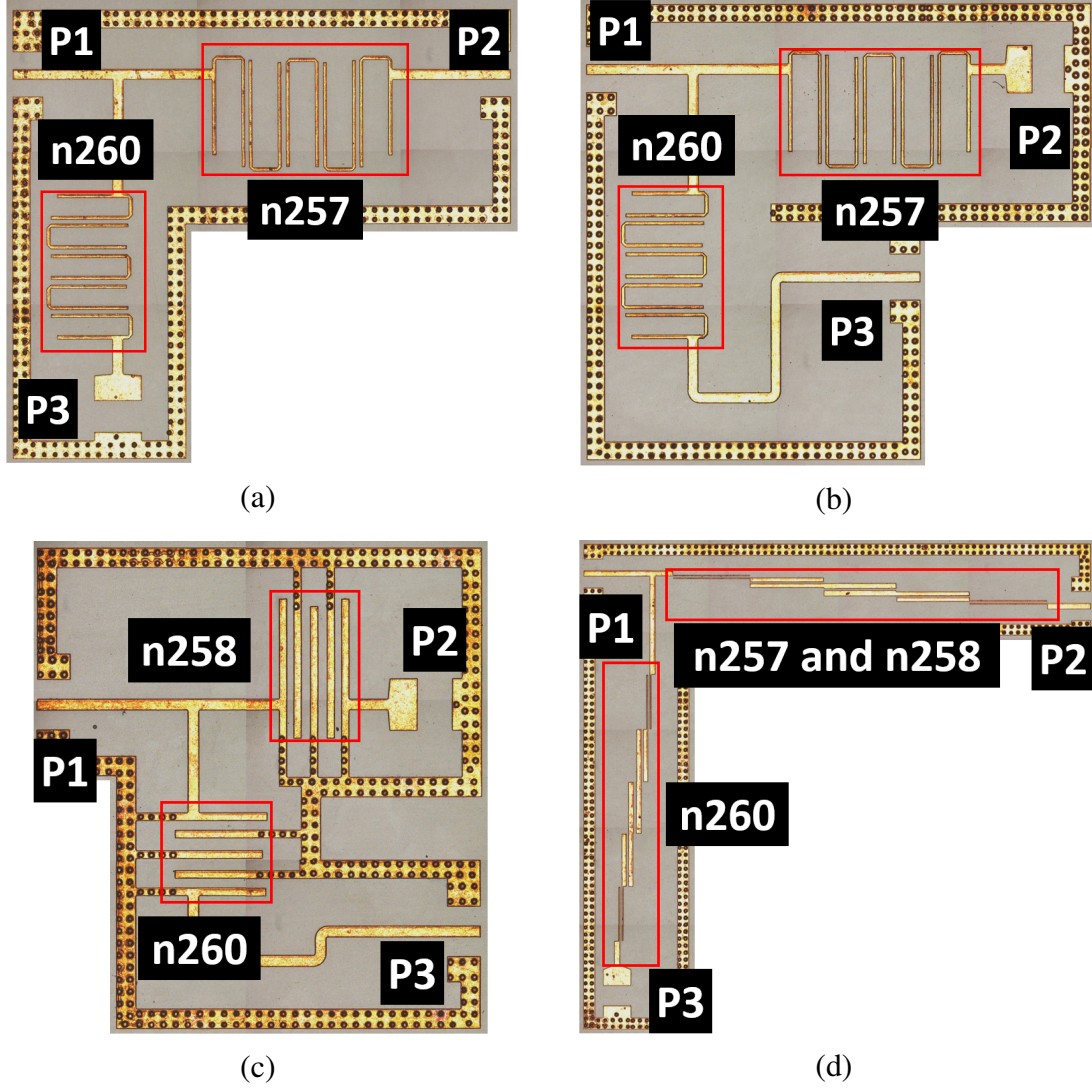
Figure 4.10: Coupons of fabricated diplexers: (a) hairpin for band n257 and n260 (S_{21} measurement only), (b) hairpin for band n257 and n260 (S_{31} measurement only), (c) interdigital for band n258 and n260 (S_{31} measurement only), and (d) edge-coupled for combined bands n257 and n258, and n260 (S_{21} measurement only).

4.1.5 Characterization Results

In this section, characterization methodology of fabricated filters and diplexers is discussed in detail. There are two fundamental limitations of available measurement setup which influence design stage. The first one is truncation of measured data at highest frequency of available VNA (40 GHz). It primarily affects measurements of band n260 as upper stopband performance cannot be observed. The second limitation which significantly results

in an extensive and elaborate design stage is the number of VNA ports (limited to two). Since diplexers are multi-port networks, several versions of the same structure need to be designed with remaining ports terminated using broadband terminators, as evident in Figure 4.10a and 4.10b. In this way, a three-port network such as a diplexer requires three design variants to obtain all six s-parameters and a four-port network requires six measurements for all sixteen s-parameters. In general, the number of measurements required to fully obtain the s-parameter matrix for a N-port network using a M-port VNA is given by Equation (4.6) [152]:

$$\binom{N}{M} = {}^{N}C_{M} = \frac{N!}{M!(N-M)!} \tag{4.6}$$

Since measurement setup is limited to two-ports only, it greatly influences the design stage. Thus, variants of diplexers are designed and fabricated in such a way that their key s-parameters (S_{11}, S_{21} and S_{31}) can be measured. The third port needs to be terminated using a broadband terminator.

Characterization Challenges and Techniques

The selection of broadband terminator is another challenge that needs to be addressed for mm-wave device characterization. There are two options given the availability of two-port measurement setup: 1) use a broadband terminator such as a high-frequency resistor, and 2) use a third GSG probe terminated with 50-Ω. The integrated passive components are designed using the former approach. High-frequency chip resistor with 0402 (1005 metric) footprint are chosen as broadband terminators [153]. Non-ideal behavior of these terminators such as unwanted reactance at high frequencies can affect the accuracy of measurements. Some of the soldered resistors are shown in Figure 4.11.

Finally, the best solution to all these challenges is to use a multi-port measurement setup with a combination of GSG and GSGSG probes. This reduces the effort in both design and
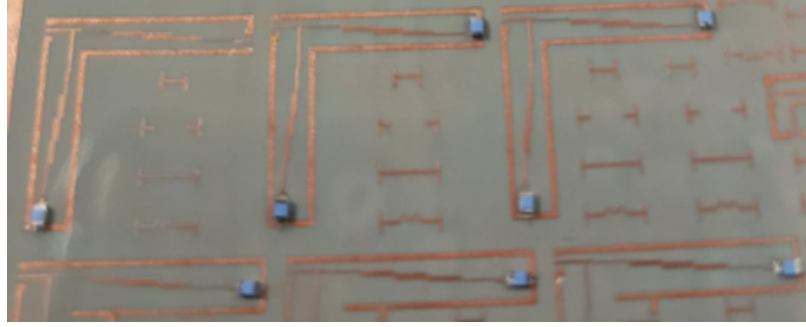
Figure 4.11: 0402 (1005 metric) footprint resistors soldered onto diplexer coupons.

fabrication stages by reducing the number of design variants, saving panel real-estate and reducing cost of fabrication and characterization. The calibration of multi-port networks can be complex but it can be performed using electronic calibration (eCal) modules [154]. The additional line lengths such as shown in Figure 4.10b and 4.10c with band n260 filter are for ease-of-measurement purposes and are de-embedded in post-processing to obtain the final measurement results from all multi-port coupons.

Characterization Results of Bandpass Filters

The simulated and measured results of hairpin BPF for band n257, interdigital BPF for band n258 and edge-coupled BPF for band n260 is shown in Figure 4.12a, 4.13a and 4.14a, respectively. The hairpin filter depicts maximum passband insertion loss of 2.6-dB, return loss more than 20-dB and VSWR less than 1.22. Similarly, the interdigital filter depicts

(a) (b)
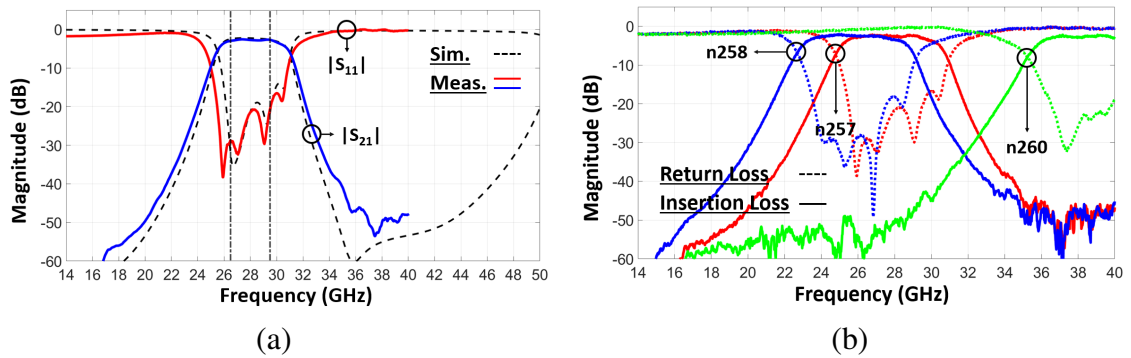
Figure 4.12: (a) Comparison of simulated and measured results of fifth-order hairpin filter for band n257, and (b) Measured results of all fifth-order hairpin filters.

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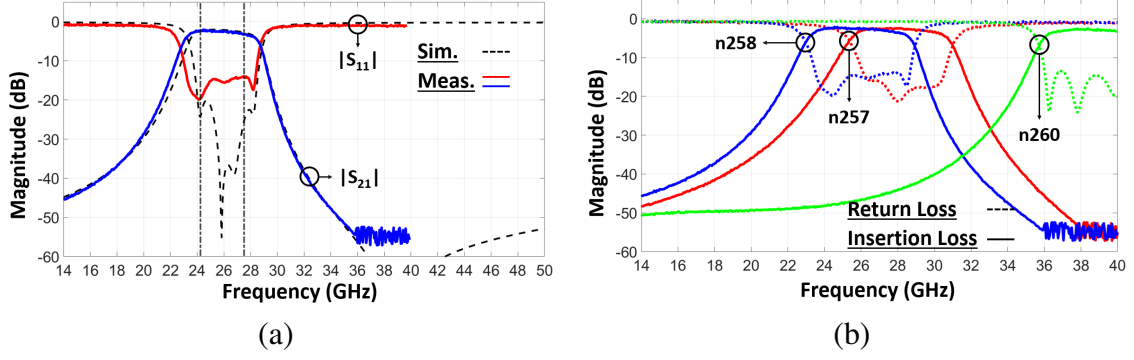
Figure 4.13: (a) Comparison of simulated and measured results of fifth-order interdigital filter for band n258, and (b) Measured results of all fifth-order interdigital filters.

the same insertion loss, its return loss is more than 15-dB and VSWR is less than 1.43. The edge-coupled filter also has the same insertion loss, return loss more than 17-dB and its VSWR is less than 1.32. The combined measured response of all fabricated hairpin, interdigital and edge-coupled filters is shown in Figure 4.12b, 4.13b, and 4.14b, respectively. The stopband performance of these filters is defined as the frequency ratio of 30-dB attenuation point to band-edge on both upper and lower sides of passband. This ratio is less than 1.17 for hairpin filters, 1.2 for interdigital filter and 1.22 for edge-coupled filters.
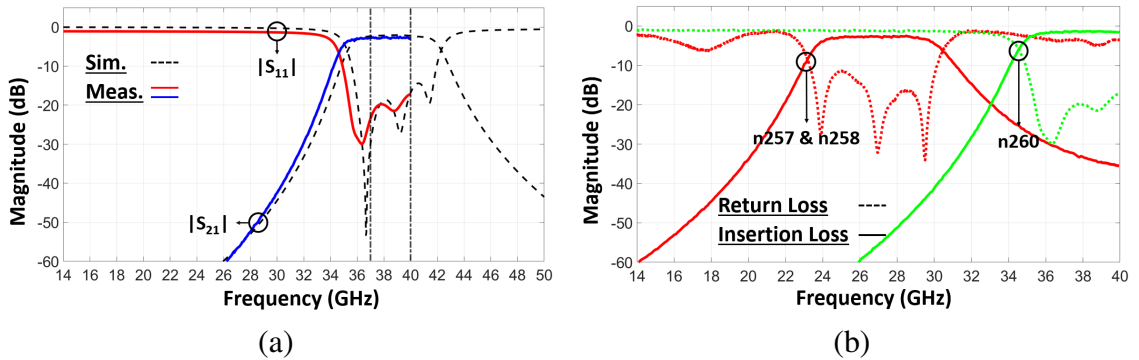
Figure 4.14: (a) Comparison of simulated and measured results of fourth-order edge-coupled filter for band n260, and (b) Measured results of both fourth-order edge-coupled filters.
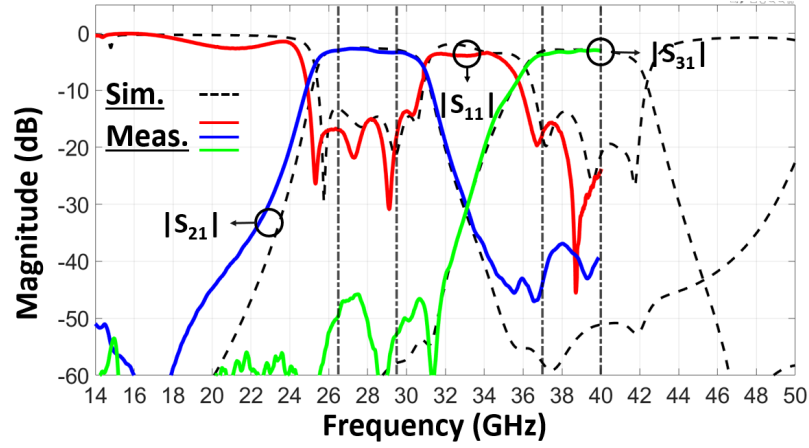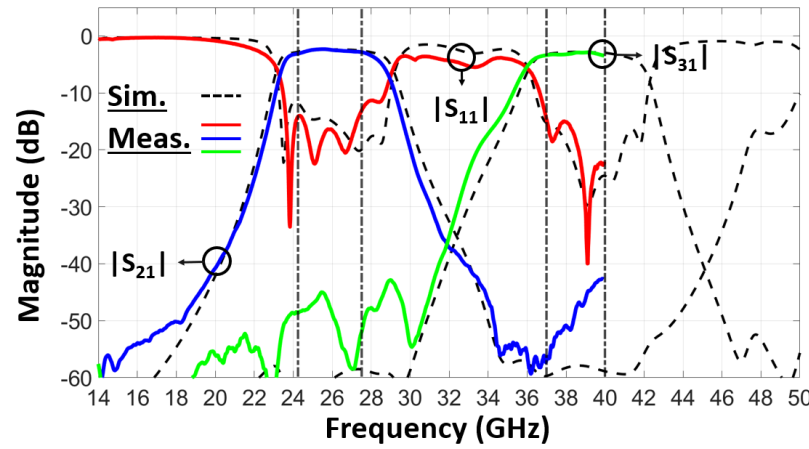
Figure 4.15: Comparison of simulated and measured results of hairpin diplexers (a) for band n257 and n260, and (b) for band n258 and n260.

Characterization Results of Diplexers

1) Hairpin Diplexers

The comparison of simulated and measured results of fabricated hairpin diplexers for band n257 and n260, and band n258 and n60 is shown in Figure 4.15. The s-parameters (S_{11}, S_{21} and S_{31}) are measured on separate coupons and combined with simulated results to show the comparison. As evident from Figure 4.15, non-ideal behavior of high frequency resistors used as broadband terminators starts appearing in the stopband region of one filter which has the same frequency as passband of other filter. This implies that impedance of broadband terminator is not purely resistive, rather it has some reactance associated with it.
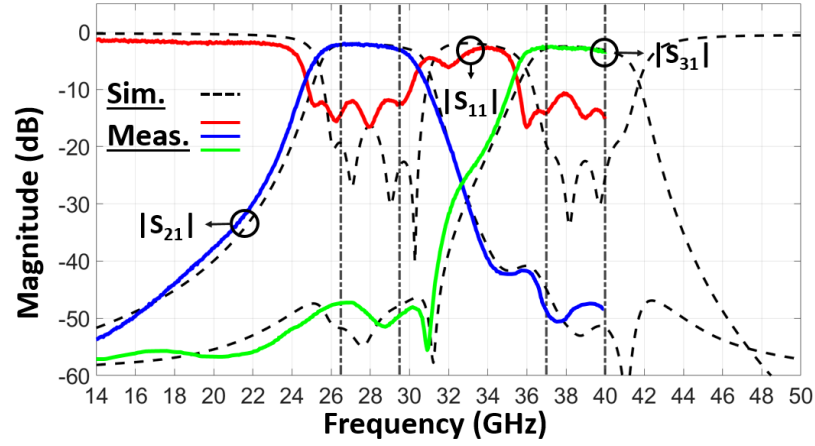
(a)
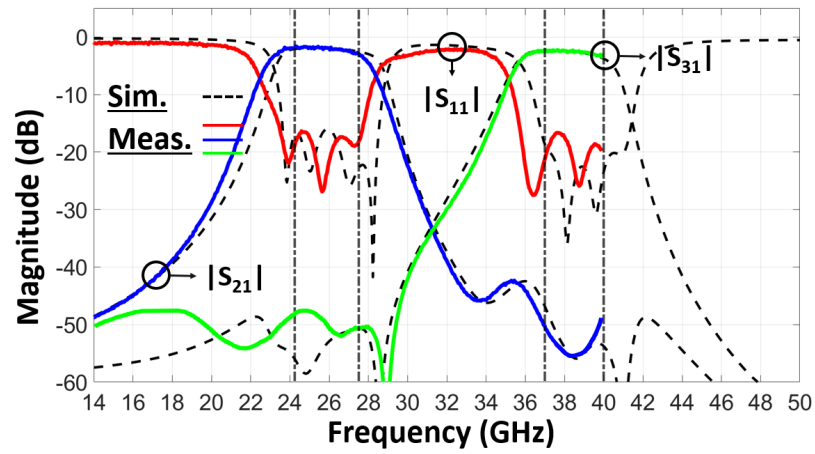
(b)

Figure 4.16: Comparison of simulated and measured results of interdigital diplexers (a) for band n257 and n260, and (b) for band n258 and n260.

The maximum passband insertion loss of both diplexers is 3-dB, return loss is better than 14-dB and VSWR is less than 1.5. The isolation between two filters in both diplexers is better than 50-dB. The cross-over point of hairpin diplexer (band n257 and n260), shown in Figure 4.15a is at 33.12 GHz with insertion loss of 30.6-dB. Similarly, the cross-over point is at 32.07 GHz with 37-dB insertion loss for hairpin diplexer (band n258 and n260) as depicted in Figure 4.15a.

2) Interdigital Diplexers

The comparison of simulated and measured results of fabricated interdigital diplexers for band n257 and n260, and band n258 and n60 is shown in Figure 4.16. The resultant effect
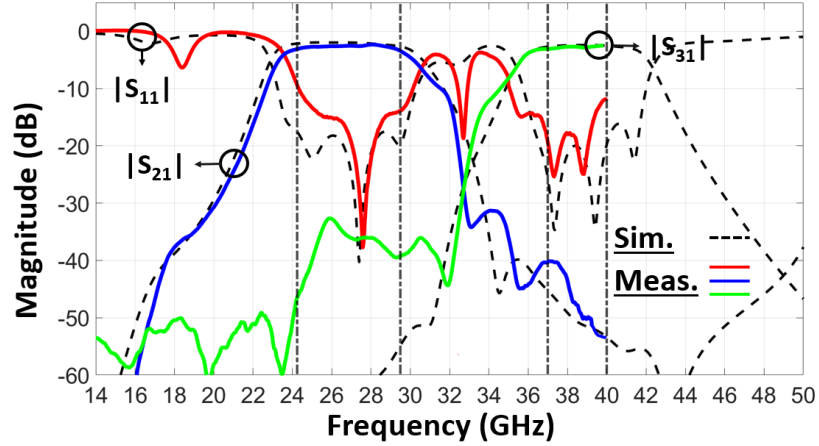
Figure 4.17: Comparison of simulated and measured results of edge-coupled diplexer for combined bands n257 and n258, and n260.

of non-ideal behavior of broadband terminators is also evident in these diplexers. The maximum passband insertion loss of both diplexers is 3-dB, return loss is better than 10.5-dB and VSWR is less than 1.92. The isolation between the two filters of both diplexers is better than 45-dB. The cross-over point for band n257 and n260 diplexer is at 32.66 GHz with 26.5-dB insertion loss and for band n258 and n260 diplexer, the cross-over point is at 31.43 GHz with 34-dB insertion loss.

3) Edge-Coupled Diplexers

The comparison of simulated and measured results of edge-coupled diplexer for combined bands n257 and n258, and n260 is shown in Figure 4.17. Out of all the measured responses of the diplexers, this one suffered most from non-ideal behavior of the terminator as evident by stopband response of band n260 filter in 28 GHz passband. The maximum passband insertion loss of this diplexer is 3-dB, return loss is better than 14.3-dB and VSWR is less than 1.48. The isolation between two filters is better than 40-dB. The cross-over point of both filters is at 32.73 GHz with insertion loss of 27-dB.

4.1.6   Dimensional Analysis and Comparison with Recent Prior Art

The dimensions of the fabricated structures along with their electrical dimensions are given in Table 4.4. The electrical dimensions are obtained by normalizing their physical dimen-

Table 4.4: Physical and electrical dimensions of fabricated filters and diplexers.

Structure	Physical Dimensions (mm³)	Electrical Dimensions (λ_0^3)
Filter - Hairpin n257	4.64×2.11×0.202	0.42×0.19×0.018
Filter - Hairpin n258	4.75×2.20×0.202	0.43×0.20×0.018
Filter - Hairpin n260	4.14×1.72×0.202	0.53×0.22×0.026
Filter - Interdigital n257	2.98×2.62×0.202	0.27×0.23×0.018
Filter - Interdigital n258	2.94×2.76×0.202	0.26×0.25×0.018
Filter - Interdigital n260	3.12×2.17×0.202	0.40×0.28×0.026
Filter - Edge-coupled n257 and n258	9.16×0.56×0.202	0.82×0.05×0.018
Filter - Edge-coupled n260	6.09×0.75×0.202	0.78×0.10×0.026
Diplexer - Hairpin n257 & n260	5.85×4.42×0.202	0.63×0.47×0.022
Diplexer - Hairpin n258 & n260	6.42×4.67×0.202	0.69×0.50×0.022
Diplexer - Interdigital n257 & n260	4.54×4.36×0.202	0.49×0.47×0.022
Diplexer - Interdigital n258 & n260	4.40×4.60×0.202	0.47×0.49×0.022
Diplexer - Edge-Coupled n257, n258 & n260	11.2×8.49×0.202	1.2×0.91×0.022

sions by free-space wavelength (λ_0) corresponding to the operating frequency. The center frequency (f_c) of 28 GHz 5G band (24.25-29.5 GHz) is 26.875 GHz and corresponding λ_0 is 11.16-mm. Similarly, λ_0 is 7.8-mm for f_c of 39 GHz band (38.5 GHz). For diplexers, couplers and their integrated versions, f_c of 24.25-40 GHz band is used to obtain their electrical dimensions. The corresponding λ_0 is 9.34-mm.

The filters have a footprint smaller than $0.12\lambda_0^2$, hairpin and interdigital diplexers are smaller than $0.35\lambda_0^2$, and edge-coupled diplexer is smaller than $1.1\lambda_0^2$. In spite of their compact size and small footprint, they depict excellent performance in terms of passband inser-

Table 4.5: Comparison of diplexers using various substrate technologies for mm-wave applications.

Ref.	Substrate / Structure	f_{cL} & BW (GHz) IL (dB)	f_{cH} & BW (GHz) IL (dB)	Size (mm^2)
[131]	Rogers Laminate / Microstrip	14 & - 1.9	28 & - 4.7	∼80
[155]	Rogers Laminate / Microstrip	32 & 2 3.5	35 & 1.3 3.2	645.16
[156]	Rogers Laminate / SIW	24.925 & 1.35 2.05	26.8 & 1.8 1.95	∼2500
This Work	Laminated Glass / Microstrip	28 & 3 3	38.5 & 3 3	25.86
This Work	Laminated Glass / Microstrip	25.875 & 3.25 3	38.5 & 3 3	20.24

tion loss, stopband rejection, selectivity and their ease-of-use in heterogeneously-integrated packages since they can be implemented in top metal layers of RF FEM packages or pre-fabricated as standalone IPDs. The diplexers are also compared with similar structures in literature in terms of center frequency of low-band (f_{cL}) and high-band (f_{cH}) filter, bandwidth, insertion loss and size in Table 4.5. The demonstrated filters and diplexers are the smallest structures reported in terms of x-y dimensions as well as z-height for package-level applications

4.2 Integrated Passive Components

For the design and demonstration of integrated passive components, a diplexer is combined with a coupler covering the entire 24.25-40 GHz band. This integrated block of diplexer and coupler finds its place in a power detection and control circuitry in a modern RF power amplifier (PA) front end module (FEM) whose schematic diagram is shown in Figure 4.18 and is used as an example in this work [157]. It consists of an amplifier block

in conjunction with a diplexer, a directional coupler with power detector and an antenna array. It is typically used in WCDMA and GSM/EDGE systems for their output power control requirements, specially under mismatched load conditions [158, 159]. The filters in diplexer act as harmonic filters and they combine the signals coming from 28 and 39 GHz band amplifiers. The coupler can have variable or fixed coupling factor depending upon the required level of control on output power. The transmitter chain in Figure 4.18 is used to quantify distortion of the fabricated block as well as to discuss an co-simulation approach to compare passive components using system-level performance metrics such as EVM. The choice of modulation schemes $\pi/4$ differential quadrature phase shift keying ($\pi/4$ DQPSK) and 64-state quadrature amplitude modulation (64-QAM), but any desired modulation scheme can be used.

4.2.1 Material Stackup

The material stackup for design and demonstration is the same as discussed in Section 4.1.1.
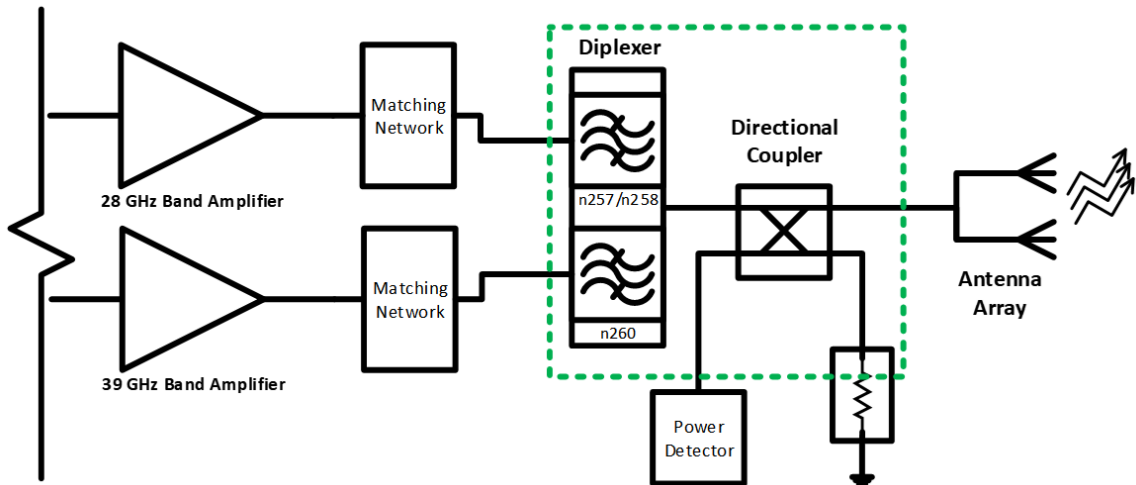
Figure 4.18: A power detection and control circuity in a power amplifier FEM.

4.2.2 Design of Integrated Passive Components Block

The coupler is an important component in this RF transmitter chain as it samples a fraction of power from the main signal line and the sampled power can be used as a feedback to control output power of the amplifier to meet the transmission power standards. Its layout and port designations are shown in Figure 4.19a. The s-parameters are related to coupler parameters as follows:

- Return loss: S_{11}

- Insertion loss: S_{21}

- Coupling factor: S_{31}

- Isolation: S_{41}

For this demonstration, a passive, three-section coupled-line coupler with 20-dB coupling factor is designed which can be connected to a power detector and measure the

(a)　　　　　　　　　　　　(b)

(c)
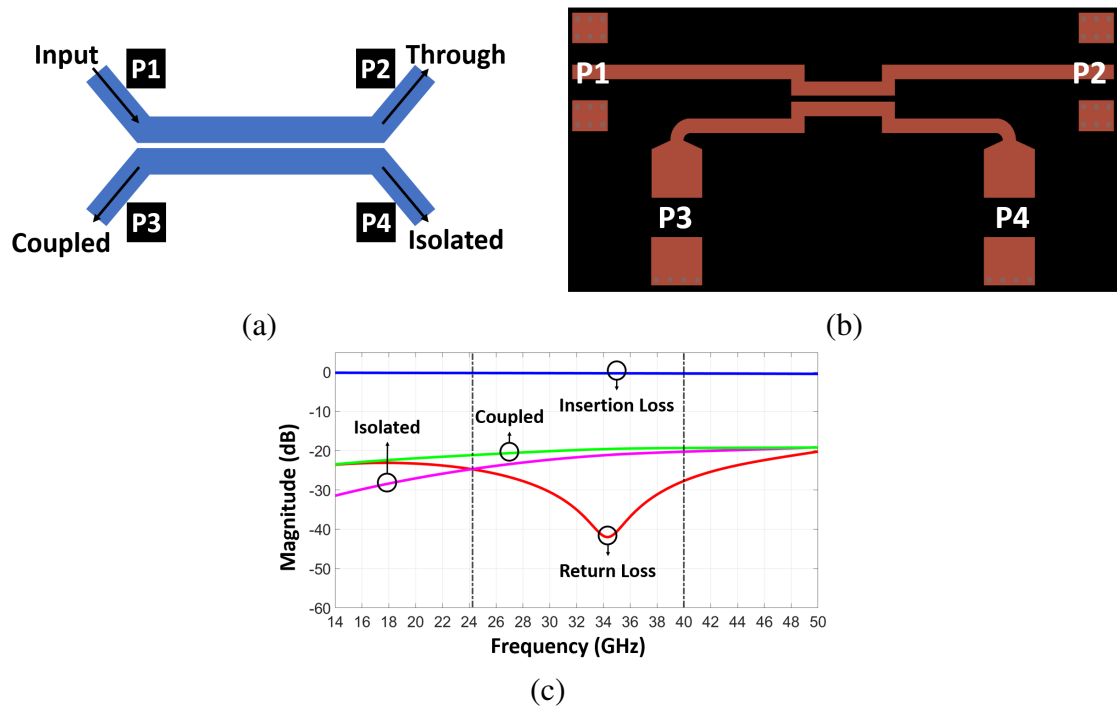
Figure 4.19: (a) Layout of a single-section coupled-line coupler. (b) Layout of a three-section 20-dB coupled-line coupler covering 24.25-40 GHz, and (c) its response.

output power of the antenna. Multi-section coupler design is discussed in detail in [113, Chapter 7]. The design process involves calculating even- and odd-mode impedances for multi-section coupled-lines which can then be converted into microstrip coupled-lines using LineCalc tool in Keysight PathWave ADS. Three-section coupler is selected because it can easily cover the desired frequency range. Since coupling factor is selected to be 20-dB, only 1% of power is coupled from main line of the coupler to its coupled section, ensuring better signal integrity in the critical signal path to antenna. The coupler covers desired bandwidth of 24.25-40 GHz and has a maximum passband insertion loss of 0.35 dB with small variation in coupling in the desired frequency range. One critical condition for constant coupling factor is termination at the isolation port of coupler. Variations in impedances at the coupler termination ports can lead to undesired response but it can also be compensated using complex termination techniques at isolated port as discussed in [160]. The simulated response of the coupler and its layout are shown in Figure 4.19b and 4.19c, respectively.

The integrated block of passive components is also simulated to extract its response. Since it is a five-port network, characterizing it on a two-port VNA requires ten design variants. To maintain practicality in measurements, design variants are designed in such a fashion that s-parameters of the desired paths can be measured. However, the simulation results can give insights on the overall behavior of the network. The layout of the passive components block and its simulation response are depicted in Figure 4.20. Notice in Figure 4.20a, an additional line length is added with BPF for band n257. This is done in order to land the GSG probes horizontally for characterization. The result of this added line length is increased insertion loss at for band n257 BPF but it is de-embedded from the final results to obtain the simulated responses shown in Figure 4.20b and 4.20c.
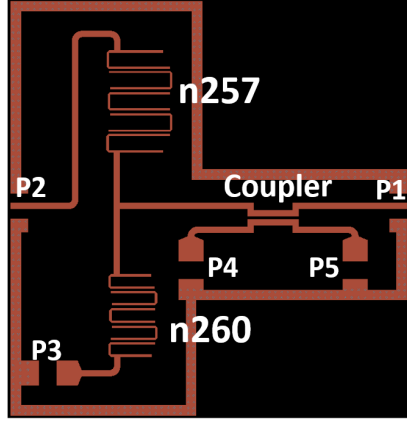
(a)
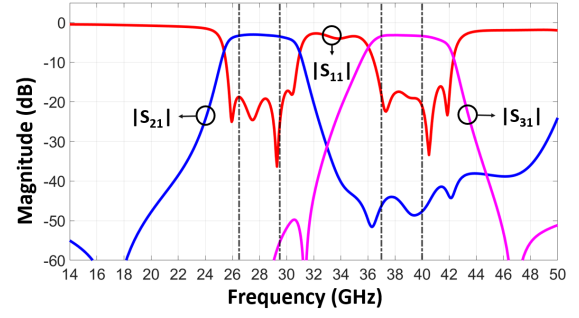
(b)
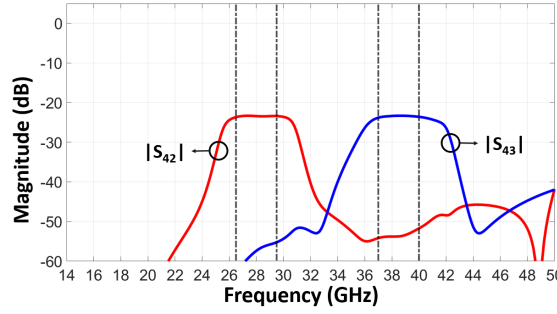
(c)

Figure 4.20: Integrated passive component block (Hairpin diplexer for band n257 and n258 combined with coupler) for S_{21} measurements only (a) layout, (b) simulated s-parameters S_{11}, S_{21} and S_{31}, and (c) S_{41} and S_{43}.

4.2.3 Fabrication Process

The process of fabricating integrated passive components is similar to the one discussed in Section 4.1.4. The fabricated variants of coupler are shown in Figure 4.21 and two of the fabricated integrated passive component blocks are depicted in Figure 4.22.

4.2.4 Characterization Results

The characterization challenges of integrated passive components are similar to the ones discussed in Section 4.1.5. The complete characterization of coupler requires six design variants but it is performed using three different design variants to measure insertion loss, coupling and isolation parameters, which are shown in Figure 4.21. The comparison of
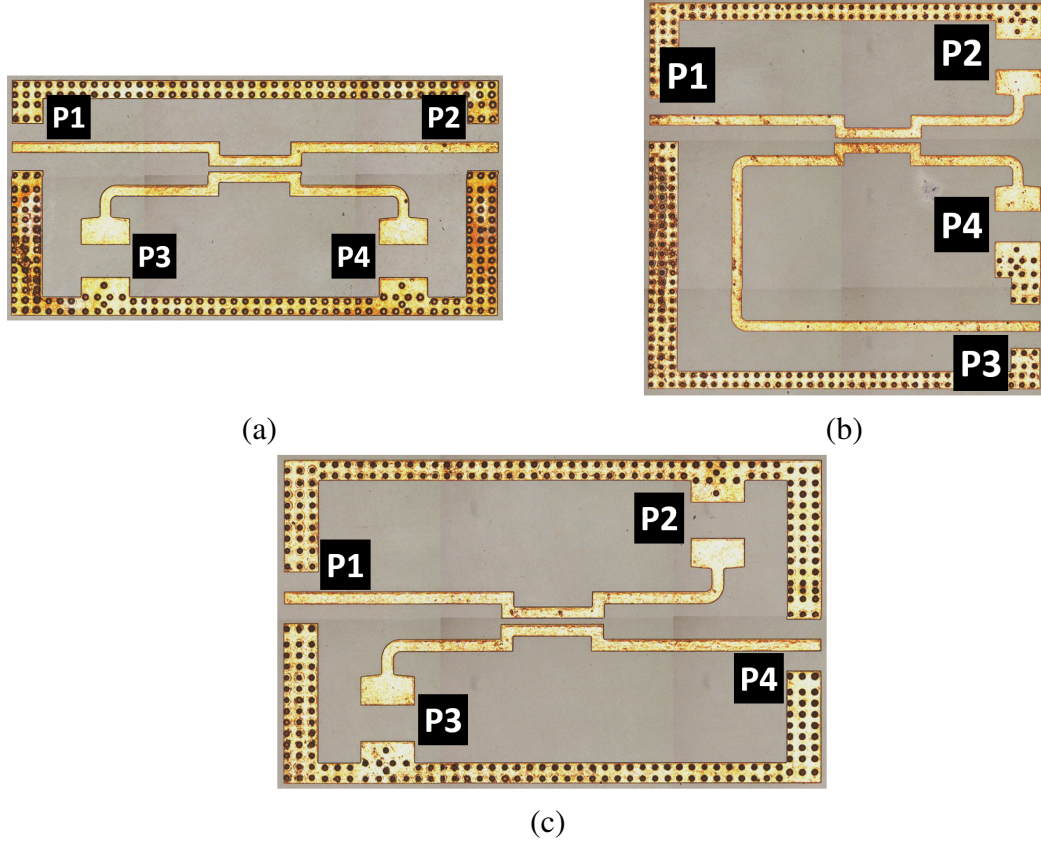
Figure 4.21: Fabricated coupler variants (a) for S_{21} measurement only, (b) for S_{41} measurement only, and (c) for S_{31} measurement only.

simulated and measured results of coupled-line coupler covering 24.25-40 GHz frequency range is shown in Figure 4.24. The maximum measured insertion loss of the coupler in the entire frequency range is 0.4-dB, return loss is more than 20-dB and coupling is about 20-dB with small variation.

Only two paths are measured for one of the fabricated integrated passive components block (hairpin diplexer for band n257 and n260 combined with coupler): band n257 filter in diplexer to the antenna port and band n257 filter to the coupled port of the coupler. All additional line lengths to accommodate for ease-of-testing are de-embedded to obtain the results shown in Figure 4.25.
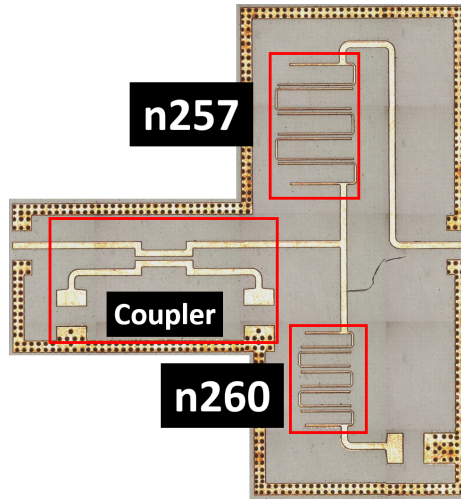
(a)
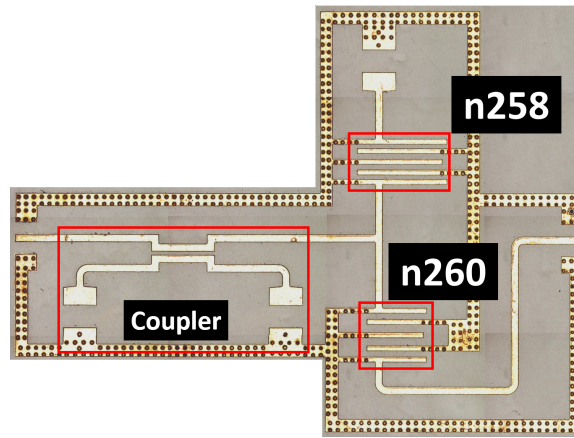
(b)

Figure 4.22: Fabricated variants of integrated passive components (a) hairpin diplexer for band n257 and n260 combined with coupler (S_{21} measurement only), and (b) interdigital diplexer for band n258 and n260 combined with coupler (S_{31} measurement only).
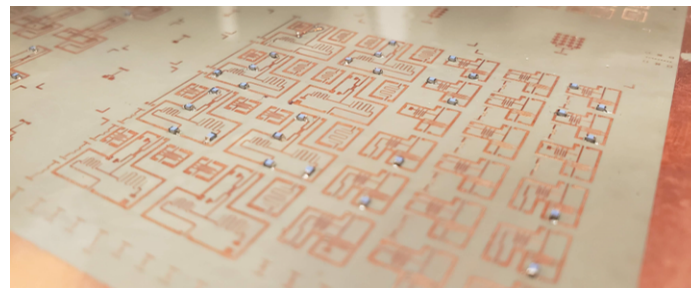
Figure 4.23: 0402 (1005 metric) footprint resistors soldered onto coupons of integrated passive components.
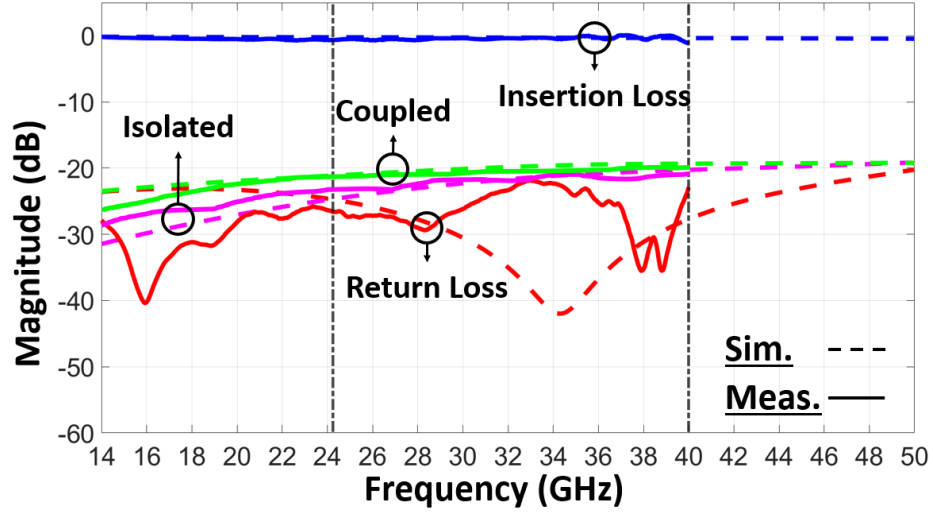
Figure 4.24: Comparison of simulated and measured results of three-section coupled-line coupler covering 24.25-40 GHz frequency range.
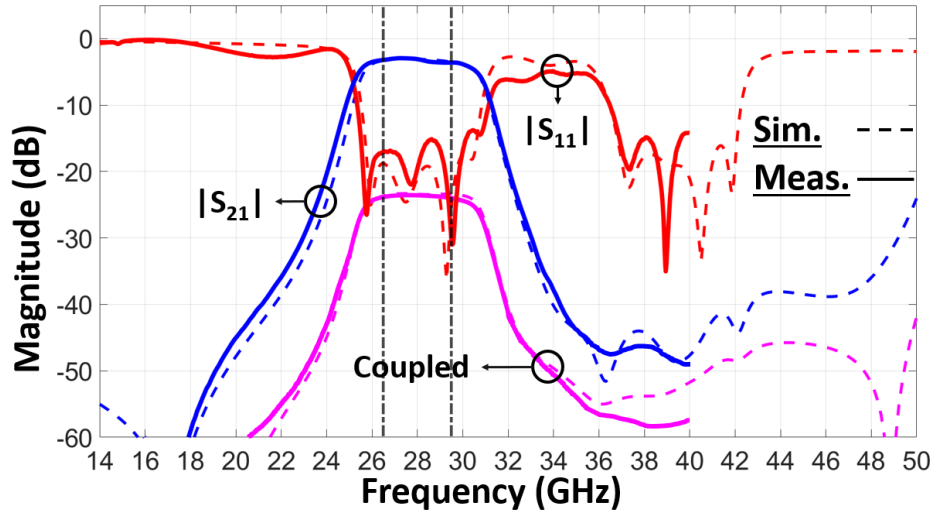
Figure 4.25: Comparison of simulated and measured results of integrated passive components block.

4.2.5   System Performance Analysis

In this section, a system-level performance analysis is presented for the integrated passive components fabricated in this paper. The purpose of these simulations is to provide insights on system performance of components in a transmitter and/or receiver chain and to provide accuracy in link budget and operation range analysis [161]. They are also useful in translating system performance metrics to component-level requirements. The hairpin diplexer

for band n257 and n260 is selected for these simulations as two-port measurements are performed to characterize the following paths:

- Path-1: RF Source -> PA -> Diplexer (band n257) -> Coupler (Thru) -> Antenna Input

- Path-2: RF Source -> PA -> Diplexer (band n257) -> Coupler (Coupled) -> Power Detector

These paths are highlighted in Figure 4.26a. They can be corroborated with the fabricated integrated passive components block as shown in Figure 4.26b. The following system-level simulations are performed to quantify the distortion caused by this block:

1. Group delay variation at antenna port and power variation at detector port of the system as RF source power is varied.

2. EVM of integrated passive component block using RF carrier modulated by $\pi/4$ DQPSK and 64-QAM.

To perform these simulations, a suitable PA with 24 to 34 GHz range of operation, 34-dBm saturated output power (P_{SAT}), 23-dB gain, 39-dBm output third-order intercept (OIP3) and 4.9-dB noise figure (NF) is selected and modeled in Keysight PathWave ADS [162]. Also, an assumption is made that all terminating impedances such as at antenna and detector port are 50-Ω. The PA is modeled in Keysight ADS along with rest of the components to form a transmitter chain. The comparison of this model with the datasheet is depicted in Figure 4.27.

System-level Simulation # 1

Using a large-signal s-parameter (LSSP) simulation, the group delay in Path-1 and power variation in Path-2 is extracted as the amplifier is driven into compression. The frequency sweep is from 22 to 34 GHz. The group delay is shown in Figure 4.28a. As evident from
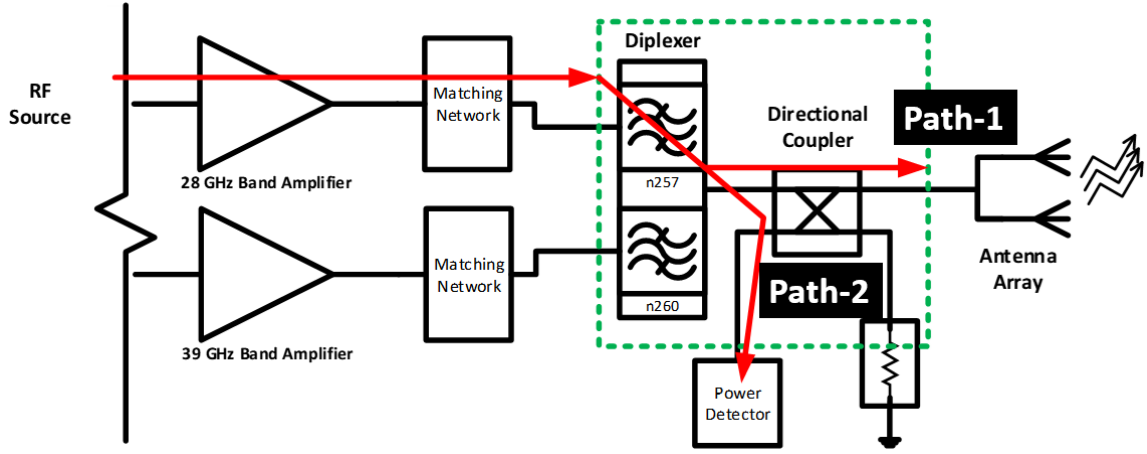
(a)
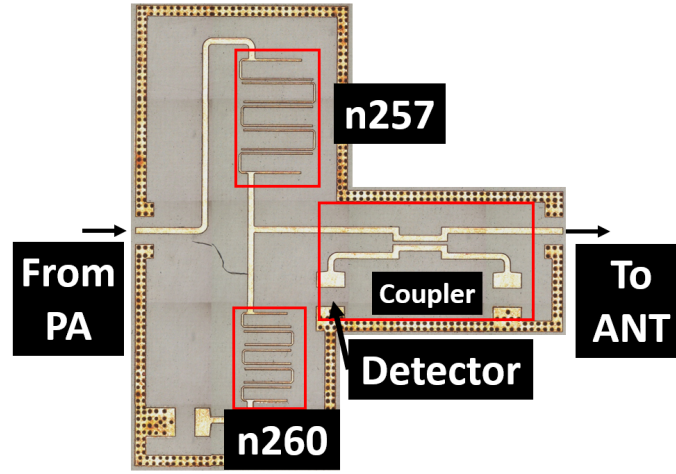
(b)

Figure 4.26: (a) PA FEM block with highlighted simulation paths, and (b) integrated passive components block.

the figure, peak group delay in Path-1 is slightly higher than 700-ps when input power to the amplifier is 0-dBm. Also, group delay contribution from standalone amplifier is about 250-300 ps which leads to 400-ps contribution from the integrated passive components block. This 400-ps group delay is comparable to state-of-the-art filters in industry: TDK $\sim$250-ps [163], Knowles >400-ps [164] and >1000-ps [165].

To check the power variation at the detector port of the coupler, RF source power is swept from 0-20 dBm with step size of 5-dBm. The output power at the detector port is
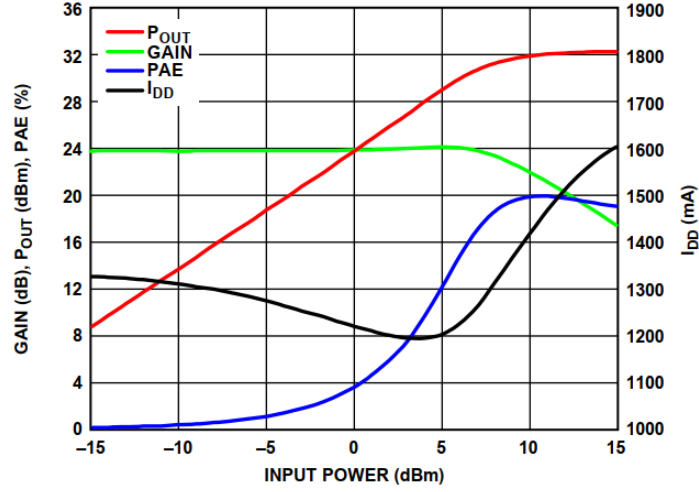
(a)
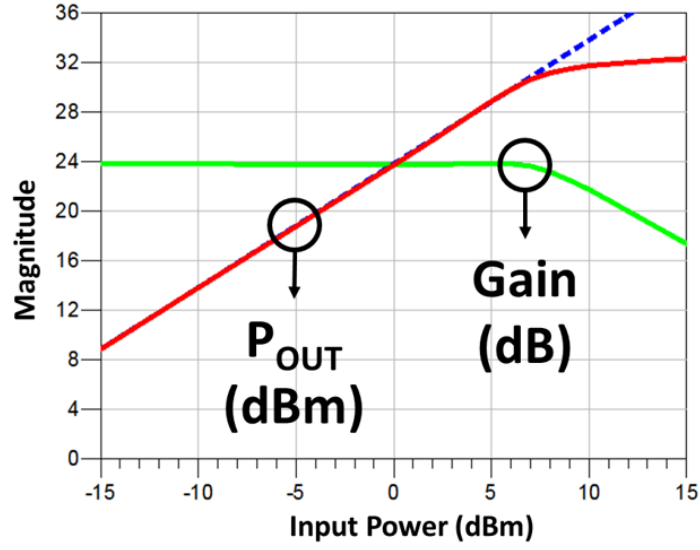
(b)

Figure 4.27: Comparison of PA model in (a) datasheet, with (b) model in Keysight PathWave ADS.

given by Equation (4.7):

$$P_{Det.}(dBm) = P_{RF\_in}(dBm) + Gain_{Amp.}(dB) - Loss_{Dip.}(dB) - C(dB) \qquad (4.7)$$

where P_{RF_in} is the power level of RF source, $Gain_{Amp}$ is amplifier gain, $Loss_{Dip.}$ is the insertion loss of band n257 filter leg in diplexer and C is coupling factor of the coupler. The
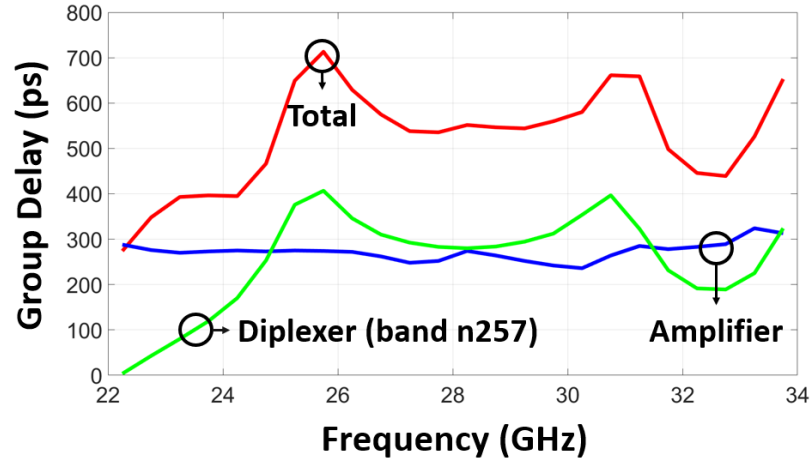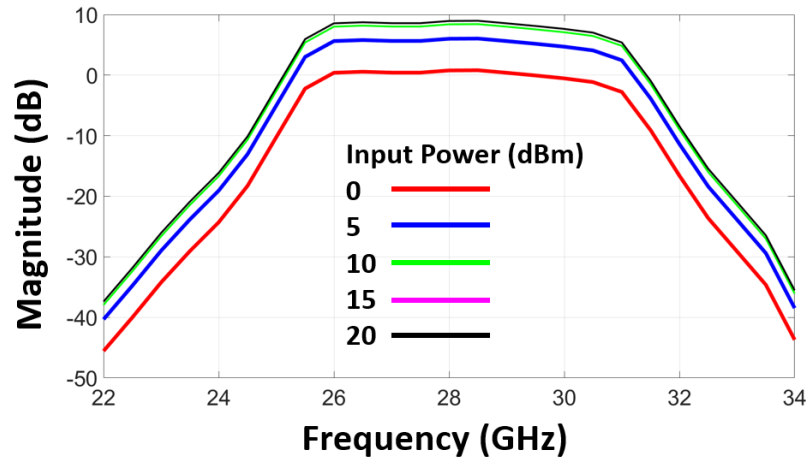
Figure 4.28: (a) Group delay distortion observed in path-1, and (b) power variation at detector port of coupler as RF source power is increased (path-2).

amplifier is driven into saturation when P_{RF_in} reaches 8-dBm and afterwards it operates in compression. As a result, power variation at the detector port of coupler can be observed in Figure 4.28b. The power at detector port saturates as RF source power is increased. A peak power detector can be used to track power variation and can be used as feedback to control the output power of amplifier.

System-level Simulation # 2

The performance of a digital communication system is typically estimated with EVM, which is the magnitude of difference between a complex transmitted data symbol and its

ideal counterpart as discussed in Chapter 1. It is a figure of merit of modulation accuracy. In addition to worst-case EVM for $\pi/4$ DQPSK and 64-QAM modulated signals, a technique is presented in this section to characterize EVM of Path-1 in Figure 4.26a and how it is related to component parameters. Before calculating EVM for 5G NR radio transmission and reception in practice, measured waveform is corrected by sampling timing offset, RF frequency offset, removal of carrier leakage and equalization in the receiver. The EVM level of each NR carrier for 5G are specified by 3GPP and for QPSK and 64-QAM as 17.5% and 8%, respectively [12, 34].

A variety of different modulation techniques such as phase shift keying (PSK) and quadrature amplitude modulation (QAM) with 16, 64 and 256 states are considered for 5G applications along with orthogonal frequency division multiplexing (OFDM) scheme, similar to LTE [166]. It is to be noted that for purpose of this demonstration, the carrier frequency and symbol rate are scaled to 5G NR mm-wave bands. In this particular case, an ideal receiver is used to demodulate the 28 GHz RF source modulated by $\pi/4$ DQPSK waveform with 3 GHz symbol rate. For reference, spectral efficiency of $\pi/4$ DQPSK is better in comparison to QPSK, 8-PSK and DQPSK and this is why it is selected as a lower order modulation scheme for this research [167]. As the symbol rate is equal to bandwidth of band n257, worst-case performance is evaluated.

(a)   (b)
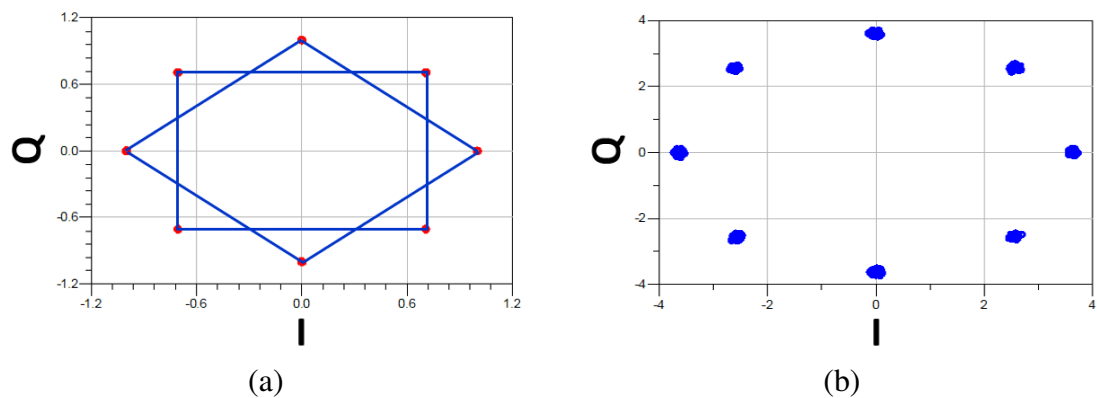
Figure 4.29: Constellation diagram of $\pi/4$ DQPSK signal with 3 GHz symbol rate modulated on 28 GHz RF carrier (a) ideal, and (b) distorted.
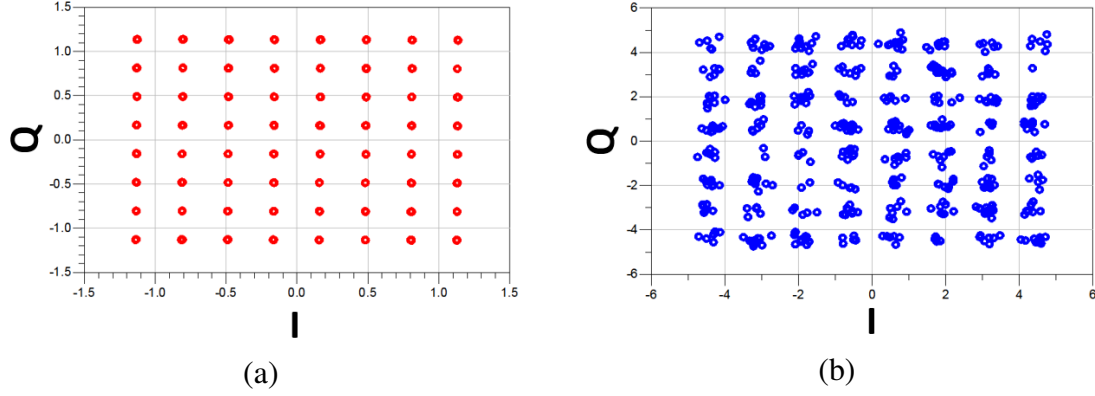
Figure 4.30: Constellation diagram of 64-QAM signal with 3 GHz symbol rate modulated on 28 GHz RF carrier (a) ideal, and (b) distorted.

EVM includes the effects of filter (diplexer), coupler and PA nonlinearity in this case. The ideal and distorted constellation of 28 GHz RF carrier modulated by $\pi/4$ DQPSK is shown in Figure 4.29. The symbol rate is selected to be equal to bandwidth of the band n257 filter: 3 GHz. The total EVM is 2% out of which 0.1% is contributed by the amplifier. The rest is the EVM signature of integrated passive components block. It is to be noted that the source power is set to 0-dBm so that the amplifier operates in linear region. Similarly, the ideal and distorted constellation of 28 GHz RF carrier modulated with 64-QAM signal and 3 GHz symbol rate is depicted in Figure 4.30. In this case, total EVM is 5.6%, which is 2.4% lower than the specified levels for 64-QAM by 3GPP for 5G NR. As mentioned earlier for EVM measurements, this value will be lower in practice after the corrections schemes are applied at the receiver.

Sweeping RF carrier frequency with variable symbol rate can give an insight on effects of various component design parameters on EVM [168]. The methodology presented in this section can also be scaled to extract EVM contributions with various modulation sources in conjunction with performance metrics of mm-wave filters, diplexers and other passive components [169]. To understand the contribution of insertion loss variation to EVM, 64-QAM modulated RF carrier with 1.5, 2 and 3 GHz symbol rate is swept over passband of two filters (A and B) for band n257 as shown in Figure 4.31. It can be seen that as
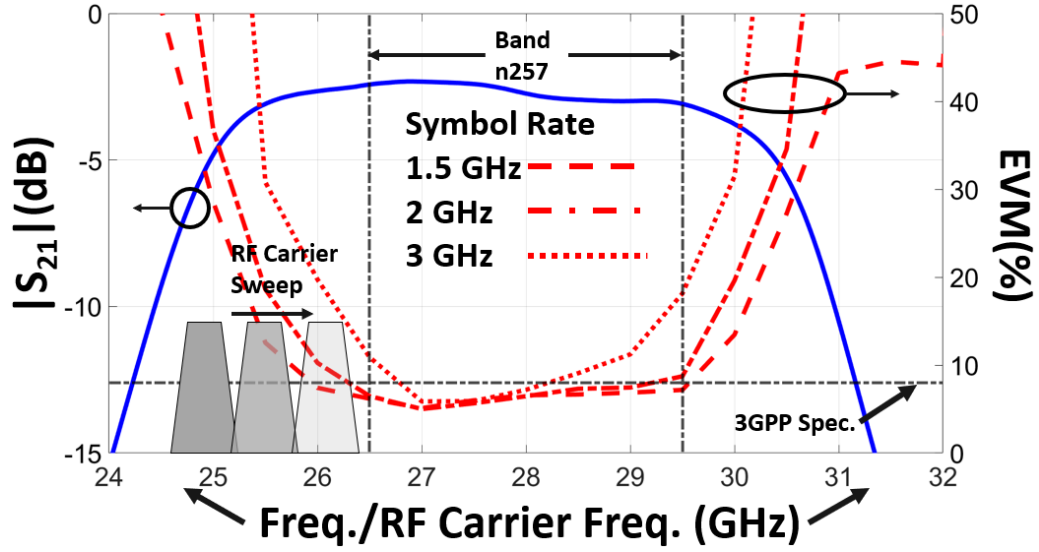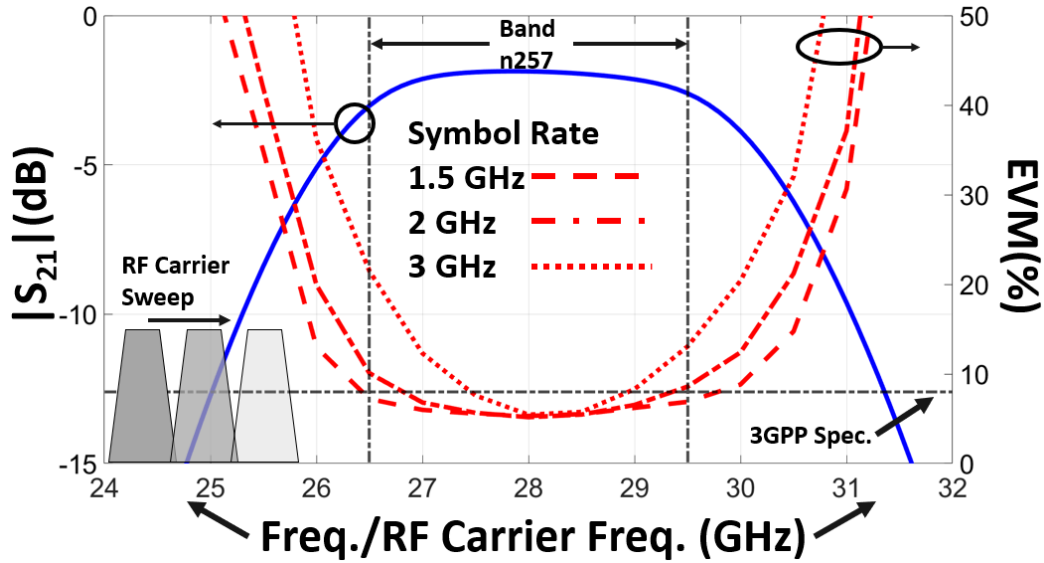
Figure 4.31: Simulated EVM compared to insertion loss variation and bandwidth of band n257 filter in diplexer using 64-QAM modulated RF carrier frequency sweep with varying symbol rate (a) filter A, and (b) filter B.

symbol rate is increased from 50% to 100% of filter bandwidth, EVM degrades rapidly. It increases as RF carrier frequency is close to band edge of the filter. This can help in defining the specifications of filters. Given the low ripple of the fabricated filter in the diplexer, EVM has low variation (ΔEVM<2.3% for 1.5 GHz symbol rate) for filter A with minimum value of 5.6%. Similar behavior is observed for filter B: it has a minimum EVM

of 5.2% and due to lower ripple, ΔEVM is less than 1.9% for 1.5 GHz symbol rate, which is 17.4% smaller than filter A. Also, the asymmetric response of EVM is representative of asymmetric rejection roll-off of filters on both sides of filter passband. Thus, it can be concluded that EVM is sensitive to component parameters: it is correlated to ripple, bandwidth as well as roll-off factor of a filter. Moreover, this methodology can be used to compare similar filters and other passive components such as power dividers or phase shifters, based on their system-level performance metric such as EVM.

4.3 Summary

In this chapter, high-performance and miniaturized diplexers and integrated passive components are presented for the first time on ultra-thin laminated glass substrates. Key performance and miniaturization attributes of diplexers are given in Table 4.6. The comparison of objectives and accomplishments of integrated passive components are given in Table 4.7.

In this chapter, diplexers using miniaturized filters are presented on ultra-thin laminated

Table 4.6: Comparison of objectives and accomplishments for diplexers.

Topics	Metrics	Objectives	Accomplishments
Diplexers	Performance	• Filter design: doubly terminated • IL < 3-dB • RL > 20-dB • Isolation > 40-dB	• Doubly terminated filters for diplexer design • Max. IL < 3-dB • RL > 20-dB for a large fraction of bandwidth • Isolation > 50-dB for Hairpin Diplexer, > 45-dB for Interdigital Diplexer, > 40-dB for Edge-Coupled Diplexer
	Miniaturization	• Footprint: $< 2\lambda_0 \times 2\lambda_0$	• Footprint: $< 0.12\lambda_0^2$ for filters, $< 0.35\lambda_0^2$ for hairpin and interdigital diplexers, and $< 1.1\lambda_0^2$ for edge-coupled diplexer

Table 4.7: Comparison of objectives and accomplishments for integrated passive components.

Topics	Metrics	Objectives	Accomplishments
Integrated Passive Components	System Performance Analysis	• EVM < 17.5% for QPSK • EVM < 8% for 64-QAM (Defined by 3GPP for 5G)	• EVM < 2% for QPSK • EVM < 5.6% for 64-QAM • Extraction of EVM for the integrated passive component block in a RF transmitter chain. • Developed a co-simulation technique to analyze the relationship of electrical performance metrics of passive components (filters) to system performance metric such as EVM

glass substrates for mm-wave applications in emerging RF FEMs. Miniaturized hairpin, interdigital and edge-coupled doubly-terminated bandpass filters, covering 5G NR mm-wave bands: n257, n258 and n260 are used to design non-contiguous diplexers. SAP process is rigorously optimized for metallization patterns on laminated ultra-thin glass substrates to obtain reliable dimensions and tight variation tolerance. As a result, the diplexers have excellent model-to-hardware correlation. They depict low insertion loss, low VSWR, high stopband rejection, high selectivity, high isolation and ease-of-integration in packages. Small footprint of these diplexers along with their electrical performance makes them ideal candidates for heterogeneously-integrated 5G and mm-wave RF FEMs.

Along with a wideband coupler, these passive components are also configured in a power detection and control circuitry, and a co-simulation methodology is introduced to evaluate the effect of component interactions on group delay variation, power variation, and distortion in amplitude and phase using EVM as the performance metric. It is observed that the fabricated integrated passive components block introduces a peak group delay of 400-ps. The power variation at detector port of coupler can be used as feedback to control the output power of the amplifier. Moreover, a relationship between filter parameters such as insertion loss, ripple, center frequency and bandwidth, and EVM is presented to compare

two filters using RF carrier modulated with 64-QAM signal. This approach extracts the EVM signature of passive components and thus, it can be used to discriminate between similar structures as EVM is sensitive to component parameters. Also, it can be scaled to test other passive components using the methodology discussed in this chapter.

CHAPTER 5

RESEARCH SUMMARY, NOVELTY OF RESEARCH AND SUGGESTIONS FOR FUTURE WORK

5.1 Research Summary

The objective of this research is to model, design, fabricate and characterize integrated passive components for 5G and mm-wave applications on advanced substrates such as ultra-thin laminated glass. These passive components include filters, power dividers, antenna arrays, diplexers and their integrated versions. The target frequency range of these passive components are the 5G new radio (NR) bands: 28 and 39 GHz and the bands of interest are in the Frequency range 2 (FR2) as defined by 3GPP: n257, n258 and n260.

Both circuit-level simulation and full-wave electromagnetic (EM) simulation are employed to design these passive components for 5G and mm-wave applications. Glass substrate is emerging as an ideal candidate to realize mm-wave technologies. This is mainly because of its low loss, superior dimensional stability, ability to form fine-pitch through-vias, stability to temperature and humidity, matched coefficient of thermal expansion (CTE) with devices, and availability in large-area, low-cost panels. Passive components such as filters, power dividers, antenna arrays and diplexers can benefit from the aforementioned advantages of glass substrates along with precision redistribution layers (RDL) to enable miniaturization. These components can be designed and fabricated to achieve dimensions of less than twice the free space wavelength corresponding to the operating frequency and can be integrated in electronic packages such as RF front-end modules (FEM), as integrated passive devices (IPD). Precision linespace capabilities also empower the designer to opt for higher-impedance structures for filters, reducing the footprint. The demonstrated filters exhibit low loss, low standing wave ratio (VSWR) and high selectivity. Similarly,

the power dividers are designed and fabricated in two-, three- and four-way equal-split ratios, and they can used in low-power on-device antenna-to-chip chain to provide power to corresponding antenna array configurations. Moreover, they utilize minimal matching techniques to efficiently cover the entire 28 GHz 5G band and exhibit low VSWR as well as minimal phase shift variation between the output ports. Yagi-Uda antennas are used to demonstrate antenna arrays utilizing the designed power dividers.

The diplexers are designed using the filters for 5G NR bands and they exhibit low insertion loss, high stopband rejection, high selectivity, ease-of-integration in packages as well as small footprint. The diplexers are also integrated with couplers to emulate a power detection and control circuitry in a modern RF power amplifier (PA) FEM. The coupler covers the entire 5G mm-wave bands: from 24.25 GHz to 40 GHz. Using this integrated passive component block as an example, a system performance analysis using a co-simulation technique is presented to quantify the distortion in amplitude and phase produced by the fabricated passive component block. Moreover, the scalability of this approach to compare similar passive components based on their specifications and evaluation of their signature using a system-level performance metric such as error vector magnitude (EVM) is discussed.

For the fabrication of these passive components, semi-additive patterning (SAP) process is utilized using a glass substrate as a core. Unlike subtractive patterning process, where a thick copper foil is etched off from the undesired areas to form circuit patterns, SAP yields better dimensional and copper sidewall control. Finally, dimensional analysis is performed to find the discrepancy between desired and obtained feature dimensions. All of the demonstrated passive components have a footprint which is a fraction of the unit free-space wavelength of their operating frequencies. It is observed that the feature dimensions do not vary by more than 5%, resulting in an excellent model-to-hardware correlation of fabricated passive components. Thus, the superiority of glass based IPDs for RF FEMs is demonstrated.

5.2 Novelty of Research

The novelty of this research lies in the design and demonstration of miniaturized integrated passive components for 5G and mm-wave applications on ultra-thin laminated glass substrate. Within this broad research, there are many novelties that are pursued and demonstrated. According to author's knowledge, no comprehensive work is dedicated to modeling, design, fabrication and characterization of passive components: filters, power dividers, antenna arrays, diplexers and their integrated versions for 5G mm-wave frequency bands. The target 5G bands are 28 (US) and 39 GHz (EU) bands along with the bands of interest in FR2 as defined by 3GPP: n257, n258 and n260.

Glass substrates is an emerging candidate to realize mm-wave technologies mainly because of its low loss tangent, superior dimensional stability, ability to from fine-pitch low-loss vias, stability to temperature and humidity variations, matched CTE as well as panel-scale low-cost processing. Moreover, it can be laminated with low-loss polymers, which act as redistribution layers for precision metal patterns, on which passive components can be realized. Compared to on-chip and traditional off-chip methodologies of realizing passive components, on-package approach on laminated glass substrates is advantageous as it enables short interconnect lengths with excellent electrical performance and miniaturization while taking advantage of multiple combined attributes of LTCC and organic laminate substrate technologies. These components can be utilized in RF FEMs either as integrated films in substrates or as IPDs. The modeling and design phase of these passive components includes the utilization of both circuit-level and full-wave simulation. SAP process is utilized for fabrication of each passive component to obtain precision metallization patterns with rectangular profile, unlike subtractive etching which can lead to issues such as undercut and trapezoidal profiles of the deposited patterns. The variation tolerance in dimensions of the realized features is below 5%.

The filters reported in this research exhibit low insertion loss, low VSWR and high se-

lectivity. Their footprint is also smaller than twice the free-space wavelength corresponding to the operating frequency of 5G mm-wave bands. Analysis of recent prior art mentioned in this dissertation suggests that these filters are few of the smallest reported structures with respect to footprint and z-height, while also featuring superior electrical performance. Similarly, power dividers are designed and fabricated in two-, three- and four-way equal-split ratios for low power on-device antenna-to-chip chain to provide power to corresponding antenna array configurations. Moreover, they utilize minimal matching techniques to efficiently cover the entire 28 GHz 5G band and exhibit low VSWR as well as minimal phase shift variation between the output ports. Yagi-Uda antennas are used to demonstrate antenna arrays utilizing the designed power dividers. Their footprint is smaller than unit free-space wavelength corresponding to the 28 GHz band frequency.

Finally, the diplexers are designed using filters for 5G NR bands to exhibit low insertion loss, high stopband rejection, high selectivity, ease-of-integration in packages as well as small footprint as compared to recent prior art reported in the literature. The diplexers are also integrated with a broadband coupler to form an integrated passive component block commonly found in a power detection and control circuitry in a modern PA FEM. Using this integrated passive component block as an example, system performance analysis using a co-simulation technique is presented to quantify the distortion in amplitude and phase produced by the fabricated passive component block. Moreover, the scalability of this approach to compare with similar passive components based on their specifications and evaluation of their signature using a system-level performance metric such as EVM is discussed for the first time for 5G and mm-wave passive components.

5.3   Suggestions for Future Work

Modeling, design, fabrication and characterization of 5G passive components on ultra-thin laminated glass substrates form the key focus of this dissertation. Suggestions for future research directions are provided below:

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- Filters are one of most important passive components in a transceiver. In this work, planar filters on ultra-thin laminated glass are extensively discussed. However, alternative filtering topologies that take advantage of the excellent electrical, mechanical and thermal properties of glass also hold lot of promise. Particularly, planar filters based on SIW, lossy filters, reflection-less and absorptive filters, multiple band BPFs and tunable filters are potential research tracks for mm-wave filters.

- The work on power dividers can be extended to feeding networks for N-element antenna arrays which are a requirement for 5G applications. Moreover, N-way power dividers with minimal and wideband matching techniques are useful for small-cells and line-of-sight communications.

- Diplexers and multiplexers based on acoustic wave filters have dominated the sub-7 GHz domain due to their superior electrical performance and small footprint. However, those technologies are currently not scalable to mm-wave frequency range. Therefore, multiplexers with novel filtering structures and different filter combinations (LPF & BPF, BPF & BSF & BPF and others) need to be explored.

- System performance analysis of passive components in mm-wave range has been introduced in this research. This work can be extended to extract system performance signature of passive components based on different metrics commonly utilized to evaluate performance of a RF chain. Moreover, experimental verification techniques of system-level performance signature can also be investigated.

- Passive components with multiple functional capabilities: filtering power dividers, power dividers with tunable split-ratio and others can be evaluated for their potential applications in 5G transceivers.

5.4 Publications and Awards

The research outcomes from this dissertation and other research-related activities of the PhD candidate have resulted in the following publications and awards:

Peer-reviewed Journals

1. **M. Ali** *et al.*, "First Demonstration of Compact, Ultra-Thin Low-Pass and Bandpass Filters for 5G Small-Cell Applications," in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 12, pp. 1110-1112, Dec. 2018. [170]

2. **M. Ali**, A. Watanabe *et al.*, "Package-Integrated, Wideband Power Dividing Networks and Antenna Arrays for 28 GHz 5G New Radio Bands," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 9, pp. 1515-1523, Sept. 2020, doi: 10.1109/TCPMT.2020.3013725. [171]

3. A. Watanabe, T-H Lin, **M. Ali** *et al.*, "Ultra-Thin Antenna-Integrated Glass-Based Millimeter-Wave Package with Through-Glass Vias," in *IEEE Transactions on Microwave Theory and Techniques*, doi: 10.1109/TMTT.2020.3022357. [172]

4. A. Watanabe, **M. Ali** *et al.*, "A Review of 5G Systems Package Integration," accepted for publication in *IEEE Transactions on Components, Packaging and Manufacturing Technology*.

5. **M. Ali** *et al.*, "Laminated Glass-based, Compact Inline Stepped-Impedance Resonator Bandpass Filters for 5G New Radio Modules," submitted to *IEEE Transactions on Components, Packaging and Manufacturing Technology*.

6. **M. Ali**, A. Watanabe *et al.*, "Package Integration and System Performance Analysis of Glass-based Passive Components for 5G New Radio Millimeter-Wave Modules," submitted to *IEEE Transactions on Microwave Theory and Techniques*.

Conference Proceedings

1. A. O. Watanabe , **M. Ali** *et al.*, "First Demonstration of 28 GHz and 39 GHz Transmission Lines and Antennas on Glass Substrates for 5G Modules," *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, 2017, pp. 236-241. [173]

2. **M. Ali** *et al.*, "Miniaturized High-Performance Filters for 5G Small-Cell Applications," *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, 2018, pp. 1068-1075. [174]

3. A. Watanabe, T. Lin, **M. Ali** *et al.*, "3D Glass-Based Panel-Level Package with Antenna and Low-Loss Interconnects for Millimeter-Wave 5G Applications," in *Proc. IEEE IMC-5G*, August 2019. [175]

4. **M. Ali**, A. Watanabe *et al.*, "3D Glass Package-Integrated, High-Performance Power Dividing Networks for 5G Broadband Antennas," *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2019, pp. 960-967. [176]

5. **M. Ali**, A. Watanabe *et al.*, "Ultra-Wideband, Glass Package-Integrated Power Dividers for 5G and mm-Wave Applications," *2019 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Atlanta, GA, USA, 2019, pp. 863-864. [177]

6. **M. Ali**, A. Watanabe *et al.*, "Heterogeneous Integration of 5G and Millimeter-Wave Diplexers with 3D Glass Substrates," in *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, 2020, pp. 1376-1382. [178]

7. T. Kakutani, D. Okamoto, Z. Guan, Y. Suziki, **M. Ali** *et al.*, "Advanced Low Loss Dielectric Material Reliability and Filter Characteristics at High Frequency for mmWave

Applications," in *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, 2020, pp. 653-659. [179]

8. A. Watanabe, **M. Ali** *et al.*, "Glass-Based IC-Embedded Antenna-Integrated Packages for 28-GHz High-Speed Data Communications," in *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, 2020, pp. 89-94. [180]

Book Chapters

M. Ali, P. M. Raj, R. Tummala, "Applications of packaging technologies in communication systems," in *Fundamentals of Device and Systems Packaging: Technologies and Applications*, Second Ed., Vol. 2, McGraw Hill Professional, 2019, pp.729-751.

Awards

1. Fulbright Scholar at Georgia Institute of Technology (MS ECE, 2015-2017)

2. Second Position in Poster Presentation in "Future Car: New Era of Automotive Electronics" workshop, held at Georgia Institute of Technology (2017)

3. Intel Best Student Paper Award for the paper titled: "Miniaturized High-Performance Filters for 5G Small-Cell Applications" at IEEE ECTC (2018)

4. IEEE EPS Student Travel Award for the paper titled: "3D Glass Package-Integrated, High-Performance Power Dividing Networks for 5G Broadband Antennas" in IEEE ECTC (2019)

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VITA

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