

**HIGH-BANDWIDTH, WIDE LC- R_{ESR} COMPLIANT SIGMA-DELTA
($\Sigma\Delta$) BOOST DC-DC SWITCHING CONVERTERS**

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($\Sigma\Delta$) BOOST DC-DC SWITCHING CONVERTERS**

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[To my family]

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LIST OF SYMBOLS AND ABBREVIATIONS

$\Sigma\Delta$	Sigma-Delta control
V_{IN}	DC-DC converter input voltage
V_O	DC-DC converter output voltage
V_{PH}	Voltage at the switching node in the converter power stage
C_O	Output filter capacitor in a dc-dc converter
L	Filter inductor in a dc-dc converter
R_{ESR}	Equivalent series resistance of the output capacitor
R_{ESRL}	Equivalent series resistance of the filter inductor
I_O	Current demanded by the load on a dc-dc converter
I_L	Current in the filter inductor
f_{sw}	Switching frequency of a dc-dc converter
$f_{0,dB}$	Unity-gain frequency of the control loop gain
PM	Phase margin of a control loop gain
GM	Gain margin of a control loop gain
Z_{RHP}	Right-half plane zero in a control loop gain
Z_{LHP}	Left-half plane zero in a control loop gain

SUMMARY

In low power, battery-operated, portable applications, like cell phones, PDAs, digital cameras, etc., miniaturization at a low cost is a prominent driving factor behind product development and marketing efforts. With that basis, integrated circuit (IC) solutions offer significant relief in system cost, size, and design complexity. This trend is also observed in DC-DC converters, which form a controlling and regulating interface between the off-chip power source (e.g. battery) and the on-chip power consuming circuitry. A critical hurdle in obtaining a fully integrated DC-DC converter solution is the frequency compensation circuit, which has to be designed based on the values of off-chip, passive filter components (LC), and associated parasitic elements, like the capacitor equivalent series resistance (ESR). The values of these external components vary due to manufacturing tolerances, parameter drift, and, more significantly, various design requirements. For example, the selection of the output capacitor type (e.g., electrolytic or ceramic) can change the ESR by orders of magnitude, not to mention its variation with temperature. Such variations in filter parameters correspondingly lead to variations in the loop-gain frequency characteristics of the converter, jeopardizing its transient response and stability. Therefore, to ensure stability of the converter over a wide filter space, the bandwidth (and hence the transient response) of the converter has to be severely limited. On the other hand, to obtain high loop bandwidth concurrently with stability, the choice of LC values must be limited within a narrow design range. To overcome this limitation, it is essential to design a DC-DC converter IC that can yield optimal performance for widely varying passive filter values. This research aims to develop and implement a DC-DC converter IC that will yield stable operation and impart fast transient response for large variations in LC values.

Voltage-mode hysteretic or sigma-delta ($\Sigma\Delta$) control in voltage step-down or buck converters, in regulating the output voltage ripple, indirectly controls inductor current ripple sensed through the capacitor ESR, simplifying the control loop to single-pole characteristics, and giving an inherently stable system without a frequency compensation circuit, thus being suitable for integration. Any changes in LC and ESR values are automatically accommodated via a change in switching frequency. However, in voltage step-up or boost converters, which are widely used in portable electronics for stepping up single or dual-cell battery voltages for 3.3V or 5V applications, the technique is not readily adaptable because the inductor current cannot be completely sensed or controlled simply by regulating output voltage ripple. The following dissertation proposes a circuit and control technique that overcomes this inherent limitation and incorporates voltage-mode $\Sigma\Delta$ control in boost converters using separate voltage and current $\Sigma\Delta$ loops, giving fast transient response and stable operation for orders of magnitude variations in LC parameters.

The proposed technique is developed conceptually and analytical expressions for stability range and transient response are derived. After an initial verification through extensive simulations, the circuit is validated using a discrete PCB prototype board. The proposed system is then fabricated on an IC designed in the 0.5 μ m CMOS process from American Microsystems (AMI) and experimentally evaluated on a power-supply board designed for that purpose. The above work has been accepted for publication in two journals, and published in four conferences and five trade journal articles. In addition, one journal paper has been submitted for publication, and the reviews are pending.

The rest of the dissertation is organized as follows. Chapter 1 introduces high-performance power supplies, followed by Chapter 2 that builds the background by reviewing basic concepts in the operation and control of linear and switching regulators. State-of-the-art techniques in the literature that are compliant to filter LC variations are discussed in Chapter 3. Chapters 4 and 5 present the proposed dual-loop and dual-mode

boost converters along with relevant simulations and discrete prototype experimental results. IC design cycles I and II are described in Chapters 6 and 7 respectively including circuit design, die layout details, and experimental results. Conclusions and a brief summary of the proposed work including key contributions, drawbacks, and envisioned future work are presented in Chapter 8. Involved analytical derivations are limited to Appendices A and B so as not to interrupt the largely conceptual and intuitive flow of the rest of the dissertation.

CHAPTER 1

INTRODUCTION TO HIGH-PERFORMANCE POWER SUPPLIES

The past decade has witnessed a feverish growth in the development of compact, high performance, battery-powered consumer electronic products like cell phones, PDA's, portable audio/video players, etc. This growth, which is fueled by an increasing consumer demand for portability, mobility, as well as a sense of fashion, is largely enabled by advancements in semiconductor fabrication processes. However, the key feature of a mobile device being its battery life, any enhancement in portable electronics has to be supported by and is limited by battery technology. As such, power management and supply circuits, which efficiently manage and transfer battery energy, assume critical importance (the worldwide power management market for consumer electronics that was \$US 9 billion in 2005 is expected to almost double to US \$16.7B by 2010 [1]).

1.1. Power Management System Description

In a typical power management system, e.g., for a portable MP3 player [2], the individual functional circuit-blocks (Fig. 1.1) like the digital signal processor (DSP), audio amplifier, LCD display, etc., generally do not operate at the same input voltage. To accommodate this discrepancy, the input battery power is transferred through dc-dc power converters, which convert the battery voltage to well-regulated voltage levels compatible with the load circuit-blocks. The most important function of the dc-dc converter is to maintain its output voltage constant against variations in battery voltage, load current levels, and other disturbances. As such, each converter typically employs a negative feedback loop that adjusts some internal control parameter (e.g., pulse duty-cycle, frequency, transistor overdrive, etc.) to compensate for any deviations in the output

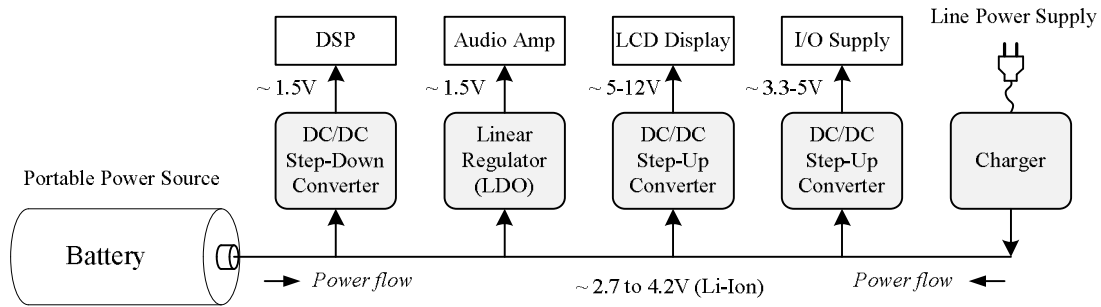


Fig. 1.1. Power management system for a typical portable MP3 player.

voltage from its desired value. (In the case of some dc-dc converters like the battery charger, the output current may be regulated rather than the output voltage.)

The choice of converter topology is based primarily on the required input to output voltage conversion ratio. Due to various factors (described in Chapter 2), mainly simplicity, voltage step-down or buck dc-dc converters have been quite popular in low-cost portable products. However, voltage step-up or boost dc-dc converters are indispensable in applications like high-voltage displays, portable hard-drives etc [3]. In the above example, the high operating voltage (5-12V) of the LCD display has to be generated from a single Lithium-Ion battery (2.7-4.2V). In future ultra-portable systems, high energy-density micro-fuel cells with a low terminal voltage around 0.5V are foreseen to be used to power higher voltage blocks [4], thus requiring step-up converters.

Converter design depends on several load-circuit specifications like power efficiency, dc and transient accuracies, supply noise, cost, etc. These general application-driven requirements of dc-dc converters are discussed in the next section. The discussion is classified into three broad categories – physical, electrical, and design & development driven requirements.

1.2. DC-DC Converter Requirements

In the simplest terms, a dc-dc converter forms an interface block between the input power source, e.g., a battery, which supplies power and the load that consumes the power. As such, not only should the ideal dc-dc converter improve and indeed sometimes

enable the operation of electronic systems, but also be non-intrusive in that process. This seemingly simple requirement translates to an involved set of characteristics, sometimes contradicting each other, as discussed below.

1.2.1. Physical Requirements

Physical restrictions and needs of dc-dc converters come from two concerns, viz., the compactness of the actual system and the need to be able to dissipate heat – thermal considerations. Of these, compactness is easily appreciated for consumer electronics, which are battery powered primarily with the intention of making them mobile. As a result, they also need to be light and wieldy, and in many cases, enough to be operated as handheld devices. Smaller size and a demanding aspect ratio are also preferred for high-end electronics from the aesthetic point of view (e.g. iPhone, Motorola RAZR, etc.). Although the prevalence of solid-state circuits supports this aim (besides giving significant performance improvements), passive electronic components like energy-storage elements – capacitors and inductors, crucial to satisfactory filtering performance, are inherently bulkier and therefore cumbersome [5].

The other hindrance to a compact solution is the size of a heat-dissipating surface. DC-DC converters lose power in the process of input to output voltage conversion and this power loss, if not adequately dissipated to the environment, leads to temperature rise and a hot electronic device. At high temperatures, not only is the system performance deteriorated, but also usability of a handheld device is limited. Furthermore, an attempt to decrease size by reducing passives – inductances and capacitances, is associated with an increase in power loss (Appendix A), thus opposing size reduction. As such, it gets more challenging to increase the *power density*, which is a concern in the face of high functionality (and therefore high power) compact electronics [6].

1.2.2. Electrical Requirements

Electrical requirements or specifications for a dc-dc converter are application driven and therefore numerous in their variegations. This section deals with specifications that are fundamental in nature and are more common in portable applications.

Accuracy

Being used primarily as regulators of dc voltage (or current), dc-dc converter accuracy is important in all applications and critical in most. As such, the converter output voltage (or current) is usually regulated by a negative feedback loop with a high dc gain, to reduce the error in the dc or average value of the output voltage. In applications where the dc output voltage is used either to contain information to be transmitted or where the output voltage controls a system parameter like clock frequency, an inaccuracy in the regulated voltage translates to errors in system operation [7]. Typical accuracy numbers – variations within $\pm 5\%$ of the desired dc value [8] – prove to be stringent for low voltages. For example, at 1V output, the desired variation is within $\pm 50\text{mV}$ across input voltage/load variations. As seen next, net accuracy specifications ($\pm 5\%$) consist of dc as well as transient variations.

The load (e.g. current drawn by a DSP) on a dc-dc converter varies as per system operating conditions. For example, when a suddenly cell phone wakes up from its standby mode where it consumes a small current, to regular operation where the load current can be substantial, the output voltage shows a glitch because the response speed of the converter is finite. This glitch or transient voltage drop should typically be within the 5% variation mentioned above. Clearly, the transient voltage drop is curtailed by decreasing the closed-loop output impedance of the converter at high frequencies. This output impedance reduction is achieved by increasing the controller bandwidth to include higher frequencies in the control loop and/or decreasing the open-loop output impedance by adding a large filtering capacitance at the output. The latter option is common because

control bandwidth is usually limited by stability concerns, as seen later. The resulting high output capacitance increases system size (seen earlier) and/or cost.

A transient voltage rise occurs, in the above example, when the cell phone goes from regular operation to standby mode and this rise is limited by similar techniques. The transient disturbance, instead of being a load change, can also be sudden change in the input voltage with similar effects and remedies. Transients will be analyzed in detail in Chapters 5 and 6. Specific transient requirement distributions are determined by the application. For example, microprocessors, which typically impose sharp load variations, require their voltage regulators to have fast transient response. On the other hand, when powering dynamically biased RF power amplifiers (RFPA), load transients take a lower priority in favor of the need to be able to change the output voltage quickly that necessitates high control bandwidth and lower output capacitance.

While transient disturbances are typically infrequently occurring events, switching dc-dc converters also introduce a regular deviation from the ideal dc output voltage – a ripple in the output voltage. As seen later (Chapter 4) in more detail, this so-called switching ripple, resulting directly from the converter switching activity, is periodic at the converter switching frequency. Clearly, the ripple introduces unwanted high-frequency content (at the switching frequency and its harmonics) into the ideally dc output voltage [9]. The magnitude of this high-frequency content depends on the shape and amplitude of the switching ripple that in turn are determined by the converter topology, input/output dc voltages, load level, and more controllably, the size of passive LC filter parameters. The higher the filter inductance and capacitance, the greater their filtering effect and the lower the output ripple, but the larger their size. In addition, while it may seem that design requirements for lower switching ripple coincide with those for lower transient voltage drop, it should be noted that in certain converters, increasing the filter inductance reduces the output voltage ripple while resulting in higher open-loop output impedance, degrading the transient response [10].

Efficiency

Earlier, power losses in the dc-dc converter were seen to limit the power density of electronic systems (thermal standpoint). In addition, in battery-powered applications, where the energy reservoir (battery) is limited, efficient usage of power is critical to improving battery life, an important measure of mobility. As such, the choice of power-converter architecture is largely determined by the resulting overall system efficiency. As will be seen later, the overwhelming prevalence of switching dc-dc converter topologies over their non-switching, linear counterparts is due to significant efficiency benefits, especially at heavy loads and high voltage-conversion ratios. This popularity withstands the clear disadvantages of switching converters including switching noise, non-dc output voltage, and degraded transient response.

However, switching regulators are not uniformly efficient over their entire load range. While a detailed power loss analysis can be found in Appendix A, it will suffice to say here that switching converters, which consist of large switches that switch on and off at a predetermined frequency – the switching frequency, incur an energy loss for every on-off switching activity because of lossy charging and discharging of parasitic capacitances [11]. Hence the higher the rate of switching activity (higher switching frequency), the higher is the “switching” power loss component. This power loss is the dominant component at low load current levels, where the ohmic (I^2R) component of the power loss is small. In portable devices, which are more prone to spending their time in the (low power) standby or “sleep” modes whenever they are not in active use, the switching losses mentioned above are critical to improving overall battery life. Therefore, generally put, it is preferable to reduce switching frequency from the efficiency point-of-view, especially at high input and output voltages. However, as seen in the previous section, the switching ripple in the regulated output voltage is attenuated by a low-pass LC filter that is more effective at higher switching frequencies. If the switching frequency

is lowered for efficiency, the filter value (and hence its physical size) needs to be increased to proportionately reduce the switching ripple back to its specified value.

The other significant source of power loss, known as the conduction (I^2R) power loss, is caused by parasitic resistances in the current path including the switch on-resistance and equivalent series resistance (ESR) of the filter inductor and capacitor. For all these components, the parasitic resistance is reduced by increasing the cross-sectional area of the current-carrying path, which naturally results in larger component sizes. For example, a wire-wound inductor that consists of a magnetic core with several turns of wire wrapped around it can lower its ESR by using a thicker wire, but at the cost of larger the inductor size. Besides the size factor, an increase in size leads to higher parasitic capacitances at the switching nodes, raising switching power losses.

The final source of power loss discussed here – bias power loss, being dominant at the ultra-low power levels, serves as an indication of the lower limit in the attempt to reduce power waste. DC-DC controller blocks typically use analog control blocks for simplicity, compactness, and importantly, lower cost. The bias currents for these analog circuits lead to a power consumption that increases for high-speed designs. Therefore, sleep modes in portable devices typically involve shutting off all analog circuits except the critical and/or status monitoring “watchdog” circuits [12].

Noise

Noise in electronic systems is gaining significance commercially because of the common application of wireless technologies where the low signal power levels are susceptible to corruption by noise signals of comparable power. Secondly, in situations where multiple systems have a common power source, the noise generated by one system can interfere with the satisfactory operation of another. As such, the noise injected into the supply line has to be within certain limits as determined by specific electromagnetic

interference (EMI) standards that are met by either reducing the generated noise and/or by curtailing the propagation of the generated noise [13].

In switching dc-dc converters, noise is primarily generated at the switching frequency and its harmonics. This noise is then filtered by so-called EMI filters at the converter input, which prevent the noise from being propagated to other systems being powered from the same source. This filter is typically designed around specific target switching frequencies, which therefore have to remain within certain variation limits for the filter to be effective. The frequency invariance preference is primarily responsible for the wide acceptance of converters that switch at a predetermined, constant frequency. In wireless applications, a technique called frequency dithering or frequency spread-spectrum (FSS) is used to continuously vary the frequency, ideally randomly, around the operating “bias” frequency so that the noise power is spread over a frequency band thus reducing the peak noise power levels [14].

Switching speed, i.e., the slew-rate at which the switch transitions from on to off state and vice-versa is considerably higher than the switching frequency. These switching edges generate high-frequency noise that can be controlled by slowing the switching speed as required. However, as seen in Appendix A, slowing the switching speed comes at the cost of increased switching power loss and the related tradeoffs described earlier.

1.2.3. Design and Development Requirements

The design and development of a power supply is typically determined largely by non-technical – logistical and cost concerns and to a small extent by technical issues. For example, the power supply has to adhere to certain quality and reliability specifications that require every part used in the circuit to be appropriately qualified. Use of a new, unqualified component forces a new and potentially lengthy qualification process extending the design time. Similarly, increasing the component count (number of parts used) increases not only the inventory management costs in stocking a wide variety of

qualified parts, but also the assembly cost. As a result, the general rule is to minimize the number of components and to reuse designs and/or components. To that end, integrated circuit (IC) controllers are displacing discrete controllers even if the cost of a controller IC equals the total cost of all components making up the discrete controller. However, even when using IC controllers, sometimes the power switches, and more commonly, the filter LC components are off-chip because of their large size. The system cost then needs to be evaluated carefully depending upon the application requirements. For example, inexpensive electrolytic capacitors exhibit a lower lifetime as against expensive ceramic capacitors that may prove cheaper in the end.

Off-chip filter components also exhibit significant variations that compromise any attempt towards an invariant design. As will be seen in the next chapter, variations in the filter components and their parasitic parameters require redesign in the feedback or frequency compensation circuit to keep the closed-loop converter stable. Such redesign not only increases design time but also increases the inventory and assembly costs mentioned earlier. Filter parameters can also change when addressing new application specifications (e.g., lower output ripple, faster response, etc.) correspondingly requiring a change in the frequency compensation circuit. In many cases, power supplies are designed by non-experts who can be considerably challenged when building a specific system with satisfactory accuracy, stability, transient performance in the face of the above variations. As a result, it is desired to have a user-friendly dc-dc controller IC around which a power-supply can be easily designed against off-chip component variations thus yielding effectively, a wide application space.

1.3. Summary

Heavy demand for handheld, portable electronic devices is driving the supporting technologies, viz., batteries, and battery power-management circuits. Of the latter, dc-dc converters form the power handling core and therefore have to be optimized for various,

often conflicting requirements – compactness, efficiency, steady-state and transient accuracies, and design ease, and the bottom line, cost. Filter LC components, which need to be bulky in order to be effective, play a crucial role in the optimization procedure by not only resisting on-chip integration, but also requiring additional off-chip components – the frequency compensation circuit. As a result, designing an optimized power supply against widely varying specifications is a challenging process that calls for a user-friendly, easy-to-adjust dc-dc controller IC. It is the design of such a “self-optimizing” dc-dc converter that is the focus of the rest of this dissertation.

CHAPTER 2

VOLTAGE REGULATORS

So far, the dissertation briefly looked at market trends that are propelling battery-powered electronics and power management circuits to the forefront. While the application driven requirements of dc-dc converters were qualitatively discussed in the last chapter, this chapter goes into the details of converter operation and their influence on the above requirements. The first section explains the concepts of converter power stages – power handling or current carrying blocks, followed by control concepts in the second.

2.1. DC-DC Converter Operation

As mentioned above, a dc-dc converter transfers power from an input supply (e.g., battery) at a dc voltage V_{IN} , to a load (e.g., DSP) that operates at a different dc voltage V_O . As such, dc-dc converters are essentially dc power amplifiers with the difference in their implementation from equivalent signal amplifiers being low resistances in most circuit paths to reduce power loss. The general circuit consists of a gain/attenuating block, followed by a low-pass filter that ensures a low frequency (close to dc) output.

2.1.1. Step-Down Converter

When the supply voltage V_{IN} is higher than the desired output voltage, a step-down dc-dc converter circuit as depicted in Fig. 2.1 is used. In its simplest form – known as a linear regulator, a variable current source forms the level-shifter that is implemented by a MOS transistor in saturation. The drain current is regulated depending upon the load to maintain the desired output voltage. The capacitor C_O forms a low-pass filter with the output resistance that is a parallel combination of the transistor output and the load resistances.

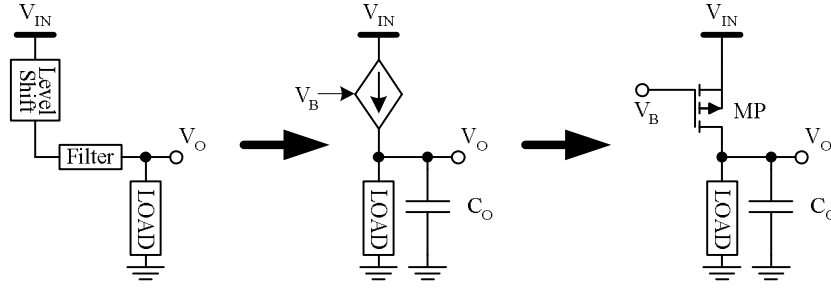


Fig. 2.1. Basic schematic of a voltage step-down dc-dc converter.

Apart from the circuit simplicity, other advantages of the linear regulator are excellent output voltage regulation under load transients – due to high control bandwidth (control speed), and low output noise – due to low output impedance and absence of any continuous switching activity [15]. However, the transistor MP, which supports the input-output voltage difference (known as the dropout voltage) while carrying the full load current, incurs a power loss that becomes increasingly significant as the input-output voltage difference increases. The resulting drop in power efficiency limits the linear regulator to low dropout, low power applications or for powering loads that are sensitive to supply noise.

Switching Step-Down or Buck Converter

The attenuation/level-shift that was obtained using a transistor current-source in the linear regulator can also be obtained by applying the supply voltage to the load on a duty-cycled basis as shown in Fig. 2.3(a) [16]. Since the switches S1 and S2 switch in a complementary, non-overlapping fashion, the voltage v_{PH} at the phase node alternates between V_{IN} and ground, and its average (dc) value, determined by the switching duty cycle, is passed through an LC filter to be applied across the load. The key feature of this strategy is that the circuit elements that simultaneously sustain high voltage and high current are the filter inductor and capacitor, which are reactive (non-dissipative) as against the resistive (dissipative) current source in Fig. 2.1. As such, power losses in a switching converter are greatly reduced giving an ideal efficiency of 100%. Practically,

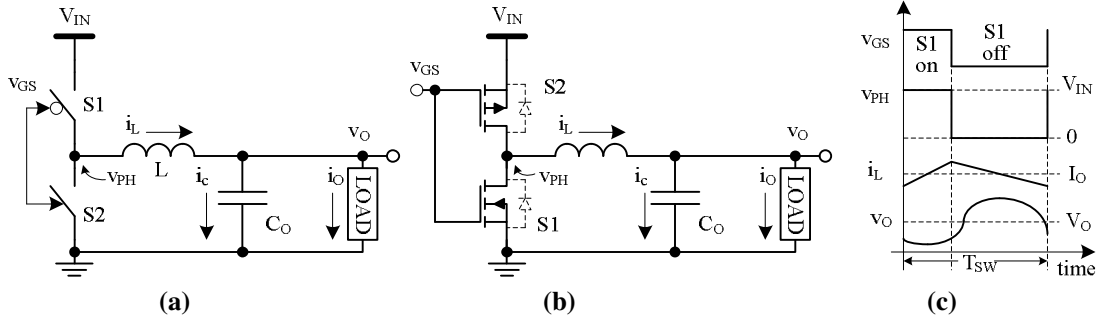


Fig. 2.2. Buck dc-dc switching converter showing (a) simplified schematic, (b) switch implementation, and (c) relevant waveforms.

parasitic resistances and capacitances lead to ohmic and switching losses respectively, reducing the efficiency, typically to around 90%.

Since the inductor is ideally shorted at dc, the average value of the output voltage V_O equals the average value of the phase voltage v_{PH} , given by

$$V_{O(avg)} = V_{PH(avg)} = \frac{1}{T_S} (V_{IN} \cdot t_{on_S1} + 0 \cdot t_{off_S1}) = D \cdot V_{IN}, \quad (2.1)$$

where T_S is the switching period of $S1$ - $S2$ and D is the duty-cycle of switch $S1$. In a closed-loop buck converter, the control normally adjusts the duty-cycle D to regulate the output voltage to the desired value against variations in the input (battery) voltage. The above expression (and the rest of the analysis in this chapter) assumes that the inductor voltage is never zero, i.e., the inductor current is in continuous conduction. In that case, ideally, the switch duty-cycle D is independent of the load current level.

Since the filter capacitor C_O is typically designed to have a time-constant $R_{LOAD}C_O$ much higher than the switching period, the output voltage can be considered approximately constant at its dc value. Thus, the inductor voltage is approximately a square wave swinging between $(V_{IN}-V_O)$ and $(-V_O)$. This voltage square wave is integrated by the inductor into a triangular inductor current ac ripple in addition to a dc current that equals the load current. This inductor current ripple, which can be assumed to flow entirely through the output filter capacitor C_O , leads to a small voltage ripple riding on top of the dc output voltage. The implication of this voltage ripple is additional output

noise that may not be acceptable when supplying applications like high-performance, low-power audio amplifiers. As seen in the last chapter, the output voltage ripple can be reduced by a large output capacitance, sacrificing cost and compactness.

The second main drawback of switching buck converter, and dc-dc converters in general, as seen later, is the bandwidth of the control loop that is limited to a maximum value of a half of the switching frequency, and practically, a fifth of the switching frequency. Moreover, since the switching frequency itself is restricted by switching power losses, the transient response of the buck converter is generally poorer than that of the linear regulator.

2.1.2. Step-Up or Boost Converter

A step-up or boost converter [16], which is used to obtain a dc output voltage higher than the input battery voltage, can be conceptually obtained simply by interchanging the input and output terminals (and switch names S1/S2) in the buck converter from Fig. 2.3, to give the circuit in Fig. 2.3. The evident result of this interchange is that the average inductor current now equals the dc input current, and is higher than the load current since it flows to the output as load current only for that part of the switching period when switch S2 is on. Additionally, the output filter capacitor C_O now carries a discontinuous current that is a square wave between $(-i_O)$ and $(i_L - i_O)$ corresponding to the on and off times of switch S1, respectively. As a result, the capacitor

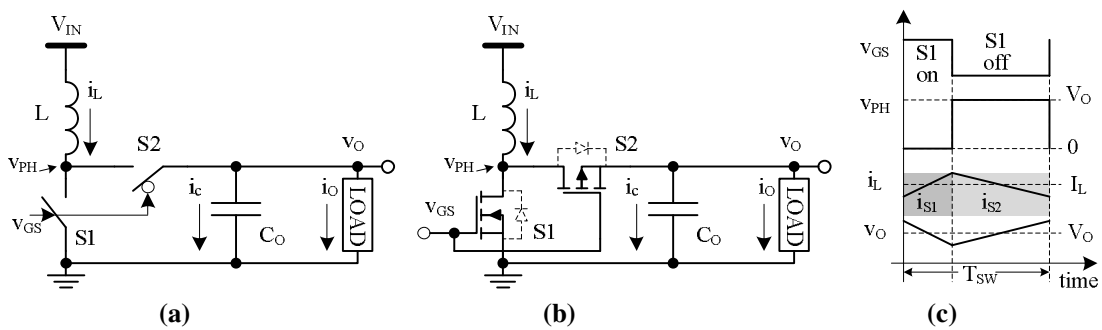


Fig. 2.3. Boost dc-dc switching converter showing (a) simplified schematic, (b) switch implementation, and (c) relevant waveforms.

ripple, which, being an integrated version of the square capacitor current closely resembles a triangle wave, is largely dependent on the average inductor and load currents rather than the inductor current *ripple* as in the buck converter.

The input to output voltage conversion ratio is given by essentially the same expression as equation (2.1), after accounting for the input/output terminal exchange:

$$V_{IN} = V_{PH} \text{ (avg)} = \frac{1}{T_S} (V_O \cdot t_{\text{off}_S1} + 0 \cdot t_{\text{on}_S1}) = (1 - D) \cdot V_O, \quad (2.2)$$

where D is again the duty-cycle of $S1$. Thus, for any given input voltage V_{IN} , the dc output voltage V_O increases with increasing duty-cycle D .

2.1.3. Step-Down/Up or Buck-Boost Converter

Some applications require an output voltage both lower and higher the input battery voltage. For example, the voltage across a Li-ion battery varies from almost 4.2V when it is fully charged, to almost 2.7V when it is discharged enough to require recharging. Therefore, when supplying a load that operates at, say, 3.3V from a Li-ion battery, the interfacing dc-dc converter needs to be able to buck as well as boost the battery voltage and either one of the converters above will not do. On second thought, a series connection of the two converters should be up to the task. Such a series connection can be simplified into a single buck-boost converter using only one inductor (Fig. 2.4).

To operate the buck-boost converter in the “buck” mode, switch $S4$ is permanently switched on (and switch $S3$ is permanently off). The circuit then reduces to the buck converter in Fig. 2.3(a) with switches $S1/S2$ switched on a duty-cycle basis at

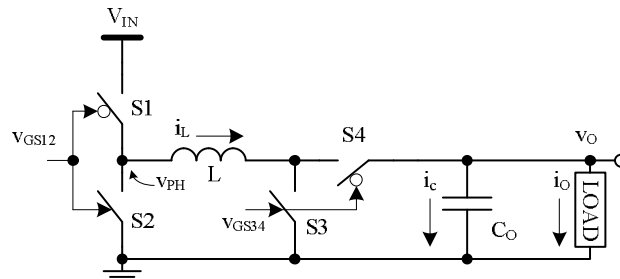


Fig. 2.4. Simplified schematic of a buck-boost dc-dc switching converter.

the switching frequency as before. Similarly, when switch S1 is permanently on and switch S2 is permanently off, the circuit reduces to a boost converter in Fig. 2.3(a). A third operating mode, the buck-boost mode, is commonly used at the boundary of buck and boost mode operations when V_{IN} and V_O are close to each other. In this mode, all four switches switch at the switching frequency with switch pair S1/S3 closed and opened simultaneously followed by the pair S2/S4 switched simultaneously, both for short durations [17]. For the largest portion of a switching cycle, switches S1 and S4 are simultaneously closed essentially connecting the input directly to the output through the inductor. With the switches S1/S3 closed, the inductor voltage (V_{IN}) resembles that during the on time of S1 in a boost converter, and with switches S2/S4 closed, the inductor voltage ($-V_O$) resembles the off-time of S1 in the buck converter. If V_{IN} and V_O equal each other, then the net input-output transfer is a buck-boost series (multiplicative gain) operation giving

$$V_O = \frac{D}{(1-D)} \cdot V_{IN}, \quad (2.3)$$

where D is the duty-cycle of the switch pair S1/S3. This buck-boost converter is sometimes referred to as a “non-inverting” buck-boost converter to differentiate it from its cousin – an “inverting” buck-boost converter whose output dc voltage has a negative polarity with respect to ground.

So far, the basic dc-dc converter topologies most commonly used in portable applications are described. An important derivative of the above converters is what is referred to as the multi-phase dc-dc converter. Multi-phase converters are essentially parallel-connected dc-dc converters with an important aspect – the switching instants of the various parallel converters are shifted away from each other. For example, 2-phase buck converters with common input and output nodes have switching instants shifted 180 degrees apart. The resulting inductor current ripples therefore oppose each other so that the net ripple current flowing into the output capacitor is reduced. At 50% duty-cycle, the

ripple currents in the two inductors completely cancel each other out so that near zero ac current flows in the capacitor virtually eliminating the output voltage ripple. As a result, such converters are commonly used in applications that require ultra-low output ripple.

Other derivatives of these converters, including but not limited to transformer-isolated (dc isolated) structures and multi-level (series) converters that are used in special applications, are not described here; the interested reader can find extensive reading material about them in the literature. Instead, the next section, very briefly explains the concepts of inductor-less dc-dc converters – switched capacitor converters.

2.1.4. Switched-Capacitor DC-DC Converters

In general, all passive components are area-expensive in integrated power converters, and filter inductors are no exception. Furthermore, inductors are most incompatible with standard lithographic processes used in IC fabrication. As such, inductor-less converters are much desired, especially in small, integrated power supplies within otherwise large systems. Such non-magnetic dc-dc conversion is achieved using only capacitors and parasitic resistors [18].

For example, a switched-capacitor voltage doubler (Fig. 2.5) charges capacitor C_T to voltage V_{IN} when switches S2/S3 are turned on in phase 1. In phase 2, switches S2/S3 are turned off and switches S1/S4 turned on so that the charged capacitor C_T is connected in series with the input to give an output voltage V_O that is ideally twice V_{IN} . Actually,

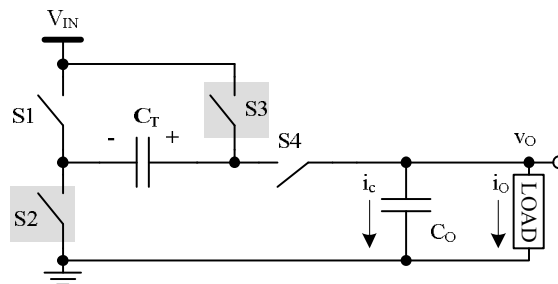


Fig. 2.5. Switched-capacitor dc-dc converter (doubler).

switch parasitic resistances reduce the output voltage in the presence of increasing load current. Hence, the doubler is usually used for output voltages less than twice the input.

Switches S1-S4 are typically run at a high frequency ($>1\text{MHz}$) to keep the capacitance C_T low and therefore integrable. Although quite popular in low current, compact, on-chip applications, switched capacitor converters have a serious drawback. Capacitor C_T is charged and discharged through resistive switches in a lossy manner. Hence, the higher the voltage swing across C_T , the greater is the power lost in charging and discharging it. This power loss ultimately limits the power efficiency of switched capacitor converters making them impractical for high power applications.

2.2. Non-Idealities in DC-DC Converters

2.2.1. Parasitic Resistances and Capacitances

All the converter analyses so far assumed ideal components and operation. In reality, all switches, inductors, and capacitors have equivalent series resistances (ESR) that dissipate power when current passes through them. Similarly, charging and discharging of parasitic capacitances at switching nodes, including gates of MOS transistors, lead to switching power losses. A detailed analysis of converter power losses and efficiency analysis is given in Appendix A.

In addition, dc voltage drops across parasitic series resistances make the ideal equations (2.1), (2.2), and (2.3) invalid. For example, in the switching buck converter, the average voltage at the phase node was assumed equal to the dc output voltage, whereas, the actual value of the dc output voltage is

$$V_O = V_{PH}(\text{avg}) - I_L \cdot \text{ESR}_L, \quad (2.4)$$

where ESR_L is the equivalent series resistance of the inductor L . The result of such parasitic voltage drops is that the actual switch duty-cycle D now depends on the load

current and is somewhat higher than its ideal predicted value in order to maintain the desired output voltage.

2.2.2. Dead Time and Diode Conduction

Considering the buck converter Fig. 2.3(a) during a switching transition, there is an overlap period when both the switches S1 and S2 are simultaneously closed because both switches take finite, non-zero switching times due to parasitic capacitances. During this overlap period, the closed switches form a low resistance connection from V_{IN} to ground leading to a large “shoot-through” current spike twice every switching period. To avoid the associated power loss and potential risk of catastrophic switch damage, the overlap period is prevented by inserting a “deadtime” between the switching instants of S1 and S2, during which, both switches are off. During the deadtime, the inductor current, which cannot be instantaneously reduced to zero, is diverted to the appropriate switch body-diode (or any other parallel-connected diode), depending upon the direction of current flow. The deadtime and the diode voltage drop, which is generally much higher than the voltage drop across the switch, introduce a non-ideality that requires a further increase in the switch duty-cycle to maintain constant output voltage.

Ideally, equations (2.1) through (2.3) suggest that for a given input voltage V_{IN} , a constant duty-cycle D ensures a constant dc output voltage V_O . However, the non-idealities discussed above introduce V_O dependence on such parameters as the switching frequency f_{sw} and the load current i_O . Furthermore, a step change in either the load current or the input voltage causes the output voltage to deviate temporarily from its steady-state value. This “transient response” v_o of the output voltage, which is critical when supplying certain loads like microprocessors, hard-drives, etc., needs to be limited to a quick and small deviation based on the system specifications (typically $\leq \pm 5\%$ of V_O). Therefore, to regulate v_o accurately under dc and transient conditions, one or more feedback loops are employed resulting in a closed-loop dc-dc converter structure. The

next section describes some important and commonly used feedback control techniques in dc-dc converters. However, before that, basic concepts and terminology in control theory are reviewed.

2.3. DC-DC Converters: Control Theory and Techniques

The following section is intended as a refresher in fundamentals of control theory and closed-loop system stability. As before, this consists of a qualitative review to introduce the concepts and terms that will then be used frequently in the next section as well as the rest of the dissertation. For a treatise on control theory, the reader is directed to the literature, some of which is included in the bibliography.

2.3.1. Basics of Control Theory

Linear, time-invariant (LTI) systems that can be described by ordinary differential equations with constant coefficients are commonly analyzed in the frequency domain (as against in the time domain) in terms of the system transfer-functions, which denote input-output relationships in the frequency domain [19]. The mapping from the time domain differential equations to frequency domain algebraic equations in the complex frequency variable s is performed using the Laplace transform. For example, in the frequency domain representation of a voltage amplifier, the input and output voltages are related by the transfer-function $A(s)$ as below

$$V_O(s) = A(s) \cdot V_{IN}(s), \quad (2.5)$$

where $V_O(s)$, $V_{IN}(s)$, and $A(s)$ are the Laplace transforms of the output voltage $v_O(t)$, input voltage $v_{IN}(t)$, and amplifier gain A respectively. The gain A , which in the time domain can be, in general, a proportional-integral-derivative (PID) operator, is represented in the frequency domain as the ratio of two polynomials in s as [19]:

$$A(s) = \frac{b_m s^m + b_{m-1} s^{m-1} + \dots + b_1 s + b_0}{s^n + a_{n-1} s^{n-1} + \dots + a_1 s + a_0} = |A| \angle \Phi, \quad (2.6)$$

where the coefficients $b_m \dots b_0$ and $a_m \dots a_0$ are constants, s is the complex frequency, and the rightmost side represents a polar representation of $A(s)$ with its magnitude and phase. For physical systems, m is less than n indicating that at high frequencies, $|A|$ approaches zero giving zero output voltage. The values of s which lead to the transfer function $A(s)$ becoming zero and infinity, are known as zeroes and poles of the transfer function respectively. These zeroes and poles affect the stability of the system as stated next.

Closed Loop Systems: Classical Stability Analysis

Closed loop systems – systems that use a negative feedback loop – are used to regulate some system parameter against variations in the system transfer function or disturbances such as noise [19]. For example, a negative feedback loop can be employed around the earlier amplifier to give a system as shown in Fig. 2.6. Now the effective closed-loop transfer-function is given by

$$A_{CL}(s) = \frac{A(s)}{1 + A(s)F(s)} = \frac{A(s)}{1 + LG(s)} \approx \frac{1}{F(s)}, \quad (2.7)$$

if $A(s)F(s)$ is much greater than unity, where $F(s)$ is the transfer function of the feedback circuit. Thus, if the product $A(s)F(s)$, known as the open-loop gain $LG(s)$ or simply loop gain, is significantly greater than unity, the closed-loop gain depends only on the feedback gain $F(s)$ that is typically accurately controlled. The greatest requirement from the amplifier, that its gain $A(s)$ should be large in magnitude, is typically true under low frequency conditions. However, the amplifier, which is usually a multi-stage cascaded structure (Fig. 2.7(a)) (for high gain), exhibits a frequency-dependence of gain due to the parasitic capacitors at the output of each stage that short out the voltage across them at high frequencies. In the sense of equation (2.6), the resistor-capacitor parallel combinations constitute poles that lead to a loop-gain frequency response as shown in Fig. 2.7(b).

Each pole contributes a phase lag that gradually increases from approximately a tenth of the pole frequency until it reaches 90° roughly at ten times the pole frequency. Each pole also leads to a gain-magnitude reduction at the rate of 20dB/decade. If the phase of the loop gain is -180° at the unity-gain frequency f_{0dB} , i.e., if $LG(s)$ is -1 , the denominator of equation (2.7) is zero, so that the closed-loop gain tends to infinity. The Nyquist Stability Criterion (based on Cauchy's Principle of the Argument in Complex Analysis) shows that the above condition indicates the onset of instability beyond which the amplifier output will grow monotonically in amplitude, ideally unbounded, but practically to a saturation limit outside the normal operating range of the amplifier. Qualitatively, the 180° phase lag of the loop gain suggests that the signal fed back through $F(s)$ (Fig. 2.6), instead of being subtracted (negative feedback) from the input $V_{IN}(s)$, has actually inverted in phase and is therefore being inadvertently added (positive or regenerative feedback) to $V_{IN}(s)$ causing the instability. Naturally, at the frequency f_{0dB} , the lesser the phase-lag Φ is than 180° , the greater the margin the system has to avoid instability. This margin – the difference between 180° and the actual phase lag Φ –

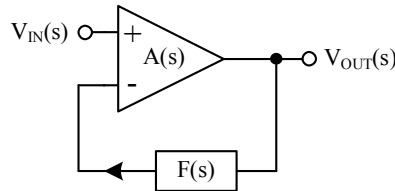


Fig. 2.6. Closed-loop amplifier with feedback $F(s)$.

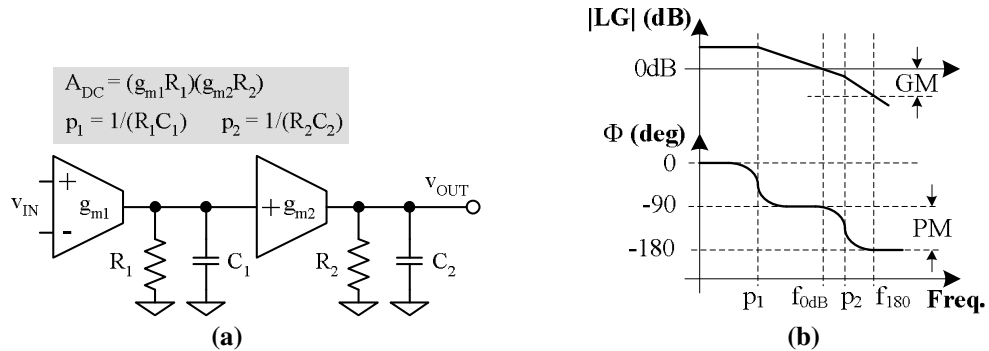


Fig. 2.7. (a) Simplified schematic of a two-stage amplifier and (b) relevant Bode plots.

is known as the phase margin (PM). Similarly, when the phase Φ does reach 180° at frequency f_{180} , the difference between 0dB (unity gain) and the actual gain magnitude is known as the gain margin (GM). Both phase and gain margins need to be large enough for good “relative stability.”

Frequency (or Feedback) Compensation

It is assumed in Fig. 2.7 that the feedback circuit-gain $F(s)$ is independent of frequency and the only poles in the loop gain come from the amplifier $A(s)$. In actuality, poles and zeroes are deliberately inserted in the transfer function $F(s)$, which, in conjunction with the poles and zeroes of $A(s)$, shape the loop gain frequency-response to give good phase and gain margins, among other reasons. For example, a zero in $F(s)$ located at the same frequency as pole p_2 cancels out the effects of p_2 on both the magnitude and phase such that the resulting transfer function $LG(s)$ now only has 1 pole (p_1) and therefore a phase margin of 90° . This process of reshaping the loop gain frequency-response to achieve the desired control characteristics is known as frequency or feedback compensation. Despite the simplicity of the above example, it brings forth the point that will be repeated throughout the rest of this thesis – that optimal frequency compensation depends on the locations of poles and zeroes of the system being compensated (in this case, the amplifier). Therefore, accurate knowledge of the roots (in this case, p_2) of the system transfer function is critical. Any variations in the system transfer function, degrade the effects of frequency compensation, and in the worst case, can destabilize the closed-loop system.

2.3.2. DC-DC Converter Control Techniques

Since dc-dc converters operate in a discrete, switched manner, their models are averaged (to remove switching discontinuities) and linearized (neglecting any 2^{nd} order or higher terms) before applying control theory developed for LTI systems [20]. The

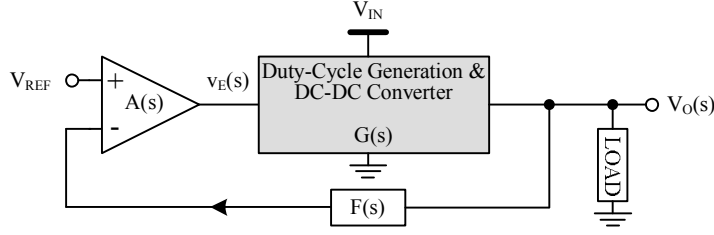


Fig. 2.8. General representation of a closed-loop dc-dc converter.

averaging is performed over one switching period thus neglecting any switching ripples in the inductor current and output capacitor voltage. As such, the models thus developed are valid for analysis only up to frequencies lower than half the switching frequency. Some control techniques (seen next) that are based on the switching ripple itself cannot be completely analyzed using such averaged models. Linearization of models is based on the small-signal assumption, thus limiting model validity to small-signal perturbations only.

As mentioned earlier, most dc-dc converters regulate the output voltage; hence, the feedback circuit senses the output voltage and compares it to an accurate reference voltage V_{REF} to generate an error voltage v_E that is ultimately used to determine the switch duty-cycle. This feedback constitutes what is known as the “voltage feedback loop” or simply, voltage loop, and will be the common feature in all the control techniques studied next. As such, the closed-loop dc-dc converter can be related to Figs. 2.3 through 2.7 as shown in Fig. 2.8. The general closed-loop expression is therefore given by

$$V_O(s) = V_{REF} \cdot G_{CL}(s) = V_{REF} \left(\frac{A(s)G(s)}{1 + A(s)G(s)F(s)} \right) = V_{REF} \left(\frac{A(s)G(s)}{1 + LG(s)} \right) \approx \frac{V_{REF}}{F(s)}, \quad (2.8)$$

if the loop gain $A(s)G(s)F(s)$ is much greater than unity, where $G(s)$ is the gain of the shaded block, and $G_{CL}(s)$ is the system’s closed-loop gain. The factors that differentiate various control techniques are the process (known as modulation) of generating the duty-cycle, the bandwidth of the feedback circuit $F(s)$, and the use of additional sensed variables/feedback loops within the shaded block of Fig. 2.8.

Voltage Mode PWM Control

Arguably the most common of techniques discussed here, the name voltage mode control is used to indicate a pulse-width modulated (PWM) scheme where the error voltage v_E information, by comparison with, commonly, a sawtooth (or less commonly, triangular) signal, is modulated into the duty-cycle of a square-wave pulse (Fig. 2.9) [20]. This duty-cycle ultimately determines the output voltage V_O , as explained earlier and given by equations (2.1) through (2.3). The switching frequency, set by the frequency of the modulating sawtooth signal, is by default constant, which is an advantage in some applications from the point of view of filtering out the switching noise. The basic idea behind modulation is to sample the low frequency components of the error voltage-signal v_E at a sampling rate equal to the switching frequency. As such, the feedback circuit $F(s)$ and/or the amplifier $A(s)$ contains a pole that serves to virtually eliminate any components in $v_E(s)$ beyond approximately a fifth of the switching frequency. This pole places an upper limit on the bandwidth of the control loop.

Besides the above pole, the frequency compensation may contain one zero to compensate partially for the effects of the double-pole introduced by the LC filter in any dc-dc converter. However, when using electrolytic output capacitors, their typically high equivalent series resistance (ESR) naturally gives a zero in the dc-dc converter transfer function itself, eliminating the requirement for any special zero in the feedback compensation network. In addition to the aforementioned poles and zeroes, in order to improve dc accuracy, a pole is added at the origin giving very high dc gain, followed by a

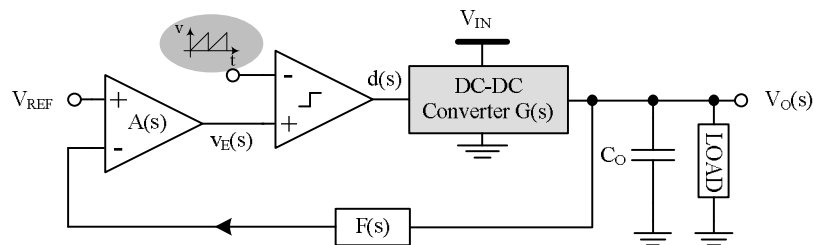


Fig. 2.9. General representation of a voltage-mode PWM dc-dc converter.

zero within 2-3 decades to cancel the phase lag effects of the pole and curb the gain drop-off. This pole-zero pair limits the low-frequency performance – settling time, of the output voltage, following a transient event.

Voltage-mode control is popular for its simplicity – a single feedback loop and easy sensing of the regulated voltage. In buck converters, voltage-mode control also permits a high-bandwidth control loop. As a result, despite the development of exotic control strategies, voltage-mode control is still common in general-purpose applications.

The main drawback of a voltage-mode controlled converter is that while the dc-dc converter is a second order system, i.e., essentially, it has two poles, only one contributor to those poles (capacitor voltage) is sensed, while the other contributor – the inductor current, is indirectly sensed through the capacitor voltage. This “incomplete” sensing poses a problem in the boost converter, where the inductor current, being disconnected from the output when switch S1 (Fig. 2.3) is open, is not completely observed in terms of the output voltage, potentially leading to instability. In addition, power supply (V_{IN}) rejection or audio-susceptibility, as it is known in the context of switching converters, which, in voltage-mode control is ensured through a slow-feedback loop, may not satisfy some application requirements. All these issues are addressed when the inductor current is regulated in addition to the capacitor voltage.

Current Mode Control

In current-mode control, the inductor current is regulated in a separate control

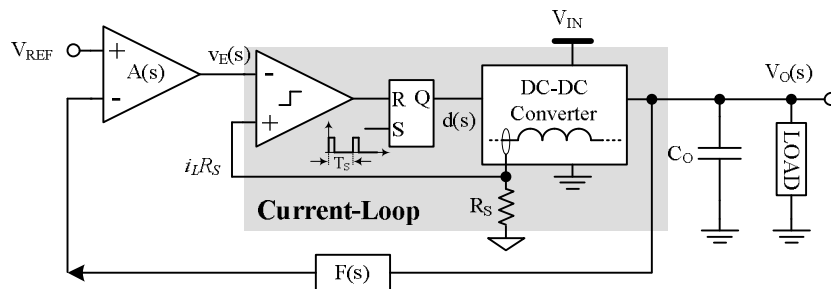


Fig. 2.10. Simplified schematic of a peak current-mode controlled dc-dc converter.

loop that operates at a higher bandwidth than the voltage loop [20]. As a result, the inductor and its control loop look like a voltage-controlled-current-source for all frequencies of interest to the voltage loop. In other words, the inductor current variation (and hence the associated pole) is suppressed for all frequencies within the bandwidth of the voltage loop. Thus, only the one pole associated with the output capacitor remains in the closed-loop system simplifying the compensation requirements. Besides this improvement, the inductor current source virtually isolates the output voltage from small-signal changes in the input voltage v_{IN} . The voltage error signal is used to set the reference for the voltage-controlled inductor current-source. Beyond the unity-gain frequency of the current loop, the inductor ceases to be a current source leading to the appearance of the inductor pole; however, this pole is much beyond the bandwidth of the main voltage loop leaving the net phase or gain margins largely unaffected.

With that basic ideology, the inductor current can be controlled either by regulating its peak, valley, or average current levels. In peak or valley current-mode control, the inductor ripple is usually designed small so that the peak/valley current levels are approximately equal to the average value. A simplified schematic of a peak current-mode controlled dc-dc converter is shown in Fig. 2.10. In this case, the switch S1 (Figs. 2.3, 2.4, 2.6) is turned on periodically at fixed instants determined by a clock, while it turns off when the peak inductor current reaches its reference current level, determined

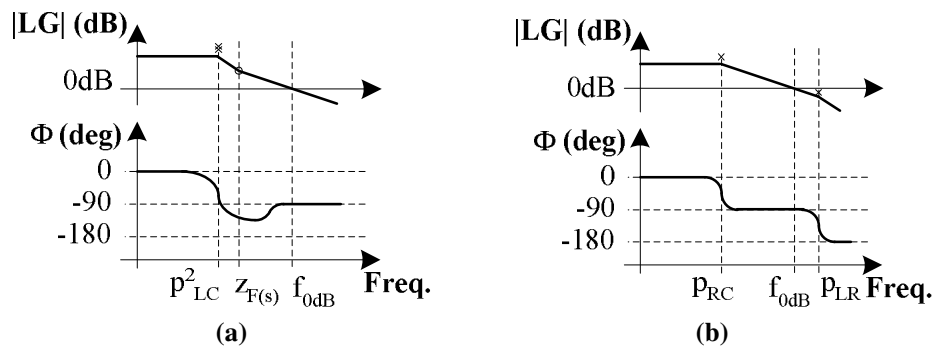


Fig. 2.11. Frequency responses of basic (a) voltage and (b) current-mode control strategies.

by the voltage error signal $v_E(s)$.

A comparison of basic loop-gain frequency responses for voltage and current-mode control strategies is shown in Figs. 2.11. While the compensation zero $z_{F(s)}$ tries to offset the effect of one of the poles of the LC filter in voltage-mode control, the inductor pole itself is pushed out to higher frequencies in current-mode control. As such, the compensation requirements in current-mode controlled strategies are greatly simplified.

Hysteretic Control

In both the control strategies above, the switching frequency is constant and, in fact, is an unwanted factor of the control loop so long as it is high enough to keep current and voltage ripples low. Admittedly, the peak current-mode control strategy tries to maximize the effect of the switching frequency by regulating the peak of the inductor current switching ripple; however, the voltage loop still treats the sensed voltage as a low-frequency variable that is sampled at the switching frequency. Hysteretic control refers to a modulation strategy where the natural frequency of the regulated signal itself is used as the sampling frequency thus allowing the maximum loop bandwidth equal to the switching frequency.

A hysteretic buck converter (Fig. 2.12) consists of a hysteretic comparator CP_V that senses the output voltage ripple and regulates it to within its hysteresis window by controlling the switching frequency and duty-cycle of switch S1 [21]. In terms of the frequency response, the hysteretic comparator (modulator) forces the loop-gain to have a zero phase-margin, thus resembling an oscillator. Unlike regular oscillators though, the amplitude of these oscillations is limited very close to the width of the hysteretic window of the comparator. In a sense, by allowing the sensed output voltage to have a switching ripple, the hysteretic comparator introduces a time delay, which translates to a phase delay as

$$\Phi_{\text{delay}} = t_{\text{delay}} \cdot 2\pi \cdot f , \quad (2.9)$$

at a frequency f . The comparator essentially adjusts the switching frequency so that this phase delay at the switching frequency makes up for the balance between 180° and the phase delay contribution of the converter power stage.

From another point of view, hysteretic control can be visualized as a scheme where the capacitor voltage and inductor current are simultaneously controlled as in current-mode control, as follows. The inductor current ripple, in flowing through the output capacitor, drops an in-phase ripple voltage v_{esr} across the capacitor ESR in addition to the 90-degrees out-of-phase capacitive ripple v_c (Fig. 2.12). Since the capacitor ESR in these converters is large, the ESR voltage v_{esr} usually dominates v_c around the switching frequency (i.e. $v_o \approx v_{\text{esr}}$). As a result, the loop, in regulating the output voltage, in essence regulates the sensed inductor current ripple v_{esr} at and around the switching frequency, and the capacitance voltage v_c at low frequencies. This situation thus resembles a high-frequency current-loop within a low frequency voltage loop as in current-mode control. As seen in the last subsection, such current-mode control eases frequency compensation requirements. Consequently, the hysteretic converter has a wide stable operating range and a fast transient response, almost irrespective of the filter LC values and without using any frequency compensation circuit. Any change in the filter values is accommodated by a change in the switching frequency (loop bandwidth) so that maximum loop bandwidth is always achieved.

The main drawbacks of hysteretic control are the variations in its switching frequency with input voltage/load current variations and its sensitivity to noise. The

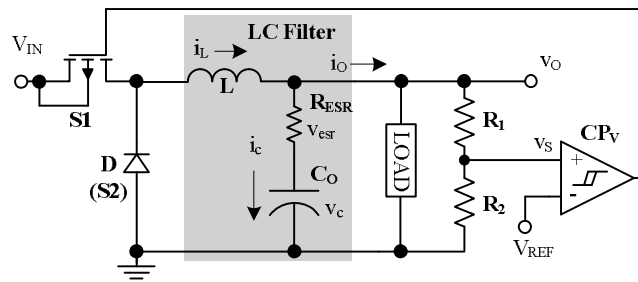


Fig. 2.12. Simplified circuit schematic of a hysteretic buck converter with a high-ESR output capacitor

former challenges the design of a suitable EMI filter in line-powered applications while the latter becomes an issue in low voltage applications where the small comparator hysteresis window along with the high-bandwidth feedback loop can jeopardize periodic switching in the converter. Nevertheless, simplicity of operation and the ability to yield almost a universally stable dc-dc converter with fast transient response without using a frequency compensation circuit are greatly attractive features that have made hysteretic buck converters well accepted in compact, high-performance applications.

Hysteretic control along with its advantages cannot be similarly employed in boost converters. Based on the current-mode control explanation, it is easy to see why. In boost converters (Fig. 2.3), the inductor current does not flow to the output when switch S1 is turned on. As a result, inductor current information cannot be completely obtained simply by sensing the output voltage as in buck converters and in the absence of current-mode-like characteristics, hysteretic control based on output voltage cannot be implemented. As such, the obtaining a universally stable boost converter that also gives fast transient response against design and manufacturing variations in filter values is strongly desired.

2.4. Research Objective

As seen earlier, optimal frequency compensation in switching dc-dc converters requires knowledge of system poles and zeroes that are introduced by the filter inductor and capacitor values. Since these filter parameters are bulky in size, typically, they cannot be mounted on-chip. Once off-chip, these filter elements are beyond the control of the controller IC designer and therefore subject to variations due to design requirements, component tolerances, etc. In order to stabilize the system against such filter variations, the frequency compensation circuit has to be variable and therefore necessarily has to be mounted off-chip as well, increasing the component count, not only on the board, but also in the inventory. Besides, designing the frequency compensation circuit for variable filter

situations increases design complexity and increases design time ultimately leading to higher cost. If the frequency compensation circuit is integrated on-chip in an attempt to reduce design time and cost, the range of filter values and hence the application space of the controller IC is starkly limited.

All these problems are largely addressed in buck hysteretic converters that, in emulating current-mode control, give a universally stable converter with fast transient response without using a frequency compensation circuit. However, in boost converters, popular in stepping up battery voltages for 3.3V, 5V, 12V, etc applications, hysteretic control cannot be similarly implemented. The objective of this research is therefore to investigate, design, and develop a boost dc-dc converter both widely stable against filter LC variations and fast against line and load transients.

2.5. Summary

This section discussed qualitative details of magnetic switching dc-dc converters concentrating on the three main converters – buck, boost, and buck-boost. Non-magnetic topologies – linear regulators and switched capacitor converters, were also discussed with their benefits and drawbacks. Following an introduction to control theory, popular control techniques in dc-dc converters including voltage- and current-mode controls were described. Hysteretic control in buck converters was seen to be a variation of current-mode control, yielding almost a universally stable and fast converter against filter variations.

CHAPTER 3

LC COMPLIANCE IN POWER SUPPLIES

Variations in the bulky, off-chip filter components jeopardize the stabilizing effects of the frequency compensation circuit, as concluded in the last chapter. Several techniques from the literature aimed at adapting to or compensating the filter LC variations are summarized in this chapter. While some techniques focus on specific converter topologies, most of them present control techniques for switching dc-dc converters in general. The following description begins with techniques that address specific filter-related issues – the ESR zero and the RHP zero in boost converters, and goes on to describe techniques that try to minimize the effects of overall filter variations.

3.1. LHP Zero Via Feedforward Path

The influence of the capacitor ESR zero, although stabilizing in the presence of an LC double-pole, is unpredictable due to the wide variations in ESR value depending on capacitor type and value. For example, the ESR of an aluminum electrolytic capacitor is typically orders of magnitude higher than that of a ceramic capacitor. The following technique introduces a more reliably positioned zero, thus minimizing or eliminating the influence of ESR on converter performance.

An additional feedforward (FF) path is added from the input of the L-C filter (node v_{PH} in Fig. 2.2) to the negative input of the error amplifier as shown in the Fig. 3.1(a) [22], [23]. The feedforward path is designed to have a single pole roll-off before the loop-gain crossover frequency (f_{0dB}), as against the double pole roll-off in the path of the LC filter, as shown in Fig. 3.1(b). The net loop gain LG is determined by the main path gain ($G_P Y_1$) before the zero frequency z_{FF} and by the feedforward path gain (A_{FF})

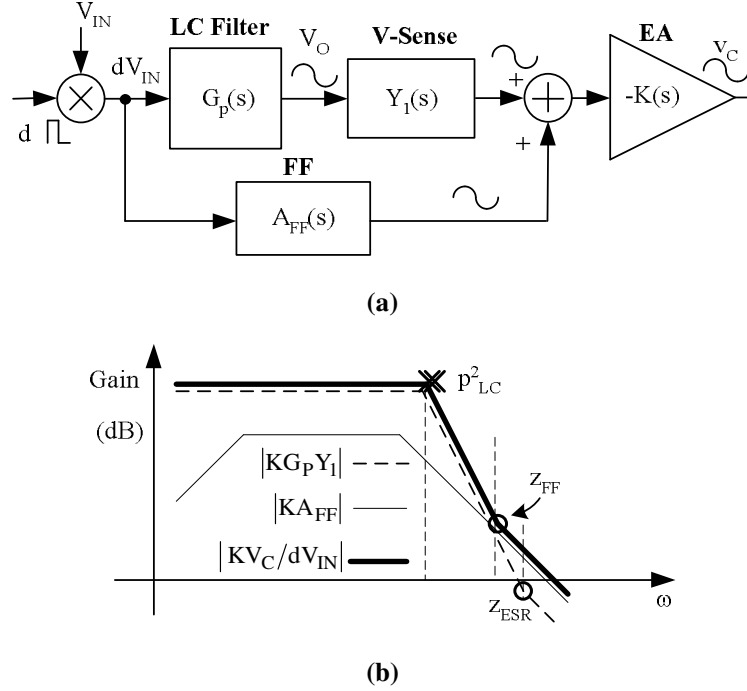


Fig. 3.1 (a) Block representation of the feedforward scheme to eliminate the ESR zero from the net loop-gain and (b) Bode magnitude plot.

beyond z_{FF} . Clearly, by locating z_{FF} sufficiently low always to precede the ESR zero z_{ESR} , the latter never affects the loop-gain. Thus, the zero z_{FF} introduced by the feedforward path ensures a crossover frequency and phase margin independent of z_{ESR} . The results in [22] show that a reduction in the ESR value from 40m Ω to 20m Ω is associated with a minor reduction in the crossover frequency from 21 kHz to 19.7 kHz and an increase in the phase margin from 62° to 70°. However, while the control to output gain is stabilized using the feedforward network, the converter output impedance at high frequencies is worsened since shunt feedback is inactive beyond the frequency z_{FF} .

3.1.1. Elegant Circuit Embodiment of Feedforward Control

In the hysteretic controller, seen in Chapter 2, the system response and stability are essentially independent of load parameters as any change in them only leads to a change in the switching frequency. The limitation in this technique comes from the

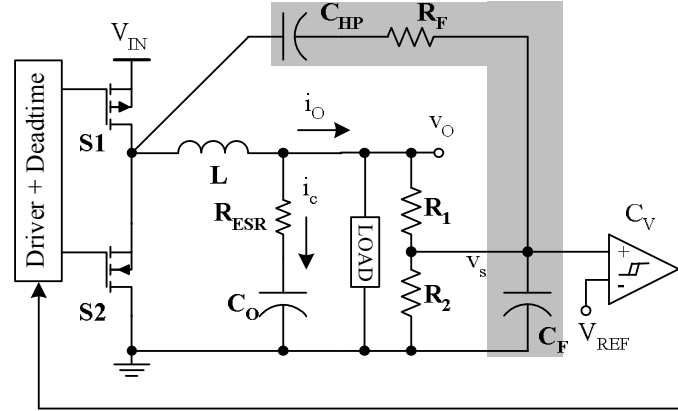


Fig. 3.2. Schematic representation of the feedforward scheme in hysteretic buck converters to eliminate dependence on the capacitor ESR.

variation in the switching frequency with capacitor ESR (R_{ESR}). A modified hysteretic control scheme to tackle this issue is shown in Fig. 3.2.

An integral of the waveform at the input of the LC filter is a triangular signal, the average value of which is approximately equal to the DC output voltage (V_O) [24], [25]. This triangular signal, which resembles an artificial ripple voltage independent of the output capacitor ESR, is added to the sensed output voltage at the comparator non-inverting input. The combination R_F - C_F is designed to give a magnitude of the artificial ripple larger than the actual output ripple. In that case, triggering of comparator C_V and the consequent switching of switch S1 is determined by the additional signal, increasing the switching frequency and making it independent of the output voltage ripple and hence the ESR of capacitor C_O . The high-pass capacitor C_{HP} prevents dc voltage at the filter input from being fed forward thus making the main feedback path dominant at low frequencies [26].

The increased switching frequency enables usage of smaller, low-ESR, and surface-mount ceramic capacitors at the converter output, giving considerable savings in

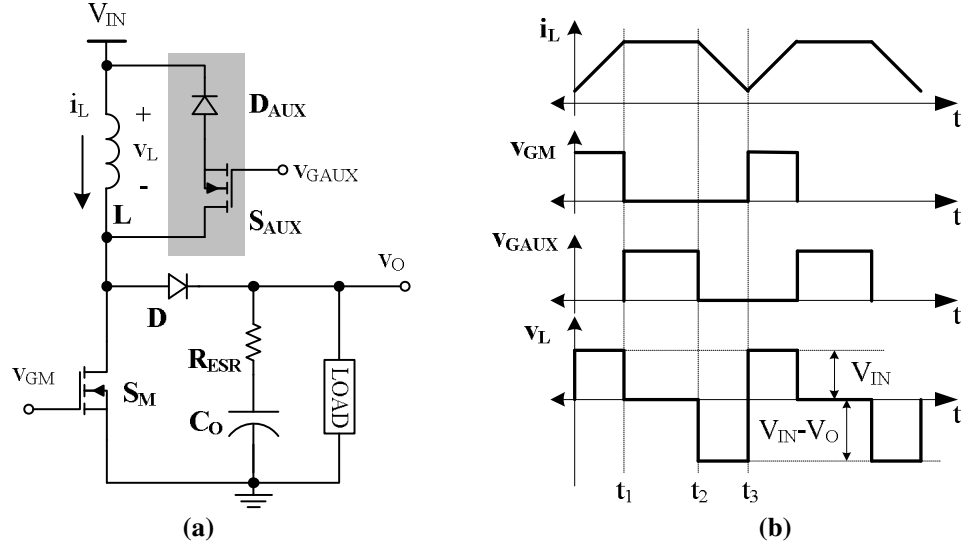


Fig. 3.3. (a) Schematic representation of the constant capacitor-discharge scheme to eliminate the RHP zero in boost converters and (b) relevant waveforms.

the system size, cost, and reliability. However, operation at higher switching frequencies brings about increased switching power losses and slightly reduced efficiency.

3.2. RHP Zero Removal in Boost/Buck-Boost Converters

The schematic in Fig. 3.3(a), neglecting the shaded part, shows a standard boost converter circuit. As an immediate reaction to increasing the duty cycle of switch S_M , the capacitor C_O discharges for a longer time, causing the output voltage V_O to drop initially, before rising to its steady-state value. This initial voltage drop, which illustrates the presence of a right-half plane (RHP) zero in the control loop, tends to de-stabilize the system. The following section discusses two techniques that may be followed to reduce the effect of or eliminate the RHP zero.

3.2.1. Constant Capacitor Discharge-Time Control

The RHP zero is eliminated by keeping the total capacitor discharging time constant [27]. As shown in Figs. 3.3(a) and (b), when the auxiliary switch S_{AUX} is turned

on for a portion of the off time of the main switch S_M , the inductor current freewheels, letting the capacitor C_O discharge through the load. Thus, an additional discharging time is introduced. Since the interval (t_1 to t_2) is only a freewheeling period, the inductor voltage is assumed to be zero and there is no contribution from the input to the output. The output voltage in continuous conduction is then given by

$$V_O = V_{IN} \frac{t_1 + (t_3 - t_2)}{(t_3 - t_2)}. \quad (3.1)$$

As seen from equation (3.1), in the absence of the auxiliary switch i.e. when t_1 equals t_2 , the output voltage follows the standard boost converter relationship in continuous conduction mode [28].

The total capacitor discharge time, which is the sum of on times of switches S_M and S_{AUX} , is kept constant by modulating the on time of switch S_{AUX} to match changes in the on-time (duty cycle) of switch S_M . Thus increasing duty cycle of switch S_M does not cause the capacitor C to discharge more, eliminating the RHP zero. However, the extra freewheeling period leads to a higher average inductor current, causing an increase in switching and conduction losses, which is a drawback of this technique.

3.2.2. Peak Output Voltage Control

The output voltage of a boost DC-DC converter, including the effect of output capacitor ESR, is shown in Fig. 3.4(b). Since the current flowing in the output capacitor is discontinuous due to the switching of diode D_M , the ripple voltage across the capacitor ESR exhibits sharp edges (a replica of the capacitor current). If the capacitor ESR is sufficiently high, then the peak output voltage (point E) does not exhibit RHP zero, as does the trough (point D). It is seen therefore that the point E does not exhibit the same

behavior as point D and rises uniformly. This response can be attributed to the output capacitor ESR and it can be further shown that such uniform rise in the point E occurs if the following condition is satisfied [29]

$$R_{\text{ESR}} C_O > \frac{L}{R_O (1 - D_M)} . \quad (3.2)$$

where C_O is the value of the output capacitance, R_{ESR} is the output capacitor ESR, R_O is the load resistance, L is the boost inductor, and D_M is the operating duty cycle of S_M .

Control issues arise when the average output voltage, which exhibits a RHP zero, is used in the negative feedback. However, if the peak output voltage (corresponding to point E) is fed back then based on the previous discussion the RHP zero is not encountered. In order to use the peak output voltage for negative feedback control, the instant at which the off-time of the switch ends, must be variable. In other words, the instant at which the switch turns on should depend on the value of the voltage fed back (point E). In normal systems, the type of modulation used is trailing edge modulation where the switch turn-off instant is regulated while the switch turn-on always occurs at the clock edge. Hence, the peak voltage feedback fails with trailing edge modulation. If however, leading edge modulation is employed where the switch turns on at variable instants and always turns off at the clock edge, then peak-output voltage feedback as described above, can be used. In addition, the feedback compensation must be designed so as not to average out the output voltage ripple.

In order for this technique to be effective, the capacitor ESR voltage must override the capacitive voltage thus forcing the output voltage to follow the average capacitor current rather than the capacitive voltage, during a transient. This requirement forces the capacitor ESR to be exorbitantly high resulting in a large output ripple that

resembles a square wave. Additionally, in order to feed back instantaneous output voltage, the feedback loop must have high bandwidth, making the system more susceptible to noise.

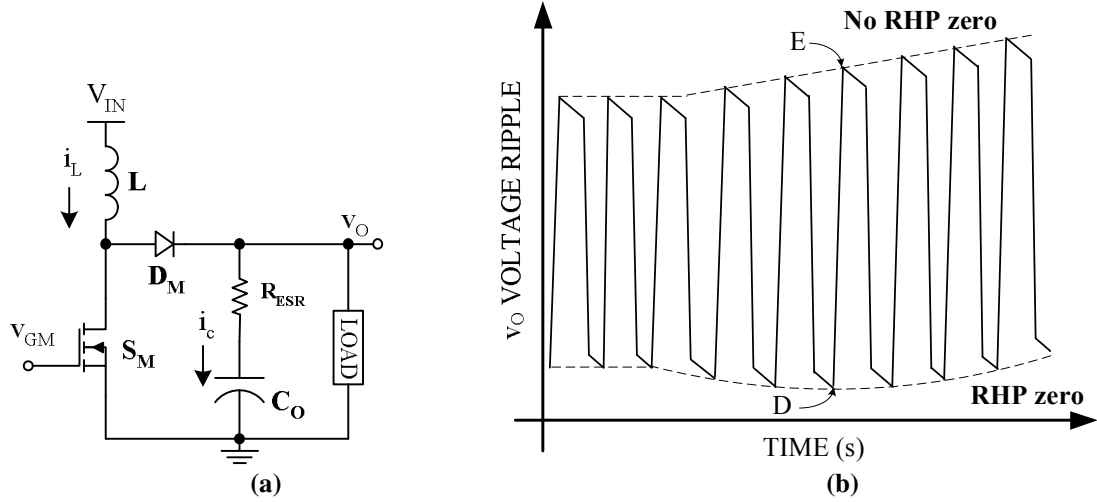


Fig. 3.4. (a) Schematic representation of the peak output-voltage control scheme to eliminate the RHP zero in boost converters and (b) output voltage ripple waveforms during transients.

3.3. Compensating L-C Filter Variations

3.3.1. Constant L-C-R Load Control

The basic objective of the following technique is to make the effective error amplifier see a constant set of filter values. The auxiliary controller has essentially the inverse transfer function of the converter based on a nominal set of load and passive component values [30]-[32]. As such, the error amplifier can be designed for predetermined, nominal LC values. From Fig. 3.5, the control signal to the converter power stage is generated by adding a separate weighted error signal to the error amplifier output, since it is based on preset nominal values of LCR filter elements. Any variation of the actual LCR values from the preset ones is accommodated only by modulating the weighted error signal such that error amplifier output is invariant to LCR variations. The

error signal is obtained as the difference between the actual converter control signal and the control signal that would be required if the LCR values equaled the preset ones.

The transfer function seen by the error amplifier looking into the white area can be shown to be as follows,

$$V_{OU}(s, W) = \frac{V_{OC}(s)}{1 - W + (W)[V_{OC}(s)][G_{AUX}(s)]}. \quad (3.3)$$

As can be seen, as the weighting factor W approaches 1, $V_{OU}(s, W)$ becomes independent of $V_{OC}(s)$. When W equals 1,

$$V_{OU}(s, W) = \frac{1}{G_{AUX}(s)}. \quad (3.4)$$

The overall loop gain is given by

$$T_V(s, W) = [V_{OU}(s, W)][G_{VS}(s)] \cdot b. \quad (3.5)$$

Clearly, the effects of variation of the converter filter elements can be masked by using an additional control block.

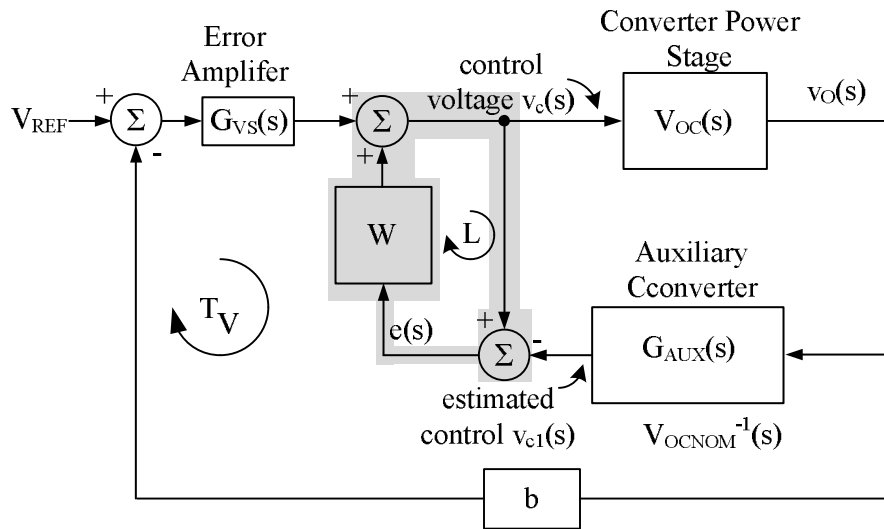


Fig. 3.5. Block representation of the constant-L-C-R control technique to compensate for filter variations.

From the schematic in Fig. 3.5, it can be seen that a value of 1 is not possible for W as it would lead to instability in the positive feedback loop formed at the summation junction of the outputs of $G_{VS}(s)$ and W . Hence complete elimination of $V_{OC}(s)$ is not possible from the expression of $V_{OU}(s, W)$. The other design concern is that $G_{AUX}(s)$ essentially acts as a high pass filter and tends to amplify switching ripple from the output. An additional pole has to be added to limit high frequency gain. Finally, in boost and buck-boost derived converters, the presence of a right-half plane zero gives rise to design difficulties.

3.3.2. Multiple Operating Point Control

As seen in the last chapter, DC-DC converter control theory is typically based on the small-signal linearization around the operating point. This means that the designed control loop is valid and functions appropriately only when perturbations in any parameter are small in magnitude as compared to its steady-state value. For large-signal variations, the analysis proves inaccurate. Grid point or multiple-operating point control tackles the issue by partitioning the total operation space into different regions, each characterized by a single operating point called grid point [33], [34]. Each grid point and its respective control equations are designed independently to yield optimal performance. In essence, the controller adapts in a discrete manner with the space around each grid point determining the step transition from one operating region to another. The obvious disadvantage of this technique is that system performance and stability during changeover between grid spaces is compromised.

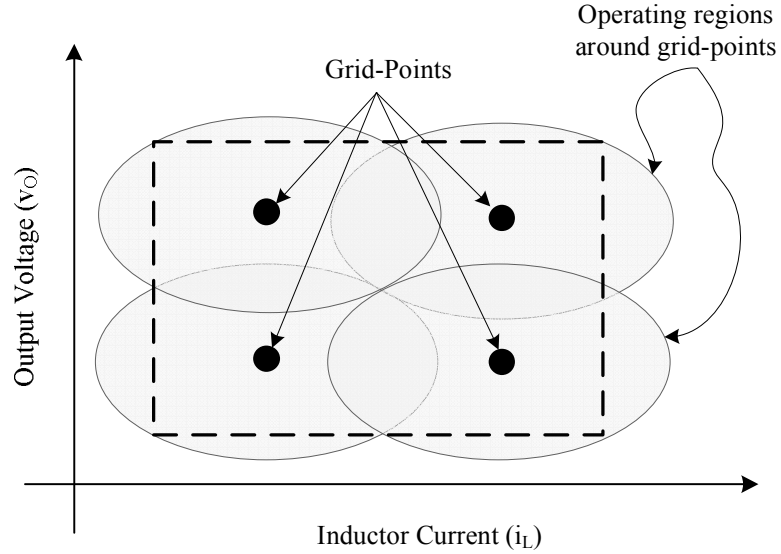


Fig. 3.6. Graphical representation of the grid-point scheme.

3.3.3. Digital Control

Digital control, as against the traditional analog control, employs a digital signal processor (DSP) to perform the control loop calculations that ultimately determine the duty-cycle of the switch pulses to the converter power stage. As such, the frequency compensation circuit is not made up of actual components, but rather coded into the DSP. As such, theoretically, it is relatively easy to adapt the compensation network in response to changes in filter LC parameters [35]. However, this adaptive or programmable control and system-level power management capabilities, takes multiple clock cycles to process information thereby limiting its ability to respond quickly. Hence, despite its advantages in terms of versatility, transient response is poor [36]-[38] as compared to typical averaged analog control techniques and hysteretic control.

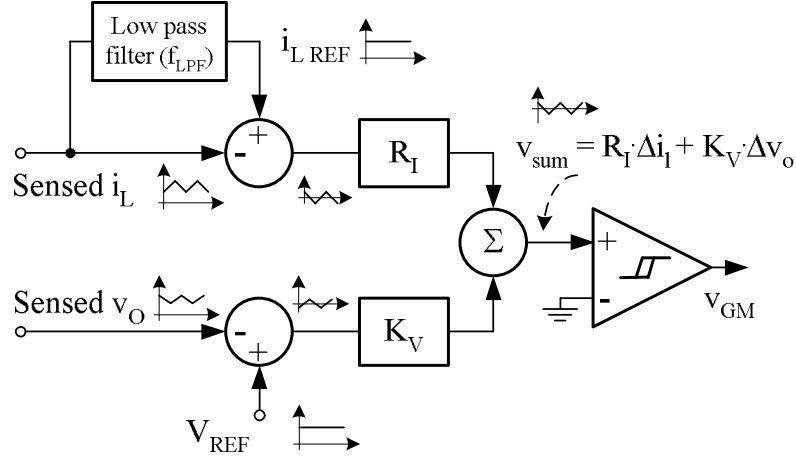
In addition, the implementation of a digital controller involves a significant increase in system complexity and hence the resulting system architecture. The result is high cost,

typically several-fold higher than that of the simpler analog controller. This cost issue has significantly limited the acceptance of digital controllers.

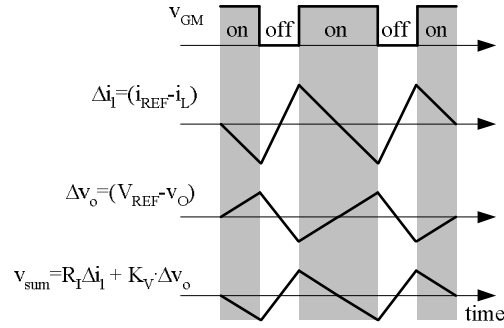
3.4. Sliding-Mode Control

The last chapter discussed hysteretic control in buck converters where the scheme was shown to resemble current-mode control therefore yielding a single-pole-like response and stability over a wide filter LC range. It was also seen that since in boost converters, the inductor current ripple does not flow through the output capacitor at all times, such inherent current-mode-like control was not possible. A general control form known as sliding-mode control partially overcomes this problem by explicitly combining the inductor current and output voltage ripples (Fig. 3.7(a)).

Sliding-mode control [39], [40] combines scaled values of the inductor current (i_L) and capacitor voltage (v_O) errors, to form a new variable v_{SUM} , which is regulated in a negative feedback loop. Typically, the composite variable v_{SUM} is modulated into the switch duty-cycle by means of a hysteretic comparator, but constant-frequency modulations schemes are also possible at the cost of slower transient response and narrower stability range. The inductor current and output voltage ripples are extracted by removing the dc values from their respective sensed signals. For the sensed output voltage, the dc value is given by its reference voltage V_{REF} , while for the inductor current, whose dc value can change with load, the dc (or low frequency) value is obtained as a low-pass filtered version of the sensed current itself.



(a)



(b)

Fig. 3.7. (a) Simplified representation of a sliding-mode controller, and (b) waveforms.

This is shown in Fig. 3.7, where the regulating loop controlling the combined variable v_{SUM} , is a high-frequency hysteretic loop. In a buck converter, voltage hysteretic control inherently combines output voltage and inductor current information through output capacitor ESR. However, it is shown in Appendix B that in order to obtain stable sliding-mode operation in boost converters, the scaling factor R_I for the inductor current ripple needs to hold a certain relationship with the scaling factor K_V for the output voltage ripple, as follows

$$\frac{K_V}{R_I} \leq \frac{V_O \cdot C_O \cdot (1 - D_M)}{I_O \cdot L}, \quad (3.6)$$

where C_O is the output capacitance, D_M is the duty-cycle of switch S_M (Fig. 3.4), and L is the filter inductance.

This technique has two disadvantages. From equation (3.1) stable operation for large inductance and small capacitance values at high loads requires the ratio of R_I to K_V to be greater than a specific value. This choice of R_I and K_V , besides removing the one-cycle fast transient response of hysteretic-type controllers, gives impractically high switching frequencies for small inductance and large capacitance values. In addition, the time constant τ of the low-pass filter (LPF) that extracts the inductor current ripple, needs to be low enough to filter out the lowest switching frequencies that occur for high inductance and low capacitance values. The low-bandwidth filter pole slows down the rate of increase or decrease of the current reference and hence the inductor current in a transient, causing further deterioration of the converter transient response.

3.5. Summary

Table 3.1 shows a qualitative comparison of the studied techniques based on various criteria, like system complexity, transient response, power losses, output ripple accuracy, stability in a variable L-C-R environment, and versatility of application to various converter topologies. Schemes (2) and (3), based on averaged feedback control though effective in eliminating the RHP zero and the adverse effects of L-C variations respectively, are complex, inefficient, and/or slow. On the other hand, voltage-mode hysteretic control as applied to buck converters is fast, simple, and impervious to L-C variations, thus being most suitable for IC implementation. However, the technique is less versatile and has yet to be a solution for boost and buck-boost converters. Sliding-mode control offers a partial solution to the LC compliance problem by explicitly mixing

sensed current and voltage errors to enable current-mode control, however like conventional PWM solutions, the LC compliance comes at the cost of a severe drop in system bandwidth and hence, transient response.

Table. 3.1. Comparison of state-of-the-art stabilization techniques studied

	Masking L-C-R (and/or ESR) Parameters			RHP Zero Elimination		Adaptive control		Boundary control	
Parameter	Feed forward	Modified Hysteretic	Constant L-C-R load	Constant capacitor discharge	Output peak control	Multiple operating point	Digital control	Voltage hysteretic control	Sliding- mode control
Complexity	Medium	Low	Highest	Medium	Medium	High	High	Lowest	Medium
Response	Slowest	Fast	Medium	Medium	Slow	Slow	Slow	Fastest	Medium
Power loss	Low	Medium	Low	Highest	Low	Low	Low	Low	Low
Output ripple	Low	Lowest	Low	Low	High	Low	Low	Low	Low
L-C-R variation	Medium	Highest	High	Low	Lowest	High	High	High	Highest
Versatility	High	Medium	Low	Low	Low	High	Highest	Medium	High

CHAPTER 4

DUAL-LOOP SIGMA-DELTA ($\Sigma\Delta$) CONTROL

As seen in chapter 3, in general, obtaining filter LC compliance in power supplies comes at the cost of lowered loop bandwidth. In such cases, the essential idea is to reduce the bandwidth of the frequency compensation circuit and hence the unity-gain frequency of the closed loop converter to a value much lower than the worst-case locations of the filter LC poles and in the case of boost converters, the RHP zero. This bandwidth reduction ensures that the closed-loop response is largely independent of filter components, making the system LC compliant. Clearly, this bandwidth decrease comes at the cost of a severely degraded transient response, over the entire filter LC range. This chapter introduces a dual-loop asynchronous sigma-delta ($\Sigma\Delta$) control technique that achieves wide LC compliance without compromising transient response. After a brief introduction to asynchronous $\Sigma\Delta$ control, referred to hereafter simply as $\Sigma\Delta$ control, this chapter goes on to describe the operation of the proposed circuit that is then validated through simulation and experimental results.

4.1. Sigma-Delta Control in Switching Supplies

4.1.1. Basics of $\Sigma\Delta$ Control

Literature of sigma-delta ($\Sigma\Delta$) control in switching power supplies primarily focuses on its relevant noise-shaping qualities [41-42], not stability and bandwidth, which are the focus of this work. The basic operation of a first-order $\Sigma\Delta$ controller can be inferred from Fig. 4.1 [43]. Qualitatively, a negative feedback loop comprised of a low pass filter, a gain, and two summers, one of which is in the form of a comparator, ensures the output and average of signal u are regulated against REF and R, respectively. Since

feedback loop modulates the duty-cycle to ensure that the average resistor-divided version of v_O is regulated to V_{REF} .

Operationally, average inductor current I_L flows to the load as I_{OUT} creating the DC voltage V_O , while ac ripple i_l flows directly into output capacitor C as i_c . The voltage across capacitor C_O 's equivalent series resistance (ESR) is normally dominant in these converters [21], forcing output ripple voltage v_o to mimic inductor ripple current i_l (i.e., $v_o \approx v_r = i_l \cdot R_{ESR}$). The end result of this is that the inductor's ac current is also regulated, for all practical purposes turning the inductor into a current source and simplifying the feedback loop response to a single pole response (complex-conjugate LC pole pair is eliminated), which is characteristic of current-mode switching converters. A single pole, of course, guarantees stability, irrespective of LC values.

When rearranged (Fig. 4.2(b)), this buck converter simplifies to the basic $\Sigma\Delta$ loop shown in Fig. 4.1. Comparator CP_V translates to a binary comparator with a series inverting V_{IN} multiplier, constraining the effective R of the $\Sigma\Delta$ loop (v_O in this case) within 0 and V_{IN} . Inductor L adds the second summer and $1/Ls$ filter to the loop. This summing relationship results because inductor current i_L is a function of v_O , $(V_{IN} - v_{OUT})/Ls$ for a "1" and $-v_{OUT}/Ls$ for a "0" state of signal V_u .

Note 1: From Fig. 4.1, signals v_u and R need to feed into a low-pass filter (k/s) to operate the $\Sigma\Delta$ loop. Generalizing from Fig. 4.2(b), when these signals are voltages, an inductor is compatible as the corresponding low-pass filter ($1/Ls$). Similarly, in a dual representation of Fig. 4.2(b), when the effective u and R are currents, a capacitor would form the compatible filter ($1/Cs$).

Signal v_O in Fig. 4.2(b) (R in Fig. 4.1) corresponds to the DC (V_O) and ac (v_o)

portions of the output voltage, the latter of which is practically (and by definition) significantly smaller (e.g., v_o is less than 2% of V_O). The inductor ripple current is consequently mostly a function of V_O , the DC portion of the output voltage (i.e., $R \approx V_O$). Since the output of a buck converter is always less than V_{IN} , the effective R is naturally constrained within the range of $(0 \times V_{IN})$ and $(1 \times V_{IN})$, satisfying inequality (4.1).

4.1.3. Sigma-Delta Control in Boost Converters

In a boost converter (Fig. 4.3), the output voltage is the peak of the duty-cycle modulated switching signal v_{PH} , not the average, like in the buck converter. Signal v_{PH} swings from ground through switch S_M to a voltage higher than V_{IN} . Since the average voltage across L is 0 (i.e., V_{PH} equals V_{IN}), the duty-cycle of v_{PH} determines its peak voltage, which is captured by output capacitor C_O through diode D . As a result, C_O is disconnected from inductor L when v_{PH} is grounded (during the on-time of switch S_M) and inductor current i_L is therefore not fully impressed across resistor R_{ESR} . The end-result is that current is not fully sensed and the conditions leading to the buck converter's single pole response are no longer present. In other words, the boost circuit is not inherently stable and v_O cannot be used as an independent $\Sigma\Delta$ variable [16].

For $\Sigma\Delta$ (sliding-mode) control and inherent stability in boost converters, as in the sliding-mode buck regulator, output voltage and inductor current (i_L) must be sensed and

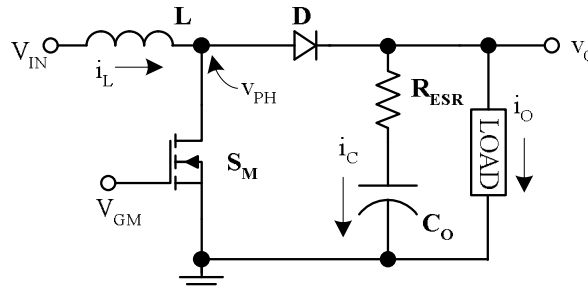


Fig. 4.3. Simplified schematic of a boost converter.

summed to give a combined variable, which is then regulated in a single $\Sigma\Delta$ loop [38, 39]. Although this approach provides stable operation for a wide range of LC values, its transient response performance is limited. Since the current loop must regulate i_L to sustain load current I_O , current reference I_{REF} is derived by averaging i_L with a low pass filter pole significantly lower than the lowest switching frequency [45], [46] which in turn is determined by the worst-case LC filter combination (i.e., highest L and C). This low frequency pole ultimately determines the effective bandwidth of the system, forcing a slower than ideal transient response for lower LC values [47].

Other $\Sigma\Delta$ -based boost converter schemes operate in pulse frequency modulation (PFM) mode. Of these, the common “Burst mode” technique [48] has high peak to average current ratios, narrowing its application to low output current devices. Reference [49] describes a PFM circuit that operates at a constant predetermined duty-cycle, which eliminates high peak currents, but at the cost of non-linear compensation requirements with respect to application design parameters [49] and input voltage dependence. The key feature of the proposed dual $\Sigma\Delta$ -loop approach is that the inductor current and output voltage are regulated in separate $\Sigma\Delta$ loops. Regulating the inductor current independently allows the inductor current reference to respond faster to load-dump events. As a result, LC compliance is obtained for a wide range of loading applications without sacrificing bandwidth and hence transient response.

4.2. Proposed Dual-Loop Sigma-Delta ($\Sigma\Delta$) Controller

To achieve the LC compliance desired with no compensation circuit, v_O and i_L are sensed and controlled separately. i_L is regulated with main switch S_M (Fig. 4.4) at higher bandwidth to produce 5% more current than necessary to support i_O , the result of which is

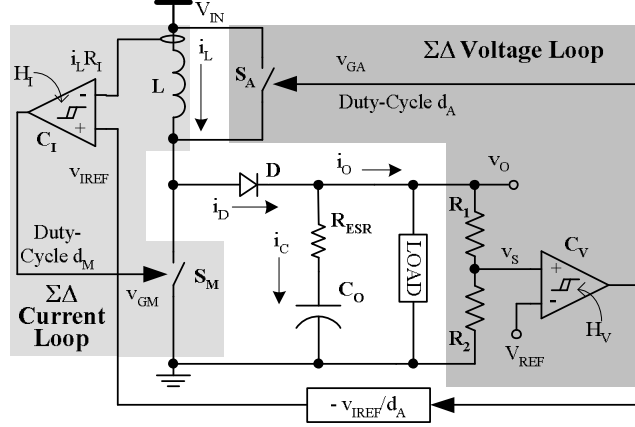


Fig. 4.4. Proposed Dual-Loop $\Sigma\Delta$ -boost converter circuit.

that the inductor acts like a current source at lower frequencies (Fig. 4.5(a)). Auxiliary switch S_A is switched to supply the load with only the current required (additional 5% circulates through S_A), thereby regulating v_O . In comparing Figs. 4.5(b) and 4.5(c) with Fig. 4.1, the current and voltage $\Sigma\Delta$ loops are observed to be stable because their cross-referenced R 's (i.e., V_{IN} and I_O , respectively) lie within 0 and V_O and 0 and $D'_M I_L$, where $D'_M = (1-D_M)$, satisfying inequality (4.1).

A reference current that is 5% higher than the necessary load current is derived and averaged from the voltage loop with a duty-cycle-to-voltage demodulator. Since switch S_A is modulated to ensure only the load current is supplied, its duty-cycle d_A contains load current information. Consequently, a d_A of 5% implies 5% of the total

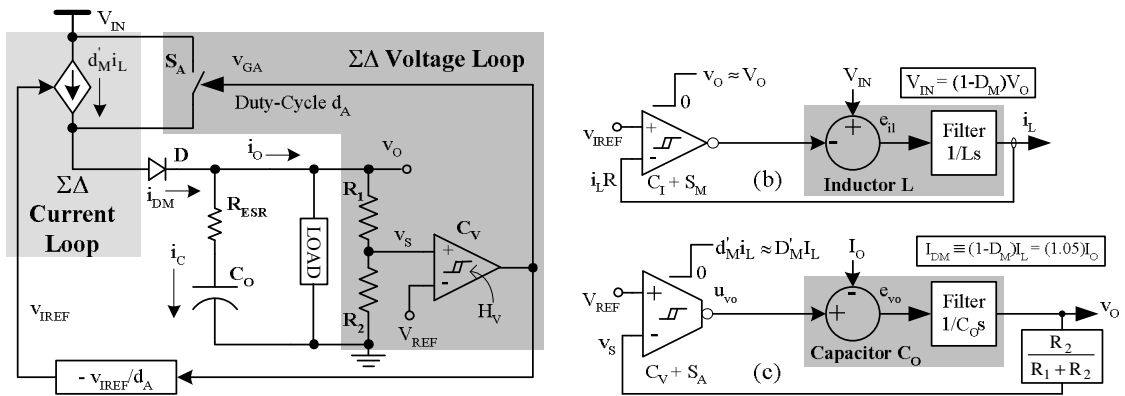


Fig. 4.5 (a) Equivalent low-frequency circuit and its corresponding (b) current and (c) voltage $\Sigma\Delta$ -loop models.

inductor current is circulated back through S_A and not supplied to the load. This additional current, which constitutes a conduction power loss not present in conventional boost converters, is kept low at only 5% above the nominal value.

Fig. 4.6 shows how this demodulator can be implemented. Capacitor C_1 is charged and discharged by complementary switching current sources I_{CH} and I_{DCH} and its sequence is synchronized to d_A . Steady-state is achieved when the average capacitor current is zero, which occurs when the charge injected into C_1 by I_{CH} during S_A 's off time balances the charge removed by I_{DCH} during S_A 's on time. By designing I_{DCH} to be 19 times larger than I_{CH} , V_{IREF} reaches steady state only when S_A 's off time (i.e., I_{CH} charging C_1) is 19 times greater than S_A 's on time (i.e., I_{DCH} discharging C_1), in other words, when d_A is 5%.

Comparator C_T is added to clamp the current reference to a higher than normal value during a positive load-dump event, when load current increases quickly. Without it, the inductor current is not sufficiently large to support the higher load. Comparator C_T therefore increases the reference current (V_{IREF}) to a peak value (V_{IPK}) when the output voltage drops sharply beyond a percentage of its nominal value (e.g., 2% below), which corresponds to a load dump. V_{IPK} represents the peak-rated load current of the converter, above which load current cannot be sustained. Inductor current i_L consequently slews until it reaches its peak rating in a single switching cycle of S_M , after which output

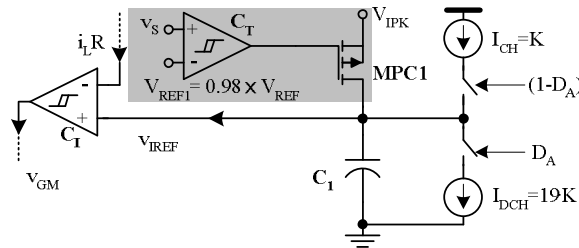


Fig. 4.6. Charge-based duty-cycle-to-voltage demodulator.

capacitor is charged to its desired level in a single switching cycle of S_A . Once these two levels are reached, switch S_T turns off and inductor current reference v_{IREF} gradually decays until duty-cycle d_A is again at 5%.

The current loop has higher bandwidth and is therefore switched at higher frequencies via switch S_M . The duty-cycle of switch S_A is only 5% to keep conduction

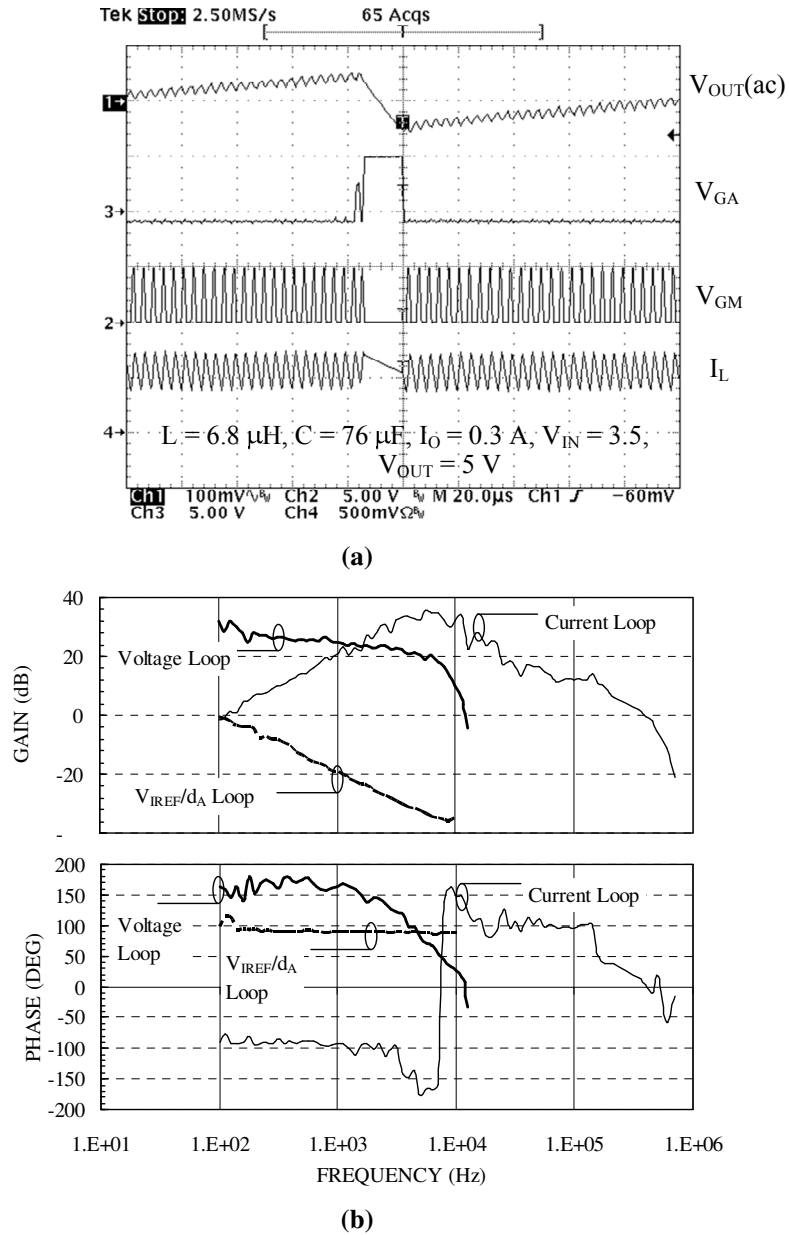


Fig. 4.7. (a) Measured steady-state waveforms for the proposed dual-loop boost $\Sigma\Delta$

power losses low. The resulting output ripple voltage is therefore a combination of a high frequency low voltage ripple (e.g., 30 mVp-p) due to d_M and a low frequency high voltage ripple (e.g., 170 mVp-p or $\pm 1.7\%$ of V_O) due to duty-cycle d_A , which is compatible with the performance of some commercially available boost regulator ICs [49] used in applications where low ripple voltage is not paramount.

In general, the switching frequencies of both the control loops vary with the slopes of the regulated current or voltage ripples, which depend on V_{IN} and/or I_{OUT} . Specifically, the rising and falling slopes of the current ripple vary in opposite directions with increasing V_{IN} ; hence, the S_M 's switching frequency exhibits a parabolic variation that peaks when the slopes are equal in magnitude – 50% duty cycle. In the voltage loop, the rising/falling slopes and the switching frequency increase with I_O . Solutions to switching frequency variations including variable hysteresis [50], variable delay [51], dither [52] etc., are found in literature.

Continuously sensing the inductor current can be a power-consuming function and a review of available sensing techniques in the literature is offered in [53]. The simplest and most accurate means of sensing a current is through a series sense resistor; however, its related conduction losses (e.g., $i_L^2 R$) are sometimes prohibitive. Quasi-lossless techniques such as R_{DS} sensing and the one proposed in [53] are feasible, though often complex. A sense resistor is used in this paper for simplicity but the reader is encouraged to consider lower power alternatives.

4.2.1. Steady-State Analysis

Switches S_A and S_M essentially attenuate the amount of inductor current delivered to the output by increasing their respective duty-cycles. In other words, the average

current sourced by the L-S_A combination (I_{LA}) over a switching cycle of switch S_A is a fraction of the inductor current and is set by S_A's duty-cycle D_A ,

$$I_{LA} = I_L(1 - D_A). \quad (4.2)$$

Similarly, the current supplied to the output capacitor and load through diode D (I_D) averaged over a switching cycle of S_M is a fraction of aforementioned average current I_{LA} and set by S_M's duty-cycle D_M ,

$$I_D = I_{LA}(1 - D_M) = I_L(1 - D_A)(1 - D_M). \quad (4.3)$$

This diode current is then decomposed in two, into load current I_O and capacitor current i_c :

$$I_D = I_O + i_c = I_L(1 - D_A)(1 - D_M), \quad (4.4)$$

and since capacitor current in steady-state is zero,

$$I_L = \frac{I_D}{(1 - D_M)(1 - D_A)} = \frac{I_O}{(1 - D_M)(1 - D_A)}. \quad (4.5)$$

In a standard boost converter, switch S_A is absent; D_A therefore reduces to zero in equations (4.2)-(4.5), giving the nominal average inductor current for the proposed circuit and corresponds to a conventional boost converter relation [20],

$$I_{LNOM} \equiv \frac{I_O}{(1 - D_M)}. \quad (4.6)$$

In the proposed switching supply, D_A is set to 5%, thereby increasing the average inductor current and related conduction losses by approximately 5%. The dc switch-conduction power loss, easily seen to be

$$P_{DC} = I_L^2 \left(R D_A' + R_{ONSA} D_A \right) = \frac{I_{L(MIN)}^2 R}{D_A'} \left(1 + \frac{R_{ONSA}}{R} \frac{D_A}{D_A'} \right), \quad (4.7)$$

where R_{ONSA} and $R=R_{\text{ONSM}} \approx R_{\text{ONSD}}$ are the on-resistances of switches S_A and S_M , S_D respectively, is clearly higher than that in a conventional boost converter ($I_{\text{L(MIN)}}^2 R$), and hence is kept small by designing D_A at 5%. In an IC implementation, the switch S_A can be reduced to a fraction of S_M , to save die area and cost, so long as S_A 's on-state voltage drop is small compared to $(V_O - V_{\text{IN}})$, i.e., S_A acts as a short. The increased power loss due to a higher R_{ONSA} can be partially compensated by reducing D_A to less than 5%. Additional energy loss is also incurred in switch S_A during a transient while the inductor current settles from its peak to its steady-state value (section III(B)); however, load/line transients are typically infrequent events and the impact on overall power efficiency is considered negligible.

4.2.2. LC Compliance Limits

Sigma-delta regulation of the output voltage requires inductor current I_L to be regulated throughout the bandwidth of the main voltage loop to ensure the inductor acts like a current source, eliminating the cumbersome LC complex conjugate pole pair. Consequently, the bandwidth of the current regulation loop must be higher than that of the voltage regulation loop and, since the unity-gain bandwidth in self-oscillating control is at the switching frequency of the switch [39], the switching frequency of S_M must be higher than that of S_A .

To ensure S_M switches faster than S_A , the output ripple voltage resulting in a switching cycle of S_M , which is set by the hysteresis window H_I of the current regulation-loop comparator, must be lower than in a switching cycle of S_A , as illustrated in Fig. 4.7. The on time of S_M is set by the hysteresis window H_I ,

$$t_{ON} = \frac{H_I}{(di_I/dt)_{ON} R_I} = \frac{H_I L}{V_{IN} R_I}, \quad (4.8)$$

where R_I is the current-sensing resistor. During this on time, output capacitor C_O is discharged by load current I_O , and assuming a high frequency capacitor is used (i.e., low R_{ESR}), the resulting output ripple voltage for a switching cycle of S_M is

$$\Delta V_{OM} = t_{ON} \left(\frac{dv_O}{dt} \right)_{ON} = \left(\frac{H_I L}{V_{IN} R_I} \right) \left(\frac{I_O}{C_O} \right). \quad (4.9)$$

To satisfy the aforementioned bandwidth requirement, ΔV_{OM} must be less than the overall voltage window of v_{OUT} , which is set by the hysteresis window of the voltage control-loop comparator (H_V),

$$\Delta V_{OM} = \left(\frac{H_I L}{V_{IN} R_I} \right) \left(\frac{I_O}{C_O} \right) \leq \frac{H_V}{M} \quad (4.10)$$

or

$$C_O \geq \left(\frac{H_I}{H_V} \right) \left(\frac{I_O M L}{V_O R_S (1 - D_M)} \right) = C_{MIN}, \quad (4.11)$$

where M is the feedback resistor-based voltage divider ratio at the output, V_{IN} is replaced by conventional boost converter relationship $V_O(1-D_M)$ [20], and C_{MIN} is the minimum capacitance required for stable conditions to prevail, given an inductor value L .

4.2.3. Small-Signal AC Analysis

The voltage loop senses v_O and modulates duty-cycle d_A to ensure that only the demanded load current flows through the diode to the output, and the rest of the inductor current freewheels. Hence, the diode current is

$$i_D = (1 - d_A)(1 - d_M)i_L = i_c + i_O. \quad (4.12)$$

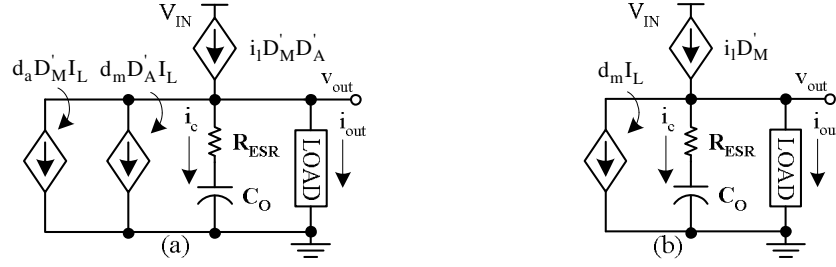


Fig. 4.8. Averaged and linearized models of (a) proposed and (b) conventional boost converters.

In terms of ac analysis, Eq. (4.12) can be written in terms of its dc and ac components:

$$I_D + i_d = (D'_A - d_a)(D'_M - d_m)(I_L + i_l) = I_O + i_c + i_o, \quad (4.13)$$

and linearized against small-signal stimuli:

$$i_d = -d_a D'_M I_L - d_m D'_A I_L + i_l D'_M D'_A, \quad (4.14)$$

to define the small-signal equivalent circuit model shown in Fig. 4.8(a), which simplifies to Fig. 4.8(b) in standard boost converters, where S_A is absent (i.e., d_A is 0). Therefore, in traditional boost converters, any small-signal variation (e.g., change in i_o) requires a corresponding change in inductor current i_L to meet the new load requirement. This change in i_L is brought about by a change in d_M , which also introduces an out-of-phase feed-forward path to the output, creating a right-hand plane (RHP) zero. On the other hand, a similar load change in the proposed converter is met simply by modulating

Table 4.1. Converter simulation parameters and operating conditions for the dual-loop $\Sigma\Delta$.

Parameter	Value	Parameter	Value
V_{IN}	1-1.5V	V_O	$3.3 \pm 5\%$
I_O	0.1-1A	L	2 μ H
C	44 μ F	ESR_C	20m Ω
S_M (N-ch) R_{ON}	0.1 Ω	S_A (N-ch) R_{ON}	0.1 Ω
D (P-ch) R_{ON}	0.15 Ω	I_{CH}	1 μ A
I_{DCH}	19 μ A	C_1	10nF
V_O H_V	36mV	I_L hysteresis H_I	40mV
M	0.364V/V	R_I	0.1 Ω
Simulator	Spectre-S	Technology	0.5 μ CMOS

auxiliary duty-cycle d_A , keeping d_M and i_L virtually unchanged and eliminating the RHP zero effect.

4.3. Simulation and Experimental Results

4.3.1. Circuit Simulations

The proposed circuit was designed in the AMI 0.5 μ m CMOS process and simulated in the Cadence environment using the circuit simulator Spectre-S under the conditions listed in Table 4.1. Fig. 4.9(a) shows the steady-state waveforms of the output voltage, inductor current, the gate voltage of switch S_A , and the reference voltage for the sensed inductor current. The average output voltage of 3.297V has a small, high frequency ripple during the off time of switch S_A , corresponding to switching of S_M , superimposed on a low frequency ripple of ± 35 mV corresponding to the switching of S_A . Similarly, the inductor current has a high frequency ripple of ± 250 mA superimposed on a low frequency ripple of ± 50 mA, the latter being a reflection of the voltage ripple on V_{IREF} . The recorded switching frequencies (1.6MHz for S_M and 7.4kHz for S_A) easily

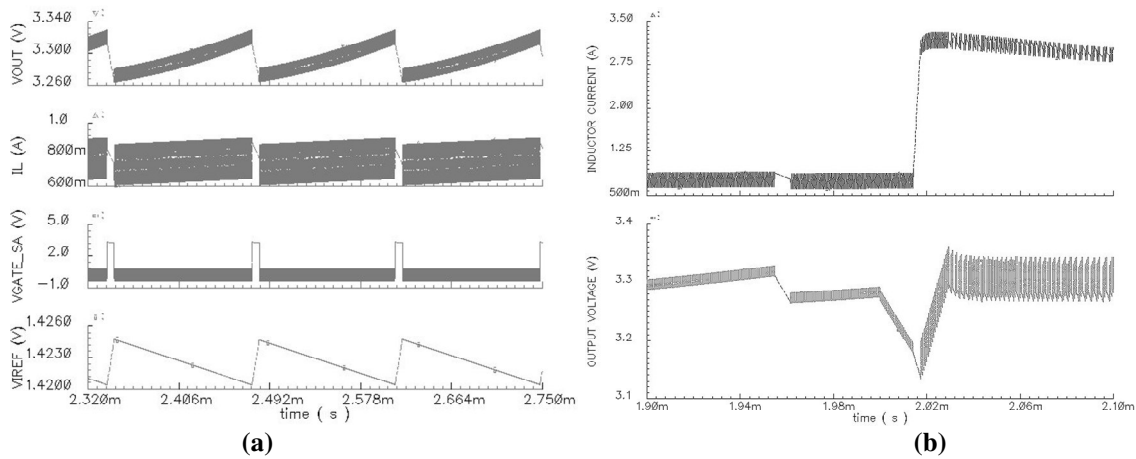


Fig. 4.9 Waveforms for the proposed circuit showing three switching cycles of switch S_A during steady state operation at $V_{IN}=1.5$ V, $I_O=0.3$ A, $V_O=3.3$ V, $f_{SW}(S_A)=7.4$ kHz, $f_{SW}(S_M)=1.6$ MHz, and (b) transient waveforms: step load 0.3 to 0.6A, $V_{IN}=1.5$ V, $V_O=3.3$ V.

satisfy the conditions as required for inequality (7).

Transient response of the simulated circuit, for a load step of 0.3 to 0.6 A in 10 ns, is shown in Fig. 4.9(b). The inductor current rises in a single step to about 3.4 A, which is slightly larger than the 3.2 A required to support a full load current of 1 A. Decay in the inductor current is also observed, once the output voltage reaches 3.3 V.

4.3.2. Experimental Prototype Evaluation

A prototype printed-circuit board (PCB) of the proposed solution (shown in Fig. 4.10) was built and evaluated to validate and quantify its operational limits. The experimental results were compared against a reference leading commercially available peak current-mode controller IC, referred to in the foregoing text as “state-of-the-art.” The same power stage and gate-drivers were used for both control schemes (bold circuit) to ensure the comparisons were reasonable. The resulting prototype circuit is therefore the combination of the proposed $\Sigma\Delta$ control strategy, which is selected with $\Phi1$, and the state-of-the-art scheme, which is selected with $\Phi2$.

Switch S_A in the voltage loop is implemented with two back-to-back NMOS devices to achieve bi-directional operation without having to bias the bulk terminal separately, which would have been required to ensure the body diode is always reverse-biased. For simplicity and proof of concept, the inductor current is sensed with a series resistor – any other technique would have also worked and generated higher efficiency but at the cost of complexity. Table 4.2 provides a summary of the important parameter values of the proposed 3.5-to-5 V boost converter.

TABLE 4.2. Summary of parameters used in dual-loop $\Sigma\Delta$ measurements.

Parameter	Value	Parameter	Value
V_{IN}	3.5V	V_O	5V
L	3.9-15 μ H	C_O	3.3-250 μ F
R_{ESR}	30–110m Ω	I_O	0.1-1A
R_{ONSM}	22m Ω	R_{ONSD}	58m Ω
R_S	50m Ω	R_{ONSA}	44m Ω
C_V Hyst.	400mV	C_I Hyst.	80mV
C_I (Fig. 4.6)	0.6 μ F	$V_S/V_O = M$	0.5
I_{CH} (Fig. 4.6)	50 μ A	I_{DCH} (Fig. 5)	0.8mA

The state-of-the-art converter uses peak current-mode control and its gate-driving signal is injected to S_M and S_D 's dead-time drivers via a low impedance switch controlled by $\Phi 2$. Its switching frequency is adjustable and set to match that obtained in the proposed self-oscillating $\Sigma\Delta$ converter. Frequency compensation is realized with an external series R_C - C_C circuit connected to the output pin of the internal error amplifier. The comparative evaluation results are presented next.

LC Compliance: In a conventional controller with an integrated and therefore fixed frequency compensation circuit, the lag compensation network can be set according to

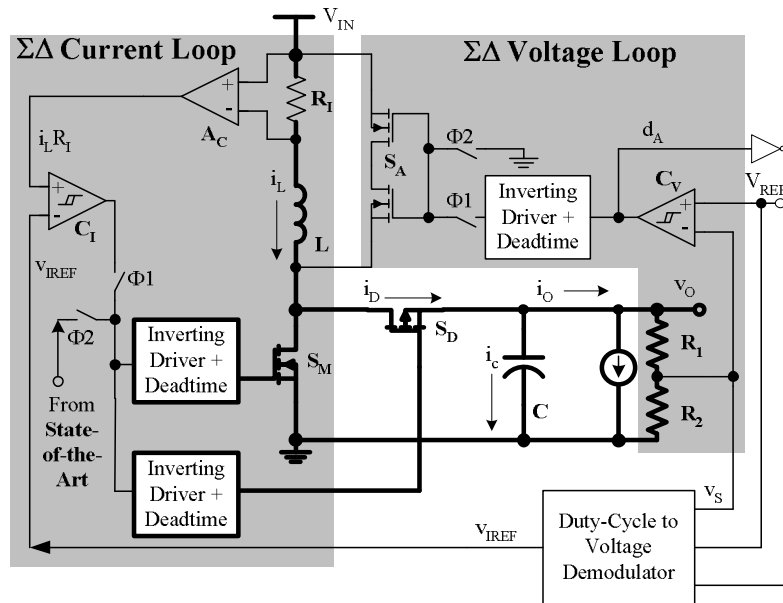


Fig. 4.10. Schematic of the dual-loop boost $\Sigma\Delta$ converter prototype.

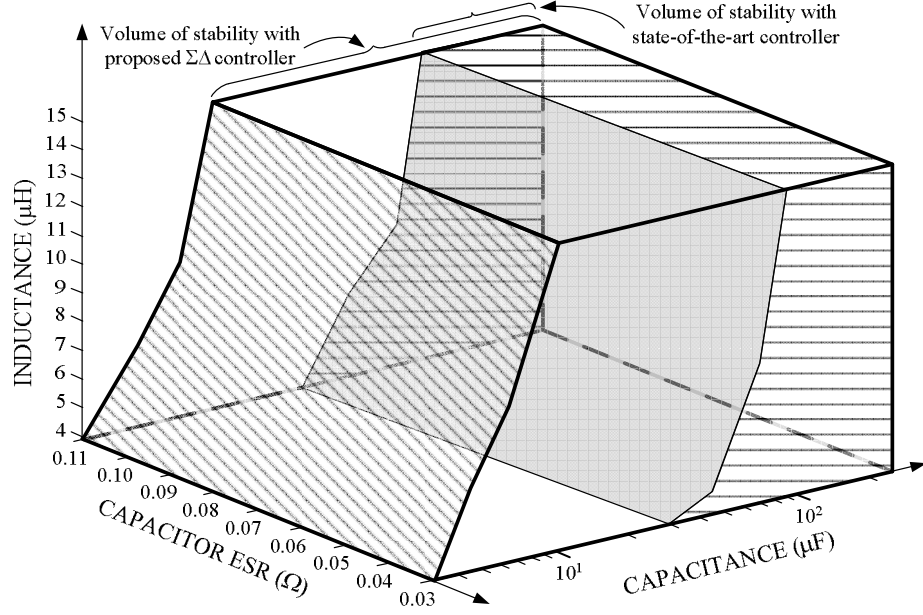


Fig. 4.11. 3-D contour curves of stability for the proposed and state-of-the-art (reference) boost converter circuits under various L , C , and R_{ESR} conditions.

the highest LC combination to tolerate a wide range of LC parameter variations. That feature, however, comes *at the expense of speed (bandwidth)* [54], and large output capacitance to accommodate for fast load and line transient events. The 3.5-to-5V, 1A state-of-the-art circuit is therefore designed to yield a maximum bandwidth of 25kHz and phase margin (PM) of 72° with an R_C - C_C compensation filter of $7.5k\Omega$ and $47nF$ and output LC filter of $3.9\mu H$ and $90\mu F$. Then, with the compensation circuit unchanged, LC values are varied until stable operation limits (10° PM) are reached. The worst-case condition for stability is observed to be at the highest load level, when the RHP zero is at the lowest frequency [20].

The same stability-testing procedure is subsequently repeated for the proposed $\Sigma\Delta$ converter. Its stability limit is reached when the current- and voltage-loop bandwidths are near one another. The smallest acceptable value of output capacitor C_O is determined at the highest load, as predicted by inequality (4.11). The maximum tested capacitance is limited to $250\mu F$, as a practically used limit for the evaluated power levels.

The resulting regions of stability, sometimes called “curves of death,” can be described by the LC-ESR “stability space volume” enclosures of Fig. 4.11. Since output ripple voltage requirements at 1 A must be met and the pulsed capacitor current in a boost converter leads to a pulsed output ripple voltage in the presence of a capacitor ESR, resistor ESR was limited to 110m Ω . Given these characteristics and constraints, the proposed $\Sigma\Delta$ converter approximately encloses an order of magnitude more volume than the state-of-the-art circuit, indicating significantly greater LC compliance.

At L and ESR of 6.8 μ H and 30m Ω , the minimum output capacitor value is approximately 50 μ F for the state-of-the-art boost converter, which is more than 10 times the corresponding minimum value of 4.5 μ F in the proposed $\Sigma\Delta$ converter. With increasing ESR values, however, the difference is slightly less. This results because the resistive component of the output ripple voltage increases with increasing ESR values, and to restrain the overall ripple voltage from surpassing design limits, the minimum output capacitor is slightly increased to 5.5 μ F in the proposed converter (at L and ESR values of 6.8 μ H and 110m Ω) to reduce the capacitive contribution and therefore offset the ESR-induced increase. On the other hand, the left-half plane (LHP) zero of the state-of-the-art boost converter is shifted to lower frequencies with increasing ESR values, decreasing the minimum capacitor value to 45 μ F (at L and ESR of 6.8 μ H and 110m Ω). Thus, the difference in the stability regions of the two strategies decreases slightly at higher ESR values, but remains roughly an order of magnitude better.

Transient Response: For a load-step response measurement, the compensation network is designed with an R_C - C_C filter of 3k Ω and 47nF to give a PM of 60° and crossover frequency of 22kHz, approximately half the frequency of the worst-case RHP zero

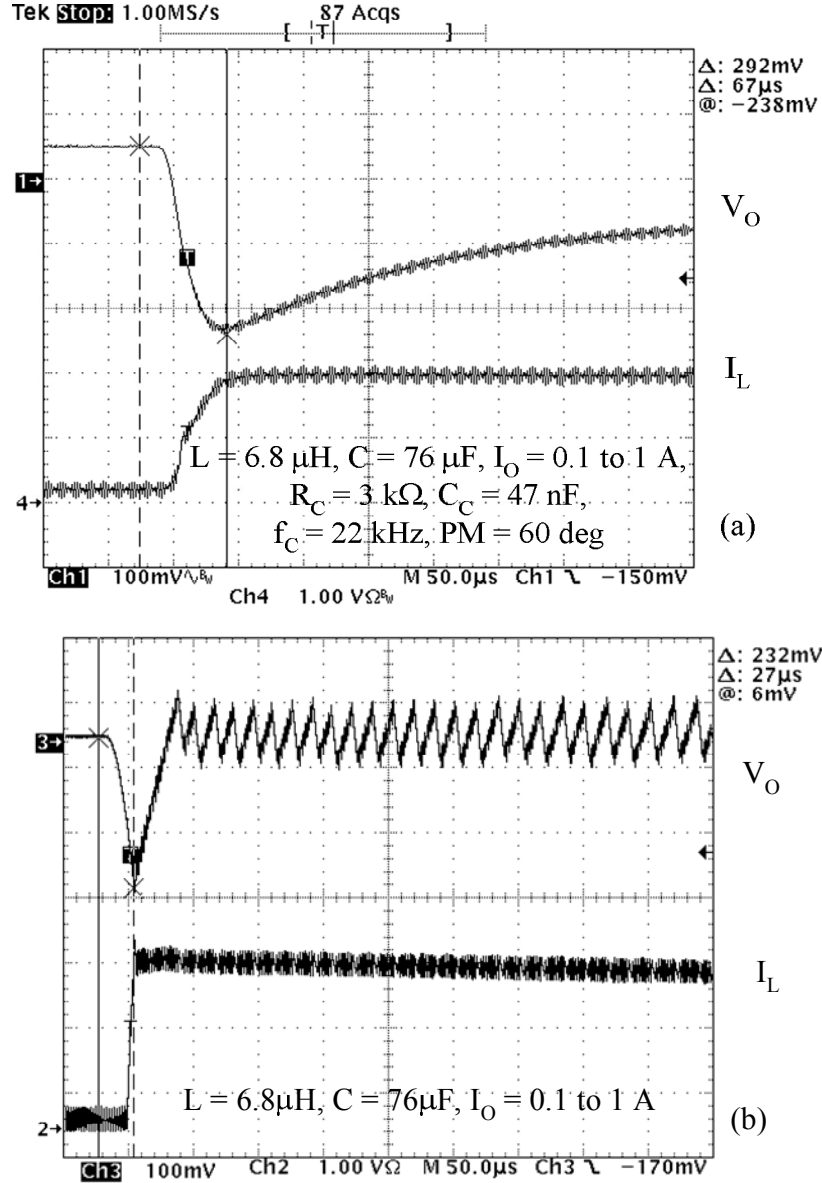


Fig. 4.12. Transient response to a 0.1-1A load step for the (a) reference and (b) proposed $\Sigma\Delta$ -boost converters.

(42kHz at 1 A load). Figs. 4.12 and 4.13 illustrate the transient response performance of the (a) state-of-the-art and (b) proposed $\Sigma\Delta$ converter circuits, the former of which is limited by loop bandwidth, exhibiting a larger voltage droop of 292mV with a response time of 400μs. The $\Sigma\Delta$ boost regulator's response time is limited only by the inductor slew rate (the inductor current is allowed to slew to 3A, as determined by V_{IPK} in Fig. 4.6), producing a sag of 230mV with a response time of 50μs. It is noted that the

compensation circuit for the state-of-the-art converter was designed for specific LC values to give a high crossover frequency; non-optimal compensation will further degrade transient performance, not improve it.

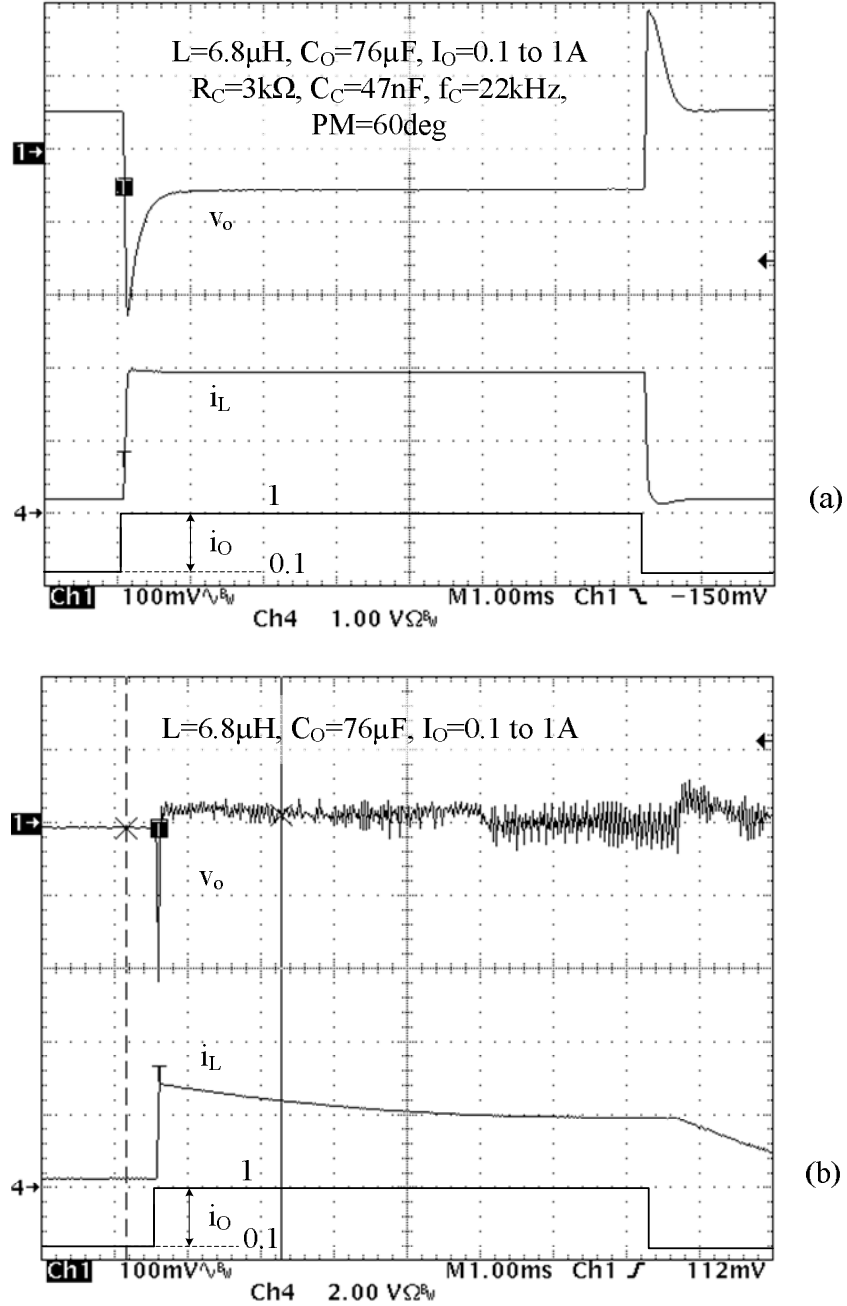


Fig. 4.13. Transient response to 0.1-1A and 1-0.1A load steps for the (a) reference and (b) proposed $\Sigma\Delta$ -boost converters.

Efficiency: Since faster transient response and better LC compliance in the proposed $\Sigma\Delta$ converter result at the cost of increased conduction power loss, efficiency is expected to be relatively lower. Fig. 4.14 shows the efficiency of the proposed and state-of-the-art converters at 300, 450, and 600kHz. The measurements include the power losses of the power stage and gate-drivers, common to both converters.

At lower frequencies, the efficiency of the proposed solution is always lower, 1.9% lower under high load current (5W) and at 300kHz. But as switching frequencies increase and loads fall below 2.5W, the efficiency of the proposed converter improves and even outperforms (2% better under 0.5W and at 600kHz) that of the state-of-the-art because switching losses become more dominant at lighter loads and the switching frequency of the proposed solution decreases with load.

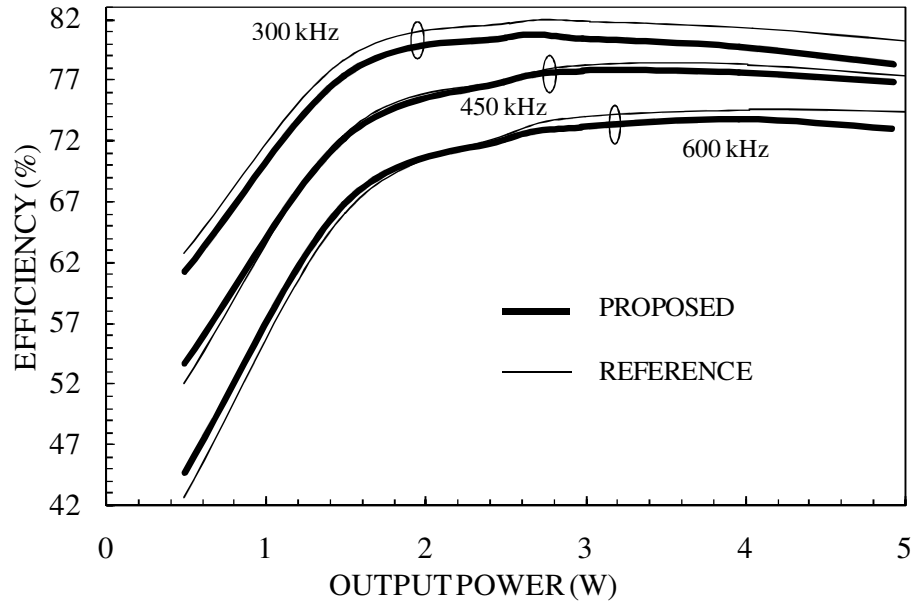


Fig. 4.14. Experimental efficiency performance of the proposed $\Sigma\Delta$ and reference converters, both operating at 300, 450, and 650kHz..

During the on time of auxiliary switch MNP3 (S_A), switches S_A and S_D are off for several switching cycles, eliminating the associated switching and gate-driver losses and

therefore improving power efficiency. The crossover point of the two curves, which is about 2.5W in the foregoing case for 600kHz, may be at lower load levels if smaller switches are used (e.g., integrated FETs), which yield higher conduction (i.e., higher resistance) and lower switching losses (i.e., lower capacitance).

4.4. Summary

The proposed dual $\Sigma\Delta$ -loop boost converter has roughly an order of magnitude better LC compliance and about 20% better transient response performance than the leading state-of-the-art boost circuit without the need for a frequency compensation circuit. It is able to achieve this performance by emulating the operation of the $\Sigma\Delta$ buck converter, which is inherently stable because both the inductor and output voltage are regulated. As a result, a $\Sigma\Delta$ loop is used to regulate the current at a higher frequency than the $\Sigma\Delta$ loop used to regulate the output voltage, which establishes the design constraint for this topology. The RHP zero path prevalent in conventional boost converters (i.e., oppositely phased feed-forward path through main switch S_M) is eliminated by virtue of decoupling the voltage feedback loop from boosting switch S_M .

The drawbacks to the proposed solution are higher conduction losses (e.g., 1.9% at 5W and 300kHz) and output ripple voltages. The higher switching losses, however, are offset at higher switching frequencies and lighter load levels because of lower switching and gate-driver losses (e.g., 2% better than that of the state-of-the-art at 0.5W and 600kHz). The steady-state output ripple voltage was higher than that of the state-of-the-art ($5V \pm 1.7\%$), but still well within typical accuracy specifications ($5V \pm 5\%$). In the end, the proposed boost converter circuit is close to the highly sought after attributes of “unconditional stability” and “high bandwidth,” all without any external frequency

compensation circuit, which is optimal for user-friendly, compact, low cost, and low power mobile applications.

CHAPTER 5

DUAL MODE SIGMA-DELTA ($\Sigma\Delta$) CONTROL

The last chapter discussed the dual-loop asynchronous sigma-delta ($\Sigma\Delta$) control technique that regulated the inductor current and output voltage using independent $\Sigma\Delta$ control loops that were controlled using separate switches. It was noted then that in providing the necessary filter compliance and transient response, this technique led to additional steady-state switching activity and somewhat higher steady-state voltage ripple. In some ripple-sensitive applications like audio amplifiers, critical processors, etc. [49], a high ripple voltage can degrade the performance of the electronic system being supplied, as explained in chapter 1. The controller proposed here overcomes the above limitation by implementing a dual-mode technique that gives both the LC-compliance and fast transient response of the aforementioned technique as well as the steady-state accuracy performance of a standard boost dc-dc converter.

5.1. Dual-Mode Converter System

5.1.1. Block Description

Functionally, the proposed converter [47] consists of two operating modes, viz., the main mode that operates in steady-state conditions and the bypass mode that operates during transient conditions only. A mode transition circuit enables transition between the two modes. A block-level representation of such a circuit is shown in Fig. 5.1(a). Both the main and bypass modes operate under the control of sigma-delta ($\Sigma\Delta$) control loops that effectively control the same system parameters (or system states), viz., the inductor current i_L and the output capacitor voltage v_O , although in differing fashions. While the bypass mode consists of threshold-based high-bandwidth control paths, the main mode consists of a continuous (after averaging – see Chapter 2) but low-bandwidth control

loop. As a result, the main control effectively has higher dc gain than the bypass control and therefore determines the steady-state operation of the converter. In other words, during steady state, the bypass mode controller is open and does not contribute to the regulating action in any way. On the other hand, during fast transients, the response of the main mode controller is negligible because of its low bandwidth. Therefore, the bypass control dominates and the system transient response becomes a function of the fast dynamics of the bypass mode. In other words, the main path is effectively open at high frequencies because its loop-gain is less than unity allowing the auxiliary bypass controller to take over temporarily the overall regulation of the dc-dc converter.

In terms of ac-equivalent frequency response, as shown in Fig. 5.1(b), the open-loop gain of the main control loop has a higher dc value but contains a low-frequency pole p_1 that leads to a gain drop-off at medium to high frequencies. The bypass loop, on the other hand has a low dc gain, but since its dominant pole p_2 is at a high frequency, its gain dominates over that of the main control beyond the frequency at which the two gain responses cross each other. This crossing frequency represents a zero z_1 in the overall system loop gain, which is the sum of the main and bypass loop responses. Therefore, the overall loop gain effectively has both a high dc gain and an extended bandwidth due to the feedforward zero z_1 giving the system good dc as well as high-frequency

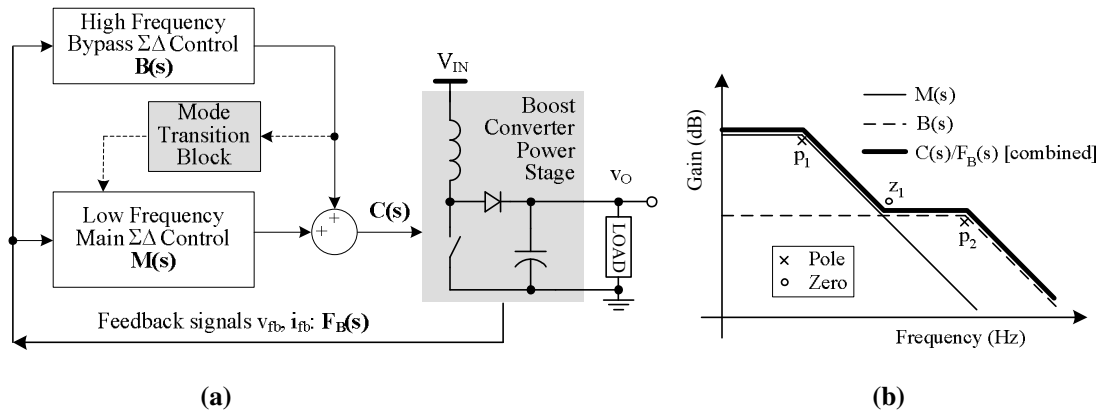


Fig. 5.1. (a) Block representation of the dual-mode boost dc-dc converter and (b) its simplified frequency response (Bode magnitude plot).

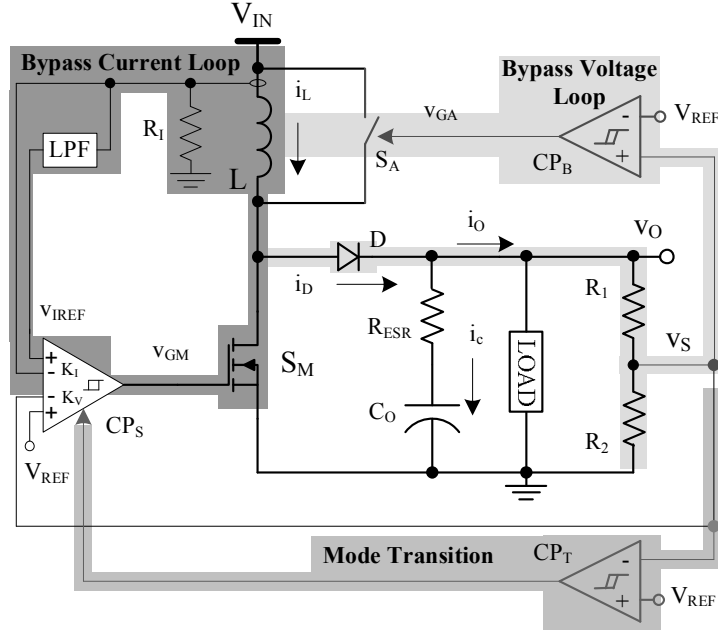
performances. Since each of the two modes is controlled by separate pairs of $\Sigma\Delta$ loops, a mode transition circuit gradually brings about the transition conditions to facilitate a smooth mode transfer.

5.1.2. Steady-State and Bypass Operation

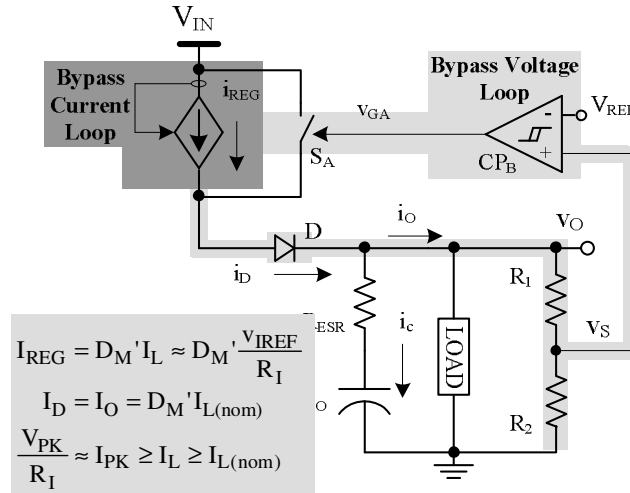
The proposed dual-mode converter (Fig. 5.2(a)) overcomes the low-bandwidth limitation by defining and asserting a high-speed mode during transient load-dump events. The basic objective is to bypass and override equivalent average inductor current v_{IREF} to a higher value almost instantly only during load dumps. During steady-state conditions, load current I_O and S_M 's off duty cycle D_M' (i.e., one minus on duty cycle D_M) set the nominal average inductor current I_{LNOM} required to support a given I_O because S_M splits I_L to ground and v_O according to duty-cycle D_M :

$$I_{LNOM} = \frac{I_O}{D_M'} = \frac{I_O}{1-D_M}. \quad (5.1)$$

In the bypass mode, the inductor current and the output voltage are regulated in independent loops (Fig. 5.2(a)). The bypass current loop, that modulates switching frequency and duty-cycle of main switch S_M , is the higher frequency loop and appears as a current source for frequencies of interest to the lower-bandwidth bypass voltage loop that controls auxiliary switch S_A . The sensed inductor current is regulated at its reference v_{IREF} such that the inductor current is more than its nominal value I_{LNOM} , needed to support the load current I_O . In other words, the average diode current I_D tends to be higher than I_O , causing the output capacitor C_O to overcharge. This overcharge is limited by the bypass voltage loop that regulates the output voltage by means of switch S_A and comparator C_B . When the sensed voltage v_s reaches the upper hysteretic window limit of C_B , switch S_A conducts, diverting excess inductor current away from the load and reverse biasing the diode D . As a result, the load current I_O discharges capacitor C_O until v_s



(a)



(b)

Fig. 5.2. (a) Simplified schematic of the proposed $\Sigma\Delta$ converter and (b) equivalent representation in the bypass mode showing the closed current loop.

reaches the lower hysteretic window of comparator C_B . At this point, switch S_A opens and the cycle repeats.

As long as the inductor current i_L exceeds I_{LNOM} , the bypass voltage loop, by independently regulating the output voltage, ensures that the voltage inputs of summing comparator C_S are virtually shorted, allowing C_S to regulate only i_L . The current loop, by consequently regulating the inductor current above I_{LNOM} , in turn allows the bypass

voltage loop to operate. The bypass mode thus sustains itself until the regulated current drops below I_{LNOM} .

During the bypass mode, the system stability and regulating performance is ensured when the $\Sigma\Delta$ current loop has a higher bandwidth than the $\Sigma\Delta$ voltage loop so that the current loop appears as a current source within the voltage loop. The unity-gain bandwidth of a $\Sigma\Delta$ loop being its switching frequency, the above condition means that the switching frequency of switch S_M be greater than that of switch S_A giving the stability requirement as shown in the last chapter:

$$C_O \geq \left(\frac{H_I}{H_V} \right) \cdot \left(\frac{I_O L}{V_O R_I (1 - D_M)} \right) \cdot \left(\frac{R_2}{R_1 + R_2} \right) = C_{OMIN}, \quad (5.2)$$

where H_I and H_V are the hysteretic windows of comparators C_S and C_B respectively, R_1 and R_2 are the voltage sense resistors, and C_{OMIN} is the minimum output capacitance for which stability is guaranteed.

5.1.3. Mode Transition

In a positive load transient, the load current suddenly rises causing the output

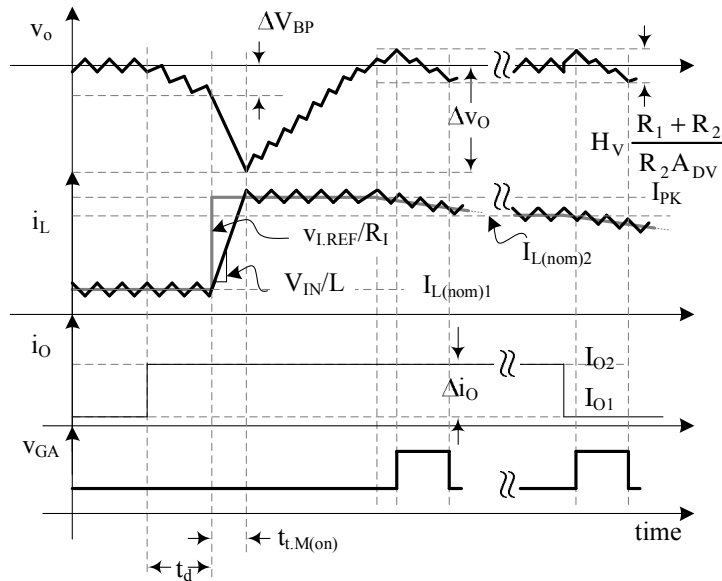


Fig. 5.3. Graphical representation of the transient performance of the proposed converter in response to positive and negative load transients.

voltage to droop. Transient comparator C_T perceives the load transient by sensing when the voltage drops below V_{REF} by a preset bypass voltage threshold of ΔV_{BP} , which in this case is 2.5% of V_{REF} , and clamps v_{IREF} to V_{PK} , where V_{PK} represents the maximum load the supply can drive. The inductor current i_L consequently slews until it reaches its peak rating I_{PK} in a single cycle of switch S_M , quickly charging C_O immediately after that in a single cycle of switch S_A . The resulting net transient-induced v_O drop (Δv_O) is the sum of pre-set voltage limit ΔV_{BP} and the additional voltage droop caused by I_O while i_L slews from $i_{L(ave)}$ to I_{PK} , as shown in Fig. 5.3:

$$\begin{aligned}\Delta v_O &= \Delta V_{BP} + \left(\frac{dv_O}{dt} \right) \cdot t_{iL} = \Delta V_{BP} + \left(\frac{I_O}{C_O} \right) \cdot \left(\frac{I_{PK} - i_{L(ave)}}{\left(\frac{di_L}{dt} \right)_{S_{M_on}}} \right) \\ &= \Delta V_{BP} + \left(\frac{I_O}{C_O} \right) \cdot \left[\left(\frac{V_{PK} - v_{IREF}}{V_{IN}} \right) \cdot \left(\frac{L}{R_I} \right) \right],\end{aligned}\tag{5.3}$$

where t_{iL} is the time for which the current i_L slews to I_{PK} . At this time, since the inductor current exceeds the required nominal value I_{LNOM} to support the present value of load I_O , the system automatically enters the bypass mode.

As mentioned earlier, the bypass mode sustains itself so long as the inductor current is in excess of the requisite steady-state current. Hence, to transition the circuit to steady state operation, a negative offset voltage V_{IOS} is introduced in the path of the current reference v_{IREF} (Fig. 5.4(a)) such that the actual average value of the sensed inductor current is higher than the reference v_{IREF} that the summing amplifier C_S perceives as the inductor current average. From Fig. 5.4(b), since the current inputs of the summing amplifier C_S are virtually shorted due to the $\Sigma\Delta$ current loop, the offset V_{IOS} appears across the filter resistance R_F of the low-pass filter (LPF) that generates the current reference v_{IREF} . As a result, the current loop essentially converts V_{IOS} into an offset current I_{IOS} that discharges the capacitor C_F causing v_{IREF} and therefore the inductor current to decay monotonically.

This decay continues until inductor current approaches the nominal value $I_{L\text{NOM}}$ required to supply the load current. At this point, the excess inductor current ($i_L - I_{L\text{NOM}}$) approaches zero thus eliminating any overcharge of the output capacitor C_O . In other words, auxiliary switch S_A stops switching and the bypass $\Sigma\Delta$ voltage loop opens up. Consequently, the virtual short across the voltage inputs of comparator C_S is removed enabling output voltage regulation via C_S . Any further decay in the inductor current is now prevented by C_S whose sensed voltage input v_s decreases if the average inductor current drops below $I_{L\text{NOM}}$. Thus, the inductor current and output voltage reach the main operating mode or steady state through a continuous and smooth process.

In the case of a negative load transient, the load suddenly drops to a lower value. As a result, the existing inductor current instantaneously is in excess of the required nominal current; hence, the system immediately transfers operation to the bypass mode with switch S_A diverting the excess inductor current. The mode transition from bypass to

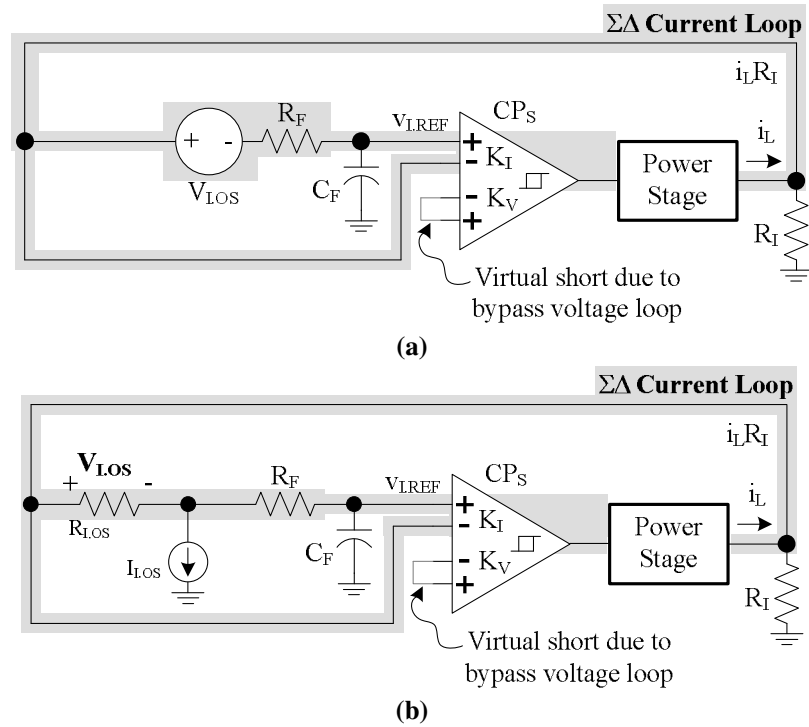


Fig. 5.4(a) Conceptual circuit schematic of the $\Sigma\Delta$ current loop during transition from the bypass mode to the main (steady-state) mode and (b) its simplified equivalent representation.

main mode is the same as described earlier. The performance and stability of the converter operating in the bypass mode was analyzed in the last chapter. This chapter therefore analyzes the stability and various performance aspects of the dual-mode converter in steady state.

5.2. Converter Analysis

5.2.1. Stability Analysis

The variation of the poles and zeros that depend on the output filter limits the $R_{ESR}LC$ space for which the $\Sigma\Delta$ controller is stable. To be more specific, LC values in a boost converter produce (Uncompensated L_{GV} in Fig. 5.6(b)) a pair of complex-conjugate poles (p_{LC}) and a right half-plane (RHP) zero (z_{RHP}) and the capacitor and its ESR a left half-plane zero (z_{ESR}). The latter typically does not reside within frequencies of interest intentionally because larger ESR values increase the output ripple voltage [20]. While an increase in the on time of switch S_M increases the energy stored in the inductor and subsequently the output voltage, disconnecting the output to do so allows the output voltage to droop, opposing the ultimate effect of increasing S_M 's on time. This opposing effect amounts to an out-of-phase, feed-forward path in the voltage loop from the gate of

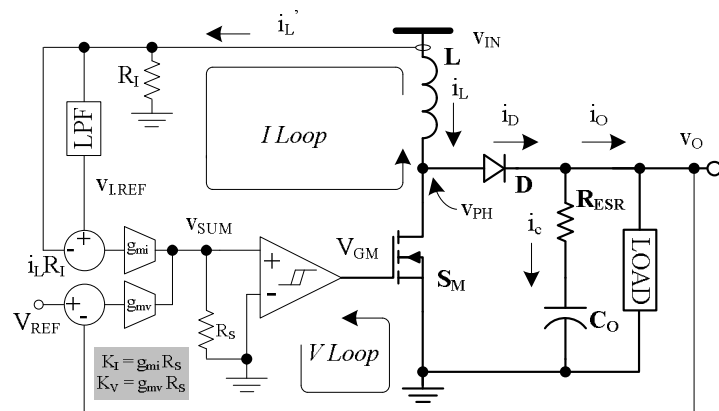


Fig. 5.5. Simplified schematic representation of current and voltage mixing in the $\Sigma\Delta$ boost converter in steady state.

switch S_M to the output (z_{RHP}).

The current loop is actually an inner loop for the voltage loop (Fig. 5.6(c)) [56]. As such, the current loop must first be stable and its closed-loop form used to determine the stability conditions of the voltage loop. One peculiarity of the boost converter is that the outer loop extracts two signals from the inner loop, as the diode current is the product of inductor current i_L and off duty cycle d_M' , which is a signal-flow way of describing z_{RHP} and why Fig. 5.6(c) extracts two feed-forward closed-loop signals (e.g., $i_{ddm.cl}$ and $i_{dl.cl}$) to output v_o .

The gain across the current loop is the product of the gains across the low-pass filter (LPF) and accompanying $R_{Igm}R_S$ combination, modulator gain M , and switch-

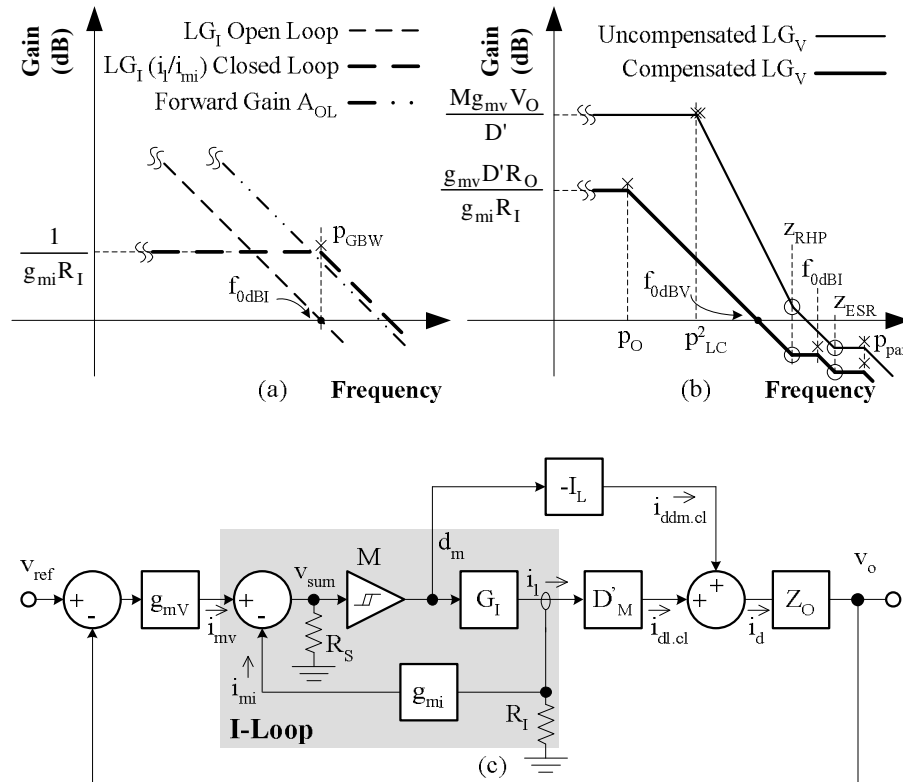


Fig. 5.6. High-frequency Bode magnitude plots of the (a) current and (b) voltage loops in the main-mode of the $\Sigma\Delta$ boost converter, and (c) equivalent control diagram highlighting the current loop, an inner closed-loop gain for the overall voltage loop.

inductor S_M -L combination. Under dc conditions, the sensed inductor current $i_L R_I$ equals its self-reference v_{IREF} , giving a zero at the origin because the difference between the two is zero, but the difference increases with frequency as the output v_{IREF} of the LPF is shunted to ground. Beyond the filter pole p_{LPF} , however, v_{IREF} has negligible ac signals and the loop gain levels.

The small-signal gain across switch-inductor S_M -L (G_I) is the ratio of small-signal inductor current i_l and duty cycle d_m , which results from applying dc output voltage V_O (variations in v_O are negligible at high-frequency) across inductor impedance L_s during the fraction of time S_M is off (off duty cycle d_M' or $1-d_M$ or its small-signal equivalent $-d_m$):

$$G_I \Big|_{f > p_{LC}^2} \equiv \frac{i_l}{d_m} = \frac{V_{IN} - v_{ph}}{d_m L_s} = \frac{0 - (-d_m V_O)}{d_m L_s} = \frac{V_O}{L_s}, \quad (5.4)$$

where the lower-case and capital subscripts indicate ac and dc quantities, respectively.

Thus, the current loop gain $|LG_I|$ at frequencies past LPF p_{LFP} (and LC poles p_{LC}^2) is:

$$|LG_I|_{f > p_{LFP}} = \left(\frac{v_{sum}}{i_l} \right) \left(\frac{d_m}{v_{sum}} \right) \left(\frac{i_l}{d_m} \right) = (R_I g_{mi} R_S) M \left(\frac{V_O}{L_s} \right). \quad (5.5)$$

Hence, at high frequencies, LG_I has a single pole response (Fig. 5.6(a)) and is therefore stable. Its unity-gain frequency (f_{0dBI}) largely sets the switching frequency of S_M at

$$f_{0dBI} = \frac{R_I g_{mi} R_S M V_O}{2\pi L}. \quad (5.6)$$

The compensated loop gain of the voltage loop ($|LG_v|$) is the product (Fig. 5.6(c)) of the gains across transconductor g_{mv} , the closed-loop current gain $A_{I,CL}$ of the current loop from i_{mv} to diode current i_d , and the load impedance Z_O . The latter is a parallel combination of output capacitive impedance $1/sC_O$ and output resistance R_O . Diode current i_D is the product of i_L and d_M' so its linearized small-signal counterpart varies with both i_l and i_{dm} :

$$i_d = i_l \left(\frac{\partial i_d}{\partial i_l} \right) + d_m \left(\frac{\partial i_d}{\partial d_m} \right) = i_l D_M' - d_m I_L, \quad (5.7)$$

where D_M' and I_L are the dc off duty cycle $(1-D_M)$ and inductor current, respectively, the latter of which is equivalent to I_O/D_M' or $I_O/(1-D_M)$. Note the feed-forward component is $d_m I_L$, which is out of phase with i_l (Fig. 5.6(c)).

Because two current-loop current components $i_l D_M'$ and $d_m I_L$ are fed to Z_O (Fig. 5.6(c)), closed-loop current gain $A_{I,CL}$ (from i_{mv} to i_d) is comprised of the closed-loop gain to i_l and d_m and their translation to i_d :

$$A_{I,CL}|_{f \gg p_{LPF}} = \left(\frac{i_l}{i_{mv}} \right)_{CL} D_M' - \left(\frac{d_m}{i_{mv}} \right)_{CL} I_L = \left(\frac{i_l}{i_{mi}} \right)_{CL} \left(D_M' - \frac{L_S I_L}{V_O} \right), \quad (5.8)$$

where

$$\left(\frac{i_l}{i_{mi}} \right)_{CL} = \frac{A_{OL}}{1 + |LG_I|} = \frac{R_S M \left(\frac{V_O}{L_S} \right)}{1 + R_I g_{mi} R_S M \left(\frac{V_O}{L_S} \right)} \approx \frac{1}{R_I g_{mi}}, \quad (5.9)$$

where A_{OL} is the forward gain from i_{mi} to i_l and a RHP zero results in equation (5.8) when feed-forward component $L_S I_L/V_O$ just exceeds D_M' , which happens at $D_M' V_O / 2\pi L I_L$ (z_{RHP}).

The compensated voltage loop gain ($|LG_V|$) is therefore

$$\begin{aligned} |LG_V|_{f \gg p_{LPF}} &= g_{mv} A_{I,CL}|_{f \gg p_{LPF}} \left(R_O \parallel \frac{1}{sC_O} \right) \\ &\approx g_{mv} \frac{D_M' - \frac{L_S I_L}{V_O}}{R_I g_{mi}} \left(R_O \parallel \frac{1}{sC_O} \right) \Big|_{f > p_O} \approx \frac{g_{mv} \left(D_M' - \frac{L_S I_L}{V_O} \right)}{R_I g_{mi} sC_O}, \end{aligned} \quad (5.10)$$

where the loop has a single pole at p_O or $1/2\pi R_O C_O$, z_{RHP} remains, and its unity-gain frequency is at

$$f_{0dBV} \approx \frac{g_{mv} D_M'}{2\pi R_I g_{mi} C_O}. \quad (5.11)$$

Assuming that the pole introduced by the current loop at $f_{0\text{dBI}}$ is well beyond $f_{0\text{dBV}}$, z_{RHP} needs to be above $f_{0\text{dBV}}$ giving the first stability condition for the system:

$$z_{\text{RHP}} = \frac{D_M' V_O}{2\pi L I_L} > f_{0\text{dBV}} \approx \frac{g_{\text{mv}} D_M'}{2\pi R_{\text{Igmi}} C_O} \quad (5.12)$$

or

$$\frac{L I_L}{V_O C_O} = \frac{L I_O}{C_O V_O D_M'} < \frac{R_{\text{Igmi}}}{g_{\text{mv}}}. \quad (5.13)$$

Consequently, for the closed-current-loop expression used ($1/R_{\text{Igmi}}$) to remain valid through $f_{0\text{dBV}}$, the unity-gain frequency of the current loop ($f_{0\text{dBI}}$) must well exceed $f_{0\text{dBV}}$, providing the second stability condition:

$$f_{0\text{dBI}} \approx \frac{R_{\text{Igmi}} R_S M V_O}{2\pi L} \gg f_{0\text{dBV}} \approx \frac{g_{\text{mv}} D_M'}{2\pi R_{\text{Igmi}} C_O}. \quad (5.14)$$

The linearized modulator gain M can be estimated by recognizing that the converter switching frequency in this self-oscillating $\Sigma\Delta$ controller corresponds to $f_{0\text{dBI}}$ when inequality (5.14) is satisfied or in other words, the current-ripple dominates in v_{SUM} . Then, the switching frequency given by

$$f_{\text{sw}} = \frac{g_{\text{mi}} R_S R_I}{\frac{V_H}{|di/dt|_{\text{on}}} + \frac{V_H}{|di/dt|_{\text{off}}}} = \frac{g_{\text{mi}} R_S R_I}{L} \left(\frac{V_{\text{IN}} (V_O - V_{\text{IN}})}{V_O V_H} \right), \quad (5.15)$$

where V_H is the width of the comparator hysteresis window, is equated to $f_{0\text{dBI}}$ to give

$$M \propto \frac{V_{\text{IN}} (V_O - V_{\text{IN}})}{V_O^2 \cdot V_H} = \frac{D_M D_M'}{V_H}. \quad (5.16)$$

The last stability condition is for the LPF pole p_{LPF} to remain low enough to ensure LG_I exceeds unity below the RHP zero thereby closing the current loop and masking the effects of said zero. This low frequency LPF pole, because it slows the response time of the effective inductor current reference (v_{IREF}) and therefore its ability to converge on the average output load current (I_O), delays the response of the system and degrades transient response [47].

Time Domain Perspective of Stability Analysis

In a boost dc-dc converter, the inductor current increases with an increase in the duty cycle of switch S_M , because an increased duty cycle implies a higher average voltage across the inductor. This increased current reaches steady state by correspondingly increasing the output voltage v_O to maintain volt-second balance. This increase in the output voltage is brought about due to a higher diode current i_D , which is the portion of the inductor current that flows to the output when switch S_M is off. As a result while the inductor current increases with duty-cycle, the converter temporarily experiences conditions where the inductor current is still not high enough to support the load current, but the output capacitor is being discharged for a longer time by the load current I_O during the increased on-time of switch S_M . Thus, for a fast increase in duty cycle, the output voltage actually decreases before it starts increasing and vice-versa for a fast decrease in duty cycle. This phenomenon, represented by a RHP zero in the frequency domain [20] as seen earlier, leads to positive gain in the voltage loop at fast enough duty changes. This is seen in steady state as a voltage ripple that is out of phase with the duty cycle d_M (Fig. 5.7).

On the other hand, the inductor current always increases with increasing duty cycles either for slow or fast changes. Hence, a negative feedback current loop is easily

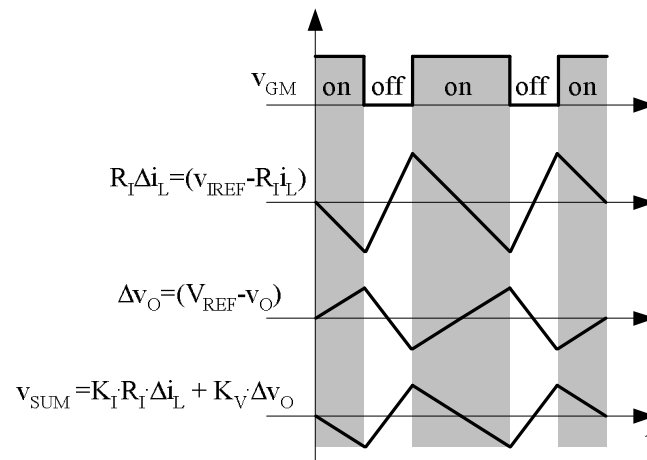


Fig. 5.7. Time domain representation of $\Sigma\Delta$ control where the ripple in the summed voltage v_{SUM} is dominated by the sensed current $R_I i_L$, suppressing the ripple in the sensed output voltage.

stabilized. As before, this positive gain between duty and current is seen as an in-phase current ripple (Fig. 5.7). Given this background, the $\Sigma\Delta$ converter sums the scaled inductor and output voltage ripples in such a way that the inductor current ripple dominates the net sum. By doing this, the right-half plane zero is not eliminated, but its effect is not seen in the loop because it is overwhelmed by the stabilizing effect of the inductor current. Essentially, therefore, the requirement of stability is that the scaled sensed-inductor current ripple exceeds the scaled sensed-output voltage ripple, which can be analyzed to yield a condition similar to that in equation (5.13).

5.2.2. Steady-State Error

To regulate DC output voltage V_O , the $\Sigma\Delta$ loop controls combined parameter v_{SUM} , whose steady-state value is unaffected by the current loop, with a hysteretic comparator (Fig. 5.5). Including the switching effects of delays t_{d_ON} and t_{d_OFF} in the turn-on and turn-off of switch S_M extends the ripple in v_{SUM} (assumed linear) beyond the boundaries set by the hysteresis window (H) (Fig. 5.8). The average of the resulting triangular signal sets the steady-state accuracy of the circuit [57].

As observed in Fig. 5.8, steady-state accuracy is worst (average value of v_{SUM} , viz. V_{SUM} , is not zero) when the rising-to-falling slopes ratio is high:

$$\begin{aligned} V_{SUM} &= \frac{\frac{H}{2} + S_{err+} + \left(-\frac{H}{2} - S_{err-}\right)}{2} \\ &= \frac{1}{2} (M_1 t_{d_ON} - M_2 t_{d_OFF}), \end{aligned} \quad (5.17)$$

where M_1 and M_2 are the rising and falling slopes of v_{SUM} . Assuming K_I at the switching frequency (K_{I_fsw}) is designed to be considerably greater than K_V (K_{V_fsw}) and delays t_{d_ON} and t_{d_OFF} are equal to t_d , equation (5.17) simplifies to

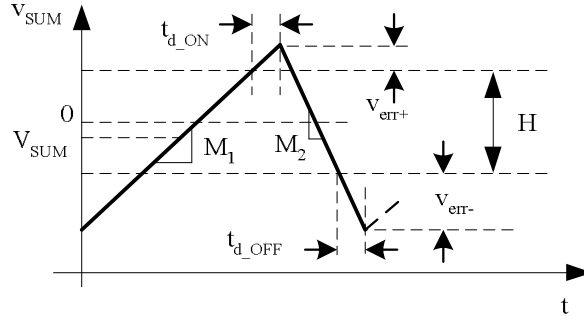


Fig. 5.8. Effect of switching delays on regulated variable v_{SUM} .

$$\begin{aligned}
 V_{SUM} &= \frac{t_d}{2} K_{L_{fsw}} \left(\left| \frac{di}{dt} \right|_{OFF} - \left| \frac{di}{dt} \right|_{ON} \right) \\
 &= \frac{K_{L_{fsw}} t_d (V_O - 2V_{IN})}{2L},
 \end{aligned} \tag{5.18}$$

and equating to the low frequency form of v_{SUM} , which is

$$V_{SUM} \approx K_{V_{DC}} (V_{REF} - V_O), \tag{5.19}$$

where $K_{V_{DC}}$ is the DC version of K_V , which is assumed to be greater than $K_{L_{DC}}$ at low frequencies as dictated by design, indicates DC error voltage V_{err} increases with increasing $K_{L_{fsw}}$ and t_d and decreases with $K_{V_{DC}}$ and L :

$$V_{err} = V_O - V_{REF} = \left(\frac{K_{L_{fsw}}}{K_{V_{DC}}} \right) \left(\frac{t_d}{2L} \right) (2V_{IN} - V_O). \tag{5.20}$$

Arbitrarily decreasing K_I and increasing K_V to reduce V_{err} compromises the stability condition stated in equation (5.13). Equation (5.20) suggests a small switching-frequency value of K_I and a large dc value of K_V for low steady-state error. The error is the worst at the smallest inductor value in a variable LC environment. The switching ripple is inversely dependent on the output capacitance and switching frequency, which, for a well-designed converter, is approximately equal to f_{0dBI} .

5.2.3. Switching Frequency

Switching frequency f_{sw} is a function of the times it takes v_{SUM} to traverse hysteresis window H both in the up and down directions. Since the rising and falling rates

of inductor current i_L are set by the application (V_{IN} , V_O , and $1/L$), switching frequency f_{SW} is inversely proportional to the hysteretic window H , L , and parasitic S_M delay times t_{d_ON} and t_{d_OFF} . From inspection (Fig. 5.8), the off and on times (t_{OFF} and t_{ON}) of switch S_M are governed by the rising and falling rates of v_{SUM} , hysteresis window H , and delay times t_{d_ON} and t_{d_OFF} [57]:

$$t_{OFF} = \frac{H}{|M_1|} + \frac{V_{err-}}{|M_1|} + t_{d_ON} \quad (5.21)$$

and

$$t_{ON} = \frac{H}{|M_2|} + \frac{V_{err+}}{|M_2|} + t_{d_OFF}. \quad (5.22)$$

Assuming as before that t_{d_ON} and t_{d_OFF} equal t_d and K_I is considerably greater than K_V at the switching frequency, f_{SW} simplifies to

$$f_{SW} = \frac{1}{t_{OFF} + t_{ON}} = \frac{V_{IN} (V_O - V_{IN})}{V_O^2 \left(t_d + \frac{HL}{V_O K_{I_f_{SW}}} \right)} \propto K_{I_f_{SW}}. \quad (5.23)$$

Switching frequency f_{SW} decreases for any increase in input voltage V_{IN} beyond $V_O/2$, and since t_d is normally small, with increasing inductance values. A change in the switching frequency can be partially offset by varying K_I inversely with frequency, the net result of which is negative feedback with respect to frequency (K_I attempts to increase f_{SW} when f_{SW} decreases as a result of any other parameter change).

5.3. System Simulations

The main feature of the foregoing design is LC compliance and key design parameters for stability, regulation, and frequency performance are voltage and current gains g_{mv} and $R_{Ig_{mi}}$. The primary objectives of the proposed design are for g_{mv} (K_V) to exceed $R_{Ig_{mi}}$ ($R_I K_I$) at low frequencies to reduce steady-state dc errors in v_O and $R_{Ig_{mi}}$ to exceed g_{mv} at moderate-to-high frequencies to shift f_{0dBI} (f_{SW}) above f_{0dBV} and in the process turn i_L into a current source in the voltage loop masking the effects of the LC

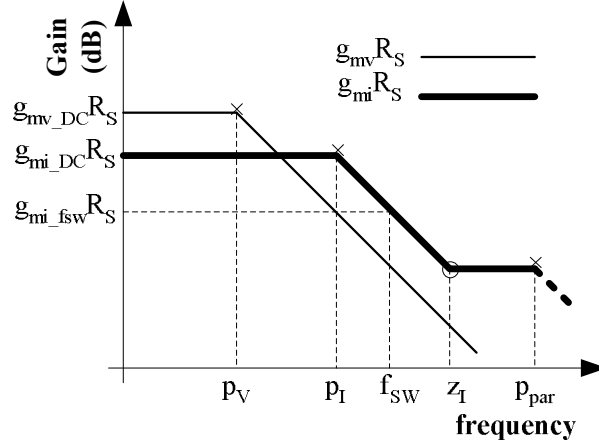


Fig. 5.9. Frequency-dependent voltage and current gains g_{mv} and g_{mi} .

Table 5.1. Dual-mode system design parameters.

Parameter	Value	Parameter	Value
V_{IN}	2.7–4.2V	V_O	$5 \pm 5\% V$
C_O	15–350 μ F	L	1–30 μ H
K_{V_DC}	40V/V	p_v	7.5kHz
K_{I_DC}	10 V/V	K_{I_HF}	2.5V/V
p_i	160kHz	z_i	800kHz
p_{par}	10MHz	I_O	0.1–1A

complex-conjugate pole pair and RHP zero. Another design goal is to make g_{mi} inversely proportional to frequency below and near f_{0dbI} (f_{SW}) by means of pole p_i as shown in Fig. 5.9, to compensate partially for switching frequency variations, without resorting to additional frequency-regulating loops. The pole p_i that constitutes a second pole in the current loop in addition to that in G_I , is compensated by the zero z_i . Fig. 5.9 illustrates the proposed frequency-dependent current and voltage gains g_{mi} and g_{mv} , Table 5.1 describes the operating conditions and design parameters of the simulated converter targeted for a 2.7–4.2V Li-Ion input, and a 5V–1A. To validate the operation of the proposed technique and to compare its performance under identical operating conditions with state-of-the-art sigma-delta boost converters, circuit simulations were performed using the simulator Spectre™, which is a part of the Cadence suite.

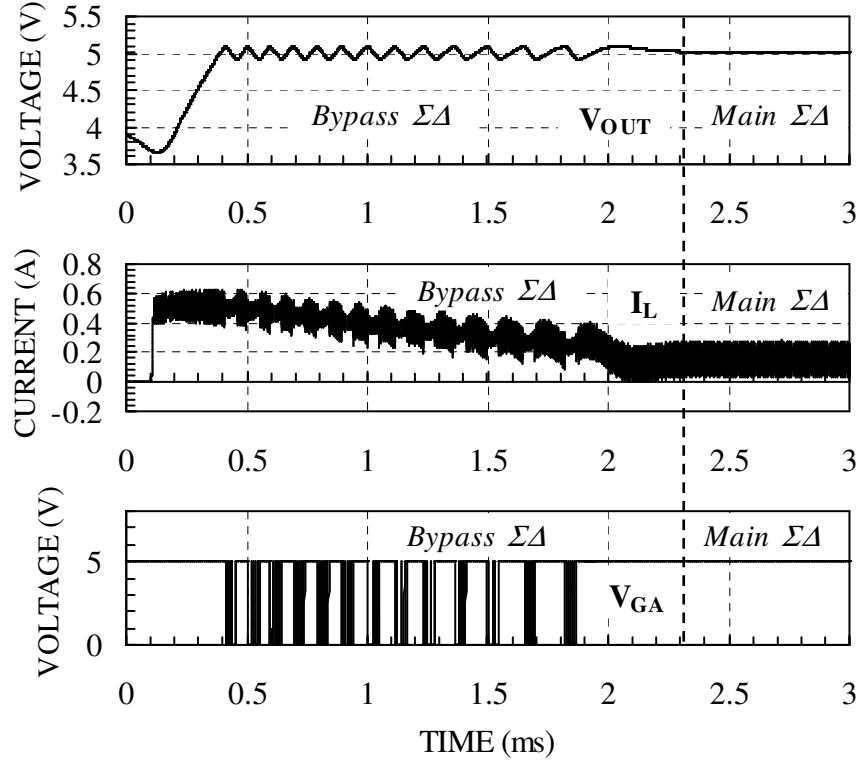


Fig. 5.10. Mode transition and steady-state waveforms of the proposed dual-mode $\Sigma\Delta$ converter solution for $L=5\mu\text{H}$, $C=47\mu\text{F}$, and $I_O=0.1\text{A}$.

5.3.1. Steady-State and Mode Transition

Steady-state waveforms of the proposed circuit where L is $5\mu\text{H}$, C is $47\mu\text{F}$, and I_O is 0.1A , are shown in Fig. 5.10. It is seen that the circuit starts as a dual $\Sigma\Delta$ loop converter with an output voltage ripple of $\pm 100\text{mV}$ ($\pm 2\%$ of V_O). At this time, the inductor current is in excess of the minimum required inductor current. During mode transition, the excess inductor current gradually decreases and finally disappears, and the circuit transitions to the main $\Sigma\Delta$ mode or steady state. This is also seen in terms of switch S_A that diverts excess current in the bypass mode. The duty cycle of switch S_A reduces gradually with decreasing inductor current until finally the gate voltage v_{GA} (active low) stops pulsing as the circuit enters main $\Sigma\Delta$ loop mode. The steady-state voltage ripple is approximately $\pm 0.2\%$.

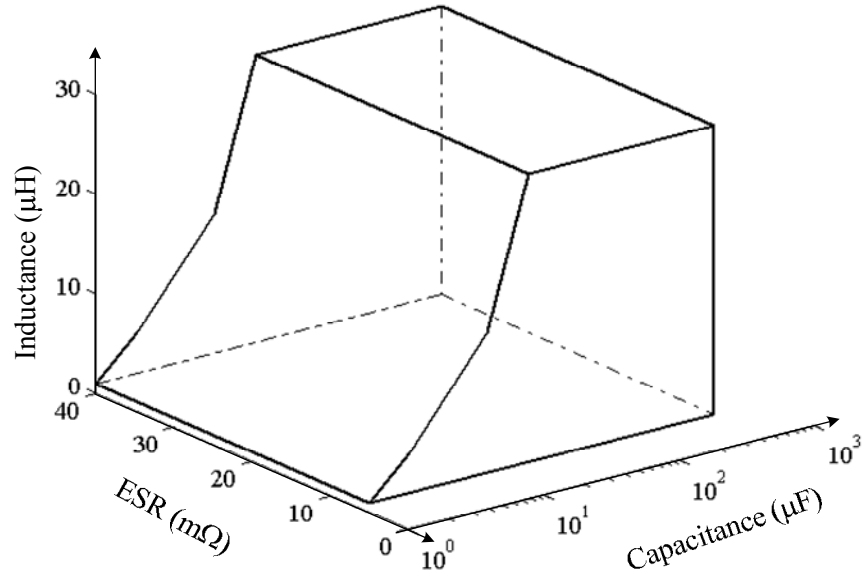


Fig. 5.11. 3-D volume of stability for the proposed dual-mode $\Sigma\Delta$ converter.

5.3.2. $R_{ESR}LC$ Stability Space

Fig. 5.11 illustrates the volume space for which the converter was verified to be stable by subjecting the circuit to 0.1-0.8A load steps. As the filter inductance increases, the filter LC double-pole and more importantly, the right-half plane (RHP) zero moves to lower frequencies as seen from equation (5.8). In addition, the unity-gain frequency of the current loop, being inversely proportional to L , also decreases. As a result, for stability conditions to prevail as derived earlier, the filter capacitor C_O has to increase correspondingly to lower the unity-gain frequency of the voltage loop below the RHP zero and the unity-gain frequency of the current loop. As a result, the minimum, stable filter capacitance increases with increasing L . The maximum simulated capacitance was limited to 350 μ F as a practical limit in portable applications. Under these conditions, the LC stability space was (1-350 μ F, 1-30 μ H, 5-40m Ω).

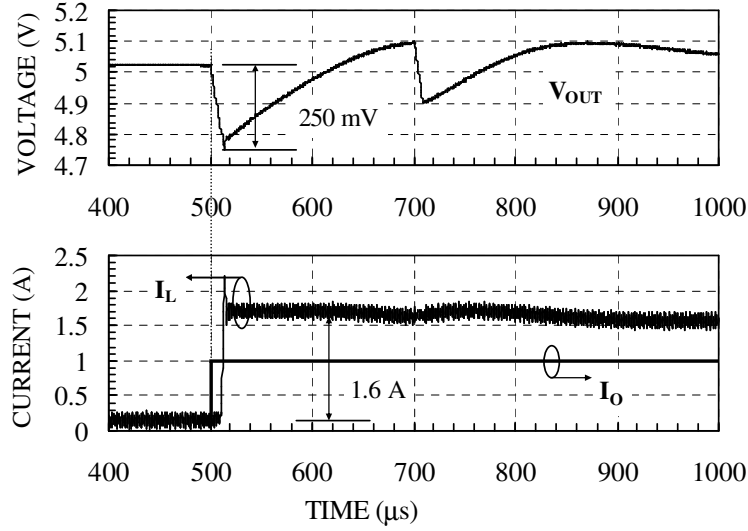


Fig. 5.12. Load-step transient waveforms of the proposed dual-mode converter for $L = 5\mu\text{H}$, $C_O = 47\mu\text{F}$, and $I_O = 0.1\text{-}1\text{A}$.

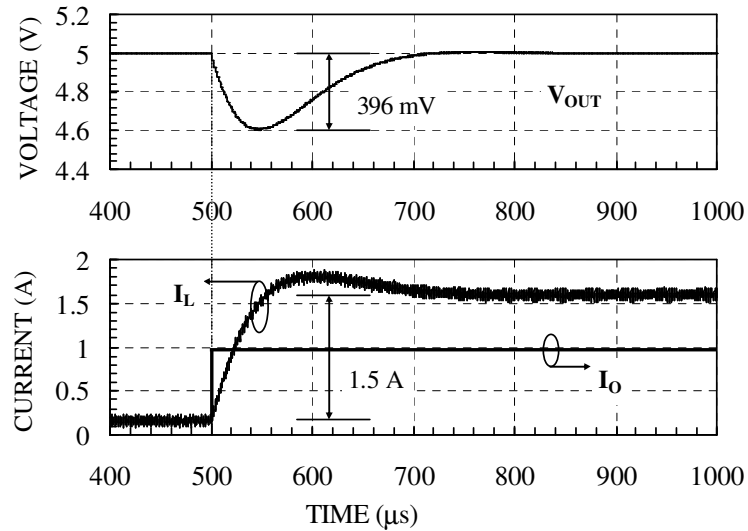


Fig. 5.13. Load-step transient waveforms of the proposed $\Sigma\Delta$ converter without the bypass mode for $L = 5\mu\text{H}$, $C_O = 47\mu\text{F}$, and $I_O = 0.1\text{-}1\text{A}$.

5.3.3. Load Transient Response

Load transient waveforms for the proposed dual-mode circuit with the above LC values and a load step from 0.1 to 1A, at $V_{IN}=3.3\text{V}$ are shown in Fig. 5.12. In response to the load step, the inductor current i_L rises in a single switching cycle, limited only by its slew rate until it reaches 1.7A. A fast voltage transient with a voltage drop ΔV of 250mV and a short transient time of 83μs is observed. In comparison, the transient response of

the converter without the bypass mode is limited by the bandwidth of the feedback network giving a multiple-cycle transient response. Load step response for this $\Sigma\Delta$ loop converter under identical conditions is shown in Fig. 5.13. As was mentioned earlier, a single $\Sigma\Delta$ loop controller has the highest bandwidth and therefore the fastest response for the lowest stable value of the current/voltage gain ratio K_I/K_V . For the waveforms in Fig. 5.13, the gain ratio was adjusted to 0.22, which was the lowest ratio guaranteeing stability at $L = 30\mu\text{H}$, $C = 20\mu\text{F}$, and $R_O = 5\Omega$. Furthermore, the value of the low-pass filter frequency f_{LPF} was designed (2.7kHz) to give an optimally damped response with the smallest voltage transient. Under these conditions, the voltage transient for a load step of 0.1 to 1 A was observed to be 396mV with a transient time of 175 μs . Thus, the proposed converter shows an improvement of 146mV (36 %) in the voltage transient, i.e., transient accuracy.

5.3.4. Steady-State Accuracy

As seen from equation (5.20) and the associated analysis, the inaccuracy in the regulated steady-state voltage increases as the regulated ripple v_{SUM} becomes more and

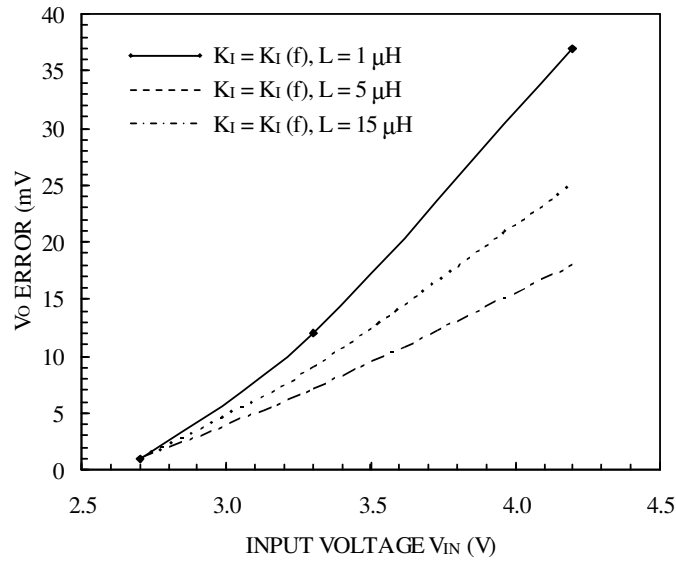


Fig. 5.14. Variation of steady-state V_O error with input voltage V_{IN} and inductance L .

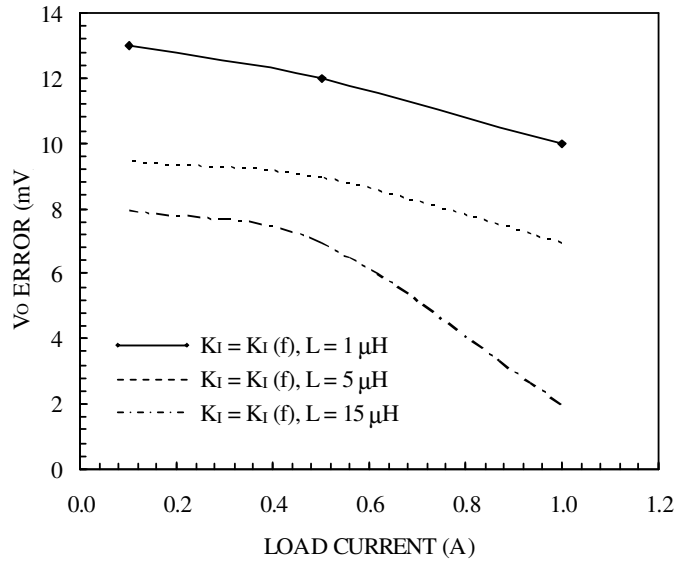


Fig. 5.15. Variation of steady-state V_O error with load current I_O and inductance L .

more asymmetrical. The effects of this asymmetry become evident at lower inductance L values where the slopes of the regulated ripple increase. Any switching delays are amplified by the ripple slopes in the presence of ripple asymmetry. For the simulated converter, the maximum symmetry (nearly 50% duty) occurs at a V_{IN} of 2.7V. Hence, steady-state output-voltage error increases with increasing V_{IN} and decreases with increasing L , as predicted in equation (5.20) and shown in Fig. 5.14, but remains below 1% of V_O . Additionally, the error is consistently positive (sensed output voltage V_S is greater than reference V_{REF}) because V_O is always less than $2 \cdot V_{IN}$, i.e., duty-cycle is always less than 50%. The load regulation – variation of the output voltage with load current, is less than 0.6% (Fig. 5.15); however, the variation shows the same trend as that for line regulation.

5.3.5. Switching-Frequency Variations

Switching frequency f_{SW} decreases with increasing inductance and V_{IN} values, as predicted by Eq. 5.23 and shown in Fig. 5.16. However, since K_I decreases with frequency, the variation in frequency is 15% lower than it would have been with a

constant K_I (Fig. 5.16), which is typically the case in conventional $\Sigma\Delta$ controller circuits. Steady-state variations in load had little impact on either the steady-state error or f_{sw} because the DC voltage gain is relatively high at low frequencies (low DC errors) and low at high frequencies, when the current loop dominates (current loop is virtually unaffected by the load). The switching frequency values themselves are lower at higher inductances since the slopes of the current ripple and hence those of the regulated combined voltage v_{SUM} are less steep. As a second-order variation, the switching frequency is also affected by the changes in the output voltage with line and load variations. For example, in the above simulations, the output voltage increases with increase in the input voltage levels. As a result, the duty cycle and hence the switching frequency of the converter does not decrease as much as they could have. Of course, Figs. 5.16 and 5.17 show frequency variation reductions taking into account this effect (i.e. over and above this effect).

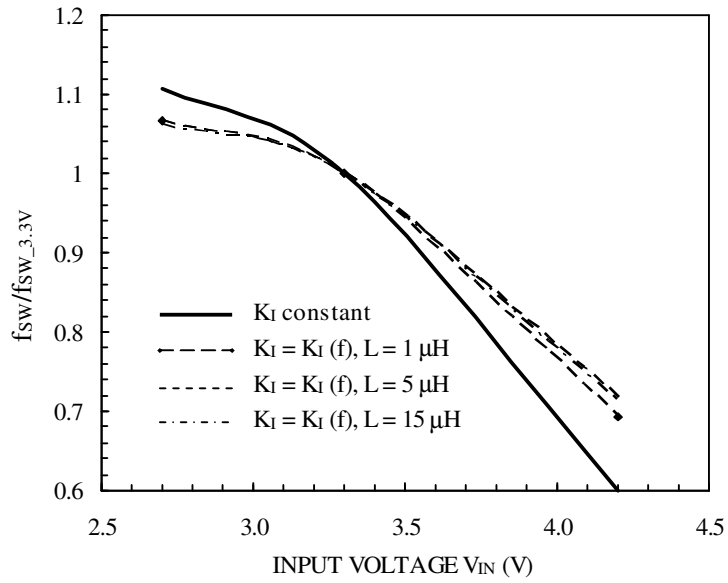


Fig. 5.16. Switching frequency versus input voltage V_{IN} (normalized to its value at 3.3V).

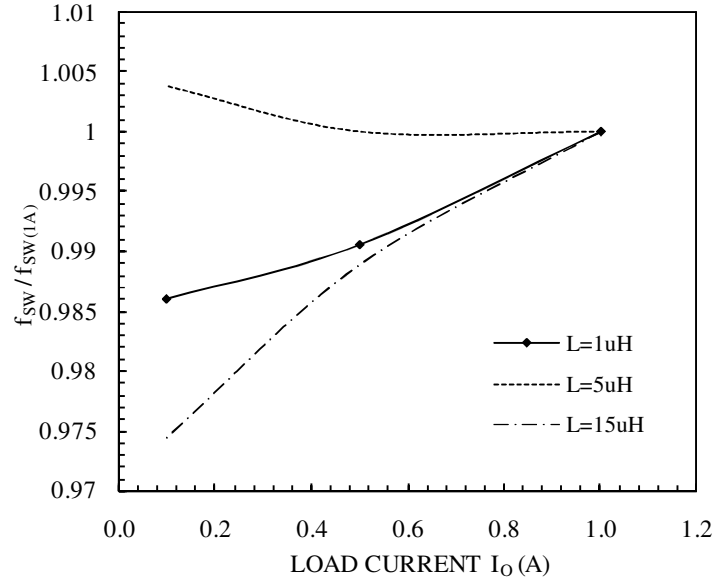


Fig. 5.17. Switching frequency (normalized to its value at 1A) versus load current I_O .

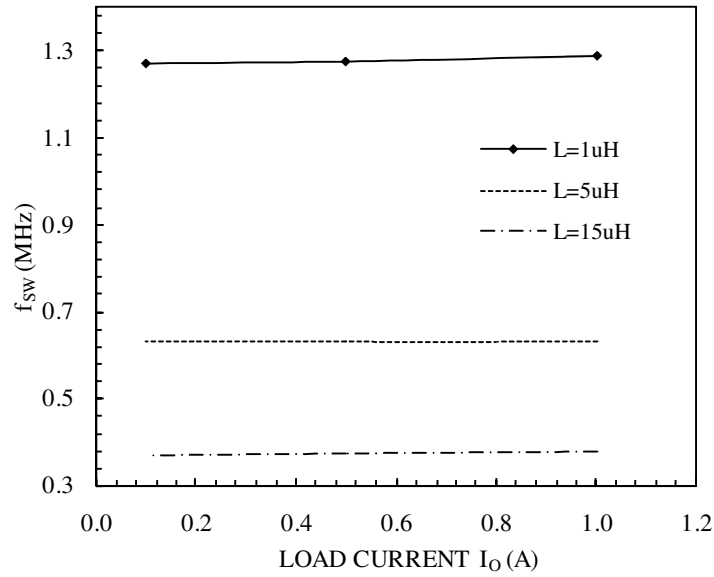


Fig. 5.18. Switching frequency versus load current I_O (absolute values).

5.4. Summary

A dual-mode control scheme was presented for boost DC-DC converters, which, in using a high bandwidth bypass mode during transients, gives a widely LC compliant stable response without using a frequency compensation circuit. The transient response of

the presented circuit is relatively unaffected by the bandwidth of the feedback network used for steady state operation, which necessarily has a lower bandwidth to achieve the required filter compliance. Instead, the circuit transient response is limited largely by the power LC filter characteristics – slew rates. Simultaneously, regulation accuracy – dc accuracy and low output voltage ripple ($\pm 0.2\%$) are achieved without any undue reduction in power efficiency or LC compliance, unlike other techniques reported in literature. Switching frequency variations with line and load are reduced by using a frequency dependent gain in the control loop itself, leading to a reduction of over 15% in frequency variation. The proposed technique thus decouples the conflicting requirements of high relative stability and fast transient response in boost DC-DC converters, enabling an optimal, almost fully integrated solution, except the passive LC filter.

CHAPTER 6

SINGLE-MODE SIGMA-DELTA ($\Sigma\Delta$) BOOST CONTROLLER IC

The dual-mode control technique that regulates the inductor current and output voltage in independent control loops, gives both the LC-compliance and fast transient response was proposed and described in the last chapter. The next two chapters elucidate the integrated circuit (IC) implementation of the proposed sigma-delta control. This chapter describes the design considerations, transistor-level circuits, and layout considerations for an integrated version of the main mode or steady-state operating mode of the dual-mode control technique. The primary objective of this IC was to verify the operation of the circuit blocks in a simpler implementation of the system and to quantify and improve its performance through any required circuit/layout modification for the second and final IC implementation.

6.1. Converter System Description

6.1.1. Design Considerations

As explained in the previous chapter, the main feature of the proposed design is LC compliance and key design parameters for stability, regulation, and frequency performance are voltage and current gains g_{mv} and $R_I g_{mi}$. The primary objectives of the proposed design are for g_{mv} to exceed $R_I g_{mi}$ at low frequencies to reduce steady-state dc errors in v_O and $R_I g_{mi}$ to exceed g_{mv} at moderate-to-high frequencies to shift f_{0dBI} (f_{SW}) above f_{0dBV} and in the process turn i_L into a current source in the voltage loop masking the effects of the LC complex-conjugate pole pair and RHP zero. Another design goal is to make g_{mi} inversely proportional to frequency below and near f_{0dBI} (f_{SW}) by means of pole p_I (Fig. 6.1) to compensate partially for switching frequency variations, without resorting to additional frequency-regulating loops. The pole p_I that constitutes a second

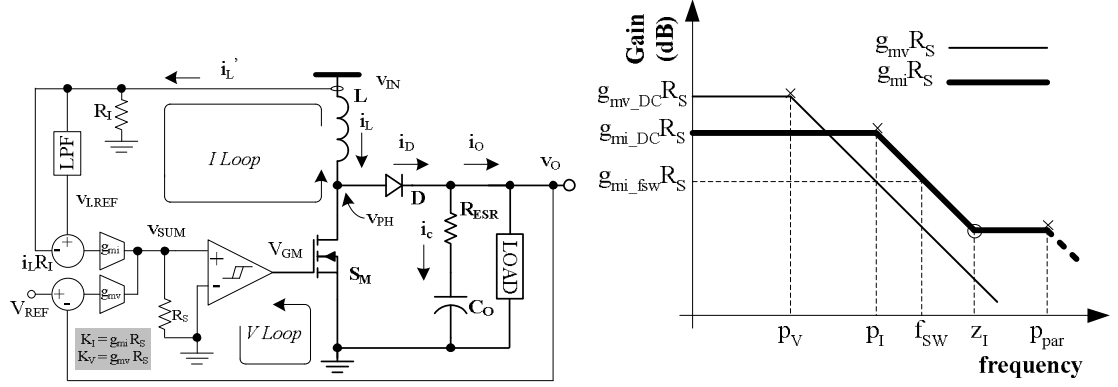


Fig. 6.1. (a) Simplified schematic representation of current and voltage mixing in the $\Sigma\Delta$ boost converter IC in steady state and (b) frequency-dependent voltage and current gains g_{mv} and g_{mi} .

Table 6.1. System Design Parameters

Parameter	Value	Parameter	Value
V_{IN}	2.7–4.2V	V_O	$5 \pm 5\%V$
C	15–350 μ F	L	1–30 μ H
K_{V_DC}	40V/V	p_V	7.5kHz
K_{I_DC}	10V/V	K_{I_HF}	2.5V/V
p_I	160kHz	z_I	800kHz
p_{par}	10MHz	I_O	0.1–0.8A

pole in the current loop in addition to that in G_I , is compensated by the zero z_I . Fig. 6.1 illustrates the proposed frequency-dependent current and voltage gains g_{mi} and g_{mv} . Table 6.1 describes the operating conditions and design parameters of the targeted 2.7-4.2V Li-Ion powered, 5V-0.8A output supply.

High-frequency switching converters involve fast current and voltage transients caused by the switching activity of switches in the power stage and their gate drivers. In conjunction with parasitic capacitances at the switching nodes and parasitic inductances in the power supply V_{DD} and ground lines, the switching voltage and current transients produce noise currents and voltages respectively. In standard PWM converters, this high-frequency noise is filtered out of any processed signals by suitably filtering out frequencies higher than, typically, not more than a fifth of the switching frequency. However, since the feedback in the proposed $\Sigma\Delta$ controller necessarily includes high-bandwidth signals with harmonic components exceeding the switching frequency, such

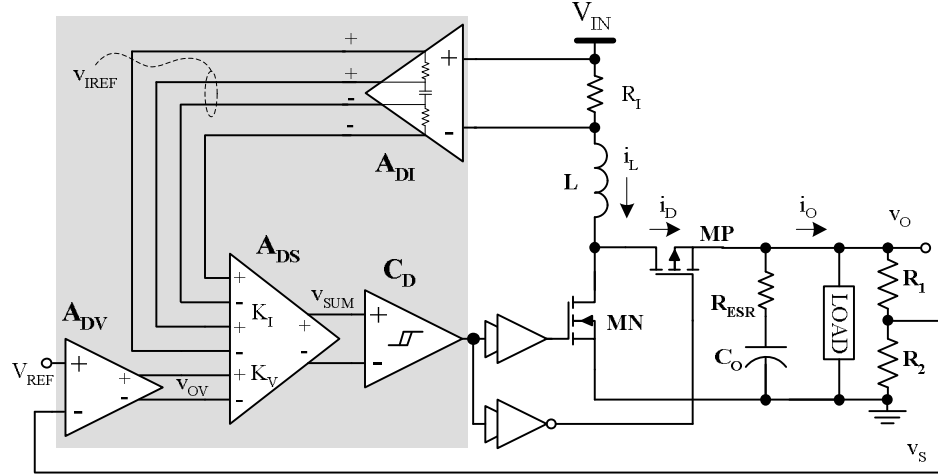


Fig. 6.2. Differential $\Sigma\Delta$ boost converter system.

filtering cannot be employed and the circuit must be tolerant to switching (supply and ground) noise, which is why a differential controller is proposed (Fig. 6.2). Inductor current, sensed through sense-resistor R_I , is amplified by amplifier A_{DI} whose differential output is internally low-pass filtered through an RC filter to generate a second output, viz., self-referenced signal v_{IREF} . The ripple in the sensed output voltage is amplified by amplifier A_{DV} , which also introduces pole p_v in the voltage path. The outputs of amplifiers A_{DI} and A_{DV} are then mixed by summing amplifier A_{DS} whose output is ultimately modulated into the duty-cycle of switches MN and MP by hysteresis comparator C_D . In this IC prototype, the switches and their gate drivers are off-chip, along with the LC filter elements.

6.1.2. IC Design

State-of-the-art $\Sigma\Delta$ controllers [51] employ high loop-gain, op-amp based, closed-loop amplifiers to accurately scale the gains of the sensed variables. Such closed loop structures are required for accuracy of gains. Besides being susceptible to supply and ground noise, given their signals are single-ended, the switching frequency is limited by the speed of the controller, which is in turn set by the op amp's bandwidth. Current-mode processing based on current-conveyors [52] improves the bandwidth by reducing the

number of high-impedance nodes and their associated voltage swings, but their vulnerability to noise, although somewhat improved, is still limited to the capabilities of single-ended processing schemes.

The presented controller implements a differential circuit where the feedback loop is closed around a single transistor and its source degenerating resistor, thereby allowing high bandwidth operation. In addition, the complexity associated an output common-mode feedback circuit is eliminated. The proposed system, designed in a 0.5μ double-poly, CMOS process with poly-poly capacitor ($1\text{fF}/\mu^2$) and high-resistance poly ($1\text{k}\Omega/\square$) options, also shows that the open-loop gain can be reduced to achieve high bandwidth without incurring a significant tradeoff in accuracy.

A. Basic Source-Degenerated Amplifier Structure

Transistor source degeneration by means of explicit source impedance introduces series-series feedback wherein the source current of the degenerated transistor is sensed in terms of the voltage across the degenerating impedance. This voltage is also effectively series mixed with the transistor gate-source input to close the feedback loop. Thus, with high enough feedback gain, the degenerative feedback loops regulates the transistor source current as seen below.

The source-degenerated input transistor MNI produces an ac drain current i_d that is folded through cascode PMOS transistor MPC to the output resistor R_2 , generating the amplified output voltage v_o . The ac gain of this circuit is

$$A = \frac{v_{so}}{v_{si}} = \frac{R_2}{R_1} \left(\frac{g_m R_1}{1 + g_m R_1} \right) \equiv \frac{R_2}{R_1} (K), \quad (6.1)$$

where g_m is the transconductance of MNI. Since the ratio R_2/R_1 can be designed with very high accuracy ($< 0.5\%$) the net accuracy of A across process and temperature variations is determined through the sensitivity of K to small, and in the worst case, uncorrelated variations in the g_m and R_1 :

$$K + \Delta K = \frac{(g_m + \Delta g_m)(R_1 + \Delta R_1)}{1 + (g_m + \Delta g_m)(R_1 + \Delta R_1)} \approx K + \frac{\Delta g_m R_1 + \Delta R_1 g_m}{(1 + g_m R_1)^2}, \quad (6.2)$$

where Δg_m and ΔR_1 are small variations in g_m and R_1 respectively, and second order terms are ignored. Therefore the relative sensitivity of K is

$$\frac{\Delta K}{K} \approx \frac{1}{1 + g_m R_1} \left(\frac{\Delta g_m}{g_m} + \frac{\Delta R_1}{R_1} \right). \quad (6.3)$$

Equation (6.3) confirms that the term $g_m R_1$, which is the open loop gain of the source-degenerating MNI- R_1 series feedback loop, suppresses the variations in i_d from those in its determining terms g_m and R_1 . As a result, by appropriately increasing the value of $g_m R_1$, a desired accuracy specification for gain A (e.g., $\pm 10\%$), can be met. In the limit, when the loop gain $g_m R_1$ is much greater than unity, K tends to a constant value of unity and $A \approx R_2/R_1$.

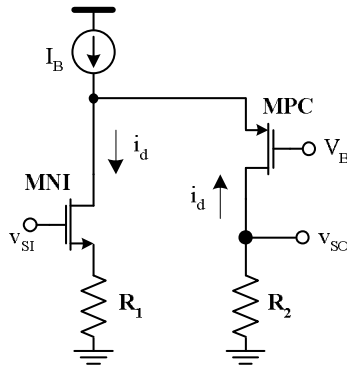


Fig. 6.3. Basic source-degenerated amplifier structure.

The MNI- R_1 loop that determines i_d , has high bandwidth limited only by the product of R_1 and the parasitic diffusion capacitance at the source of MNI. The pole at the other relatively high-resistance node i.e., the output node, is also at a high frequency because the cascode transistor MPC is designed with almost the minimum drawn length, keeping its drain capacitance small. Overall, a high-bandwidth amplifier can be achieved with a desired level of accuracy. The following sub-sections describe adaptations of the aforementioned circuit to the controller blocks shown in Fig. 6.2.

B. Differential Current-Sense Amplifier (A_{DI})

The amplifier circuit (Fig. 6.4) implements a fully differential version of the basic cell in Fig. 6.3. Accordingly, the effective source-degenerated transconductor MNI+ R_1 from Fig. 6.3 is replaced by a matched differential transconductor (G_R) composed of MN11-12+ R_{11-12} , where the common node v_C is ac-ground. The amplified differential voltage across the resistors R_{21-22} is buffered by the source-follower stages MP31-32, to give the primary differential output v_{IL} . A differential RC filter yields the low-frequency component (v_{ILREF}) of v_{IL} as the sensed current reference. In actuality, the capacitors in the RC filter are implemented using voltage-mode capacitor multipliers [53] to save area. The output common-mode level is naturally set by the DC current flowing through resistors R_{21-22} , and the source-gate voltages of buffer transistors MP31-32, both component pairs being carefully laid out to minimize offsets. As for the other following blocks, the DC gain of current-sense amplifier is designed for an accuracy of $\pm 10\%$ over worst-case PVT corners by appropriate choice of input devices MN11-12 and resistors R_{11-12} .

The poly2 resistor pair R_{11-12} is laid out in a multi-segment, common centroid format [54] with segment width twice the lithographic minimum of $1.5\mu\text{m}$, with identical width dummy segments at the edges of each array. In the AMI $0.5\mu\text{m}$ process, not only does the poly2 resistor have a high sheet resistance and therefore a more compact layout, but its capacitive coupling to the substrate is weak (approximately $60\text{aF}/\mu^2$) thus enabling high (large area) resistances without compromising noise and bandwidth performance. For accuracy in the amplifier gain, resistors R_{11-12} are matched with output resistors R_{21-22} . The resistors and capacitors in the RC filter are also laid out in the common-centroid formations surrounded by dummies.

C. Differential Voltage-Sense Amplifier (A_{DV})

One of the drawbacks of the circuit in Fig. 6.4 is that the input common-mode range (ICMR) is reduced by the additional DC voltage drop across the source-degenerating resistors R_{11-12} . While this is not a concern for the current-sense amplifier whose input common-mode level is close to V_{DD} , it poses a problem for the voltage-sense amplifier whose common-mode input is at the reference voltage ($\sim 1.2\text{ V}$). To improve the ICMR, the tail current is split into two sources I_{T1} - I_{T2} (Fig. 6.5) each half of the original value and the source-degenerating resistors R_{11-12} are relocated so that they do not carry any DC current. The transistor DC biasing currents and the ac equivalent circuit are unchanged with node v_C being ac ground; hence, resistors R_{11-12} provide identical series feedback as described for Fig. 6.3 giving similar amplification.

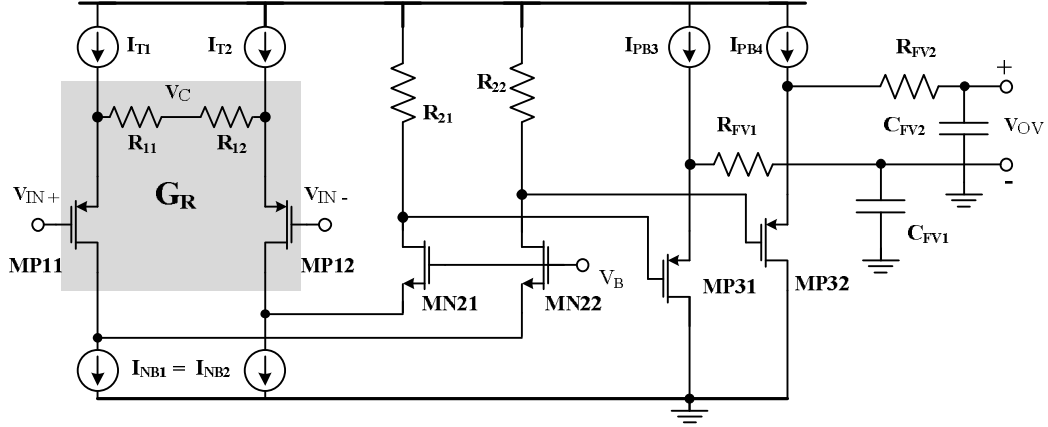


Fig. 6.5. Simplified circuit schematic for the voltage-sense amplifier.

The expected repercussion of splitting the tail current is that the distribution of the bias currents for the input PMOS transistors MP11-12 is now also determined by the tail currents I_{T1} - I_{T2} themselves. As a result, there is an increased possibility of mismatch and therefore, a higher input-referred offset voltage; however, it can still be kept small by careful design and layout as described earlier. Apart from this change in the input stage, the rest of the amplifier design is conceptually the same as in Fig. 6.4, with changed polarities of the input and cascode transistors to meet input common-mode requirements. The body connections of transistors MP11-12 are connected to the ac ground node v_C to reduce the bulk bias effect and any related mismatch. Despite the resulting additional n-well capacitance at the node v_C , the amplifier bandwidth is maintained well within its specifications. An RC filter at the amplifier output introduces the desired pole p_V (Fig. 6.5) in voltage path. As before, the physical filter capacitors are reduced in size by capacitor multipliers.

D. Differential Summing Amplifier (A_{DS})

The summing amplifier is readily realized by combining the output currents of multiple differential transconductors (Fig. 6.6) based on the circuit in Fig. 6.3. Consequently, in the circuit implementation each summed input corresponds to a

differential pair that feeds its output ac current to a common pair of cascode (common-gate) transistors MP21-22. The differential output voltage v_{SUM} across resistors R_{21-22} , by superposition, is

$$v_{SUM} = (i_v + i_{i1} + i_{i2}) Z_S = (G_{RV} v_v + G_{RI} v_{i1} + G_{RI} v_{i2}) Z_S, \quad (6.4)$$

where the $G_{RV, I}$ are the differential transconductances, v_v, i_{i1}, i_{i2} and i_v, i_{i1}, i_{i2} are the input voltage and output current contributions from each input differential pair, and Z_S is the differential impedance looking into the output given by

$$Z_S \approx 2R_{21} \parallel \left(2R_{23} + \frac{1}{sC_2} \right), \quad (6.5)$$

ignoring the impedance looking into the drains of the cascode transistors MP21, 22. The gain from each input to the output is designed by choosing the appropriate source

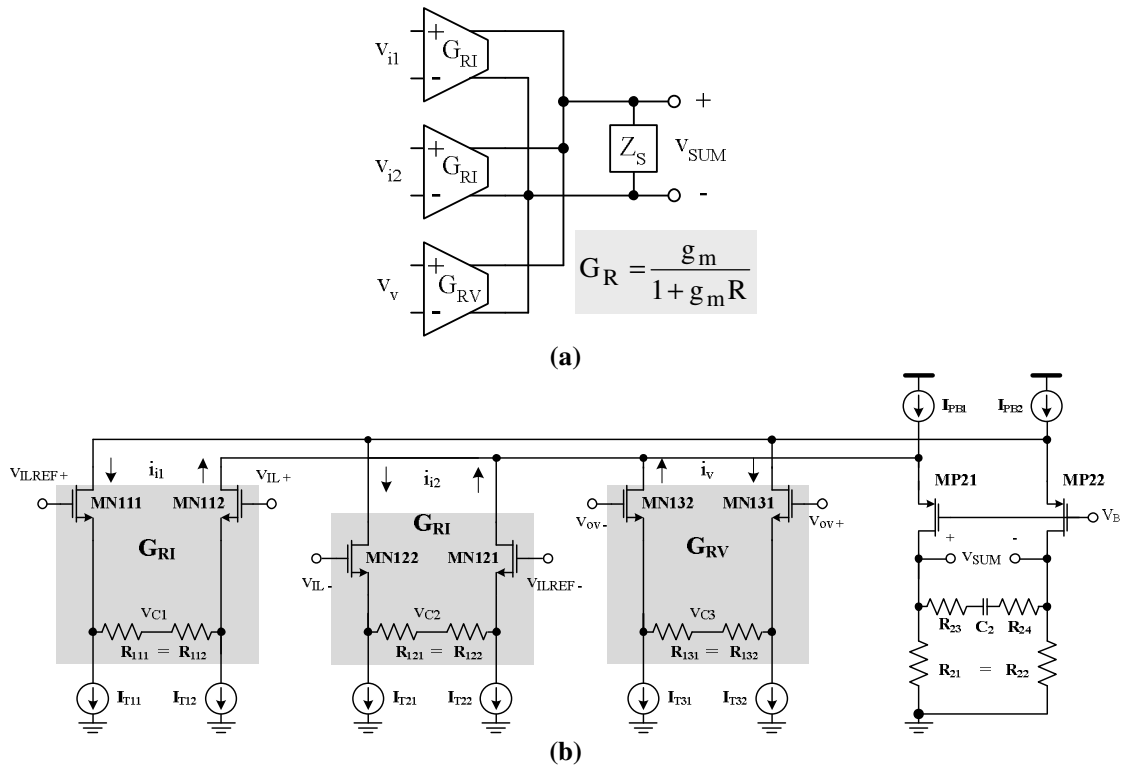


Fig. 6.6. Simplified (a) block diagram and (b) circuit schematic for the summing amplifier

A_{DS} from Fig. 6.2.

Table 6.2. Circuit blocks specifications table summarizing the simulation coverage over variations in process, voltage, and temperature (PVT).

	Component	Parameter	Performance					
			Min	Typ	Max	Worst-Case Sims (min)	Nominal Sims	Worst-Case Sims (max)
1	Current Sense	VDD_MIN (V)			2.7	2.1		2.47
		ICMR (V)	Vdd-0.2		Vdd	1.4		Vdd
	Amplifier	Output DC Level (V)	1.7		2.1	1.83	1.9	2.06
		Vos (mV)	-10		10			
		DC gain (V/V)	7.2	8	8.8	7.35	8.2	8.8
		Dominant pole (MHz)	10			12	16	22
		Ibias (μ A)				125	153	200
2	Current ripple	VDD_MIN (V)			2.7	2.1		2.5
		ICMR (V)	1.2		Vdd	1.2		Vdd
	Transconductor	Output DC Level (V)	1.3		Vdd-0.2	1.74	1.85	1.96
		Vos (mV)	-10		10			
	Part of SUMAMP	DC gain (dB)	25.1	26	26.9	25.39	25.94	26.21
		Parasitic pole (MHz)	10			13	24	35
		Low-pass pole (kHz)	94	150	240	96	150	230
		Low-pass zero (kHz)	470	750	1200	480	750	1200
		Ibias (μ A)				259	264	277
3	Voltage	VDD_MIN (V)			2.7	2.4	2.52	2.6
		ICMR (V)	1.1	1.2	1.3	0		1.35
	Preamplifier	Output DC Level (V)	1.3		Vdd-0.2	1.56	2.3	3.2
		Vos (mV)	-10		10			
		DC gain (V/V)	4.5	5	5.5	4.62	5.14	5.5
		Dominant pole (MHz)	2			3	5	8.3
		Ibias (μ A)				68	82	105
4	Voltage Ripple	ICMR (V)	1.4		Vdd	1.3		Vdd
		Vos (mV)	-25		25			
	Transconductor	DC gain (dB)	17.1	18.1	18.9	17.53	18.1	18.32
		Dominant pole (kHz)	5	8	12.8	5.1	8	12.3
	Part of SUMAMP	Parasitic pole (MHz)	1			5		
5	Hysteretic	VDD_MIN (V)			2.7	1.8		2.52
		ICMR (V)	1.6		Vdd	1.3		Vdd
	Comparator	Vos (mV)	-20		20			
		Hysteresis pk-pk (mV)	117	130	143	125	130	137
		Propagation delay (ns)		25		16	30	43
		Ibias (μ A)				117	141	179

degenerating resistor value based on the earlier analysis for Fig. 6.3.

The inputs to each differential pair are chosen to have the same common-mode value under steady state conditions to reduce body-effect related mismatch. Furthermore, since the differential dc input voltage that represents the amplified dc value of the sensed inductor current can be approximately 1V (for 2.5A peak), appropriate choice of inputs is necessary so as not to violate the input differential range of the summing amplifier input

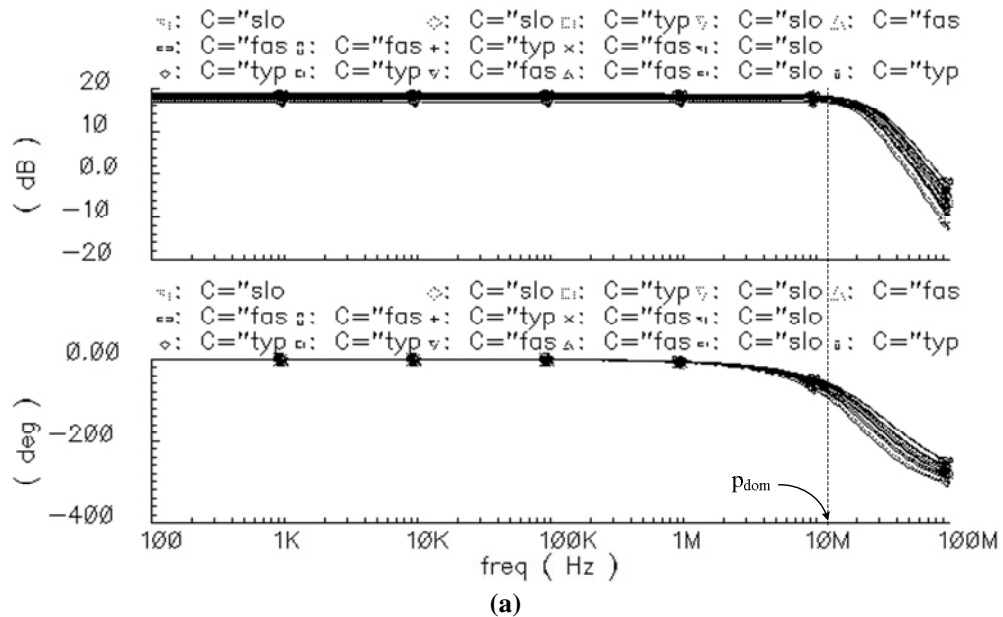
pairs. As such, the second input to a current input pair is simply the average (dc) value of the other input so that the differential input to each pair is amplified current ripple only. In the actual circuit, the summed output v_{SUM} is followed by source follower buffers, but these are omitted for simplicity from Fig. 6.6. The resistors R_{23-24} and capacitor C_2 at the output introduce the pole-zero pair p_I - z_I from Fig. 6.1.

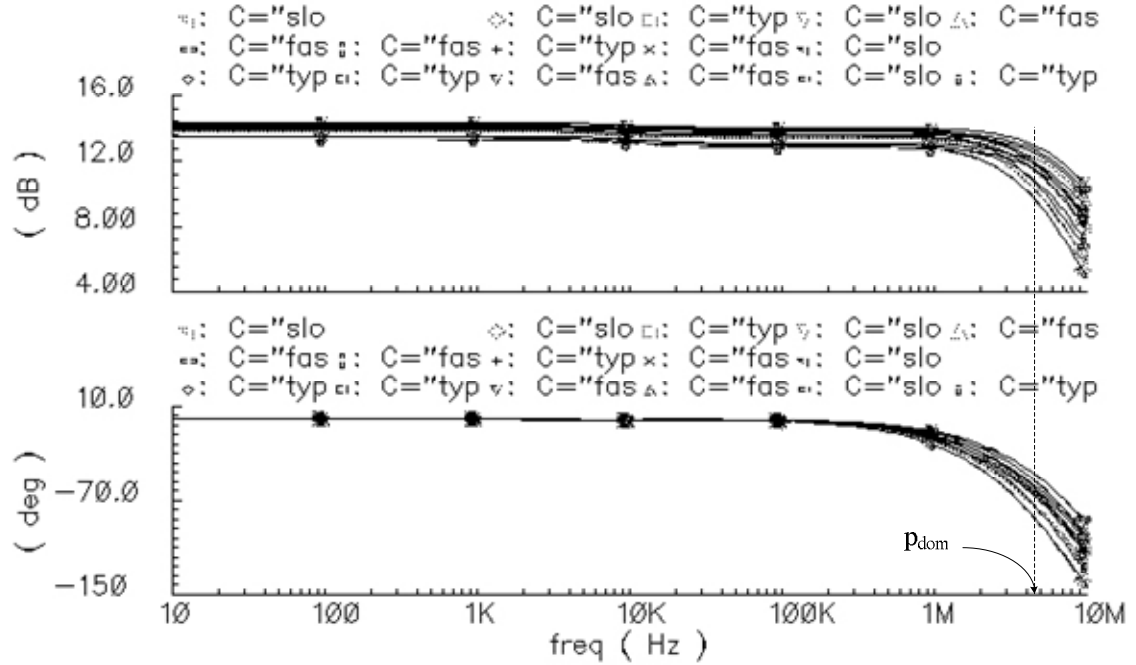
6.2. Circuit Evaluation

6.2.1. Circuit Block Simulations

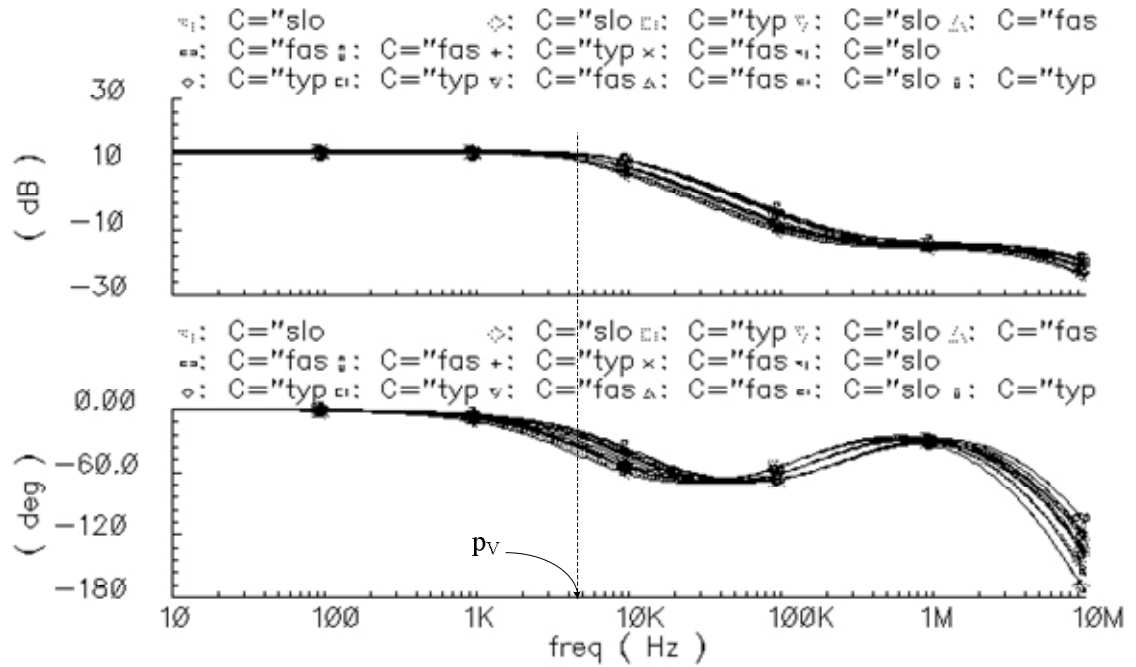
The circuit blocks described earlier were simulated using BSIM2v3 models provided by AMI. Effects of process variations were accounted by including slow, fast, and skew (slow-fast) models for the MOS transistors. Resistors and capacitors were assumed to vary by $\pm 20\%$ and $\pm 15\%$ respectively, in an uncorrelated manner. Temperature was varied from -50°C to 125°C and supply voltage from 2.7V to 4.2V. Under these conditions, the results of the simulation coverage are summarized in Table.

6.2.





(a)



(b)

Fig. 6.8. Simulated frequency response curves for (a) the voltage preamplifier and (b) its version with a low frequency pole over PVT variations.

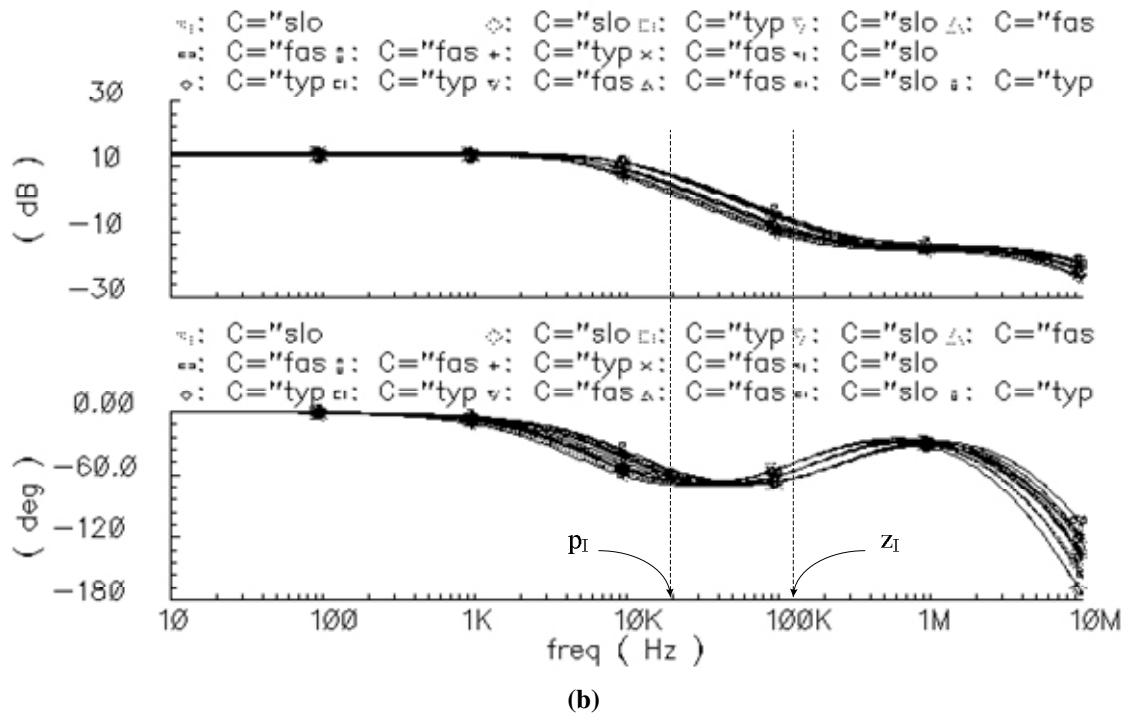
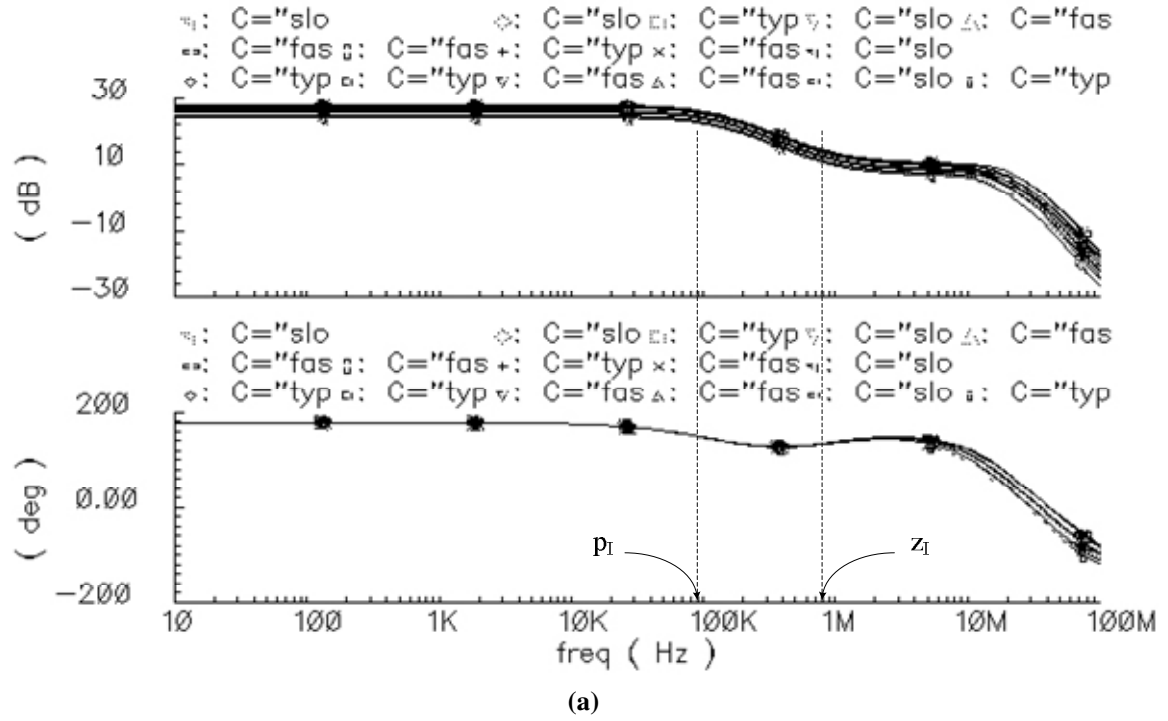


Fig. 6.9. Simulated frequency response curves for the summing amplifier showing the gain from (a) the current inputs and (b) the voltage input over PVT variations.

6.2.2. Experimental Results

A chip microphotograph of the fabricated IC is shown along with Table 6.3, highlighting only the internally connected blocks (not the ones individually connected to pins). In general, the noise generating blocks – the comparators are placed at the bottom of the die, and surrounded by 20μ thick N-well guard rings and 20μ thick p+ contacts to substrate to prevent substrate de-biasing due to any current injected from the switching comparator nodes. Given the low power of the comparators, this is not a significant issue, but as will be seen in the next chapter, the trend is the same for higher power gate-driver circuits that will be incorporated in the second IC. In order to validate the functionality of the circuit blocks as well as the controller system, the prototype IC (in DIP40 package) is designed in two parts –

- A. a set of circuit blocks that are not interconnected on-chip have all their I/O terminals accessible via package pins, and,
- B. an additional set of identical circuit blocks are interconnected on-chip as in Fig. 6.2 with the only inputs of amplifiers A_{DI} - A_{DV} and the output of comparator C_D accessible off-chip via separate pins.

VDD	2.7V-4.2V
I_{bias}	$600\mu A$
Area	$0.9mm^2$
Peak Converter Efficiency	95%
R_{ESRLC} space	5-50m Ω 1-30 μH 1-350 μF
Feature Size	0.5 μm

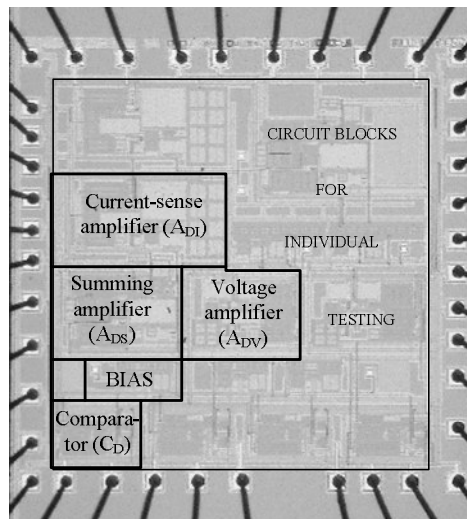


Table. 6.3. Die photograph and key specifications of the fabricated $\Sigma\Delta$ controller

A. Performance of Amplifier Blocks

Because of high package parasitics, it is possible to measure accurately only the DC and low frequency characteristics of the pinned out blocks. To validate the accuracy of the controller IC over process variations, the above measurements are conducted for 39 parts in the production lot. The measured net DC gains $g_{mi}R_S$ and $g_{mv}R_S$ (Fig. 6.10(a)), accounting for the gains of amplifiers A_{DI} , A_{DV} , and A_{DS} , vary by less than 6% around their mean values of 7.4V/A and 37.2V/V respectively. The net offset voltage (Fig. 6.10(b)) referred to the input of amplifier A_{DV} (including the effect of A_{DS}) is higher than that for A_{DI} because of the additional mismatch in the tail currents biasing the input differential pair of A_{DV} . Nonetheless, the standard deviation (σ) for net input offset voltages of both A_{DI} and A_{DV} remains low (0.86mV and 2.01mV respectively). The simulated 3dB frequencies (due to parasitic poles) at the worst-case corners for amplifiers A_{DI} , A_{DV} , and A_{DS} are 12MHz, 5MHz, and 13MHz respectively, with typical values roughly 40% higher.

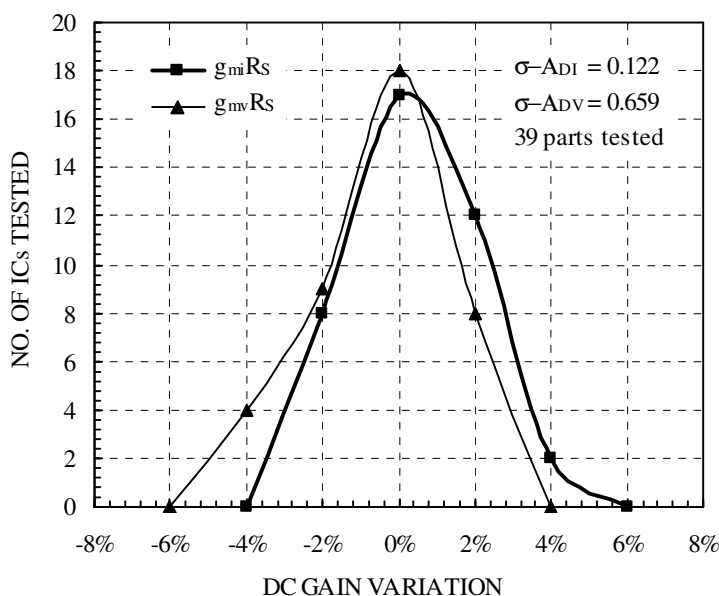


Fig. 6.10(a). Net dc gain variations for current and voltage loop gains $g_{mi}R_S$ and $g_{mv}R_S$.

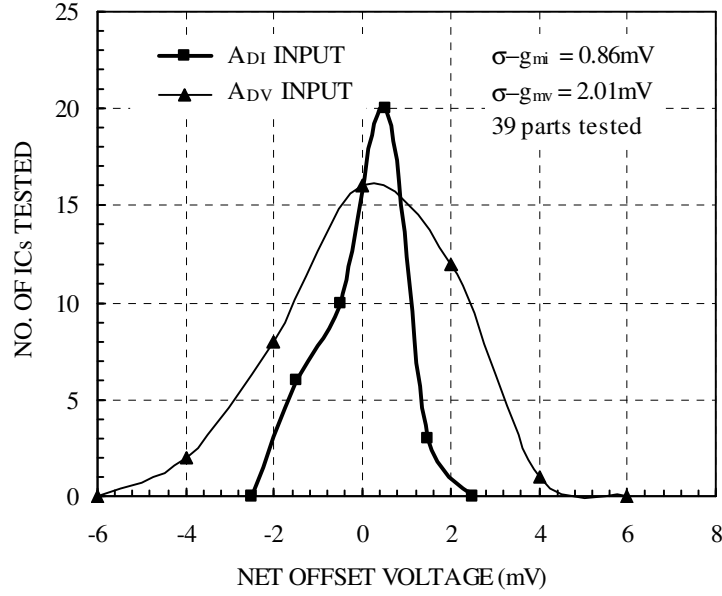


Fig. 6.10(b). Effective input offset voltage variations for Q_1 and Q_v .

B. Performance of $\Sigma\Delta$ Boost Converter

In assembling the system, the gate signal from the controller IC is buffered by an off-chip gate driver to drive the power switches. Various system performance parameters including stability, line/load regulation, power efficiency, and switching frequency variations are studied for a wide range of filter LC values. The results are discussed in the following text.

1) *Steady-State*: Steady-state inductor current and output voltage waveforms at $V_{IN}=2.7V$, $V_O=5V$, $L=22\mu H$, $C\approx 62\mu F$, $I_O=0.8A$, (Fig. 6.11) show ripples in the output voltage (40mV pk-pk) and inductor current (190mA pk-pk), which are sensed by the $\Sigma\Delta$ controller through sensing ratios of 0.24V/V and ($A_{DI}R_I$) 0.4V/A respectively. The effective hysteresis window is roughly 650mVpk-pk and at the switching frequency of 330kHz, the value of $g_{mi}R_S R_I$ (from Table 6.1) is approximately 3.8V/A, which corresponds to a current ripple of 170mA pk-pk. The slight discrepancy between the measured and hand-calculated values is attributed to additional switching delays.

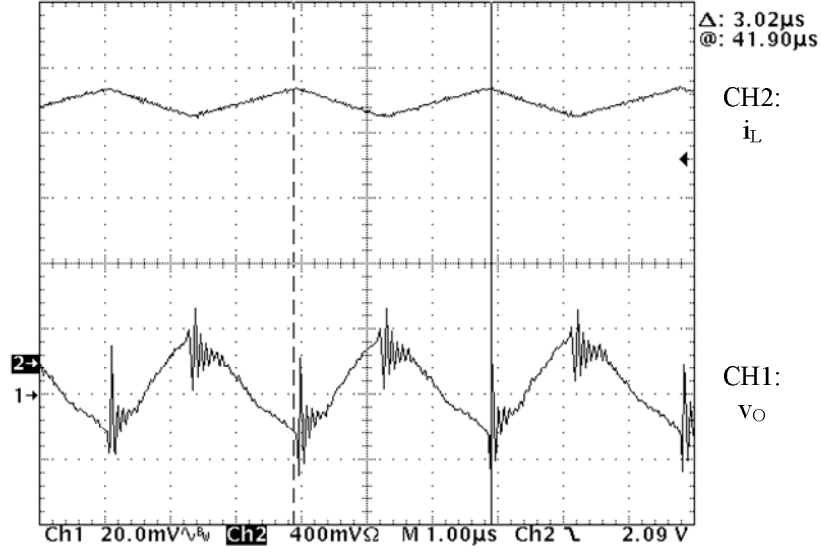


Fig. 6.11. Steady-state inductor current i_L and output voltage v_o waveforms.

2) *Stability*: The unity-gain frequency of the voltage loop approaches that of the current loop for increasing filter inductor and decreasing output capacitor values, destabilizing the $\Sigma\Delta$ operation, as seen from the previous chapter. In the evaluated circuit, the worst-case LC operation limits were determined in terms of the minimum capacitor value for a given inductor value at the maximum rated load (0.8A) and minimum supply voltage (2.7V) (equation (5.13)). Therefore, for a set value of the filter inductor, the capacitor value was gradually decreased (in steps of $0.5\mu\text{F}$) and the converter subjected to a load step of 0.3 to 0.8 A for each capacitor value, until the circuit became unstable with the inductor current and the output voltage showing persistent oscillations (Fig. 6.12).

In the other direction, the highest capacitor value was restricted to $350\mu\text{F}$ as a practical limit in portable applications. A similar procedure was followed for RESR, which was limited to $50\text{m}\Omega$ from ripple considerations in the output voltage. Given these constraints, the stable operating region of the $\Sigma\Delta$ controller can be represented as the enclosure of the RESRLC stability space (Fig. 6.13). As suggested by equation (5.13), the minimum capacitance for stable operation decreases – in this case from $15\mu\text{F}$ to $1\mu\text{F}$ as

the inductor decreases from $30\mu\text{H}$ to $1\mu\text{H}$. Resistance RESR has little effect on the stability since the loop response near its unity-gain (switching) frequency is determined largely by the current loop. The robustness of the controller design against process variations is confirmed by the nearly overlapping stability volumes measured for 10 samples from the production lot.

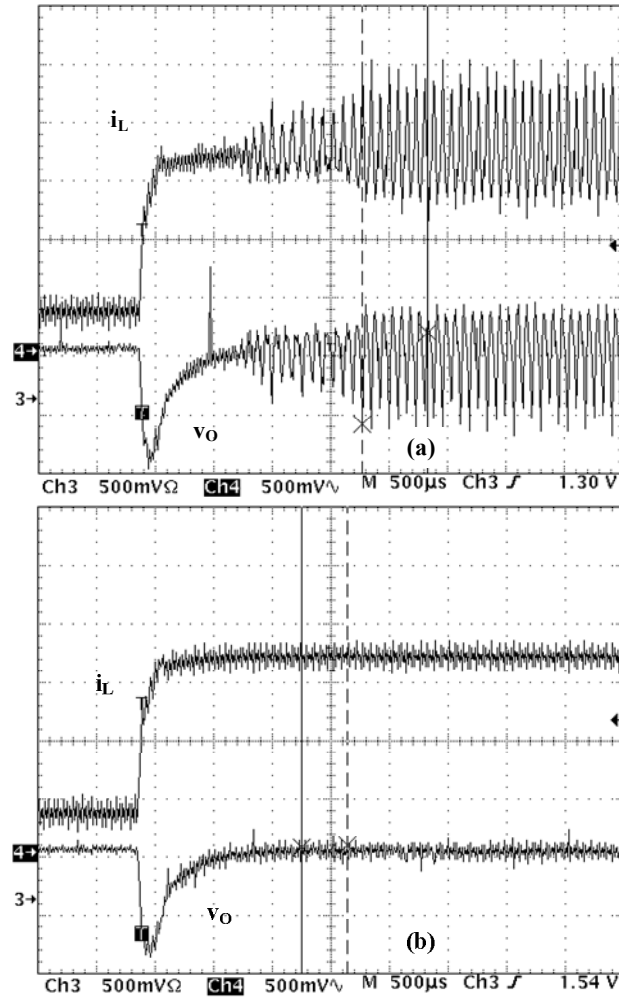


Fig. 6.12. Load step (0.3 to 0.8A) response for stability evaluation of the proposed controller at $30\mu\text{H}$, showing (a) unstable operation at $C=14\mu\text{F}$ and (b) stable operation at $C=15\mu\text{F}$.

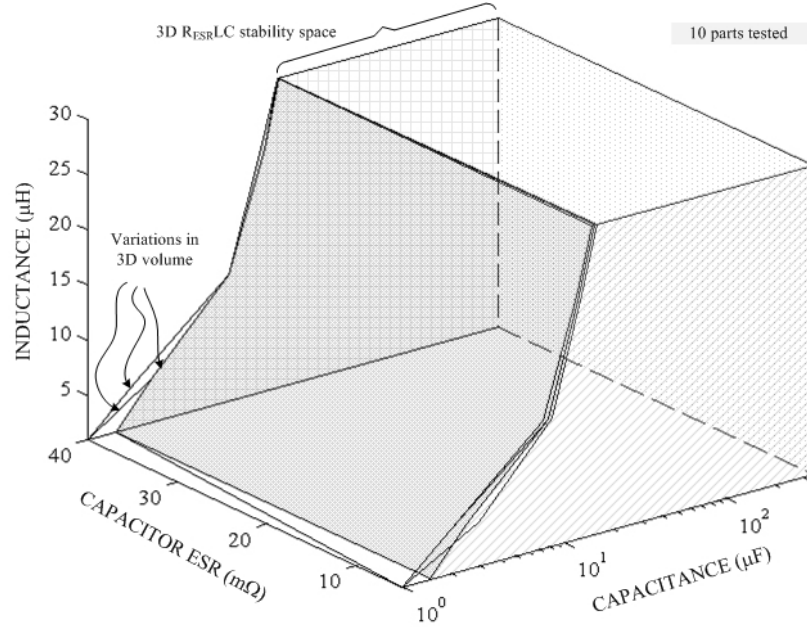


Fig. 6.13. Experimental 3-D $R_{ESR}LC$ stability space for the evaluated $\Sigma\Delta$ controller across process variations.

3) *Switching Frequency Variations*: As explained in the last chapter, switching frequency with a constant gain $g_{mi}R_S$ would be ideally expected to decrease significantly as the input voltage changed from 2.7V to 4.2V, even including the effects of a constant switching delay and line regulation. This is illustrated in the constant $g_{mi}R_S$ curve for $5\mu H$ and 0.5A (Fig. 6.14), which shows a net switching frequency variation of 43%. In comparison, the measured curve has improved performance with the switching frequency variations restricted to 25% at 0.5A because of the inverse frequency dependence of gain $g_{mi}Z_S$ (Figs. 6.1 and 6.6). Fig. 6.14 also shows that as the load increases, the resulting droop in output voltage increases the switching frequency further reducing its line variation at high loads.

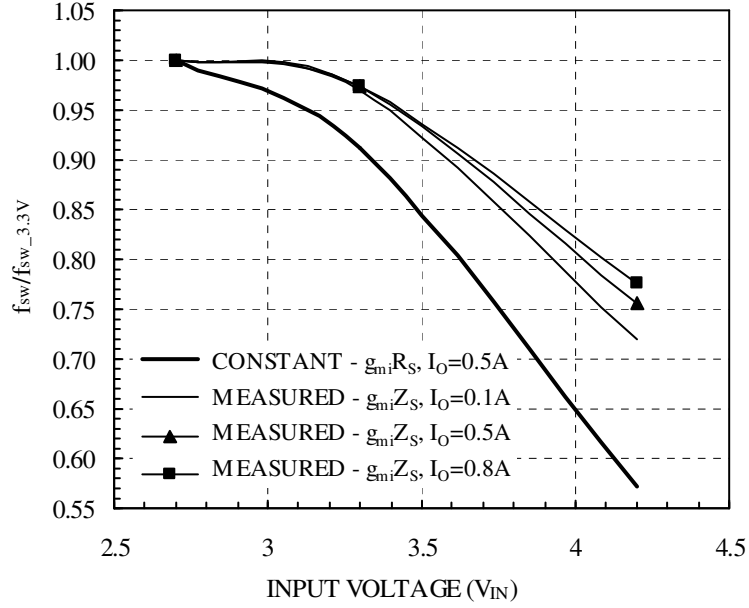


Fig. 6.14. Measured variation of switching frequency with input voltage at 5μH inductance.

4) *Line and Load Regulation*: Switching delays in the converter and finite loop-gain result in a variation of the DC output voltage from its desired value with changes in the supply voltage and load current. As the input voltage changes from 2.7V to 4.2V making the duty-cycle more asymmetrical, experimental results show that the error in the regulated output voltage becomes more negative, validating equation (5.20). Therefore, with the output voltage centered at a 3.3V input, the error voltage changes polarity as the input voltage transitions between its extreme values (Fig. 6.15). The increase in the error voltage magnitude with decreasing filter inductance expressly shows the effects of loop delays on the regulation performance. In the prototype IC, higher package parasitics (DIP40 package) and off-chip gate-drivers lead to a rise in switching delays whose effects were most evident at the lowest inductance value of 1μH (voltage error $\approx +1\%$, -2%). The steady-state error remains below $\pm 1\%$ at higher inductors that suppress the

effects of switching delays. A package with lower parasitics would further improve the performance.

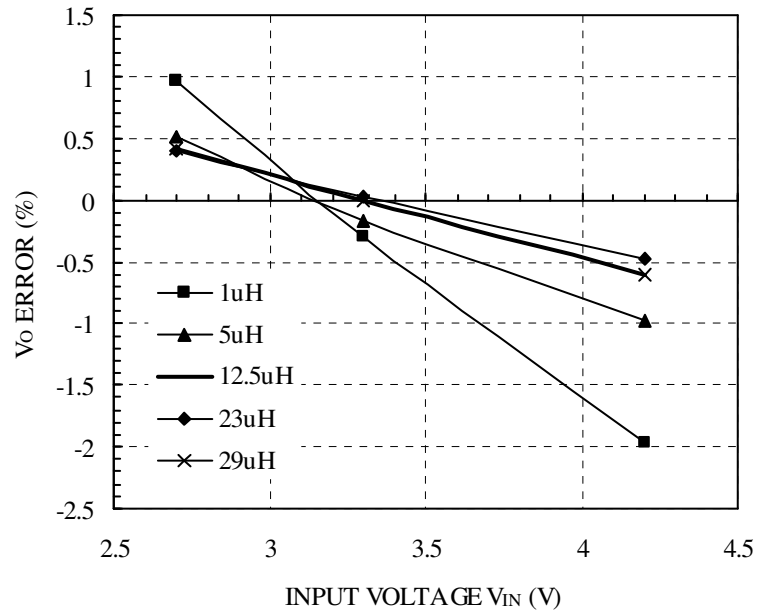


Fig. 6.15. Variation of output voltage with input voltage V_{IN} .

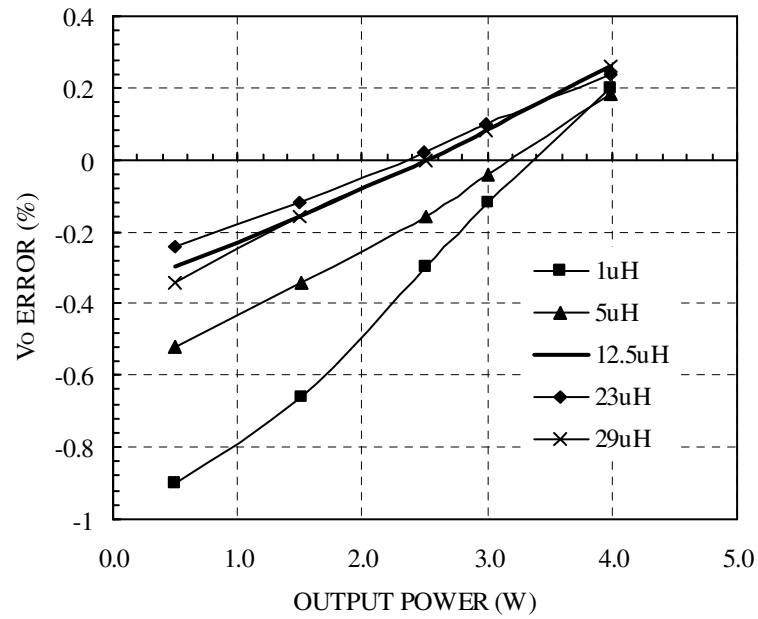


Fig. 6.16. Variation of output voltage with output power.

Since the loop response near and at the switching frequency is dominated by the current loop, load variations do not affect the output voltage (Fig. 6.16) as significantly as line voltage variations. The effect of varying filter inductance remains the same as before with worst-case error (+0.2%, -0.9%) at 1 μ H.

5) *Efficiency*: Power efficiency in a variable filter, self-oscillating $\Sigma\Delta$ converter is subjected to several loss mechanisms and the dominance of one over the others is determined by not only line voltage and load, but also by filter inductance. Measured efficiency curves at a V_{IN} of 3.3V (Fig. 6.17) show that at high inductor values the efficiencies are higher at low load currents (91% at 0.1A, 29 μ H, and 120kHz) because of low switching frequencies and consequently low switching losses. However, at increased loads, higher inductors, which have a higher equivalent series resistance (R_{ESRL}) due more coil turns, suffer from greater conduction losses leading to a reduced system efficiency (83% at 0.8A, and 29 μ H). This trend is reversed as the inductor value decreases because an increase in the switching frequency degrades low load efficiency (88% at 0.1A, 12.5 μ H, and 250kHz) and a reduced R_{ESRL} increases high load efficiency (86.5% at 0.8A, 29 μ H). However, as the inductance decreases further, increase in the switching frequency is limited not by the comparator hysteresis but by the switching delays due to package parasitics.

Therefore, the inductor-current ripple sharply increases (from 0.75A pk-pk at 5 μ H to 2.2A pk-pk at 1 μ H) making the RMS ripple current related conduction losses dominant. As a result, the overall efficiency reduces both at high and low loads (67% at 0.1A, 1 μ H, and 550kHz; 82% at 0.8A, 1 μ H).

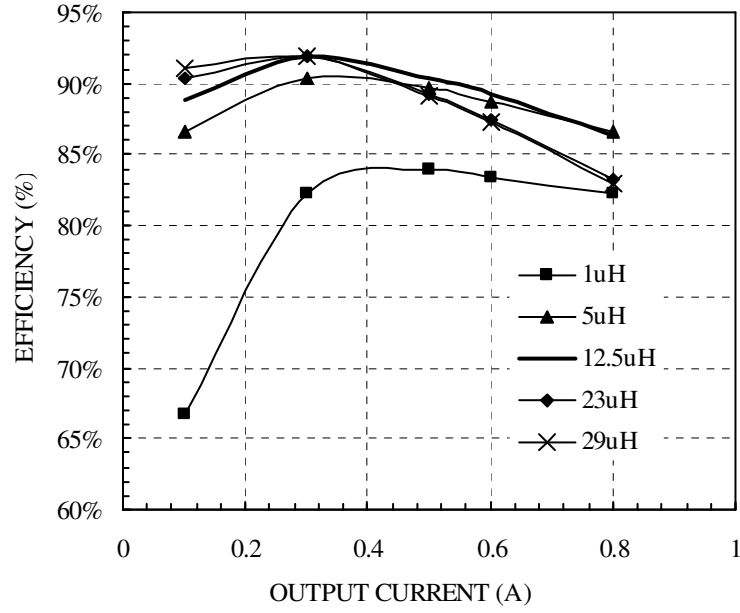


Fig. 6.17. Measured efficiency at 3.3V V_{IN} as a function of load current I_O .

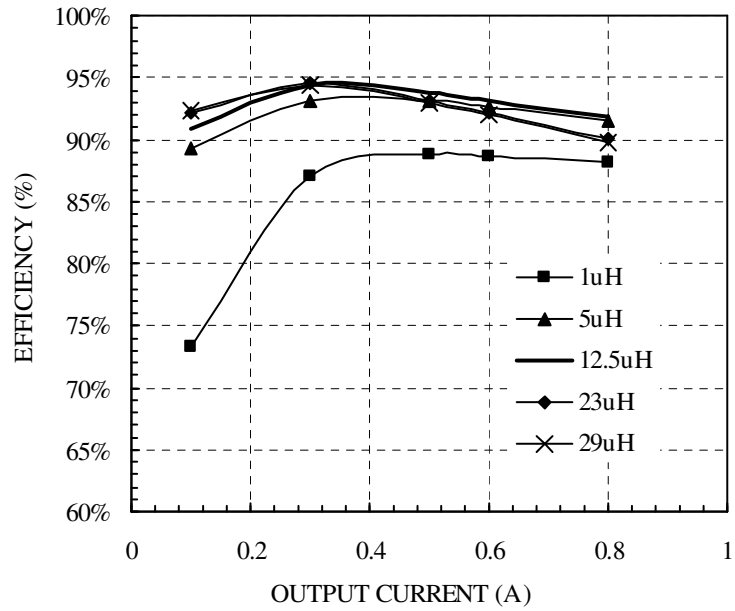


Fig. 6.18. Measured efficiency at 4.2V V_{IN} as a function of load current I_O .

At higher input voltages, the efficiencies increase primarily because of reduced inductor and switch currents. Nevertheless, the trend remains as before (Fig. 6.18) with

the lowest efficiencies at 1 μ H. The peak system efficiency approaches 94% at 0.3A, 29 μ H, and 4.2V supply voltage.

5) *Load Transient Response*: As mentioned earlier, a $\Sigma\Delta$ controller designed for a variable LC system is expected to suffer from a non-optimal transient response, and the proposed design is no exception. Nevertheless, by appropriately sizing the output capacitor, the desired transient response can be achieved. The measured 0.3-0.8A load transient response of the system (at 5 μ H, 200 μ F, and $V_{IN}=4.2$ V) is included (Fig. 6.19) for completeness.

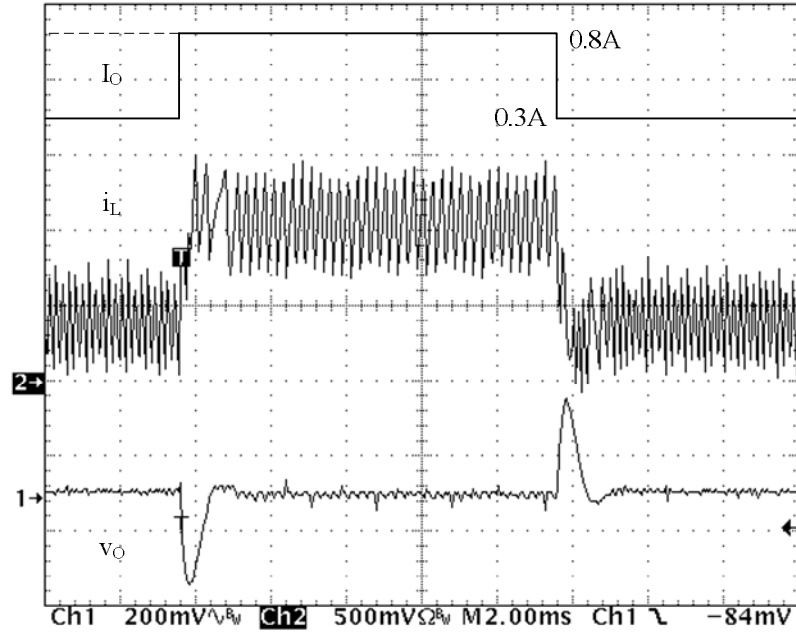


Fig. 6.19. 0.3A to 0.8A load step response at 5 μ H, 200 μ F, and $V_{IN} = 4.2$ V.

6.3. Summary

A $\Sigma\Delta$ controller optimized for filter LC variations was presented, analyzed, and implemented (in a 0.5 μ m CMOS process) using simple low-gain, high-bandwidth, differential circuit blocks consisting essentially of source-degenerated input transconductance stages. Stable converter operation for orders of magnitude variations in

filter LC and capacitor ESR values (1-30 μ H, 1-350 μ F, 5-50m Ω) was verified through experimental results. In designing the high speed $\Sigma\Delta$ controller, the use of low-gain blocks was validated by the open-loop DC gain accuracy ($\pm 6\%$ over process and line variations) and overall converter accuracy ($\pm 1.5\%$ over process, line, load, and filter variations). Although the system performance was somewhat degraded at low inductance values because of higher package parasitics, switching delays, and the consequent limitations on switching frequency, other performance metrics - efficiency (up to 95%) and switching frequency variations (improvement of 20%), were also well within specifications; a low-parasitic package would improve performance throughout the inductance range.

CHAPTER 7

DUAL-MODE SIGMA-DELTA ($\Sigma\Delta$) BOOST CONTROLLER IC

The single-mode controller IC proposed and described in the last chapter was designed, in part, to validate the operation of the transistor-level circuit design on a simpler platform and address any design drawbacks, if necessary, for the dual-mode controller IC. Accordingly, this chapter, that presents the dual-mode sigma-delta boost controller IC, begins with a description of circuit improvements performed from the previous IC. The dual-mode controller IC, in addition to the transient bypass circuit, also contains switch gate drivers and high current power switches. Hence, besides the aforementioned circuit changes, the large DIP40 package used in the previous IC was replaced by smaller packages with significantly lower parasitic inductances and capacitances to enable high current, fast switching activity. The next section describes the issues in and amendments made to the circuits in the single-mode IC. Design of additional circuit blocks including the bypass path, gate drivers, and powers switches is followed by experimental results, discussions, and conclusions.

7.1. Drawbacks in Single-Mode IC

7.1.1. Circuit Issues and Remedies

The previous IC was designed based on the MOS models obtained from AMI over several process runs [58], while poly resistor and poly-poly capacitor models and their variations over process, voltage, and temperature were merely estimated from sample typical data. As such, inaccuracies in the model add to the usual process variations in modifying (sometimes adversely) the circuit behavior from the design expectations. For example, errors in the estimates of sheet resistance and capacitance per unit area lead to higher or lower gains and/or bandwidths. In the case of the source

degenerated input stages describes in the previous chapter, such variations also lead to reduction in the input common-mode range (ICMR) due to increased voltage drop across the source degenerating resistors. The following sub-sections elaborate the performance drawbacks encountered in the various circuit blocks and the remedies implemented to address them. The following sections refer to the system shown in Fig. 6.2.

A. Summing Amplifier

In order to achieve an input common-mode range of approximately 1.2V, the input differential stages of the summing amplifier were ac degenerated such that the degenerating resistors do not carry any dc biasing currents (Fig. 6.6(b)). As a result, the tail currents were split into two thereby risking a mismatch between them. In addition, the tail currents were designed with MOS transistors of relatively large aspect ratios to reduce their saturation voltage levels and reduce the circuit ICMR. The result is that the tail current transistors have a high transconductance that produces a large current offset between them in the presence of gate voltage errors (ΔV_{tail}) due, for example, to mismatch in the threshold voltage. This offset current (I_{OS}) is overcome by the transconductance (G_{MR}) of the input stage by introducing an input voltage that is the input referred offset voltage (V_{OS}):

$$\begin{aligned} I_{\text{OS}} &= \Delta V_{\text{tail}} \cdot G_{\text{Mtail}} = V_{\text{OS}} \cdot G_{\text{MR}} \\ \therefore V_{\text{OS}} &= \frac{I_{\text{OS}}}{G_{\text{MR}}} = \frac{G_{\text{Mtail}}}{G_{\text{MR}}} \cdot \Delta V_{\text{tail}} \end{aligned} \quad (7.1)$$

The input-referred offset is lower if the input stage transconductance is much higher than the transconductance of the tail current. With the choices described earlier however, that is not the case, resulting in relatively high offset voltages referred to the input of the summing amplifier.

This problem is overcome by increasing the channel length of the transistors making up the tail current sources so that the aspect ratios are now multiples of $(30\mu/7\mu)$ from the earlier $(30\mu/5\mu)$. The benefit of this change is two-fold: not only is the tail

transconductance reduced, but the transistor area is also increased, thus reducing any threshold voltage mismatch between the tail current pair as follows. The standard deviation $V_{T\sigma}$ in the threshold voltage mismatch between two transistors of aspect ratio W/L is approximated by [59]:

$$V_{T\sigma} = \Delta V_{\text{tail}} = \frac{A_{VT}}{\sqrt{W \cdot L}}, \quad (7.2)$$

where A_{VT} is the threshold voltage mismatch coefficient and is approximated to $18\text{mV}\cdot\mu\text{m}$. Combining equations (7.1) and (7.2), and knowing that the transconductance a MOS transistor in saturation is proportional to the square root of its aspect ratio (W/L), we have

$$I_{OS} = \Delta V_{\text{tail}} \cdot G_{M\text{tail}} \propto \frac{A_{VT}}{\sqrt{W \cdot L}} \cdot \sqrt{\frac{W}{L}} \propto \frac{A_{VT}}{L}. \quad (7.3)$$

Thus, the offset current between the tail current sources is inversely proportional to the transistor length and an increase from $5\mu\text{m}$ to $7\mu\text{m}$ is expected to improve the offset performance by approximately 30%. The common-mode level of the preceding stage, the current and voltage amplifiers is increased by 100mV to accommodate the increased ICMR of the summing-amplifier input stage.

B. Voltage Sense Preamplifier

The entire controller circuit is designed using differential processing blocks that eliminate, or at least reduce any supply or ground noise because such noise appears as a common-mode signal on the differential lines. Within the IC, the voltage sense preamplifier is carefully laid out symmetrically so that any parasitics – either metal resistance or capacitive noise coupling is virtually identical and does not affect circuit performance. Thus, the only weak point in the amplifier is at its input where the signal can be compromised. In this case, such signal compromise can be caused by the package

(with asymmetrical pin structure and/or bond wires) and/or asymmetrical noise coupling on the PCB where the packaged IC is mounted.

In the evaluation of the first IC, part of the problem was noise coupling at the inputs of the voltage sense amplifier due to the fast switching activity of the power switches. The main reason was the large package (DIP40) used with long leads having significant capacitive coupling with the adjacent pins. Since the desired voltage feedback signal at the amplifier input, being the output of a resistive potential divider, is at a high impedance node, it is especially susceptible to the above noise coupling. To prevent the effects of such high-frequency noise, the revised amplifier contains a 100fF poly-poly capacitor connected at its high-resistance output noise to reduce its bandwidth from 8MHz to 5MHz.

C. Hysteretic Comparator

The comparator in the previous IC was susceptible to similar noise issues as described earlier for the voltage amplifier. To prevent such noise from affecting its performance, the comparator's delay was increased to approximately 40ns to blank out pulses narrower than that. High frequency noise coupled to the comparator input tends to produce such narrow pulses (<30ns) that are hereby prevented.

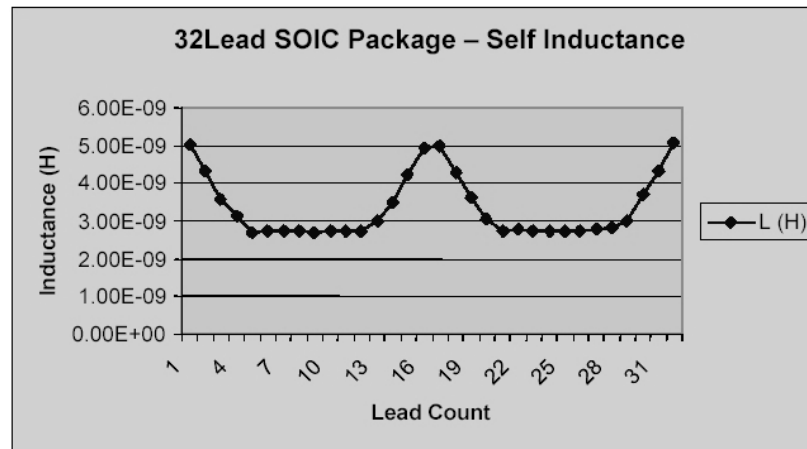
7.1.2. Package Issues

As elaborated earlier, parasitics introduced by the DIP40 package – pin/bond-wire inductance and inter-pin capacitance. The pin resistive, inductive, and capacitive parasitics classified by pin number are listed in Table 7.1 [60]. Note that these are only the pin parasitics; bond wires contribute additional inductance (~1nH/mm of bond wire) [61] and resistance (dependent on wire diameter and material). The length of the bond wires depends on the size of the die relative to that of the package – the higher the difference, the longer the wires. Hence, the large DIP40 package also leads to longer bond wires (~10mm).

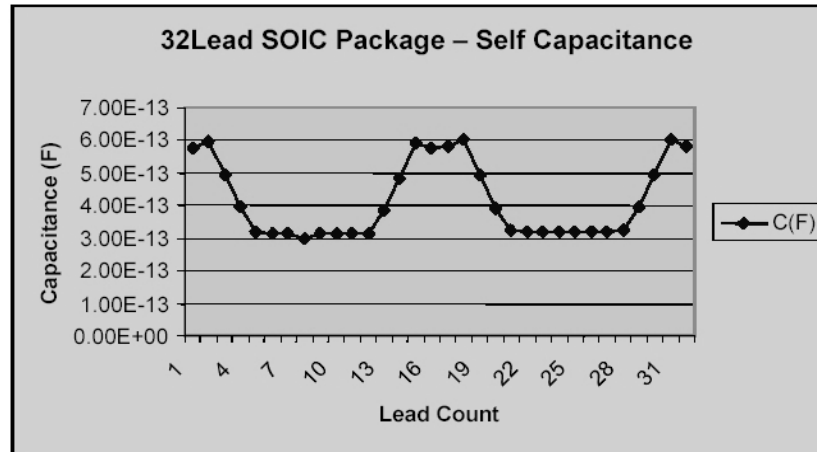
Table 7.1. Pin parasitics for the DIP40 package.

Pin No.	R (Ω)	L (nH)	C (pF)
1,20,21,40	0.217	8.18	5.32
2,19,22,39	0.177	7.92	4.39
3,18,23,38	0.154	7.34	3.37
4,17,24,37	0.11	6.48	2.34
5,16,25,36	0.103	5.69	2.16
6,15,26,35	0.0661	4.37	1.43
7,14,27,34	0.0646	4.54	1.48
8,13,28,33	0.0498	3.69	1.05
9,12,29,32	0.0378	3.54	0.863
10,11,30,31	0.0247	3.15	0.66

To alleviate the parasitic effects, the dual-mode IC was implemented in two package types – an SOIC (small outline IC package) and a QFN (leadless quad flat pack). The SOIC package is significantly smaller (approximately a third of the size) with lower pin inductances and shorter bond wires (data for 32-pin SOIC is shown in Fig. 7.1) [62]. The pin inductances and capacitances in the SOIC package are roughly half of those in the DIP package. As for the QFN package, it is a leadless package, i.e., with no pins. Hence the parasitics are constituted only by the bond wires, which are extremely short (<2mm) since the package variety chosen (5mmx5mm, 28 pin) had a die cavity only slightly larger than the die itself. This was especially expected to be beneficial because of the on-chip switches and gate drivers as seen next.



(a)



(b)

Fig. 7.1. Parasitics of a 32-pin SOIC package showing (a) pin inductance and (b) pin capacitance.

7.2. IC Design

In addition to the changes in the prior circuits as described earlier, the dual-mode IC also contains additional circuit blocks including the bypass path and high-current blocks – switch gate drivers and power switches. It should be noted that the previous IC contained several redundant blocks to test individual block functionality. These blocks are no longer present in the dual-mode IC and the resulting free die area is utilized for the additional blocks.

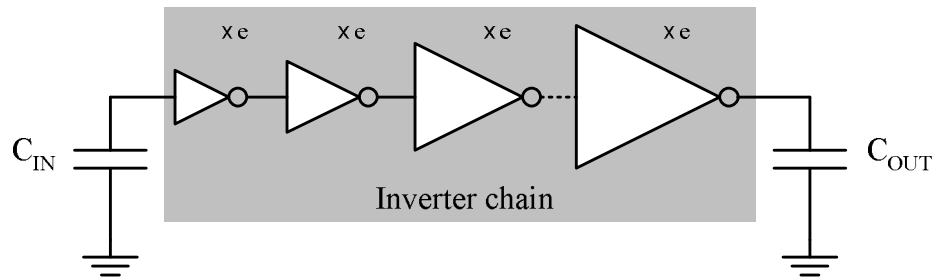
7.2.1. Gate Drivers

Power switches have significant gate capacitance and require high-current drivers to quickly charge and discharge the switch gate in order to turn the switch on and off at a high switching frequency. The design of such gate drivers is dominated by both circuit and layout aspects. This is because the on resistance of the gate driver is composed of the silicon resistance as well as the metal interconnect resistance. As such, the layout and the effective length of the current-carrying path significantly affect the driver performance. A higher resistance slows down the switching speed of the main power switch leading to increased switching overlap losses.

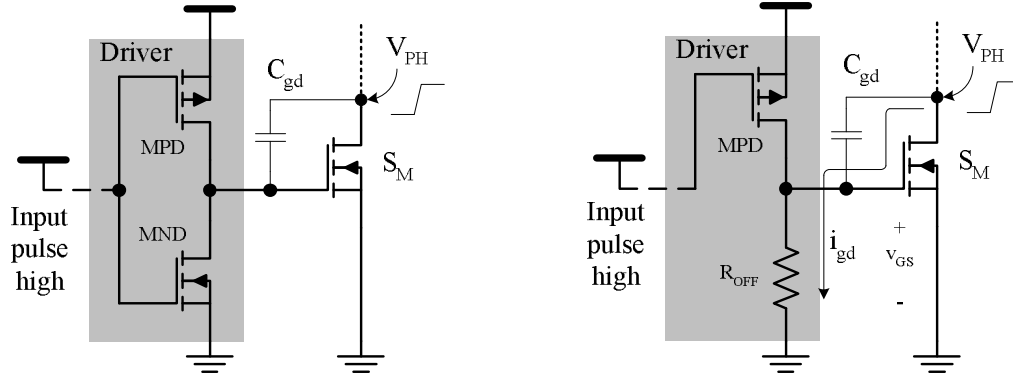
The gate driver is essentially a CMOS inverter, and in that sense, the analog circuit design challenges are few. However, the net switching delay across the driver may be increased due to either the preceding circuit that drives the driver input, or the output of the driver that drives the gate of the power switch. If the gate driver utilizes large transistors, then the gate capacitance of the driver itself is too large for the preceding circuit to charge and discharge fast. On the other hand, if the driver is too small, then it cannot satisfactorily drive the gate of the power switch. Therefore, for optimal performance, the driver is made up of a series of inverters that are progressively increasing in size. In general, it can be shown that the overall delay across the inverter “chain” is the least when the delay across each inverter in the chain is equal to each other. Since the last inverter in the chain driver the power switch, clearly the sizes of the previous stages also depend on the final load capacitance. It can be shown [63] that the net delay is close to the minimum when the number of inverter stages n is:

$$n = \ln\left(\frac{C_{OUT}}{C_{IN}}\right) = \ln\left(\frac{C_{switch}}{C_{IN}}\right), \quad (7.4)$$

where C_{OUT} or C_{switch} is the input capacitance of the power switch, and C_{IN} is the input capacitance of the inverter preceding the gate driver. When equation (7.4) is satisfied, the equalization of delay across each stage is obtained when successive inverter stages in the chain are scaled by a factor of e (approximately 2.78) from the previous stage (Fig. 7.2).



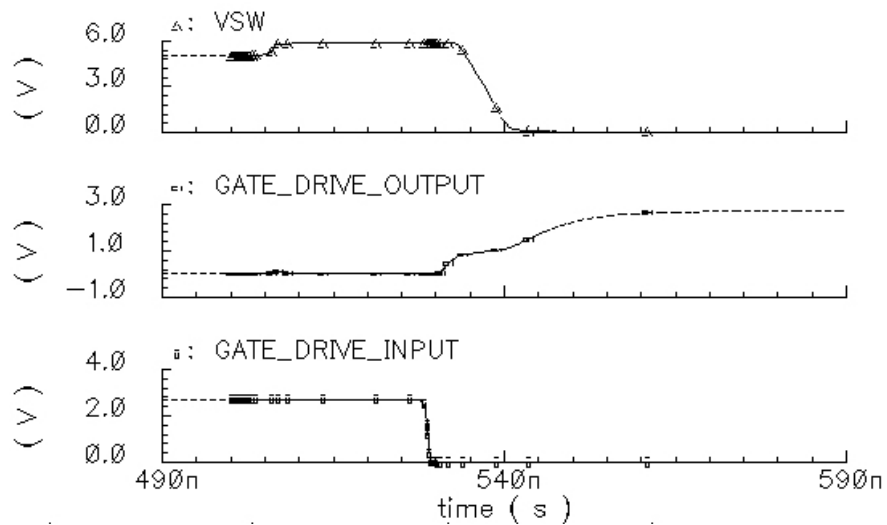
(a)



(b)

Fig. 7.2. (a) Simplified schematic of an ideal gate driver showing inverter chain and (b) schematic representation of spurious gate voltage induced due to fast rise of switch node V_{PH} .

Since the scaling factor of 2.78 (~ 3) gives a higher number of stages and therefore consumes large die area, the scaling factor was increased to 4.5 in the designed driver giving four inverter stages. The resulting increase in driver propagation delay was approximately 4ns and was easily a good tradeoff for the area savings. The main power switches (S_M and S_D) that were mounted off-chip, were expected to present an input capacitance of approximately 660pF [64]. Under these conditions, the simulated switching delay across the driver was less than 10ns (Fig. 7.3) and a switch node V_{SW} transition rate of approximately 3V/ns.



(a)

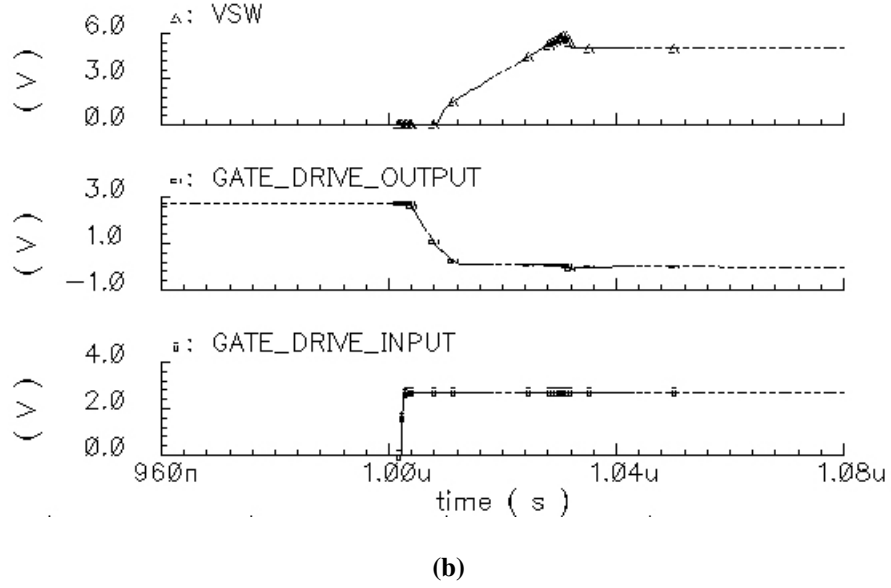


Fig. 7.3. Simulated waveforms showing the gate driver delay and switch transition times for a 2.5A load at $V_{IN}=2.7V$.

Another concern in driver design is the driver's ability to hold its output low, when off, in the face of fast switching transients. As shown in Fig. 7.2(b), when the switch node at the drain of the power switch rises, the fast voltage rise couples a current through the parasitic gate-drain capacitance C_{gd} of the power switch. This current, which has to be sunk by the pull-down NMOS of the driver, can induce a spurious voltage v_{GS} across this pull-down switch (i.e., gate of power switch) if the pull-down resistance is not low enough [65]. If this voltage is higher than the threshold voltage of switch S_M , then S_M can turn on momentarily with a high drain voltage across it. In the least, this anomalous turn-on can lead to increased power loss, and in the worst-case, can damage the switch S_M . Therefore, the pull-down NMOS MPN has to be designed larger than that given by the timing considerations from equation (7.4). In the designed drivers, the final stage of the NMOS drivers is composed of PMOS 60(30 μ /0.6 μ) and NMOS 60(28 μ /0.6 μ) drawn length, while that of the PMOS drivers is PMOS 60(90 μ /0.6 μ) and NMOS 60(28 μ /0.6 μ).

The layout of the gate driver is critical because of the resistance added by the metal interconnects. The final stage of the inverter is significantly large, i.e., it has a large

aspect ratio, but it cannot be laid out as a single long stripe. Instead, the layout is most optimal when it is laid out in multiple segments in parallel (Fig. 7.4) [66]. A group of such parallel-connected segments constitutes a segment-set. Two segment-sets are used for the PMOS and NMOS of the final stage of each integrated driver in order to achieve a square driver layout. A 160 μm metal2 or metal3 bus was laid out from the output of the drivers to its bond-pad or switch gate (switch S_A) and the length of the trace was kept short.

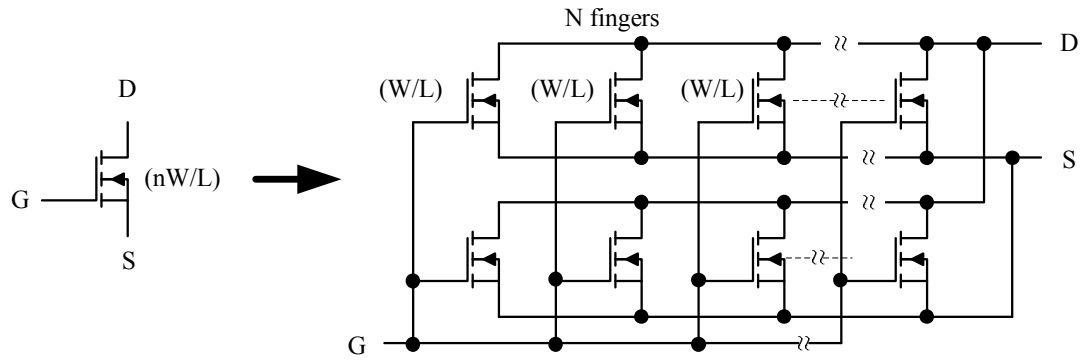


Fig. 7.4. Simplified circuit representation of the layout of each transistor in the gate driver.

7.2.2. Power Switch

The proposed IC integrates the auxiliary switch S_A to complete the dual-mode controller with the main switches S_M and S_D mounted off-chip. The switch S_A does not conduct current in steady state, hence the switch on-resistance is not crucial to steady-state power efficiency. The basic requirement is that the on-state voltage-drop across the switch does not exceed $(V_O - V_{IN})$ so that the switch appears as a short during the bypass path operation.

The implementation options for the switch are few in the AMI 5V CMOS process. A high-side NMOS switch would require a high-side floating gate drive supplied from a floating supply. In that case, the absolute value of the floating supply above ground, which is level-shifted by approximately the output voltage, exceeds the peak voltage capability of the process. As such, the high-side driver would require the capability to

produce an isolated NMOS switch inside a high-voltage NWELL. A second concern arises from the fact that when the switch is off and the switch node is at ground (switch S_M is on) the source of the power NMOS switch would, in this case, not be connected to its body increasing its body-source resistance and therefore the propensity for a parasitic lateral bipolar turn-on [66]. A second alternative is the use of a PMOS switch with its NWELL body connected to the output terminal that, in steady state, is at the highest voltage in the circuit. Although technically this configuration is suitable, the transistor source is still not connected to its body maintaining its susceptibility to turn-on of the parasitic vertical bipolar transistor. The parasitic bipolar turn-on possibility can be alleviated by reducing the current gain β of the bipolar transistor either by increasing the base dopant concentration by using an N+ tub around the NWELL. This is a feature not compatible with the implemented process hence the risk of bipolar turn-on cannot be prevented. On the other hand, if the source is connected to the body, then the body diode of the switch connects anti-parallel to the switch S_A itself with its anode (P+ source diffusion) connected to the switch node and its cathode (NWELL) at the input supply. This diode turns on naturally when the switch node exceeds V_{IN} , eliminating the use of switch S_A as a fully controlled switch.

As a result, the proposed switch S_A consists of two PMOS switches connected back to back so that their body diodes form a non-conducting path. The two switch gates are connected together and when turned on, only the channels of the two switches conduct. The bodies of the two switches are connected to their respective source or drain diffusion (source or drain depends on direction of current flow) so that one of the two NWELLs is connected to the switch node (switch S_{A2}) while the other one (switch S_{A1}) is connected to the supply V_{IN} , as shown in Fig. 7.5. The net on-resistance of the switch is the series combination of the resistances of the two switches. With the direction of the inductor current as shown in Fig. 7.5, the source-body of switch S_{A2} are connected while the drain-body of switch S_{A1} are connected.

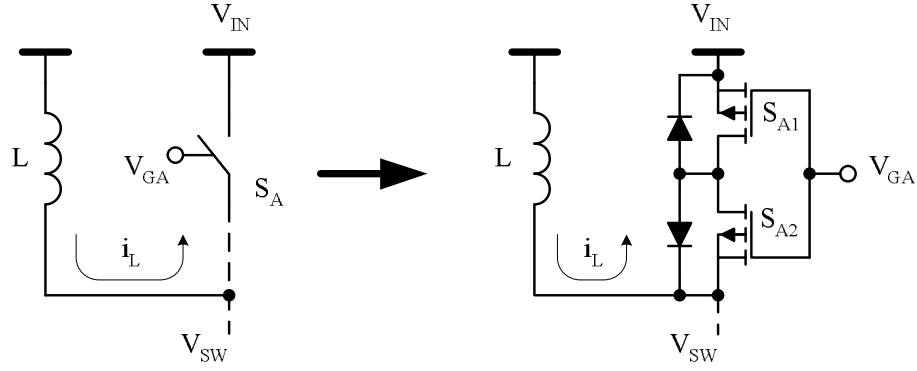


Fig. 7.5. Schematic representing the circuit implementation of the auxiliary switch S_A by connecting two PMOS switches and their respective body-diodes in series with each other.

In designing switch S_A , the predominant aspect is the switch layout that determines the switch resistance and current distribution. Similar to what was seen earlier in the gate driver the switch consists of several narrow transistor fingers connected in parallel so as to end up in a layout that is roughly square while delivering the desired switch aspect ratio. These parallel-connected transistor “fingers” have metal resistance between them and in the connection to the terminal bond pads as shown in Fig. 7.6. In a simplified picture, assuming all the metal resistances between the transistor fingers are equal to a resistance R , if the source and drain terminations lie physically on the same side as in Fig. 7.6(a), the net resistance in the paths of individual finger currents i_{1-4} increased in the direction away from the drain-source terminations. As a result, in Fig. 7.6(a), current i_1 is greater than i_2 , which is greater than i_3 , and so on, leading to an uneven current distribution with a potentially serious current crowding in i_1 . Hence, the source and drain terminations are arranged on the opposite sides of the transistor array (Fig. 7.6(b)) thus evening out the series resistance in the paths of individual finger currents, yielding a uniform current distribution [66]. The same reasoning holds higher levels of layout involving multiple groups of transistor arrays.

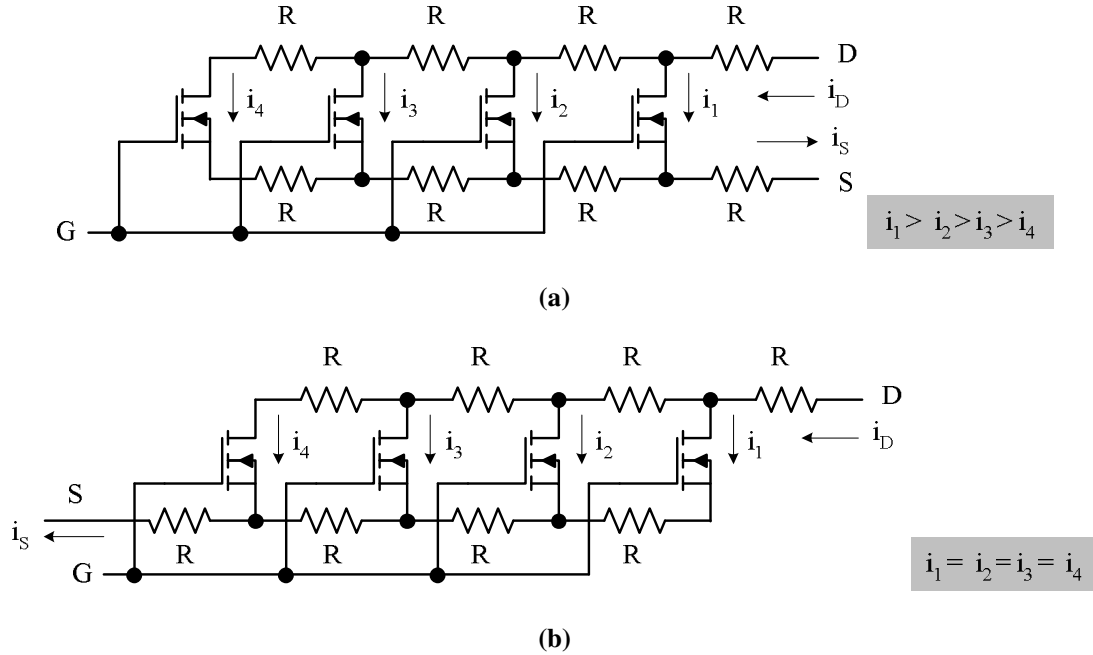


Fig. 7.6. Simplified circuit representation of a transistor layout array with parasitic resistance R showing physical locations of the transistor drain-source terminals on (a) same side of transistor array, and (b) opposite sides of transistor array.

Referring to Fig. 7.6(b), the terminal drain current i_D flows partly as channel current when it encounters a transistor finger while the rest of it flows ahead in the metallization until it hits another transistor finger, and so on. Clearly, the current flowing through the metal resistors R on the drain side (top) decreases in metal interconnects farther away from the drain terminal D. Similarly, the current through the metal interconnect resistors R on the source side (bottom) increases closer to the source terminal S. These unequal currents flowing through equal resistors R produce a higher-than-optimal net series voltage drop from the drain to source terminals. To alleviate this problem, the metals (metal2 and metal3) that make up the interconnect resistances R are designed non-uniform in thickness so that the resistors R correspondingly decrease in value closer to the drain and source terminals. Thus the product of increasing current and decreasing resistance R remains more or less constant between individual transistor fingers, minimizing the effective equivalent resistance between the drain and source

terminals. The gradual decrease in the resistance R is achieved by tapering the width of interconnect metal so that it gradually gets narrower in the direction of current flow.

7.2.3. Mode-Transition Circuit

As explained in chapter 5, the proposed circuit changes its operation to the bypass mode during transients allowing a fast transient response. Soon after, the circuit transitions back to the steady state or the main mode of operation. These mode transitions are realized by the mode transition circuit. In order to transition to the bypass mode, the reference input to the summing amplifier is stepped up to a value corresponding to the inductor current level at the peak load rating of the circuit. This reference step is achieved by selectively shorting the output of a low impedance buffer to the low-pass filtered output of the current sense amplifier. The input of the aforementioned buffer, which is equal to the sensed inductor current at peak load, is derived from the internal bias circuit. The switches that short the buffer output to the current reference are gated by the output of the transient comparator.

In transitioning from the bypass to the main mode, an offset voltage V_{IOS} is introduced between sensed current and its reference, which is now released from the clamp at the onset of the bypass mode, so that the sensed current appears higher than the reference by an amount equal to the added offset voltage. As a result, the current control loop forces the duty-cycle to decrease gradually to match the sensed current to its reference. The result is that the inductor current gradually decays until the bypass mode is exited and the circuit enters steady state.

The voltage offset V_{IOS} is introduced in the voltage buffer at the output of the current-sense amplifier A_{ID} as shown in Fig. 7.7 (refer to Fig. 6.4). The sensed current $A_I R_I I_L$ has a positive dc offset equal to I_{OSROS} with respect to its reference V_{IREF} when the switches across the resistors R_{OS} are open. The switches can be closed by a control signal that is activated once the circuit exits the bypass mode. The resistors R_{OS} are small

enough not to disturb the symmetry of the differential amplifier implementation significantly. Since the current I_{OS} is generated by a voltage controlled current source that is based on the reference voltage across an internal resistor, the voltage across the offset resistors R_{OS} is maintained quite accurate by designing R_{OS} of the same type (poly2) and width ($3\mu\text{m}$) as the resistor that creates I_{OS} . In addition, R_{OS} is aligned in the same orientation (vertical) as the current generating resistor. Metal3 trim options are made available to increase the resistance R_{OS} by 10% and 20%, if necessary.

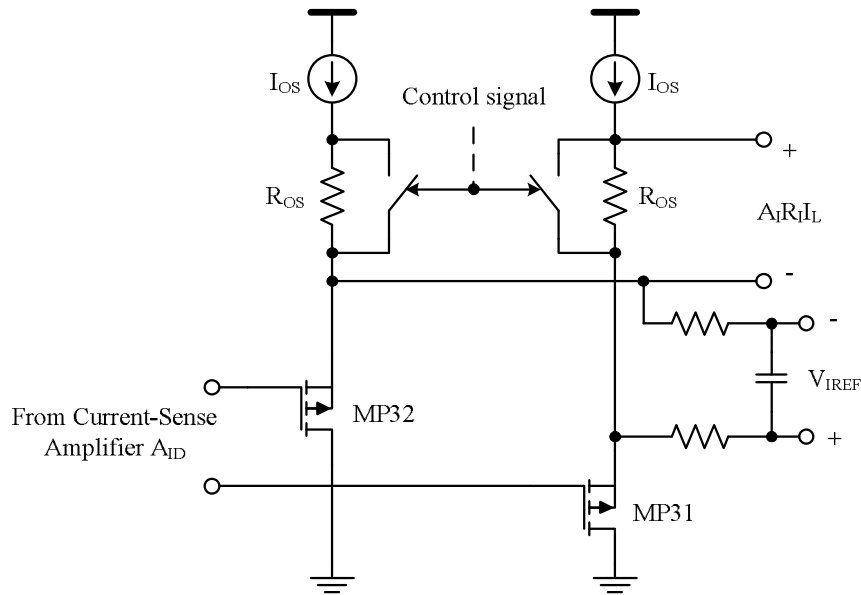


Fig. 7.7. Circuit schematic of the buffer at the output of the current-sense amplifier that introduces voltage offset V_{IOS} between sensed current $A_I R_I I_L$ and reference V_{IREF} .

A die microphotograph of the fabricated IC is shown in Fig. 7.8. Since the IC contains power switches and drivers, the overall layout is critical to successful operation. The high-current powers switch S_A is laid out at the very top of the die and surrounded on three sides with $50\mu\text{m}$ wide NWELL guard rings. Since deeper guard ring structures are not available, the NWELL rings were kept as wide as possible to maximize their ringing capability; nevertheless, this not expected to curtail sufficiently any minority carrier injection in the substrate from the rest of the die and hence, sensitive structures are kept

far away from the switches. As such, the switch gate drivers are kept closest to the switches with 30 μ m NWELL guard rings around each driver. Hysteretic comparators and digital circuits in the control/enable logic are below the drivers, both from the point of view of electrical connections and noise tolerance.

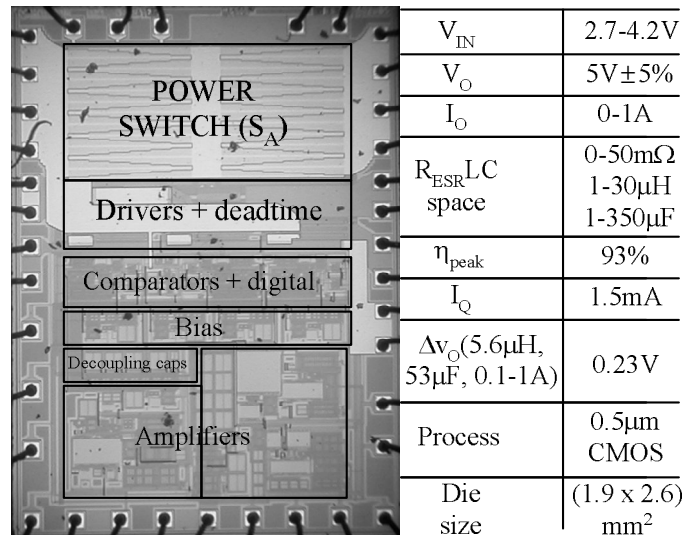


Fig. 7.8. Die microphotograph of the fabricated IC tabulating important performance parameters.

Sensitive bias circuits not only must be away from the noisy power switch and gate drivers, but they must also be far from the die edge for accurate matching. In addition, placing the bias current/voltage circuits below the comparators also help from the point of view of keeping the reference lines to the comparator inputs short and therefore less sensitive to noise. Finally, differential amplifiers are arranged below the bias circuits to minimize their interconnect lengths. All lines to and from the amplifiers are laid out perfectly symmetrical to minimize any non-symmetrical resistive components and/or capacitive coupling that would defeat the purpose of using a differential structure in the first place. Furthermore, all lines are shielded by parallel running metal lines connected to each other at regular intervals and connected to quiet signal ground.

Decoupling capacitors are used across the internal supply lines V_{DD} -gnd to alleviate any noise at the analog supply inputs. In order to prevent the ringing of these capacitors with any bond wire/pin inductances, the natural resistance of the supply lines is approximately kept at 5Ω . The impact of this resistance on the dc voltage level is insignificant enough not to affect circuit operation.

7.3. Experimental Results

The proposed $\Sigma\Delta$ controller $0.5\mu\text{m}$ IC was designed to supply power from a 2.7-4.2V Li-Ion battery and drive a 0-1A load at $5V \pm 5\%$ with as wide an $R_{ESR}LC$ range as possible (0-50m Ω , 1-30 μH , and 1-350 μF was achieved). The total silicon surface area the IC occupied was 1.9 x 2.6 mm (Fig. 7.8). The peak efficiency of the converter was 93% at 0.4A with a biasing quiescent current of 1.5mA. The total output voltage variation of the converter in response to a 0.1-1A load dump (Δi_o) with 5m Ω , 5.6 μH , and 53 μF of $R_{ESR}LC$ was 200mV, which constitutes a 4x improvement over its non-bypassed counterpart under similar conditions (800mV).

7.3.1. LC Compliance

The $R_{ESR}LC$ space for which the converter was stable is 0-50m Ω , 1-30 μH , and 1-350 μF , as illustrated in Fig. 7.9. This range was determined by subjecting the converter to 0.1-1A load dumps with 100ns rise and fall times. The stability limit was observed as a loss of regulation for the proposed $\Sigma\Delta$ converter in the bypass mode, as the bypass loop was no longer able to control the loop, and sub-harmonic oscillations for the non-bypassed (state-of-the-art) $\Sigma\Delta$ boost converter [67].

The stability limits for both converters, with and without the bypass path, are reached when their respective current-loop bandwidths ($f_{i,0dB}$) approach their voltage-loop counterparts ($f_{B,0dB}$ and $f_{V,0dB}$), as that is when L ceases to be a current source for the

voltage loop, be it the main loop or the bypass loop. As a result, because $f_{V,0dB}$ and $f_{B,0dB}$ increase with decreasing C_O and increasing I_O and $f_{L,0dB}$ and RHP zero z_{RHP} decrease with increasing L and decreasing V_{IN} , the highest L - I_O (30 μ H-1A) and lowest C_O - V_{IN} (12 μ F-2.7V) combination constitutes worst-case conditions. Since R_{ESR} essentially introduces a left-half plane zero in the voltage loop, increasing R_{ESR} also increases $f_{V,0dB}$ and $f_{B,0dB}$, which means the above-mentioned limits along with the highest R_{ESR} value (50m Ω) describes the worst-case stability point of the converter. In other words, $C_{O(min)}$ increases with increasing L , I_O , and R_{ESR} and decreasing V_{IN} .

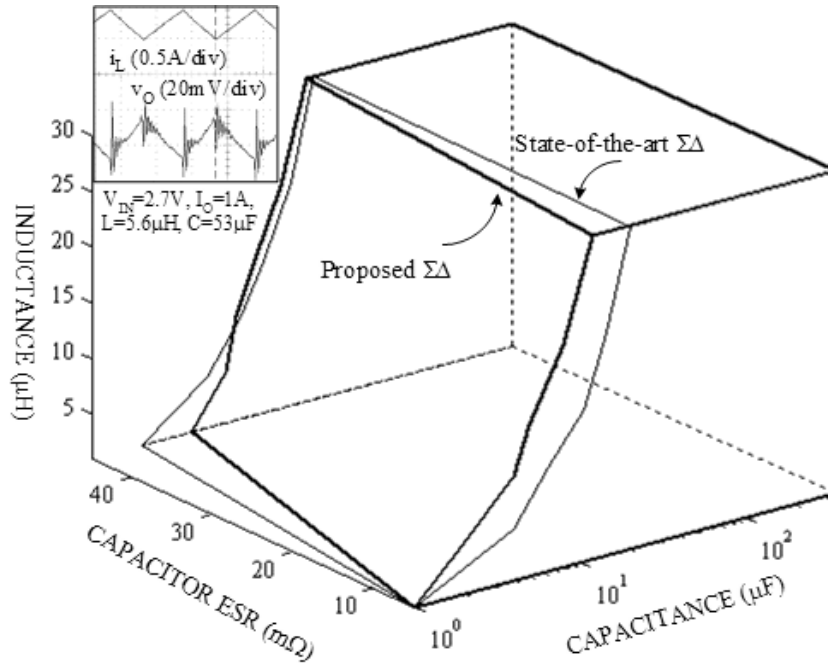


Fig. 7.9. Nominal steady-state snapshot of inductor current i_L and output voltage v_O ripples (inset) for the proposed solution and experimental R_{ESR} LC stability space for both the proposed dual- and state-of-the-art single-mode boost $\Sigma\Delta$ converters.

The maximum capacitance was limited to 350 μ F as a practical limit for the intended portable application space (the circuit is stable at higher C_O values). Similarly, the maximum R_{ESR} value was limited to 50m Ω to keep the output voltage ripple acceptably low under a 1A load. Under these conditions and constraints, the stability

spaces for the proposed and the state-of-the-art converters are approximately equal in “volume.”

7.3.2. Transient Load-Dump Response

As shown in Fig. 7.10(a), the transient-response variation of v_O (Δv_O) in response to 0.1-1A load dumps (Δi_O) with 100ns rise and fall times under 2.7V, 5.6 μ H, 53 μ F, and 5m Ω of V_{IN} , L , C_O , and R_{ESR} was 200mV for the proposed dual-mode scheme and 800mV for its single-mode state-of-the-art counterpart. While the proposed converter responds by increasing i_L above its target (to I_{PK} or V_{PK}/R_L) in one switching cycle of S_M , the state-of-the-art circuit increases i_L gradually, pulling v_O back to regulation in several cycles of S_M , which is why the proposed solution exhibits a four-fold improvement over its predecessor. In a negative load-step (Fig. 7.10(b)), while the excess inductor current is immediately bypassed by switch S_A in the proposed converter keeping the output voltage overshoot low (less than 75mV), the excess inductor energy causes a large voltage overshoot (600mV) in the state-of-the-art converter. Thus, the transient improvement in the proposed converter is both for positive and negative load dumps with an inherent energy limiting capability due to the auxiliary switch.

Decreasing (increasing) L increases (decreases) the rate at which i_L responds to a load dump, as shown in Fig. 7.11, thereby decreasing (increasing) the time v_O slews (reducing Δv_O). Similarly, increasing (decreasing) C_O decreases (increases) v_O 's droop rate in response to a load dump (Fig. 7.12). Note increasing (decreasing) C_O also increases (decreases) the delay time between the load step and the onset of bypass threshold voltage ΔV_{BP} (t_d), which is why the onset of i_L rising shifts with C_O .

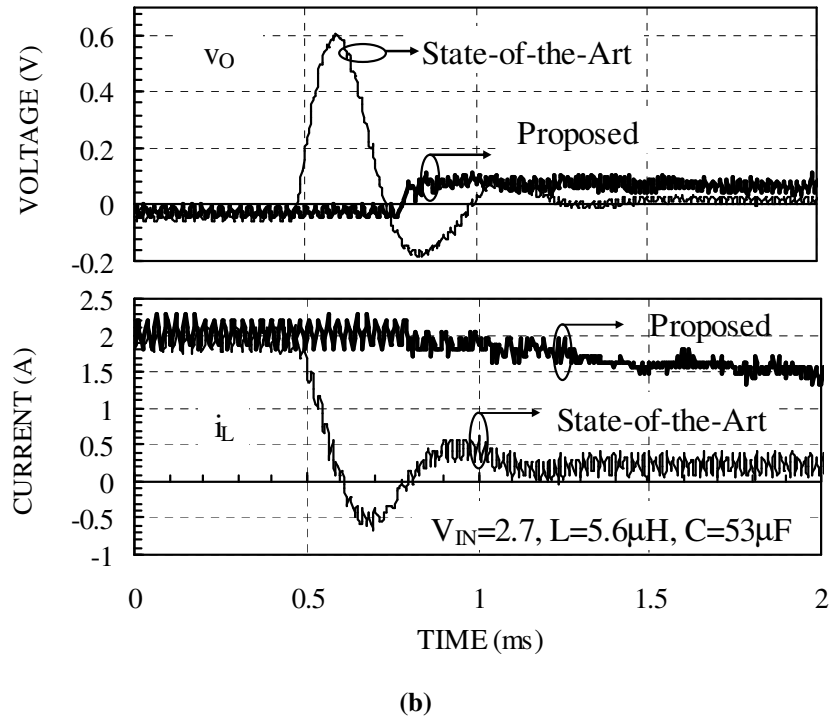
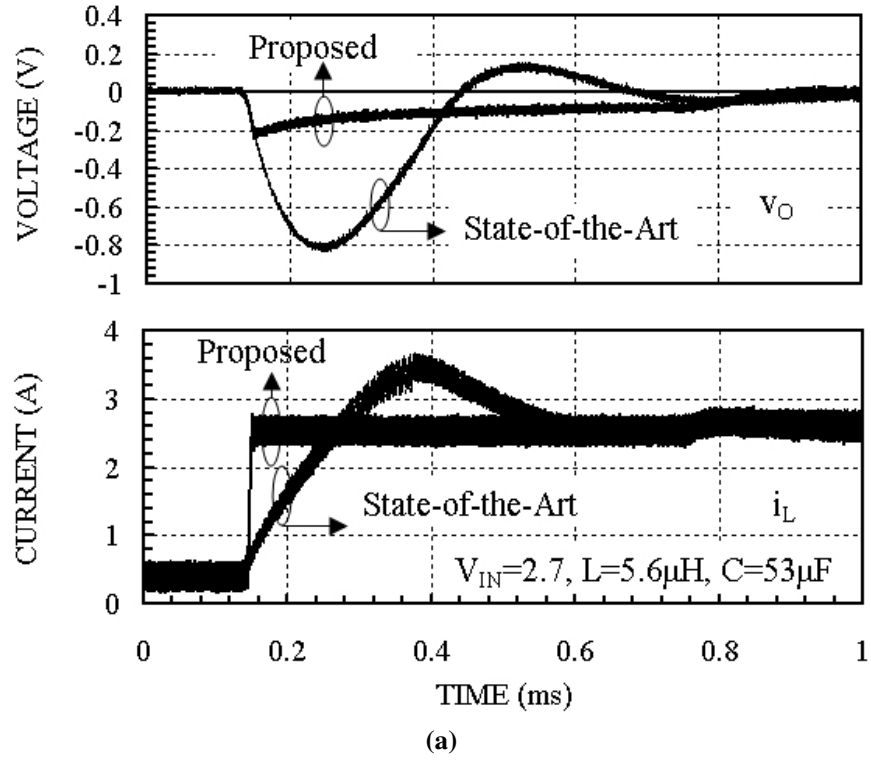


Fig. 7.10. Transient performance of the proposed dual-mode and state-of-the-art single-mode $\Sigma\Delta$ boost converters in response to (a) 0.1-1A and (b) 1-0.1A load steps.

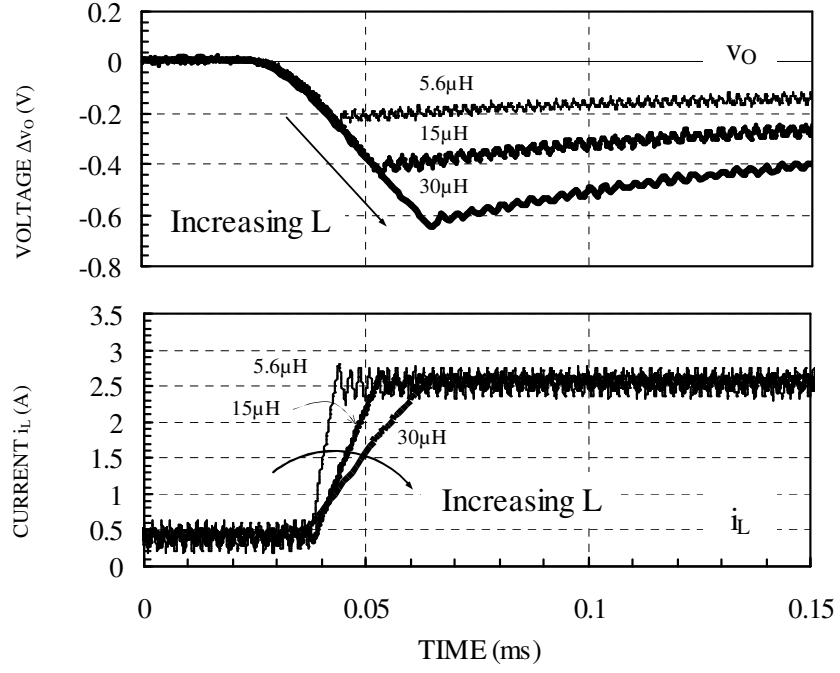


Fig. 7.11. Effects of inductance L on the transient performance of the proposed dual-mode $\Sigma\Delta$ bypass boost converter in response to 0.1-1A load dumps, $C_O=53\mu\text{F}$.

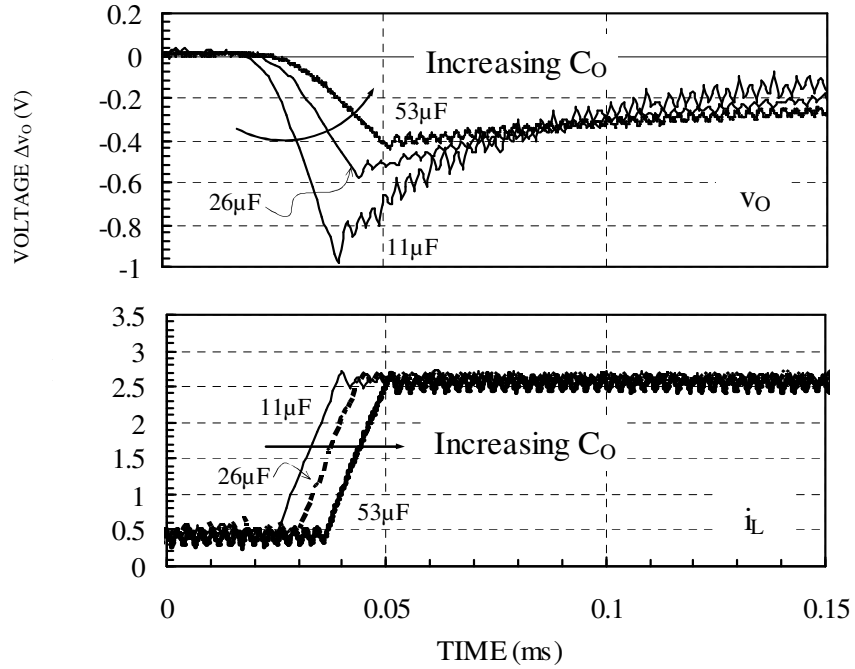


Fig. 7.12. Effects of output capacitance C_O on the transient performance of the proposed dual-mode $\Sigma\Delta$ bypass boost converter in response to 0.1-1A load dumps, $L=15\mu\text{H}$.

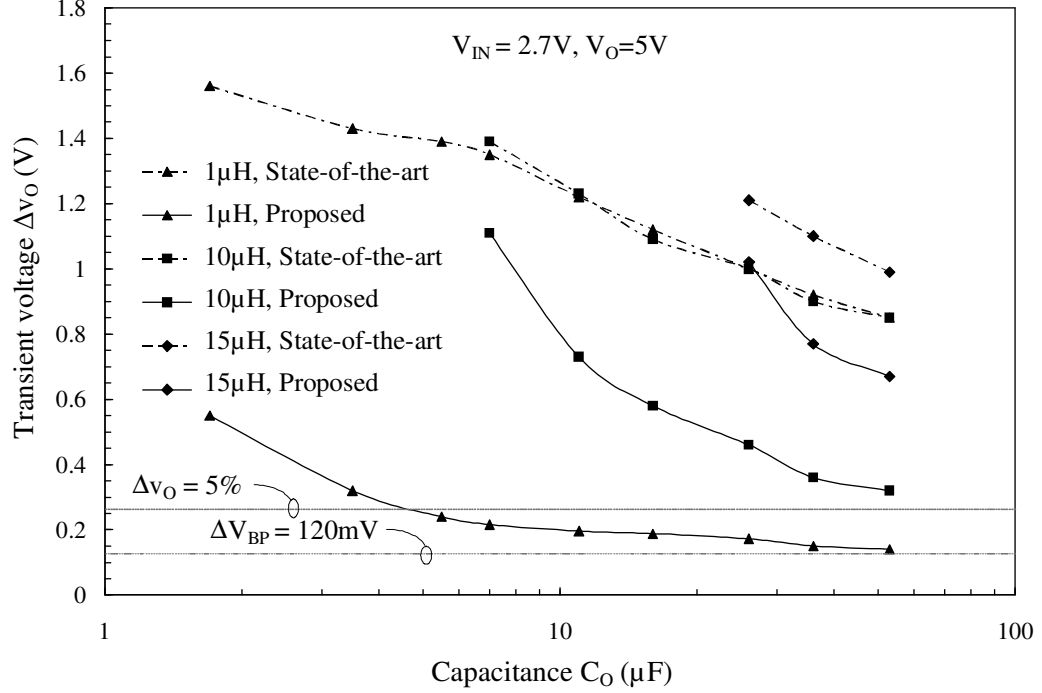


Fig. 7.13. Transient output voltage variation Δv_O under various LC combinations in response to 0.1-1A load dumps (Δi_O) for the proposed dual-mode and state-of-the-art single-mode $\Sigma\Delta$ converters.

7.3.3. Mode Transition

Figs. 7.14 and 7.15 illustrate how the proposed dual-mode $\Sigma\Delta$ bypass boost converter transitions from steady state to bypass mode and back in response to positive and negative 0.1-0.6A load dumps with an LC combination of 15 μ H and 53 μ F. As designed, the bypass mode ripple is larger at $\pm 70\text{mV}$ ($\pm(H_V/2) \cdot (R_1 + R_2) / (R_2 A_{DV}) \approx \pm 140\text{mV}/2$) or $\pm 1.4\%$ than the steady-state counterpart, which is at $\pm 15\text{mV}$ or $\pm 0.3\%$. During a positive load dump (Fig. 16), when i_O suddenly rises, a load-induced drop in v_O exceeding the ΔV_{BP} limit engages the bypass mode and increases i_L to 2.5A (I_{PK}) in one switching cycle of S_M . The circuit then takes approximately 2.5ms to gradually decrease i_L back to its new target of roughly 1.3A, at which point S_A stops switching and the converter is back in steady state. During a negative load dump (Fig. 17), i_L is automatically above its target and S_A consequently starts diverting some of i_L back to V_{IN}

almost immediately, until 2.5ms later, when i_L drops to its new target. Thus, a single offset voltage V_{IOS} (Fig. 7.7) enables transition from the bypass to main operating mode following both positive and negative load dumps.

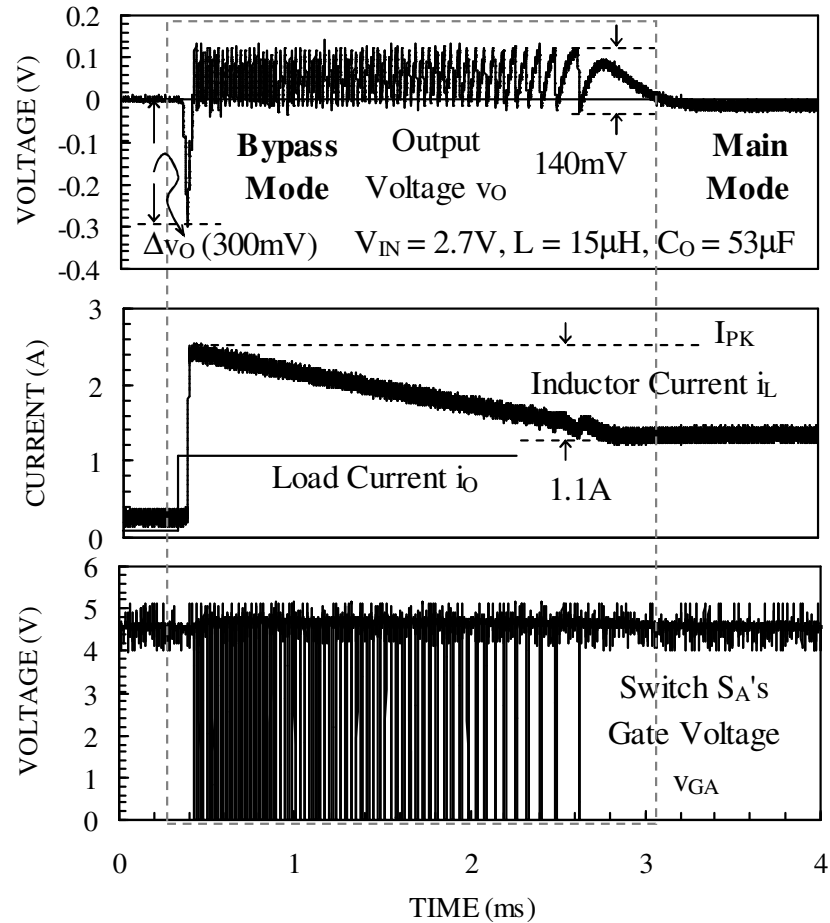


Fig. 7.14. Steady state-to-Bypass and back transitions in response to positive 0.1-0.6A load dumps (positive Δi_O).

The main drawbacks of the auxiliary bypass path are the silicon real estate, power, and switching noise associated with power switch S_A . The latter two shortcomings, however, are more often than not inconsequential because they only occur during transient events, which are typically sporadic, short, and seldom occur without significantly affecting the steady-state power efficiency (Fig. 7.16). During the transition time when the system settles to the main mode, the output voltage is still held within $\pm 1.5\%$ of the output value, an accuracy level suitable for all but the most critical

applications like high-quality audio supplies. The prominent disadvantage of the proposed solution is therefore additional silicon real estate for S_A because it carries substantial current. The transient-performance benefits of S_A and the bypass path that drives it, however, offset this cost. Furthermore, it is expected that in a process with better isolation structures, a single PMOS device can be used without fear of latchup, thus reducing the implemented size of switch S_A as well.

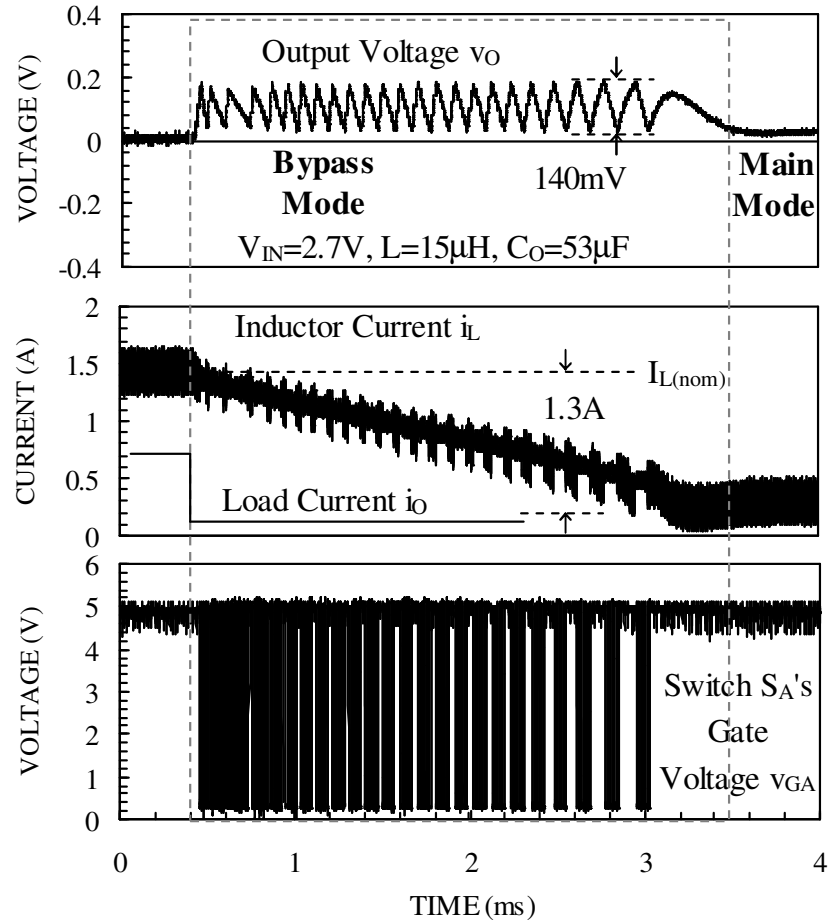


Fig. 7.15. Steady state-to-Bypass and back transitions in response to negative 0.6-0.1A load dumps (negative Δi_O).

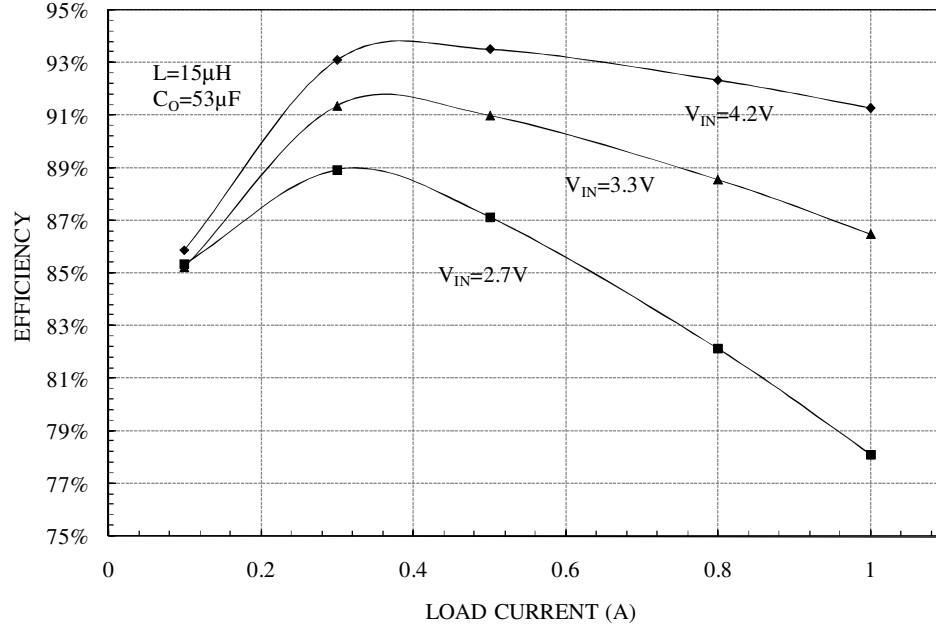


Fig. 7.16. Steady state efficiency with respect to load current I_O for the proposed converter.

7.4. Summary

A dual-mode $\Sigma\Delta$ bypass boost dc-dc controller 0.5 μ m CMOS IC that is stable for an $R_{ESR}LC$ filter range of 0-50m Ω , 1-30 μ H, and 1-350 μ F and responds to positive and negative load dumps in one switching cycle has been proposed, designed, fabricated, and evaluated. The driving feature of the foregoing solution is a robust on-chip (i.e., smooth transitioning) $\Sigma\Delta$ bypass path that responds only during transient load dumps. While the converter increases inductor current i_L in one switching cycle in response to a sudden rise in load current i_O and uses it to quickly slew output capacitor C_O back to its target, it also limits how much of i_L flows to C_O in the case of a negative load dump, when i_O drops, limiting the total transient variation of output voltage v_O and therefore improving accuracy performance. The transient-response benefits of the proposed scheme, as compared to state-of-the-art single-mode $\Sigma\Delta$ converters, are highest at low values of L (e.g., 6x at 1 μ H and 1.41x or 40% improvement at 30 μ H) because L limits how fast i_L rises and falls to its targets. The main drawback of the proposed technique is the

additional silicon real estate required for auxiliary power switch S_A , which is partially (and often completely) offset by its improved accuracy performance. In summary, the proposed dual-mode $\Sigma\Delta$ bypass boost converter is fast, widely LC compliant (robust), and easily implemented.

CHAPTER 8

FINAL SUMMARY AND CONCLUSIONS

With the ever-growing demand for portable electronics, switching dc-dc power supplies that serve as the critical power interface blocks between the portable energy source (i.e., battery) and the electronic circuits (e.g., cell-phones, MP3 players, etc.) have been seeing increasing focus and development efforts. These development efforts concentrate predominantly on realizing dc-dc power converters that are compact, inexpensive, efficient, fast, and easier to build. Switching converters necessarily contain power LC filter devices to filter out the inherent switching noise, and this LC filter is physically bulky preventing its integration on IC's except in very high-frequency, niche applications. Given that, compact and low-component-count power supplies are hindered by the feedback (or frequency) compensation circuit, which has to be located off-chip because it must be designed around the off-chip power filter LC devices beyond the control of the controller IC designer. This hindrance has been preponderant in boost (step-up) dc-dc converters because of the right-half plane (RHP) zero in their control loop.

The basic purpose of this research was to investigate and develop a technique to realize a boost switching dc-dc converter that displays stable performance and good transient response (which in itself is an indicator of the relative stability of the converter), ideally for any value of filter inductor-capacitor LC variations without using an external compensation circuit. In that regard, a dual-loop sigma-delta ($\Sigma\Delta$) control technique was developed for boost dc-dc converters and its design validated via a board-level prototype. The technique was advanced as a dual-mode system compatible with the state-of-the-art $\Sigma\Delta$ techniques, analyzed, and developed in a 0.5 μm CMOS process to validate IC

operation. This chapter summarizes the salient features, key conclusions, and contributions derived in the course of the aforementioned work. Critical tradeoffs in the proposed technique and any resulting application specializations follow. Finally, future work, directions, and potential conceptual developments introduced by this work are presented.

8.1. Conclusions

The introductory chapters reviewed switching converters to illustrate that although at the time intervals close to the switching period the system is non-linear, applying classical control techniques inherently implies linearizing the converter operation. This linearizing essentially applies to frequencies significantly lower than the switching frequency and ignores activities at and close to the switching frequency as a result of the circuit averaging process. As a result, there is a necessary reduction in the control loop bandwidth, limited in the extreme to half of the switching frequency and practically, to a fifth of the switching frequency. Besides, as in any classically controlled negative-feedback system, the control loop experiences an innate tradeoff between the open loop bandwidth or system speed, and loop stability. This is because parasitic poles in the control loop (e.g., due to parasitic capacitances) are located at high frequencies and start adversely influencing the phase and gain margins as the loop bandwidth increases.

In the case of switching converters, the system parameters that predominantly determine loop performance are the LC filter values and their related parasitic elements. Therefore the aforementioned speed-stability tradeoff relates to the worst-case design conditions encountered in the design space defined by variable filter parameters. For a buck dc-dc converter system, the onset of this tradeoff can be pushed to high frequencies very close to the switching frequency; nevertheless, this requires appropriately designing a frequency compensation circuit based on the chosen combination of the filter parameters. To avoid the readjustment of the frequency compensation circuit for every

change in LC values, a process that is impractical in converters with an integrated compensation circuit, and at the same time achieve good speed and stability, there is a need to fundamentally break the bandwidth-stability tradeoff. Such a break is obtained by reverting back to the non-linear origins of switching converters.

Sigma-Delta ($\Sigma\Delta$) or hysteretic control in buck converters provides such a non-linear method that operates essentially at a loop bandwidth equal to the switching frequency. The key feature in such converters is the possibility to have 100% duty-cycle operation for the active or energizing switch, which means that the active switch can remain closed for several consecutive switching cycles. When compared to a classical PWM control scheme, this corresponds to the abnormal situation when the regulating error amplifier is saturated. The situation is very indicative of the state of affairs in the $\Sigma\Delta$ controller, which controls the power stage by slewing its filter elements within a narrow controlled band. As such, the response speed of such a controller is automatically limited by the filter slew rates that represent the maximum speed of response in the converter.

To achieve this slew-limited response, the bandwidth of the feedback path is designed much higher than that of the converter power stage itself thus realizing an output compensated system. Secondly, the feedback gain is high enough to ensure that loop unity-gain bandwidth equals the self-oscillating switching frequency with a zero phase margin. In other words, the control loop is designed to be unstable in the classical sense, but is operated so that while the filter slews in either direction due to its instability, the excursion of the filter output, i.e., the output voltage ripple, is tightly controlled. Clearly, the control loop requires no compensation circuit to regulate the output voltage.

In boost converters, the inductor current is increased independently in a part of the switching cycle when the output voltage is discharged by the load. Hence, an attempt to increase the inductor current leads to a decrease, usually temporary, in the output voltage while the inductor current increases to its higher value. In other words, the increase in the

inductor current is invisible at the output. As such, trying to control the slewing excursions of the output voltage is not the same as controlling the excursions in the inductor current, which can increase or decrease monotonously. Therefore, boost sigma-delta control must necessarily include the inductor current information in the control strategy. However, simply summing the inductor current ripple with the capacitor voltage ripple, although successful in realizing widely filter LC-compliant $\Sigma\Delta$ control, resurrects the aforementioned speed-stability tradeoffs by making the system resemble classical PWM control. The proposed system prevents this resurrection and provides speed without loss in relative stability.

What is proposed, developed, and experimentally validated in this work is a technique to break away from the linear system operation of conventional dc-dc converters by changing the operating mode in the case of transient events. By being able to transition between two different operating modes, the system overcomes the disadvantages of a linearized system while providing the filter compliance of $\Sigma\Delta$ control. The net result is a system that is stable over orders of magnitude variations in the filter values at the same time exhibiting fast, filter slew-limited, single-switching-cycle transient response over the entire filter range, and all this without using any frequency compensation circuit. Such an LC compliant, compensation-free boost dc-dc converter goes a long way towards building a user-friendly, compact, and on-chip power supply.

8.2. Key Contributions

The primary purpose of this work was to investigate fast, self-stabilizing or LC-compliant boost dc-dc converters and develop a converter strategy that meets these conditions. In that regard, the primary contribution of this work is the development of the dual-mode $\Sigma\Delta$ controller IC that displays stable operation and single-switching cycle fast transient response for orders of magnitude variations (1-30 μ H, 1-350 μ F, and 5-50m Ω) in the filter LC and ESR parameters. Simultaneously, single-step transient response enables

the strategy to exhibit over 4-fold improvement in the transient response compared to state-of-the-art $\Sigma\Delta$ techniques. This proposed technique is expected to present a compensation circuit-free solution that would enable a compact power supply with a minimum number of off-chip components at the same time allowing flexibility in LC filter choice and achieving accurate regulation due to high bandwidth.

In addition, in a more general sense, the presented bypass circuit provides an add-on option to an existing converter circuit, with which the transient performance of the resulting converter achieves a single-step response for any value of filter LC values. This benefit is obtained without any deleterious effect on the steady state operation of the circuit. The bypass circuit in itself provides wide LC tolerance; the net LC compliance is limited by the steady-state stability of the converter.

The dual-loop $\Sigma\Delta$ converter from chapter 4 presents an independently operable and simple boost dc-dc converter with the RHP zero eliminated. As a result, the converter is widely stable against filter variations, and as for the aforementioned converters, has single-step transient response. Although this converter suffers from higher than normal steady-state ripple ($\pm 1.7\%$ measured), it has its advantages in low component count and simplicity of design and operation due to the absence of the RHP zero.

In the single-mode $\Sigma\Delta$ converter from chapter 6, a technique was introduced to alleviate the switching frequency variations by using a pole-zero pair in the gain path. Although, the technique does not eliminate frequency variations, the variations are reduced by over 20% without using any additional frequency regulating loops. The method can be, in general, implemented with any $\Sigma\Delta$ controller, and if necessary, augmented with a more comprehensive frequency controlling circuit.

8.2.1. Publications

In the course of the research, three journal papers were submitted, out of which two have been accepted for publication and response is awaited on the third. In addition,

four conference papers were published on various aspects of $\Sigma\Delta$ controllers. Finally, five articles were published in trade journals, out of which one was selected for publication in Electronic Engineering Times and was also translated in Japanese for publication in the Electronic Engineering Times, Japan. These publications are listed below:

Journal Publications

[1] N. Keskar and G.A. Rincón-Mora, "One Clock-Cycle Response 0.5 μ m CMOS Dual-Mode $\Sigma\Delta$ DC-DC Bypass Boost Converter Stable over Wide $R_{ESR}LC$ Variations," submitted to *IEEE Transactions on Power Electronics*.

[2] N. Keskar and G.A. Rincón-Mora, "A Compact 1-30 μ H, 1-350 μ F, 5-50m Ω ESR Compliant, 1.5% Accurate 0.6 μ m CMOS Differential $\Sigma\Delta$ Boost DC-DC Converter," *Analog Integrated Circuits and Signal Processing Journal*, vol. 54, No. 3, pp. 157-169, 2008.

[3] N. Keskar and G.A. Rincón-Mora, "A Fast, Sigma-Delta ($\Sigma\Delta$) Boost DC-DC Converter Tolerant to Wide LC Filter Variations," *IEEE Transactions on Circuits and Systems-II*, accepted for publication.

Conference Publications

[1] N. Keskar and G.A. Rincón-Mora, "Designing an Accurate and Robust LC-Compliant Asynchronous $\Sigma\Delta$ Boost DC-DC Converter," *IEEE International Symposium on Circuits and Systems*, 2007, pp. 549 - 552.

[2] E. Torres, L. Milner, N. Keskar, M. Chen, H. Pan, V. Gupta, P. Forghani, and G.A. Rincón-Mora, "SiP Integration of Intelligent, Adaptive, Self-Sustaining Power Management Solutions for Portable Applications," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2006, pp. 5311-5314.

[3] N. Keskar and G.A. Rincón-Mora, "A high bandwidth, bypass, transient-mode sigma-delta DC-DC switching boost regulator with wide LC compliance," *IEEE Industrial Electronics Conference*, 2005, pp. 543-548.

[4] N. Keskar and G.A. Rincón-Mora, "Self-Stabilizing, hysteretic, boost dc-dc converter," *IEEE Industrial Electronics Conference*, 2004, pp. TA3-4.

Trade Articles

[1] G.A. Rincón-Mora and N. Keskar, "Unscrambling the power losses in switching boost converters" *Power Management Design Line (PMDL)*, August 18, 2006.

[2] G.A. Rincón-Mora and N. Keskar, "Cloaking the non-idealities of DC-DC converter stability" *Planet Analog*, January 20, 2006.

[3] N. Keskar and G.A. Rincón-Mora, "A fast, accurate, LC compliant DC-DC boost regulator...Is it possible?" *Power Management Design Line (PMDL)*, August 22, 2005.

[4] N. Keskar and G.A. Rincón-Mora, "A user-friendly boost DC-DC converter topology," *Electronic Engineering Times Japan*, no. 0, 2005.

[5] N. Keskar and G.A. Rincón-Mora, "A user-friendly boost DC-DC converter topology - it's fast and widely stable," *Planet Analog*, January 26, 2005.

8.3. Tradeoffs in the Proposed Work

The work described in the dissertation so far successfully achieves the desired requirements of filter compliance, i.e., stability and single-cycle fast transient response over orders of magnitude variations in the filter inductor and capacitor values. In realizing these objectives, the system has to tradeoff certain benefits of other converter techniques; however, it is the author's opinion that the benefits greatly outweigh the drawbacks. Nevertheless, the system tradeoffs, due to systemic issues and the circuit implementation, and their solutions and/or alleviations are described below and summarized in Table 8.1.

8.3.1. Switching Frequency Variations

Inherently, asynchronous $\Sigma\Delta$ control consists of a self-oscillating control loop that is not externally driven by a constant frequency clock signal. As such, the switching

frequency, which is also the loop crossover frequency, is determined by the loop gain that in general varies with the terminal voltages and currents, not to mention filter LC parameters. The net result is a widely variable switching frequency over the range of filter values and terminal voltages. The main benefit of this variable switching frequency is the wide LC compliance without the use of a compensation circuit; however, it adversely impacts the design of the electromagnetic interference (EMI) filter placed at the input of the power supply to limit the noise that the converter injects back into the supply lines that are shared by other equipment, which may be sensitive to such injected noise. The EMI filter is designed based on the target value of the switching frequency and hence any variations in the switching frequency can reduce its optimal performance.

Solution and Alleviation: Once the LC filter is chosen, the switch frequency variations are only due to variations in V_{IN} and I_O and are significantly lower than those due to filter variations themselves. Furthermore, these variations are attenuated by the frequency-dependent gains in the current loop as explained in Chapter 6. Additional frequency controlling methods including the use of a variable hysteresis window, variable delay, and/or fixed frequency modulating signal are possible [50]-[52] that reduce frequency variations within $\pm 10\%$ of the nominal value. Finally, even for fixed frequency switching converters, the typical specified frequency variation is approximately 20-25% around the nominal value. Hence, the EMI filter has to be designed for such variations in either a fixed frequency or an asynchronous case.

8.3.2. Additional Switch

In IC technology, economics of the business rely on mass production or the number of die manufactured per wafer of silicon. Hence, a larger die size affects overall cost. Of the area consuming blocks, power switches usually end up the being the culprits since in order to offer low on-resistance, they have to be designed substantially wide. The proposed technique uses an additional power switch S_A and hence has inherently higher

die cost than a standard boost controller IC that does not use this switch. Furthermore, the converter experiences switching activity of the bypass mode in addition to that of the main mode, which is standard in conventional converters. This additional switching results in higher switching noise and output voltage ripple ($\approx \pm 1.5\%$) in the bypass mode. Alleviation: Regarding the effect of die size, it is important to consider the overall system cost, i.e., the cost encountered by a power-supply designed around the controller IC. Such a power supply consists of off-chip components – importantly, the filter LC parameters and the frequency compensation circuit. The cost associated with these components is not only the material cost and the associated inventory costs, but critically also the cost tied to the design time needed to complete a complex system. It is commonly accepted that in general, power supply designers find designing the frequency compensation circuit as the greatest stumbling block. Hence, eliminating the external frequency compensation circuit offers significant cost benefits by reducing design time. At the same time, the choice or combination of external filter LC components expands over orders of magnitude helping in the same role. With regards the additional switching in the bypass mode, the switching noise due to the transients themselves is expected to be equally or more deleterious.

Table. 8.1. Summary of tradeoffs in the proposed research.

	Parameter	Advantage	Drawback	Solution/Alleviation of Drawback
1	Self-Oscillating $\Sigma\Delta$ Control	Filter LC compliance without off-chip frequency compensation	Switching frequency variations with line and load causing EMI concerns	1. Additional switch frequency regulation schemes possible 2. Fixed frequency converters have frequency variation $\approx 20\text{-}25\%$
2	Additional Switch	Fast transient response dependent only on filter slew-rate	Increased die cost	Overall power-supply solution cost reduced due to reduced part count and design complexity

8.4. Future Work and Directions

8.4.1. Circuit and System Variations

During the bypass mode, the inductor current circulates through the switch S_A dissipating conduction power loss in the process. Instead of simply freewheeling, the current could be used more productively to generate a secondary voltage output. In another variation, the capacitor at the output can be replaced by a secondary system source or a battery to obtain regenerative action in the bypass mode (Fig. 8.1(a)). As an alternative, the auxiliary switch can be connected as a part of a secondary output buck supply (Fig. 8.1(b)) that forces the inductor current to be higher than that required to supply the boost converter load i_O . In case of a load step in i_O , the auxiliary switch opens and the extra inductor current supplies the new load requirement. In both the above cases, the secondary supply or output is, in general, less tightly regulated or stringent than the main supply or output.

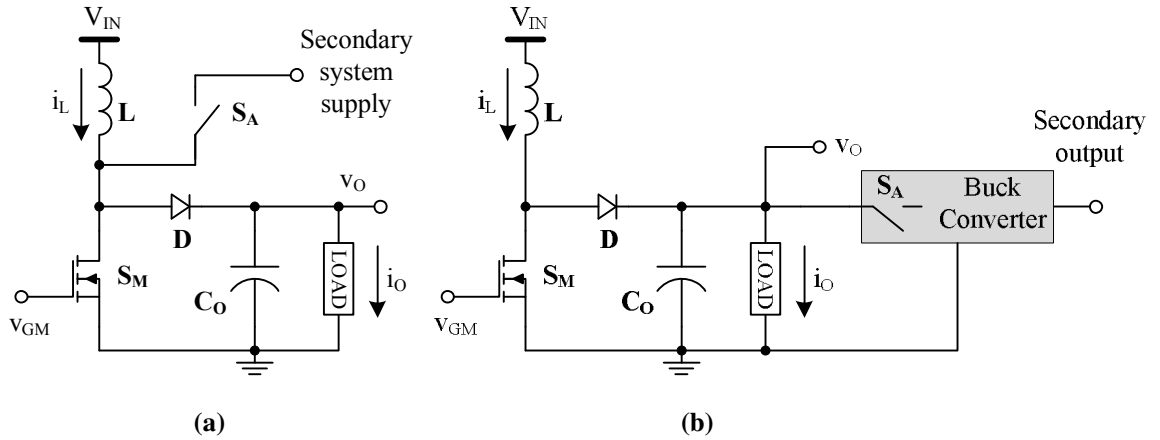


Fig. 8.1. Possible variations of the proposed scheme in a multiple input or multiple output environment where the auxiliary switch S_A can be utilized as part of the (a) inherent secondary/auxiliary supply or (b) secondary output.

8.4.2. Broader Extensions of the Proposed Scheme

In a general sense, the proposed technique presents a scheme where the system transitions to a temporary mode during a transient and settles back down gradually to the

steady-state mode. This principle of the implemented technique can be used in other ways. For example, in a standard PWM converter, an error amplifier compares the sensed output voltage to a reference value to generate the error signal that ultimately is modulated to give the gate signal of switch S_M . In a transient event, this output of the error amplifier can be rapidly clamped in a pseudo-bypass mode to a high or low rail as per high or low duty-cycle requirements. As the regulated output voltage approaches the desired value, the error amplifier output gradually settles down to its new steady-state value.

While the technique has been proposed for a system with an inherent right-half plane (RHP) zero, and indeed, the technique may be more easily adapted to such systems, in a more fundamental form, the proposed principle can be applied in any environment where the bandwidth is normally curtailed to a low value for some other purpose. For example, in a regulated switching current source, the filter inductor that carries the regulated current is bound to be large to maintain low current ripple. Even if such a current regulator is imagined to be of the form of the boost converter described in this work, the regulated inductor current loop itself has no RHP zero. Yet, because of the large inductance, the current loop bandwidth is limited and can be buttressed during transients by using a bypass mode containing a smaller inductor value. Thus, the regulated current bandwidth is temporarily increased at the cost of somewhat higher ripple, while maintaining steady-state operation with the desired filter parameters.

8.5. Summary

The proposed system primarily contributes a technique to break away from the speed-stability tradeoff imposed by the classical control of conventional state-of-the-art boost dc-dc controllers. By temporarily introducing a high-bandwidth $\Sigma\Delta$ mode during transients, stability over orders of magnitude filter variations is achieved, counter intuitively, simultaneously with as much as a 4-fold improvement in transient response.

The benefits of this technique come at the cost of higher silicon area, but it is expected to be compensated by the cost benefits resulting from the design ease and reduced part count. The usage of this method can be extended, in general, to any system whose bandwidth in steady-state is limited to lower values due to other design requirements. In such situations, the presented technique maintains the low bandwidth advantages including filter compliance, while increasing response speed, without any compensation circuit, thus taking a significant step towards a compact, user-friendly, and fully integrated dc-dc converter solution.

APPENDIX A: POWER LOSSES IN SWITCHING BOOST DC-DC CONVERTERS

A.1. Background

In a boost converter (Fig. A.1(a)), switches MN and MP are turned on in a complementary fashion. Since the average voltage across the inductor in steady state must be zero, the average voltage at the phase node V_{PH} is equal to the input voltage V_{IN} . Furthermore, V_{PH} is grounded when switch MN is turned on, hence during the off-time of MN (on-time of MP), V_{PH} must reach a voltage $V_{PK} (> V_{IN})$ to keep its average value equal to V_{IN} . The diode-switch combination (D-MP) along with capacitor C functions as a peak detector that catches this peak voltage V_{PK} into capacitor C, as the converter output voltage V_O . This is seen from the switching waveforms in Fig. A.1(b).

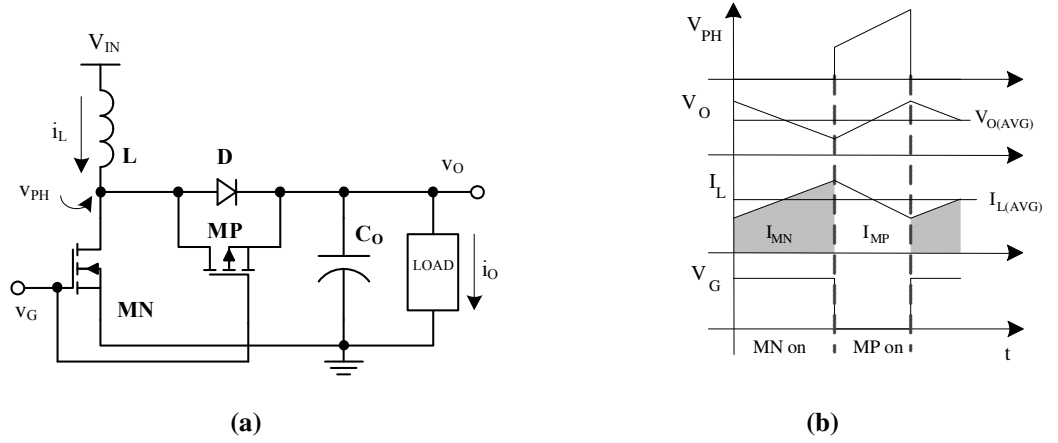


Fig. A.1. (a) Simplified circuit schematic and (b) switching waveforms of a switching boost converter

From Fig. A.1(b), the inductor current flows through MN during the on-time of MN and through MP during the off-time of MN. Broadly, power is lost in this system because of three mechanisms as follows. Firstly, any current flowing through switch or inductor parasitic resistance causes I^2R or conduction losses. Secondly, during the on-off transition time of each switch, the transitioning switch current and voltage overlap giving a non-zero V-I product. Thirdly, the charging and discharging of switch gate capacitances

result in inherent power losses. These loss mechanisms are explained in more detail in the next section.

A.2. Analysis of Power Losses

A.2.1. Conduction Power Loss (I^2R Loss)

The current distribution in various parasitic resistances of a boost converter circuit is shown in Fig. A.2. The equivalent RMS inductor current I_{L-RMS} leading to I^2R losses is composed of a DC component I_{L-AVE} and an ac ripple component I_{L-RIP} . The time for which this RMS inductor current flows through the switch MN is represented as a fraction of the total switching period by the duty-cycle D . In a complementary manner, the inductor current flows through the switch MP for a fraction of the switching cycle represented by $(1-D)$. Since the DC value of the current I_{MP} flows to the load, the DC value of the inductor current is given by

$$I_{L-AVE} = \frac{I_{MP-AVE}}{(1-D)} = \frac{I_O}{(1-D)}. \quad (A.1)$$

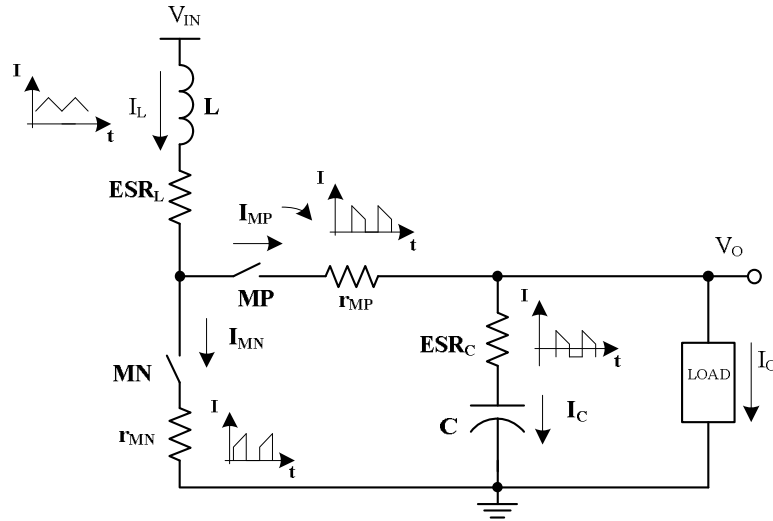


Fig. A.2. Parasitic resistances and current distribution in a boost converter.

The RMS value of the inductor current ripple, which flows through the capacitor C for the fraction (1-D), can be shown to be $I_{L-RIP} = \Delta I / \sqrt{12}$ [2], for a peak-to-peak inductor current ripple of ΔI . Then, the total conduction losses can be decomposed to get a loss component due to the DC value of the inductor current and a loss component due to the RMS value of the ac-ripple of the inductor current, as follows

$$P_{IL-AVE} = I_{L-AVE}^2 ESR_L + D(I_{L-AVE}^2 r_{MN}) + (1-D)(I_{L-AVE}^2 r_{MP}), \text{ and} \quad (A.2a)$$

$$P_{IL-RIP} = I_{L-RIP}^2 ESR_L + D(I_{L-RIP}^2 r_{MN}) + (1-D)(I_{L-RIP}^2 r_{MP}) + (1-D)(I_{L-RIP}^2 ESR_C). \quad (A.2b)$$

A.2.2. Switching I-V Overlap Losses

The gate of switch MN is typically driven by a drive circuit shown in Fig. A.3(a), where the gate resistance R_G represents any gate resistance in series with an ideal buffer, C_{gs} and C_{gd} are the parasitic capacitances of switch MN, and C_d is the combination of any switch capacitance and any other parasitic capacitance at the phase node. For the very short switching transient, the inductor is assumed a current source of value $I_{LA} \pm \Delta I/2$, depending upon whether MN is turning on or turning off.

Typically, C_{gd} is greater than or equal to C_d , in which situation the switching voltage transition is predominantly determined by C_{gd} . Before the turn-on transient (during deadtime), the inductor current flows through the diode D to the output. Voltage V_{PH} across MN is thus clamped by the diode D approximately to V_O . The switch current I_{MN} is directly controlled by gate voltage V_G , which charges through the series R-C combination of $R_G - (C_{gs} + C_{gd})$. Current I_{MN} , which starts rising at time t_1 (Fig. A.3(b)) after V_G exceeds the threshold voltage V_T , increases until it equals the inductor current $I_{LA} - \Delta I/2$ at time t . The diode D is thus starved of current and the switch voltage V_{PH} drops

during the interval t_2 - t_3 . During this interval, negative feedback from the drain to the gate of MN through C_{gd} holds the gate voltage V_G more or less constant to an overdrive above the threshold voltage. After time t_3 , the gate node, which is released from the negative feedback, rises to the gate drive voltage V_P . A similar process takes place in reverse order during turn-off. Power loss due to V-I overlap occurs during the intervals $(t_1$ - $t_3)$ and $(t_4$ - $t_6)$.

For design simplicity in determining the switching times, we make first-order linear approximations. As a result, during time $(t_2$ - $t_1)$, the parallel combination of capacitances C_{gs} and C_{gd} is charged by a constant gate current that is given by the voltage across R_G (which is V_P - $V_G(t_2)$) divided by R_G . After time t_2 up to t_3 , the gate voltage is constant, hence only the capacitance C_{gd} is charged by the same current. Therefore, the turn-on time is given by

$$t_{sw_on} = (t_2 - t_1) + (t_3 - t_2) = \frac{(V_T + V_{OV-ON}) - V_T}{\left(\frac{dV_{gs}}{dt}\right)} + \frac{V_O - 0}{\left(\frac{dV_{gd}}{dt}\right)} \quad (A.3a)$$

$$= \frac{V_{OV-ON} R_G (C_{gs} + C_{gd})}{V_P - (V_T + V_{OV-ON})} + \frac{V_O R_G C_{gd}}{V_P - (V_T + V_{OV-ON})}$$

The process is similar during the turn-off transient, except for the gate-capacitance discharging current, which is now given by a different voltage across R_G (which is $-V_G(t_4)$) divided by R_G . The turn-off time is then

$$t_{sw_off} = (t_6 - t_5) + (t_5 - t_4) = \frac{(V_T + V_{OV-OFF}) - V_T}{-\left(\frac{dV_{gs}}{dt}\right)} + \frac{V_O - 0}{-\left(\frac{dV_{gd}}{dt}\right)} \quad (A.3b)$$

$$= \frac{V_{OV-OFF} R_G (C_{gs} + C_{gd})}{V_T + V_{OV-OFF}} + \frac{V_O R_G C_{gd}}{V_T + V_{OV-OFF}}$$

The total overlap power-loss in switch MN is then given by (shaded area in Fig. A.3(b))

$$P_{\text{SWOL}} = \left[V_O \left(I_{\text{LA}} - \frac{\Delta I}{2} \right) \frac{t_{\text{sw_on}}}{2} + V_{\text{OUT}} \left(I_{\text{LA}} + \frac{\Delta I}{2} \right) \frac{t_{\text{sw_off}}}{2} \right] f_{\text{sw}}, \quad (\text{A.4})$$

where f_{sw} is the switching frequency.

While switch MN incurs V-I overlap losses as above, in the case of switch MP, the diode D always conducts current (during deadtime) before MP is turned on and after MP is turned off, so long as the inductor current does not become negative. Hence, the switching voltage across MP is always clamped to one diode drop V_D . Therefore, in most cases, the overlap power loss in MP can be neglected. Nevertheless, an analysis similar to the one above can be performed for MP after replacing the switching voltage by V_D .

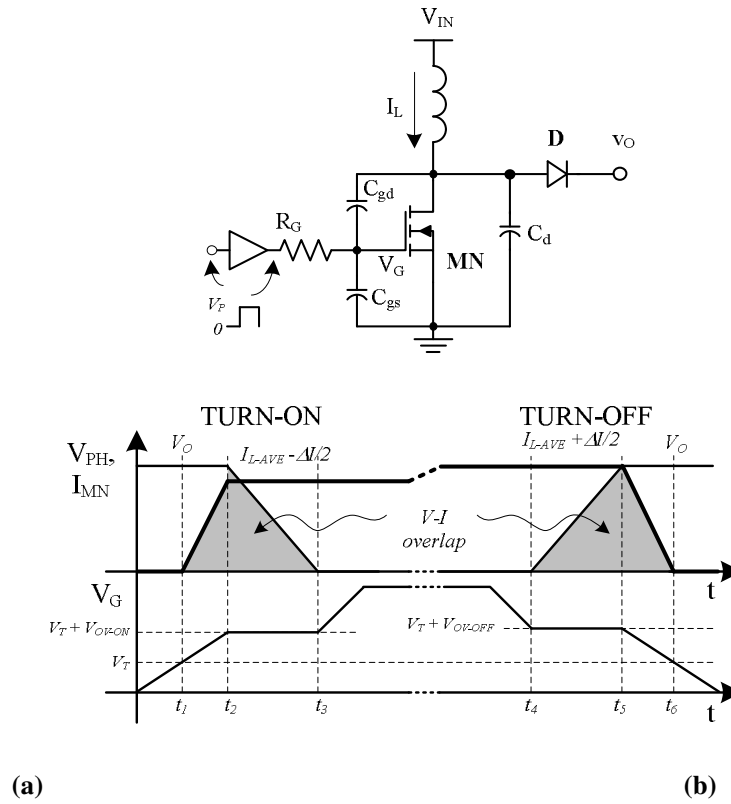


Fig. A.3. Switching analysis for MN showing (a) equivalent circuit and (b) switching waveforms.

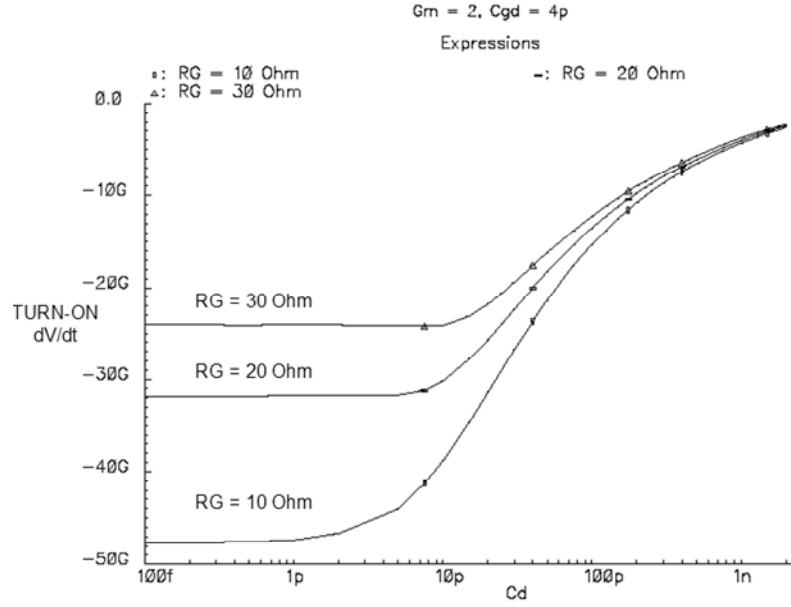


Fig. A.4. Change in turn-on dV/dt of MN as a function of drain parasitic capacitance C_d .

The previous analysis assumed that any parasitic capacitance C_d is less than or equal to C_{gd} . In special cases (snubbers etc.) where C_d is greater than about $5.C_{gd}$, the voltage transition times (t_3-t_2) and (t_5-t_4) increase. As an example, Fig. A.4 shows the change in turn-on dV/dt for a typical switch MN ($G_m = 2S$, $C_{gd} = 4pF$) as a function of the drain capacitance C_d . Until C_d exceeds approximately 5 times C_{gd} , it has negligible effect on the rate of fall of the switch voltage. Beyond this capacitance value, the voltage transition is determined by the slew-rate of C_d .

A.2.3. Gate Drive Losses

There is an inherent energy loss associated with charging and discharging any capacitance through a resistor. Typically, in battery-powered applications, the gate of switch MN is driven by a driver powered from V_{IN} . In that case, during one switching cycle, C_{gs} charges to V_{IN} and discharges back to zero. The capacitance C_{gd} , however, charges to V_{IN} when MN is on and discharges to $-V_O$ when MN is turned off. Similarly,

with the gate of switch MP assumed to be driven by pulses of peak value V_O (which is reasonable for applications up to about 5V), C_{gs} charges and discharges between 0 and V_O , while the voltage across C_{gd} swings from V_O to $-V_O$. The total power lost in charging and discharging gate capacitances is therefore:

$$\begin{aligned}
 P_{GT} &= (\text{Energy lost per cycle}) \times \text{cycles per second} \\
 &= [C_{gsMN} V_{IN}^2 + C_{gdMN} (V_{IN} + V_O)^2 + C_{gsMP} V_O^2 + C_{gdMP} (2V_O)^2] f_{sw} \quad (A.5)
 \end{aligned}$$

APPENDIX B: LOW FREQUENCY ESTIMATE OF TRANSFER FUNCTION OF A HYSTERETIC COMPARATOR (MODULATOR)

B.1. Background

In a $\Sigma\Delta$ buck converter (Fig. B.1) the ripple in the sensed output voltage v_s is regulated within the hysteretic window of the comparator CP_V . It was shown in Chapter 4 that the ripple in the sensed voltage is dominated by the voltage drop across the capacitor ESR (R_{ESR}) caused by the inductor current ripple, which is triangular. Therefore, the following analysis assumes that the output voltage ripple is triangular. Although the analysis is performed for this converter, the involved principles can be generally applied to similar converters where the regulated waveform has a triangular ripple, for example, the current loop in the $\Sigma\Delta$ boost converter in Fig. 4.4.

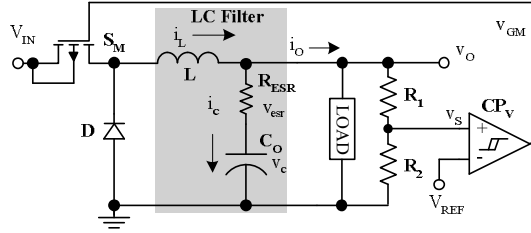


Fig. B.1. Circuit schematic of a $\Sigma\Delta$ buck converter.

B.2. Small-Signal Analysis

The sensed voltage, regulated within the hysteretic window V_{hyst} is shown in Fig. B.2. The rising and falling slopes of the triangular ripple, denoted by M_{on} and M_{off} respectively, together with hysteresis window, determine the operating frequency f_{sw} and duty-cycle D_M :

$$f_{sw} = \frac{1}{t_{on} + t_{off}} = \frac{1}{V_{hyst}/M_{on} + V_{hyst}/M_{off}} = \frac{1}{V_{hyst}} \frac{M_{on} \cdot M_{off}}{M_{on} + M_{off}}, \quad (B.1)$$

$$D_M = \frac{t_{on}}{t_{on} + t_{off}} = \frac{M_{off}}{M_{on} + M_{off}}, \quad (B.2)$$

where t_{on} and t_{off} that represent the on and off times of switch S_M , are as indicated in Fig.

B.2.

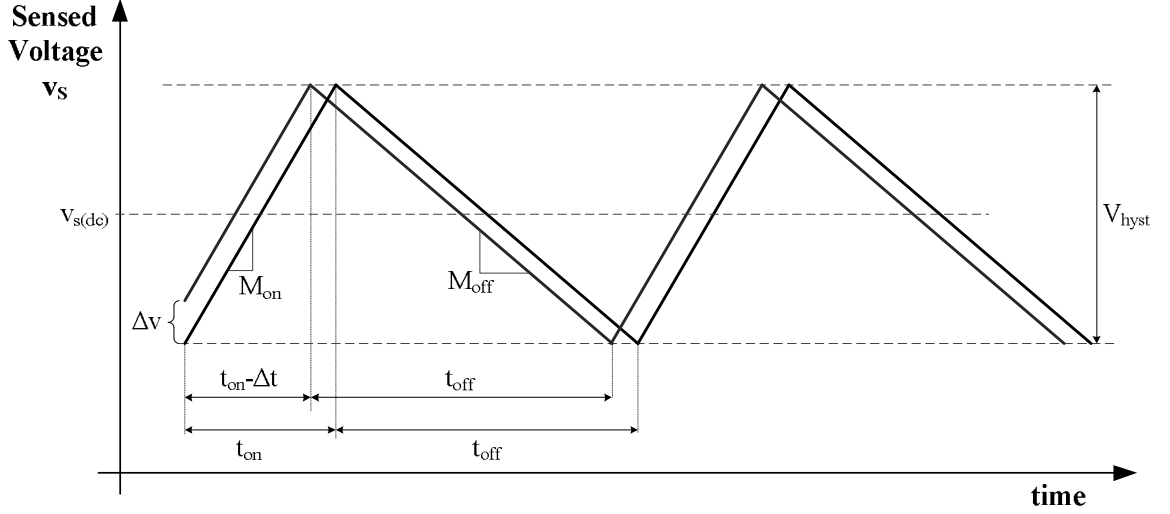


Fig. B.2. Waveforms showing triangular sensed voltage ripple and change in the rise time following a low-frequency, small-signal perturbation Δv in the sensed voltage.

For a small-signal perturbation Δv (Fig. B.2) in the sensed voltage v_s at a frequency much lower than the switching frequency, the time t_{on} changes for the next switch cycle by an amount Δt , leading to a small change in the duty-cycle d such that:

$$D_M + d_m = \frac{t_{on} - \Delta t}{t_{on} - \Delta t + t_{off}} = \left(\frac{t_{on} - \Delta t}{t_{on} - \Delta t + t_{off}} \right) \left(\frac{t_{on} + \Delta t + t_{off}}{t_{on} + \Delta t + t_{off}} \right) \approx \frac{t_{on}(t_{on} + t_{off}) - \Delta t \cdot t_{off}}{(t_{on} + t_{off})^2}, \quad (B.3)$$

where the approximation results from the small-signal assumption following which, any terms containing higher powers of Δt are ignored. Equation (B.3) can be further simplified to give

$$D_M + d_m \approx \frac{t_{on}(t_{on} + t_{off}) - \Delta t \cdot t_{off}}{(t_{on} + t_{off})^2} = \frac{t_{on}}{t_{on} + t_{off}} - \frac{\Delta t \cdot t_{off}}{(t_{on} + t_{off})^2} = D_M - \frac{\Delta t \cdot (1 - D_M)}{t_{on} + t_{off}}. \quad (B.4)$$

But, by observation from Fig. B.2, the change Δt in t_{on} is simply the ratio of the initial voltage perturbation Δv and the slope M_{on} , thus simplifying equation (B.4) to

$$d_m = \frac{\Delta v \cdot (1 - D_M)}{M_{on} \cdot (t_{on} + t_{off})} = \frac{\Delta v (1 - D_M)}{\left(\frac{V_{hyst}}{t_{on}} \right) (t_{on} + t_{off})} = \Delta v \frac{D_M (1 - D_M)}{V_{hyst}}. \quad (B.5)$$

Finally, the modulator transfer function is:

$$\frac{d_m}{\Delta v} = \frac{D_M (1 - D_M)}{V_{hyst}}. \quad (B.6)$$

Thus, the modulator gain is inversely proportional to width of the hysteretic window. The same expression can also be derived by recognizing that the switching frequency (equation B.1) in self-oscillating control corresponds to the unity-gain frequency of the control loop and knowing all the components of the loop gain other than the modulator gain. The relationship in equation (B.6) also applies to the main mode of the proposed $\Sigma\Delta$ converter in Chapter 7, where the current loop dominates the voltage loop.

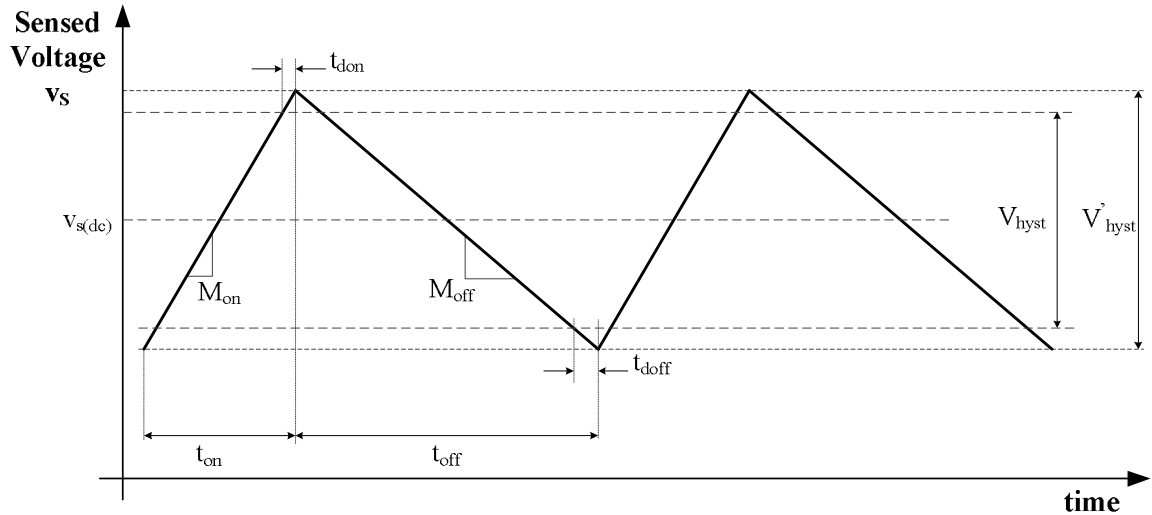


Fig. B.2. Waveforms showing triangular sensed voltage ripple and change in the rise time following a low-frequency, small-signal perturbation Δv in the sensed voltage.

In the presence of switching, comparator delays, etc., the ripple in the sensed voltage extends beyond the limits set by the hysteretic window V_{hyst} . As shown in Fig. B.2, the switching turn-on and turn-off delays t_{don} and t_{doff} effectively increase the width of the hysteretic window to a larger value V'_{hyst} , which reduces the modulator gain:

$$\frac{d_m}{\Delta v} = \frac{D_M (1 - D_M)}{V'_{\text{hyst}}} = \frac{D_M (1 - D_M)}{V_{\text{hyst}} + M_{\text{on}} \cdot t_{\text{don}} + M_{\text{off}} \cdot t_{\text{doff}}} . \quad (\text{B.7})$$

In terms of the loop gain, this reduction in modulator gain reduces the overall loop-gain and hence the unity-gain frequency, which is also the switching frequency in self-oscillating converters. Therefore, switching delays lead to a decrease in the switching frequency. Furthermore, for the same time delays, the effective hysteresis window V'_{hyst} is wider for higher values of the ripple slopes M_{on} and M_{off} . In the case of the $\Sigma\Delta$ buck converter with high capacitor ESR, slopes M_{on} and M_{off} are proportional to the inductor current ripple slopes that are inversely dependent on the inductor value itself. Hence, the reduction in switching frequency due to delays is more significant for smaller inductors than for larger ones because the slopes M_{on} and M_{off} are steeper. Finally, the modulator gain is the highest when the product of the duty-cycle and its complement is at its maximum value when the slopes M_{on} and M_{off} are equal to each other.

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