GEORGIA INSTITUTE OF TECHNOLOGY — OFFICE OF CONTRACT ADMINISTRATION

PROJECT ADMINISTRATION DATA SHEET

[X] ORIGINAL [ ] REVISION NO. _____

Project No. E-21-F10 (R6229-0A0) GTRC/~~GTX~~ DATE 10/20/86

Project Director: Dr. Phillip E. Allen School/~~Lab~~ EE

Sponsor: Semiconductor Research Corporation

Type Agreement: Contract No. 86-08-091

Award Period: From 9/1/86 To 8/31/87 (Performance) 10/30/87 (Reports)

Sponsor Amount:	This Change	Total to Date
Estimated:	$ 124,741	$ 124,741
Funded:	$ 124,741	$ 124,741

Cost Sharing Amount: $ None Cost Sharing No: N/A

Title: Analog CAD Methodology

ADMINISTRATIVE DATA

OCA Contact Brian J. Lindberg X4820

1) Sponsor Technical Contact:

Dr. Ralph K. Cavin
Semiconductor Research Corporation
P. O. Box 12053
Research Triangle Park, NC 27709

2) Sponsor Admin/Contractual Matters:

Richard LaScala
Manager, Contracts and Grants
Semiconductor Research Corporation
4501 Alexander Drive-Suite 301
Research Triangle Park, NC 27709
(919) 541-9400

Defense Priority Rating: N/A Military Security Classification: N/A
(or) Company/Industrial Proprietary: N/A

RESTRICTIONS

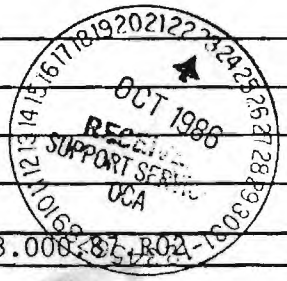
See Attached N/A Supplemental Information Sheet for Additional Requirements.

Travel: Foreign travel must have prior approval – Contact OCA in each case. Domestic travel requires sponsor approval where total will exceed greater of $500 or 125% of approved proposal budget category.

Equipment: Title vests with Sponsor for all Equipment with Value of $1,00 or more.

COMMENTS:

Follow-on to Project E-21-632.



SPONSOR'S I. D. NO. 02.218.008-87.R02-1

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FORM OCA 65:285

GEORGIA INSTITUTE OF TECHNOLOGY OFFICE OF CONTRACT ADMINISTRATION

SPONSORED PROJECT TERMINATION/CLOSEOUT SHEET

SA993

Date 2/24/88

Project No. E-21-F10 School/~~Lab~~ EE

Includes Subproject No.(s) N/A

Project Director(s) P. E. Allen GTRC/~~GIT~~

Sponsor Semiconductor Research Co.

Title ~~Analog~~ Analog CAD Methodology

Effective Completion Date: 8/31/87 (Performance) 10/30/87 (Reports)

Grant/Contract Closeout Actions Remaining:

- [ ] None
- [x] Final Invoice or Copy of Last Invoice Serving as Final
- [ ] Release and Assignment
- [x] Final Report of Inventions and/or Subcontract:
  Patent and Subcontract Questionnaire sent to Project Director [x]
- [ ] Govt. Property Inventory & Related Certificate
- [ ] Classified Material Certificate
- [ ] Other _____

Continues Project No. _____ Continued by Project No. _____

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SRC REPORT/PUBLICATION SUBMISSION FORM

Please complete this form for all reports and publications submitted to SRC.

PRODUCED UNDER SRC CONTRACT? Yes/No/(In Part) SRC CONTRACT #: 84-07-051
OTHER SOURCES OF SUPPORT? _____

NAME OF PERSON RESPONSIBLE

Phillip E. Allen
Schlumberger Professor

NAME AND ADDRESS OF ORGANIZATION

Georgia Institute of Techology
School of Electrical Engineering
Atlanta, GA 30332

REPORT TITLE

Quarterly Report, September 1, 1986 to December 31, 1986

REPORT AUTHOR(S)

Phillip E. Allen

TYPE OF REPORT	TIME COVERED (if applicable)	REPORT DATE	PAGE COUNT	DATE SUBMITTED TO SRC
X Qtrly Progress _ Annual Report _ Final Report _ Thesis	FROM: 09/1/86 TO : 12/31/86	02/03/87	8	

_ Pub.Preprint - submitted to ... _____ date: _____
_ Presentation - presented at ... _____ date: _____

_ Other - please describe ..... _____

ABSTRACT OF CONTENTS OF THIS SUBMISSION (not to exceed one single spaced page)

This report covers the progress made on the development of a multi-level analog integrated CAD design during the Fall 1986 Quarter. A cell compiler is being developed which can be incorporated into the AIDE2 program for the automated component design. Three methodologies to model the output conductance of short-channel MOS devices were explored and the table look-up approach with the cubic spline interpolation methods was found to be the best method to model the output conductance. An algorithm was developed to calculate the time domain response and a synthesis program was developed for the two-state unbuffered op amp using an algorithmic approach.

SUBJECT KEYWORDS (circle keywords supplied on reverse - note any additions)
LIST A: Analog, CAD, CMOS LIST B: IC/CAD Tools, auto. layout, dev. modeling

* * * F O R S R C U S E O N L Y * * *

DATE RECEIVED: _____ SRC PUBLICATION ID: _____

GEORGIA INSTITUTE OF TECHNOLOGY
SCHOOL OF ELECTRICAL ENGINEERING
ATLANTA, GEORGIA 30332

ELEPHONE: (404) 894- 6251

February 6, 1987

MEMORANDUM

TO: Ralph K. Cavin, III, Director of Design Sciences, SRC

FROM: Phillip E. Allen, School of EE, Georgia Tech

RE: Quarterly Report, Sept. 1, 1986 to Dec. 31, 1986, SRC Project No. 84-07-051: "Analog CAD Methodology"

Introduction

This report covers the period from Sept. 1, 1986 to Dec. 31, 1986, for the SRC sponsored research program at Georgia Institute of Technology titled, "Analog CAD Methodology". The objective of this program are listed as follows:

1. Development of performance oriented analog CAD tools.

2. Development of models, multilevel, and mixed-mode simulators for analog VLSI circuits.

3. The development of a means for circuit testability and fault diagnosis.

4. Development of high level analog design programs.

These objectives are the results of previous research in developing a base for undertaking research in analog CAD methodology. This research has the objective to reduce the design time of analog integrated circuits, increase the chance of successful design, and extend the design of analog integrated circuits to the systems designer.

Organization of This Quarterly Report

Each of the individuals working on this research program have written a one page summary of their efforts this quarter. These summaries follow this page. The research topic and students are listed as follows:

AIDE2 Research Activities - Seong K. Hong
Precision Small Signal Models for CMOS Technology - Kwang Yoon
Multilevel Simulation of Analog Circuits - John Parish
Automated Design of Analog Integrated Circuits - Juvena Loo

A list of SRC expenditures is given on the last page.

AIDE2 Research Activities

Seong K. Hong

Quarterly Report for Fall 1986

RESEARCH ACTIVITIES

A cell compiler is being developed which can be incorporated into AIDE2 program for the automated component design. With the component generation technique which is called parameter preprocessing provided by AIDE2, components are designed in a geometric format which allows software controllable operators. Fig 1. shows the cell compiler organization. The parameter preprocessor allows data from circuit description and library cell to be modified by software. This technique has several advantages as follows:

1. The simulation file may be parameterized;
2. The circuit may be optimized by modifying the software operator values;
3. Selective parts of the circuit may be preprocessed.

For multiple level circuit descriptions, the user must be able to interconnect low level components with high level circuits produced by synthesis interface with AIDE2. The hierarchical organization allows for a multilevel user interface in which a circuit description may specify the interconnection of standard cells, parameterized cells and synthesis interface. This access is provided through a library of description routines and geometric components. The layout control capability includes the interconnection of an entire system or low level design, layout and abstraction of basic components.

Also, the cell compiler aspect of the AIDE2 research should address the problem of permitting entry cells using new or different technologies to be implemented into AIDE2 library.

PUBLICATION AND PRESENTATION

On August 1986, a paper titled "Physical testability of analog integrated circuits designed by using AIDE2" was presented at the 29th midwest symposium on circuits and systems at Lincoln, Nebraska. A copy of this paper is appended to this report.

Mr. Munday, from IMP, visited on December 11 and we explained and demonstrated the general features of the AIDE2 program, the cell compiler and testability aspects.

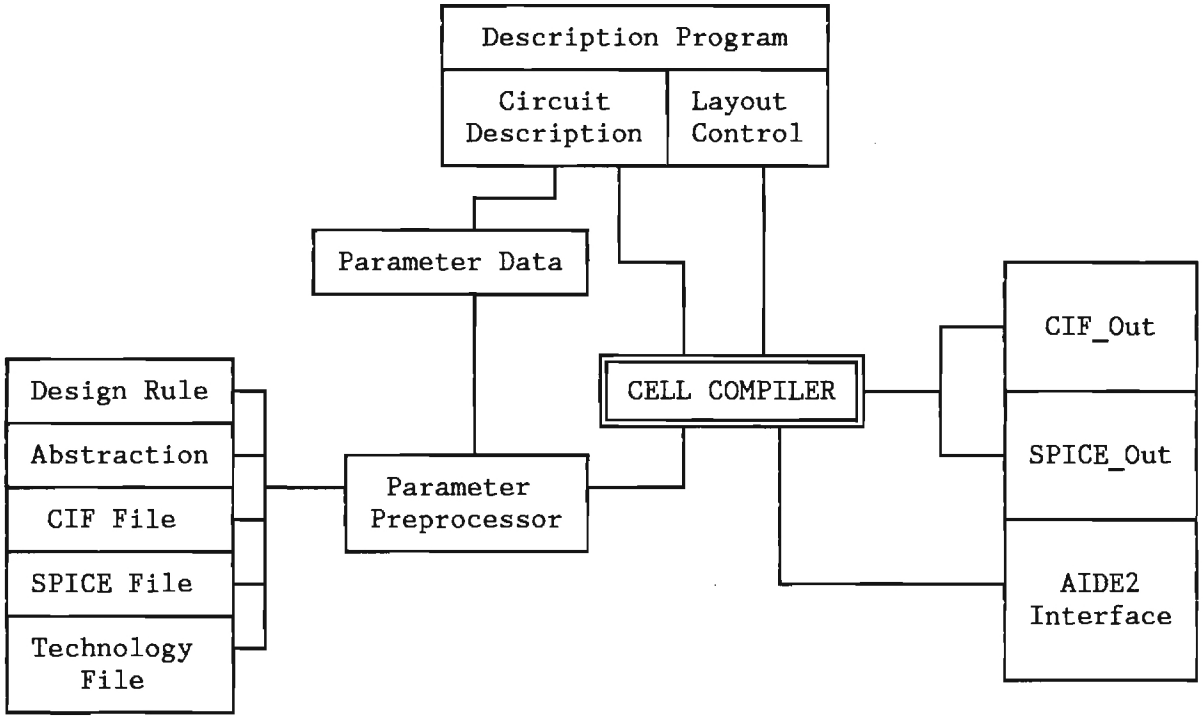

Fig 1. CELL COMPILER ORGANIZATION

Precision Small Signal Models for CMOS Technology

Kwang Yoon

Quarterly Report For Fall, 1986

The three methodologies to model the output conductance of short-channel MOS devices were explored: (1) Analytical, (2) Empirical, and (3) Table look-up approach.

Of three approaches, the table look-up approach with the cubic spline interpolation methods was turned out to be the best way to model the output conductance and it produced the simulated data within 6 % of rms error with respect to the experimental data. This approach may be applicable to the modeling of both transconductance and substrate transconductance. Scaling factor of three small-signal conductances should be also examined and identified, if any. In order to investigate the scaling factors, the graphs of small-signal conductanes as a function of many variables such as terminal voltages, drain current, and so on are being used.

The layouts for MOSIS 1.6 um process were done which included (1) the individual long-channel and short-channel devices for NMOS and PMOS, (2) three CMOS push-pull inverters with three different channel lengths, (3) two CMOS operational amplifiers with the channel lengths of 1.6 um and 3.2 um, (4) test structures to measure the short-channel and long-channel capacitances such as C_{GD}, C_{GS}, and C_{GB}. The CMOS inverters and operational amplifiers will be used for the benchmark of the modeling of small-signal conductances and capacitances after the development of the short-channel small-signal parameters.

Multilevel Simulation of Analog Circuits

John T. Parish

Quarterly Progress Report for Fall 1986

During the spring quarter, a graphical analysis program was reported which finds network functions in the frequency domain. In the fall quarter, an algorithm was developed to calculate the time domain response. The algorithm performs the simulation of networks described as rational functions in the complex frequency variable s. An inverse Laplace transform is calculated. To get the transform, a partial fraction expansion is performed, and then the terms of the expansion are identified with functions of time. The algorithm requires initial condition data for the modeled network, in order to complete the solution. Polynomials with repeated roots are allowed in the network function. This algorithm is currently being coded. When complete, the time domain response program will be one of the routines in a software tool for the solution of large networks. The time domain response, calculated from a subnetwork described in the frequency domain, will be used in a waveform relation algorithm calculating transient response.

Automated Design of Analog Integrated Circuits

Juvena W. Loo

Quarterly Report for Fall 1986

Objective: Applications of artifical intelligence techniques to analog integrated circuit design.

Accomplishments: Development of a synthesis program for the two-stage unbuffered opamp using an algorithmic approach. The design procedure incorporates several categorical parameters such as DC gain, unity gain bandwidth, input common mode range, load capacitance, slew rate, settling time, output voltage swing, and power dissipation. Noise effects, however, are not taken into account. The program is written in Pascal and has been installed on the Vax, MicroVax, Amiga, and IBM PC.

Plans: Development of synthesis program for the two-stage cascode operational amplifier.

Presentations: Demonstration of the program for the unbuffered operational amplifier to Mr. Munday of IMP, England.

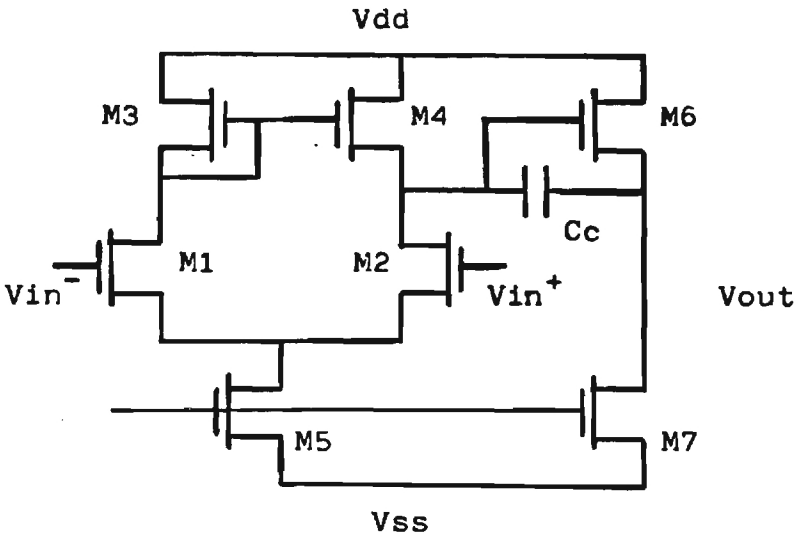

Figure 2 An Unbufferred two-stage CMOS Opamp

	Type	Size
M1	NMOS	67U/6U
M2	NMOS	67U/6U
M3	PMOS	5U/5U
M4	PMOS	5U/5U
M5	NMOS	18U/6U
M6	PMOS	617U/6U
M7	NMOS	898U/6U

	Specifications	Simulations
DC Gain	2000	4600
Unity Gain Bandwidth	3 MHz	3.5 MHz
Slew Rate	5 V/us	4.8 V/us
Phase Margin	--	75^{o}
Input Common Mode Voltage	$\pm$ 3 V	--
Output Voltage Swing	$\pm$ 4 V	--
Power Dissipation	20 mW	14.4 mW
Load Capacitor	20 pf	--
Itail	22 uA	26 uA
Power Supply	$\pm$ 5 V	--
Input Offset Voltage	--	0.3 mV

Table 2a Specifications and Simulation Results for the opamp of Figure 2

SRC EXPENDITURES

Fall Quarter 1986

	Sept. '86	Oct. '86	Nov. '86	TOTAL
Personal Services	$3,175.00	$3,739.00	$ 7,620.00	$14,534.00
Fringe Benefits	1,115.00	118.00	-	1,233.00
Materials & Supplies	43.00	1,276.00	-	1,319.00
Travel	-	-	-	-
Computer	-	-	-	-
Overhead	2,752.00	3,259.00	4,839.00	10,850.00
TOTALS	$7,085.00	$8,392.00	$12,459.00	$27,936.00

SRC REPORT/PUBLICATION SUBMISSION FORM

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PRODUCED UNDER SRC CONTRACT? Yes/No(In Part) SRC CONTRACT # 84-07-051
OTHER SOURCES OF SUPPORT? Schlumberger Chair Funds and GT E-Funds and GE Grant

NAME OF PERSON RESPONSIBLE
Phillip E. Allen
Schlumberger Professor

NAME AND ADDRESS OF ORGANIZATION
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, GA 30332

REPORT TITLE

Quarterly Report, December 1, 1986 to Feb. 28, 1987, "Analog CAD Methodology"

REPORT AUTHOR(S)

Phillip E. Allen, Seong Hong, Juvena Loo, Kwang Yoon, John Parish, Malsook Yu, Harry Li, Terry Groom

TYPE OF REPORT (check one)	PERIOD COVERED (if applicable)	REPORT DATE	NUMBER OF PAGES	DATE SUBMITTED TO SRC
x Quarterly Progress __ Annual Report __ Final Report __ Thesis	FROM ~~12/01/86~~ TO 02/28/87	~~5/12/87~~	_____	_____

__ Publication Preprint
to be submitted to _____ date _____
__ Presentation
to be presented at _____ date _____

__ Other (please describe) _____

ABSTRACT OF CONTENTS OF THIS SUBMISSION (not to exceed one single spaced page)

This report covers the activities and progress of the SRC Project No. 84-07-051 during the winter of 1987. A synthesis program for generating an op amp is being developed. This program will compute a set of W/L ratios for one of four different op amp topologies. Modification of the ADDAC test cells to conform with MOSIS process parameters and design rules was successfully completed. The new MOSIS ADDAC cells were implemented into AIDE with no major problems and have given ADDAC users the option of choosing the fabrication process in which to layout the A/D. Work has begun on the update of the Programmer's Manual for the AIDE2 program. A cell compiler is being developed which can be incorporated into the AIDE2 program for automated component design. It is based on the procedural component generation technique which is called parameter preprocessing provided by AIDE2. A 3-dimensional table look-up model for a large signal model was developed using the piecewise hermite cubic spline interpolation technique which produces monotonous drain current curve and its continuous first derivative. Further progress was made in several sections of the Multilevel Analog Simulator (MAS) which performs response computations for analog networks at intermediate levels of design. Solving example networks determined the computer resource usage of the graphical analysis program (GAP). Algorithms for computing transients from network functions were tested and compared.

SUBJECT KEYWORDS (circle keywords supplied on reverse - note any additions)
LIST A: Analog, CAD, CMOS LIST B: IC/CAD Tools, auto. layout, dev. modeling

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SCHOOL OF ELECTRICAL ENGINEERING
ATLANTA, GEORGIA 30332

TELEPHONE: (404) 894-6251

May 14, 1987

MEMORANDUM

TO: Ralph K. Cavin, III, Director of Design Sciences, SRC

FROM: Phillip E. Allen, School of EE, Georgia Tech

RE: Quarterly Report, Dec.. 1. 1986 to Feb. 28, 1987, SRC Project No. 84-07-051: "Analog CAD Methodology"

Introduction

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2. Development of models, multilevel, and mixed-mode simulators for analog VLSI circuits.
3. The development of a means for circuit testability and fault diagnosis.
4. Development of high level analog design programs.

These objectives are the results of previous research in developing a base for undertaking research in analog CAD methodology. This research has the objective to reduce the design time of analog integrated circuits, increase the chance of successful design, and extend the design of analog integrated circuits to the systems designer.

Organization of This Quarterly Report

Each of the individuals working on this research program have written a one page summary of their efforts this quarter. These summaries follow this page. The research topic and students are listed as follows:

Analog Integrated Circuit Design Automation	Juvena W. Loo
AIDE2 Research Activities	Seong K. Hong
Analog Integrated Circuit Design 2	Malsook Yu
ADDAC	Terry Groom & Harry Li
Analog Small Signal Model for Submicron MOS Devices	Kwang Yoon
Winter Quarter Multilevel Analog Simulator Research	John Parish

A list of SRC expenditures is given on the last page.

Analog Integrated Circuit Design Automation

Juvena W. Loo

Winter 1987

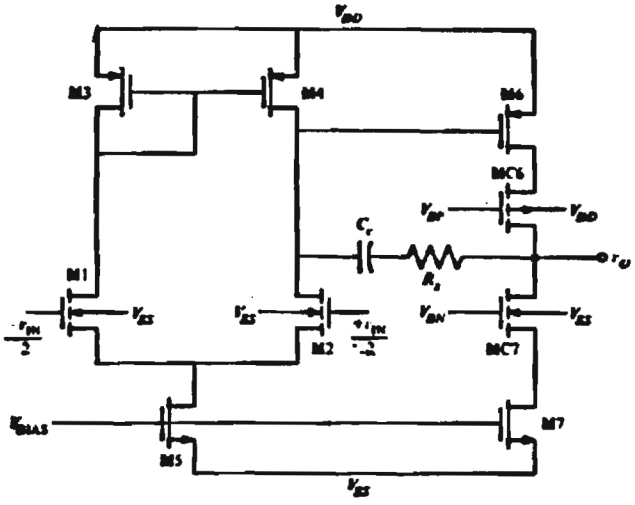
A synthesis program for generating an opamp is being developed. This program will compute a set of W/L ratios for one of four different opamp topologies (Figure 1). The required inputs to the program are as follows:

DC gain (Av)
Gain-bandwidth (GB)
Input CMR (Vin)
Output Voltage Swing (Vout)
Load Capacitance (CL)
Slew Rate (SR)
Power Supplies (Vdd and Vss)

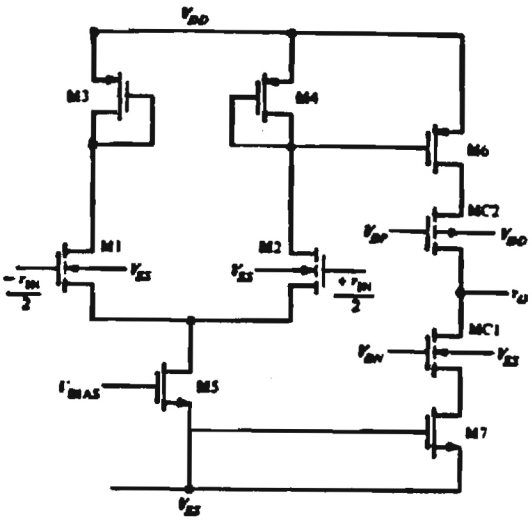
The program selects a suitable configuration by assigning various weights to the four circuits according to the input specification. After the value function finishes its calculations, the circuit with the highest score is chosen. Once a topology is selected the calculations are carried out.

The synthesis program also has a self-adjusting algorithm. There are two levels of parameters the program can modify whenever any specification(s) are not satisfied. The first level is varying the drain-to-source voltages to correct the unsatisfied constraints. If the requirements are still not met, the second level of parameter is being changed. At this level, the bias current of the differential amplifier is altered.

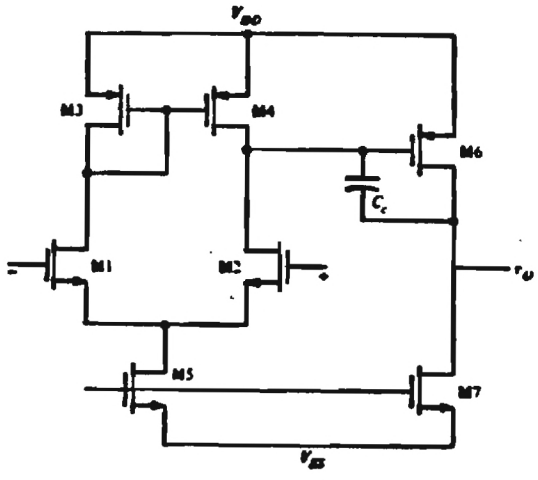
At the present time, the program is still under development and is expected to be completed by June, 1987.



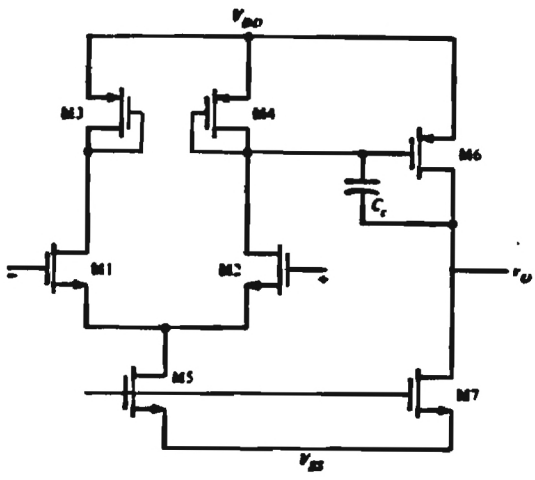
circuit "B"



circuit "D"



circuit "A"



circuit "C"

Figure 1 The four topologies used by the synthesis program

AIDE2 Research Activities

Seong K. Hong

Winter 1987

RESEARCH ACTIVITIES

A cell compiler is being developed which can be incorporated into the AIDE2 program for the automated component design. It is based on the procedural component generation technique which is called parameter preprocessing provided by AIDE2. This technique offers the possibility to describe flexible components by expressions and parameters and to adapt designs quickly to different foundry design rules. Components are designed in a geometric format which allows software controllable operators.

Also, the cell compiler aspect of the AIDE2 research is now addressing the problem of permitting entry cells using new or different technologies to be implemented into the AIDE2 library. This can be implemented by allowing the AIDE2 program to take its technology description information from a technology file in an internal library and altering or replacing the files to represent different fabrication technologies at different installations.

PRESENTATION

Mr. Joe Wilde, from HARRIS Semiconductor Co.. visited on February 19 and we explained and demonstrated the general features of the AIDE2 program and the cell compiler.

Analog Integrated Circuit Design 2

MalSook Yu

Winter 1987

Accomplishments

My main goal was to get acquainted with the AIDE2 program, UNIX operating system, and other necessary programs required to understand the operation of the computer aided design systems here at Georgia Tech.
This was accomplished by :

1. Implementing fixed cells in a third order elliptical low pass filter design.
2. Writing C description input files for the AIDE2 program.
3. Learning how to use and operate the AIDE2 program.

Plans

My main goal is to write the Programmers Manual for the AIDE2 program and to make modifications of the AIDE2 program. Also, to make changes in AIDE2 which will allow better performance in the resulting circuits.

ADDAC
Terry Groom and Harry Li
Winter 1987

Accomplishments

The goals for Winter quarter of 1987 were the following:

1. The modification of the ADDAC test cell to conform with MOSIS process parameters and design rules.

2. To modify fixed ADDAC cells to conform with MOSIS process parameters and design rules. This included the Successive Approximation Register and comparator block.

3. To design and simulate a new comparator block for higher performance and smaller die size.

4. Implement new MOSIS ADDAC cells into AIDE2.

The original ADDAC cells were layed-out using the Harris 5 um process design rules. Modifying the cells required surrounding all P diffusions with a P+ select ring. Since the Harris process did not require a P+ select ring but allowed an entire layer to be designated for the guard rings, all the P wells had to be totally restructured in order for the MOSIS guard rings to meet the design rules of the MOSIS process.

The new comparator block was deemed neccesary due to a potential yield problem caused by a high sensitivity to device mismatch. This sensitivity had the potiential to cause the device to be nonfunctional. This problem was corrected and the end result was a smaller device with higher performance.

The new MOSIS ADDAC cells were implemented into AIDE with no major problems and have given ADDAC users the option of choosing the fabrication process in which to layout the A/D.

Plans

Spring quarter goals include converting parameterized cells to meet MOSIS requirements, as well as, gaining an understanding of the programming involved with entering a parameterized cell into AIDE2, simulating the converter performance at the transistor level using SPICE in order to discover the limitations associated with the design, and if time permits, using an extractor to determine the effects of parasitic resistances and capacitances of the layout on circuit performance.

Simulating a large circuit using SPICE will no doubt give rise to convergence problems. If SPICE is not successful, then SPLICE will be considered as well as investigating a macromodel for the A/D converter.

Analog Small Signal Model for Submicron MOS Devices

Kwang S. Yoon

Winter 1987

Goal of this quarter: To develop the table look-up models for large signal and small signal models

Progress: Since MOS devices operates on three bias voltages(VDS, VGS, VBS), 3-dimensional table models with scaling factors related to device geometries(channel length and channel width) should be developed. A 3-dimensional table look-up model for a large signal model was developed using the piecewise hermite cubic spline interpolation technique which produces monotonous drain current curve and its continuous first derivative. The model developed was computer efficient and accurate. The scaling factors between devices with differnt geometries were investigated. If scaling factors of drain current are identified and implemented into table models, a small signal model will be developed based on the large signal table look up model.

Difficulties to achieve goal:

To identify the scaling factors between devices, all the devices had to be measured to find out which devices have the typical large signal characteristics. Using only devices with typical characteristics, scalings between different devices were explored.

Winter Quarter Multilevel Analog Simulator Research

John Parish

Winter 1987

The objective of the Multilevel Analog Simulator (MAS) is to perform response computations for analog networks at intermediate levels of design. Winter Quarter research made progress in several sections of the MAS. Solving example networks determined the computer resource usage of the graphical analysis program (GAP). Algorithms for computing transients from network functions were tested and compared. Methods were explored for constructing network graphs by computer. In addition to these accomplishments, plans were made for future research.

Several activities are planned for Spring Quarter. During the Spring Quarter, the growth of processing time with network complexity will be measured. Development will begin on a preprocessor to automatically build network graphs. Remaining questions on including nonlinear components in the time domain calculations and on partitioning the network graph to reduce processing time will be considered. These plans will build on the accomplishments of the Winter Quarter.

During the Winter Quarter, several different examples were developed to demonstrate the use of GAP and to establish the speed, accuracy and memory requirements of the GAP program. The time for the MAS to reduce the graph and produce a frequency response plot was compared to the time to produce the same response using the SPICE program. The MAS was faster. A biquadratic active filter section was used for the comparison. In the MAS network elements

connected in parallel were represented as single edges of the graph and active elements were modeled by nullors. In SPICE, the active elements were modeled by controlled sources. Other examples which have been created include a ladder filter and a state variable filter. During the Spring Quarter, the examples will be used to create plots of computer resource usage as a function of circuit complexity.

Algorithms for performing numerical Laplace transform inversion were tested. One method of inversion computes the time domain solution in closed form. The algorithm which was tested could not compute partial fraction expansions of network functions that contained repeated complex roots. However, repeated roots could be accomodated by changing the polynomial root finding program and then modifying the residue calculation. A different method of inversion had no difficulties with network functions containing repeated roots. The latter method sums the residues at the poles of a Pade approximation to the exponential weighting in the Laplace transform integral.

Methods were explored to automatically construct a network graph. Although these methods were executed by hand, the procedure could be performed by a computer. To construct the graph a subgraph template was chosen for each element. Next, the template subgraphs were interconnected to form the network graph.

Important questions remain about the inclusion of nonlinear components in time domain response calculations. If nonlinear components are included in the network graph, and Laplace transform inversion is used, then the graph must be reduced again many times during time domain calculations. Closed form solution for the time domain response is not possible. On the other hand, if nonlinear elements are represented by their constitutitve equations, and a numerical integration is used, then large companion matrices are required to

represent the differential equations of the linear subnetworks. The best solution may be to incorporate nonlinear subnetworks in the graph. The network function is reevaluated whenever a "significant" change occurs to the terminal variables of a nonlinear subnetwork. Decomposing the network graph would speed up computation of the network function.

SRC EXPENDITURES

Winter Quarter 1987

	Dec. '86	Jan. '87	Feb. '87	TOTAL
Personal Services	$ 4,729.08	$4,143.36	$ 7,753.92	$16,626.36
Fringe Benefits	216.90	151.83	310.09	678.82
Materials & Supplies	182.40	885.08	1,470.09	2,537.57
Travel	-	156.00	-	156.00
Computer	-	-	-	-
Overhead	3,256.52	3,388.53	6,054.15	12,699.20
TOTALS	$ 8,384.90	$ 8,724.80	$15,588.25	$32,697.95

SRC REPORT/PUBLICATION SUBMISSION FORM

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Schlumberger Professor

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School of Electrical Engineering
Georgia Institute of Technology
Atlanta, GA 30332

REPORT TITLE

Quarterly Report, March 1, 1987, to May 31 , 1987, "Analog CAD Methodology"

REPORT AUTHOR(S)

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TYPE OF REPORT (check one)	PERIOD COVERED (if applicable)	REPORT DATE	NUMBER OF PAGES	DATE SUBMITTED TO SRC
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__ Annual Report				
__ Final Report	TO 05/31/87			
__ Thesis				

__ Publication Preprint
to be submitted to _____ date _____

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to be presented at _____ date _____

__ Other (please describe) _____

ABSTRACT OF CONTENTS OF THIS SUBMISSION (not to exceed one single spaced page)

This report covers the activities and progress of the SRC Project No. 84-07-051 during the spring of 1987. The conversion of the parameterized ADDAC cells to conform with MOSIS design rule specifications was accomplished. Work was continued on the development of the SMARTAMP automated op amp design program which uses an algorithmic approach. Updating the Programmer's Manual for the AIDE2 program was continued. Circuits designed by AIDE2 and fabricated were tested and agreed with simulated performance. Further development of the cell compiler for the AIDE2 program for the automated basic component design was made. Accomplishments were also made in both the theoretical investigation to accelerate reduction of graphs and the practical production of code to implement automatic graphical construction. Table look-up models for large signal and small signal were developed and implemented into both the HP 9836 C desktop computer and the SPICE 2G-6 circuit simulator.

SUBJECT KEYWORDS (circle keywords supplied on reverse - note any additions)
LIST A: Analog, CAD, CMOS LIST B: IC/CAD Tools, auto. layout, dev. modeling

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DATE RECEIVED _____ SRC PUBLICATION ID _____

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June 19, 1987

MEMORANDUM

TO: Ralph K. Cavin, III, Director of Design Sciences, SRC

FROM: Phillip E. Allen, School of EE, Georgia Tech

RE: Quarterly Report, Mar. 1. 1987 to May 31, 1987, SRC Project No. 84-07-051: "Analog CAD Methodology"

Introduction

This report covers the period from Mar. 1, 1987 to May 31, 1987, for the SRC sponsored research program at Georgia Institute of Technology titled, "Analog CAD Methodology". The objective of this program are listed as follows:

1. Development of performance oriented analog CAD tools.
2. Development of models, multilevel, and mixed-mode simulators for analog VLSI circuits.
3. The development of a means for circuit testability and fault diagnosis.
4. Development of high level analog design programs.

These objectives are the results of previous research in developing a base for undertaking research in analog CAD methodology. This research has the objective to reduce the design time of analog integrated circuits, increase the chance of successful design, and extend the design of analog integrated circuits to the systems designer.

Organization of This Quarterly Report

Each of the individuals working on this research program have written a one page summary of their efforts this quarter. These summaries follow this page. The research topic and students are listed as follows:

Automated Design of Analog Integrated Circuits	Juvena W. Loo
AIDE2 Research Activities	Seong K. Hong
Analog Integrated Circuit Design 2	Malsook Yu
ADDAC	Harry Li
Precision Analog Small Signal Model for Short-Channel MOSFET	Kwang Yoon
Multilevel Simulation of Analog Circuits	John Parish

A list of SRC expenditures is given on the last page.

AUTOMATED DESIGN OF ANALOG INTEGRATED CIRCUITS

Juvena W. Loo

June 10, 1987

I have continued working on the development of the SMARTAMP program which uses an algorithmic approach and will generate either an unbuffered two-stage or cascode op amp from a set of specifications such as DC gain, gainbandwidth, input CMR, output swing, slew rate, and load capacitance.

At the present time, efforts are being made on improving the interface between the program and the user, as well as, incorporating noise analysis into the program.

AIDE2 Research Activities

Seong K. Hong

Quarterly Report for Spring 1987

RESEARCH ACTIVITIES

The primary activity during this quarter has been developing the cell compiler for the AIDE2 program for the automated basic component design, by using the procedural component generation technique, which is called parameter preprocessing provided by AIDE2. Components are designed in a geometric format, which allows software controllable operators. The cell compiler aspect of the AIDE2 research is now addressing the problem of permitting entry cells, using new or different technologies, to be implemented into AIDE2 library. This can be implemented by allowing the AIDE2 program to take its technology description information from a technology file in an internal AIDE2 library or from a technology provided by the user-interactive routines so that files can be altered or replaced to represent different fabrication technologies at different installations.

During May, the integrated circuits designed by the AIDE2 program and fabricated by Harris Semiconductor were returned for testing and evaluation. Fig. 1 shows the layout of the fifth-order lowpass filter which was designed as a benchmark circuit. The frequency responses of this filter are shown in Fig. 2. The solid line with a triangle is the data from the experiment and the solid line with an x mark is the data from the simulation data. The response of this filter has a little discrepancy at the cutoff frequency. We are currently investigating the reason why this is happening. Also, we tested the third order elliptic lowpass filter with different shapes of layout in Fig. 3.

The frequency responses of these filters are shown in Fig. 4. The solid lines with a square, a triangle, and a circle are measured data and the solid line with an x mark is the simulated data. The responses of this filter also have discrepancies of about .5 DB deviation at the cutoff frequency.

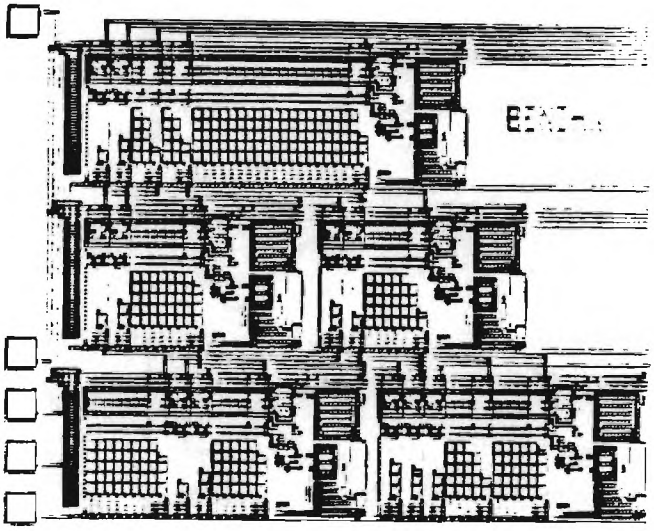


Fig. 1. Layout of 5th order benchmark filter

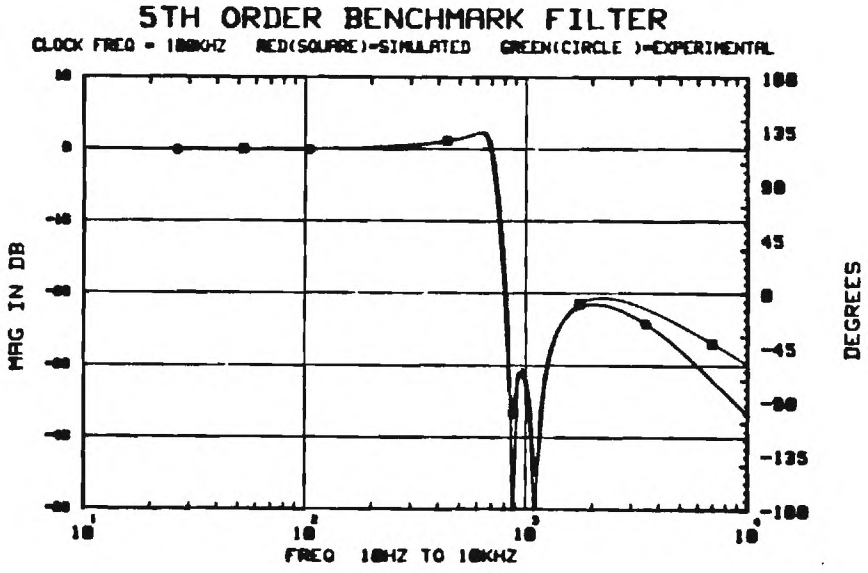
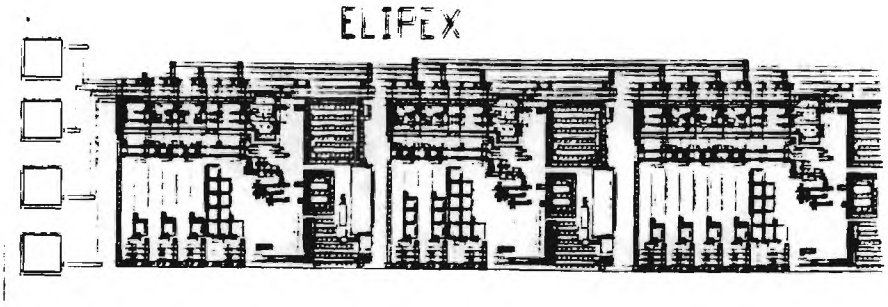
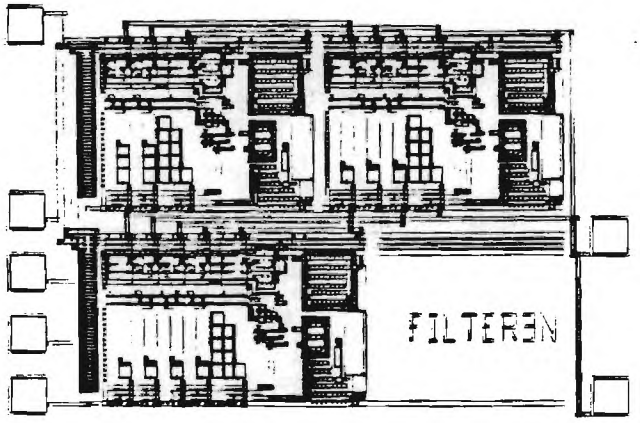


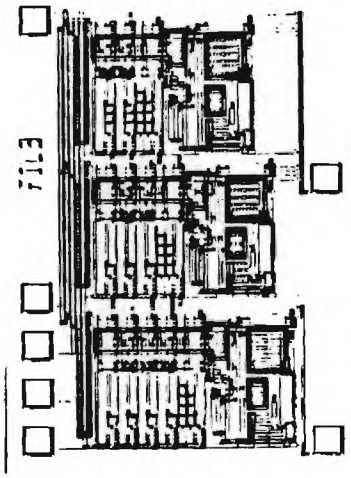
Fig. 2. Frequency response of 5th order benchmark filter



(a)aspect ratio 50



(b) aspect ratio 100



(c) aspect ratio 200

Fig. 3. Layout of third order filter with different aspect ratio

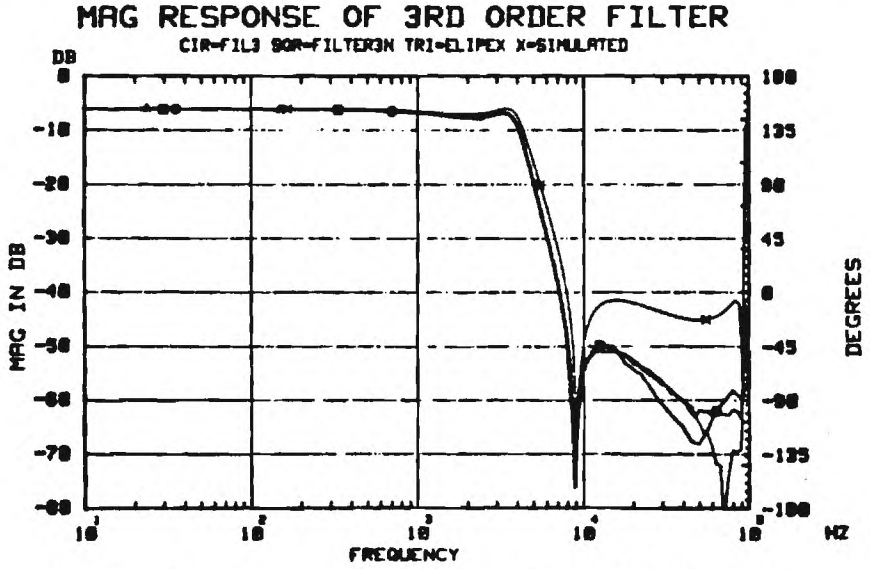


Fig. 4. Frequency responses of third order filter

ANALOG INTEGRATED CIRCUIT DESIGN 2

MALSOOK YU

SPRING, 1987

Acomplishments

My main goal was to get acquaintd with the AIDE2 program and to write the Programmers Manual for the AIDE2 program.
This was accomplisheded by :

1. Writing the AIDE2 Programmers Manual.
2. Laying the Capacitor Array out by using two metals to fabricate at MOSIS.
3. Laying the 5th Order chebyshev Low Pass Filter out by using AIDE2 layout capability in order to compare automated design vs custom design of analog IC's.

Plans

My main goal is to complete the Programmers Manual for the AIDE2 program and to compare automated design vs custom design of analog IC's and identify performance of limitations cause by CAD tools. Also make modifications of the AIDE2 program and make changes in AIDE2 which will allow better performance in the resulting circuits.

ADDAC

Harry Li

Spring 1987

Accomplishments:

The following work was accomplished during the Spring Quarter:

1.) Conversion of the parameterized ADDAC cells to conform with MOSIS design rule specifications.

2.) Remodification of the standard cells in order to eliminate the formation of parasitic transitors on the edges of the p wells.

3.) Preparation of a test cell for MOSIS fabrication.

4.) Preparation of an eight bit A/D for MOSIS fabrication.

5.) Simulation of the A/D using SPICE and SPLICE.

It was discovered that the possibility for "nonfatal" parasitic transistors existed in the layout of the ADDAC cells for the MOSIS process. The process does not allow poly1 to cross over the guard rings at any point. Therefore, all poly which crossed over the guard rings was first connected to metal before crossing. This required modification of all the fixed and paramterized cells. The parameterized cells were also converted from a Harris 5um process to a 3um MOSIS process.

A mixed mode simulator was needed in order to simulate the A/D. SPLICE was used and proved to be an effective tool in simulating the digital portion of the circuit (Successive Approximation Register). Time did not allow mixed mode simulation.

Plans:

Summer quarter--Summer Internship at General Electric Corporate Research and Development Center.

Fall quarter--Continuation of the simulation, evaluation of the fabricated circuits, investigation of possible methods of implementing a higher performance A/D converter into AIDE2.

STATUS REPORT FOR SPRING QUARTER, 1987

Title: Precision analog small signal model for short-channel MOSFET

Name: Kwang S. Yoon

Date: June 10 , 1987

Accomplishments

The objectives of this research were to develop models and model methodology which result in precise and computer efficient small signal models for short-channel MOSFETs including submicron devices. Table look-up models for large signal and small signal were developed and implemented into both HP 9836 C desktop computer and spice 2G.6 circuit simulator. Piecewise hermite cubic spline technique was employed to interpolate data points between data stored into table array for large signal model. The behavior of table look-up large signal model for NMOS 20um/1.2um is shown in Fig. 1(a). However, the same interpolation technique was not able to generate the smooth and monotonous small signal model parameters. Therefore it was necessary to modify the piecewise hermite cubic spline technique such that it could produce the smooth and monotonous small signal parameters with accuracy. Fig. 1(b) shows the output conductance curve as a function of V_{DS} and V_{GS}. The total number of data stored into table array and total number of experimetal data used were 156 and 441, respectively. The same table model was applied to GaAs MESFET 20um/10um device and the same accuracy was obtained, as shown Fig. 2(a) and 2(b).

Plans

The model accuracy against the statistical variation of experimental data will be evaluated and temperature modeling methodologies will be investigated. Table look-up model will be extended to develop capacitance models.

TABLE LOOK-UP MODEL FOR MOS 20μm/1.2μm

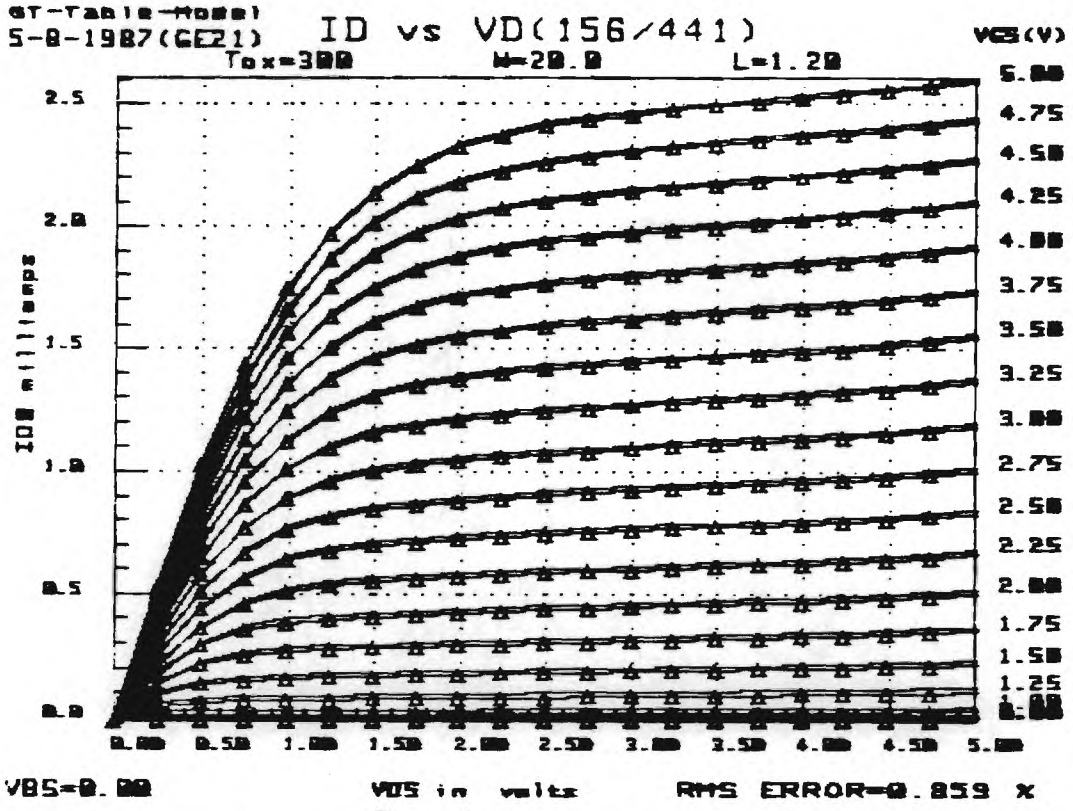


Fig. 1(a)

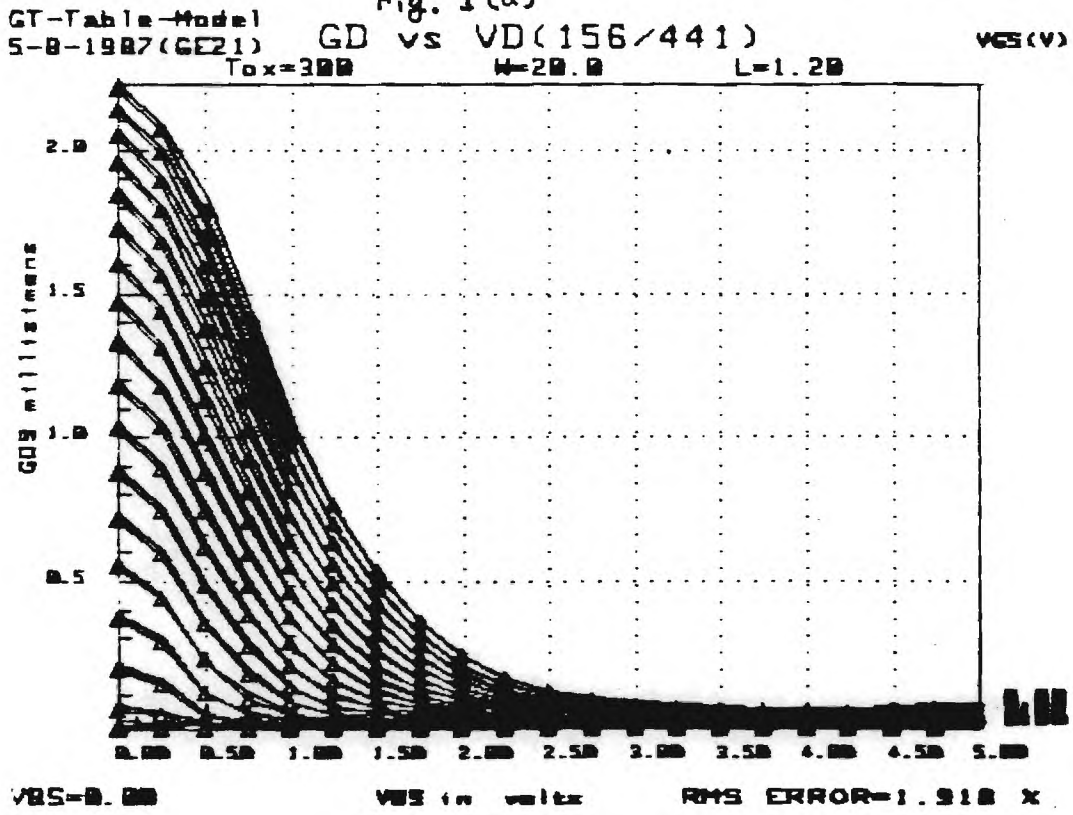


Fig. 1(b)

— Simulated data

-Δ- Experimental data

TABLE LOOK-UP MODEL FOR GaAs 20μm/10μm

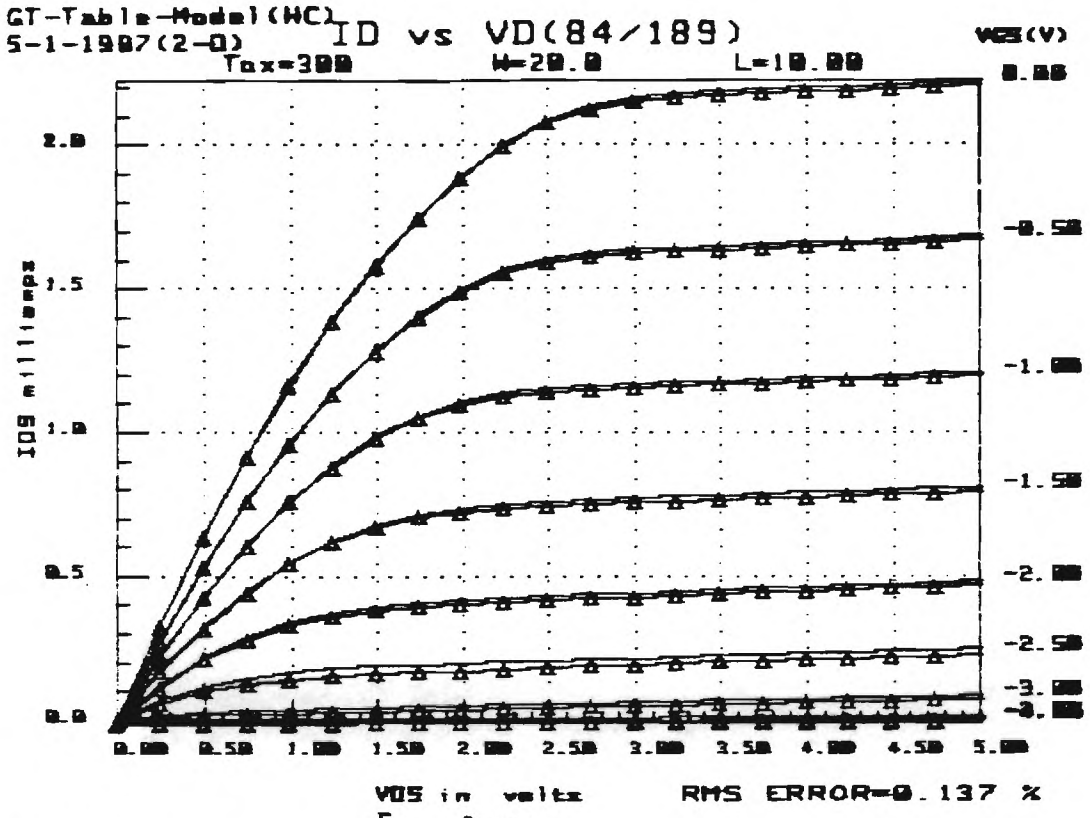


Fig. 2(a)

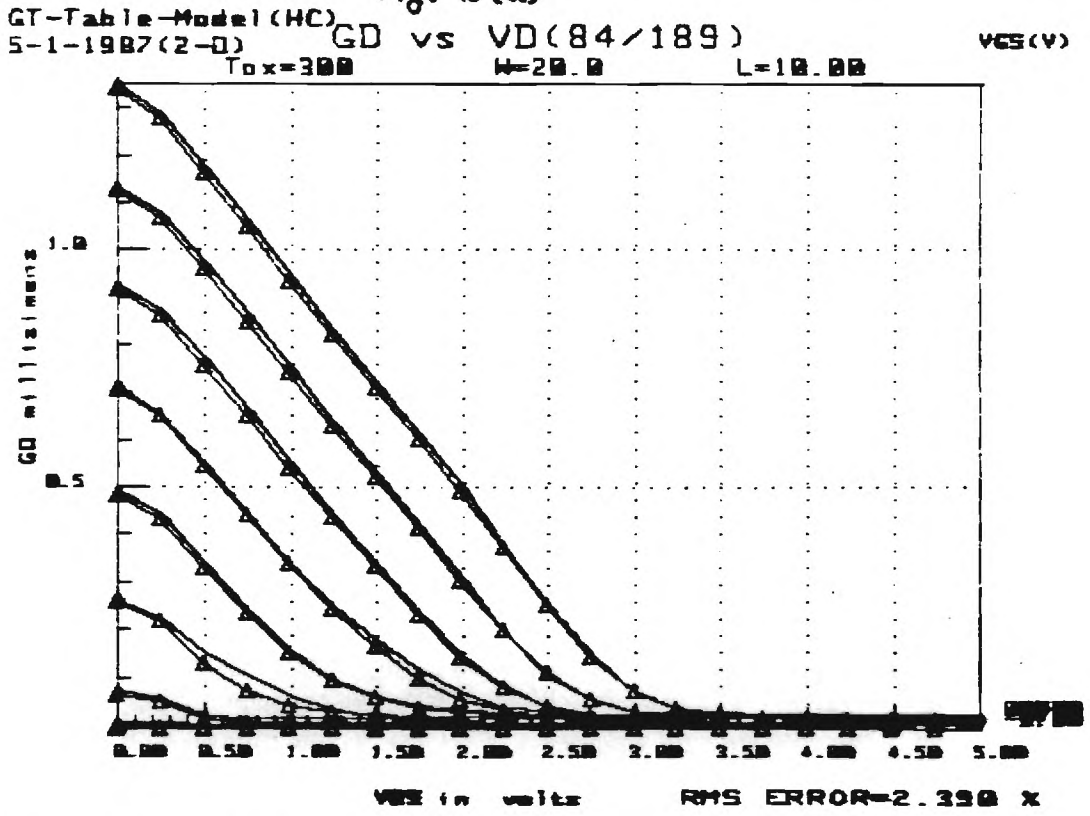


Fig. 2(b)

— Simulated data

+ Experimental data

Multilevel Simulation of Analog Circuits

John Parish

Quarterly Progress Report of Spring 1987

The spring quarter research goals included both theoretical investigation to accelerate reduction of graphs, and also practical production of code to implement automatic graphical construction. These efforts will make multilevel simulation more effective when the research goals of DC transfer curve, frequency response, and transient response are achieved. The next effort, to be pursued during the summer, is to produce the DC transfer curve. In addition to the two research thrusts already mentioned, benchmarks were found for an example circuit. This circuit was processed in the same form by the graphical analysis package (GAP) and by SPICE, and it was found that GAP was more than 30 times faster.

Since graphical analysis is the key to multilevel simulation, accelerating graphical analysis will improve the multilevel analog simulator. Two theoretical methods have been identified which can be used to accelerate graphical analysis. The first method is to decompose the graph without rearranging any graph branches. This method is projected to be effective at reducing the graph processing time, and is also expected to be easily applied to most types of MOS circuits. The second method is intended to be used following the application of the first method. The second method involves rearranging the branches of the graph in a manner which does not change the results of the analysis, but which simplfies the analysis. By rearranging the branches, disconnected substitute graphs are produced, so the second method implements a "divide and conquer" approach to graphical analysis.

An input processor is now operating which incorporates the graphical elements invisioned for the multilevel analog simulator into the syntax used for SPICE. The input processor allows the behavioural level models used in the MAS to be included in a SPICE deck. The graphical elements are recognized and collected by the input processor. The input processor then constructs a graph which contains the necessary data for a DC transfer curve analysis. This tears the circuit into two parts, a part which is processed by a GAP, and a part which is processed by SPICE-PAC. During the summer, augmenting sources will be added to complete the tearing of the network. Eventually, the theoretical means of accelerating the graphical analysis will also be incorporated into the simulator. At that point, benchmarks will be produced for the DC transfer curve calculation.

Another way of accelerating graphical analysis is to reduce the order of the complex rational functions for the graph transfer functions. A routine has been located which implements Muller's method for this purpose.

Other SRC sponsored activities were contacted in conjuction with research at Georgia Tech. The SPLICE mixed mode simulator was installed on the VAX 11/780 used by the SRC group, with the assistance of Dr. Saleh of the University of Illinois. The CINNAMON program will also be made available as a result of contact with Prof. Walker at CMU.

SRC EXPENDITURES

Spring Quarter 1987

	Mar. '87	April '87	May '87	TOTAL
Personal Services	$ 6,537.00	$ 6,507.00	$ 6,820.00	$19,863.00
Fringe Benefits	497.00	150.00	224.00	872.00
Materials & Supplies	253.00	299.00	244.00	796.00
Travel	1,061.00	-	611.00	1,672.00
Computer	-	-	-	-
Overhead	5,301.00	4,417.00	5,016.00	14,734.00
TOTALS	$13,649.00	$11,373.00	$12,915.00	$37,937.00

SRC REPORT/PUBLICATION SUBMISSION FORM

PLEASE COMPLETE THIS FORM FOR ALL REPORTS AND PUBLICATIONS SUBMITTED TO SRC

PRODUCED UNDER SRC CONTRACT? Yes/No/In Part SRC CONTRACT # 84-07-051
OTHER SOURCES OF SUPPORT? Schlumberger Chair Funds and GT E-Funds and GE Grant

NAME OF PERSON RESPONSIBLE
Phillip E. Allen
Schlumberger Professor

NAME AND ADDRESS OF ORGANIZATION
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, GA 30332

REPORT TITLE

Quarterly Report, June 1, 1987 to August 31, 1987, "Analog CAD Methodology"

REPORT AUTHOR(S)

Phillip E. Allen, Seong K. Hong, Alan Mantooth, John Parish, Kwang S. Yoon, and Malsook Yu

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x Quarterly Progress	FROM 06/01/87	12/15/87	10	12/15/87
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__Final Report	TO 08/31/87			
__Thesis				

__Publication Preprint
to be submitted to _____ date _____

__Presentation
to be presented at _____ date _____

__Other (please describe) _____

ABSTRACT OF CONTENTS OF THIS SUBMISSION (not to exceed one single spaced page)

This report covers the activities and progress of the SRC Project No. 84-07-051 during the summer of 1987. Primary results for the summer include measurement and comparison with simulation of several AIDE2-designed circuits, visiting 11 companies concerning their interests in mixed, analog-digital simulators, writing the report titled "Multilevel Simulation of Analog Circuits", implementation of the table look-up extraction routine into the HP 9836C, the implementation of the table look-up model into a version of SPICE 2G.6, design and submission of short channel analog test structures and circuits to the MOSIS 1.25 micron CMOS bulk process, continued development of the AIDE2 programmers manual, and the measurement of performance limits of AIDE2 designed circuits. One of the major accomplishments was to demonstrate that AIDE2 can be used to design circuits which have comparable performance with similar custom-designed analog integrated circuits fabricated in the same technology.

SUBJECT KEYWORDS (circle keywords supplied on reverse - note any additions)
List A: Analog, CAD, CMOS List B: IC/CAD Tools, automatic layout, dev. modeling

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December 15, 1987

MEMORANDUM

TO: Ralph K. Cavin, III, Director of Design Sciences, SRC

FROM: Phillip E. Allen, School of EE, Georgia Tech

RE: Quarterly Report, June 1, 1987 to August 31, 1987, SRC Project No. 84-07-051; "Analog CAD Methodology"

Introduction

This report covers the activities and progress of the SRC Project No. 84-07-051 titled "Analaog CAD Methodology" during the summer quarter of 1987 or from June 1, 1987 through August 31, 1987. The objectives of this program are listed as follows:

1. Development of performance oriented analog CAD tools.
2. Development of accurate models, multilevel and mixed-mode simulators for and VLSI circuits.
3. Development of a means for circuit testability and fault diagnosis of analog integrated circuits.
4. Development of high level analog design programs.

These objectives are the results of previous research in developing a base for undertaking research in analog CAD methodology. This research has the objective of reducing the design time for analog integrated circuits, increasing the chance of successful design and extending the design of analog integrated circuit to the systems designer.

Summary and Overview of Research Results

Normally 6 PhD students and 1 MS student are working on the SRC research described above. However, during the summer two of the PhD students were absent from campus because of summer employment or other reasons. The students present include Seong Hong, Alan Mantooth, John Parish, Kwang Yoon and Malsook Yu. Primary results for the summer include measurement and comparison with simulation of AIDE2 designed circuits, visiting 11 companies concerning their interests in mixed, analog-digital simulators, writing a report titled "Multilevel Simulation of Analog Circuits", implementation of the table look-up extraction routine into the HP 9836C, the implementation of the table look-up model into a version of SPICE 2G.6, design and submission of short channel analog circuits to MOSIS 1.25 micron CMOS bulk process, continued development of the AIDE2 programmers manual, and measurement of performance limits of AIDE2 circuits. The major accomplishment was to demonstrate that AIDE2 can design circuits which have comparable performance with similar custom designed analog integrated circuits fabricated in the same technology.

Report Organization

Each of the individuals working on this research program during the SUmmer 1987 quarter have written a brief summary of their efforts. These summaries follow this page. The research topic and student are listed as follows:

Cell Compiler and AIDE2 Research Activities	Seong Hong
Mixed, Analog-Digital Simulation	Alan Mantooth
Multilevel Simulation of Analog Circuits	John Parish
Precision Small Signal Model Development for Analog IC Design	Kwang Yoon
AIDE2	Malsook Yu

Budget Expenditures

The personnel supported by SRC during this quarter include Dr. Allen, Seong Hong, Alan Mantooth (SRC Fellow), John Parish, Kwang Yoon and Malsook Yu. The expenditures for this period are listed below:

Expenditure Category	June 1987	July 1987	August 1987	Totals
Personal Services	$6,811.44	$4,504.71	$4,441.56	$15,757.71
Fringe Benefits	$222.18	$1,044.58	$1,027.15	$2,293.91
Materials & Supplies	$643.23	$92.85	$57.10	$1,281.45
Travel	$638.00	$643.45	$0.00	$1,281.45
Computer	-	-	-	-
Overhead	$5,279.93	$3,771.35	$3,315.49	$12,366.77
TOTALS	$13,594.78	$10,056.94	$8,841.30	$32,493.02

CELL COMPILER AND AIDE2 RESEARCH ACTIVITIES

Seong K. Hong

Quarterly Report for Summer 1987

Research Activities

The primary activity during this quarter has been developing the several macromodels for the OPAMP in AIDE2 program. We finished making the models for the gain-bandwidth effect and power supply rejection ratio of the OPAMP and implementing these models into the AIDE2 program. The gain effect can be easily implemented by using the voltage controlled voltage source model. The finite bandwidth effect of the OPAMP can be implemented by adding the 1st order switched capacitor filter in Fig. 1 to the OPAMP model. The new OPAMP model can be automatically implemented into the AIDE2 program and the user can supply the specific information on the OPAMP gain-bandwidth. In other work, the sample and hold model for the switched capacitor circuit is complete and the noise model is in development.

With the development of the several macromodels, the OPAMP and switched capacitor filter which were designed by AIDE2 program and fabricated by Harris Semiconductor have been measured and compared with simulations. Fig. 2 shows the comparison of power supply rejection ratio between macromodel and measured data. Fig. 3 and Fig. 4 show the comparison between data from the Harris specification and data from the AIDE2 program.

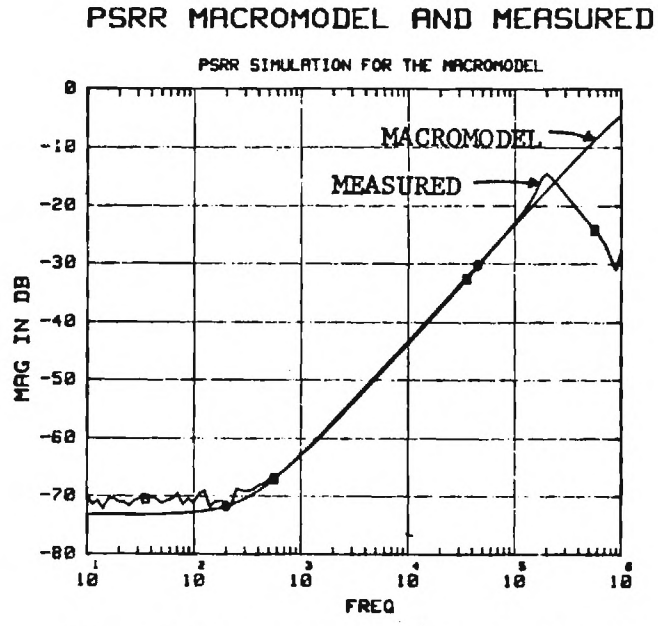


Fig. 1 PSRR characteristics of OPAMP

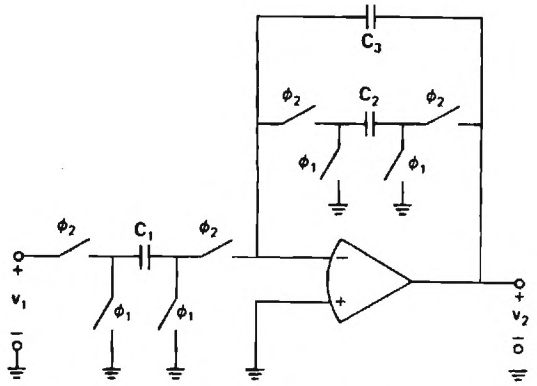


Fig. 2 SC first-order filter

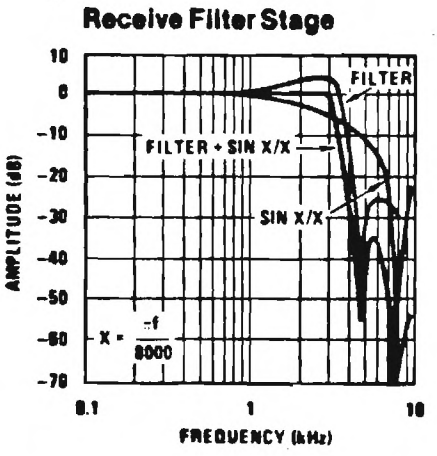


Fig. 3 Performance data from Harris for the Benchmark filter

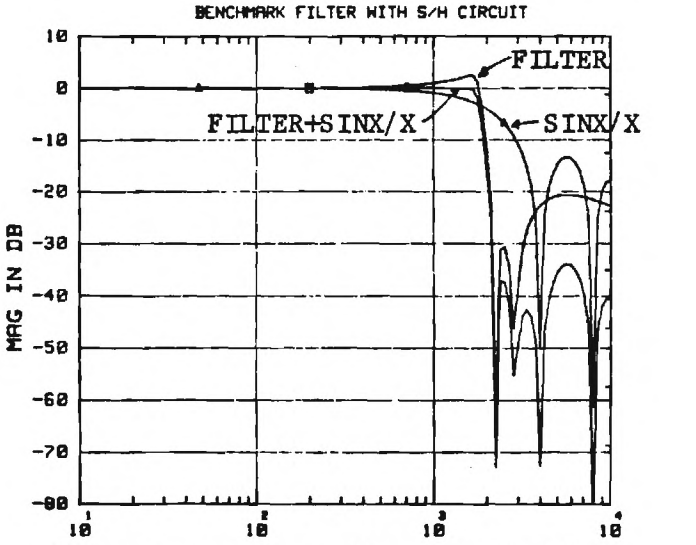


Fig. 4 Performance data from AIDE2 for the Benchmark filter

Mixed, Analog-Digital Simulation

H. Alan Mantooth

September 30, 1987

Accomplishments

The main objective of this research this summer was to investigate mixed, analog-digital simulation as a viable PhD topic. This topic has been reported to be of great interest to SRC member companies. First, an extensive literature review was initiated to become familiar with existing work on the subject. Next, nine SRC companies and two non-SRC companies were visited concerning this research. The impetus of these visits was to obtain the companies' perspectives on exactly needs to be done on this problem and to identify areas of research. Among the information received from these companies were wish lists, specific applications to which a mixed-mode simulator would be applied, and possible approaches to the problem. The outcome of these meetings was, in general, twofold. First, the meetings served to identify Georgia Tech, Dr. Phillip Allen, and myself with the mixed-mode simulation problem to industry. Secondly, valuable "real-world" insight was acquired to this problem. This insight may quite helpful in defining what exactly is to be done in our research. Lastly, a SSCTC workshop on mixed-mode simulation and an SRC conference on design verification were attended to learn of the most recent developments in this area.

Plans

The most significant problem encountered during this research has been the actual definition of what needs to be done. The main goal of the next quarter is to mentally and physically define the research problem. This will be accomplished by reviewing the information obtained in meetings with companies, at conferences, from the literature, and from further discussions with Dr. Allen and industrial contacts. The only significant forseeable problem is in identifying a **unique** approach.

Presentations

A formal presentation on analog/digital mixed-mode simulation was made to the following list of companies.

Rockwell International	Aug. 10	Newport Beach, CA
Hughes Aircraft	Aug. 11	El Segundo, CA
Silicon Systems	Aug. 12	Tustin, CA
Hewlett-Packard	Sept. 1	Santa Clara, CA
National Semiconductor	Sept. 2	Santa Clara, CA
GE Intersil	Sept. 3	Cupertino, CA
AT&T Bell Labs	Sept. 14	Murray Hill, NJ
General Electric	Sept. 17	Schenectady, NY
Analog Devices Semiconductor	Sept. 18	Wilmington, MA

Hayes Microcomputer Products in Atlanta and Texas Instruments in Dallas were also visited, but no presentation was given. This research was also discussed with Bill Needles from National Semiconductor while he was visiting Georgia Tech on August 27.

MULTILEVEL SIMULATION OF ANALOG CIRCUITS

John Parish

Quarterly Progress Report of Summer 1987

A research status report, entitled "Multilevel Analog Simulation: Status of Research at Georgia Tech", was also submitted to the SRC during the summer quarter. This report summarizes my work under this contract.

My current activities include a review of newly available software which performs functions closely related to my research work. During the Fall Quarter, this effort will be completed.

SRC Quarterly report on summer 1987

Precision small signal model development for analog IC design

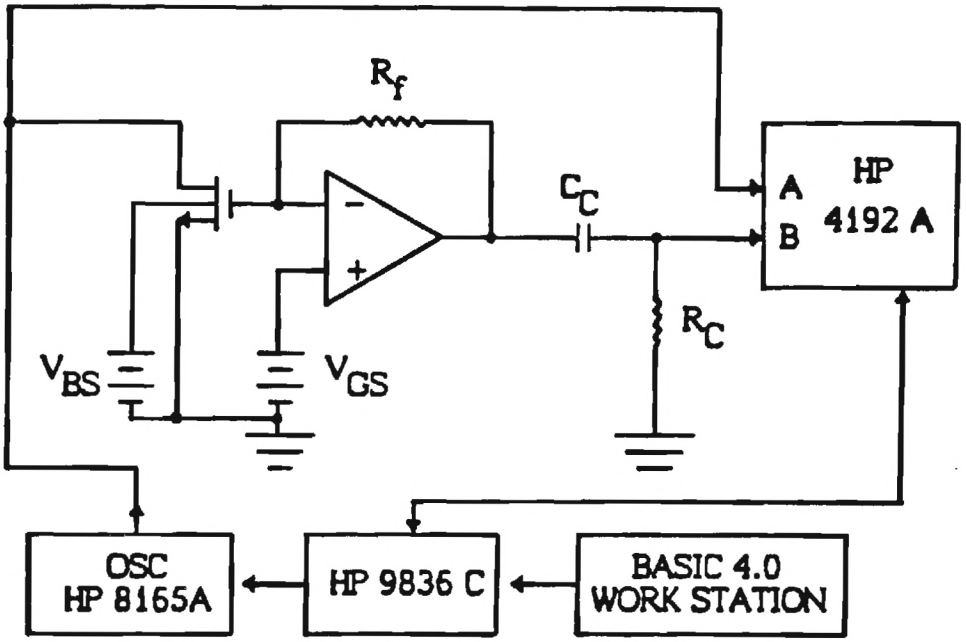
Kwang S. Yoon

October 2, 1987

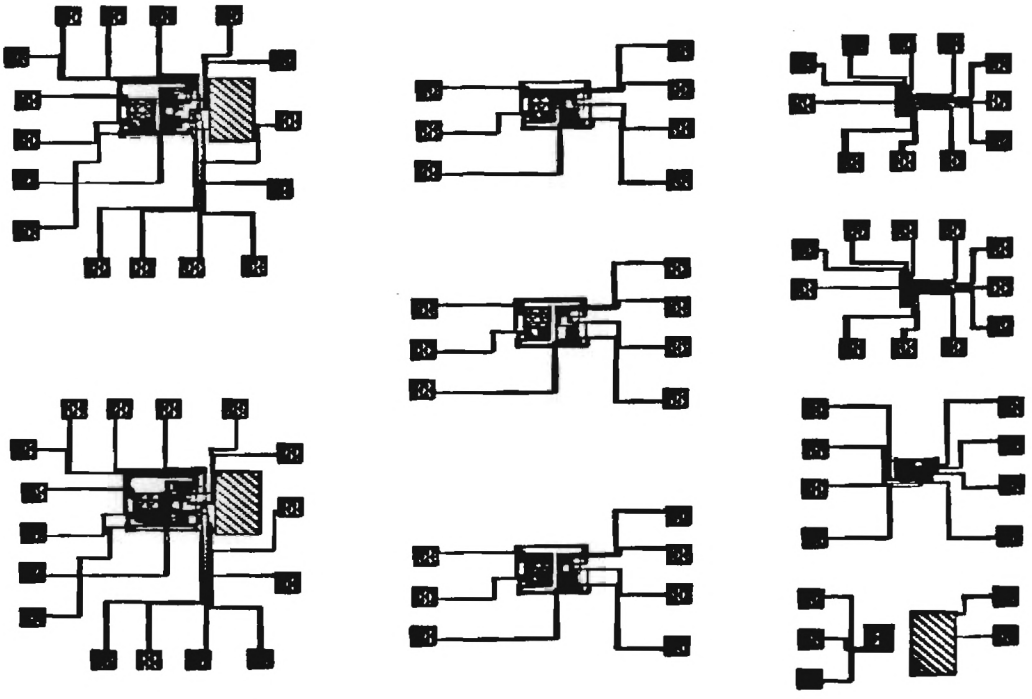
The objective of the research was to develop models and model methodology which result in the computer efficient, accurate analog small signal models for short-channel MOSFETs including the submicron devices. The large signal table look-up model and small signal contuctance have been developed and implemented into Hp 9836C and the SPICE cirucit simulator.

In order to model the intrinsic capacitances(C_{GS}, C_{GD}, and C_{GB}) of MOSFET devices, the measurement of short-channel MOSFET intrinisc capacitances requires the simplest setup to minimize the stray and parasitic capacitances and an automated measurement technique so as not to degrade the device characteristics because it has been well known that dc and ac stressing on MOS devices result in injecting many hot carriers into the gate region and limit the lifetime of MOS devices. Another reason necessary to have the automated measurement technique is that in order to model the intrinsic capacitances as a function of five variables(V_{DS}, V_{GS}, V_{BS}, W, and L), a large amount of data must be measured. An automated off-chip capacitance measurement scheme was developed to measure the experimental intrinsic capacitances, as shown in Fig. 1(a). Test and simulation of the capacitance measurement scheme was proceeded and the optimal operating frequecy to measure the intrinsic capacitances was found to be 10 KHz.

The analog circuits and test arrays designed and implemented in a CMOS bulk 1.25 micron n-well single poly and double metal process were fabricated and returned in the middle of August, 1987. The overall circuit layout is shown in Fig. 1(b). Those analog circuits and devices will be characterized and utilized to evaluate and further improve the table look-up model.



(a)



(b)

Fig.1. (a) An automated off-chip capacitance measurement scheme and
(b) the overall circuit layout for MOSIS 1.25 micron CMOS bulk process.

ANALOG INTEGRATED CIRCUIT DESIGN 2

MALSOOK YU

SUMMER, 1987

Accomplishments

My main goal was to get acquainted with the AIDE2 program and to write the Programmers Manual for the AIDE2 program. Also identify performance of limitations cause by CAD tools.
These were accomplished by :

1. Writing the AIDE2 Programmers Manual.
2. Identify performance of limitations cause by CAD tools by comparing the frequency response between simulated data and experimented data of 3rd-Order Low Pass Filter in different layouts.

Plans

My main goal is to complete the Programmers Manual for the AIDE2 program and to write a SRC Report on "Influence of CAD Techniques on AIDE2 Designed Analog Circuits" Also make modifications of the AIDE2 program and make changes in AIDE2 which will allow better performance in the resulting circuits.

Presentations

Mr. Bill Needles (National Semiconductor)
Demonstrated AIDE2 and ADDAC on August 27, 1987.

GEORGIA INSTITUTE OF TECHNOLOGY
SCHOOL OF ELECTRICAL ENGINEERING
ATLANTA, GEORGIA 30332

ELEPHONE: (404) 894- 2983

February 10, 1987

Dr. Ralph K. Cavin, III
Director, Design Sciences
Semiconductor Research Corporation
P.O. Box 12053
Research Triangle Park, NC 27709

Dear Dr. Cavin:

Enclosed are the biographical sketches for Dr. Allen's Graduate Research Assistants currently participating in SRC research.

If there is any further information you need, please let me know.

I hope all is well with you and your family.

Sincerely yours,

Sherri Brenner
Assistant to Professor Phillip E. Allen

SB
Enclosures

HARRY W. LI

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ext. 7

OBJECTIVE: Summer Internship in the area of silicon compilers for analog integrated circuit design.

EDUCATION:

Georgia Institute of Technology — 1/86
Ph.D. candidate
Current GPA 3.2 Advisor: Dr. Phillip E. Allen.

Georgia Institute of Technology — 9/84-12/85
M.S.E.E. GPA 3.1
Emphasis in digital and analog electronics.

University of Tennessee — 9/78-6/84
B.S.E.E. GPA 3.19
Emphasis in Computer Engineering.

WORK HISTORY:

Georgia Institute of Technology, Atlanta, GA. — 3/85
Graduate Teaching Assistant
Taught Elementary Electronics course as well as instructed Industrial Electronics and Electrical Machinery Laboratories.

Christian Service Corps, Tucson, AZ. — 6/84-9/84
Volunteer Summer Missionary
Worked as a camp counselor for underprivileged children.

Warner Robins Air Logistics Center, RAFB, GA. — 1/81-9/83
Cooperative Education Student
Designed hardware and wrote software for Z8000 based controllers. Held security clearance.

REFERENCES: Available upon request.

CITIZENSHIP: U.S.

Terry J. Groom

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Arlington, Texas 76014

(817) 467-5657

Objective:

Continue education to include high speed monolithic IC's and microwave design techniques.

Education:

Georgia Institute of Technology — Projected Graduation
Persuing MSEE — AUG 1987

Texas A&M University — GPR 3.07/4.0
BSEE — MAY 1984

Work Experience:

Harris Semiconductor Linear IC Design — June 1984 - August 1986

PROJECTS: HA5101 - Low Noise High speed operational amplifier. Device worked on the first silicon and is nearing production release. Two patents are pending on circuits developed for this amplifier.

HA51X4 - Low noise dual and quad operational amplifier.

RESEARCH - Design of a wideband (50 Mhz), high speed operational amplifier using composite amplifier techniques. One patent application. Design of a high speed BiMOS analog switch .Unpublished internal papers on low noise design techniques , thermal modeling , wideband mirroring techniques , and mismatch analysis.

PROCESS DEVELOPMENT - Design representative for advanced BiMOS and High Speed bipolar processes for linear products.

Georgia Institute of Technology — August 1984 -

Graduate research assistant for Dr. Phillip Allen.

Design and evaluation of ADDAC , a silicon compiler for A/D and D/A converters.

References:

Available on request

JOHN TILLA PARISH III

Address
300 Home Park Ave., No. 1002
Atlanta, GA 30318

Telephone
(404) 874-4623

Education: MSEE Georgia Institute of Technology 1982
BSEE University of Colorado at Colorado Springs 1980

Mr. Parish is pursuing the Ph.D. degree in Electrical Engineering at the Georgia Institute of Technology. His research area is multilevel simulation of analog circuits. Mr. Parish has maintained a 3.4/4.0 GPA over graduate courses in electrical engineering applicable to the PH.D. In addition to the schools listed above, he also attended the United States Air Force Academy, from 1973-1977, where he majored in Engineering Science.

Experience:

Harris Corp., Semiconductor Sector : Engineer Temporary (1986)
Responsiblities: Integrated a hardware accelerator into the Harris CAD system.

Georgia Tech Research Institute: Research Engineer (1982-1985)
Responsibilities: Developed requirements, software plan, and effects simulation methodology for a closed loop radar simulator. Presented a two-day very high speed integrated circuits (VHSIC) familiarization session at Warner Robbins Air Force Base. Designed the EEPROM CPU adapter for a technology insertion project, whose subject was a military radar warning receiver.

Litton Data Systems Div., Litton Systems Inc.: Engineer (1980)
Resposibilities: Performed engineering test of various components of a military tactical air operations central (TAOC), including the central computer, display group, and radar processor.

Ampex Corp.: Electronics Tech. II (1978-1979)
Responsiblities: Tested broadcast video tape equipment.

Metric Systems Corp.: Field Engineer (1977)
Responsiblities: Tested voice communications equipment.

Publications:

"Multilevel Analog Simulator," IEEE Midwest Symposium on Circuits and Systems, Lincoln, Neb., 1986

"EWISTL Closed Loop Simulation Development Vol. I: System Design (U)," GT-TR-3806, Georgia Institute of Technology, Atlanta, GA, Dec. 1985

"EO/RF Combined Simulation Feasability (U)," AFWAL-TR-84-1043, Air Force Wright Avionics Laboratory, Wright-Patterson AFB, OH, Dec. 1983

"Very High Speed Integrated Circuits Familiarization Session," Contract FO9603-B2-G-3367, Georgia Inst. of Tech., Atlanta, GA, Nov. 1983

"EEPROM CPU Adapter Developmental Design Data and Technical Manual," Sub-Contract BED 21121, Georgia Inst. of Tech., Atlanta, GA, Mar. 1983

BIOGRAPHICAL SKETCH

SEONG K. HONG
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EDUCATION :

BSEE Hanyang University Seoul, South Korea 1980
(GPA : 3.8/4.5)

MSEE Hanyang University Seoul, South Korea 1982
(Special Area : Fault Dignosis in digital systems)
(GPA : 4.0/4.0)

MSEE Georgia Institute of Technology 1984
(GPA : 3.5/4.0)

Mr. Hong is now working toward a doctoral degree in the School of Electrical Eng. at Georgia Institute of Technology and developing the AIDE2 program which is a multilevel computer aided design software package intended to facilitate the design of analog integrated circuits. His research area is cell compiler and testability for the analog integrated circuits.

EXPERIENCE :

Hanyang University : Teaching Assistant (1980 - 1983)
(for digital system lab.)

Georgia Inst. of Tech. : Research Assistant (1984 -)
(for analog testability and
cell compiler)

PUBLICATION :

P.E. Allen and Seong K. Hong, "Physical Testability of Analog Integrated Circuits," Proc. of 29th MWCAS, Lincoln, NB, Aug. 1986.

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Objective:

Application of artifical intelligence techniques to analog integrated circuit design.

Education:

Georgia Institute of Technology
PhD. Candidate

Georgia Institute of Technology — GPA 3.0/4.0
MSEE — March 1986

Ohio State University — GPA 3.0/4.0
BSEE — June 1983

Advanced Course Work : Analog Integrated Circuit Design, Solid-State Microelectronics, Digital Signal Processing, and Communications.

Skills:

Engineer In Training

Programming Languages: Proficient in FORTRAN, Pascal, and C.

Operating System Environments: UNIX, Ultrix, and MS-DOS.

Work Experience:

Georgia Institute of Technology — 9/85-present
Graduate Research Assistant: Modified and maintained CAD tools on the VAX 11/780 and MicroVax Workstation, devloped within the AIDE2 software a standard cell subroutine utilizing the MOSIS fabrication process, implemented an interactive program to generate an unbufferred two-stage operational amplifier using an algorithmic approach. Responsible for computer facilities and the acquisition of new software.

Georgia Institute of Technology — 9/84-9/85
Graduate Teaching Assistant: Supervised electronics laboratories, Tutored, and Graded papers.

References:

Available upon request.

KWANG SUB YOON

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Home Telephone: (404) 873-3657 School Telephone: (404) 894-2967

Objective: Summer Internship in the area of the precision small-signal modeling for submicron MOSFET devices and analog integrated circuit designs

Education: BSEE Feburary 1981. GPA=3.3, INHA university, Korea
MSEE June 1983. GPA=3.7, Georgia Institute of Technology, Georgia
Ph.D. Candidate Thesis topic: Precision small-signal modeling for submicron MOSFET devices

Experience: 1984 - 1986, Research Assistant, Georgia Institute of Technology
1984 - 1985, Responsibilities: (1) Development of the Generic technology including generic design rules and generic process parameter sets for CMOS 3um to 5 um process (2) Development of the partial capacitor algorithm for AIDE2 program in C (3) Fabrication of MPC including the switched capacitor filters generated by AIDE2 program, and CMOS test circuits.
1985 - 1986, Responsibilities: (1) Evaluation of the existing analytical small-signal models for short-channel MOSFET devices (2) Development of precision small-signal model for the submicron MOSFET devices.

VISA status: Student visa(F-1) in U.S.A.

Citizenship: Korea

E-21-F10

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Multilevel Analog Simulation: Status of Research at Georgia Tech

REPORT AUTHOR(S)

Phillip E. Allen, John T. Parish III

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ABSTRACT OF CONTENTS OF THIS SUBMISSION (not to exceed one single spaced page)

Because of its importance as a computer aid for analog designers, multilevel analog simulation research has been undertaken at the Georgia Institute of Technology. While mixed-mode simulators for digital simulation have already been developed, the development of the corresponding multilevel analog capability is only now being explored. The requirements and goals for the research program at Georgia Tech are stated, and a discussion follows of the current progress in the research. Finally, plans for future work are outlined, and the intention is stated that this research will serve ultimately to complement the design of a digital multilevel simulator. Thus, the multilevel analog research will provide a vehicle for combined analog and digital simulation.

SUBJECT KEYWORDS (circle keywords supplied on reverse - note any additions)
LIST A: Modeling simulation LIST B: Circuit simulation, graph theory, simulation

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Multilevel Analog Simulation: Status of Research at Georgia Tech

PHILLIP E. ALLEN AND JOHN T. PARISH III

Abstract — **Because of its importance as a computer aid for analog designers, multilevel analog simulation research has been undertaken at the Georgia Institute of Technology. While mixed-mode simulators for digital simulation have already been developed, the development of the corresponding multilevel analog capability is only now being explored. The requirements and goals for the research program at Georgia Tech are stated, and a discussion follows of the current progress in the research. Finally, plans for future work are outlined, and the intention is stated that this research will serve ultimately to complement the design of a digital multilevel simulator. Thus, the multilevel analog research will provide a vehicle for combined analog and digital simulation.**

I. Introduction

TWO PURPOSES exist for multilevel analog simulation research. The first purpose of a multilevel simulator is to provide a designer with feedback during the early stages of the design process. The second purpose of such a simulator is to serve as the analog oriented companion to a digital oriented mixed-mode simulator. The multilevel analog simulator enables the designer to begin creating simulation data before the design is finished. To provide this feedback, portions of the design are represented in terms of behavioural models. These behavioural models can take the form of network functions, state equations, or algebraic equations. The designer is then able to concentrate on the further definition of parts of his design, while continuing to obtain data about system performance. By having simulation data available at early stages of the design process, it is easier to produce specifications, and to study the interaction of different design architectures.

The second purpose of a multilevel analog simulator is to provide the analog-oriented companion to a digital-oriented mixed-mode simulator. Mixed-mode simulators, such as SPLICE [1] and SAMSON [2], provide the capability of obtaining simulation data from high level representations of digital circuitry. These simulators allow a circuit such as a logic gate to be represented by an algebraic equation, while another circuit, such as a boot strapped inverter, can be represented as a collection of electrical devices. By combining high level and low level models, like the gate and the inverter, accurate and suitably detailed data can be produced about large circuits. A similar capability is needed for analog circuits. By using high level models to represent analog circuits as well as digital circuits, a capability can be created for simulating large circuits that contain both digital and analog components.

This report provides the status of the multilevel analog simulation research program at Georgia Tech. The first section states requirements and goals for a proposed simulator. The second section describes the architecture of a multilevel analog simulator that meets the given objectives (Fig. 1). The third section describes the graphical analysis package that has been developed for use in the simulator. The fourth section describes response calculation algorithms useful for multilevel analog simulation. The fifth section outlines plans for a future analog and digital mixed mode simulator.

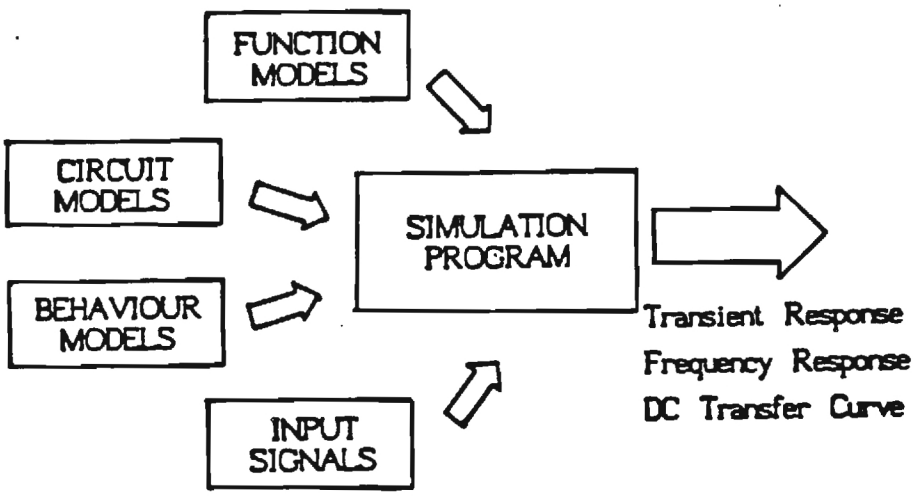

Fig. 1. Organization of a multilevel analog simulator.

II. Requirements and goals

The objective of multilevel analog simulation research is to simulate analog circuits using models from all levels of design (Fig. 2). In order to achieve this objective, requirements have been identified, and goals have been set. There are three requirements. First, a multilevel analog simulator must be able to produce time domain and frequency domain responses for linear and nonlinear circuits. For the frequency response, the inputs are assumed to contain DC bias, and small sinusoidal signals. For the time domain analysis, the signals are assumed to be either elementary time functions or piecewise linear time functions. Second, the simulator must be able to use models from different levels of design simultaneously. Finally, the simulator must provide a basis for research into mixed-mode simulation.

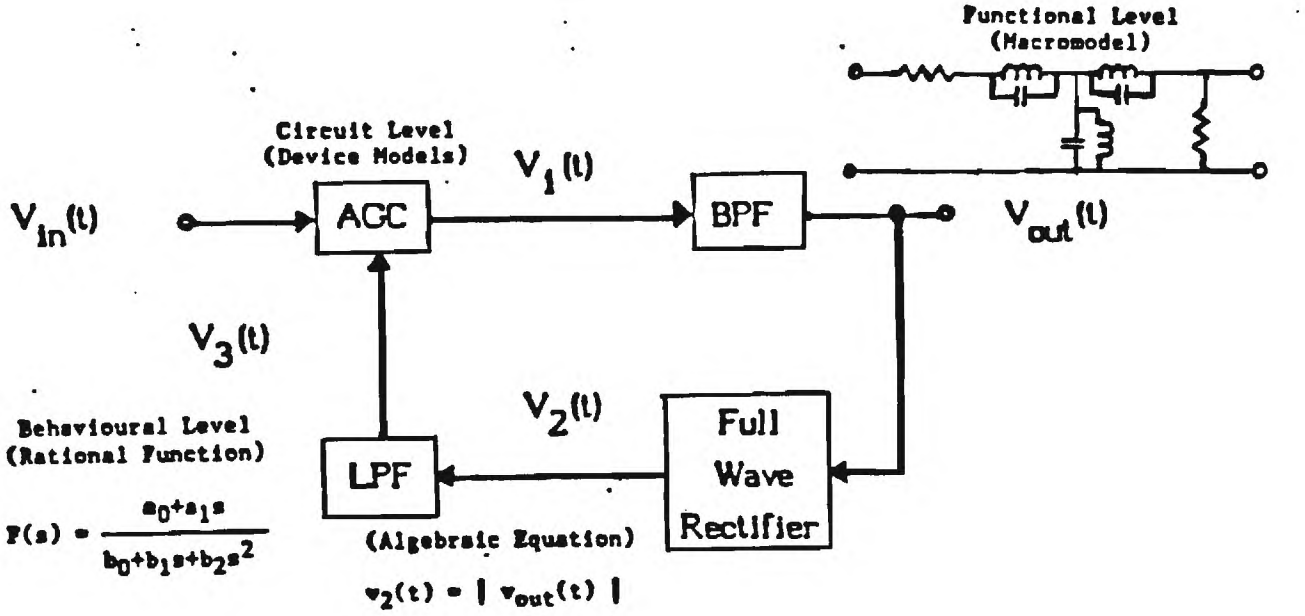

Fig. 2. Use of models from different levels simultaneously.

In order to satisfy these requirements, several goals have been set. The first goal identifies the time domain responses to be achieved. The simulator should produce a transient response to any input that can be expressed as a sequence of voltage or current values. This includes elementary time functions and piecewise linear time functions. Next, the simulator must produce DC transfer curves, by calculating a sequence of steady state solutions for constant inputs. Finally, in the frequency domain, the small signal frequency response should be computed from a network function of a linearized model of the analog circuits.

III. Multilevel analog simulator architecture

The multilevel analog simulator coordinates the flow of data between several different simulation tools (Fig. 3). The simulator runs on a VAX 11/780 that uses the UNIX 4.2 BSD operating system. Some of the simulator programs are written in the high level language C, and others are written in Fortran 77. The simulator control routines are files of command scripts, which activate the different tools in the simulator. The information processed by one tool is stored in a disk file for access by the next tool that the script calls. When the command requires an iteration involving several tools, the script starts an application program which can repeat accesses to each of the tools. In effect, the application program interfaces the different tools. Since each tool uses a different collection of model levels and model types, interfacing the tools means interfacing the data produced by the tools. The interface programs both control the tools and also interface the data that the tools produce.

The models used in multilevel simulation can be arranged in a hierarchy. Four levels of models are used in electrical simulation (Fig. 4). The top three levels are the most important for circuit designers. Modern analog simulators are building on the circuit level models used by the first simulators, and extending the range of models into the top two categories. At the lead in this research, simulators such as SABRE [3], and SUPER-SCEPTRE [4] are extending analog simulation to the behavioural level. Behavioural level models for analog simulation include nonlinear operators, such as rectifiers and comparators, as well as linear operators, such as filters. A multilevel analog simulator adds the behavioural level to the range of models included in analog simulation.

DESIGN ABSTRACTION	SIMULATION PRIMITIVE
Behavioural Model	Rational Function State Equation Algebraic Equation
Functional Model	Logic Equation Input / Output Table Macromodel Circuit
Circuit Model	Passive Device Semiconductor Device Ideal Source
Device Model	Physical Equations

Fig. 4. Heirarchy of primitives for multilevel analog simulation.

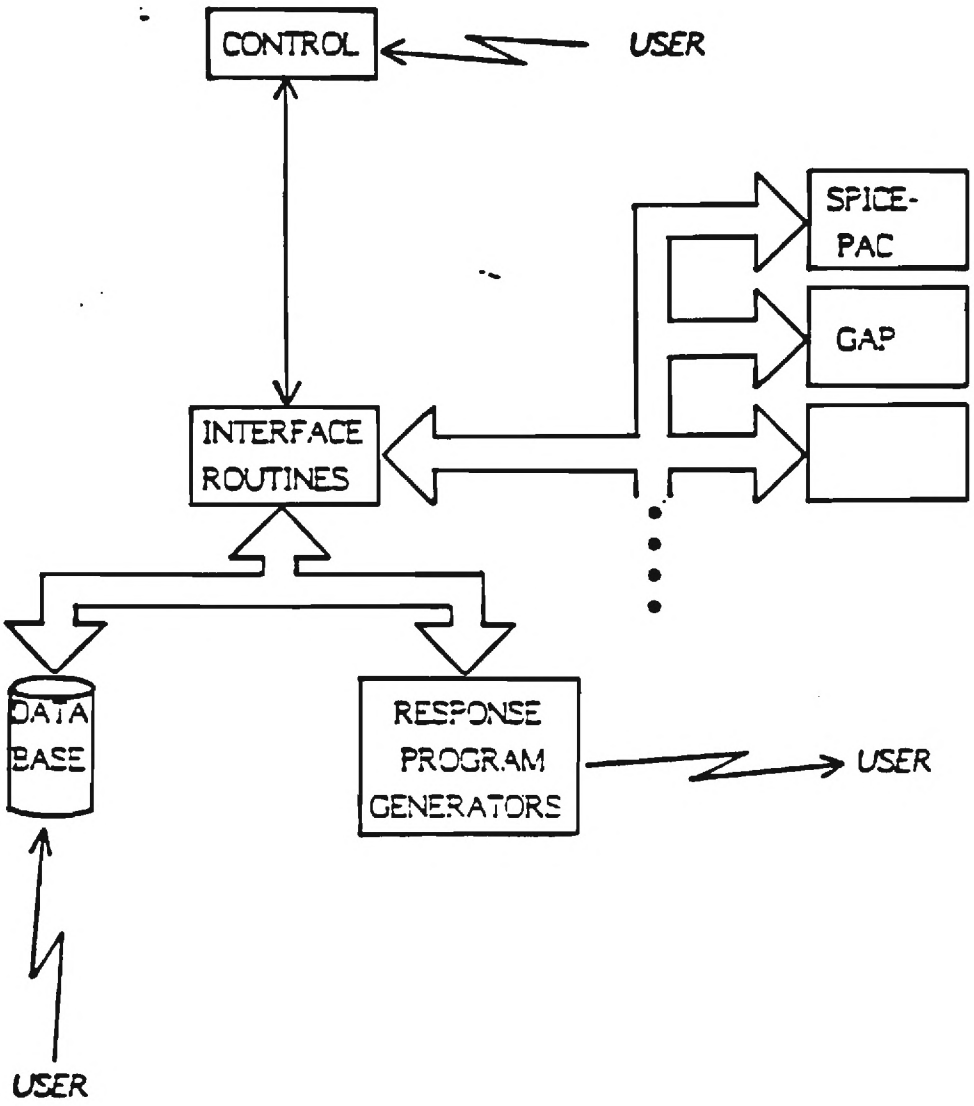

Fig. 3. Organization of a multilevel analog simulator.

A variety of model levels and types have been used in other simulators (Table I). Most early simulators were either analog oriented or digital oriented. Early simulators operated on either the circuit level or the functional level. Circuit simulators, such as SPICE [5] and ASTAP [6], used circuit level models, such as capacitors, MOS transistors, and idealized sources. Circuit simulators also allowed some types of functional models to be created. A SPICE user, for instance, can create his own functional level macromodels from the circuit level models supplied in the SPICE program. As an example, a designer may use a switched

capacitor filter to emulate an analog filter. So, the analog filter can serve as a macromodel that replaces the switched capacitor filter in a simulation. The macromodels have fewer components than the original circuit, and they approximate the function of the original circuitry. On the other hand, the first digital simulators used only functional models in their simulations. Such digital simulators as DL [7], FUSION [8], ADLIB [9], RSIM [10], MOSSIM [11], and TEGAS [12] still use functional models for the operation of digital logic. More recently, circuit level simulators have been optimized for digital circuits. These digital oriented simulators, such as MOTIS [13] and RELAX [14], use modified calculation algorithms to concentrate computational effort on the logic components whose inputs and outputs are rapidly changing. Ultimately, simulators were developed that included both functional level digital models and circuit level analog models. Mixed-mode simulators, such as SPLICE and SAMSON, incorporate both types of models. Moreover, the register transfer models included in later versions of SPLICE have added digital behavioural models to the SPLICE simulator. The device models, found at the lowest level, take too long to process for inclusion in a multilevel analog simulator. In fact, the detail incorporated into the device level models is too specialized for interest by most designers. A multilevel analog simulator provides models from the upper three levels in the model hierarchy. The goal of multilevel analog simulation is to extend the range of models to the behavioural level.

TABLE I. TABLE OF MODEL LEVELS USED IN VARIOUS SIMULATORS.

SIMULATOR	MODEL LEVELS					
	DIGITAL			ANALOG		
	CIRC	FUNC	BEH	CIRC	FUNC	BEH
SPICE				X	X	
ASTAP				X	X	
SABRE				X	X	X
SCEPTRE				X	X	X
SAMSON		X		X[1]		
SPLICE		X	X	X[1]		
RELAX				X[1]		
MOTIS	X					
DIANA	X			X	X	
DL			X			
FUSION		X				
ADLIB		X	X			
RSIM		X				
MOSSIM		X				
ESIM		X				
TEGAS		X				

1. These simulators are intended for digital MOS networks.

Each model used in a multilevel simulation has at least one equation. Some of the models, such as the model of a transistor, contain several equations. A multilevel analog simulator uses these equations to

define the circuit characteristics. Thus, the model equations are the primitives of the simulator. Examples of primitives include the circuit model of an inductor,

$$V_L(s) = Ls \; I_L(s) \quad , \tag{1}$$

and the behavioural model of a transresistance amplifier

$$V_{out}(s) = R_M \frac{s+1}{b_2 s^2 + b_1 s + 1} \; V_{in}(s) \quad . \tag{2}$$

An input file for a circuit must define not only the values used in each primitive, but also the topology that connects each primitive into the circuit.

Both linear and nonlinear primitives are included in a multilevel simulator. As part of the processing, the linear primitives are incorporated into a linear graph. The graph allows branch transmittances to be rational functions of the complex frequency variable, so that network functions can be included as branches of the linear graph. The graph can include all levels of linear primitives. On the other hand, nonlinear primitives must be linearized before they can be included in the graph. For the frequency domain response calculation, the nonlinear models are first linearized for the DC operating point of the circuit, and then included in the graph. It is not reasonable to linearize the nonlinear primitives, since time domain responses involve large signals. With large signals, the operating region of the nonlinear models may change. For time domain calculations, some of the nonlinear primitives can be evaluated using the models in the circuit simulator SPICE-PAC. Because it is a collection of tools, rather than a batch mode simulator, SPICE-PAC allows flexible use of the facilities built into SPICE. Each element of an input file contains an identification of the type of primitive, the parameter values for the primitive, and the topological information that connects that primitive to the circuit. The input files containing simulation primitives comprise the base of the simulator (Fig. 5).

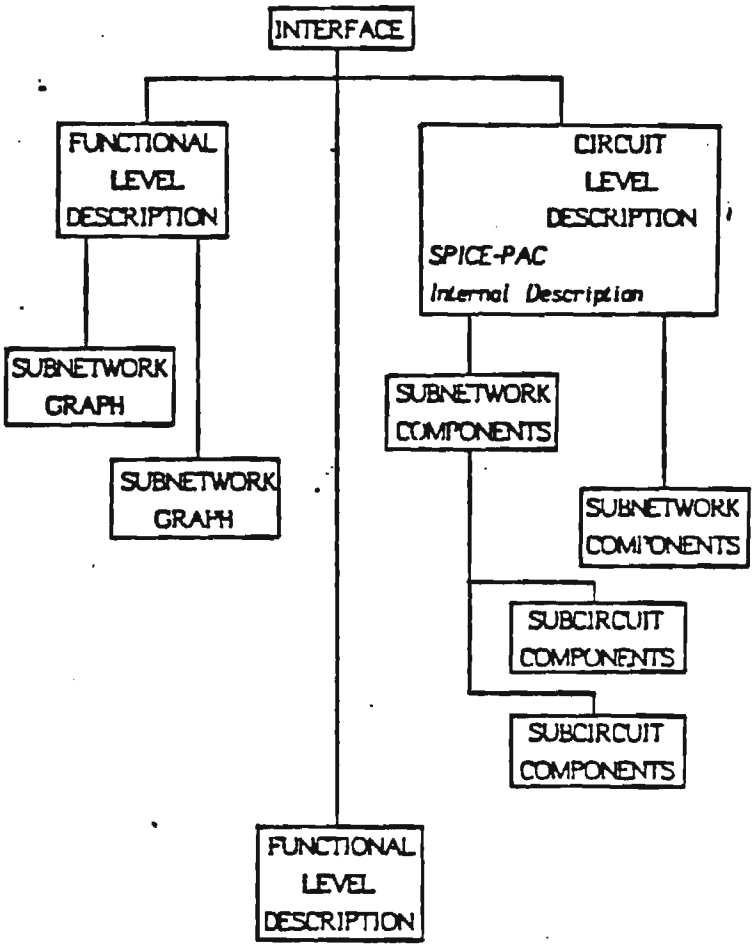

Fig. 8. Simulation data base.

IV. Graphical analysis package

The graphical analysis package uses signal flow graph principles to find transfer functions in a linear graph. These transfer functions can represent the various network functions of an electrical circuit. The example given below motivates the use of graphical analysis for multilevel analog simulation. For this example, the GAP program is ten times faster than the simulator SPICE. However, in larger examples, a problem has been observed with graphical analysis. The processing time grows rapidly with the number of elements in a graph. By decomposing the graph, the processing time can be accelerated. The research program is currently addressing this problem.

To obtain the network functions, all of the linear primitives in a given circuit can be incorporated in a linear graph. The linear primitives include fixed value resistors, and capacitors, at the circuit model level. Other linear primitives are found at higher levels. For instance, the linear primitives also include behavioural level models, such as filters, which are themselves represented in network functions. A given simulation uses not only linear primitives, but also nonlinear primitives. Before nonlinear primitives are included in a linear graph, the nonlinear primitives must be linearized. The linearized versions of the nonlinear primitives are in turn modeled as linear primitives, which are then incorporated into the graph. With the understanding that the graph is valid for small signals only, this process enables all types of analog functions to be included in a linear graph.

The following example displays the use of graphical analysis to simulate an active filter (Fig. 6). GAP provides the voltage transfer function for the filter, as a rational function of the complex frequency variable. The solution, which is the frequency response, is verified by manual calculation. For comparison, the example is also solved by the simulator SPICE.

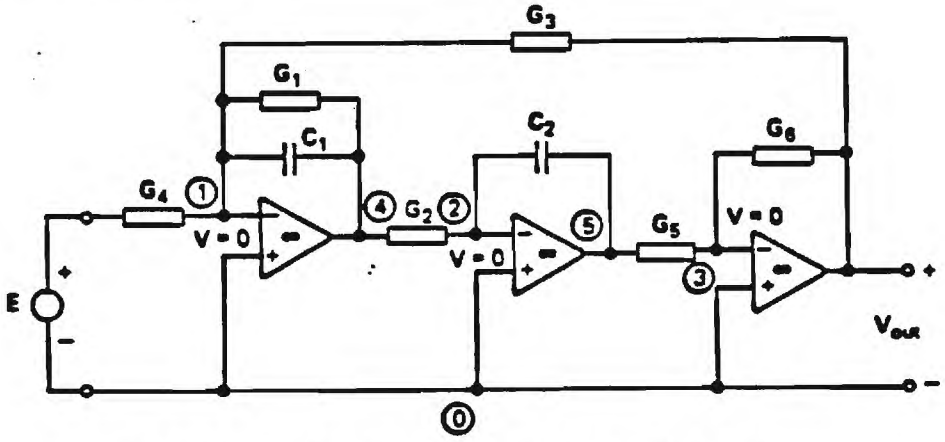

Fig. 6. Example active filter circuit for graphical analysis.

A linear graph actually implements Ohm's Law and Kirchoff's Laws for an electrical circuit. For instance, the modified nodal admittance equations for the circuit in the figure are given by

$$\begin{bmatrix} -G_1 - sC_1 & 0 & -G_3 \\ -G_2 & -sC_2 & 0 \\ 0 & -G_5 & -G_6 \end{bmatrix} \begin{bmatrix} V_4 \\ V_5 \\ V_{out} \end{bmatrix} = \begin{bmatrix} EG_4 \\ 0 \\ 0 \end{bmatrix} . \tag{3}$$

To create these equations, the OPAMPS were modeled as nullors [15]. The most convenient type of graph to construct from this set of equations is the Coates graph (Fig. 7). This graph contains a branch for each of the entries in the nodal admittance matrix.

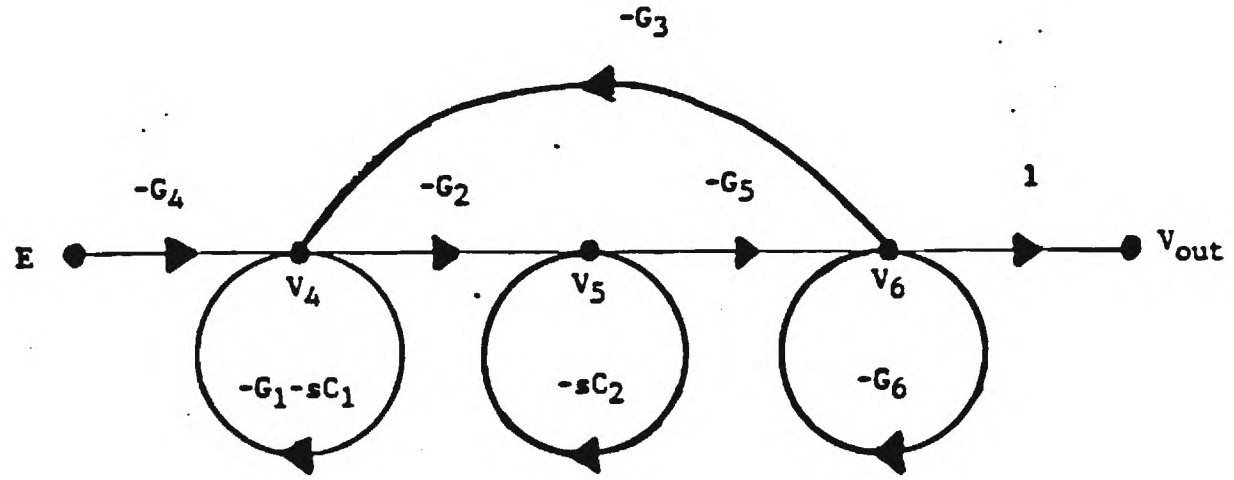

Fig. 7. Coates graph of active filter circuit.

However, it is easier to process a Mason signal flow graph, which has fewer loops than a Coates flow graph (Fig. 8). The self loops of the Coates graph may be removed by normalizing the inputs of each node with respect to the self loop transmittance. This operation is equivalent to dividing each equation by the term on the matrix diagonal. Then, by adding 1 to each self loop, the graph is converted from a Coates flow graph to a Mason signal flow graph [16].

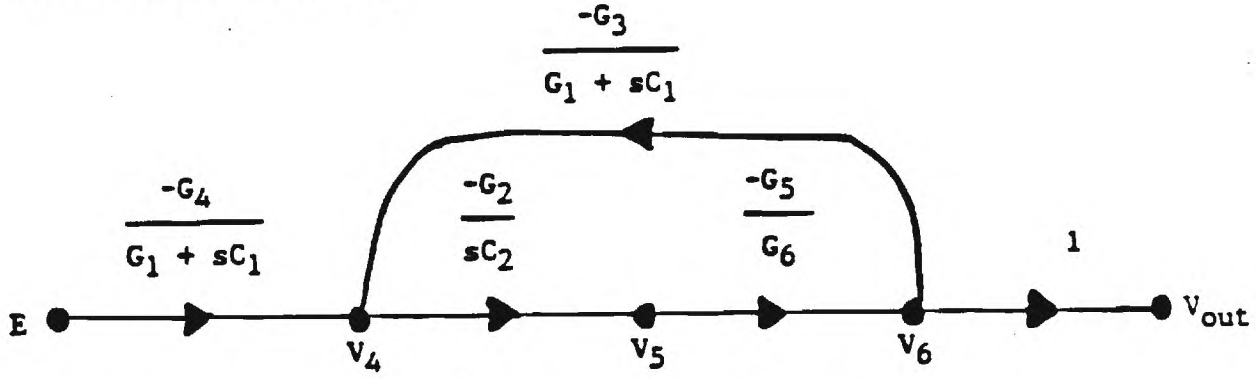

Fig. 8. Mason graph of active filter circuit.

The Mason signal flow graph is the input to the GAP program. GAP calculates the transfer functions of the graph, according to Mason's rule.

The GAP *input* file contains one line for each branch of the signal flow graph. The first two numbers on each line are the origin and target node, respectively, of the branch. The rest of the line supplies values for the rational function that gives the transmittance of the branch. The third number on the line is the number of coefficients in the numerator polynomial. The coefficients of the numerator follow, in ascending powers of the complex frequency variable s. The next number gives the number of coefficients in the denominator polynomial. The coefficients of the denominator are the last numbers on the line. For example, in Fig. 9, values are supplied for the resistors and capacitors used in the example filter circuit. The file is simply an ASCII file, named *input*, and it is created before running GAP.

```
1  4  0  -1.0e-4  1  1.0e-5  1.0e-6
4  5  0  -1.0e-4  1    0     1.0e-7
5  6  0  -1.0e-4  0  1.0e-4
6  7  0     1     0    1
6  4  0  -1.0e-5  1  1.0e-5  1.0e-6
```

Fig. 9. Graph of active filter as input to GAP.

The GAP *transfer* file identifies the transfer functions for GAP to calculate. In this example, only one transfer function is desired (Fig. 10). The voltage transfer function is requested by asking for the gain between node 1 and node 7.

```
1 7
```

Fig. 10. Network functions to be calculated by GAP.

The GAP *output* file contains the results of the transfer function calculations. A command from the UNIX shell starts the GAP program. GAP reads the *input* and *transfer* files, calculates the network functions, and stores the results in the disk file *output*. The *output* file for this example (Fig. 11) contains a single network function. The numerator and denominator of the function are listed in succession, and the function is identified by the numbers of the input and output vertices in the graph.

```
from node 1          to node 7
numerator      -1.000000e+01*s^0  + -1.000000e+00*s^1
denominator     1.000000e+00*s^0  +  1.010000e-01*s^1  +  2.000000e-04*s^2
              +  1.000000e-05*s^3
```

Fig. 11. Results of GAP calculations.

The plot of this function is the frequency response (Fig. 12).

The output of the GAP program can be verified using Cramer's rule. The equation is solved,

$$\frac{V_{out}}{EG_4} = \frac{\begin{vmatrix} -G_1 - sC_1 & 0 & 1 \\ -G_2 & -sC_2 & 0 \\ 0 & -G_5 & 0 \end{vmatrix}}{\begin{vmatrix} -G_1 - sC_1 & 0 & -G_3 \\ -G_2 & -sC_2 & 0 \\ 0 & -G_5 & -G_6 \end{vmatrix}} = \frac{-G_2G_5}{G_2G_3G_5 + sG_1G_6C_2 + s^2G_6C_1C_2} . \qquad (3)$$

When the values used in GAP are substituted for the variables in (3), the transfer function is identical to the output file of GAP.

For comparison, the same example was solved using the SPICE program. The OPAMPS were modeled as high gain voltage controlled voltage sources (Fig. 13).

FREQUENCY RESPONSE OF THE TRANSMITTANCE FROM 1 TO 7

```
        phase (deg)          -180.0      -90.0        0.0        90.0       180.0
      magnitude (dB)          -90.0      -55.0      -20.0        15.0        50.0
frequency   magnitude     phase
1.000e+00  2.003e+01 -3.614e-01 !----------!----------P----------!M----------!
1.585e+00  2.009e+01 -5.763e-01 !          !          P          !M          !
2.512e+00  2.022e+01 -9.273e-01 !          !          P          !M          !
3.981e+00  2.056e+01 -1.528e+00 !          !          P          ! M         !
6.310e+00  2.148e+01 -2.693e+00 !          !          P          ! M         !
1.000e+01  2.432e+01 -5.927e+00 !----------!----------P----------!--M-------!
1.585e+01  4.001e+01 -8.521e+01 !          !P         !          !     M     !
2.512e+01  1.648e+01 -1.740e+02 !P         !          !          M           !
3.981e+01  5.576e+00 -1.773e+02 P          !          !        M !           !
6.310e+01 -3.359e+00 -1.785e+02 P          !          !      M   !           !
1.000e+02 -1.171e+01 -1.791e+02 P----------!----------!-M--------!----------!
1.585e+02 -1.984e+01 -1.794e+02 P          !          M          !           !
2.512e+02 -2.789e+01 -1.796e+02 P          !        M !          !           !
3.981e+02 -3.591e+01 -1.798e+02 P          !    M     !          !           !
6.310e+02 -4.392e+01 -1.799e+02 P          !  M       !          !           !
1.000e+03 -5.193e+01 -1.799e+02 P----------!M---------!----------!----------!
1.585e+03 -5.993e+01 -1.799e+02 P         M!          !          !           !
2.512e+03 -6.793e+01 -1.800e+02 P      M   !          !          !           !
3.981e+03 -7.593e+01 -1.800e+02 P    M     !          !          !           !
6.310e+03 -8.393e+01 -1.800e+02 P M        !          !          !           !
1.000e+04 -9.193e+01 -1.800e+02 *----------!----------!----------!----------!
```

Fig. 12. Frequency response determined by GAP.

```
Active Filter
.TF V(6) VIN
VIN    7  0          AC 1V
R1     4  1           100K
R2     4  2            10K
R3     6  1           100K
R4     7  1            10K
R5     5  3            10K
R6     6  3            10K
C1     4  1           1.0UF
C2     5  2           0.1UF
E1     4  0  1  0    -100K
E2     5  0  2  0    -100K
E3     6  0  3  0    -100K
.AC DEC 5 1.0 10KHZ
.WIDTH OUT=80
.PLOT AC VDB(6) VP(6)
.END
```

Fig. 13. Components of active filter as input to SPICE.

The frequency response plot of SPICE is identical to the plot of the GAP transfer function. However, SPICE gives only the DC voltage gain. Thus, GAP provides more information than SPICE. The SPICE program required 5 seconds of CPU time. However, producing the network function and the plot, using GAP, required only .4 seconds of CPU time. For this example, GAP is more than ten times faster than SPICE.

One of the problems with graphical analysis is the rapid growth in processing time in proportion to the number of graph branches. GAP uses the theoretically optimum algorithm for locating the directed circuits of the graph. The details of this algorithm are discussed in [17]. GAP uses an efficient coding scheme to

identify the terms in the graph determinant. Similar methods are used to find first the forward path, and then the generalized cofactor, in the signal flow graph transfer function. The most time consuming operation is the location of the directed circuits of the graph. It can be shown that, for a graph containing N^2 branches, the number of operations OP necessary to explore the graph can be bounded

$$OP = e \cdot \left(1 + \int_1^N \Gamma(x+1)\,dx\right) \quad . \tag{5}$$

The processing time T to explore the graph is proportional to the number of operations OP as

$$T \approx \alpha \cdot OP \quad , \tag{6}$$

where α is a proportionality constant depending on the efficiency of the GAP program. When the proportionality factor is filled in, this equation provides an upper bound on the processing time. The significance of the equation, however, is the rate of growth, and not the absolute time. In fact, most graphs will not require this much processing. Moreover, decomposing the graph will reduce the amount of processing required.

It is easier to address the processing time problem in some technologies than in others. Some technologies generate circuits which are easily decomposed. The CMOS amplifier in Fig. 14a can be broken into three subcircuits, an input stage, an amplification stage, and an output stage. Separating the amplifier into stages is analogous to decomposing a graph of the amplifier.

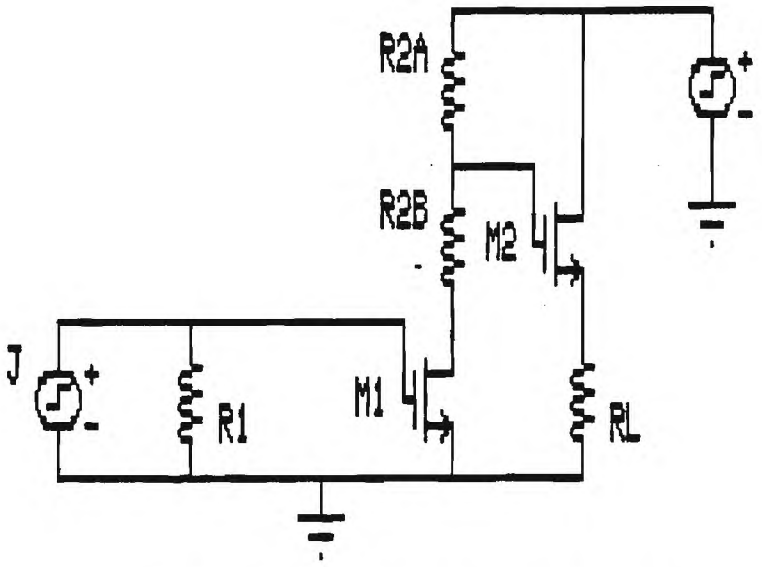

Fig. 14a. CMOS amplifier schematic diagram.

The graph can be decomposed by identifying cuts (the dotted lines in Fig. 14b) through which all branches are oriented in the same direction. No loop can be formed that includes nodes on both sides of such a cut. Therefore, the set of nodes that must be explored for directed circuits is reduced to two smaller sets. It takes less time to process the two smaller sets because the processing time growth curve is so steep.

Even when no natural breaks occur in the circuit graphs, the graph may still be decomposable. The graph in Fig. 15 can be decomposed into a substitute graph including only nodes 3 and 4, and another

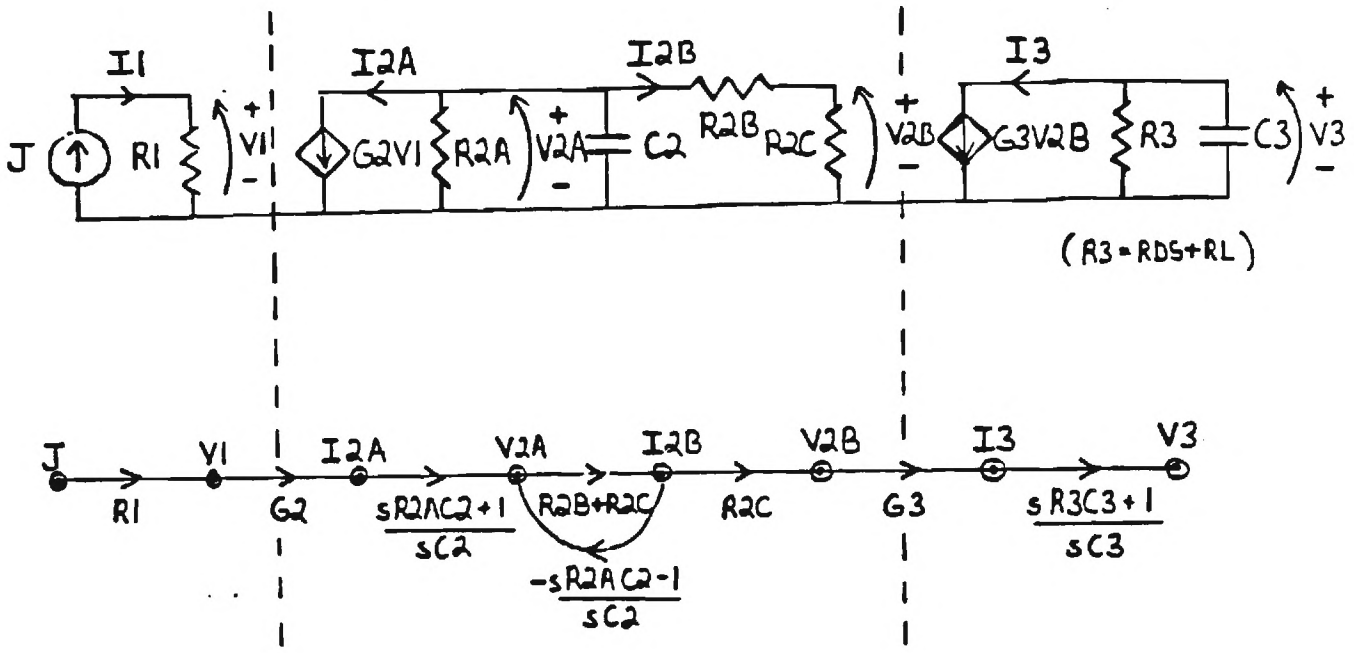

Fig. 14b. CMOS amplifier equivalent circuits decomposed.

substitute graph including the remaining nodes. The determinant of the original graph is the product of the determinants of the two substitute graphs. Because there are fewer loops in the two substitute graphs, and because the loops are shorter, the work involved in calculating the determinant of these graphs is reduced by 80%. This fact is verified in a previous report [18], which also proposes an algorithm for decomposing a graph with a digital computer.

A future step in the multilevel analog simulation research will be to develop an input processor that reads a file of linear primitives and decomposes the graph it produces. This processor will automate the process of creating the linear graph.

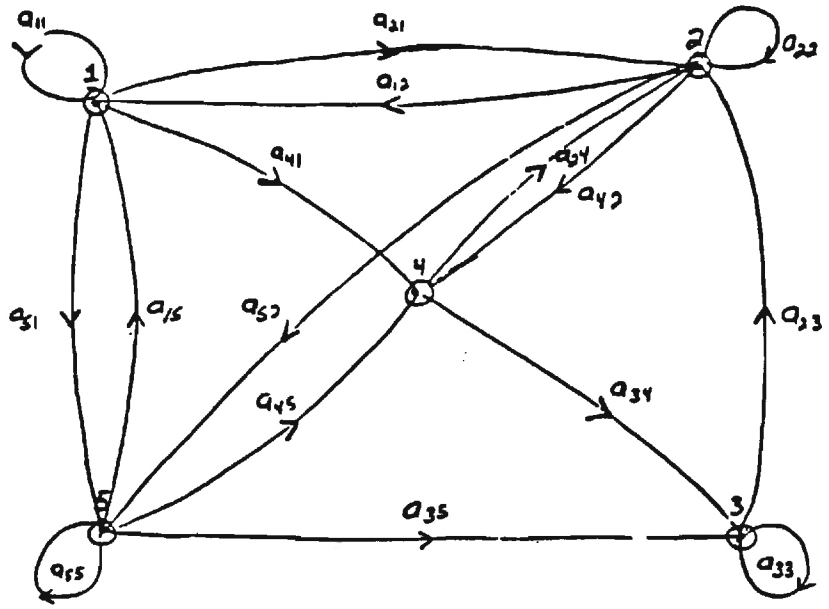

Fig. 15a. Graph to be decomposed.

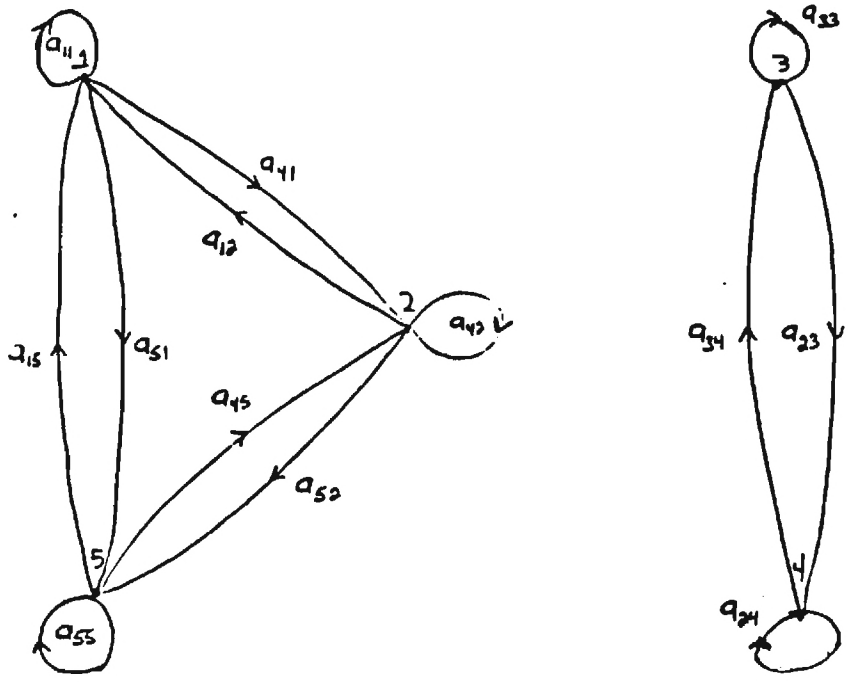

Fig. 15b. Two substitute graphs created during decomposition.

V. Response Calculations

As discussed previously, the goals of multilevel analog simulation research include producing three different types of responses. In the frequency domain, the goal is the small signal frequency response. In the time domain, the goals are the DC transfer curve, and the transient response. Once the input processor is finished, the next step in the multilevel analog simulation research will be the DC transfer curve algorithm.

The DC transfer curve algorithm uses both the GAP program and SPICE-PAC. To get the DC transfer curve, an application program will run GAP and SPICE-PAC in succession. By examining changes in the output files from iteration to iteration, the application routine tests for convergence of the iteration. The linear primitives in the input file are separated from the nonlinear primitives (Fig. 16). A linear graph can be created using the linear primitives. However, without the nonlinear primitives to complete the circuit, the linear graph is not necessarily connected. In that case, GAP can still find the transfer functions between nodes of any connected subgraphs. Transfer functions between nodes that are not connected are zero. Each connection between a nonlinear primitive and a linear primitive is broken when the linear graph is created. At each break, a grounded voltage source is attached to the terminal of the nonlinear part of the circuit, and a grounded current source is attached to the terminal of the linear part of the circuit. The external inputs of the circuit, which are chosen by the person using the simulator, are also attached to terminals of the circuit. To start the iteration, a value is assumed for each voltage source attached to the terminals of the nonlinear circuit, and the current in these voltage sources is calculated using SPICE-PAC. Next, the calculated current in each voltage source sets the value of the current source attached to the corresponding terminal of the linear circuit. The voltage across each current source is the sum of voltage due to each input of the linear circuit. The zeroeth order value of the transfer function from each other input terminal is used to calculate the voltage across each current source. The calculated voltage across the current source is then used to set the corresponding voltage source on the input to the nonlinear part of the circuit. This is one cycle of the iteration. The iteration converges to the steady state DC operating point of the circuit [19]. By examining the change in the SPICE-PAC output files at successive iterations, the DC transfer curve algorithm can detect convergence of the iteration.

After a DC operating point is found, the frequency response algorithm requires only a few additional steps. The first additional step is to create a graph that includes all of the primitives in the simulation. The nonlinear primitives must be linearized before they are included in a linear graph. Some of the nonlinear primitives, such as a piecewise linear rectifier, can be linearized as soon as the operating point is known. Other primitives require equivalent circuits to be created. For instance, the element values of a small signal equivalent circuit of a MOS transistor are available from the SPICE-PAC program. After calculating the operating point, and obtaining the values for the equivalent circuit elements, the input processor can be employed again. This time, the input processor connects to the graph the primitives for the linear components in the equivalent circuit. Finally, GAP is used to compute the desired transfer function of the graph. Plotting the transfer function completes the frequency response analysis.

Two different techniques are advanced for the transient response. Both techniques begin, as in the DC transfer curve algorithm, by making a linear graph from the linear primitives, and by calculating transfer functions between terminals of the graph. From that point, there are two different courses. The first algorithm includes the nonlinear primitives into the graph, but allows the parameters of the nonlinear primitives to change during the circuit calculation. In order to accomplish these changes, the primitives of the equivalent circuits of the nonlinear primitives are included into the linear graph. This is similar to the

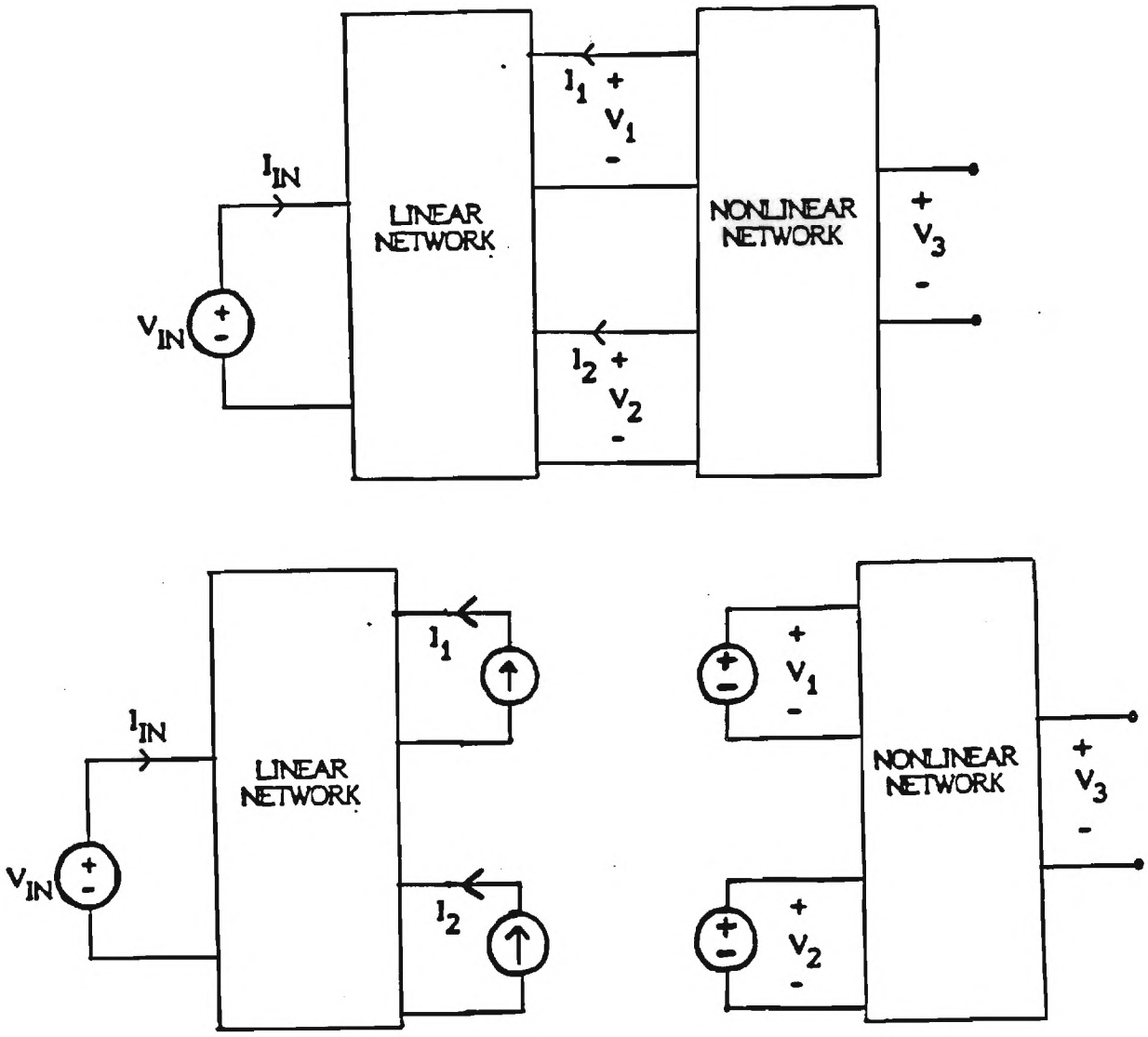

Fig. 16. Segregation into linear and nonlinear primitives.

frequency response algorithm. For the transient response, however, careful track is kept of those transfer function terms which are products of the nonlinear primitive parameters. When the circuit conditions change, new values of the parameters are obtained from SPICE-PAC. The new values are used to change the transfer function terms, and the calculation continues. This approach requires symbolic transfer functions. To implement this approach, additional data must be stored about the transfer functions calculated by GAP. As a result, this approach requires more data storage than the original GAP program. The transient response is calculated by numerical inverse Laplace transform of the network functions selected by the program user.

The second approach to the transient calculation is to describe the circuit by differential equations, and

then to numerically integrate the equations. Behavioural and functional level primitives which are linear can be reduced to transfer functions by GAP. The transfer functions known to GAP are then transformed to state equations. This transformation may be performed by calculating the Markov parameters for the transfer functions. The state equations are included in the differential equations that describe the operation of the circuit. The set of differential equations is then integrated to get the transient response.

VI. Mixed-mode simulaton

The multilevel analog simulation research is to serve as a foundation for a future mixed mode simulator. The mixed mode simulator SPLICE is currently being used to simulate circuits of an analog to digital converter which was designed at Georgia Tech. A simulator such as SPLICE, or SAMSON, can provide a framework in which an analog and digital multilevel simulation capability can be created. The high level models of SPLICE do not include some of the high level primitives discussed for the multilevel analog simulator. Moreover, SPLICE is designed for only transient response. The numerical integration and digital-analog interface techniques used in SPLICE can be used in a multilevel simulator for combined analog and digital simulation. Routines to get frequency response of the analog part of the circuit, and to include the high level analog primitives in the transient response, are required. Such response routines make possible analog-digital multilevel simulation. The methods of obtaining these responses are discussed in the previous section of this report. The multilevel analog simulation research will be compatible with future research into mixed mode simulation.

VII. Conclusion

This report has discussed the objectives, requirements, and goals of multilevel analog simulation research. Much has been accomplished at Georgia Tech toward achieving these goals. A graphical analysis package has been created for all levels of linear primitives. Although processing time problems are found with the graphical analysis approach, ways to overcome these problems were discussed. In addition, calculation algorithms to be used by the simulator have been given. An input processor is required before these algorithms can be tried. Finally, one of the goals of the research is to lay the foundation for a mixed mode simulator which will perform analog and digital multilevel simulation. Mixed mode simulators are currently being used at Georgia Tech, and it is anticipated that a mixed mode simulator which includes multilevel analog simulation will be produced. The mixed mode simulator research will follow on the results of the multilevel analog simulator.

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ANNUAL PROJECT REPORT

ANALOG COMPUTER AIDED DESIGN METHODOLOGY

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ABSTRACT OF CONTENTS OF THIS SUBMISSION (not to exceed one single spaced page)

This report describes the progress made during 1988-87 in analog CAD methodology research. This research includes performance oriented analog CAD tools, precision analog device models, analog compliers, multilevel and mixed analog-digital simulation, automated analog design, and analog testability.

CAD tools have been used to design several integrated circuits which have been carefully measured to determine performance limits due to CAD methods. The simulation capability of switched capacitor circuits was extended to include the op amp GB, PSRR, and noise. A high-level analog compiler for A/D converters was used to design a 4-bit and 8-bit A/D converter. Neither design was successful due to a combination of layout, design, and foundry errors.

A low-level compiler is being developed to allow quick entry of cells into the AIDE2 program and explore the performance limitations of device level CAD methods. A precise and efficient model has been developed using a table look-up approach. This model has been implemented into a version of SPICE2G.6 containing the BSIM model. An order of magnitude more accuracy with 50% less computational time has been observed for several MOS circuits modeled by the developed techniques compared with BSIM and SPICE models. Simulation research results include a performance evaluation of high and low level simulators for analog circuits and a report based on the visit of 9 companies.

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IN SITU PROCESS
IN-PROCESS
INSULATOR
INTEGRATED CAD/CAM/CAT
INTERCONNECTIONS
INTERFACE DESCRIPTION
INTERFACE STATES
INTERFACES
ION CLUSTER BEAM DEPOSITION
ION IMPLANTATION
ION MILLING
KNOWLEDGE-BASED
LASER ANNEALING
LASER ETCHING
LASER PHOTOCHEMISTRY
LATCHUP
LAYOUT TOOL
LAYOUT
LISP
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OXIDE ISOLATION
OXIDE
P-N JUNCTIONS
PARALLEL
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STANDARD CELLS
STATISTICAL ANALYSIS
STATISTICAL PROCESS CHARACTERIZATION
STOCHASTIC PROCESS MODELS
STRESS
SUPERLATTICE SUBMICRON
SURFACE STATES
SWITCH-LEVEL SIMULATION
SYMBOLIC SIMULATION
SYSTEM PARAMETERS
SYSTEMS
SYSTOLIC ARRAYS
TEM
TEST AND RELIABILITY
TEST CHIP/STRUCTURE
TESTABILITY
THERMAL NITRIDATION
THERMAL SIMULATION
THIN OXIDE LAYERS
TIMING SIMULATION
TOPOLOGICAL DESIGN
TRANSITION METAL SILICIDES
TRANSMISSION LINES
TRENCHES
TUNGSTEN
TUNNELING
ULSI
ULTRACOMPUTER
VLSI
VPE
WAFER DIAGNOSTICS
WORKSTATION
WSI
X-RAY
YIELD MODELING
YIELD

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ANALOG COMPUTER AIDED DESIGN METHODOLOGY

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COMPUTER AIDED DESIGN AND MODELING OF ANALOG INTEGRATED CIRCUITS

Abstract

This report describes the progress made during 1986-87 in analog CAD methodology research. This research includes performance oriented analog CAD tools, precision analog device models, analog compilers, multilevel and mixed analog-digital simulation, automated analog design, and analog testability.

CAD tools have been used to design several integrated circuits which have been carefully measured to determine performance limits due to CAD methods. The simulation capability of switched capacitor circuits was extended to include op amp GB, PSRR, and noise. A high-level analog compiler for A/D converters was used to design a 4-bit and 8-bit A/D converter. Neither design was successful due to a combination of layout, design, and foundry errors.

A low-level compiler is being developed to allow quick entry of cells into the AIDE2 program and explore the performance limitations of device level CAD methods. A precise and efficient model has been developed using a table look-up approach. This model has been implemented into a version of SPICE2G.6 containing the BSIM model. An order of magnitude more accuracy with 50% less computational time has been observed for several MOS circuits modeled by the developed techniques ,compared with BSIM and SPICE Level 2 models. Simulation research results include a performance evaluation of high and low level simulators for analog circuits and a report concerning the needs and present approaches of 9 semiconductor companies. Two computer programs have been developed to automatically design CMOS opamps.

This research in analog CAD has continued to develop methodology to shorten the design time and increase the probability of success for analog integrated circuits. This capability will permit the system designer to utilize existing and new VLSI technologies.

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1.0 INTRODUCTION

The general goals of the Design Sciences program of the Semiconductor Research Corporation (SRC) are focused on the design methods, test methods, and chip architectures that will support the chip performance, functionality, and producibility requirements of systems to be designed in 1994. The pertinent SRC goals to this research are to be able to "design systems that enable the design of chips with the specified complexity using less than 6 engineering man-months of effort beginning with logic (or high level) entry." [1].

The objective of this research in the area of computer aided design and modeling of analog integrated circuits is to develop methodologies for analog circuit design which can be implemented by the computer. This research supports the SRC goals by developing methodologies for analog integrated circuit and implementing them in a software platform that can be used together with digital CAD tools to design and layout signal processing systems containing both analog and digital circuitry.

This report describes the results of the fourth year (1986-87) of research in the area of analog CAD methodology and its application to analog integrated circuit design. The results of the previous three years have been described in earlier reports [2-4]. The research has now progressed to the point where several areas are beginning to mature. The CAD tools have been used to design successful integrated circuits which have been fabricated and measured. This information is providing input on the actual capabilities and limitations of analog CAD. The efforts to achieve a more accurate model for analog IC design has resulted in an order of magnitude more accuracy using less computational time than existing methods. Several of the other areas described in this report are showing promising results.

The work described in the 1986-87 Proposal lists the following areas of research activities: 1.) performance oriented analog CAD tools, 2.) precision analog small signal models, 3.) mixed analog-digital simulators, 4.) multilevel analog simulators, 5.) circuit testability, and 6.) automated analog circuit design programs. This report will address these areas by breaking them down further into the following eight areas: 1.) performance oriented CAD, 2.) analog silicon compilers, 3.) cell compilers, 4.) analog device modeling, 5.) multilevel analog simulation, mixed analog-digital simulation, 7.) testability of analog IC's, and 8.) automated design of analog circuits.

The large number of areas of activity within this SRC project demand careful coordination and organization to avoid fragmentation and insufficient use of resources. Fig. 1 illustrates the interrelationship between the various projects. Each of the boldface numbers indicate the major section headings 2.0 through 9.0 of this report. The overall objective of this research is the development of analog CAD methodology. It is seen that the previous research resulting in the AIDE2 program serves as a CAD platform for this work. Fig. 1 can be understood better by assuming that there are three distinct levels of design definition and implementation. These hierarchical levels from lowest to highest are circuits, functional, and behavioral. The circuits level is well-known to designers. The functional level uses nonlinear algebra and functional relationships to model circuit performance. The behavioral level is linear and uses time or frequency domain techniques to define circuit and system performance.

At the circuits level, the research activities include automated analog design programs to create circuits from a performance and technology description. These circuits are passed to the cell compiler which creates

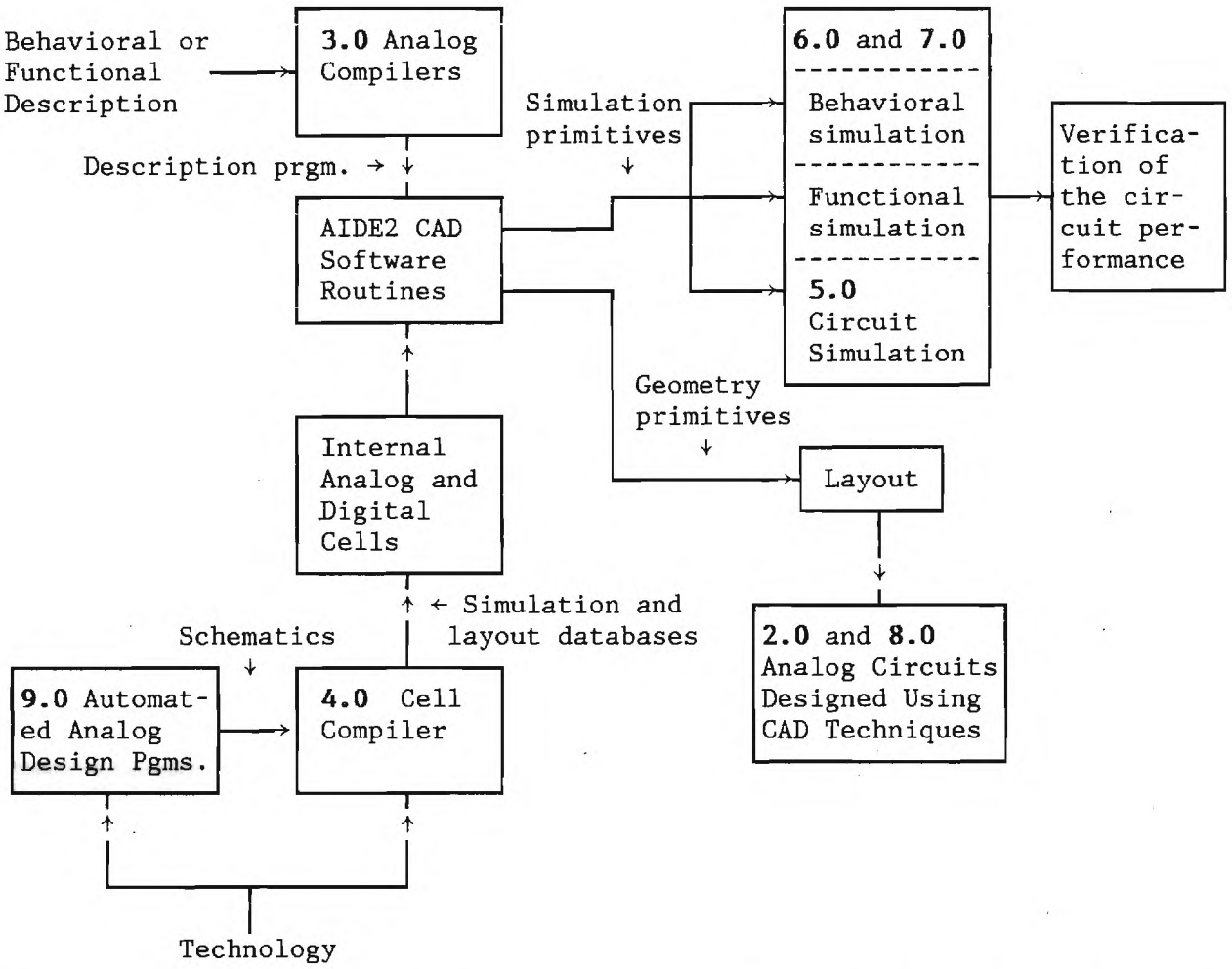


Fig. 1 - Overall perspective and organization of the analog CAD research described in this report. Boldface numbers refer to report section numbers.

simulation and layout databases for a cell in the AIDE2 internal library. At the functional or behavioral levels, analog compilers can be used to create the C-language description program which enables the AIDE2 program to provide a simulation and geometry implementation of the functional or behavorial description. One of the major problems in this research has been the lack of simulation tools to simulate at the level of design. The research described in the multilevel and mixed analog-digital simulation is a key aspect of fulfilling this need. Finally, in order to achieve sufficient prediction of the circuits simulated performance, it is necessary to improve the accuracy of the device models. This work has provided an indication that the model

accuracy can be reduced by a factor of 10 using less computational time than is used for present models. The actual integrated circuits produced by the above CAD methodology can be used to verify methods of improving and testing performance.

This report will describe the progress and results of each of the eight separate research activities indicated in Fig. 1 and the Table of Contents. The availability of successful analog IC's designed by analog CAD techniques has provided the ability to determine the performance capability of these circuits and to make an attempt to compare them with custom-designed circuits. The performance of a benchmark circuit and three filters with different layouts will be described. Methods of simulating the noise, PSRR, and GB of switched capacitor circuits using SPICE will be outlined.

The next two sections deal with the research in the area of compilers. A high level compiler called ADDAC has been used to create an 8-bit, successive approximation analog-digital converter. The performance and status of that circuit will be discussed. The low level compiler is only partially completed. It has the objective of providing a layout and simulation database suitable for cells in AIDE2. One of the benefits of the cell compiler will be to efficiently and quickly use different technologies.

A description of the results of the model research follows next. This work has selected the table look-up approach to implement a model which has the ability to accurately model both the DC and AC characteristics of the transistor. This model has been implemented in SPICE2G.6 containing the BSIM model. It has been applied to model both MOSFET's and GaAs MESFET's more accurately and quickly than existing models.

The next two sections discuss the status of the multilevel and mixed analog-digital simulation research. A behavioral-level program has been

implemented and interfaced with SPICE to illustrate the concept. Simulation of various circuits at both the high and low level are compared with respect to computational time and accuracy. The mixed analog-digital simulation research has begun by conducting an extensive survey of what is being done in industry, what are the needs, and how will such simulators be used?

The results of a built-in testability of analog circuits designed with AIDE2 will be discussed. This work has resulted in various integrated circuits with and without testing procedures to investigate the area and performance penalty.

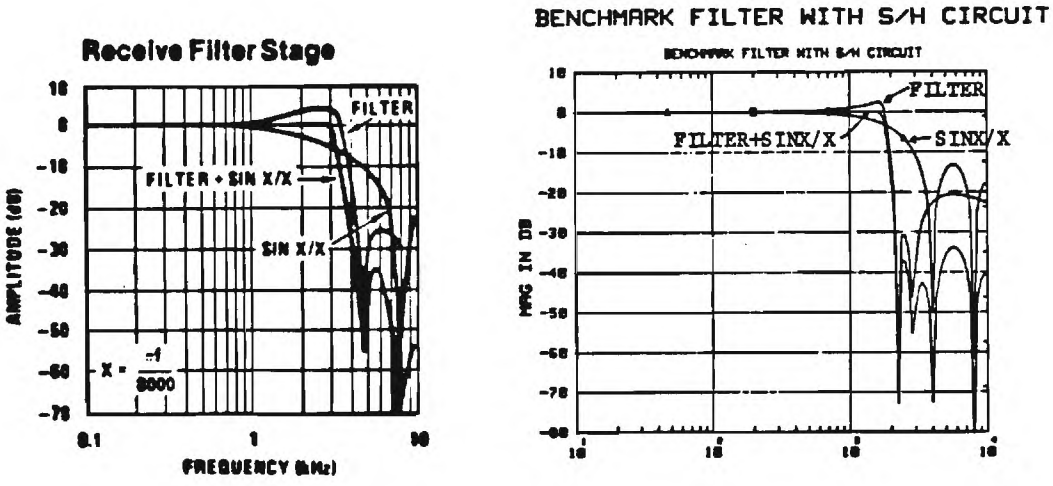
Finally, this report will address the progress made in the area of automated design of analog circuits. Two programs which can design a CMOS op amp are discussed along with the integrated circuits that were designed. A generalized approach to synthesizing analog circuits will be described. This approach is technology independent and has promise of being an excellent design tutor to new designers and a design confirmation tool for experienced designers.

2.0 PERFORMANCE ORIENTED CAD

The goal of this research effort is to identify those aspects of CAD techniques which limit the performance of CAD-designed integrated circuits. This information will be invaluable in helping to develop CAD techniques that provide optimum performance for analog and digital circuits designed using CAD methodology. This research has accomplished two results thus far. The first is the design of a benchmark analog circuit using CAD techniques which has been compared to the custom-designed circuit and the second is the beginning of measurements designed to identify limitations due to routing and placement. In order to compare the experimental measurements to a reference, the simulation modeling database of AIDE2 was extended to incorporate finite gain

bandwidth, noise, and PSRR effects of op amps in the discrete time simulation.

At the time the AIDE2 program was completed, a benchmark circuit was identified for the purpose of being able to compare circuits designed with AIDE2 to those which were custom-designed. The circuit selected for the benchmark was the receive filter of the Harris HC-5512/5512A PCM Monolithic Filter. This selection was made for two reasons. The first is that it used the same technology used to design the cells in the AIDE2. The second was that the receive filter was a 5th-order, switched-capacitor, low-pass filter which was not too complex and compatible with the cells in AIDE2. The only comparison made to date was the comparison of the frequency performance. Fig. 2 shows the comparison of the magnitude of the two filters. Although the two responses are not presented on the same curve (because sufficient accuracy on the HC-5512 is not available) the two have been carefully compared and are almost identical. After an HC-5512 part has been obtained, the frequency response, area, power, noise, PSRR will be compared in more detail.



(a.) (b.)

Fig. 2 - Frequency response of (a.) custom- and (b.) AIDE2 design filters.

A second accomplishment has been a study of three identical, third-order, low-pass filters designed by AIDE2 but layed out with different aspect ratios. Fig. 3 shows the layout of the three circuits. Fig. 3a is called ELIPEX and has been designed to have all three cells in one row. Fig. 3b is called FILTER3N and has a square layout consisting of two rows, one with two cells and the other with one cell. Fig. 3c is called FIL3 and has three rows, each containing one cell. While the routing has been done under the control of algorithms embedded in AIDE2, it is different for each circuit. In ELIPEX, the intercell routing is more complex while the power supply and ground routing is simpler. The opposite situation is found in FIL3.

At the present time, the frequency response of each of the circuits has been measured. No significant discrepancy was observed between each of the three types of frequency response until the clock frequency was increased from the designed 100KHz to 1MHz. In order to be able to characterized the

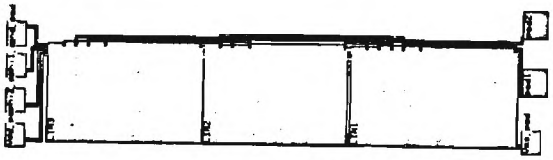


Fig. 3a ELIPEX

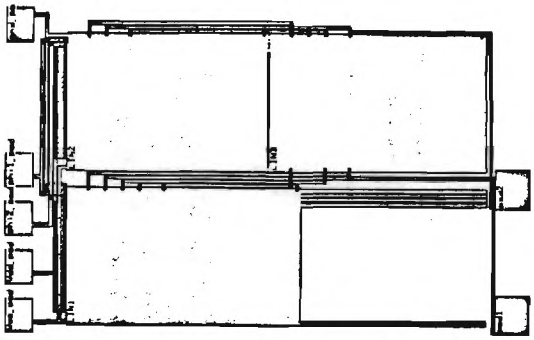


Fig. 3b FILTER3N

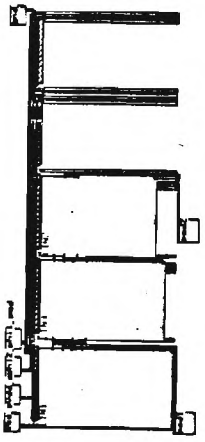


Fig. 3c FIL3

Fig. 3 - Layout of third-order filter with different aspect ratios.

frequency performance, various amplitudes, phases, and frequencies have been measured and tabulated in Table 1. The experimental data represents the average of measurements of at least three different chips. At the present,

Frequency Response Characteristic ↓	Simulated Data with finite Gain Bandwidth	Experimental Data		
		FILTER3N (R=100)	ELIPEX (R=50)	FIL3 (R=200)
Amplitude at 10 Hz (Hz)	-6.015	-7.071	-7.342	-7.187
Frequency of the peak (Hz)	35480	34145	31623	32434
Amplitude of the peak (dB)	-6.806	-3.966	-5.766	-5.121
Phase at the peak freq.	-115.5°	-138.0°	-124.8°	-133.7°
Frequency of notch (Hz)	100,000	95,075	85,770	117,262
Depth of the notch (dB)	-50.78	-55.42	-68.73	-65.21
Phase at the notch	-91.18°	10.59°	-146.36°	-119.49°

Table 1 - Average frequency response characteristics of three of each of the three different layouts (R=100 is square, R=50 is short and wide, and R=200 is tall and thin).

the nature of the routing between parts of the various cells and between the V_{DD}, V_{SS}, and ground pad to each op amp is being extracted. When this is complete, a correlation will be attempted between the performance illustrated in Table 1 and the extracted data. Future plans include the measurement of noise, PSRR, DC offset, voltage transfer function (linearity), and power dissipation. Again, these results will be considered from the viewpoint of the differences in routing and placement.

Except for the benchmark circuit, the only basis for comparing the response of the AIDE2 designed circuits was to compare with the simulation response. Unfortunately, the simulation did not incorporate any nonideal aspects of the op amp or the switched capacitor circuit. In order to improve,

the simulation capability, the noise, gain-bandwidth, and PSRR of the op amp was included within the simulator. This is significant from the standpoint that SPICE was the simulator. It is well known that SPICE can be used to model two-phase switched capacitor circuits [4,5]. Such techniques use transmission lines, resistors, independent sources and controlled sources. Clever techniques will permit the modeling of three op amp characteristics listed above uses these circuit elements.

The gain-bandwidth is modeled by replacing the controlled source representing the amplifier by a first-order low-pass circuit clocked at a frequency much higher than the clock for the switched capacitor circuit. The PSRR is modeled by an independent voltage source whose value is 1/PSRR, connected to the positive controlling node of the op amp model. Fig. 4 shows the model of the op amp modified to include the gain bandwidth and PSRR. Fig. 5 gives the comparison of the model with actual experimental data. The noise model is almost complete and will be implemented by using the voltage across a pn junction to control a voltage source in series with the positive

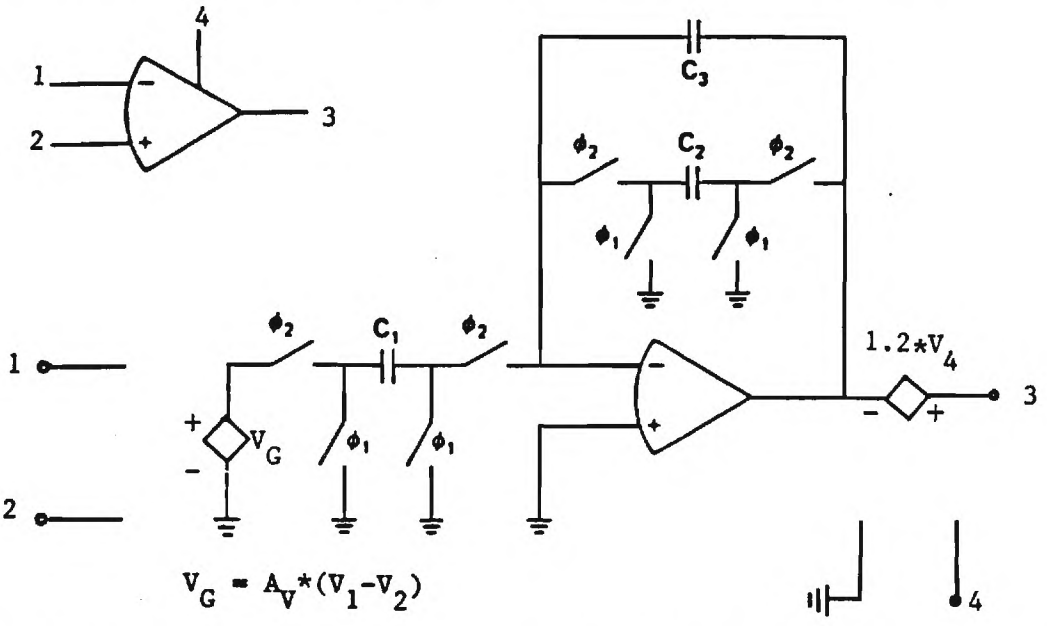


Fig. 4 - Discrete-time model of a practical op amp including PSRR and GB.

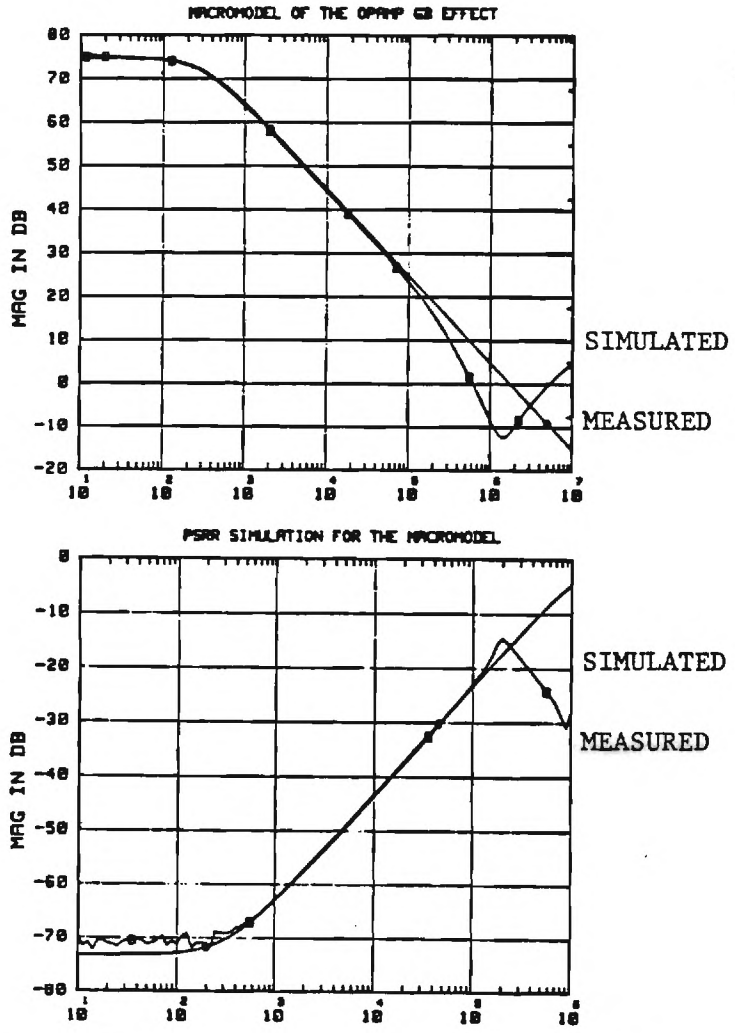


Fig. 5 - PSRR and GB simulation compared to experimental results.

controlling node of the op amp. This model will include both 1/f and thermal noise. The noise of the switches will not be modeled.

Although CAD limitations on circuit performance have yet to be identified, the background has been established to make significant progress toward the goals of this research. After the noise model is complete, noise and PSRR measurements will be made on the above circuits plus others. The performance of the HC-5512 will be compared in detail with the AIDE2 version of this circuit. It is hoped that the comparison of the three circuits of Fig. 3 will suggest experiments which will identify and isolate the causes of performance limitations due to CAD techniques.

3.0 ANALOG SILICON COMPILERS

The AIDE2 program has served as a CAD platform on which to gain experience in developing analog silicon compilers. The quick and successful design of complex analog and digital systems is very important to ASIC applications. Previous reports [4] described the development of a silicon compiler for successive approximation analog-digital and digital-analog converters (ADDAC). A four-bit A-D converter was fabricated using the Harris CMOS technology. Unfortunately, there were no V_{DD} connections to each of the three latches in the four successive approximation registers. In addition, a shift in the layout caused shorting in the routing and power busses.

One of the goals accomplished during the year was the conversion of the cells for ADDAC to the MOSIS 3 micron, double-poly, CMOS process. The comparator was redesigned and several test cells were devised to help evaluate the 8-bit A-D converter which was also designed. The individual cells of the converter were thoroughly simulated. An attempt was made to simulate the entire converter using SPLICE. SPLICE was able to simulate up to four bits of the logic portion of the converter. A mixed analog-digital simulator capable of simulating the entire circuit was needed.

In the Spring, an 8-bit, successive approximation, analog-digital converter and test cells were submitted to MOSIS. A photograph of the layout is shown in Fig. 6. Examination of this circuit revealed four classes of errors. The first errors were layout errors which were corrected by microsurgery. The second errors were software errors in the CAD program which caused a 5 micron shift in the various cells. Unfortunately, microsurgery could not correct the problems which resulted. The third category of errors were design errors and included a charge sharing problem. The last category of error was fabrication errors due to the silicon foundry. The metal runs

showed numerous short circuits between adjacent metal and discontinuities in metal runs. The first three errors have been corrected and a resubmission of the circuit for fabrication has been made.

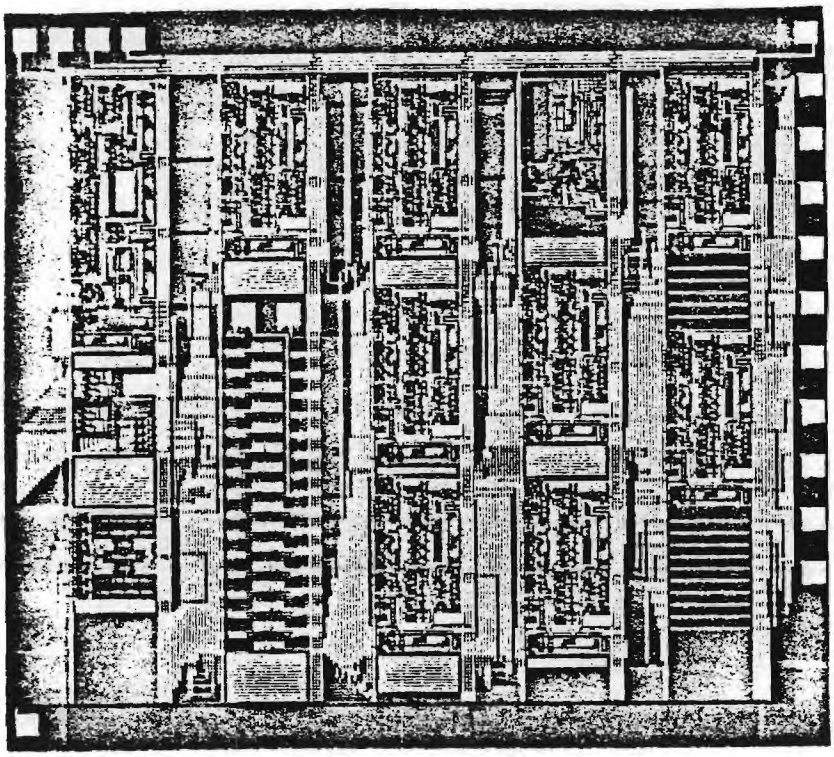


Fig. 6 - 8-bit, successive approximation A-D converter designed by ADDAC.

Future plans include measurement of the resubmitted circuit with emphasis on the performance limitations. This circuit will also serve as an example circuit for the multilevel, mixed analog-digital simulation research. An attempt will be made to identify a comparable commercial product and to compare the performances of the two circuits.

4.0 CELL COMPILER

The objective of the cell compiler of AIDE2 program is to develop the component level use of AIDE2 for generating the simulation and layout of the basic component which can be implemented into the AIDE2 program. The component level use would correspond to case when the designer is not

satisfied with existing blocks or cells and wants to develop his own which he can have the total control of the circuit design and layout.

Fig. 7 shows the cell compiler organization which can be incorporated into AIDE2 program. Once the user writes the cell description program with the cell schematics with structural information and layout control, the parameter preprocessor which already exists in AIDE2 will receive the parameter data from circuit description and technology information such as design rules or device parameter, from the technology file in the library. Then the cell compiler will receive the information on the parameterized cell from the preprocessor and place and/or interconnect and generate the simulation and/or layout file for the basic component which can be implemented to the AIDE2 program.

The basic objective of the simulation for the automated component design is to translate the user's circuit description which includes the structural

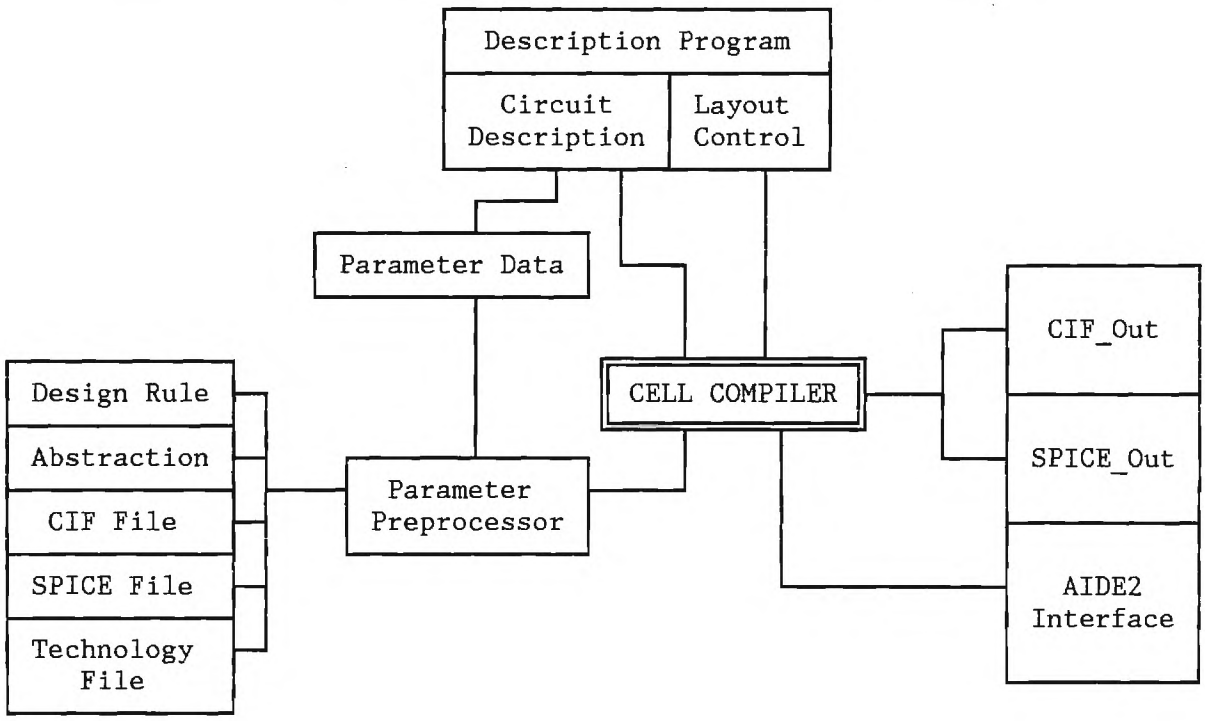


Fig. 7 - Organization of the cell compiler.

database of the circuit into a form that a simulation program such as SPICE can understand. Once the circuit has been defined by the user in the description program for generating analog circuit from transistor level rather than polygon level, the cell compiler gets the information on the device name, transistor netlist description which shows the four nets for the drain, gate, source, and substrate, types of the transistor such as P-type or N-type, and width/length variables to create the geometry.

For the layout, we are now using the parameter preprocessing technique for component generation. This technique allows the data from circuit description and library cell to be modified by software which produces the component level circuit description and optimizes the circuit design to achieve the desired input specification. Especially, the cell compiler aspect of AIDE2 research address the problem of permitting cells using new or different technologies to be quickly implemented into AIDE2 library.

The technology independence of the cell compiler should be considered from the two viewpoints for simulation and layout. During the translation to SPICE format, the cell compiler can access to the process parameter database in the technology library to make the cell compiler be flexible to give a wide range of user specification and to compile correctly for various foundry process. Design rule independence for the layout can be achieved by expressing the locations of each device in terms of the foundry dependent design rules. Depending on the choice of foundry, the required spacing or width of the each layer will be determined. The parameters can be considered by two databases: process parameter and user-definable parameter. The process parameters are subject to the technology and the user-definable parameter can be controlled by the user during the circuit design. This can be done by allowing AIDE2 program from a technology file in internal AIDE2 library or

from a technology provided by the user-interactive routines so that files can be altered or replaced to represent different fabrication technology at different installations.

In summary, we have been developing the cell compiler to create the new cells using different technologies, developing the parameterized cells to support the geometric data for layout of cell, and trying to implement cell compiler into AIDE2 program.

5.0 PRECISION ANALOG MODELS FOR SHORT CHANNEL CMOS

The objective of this research is to develop models for analog circuit design which are more accurate and more computer efficient than existing models. Existing models demonstrate significant error in small signal applications [7]. The first phase of this research attempted to identify the model methodology which would be most appropriate for solving the problem. The methodologies considered were analytical, empirical, table look-up, and combinations for these three. Of the approaches, the table look-up approach offered the best solution from the standpoint of accuracy, adaptability, and complexity.

Initially, the small signal conductance and transconductances were stored as a function of the terminal voltages with respect to the source voltage of the MOSFET. However, it turned out to be more efficient to store the drain current as a function of the terminal voltages (V_{DS}, V_{GS}, and V_{BS}). This data not only provided an alternative to present large signal modeling methods (which appear to provide sufficient accuracy) but permitted the small signal conductance and transconductances to be generated more efficiently.

In order to be able to apply the model methodology to a short-channel analog circuit, a test array, 3 CMOS inverters, and 2 op amps were designed using minimum channel lengths of 1.6 microns. The model methodology will be

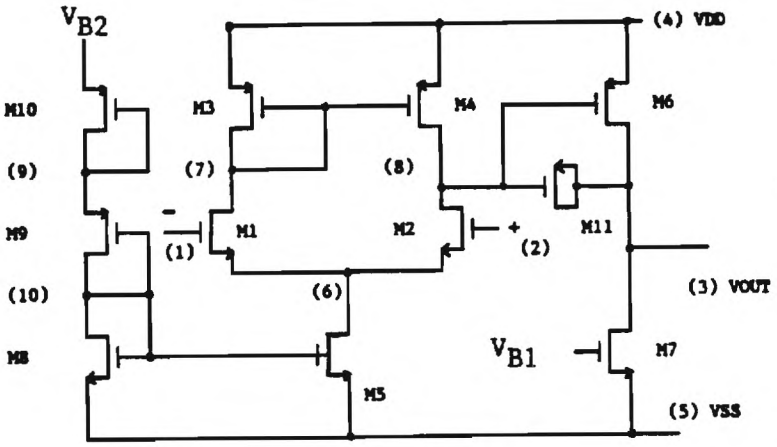
applied to these circuits and compared to the experimental response. The test array had the W/L values given in Table 2. The CMOS inverters had PMOS/NMOS W/L ratios of (4.8/1.6)/(1.6/1.6), (9.2/2.4)/(2.4/2.4) and (24/8)/(8/8). Fig. 8 shows the schematic and W/L values for the op amp with all L values equal to 1.6 microns (except for M9 through M11). A second op amp with identical W/L ratios but with L equal to 3.2 microns was also designed and fabricated.

Device Type	W/L in microns/microns							
NMOS	16/1.6	16/2.4	16/3.2	16/8	16/16	1.6/1.6	2.4/2.4	8/8
PMOS	16/1.6	16/2.4	16/3.2	16/8	16/16	4.8/1.6	7.2/2.4	24/8

Table 2 - W/L values of test array devices.

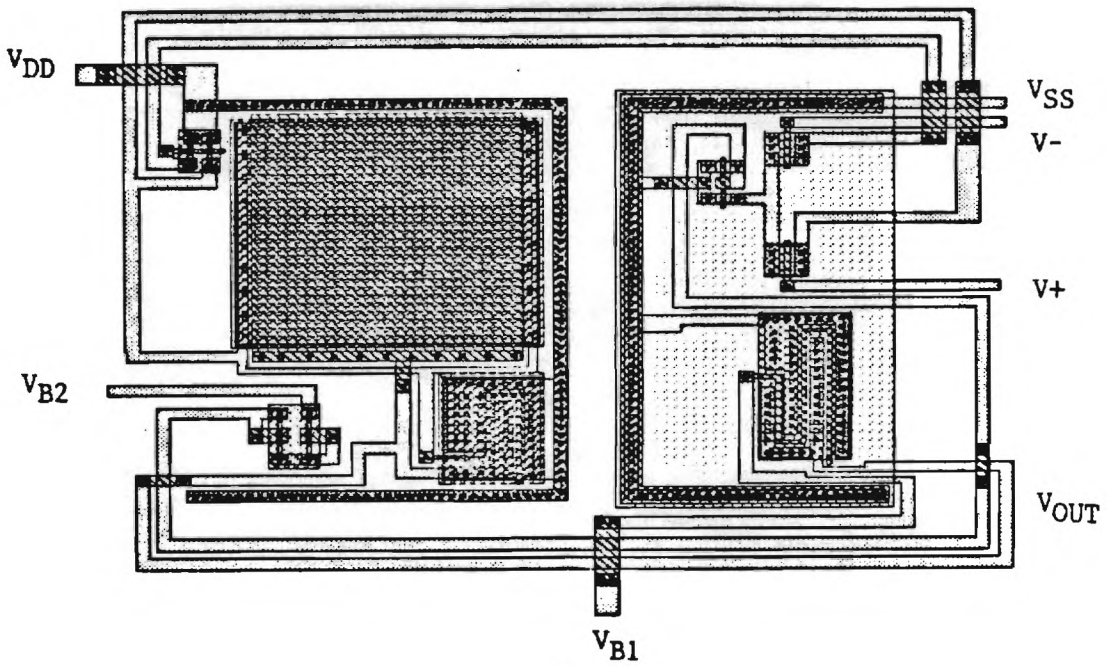
The next step in this research was to implement a means of extracting the model data for the table look-up. The extraction methodology was developed on the HP 9836 in conjunction with the HP 4145 Semiconductor Parameter Analyzer. Typically, more points are measured than are stored in the table. Once the data is contained in the table, it was necessary to employ interpolative methods to be able to apply the model. A piecewise hermite cubic spline technique was employed to interpolate data points between data stored into the table array for the large signal model. However, the same interpolation technique was not able to generate the smooth and monotonous small signal model parameters. Therefore it was necessary to modify the piecewise hermite cubic spline technique so that it could produce smooth and monotonous small signal parameters with the desired accuracy. This was accomplished by calculating the small signal model parameters at the data points and interpolating between these small signal model parameters.

The table look-up model has been successfully applied to MOS devices to model the large signal characteristics and the frequency independent small



(a)

Geometric Dimension W/L (in microns)	
Device	W/L
M1	14.4/1.6
M2	14.4/1.6
M3	1.6/1.6
M4	1.6/1.6
M5	4.8/1.6
M6	100.8/1.6
M7	166.4/1.6
M8	4.8/1.6
M9	1.6/6.4
M10	1.6/6.4
M11	100.8/100.8



(b)

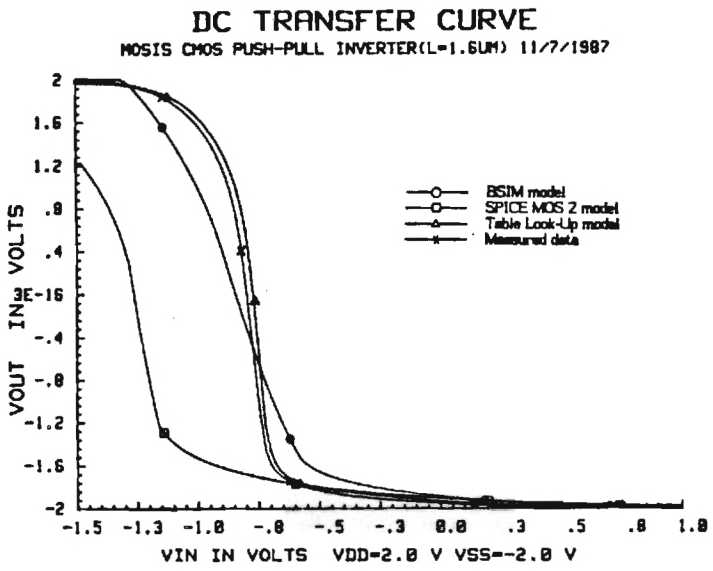
Fig. 8 - (a.) Op amp and W/L values which was designed to test the model methodology. (b.) Layout of the op amp using a channel length of 1.6μm.

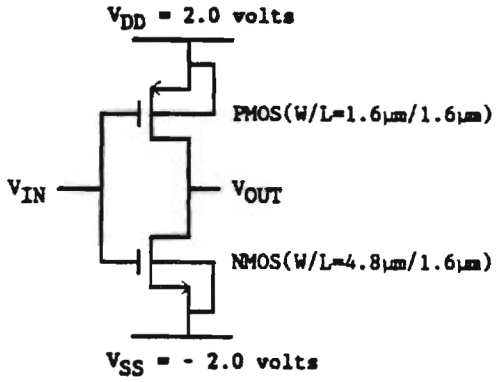
signal characteristics. It has also been applied to GaAs MESFET devices to illustrate the adaptability of the model. The table look-up model was installed in a version of SPICE 2G.6 containing the BSIM model for purposes of comparison. It has been applied to the CMOS inverters described above to simulate the DC and small signal frequency independent performance. The results of the table look-up model are compare with the SPICE Level 2 and BSIM models in Fig. 9. It is shown in Table 3 that the accuracy of the table look-up model is at least an order of magnitude less using less CPU time than the BSIM or SPICE Level 2 models.

	Accuracy (RMS % Error)		CPU Time (Seconds)	
	NMOS: (W/L= 4.8μm/1.6μm)	PMOS:(W/L= 1.6μm/1.6μm)	NMOS	PMOS
BSIM	22.19	33.24	5.37	5.43
SPICE 2	109.04	80.16	5.53	5.58
Table Look Up	0.8	2.36	3.18	3.32

Table 3 - Accuracy and efficiency comparison of analog models.

The next steps in this research are to improve the computation efficiency and accuracy of the model further, include the gate-source and gate-drain capacitances into the model, and to extend the model to include temperature. A method for automatically extracting the capacitances has been developed and verified. This method is based on techniques proposed in the literature [8,9]. The table look-up model will be applied to the op amps of Fig. 8 and compared with SPICE Level 2 and BSIM models for accuracy and efficiency.





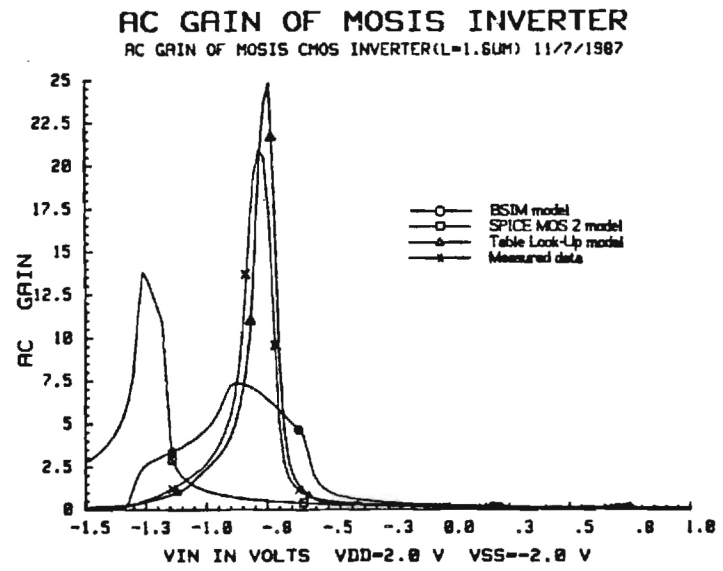


Fig. 9 - Large and small signal model comparison for the CMOS inverter.

6.0 MULTILEVEL ANALOG SIMULATION

Efficient use of CAD tools to design complex analog and digital IC's requires an efficient and flexible simulation capability. Simulators must be able to simulate at the level of design particularly as the design level increases. Presently, complex commercial circuits are simulated in part but never simulated from an overall viewpoint. The objective of this research is to develop simultaneous methods of simulating analog circuits at any of the three levels; behavioral, functional, or circuits.

A simulator has been developed using signal flow methods to characterize and simulate circuits at the behavioral level. This simulator was called Graphical Analysis Program (GAP) and uses well-known methods to find either the linear frequency or time domain response from a signal flow graph description of the circuit to be simulated. The signal flow graph simulation primitives are interesting in that they have an inherent transparency to the various levels. For example, a branch of a signal flow graph can be as simple as the ohmic relationship between current and voltage in a single element or as complex as the polynomial for a high-order filter.

GAP has been coupled to SPICE in a crude manner to examine one possible approach to a multilevel simulator. SPICE has been used to solve for the DC solution of the circuits using normal SPICE primitives and the primitives of the signal flow graph at DC. The DC solution has been used to linearize the circuit level (SPICE) part of the circuit. The linearized, circuit level is easily converted to a signal flow graph primitive and the entire linear response simulated by GAP. Needless to say, the success of this method depends greatly on the circuit which is to be analyzed. A large number of branches in the graph will cause the solution to become very inefficient.

To illustrate the efficiency of higher level simulators, the circuit of

Fig. 10 was solved by the GAP program and by SPICE. The op amps were considered to be ideal with infinite voltage gains. After deriving the graphs, GAP was used to find the frequency response of the filter. The total time required was 0.32 CPU seconds (VAX 11/780). The total time required for SPICE to find the frequency response was 5.0 CPU seconds (VAX 11/780). The simulation results were found to be identical. For this example, the speed up in simulation was approximately 30.

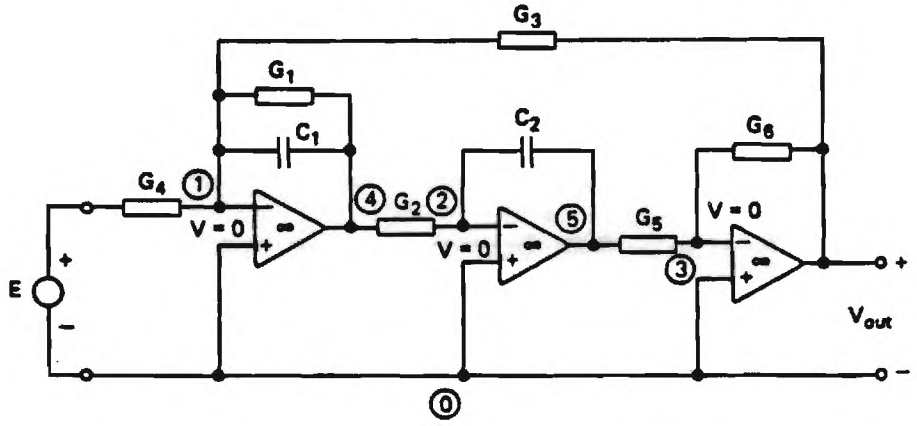


Fig. 10 - Second-order, active filter used to compare GAP and SPICE.

One of the difficulties in using GAP is the preprocessing that must be done to convert a circuit to the signal flow graph primitives. A preprocessor is being developed to do this step automatically and will increase the time required for the higher level simulation. Presently, the multilevel analog simulator (MAS) consists of SPICE PAC [10] and GAP simulators. An input processor allows graphical behavioral models to be included in the SPICE input description. The input processor constructs a graph which contains the necessary data for a DC solution by SPICE. After the DC solution, a graphical solution can be made using GAP.

Methods of more efficiently solving the signal flow graph have been investigated. Two methods examined include a decomposition method without

rearranging any graph branches. This method is projected to be effective at reducing the graph processing time and is also expected to be easily applied to most type of MOS circuits. The second method is intended to be used following the application of the first method. It rearranges the branches of the graph in a manner which does not change the results of the analysis, but which simplifies the analysis. By rearranging the branches, disconnected substitute graphs are produced allowing the implementation of a divide and conquer approach to graphical analysis. The status of this research effort has been summarized in a report titled "Multilevel Analog Simulation: Status of Research at Georgia Tech" [11].

Before continuing this research, it is proposed to obtain and evaluate two existing simulators which claim to be multilevel analog simulators. These simulators are IGSPICE [12] and SABER [13]. These simulators will be examined carefully from the viewpoint of true hierarchical capability, the interrelationships between the simulation level primitives, and the capability of interfacing or including digital circuits. Two benchmark circuits have been selected to test the simulators. The first is the 8-bit successive approximation analog-digital converter described section 3.0 and the second is a 1200 baud modem.

7.0 MIXED ANALOG-DIGITAL SIMULATION

Practical integrated circuits contain much more digital than analog circuitry. For this reason, it is important that the development of CAD tools also work with digital circuits. In fact, the CAD tools for both types of circuits are not inseparable. The objective of this research is to incorporate existing digital multilevel simulators [14-16] into the multilevel analog simulator research described above. The mixed, analog-digital simulation problem has been reported to be of great interest to SRC member

companies.

The first effort was an extensive literature review to become familiar with existing work on the subject. Next, nine SRC companies and two non-SRC companies were visited concerning this research. The impetus of these visits was to obtain the companies' perspectives on exactly needs to be done on this problem and to identify areas of research. Among the information received from these companies were wish lists, specific applications to which a mixed-mode simulator would be applied, and possible approaches to the problem. The outcome of these meetings was, in general, twofold. First, the meetings served to identify Georgia Tech's interest in the mixed-mode simulation problem to industry. Secondly, valuable "real-world" insight was acquired to this problem. This insight may quite helpful in defining what exactly is to be done in our research. Lastly, a SSCTC workshop on mixed-mode simulation and an SRC conference on design verification were attended to learn of the most recent developments in this area.

The most significant problem encountered during this research has been the actual definition of what needs to be done. The main goal of the next effort is to mentally and physically define the research problem. This will be accomplished by reviewing the information obtained in meetings with companies, at conferences, from the literature, and from further discussions with academic and industrial contacts. A report titled "Mixed Analog-Digital Simulation Survey" includes more information on the results of visiting the companies shown in Table 4 [17]. Hayes Microcomputer Products in Atlanta and Texas Instruments in Dallas were also visited, but no presentation was given. The first step in this research area will be to examine existing programs which claim to be solutions to the mixed analog-digital simulation problem. These programs will be evaluated and measured against a benchmark circuits

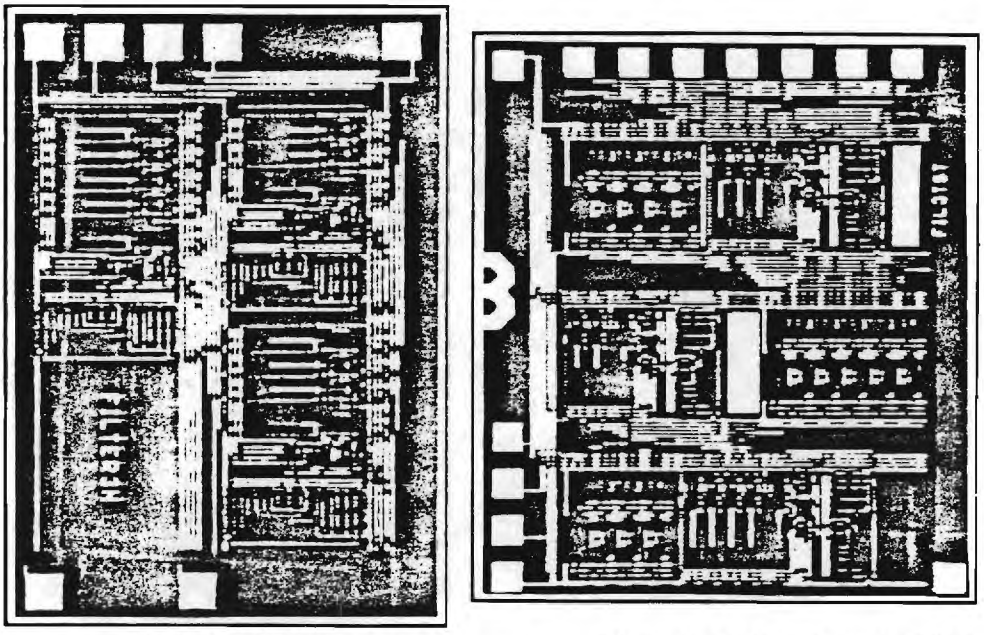
used for the multilevel analog simulation research.

Company	Date	Location
Rockwell International	Aug. 10	Newport Beach, CA
Hughes Aircraft	Aug. 11	El Segundo, CA
Silicon Systems	Aug. 12	Tustin, CA
Hewlett-Packard	Sept. 1	Santa Clara, CA
National Semiconductor	Sept. 2	Santa Clara, CA
GE Intersil	Sept. 3	Cupertino, CA
AT&T Bell Labs	Sept. 14	Murray Hill, NJ
General Electric	Sept. 17	Schenectady, NY
Analog Devices Semiconductor	Sept. 18	Wilmington, MA

Table 4 - Companies visited concerning mixed analog-digital simulation research.

8.0 BUILT-IN TESTABILITY OF AUTOMATICALLY GENERATED ANALOG CIRCUITS

The testability described in earlier research results [4] was applied to a third-order filter in order to determine the influence of the test methodology on the performance of the circuit. Fig. 11 is a microphotograph of the third-order without built-in testing and with maximum built-in testing



Circuit without testing Circuit with maximal testing

Fig. 11 - Third-order filter without and with maximum testing capability.

capability. The circuit having maximal testability required an area penalty of 1.75 compared to the circuit with no testing capability. Unfortunately, the clocks for the serial shift register were mistakenly connected internally to the clocks of the switched capacitor filter which prevented the circuit with the testing capability from working. This mistake is being corrected and the circuit refabricated. The nature of this testability would be appropriate for first time implementation of the circuit where one wishes to obtain a maximum amount of diagnosabilty if the integrated circuit does not work.

9.0 AUTOMATED DESIGN OF ANALOG CIRCUITS

The research concerning automated design of analog circuits is oriented to the circuits level and is designed to interface with the cell compiler described in Section 4.0. There are three separate activities that constitute the research in this area. The first is a PC-based program written in PASCAL which will generate the design of a two-stage, unbuffered CMOS op amp. The second is an extension of the previous program allowing a selection of four possible topologies to implement the specifications. The third activity is the development of a generalized synthesis capability for analog integrated circuits independent of technology.

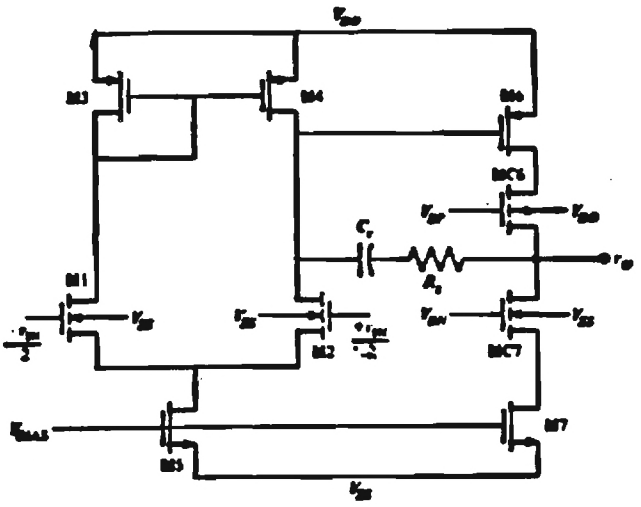
The approach selected in developing automated design programs to date has used algorithmic methods. Algorithmic methods are defined as those which given an input, the output(s) are predictable. While artificial intelligence and associated techniques have been closely examined, they have not been used. The thrust of this research has been to develop the relationships and methodology which allows the design of analog circuits to be implemented by CAD means.

The first research activity had the objective of becoming familiar with the problems of implementing the automatic design of an integrated circuit.

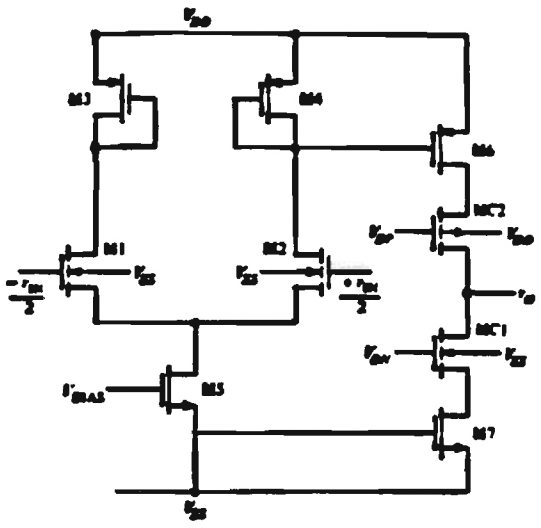
The automated design of a two-stage, unbuffered CMOS op amp was selected because its design is well understood. The resulting PC-based program is called AUTOAMP and is described in more detail in an internal report [18]. The inputs to AUTOAMP are the DC gain, gain bandwidth, input common mode range, output voltage swing, slew rate, power dissipation, power supply voltages, and the load capacitance. The SPICE model parameters for the technology used must be inputted. The program uses relationships which associate the performance specifications with the design of the individual transistors of the fixed topology op amp. The output is a SPICE file containing the W/L ratios of each of the transistors. Two different op amps have been designed using AUTOAMP and are being fabricated in the MOSIS 3 micron, double poly process. When these op amps are fabricated, their performance will be compared to the original specifications.

The second activity in the area of automated design of analog circuits was to create a program similar to AUTOAMP but capable of topological modification. The resulting program called SMARTAMP was written in C and implemented on the VAX or MicroVax. It permits the design of a two-stage, unbuffered CMOS op amp where each stage has two possible topologies which offer significantly different performance capabilities. The possible topologies are shown in Fig. 12. The input stage consists of a high-gain or low-gain differential amplifier. The output stage consists of a Class A or a cascode, push-pull amplifier. The various combinations of these stages provide a much wider set of input performance specifications that can be satisfied than the AUTOAMP program.

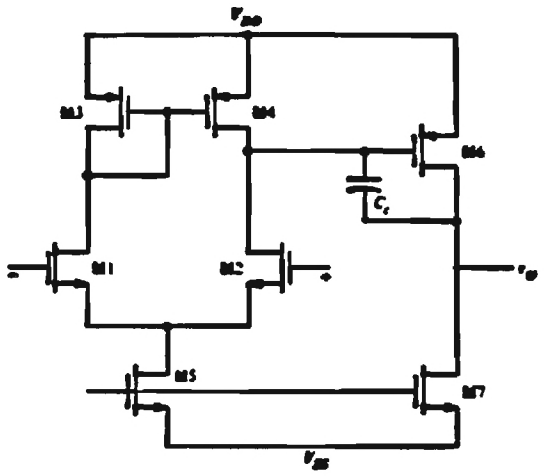
The inputs are similar to the AUTOAMP program except that the noise performance can also be specified. Each specification can have a weighting factor which is used to help select the best of four possible combinations to



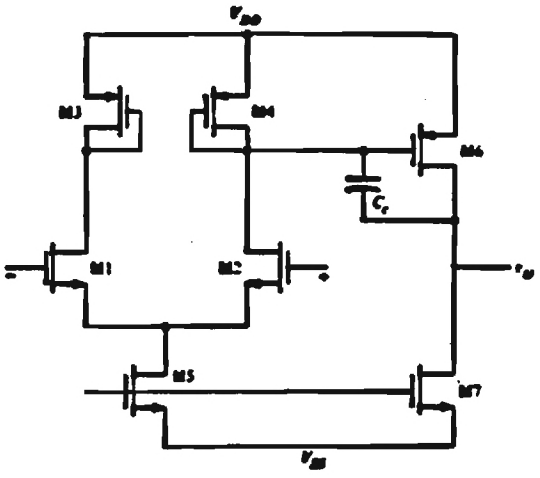
circuit "B"



circuit "D"



circuit "A"



circuit "C"

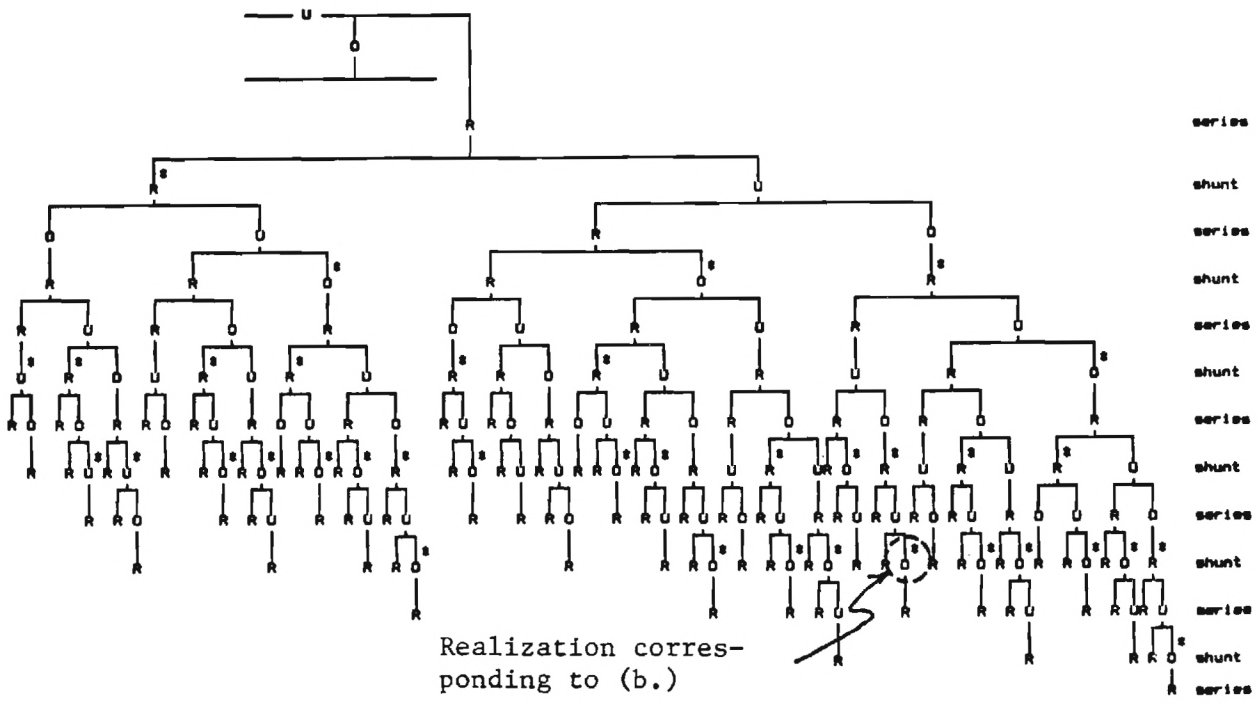
Fig. 12 - Four possible topologies used by the SMARTAMP program.

satisfy the specifications. The program interacts with the designer andpermits changes of the specifications to help reach a design compromise. The output file consists of a SPICE input file containing the W/L ratios. The SMARTAMP program has been written and debugged. Examples of various designs have been tested. The incorporation of the noise specification has not been satisfactory and is being re-examined. When the noise specification is complete, several circuits will be designed and implemented to compare the experimental performance with the original specifications.

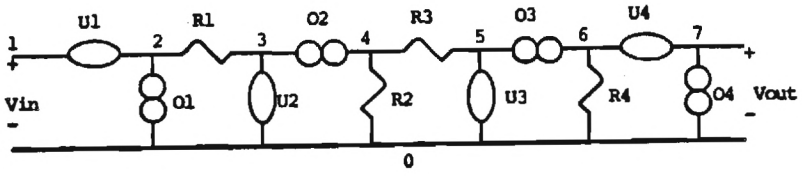
The third area of research in this area is the development of a generalized design capability for analog integrated circuits. A suitable methodology has been identified and is in the process of being implemented. The methodology uses the concept of degenerate circuit elements [19] to generate realizations to a given transfer function. The first step in this effort is to be able to generate all the degenerate circuit element realizations given a two-port, frequency independent transfer function. The second step is the selection of practical circuit realizations given the technology (MOS, BJT, BIMOS, etc.).

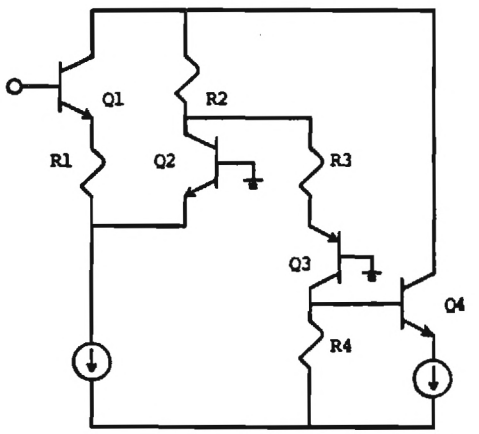
The input to this program is the transfer function value and whether the input and output variables are voltage or current, the input resistance, and the number of active devices. An algorithm has been developed which will find all possible realizations in terms of degenerate circuit elements (nullors) and resistors. The present topology is limited to a ladder topology but will be generalized. Fig. 13 shows all possible realizations for a voltage-controlled voltage source (VCCS) having infinite input resistance and a positive real gain.

One of the key steps in this approach was the development of an efficient method of analyzing the realization to verify its correctness. A method of



(a)





(b) (c)

Fig. 13 - (a.) The possible realizations of a VCCS using no more than 4 active devices. (b.) Nullor realization. (c.) Practical BJT realization.

matrix manipulation based on degenerate circuit elements has been developed. This method allows the quick analysis of a circuit containing degenerate circuit elements. The beginning point is to form a nodal admittance matrix of all elements in the realization which are not degenerate circuit elements. Next, the influence of each degenerate circuit element is applied to reduce the matrix. For example, a nullator connected from the ith node to ground will cause the ith column to be deleted. A nullator connected between the ith and jth node will cause the ith and jth columns to be added. A norator connected from the ith node to ground causes the ith row to be deleted. Finally, a norator connected between nodes i and j will cause the ith and jth rows to be added.

The next step is to take each successful degenerate circuit element and to transform it into a practical circuit realizable by the desired technology. The combination of a nullator, norator, and resistor of $1/g_m$ ohms is realized very closely by a BJT or MOSFET device. For the BJT, it is also necessary to add a resistance of value r_π to account for low values of β. Techniques of transforming degenerate circuit elements into practical integrated circuits have been developed [20,21] and will be investigated.

The methodology developed to manipulate the nodal admittance matrix can be reversed to expand a desired transfer function given in terms of a simple two-port nodal admittance matrix into a realization containing the individual passive elements (resistance and capacitance) and degenerate circuit elements. This will provide a general realization methodology for a frequency dependent transfer function.

The results of the design methodology using degenerate circuit elements are expected to be of importance to both the novice and expert analog circuit designer. The program can serve as a tutor to the new designer in providing

ideas for design and providing direction for investigation. The experienced designer could use the program to check that no design possibility has been overlooked and to confirm the design proposed. While the program will be capable of designing circuits such as op amps, it will also be capable of designing higher level systems such as filters. Interestingly enough, the resulting system designs will follow a localized feedback philosophy rather than a global feedback philosophy. This may have some application to extremely high frequency signal processing circuits using technologies capable of operating at 500 MHz and higher.

10.0 SUMMARY AND PLANS

This report has summarized the results of research performed in analog CAD methodology during the academic year, 1986-1987. The objective of this research in the area of computer aided design and modeling of analog integrated circuits is to develop methodologies for analog circuit design which can be implemented by the computer. This research supports the SRC goals by developing methodologies for analog integrated circuit and implementing them in a software platform that can be used together with digital CAD tools to design and layout signal processing systems containing both analog and digital circuitry.

This report has described the results of the fourth year (1986-87) of research in the area of analog CAD methodology and its application to analog integrated circuit design. It has addressed the addressed the following eight areas: 1.) performance oriented CAD, 2.) analog silicon compilers, 3.) cell compilers, 4.) analog device modeling, 5.) multilevel analog simulation, mixed analog-digital simulation, 7.) testability of analog IC's, and 8.) automated design of analog circuits.

The research has now progressed to the point where several areas are beginning to mature. The CAD tools have been used design successful integrated circuits which have been fabricated and measured. This information is providing input on the actual capabilities and limitations of analog CAD. The efforts to achieve a more accurate model for analog IC design has resulted in an order of magnitude more accuracy using less computational time than existing methods. Several of the other areas described in this report are showing promising results.

The plans for this research activity are to follow through on what has been started. It is anticipated that the research on precision models for analog circuit design using the table look-up approach will be complete in December 1988. This work will be implemented into SPICE along with a Basic program designed to use the HP controller and semiconductor parameter analyzer to automatically extract the model parameters.

The performance limitations in analog circuits due to CAD techniques should be characterized and identified. Depending upon the results, an effort may or may not be made to develop performance optimized CAD techniques for designing analog circuits. The benchmark filter will be compared in more detail with the result using the AIDE2 program.

The analog silicon compiler research will continue with the measurement of the resubmitted circuit with emphasis on the performance limitations. This circuit will also serve as an example circuit for the multilevel, mixed analog-digital simulation research. An attempt will be made to identify a comparable commercial product and to compare the performances of the two circuits. A generalized high level compiler may be developed depending upon the results of this phase of the research.

An important link in the automated design process is the implementation of the designs into a CAD environment such as AIDE2. The cell compiler research will be used to create the new cells using different technologies. The capability of compiling parameterized cells to support the geometric data for layout of the cell will be incorporated into AIDE2 program. The knowledge gained from the study of the performance limitations will be used in this research effort.

The next step in the multilevel, analog simulation research is to obtain and evaluate the multilevel analog simulators called IGSPICE and SABER. These simulators will be examined carefully from the viewpoint of true hierarchical capability, the interrelationships between the simulation level primitives, and the capability of interfacing or including digital circuits. Two benchmark circuits have been selected to test the simulators. The first is the 8-bit successive approximation analog-digital converter described section 3.0 and the second is a 1200 baud modem.

The mixed analog-digital simulation research will follow up on the information and momentum gained by the various visits last summer by examining the existing programs which claim to be solutions to the mixed analog-digital simulation problem. These programs will be evaluated and measured against a benchmark circuits used for the multilevel analog simulation research.

The plans for the automated analog design research are to measure the experimental performance of the op amps designed by AUTOAMP, to complete the SMARTAMP program and generate several examples to test the program, and to take each successful degenerate circuit element realization of a frequency independent transfer function and to transform it into a practical circuit realizable by the desired technology. The program will next be extended to include frequency dependent transfer functions.

As the various parts of Fig. 1 begin to mature, methods and techniques of designing analog and digital integrated circuits using the computer which increase design productivity and performance will be available to SRC member companies. One of the advantages of this research program is that an overall viewpoint is being taken to the problem of automatic implementation of complex circuits and systems. It is important that the simulation capabilities are consistent with the design capabilities. The next few years should see a real payoff to SRC member companies in the expertise developed and students graduated.

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