LARGE-SIGNAL RELIABILITY OF SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTOR AMPLIFIERS

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2016

LARGE-SIGNAL RELIABILITY OF SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTOR AMPLIFIERS

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for my family

ACKNOWLEDGEMENTS

Were it not for the invitation of Dr. Cressler to join his group at a critical moment in my graduate education, I would never have earned a Ph.D. at Georgia Tech. I thank him for committing to me and helping me to develop as a professional. I was truly fortunate to have landed in his group, and will always be grateful.

I thank the current and former members of the SiGe Devices and Circuits Group for their support over the years. Special thanks must be extended to Seungwoo, Ick-hyun, Saeed, Adilson, Peter and Zach for their collaborations on various publications. I am deeply indebted to Brian, Uppili and Partha for helping me enter the realm of device engineering by answering my incessant questions.

I am very thankful for the resources my sponsors have given me. I thank RFMD, Qorvo and Raytheon SAS for supporting my Ph.D., and Samsung, the GEDC and the Institute for supporting my initial efforts at Georgia Tech. Special thanks to Glenn, Cynthia, Julio, Mike, Phil, Kyu Hwan, Dong-Ho, and Chang-Ho. I also thank my dissertation reading committee for accepting my invitation to serve and for providing feedback on this work.

Having taught my first classes at Georgia Tech, I now realize how truly great my teachers have been over the years. At the top of the list, directly above my advisor, are my parents, Ted and Wanda. My father is the greatest teacher I have ever had, without question, and I deeply appreciate the example he has set for me. My mother's kindness and love are undeniable influences on my character, and I am thankful to be her son. Finally, thanks to my extremely talented sister Amanda for convincing everyone that I am smart. Hopefully, from time to time, I will be.

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SUMMARY

This objective of this work is to answer open questions related to the large-signal reliability of SiGe HBT amplifiers. These questions are primarily focused on the impact of large RF voltage swings on both the base of LNAs and the collector of PAs. The limitations set by time-varying *ac* voltage swing had been cursorily investigated, but not to the depths explored in this dissertation. At the basic level, the evaluation of internal device temperatures is a crucial aspect of the knowledge set forth in this document. The primary benefit of this work is to set forth techniques that maximize the performance of SiGe HBT PAs without sacrificing long-term reliability. Additionally, the input power ruggedness of LNAs can be maximized with these techniques. The understanding communicated in this dissertation can be applied to failure analysis of SiGe HBT amplifiers in any circuit, such that the impact of *dc* voltage bias and *ac* voltage swing can be quantitatively reasoned as the root cause.

It is the intention of the author that circuit designers will be able to glean essential device knowledge to maximize performance, and device engineers will obtain a perspective on amplifier design necessary to advance technology toward the needs of a required specification. Bridging the gap between the two disciplines is the overarching principle of this work, which is organized as enumerated below.

1. An introduction to the SiGe HBT device concepts necessary to understand the work is established.

2. An analysis of SiGe HBT driver amplifier reliability under large *ac* swings is presented. The capacitive portion of the collector current is separated from the simulated current to understand voltage swing beyond *dc* breakdown conditions. This work was first presented at IEEE RFIC 2014 in Tampa Bay [1] and later

extended to *IEEE Transactions on Electron Devices* [2].

3. An in-depth analysis of the thermal effects of a third-generation SiGe HBT as part of a LNA is conducted. Measurement on various LNAs and cascode structures are presented, showing noise degradation caused by large negative swings on the base of the amplifier. This has been submitted for publication to *IEEE Transactions on Electron Devices* [3].

4. Waveform analysis of SiGe HBT devices as well as TCAD visualizations of the thermal impact inside the device under *ac* operation are explored. This work is a first step beyond the concepts in [2] and supplements the work described in [3] in a separate technology.

5. Assessment of mutual thermal coupling between devices in a SiGe HBT power array is presented. The impact of process variations on array temperature is visualized electrically for the first time. This work has been submitted for publication to *IEEE Transactions on Electron Devices* [4].

6. Switches on high-resistivity (1 kΩ) substrate are briefly evaluated for three applications: SPDT antenna switches, resizable power cores and programmable arrays of capacitors. Comparisons to 50 Ω substrate are also provided.

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Acknowledgment of Support

This material is based upon work supported by Raytheon Space and Airborne Systems, RF Micro Devices and Qorvo.

CHAPTER 1

INTRODUCTION

1.1 Origin and History of the Problem

The two most important failure mechanisms to consider when designing integrated silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) circuits are electromigration and impact ionization [5,6]. Electromigration is a well-understood topic concerning void formation in metal, and from this understanding the average lifetime of integrated circuit interconnects can be established [7]. If SiGe HBT interconnects are designed to withstand electromigration issues, operational lifetime of the device will be dominated by this mechanism, assuming guidelines set for the voltage across transistor junctions are also followed. Properly quantifying voltage maximums under large-signal operation, particularly at the output of power amplifier (PA) transistors, remains an unsolved problem that must be addressed in the field of SiGe HBT reliability.

Limitations on junction voltage are necessary to reduce impact ionization, which causes hot-carrier damage and eventual breakdown of the collector-base (CB) junction once a critical electric field is reached. Although the effects of impact ionization can be simply correlated to constant current conditions for a given SiGe HBT circuit, the onset and extent of the resultant damage created under radio frequency (RF) operation is not completely understood, therefore safe operating conditions are derived solely from direct current (dc) measurements in practice. This leads to unnecessarily conservative biasing of large-signal amplifiers, wasting the efficiency and output power benefits attributable to maximized voltage swing. Therefore, the careful study of differences between dc and RF operation with respect to impact ionization will result

in optimized, and reliable, large-signal PA performance using SiGe HBTs.

Understanding RF reliability is an important step for SiGe HBTs, which are consistently integrated with silicon complementary metal-oxide-semiconductor (CMOS) processes to leverage the advantages of bipolar and CMOS transistors in a single platform (BiCMOS) [8]. SiGe HBTs also exhibit a robustness to radiation, allowing implementations in extreme environment electronics [9]. In extreme environment radar applications, voltage swing maximums are particularly important as output power is the primary design objective, and cascode amplifier cores are typically employed to increase voltage handling. Since the impact of hot-carrier damage can be mitigated with a cascode configuration, through the isolation provided by the additional device, the true limitation impact ionization introduces in a cascode amplifier is catastrophic failure due to avalanche breakdown [1]. Hence, quantifying this limit in terms of RF voltage and current for various SiGe HBT technologies will provide device and circuit designers an essential tool for optimizing performance.

Reliability analysis of large-signal bipolar circuits is an under-investigated topic in electronics design literature, perhaps due to the complexity presented by time-dependent thermal considerations necessary to correlate RF to *dc* damage. Most explorations in the literature concerning SiGe HBTs are limited to either *dc* safe operating area (SOA) or qualitative RF comparisons [10–15].

To get at RF reliability, a well-founded understanding of SiGe HBT hot-carrier effects and avalanche-induced breakdown is necessary. The next two sub-sections review these topics in the context of a cascode amplifier (Figure 1.1), a widely used topology for SiGe HBT amplifiers, in large part due to its increased voltage handling.

Subsequently, electromigration in extrinsic back-end-of-line (BEOL) metals will be discussed briefly to further present the complexity of design for reliability. In the final two sub-sections, an overview of benefits arising from high-resistivity substrates and the limitations of CMOS RF stress will be simply stated.

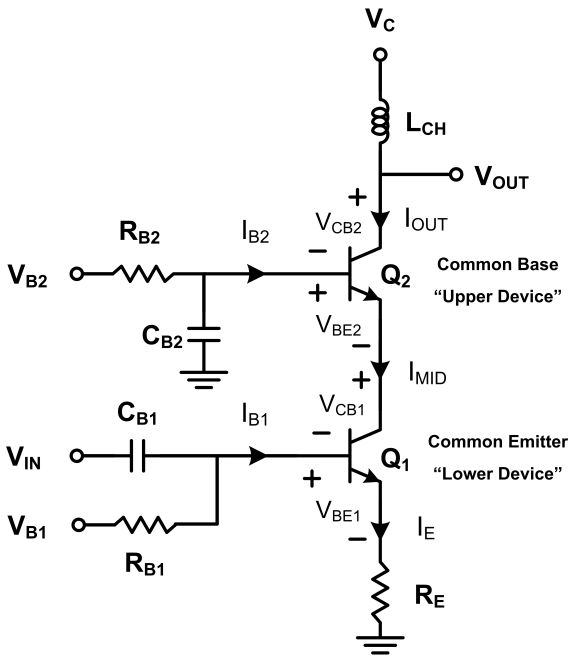

Figure 1.1: Schematic of an emitter-ballasted cascode HBT amplifier. © 2015 IEEE [2]

1.2 Hot-Carrier Effects

High electric fields in the collector-base (CB) region of a SiGe HBT caused by high CB voltage (V_{CB}) produce high-energy carriers. The changes to the overall transistor performance caused by these carriers are referred to as hot-carrier effects. For example, hot carriers are more capable of propagating to the emitter-base (EB) spacer as V_{CB} increases. The energy of the carrier upon reaching the oxide interface can break hydrogen bonds, forming interface traps. These traps contribute to a voltage-dependent parasitic base-leakage current, which increases with stress duration. Trap annealing simultaneously occurs at a rate dependent on temperature, and the operating conditions of the SiGe HBT determine the dominant mechanism.

For a single SiGe HBT in a common-emitter configuration, device lifetime can be calculated as the point where current gain is degraded by 10%. For the cascode configuration, device lifetime is unaffected by base leakage as it accrues only in the common-base (or upper) device for which the current is set by the common-emitter

(or lower) device. The lower device is shielded from hot-carrier-inducing high-V_{CB} swings by the shunt decoupling capacitance placed on the base of the upper device; although extremely high input voltage swings will in fact cause damage to the lower device [1, 14].

1.3 Avalanche-Induced Hard Breakdown

While the shunt capacitance placed at the base of the upper cascode device protects the lower transistor, series resistance at the upper device's base terminal limits the safe operating voltage for the CB junction of that device. Breakdown voltage decreases with increasing resistance at that terminal, ranging from the larger open-emitter breakdown voltage (BV_{CBO}) to the smaller open-base breakdown voltage (BV_{CEO}) as the series resistance is increased [16–19]. This upper limit deteriorates with increasing emitter current and temperature due to positive thermal feedback during avalanche [20–23]. This limit is often mitigated in designs through the incorporation of base and emitter ballast in the lower device [24]. The quantification of this limit as a function of base resistance has been termed BV_{CER} [25, 26].

The range of breakdown in relation to base resistance is a consequence of base current reversal (BCR) which occurs at voltages above BV_{CEO} [27–34]. As the name suggests, base current reverses direction in response to increased voltage due to avalanche-generated carriers, flowing toward the biasing voltage source. With increased impedance at the base node, majority carriers are directed to the emitter where gain of the device contributes further to the avalanche mechanism, causing breakdown to occur at a reduced voltage. In concert with non-zero intrinsic base resistance, this reversed current also creates a differential in electric field within the SiGe HBT, with voltage reaching a peak at the center of the emitter stripe. This differential causes current to pinch-in to the center of the transistor, and eventually avalanche multiplication leads to thermal runaway and the likelihood of catastrophic

junction damage. The point at which the derivative of current with respect to voltage tends to infinity is considered the flyback locus for a given base bias. Due to the thermal instability of these points in the I-V plane, the flyback loci delineate the worst-case *dc* SOA for SiGe HBTs. These points are quantifiable for a SiGe HBT cascode amplifier, as a function of thermal and resistive quantities [24]. For example, failure of the junction can be shifted to higher voltages by resistively ballasting the emitter-to-ground connection of a cascode amplifier. From the opposing viewpoint, failure is shifted to lower voltages by increasing positive feedback at the upper device emitter, from a maximum boundary of BV_{CBO} when no current is present.

1.4 Electromigration and Mutual Heating

The redistribution of metallic mass caused by high current density is referred to as electromigration. In integrated circuit interconnects, this redistribution aggregates in voids and hillocks, which eventually form unintended opens and shorts in a circuit design [35]. This eventuality can be quantified as a mean time-to-failure (MTTF), which is proportional to temperature and the square of current density, yet inversely proportional to cross-sectional area of the interconnect [7]. Aluminum interconnects have worse electromigration failure rates than copper, but are still employed in some first-generation technologies due to the reduced cost of aluminum [36]. As higher-frequency applications continue to drive the decrease in HBT emitter width and spacing, the available cross-sectional area for connecting to the transistor terminals decreases, and copper is used to add robustness [37].

In large arrays of transistors, mutual heating between transistors will lead to increased temperature and current density at the center of the array [38]. Although there are techniques for flattening the temperature differential, they are oftentimes impractical due to increased periphery and design complexity [39, 40]. Therefore, the central cells of the array will tend to fail sooner than the outer cells. Similarly, central

fingers of an HBT unit cell (a pair of collector connections on either side of multiple emitter stripes, each separated by base connections) will conduct more current than the outer fingers.

It should be noted that the central cells do not always dominate the current of the overall power core, due to process variation and the ongoing development of electromigration voids and hillocks. Current bifurcation has been shown to occur in multi-cell arrays, whereby one cell can dominate the overall current regardless of position [41]. Hence, the common mitigation technique for preventing current from becoming increasingly disproportionate due to electrothermal feedback is resistive ballasting [42]. For increased lifetime, cross-sectional area of interconnects should be maximized and current should be shared across an increased emitter area to reduce current density within the transistors.

1.5 SiGe BiCMOS on High-Resistivity Substrates

The addition of through-silicon via (TSV) and high-resistivity substrate are helping first-generation SiGe HBT technologies to find increased application from 1 to 10 GHz [36, 43, 44]. The high breakdown of these devices (approximately 7 V BV_{CEO} and 20 V BV_{CBO}) makes them useful in watt-level cellular handset applications. The inclusion of TSV improves gain by reducing emitter degeneration. High-resistivity substrates reduce losses in passives and CMOS switches, since increased frequency leads to additional substrate eddy currents [45,46]. This reduction in loss contributes improved efficiency to PA designs, which might be traded for additional functionality, such as tunable matching or core resizing [47, 48].

1.6 RF Voltage Stress in MOSFETs

With the availability of reduced-loss metal-oxide-semiconductor field-effect transistors (MOSFETs), the incorporation of FET switches in the RF path becomes a more

attractive idea to explore. Indeed, RF CMOS using silicon-on-insulator (SOI) technology is a major player in the RF switch market [49,50]. Similar to HBTs, FETs accrue gate-oxide traps, from hot-carrier injection, that increase threshold voltage over time. The *on*-state drain-source resistance also shifts over device lifetime. Damage to the oxide eventually leads to shorts between the gate and channel in the device, effectively breaking down the dielectric insulation and resulting in a catastrophic failure of the transistor [51–54]. This is in contrast to dieletric damage in HBTs, which only introduces parasitic leakage as opposed to an electrical short. To reduce the impact of breakdown phenomena, the electric field between the drain and gate must be minimized in FETs. In CMOS PAs and switches, MOSFETs are carefully stacked together to share the voltage burden for this reason [55–60].

1.7 Summary

For watt-level handset and radar applications, SiGe BiCMOS is an emerging solution due to an attractive cost-performance ratio. Since oxide damage in HBTs is non-catastrophic in nature, SiGe HBTs inherently hold an advantage over CMOS. Hence, understanding RF breakdown conditions for SiGe HBTs is crucial to evaluating the full potential of any BiCMOS technology. The challenge is identifying the onset of thermal runaway under a variety of RF operating conditions. Neither soft breakdown (performance shifts from hot-carrier damage) nor hard breakdown (catastrophic failure from thermal runaway) have been fully evaluated with respect to RF operation in the SiGe HBT literature. An improved understanding of large-signal SiGe HBT reliability holds promise, perhaps leading to techniques that can be applied during the circuit design process to improve performance without sacrificing operational lifetime.

CHAPTER 2

SIGE HBT DRIVER AMPLIFIER RELIABILITY

2.1 Introduction

This chapter reviews original research into the effects of large-signal voltage swings on SiGe HBT cascode amplifiers. This analysis resulted in two published works [1,2]. This work provides a perspective for relating RF to *dc* damage through the lens of the intrinsic transistor's forward transit current (referred to as the junction waveform) as opposed to the extrinsic transistor waveform, which includes capacitive currents. Capacitive currents are shown to have minimal effect on hot-carrier damage. The limitations of junction waveform analysis are also set forth.

2.2 Cascode Gummel Characteristics

To assess hot-carrier damage, code was developed to control three separate voltage supplies connected to V_{B1}, V_{B2}, and V_C (refer to Figure 2.1). Following a period of stress (either *dc* bias alone or under RF drive), the cascode Gummel (terminal currents measured across an increasing base-emitter bias voltage) was measured, and thereafter the stress conditions were reapplied. During Gummel measurements, V_C was set such that V_{CB2} remained constant at 1.0 V, while V_{B2} was set such that V_{CB1} would remain as close as possible to 1.0 V. A low V_{CB} is necessary to prevent additional hot-carrier damage during the Gummel measurement. (Low V_{CB} is particularly necessary in the case of fourth-generation 1.5 V BV_{CEO} SiGe HBTs where the order of bias application becomes of prime importance.) V_{B1} was increased in equal steps up to a maximum 1.0 V (or lower in cases where high-current annealing was considered a factor) to control the current through both devices, while V_{B2} and V_C were increased at twice the rate

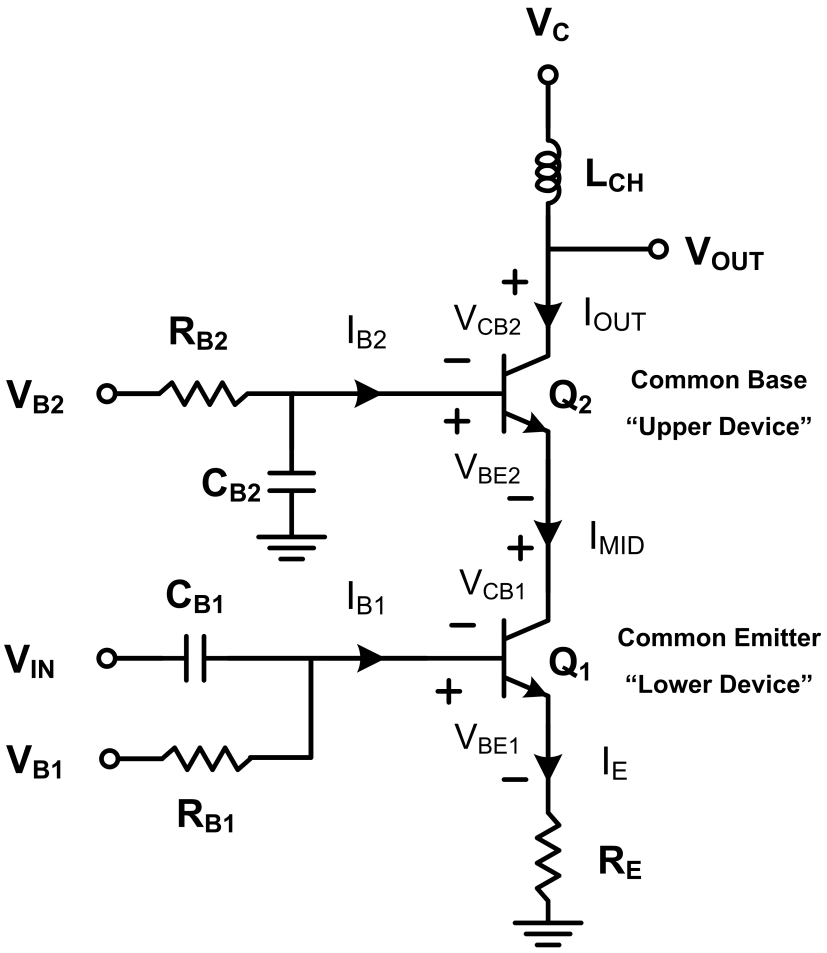

Figure 2.1: Schematic of an emitter-ballasted cascode HBT amplifier. © 2015 IEEE [2].

of V_{B1} to maintain equivalent voltage drops across like terminals in both devices.

This method of comparing currents is effective when the upper and lower devices have equivalent emitter area (as was the case for Figure 2.2). Although the precision of this measurement is complicated by emitter ballast and base currents, this measurement method nonetheless results in an adequate depiction of the upper device base currents, since ballasting effects are minimal at the low-current-density settings where damage-induced leakage is most evident.

The currents I_{B1} and I_{B2} will be equivalent across V_{BE} prior to stress (using the above method), which serves as indication that the device has not been stressed previously. Because of this equivalency, changes in I_{B2} can be set relative to initial I_{B1} values to account for percent damage caused by prior operation. This is particularly important when analyzing aggressively biased amplifiers, as the bias point and input drive contribute quickly to hot-carrier damage. For example, the leakage evident in Figure 2.2 is plotted in 30-second intervals of nominal RF continuous-wave operation.

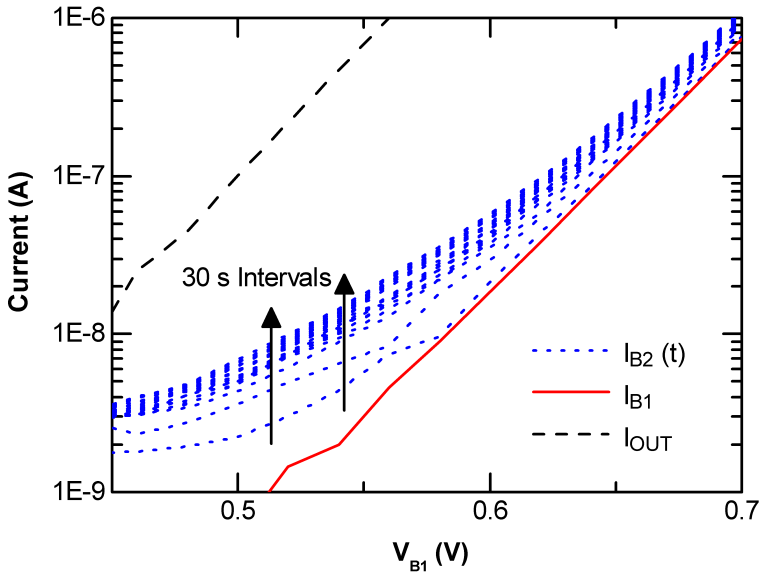

Figure 2.2: The upper device's base leakage as a function of RF stress duration. © 2015 IEEE [2].

2.3 Cascode Base Leakage

Hot-carrier reliability of two emitter-ballasted IBM 7HP SiGe HBT cascode driver amplifiers (X-band and C-band) was studied under normal operation. Due to the high voltage swing across V_{CB2}, hot-carrier damage, seen in the base current of the upper device, approaches a slope of twice the inverse thermal voltage on the order of minutes, as opposed to the hours necessary for more modestly biased amplifiers (refer to Figure 2.2). This observed damage is consistent with impact ionization induced trap generation at the EB spacer region. Figure 2.3 shows the voltage dependence of base leakage over RF stress time. Nominal operation of the driver amplifiers in this study increases damage, whereas the quiescent bias stress alone is shown to anneal traps once a certain density of traps is reached (in Figure 2.4).

As evident in data, two concurrent effects must be included to properly model base leakage in stressed SiGe HBTs: (1) thermally dependent annealing and (2) electrically dependent hot-carrier rates. The TCAD models used in this work do not include annealing effects as this is an ongoing area of research, so analyzing impact ionization is the focus of the following sections.

2.4 The Junction Waveform

In [1], the concept of revising the dynamic load line across a device to exclude capacitive currents internal to the transistor was first presented. What remains is the junction waveform, namely the voltage across and current through the depletion region existing at a particular junction (e.g., V_{CB2}). A visualization of the junction waveform being compared to the traditional transistor waveform (referenced henceforth as the extrinsic-transistor current) is presented in Figure 2.5. For the cascode driver amplifiers studied here, the CB junction current collapses to zero in the upper device, effectively protecting the amplifier from damage. Self-protection during saturated operation is discussed in [15], to which junction waveform analysis

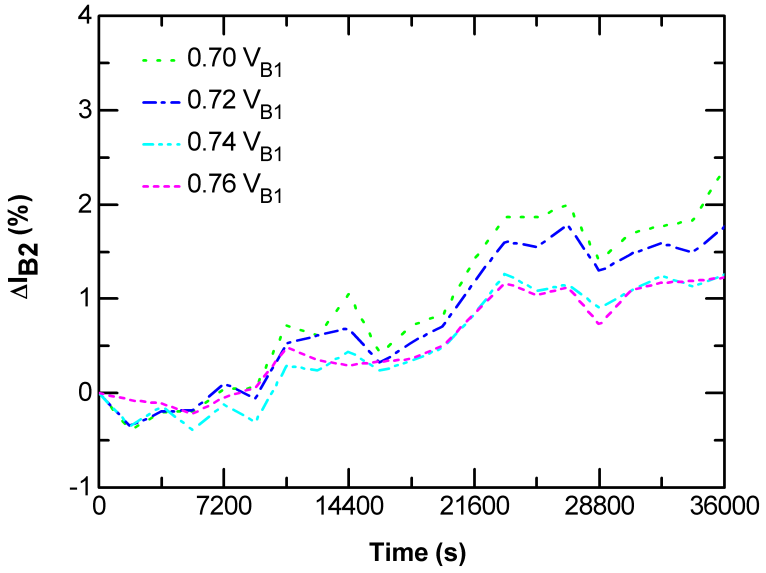

Figure 2.3: Example of accruing damage under nominal RF operation. © 2015 IEEE [2].

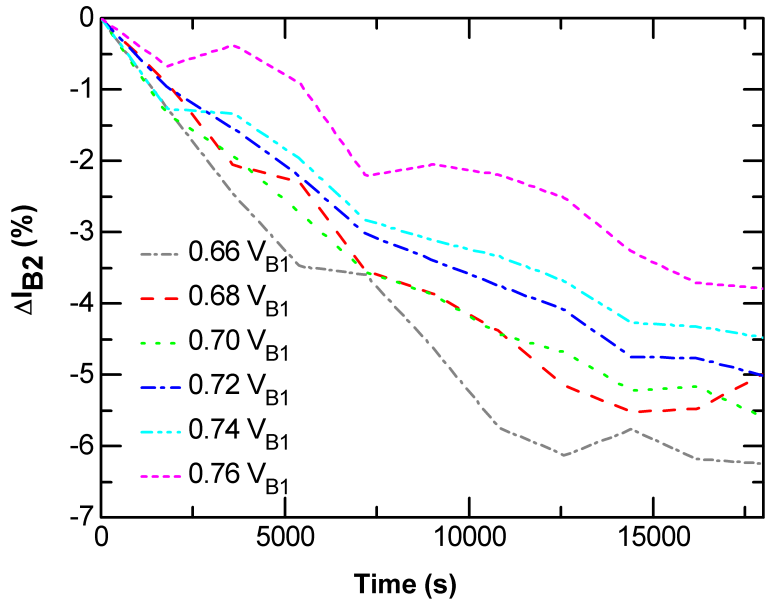

Figure 2.4: Example of annealing when RF is *off* and quiescent bias continues. © 2015 IEEE [2].

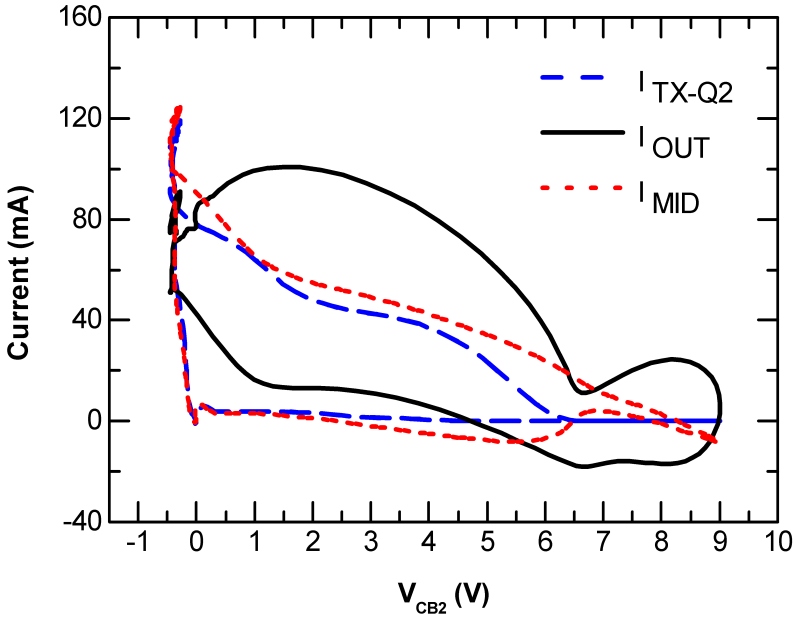

Figure 2.5: Collector, emitter and forward transit currents as a function of voltage over one period of RF operation. © 2015 IEEE [2].

adds support and perspective. It should be noted that the junction current calculation in this study ignores a portion of the current passing to the base under BCR, assuming it to be capacitive in nature. In practice this may not be the case if V_{CB2} is biased well above the reversal point, where swings are aggressively large.

A junction's time-dependent current can be directly calculated from simulated harmonic balance data using equations specific to the transistor model. This is achieved by saving intrinsic voltage nodes during simulation and then calculating current from appropriate equations available from the model, as intrinsic currents are not typically saved by a harmonic balance simulator. The simulated current I_{MID} closely approximates the upper CB junction waveform and can be used as a first-order design tool (shown in Figure 2.5). This current includes capacitive currents related to the upper EB junction (as does I_{B2}, which also includes CB-related depletion capacitance current) and therefore exaggerates the current. For a better approximation, these capacitive currents can be calculated and filtered out of the emitter current.

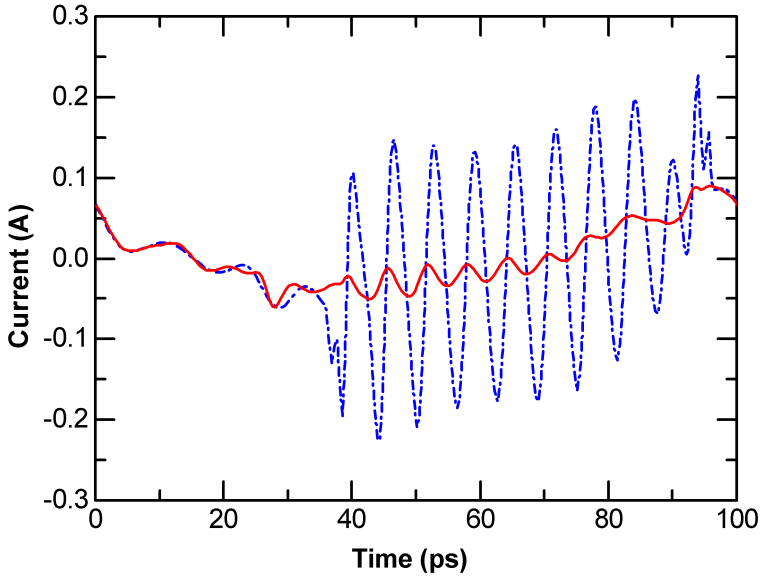

Figure 2.6: CB capacitance calculated by two methods to assess simulation precision. © 2015 IEEE [2].

To verify the precision of the simulations, the junction current should equal the value calculated by subtracting capacitive currents (primarily voltage-dependent CB depletion charge over time) from the extrinsic-transistor currents. For a designer working to simulate the junction waveform for the first time, this equivalence will bring to light large errors in the multitude of manually entered variables and equations used to derive the intrinsic-transistor currents.

An equivalent method of verifying simulation setup would be to graph the capacitive currents in two ways: (1) by calculating the derivative of intrinsic CB charge in Q_2, and (2) by comparing it to the current calculated by Kirchhoff's circuit law (KCL) at the intrinsic collector node. Figure 2.6 gives the results of such a comparison. The magnitude of this current is considerable, yet has negligible impact on hot-carrier damage, since it never crosses into the region where the overwhelming majority of hot carriers are created. Once setup is validated, differences in current in such a comparison will also show the designer if further harmonics are necessary in the simulation.

2.5 Differences in RF and *dc* Damage

This section describes the complications associated with correlating RF to *dc* hot-carrier damage. Visualized through TCAD cross-sections (Figure 2.7 and Figure 2.8) based on the I-V conditions set forth in Figure 2.9, differences in current density and impact ionization are clearly evident. Flyback loci for the single device output characteristics in Figure 2.9 are located at the ends of the curves, coincident with TCAD simulation conditions that produce non-convergence issues. Convergence at higher V_{BE} values is attributable to secondary flyback caused by R_E. For the cascode, flyback extends to breakdown, although mutual heating between the upper and lower device will shrink this *dc* SOA for the cascode [24]. Self-heating and mutual-heating effects are ignored in TCAD simulations shown here.

Inspecting the TCAD cross-sections under RF and *dc* for identical I-V conditions, *dc* simulations have significantly increased current and impact ionization over the RF

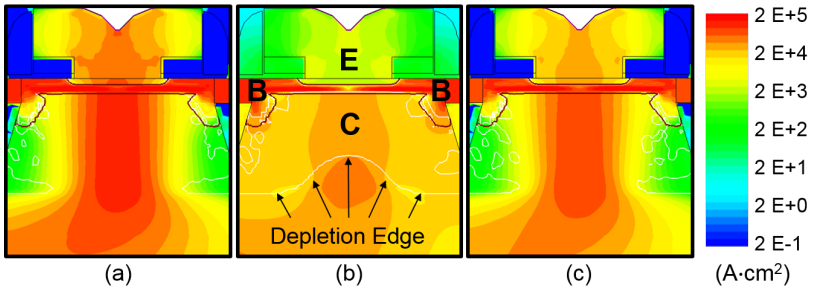

Figure 2.7: TCAD cross-sections showing RF and *dc* comparisons of total current in a SiGe HBT. © 2015 IEEE [2].

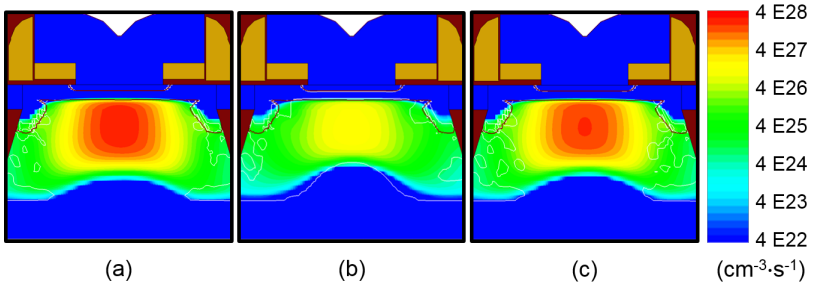

Figure 2.8: TCAD cross-sections showing RF and *dc* comparisons of impact ionization in a SiGe HBT. © 2015 IEEE [2].

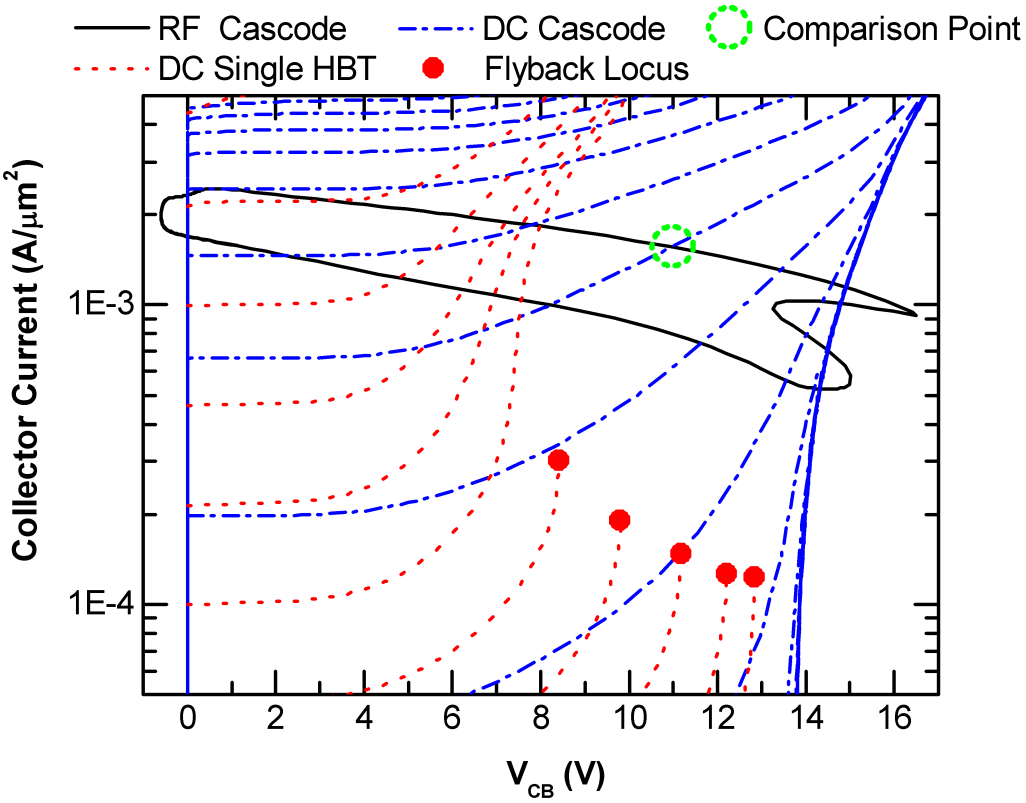

Figure 2.9: RF and *dc* output characteristics for SiGe HBTs in common emitter and cascode configurations. © 2015 IEEE [2].

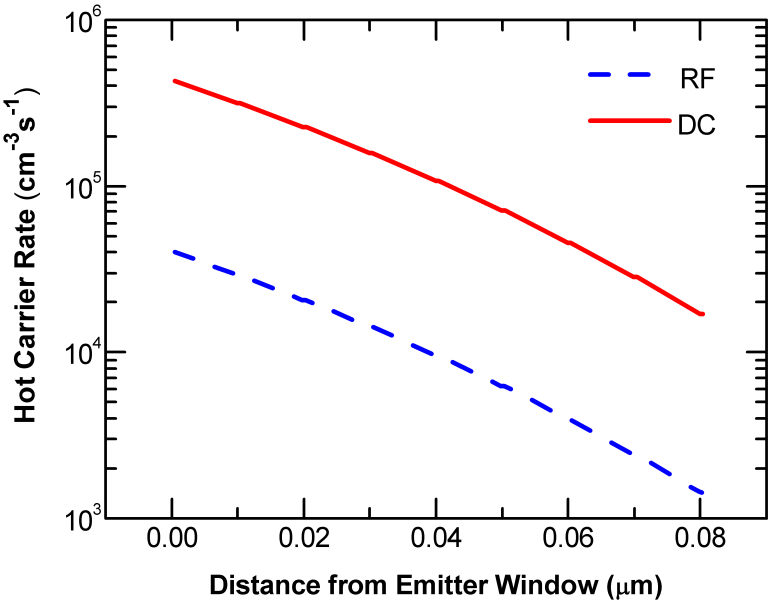

Figure 2.10: Comparison of RF and *dc* hot-carrier damage for a given point in the output plane. © 2015 IEEE [2].

simulation snapshots. This can be attributed to differences in V_{BE2} which is effectively cut in half under RF. Under *dc*, a specific V_{BE2} (set by V_{BE1}) is necessary for a given current (0.9 V and 0.875 V for the TCAD cross-sections shown). Under RF, the current follows the voltage waveform, thus by the time the current matches *dc*, V_{BE2} has dropped into cut-off at 0.4 V, choking off the positive feedback mechanism at the upper device emitter. With the time dependence of avalanche also playing part, this explains the reduced pinch-in seen under RF.

Hence, attempting to correlate RF damage from *dc* data along the extrinsic RF load line points would prove highly inaccurate. Indeed, since the waveform can travel beyond *dc* breakdown conditions, gathering such data would result in catastrophic failure of the SiGe HBT due to thermal runaway exacerbated by the pinch-in effect.

In Figure 2.7(a), the pinch-in under *dc* conditions is pronounced, while an RF snapshot in time at the same I-V point, in Figure 2.7(b), shows this centralization of current only reaching the collector-side edge of the space-charge region. This halting of current under RF is consistent with the intrinsic capacitive currents.

In [1], correlating *dc* damage to RF damage was performed, and found to be significantly complicated by annealing effects. In subsequent attempts to integrate *dc* data along the junction waveform, the data repeatedly overestimated the damage measured under the corresponding RF conditions. Of course, the temperature and interface-trap dependence of annealing behavior complicates this correlation, but TCAD simulations still show increased impact ionization and hot-carrier rates under *dc* conditions, even if the junction waveform is considered as the reference. Numerically, *dc* hot-carrier damage at the EB spacer outpaces the RF damage by an order of magnitude at the same bias point (Figure 2.10).

In Figure 2.12, trends in leakage current created by cycled *dc* stress along the junction waveform (at the points indicated in Fig 2.11) are shown to be a balance of annealing and damaging behavior. The mutually positive points in Figure 2.11 (current and voltage both greater than zero), account for a small portion of the waveform period, as can be gleaned from Figure 2.13, which plots both as a function of time.

In summation of these findings, acquiring RF hot-carrier damage rates from *dc* data will overestimate damage, and hence RF damage should be investigated through direct experiment. This data can then be used to calibrate TCAD simulations.

2.6 Avalanche Breakdown Under RF

Driver amplifiers are driven deeply into saturation, resulting in significant harmonic content, as well as periods where the transistor junctions are non-conductive. The natural question that follows concerning the time dependence of avalanche in SiGe is somewhat hidden in this study, as any increasing effect of avalanche over RF stress is quelled by the fact that the CB junction of Q_2 is effectively off for a majority of the time (Figure 2.13), acting primarily as a voltage-dependent capacitor. In saturated operation, breakdown is primarily dependent on reverse current induced by the high

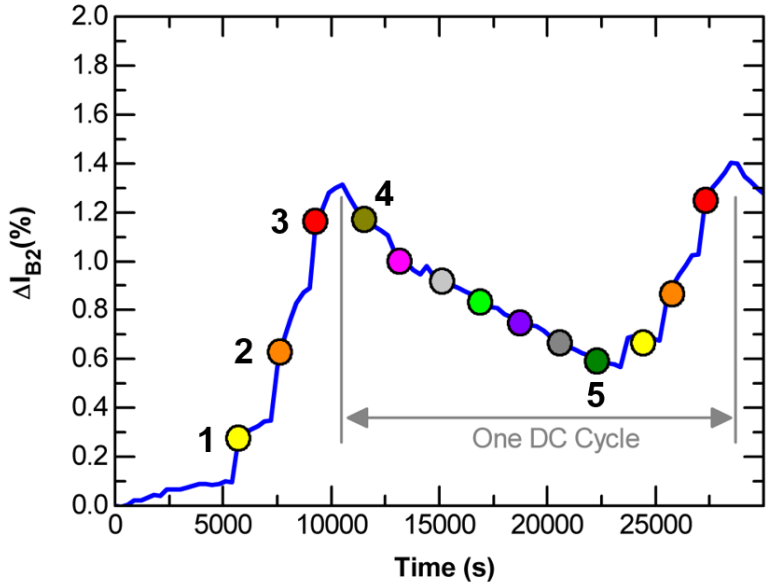

Figure 2.11: Shift in base leakage during *dc* cycled stress. © 2015 IEEE [2].

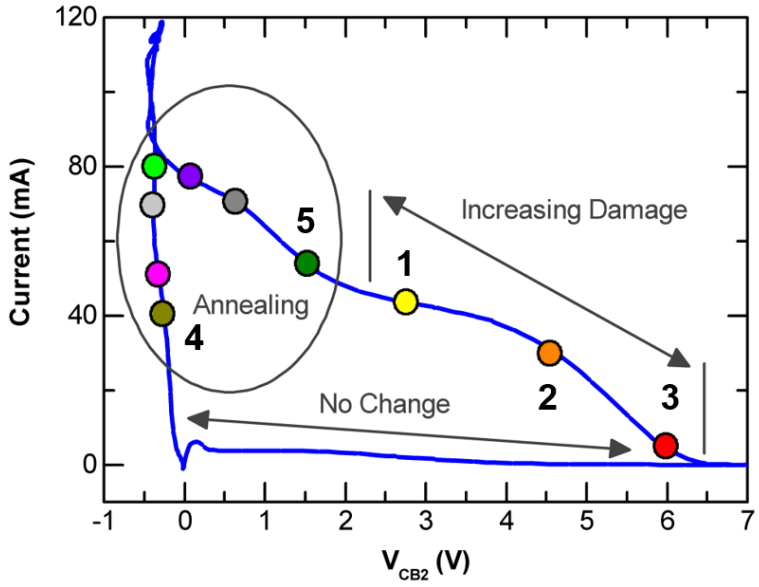

Figure 2.12: Points chosen for *dc* cycled stress. © 2015 IEEE [2].

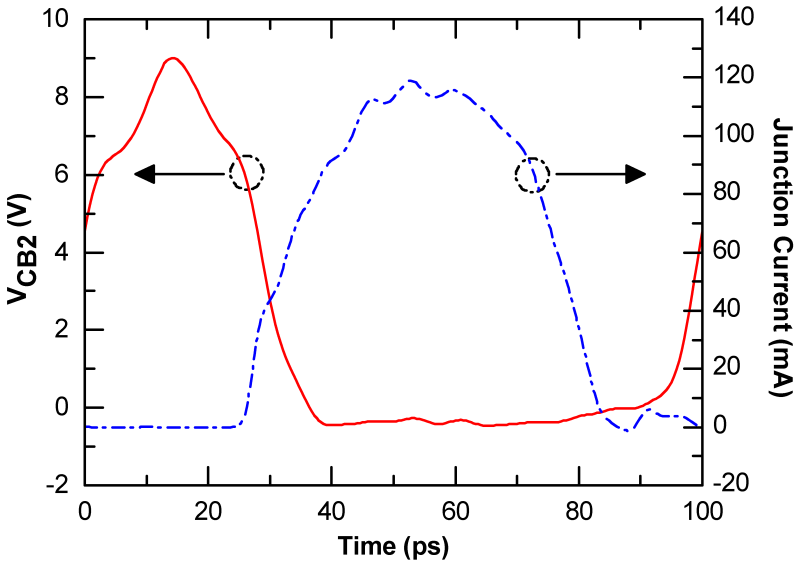

Figure 2.13: Junction current and voltage waveforms as a function of time. © 2015 IEEE [2].

field, hence RF stressing the CB junction leads to a good understanding of SiGe HBT cascode driver reliability.

As an example of how to experimentally determine the RF safe operating area (SOA) of a real driver amplifier design, fourth-generation IBM SiGe HBTs were CB-junction stressed with 1.0 V amplitude signals at 10 GHz. The base was well-grounded with respect to RF, and the waveform was applied to the collector. This was done to isolate the effects of emitter current on the CB voltage swing maximum. Fixed-bias *dc* breakdown for these devices occurred nominally at 5.4 V, while the full RF signal could swing to 6.1 V (centered at 5.1 V) before catastrophic failure resulted from 0.1 V steps. Base leakage under high-voltage capacitive swings might also be correlated from this methodology. By increasing the voltage amplitude and shifting the bias point, the time dependence of this phenomenon can be explored experimentally for a given frequency.

2.7 Summary

In this work, the complications of correlating RF and *dc* hot-carrier damage are investigated. TCAD simulations show that RF damage cannot be calculated from *dc* points along the RF load line, as this will overestimate damage. Furthermore, the temperature dependence of trap annealing also complicates this correlation, as the currents within the transistor are distributed differently, which also influences pinch-in phenomena. Therefore, to accurately model hot-carrier effects in SiGe HBT cascode amplifiers, fully calibrated TCAD models are necessary.

Nonetheless, a worst-case ceiling for base leakage can be taken from *dc* cycled stress along a revised load line consisting of the intrinsic-transistor CB-junction current. More importantly, this junction waveform can be used to analyze SOA with respect to catastrophic breakdown. Since hot-carrier damage does not lead to failure of a SiGe HBT cascode, as shown herein and throughout the literature, preventing catastrophic failure is the major design consideration for these structures.

A SiGe HBT can be swung above BV_{CBO}. If the junction is off (zero emitter current), as in the case of highly compressed driver amplifiers, the extent of this swing can be derived from capacitive swing measurements on single devices or from convergence issues seen in TCAD simulations. As a guideline, purely capacitive swing above breakdown may extend anywhere from 10% to 20%, dependent on upper-base resistance and ballast.

CHAPTER 3

RELIABILITY ANALYSIS OF SIGE HBT AMPLIFIERS UNDER LARGE VOLTAGE SWINGS

This work analyzes the effects of large voltage swings on a third-generation silicon-germanium heterojunction bipolar transistor (SiGe HBT) as part of a cascode amplifier. Output swing beyond *dc* hard breakdown and input swing well beyond the input-referred 1 dB compression point are evaluated in device simulation and measurement. To better understand power amplifier maximum output swing (as limited by hard breakdown), transistor lattice temperature is evaluated using calibrated device models with particular focus on the electrothermal impact of an aggressively biased collector-base junction. In an examination of soft breakdown in low-noise amplifiers, the impact of interface trap creation caused by large input signals is shown to effect noise figure and gain. With this work, practitioners in SiGe HBT amplifier design will gain insight into the onset of damage under various bias conditions and input power levels, resulting in improved trade-off between performance and reliability.

3.1 Introduction

Performance of silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) circuits is limited by junction breakdown mechanisms. To provide reliability guidelines, output voltage limits are based upon two *dc* measurements, the open-base and open-emitter breakdown voltages, BV_{CEO} and BV_{CBO}. BV_{CEO} marks the onset of base current reversal (BCR) during forward active operation, after which higher collector-base (CB) potentials avalanche-multiply majority carriers in the base [18]. These

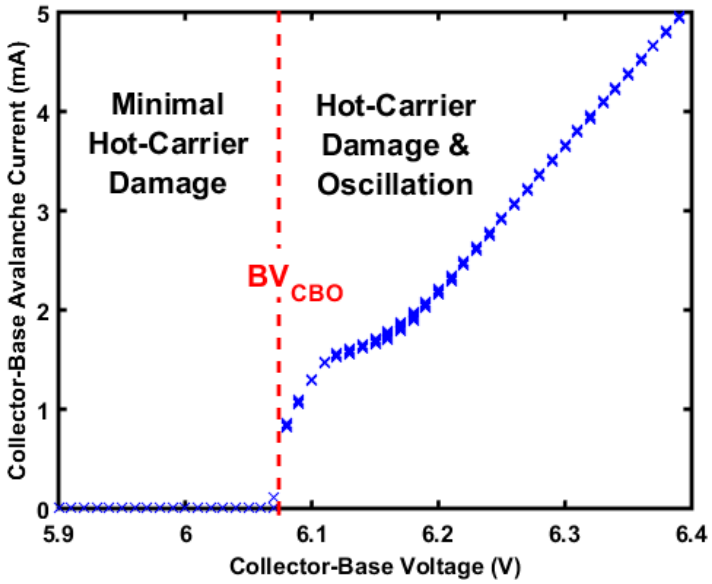

Figure 3.1: Current vs. collector-base voltage with an open emitter, with BV_{CBO} indicated. Above breakdown the device current sharply increases.

carriers either find a low impedance path out of the extrinsic base terminal (producing the reversed current), or proceed to the emitter if base impedance is restrictively high. If directed to the emitter-base (EB) junction, carriers are multiplied by the current gain of the SiGe HBT such that a large number of minority carriers are injected back into the base, to be swept across the CB junction, thus exacerbating avalanche. This positive feedback mechanism contributes toward thermal runaway which can result in irreparable device damage from the influence of excessive heat on the silicon lattice. Because of the dependency on base impedance, a breakdown voltage relative to base resistance (BV_{CER}) is sometimes quantified, ranging between BV_{CEO} and BV_{CBO} [26].

Unfortunately, any *dc* limit provided to the circuit designer will be overly constricting in an application preferring maximized voltage swing, as in a wireless power amplifier (PA), as lattice temperatures will differ from large-signal *ac* operation. Furthermore, *dc* values for breakdown are sometimes quantified at the point of inflection in the current, rather than the voltage at which catastrophic failure occurs. For example, breakdown voltage values for the GlobalFoundries 8HP SiGe HBTs used

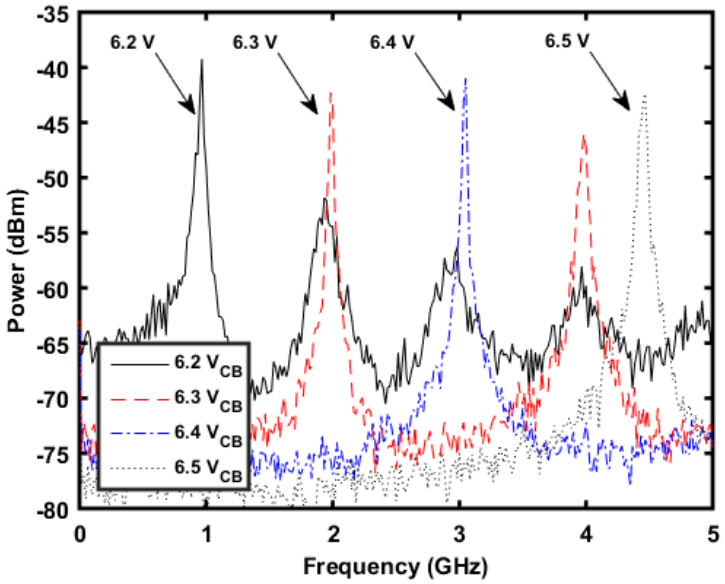

Figure 3.2: Oscillations seen in a cascode SiGe HBT test structure when biased above BV_{CBO}.

in this work are quantified by the foundry at a given current, above which current rapidly increases with CB voltage, as in Figure 3.1.

Hence, the term 'breakdown voltage' can be misleading from an *ac* perspective, especially since performance drift, or soft breakdown, is related to hot-carrier effects, while catastrophic failure, or hard breakdown, is dependent on the onset of thermal runaway [2]. Indeed, large-signal swings 10-20% beyond breakdown have been shown to be possible on the output side of a cascode pair [1, 2, 12]. Although the device can survive *dc* bias well beyond BV_{CBO}, the stability of the device is quite volatile. Spikes in current during bias adjustment, caused by increasing the voltage in too large of a step, led to immediate destruction of the SiGe HBTs in this work. In some cases, oscillations are evident, as shown in Figure 3.2, during a BV_{CBO} extrapolation using the common-base device in a cascode structure (V_{CB2} in Figure 3.3, with both base-emitter junctions *off* via reverse biasing).

For input-side power handling, the EB junction is of greater concern. Excessive negative voltage swing, as might be applied to the base of a low noise amplifier (LNA)

by a nearby PA, accelerates hot-carrier damage in the EB spacer oxide resulting in a parasitic leakage current evident in the base [61–65]. This current can affect biasing, and therefore scattering (S-) parameters are known to shift [66]. Furthermore, large input swings on the LNAs in this study will be shown to degrade noise figure (NF). The EB junction enters breakdown at a lower voltage than the CB junction due to higher donor doping concentration [67], although failure requires greater over-voltage in comparison with the CB junction. In a high-gain PA with an aggressive collector bias, the CB junction will likely fail first [12]. In an LNA, the CB junction voltage is limited by high current effects acting on a small device periphery, which saturate the output current and limit output voltage swing, as described in [15] as RF stress quenching. Hence, device damage and performance drift in cascode SiGe LNAs as observed in [14, 68] are primarily attributable to EB stress as outlined in [15], since output swings have minimal effect on cascode amplifier performance [1, 2].

The advantages of quantifying *ac* limitations of SiGe HBTs are related to both performance and reliability. Higher voltage swings allow for reduced current in achieving the same target output power, and thus have the added benefits of increased efficiency and output impedance [69]. Increased output impedance contributes to more efficient output matching networks due to reduced impedance transformation ratios [70]. Hence, understanding the impact of swinging above breakdown is important to the SiGe HBT circuit design process, especially for PA applications. For LNA design, increased voltage headroom equates to improved dynamic range as collector voltage increases to extend P1dB [70].

Thus far in the literature, the negative impact of pursuing more aggressive bias schemes has not been fully addressed. The long term reliability of SiGe BiCMOS processes is primarily restricted by electromigration in the back-end-of-line (BEOL) metal layers closest to the device [7, 35], since short-term stress has minimal effect on performance [1, 2]. This is oftentimes outside the scope of scholarly investigations

which observe short-term breakdown effects. Additionally, BEOL temperature and device self-heating may be difficult to incorporate into the design process due to the added complexity of mutual heating between devices in the amplifier core [4, 24]. To fill this void, the present work presents thermally calibrated device simulations. The objective of this work is to provide the designer with a full introduction to the complexities of SiGe design-for-reliability such that the performance-reliability trade-off can be optimized. The next paragraphs continue this introduction in a broad sense.

3.1.1 PA Breakdown

When designing wireless PAs that venture above BV_{CEO} there are two major issues to understand: junction breakdown and hot-carrier effects. Whenever possible, the design should provide a low resistance path at the base to stave off the onset of junction breakdown [26]. In a single-transistor common-emitter design, this low resistance path may, in practice, oppose resistive biasing and ballast requirements [71,72], hence, many designs will closely adhere to the BV_{CEO} guideline to compensate. Above BV_{CEO}, BCR also has some influence on non-linearity for swings that cross BV_{CEO}. Additionally, larger voltages increase impact ionization in the CB junction, which can damage the oxide used to shape the emitter window in a vertically integrated SiGe HBT. This damage leads to a parasitic base-leakage current, effectively lowering the current gain of the device over time. In some applications, this might be thwarted over the design lifetime with bias adjustments, without which the design performance may eventually drift beyond acceptable limits [14, 68]. This soft breakdown effect, in concert with electromigration in the metal interconnects which is also exacerbated by increased CB voltage, sets the lifetime of a SiGe HBT circuit design [7, 35].

As higher frequency applications continue to emerge for SiGe HBTs, cascode amplifiers are increasingly necessary to improve voltage handling. Fortunately, an

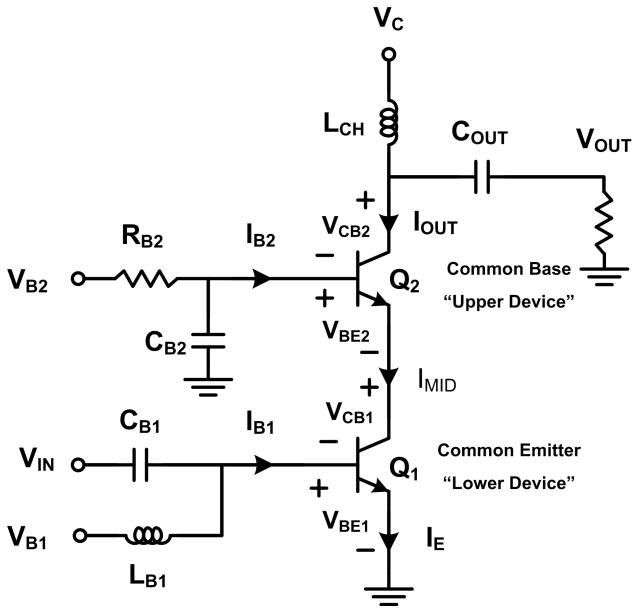

Figure 3.3: Cascode schematic used to describe circuit voltages and currents.

additional benefit of the cascode is protection from soft breakdown, as hot-carrier damage has limited impact in the common-emitter, or lower, device, since high fields are handled solely by the common-base, or upper, device [2]. This protection assumes modest input voltage and sufficient shunt capacitance on a low-resistance upper-base terminal. Under these circumstances, concern shifts to the onset of hard breakdown (the conditions under which catastrophic failure of the device occurs) with a focus on V_{CB2} as the limiting quantity, with increasing R_{B2} shrinking this limit further (see Figure 3.3). Under large-signal *ac* operation, it has been shown experimentally that V_{CB2} can safely swing above BV_{CBO} (by about 10% if swinging down to the knee voltage) when R_{B2} is kept low (on the order of 10 Ω) [1, 2, 11, 12].

3.1.2 LNA Breakdown

As input voltage swing increases on a SiGe HBT LNA, the cascode output swing is limited by high injection effects. Hence, the one-decibel compression point (P1dB) of the design limits the voltage swing on the CB junction, rendering it very difficult to create hard failures in SiGe HBT LNAs on the output side. Experimentally, the

present work will show that driving an X-band and a K_u-band LNA with 29 dBm is possible without causing hard breakdown. However, soft breakdown is accelerated for large input swings on the lower base due to stress caused by the negative BE potentials applied by the input drive.

Soft breakdown in SiGe HBTs implies the onset of a parasitic base-leakage current. For large output swings in cascode power amplifiers, this leakage can be limited to the upper device by limiting the input drive. In contrast, if input drive increases, the lower device will exhibit leakage. Since the emitter-base breakdown BV_{EBO} is smaller than BV_{CBO} due to doping differences [67], this occurs at a lower voltage than on the collector. Furthermore, hot carriers are created closer to the regions that can become damaged, therefore effects occur more rapidly. This increased current leads to increased noise figure (NF) and can result in deflated gain (which correlates to the NF shift) if the leakage current affects the input match, as will be shown in this work. As transistors get faster, breakdown voltage inherently decreases via the Johnson limit. Hence, understanding how the devices in cascode designs react to aggressive voltage swings beyond breakdown is an important step toward realizing the full potential of SiGe HBTs as the technology scales.

3.2 TCAD Simulations

Two-dimensional TCAD models of BiCMOS 8HP were calibrated from HBT measurement data to enable comparison with actual hardware. Models were updated with thermal boundary conditions consistent with parameter values accessible in the design kit (Figure 3.4). The detailed intricacies of the thermal boundary conditions are not precisely shown, for proprietary reasons, but parabolic spread is assumed at the substrate connection to help account for thermal discrepancies between the simplified two-dimensional simulations used and known three-dimensional effects. Device temperature will aggregate further to the center of the device when the third

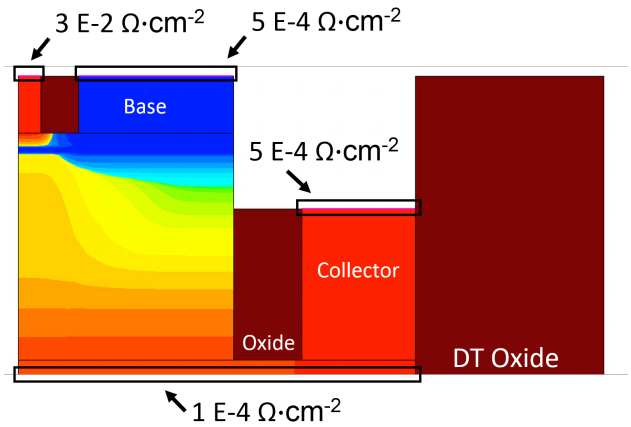

Figure 3.4: A one-half TCAD cross-section with approximate thermal surface resistance for the four-terminal device. The location of the surface used for the substrate connection (at bottom) begins below the deep trench and not in the location shown.

dimension is added to the model, hence the data shown underestimates the impact of electrothermal interaction, particularly pinch-in. Avalanche multiplication (M-1) was calibrated from measured data to capture the impact of large CB potentials. Doping-dependent thermal properties were also included in the model.

Previous work on cascode amplifiers in the same technology recommended limiting collector-base maximum voltage to 10% above BV_{CBO} [5]. This is consistent with a 20% maximum voltage above BV_{CBO} if typical values for breakdown are assumed, as opposed to minimum values resulting from process variation. Hence, for a TCAD model set up for typical GlobalFoundries BiCMOS 8HP SiGe high-performance HBT process values, it can be hypothesized that 20% above breakdown is the predictive RF breakdown level for Class A operation utilizing the full linear range of the device (i.e, the low end of the swing hits the knee voltage) [69]. Non-optimal load lines could result in a decrease in the 20% approximation due to increased average CB voltage and therefore increased temperature.

A 10 GHz continuous-wave transient simulation was performed in Synopsys TCAD

under 11 mA quiescent bias conditions, with a V_{CB2} of 2.2 V. The upper-base resistance was kept at 10 Ω. The device size was scaled from one 0.12 μm by 10 μm single-stripe CBEBC-layout unit cell. Half-device structures of 1 μm were modeled in two-dimensional TCAD to reduce simulation time, and the currents were scaled by 20 to match overall current to the measured device data.

The first TCAD experiment looked at internal device temperature of the upper device in the cascode structure. A large 0.4 V amplitude signal was applied to an unmatched cascode structure, as in Figure 3.3, to force the output swing to approach BV_{CBO}. Inductors were 10 nH and all capacitances were 20 pF. A decoupled load resistance was attached and set to 100 Ω to maximize the output swing. The maximum internal temperature for various collector-base voltage settings is given in Figure 3.5. As the maximum internal temperature is rising, there is some concern that thermal boundary conditions are too harsh in the setup. Furthermore, the simulations showed no thermal coupling to the lower device. Hence, a second setup was pursued including both devices in the same model, instead of each device being simulated separately in the cascode. With this revision, which took significantly longer to simulate, thermal coupling was determined to be minimal above 30 μm separation, which is a reasonable design metric, so the original simulations were deemed sufficient.

Nonetheless, the 10-year lifetime temperature for the metals in this process limits the maximum collector-base voltage that can be reliably employed. With the results of Figure 3.5, a 3 V maximum is suggested. Although a short-term measurement for soft and hard breakdown would lend itself to a conclusion that it would be safe to increase V_{CB2} further, this would not capture the full impact of aggressive bias. In the hundreds of 8HP devices and circuits stressed in this work, catastrophic failure points varied, as electrothermal instability during RF operation might occur at any point above 50% of BV_{CBO} for a given circuit. This is primarily evident in PAs or cascode cores where a shift in bias left the device conducting for the majority of the

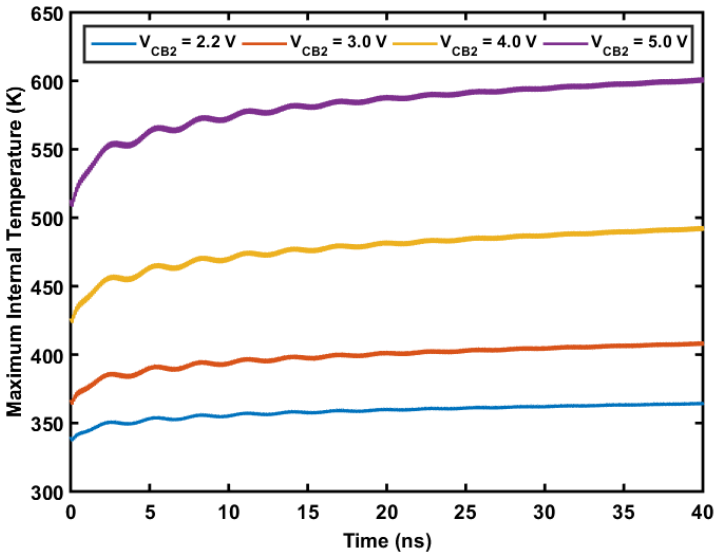

Figure 3.5: Maximum device temperature vs. time for the first 400 periods of a 10 GHz, 0.4 V amplitude input signal, across various collector-base voltages, indicating the danger of aggressive bias.

period, and therefore is not of immediate concern. However, to observe the electrical conditions that produce this effect, an LNA design with a high base resistance was evaluated.

As example, a 2.4 GHz cascode LNA was *dc* stressed to 3 V V_{CB2} with a 2.5 V V_{B2}. Over time, even small amounts of *dc* stress led to thermal runaway and amplifier failure. This phenomenon would first appear to conflict with previous data, but is attributable to two elements: the upper-base bias, 2.5 V V_{CB2}, and the high impedance bias network driving the lower base voltage V_{BE1} (refer to Figure 3.6). Because the upper-base voltage is high, the lower device is biased very close to BV_{CEO}. Avalanching current in the upper device is forced out of the upper device's base terminal, and the reversed current further increases the collector bias of the lower device, since the upper-base bias point adjusts with resistive effects and the direction of the current. With a base resistance above 1 kΩ for the lower device in the cascode, going beyond 1.5 V (worst-case BV_{CEO}) on V_{CB1} leads to thermal runaway in the lower device. Hence, it would be expected that this circuit would fail from an RF

stress level that is lower than that of a similar amplifier that had a reduced bias point and low-impedance bias network. A comparison with such an amplifier is documented in the next section.

3.3 Comparing LNA Breakdown Points

This section looks at three separate cascode LNA circuits in BiCMOS 8HP: (1) a 2.4 GHz LNA with a high impedance bias network on the lower base, (2) a 0.3-15 GHz resistive LNA with high gain [73], and (3) a 15 GHz LNA with a broadband match. The latter two LNAs use a relatively low-voltage upper-device bias and lower-resistance upper-device base resistance in comparison to the 2.4 GHz LNA, which improves their overall power handling, as tabulated in Table 3.1. The lower input power handling for the 2.4 GHz LNA supports the analysis presented in the previous section.

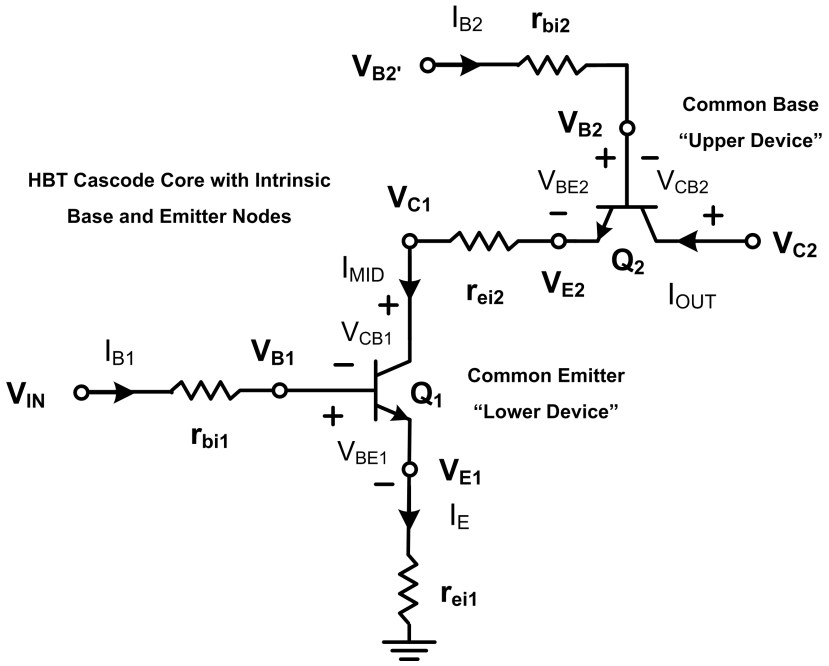

Figure 3.6: Cascode SiGe HBTs with crucial voltages labeled, and including intrinsic resistances.

Table 3.1: Hard failure input power levels for three third-generation SiGe HBT Cascode LNAs.

LNA	Frequency (GHz)	Safe Power (dBm)	Destructive Power (dBm)
2.4 GHz Narrowband	2.4	11	12.5
0.3-15 GHz Resistive	10	29	30
15 GHz Wideband	14.9	32	>32

Table 3.2: NF for three third-generation SiGe HBT Cascode LNAs.

LNA	Frequency (GHz)	NF (dB)
2.4 GHz Narrowband	2.4	2.0
0.3-15 GHz Resistive	10	1.8
15 GHz Wideband	14.9	1.7

Over increasing input stress, these LNAs drift in NF performance from the measured NF in Table 3.2 taken before RF stress is initiated. This degradation is coincident with soft breakdown of the lower device. The damage to the 2.4 GHz narrowband LNA, the 0.3-15 GHz Resistive LNA and the 15 GHz Wideband LNA are displayed in Table 3.3, Table 3.4 and Table 3.5, respectively.

Since the creation of interface traps introduce additional recombination current, the current flowing through the emitter is actually larger as traps form in the polysilicon interface with the intrinsic emitter. This leads to increased shot noise across the base-emitter junction, and therefore more noise. The EB-spacer oxide contributes $1/f$ noise, which should not effect the overall NF at high frequency, hence the NF increase must be attributable to either shifts in the bias point, or increased shot noise from the lower device in the cascode. The increase in current over RF stress is shown in Figure 3.7. The sharp increase in lower base current for the 15 GHz wideband LNA is coincident with a rise in noise figure in that LNA as well as the 0.3-15 GHz resistive

Table 3.3: The 2.4 GHz narrowband LNA's NF response to stress from a 2.4 GHz continuous-wave input power sweep, extending to hard failure.

Step Number	Input Power (dBm)	Duration (min)	NF (dB)
0	-	-	1.96
1	0	10	1.96
2	5	20	1.97
3	7.5	20	2.01
4	10	900	2.04
5	12.5	20	2.20
6	12.5	2700	(failure)

Table 3.4: The 0.3-15 GHz Resistive LNA's NF response to stress from a 10 GHz continuous-wave input power sweep, extending to 20 dBm.

Step Number	Input Power (dBm)	Duration (min)	NF (dB)
0	-	-	1.83
1	0	20	1.82
2	10	20	1.87
3	12	20	1.87
4	14	20	1.91
5	16	1200	1.91
6	18	20	1.91
7	19	20	2.05
8	20	20	2.12
9	22	20	2.19

LNA. This leakage current develops rapidly as the LNA approaches the stress levels seen in Table 3.5, as illustrated in Figure 3.8. Additionally, there is decay in gain (Figure 3.9). This can also be seen in TCAD simulations with a fixed base current (Figure 3.10).

Table 3.5: The 15 GHz wideband LNA's NF response to stress from a short-term and long-term 26 dBm 14.9 GHz continuous-wave input power stress.

Device	Input Power (dBm)	Duration (min)	NF (dB)	Gain (dB)
Unstressed	-	-	1.72	21.8
DUT1	26	5	1.91	19.6
DUT2	26	10,000 (1 week)	2.16	19.24

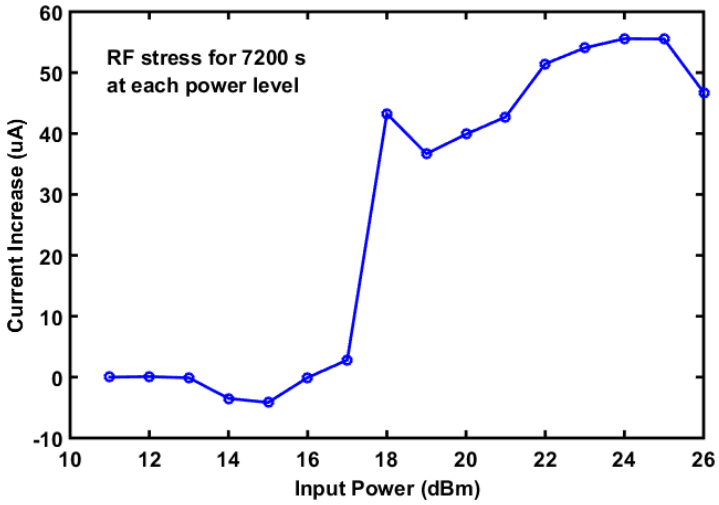

Figure 3.7: Leakage current in the 15 GHz wideband LNA as a function of 7200 s RF input stress.

3.4 Conclusions

This work gives guidance for the implementation of aggressively biased cascode amplifier structures (both PA and LNA), suggesting that the bias point should be limited to 50% of BV_{CBO} for the upper device's base terminal. The voltage itself should not force the lower device to have a voltage above BV_{CEO} if a high-impedance bias network is implemented. In this study high-impedance was measured to be above 500 Ω for either base terminal in the cascode structure, but smaller resistances should be implemented whenever possible, preferably on the order of 10 Ω. Furthermore, LNAs with low-impedance bias networks enjoy greater ruggedness to input power.

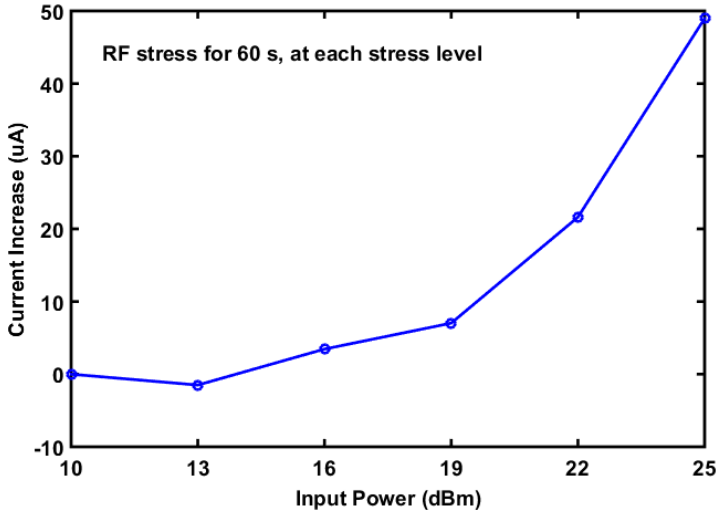

Figure 3.8: Leakage current in the 15 GHz wideband LNA as a function of 60 s RF input stress.

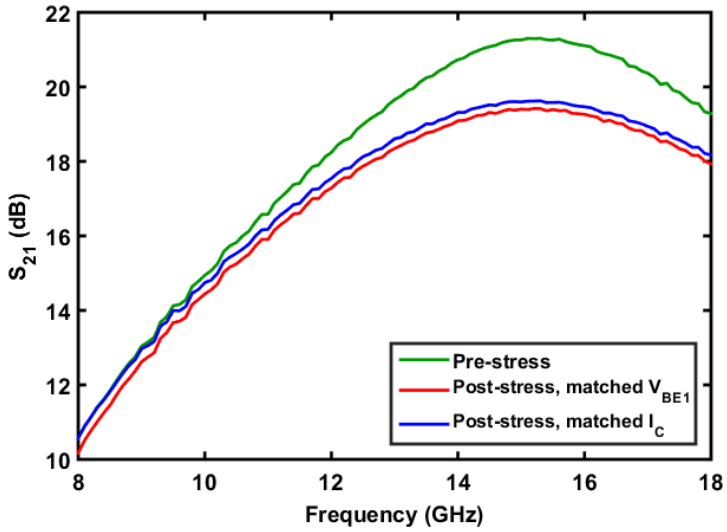

Figure 3.9: Measured gain degradation in the 15 GHz wideband LNA after high RF input stress.

Two examples are described in the present work that could endure 29 dBm RF stress without hard failure, although electromigration was not evaluated. There is a penalty to noise performance that begins to accrue at 13 dBm for these amplifiers, and accrues more quickly above 18 dBm. As a reference for the designer, this onset is coincident with negative swings near BV_{EBO}, although, in practice, simulations will likely not

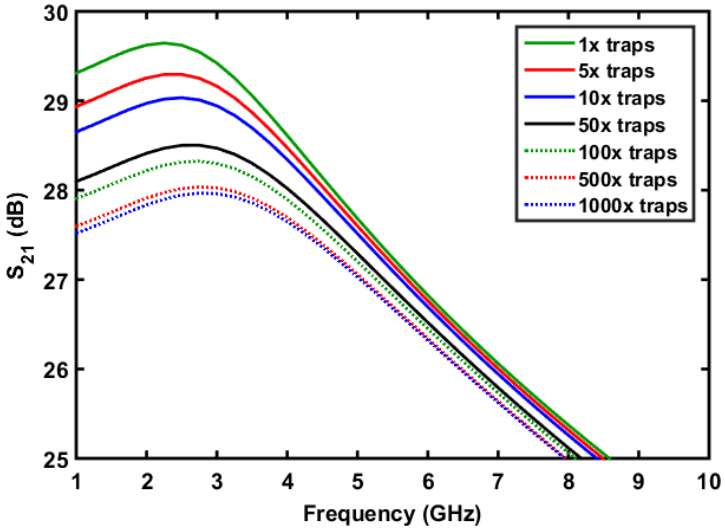

Figure 3.10: Gain degradation correlation in TCAD with increasing trap density.

converge to allow for an exact analysis. This work suggests RF swings up to worst-case BV_{EBO} can be assumed for calculations concerning input ruggedness of LNAs. This is supported by BV_{CBO} measurements, which show damage up to the inflection in avalanching current.

Over time, performance will drift as the input match degrades from shifts in the bias point, and possibly the introduction of traps in the emitter and the nearby oxides. This change degrades gain and noise figure over time. For a high-impedance bias network, failure occurs at much lower input power, 12.5 dB in the example given in this work, and damage is evident at lower power levels, as well.

For a typical design with low-impedance bias networks, measurements presented in this work suggest that 8HP SiGe HBT LNAs will suffer 0.2-0.4 dB NF degradation and 2 dB gain degradation at high levels of input stress. Hence, 8HP SiGe LNAs can handle about 20 dB above input P1dB before NF is degraded.

CHAPTER 4

TCAD WAVEFORM ANALYSIS FOR SIGE HBTS

This work presents the impact of large voltage swings on a first-generation silicon-germanium heterojunction bipolar transistor (SiGe HBT) as part of a cascode amplifier. By providing simulated device cross-sections taken at equal intervals during one period of 10 GHz continuous-wave operation, an understanding of the complexity of design-for-reliability with SiGe HBTs is outlined. To quantify the onset of hard breakdown, or catastrophic failure, under large-signal operation, the product of electric field and current density is computed along a center cut-line of the simulated device. Taken at evenly spaced intervals, and in sufficient quantity, the average *ac* power density is compared to *dc* power density at a known catastrophic collector-base junction breakdown voltage, as indicated by fly-back. In so doing, previous studies, which have indicated a 10-20% voltage swing allowance above *dc* breakdown, are supported. This analysis method can be applied to any SiGe HBT circuit regardless of generation to determine the onset of hard breakdown under all forms of radio frequency operation.

As transistors get faster, breakdown voltage inherently decreases via the Johnson limit. Hence, understanding how the devices in cascode designs react to aggressive voltage swings beyond breakdown is an important step toward realizing the full potential of SiGe HBTs. The present work introduces a method for evaluating the onset of SiGe HBT hard breakdown during RF operation by comparing RF simulations to dissipated power measured at *dc* breakdown. This can be applied

to any circuit as long as the transistor is well-modeled in a technology computer-aided design (TCAD) platform. Using the proposed method, safe RF operation can be achieved with swings beyond BV_{CBO}.

4.1 TCAD Setup

This work looks at large-signal device simulations of a first-generation SiGe HBT using a TCAD simulator. The device model has been carefully calibrated to *dc* measurements [74, 75]. The challenge of getting a first-generation SiGe HBT cascode amplifier to swing beyond breakdown requires seemingly impractical load conditions, which will be unnecessary in future higher technology nodes. BV_{CBO} is about twice that of the second generation device, and since the variation in V_{CB} is proportional to the load impedance, achieving a large swing for a small TCAD device requires a large resistance. This is acceptable, since the device studied here is part of a larger periphery of parallel SiGe HBTs used to create the core of the PA. As an example, given that a unit cell matching our TCAD device will provide 5% of the total current, a 50 Ω design load looks like 1 kΩ. Reiterated using Ohm's Law, voltage is shared across parallel devices and is thus constant, while the current is divided by 20 when transformed from the load to the collector of the unit cell; hence the impedance on the output drops by the same factor for our small TCAD device. Hence, a large load is not impractical for this endeavor. This work uses a load line on the order of 1 kΩ.

To get a 14 volt swing, the upper collector-base potential (V_{CB2}) is set to about 6 V. The lower device CB potential is kept low by setting V_{B2} to a reasonable value. There is considerable distortion in the output waveform, but this will be a consequence of most designs at the breakdown edge, since the device will encounter gain degradation due to the effects of low injection and the Kirk effect.

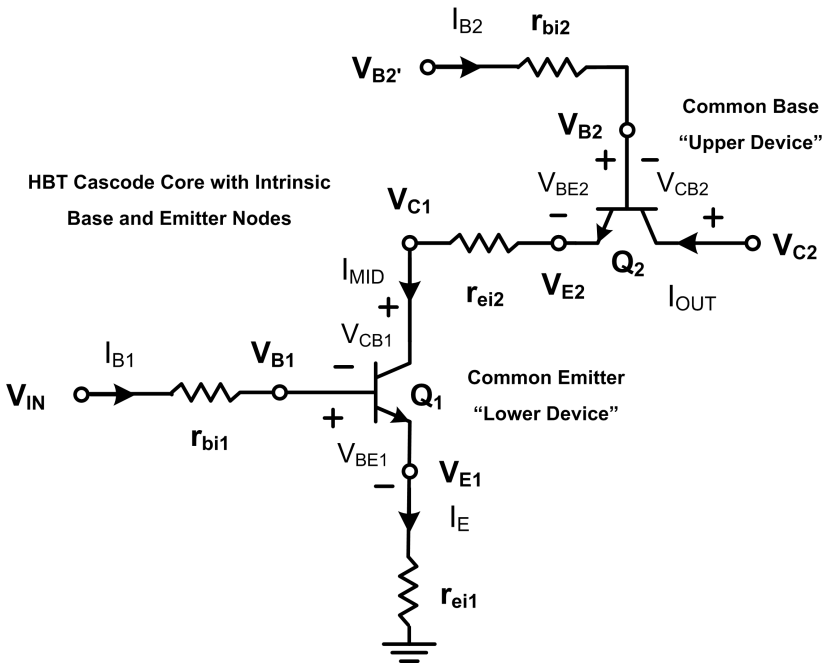

Figure 4.1: Voltage nodes and current designations for cascode waveform analysis, showing intrinsic emitter and base resistances.

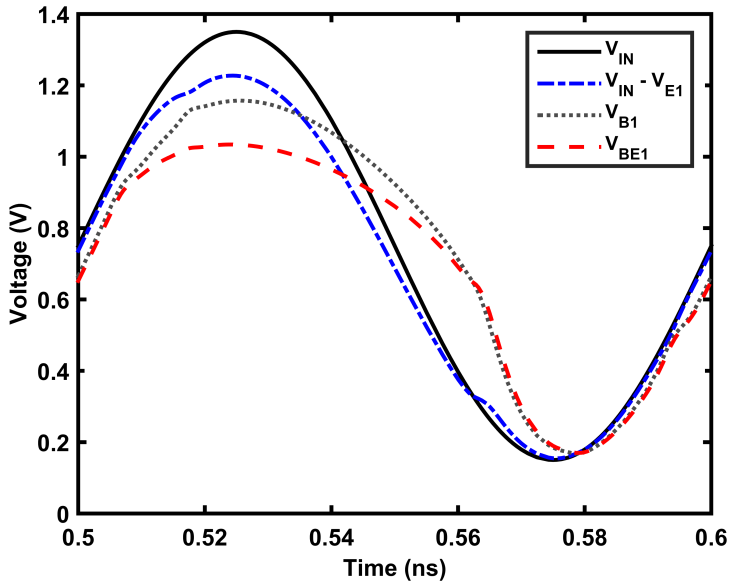

Figure 4.2: Input voltage distortion due to intrinsic base and emitter resistances. This distortion affects the upper device, which produces additional distortion.

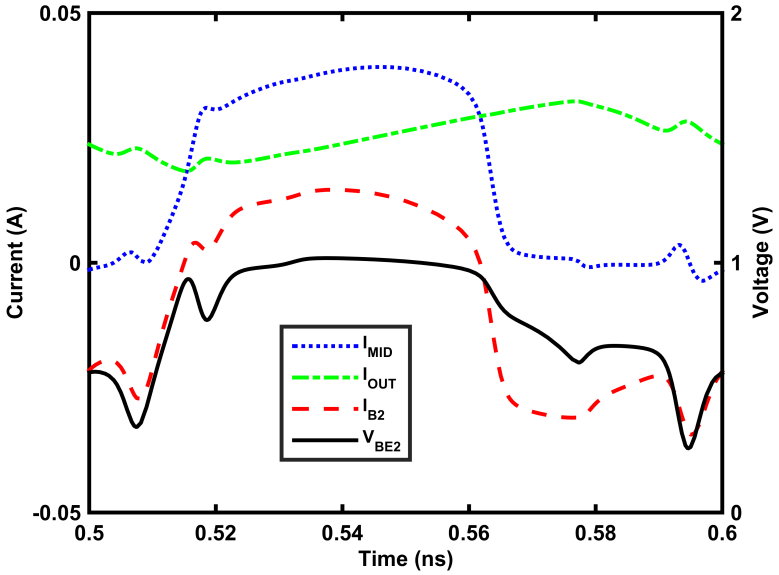

Figure 4.3: TCAD (transient simulation) node currents and intrinsic base-emitter voltage for the upper device for one period of aggressive voltage swing.

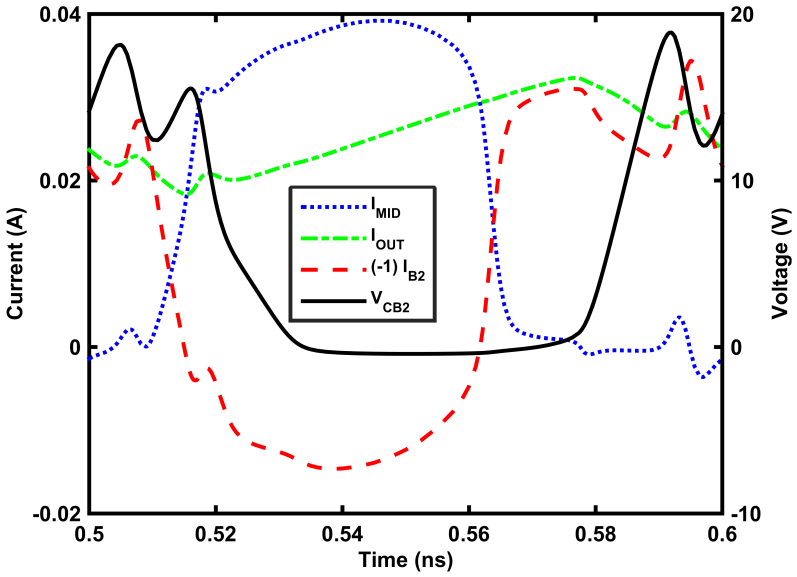

Figure 4.4: TCAD (transient simulation) node currents and intrinsic collector-base voltage for the upper device for one period of aggressive voltage swing. The upper device's base current is reversed to better indicate the onset of BCR.

4.2 Cascode RF Simulations

The waveforms displayed in Figures 4.2, 4.3 and 4.4 show intrinsic node voltages juxtaposed with the branch currents into the transistors (as shown in Figure 4.1). It should be noted that portions of the current do not flow completely through the transistor junctions, since there are capacitive currents involved. Separating out the capacitive portion of the waveform can have some benefit in approximating RF damage [1]. The limitations of relating RF and *dc* damage have also been explored in TCAD [2].

There are interesting complications that can be gleaned by examining the waveforms in Figures 4.2, 4.3 and 4.4. First, there are several distortion mechanisms that get engaged at high currents. In Figure 4.2, the base and emitter resistance distort the voltage across the intrinsic base-emitter junction (V_{BE1}). Second, there is some ringing in the upper transistor waveforms as the current attempts to sharply change. For the upper CB voltage waveform (V_{CB2}) three peaks are seen, triggering about a central voltage that coincides with the cascode fly-back point (15 V in this example). Similar overshoot about the cascode fly-back boundary has been seen in previous work [3]. In Figure 4.4, the peak V_{CB2} reaches 18.8 V. This ringing may also be related to a cascode self-protection mechanism elucidated in an earlier study [15], or it may simply be harmonic content.

From Figure 4.2, power dissipation in the base-emitter junction can be seen as the in-phase overlap between voltage and emitter current, but the majority of the heat will come from the CB junction, due to higher fields. The overlap of high emitter-terminal current (I_{MID}) and large V_{CB2} estimates the power dissipated in the junction, yet there is additional dissipation via reversed base current and V_{CB2} (refer to Figure 4.4). At moderate power levels, V_{CB2} is mostly out-of-phase with I_{OUT}, and BCR is minimal due to moderate V_{CB2}. Indeed, this is generally the case in PA circuits due to efficiency requirements. As the input voltage changes get more

pronounced, current increases faster on the upslope and the capacitive flow of current introduces multiple peaks in voltage and BCR current.

The complex interaction between electric field and current density can be seen in the sequential snapshots shown in Figure 4.6 and Figure 4.7. Note that the waveforms and cross-sections are taken from the fifth period of a transient simulation. The cross-section at 0.550 ns is omitted in order to coincide the first cross-section with 0.500 ns and the last cross-section with 0.600 ns, the left and right edges of the waveform graphs. The sequence reads from left to right, then continues in this fashion by rows, top to bottom. The active regions of the transistor are shown in Figure 4.5 for reference. Capacitive currents can most clearly be seen in the next to last row of Figure 4.8, although the very last row of cross-sections shows an interesting interplay between electron and hole current, as well as impact ionization (refer to Figure 4.9, Figure 4.10 and Figure 4.11.

This interplay between current and electric field is most deleterious to the center of the collector. As the device gets hotter, current pinch-in will become more pronounced

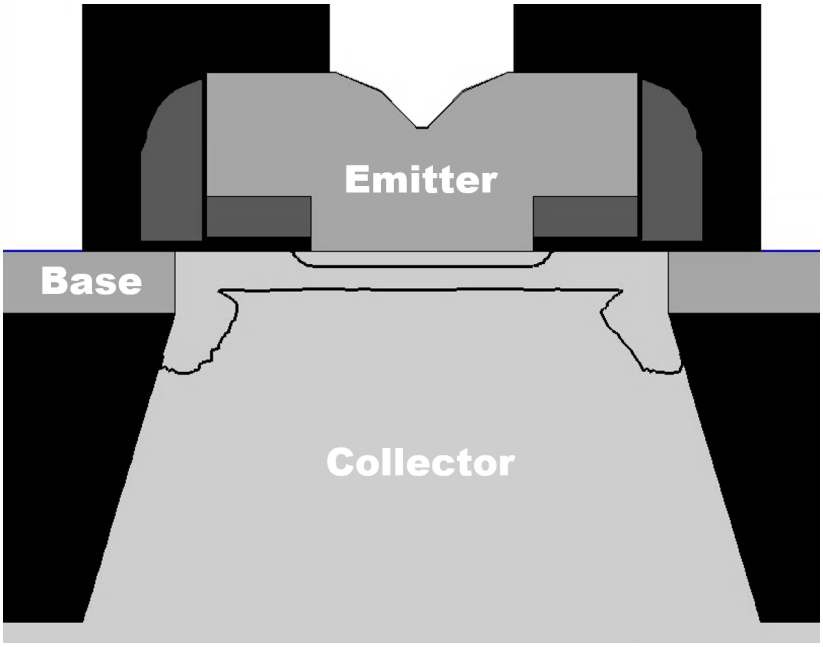

Figure 4.5: A labeled TCAD cross-section.

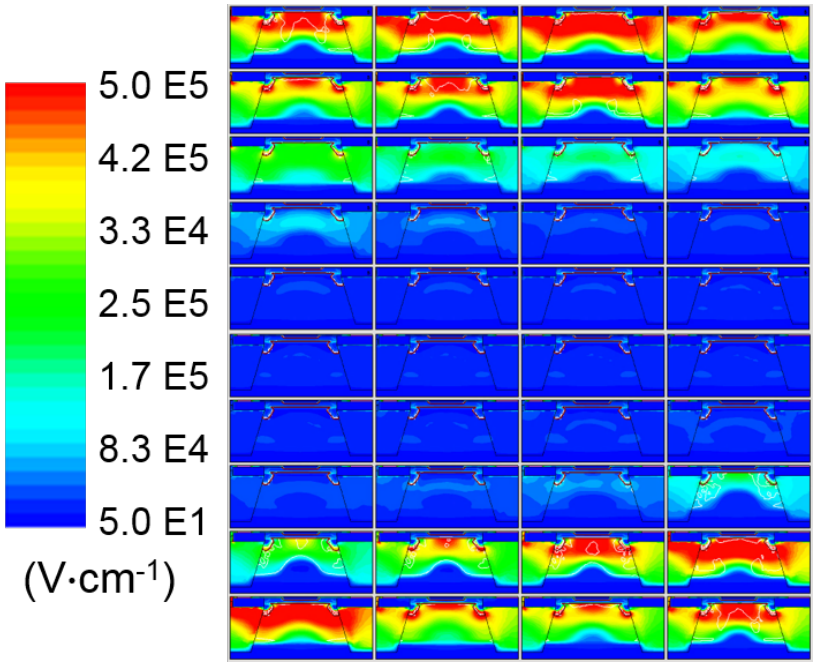

Figure 4.6: Electric field cross-sections taken at 40 of 41 equally spaced intervals across one period.

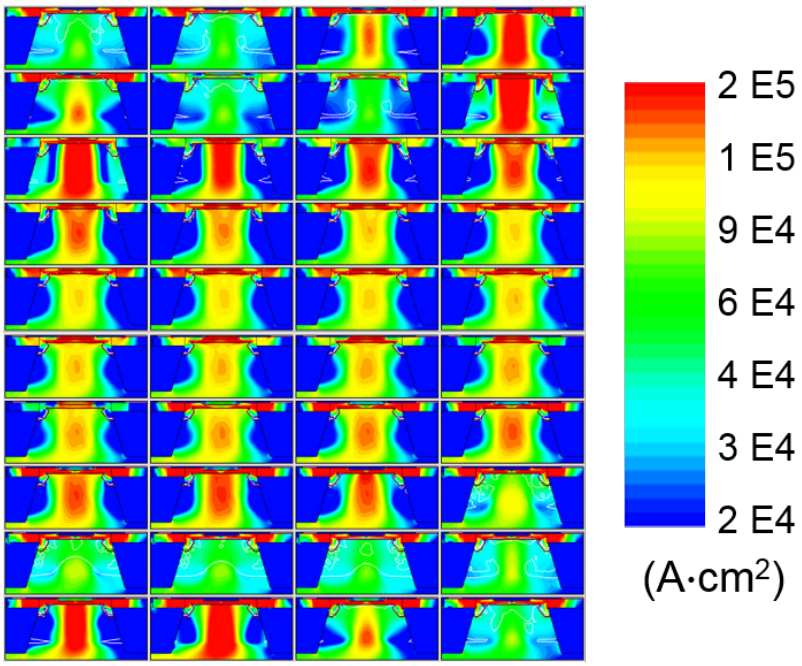

Figure 4.7: Total current cross-sections taken at 40 of 41 equally spaced intervals across one period.

and a cut-line through the center of the device will give the worst-case product of the two quantities. The next section discusses a method for approximating the RF

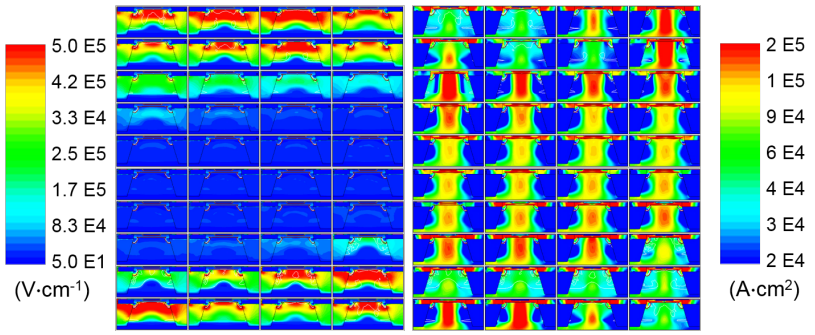

Figure 4.8: A side-by-side comparison of Figure 4.6 and Figure 4.7, electric field on the left and total current on the right.

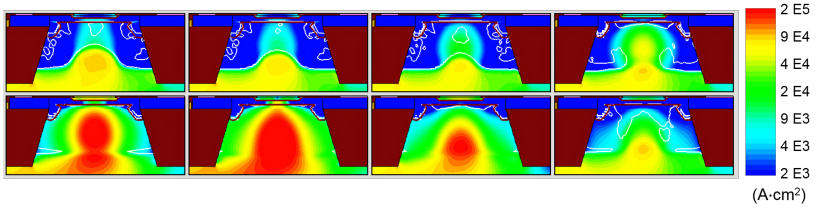

Figure 4.9: Electron current only, matching last two rows in Figure 4.8.

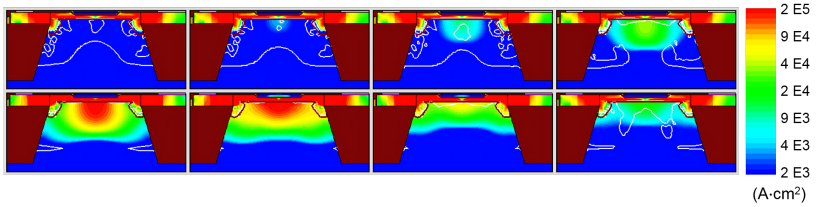

Figure 4.10: Hole current only, matching last two rows in Figure 4.8.

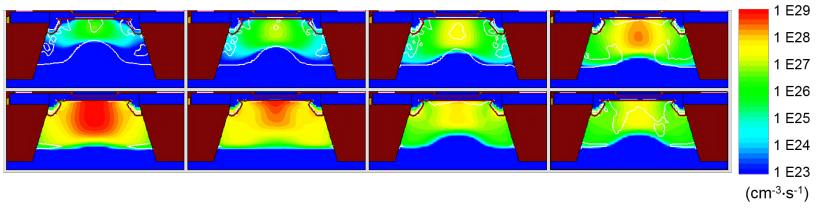

Figure 4.11: Impact ionization only, matching last two rows in Figure 4.8.

breakdown point based upon the electric field and current density using data taken at a center cut-line (vertical).

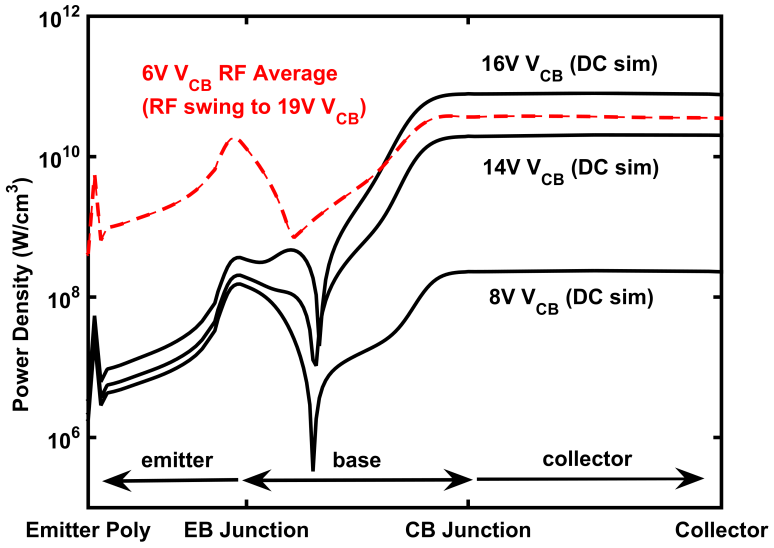

Figure 4.12: Average power dissipation for RF operation (as shown in previous figures) compared to *dc* simulation with a varying CB voltage. RF operation is comparable to 15 V across V_{CB2}, although swinging up to 18.8 V.

4.3 Differences in RF and *dc* Damage

Evaluating RF safe operation boils down to limiting the lattice temperature in the collector. Figure 4.12 is a plot of power density, calculated from electric field and current density, in relation to position in the transistor. For similar thermal conditions, calculation of the power density allows for an approximation of the self-heating that occurs within the device. Due to the additional feedback mechanism of avalanche generation, the collector region is most prone to thermal runaway conditions. Calculations are performed along a vertical cut-line at the center of the transistor. Power dissipation during RF operation is comparable to 15 V across V_{CB2} (as indicated by the distance to the 14 V and 16 V *dc* simulations in Figure 4.12), although swinging up to an 18.8 V maximum. Previous studies investigating RF to *dc* comparisons have indicated a 10-20% range above *dc* breakdown, to which this present calculation adds further understanding.

4.4 Implications and Summary

Large-signal waveforms can be complex. TCAD evaluation of hard breakdown can be performed by looking at the power dissipated in the device under *dc* and RF operation. In this work, we calculate that a cascode dissipates equivalent power in the collector region using an RF signal that reaches 20% of the established *dc* power at fly-back. As external base resistance is increased, reduced swing should be expected. Although requiring further development to properly include resistive and temperature effects (e.g., base resistance, ballasting and mutual heating), this method of comparing RF to *dc* breakdown shows promise as a solution for reliably maximizing performance of large-signal SiGe HBT circuits during the design phase. For extension of reliability concepts to complex modulation schemes or pulsed operation, observing the device in TCAD has additional value.

CHAPTER 5

ASSESSING SIGE HBT MUTUAL HEATING

This chapter presents measurements on a 10-cell silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) shared-subcollector array, intended for use as part of a power amplifier core. By physically separating the 10 base terminals in the parallel SiGe HBT array such that currents can be monitored individually, the thermal interactions between the devices are observed. For further insight into the electrothermal interaction between devices in relation to separation distance, and also to determine the feasibility of power core resizing, SiGe HBTs in the array are turned *off* and *on* in various combinations. The influence of process variation affecting the current profile of the array is also presented. Simulations of this array's thermal profile when packaged using copper pillar flip-chip technology is also reviewed in the final section.

5.1 Introduction

In designing a compact watt-level RF power amplifier core using silicon-germanium (SiGe) heterojunction bipolar transistors (HBT), a reduction in the layout footprint can be achieved by overlapping adjacent collectors. The resulting shared subcollector structure removes the trench isolation between SiGe HBT unit cells, thereby increasing mutual heating (MH) in the more compact array, since thermal coupling increases between devices [38,76–80]. Understanding the thermal interaction between each pair of unit cells in the array becomes more necessary as the power core increases in size, and can be estimated through thermal imaging [39, 41, 81, 82] or technology computer-aided design (TCAD) modeling [83,84]. These solutions present additional

challenges, however, since accurate thermal imaging is often impeded by the back-end-of-line (BEOL) metallization, and TCAD simulations are often limited by the approximations made in calibrating the thermal boundary conditions. To observe the operating temperature electrically, sensor circuitry can be added in proximity to the core [85], but this does not capture the actual currents or the junction temperatures within each device. Nonetheless, since the primary goal of thermal modeling is often for determining the electromigration lifetime in the BEOL, these techniques may be sufficient. But if the goal is to correctly model device currents and the impact of memory effects on the design [71, 72, 86–88], the better solution would be to measure the device currents individually. The present work performs this measurement with a custom integrated circuit and provides a measurement methodology for analyzing mutual heating in SiGe HBT arrays. In practice, reproduction of this data is limited by access to measurement resources (specifically, power supplies for each SiGe HBT); hence this work will detail atypical results and issues encountered during data collection.

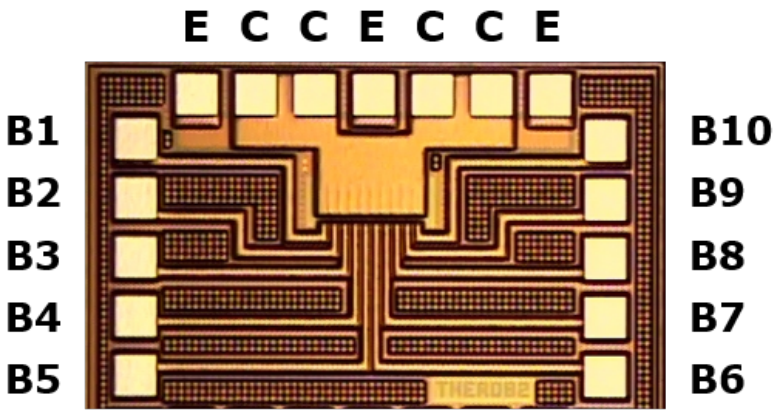

Figure 5.1: A labeled die micrograph of the mutual heating test structure, a 10-cell, shared-subcollector SiGe HBT array. The emitter terminals are connected by through-silicon vias to a grounded backplane, minimizing emitter degeneration.

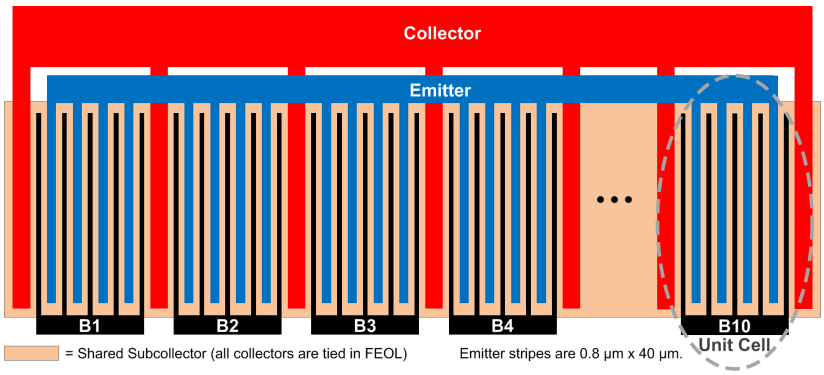

Figure 5.2: Layout of the 10-cell array indicating 4-stripe emitter unit cells (not to scale).

5.2 Measurement Methodology

The present work examines the actual currents that are influenced by mutual heating in a 10-cell shared-subcollector array, by separating the base terminals of each unit cell, such that base currents can be measured individually (see Figure 5.1 and Figure 5.2). Since the collector is shared and the emitter is tied to ground using through-silicon vias (TSVs), the base currents serve as the only experimental access point for electrically observing mutual heating effects.

Initial measurements were attempted by wafer probing on a hot chuck, but the heat generated by the array made probe contact difficult above 1 V on the collector. Below 2 V on the collector, mutual heating is insignificant, and the current distribution of each base is essentially flat for the interior eight SiGe HBTs, with the outer two SiGe HBTs being slightly cooler. Above 1 V on the collector, wafer-probed measurements were consistently unstable for the unballasted first-generation GlobalFoundries BiCMOS 5PAe (5PAe) SiGe HBTs in this study (0.8 μm x 40 μm x 4 stripes x 10 cells as in Figure 5.2; high-resistivity substrate). To observe the devices at higher junction temperatures where mutual heating would be more pronounced (and where a PA would typically be biased during operation), wafer probing was abandoned as a reliable technique. Instead, a wire-bonded solution that could provide additional base ballast was pursued.

To achieve reliable data, the integrated circuit was attached to a custom printed circuit board (PCB) and each base was wire bonded to a trace with a dedicated connector (Figure 5.3). The PCB incorporated series resistance in each base path to ballast the array against thermal runaway during testing. Ballasting resistance was within 2% tolerance for each surface mount resistor used, and the same value resistance was used for each path (570 Ω on each base terminal).

The data collected on the test structure in Figure 5.3 includes variation in base-emitter voltage (VBE) from 0.76 to 0.84 V in 0.02 V steps, and collector voltage (VC) increases from 1 to 4 V in 1 V steps. The actual extrinsic base-emitter voltage for each SiGe HBT is reduced by the current through the base ballast. Cells in the array were iterated in all possible combinations (2^{10} in total) for each bias point, to observe the effects on current when some SiGe HBTs were in an *off*-state. The *off*-state consisted of a 0 V VBE condition for that particular device.

The purpose of the *off*-state data collection is three-fold. First, this allowed for the analysis of current increase as a function of separation distance (unit cells were 18 μm apart). Second, any imbalance intrinsic to the design or due to process variation could be observed. Lastly, the feasibility of core resizing could be analyzed. For example, turning *off* half of the unit cells would theoretically reduce the output power of a PA by 50%, while improving efficiency, when compared to the full power cell array being *on*.

To eliminate bias presented by the order of data collection, data was also recollected in the reverse binary progression, using B10 in Figure 5.4 as the least significant bit as opposed to using B1, since the terminals could only be turned *on* sequentially. Additionally, the thermal capacitance was high due to the quality of the thermal epoxy used in the setup, which presented memory effects in switching between configurations. Hence, measurement settling time was included in the procedure to allow for the current to reach equilibrium. Redundant measurements were taken

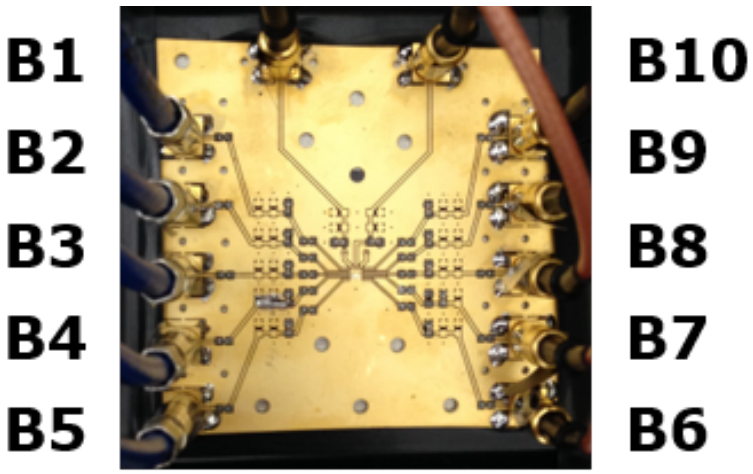

Figure 5.3: A photo of the PCB used in the mutual heating experiments..

to identify any anomalies introduced by the interaction between the circuit and the measurement system as a function of time. This repetition also provided insight into startup behavior for the array, as in Figure 5.7, showing the effect of high thermal capacitance introduced by the substrate-to-PCB epoxy. The currents settle into their final values at around 60 seconds, with the majority of the increase occurring in the first 10 seconds.

5.3 Measurement Results

An overview of the data for a power cell array that exhibits natural imbalance is presented. Since one of the main objectives of this research is to identify issues with turning *off* individual cells in a shared-subcollector SiGe HBT array in order to improve efficiency at a lower output power, presenting an example of this imbalance can broaden understanding and possibly lead to design improvements. The source of imbalance is likely process variations, since PCB design and base ballast variation were eliminated as the root cause of this imbalance.

Figure 5.5 shows the current profile for an array with a more volatile device at position 10, at the edge of the array. Alone, it conducts significantly more current than other SiGe HBTs, and in combination with those devices, it shifts the peak in

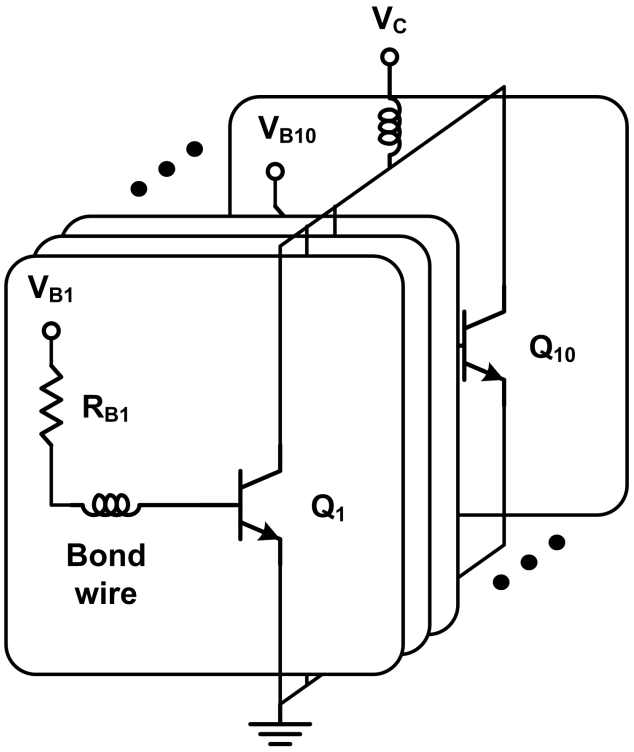

Figure 5.4: Schematic of the mutual heating test circuit. The ground connection is a combination of bond wires and through-silicon vias, and the collector connection is also wire bonded. The base resistance is surface mounted on the PCB.

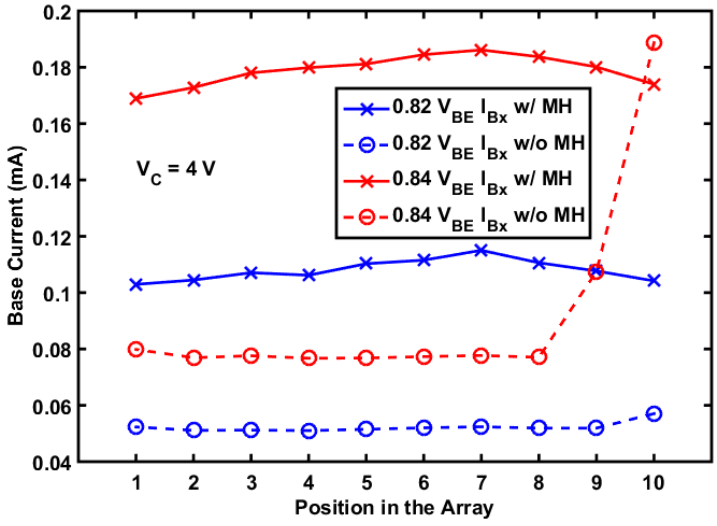

Figure 5.5: Base current for each HBT in the 10-cell array, with and without mutual heating at 4 V on the collector. The base currents without mutual heating are collected with all other HBT base voltages set to zero volts.

the temperature profile closer to itself. The bias condition has been chosen to accent this asymmetry. The characteristic peak in current shows bias toward devices with a naturally higher base current from more pronounced self-heating. Figure 5.6 plots the current gain of each device in the array (collector current divided by base current for each device). Observe that the current gain decreases more rapidly for position 10 as base voltage increases.

Figure 5.8 indicates the impact of turning half the devices *off* in the array, while Figure 5.9 reduces the array size further, showing four *on* devices in different configurations. Spacing the *on* devices equally results in the best performance. Turning *off* the centermost and the outermost cells results in the lowest collector current, and therefore the lowest net operating temperature. For the 10100—00101 case, the rightmost device is the one that is running hotter due to process variation. It is hogging a majority of the overall current which makes it and its neighbors hotter than the left side of the array. For the 00011—11000 case, the increased current for the outer devices may be related to the additional collector periphery available to those devices. Hence, the collector resistance is reduced for the outer devices, and therefore it is not unreasonable to expect additional current from a higher collector-base voltage. Additionally, if current from the center devices is flowing to collector regions further away from those devices, the outer devices may be running hotter due to the additional current flowing beneath them in the shared subcollector. Figure 5.6 illustrates the average contribution of a single SiGe HBT under the effects of mutual heating. When all devices are *on*, mutual thermal coupling is significant, and contributes considerably to the overall collector current. The sudden drop in current gain for the hotter cells in the array (positions 9 and 10 on the x-axis) as base voltage increases is the result of further increases in temperature due to more pronounced self-heating.

Figure 5.6 plots the current gain of each device in the array (collector current

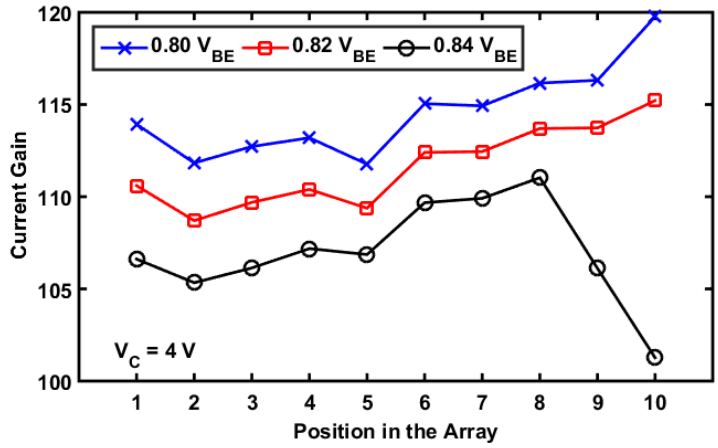

Figure 5.6: Collector current divided by base current for each HBT in the 10-cell array, without mutual heating, at 4 V on the collector.

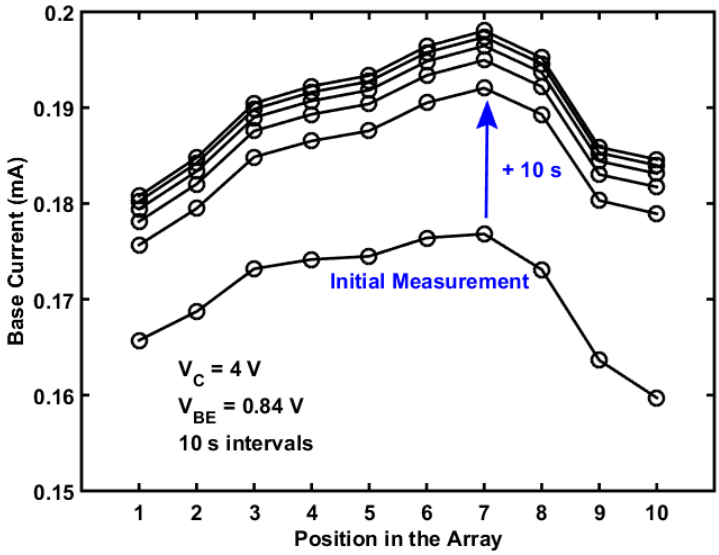

Figure 5.7: Time progression of base currents in the array in 10 s intervals, indicating how the array heats up over time.

divided by base current for each device). The current gain decreases more rapidly for position 10 as base voltage increases.

Figure 5.7 shows the time evolution of the base currents as the devices are turned *on*. The currents settle into their final values at around 60 seconds, with the majority of the increase occurring in the first 10 seconds.

Figure 5.8 indicates the impact of turning half the devices *off* in the array, while

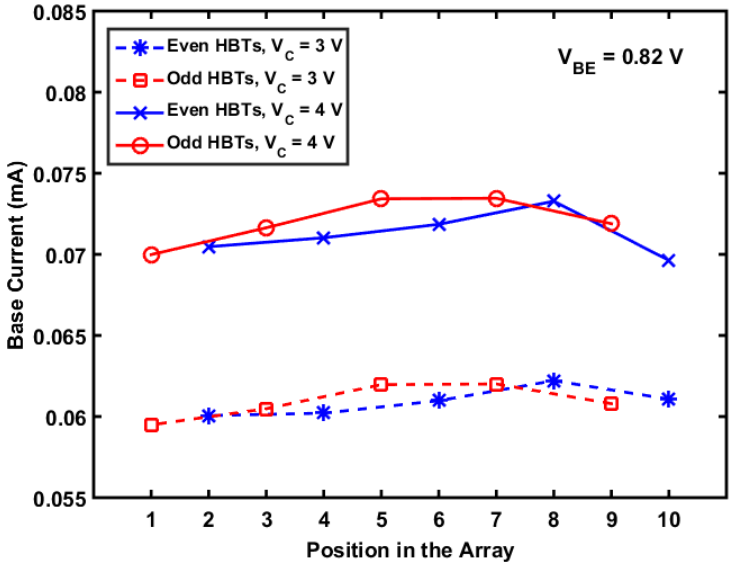

Figure 5.8: Base currents when half of the array is *off*. Even and odd positions in the array are turned *off* and compared.

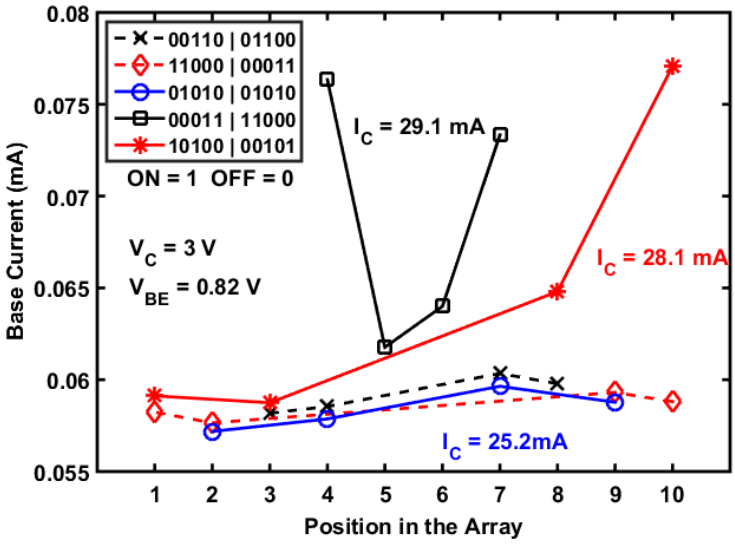

Figure 5.9: The impact of resizing the array to 4/10 size with 4 of 10 HBTs *on*. Various configurations are shown, with binary representations in the legend.

Figure 5.9 reduces the array size to four devices in different configurations. Spacing the *on* devices equally results in the best performance. Turning *off* the centermost and the outermost cells results in the lowest collector current, and therefore the lowest operating temperature.

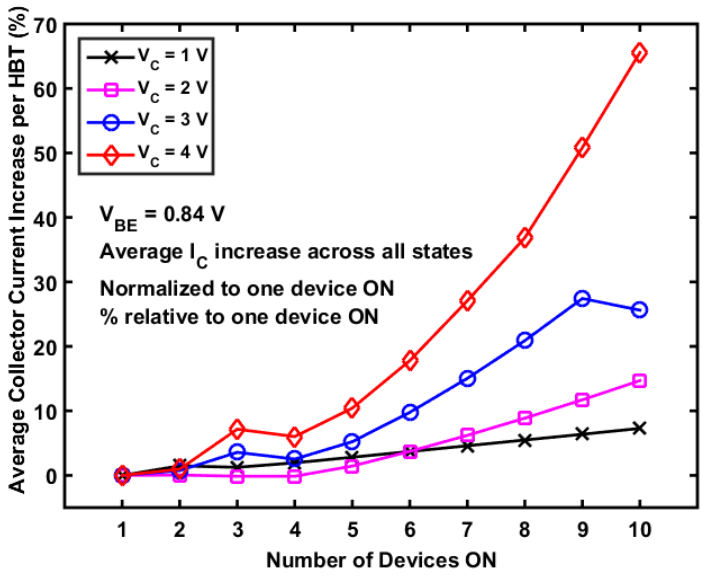

Figure 5.10: The average contribution to collector current by a single HBT plotted against the number of devices *on*. The currents are all relative to the average current of a single device being *on*.

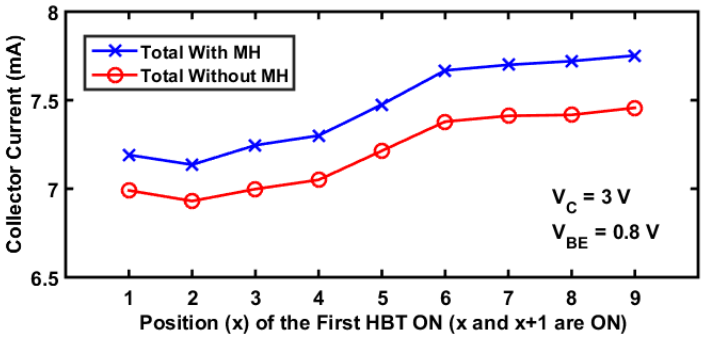

Figure 5.11: Collector current when two adjacent devices are *on* in the array. The collector current without MH is taken as the sum of the collector currents measured when each of the devices is *on* individually.

Figure 5.10 illustrates the average contribution of a single HBT under the effects of MH. When all devices are *on*, mutual heating is significant, and contributes considerably to collector current. When all devices are *on*, mutual thermal coupling is significant, and contributes considerably to the overall collector current.

Figure 5.11 and Figure 5.12 show the impact of distance on thermal coupling. Figure 5.11 plots data for devices that are adjacent, and the increase in collector current is fairly even across all such pairs in the array. The x-axis represents the first

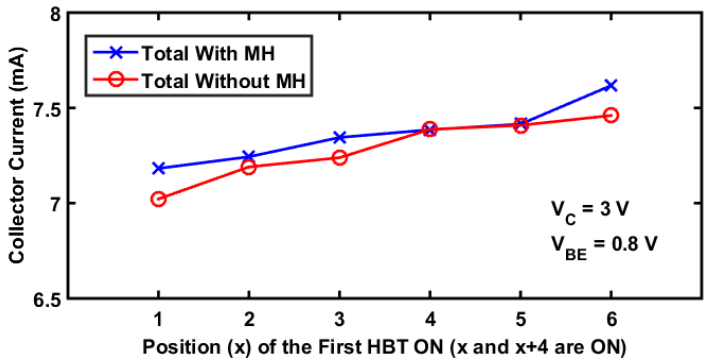

Figure 5.12: Collector current when two devices, four cells apart, are *on* in the array. The collector current without MH is taken as the sum of the collector currents measured when each of the devices is *on* individually.

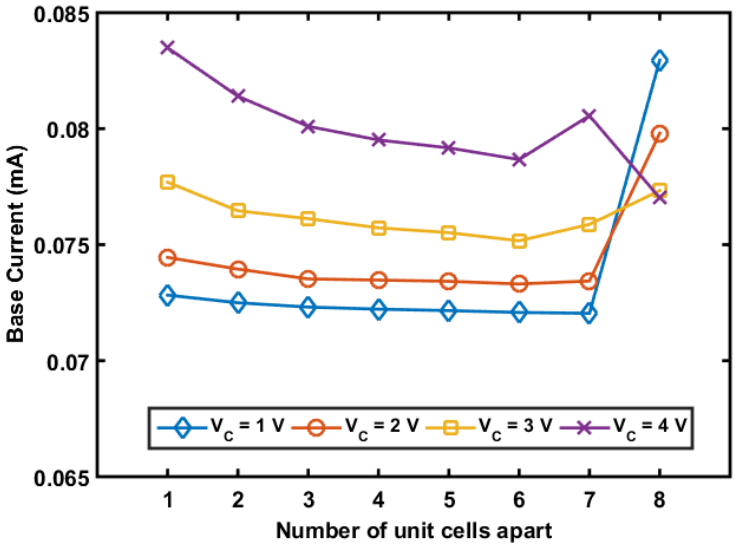

Figure 5.13: Base current for an interior device when two devices are *on* in the array, indicating the increasing effect of mutual thermal coupling as the devices are closer. Increased influence can also be seen when devices are the furthest apart, partly due to measurement memory effects.

SiGe HBT unit cell that is turned *on* in the pairing, so, as an example, the data at position 3 is compiled for the case when SiGe HBTs in position 3 and position 4 are both *on*. The data points labeled as without MH are summations taken from the SiGe HBT unit cells turned *on* in isolation, hence position 3 in Figure 5.11 is a sum of the data from position 3 and position 4 when each is the only device turned *on* in the array. Figure 5.12 follows the same scheme, with only two cells turned *on*, four

transistors apart, and hence have three SiGe HBTs between them. Figure 5.13 shows the impact as the devices are placed farther apart, with some memory effects evident from the measurement being taken too quickly after the full array had been active.

Of particular importance to the present work is to set forth a strategy for collecting data relevant to the 5PAe design kit, which includes a specific thermal network design whereby mutual thermal coupling can be added via thermal resistance and capacitance values. By measuring currents for each pair of unit cells in the array, mutual thermal resistance between all pairs can be estimated through parameterized simulation. The value of mutual resistance can then be selected as the closest fit to the measured data. In other words, the thermal networks can be chosen to fit the data using this technique. The actual array can be measured (i.e., using actual thermal properties from a fully packaged test structure), providing designers a more complete model than the foundry can provide, since the foundry cannot address specific packaging parasitics. In practice, complicated thermal networks may suffer from convergence issues, so a simpler approach would be to set the temperature of each device in the array manually by observing the unit cell currents from measurement when all devices are *on* in the array, and then choosing an appropriate device temperature to create that current. Beyond four cells apart, or approximately 100 m, there is little effect, so mutual heating could be ignored for such devices to improve convergence.

Although capacitive thermal coupling is beyond the scope of this work since only a *dc* structure was fabricated, revision of this test structure could incorporate secondary paths for *ac* signals, coupled into each unit cell in parallel with the base ballast and bias. In this manner, the effect of mutual thermal coupling on scattering parameters, linearity or reliability might be investigated. Nonetheless, by observing the *dc* data alone, a PA design would expect to see radio frequency (RF) performance shifts from mutual thermal coupling primarily from the significant shift in base and collector bias current. Figure 5.5 indicates a 100% increase in base current at 4 V collector

bias, and Figure 5.10 shows a 70% increase in collector current for the same bias. Hence, resistive components of scattering parameters would shift significantly, since these quantities are inversely proportional to current, thus altering the input and output match required for optimal RF performance. Small capacitive shifts may also be seen from high injection effects (collector resistance) on the collector-base capacitance. In practice, large SiGe HBT power cells would need to be tuned for improved performance in the absence of precise thermal models, although this work is a step further toward a solution.

In addition to the RF parameter shifts, the safe operating area will be reduced by thermal effects evident in the data, as is the electromigration lifetime of the BEOL metals, since increased current would be dissipated in the SiGe HBT as heat, reducing PA lifetime.

5.4 Implications

Dominant devices in shared-subcollector SiGe HBT arrays will shift the electrothermal profile (distribution) at high collector currents. If the power cell array is intended for resizing, turning *off* the dominant device is crucial to minimizing collector current, as it can exhibit a strong influence on the array's collector current. If a shared-subcollector array is to be resized, iterating through expected configurations and observing the collector current will identify troublesome states to be avoided.

The test structure presented in this work can also be used to analyze the effects of separation distance on mutual thermal coupling in order to better calibrate thermal networks in compact models. The thermal networks provided within any given process design kit (PDK) will be limited in scope, as packaging effects can vary with implementation and models are typically generated from on-wafer measurements. By observing mutual heating from the electrical perspective presented in this work, discrepancies between measurement and simulation can be better understood, and

yield benefits to future SiGe HBT power amplifier designs. This work suggests using the data collected as a first-order approximation of thermal resistance, by parameterizing thermal resistance or device temperature, and selecting values that align with the data. This will help improve first-pass measurement to simulation correlation, but will not capture the effects of process variations evident in this work.

This measurement technique can be extended to more advanced SiGe HBT technologies to understand thermal coupling in higher-frequency amplifiers. As frequency increases, cascode configurations are typically employed due to decreased breakdown voltages. For the cascode, the majority of the heat will likely be generated in the common-base device. This work can be extended to explore mutual thermal coupling between the common-base and common-emitter device as a function of separation distance, in addition to the effects on parallel SiGe HBTs in the array as a whole.

5.5 Thermal Performance of Copper Pillar Flip-Chip PAs

To reduce overall cost of a packaged PA, thermally insulating materials can be selected to surround the integrated circuit. When this is the case in a wire-bonded design,

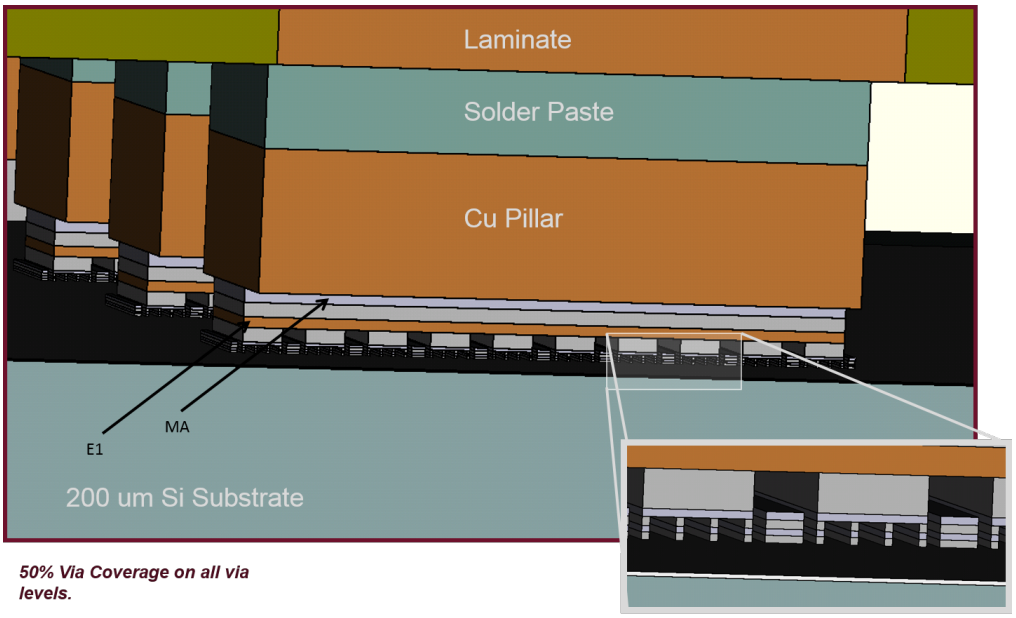

Figure 5.14: Copper pillar flip-chip BEOL layers.

the majority of the heat will escape through the silicon substrate, whereas a flip-chip design must dissipate heat through the flip-chip vias. Research into the feasibility of dissipating sufficient heat through copper pillar vias in a flip-chip package was performed, and subsequently implemented as a product for Qorvo, Inc. (formerly RFMD). The benefits of this work include reduced package area and height, making flip-chip SiGe HBT PAs more attractive for adoption into smartphones.

Considering aluminum metal interconnects typically used in a first generation SiGe HBT technology, device temperatures below 125 °C should be maintained for electromigration mitigation. A maximum 85 °C handset temperature can be assumed below the packaged PA. The package consists of a flip-chip die connected to a laminate via copper pillar and solder paste (see Figure 5.14). The laminate is a multilayer, flexible structure that serves as the base of the package, also serving to provide additional passive circuitry. All intervening and surrounding layers are simulated as thermal insulators. To reduce simulation complexity, BEOL via layers were modeled as a 50% mixture of via metal and layer dielectric. Select results are included in Figures 5.16 and 5.15. To summarize the findings, placing copper pillars in line with the transistors offers more even thermal spread and reduced operating temperature. If the emitter connections must be placed between HBT linear arrays, heat can be dissipated through dedicated connections to the substrate. Additionally, the collector metalization can further shift the thermal spread within the power core.

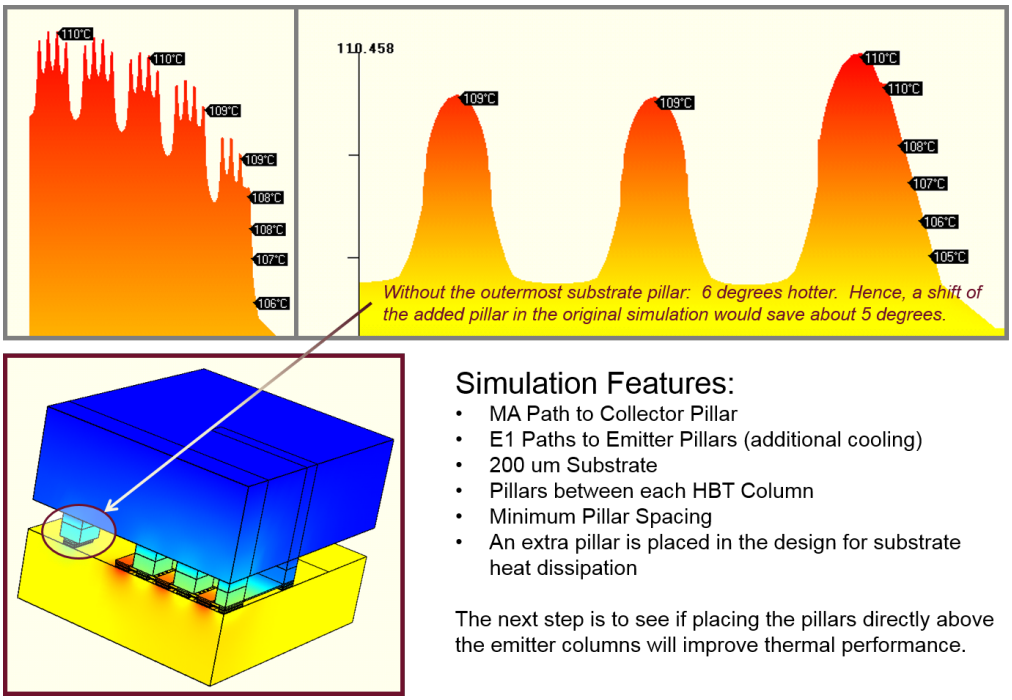

Figure 5.15: Results of thermal simulations with copper pillars between emitters.

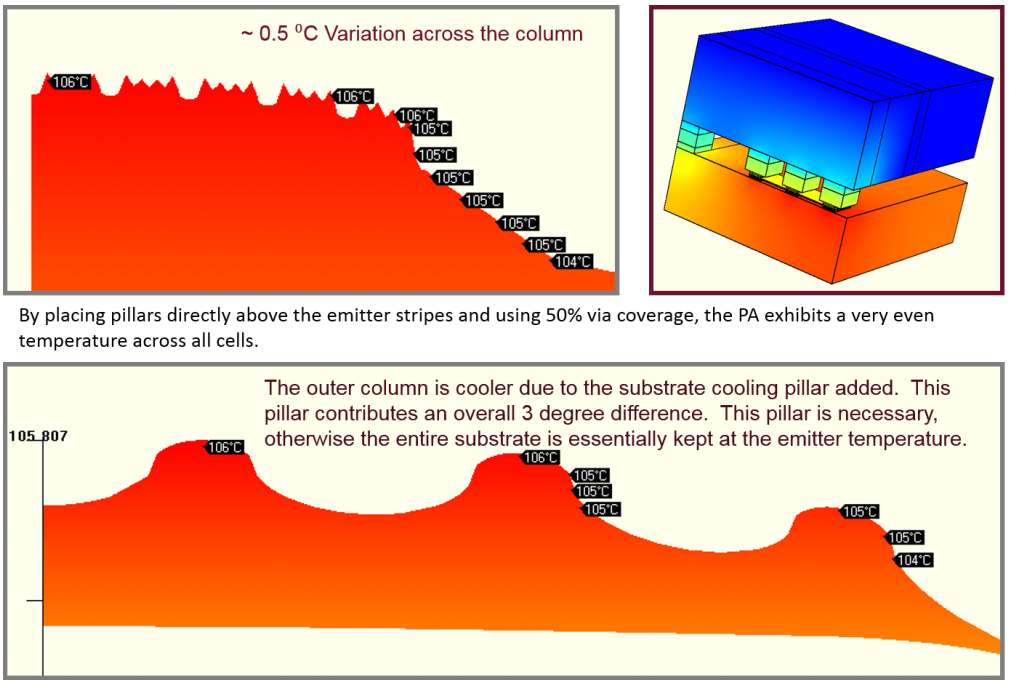

Figure 5.16: Results of thermal simulations with copper pillars above emitters.

CHAPTER 6

LEVERAGING IMPROVED PERFORMANCE OF FET SWITCHES ON HIGH-RESISTIVITY SUBSTRATES

This chapter explores the feasibility of SiGe HBT power cores that can be switched, resized and tuned by leveraging CMOS switches. A portion of this exploration began with the mutual heating study in Chapter 5, and conclusions in this section build from that work. To improve the *on*-state resistance of the NMOS switches, a process that incorporates a high-resistivity substrate is used, namely GlobalFoundries BiCMOS 5PAe. This work coincides with efforts to improve the performance of the CMOS switches, in which customers of GlobalFoundries (IBM, at the time) requested a tighter pitched NMOS device to improve the *off*-state capacitance of the device. As part of this work, new SPDT switches were evaluated, for the first time in both 1 kΩ at 50 Ω substrates, using the same design mask. To the author's knowledge, this is the first time such a study has been done. To leverage the improved Ron*Coff product of the tight-pitched switch (TPS) FET (eventually launched with an improved low-noise HBT as GlobalFoundries BiCMOS 5PAx) switched-capacitor arrays, referred to as programmable arrays of capacitors (PACs), are also evaluated.

6.1 Introduction

High-resistivity (or hi-res) substrates have a distinct advantage in RF designs as operating frequency increases, since substrate losses are reduced [36]. GlobalFoundries BiCMOS 5PAe and 5PAx are SiGe HBT processes specifically tailored for power amplifier applications, including a 1 kΩ substrate module, as well as TSVs. The

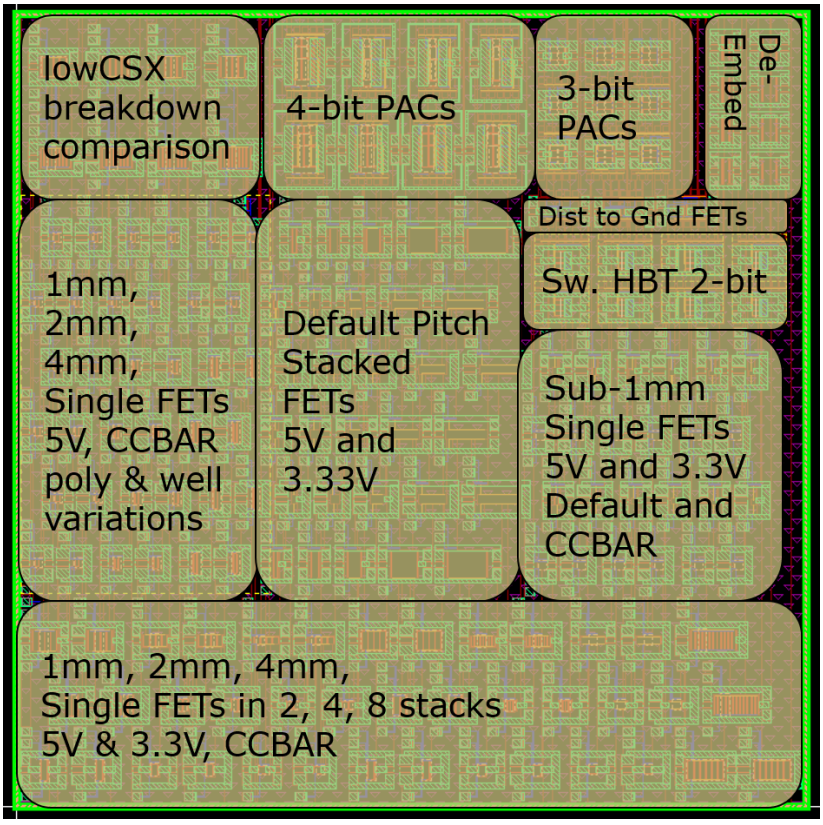

Figure 6.1: Probe structures in 5PAe for switch evaluation.

hi-res substrate increases inductor quality factor, or Q, especially at C-band and X-band frequencies, where substrate losses become significant and increased output power requires large, inductive combining structures whose performance is driven by the substrate resistivity. Fully integrated front-ends are also an important selling point for hi-res substrate technologies.

NMOS switches are typically designed in silicon-on-insulator (SOI), which is the extreme implementation of a hi-res substrate. The purpose of this study is to understand 5PAe and 5PAx as a "poor-man's SOI", to see the possible markets hi-res designs can enter. Pursuant to that goal, each section of this chapter looks at using the switch in a different way. The first section looks at stacked-FET switches and plots performance against device width for a 3.3 V and a 5 V device. The stacks are then combined to create SPDT switches for watt-level applications. The next section

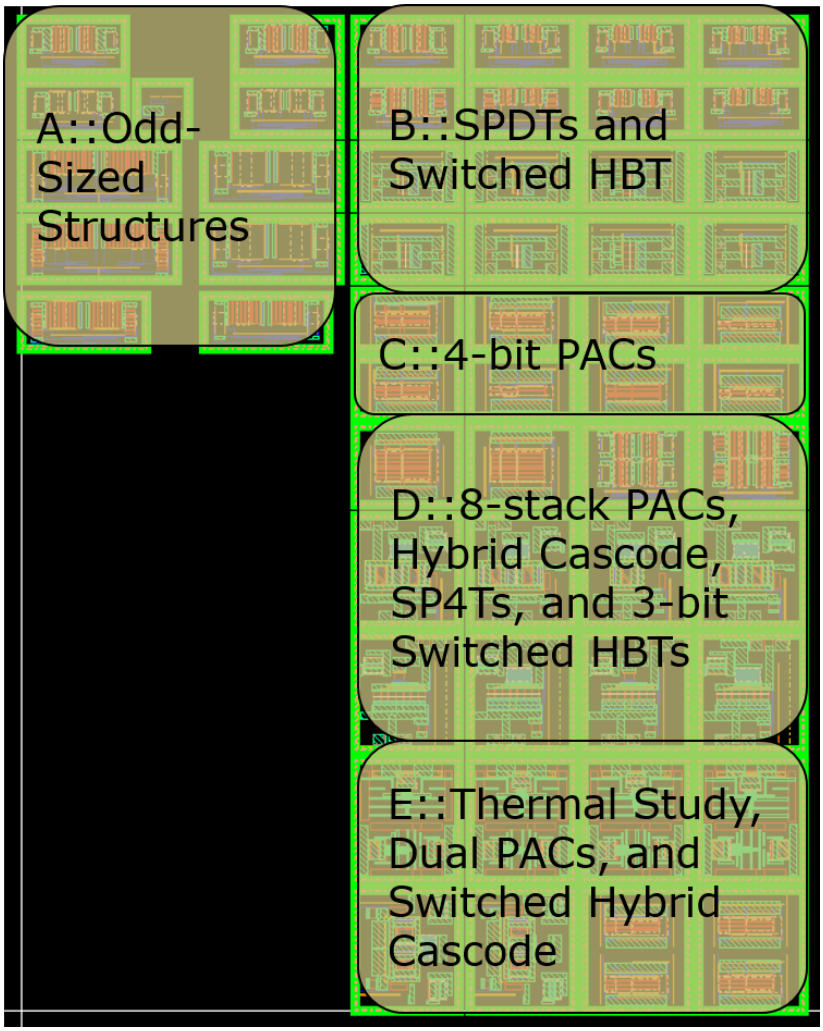

Figure 6.2: Structures for dicing from the 5PAe tapeout.

takes a brief look at using the FETs as switches to resize a power core. In this section, the reliability concerns of the earlier chapters shed light on the limitations of a series switch at the base of the SiGe HBT, and modified designs are presented. The last section uses stacked switches to create 2 and 4 bit PACs, and compares results across 1 kΩ at 50 Ω substrates. The layout area for this study was quite large, and is shown in Figure 6.1 and Figure 6.2.

6.2 Stacked FETs

Stacked NMOS devices are typically used to electrically isolate and connect RF circuits, using negative and positive gate voltage to switch between the respective states. Stacking of the devices improves isolation in the *off* state and improves the voltage handling of the overall stack [55, 56, 89]. Triple-well devices are typically used to isolate the body of the device from the substrate. The n-type well used for this purpose is set at a positive bias to keep all p-n junctions reversed-biased. The bulk connection for a series switch is kept at a negative voltage during isolation, and at 0 V during conduction. A shunt-connected stack of NMOS devices is placed at the throw of each path in a multi-pole switch in order to bring the node to ground when the series path is *off*, hence the shunt path conducts as the series path isolates. This improves isolation by grounding the series path when *off*. When the series path is *on*, the shunt path is turned *off*, adding a small parasitic capacitance associated with the stacked devices.

In this section, 1-, 2- and 4-stack series switches of 1, 2 and 4 mm width are compared across multiple settings of gate and body bias. 3.3 V and 5.0 V devices are measured, including more compact versions for evaluating improved performance. These building blocks are compared on 50 Ω and 1 kΩ substrate for the exact same layout footprint in an experimental version of GlobalFoundries BiCMOS 5PAe, eventually developed into GlobalFoundries BiCMOS 5PAx. At the end, a full switch design is presented for a single-pole double-throw switch (SPDT).

Much of this section speaks for itself. If an application can find use for these performance points, the implementation decision would be reduced to a cost comparison with other technologies. For the purpose of research endeavors, the benefit of high-resistivity substrate is clear. The 1 kΩ versions have advantages in insertion loss with no significant trade-off with isolation. Advantages in linearity should also exist, but the results of this investigation were inconclusive, possibly due to bond wire effects.

Table 6.1: Cellular band performance for a 5 V 4-stack SPDT with 4 mm series FETs and 1 mm shunt FETs

Frequency (MHz)	Substrate (Ω)	Insertion Loss (dB)	Isolation (dB)
915	50	0.78	39.03
915	1000	0.47	38.15
1850	50	1.17	31.58
1850	1000	0.69	31.55

Table 6.2: Cellular band performance for a 3.3 V 4-stack SPDT with 4 mm series FETs and 1 mm shunt FETs

Frequency (MHz)	Substrate (Ω)	Insertion Loss (dB)	Isolation (dB)
915	50	0.73	41.00
915	1000	0.43	37.70
1850	50	1.12	32.04
1850	1000	0.66	32.82

The 5 V device had better harmonic performance (lower power in the second and third harmonic), but the 3.3V device had poor third harmonic performance for the 1 kΩ substrate. Table 6.1 compares substrate usage for a 5 V 4-stack SPDT with 4 mm series FETs and 1 mm shunt FETs. The comparison is made at two cellular band frequencies (915 MHz and 1850 MHz). A 3.3 V version is tabulated in Table 6.2. To show the effect of reducing the series FET width, a 2 mm series FET (using the 5 V device) is tabulated in Table 6.3. Isolation and insertion loss for various stacked FETs are shown in the subsequent figures for the 5 V and 3.3 V devices for both the 4 mm and 2 mm widths.

Table 6.3: Cellular band performance for a 5 V 4-stack SPDT with 2 mm series FETs and 1 mm shunt FETs

Frequency (MHz)	Substrate (Ω)	Insertion Loss (dB)	Isolation (dB)
915	50	0.81	48.50
915	1000	0.52	49.50
1850	50	1.13	39.21
1850	1000	0.67	36.10

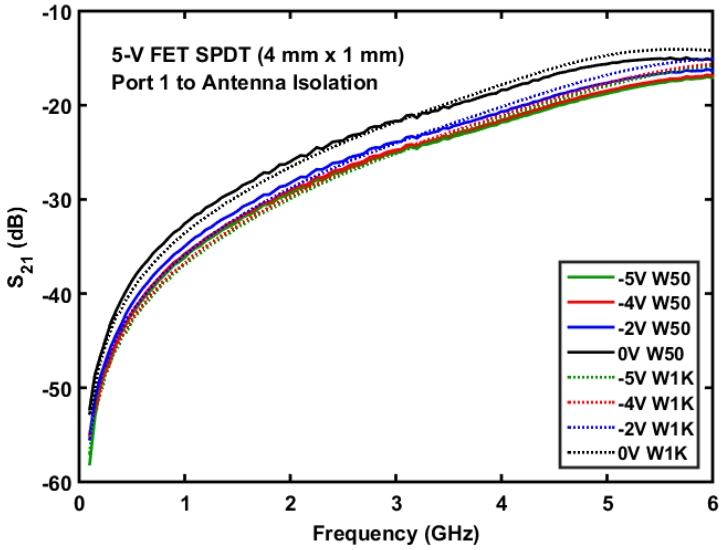

Figure 6.3: Isolation for a 4-stack, 4 mm 5 V FET across p-well bias conditions for 50 Ω and 1 kΩ substrate resistivity.

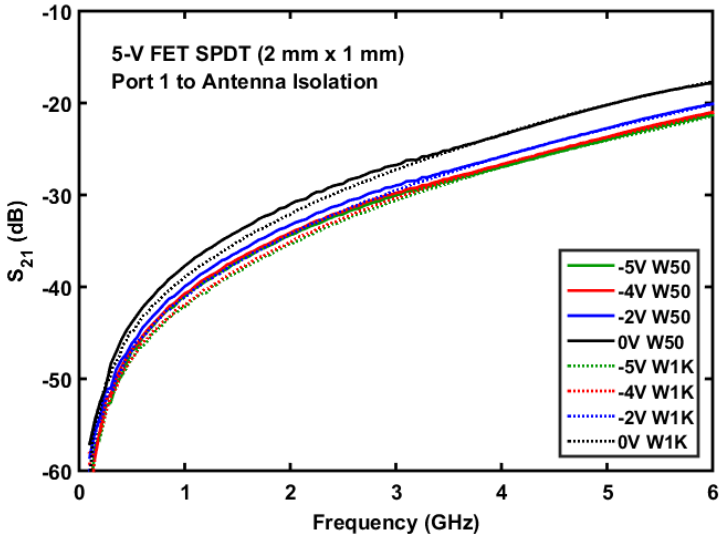

Figure 6.4: Isolation for a 4-stack, 2 mm 5 V FET across p-well bias conditions for 50 Ω and 1 kΩ substrate resistivity.

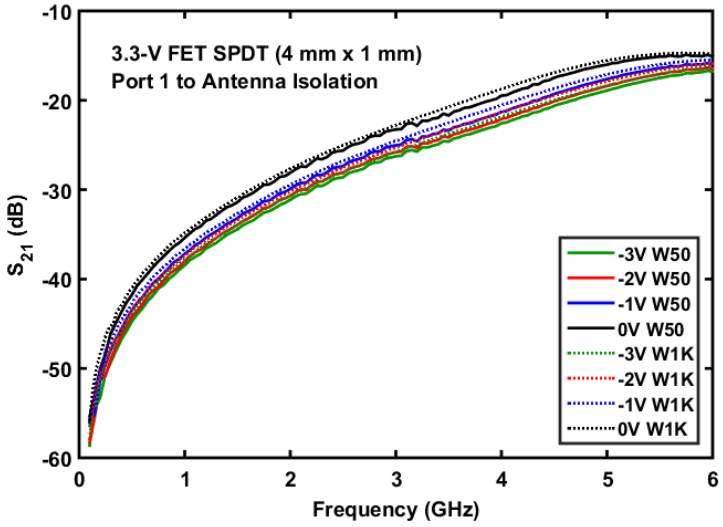

Figure 6.5: Isolation for a 4-stack, 4 mm 3.3 V FET across p-well bias conditions for 50 Ω and 1 kΩ substrate resistivity.

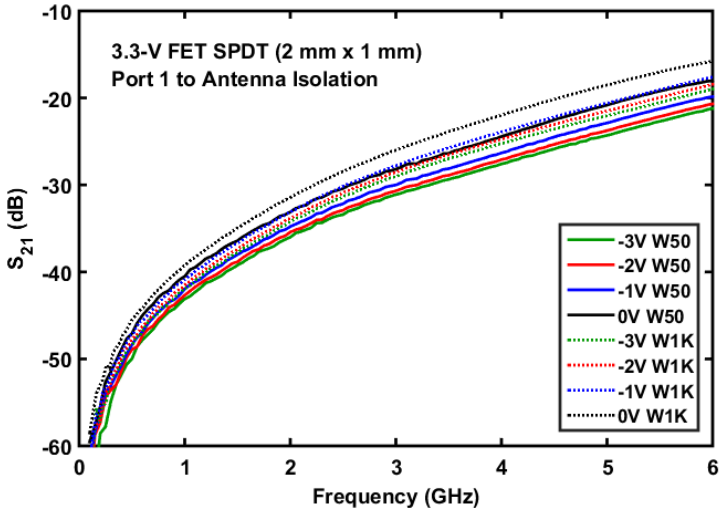

Figure 6.6: Isolation for a 4-stack, 2 mm 3.3 V FET across p-well bias conditions for 50 Ω and 1 kΩ substrate resistivity.

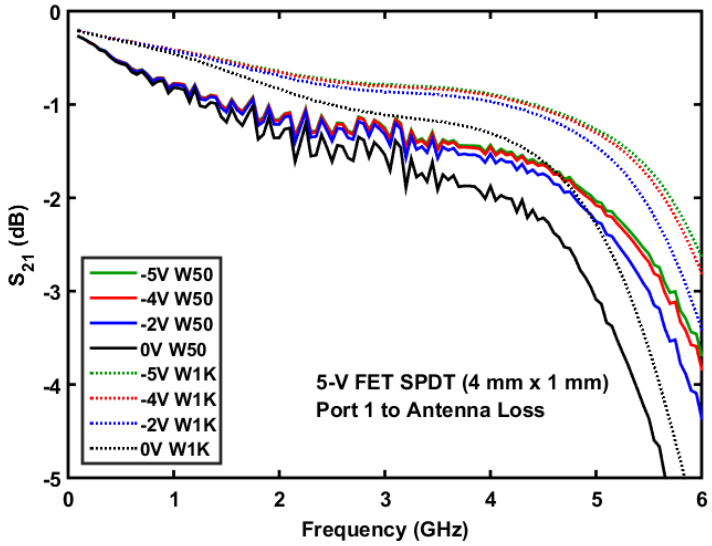

Figure 6.7: Insertion loss for a 4-stack, 4 mm 5 V FET across p-well bias conditions for 50 Ω and 1 kΩ substrate resistivity.

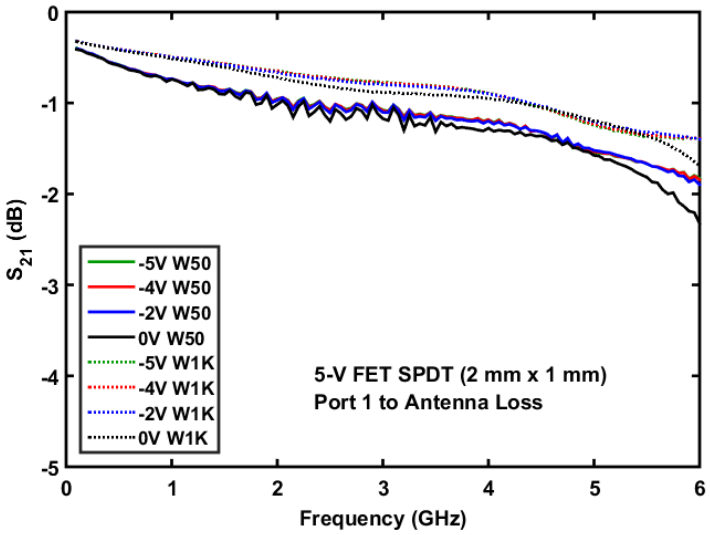

Figure 6.8: Insertion loss for a 4-stack, 2 mm 5 V FET across p-well bias conditions for 50 Ω and 1 kΩ substrate resistivity.

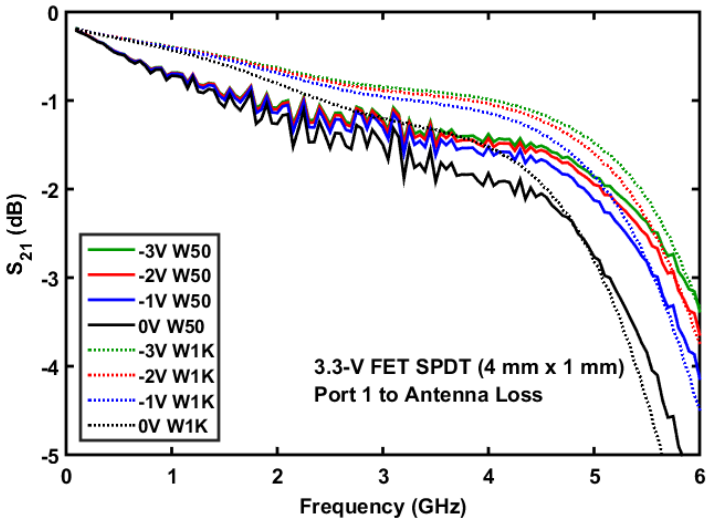

Figure 6.9: Insertion loss for a 4-stack, 4 mm 3.3 V FET across p-well bias conditions for 50 Ω and 1 kΩ substrate resistivity.

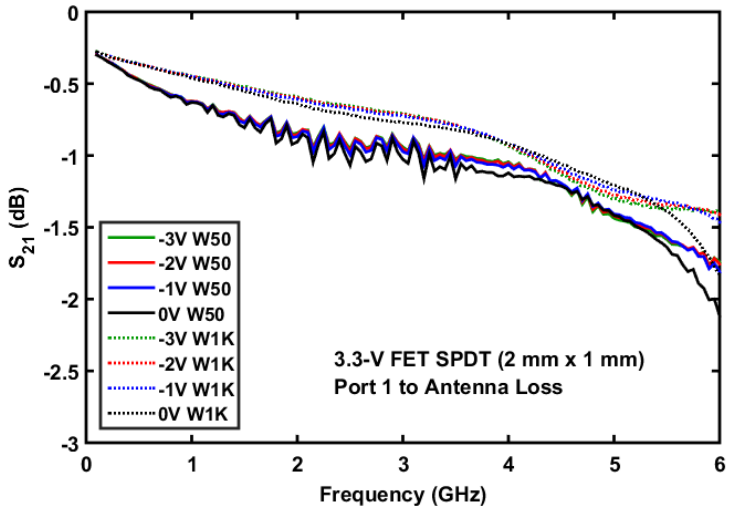

Figure 6.10: Insertion loss for a 4-stack, 2 mm 3.3 V FET across p-well bias conditions for 50 Ω and 1 kΩ substrate resistivity.

6.3 Switched-Base SiGe HBT Power Cores

This section explores the practicality of resizing watt-level power amplifier cores by switching unit cell SiGe HBT base terminals *on* and *off* with series NFETs (see Figure 6.11). This topology simultaneously provides low power modes of operation and thermal longevity with respect to aluminum electromigration failures along the

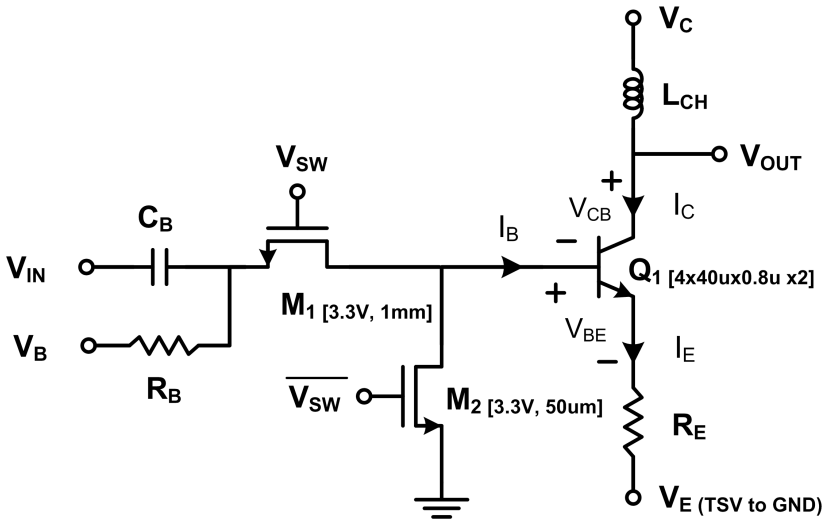

Figure 6.11: Schematic of base-switched HBT unit cell with shunt FET for breakdown protection.

emitter stripes. Thermal performance is improved by maximizing the distance between the activated transistors under average operating conditions, while a minimal footprint is maintained for the overall core necessary to accommodate high peak-to-average ratio signals. Breakdown of the *off*-state transistors is of particular concern in this configuration, suggesting the necessity of shunt switching at the base, and a simulation comparison with this alternate topology is briefly discussed. To account for the impact on input and output impedance, a tunable capacitor network is evaluated in the next section.

6.3.1 Introduction

A power amplifier (PA) designed for mobile handset applications must meet strict performance and product lifetime standards at a competitive cost. Although dominated by the relatively high power density GaAs and GaN PA, handset applications have been the objective of extensive research efforts in CMOS and SiGe BiCMOS, due to the cost benefits of these technologies, as well as the promise of fully integrated multi-band transceivers. Solutions that have been proposed for SiGe BiCMOS primarily use aluminum (Al) back-end-of-line (BEOL) solutions [36], making electromigration (EM) evaluation an essential part of product development. To mitigate EM failures at the emitter stripes and increase mean-time-to-failure (MTF) for SiGe HBT solutions, power cores are often designed with significantly increased emitter width, utilizing additional devices in parallel, which in turn decreases the quiescent current density within each device. Nonetheless, compact cell-to-cell spacing necessary for minimized periphery exacerbates thermal stress on innermost transistor cells, decreasing MTF, as shown in Chapter 5. This decrease in quiescent current density also operates the devices well below peak unity gain frequency (f_T) levels for which transistors are generally optimized, impinging more on gain as the technology node is applied to higher frequencies, thus limiting reliable application. Resistive ballasting at the

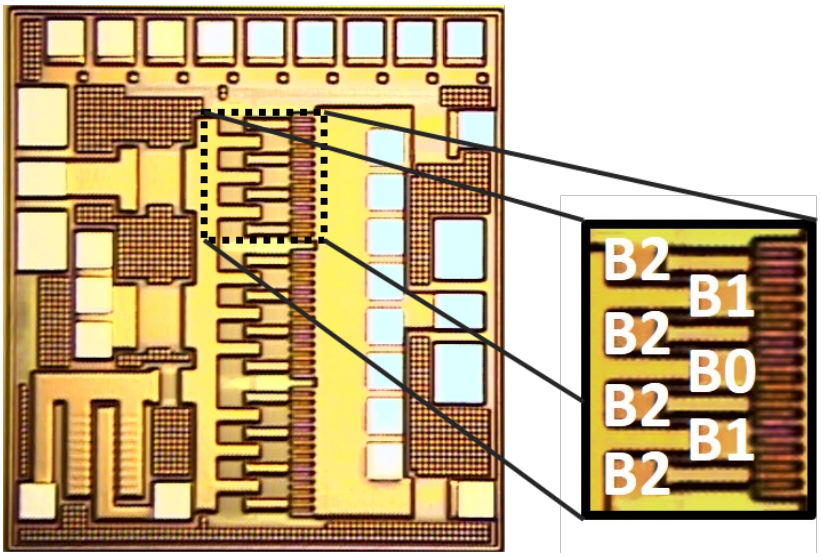

Figure 6.12: Die photo of an eight-state base-switched SiGe HBT power cell in IBM 5PAe BiCMOS. The three-bit control incorporates 3, 6 and 12 equally spaced unit cells, without the shunt breakdown protection FET.

emitter may also be employed to combat thermal effects, which further reduces overall gain.

With this backdrop in view, this work explores EM mitigation in SiGe HBTs by reducing cell-to-cell heating effects through cell separation during average power operation, while maintaining a minimal power core footprint still large enough to handle peaking events resultant from high peak-to-average power ratio (PAPR) signals. This separation is achieved by series NMOS switch FETs at the base of unit cells (Figure 6.11) within the core. Resizing necessitates 3-bit tunable capacitor networks (in the next subsection) for adjusting impedance to counterbalance virtual resizing of the core.

For all designs discussed herein, IBM BiCMOS 5PAe/5PAx, including options for through-silicon-via (TSV) and 1k substrate, is used. A custom triple-well NFET with improved contact pitch is also incorporated in this work.

6.3.2 Topology Implementation

Before designing a matched PA with base-switched HBTs (Figure 6.12) in the core, it is important to understand the reliability and practical benefits of this revised topology. For example, without the shunt switching device, the high input impedance provided by the series switch begins to breakdown those devices. Specifically, the series switch prevents base current reversal and thus severely limits safe DC operation to the open base breakdown voltage, BV_{CEO}, as opposed to the significantly higher open emitter breakdown voltage limit, BV_{CBO}, normally constricting SiGe HBT PA operation. Hence, a relatively small shunt switch at the base terminal can be activated in opposition to the series NFET to solve this problem.

Downsizing the core is achieved by setting equidistant series FETs to the off-state, depriving the associated HBTs of base current necessary for operation (refer to Figure 6.12). The impact of EM failures is mitigated by cell separation and by rotating usage across the full cell. In Chapter 5, the complexity of leaving a few devices on in a shared-subcollecto array was explored, and the mutual heating effects were shown to be minimized by spacing devices at least four apart. Typically, back-off power requires a halving of the number of devices for each 3 dB of reduction, hence 6 dB would show benefits as every fourth device would be left *on*. Downsizing while simultaneously increasing current density can also recapture attainable gain as the SiGe HBTs are biased closer to peak f_T. This adjustment would theoretically allow a large 1 GHz 5PAe core to address 5 GHz, for example. Additionally, it should be noted that significant efficiency enhancements sought from downsizing also require reduced collector voltage.

In resizing the base-switched core and adjusting bias points, the input and output impedances are altered. For optimization purposes, tunable capacitor networks can be incorporated to adapt to these changes. Toward an integrated solution, the 3-bit switched capacitor network in the next section was developed.

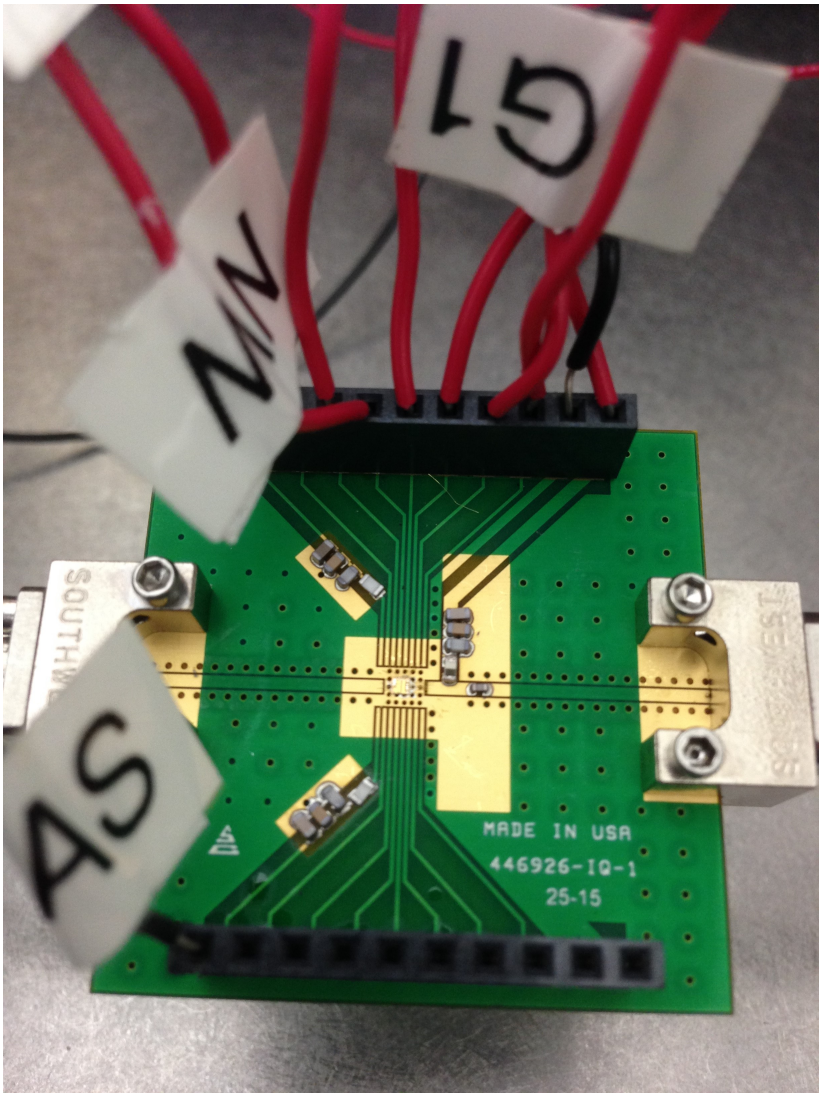

Figure 6.13: Photograph of the PCB for the switched-base amplifier load pull experiments.

6.3.3 Measurements

For large power cores, thermal as well as spatial factors often complicate first-pass simulation accuracy, hence PCB measurements characterizing the core itself (Figure 6.12) were performed across various configurations. The PCB is shown in Figure 6.13. During the measurement process, a fatal flaw was discovered in the original inception of the core, for there was no shunt switch to protect against breakdown in this solution, and therefore the devices did not survive load pull tuning, and therefore only data for

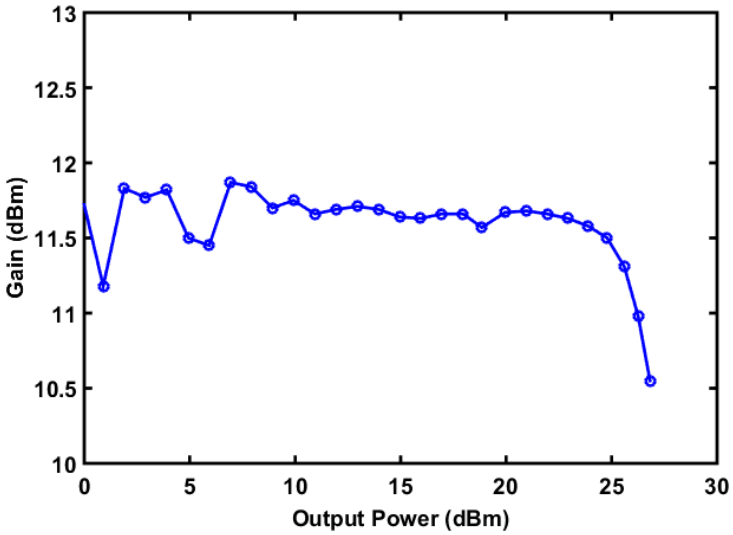

Figure 6.14: Gain vs. output power for the matched switched-base amplifier, with all devices *on*.

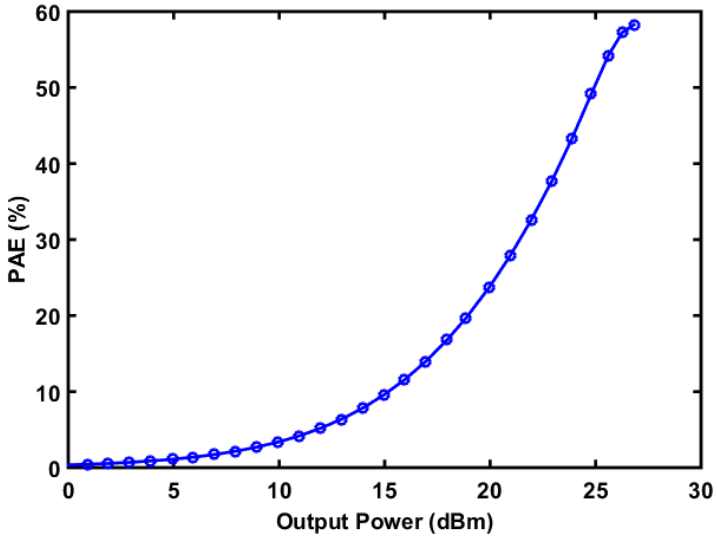

Figure 6.15: PAE vs. output power for the matched switched-base amplifier, with all devices *on*.

the core as a whole was taken. Figure 6.14 shows the gain of the full cell, for a best power output match on the load and source tuners. Figure 6.15 gives the power added efficiency (PAE). Future tapeouts were completed but never made it to fabrication due to lack of space on 5PAe on multi-project wafer runs, so this investigation is left for future work. Nonetheless, the structure, if eventually made reliable, would require

tunability, which will be discussed in the next section.

6.4 Programmable Arrays of Capacitors (PACs)

Programmable arrays of capacitors (PACs) in SOI can be successfully employed for antenna tuning applications or dedicated tunable matching networks [90–92]. Similar techniques are used on bulk silicon processes to incorporate tunable matching on the PA die itself [48, 93]. With access to hi-res substrates, and the benefits outlined in the previous subsections, an examination of hi-res PACs is the logical next step in implementation. This subsection looks at data from 3-bit, compact PACs for interstage matching, using 2-stack 1 mm FETs on 50 Ω and 1 kΩ substrates. A die photo and schematic are presented in Figure 6.16.

Figures 6.17 and 6.18 show an unexpected result in the calculated quality factor (Q) for the PACs studied in this work. The Q for the 1 kΩ substrate should show better performance, but actually has a worse Q when compared to 50 Ω substrate. The only difference in the designs, since both layouts are exactly the same, comes in the application of a negatively masked protection layer which surrounds the entire circuitry. This protection layer, to the best of our knowledge, is used to mask the

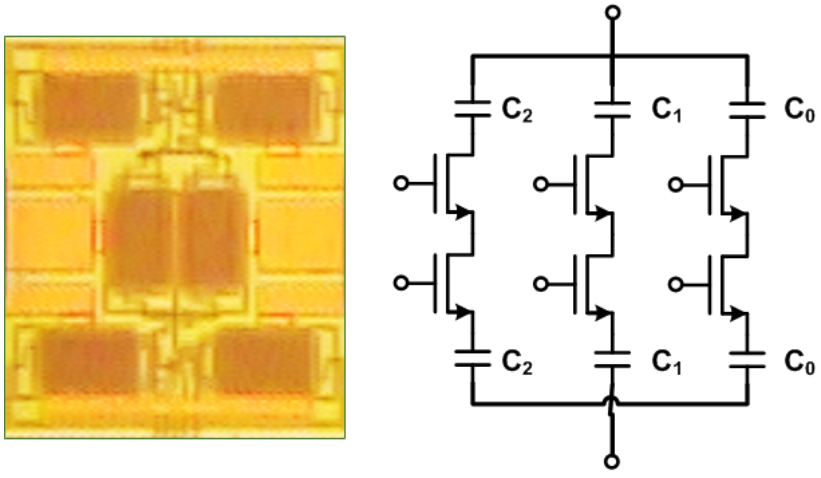

Figure 6.16: Die photo and schematic from a 3-bit minimal resolution switched capacitor network.

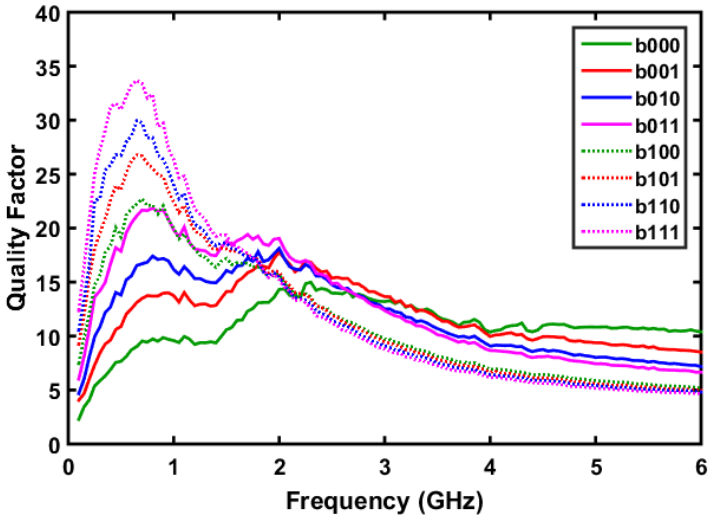

Figure 6.17: 3-bit capacitor Q as a function of frequency on 50 Ω substrate.

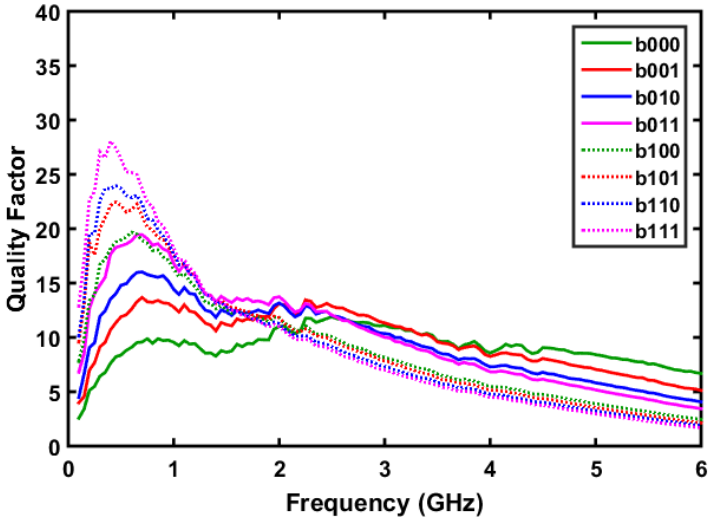

Figure 6.18: 3-bit capacitor Q as a function of frequency on 1 kΩ substrate.

hi-res correction implant that makes the top surface of the substrate look like 1 kΩ. It can be conjectured that the hi-res interface with the dielectric in the BEOL is contributes to loss, hence this layer must be used beneath passive circuitry to maintain the benefits of the hi-res substrate. As this correction layer must not be implanted over the actives, there is an extension of the keep-out region created by this mask well outside of the FETs used in the PAC (faintly apparent in Figure 6.19).

In the versions documented here, this layer is also under the capacitors and

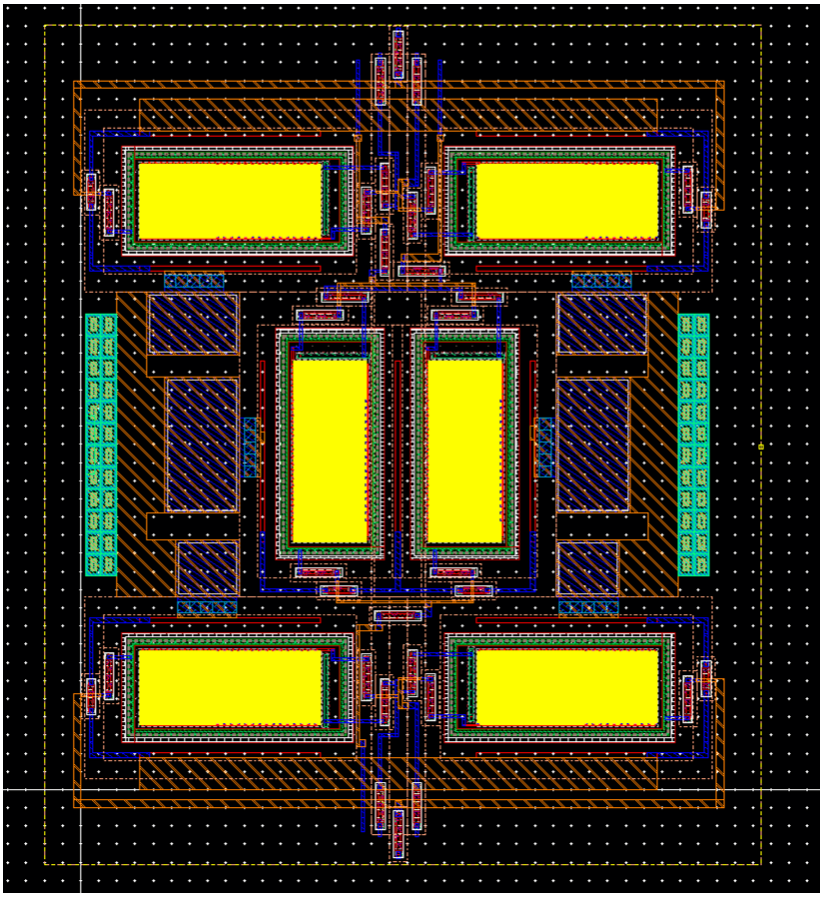

Figure 6.19: A 3-bit compact PAC layout showing the hi-res keep-out layer surrounding all of the structure, which degrades Q for the 1 kΩ structure.

interconnects used in the PAC, possibly causing the reduction in Q.

Another issue with the original design is an uneven distribution in capacitance. Fig 6.23 walks through a derivation for achieving even capacitance for the tight-pitched switch (TPS) FET in the 5PAx design kit. This is achieved by including the contributions of each FET to the overall capacitance, as shown in Figures 6.20, 6.21 and 6.22. This math can be extended to create specific capacitance levels for a particular design, perhaps for multi-band or multi-mode operation.

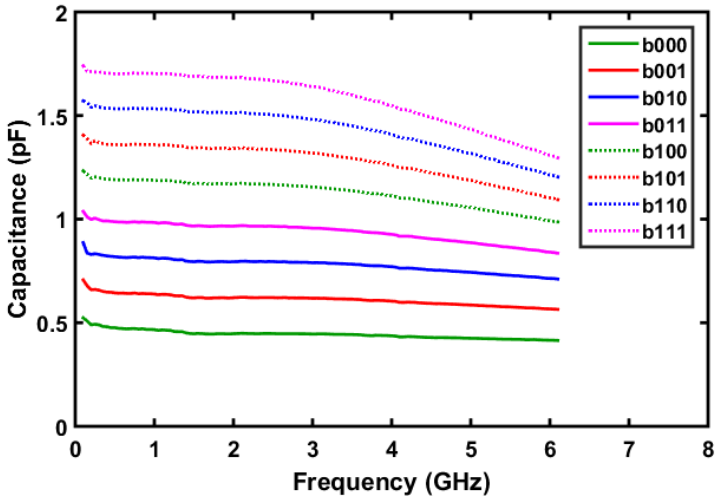

Figure 6.20: 3-bit capacitance as a function of frequency for PAC version A on 50 Ω substrate.

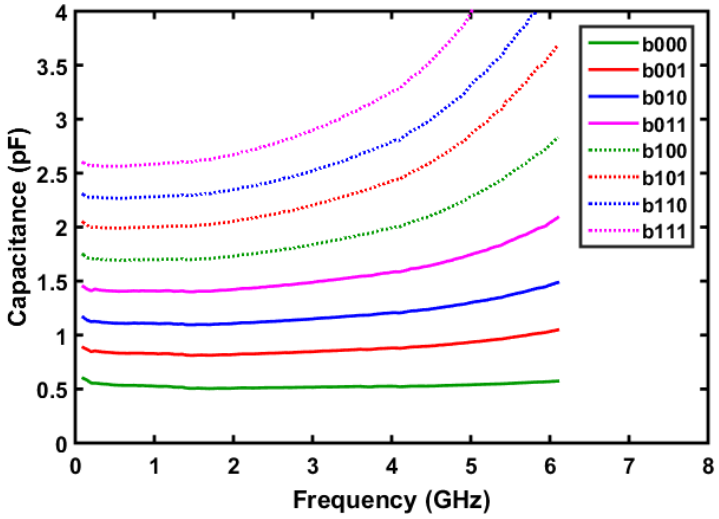

Figure 6.21: 3-bit capacitance as a function of frequency for PAC version B on 50 Ω substrate.

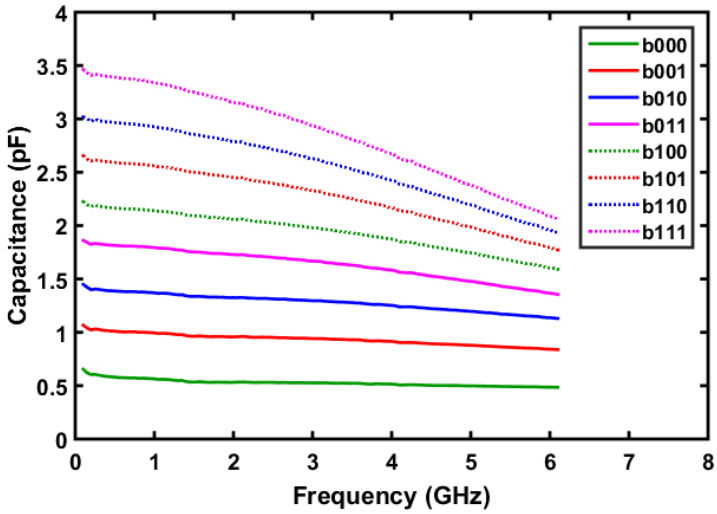

Figure 6.22: 3-bit capacitance as a function of frequency for PAC version C on 50 Ω substrate.

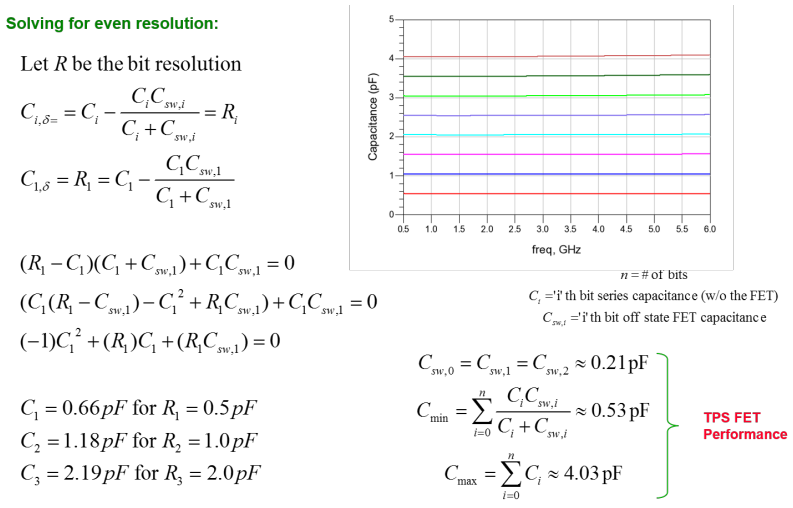

Figure 6.23: Derivation and simulation of an even capacitance distribution for a 3-bit PAC in 5PAx.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Reliability Guidelines for RF Circuit Designers

There are several conclusions the RF circuit designer can take from this work.

1. The forward transit current is a more pertinent visualization tool than the simulated collector current.

2. The crucial breakdown voltage for a cascode PA design with low base resistance (around 10 Ω) on the common-base device will be BV_{CBO}, and the collector-base bias should remain below half that value for third-generation SiGe HBT devices to protect against electromigration.

3. The crucial breakdown voltages for a design with high base resistance (around 500 Ω) will be BV_{CEO}, in order to protect against electrothermal instability.

4. If no current flows through the SiGe HBT when the voltage swings above breakdown, then reliability will be limited by electromigration, not thermal runaway, since the circuit is self-protected against an increase in internal temperature.

5. Current flow will rapidly avalanche above BV_{CBO}, and although this will not necessarily cause thermal runaway at breakdown under RF operations, it is an unreliable method for PA designs if the PA is not *off* for a large portion of the swing. Additionally, electromigration will accelerate and circuit lifetime will diminish.

6. The limiting quantity for input power handling in SiGe HBT LNAs is BV_{EBO}. Large negative swings beyond breakdown accelerate damage, causing gain and noise figure degradation.

7. Although it is very difficult to simulate large negative swings due to convergence issues, measurements have shown that 8HP SiGe HBT LNAs suffer 0.2-0.4 dB NF degradation and 2 dB gain degradation at high levels of input stress.

8. More aggressive damage accrual occurs at 18 dBm input power for the typical 8HP SiGe HBT LNA, assuming the aforementioned guidelines in reference to breakdown are observed. Typically, these LNAs can handle 1 W of input power, although electromigration effects must also be considered.

9. High-impedance bias circuitry in concert with an avalanching gain device can severely reduce power handling and worsen soft breakdown effects in a cascode LNA. The common-base SiGe HBT's base voltage should be set to a diode voltage above BV_{CEO} as a maximum value, lower if the upper device's base terminal also has a large impedance.

10. TCAD analysis is useful in determining internal device temperatures that lead to hard breakdown. It has been shown that capacitive currents in a SiGe HBT do not contribute to hot-carrier damage, and RF operation leads to less damage than *dc* operation.

11. Shared-subcollector SiGe HBT power arrays have an uneven temperature profile that can shift with process variations. If intended for resizing, the structure used in this work can identify issues related to thermal instability. Devices should be turned *on* with equal spacing, and outer devices should not be used in isolation.

12. The effectiveness of switched capacitor circuits may be limited on high-resistivity substrates, due to the impact of loss created at the substrate-dielectric interface.

Care should be taken during implementation, as quality factor can differ widely from simulation.

7.2 Contributions

Contributions in the field of SiGe HBT design for reliability are enumerated in this section.

1. Simulation techniques were discovered for separating capacitive currents from a SiGe HBT load line and the application to reliability analysis.

2. The first investigation of RF stress in TCAD for SiGe HBT cascode PAs was performed, opening the door for more advanced research in RF TCAD.

3. The reliability of SiGe HBT PA designs that swing above breakdown (BV_{CBO}) was verified, and the results were analyzed to provide RF circuit designers the tools necessary to bias devices more aggressively without sacrificing reliability.

4. Thermal analysis of flip-chip cooling via copper pillars was performed, leading to PA implementations in cellular electronics.

5. The analysis of soft and breakdown in third-generation SiGe HBT LNAs as related to increasing RF input stress was performed, identifying the maximum input power ruggedness as a function of bias impedance.

6. TCAD analysis methods for evaluating RF hard breakdown for any SiGe HBT circuit were set forth.

7. The feasibility of switched-base power cores on high-resistivity substrates was explored by examining stacked switches in a developing first-generation SiGe HBT process that was designed for front-end applications.

8. Mutual heating analysis of shared-subcollector SiGe HBT power cores was completed, identifying the complexity of thermal interactions between devices.

7.3 Suggested Future Work

Future work in this field requires more advanced TCAD modeling. Primarily, factors effecting linearity and noise should be identified. This work lays the foundation for those investigations, as decks have been created to analyze the lattice temperature's impact on RF swing.

The next logical step would be for research to step forward from two-dimensional TCAD to three-dimensional representations. The difficulty in this work would be the simulation time required. Simplifications must be made, and their impact on simulation results must be shown to introduce insignificant error. Meshing and thermal boundary conditions will take a great deal of effort, but this is valuable work to pursue.

In reference to mutual heating, this needs to be extended to trench-isolated cascode devices for higher-frequency applications. Hardware for doing this has been fabricated, and this would be an easy follow-up to the paper submitted on this topic.

Evaluation of switched-base amplifiers can be pursued, but it is more likely viable if the output network is in a separate technology where loss in the tunable matching networks can be minimized.

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VITA

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