SYSTEMATIC ANALYSIS OF THE SMALL-SIGNAL AND BROADBAND NOISE PERFORMANCE OF HIGHLY SCALED SILICON-BASED FIELD-EFFECT TRANSISTORS

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SYSTEMATIC ANALYSIS OF THE SMALL-SIGNAL AND BROADBAND NOISE PERFORMANCE OF HIGHLY SCALED SILICON-BASED FIELD-EFFECT TRANSISTORS

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To my beloved parents

and

my grandfather ...

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SUMMARY

The objective of this work is to provide a comprehensive analysis of the small-signal and broadband noise performance of highly scaled silicon-based FETs, and develop high-frequency noise models for robust radio frequency circuit design. An analytical RF noise model is developed and implemented for scaled Si-CMOS devices, using a direct extraction procedure based on the linear two-port noise theory.

This research also focuses on investigating the applicability of modern CMOS technologies for extreme environment electronics. A thorough analysis of the DC, small-signal AC, and broadband noise performance of 0.18 μm and 130 nm Si-CMOS devices operating at cryogenic temperatures is presented. The room temperature RF noise model is extended to model the high-frequency noise performance of scaled MOSFETs at temperatures down to 77 K and 10 K. Significant performance enhancement at cryogenic temperatures is demonstrated, indicating the suitability of scaled CMOS technologies for low temperature electronics. The hot-carrier reliability of MOSFETs at cryogenic temperatures is investigated and the worst-case gate voltage stress condition is determined. The degradation due to hot-carrier-induced interface-state creation is identified as the dominant degradation mechanism at room temperature down to 77 K. The effect of high-energy proton radiation on the DC, AC, and RF noise performance of 130 nm CMOS devices is studied. The performance degradation is studied up to an equivalent total dose of 1 $Mrad$, which represents the worst case condition for many earth-orbiting and planetary missions.

The geometric scaling of MOSFETs has been augmented by the introduction of novel FET designs, such as the Si/SiGe MODFETs. A comprehensive characterization and modeling of the small-signal and high-frequency noise performance of highly

scaled Si/SiGe n-MODFETs is presented. The effect of gate shot noise is incorporated in the broadband noise model. SiGe MODFETs offer the potential for high-speed and low-voltage operation at high frequencies and hence are attractive devices for future RF and mixed-signal applications.

This work advances the state-of-the-art in the understanding and analysis of the RF performance of highly scaled Si-CMOS devices as well as emerging technologies, such as Si/SiGe MODFETs. The key contribution of this dissertation is to provide a robust framework for the systematic characterization, analysis and modeling of the small-signal and RF noise performance of scaled Si-MOSFETs and Si/SiGe MODFETs both for mainstream and extreme-environment applications.

CHAPTER I

INTRODUCTION

1.1 A Brief History of Radio

"Stay connected" is the motto of today's information age. Information interchange plays a pivotal role in our everyday life. Several technologies such as telephony, wireless and optical networks, internet, and satellite communication have revolutionized the way we communicate. The modern day world is built on a robust communication infrastructure that is inextricably linked to these technologies to facilitate the seamless exchange of information in the form of speech, text, data, images, audio, and video.

In 1844, Samuel F.B. Morse successfully demonstrated the first electrical communication over a long distance by transmitting a "dot-dash" message over a single wire that connected the entities involved in the information exchange. The development of the Morse code led to the establishment of telegraph systems. This was soon followed by the invention of telephone by Alexander Graham Bell, which made distant audio communication possible. Heinrich Hertz's experimental demonstration of the existence of electro-magnetic (EM) waves established the basis for wireless communication. However, it took several years for wireless technology to be deployed for long-distance communication. In 1901, Guglielmo Marconi successfully demonstrated the transatlantic transmission of wireless signals with the help of J.C. Bose's "mercury coherer with a telephone" detector. This revolutionary experiment ushered in the age of radio. These early systems employed spark-gap transmitters and detectors for low-frequency long-distance communication. The invention of vacuum tubes and

their application as receivers and sources of EM energy in transmitters was instrumental in the development of high-frequency and microwave radios [1]-[4]. Since their inception, microwave radio systems have undergone several significant improvements over the years. The invention of the point-contact transistor by John Bardeen, Walter Brattain, and William Shockley in 1947, followed by the development of commercial silicon (Si) transistors by Texas Instruments in 1954, coupled with the advances in information theory, have facilitated the realization of affordable mobile communication systems. Today, the wireless technology market spans some important existing and emerging applications, such as mobile telephony, wireless local area networks (WLAN), radio frequency identification systems (RFIDs), radar and remote sensing, medical electronics, and intelligent transportation systems. The Federal Communications Commission (FCC) was established to ensure the efficient and effective use of the radio spectrum for various applications. The need for ubiquitous access to information is constantly driving the next-generation wireless communication technologies and has created the need for using higher-frequency carrier waves with proportionally increased modulation bandwidths. The restricted band allocation by the FCC for various applications has made it necessary to transmit more information in a limited spectrum. The need for achieving higher data rates has necessitated the use of highly complex signal modulation and multiplexing schemes in modern communication systems, thereby placing a stringent requirement on the performance of devices and circuits used for building the next-generation wireless systems.

Performance, cost, size, power consumption, and time to market are the main factors that influence the choice of device technology for radio frequency (RF) circuits. In addition to these parameters, high-density integration capability is very desirable to build smaller and faster systems that are cost effective and efficient. Modern complementary metal-oxide-semiconductor (CMOS) technologies have emerged as a strong contender for building RF integrated circuits (ICs) for myriad of commercial

and niche applications.

1.2 Evolution of Silicon CMOS Technology and its Application Space

In 1930, Lilienfeld patented the idea of surface conductance modulation of a semiconductor by the application of an electric field. The fundamental concept of surface states and conductance modulation of a surface inversion layer was suggested by Bardeen and Brattain. The n-type surface inversion layer on p-type Si and the p-type surface inversion layer on an n-type germanium (Ge) were the principal reasons for the successful operation of the field-effect point-contact transistors invented by Bardeen and Brattain in 1947. However, early attempts to fabricate a field-effect transistor were not successful because of the presence of large densities of surface states, which shielded the surface potential from the influence of an external field. In 1960, Kahng and Attala successfully fabricated the first metal-oxide-semiconductor field-effect transistor (MOSFET) on a Si substrate with silicon dioxide (SiO_2) as the gate dielectric. Figure 1 shows the photograph of the first Si-MOSFET [5], [6]. A major breakthrough in the level of integration came in 1963 with the invention of CMOS technology by Wanlass and Sah [7]. Since then CMOS technology has played a pivotal role in the development of high-density ICs, such as memory modules, logic chips, and microprocessors.

In 1974, Robert Dennard, and his team from IBM proposed the concept of constant field scaling of MOSFETs and pointed out that scaling of supply voltages along with the lithographic dimensions could achieve improvements in speed, power, and component density [8]. Remarkable improvements in optical lithography and manufacturing technology, coupled with the ever increasing need for aggressive performance, have fueled the rapid scaling of CMOS technology. Over the past few decades, the minimum feature size (gate length) of MOSFETs has decreased exponentially from micrometers well into the nanometer regime. Figure 2 illustrates the

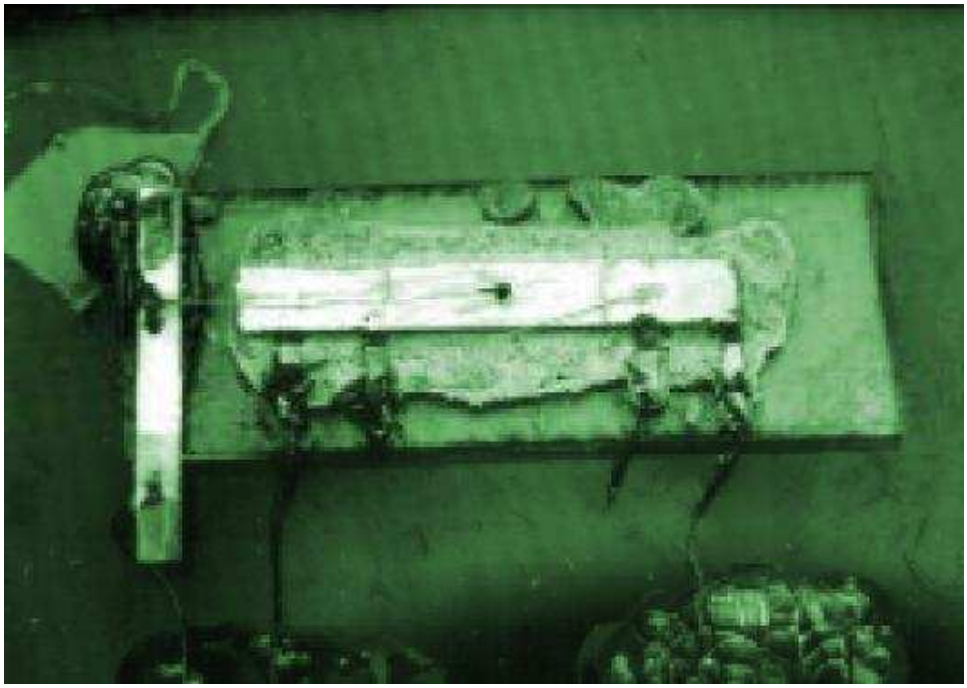


Figure 1: Photograph of the first Si-MOSFET fabricated by Kahng and Atalla in 1960.

scaling of gate lengths and operating voltages of CMOS technologies over the years [9]. The scaling of gate length and gate-oxide thickness (t_{ox}) has led to an increase in the drive current and transconductance (g_m) of MOSFETs.

Traditionally, CMOS devices were considered suitable for digital and low-frequency analog applications. However, the rapid scaling of MOSFET gate lengths has resulted in a strong improvement in the RF performance of CMOS devices. The peak cut-off frequency (f_T) of state-of-the-art CMOS technologies is well over 100 GHz, thus enhancing the useful operating frequency range of scaled CMOS devices. Scaling also has a favorable impact on the broadband noise performance of MOSFETs. As shown in Fig. 3, the modern CMOS devices exhibit a peak-f_T greater than 100 GHz and a sub-1.0 dB minimum noise figure (NF_{min}). The significant improvement in the RF performance coupled with the high levels of integration and cost effectiveness have made Si-CMOS the technology of choice for the development of RF ICs and system-on-chip (SOC) solutions for various wireless applications. Several foundries provide

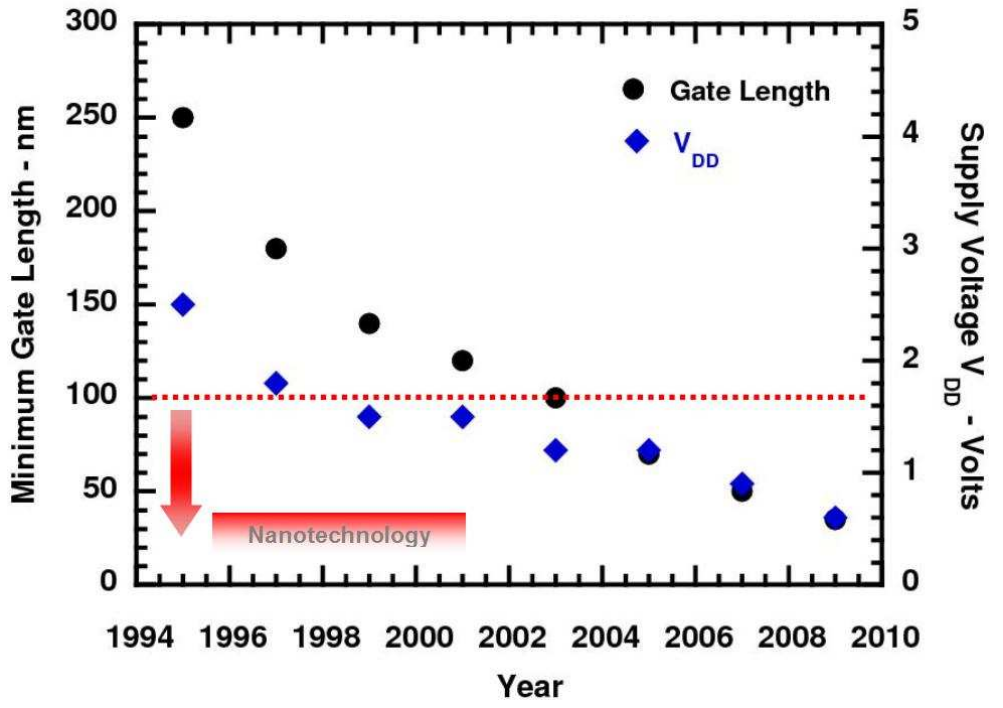


Figure 2: Scaling of minimum gate-length and supply voltage (V_{DD}) of CMOS technologies over the years.

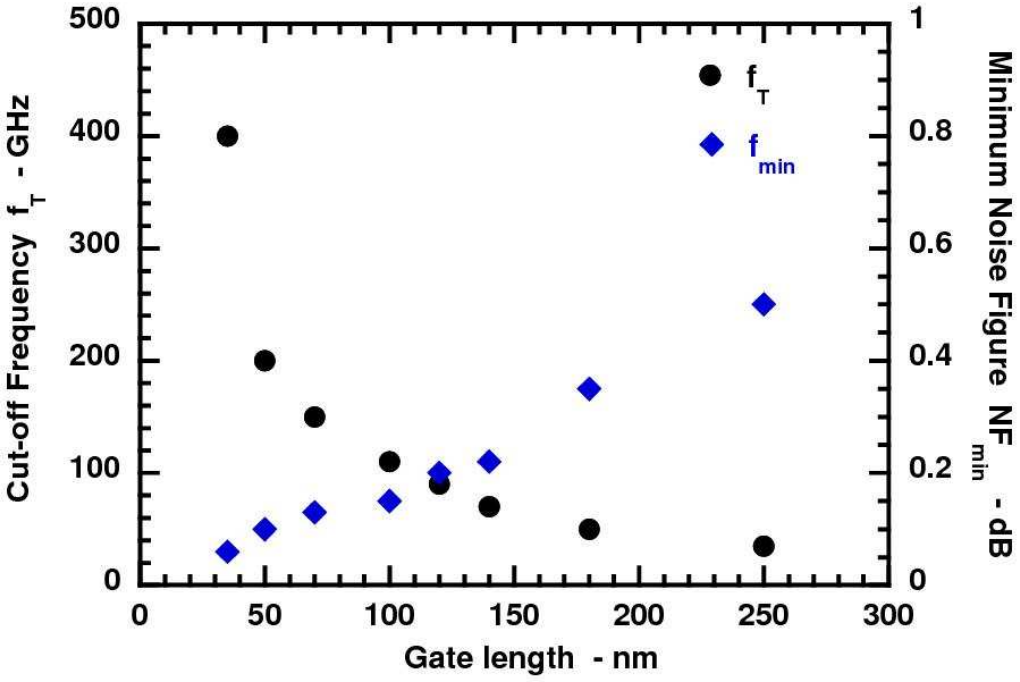


Figure 3: Cut-off frequency (f_T) and minimum noise figure (NF_{min}) versus gate-length.

high-performance RF CMOS technologies that include high gain RF CMOS devices along with passive components like inductors, varactors, and capacitors [10]–[16].

In addition to device scaling, technological innovations and novel integration approaches are being employed to enhance the performance of mainstream CMOS devices. Silicon germanium (SiGe) heterostructure technology using strained-Si and SiGe epi-layers has recently attracted substantial attention as it improves the performance of Si-based FETs by achieving higher carrier mobility and thereby opens up the possibility of employing SiGe modulation-doped FETs (MODFETs) for low-power RF applications. The need for superior performance has thus fostered active research in the field of Si-based FET device design and process optimization, high-frequency characterization and modeling of these devices, and circuit design for RF and microwave applications.

Today, Si-CMOS ICs and SOCs are widely used for several commercial applications that span both wireless and wired communication applications such as Bluetooth, IEEE 802.11 a/b/g WLANs, ultra-wideband (UWB) radios, synchronous optical networks (SONET), etc. Figure 4 shows the application space of modern CMOS technologies, that spans an entire gamut of wireless and wired communication applications and standards. In addition to the various commercial applications, there is an increasing interest in investigating the applicability of Si-CMOS devices for extreme-environment applications. Some of the important extreme-environment scenarios include operation at extreme temperatures and operation in a radiation-intense environment such as outer space. Extreme-environment electronics represents a class of important niche applications that spans deep-space electronics, radio astronomy, smart electronic systems for automobiles, semiconductor-superconductor hybrid systems, and high-sensitivity cooled sensors and detectors.

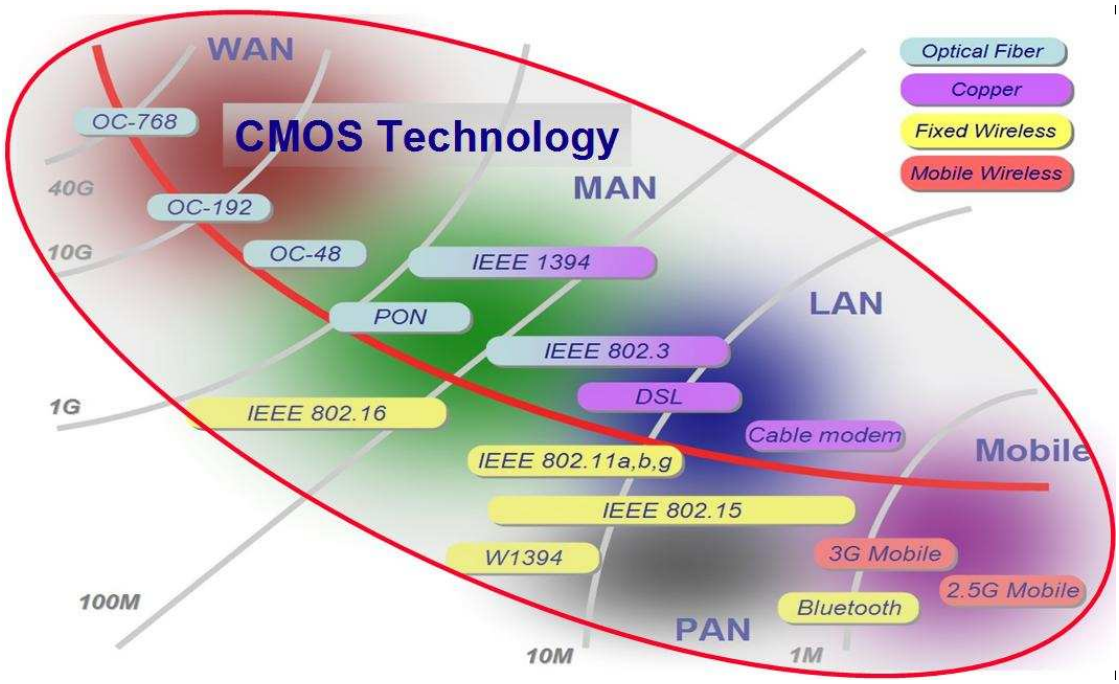


Figure 4: The application space of modern CMOS technologies (Courtesy Dr. Kyutae Lim).

1.3 Scope of the Dissertation

The aggressive scaling of CMOS technologies has resulted in a significant improvement in the RF performance of MOS devices. Consequently, CMOS radio transceivers and SOCs have been deployed in various commercial wireless communication applications that used to be traditionally dominated by the III-V technologies such as gallium arsenide (GaAs) and indium phosphide (InP).

The development of robust RF CMOS SOCs presents a host of challenges in the high-frequency characterization, modeling, and circuit design using scaled MOSFETs. Broadband noise is one of the main concerns in the design of low-noise RF front-ends, as it has a direct impact on the sensitivity of the receiver chain. A thorough characterization and modeling of high-frequency noise in MOSFETs is a prerequisite for the development of low-noise CMOS RF ICs. This work contributes to the ongoing research efforts aimed at developing accurate broadband noise models for scaled CMOS devices. The dominant sources of high-frequency noise in a MOSFET are the

channel thermal noise, the induced gate noise, and the thermal noise generated by the gate resistance. Scaled CMOS devices exhibit a higher channel thermal noise compared to the long-channel MOSFETs, and this increase is captured by introducing a parameter called the excess noise coefficient. The bias and channel-length dependence of the excess noise coefficient is still actively debated in the current literature. Widely used MOS compact models, such as the Berkeley short-channel insulated-gate FET (IGFET) model (BSIM), ignore the bias dependence of the excess noise factor, thereby causing inaccuracies in modeling the channel thermal noise. In this work, a direct extraction technique is used to determine the device noise sources from the measured noise parameters using the "noisy two port" analysis. The extracted noise sources are incorporated in a sub-circuit-based RF noise model. The evolution of the noise sources is studied as a function of bias and frequency, thereby providing a comprehensive analysis of the broadband noise performance of scaled Si-MOSFETs. The measurement and modeling results are presented for an nFET from a commercially available 130 nm CMOS technology. The impressive RF performance of the state-of-the-art Si-CMOS technologies also motivates the study of their performance in extreme environments in order to expand the application space of CMOS technologies to include these niche applications. This work encompasses a systematic investigation of the RF performance of scaled CMOS devices in two important extreme-environment scenarios, namely, 1) operation in a radiation-intense environment and 2) operation at cryogenic temperatures, down to liquid nitrogen (77K) and liquid helium (4K) temperatures. These conditions of operation are very relevant for electronic systems used in deep-space, radio astronomy, and high-precision instrumentation applications. This work is envisioned to provide a framework for the robust on-wafer RF characterization and modeling of scaled CMOS devices operating in the above-mentioned extreme-environment conditions. The room temperature noise model is extended to analyze the device noise performance at 77 K and 10 K. The hot-carrier reliability of

these scaled CMOS devices is investigated at cryogenic temperatures using DC stress techniques.

The geometric scaling of MOSFETs has been augmented by the introduction of novel FET designs, such as the Si/SiGe MODFETs. SiGe MODFETs offer the potential for high-speed and low-power operation at high frequencies and hence are attractive devices for future RF and mixed-signal applications. This work presents a systematic analysis of the small-signal and broadband noise performance of SiGe MODFETs.

1.4 Thesis Organization

The rest of the thesis is organized as follows:

Chapter 2 describes the fundamental high-frequency noise sources in MOSFETs and the basic concepts of noise figure and high-frequency noise parameters of a two-port device. The RF noise measurement system and methodology is described in detail.

Chapter 3 presents a technique for the direct extraction of the channel thermal noise, the induced gate noise, and the gate resistance thermal noise from measured RF noise parameters and scattering parameters (S-parameters). This technique is based on the linear two-port noise theory and can be applied to any two-port device. A sub-circuit-based RF noise model for MOSFETs is described, that is used to obtain the simulated noise parameters. The measurement and modeling results are presented for a 130 nm CMOS technology.

Chapter 4 discusses the operation of scaled CMOS devices at cryogenic temperatures, down to liquid nitrogen (77K) and liquid helium (4K) temperatures. The on-wafer cryogenic system is described in detail and the challenges of performing robust cryogenic measurements are outlined. A thorough DC, small-signal, and RF

noise characterization of 0.18 μm and 130 nm MOSFETs is presented. The room temperature noise model is extended to investigate the behavior of device noise sources in the cryogenic regime. The hot-carrier reliability of scaled MOSFETs is studied at cryogenic temperatures using DC stress measurements. This is necessary for understanding the dominant failure mechanisms at low temperatures and also to determine the worst-case bias conditions for hot-carrier degradation.

Chapter 5 discusses the effect of proton radiation on the RF performance of scaled CMOS devices. The total dose effects in MOSFETs are studied and the experimental results are presented for a 130 nm nFET irradiated by 63.3 MeV protons.

Chapter 6 presents the small-signal and broadband noise performance of SiGe MODFETs to explore the applicability of these novel band-engineered FETs for the development of RF and microwave ICs.

Chapter 7 summarizes the contributions of this dissertation and discusses the future work that this thesis could motivate.

CHAPTER II

FUNDAMENTALS OF NOISE AND HIGH-FREQUENCY NOISE MEASUREMENTS

In electronic systems, noise can be defined as any random interference unrelated to the signal of interest. The sensitivity of a communication system is limited by noise. The fundamental noise sources are inherent to the device or the system itself. This chapter describes the fundamental high-frequency noise sources in a MOSFET, and the measurement system and methodology used to characterize RF noise.

2.1 High-Frequency Noise in Scaled MOSFETs

The fundamental noise mechanism in MOSFETs is the thermal noise of the conducting channel [17]. Figure 5 illustrates the channel noise mechanisms in a MOSFET. The channel thermal noise is the dominant noise source and is generated by the ran-

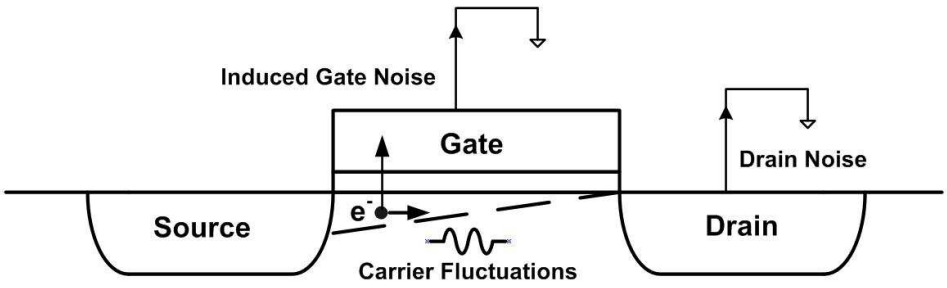


Figure 5: Cross-section of a typical MOSFET illustrating the channel noise mechanism.

dom thermal motion of charged carriers in the channel region at high frequencies. This channel thermal noise is detected at the drain terminal through the drain current fluctuation, and hence is also known as the drain current noise ($\overline{i_d^2}$). At high

frequencies, the channel thermal noise also manifests itself in the gate current spectrum owing to a significant capacitive coupling through the gate-oxide capacitance. This noise current is termed as the induced gate noise ($\overline{i_g^2}$). This induced gate noise is partially correlated with the drain channel noise, as they are generated by the same physical noise mechanism. Using Van der Ziel's theory [17], these noise sources can be expressed as

$$\overline{i_d^2} = 4kT\Delta f\ \gamma\ g_{do} \tag{1}$$

$$\overline{i_g^2} = 4kT\Delta f\ \beta\ \frac{\omega^2 C_{gs}^2}{5\ g_{do}} \tag{2}$$

$$c = \frac{\overline{i_g\ i_d^*}}{\sqrt{\overline{i_d^2}}\sqrt{\overline{i_g^2}}} \tag{3}$$

where c is the correlation coefficient,and γ and β are the excess noise factor and excess gate noise factor. These factors are in general bias dependent.

For long-channel MOSFETs γ varies from 2/3 in the saturation region to 1 for the zero drain bias condition. The long-channel values for β and c are 4/3 and $j0.395$, respectively. The channel thermal noise is observed to increase in short-channel devices, hence causing an increase in the excess noise factor γ compared to the long-channel value of 2/3 [18]-[30]. Some earlier reports have indicated a significant increase (up to a factor of 4 or 5) in γ [18] -[21], and this excess channel noise was attributed to hot-electron effects and carrier heating. However, some recent reports show a moderate increase in γ [25] - [28] for short-channel MOSFETs. The β factor is also known to increase in shorter channel MOSFETs. The results reported in [22] suggest a significant enhancement (up to a factor of 30) in β, whereas a much smaller increase in β is reported in [25] and [26]. The precise amount of increase in γ and β and the mechanisms responsible for this excess noise is still actively debated in current literature. Evidently, large enhancements in γ and β would seriously limit the

use of MOS devices for low-noise RF IC design, and hence an extensive experimental study is required.

The other dominant noise source in short-channel MOSFETs is the thermal noise generated by the distributed gate resistance (R_G). The important RF noise sources in a MOSFET are shown in Fig. 6. To determine R_G, the polysilicon sheet resistance

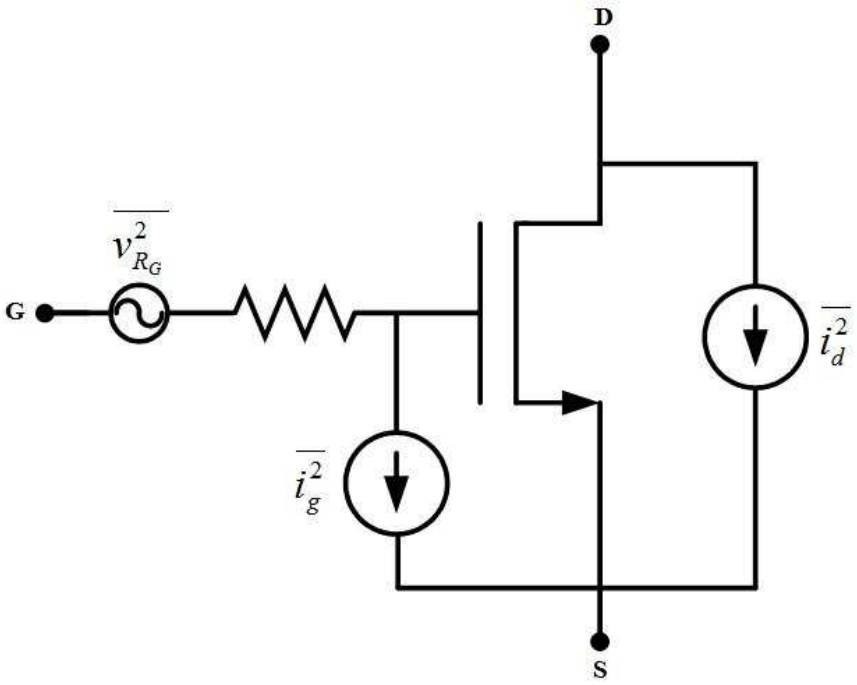


Figure 6: RF noise sources in a MOSFET

and the appropriate poly to silicide contact resistances have to be estimated [28]. The mean square thermal noise voltage generated by the gate resistance is given by,

$$\overline{v_{R_G}^2} = 4kTR_G\Delta f \tag{4}$$

The gate resistance thermal noise increases with scaling the gate-length and hence requires highly optimized device layouts. A good RF test structure employs multi-finger gate layout with narrow gate fingers and double-sided gate contacts. The distributed substrate resistance also contributes to the thermal noise of MOSFETs and can be minimized by placing a guard-ring around the device. It is also necessary

to place abundant contacts and vias at the source, drain, and gate terminals to minimize contact resistances.

In highly scaled MOSFETs with ultra-thin gate oxides, gate leakage current becomes very important owing to the direct tunneling of charge carriers through the gate dielectric. This gate leakage current gives rise to a shot noise component in the gate current, which is given by

$$\overline{i^2_{g,shot}} = 2qI_G\Delta f \tag{5}$$

where q is the electronic charge, and I_G is the DC gate current. The extraction of these noise sources from DC, high-frequency S-parameter, and noise parameter measurements is described in Chapter 3.

2.2 Noise Figure and Noise Parameters

Noise figure (NF) or the noise factor (F) is widely used as a measure of the noise performance of a system. The noise figure of a network is defined as the ratio of the signal-to-noise power ratio (SNR) at the input to the signal-to-noise power ratio at the output. The noise factor is expressed as

$$F = \frac{(SNR)_{in}}{(SNR)_{out}} \tag{6}$$

and the noise figure is expressed in dB.

$$NF = 10\ log_{10}\ F\ \ dB \tag{7}$$

Thus the NF represents the degradation in the SNR as the signal passes through a system.

The noise figure is generally affected by two factors, the intrinsic noise sources of the system and the source (input) admittance driving the system. As shown in Fig. 7, the noisefactor of a linear system exhibits a parabolic dependence on the source admittance ($Y_s\ =\ G_s\ + jB_s$) at a single frequency point, and can be expressed as:

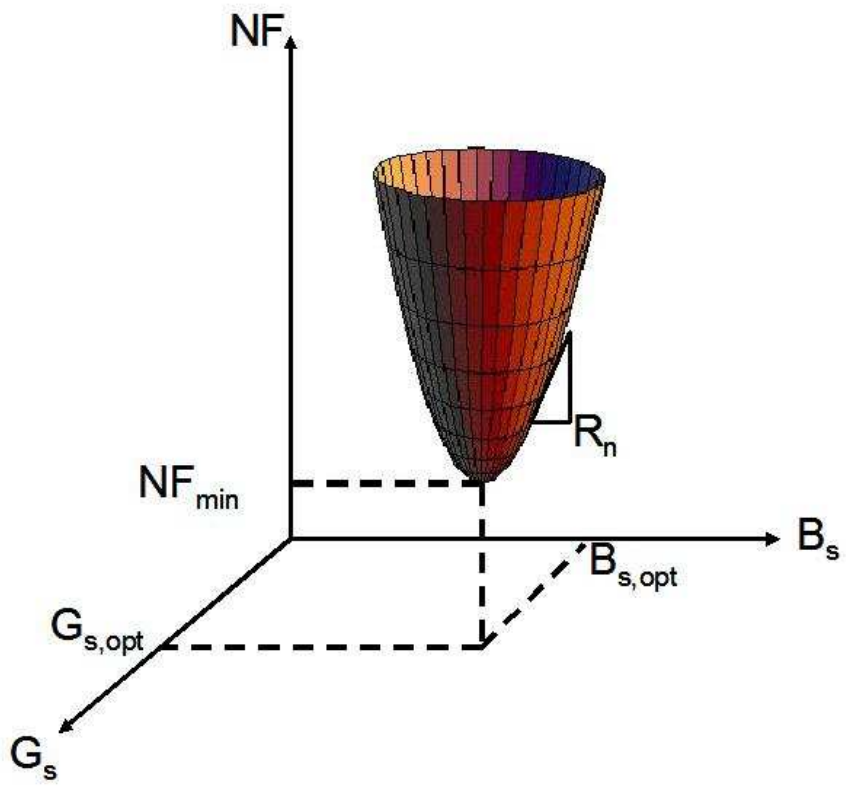


Figure 7: Dependence of noise figure on the source admittance

$$F = F_{min} \; + \; \frac{R_n}{G_s} \, |Y_s - Y_{opt}|^2 \tag{8}$$

Thus, the noise performance of any two-port network can be completely characterized by four noise parameters, namely minimum noise figure (or noise factor) F_{min}, noise resistance R_n, and the optimum source admittance Y_{opt} ($= \; G_{opt} \; + \; jB_{opt}$). Y_{opt} is the optimum source admittance at which the minimum noise figure F_{min} of the system is achieved. R_n determines the sensitivity of the noise figure of the system to the variations in the source admittance from the optimum condition. These four noise parameters are very widely used in RF circuit design and are closely related to the intrinsic device noise sources.

2.3 RF Noise Measurements

A block diagram of the RF noise measurement system is shown in Fig. 8. For the broadband noise measurements, the ATN-NP5B system is used in conjunction with

an HP8510C vector network analyzer (VNA), an HP8970B noise figure meter and a microwave probe station. The system uses a "multiple source impedance" technique

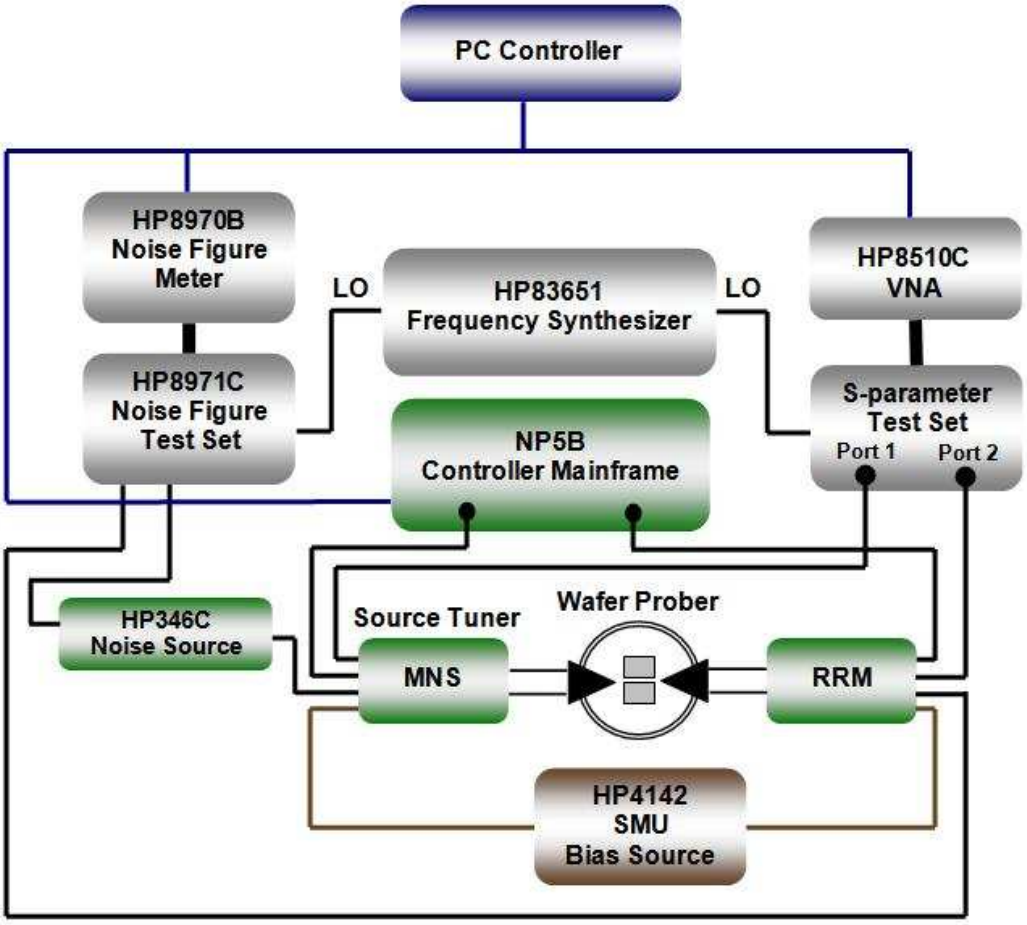


Figure 8: Block diagram of the ATN-NP5B RF noise measurement system

proposed by Adamian and Uhlir to extract the four noise parameters of the device under test (DUT) [31], [32]. The noise figure of the DUT is measured for various source admittances, and the four noise parameters are extracted using a least-square fit algorithm. The ATN-NP5B noise measurement system consists of a mismatched noise source (MNS), a remote receiver module (RRM), and a mainframe controller unit. The MNS contains a solid-state tuner that presents the DUT with multiple source admittances. The RRM contains a low-noise amplifier that is intended to lower the system noise figure, thereby reducing the measurement uncertainty. The

MNS and RRM have built-in bias tees and can be connected to an external bias source. This system allows the measurement of the four noise parameters from 2 GHz to 26.5 GHz. The system must be calibrated before performing the DUT noise characterization in order to account for the losses due to the cables, connectors, and probes, and thereby define a device reference plane. After calibration, the total noise figure of the system (F_{SYS}) is measured for various source admittances and the noise figure of the DUT can be extracted using the Friis chain equation:

$$F_{DUT} = F_{SYS} \; - \; \frac{F_{REC} \; - 1}{G_{DUT}} \tag{9}$$

where, G_{DUT} is the available gain of the DUT calculated from the DUT S-parameters and the source reflection coefficient, and F_{REC} is the noise factor of the receiver chain that is known from the calibration data. The four noise parameters of the DUT can be determined by measuring the F_{DUT} for various source admittances.

CHAPTER III

BROADBAND NOISE ANALYSIS AND MODELING OF HIGHLY SCALED MOSFETS

The dominant high-frequency noise sources in scaled MOSFETs have been enumerated in section 2.1. The development of accurate small-signal and noise equivalent circuits for MOSFETs necessitates a clear understanding of the device noise mechanisms along with a complete characterization of the device in terms of S-parameters and high-frequency noise parameters. A comprehensive analysis of the intrinsic broadband noise sources in state-of-the-art 130 nm nMOSFETs is presented in this chapter. A direct extraction procedure based on the two-port noise theory is used for obtaining the channel thermal noise, induced gate noise, and their cross-correlation from the measured S-parameters and RF noise parameters. A sub-circuit based RF noise model has been used that incorporates the channel thermal noise, the induced gate noise, and the thermal noise contribution from the gate resistance. This sub-circuit based RF noise model is used to obtain the simulated noise parameters: minimum noise figure NF_{min}, noise resistance R_n, and optimum source reflection coefficient Γ_{opt}.

3.1 Two-Port Noise Theory

From the theory of of linear noisy two-port networks [33]–[35], all the noise generated by a two-port device can be represented by its noise-less counterpart and two input-referred noise sources. Figure 9 (a) shows the noise equivalent circuit of a MOSFET with an input-referred voltage noise generator v_n and an input-referred current noise generator i_n. These intrinsic noise generators v_n and i_n can be derived from the chain

or $ABCD$ small-signal representation of the two-port network. These noise sources are, in general, correlated. By introducing a correlation admittance Y_{cor}, we have two independent noise sources v_n and i_u at the input of the two-port device, as shown in Fig. 9 (b). In this representation of the noisy two-port,

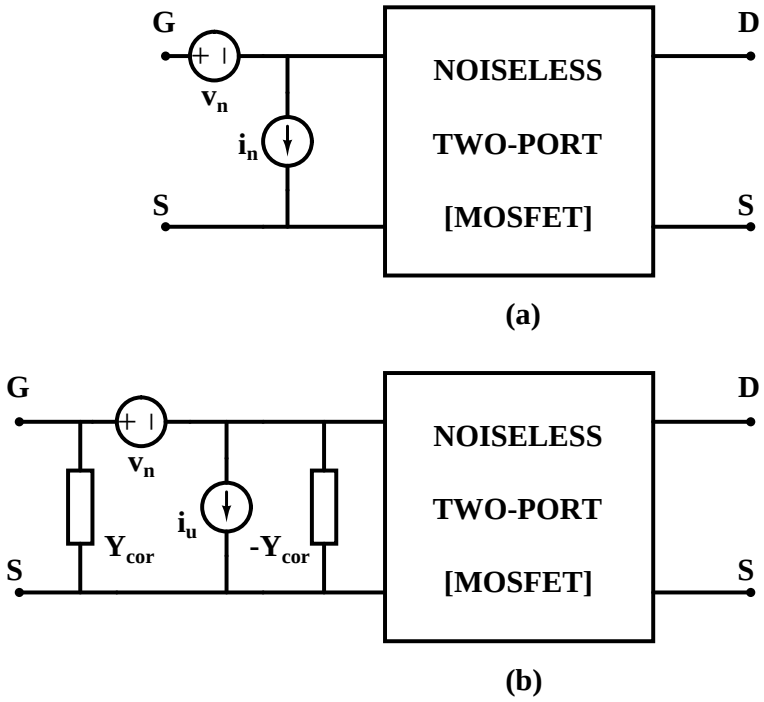


Figure 9: (a) Noise equivalent circuit with correlated noise sources (v_n and i_n) at the input of the two-port. (b) Noise equivalent circuit with uncorrelated noise current source i_u and noise voltage source v_n, with a correlation admittance Y_{cor}.

$$i_n = i_u + Y_{cor}\ v_n \tag{10}$$

$$\overline{v_n^2} = 4kT\Delta f R_n \tag{11}$$

$$\overline{i_u^2} = 4kT\Delta f G_n \tag{12}$$

The four independent noise generators R_n, G_n, and Y_{cor} (real and imaginary part) completely characterize the noise performance of a two-port device. These noise generators represent the input-referred noise sources of the device, and hence can be

directly expressed in terms of the intrinsic device noise sources. For establishing a valid noise model, these fundamental noise generators have to be determined from the measured RF noise parameters, namely, F_{min}, R_n, and Y_{opt}.

The intrinsic noise generators (R_n, G_n and Y_{cor}) can be obtained from the measured noise parameters (F_{min}, R_n and Y_{opt}) using the noise correlation matrix representation of a two-port device [36]. The noise correlation matrix of a two-port device can be written as

$$\mathbf{C_A} = 2kT \begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{F_{min}-1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix} \tag{13}$$

$$= \frac{1}{\Delta f} \begin{bmatrix} < v_n \ v_n^* > & < v_n \ i_n^* > \\ < i_n \ v_n^* > & < i_n \ i_n^* > \end{bmatrix}$$

From 13, we can write the intrinsic noise generators in terms of the measured noise parameters as follows:

$$R_n = \frac{\overline{v_n^2}}{4kT\Delta f} = R_n \ (measured) \tag{14}$$

$$G_n = \frac{\overline{i_u^2}}{4kT\Delta f} = G_{opt}(F_{min}-1) - \frac{(F_{min}-1)^2}{4R_n} \tag{15}$$

$$Y_{cor} = \frac{\overline{v_n \ i_n^*}}{\overline{v_n^2}} = \frac{F_{min}-1}{2R_n} - Y_{opt} \tag{16}$$

The intrinsic noise sources of a MOSFET can be extracted from these fundamental noise generators using the procedure outlined in the next section.

3.2 Direct Extraction of the Noise Sources of a MOSFET

Figure 10 shows the RF sub-circuit of an nFET with the intrinsic device noise sources. This sub-circuit model is used for the small-signal and RF noise modeling of

the nFET. Here, r_{ch} is the channel charging resistance, R_G is the gate resistance, g_m

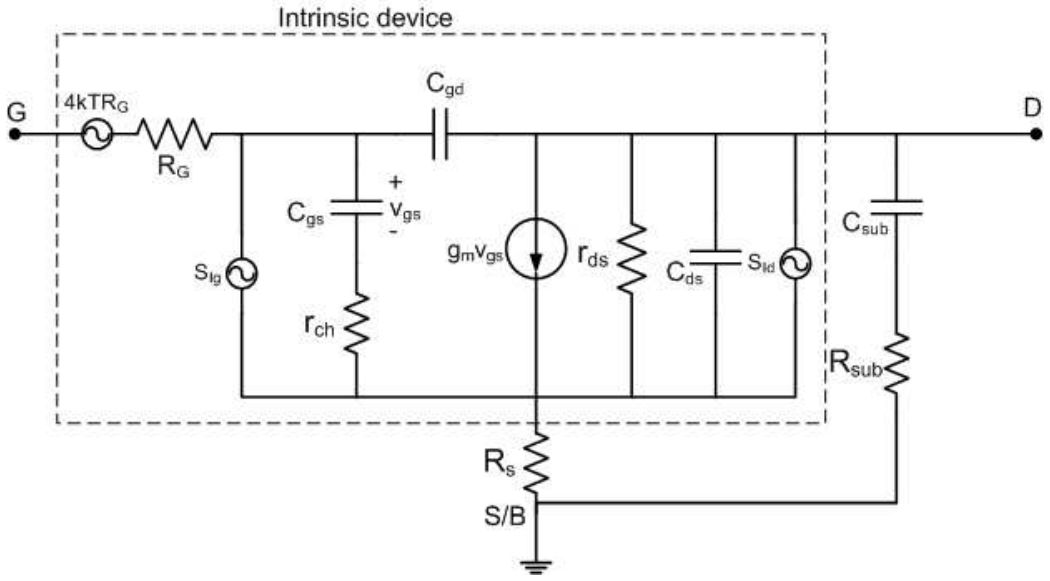


Figure 10: RF sub-circuit for small-signal and high-frequency noise modeling of a MOSFET.

is the transconductance, $1/r_{ds}$ is the channel conductance, and C_{gs}, C_{gd}, and C_{ds} are the gate-to-source, gate-to-drain, and drain-to-source capacitance, respectively. The r_{ch} is a non-quasistatic parameter and is usually inversely proportional to the channel conductance (g_{do}). The gate resistance R_G consists of two components, namely the polysilicon sheet resistance and the contact resistance between silicide and polysilicon. The R_G, for a single side gate contact, can thus be given by

$$R_G = \frac{\rho_{poly}}{3}\frac{W}{L}\frac{1}{N_f} \; + \; R_{con} \tag{17}$$

where, ρ_{poly} is the sheet resistance of polysilicon, L is the gate-length, W is the width of each gate finger, and N_f is the number of gate fingers. The elements of the small-signal equivalent circuit in Fig. (10) were extracted from the measured and de-embedded Y-parameters of the device [11], [37] – [39].

The Van der Ziel's long-channel model for channel thermal noise ($\overline{i_d^2}$), induced gate noise ($\overline{i_g^2}$), and their correlation (c) are given by equations (1)-(3). As described in section 2.1, the excess drain noise coefficient γ increases from its long-channel

value (of 2/3) for deep sub-micron MOSFETs. The gate-resistance thermal noise ($\overline{v_{R_G}^2}$), given by (4), also plays a very important role in the noise behavior of short-channel MOSFETs. Hence, modeling the γ parameter and the gate-resistance thermal noise are very essential for scaled MOSFETs. The thermal noise models in BSIM3 and BSIM4 compact models are based on Van der Ziel's MOSFET noise model. However, in the BSIM3v3 model, there are no independent parameters that can be used to fit the simulated noise parameters to the measured data. Also, BSIM3v3 does not model the induced gate noise and the gate resistance thermal noise, and hence under-predicts the F_{min} and R_n of the device. BSIM4 model has introduced more parameters to model the channel thermal noise in short-channel MOSFETs. However, the parameter NTNOI, that models the excess noise is a fixed parameter and hence does not capture the bias dependence of the γ parameter. To build a broadband noise model, it is necessary to accurately extract the intrinsic noise sources directly from the measured data and build a RF sub-circuit model that would be usable for RF circuit design. The direct extraction procedure described below is a generic approach and can be applied to any two-port device.

The channel thermal noise, the induced gate noise, and the gate-resistance thermal noise are the dominant intrinsic noise sources of a MOSFET, as shown in fig. 10. As described in section 3.1, these noise sources can be represented by an equivalent voltage (v_n) and current (i_n) noise generator at the input of the MOSFET. Using the representation shown in fig. 9, i_n can be split into two components, one that is correlated with v_n (i_c), and one that is uncorrelated (i_u). Thus, i_n can be expressed as

$$i_n = i_u \; + \; i_c = i_u \; + \; v_n Y_{cor} \tag{18}$$

The Y-parameters of the MOSFET are used for the transformation of the intrinsic noise sources of the MOSFET to the v_n–i_n representation. From the sub-circuit model

(in fig. 10), we can write

$$v_n = v_{R_G} \; + \; \frac{i_d}{Y_{21}} \tag{19}$$

$$i_n = i_g \; - \; \frac{Y_{11}}{Y_{21}} \; i_d \tag{20}$$

The induced gate noise i_g is partially correlated with the channel thermal noise i_d, and hence can be written as

$$i_g = i_{gu} \; + \; i_{gc} \tag{21}$$

where i_{gc} is correlated with i_d. Therefore, from equations (18), (20), and (21), i_n can be written as

$$i_n = i_{gu} \; + \; i_{gc} \; - \; \frac{Y_{11}}{Y_{21}} \; i_d \tag{22}$$

The intrinsic noise generators R_n, G_n, and Y_{cor} can be evaluated from the measured RF noise parameters F_{min}, R_n, and Y_{opt} as described in equations (14)-(16). These intrinsic noise generators essentially describe the noise power spectral densities $\overline{v_n^2}$ and $\overline{i_n^2}$, which are directly related to the device noise sources. The $\overline{v_n^2}$ and $\overline{i_n^2}$ are given as

$$\overline{v_n^2} = \overline{v_{R_G}^2} \; + \; \frac{\overline{i_d^2}}{|Y_{21}|^2} = 4kT_o \; \Delta f R_n \tag{23}$$

$$\overline{i_n^2} = \overline{i_{gu}^2} \; + \; |Y_{cor}|^2 \overline{v_n^2} = 4kT_o \; \Delta f \; \left[G_n \; + \; |Y_{cor}|^2 R_n \right] \tag{24}$$

Using this formulation, the power spectral densities of the channel thermal noise, induced gate noise, and their cross-correlation can be extracted as follows:

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT_o\ (R_n - R_G)\ |Y_{21}|^2 \tag{25}$$

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT_o\ R_n\ \left\{|Y_{opt}|^2 - |Y_{11}|^2 + 2\Re\left[\left(\left(1 - \frac{R_G}{R_n}\right)Y_{11} - Y_{cor}\right)Y_{11}^*\right]\ +\ \frac{R_G}{R_n}|Y_{11}|^2\right\} \tag{26}$$

$$\frac{\overline{i_g\ i_d^*}}{\Delta f} = 4kT_o\ R_n\ \left\{\left[\left(1 - \frac{R_G}{R_n}\right)Y_{11} - Y_{cor}\right]Y_{21}^*\right\} \tag{27}$$

Using Van der Ziel's formulation (1) and equation (25), the excess noise coefficient γ can be expressed as

$$\gamma = \frac{(R_n - R_G)|Y_{21}|^2}{g_{do}} \tag{28}$$

The β factor can be extracted from equations (2) and (26).

Hence, the intrinsic device noise sources are extracted directly from the measured S-parameters and broadband noise parameters. The calculated noise sources are applied to the sub-circuit shown in Fig. 10 to obtain the simulated RF noise parameters – NF_{min}, R_n, and Γ_{opt}.

3.3 Broadband Noise Modeling of 130 nm nFETs

The direct extraction method was applied to an nFET from a 130 nm CMOS technology. The measurement and modeling results are presented in this section [40].

3.3.1 Device Technology and Experiments

The MOSFETs used in this study are contained in a fully integrated, commercially available 0.13 μm CMOS technology [41], [42]. The DUTs used for our analysis are nFETs with a W/L of $8.0\mu m/0.12\mu m$ (with 32 gate fingers). Figure 11 shows the the high-frequency figures-of-merit, the cut-off frequency (f_T), and maximum frequency of oscillation (f_{max}) of this device, as a function of the drain current. This nFET exhibits a peak f_T of about 100 GHz and f_{max} over 50 GHz. The S-parameters were measured

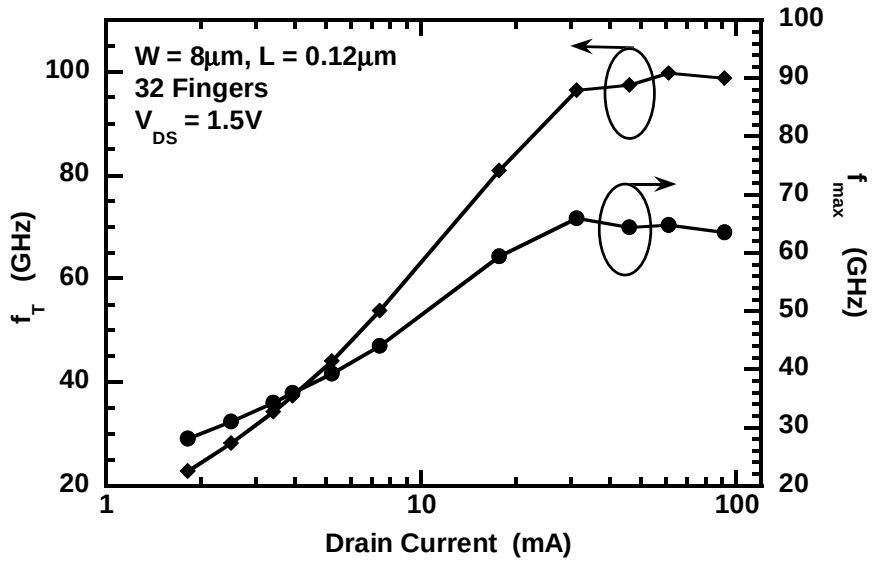


Figure 11: Cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) versus drain current for an nFET with $W/L = 8.0/0.12$ (32 fingers).

using an Agilent 8510C VNA. The conventional "Open-Short" de-embedding technique was performed on the raw S-parameters of the devices to eliminate the effects of pad parasitics. The high-frequency noise parameters were measured from 2 GHz to 26 GHz using the ATN NP5B noise measurement system, as described in section 2.3. The noise parameters were de-embedded using the generalized two-port noise de-embedding procedure [43].

3.3.2 Results and Discussion

The de-embedded Y-parameters of the DUT were used to compute the elements of the small-signal sub-circuit model shown in fig. 10. The modeled Y-parameters show a very good agreement with the measured data, as shown in fig. 12. The small-signal parameters of the DUT at a representative bias point are enumerated in Table 1.

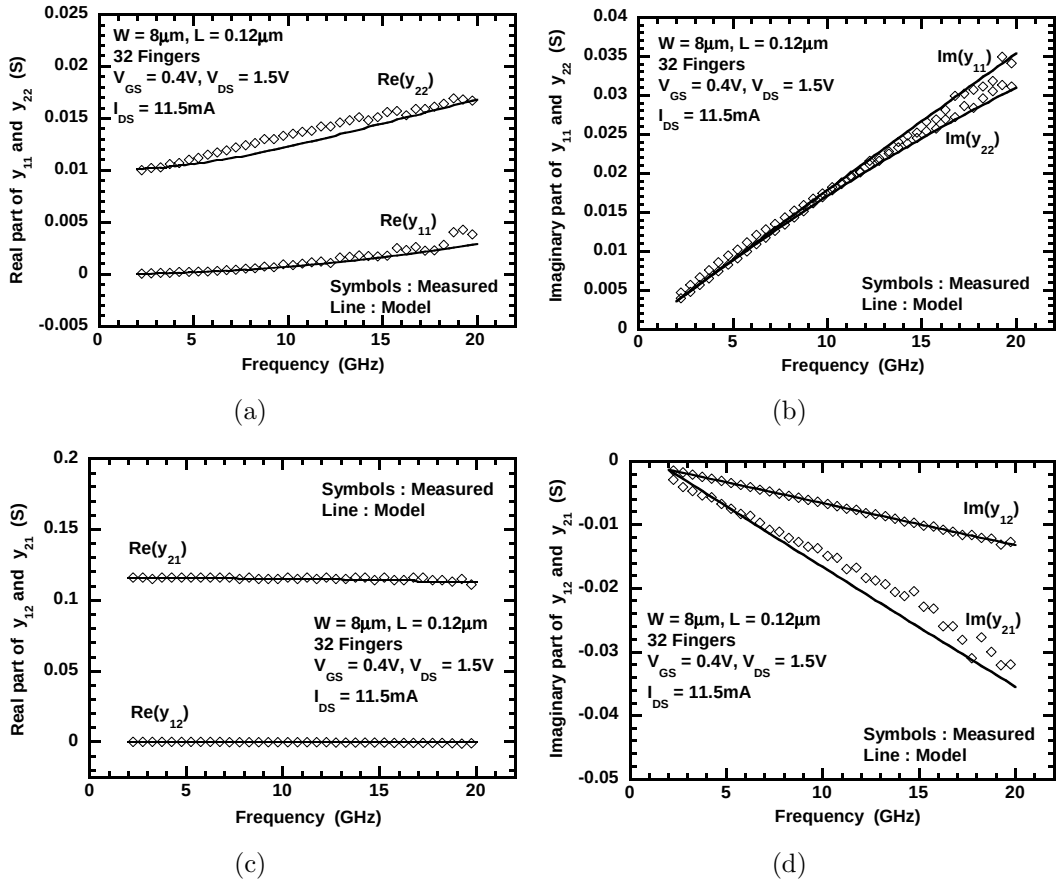


Figure 12: (a) Measured and modeled real parts of y_{11} and y_{22} versus frequency, (b) Measured and modeled imaginary parts of y_{11} and y_{22} versus frequency, (c) Measured and modeled real parts of y_{12} and y_{21} versus frequency, (d) Measured and modeled imaginary parts of y_{12} and y_{21} versus frequency – for a nFET with $W/L = 8.0/0.12$ (with 32 fingers).

Table 1: Small-signal Parameters of a nFET with $W/L = 8.0/0.12$ (with 32 fingers) biased at V_{GS}=0.6V and V_{DS}=1.2V

Parameters	R_G	r_{ch}	g_m	g_{ds}	C_{gs}	C_{gd}
Values	6.0 Ω	7.1 Ω	152.4 mS	18.8 mS	235.5 fF	101.0 fF

The intrinsic device noise sources were extracted from the measured high-frequency noise parameters and the elements of the RF sub-circuit model using the procedure described in the previous section. Figure 13 shows the frequency dependence of the

channel thermal noise and the induced gate noise. The channel thermal noise is, in general, independent of frequency. The induced gate noise, however, is proportional to the square of the frequency, as expected theoretically. The gate shot noise estimated using equation (5) is about 1.3 x 10^{-25} A^2/Hz at the frequency and bias condition of interest (I_G is about 0.4 μA). As we can see, the gate shot noise is not very significant at high frequencies. The cross-correlation between channel thermal

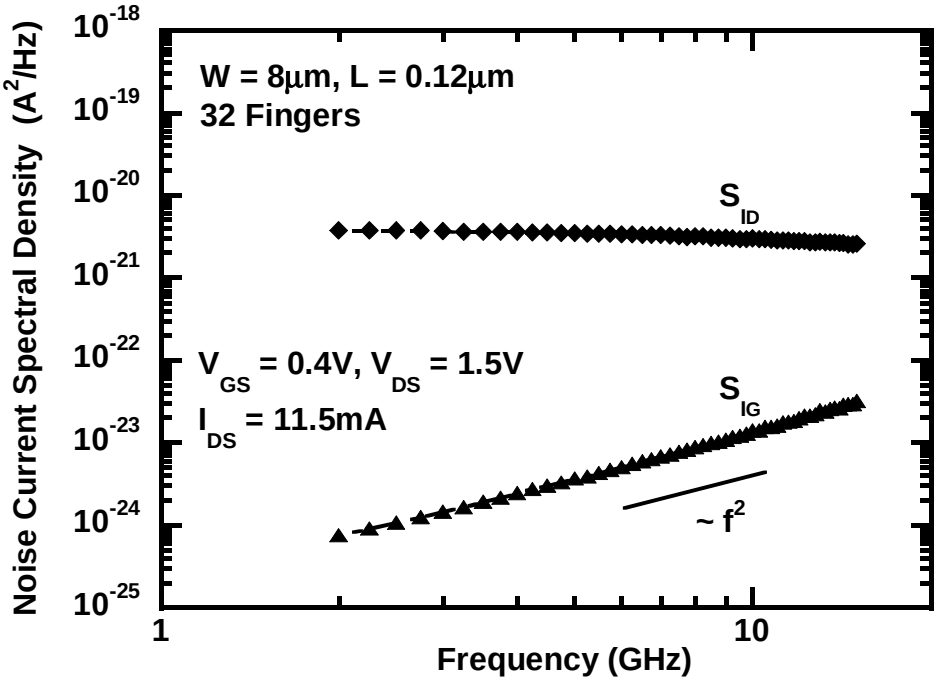


Figure 13: Frequency dependence of channel thermal noise ($\overline{i_d^2}$) and gate current noise ($\overline{i_g^2}$) for an nFET with $W/L = 8.0/0.12$ (32 fingers).

noise and induced gate noise as a function of frequency is shown in Fig. 14. The imaginary part of the correlation term is proportional to the frequency, whereas, the real part of the correlation term is almost zero up to about 10 GHz. This is mainly due to the capacitive coupling of the gate-induced noise through C_{gs}.

The dependence of channel thermal noise and induced gate noise on the drain current (at a fixed V_{DS} and varying V_{GS}) is shown in Fig. 15. The channel thermal noise shows a strong bias dependence and increases as V_{GS} increases. The induced

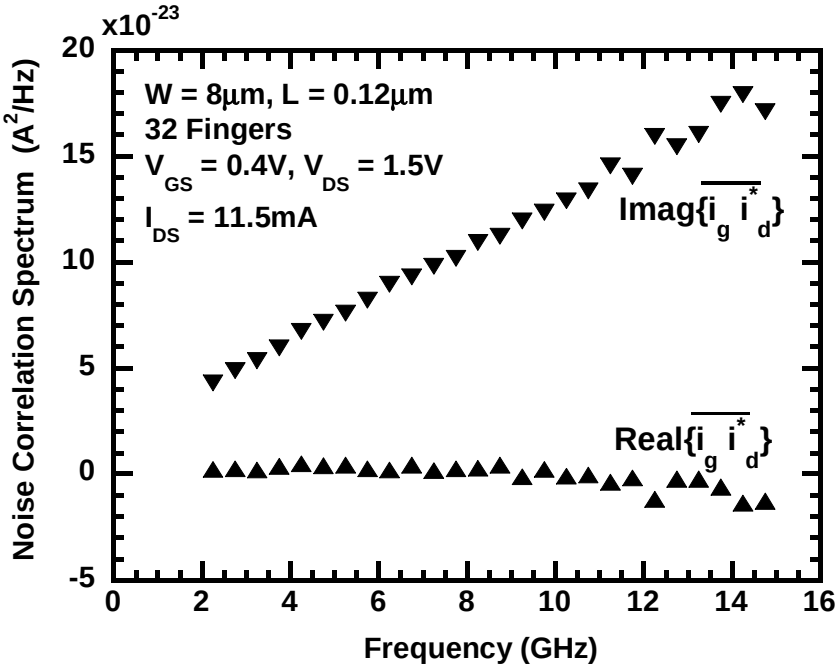


Figure 14: Frequency dependence of real and imaginary part of the cross-correlation between channel thermal noise and induced gate noise – for a nFET with $W/L = 8.0/0.12$ (with 32 fingers).

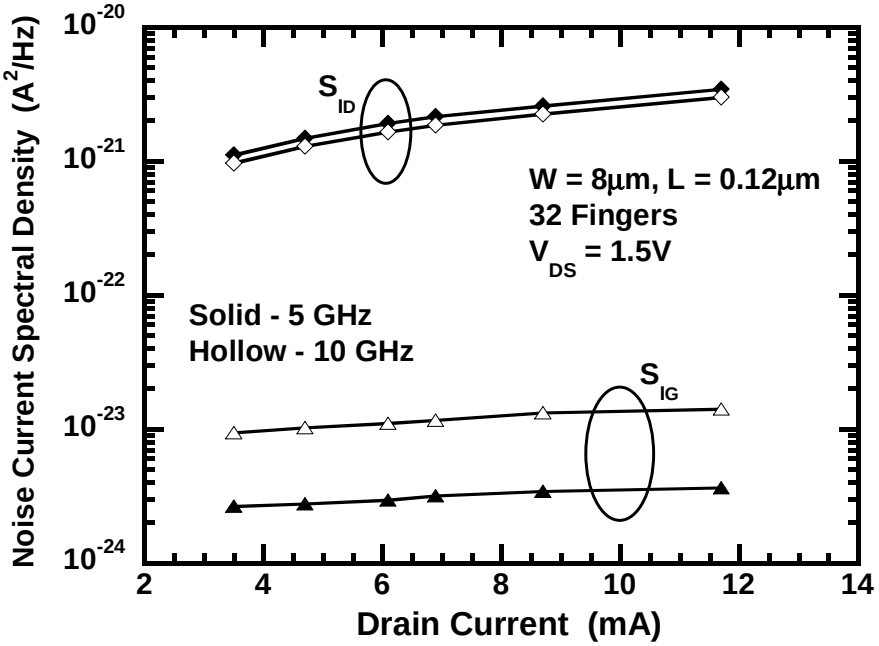


Figure 15: Bias dependence of channel thermal noise ($\overline{i_d^2}$) and gate current noise ($\overline{i_g^2}$) for an nFET with $W/L = 8.0/0.12$ (32 fingers).

gate noise shows a weaker bias dependence and increases slightly with increase in V_{GS}. This is due to the increase in the effective channel resistance due to velocity saturation at high gate bias conditions. The bias dependence of noise correlation between the channel thermal noise and induced gate noise is plotted in Fig. 16. The

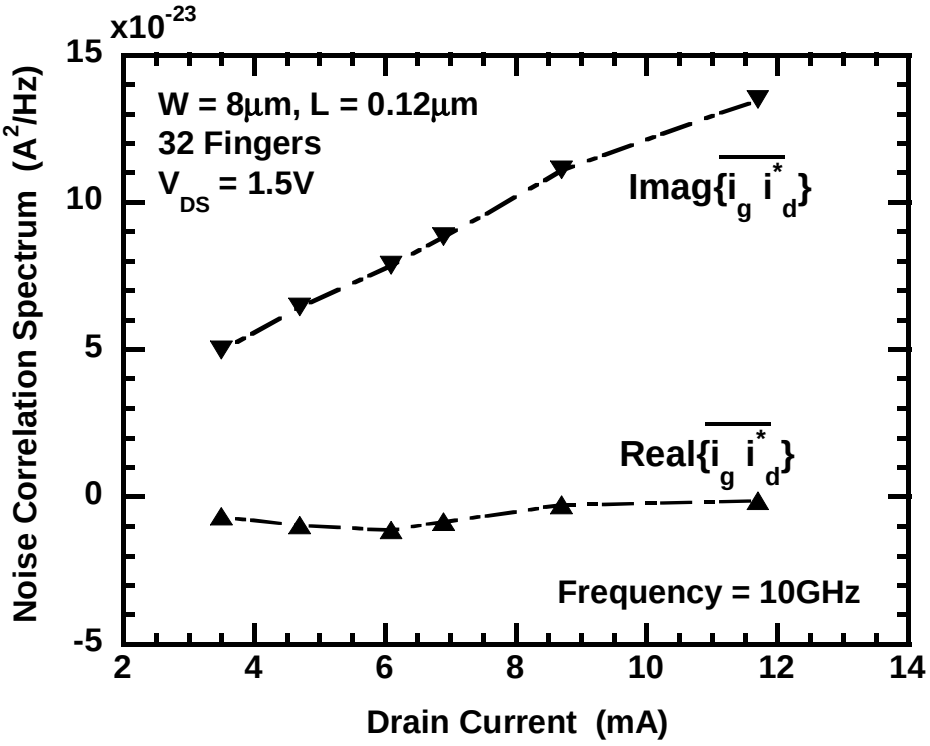


Figure 16: Bias dependence of real and imaginary part of the cross-correlation between channel thermal noise and induced gate noise – for a nFET with $W/L = 8.0/0.12$ (with 32 fingers).

imaginary part of the correlation term increases with increasing gate bias, whereas the real term exhibits a weak dependence on the gate bias. The excess noise factors γ and β are evaluated from $\overline{i_d^2}$ and $\overline{i_g^2}$ respectively. Figures 17 and 18 show the bias dependence of γ and β, respectively. It is observed that both γ and β increase with increasing V_{GS}. There is a moderate enhancement of γ compared to the theoretical long channel value of 2/3. This enhancement of γ in short-channel MOSFETs is attributed to channel length modulation and carrier heating. The maximum value of γ in saturation region is around 2, which is in agreement with the values reported for

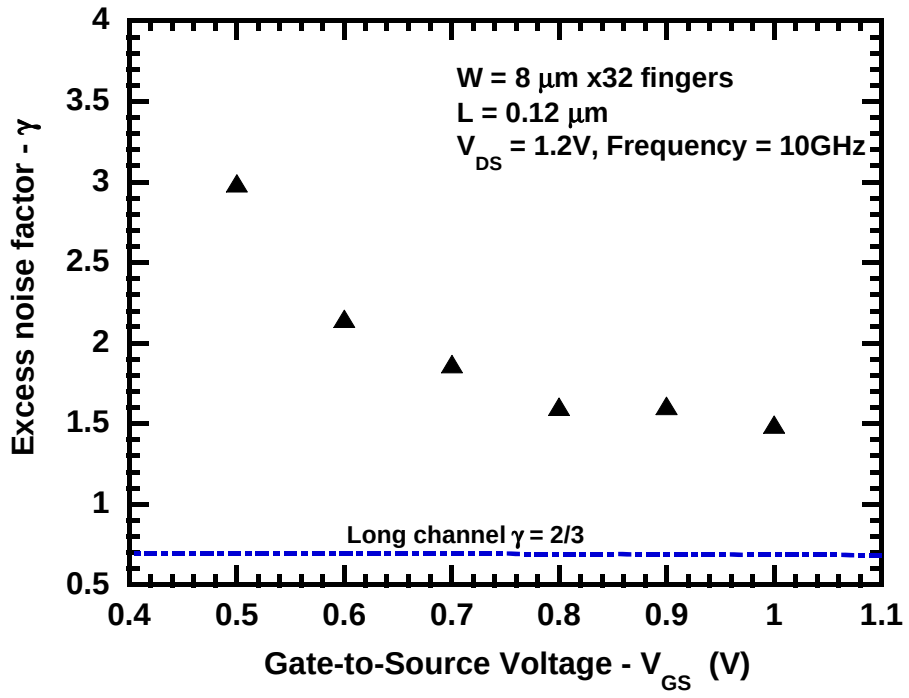


Figure 17: Bias dependence of γ for a nFET with $W/L = 8.0/0.12$ (32 fingers).

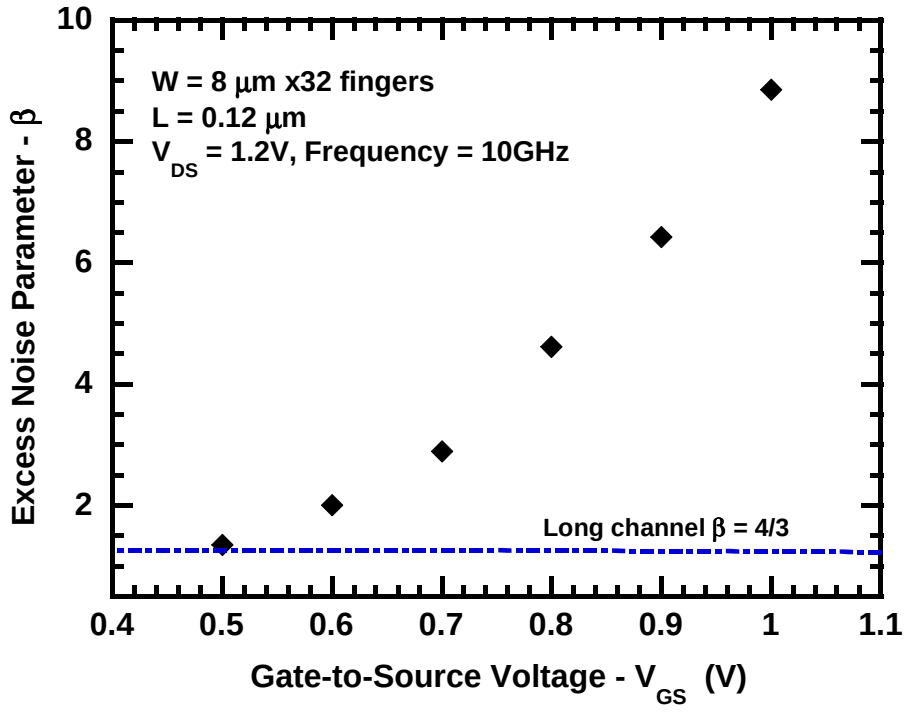


Figure 18: Bias dependence of β for a nFET with $W/L = 8.0/0.12$ (32 fingers).

a 0.18 μm technology node [25]–[27]. We see that β is close to the long-channel value of 4/3 for small gate bias and becomes as large as 8 at higher V_{GS}. The increase in β at high gate bias is due to the increase in effective channel resistance because of velocity saturation. However, it is observed that the contribution of the induced gate noise to the total device noise is relatively small for these highly scaled MOSFETs.

The impact of channel length on the intrinsic noise currents is shown in figs. 19 and 20. From fig. 19, we see that the channel thermal noise increases rapidly as the channel length decreases. This is mainly due to the more pronounced channel length modulation effect and carrier heating in short-channel MOSFETs. The increase in

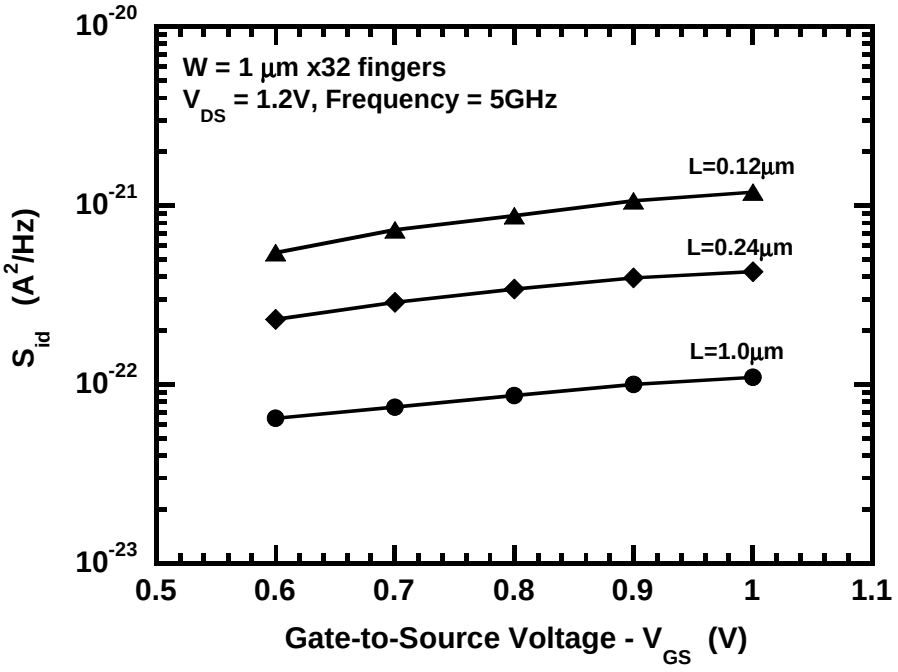


Figure 19: Bias dependence of channel thermal noise ($\overline{i_d^2}$) for various gate lengths.

current drive and channel conductance of short-channel MOSFETs leads to a decrease in the induced gate noise with decreasing gate lengths, as shown in fig. 20. As shown in fig. 21, the increase in channel thermal noise results in higher excess noise factor γ for the short-channel devices.

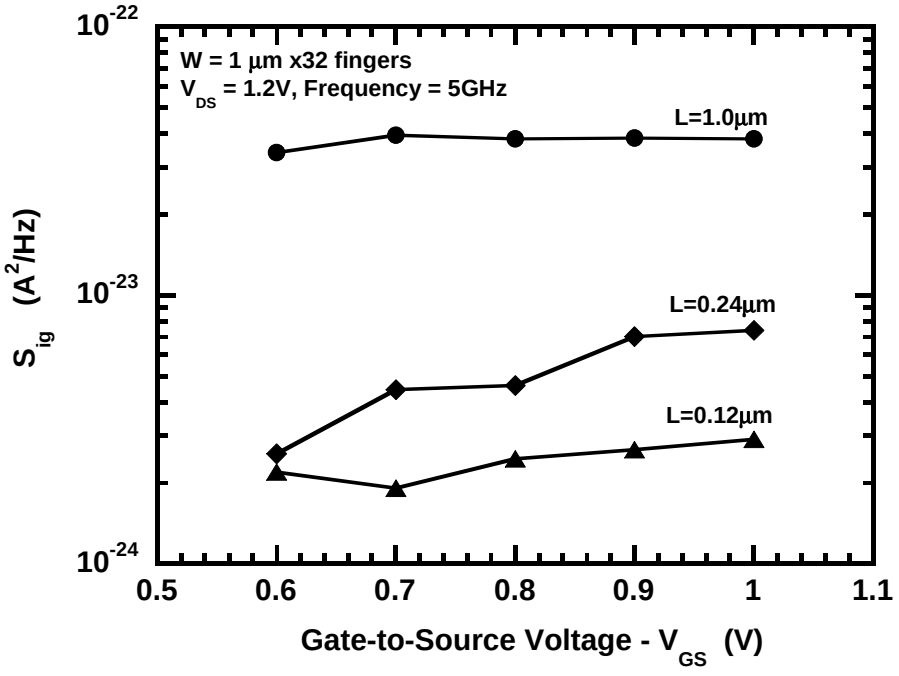


Figure 20: Bias dependence of induced gate noise ($\overline{i_g^2}$) for various gate lengths.

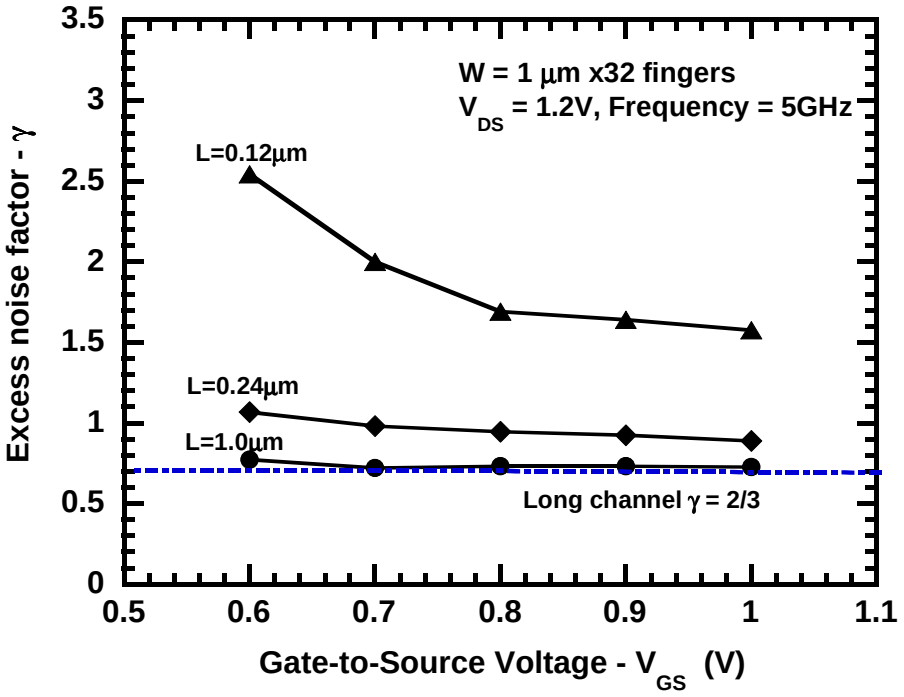


Figure 21: Bias dependence of excess noise factor γ for various gate lengths.

The extracted noise currents are fed to the equivalent circuit model to obtain the simulated RF noise parameters - NF_{min}, R_n, and Γ_{opt}. Figure 22 shows the measured and simulated NF_{min} and R_n across frequency. This 130 nm nFET device exhibits a sub-1.0dB NF_{min} up to about 10 GHz, which is very useful for C-band applications. The optimum source reflection coefficient versus frequency is shown in Fig. 23.

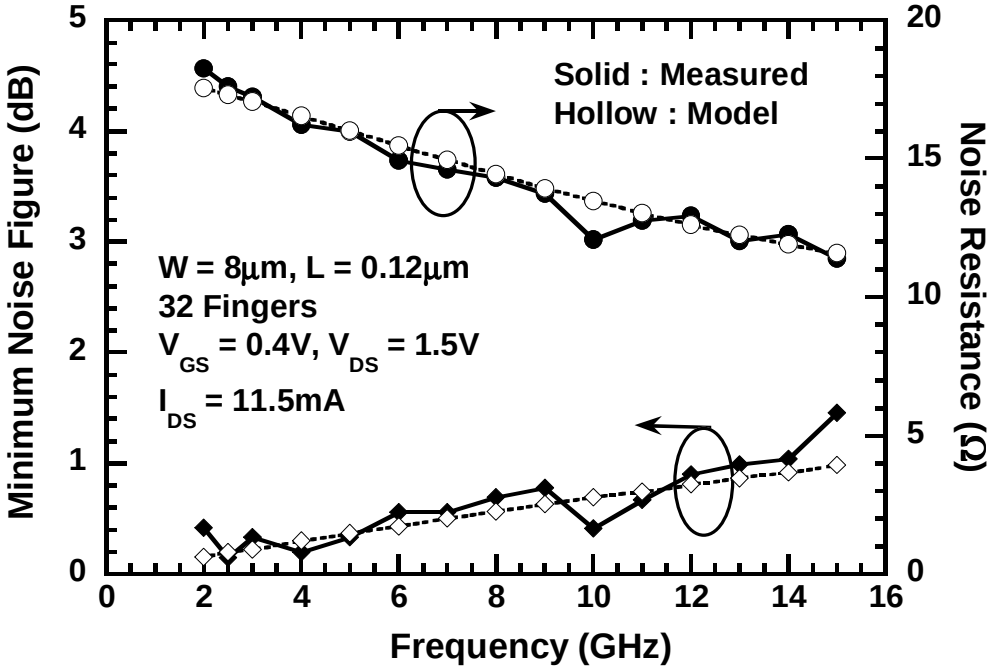


Figure 22: Measured and modeled NF_{min} and R_n versus frequency – for an nFET with $W/L = 8.0/0.12$ (with 32 fingers).

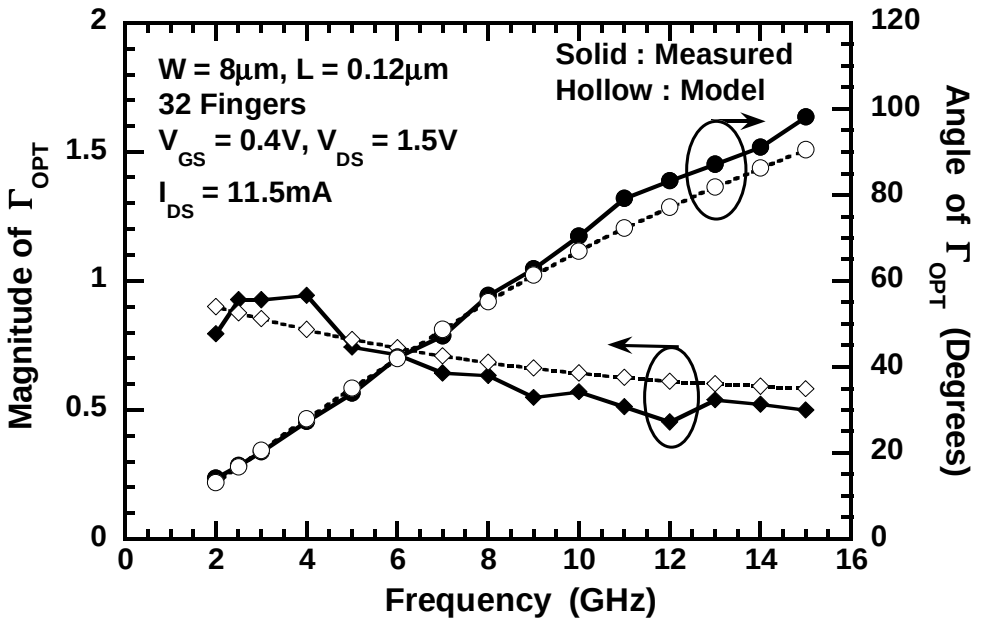


Figure 23: Measured and modeled optimum source reflection coefficient (Γ_{opt}) versus frequency – for an nFET with $W/L = 8.0/0.12$ (with 32 fingers).

The bias dependence of NF_{min} and R_n is shown in Fig. 24. Figure 25 shows the bias dependence of the (Γ_{opt}). The measured and modeled noise parameters agree

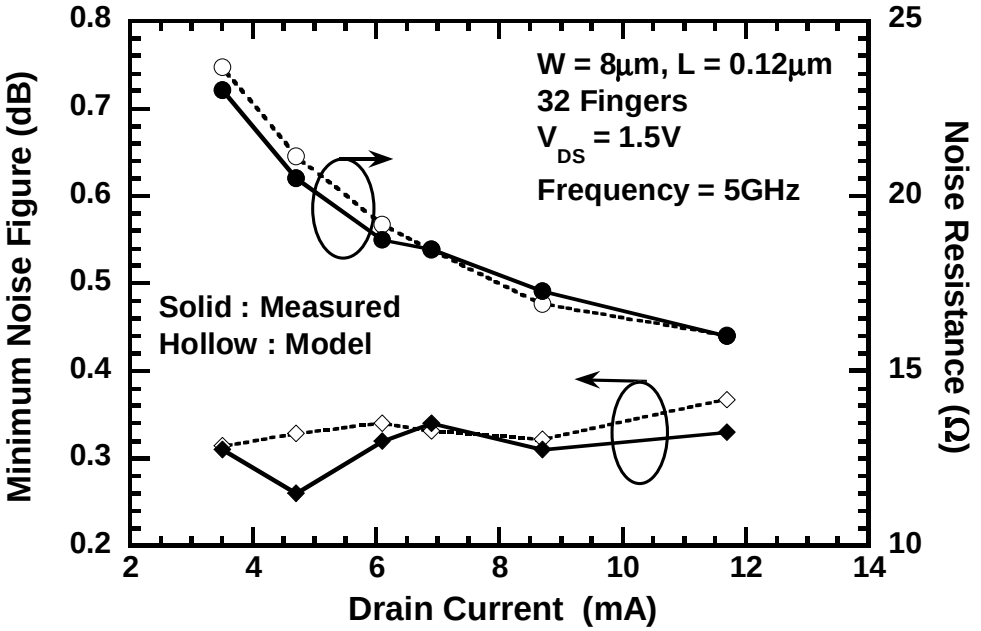


Figure 24: Measured and modeled NF_{min} and R_n across bias - for an nFET with $W/L = 8.0/0.12$ (with 32 fingers).

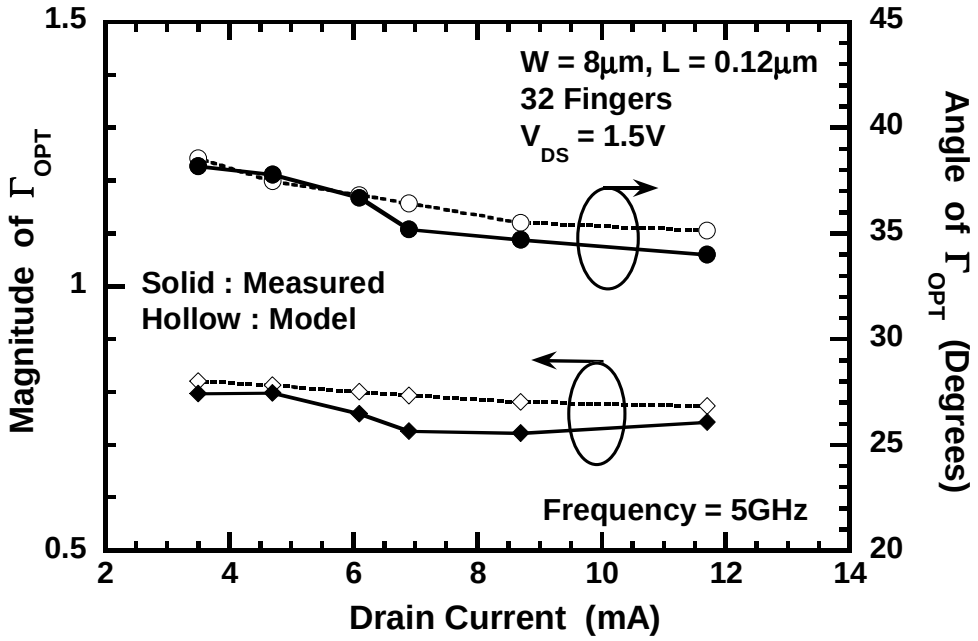


Figure 25: Measured and modeled Γ_{opt} across bias – for an nFET with $W/L = 8.0/0.12$ (with 32 fingers).

well with each other, confirming the validity of the sub-circuit model.

CHAPTER IV

CRYOGENIC PERFORMANCE OF DEEP SUB-MICRON CMOS DEVICES

Cryogenic electronics spans some important niche applications such as space electronics for deep-space and planetary missions, ultra-low-noise radio receivers for radio astronomy applications, high-sensitivity cooled sensors and detectors, and semiconductor super-conductor hybrid systems. The operation of semiconductor devices at cryogenic temperatures has received considerable attention during the past few decades, primarily for two reasons. One reason is to study and understand the material properties, and device physics and operation at low temperatures. The second reason is to explore the applicability of several device technologies for developing cryogenic electronic systems. The potential performance enhancement of Si-CMOS devices at cryogenic temperatures has motivated the study of bulk CMOS devices at low temperatures, mainly at liquid Nitrogen (77K) and liquid Helium (4K) temperatures. A comprehensive investigation of the DC, small-signal AC, and broadband noise performance of highly scaled Si-MOSFETs is presented in this chapter.

4.1 On-wafer Cryogenic Measurement System

In this work, the on-wafer cryogenic measurements were performed using two cryogenic probing systems described in the following sub-sections. One system employs a closed-cycle helium refrigeration system, and the other one uses an open-cycle cooling system.

4.1.1 Closed-cycle Helium Refrigeration System

The closed-cycle cryogenic measurement system used in this work is a custom-designed cryogenic probing system that enables on-wafer microwave measurements from 18K to 350K, from DC to 50GHz [44]–[46]. The cryogenic probe measurement system, shown in Fig. 26, contains ports for RF cables, thermometers, vacuum pumps, dry nitrogen back-fill lines, coplanar probes with manipulators, and a closed-cycle refrigerator cold head. The probe body rests on a copper block attached to a fiberglass post that reduces the thermal load, and copper braiding from the cold head thermally anchors the probe to the 12 K cold station, assuring sample temperatures of 12 to 20 K. The mechanical and thermal stability of the wafer stage is established by supporting it on fiberglass posts above the cold head and thermally anchoring it to the cold station with flexible copper braids.

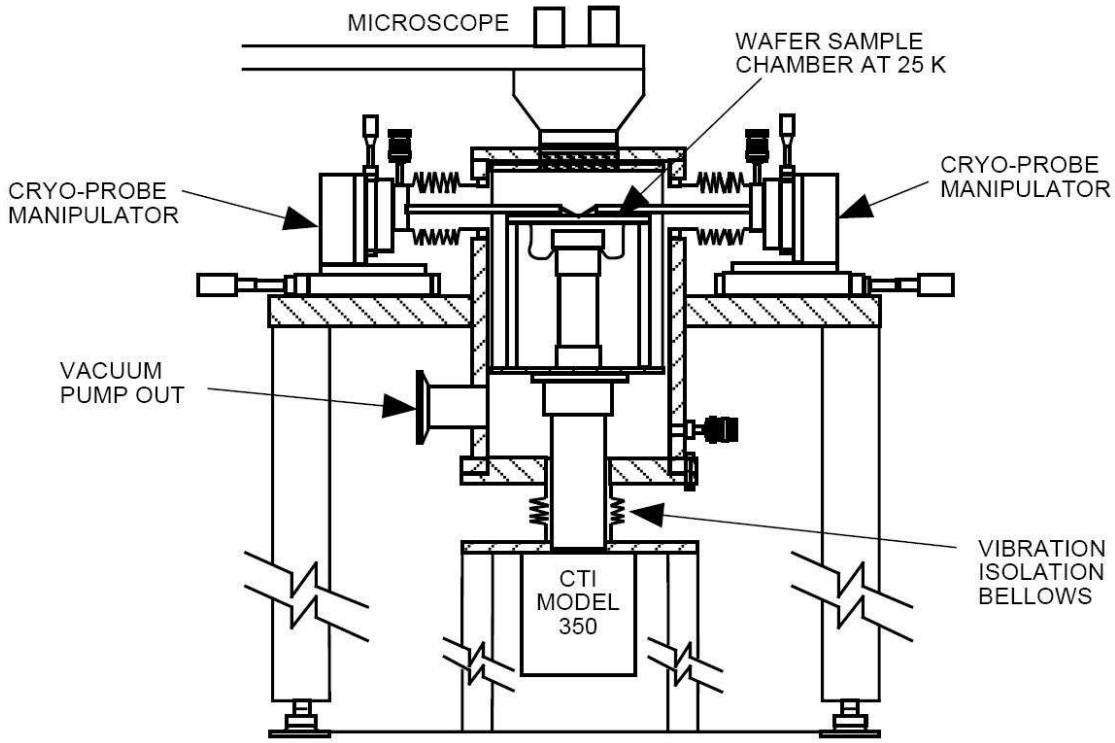


Figure 26: Schematic view of the closed-cycle cryogenic probing system.

The most important feature of this cryogenic probing system is the incorporation of a closed-cycle helium refrigeration system. The first successful designs of on-wafer cryogenic systems used open-cycle cooling to reduce start-up costs and avoid mechanical vibrations. However, for a long time use, a closed-cycle system is significantly less expensive. Decoupling and damping of the vibrations from the cold head to the probe station are accomplished with two-dimensional bellows and vibration mounts. The DUT is mounted on the cold wafer stage and the test chamber is evacuated to prevent frost build-up and large thermal grading when cooling the chamber. A view port on the top permits the accurate positioning of the RF probes on the sample. The vacuum chamber is coupled to a VNA and a noise measurement system for performing the RF measurements.

4.1.2 Open-cycle Cryogenic Probing System

The open-cycle cryogenic probing system used in this work is shown in fig. 27. Cryogenic operation is based on a continuous-transfer cryogenic refrigerator designed for this probe station, which enables on-wafer microwave measurements across the temperature range of 4.2K to 475K, from DC to 40 GHz. The main components of this system include,

1. Four independently manipulated probe-arms, each holding a DC or a RF probe;
2. An optical system, comprising of a microscope, camera, light source, and monitor, to view the sample under test;
3. A turbo vacuum pump to evacuate the test chamber;
4. A transfer line to carry the cryogen (liquid nitrogen or liquid helium) from a dewar to the refrigerator;
5. A temperature controller to regulate the sample temperature.

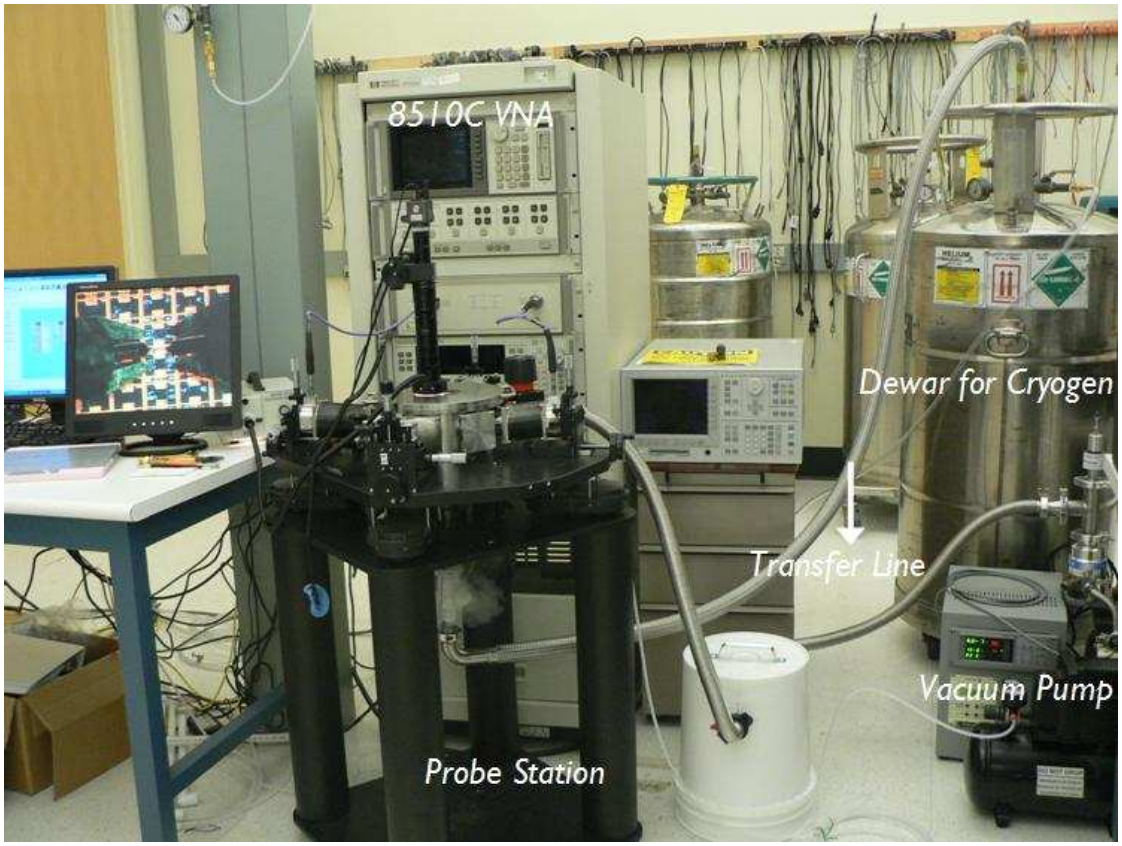


Figure 27: Photograph of the open-cycle cryogenic probing system.

The samples are placed on a copper chuck inside the evacuated test chamber and then cooled by the cryogen. Copper braids are used to thermally anchor the probes to the cold head, to ensure that the probe temperature is close to the temperature of the sample. This is especially important while doing measurements below 10K, where additional copper straps may be required to tie the probe body in order to reduce the temperature of the probe. Intermediate radiation heat shield is installed around the chuck to isolate the warm area from the cold area at the chuck, as shown in fig. 28. The device samples are mounted on the chuck using a thermal grease. The thermometry of the system is verified by mounting silicon diode sensors on the probe arms and the chuck. The probe arms are connected to an 8510C VNA for the S-parameter measurements, and the ATN-NP5B noise tuners and HP 8970B noise figure meter for the RF noise parameter measurements, as shown in fig. 29. For the noise

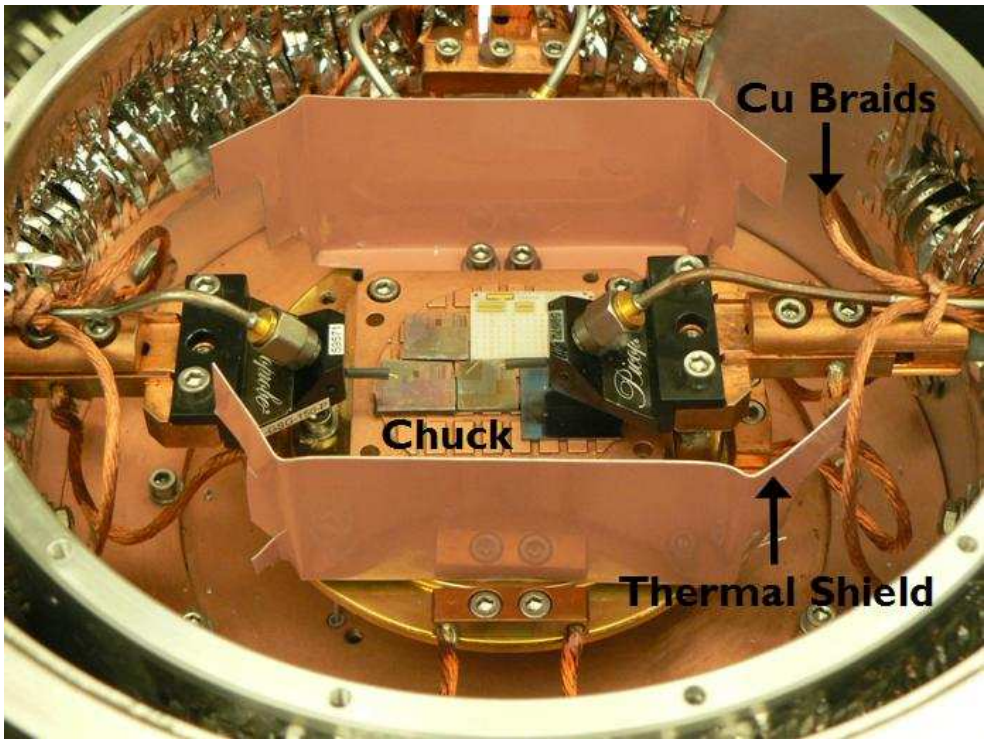


Figure 28: View of the sample holder.

measurements, the noise source and the noise tuners are kept at room temperature, and the tuners are connected to the probe arms via short cables. This system allows measurements in the frequency range of DC to 40 GHz.

4.1.3 Calibration Considerations

To achieve repeatable cryogenic on-wafer S-parameter measurements, one must provide a stable thermal environment and perform careful calibrations at each temperature point of interest. In the open-cycle system, the pressure of the cryogen must be monitored continuously to control the flow of the cryogen to the probe station in order to maintain the temperature stability within the measurement chamber. Any thermal gradient could potentially lead to drift in the S-parameter calibrations. Hence, it is also necessary to measure the calibration drift from time to time to ascertain the validity of the calibration. Decoupling any external vibrations is also

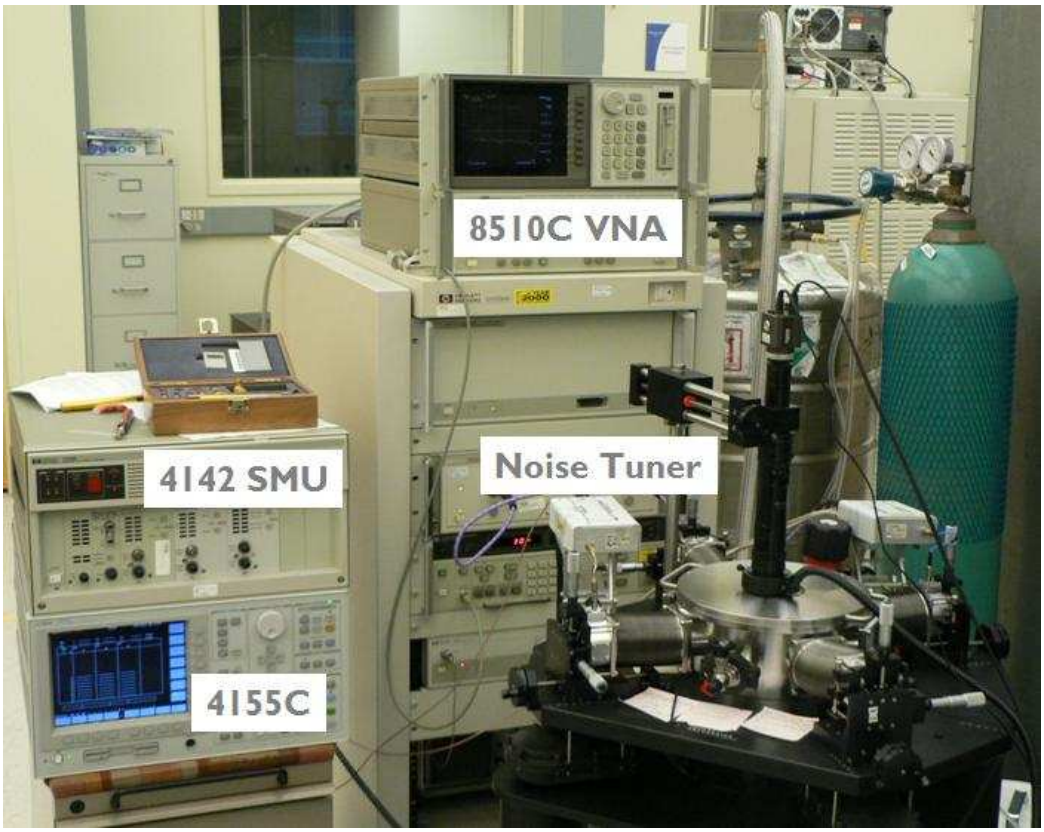


Figure 29: Photograph of the cryogenic chamber connected to the VNA and noise tuners for on-wafer S-parameter and RF noise parameter measurements.

essential to reduce errors and drift in the calibration. In this work, line-reflect-reflect-match (LRRM) calibration was performed at each temperature point for accurate broadband calibration.

The most accurate and repeatable method of measuring RF noise parameters at cryogenic temperatures is to place the impedance generator (noise tuner) within a wavelength of the DUT input. The equivalent noise temperature of the noise source must also be comparable to the DUT noise temperature. However, this approach would require a cryogenic noise generator and noise source. For the RF noise parameter measurements, the impedance state generator (source tuner) and the solid-state noise source are kept at room temperature, as shown in fig. 29. The source tuner is kept several wavelengths away from the DUT, which introduces error in the noise parameter measurements. In this configuration the input losses introduce noise

comparable to or greater than the noise of the DUT and reduces the range of available impedance states. Hence, it is very important to use extremely short low-loss feedthrough cables to connect the noise tuner to the probe arm. In this work, we used a custom made low-loss, three inch semi-rigid cable. To enhance the accuracy of the system, it would be instructive to measure the noise parameters at high frequencies ($>$ 10 GHz). Overall, this system provides for fast and efficient broadband on-wafer noise measurements.

4.2 Operation of MOSFETs at Cryogenic Temperatures

The operation Si-MOSFETs at cryogenic temperatures has received a lot of attention over the past few decades [47]–[58]. The motivation for low-temperature operation of MOSFETs arises from the expected performance improvement at both the device and the circuit level in comparison to room temperature operation. Temperature lowering allows for substantial increase in carrier mobility and saturation velocity, improved sub-threshold swing, decrease of leakage currents, reduction of short channel effects, and low voltage / low power operations. At the circuit and system level, the advantages include higher switching speed due to increased mobility and decreased interconnect resistance, enhanced reliability due to exponential slow down of thermally activated processes like electromigration. The low-temperature operation of CMOS logic circuits is especially attractive because of appreciable reduction in the power delay product. Also, CMOS operation at cryogenic temperatures is virtually latch-up free because of the decreased gain of parasitic bipolar devices.

The lowering of temperature has a profound impact on the intrinsic device properties of the MOSFET, such as the mobility, transconductance, and threshold voltage. The threshold voltage (V_T) for a nFET with uniform substrate doping is given by

$$V_T = V_{FB} \; + \; 2|\psi_b| + \; \frac{\sqrt{2\epsilon_{Si} q N_a \; (2|\psi_b| + V_{bs})}}{C_{ox}} \tag{29}$$

where V_{FB} is the flat-band voltage, ψ_b is the Fermi potential of the bulk Si with respect to the intrinsic Fermi level, ϵ_{Si} is the dielectric constant of Si, V_{bs} is the body-to-source voltage, and N_a is the bulk doping concentration. Here,

$$2\psi_b = \frac{2kT}{q} \ln\left(\frac{N_a}{n_i}\right) \tag{30}$$

From (29) and (30), we see that as the temperature is reduced, the magnitude of V_T increases. This is mainly due to an increase in the band-bending term $2\psi_b$ which is caused by the temperature dependence of the intrinsic carrier concentration n_i. The temperature dependence of n_i and the Si band-gap E_g can be expressed as [47]

$$n_i = 3.34 \times 10^{19} \left(\frac{T}{300}\right)^{3/2} e^{\left(\frac{-E_g}{2kT}\right)} \quad [cm^{-3}] \tag{31}$$

$$E_g = 1.16 - 7.02 \times 10^{-4} \frac{T^2}{T + 1108} \quad [eV] \tag{32}$$

Equations (31) and (32) indicate that the Si band-gap increases and the n_i decreases with decrease in temperature, thus contributing to the increase in the band-bending term. The temperature lowering also significantly affects the sub-threshold current, which is dominated by diffusion current. The drain current in the sub-threshold region can be writen as [59]

$$I_{ds} = \mu_{eff} \frac{W}{L} \sqrt{\frac{\epsilon_{Si} q N_a}{2\psi_b}} \left(\frac{kT}{q}\right)^2 \left(\frac{n_i}{N_a}\right)^2 e^{q\psi_b/kT} \left(1 - e^{-qV_{ds}/kT}\right) \tag{33}$$

where, μ_{eff} is the effective carrier mobility, and V_{ds} is the drain-to-source voltage. Thus, from (33), we can see that the sub-threshold drain current is drastically reduced at low temperatures, thereby leading to a much lesser off-current (I_{Off}). The sub-threshold slope S is an important parameter as it directly determines the I_{Off}, which is a critical design parameter in dynamic switching circuits. S is mainly an inverse function of temperature, and can be given by

$$S = \frac{d(\log_{10} I_{ds})}{dV_{gs}} = \frac{q}{2.3\ mkT} \tag{34}$$

where, m is the ideality factor. m can be written as

$$m = 1 \; + \; \frac{C_{dm}}{C_{ox}} \; = \; 1 \; + \; \frac{\epsilon_{Si} \; t_{ox}}{\epsilon_{ox} \; W_{dm}} \tag{35}$$

where, W_{dm} is the depletion width. The sub-threshold slope is increased substantially by lowering the operating temperature, thereby resulting in sharp turn-off characteristics. The other important device parameter is the transconductance g_m, which is proportional to the surface carrier mobility. The g_m for a MOSFET operating in the saturation region is given by

$$g_{m,sat} \equiv \; \frac{\partial I_{ds}}{\partial V_{gs}} \; = \; \mu_{eff} C_{ox} \frac{W}{L} \; (V_{gs} - V_T) \tag{36}$$

For short-channel MOSFETs, the velocity saturation limited value of the g_m is given by

$$g_{m,sat} \equiv \; \frac{\partial I_{ds}}{\partial V_{gs}} \; = \; C_{ox} W \; v_{sat} \tag{37}$$

Electron mobility improves at cryogenic temperatures owing to the reduced electron-phonon scattering at low temperatures. In addition to carrier mobilities, the saturation velocity (v_{sat}) also improves slightly at low temperatures, thus leading to an increase in the drive current and g_m.

Hence, it is expected that scaled Si-MOSFETs, even without process modifications for cryogenic operation, will exhibit enhanced performance with cooling. Much of the work in current literature has focused on the low temperature DC performance of MOSFETs for digital and low frequency analog applications [47]–[58]. However, the high-frequency performance of MOSFETs at low temperatures is a relatively less explored field and have been traditionally dominated by the $III - V$ devices [60]. Recently, Siligaris, *et. al.*, have reported the microwave performance of CMOS devices at 77K [61]. This work encompasses a comprehensive study of the DC, small-signal AC, and the RF noise performance of scaled Si-MOSFETs, to further the understanding of RF CMOS performance at cryogenic temperatures.

4.3 Broadband Noise Modeling of MOSFETs at Cryogenic Temperatures

The sub-circuit model shown in fig. 10, and described in section 3.2 is used for the small-signal ac and RF noise modeling of the MOSFET. Following the discussions in sections 3.1 and 3.2, the noise model of the MOSFET can be derived for low-temperature operation. From equations 23 and 24, the equivalent voltage noise ($\overline{v_n^2}$) and current noise ($\overline{i_n^2}$) spectrum for a MOSFET operating at cryogenic temperatures can be written as

$$\overline{v_n^2} \;=\; \overline{v_{R_G}^2} \;+\; \frac{\overline{i_d^2}}{|Y_{21}|^2} \;=\; 4kT_a\;\Delta f R_G \;+\; \frac{4kT_a\;\Delta f \gamma_a g_{do}}{|Y_{21}|^2} \;=\; 4kT_o\;\Delta f R_n \tag{38}$$

$$\begin{aligned}\overline{i_n^2} \;&=\; \overline{i_{gu}^2} \;+\; |Y_{cor}|^2\overline{v_n^2} \;=\; 4kT_a\Delta f\;\beta_a\;\frac{\omega^2 C_{gs}^2}{5\;g_{do}}\;(1-|c|^2) \;+\; |Y_{cor}|^2\overline{v_n^2} \\ &=\; 4kT_o\;\Delta f\left[G_n \;+\; |Y_{cor}|^2 R_n\right]\end{aligned} \tag{39}$$

where, T_a is the device temperature, T_o is the reference temperature ($= 290K$), and γ_a and β_a are the excess noise coefficients at temperature T_a.

Using this formulation, the power spectral densities of the channel thermal noise, induced gate noise, and their cross-correlation can be extracted as follows:

$$\frac{\overline{i_d^2}}{\Delta f} \;=\; 4kT_a\;\Delta f\gamma_a g_{do} \;=\; 4kT_o\;\left(R_n \;-\; \frac{T_a}{T_o}R_G\right)\;|Y_{21}|^2 \tag{40}$$

$$\begin{aligned}\frac{\overline{i_g^2}}{\Delta f} \;&=\; 4kT_o\;R_n\;\times \\ &\left\{|Y_{opt}|^2 - |Y_{11}|^2 + 2\Re\left[\left(\left(1 \;-\; \frac{T_a}{T_o}\frac{R_G}{R_n}\right)Y_{11} - Y_{cor}\right)Y_{11}^*\right] \;+\; \frac{T_a}{T_o}\frac{R_G}{R_n}|Y_{11}|^2\right\}\end{aligned} \tag{41}$$

$$\frac{\overline{i_g\ i_d^*}}{\Delta f} \;=\; 4kT_o\ R_n\ \left\{\left[\left(1\ -\ \frac{T_a}{T_o}\frac{R_G}{R_n}\right)Y_{11} - Y_{cor}\right]Y_{21}^*\right\} \tag{42}$$

From (40), the excess noise coefficient γ_a can be expressed as

$$\gamma_a = \left(\frac{T_o}{T_a}\ R_n\ -\ R_G\right)\frac{|Y_{21}|^2}{g_{do}} \tag{43}$$

The β_a factor can be extracted from equations (39) and (41).

The intrinsic device noise sources are extracted directly from the measured S-parameters and broadband noise parameters of the device. The evolution of the noise sources across temperature for a scaled Si-MOSFET is presented in the following sections. The calculated noise sources are applied to the sub-circuit model to obtain the simulated RF noise parameters.

4.4 Small-Signal Operation of 0.18 μm MOSFETs at Liquid Nitrogen Temperature (77 K)

The cryogenic small-signal AC performance of MOSFETs from a commercially available 0.18 μm technology node is presented in this section and was published in [62].

4.4.1 Device Technology and Experiment

The MOSFETs used in this study have a minimum drawn gate length of 0.18 μm and an oxide thickness of 3.5 nm. The RF test structures employ a multi-finger gate layout to minimize gate resistance. For this study, we have characterized RF nFETs with a drawn gate length of 0.18 μm and a finger width of 10 μm with 8 fingers.

The devices were characterized on an open-cycle cryogenic probing system, as described in section 4.1.2. Liquid nitrogen was used as the cryogen and measurements were performed at temperature points from 300 K down to 77 K. The S-parameters of the DUTs were measured from 1 GHz - 35 GHz using the Agilent 8510C VNA.

LRRM calibration was performed at each temperature point and the conventional open-short de-embedding was used to eliminate the pad parasitics and obtain the intrinsic S-parameters of the MOSFET.

4.4.2 DC Performance

The output characteristics of the nFET at 300K and 77K are shown in Fig. 30. It is observed that the peak saturation drain current improves by about 40% when the device is cooled to 77K. Figure 31 shows the DC transfer characteristics (I_D vs. V_{GS})

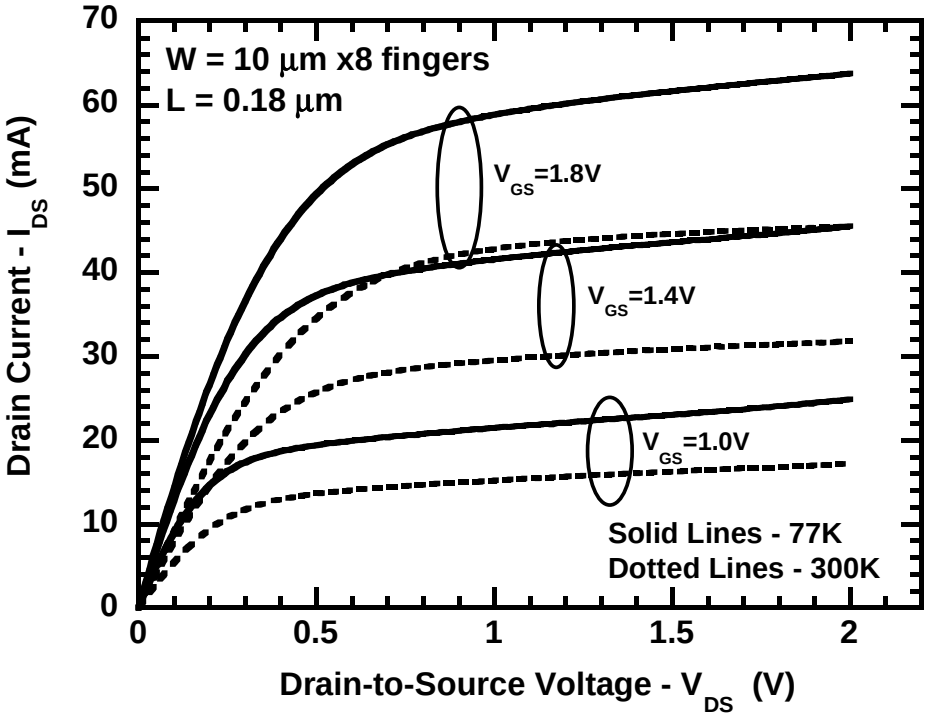


Figure 30: Drain current as a function of drain-to-source voltage, at 300K and 77K of the nFET.

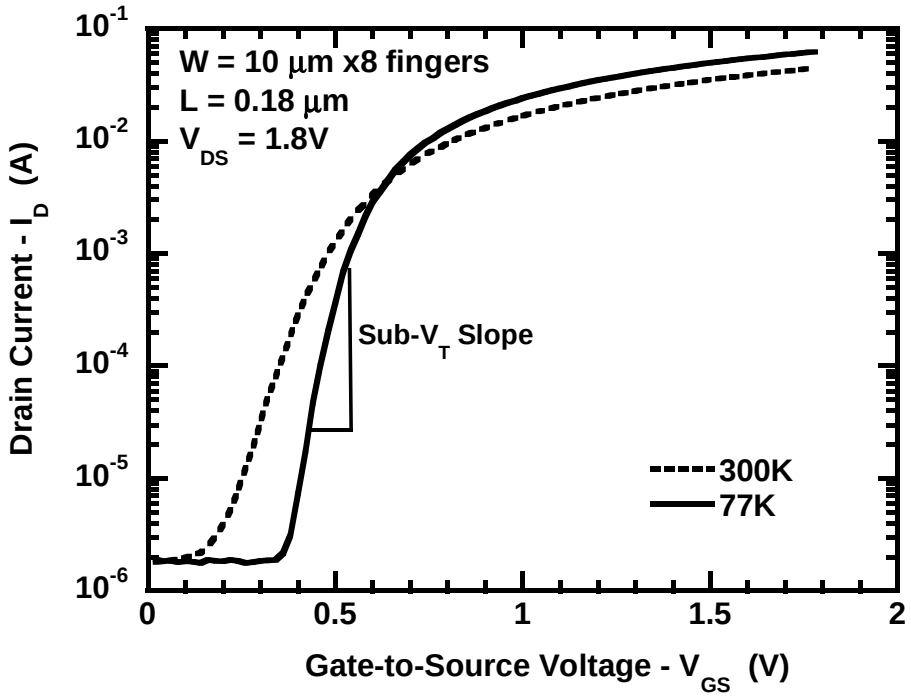


Figure 31: Drain current as a function of gate-to-source voltage, at 300K and 77K

The gate voltage swing per decade of I_D is reduced from about 100 mV/decade at 300 K to about 31 mV/decade at 77 K, thus resulting in an improvement in the sub-threshold slope (S) by a factor of 3.3. This would allow for an appreciable reduction in operating power supply voltage at low temperatures. The threshold voltage (V_T) of the nFET increases as the temperature decreases, as explained in section 4.2. For the nFET biased in saturation the increase in V_T at 77 K is about 110 mV ($V_T{}^{300K}$=0.35 V, $V_T{}^{77K}$=0.46 V). The drain-induced barrier lowering (DIBL) can be quantified by the DIBL coefficient R, that is defined as [63]:

$$R = -\frac{\delta V_T}{\delta V_{DS}} \tag{44}$$

is about 41.2mV/V at 300K and 77 K, corresponding to V_T values extracted at V_{DS} of 1.8V and 0.1V. DIBL thus remains a concern for this technology, even at 77 K. Fig. 32 shows the transconductance (g_m) as a function of gate-to-source voltage at various temperature points. The peak g_m in saturation region (V_{DS}=1.8V) increases

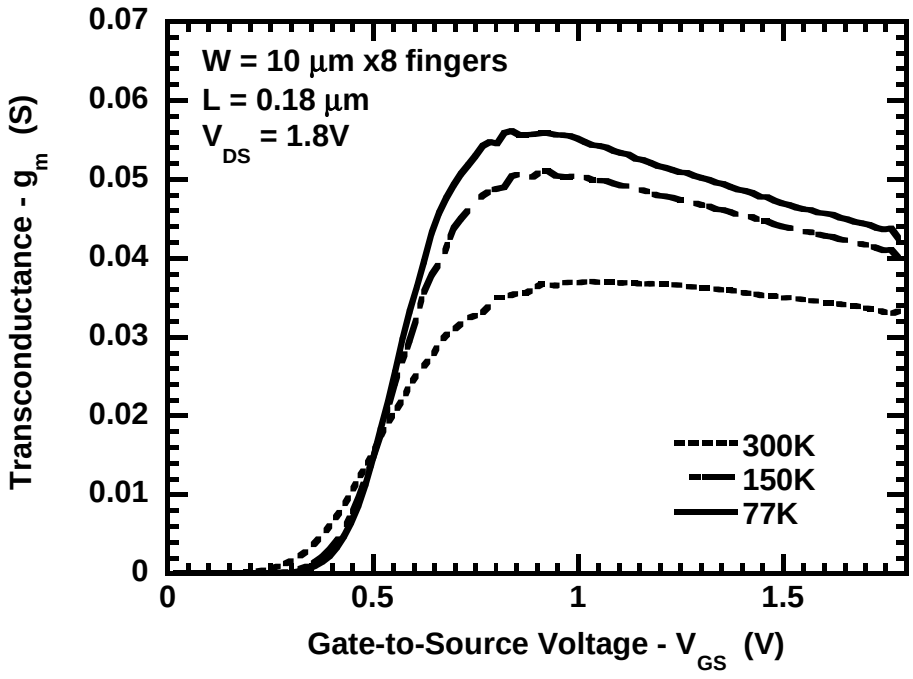


Figure 32: Transconductance as a function of gate-to-source voltage at various temperatures

from about 38 mS at 300 K to about 60 mS at 77 K. The g_m enhancement is mainly attributed to the increase in effective carrier mobility at low temperatures (from equation 36).

4.4.3 Small-Signal AC Performance

The small-signal analysis is carried out using the equivalent circuit model illustrated in fig. 10, described in section 3.2. The small-signal parameters are extracted from the measured and de-embedded Y-parameters of the nFET and are enumerated in Table 2, at 300 K and 77 K. The channel resistance r_{ch} is inversely proportional to g_m and hence decreases at low temperature. The decrease in the gate resistance R_G at 77 K is due to lower poly/silicide resistances at low temperatures. The capacitances are almost invariant with temperature. The AC transconductance (g_m) and g_{ds} increase with decrease in temperature, largely due to increase in the effective mobility. The two important RF figures of merit are the cut-off frequency (f_T) and the maximum

Table 2: Small Signal Parameters of the nFET biased at V_{GS}=1.0V and V_{DS}=1.8V, at 300 K and 77 K

Temperature	R_G	r_{ch}	C_{gs}	C_{gd}	C_{ds}	g_m	g_{ds}
300K	18.0 Ω	15.0 Ω	75.6 fF	27.0 fF	42.0 fF	39.0 mS	2.86 mS
77K	12.0 Ω	8.0 Ω	76.8 fF	28.6 fF	42.0 fF	56.0 mS	3.0 mS

oscillation frequency (f_{max}). To a first order, these parameters can be described by:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{45}$$

$$f_{max} = \frac{f_T}{2\sqrt{(R_G + r_{ch})(2\pi f_T C_{gd} + g_d)}} \tag{46}$$

The small-signal current gain (h_{21}) as a function of frequency at 300 K and 77 K is shown in Fig. 33, for the nFET biased close to the peak f_T point.

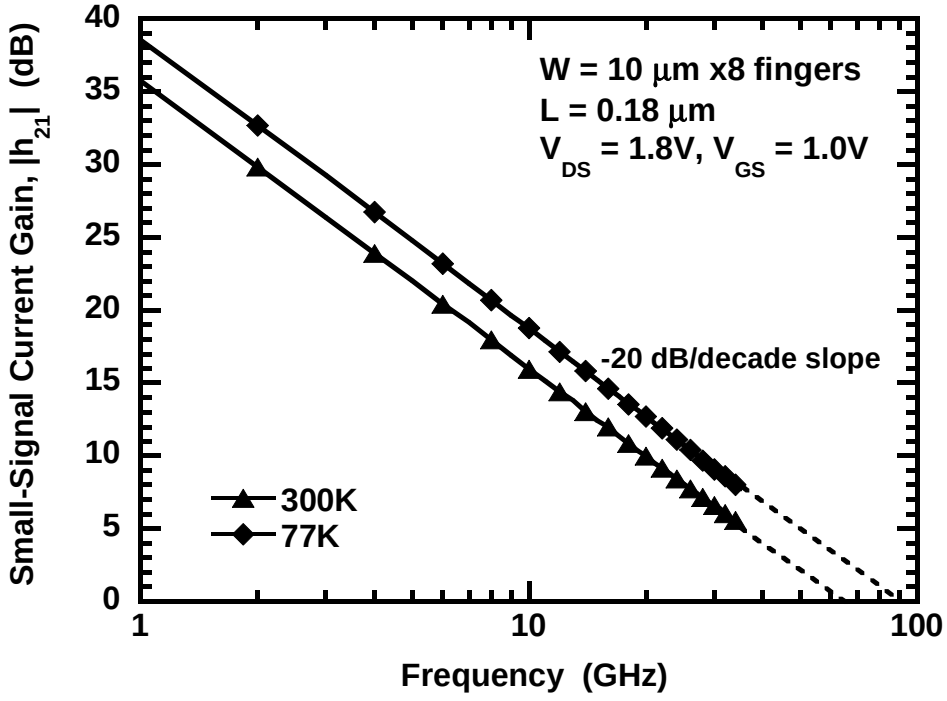


Figure 33: Small-signal current gain as a function of frequency at 300K and 77K

An ideal -20dB/decade slope is observed over a broad frequency band. The extracted f_T vs. drain current is plotted in Fig. 34. An increase in peak f_T from 63 GHz at 300 K to 90 GHz at 77 K is observed, which is due to the increase in g_m at low temperatures (45). The f_{max} of the nFET is extracted from the unilateral power gain

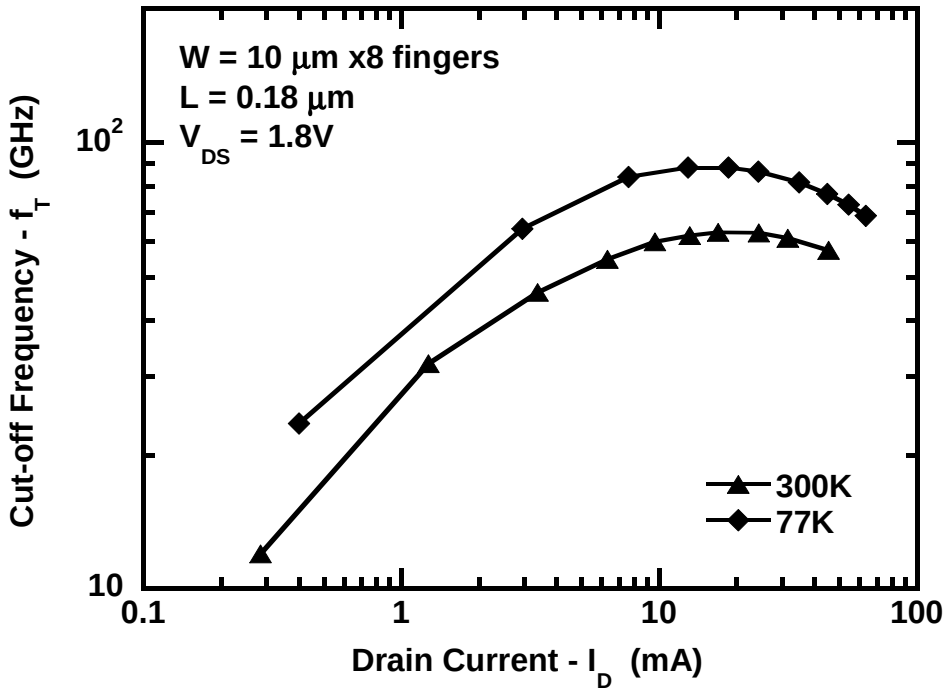


Figure 34: Cut-off Frequency as a function of drain current at 300K and 77K

of the device and is plotted as a function of drain current in Fig. 35. The peak f_{max} increases from 50 GHz at 300 K to about 78 GHz at 77 K. This improvement in f_{max} at 77 K is attributed to the decrease in r_{ch} and R_G, coupled with the increase in g_m (46). Thus, we observe that the variation of g_m, g_{ds} and the access resistances with temperature has a great impact on the RF figures of merit - f_T and f_{max}. For this 0.18 μm CMOS technology, we observe a 56% improvement in peak f_{max} and a 43% improvement in the peak f_T going from room temperature to 77 K.

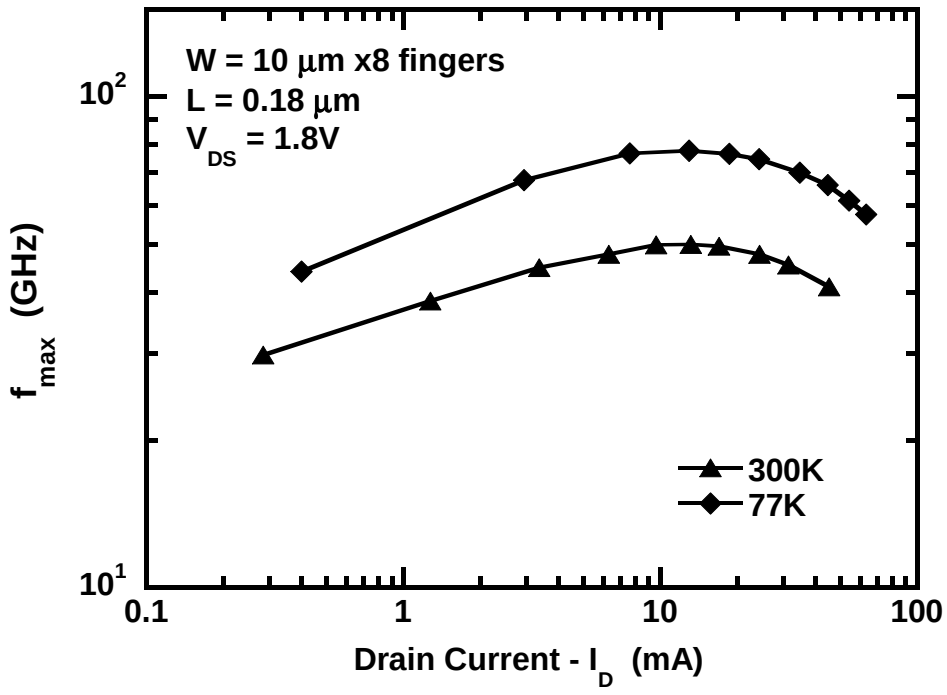


Figure 35: Maximum Frequency of Oscillation as a function of drain current at 300K and 77K

4.5 Cryogenic Performance of 130 nm MOSFETs

In this section, a comprehensive analysis of the DC, small-signal AC, and broadband noise performance of 130 nm Si-MOSFETs is presented. The hot carrier degradation mechanisms at liquid nitrogen temperature (77 K) is investigated for this technology.

4.6 Device Technology and Measurement

The MOSFETs used in this study are contained in a fully integrated, commercially available 0.13 μm CMOS technology [41], [42]. The DUTs used for our analysis are nFETs with a W/L of $2.0\mu m/0.12\mu m$ (32 gate fingers) and a W/L of $4.0\mu m/0.12\mu m$ (32 gate fingers). The RF test structures employ a multi-finger gate layout.

The on-wafer cryogenic characterization of the device samples was performed using an open-cycle cryogenic probing system, as described in section 4.1.2. The devices were cooled using liquid nitrogen and liquid helium, and the measurements were

performed at 77 K and 10 K. The S-parameters were measured from 500 MHz to 35 GHz using an Agilent 8510C VNA. The measured S-parameters were de-embedded using the corresponding open and short test structures to eliminate the effects of pad parasitics. The high-frequency noise parameters were measured from 2 GHz to 15 GHz using the ATN-NP5B noise measurement system, as described in section 2.3. The device noise sources are extracted from the measured Y-parameters and noise parameters using the procedure described in section 4.3.

4.7 DC Performance

The output characteristics of the nFET is shown in fig. 36 at 300K, 77K and 10K. The peak saturation drain current shows about a 35% improvement when the device is cooled to 77 K. This is due to the increase in the effective carrier mobility with decrease in temperature. The peak low-field mobility (μ_{eff}) is plotted as a function

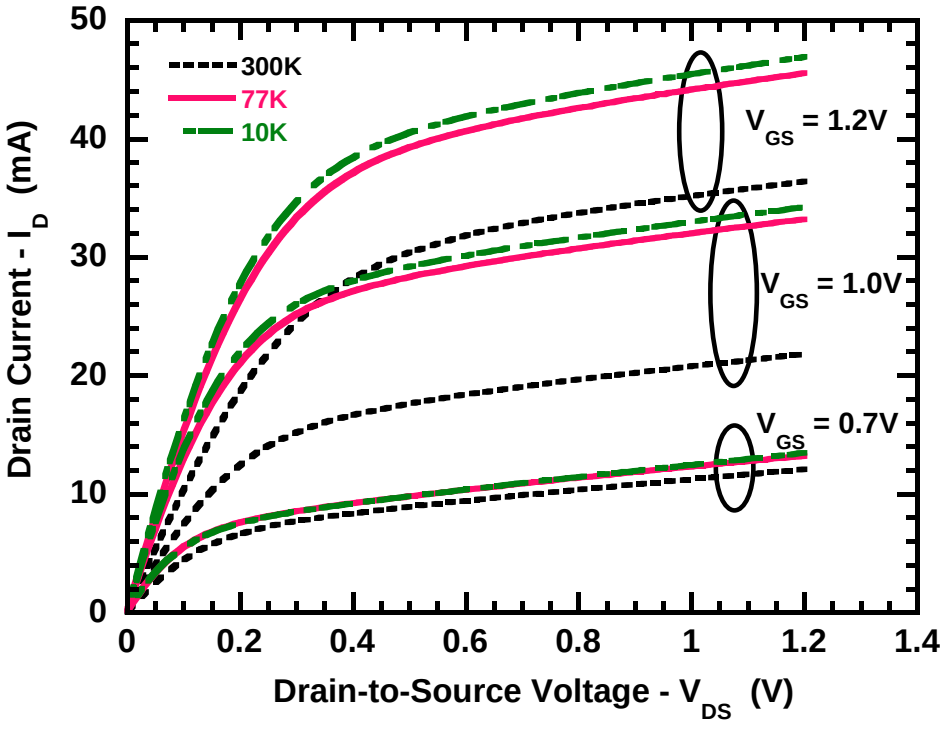


Figure 36: Drain current as a function of drain-to-source voltage, at 300 K, 77 K, and 10 K.

of temperature in fig. 37. The μ_{eff} improves by about 1.7 times on cooling to 77 K and about 1.85 times at 10 K, owing to the decrease in phonon scattering. The

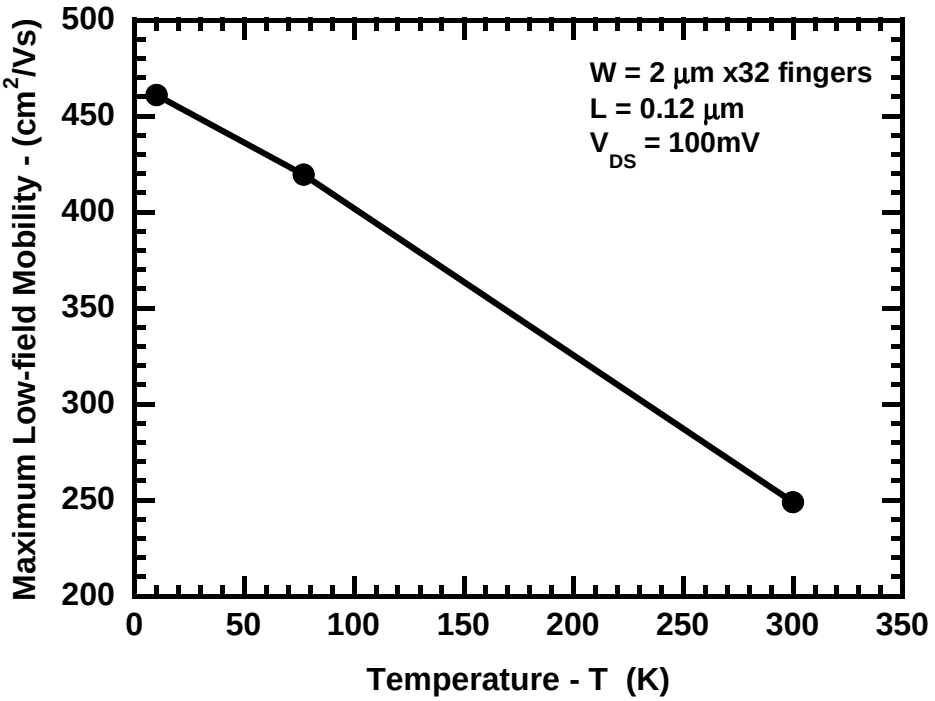


Figure 37: Peak low-field mobility for the nFET as a function of temperature.

improvement in peak saturation drain current is not very significant when the device is cooled from 77 K to 10 K. This is owing to carrier velocity saturation in these short-channel FETs. The carrier velocity saturation occurs at lower critical electric fields with cooling due to higher carrier mobilities, and hence limits the peak saturation drain current. The saturation velocity for the 0.12 μm nFETs used in this study improves by a factor of about 1.38 on cooling to 77 K, as shown in fig. 38. It is also interesting to note that the output characteristics of the nFET (refer fig. 36) does not exhibit the kink effect in saturation region at 10 K, as observed in [52]. The kink effect does not affect short-channel MOSFETs at very low temperatures as the carrier freeze-out in the bulk does not affect the surface layer to a large extent. However, the peak drive current in the saturation region is largely limited by the velocity saturation as we cool down to 10 K. The DC transfer characteristics of the device is shown in

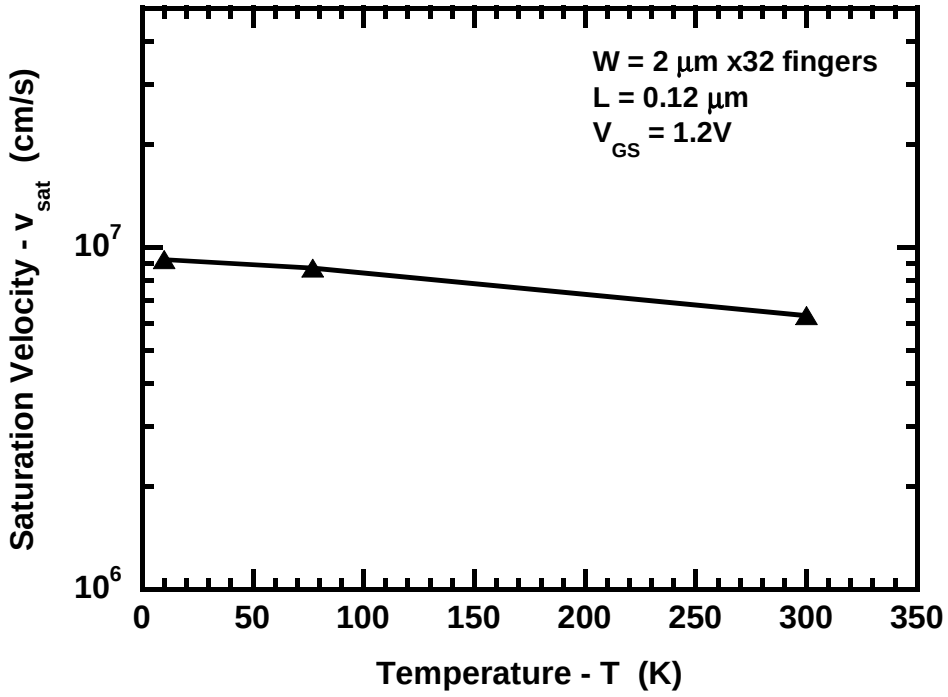


Figure 38: Saturation Velocity for the nFET as a function of temperature.

fig. 39 at 300 K and 77 K. The subthreshold slope is improved by a factor of 3 at 77 K as expected from (34), and hence results is very low off-state leakage. This is especially important in achieving good switching behavior. The threshold voltage of the device increases on cooling to 77 K, because of the increase in the band-bending term at low temperatures. For the nFET biased in saturation the increase in V_T at 77 K is about 80 mV ($V_T{}^{300K}$=0.33 V, $V_T{}^{77K}$=0.41 V). The g_m versus drain-current is plotted in fig. 40 at 300 K and 77 K. The peak g_m increases from about 50 mS at room temperature to 70 mS at 77 K. The increase in the drive current and g_m at 77 K is because of the increase in the surface mobility of the carriers.

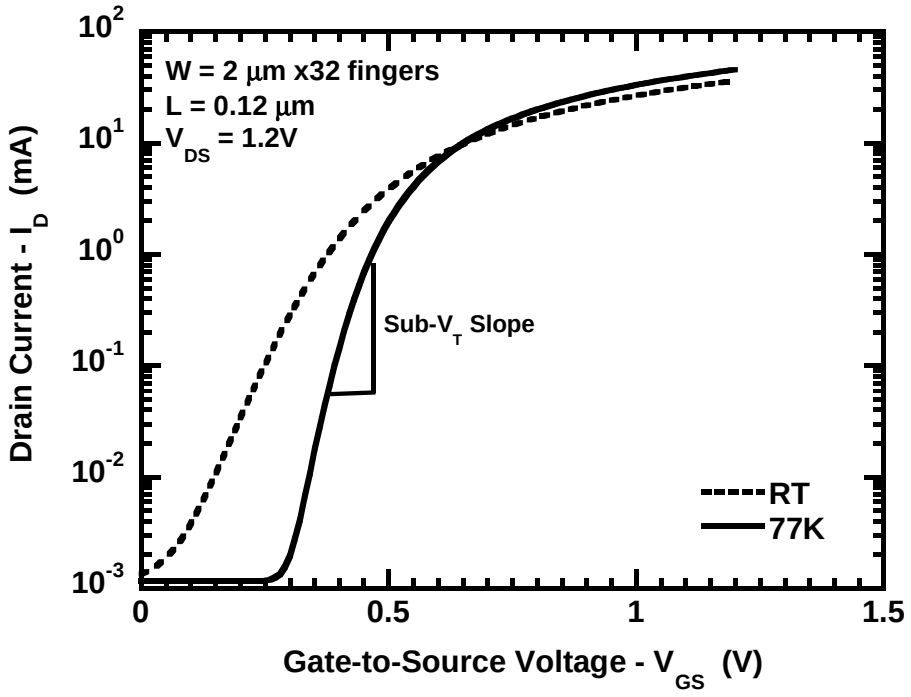


Figure 39: Drain current as a function of gate-to-source voltage, at 300 K and 77 K.

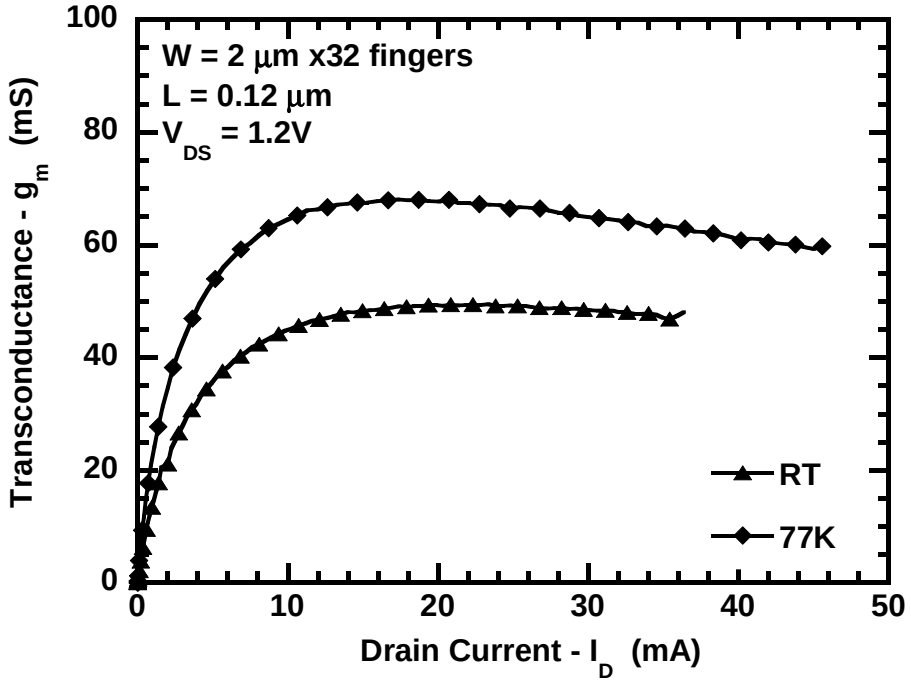


Figure 40: Transconductance as a function of drain current at 300 K and 77 K.

4.8 Small-Signal AC and Broadband Noise Performance

The equivalent circuit model illustrated in fig. 10, is used for the small-signal and high-frequency noise analysis. The intrinsic small-signal parameters are extracted from the measured and de-embedded Y-parameters of the nFET are enumerated in Table 3, at 300 K and 77 K. The decrease in R_G at 77 K is owing to the decrease in

Table 3: Small Signal Parameters of the nFET biased at V_{GS}=0.9 V and V_{DS}=1.2 V, at 300 K and 77 K

Temperature	R_G	r_{ch}	C_{gs}	C_{gd}	g_m	g_{ds}
300K	5.2 Ω	6.5 Ω	66.3 fF	29.2 fF	53.0 mS	6.5 mS
77K	2.1 Ω	2.8 Ω	64.0 fF	28.5 fF	71.0 mS	8.3 mS

the poly-silicide resistance and the contact resistances. The decrease in the channel resistance r_{ch} and the increase in g_m and g_{ds} at low temperatures is due to the increase in the surface mobility of the charge carriers. The r_{ch} tends to increase at high gate bias conditions owing to velocity saturation. The small-signal current gain (h_{21}) is plotted versus frequency in fig 41. An ideal -20 dB/decade slope is obtained at 300 K and 77 K. The cut-off frequency f_T is extracted from the extrapolated h_{21}. Figure 42 shows the extracted f_T plotted as a function of the drain current at 300 K and 77 K. The increase in peak f_T from 88 GHz at room temperature to 126 GHz at 77 K is attributed to the increase in g_m at 77 K. The f_{max} is extracted from the unilateral gain of the device. Figure 43 shows the extracted f_{max} as a function of the drain current at 300 K and 77 K. The peak f_{max} increases from 94 GHz at 300 K to 128 GHz at 77 K. This is driven by the increase in g_m and the decrease in R_G with cooling. Thus, the enhancement in the device transport properties at 77 K results in a significant improvement in the high-frequency figures of merit of the nFET.

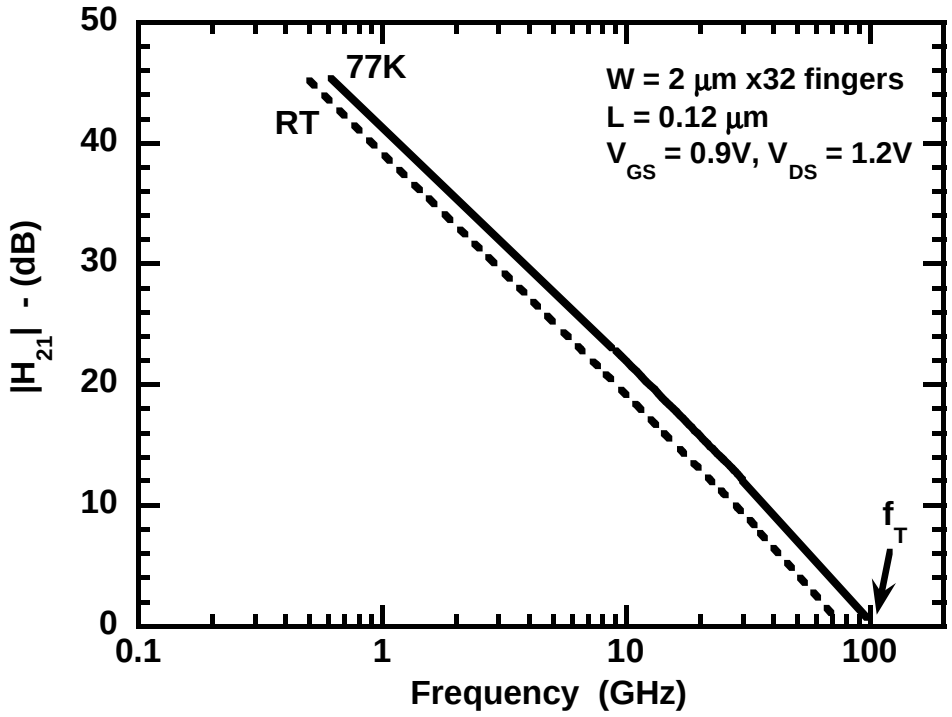


Figure 41: Small-signal current gain as a function of frequency at 300 K and 77 K

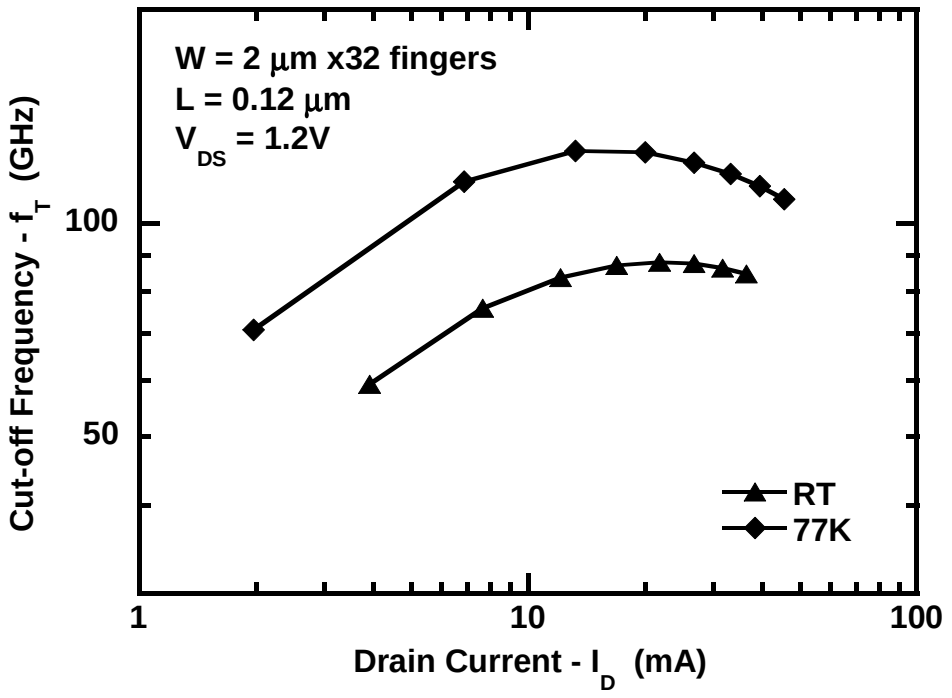


Figure 42: Cut-off Frequency as a function of drain current at 300 K and 77 K

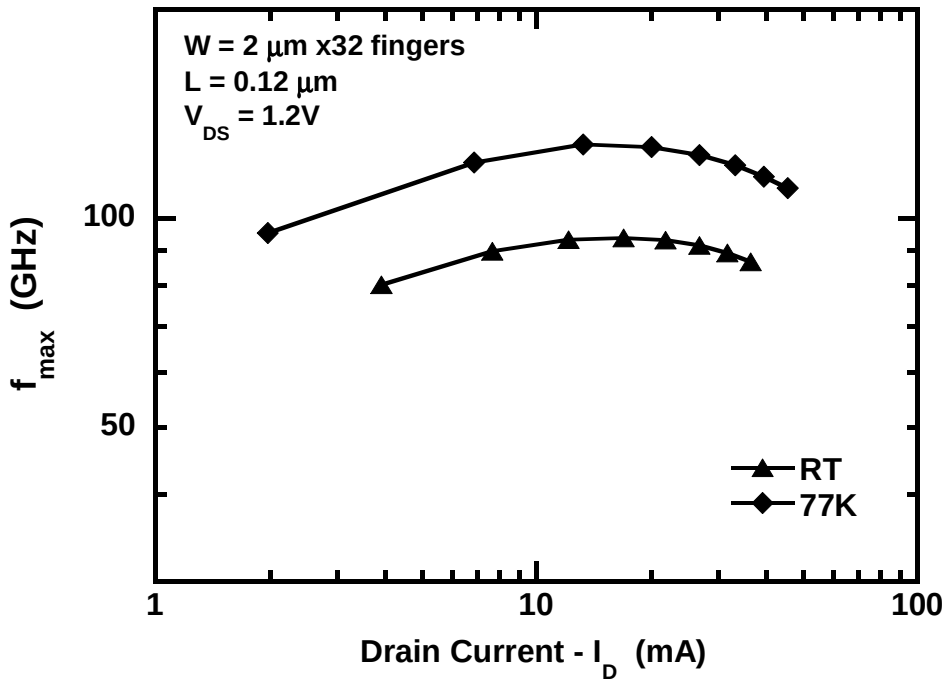


Figure 43: Maximum Frequency of Oscillation as a function of drain current at 300 K and 77 K

The channel thermal noise and the induced gate noise were extracted from the measured Y-parameters and noise parameters at 300 K and 77 K. Figure 44 shows the frequency dependence of the channel thermal noise and the induced gate noise. The drain current noise is fairly independent of frequency, whereas the induced gate noise increases as a square of the frequency. This is because of the capacitive coupling of the gate noise through the gate oxide capacitance. The variation of $\overline{i_d^2}$ and $\overline{i_g^2}$ as a function of drain current is plotted in fig. 45. It is interesting to note that the magnitude of the channel thermal noise stays relatively constant as the nFET is cooled down. From (40), one would expect the channel thermal noise to decrease as T_a goes down from 300 K to 77 K. The decrease in T_a is countered by the increase in the channel conductance g_{do} with cooling because of enhanced carrier mobility. The channel thermal noise increases with increase in gate bias. The induced gate noise decreases at 77 K owing to the decrease in the effective channel resistance (r_{ch}) with

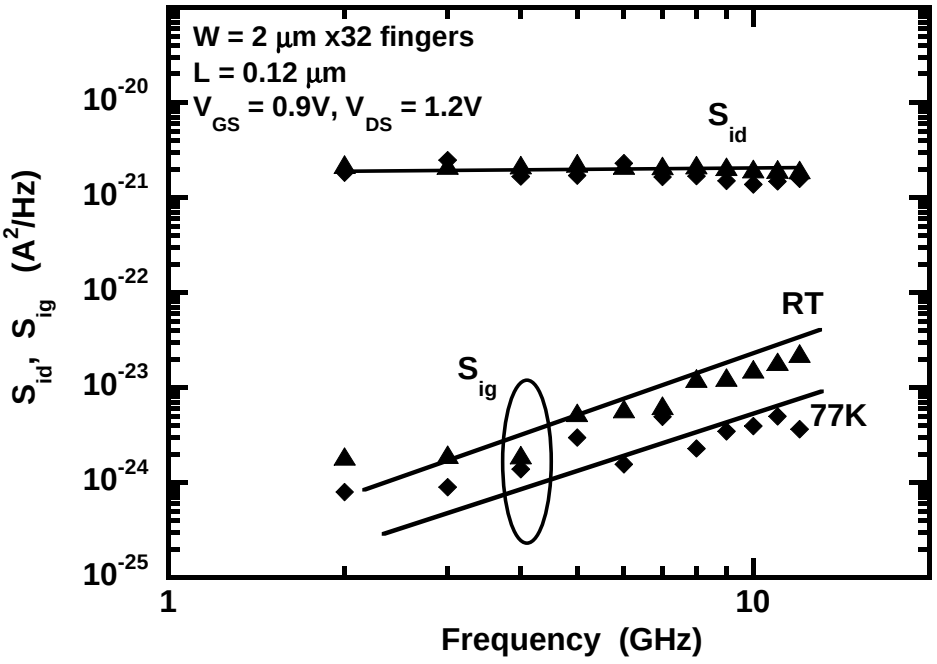


Figure 44: Frequency dependence of channel thermal noise ($\overline{i_d^2}$) and gate current noise ($\overline{i_g^2}$) for an nFET with $W/L = 2.0/0.12$ (32 fingers) at 300 K and 77 K.

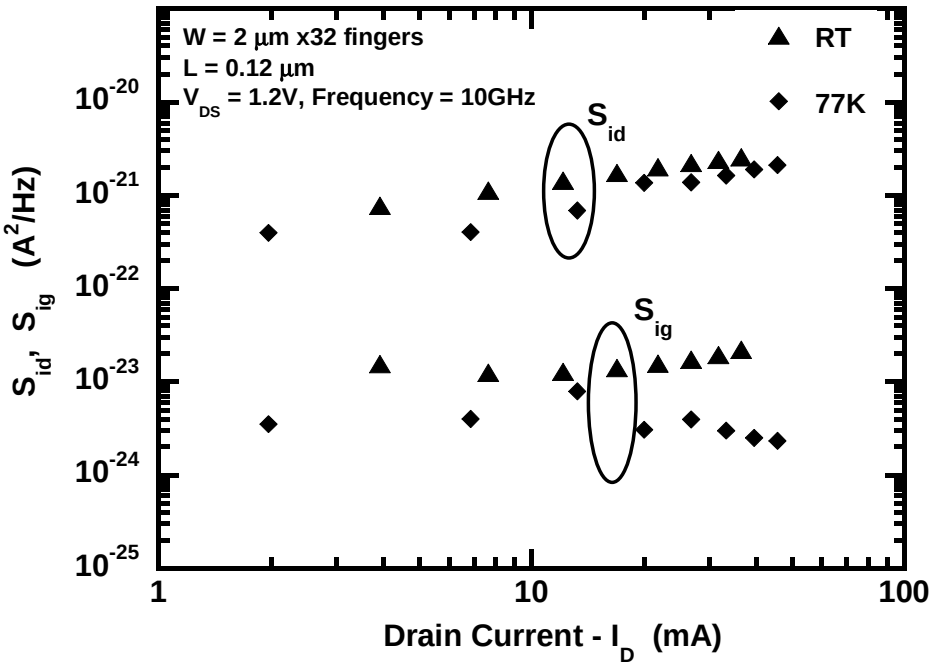


Figure 45: Bias dependence of channel thermal noise ($\overline{i_d^2}$) and induced gate noise ($\overline{i_g^2}$) for an nFET with $W/L = 2.0/0.12$ (32 fingers) at 300 K and 77 K.

cooling. The behavior of the excess noise coefficient γ as a function of drain current is shown in fig. 46 at 300 K and 77 K. The γ factor is extracted from the drain current noise using (43).

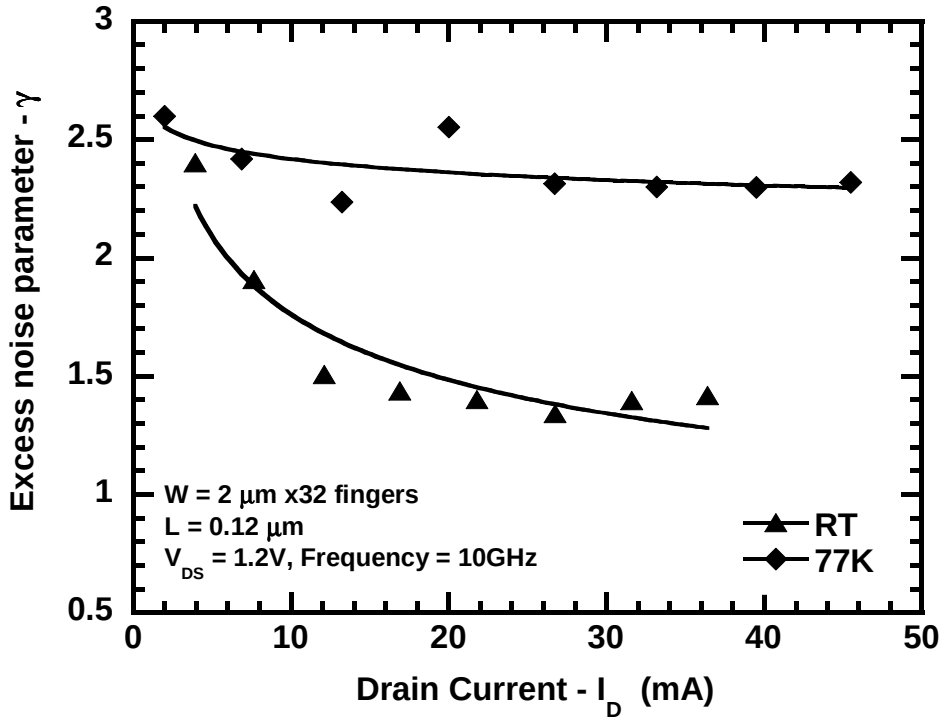


Figure 46: Bias dependence of γ for an nFET with $W/L = 2.0/0.12$ (32 fingers) at 300 K and 77 K.

The excess noise factor at 77 K can be written as

$$\gamma_{77K} \;=\; 3.8\frac{g_{do}^{300K}}{g_{do}^{77K}}\frac{\overline{i_{d77K}^2}}{\overline{i_{d300K}^2}} \;\approx\; 3.8\frac{g_{do}^{300K}}{g_{do}^{77K}}\,\gamma_{300K} \tag{47}$$

From fig. 46, we see that in addition to the enhanced transport properties of the channel, the increase in γ with cooling makes the drain current noise ($\overline{i_d^2}$) at 77 K have the same order of magnitude as in the room temperature condition. This increase in γ at low temperatures could be attributed to enhanced carrier heating.

The extracted noise sources are used with the sub-circuit model to obtain the simulated RF noise parameters. The measured and modeled minimum noise figure (NF_{min}) is plotted as a function of frequency in fig. 47. The error in the measured

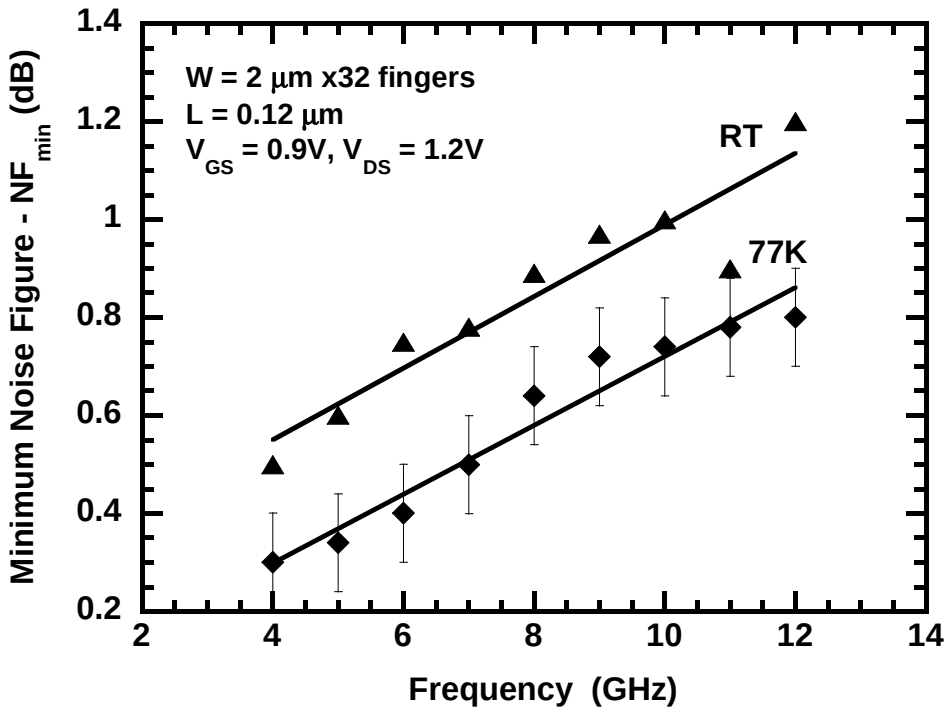


Figure 47: Measured and modeled NF_{min} versus frequency – for an nFET with $W/L = 2.0/0.12$ (with 32 fingers) at 300 K and 77 K.

NF_{min} values is of the order of $\pm 0.1dB$ and are shown in fig. 47. The NF_{min} of this device decreases from about 1 dB at 300 K to 0.68 dB at 77 K at a frequency of 10 GHz. The decrease in NF_{min} is primarily due to the increase in g_m and the decrease in R_G and other access resistances. Figure 48 shows the variation of the equivalent noise resistance (R_n) with frequency at 300 K and 77 K. We observe a strong decrease in R_n as we cool the device from 300 K to 77 K. The noise resistance at 77 K can be expressed as

$$R_n^{77K} \approx \frac{T_a}{T_o} R_G + \frac{\overline{i_{d77K}^2}}{4kT_o\, g_m^2} \tag{48}$$

Thus, from (48), we see that the decrease in R_G and increase in g_m, coupled with the decrease in the sample temperature T_a, is responsible for the decrease in R_n at 77 K. This is highly desirable for low-noise amplifier (LNA) design, as it naturally desensitizes the circuit from the source impedance mismatches. The magnitude and angle of the source reflection coefficient (Γ_{opt}) as a function of frequency is plotted

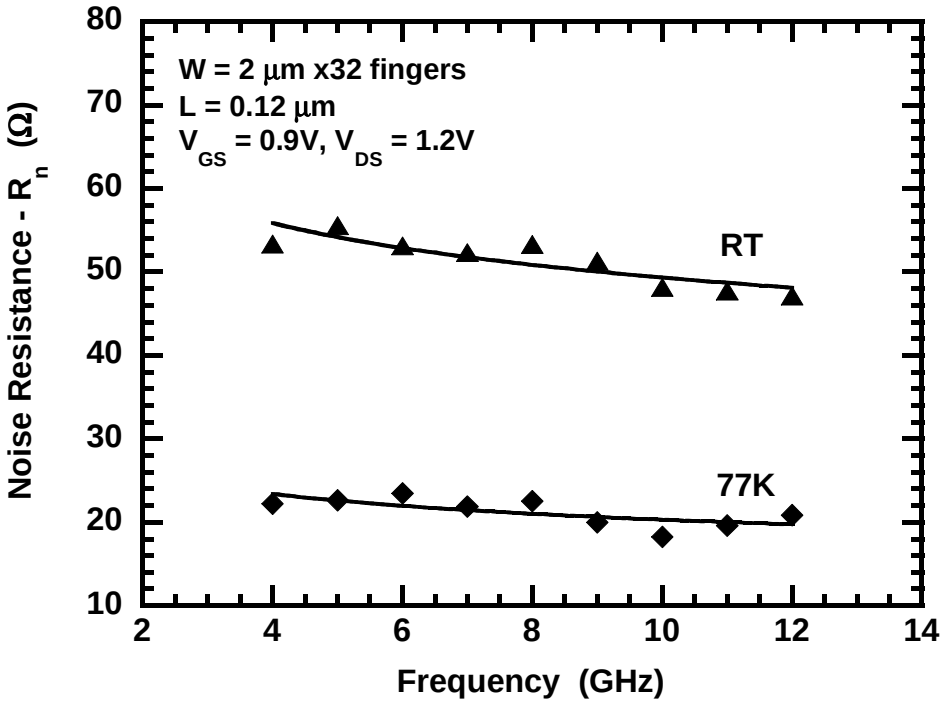


Figure 48: Measured and modeled R_n versus frequency – for an nFET with W/L = 2.0/0.12 (with 32 fingers) at 300 K and 77 K.

in figs. 49 and 50 at 300 K and 77 K. The magnitude of Γ_{opt} decreases at 77 K compared to the room temperature value, making it easier to achieve input matching for optimum noise and power performance.

Figures 51 and 52 show the measured and modeled 50Ω noise figure (NF_{50}) and R_n as a function of drain current, at 300 K and 77 K. The NF_{50} and R_n decrease with cooling, which is very good for the design of LNAs at cryogenic temperatures. The modeled data shows a good agreement with the measured noise parameters over bias and frequency.

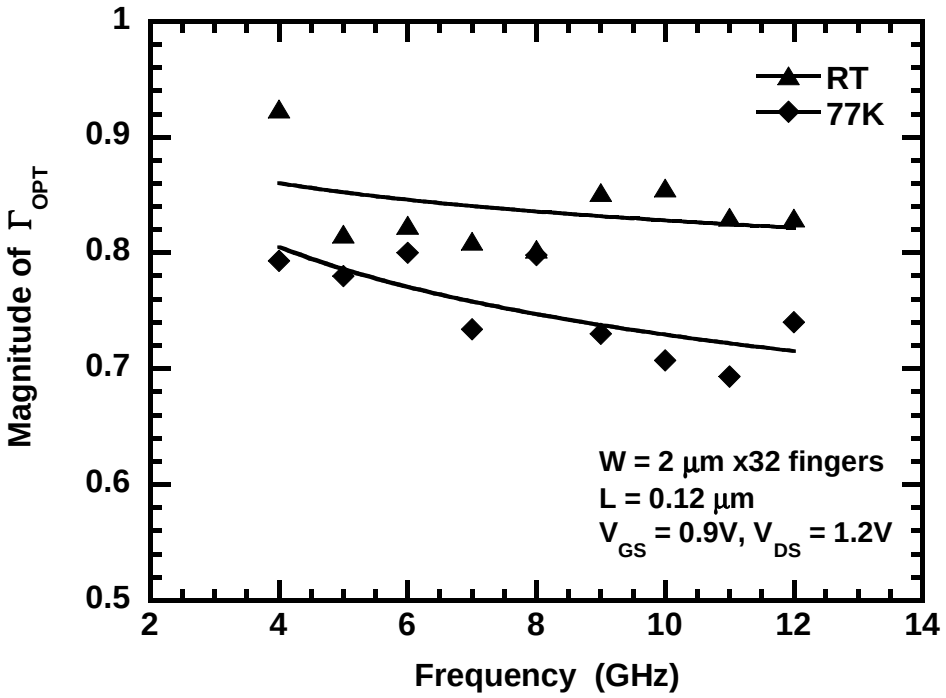


Figure 49: Measured and modeled magnitude of Γ_{opt} versus frequency – for an nFET with $W/L = 2.0/0.12$ (with 32 fingers) at 300 K and 77 K.

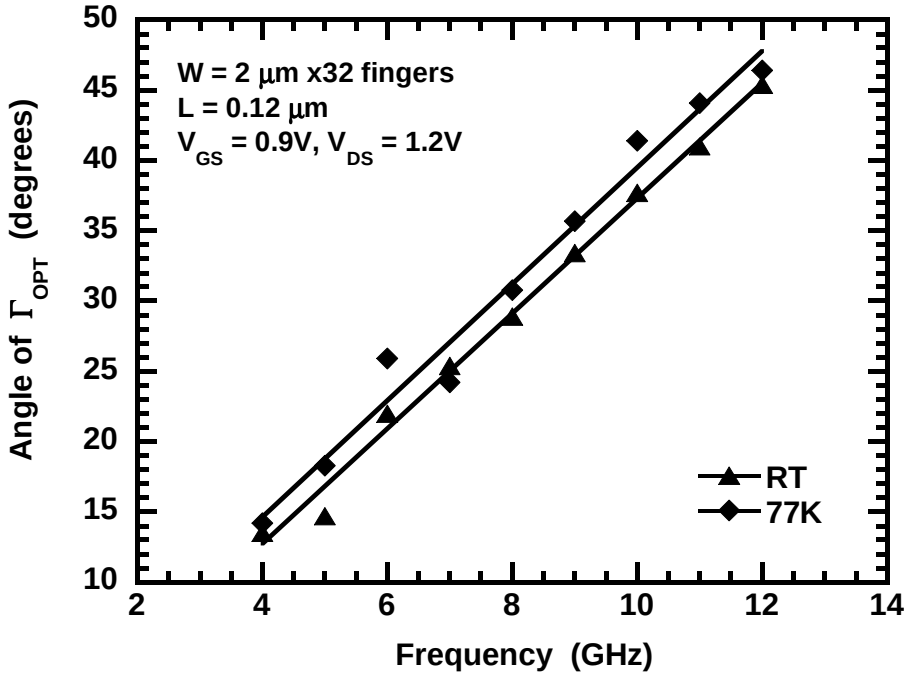


Figure 50: Measured and modeled angle of Γ_{opt} versus frequency – for an nFET with $W/L = 2.0/0.12$ (with 32 fingers) at 300 K and 77 K.

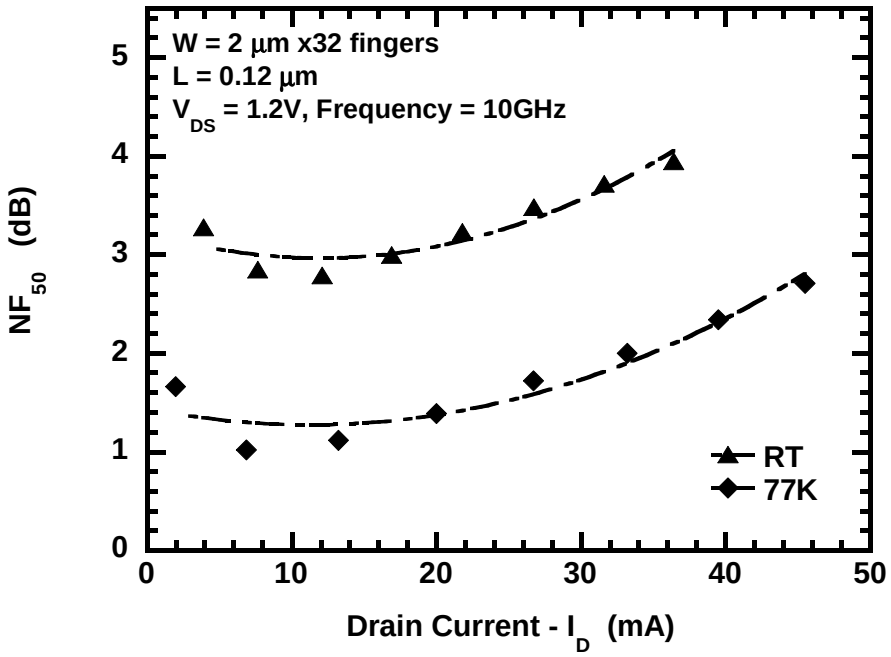


Figure 51: Measured and modeled NF_{50} versus drain current – for an nFET with $W/L = 2.0/0.12$ (with 32 fingers) at 300 K and 77 K.

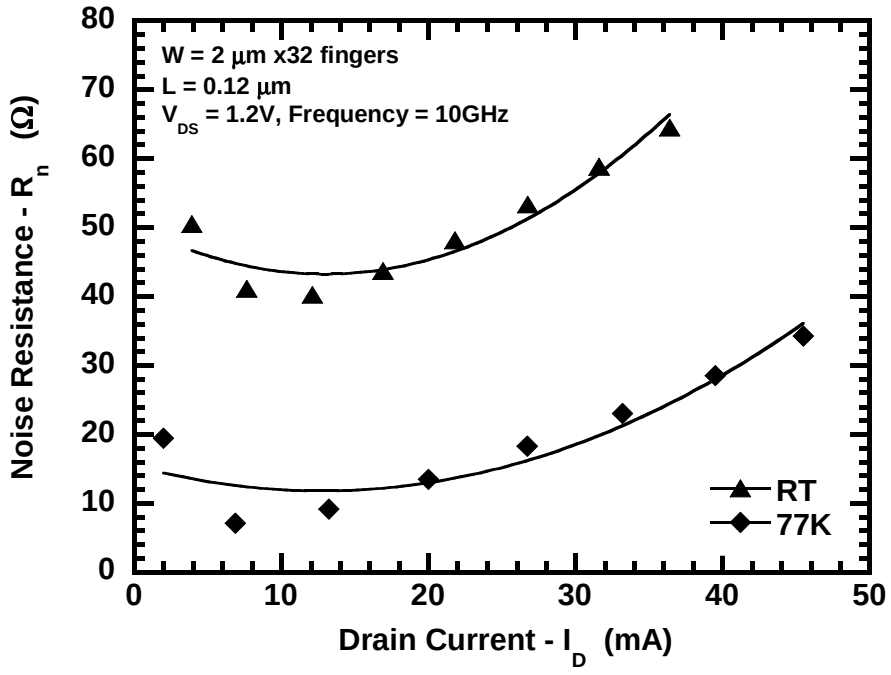


Figure 52: Measured and modeled R_n versus drain current – for an nFET with $W/L = 2.0/0.12$ (with 32 fingers) at 300 K and 77 K.

4.9 Hot-carrier Degradation of n-MOSFETs at 77 K

As discussed extensively in the previous sections, operation at cryogenic temperatures leads to a significant improvement in the DC, small-signal AC, and RF noise performance of nFETs. It is also observed that the effect of nearly all the degradation mechanisms such as electromigration and other thermally activated processes are greatly reduced at low temperatures. However, the reliability associated with hot-carrier degradation is greatly exacerbated at low temperatures. The probability that a carrier traveling in an electric field will gain sufficient energy to create impact ionization without suffering a collision can be written as $exp\left(\frac{-\Phi_b}{qE_m\lambda}\right)$, where Φ_b is the energy required for impact ionization, λ is the carrier mean free path, and E_m is the maximum electric field [64]. The reduced phonon scattering at cryogenic temperatures leads to an increase in the carrier mean free path and a concomitant increase in the kinetic energy of the channel electrons, and thus aggravates the hot-carrier effects.

Hot-carrier injection and degradation mechanisms have been studied extensively using DC voltage and current stress measurements [65]–[82]. Many mechanisms of DC device degradation have been proposed, but it is still unclear which physical characteristics of the $Si - SiO_2$ interface are affected by hot-carrier injection. In addition, the hot-carrier phenomena are strongly dependent on the gate oxide characteristics, fabrication processes, as well as the sample temperature. An illustration of the generally observed hot-carrier injection mechanisms is shown in fig. 53. The channel hot-electron (CHE) injection is caused by the injection of "lucky" electrons from the channel. For an nFET operating at $V_G = V_D$, these electrons gain sufficient energy to surmount the $Si - SiO_2$ barrier and result in a gate current (I_G). In many cases, the gate current is responsible for device degradation as a result of carrier trapping. For $V_G < V_D$, the electric field at the drain intensifies to the

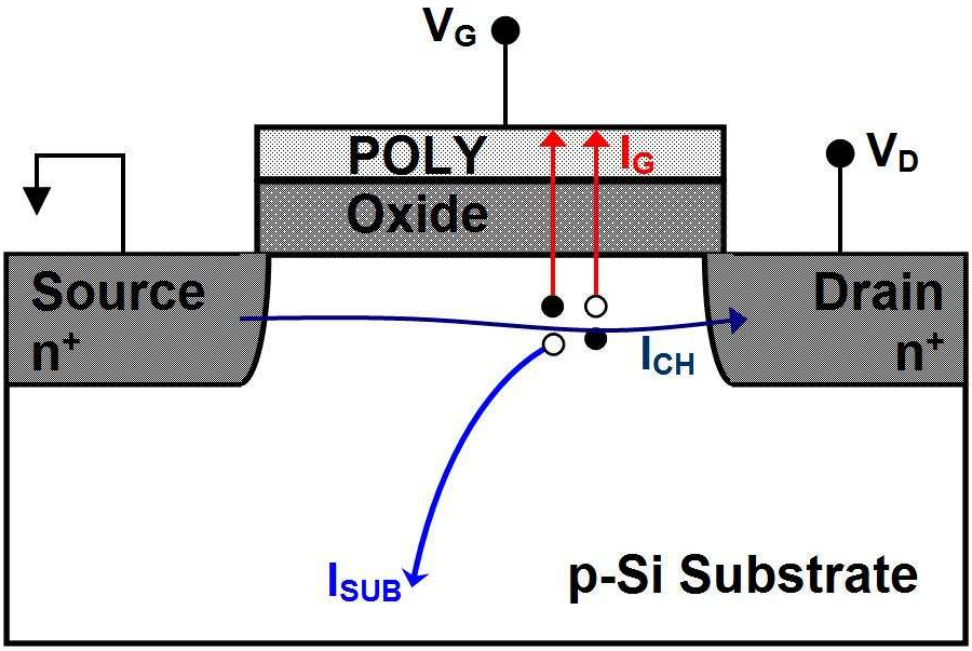


Figure 53: Hot-carrier injection mechanisms in MOSFETs.

point where avalanche multiplication due to impact ionization may substantially increase the supply of hot-electrons and hot-holes. The drain avalanche hot-carrier (DAHC) injection is observed to produce the most severe degradation and leads to a substantial increase in the substrate current (I_{sub}), threshold voltage shifts, and transconductance degradation. While it is generally accepted that the degradation is caused by the high-energy carriers generated in the high-field region, there is a considerable disagreement concerning the physical mechanisms involved. Also, the hot-carrier mechanisms at cryogenic temperatures is not very well understood. Some studies attribute the degradation of device characteristics to the presence of fixed oxide charges [67]–[69], while some studies show that the hot-carrier-induced interface state generation is the dominant mechanism [70]–[75], and other studies suggest both mechanisms are involved [76]–[78].

It is in general agreed upon that the worst-case degradation at room temperature occurs at a gate voltage corresponding to maximum substrate current (V_G @ $I_{sub,max}$)

or $V_G \simeq V_D/2$. However, the worst-case gate voltage stress condition at low temperatures is still actively debated in current literature. Some studies report that below 200 K, the worst-case degradation occurs at $V_G = V_D$ [79], [80], while some works have shown that gate voltage at maximum substrate current condition produces worst-case degradation at 77 K [74], [75]. In [81], the authors have shown that the worst-case gate voltage stress is a function of channel length, drain bias and operating temperature. Also, in [81], the authors point out that at 77 K, long-channel devices exhibit a worst-case bias condition corresponding to $I_{sub,max}$, whereas short-channel devices exhibit the worst-case bias condition corresponding to $V_G = V_D$.

In this work, the worst-case gate voltage stress condition for nFETs from a 130 nm CMOS technology is investigated at room temperature and 77 K. The impact of hot-carrier stressing on the AC performance at room temperature and 77 K is presented for the first time.

4.10 Hot-Carrier Stress Experiment

The DC hot-carrier stress measurements were performed on nFETs from a commercially available 130 nm CMOS technology. The DUTs chosen for this experiment were RF test structures with $W/L = 2.0\mu m/0.12\mu m$ (32 gate fingers). The DC hot-carrier stress experiment was performed using an Agilent 4155C semiconductor parameter analyzer. The devices were stressed at two bias conditions, namely:

- $V_{GS} = V_{DS} = 3.0V$ (maximum gate current condition)
- $V_{GS} = 1.5V$, $V_{DS} = 3.0V$ (maximum substrate current condition)

The source terminal was grounded. The stress was applied in a controlled manner over time, and was accumulated to 2000 seconds. The DUTs were stressed at room temperature as well as at 77 K. The DC and S-parameter measurements were performed for the pre and post-stress condition at 300 K and 77 K.

4.11 Results and Discussion

Figures 54 and 55 show the drain current versus V_{GS} for increasing stress time at 300 K and 77 K, respectively. It is interesting to note that there is no perceptible degradation of drain current and subthreshold slope (S) for the $V_{GS} = V_{DS}$ condition both at 300 K and 77 K. The change in the gate current after stressing was almost negligible. This indicates that the hot-electron and hot-hole injection is very small. However, a

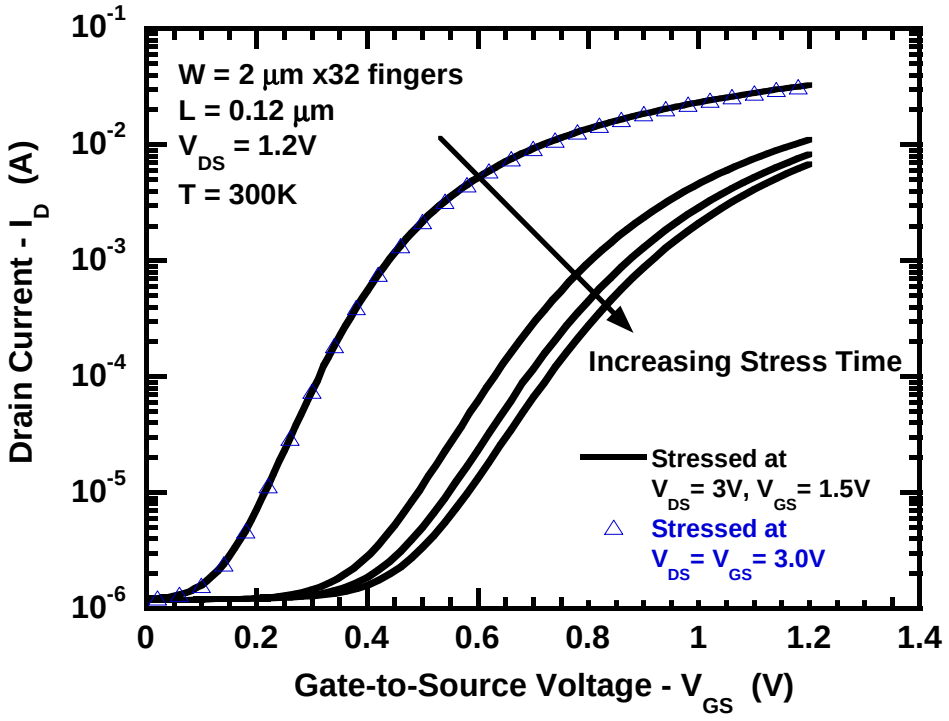


Figure 54: Drain current versus gate-to-source voltage for increasing stress time at 300 K.

significant degradation of the drain current is observed for the $V_{GS} = V_{DS}/2$ stress condition. The subthreshold slope also shows a severe degradation with increase in stress time, indicating that interface-trap generation is a dominant degradation mechanism. The percentage degradation of I_D and S is increased at 77 K than at room temperature. The gate current showed a negligible change after stressing at 300 K and 77 K, indicating that there is no significant electron trapping in the gate oxide. In the remainder of this section, the second stress condition ($V_{GS} = V_{DS}/2$) will be

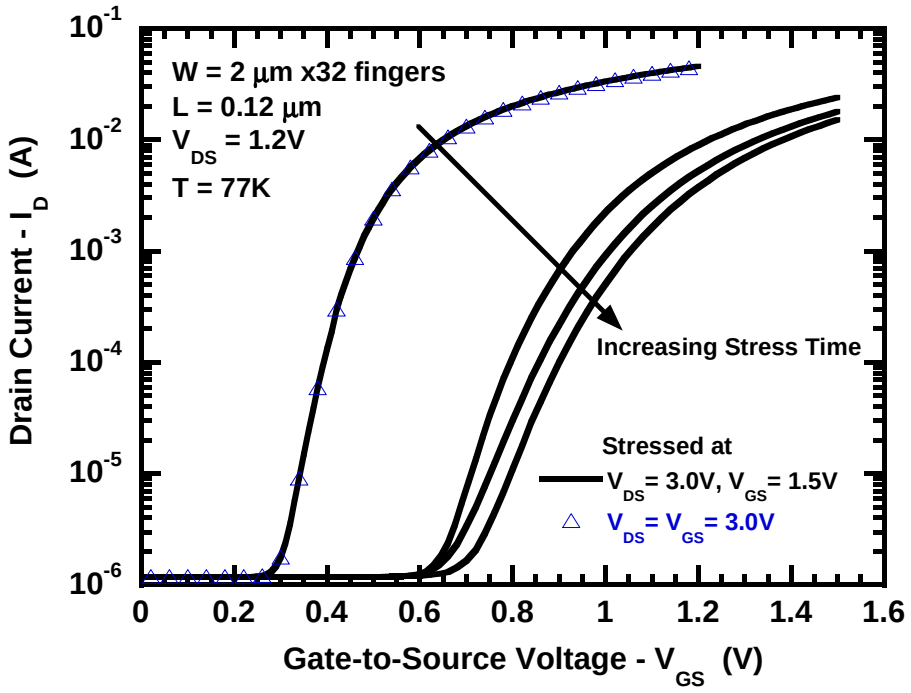


Figure 55: Drain current versus gate-to-source voltage for increasing stress time at 77 K.

discussed. Figures 56 and 57 show the transconductance degradation with increasing stress time, at 300 K and 77 K, respectively. The measured g_m shows a 35% degradation at 300 K, but a 56% degradation at 77 K for the same accumulated stress time. The larger g_m degradation at low temperature indicates a more pronounced effect of the stress-induced interface states on the effective mobility of the channel electrons. The time variation of g_m degradation is plotted in fig. **??** at 300 K and 77 K. The g_m degradation can be modeled empirically as

$$\frac{\Delta g_m}{g_{mo}} = A\, t^n \tag{49}$$

where, g_{mo} is the pre-stress value of the transconductance, A is the magnitude of the degradation, and n is the slope of a log-log plot of $\Delta g_m/g_{mo}$. The factor n is strongly dependent on V_{GS} and changes according to the hot-carrier injection mechanisms. In the case of DAHC, n is found to be between $0.5 - -1$ [65]. From fig. **??**, it is observed that n varies from about 0.53 at 300 K to about 0.8 at 77 K. This clearly

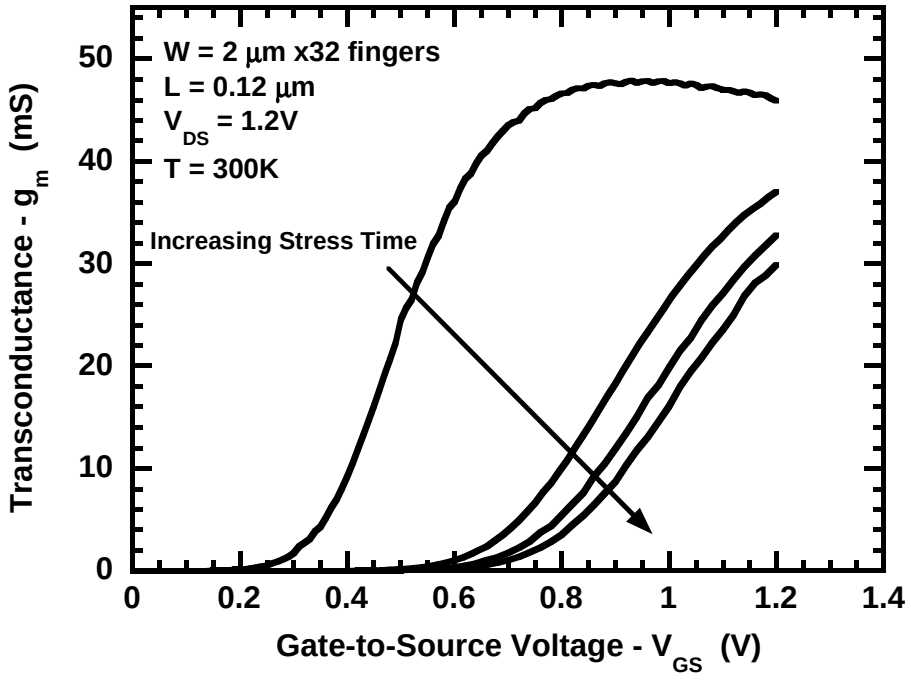


Figure 56: Transconductance versus gate-to-source voltage for increasing stress time at 300 K.

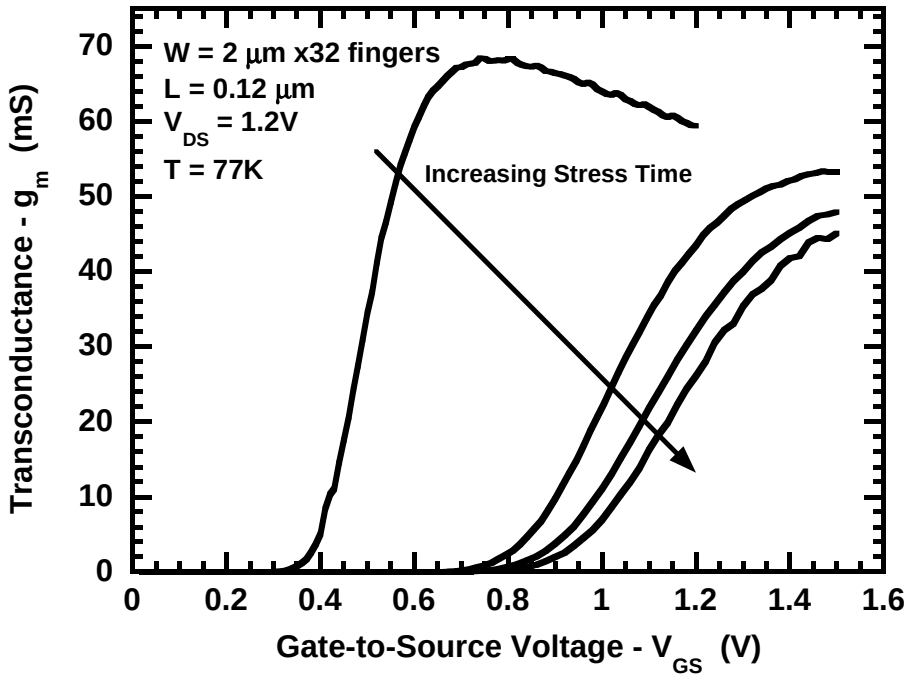


Figure 57: Transconductance versus gate-to-source voltage for increasing stress time at 77 K.

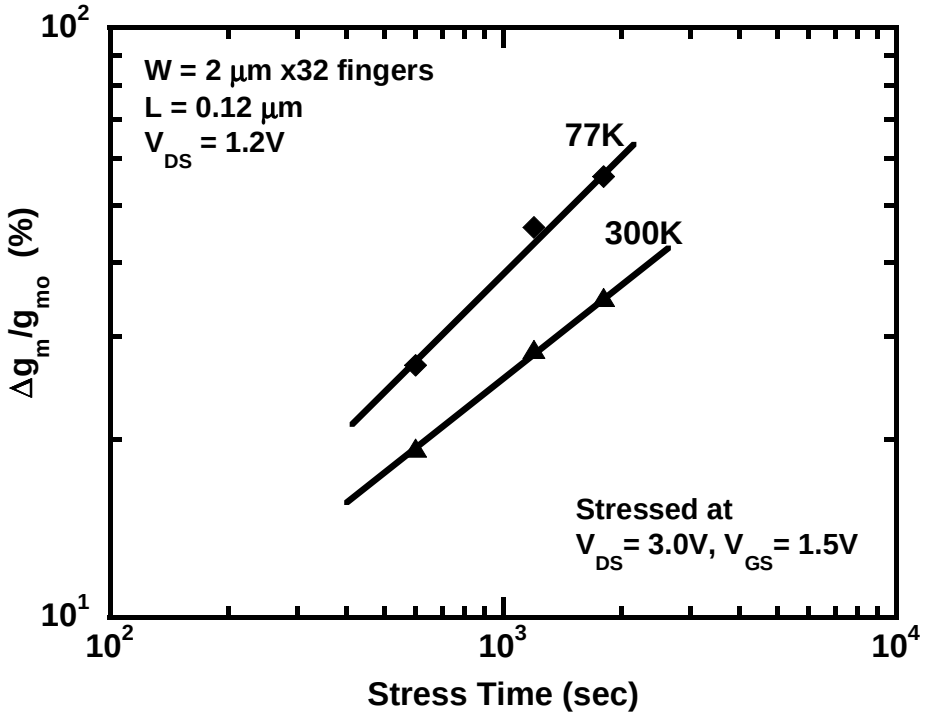


Figure 58: Time-dependent transconductance degradation at 300 K and 77 K.

indicates that hot-carrier-induced MOSFET degradation is caused by interface state generation. The time variation of V_{TH} shift is plotted in fig. 59. The saturation threshold voltage increases from $0.34V$ to $0.76V$ after stressing at 300 K, and from $0.41V$ to $0.93V$ at 77 K. The positive V_{TH} shift after stress suggests that the interface traps are acceptor type traps located mostly above the flat-band Fermi level. Thus, it is ascertained that for this 130 nm nFET, the worst-case gate voltage stress condition corresponds to the condition of maximum substrate current, as opposed to maximum gate current condition. This is quite contrary to the results reported in [81], where the authors claim a reversal in the worst-case gate voltage stress condition for the shortest channel device of the technology under consideration.

The small-signal analysis is carried out with a small-signal equivalent circuit model as shown in fig. 10. The elements of the sub-circuit model are extracted for the pre and post-stress conditions at 300 K and 77 K and are enumerated in table 4. The

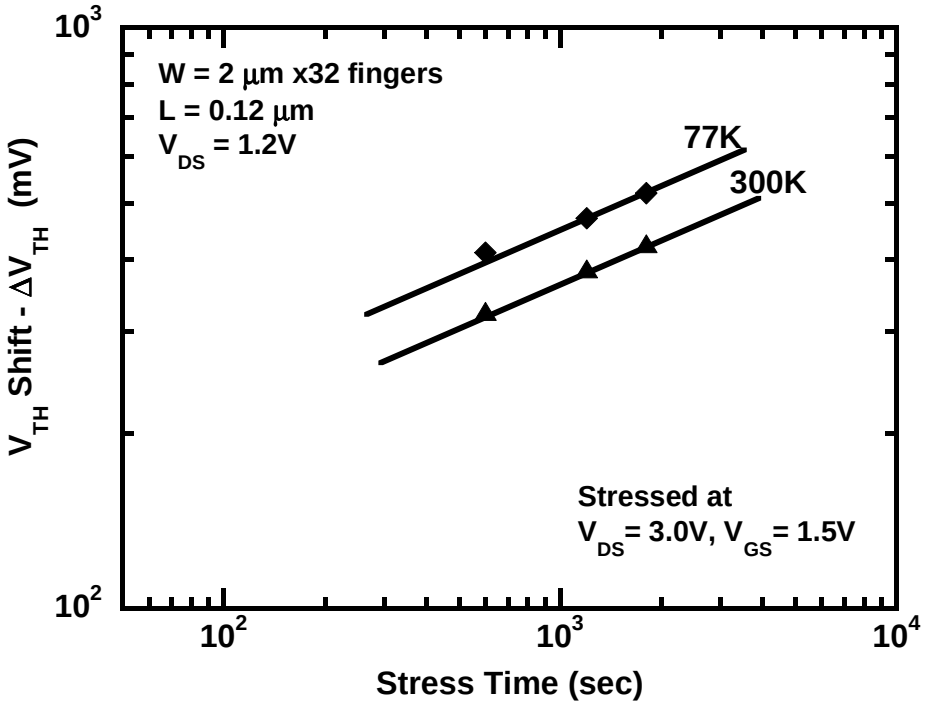


Figure 59: Time-dependent threshold voltage shift at 300 K and 77 K.

Table 4: Small Signal Parameters of the nFET biased at $V_{GS} - VTH$=0.76 V and V_{DS}=1.2V, at 300 K and 77 K

Temperature	Stress	R_G	r_{ch}	C_{gs}	C_{gd}	g_m	g_{ds}
300K	Pre	4.5 Ω	6.4 Ω	61.0 fF	26.4 fF	51.4 mS	7.5 mS
300K	Post	4.5 Ω	7.0 Ω	60.4 fF	25.0 fF	42.1 mS	8.5 mS
77K	Pre	2.1 Ω	2.8 Ω	62.0 fF	28.5 fF	62.0 mS	9.5 mS
77K	Post	2.1 Ω	4.0 Ω	61.1 fF	27.0 fF	53.0 mS	12.1 mS

stress-induced degradation of the cut-off frequency f_T is plotted as a function of gate-overdrive voltage at 300 K and 77 K in fig. 60. The peak-f_T decreases from 95 GHz to 81.3 GHz after stress at 300 K, and from 126 GHz to 99.4 GHz at 77 K. The g_m degradation directly results in the degradation of peak-f_T. The f_{max} versus $V_{GS} - V_{TH}$ is plotted in fig. 61. The peak-f_{max} decreases from 101.4 GHz to 86.6 GHz after stress at 300 K, and from 1268 GHz to 104.6 GHz at 77 K. Both the peak-f_T

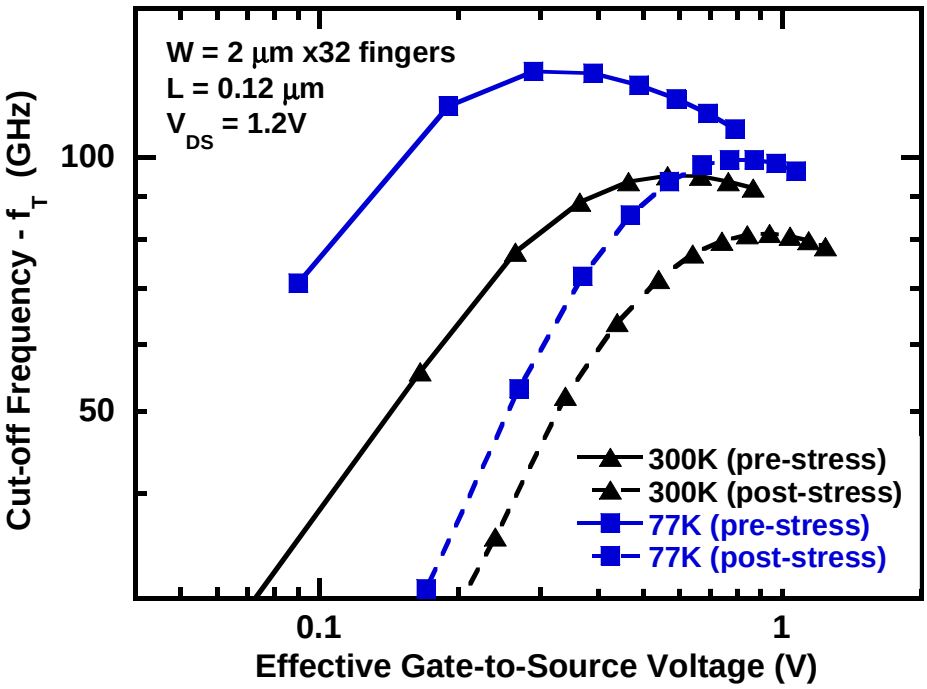


Figure 60: f_T versus gate-overdrive voltage $(V_{GS} - V_{TH})$ at 300 K and 77 K.

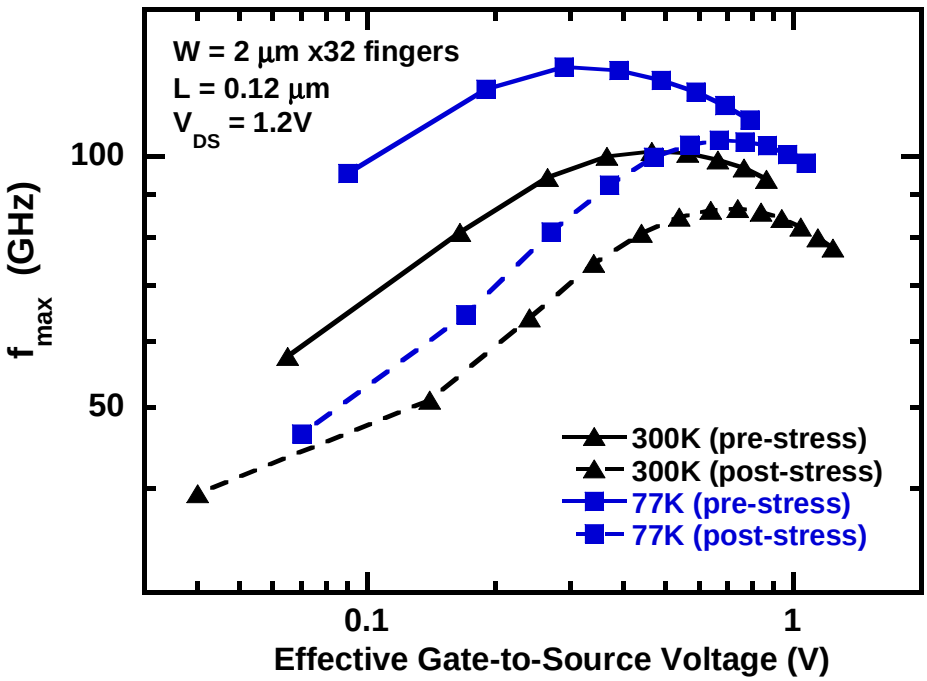


Figure 61: f_{max} versus gate-overdrive voltage $(V_{GS} - V_{TH})$ at 300 K and 77 K.

and peak-f_{max} bias point shifts to the right after stressing at 300 K and 77 K.

In this work, we have analyzed the effects of DC hot-carrier stressing on the DC and S-parameters of a 130 nm nFET at 300 K and 77 K. Stress-induced interface state generation has been identified as the dominant degradation mechanism at room temperature down to 77 K. The g_m degradation is more pronounced at 77 K owing to the effective mobility degradation due to increased surface scattering. To enhance the hot-carrier reliability of CMOS devices at cryogenic temperatures, the devices should be operated at lower gate and drain bias conditions. The enhanced device properties at cryogenic temperatures would allow for the device operation at lower power supply voltages and thereby help mitigating, to some extent, the effects due to hot-carrier degradation.

CHAPTER V

PROTON RADIATION TOLERANCE OF SCALED RF CMOS DEVICES

The space environment presents an extremely hostile environment for device and circuit operation, because of the presence of complex high energy radiation belts surrounding the earth. The high energy proton and electron belts shown in Fig. 62 have the greatest influence on the orbital space electronic systems [83].

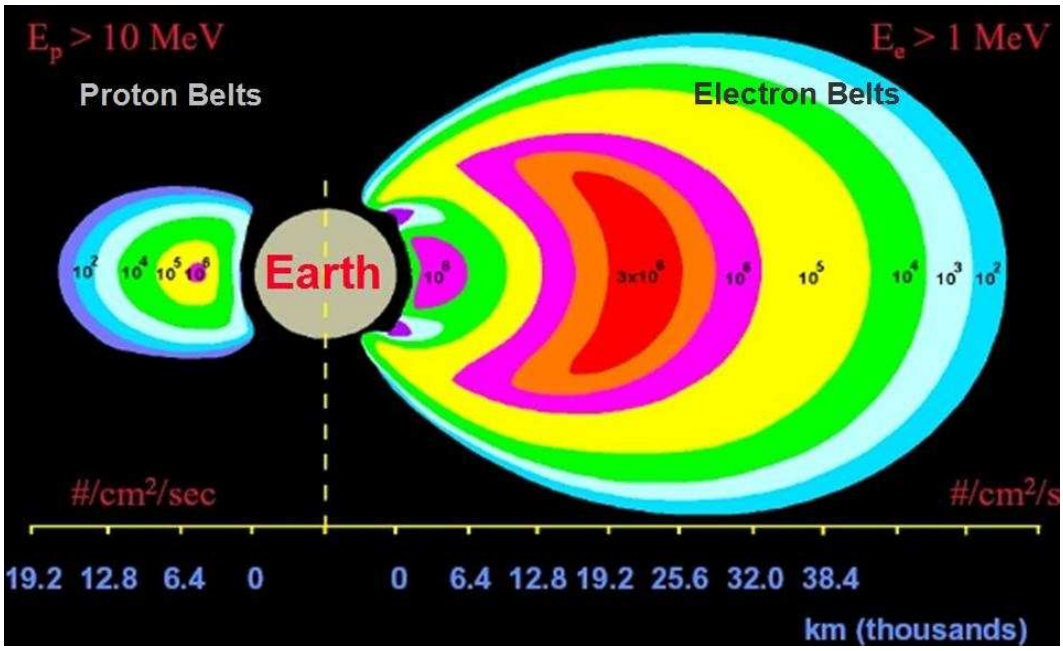


Figure 62: Proton and electron belts surrounding the Earth

Ionizing radiation effects can be broadly classified into three categories: 1) total dose effects, which are associated with the cumulative ionization damage caused by the incident charged particles, 2) displacement damage, which occurs when atoms in a material structure are displaced from their original lattice sites by the incident particle, and 3) single event effects, which arise from the interaction of single high-energy

particles with the semiconductor thereby causing transient or permanent effects [84]. Total ionizing dose (TID) effects are a key concern for MOSFETs as they lead to the degradation of several intrinsic device parameters.

Traditionally, radiation hardening has been achieved by process optimization, which requires a careful integration of several process steps that would simultaneously achieve the specifications for radiation, reliability, and performance. This would considerably increase the cost of fabricating a radiation-hardened IC. CMOS scaling to the deep-submicron regime has provided a natural path for enhancing the radiation tolerance of MOSFETs. Highly scaled CMOS technologies have ultra-thin and high quality gate oxides which naturally helps in radiation tolerance without requiring any additional process modifications. Currently, the effect of radiation on RF performance of MOSFETs has not been well explored. Hence, it is of great interest to investigate the radiation response of aggressively scaled CMOS technologies for harnessing their potential in the development of radiation-hard space electronic systems.

5.1 Total Dose Effects in MOSFETs

Total dose effects are associated with the accumulated ionization damage induced by the incident charged particles. When high-energy charged particles are impinged on a MOSFET, electron-hole pairs (EHPs) are created due to carrier excitation, thereby leading to the generation of traps in the gate-oxide layer and the $Si - SiO_2$ interface. Figure 63 illustrates the TID effects in MOSFETs. Charge trapping in the oxide layer and the interface traps are responsible for the shifts in the intrinsic device properties. The trapped charges can cause a shift in the threshold voltage, capacitance-voltage characteristics, and the sub-threshold slope in MOS transistors. Increased surface scattering due to interface charges can result in mobility degradation in MOSFETs.

Another dominant total dose effect in MOSFETs is the radiation-induced leakage currents. Radiation-induced leakage currents along the intersection of the active FET

channel and the shallow-trench isolation (STI) is usually a primary failure mechanism. Figure 64 shows the STI edge leakage path in a MOSFET. The STI edge leakage

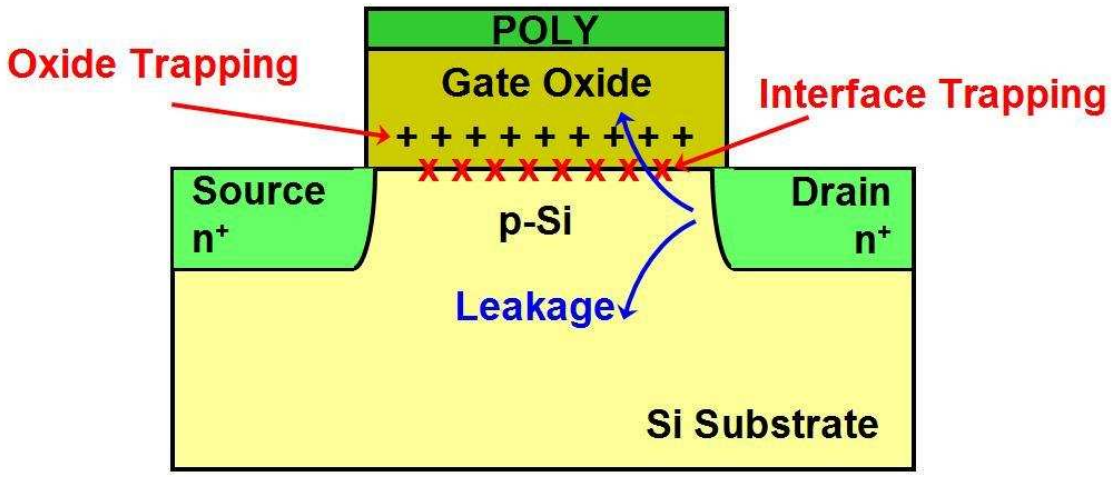


Figure 63: Illustration of total dose effects in a MOSFET

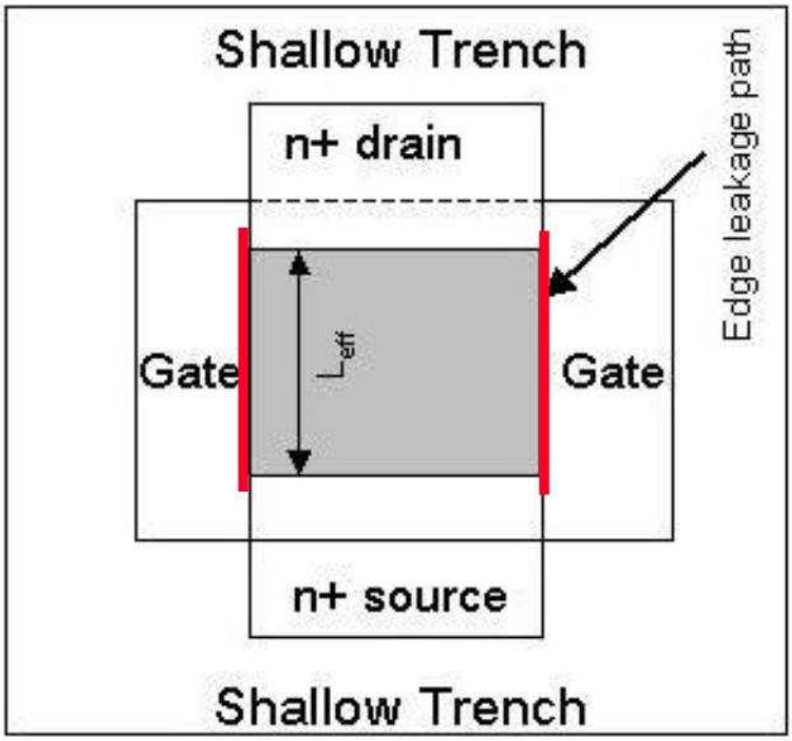


Figure 64: Schematic top view of the STI edge leakage path in a MOSFET

contributes to the off-state leakage current and is caused by the parasitic inversion channel created at the STI/active-channel interface at sufficiently high dose levels. Radiation-induced leakage currents are also caused by the trap-assisted tunneling of carriers from the substrate to gate, aided by the radiation-induced oxide traps.

TID can be measured in terms of the absorbed dose, which is a measure of the energy absorbed by matter. The absorbed dose is quantified using a unit called the "rad", an acronym for radiation absorbed dose ($1\ rad = 100\ ergs/gm\ of\ material$). Satellites and space probes used in near-Earth missions typically encounter TID between 10 and 100 krad(Si). Interplanetary missions encounter very high radiation levels ($> 1\ Mrad(Si)$).

5.2 Proton Radiation Tolerance of a 130 nm CMOS Technology

The effects of 63 MeV proton irradiation on the DC and RF performance of a 130 nm CMOS technology are presented for the first time [85], [86].

5.2.1 Device Technology and Experimental Details

The MOSFETs used in this study are contained in a fully-integrated, commercially available 0.13 μm CMOS technology [41], [42]. The process offers bulk CMOS devices with a minimum drawn gate-length of 0.12 μm and operating supply voltage of 1.2V. The thin oxide devices used in this study have a gate-oxide thickness of 2.2 nm. As shown in Fig. 65, the process features both STI and deep-trench isolation. This CMOS technology was not radiation-hardened through process optimization. nFETs with a drawn W/L of 10/0.12 were used for DC and low-frequency noise measurements. Multi-fingered nFETs with a W/L of 2.0/0.12 and 32 gate fingers were chosen for the small-signal ac and broadband noise characterization. The transistors were designed using conventional layout techniques.

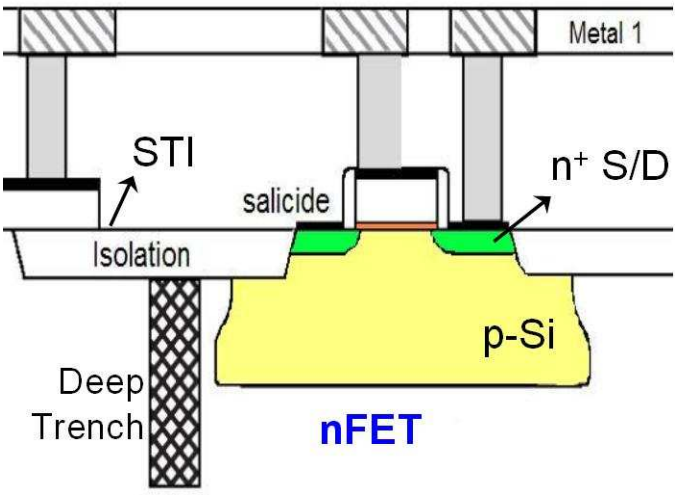


Figure 65: Schematic cross-section of the nFET

The samples were irradiated with 63.3 MeV protons at the Crocker Nuclear Laboratory at the University of California at Davis. The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup. The radiation source (Ta scattering foils) located several meters upstream of the target establish a beam spatial uniformity of about 15% over a 2.0 cm radius circular area. Beam currents from about 5 nA to 80 nA allow testing with proton equivalent gamma doses from 10 krad to 1 Mrad. The dosimetry system has been previously described [87], [88], and is accurate to about 10%. At a proton fluence of 1×10^{12} p/cm^2, the measured equivalent gamma dose was approximately 135 krad(Si). The nFETs used for the study were irradiated with the gate terminal biased at V_{DD} (1.2V) and the drain, source, and substrate terminals grounded for the DC measurements (i.e., worst case condition), and with all terminals floating for the *ac* measurements, at doses ranging from 1 krad to 1 Mrad. Samples for the DC measurements were mounted in 24 pin DIP packages and were wire-bonded. The *ac* samples were mounted on ceramic holders and exposed to proton radiation up to 1 Mrad(Si) equivalent gamma dose.

The DC device characterization was performed using an Agilent 4155C semiconductor parameter analyzer. The low-frequency noise measurements were performed using an HP 3562 dual channel dynamic signal analyzer. S-parameters of the DUTs were measured using an HP 8510C VNA. The conventional "Open-Short" de-embedding technique was performed on the raw S-parameters of the devices to eliminate the effects of pad parasitics. The high-frequency noise parameters were measured from 2 GHz to 26 GHz using the ATN NP5B noise measurement system.

5.2.2 DC Performance

The pre- and post-radiation drain current (I_D) versus gate-to-source voltage (V_{GS}) for the $10\mu m/0.12\mu m$ nFET is shown in Fig. 66. The sub-threshold characteristics

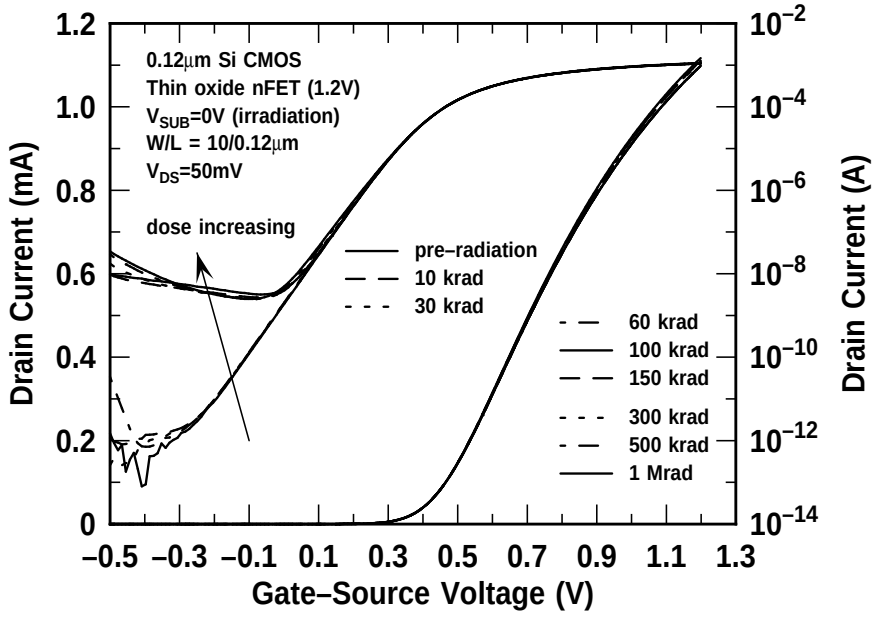


Figure 66: Drain current as a function of gate-to-source voltage, before and after radiation for an nFET with $W/L = 10.0\ \mu m/0.12\ \mu m$.

indicate that the off-state leakage current remains constant (around 1 pA) for doses up to 60 krad and then appears to saturate at approximately 10 nA for doses from 100 krad to 1 Mrad. This sub-threshold leakage is attributed to a combination of two leakage mechanisms. One of the main causes of sub-threshold leakage is the

presence of radiation-induced charge physically located in the region where the gate extends beyond the STI edge. At a sufficiently high dose, a parasitic leakage path forms between the source and drain, thus producing a shunt leakage path (refer Fig. 64). It is observed that at equivalent doses higher than 150 krad, the gate bias has no control over the leakage current for $V_{GS} < 0V$, as the parasitic conduction deep in the bulk dominates over the parasitic conduction at the surface of the STI corner [89]. The other off-state leakage mechanism is the gate induced drain leakage (GIDL), which causes a negative sloping drain current for $V_{GS} < 0V$. The transfer characteristic shown in Fig. 66 does not indicate a strong negative slope resulting from GIDL. A rather weak negative slope is observed because the STI edge leakage at high dose levels (> 60 krad) is larger than GIDL. However, it should be noted that this level of parasitic leakage is significantly better than that observed in 0.18 μm CMOS technology, and is attributed to the thinner STI used in the present technology [90]. There is also no observable change in the sub-threshold slope, indicating that there is no significant interface trapping . As seen in Fig. 67, the radiation-induced transconductance degradation is almost negligible. Figure 68 shows that the maximum radiation-induced threshold voltage shift (ΔV_{th}) for the 10 μm/0.12 μm nFETs is about $-2.2mV$ at 1 Mrad total dose. The negative shift in V_{th} is due to the positive charge buildup in the oxide layer. As the oxide layer in very thin, the trapped hole density is very small leading to a very small shift in V_{th}.

5.2.3 Low-frequency ($1/f$) Noise Performance

Low-frequency ($1/f$) noise in MOSFETs is highly sensitive to the defects present at or near the Si/SiO_2 interface. The magnitude of $1/f$ noise in MOSFETs is usually correlated with the density of carrier traps existing at the border of the $Si - SiO_2$ interface. The drain current noise spectral density (S_{I_d}) measured before and after irradiation is shown in Fig. 69. A slight increase in $1/f$ noise is observed after

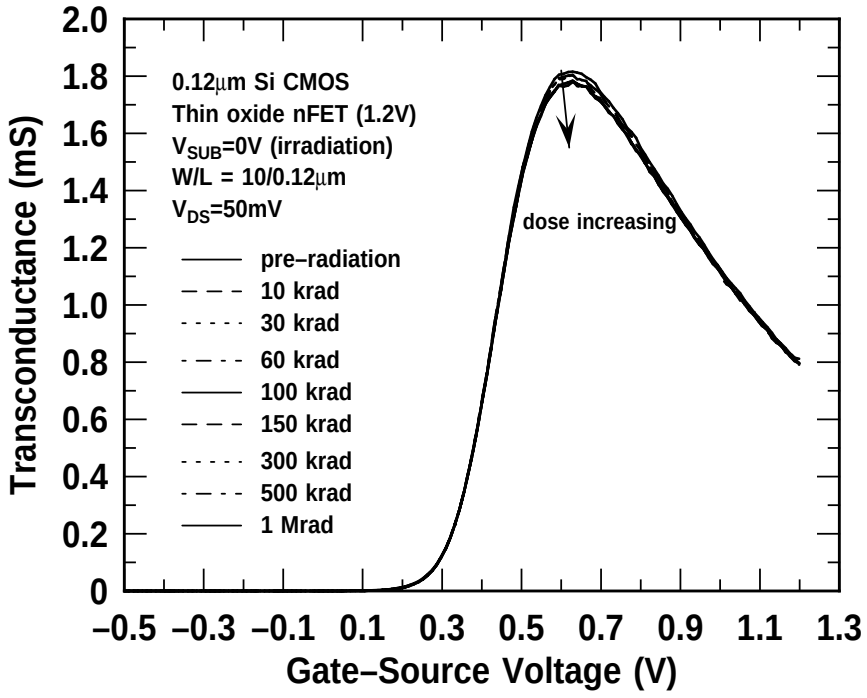


Figure 67: Transconductance (g_m) as a function of drain current, before and after radiation for an nFET with $W/L = 10.0\ \mu m/0.12\ \mu m$.

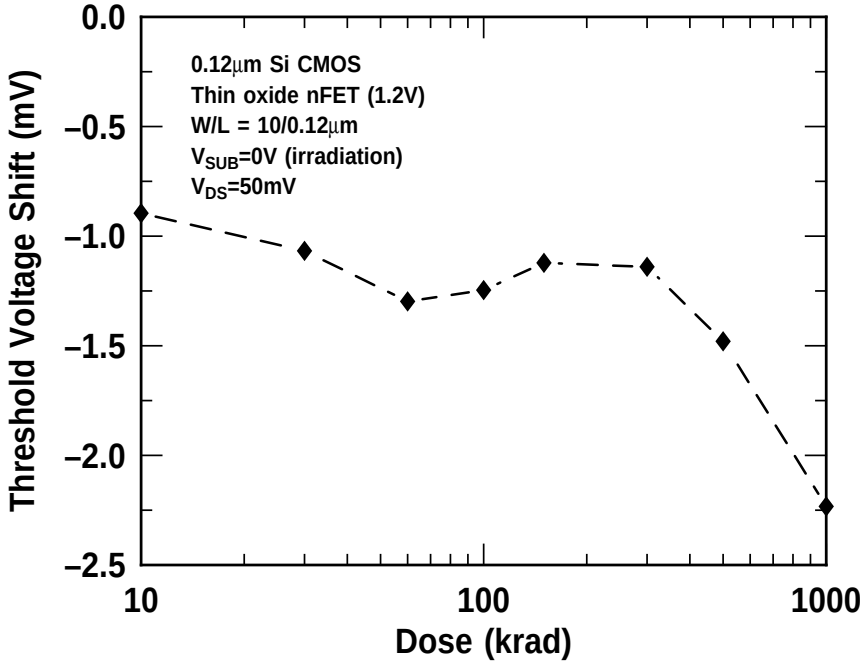


Figure 68: The threshold voltage shift as a function of equivalent total dose for both the 10.0 $\mu m/0.12\ \mu m$ nFETs

radiation, which is mainly due to the radiation-induced increase of oxide-trapped charges. The results indicate that these aggressively scaled $0.12\mu m$ nFETs are not very sensitive to radiation-induced $1/f$ noise degradation because of the very thin and high quality gate oxide.

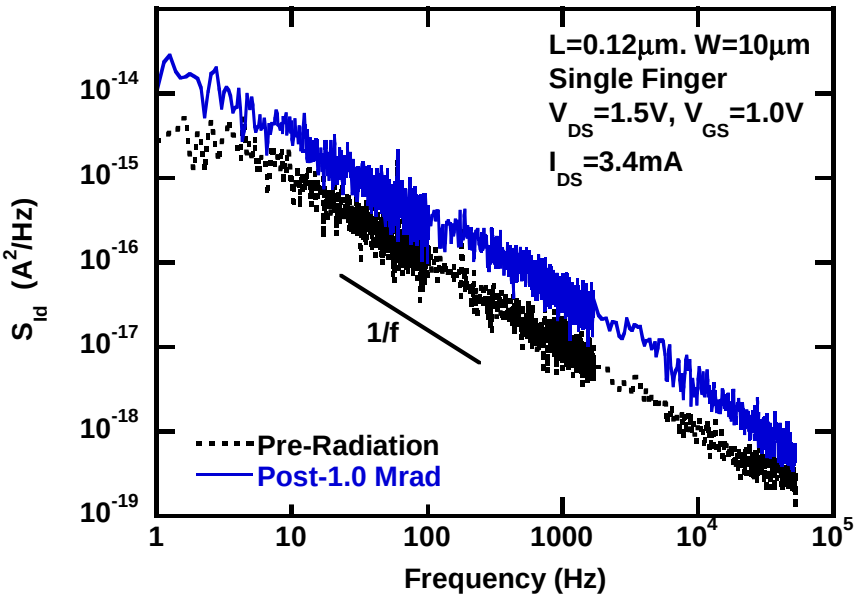
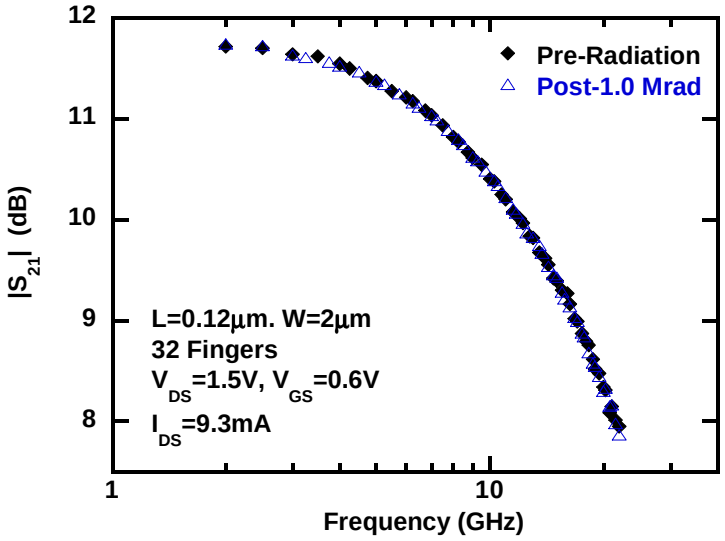


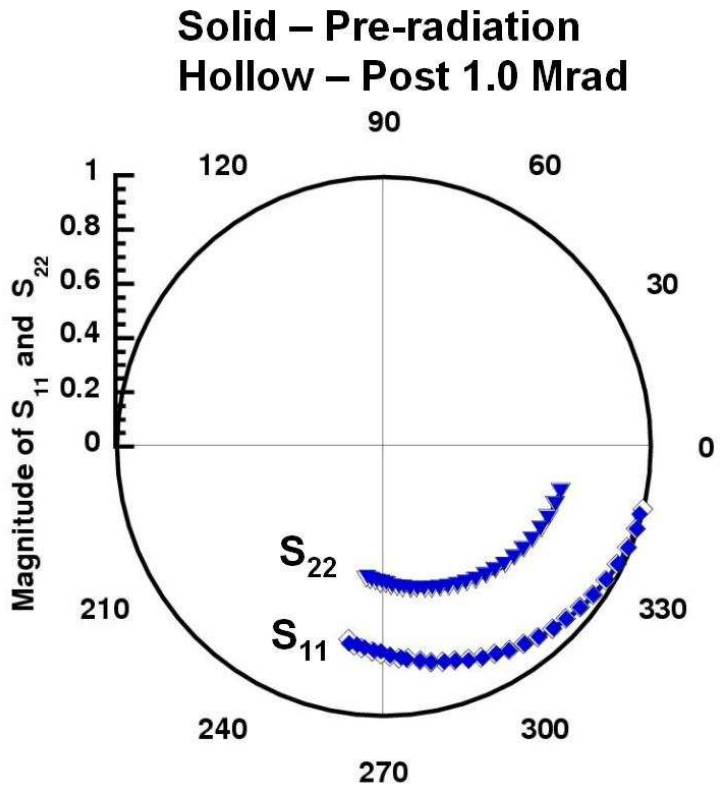
Figure 69: Drain noise current spectrum, before and after irradiation, for an nFET with $W/L = 10.0\ \mu m/0.12\ \mu m$

5.2.4 Small-Signal Performance

On-wafer S-parameter measurements were performed on RF nFETs with multi-fingered gate layout. The raw S-parameters were de-embedded using the corresponding "Open" and "Short" structures. The S-parameters of this nFET before and after irradiation are shown in Fig. 70. There is a very small decrease in the magnitude of S_{21} after radiation because of the slight decrease in g_m. No perceptible change is observed in S_{11} and S_{22} after radiation to 1 Mrad. The cut-off frequency (f_T) is extracted from the extrapolated small-signal current gain (h_{21}). The cut-off frequency versus drain current characteristics, before and after radiation, is shown in Fig. 71. The peak f_T for the 2 μm/0.12 μm (32 finger) nFET decreases from 100 GHz (prior to radiation) to about 97 GHz after 1 Mrad total dose, thus exhibiting a negligible radiation-induced degradation in the overall frequency response.



(a)



(b)

Figure 70: (a) Magnitude of S_{21} as a function of frequency, (b) Magnitude of S_{11} and S_{22} as a function of frequency - pre- and post- 1.0 Mrad, for an nFET with W/L = 2.0/0.12 and 32 gate fingers.

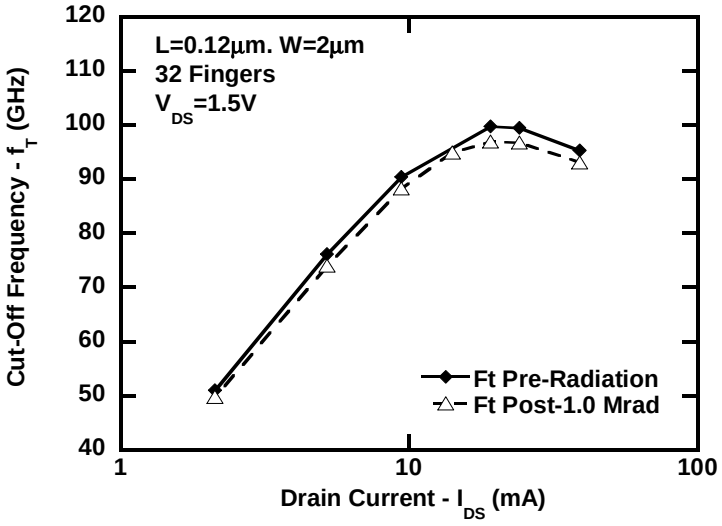


Figure 71: Cut-off frequency f_T as a function of drain current, before and after irradiation, for an nFET with $W/L = 2.0\ \mu m/0.12\ \mu m$ and 32 gate fingers.

5.2.5 Broadband Noise Performance

The main sources of broadband noise in MOSFETs are the channel thermal noise, gate resistance-induced thermal noise, and the induced gate noise. To a first order, the minimum noise figure F_{min} can be expressed as

$$F_{min} = 1 \ + \ K \ \frac{f \ 2\pi(C_{gs} + C_{gd})}{\sqrt{g_m}} \ \sqrt{R_g + R_s} \tag{50}$$

where R_g and R_s are the gate and source resistances and K is a technology-dependent fitting parameter. From (50), a small increase in F_{min} is expected after irradiation, because of the slight decrease in g_m. Figures 72 and 73 show the minimum noise figure and noise resistance as a function of frequency and drain current, before and after radiation. We observe a very slight degradation of F_{min}, as expected, and almost no change in the noise resistance after radiation.

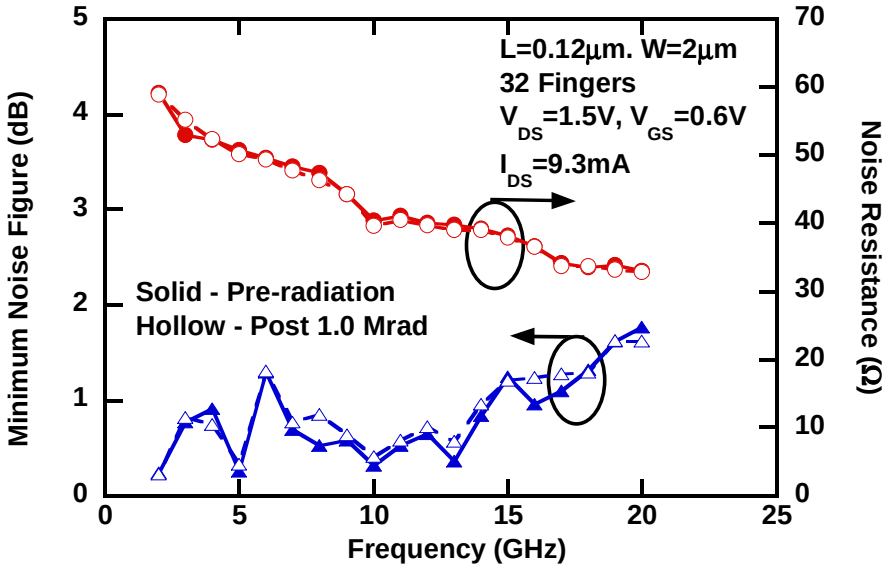


Figure 72: Minimum Noise Figure and Noise Resistance as a function of frequency, before and after radiation, for a NMOS device with $W/L = 2.0\ \mu m/0.12\ \mu m$ and 32 fingers

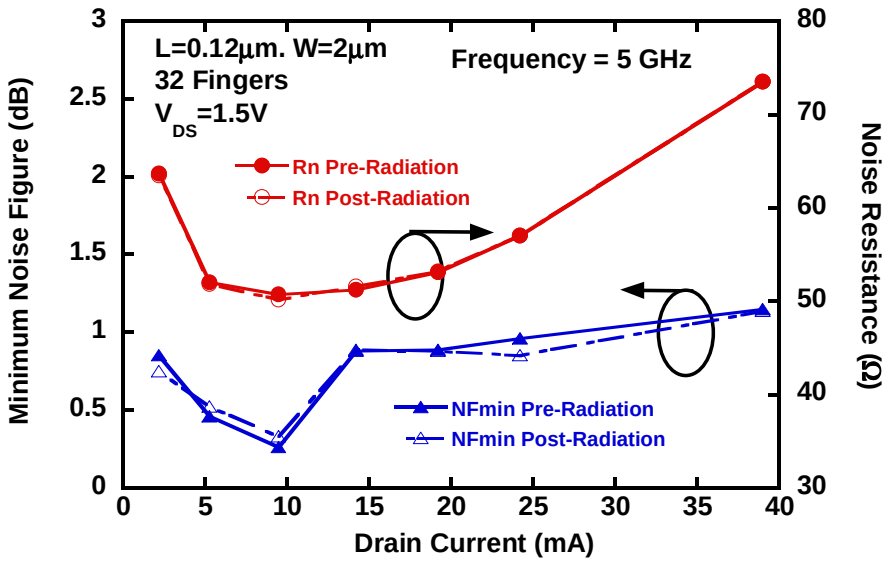


Figure 73: Minimum Noise Figure and Noise Resistance at 5 GHz as a function of drain current, before and after irradiation, for an nFET with $W/L = 2.0\ \mu m/0.12\ \mu m$ and 32 gate fingers.

5.3 Summary

The effects of proton radiation on the DC, low-frequency noise, small-signal, and RF noise performance of a 130 *nm* CMOS technology is presented for the first time.

The radiation response of the nFETs was studied up to an equivalent gamma dose of 1 Mrad(Si). The benefits of the thin gate-oxide in these scaled nFETs is seen in the very small degradation of V_{th}, g_m, and the $1/f$ noise after irradiation to 1 Mrad. The S-parameters, f_T, and the RF noise parameters show no perceptible degradation after proton exposure. The results indicate that the 130 nm CMOS technology exhibits reduced sensitivity to ionizing radiation compared to the previous-generation CMOS technologies, and hence is suitable for analog and RF applications that require a large degree of tolerance to high total doses of ionizing radiation.

CHAPTER VI

RF PERFORMANCE OF HIGHLY SCALED SILICON GERMANIUM MODFETS

Until recently, heterojunction FETs have been largely limited to devices built using the semiconductors from the $III-V$ group, such as AlGaAs/GaAs, InGaP/GaAs HFETs and MODFETs. The rapid growth and the maturation of the SiGe HBT/SiGe BiCMOS technologies have paved the way for the development of SiGe based HFETs. There has been a considerable interest in the $Si_{1-x}Ge_x$ material system, as it allows specific tailoring of the band structure providing new generations of Si-based devices which are compatible with the mainstream Si-CMOS technologies [91]–[100]. SiGe heterostructures enable the fabrication of strained-Si channel FETs with a two-dimensional electron gas and strained-SiGe channel with a two-dimensional hole gas with enhanced carrier transport properties. Most of the SiGe HFET devices that have been reported in the current literature are Si/SiGe modulation-doped FETs with Schottky gate electrodes. Electron mobilities as high as 2800 cm^2/Vs have been achieved in n-type Si/SiGe MODFETs, which represents an increase of 3–5 times compared to bulk-Si nFETs. SiGe MODFETs are very attractive devices for future RF and mixed-signal applications. This chapter presents the RF performance analysis of highly scaled SiGe MODFETs.

6.1 Device Technology

The modulation-doped heterostructure used in this work was grown on an 8" Si wafer by ultrahigh vacuum chemical vapor deposition. The as-grown layer structure consisted of a relaxed $Si_{1-x}Ge_x$ buffer layer, step-graded from $x = 0$ to a constant Ge

composition of $x = 0.3$, a 9-nm strained-Si quantum well, a 5-nm $Si_{0.7}Ge_{0.3}$ spacer layer, an 8-nm phosphorous-doped n-type $Si_{0.7}Ge_{0.3}$ supply layer and finally a 2-nm n-Si capping layer. The room-temperature electron sheet density was $2.2 \times 10^{12}\ cm^{-}2$, with a corresponding Hall mobility of 1700 cm^2/Vs [98].

The schematic cross-section of the device is shown in fig. 74. The process features

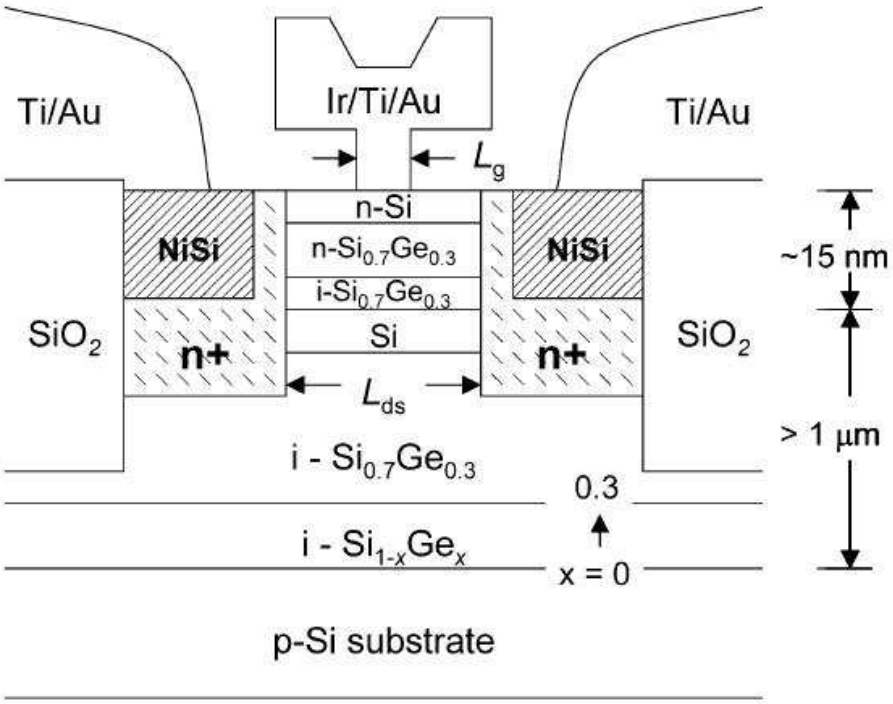


Figure 74: Schematic cross-section of a Si-SiGe n-MODFET device structure.

T-shaped Ir-Ti-Au gate metal layer, Ti-Au pad metalization, and shallow-trench isolation. The drain-to-source spacing (L_{ds}), defined as the distance between the drain and source implants, was kept at a constant value of 300 nm. The top of the T-gate had a constant width of 400 nm. The gate was not self-aligned to the source and the drain.

The devices used for our study have a gate length of 70 nm and a gate width of 20 μm and 40 μm with $L_{ds} = 300\ nm$. The DC, S-parameter, and RF noise parameter characterization was performed on these devices. The small-signal and broadband

noise modeling is carried out using an equivalent circuit model. The gate shot-noise will be incorporated in the RF noise model.

6.2 Results and Discussion

6.2.1 DC Performance

Figure 75 shows the output characteristics of the n-MODFET with $L_g = 70\ nm$ and $W_g = 40\ \mu m$ for varying gate voltages. It is seen that at zero gate bias the

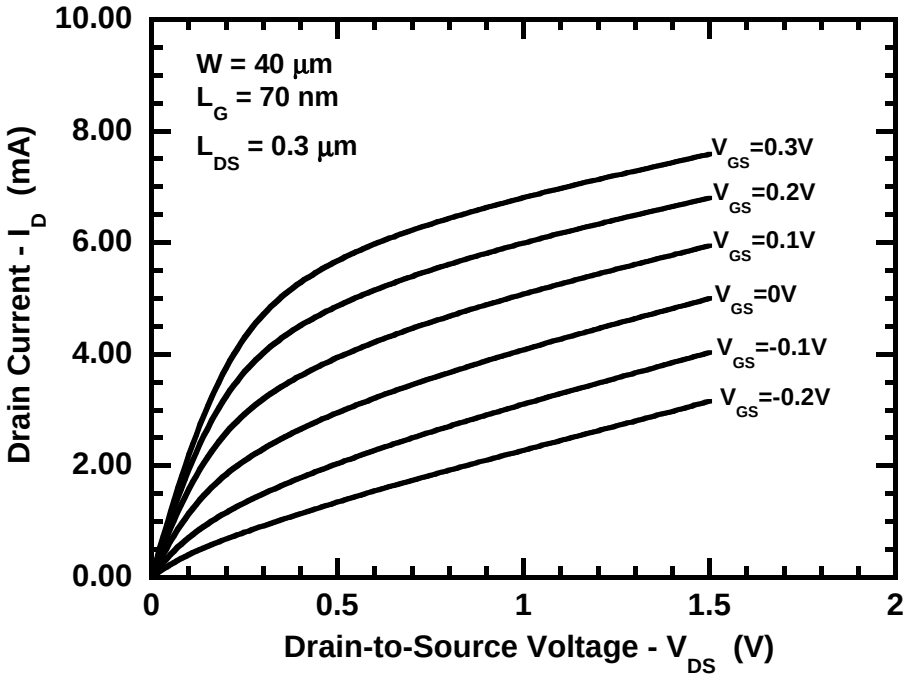


Figure 75: Drain current versus drain-to-source voltage for an n-type SiGe MODFET with L_g=70 nm, $W_g = 40\ \mu m$.

quantum well channel is not completely depleted. The drain current can be pinched off by applying a sufficient negative gate bias. The small L_{ds} of 300 nm allows the device to have a high drive current of about 200 mA/mm for a $V_{GS} = 0.3$V and $V_{DS} = 1.5$V. However, the small L_{ds} also results in considerable parasitic off-current, as can be seen in the DC transfer characteristic shown in fig. 76. The transconductance as a function of the gate-to-source voltage is plotted in fig. 77 for $V_{DS} = 100$mV and 1.5V. At $V_{DS} = 1.5$V, the peak g_m is about 250 mS/mm. The corresponding

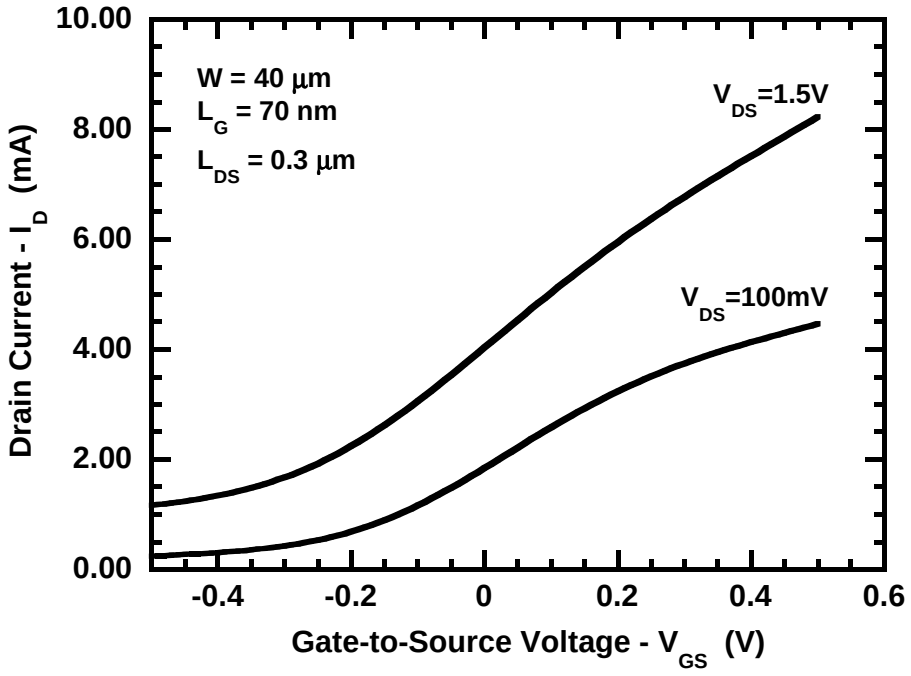


Figure 76: Drain current versus gate-to-source voltage for an n-type SiGe MODFET with L_g=70 nm, W_g = 40 μm.

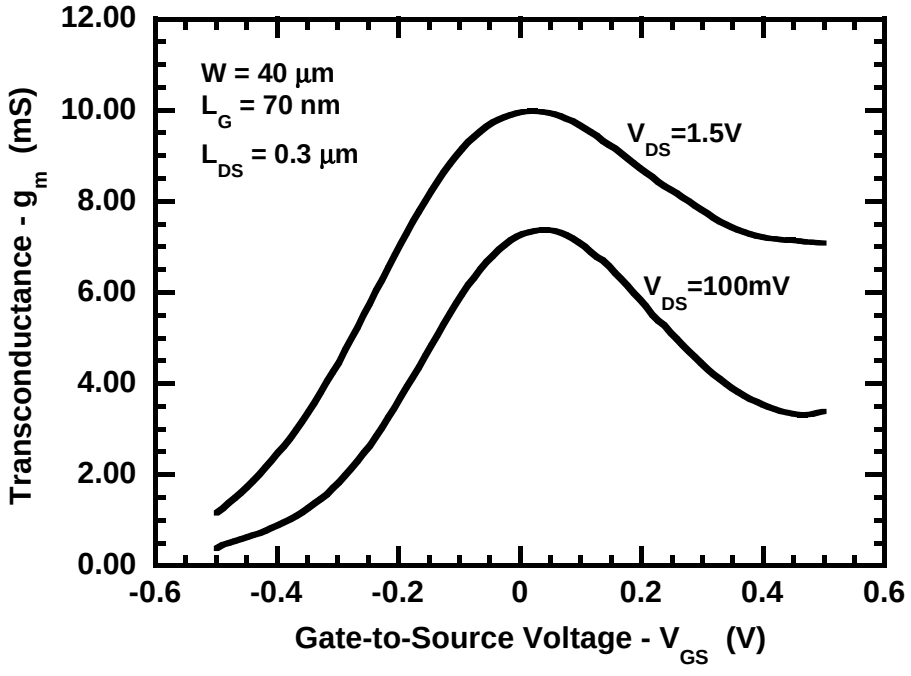


Figure 77: Transconductance versus gate-to-source voltage for an n-type SiGe MODFET with L_g=70 nm, W_g = 40 μm.

output conductance g_{ds} is about 60 mS/mm, leading to a DC voltage gain of 4.2. The relatively high output conductance of these devices is because of the fact that no p-well doping was utilized.

6.2.2 Small-Signal AC and Broadband Noise Analysis

The small-signal AC and RF noise performance of the n-MODFETs were analyzed using an equivalent circuit model shown in fig 78. The small-signal parameters were

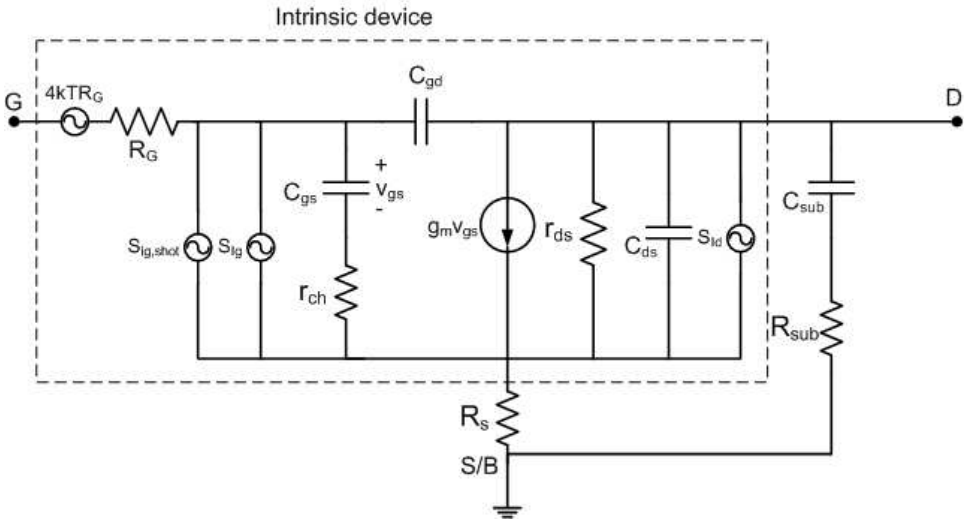


Figure 78: Sub-circuit model for the small-signal AC and RF noise analysis of an n-MODFET.

extracted from the measured and de-embedded S-parameters. The extracted cut-off frequency f_T is plotted versus drain current in fig. 79. The peak-f_T for this device is about 80 GHz. It is seen that these devices exhibit a high peak-f_T of about 78 GHz at a low drain bias value of 0.5V, thus resulting in a high-speed performance at low operating voltages.

The noise parameters of the DUTs are measured from 2 to 20 GHz and are de-embedded using the corresponding open and short test structures. Considerable effect of the parasitic access resistances is observed and has to be de-embedded carefully to obtain the intrinsic noise parameters of the device. The intrinsic device noise currents, namely the drain current noise and the induced gate noise were extracted

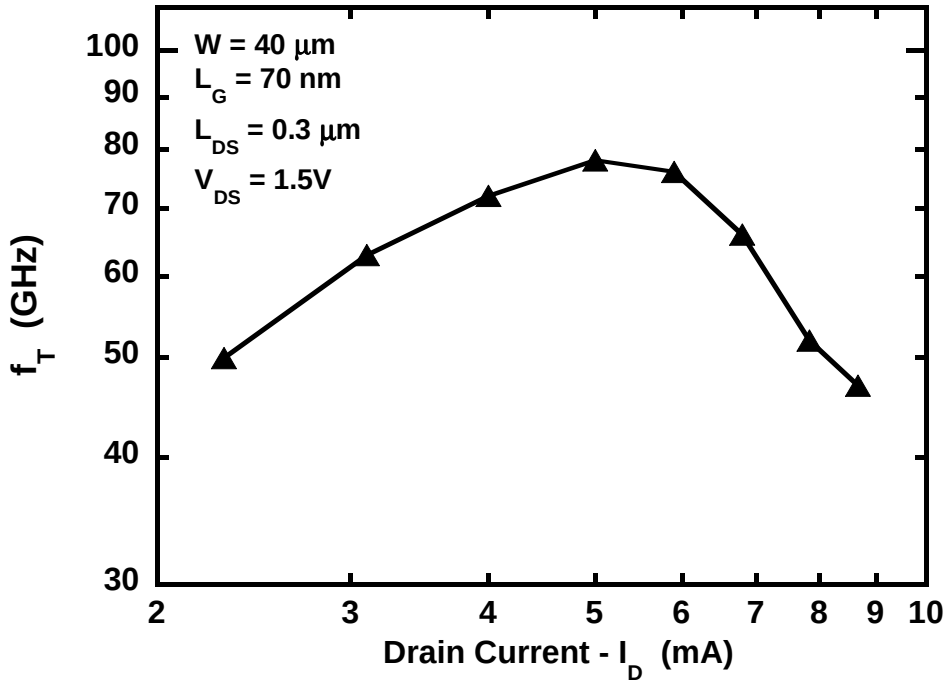


Figure 79: Cut-off frequency versus drain current for an n-type SiGe MODFET with L_g=70 nm, W_g = 40 μm.

using the procedure outlined in section 3.2. The shot noise due to the gate leakage current is also incorporated in the noise model as shown in the sub-circuit model in fig. 78. The gate shot noise is uncorrelated with the induced gate noise. The extracted noise currents are plotted versus frequency in fig. 80. The gate shot noise, given by equation 5, and is an order of magnitude less than the induced gate noise for this device at the chosen bias condition. The gate shot noise directly depends on the magnitude of the gate leakage current, and can become significant at higher gate bias conditions, especially at lower frequencies. Hence, the gate shot noise should be incorporated in the model to predict the noise parameters accurately. The extracted excess noise factor γ for the n-MODFET is plotted as a function of the drain current in fig. 81. The extracted γ value is slightly higher than that observed for short-channel MOSFETs.

The noise currents are used with the sub-circuit model to obtain the simulated

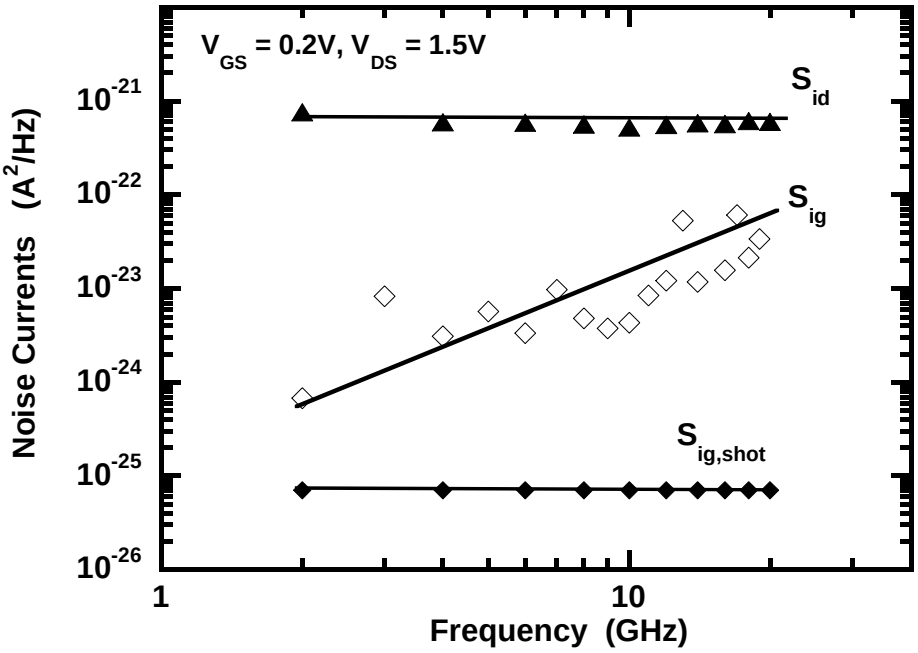


Figure 80: Power spectral densities of the channel thermal noise, induced gate noise, and gate shot noise versus frequency for an n-type SiGe MODFET with L_g=70 nm, $W_g = 40$ μm.

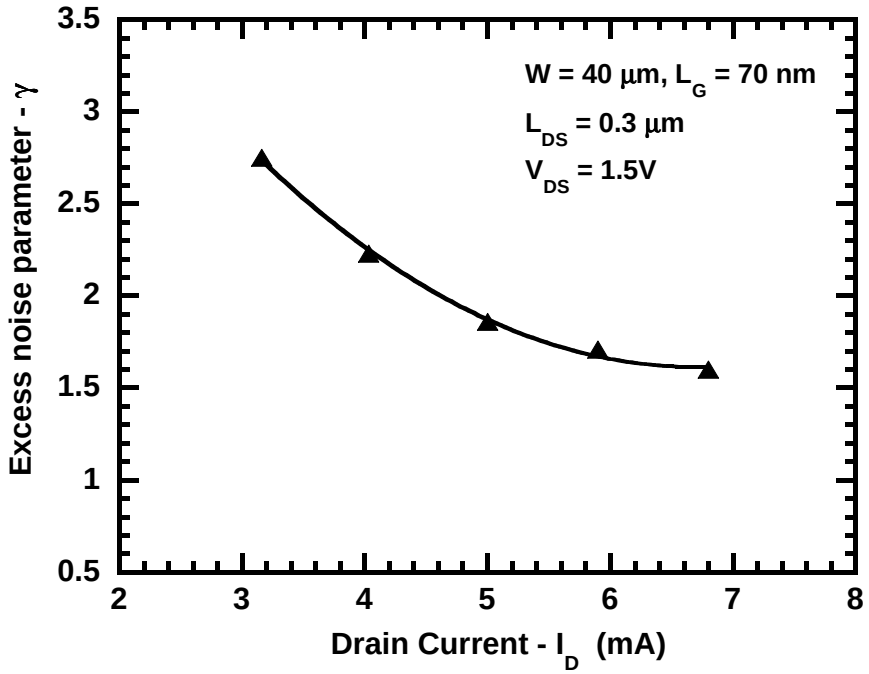


Figure 81: Excess noise factor γ versus drain current for an n-type SiGe MODFET with L_g=70 nm, $W_g = 40$ μm.

noise parameters. Figures 82, 83, and 84 show the measured and simulated noise parameters, namely the NF_{min}, R_n, and the magnitude and angle of Γ_{opt} versus frequency. The NF_{min} of this device stays below 2 dB up to about 15 GHz. The

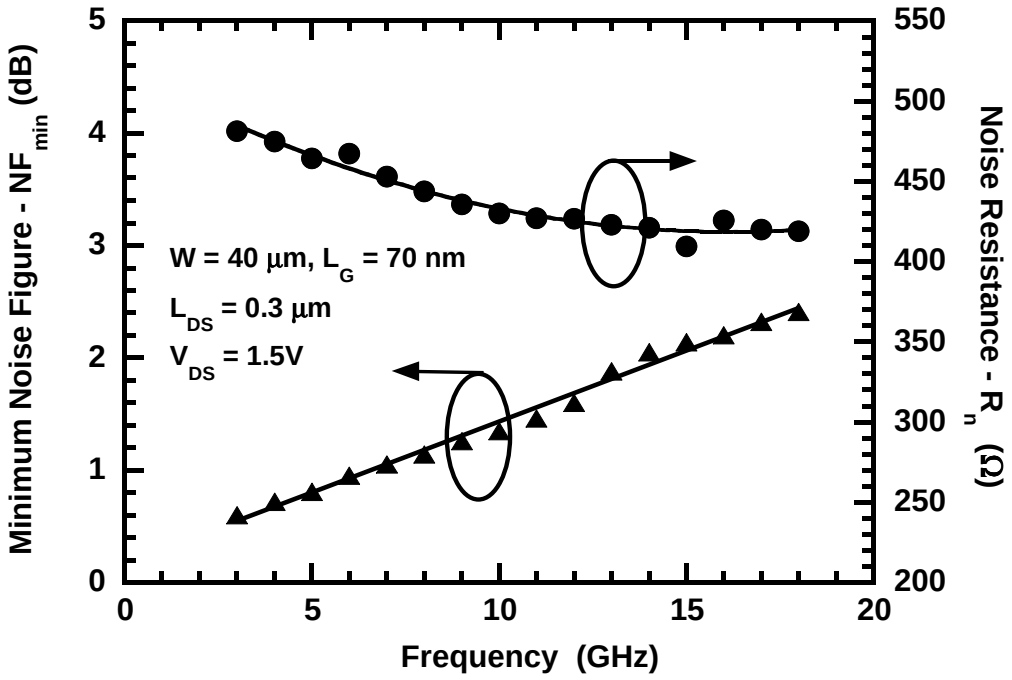


Figure 82: NF_{min} and R_n versus frequency for an n-type SiGe MODFET with L_g=70 nm, W_g = 40 μm.

NF_{min} and R_n can further be reduced by lowering the gate resistance. The RF noise performance of the SiGe MODFETs remain modest when compared with the $III-V$ HEMTs and the state-of-the-art bulk-Si MOSFETs. There is a lot of room for improvement of the SiGe MODFET device design to achieve enhanced RF performance.

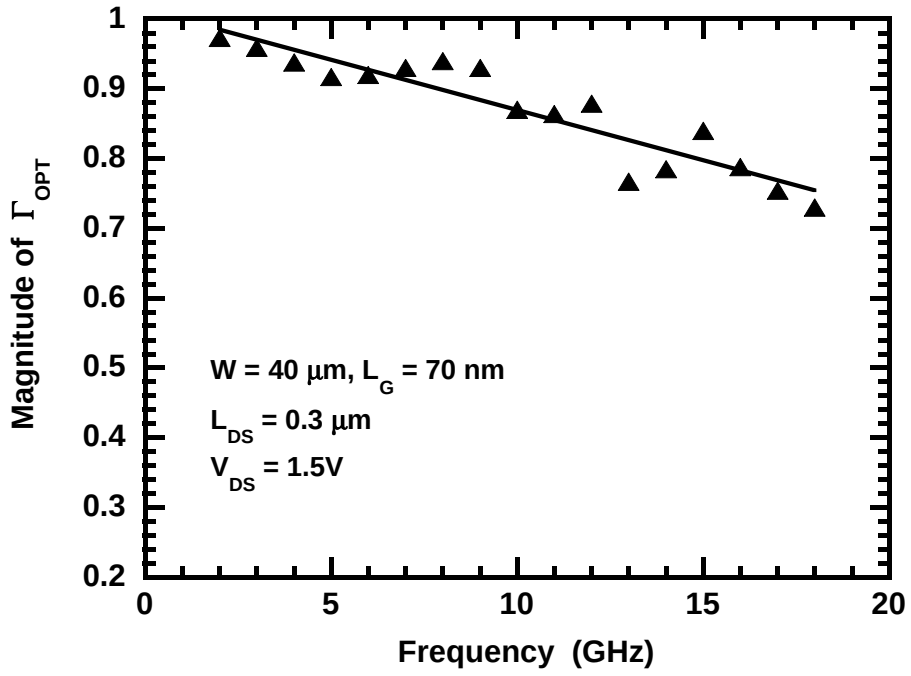


Figure 83: Magnitude of Γ_{opt} versus frequency for an n-type SiGe MODFET with L_g=70 nm, $W_g = 40$ μm.

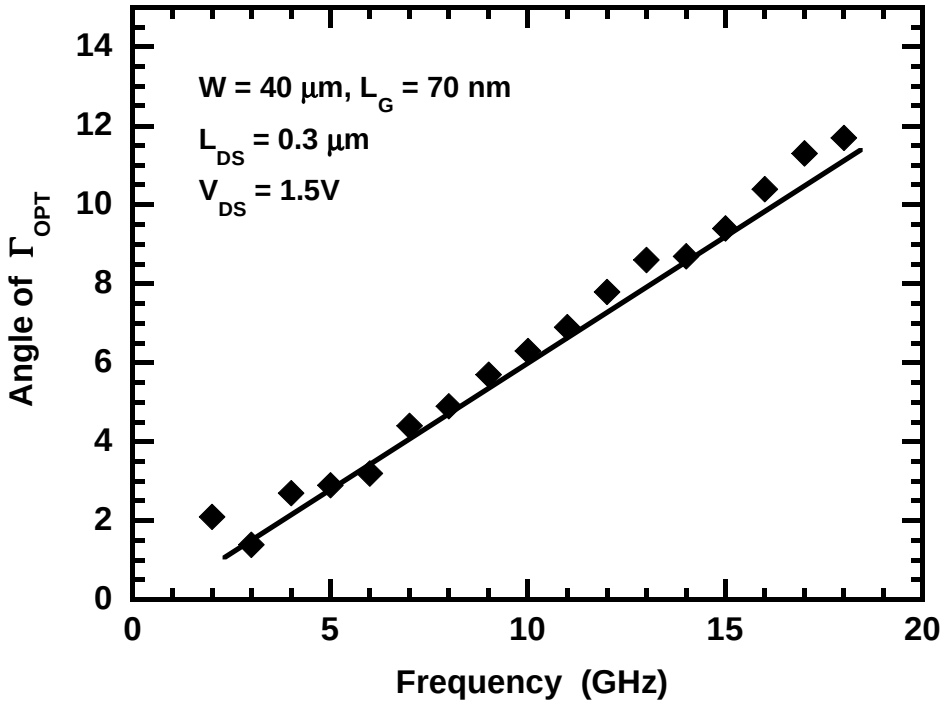


Figure 84: Angle of Γ_{opt} versus frequency for an n-type SiGe MODFET with L_g=70 nm, $W_g = 40$ μm.

CHAPTER VII

CONCLUSIONS AND FUTURE WORK

7.1 Contributions and Impact of the Dissertation

The contributions of this work can be summarized as follows:

1. An analytical RF noise model of highly scaled Si-CMOS devices is developed, using a direct extraction procedure based on the linear two-port noise theory. The intrinsic device noise sources, namely the channel thermal noise, the induced gate noise, and their correlation are extracted directly from the measured Y-parameters and RF noise parameters of the device. The behavior of the noise currents and the excess noise factor γ were studied across bias and frequency. This understanding of the device noise behavior is very crucial for the development of low-noise RF ICs.

2. A comprehensive investigation of the DC, small-signal AC, and broadband noise performance of highly scaled Si-CMOS devices operating at cryogenic temperatures has been performed. The on-wafer device characterization was performed at 77 K down to 10 K and the performance enhancement of the Si-MOSFETs has been explored for the first time. The broadband noise model developed for room temperature analysis was extended to model the RF noise performance of scaled MOSFETs at cryogenic temperatures. The hot-carrier degradation of MOSFETs at cryogenic temperatures was studied and the worst-case gate voltage stress conditions was determined. The degradation due to hot-carrier-induced interface states creation was identified as the dominant hot-carrier degradation mechanism at room temperature down to 77 K. This study is extremely important for understanding the performance of scaled Si-MOSFETs at cryogenic

temperatures, which is of critical importance in the design of circuits for deep space and radio astronomy applications.

3. The proton radiation tolerance of a 0.12 μm nFET is investigated for the first time. The DC, low-frequency noise, small-signal AC, and broadband noise performance degradation of the nFET was studied before and after irradiation up to an equivalent total dose of 1 Mrad, which represents the worst case condition for many earth orbiting and planetary missions. The goal is develop radiation-hard ICs without introducing any process modifications.

4. A comprehensive characterization and modeling of the small-signal and high-frequency noise performance of highly scaled Si/SiGe n-MODFETs is presented. The effect of gate shot noise was incorporated in the broadband noise model. This analysis is very important to explore the applicability of SiGe MODFETs for the design of high-speed and low-voltage RF and mixed-signal ICs.

Thus, this work advances the state-of-the-art in the understanding and analysis of the RF performance of highly scaled Si-CMOS devices as well as emerging technologies, such as Si/SiGe MODFETs. The key contribution of this thesis is to provide a robust framework for the systematic characterization, analysis and modeling of the small-signal and RF noise performance of scaled Si-MOSFETs and Si/SiGe MODFETs both for mainstream and "extreme-environment" applications.

7.2 Scope for Future Work

The work described in this thesis leads to several interesting and challenging topics that merit further investigation.

- The aggressive scaling of the MOSFET feature size down to sub-65 nm regime has broadened the application space of Si-CMOS technologies to include several microwave and millimeter wave applications, which require device operation at

frequencies as high as 60 GHz or more. This brings in a host of challenges in the layout of good RF test-structures, robust characterization and de-embedding schemes, and modeling methodologies to incorporate distributed effects at such high frequencies. Also, moving into the nanometer regime, requires a deeper understanding of the process and device physics, in order to be able to effectively model these devices and use them for RF IC and system design. The gate tunneling current in highly scaled MOSFETs is an important aspect that needs careful measurement and modeling, as it greatly affects the DC, low-frequency noise and the RF noise performance of MOSFETs.

- For the cryogenic characterization of these scaled MOSFETs, the current system needs to be enhanced to be able to operate at frequencies higher than 50 GHz. For accurate RF noise parameter measurements, it is necessary to be able to make these measurements at higher frequencies, as the DUT noise figures in the 2–10 GHz range is lower than the resolution of the measurement system. Further work is needed in the cryogenic RF noise modeling for a better understanding of the behavior of the intrinsic device noise sources. Also, prototype analog and RF ICs need to be designed for cryogenic operation and design optimization for cryogenic temperatures needs to be investigated.

- A comprehensive study of annular or closed-geometry FETs, in terms of their layout, and their DC, small-signal, and noise performance is required for building radiation-hard circuits.

- Further work is needed in the process optimization and device design of Si/SiGe MODFETs to further improve their RF performance. Development of more complete physical models for the SiGe MODFET simulation is also required for designing robust circuits using this technology.

APPENDIX A

PUBLICATIONS

1. S. Venkataraman, B. Banerjee, C.-H. Lee, J. Laskar, and J. D. Cressler, "Cryogenic Small Signal Operation of 0.18 μm MOSFETs," in *IEEE Silicon Monolithic Integrated Ckts.,* Jan 2007.

2. S. Venkataraman, B. Banerjee, C.-H. Lee, J. Laskar, and J. D. Cressler, "RF Cryogenic Performance and Modeling of 0.12 μm nMOSFETs," being submitted to *IEEE Trans. Electron Dev.*

3. S. Venkataraman, B. Banerjee, C.-H. Lee, J. D. Cressler, J. Laskar, J. Papapolymerou, A. J. Joseph, and S. L. Sweeney, "The Extraction and Modeling of Intrinsic RF Noise Sources in 0.13 μm nMOSFETs," in *IEEE MTT-S Int. Microwave Symp.*, Long Beach, CA, USA, Jun. 2005.

4. S. Venkataraman, B. M. Haugeraud, E. Zhao, B. Banerjee, A. Sutton, P. W. Marshall, C.-H. Lee, J. D. Cressler, J. Laskar, J. Papapolymerou, and A. J. Joseph, "Impact of Proton Irradiation on the RF Performance of 0.12 μm CMOS Technology," in *IEEE Int. Reliability Phys. Symp.*, San Jose, CA, USA, Apr. 2005.

5. B. Banerjee, S. Venkataraman, Y. Lu, Q. Liang, C.-H. Lee, S. Nuttinck, Y.-J. E. Chen, D. Heo, J. D. Cressler, J. Laskar, G. Freeman, and D. C. Ahlgren, "Cryogenic Operation of Third-Generation 200-GHz Peak-fT, Silicon-Germanium Heterojunction Bipolar Transistors," *IEEE Trans. Electron Devices*, vol. 52, pp. 585-593, Apr. 2005.

6. B. Banerjee, S. Venkataraman, C.-H. Lee, and J. Laskar, "Broadband Noise Modeling of SiGe HBT under Cryogenic Temperatures," to be presented in *IEEE RFIC Symp.,* 2007.

7. B. M. Haugeraud, S. Venkataraman, A. K. Sutton, A. P. Gnana Prakash, J. D. Cressler, G. Niu, P. W. Marshall, and A. J. Joseph, "The Impact of Substrate Bias on Proton Damage in 130 nm CMOS Technology," in *IEEE Nuclear and Space Radiation Effects Conf.,* Jul, 2005.

8. A. Raghavan, S. Venkataraman, B. Banerjee, Y. Suh, D. Heo and J. Laskar, "Direct Extraction of an Empirical Temperature-Dependent InGaP-GaAs HBT Large-Signal Model," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1443-1450, Sep. 2003.

9. B. Banerjee, S. Venkataraman, E. Zhao, C.-H. Lee, J. D. Cressler, J. Laskar, B. E.-Kareh, S. Balster, and H. Yasuda, "Modeling of Broadband Noise in Complementary (npn + pnp) SiGe HBTs," in *Dig. IEEE Radio Frequency Integrated Circuits Symp.*, Long Beach, CA, USA, Jun. 2005.

10. B. Banerjee, S. Venkataraman, Y. Lu, S. Nuttinck, D. Heo, Y.-J. E. Chen, J. D. Cressler, J. Laskar, G. Freeman and D. Ahlgren, "Cryogenic Performance of a 200 GHz SiGe HBT Technology," *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 171-173, 2003.

11. S. Pinel, S. Chakraborty, S. Venkataraman, R. Bhatia, S. Mandal, S. Nuttinck, B. Larson, and J. Laskar, "Development of SOI based MMICs for Wireless LAN Applications," in *IEEE MTT-S Int. Microwave Symp.,* pp. 10531056, 2002.

12. B. Banerjee, B. Matinpour, C.-H. Lee, S. Venkataraman, S. Chakraborty and J. Laskar, "Development of IEEE802.11a WLAN LNA in Silicon based Processes,"

in *Dig. IEEE International Microwave Symposium MTT-S*, pp. 1573-1576, 2003.

13. S. Nuttinck, B. Wagner, B. Banerjee, S. Venkataraman, E. Gebara, J. Laskar and M. Harris, "Thermal Analysis of AlGaN/GaN Power Devices," *IEEE Trans. Micro. Theory and Tech.*, pp. 2445-2452, vol. 51, no.12, Dec 2003.

14. S. Nuttinck, E. Gebara, B. Banerjee, S. Venkataraman, J. Laskar and M. Harris, "Applications of GaN Microwave Electronic Devices," *IEICE Transactions on Electronics*, in Special Issue on Microwave and Millimeter Wave Technology, pp. 1409-1415, vol. E86-C, Aug 2003.

15. S. Nuttinck, B. Banerjee, S. Venkataraman, J. Laskar and M. Hooper, "High Temperature Performances of AlGaN/GaN Power HFETs," *IEEE International Microwave Symposium MTT-S Digest*, pp. 221-223, vol. 1, 2003.

16. A. Raghavan, B. Banerjee, S. Venkataraman and J. Laskar, "Direct Extraction of InGaP/GaAs HBT Large Signal Model," in *Proc. IEEE GaAs IC Symposium*, pp. 225-228, 2002.

REFERENCES

[1] H. Sobol, "Microwave Communications - An Historical Perspective," *IEEE Trans. Microwave Theory and Tech.,* vol. 32, pp. 1170–1181, Sep. 1984.

[2] G. C. Corazza, "Marconi's History," *Proc. of the IEEE,* vol. 86, pp. 1307–1311, Jul. 1998.

[3] P. K. Bondyopadhyay, "Under the Glare of a Thousand Suns – The Pioneering Works of Sir J. C. Bose," *Proc. of the IEEE,* vol. 86, pp. 218–224, Jan, 1998.

[4] P. K. Bondyopadhyay, "Sir J. C. Bose's Diode Detector Received Marconi's First Transatlantic Wireless Signal of December 1901 (The "Italian Navy Coherer" Scandal Revisited)," *Proc. of the IEEE,* vol. 86, pp. 259–285, Jan, 1998.

[5] M. R. Pinto, W. F. Brinkman, and W. W. Troutman, " The Transistor's Discovery and What's Ahead," *in Proc. of the European Solid-State Device Research Conf.,* pp. 125–132, 1997.

[6] D. Kahng, "A Historical Perspective on the Development of MOS Transistors and Related Devices," *IEEE Trans. Electron Devices,* vol. 23, pp. 655–657, Jul. 1976.

[7] C. -T. Sah, "Evolution of the MOS Transistor – From Conception to VLSI," *Proc. of the IEEE,* vol. 76, pp. 1280–1326, Oct. 1988.

[8] R. H. Dennard, F. H. Gaensslen, H. -N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," *IEEE J. Solid-State Circuits*, vol. 9, pp. 256–268, Oct. 1974.

[9] E. Morifuji, H. S. Momose, T. Ohguro, T. Yoshitomi, H. Kimijima, F. Matsuoka, M. Kinugawa, Y. Katsumata, and H. Iwai, "Future perspective and scaling down roadmap for RF CMOS," *Dig. Tech. Papers IEEE Symp. VLSI Technology*, pp. 163–164, 1999.

[10] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H. -S. P. Wong, "Device Scaling Limits of Si MOSFET's and Their Application Dependencies," *Proc. of the IEEE,* vol. 89, pp. 259–288, Mar. 2001.

[11] T. Manku, "Microwave CMOS - Device Physics and Design," *IEEE J. Solid-State Circuits*, vol. 34, pp. 277–285, Mar. 1999.

[12] A. J. Joseph, D. L. Harame, B. Jagannathan, D. Coolbaugh, D. Ahlgren, J. Magerlein, L. Lanzerotti, N. Feilchenfeld, S. S. Onge, J. Dunn, and E. Nowak, "Status and Direction of Communication Technologies – SiGe BiCMOS and RFCMOS," *Proc. of the IEEE,* vol. 93, pp. 1539–1558, Sep. 2005.

[13] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998.

[14] A. A. Abidi, "RF CMOS Comes of Age," *IEEE J. Solid-State Circuits*, vol. 39, pp. 549–561, Apr. 2004.

[15] P. H. Woerlee, M. J. Knitel, R. van Langevelde, D. B. M. Klaassen, L. F. Tiemeijer, A. J. Scholten, and A. T. A. Z. -van Duijnhoven, "RF-CMOS Performance Trends," *IEEE Trans. Electron Devices,* vol. 48, pp. 1776–1782, Aug. 2001.

[16] K. Lee, I. Nam, I. Kwon, J. Gil, K. Han, S. Park, and B. Seo, "The Impact of Semiconductor Technology Scaling on CMOS RF and Digital Circuits for Wireless Application," *IEEE Trans. Electron Devices,* vol. 52, pp. 1415–1422, Jul. 2005.

[17] A. Van der Ziel, *Noise in Solid State Devices and Circuits,* New York, Wiley, 1986.

[18] A. A. Abidi, "High-Frequency Noise Measurements on FETs with Small Dimensions," *IEEE Trans. Electron Devices*, vol. 33, pp. 1801–1805, Nov. 1986.

[19] R. P. Jindal, "Hot-Electron Effects on Channel Thermal Noise in Fine-Line NMOS Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 33, pp. 1395–1397, Sep. 1986.

[20] G. Knoblinger, P. Klein, and M. Tiebout, "A New Model for Thermal Channel Noise of Deep-Submicron MOSFETs and its Application in RF-CMOS Design," *IEEE J. Solid-State Circuits*, vol. 36 pp. 831–837, May 2001.

[21] P. Klein, "An analytical thermal noise model of deep submicron MOSFETs," *IEEE Electron Dev. Lett.*, vol. 20, pp. 399–401, Aug. 1999.

[22] R. Kraus, and G. Knoblinger, "Modeling the gate-related high frequency and noise characteristics of deep-submicron MOSFETs," *IEEE Custom Integrated Circuits Conf. 2002*, pp. 209–212.

[23] C. -H. Chen, M. J. Deen, Y. Cheng, and M. Matloubian, "Extraction of the Induced Gate Noise, Channel Noise, and Their Correlation in Submicron MOSFETs from RF Noise Measurements," *IEEE Trans. Electron Devices*, vol. 48, pp. 2884–2892, Dec. 2001.

[24] S. Spedo, and C. Fiegna, "Analysis of thermal noise in scaled MOS devices and RF circuits," *Solid State Electron.*, vol. 46, pp. 1933–1939, Mar. 2002.

[25] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Z. Duijnhoven, and V. C. Venezia, "Noise Modeling for RF CMOS Circuit Simulation," *IEEE Trans. Electron Devices*, vol. 50, pp. 618–632, Mar. 2003.

[26] K. Han, J. Gil, S. -S. Song, J. Han, H. Shin, C. -K. Kim, and K. Lee, "Complete High-Frequency Thermal Noise Modeling of Short-Channel MOSFETs and Design of 5.2-GHz Low Noise Amplifier," *IEEE J. Solid-State Circuits*, vol. 40, pp. 726–735, Mar. 2005.

[27] A. S. Roy, and C. C. Enz, "Compact Modeling of Thermal Noise in the MOS Transistor," *IEEE Trans. Electron Devices*, vol. 52, pp. 611–614, Apr. 2005.

[28] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Z. Duijnhoven, R. de Kort, and D. B. M. Klaassen, "Compact Modelling of noise for RF CMOS circuit design," *IEE Proc.- Circuits Devices Syst.*, vol. 151, no. 2, pp. 167–174, Apr. 2004.

[29] R. P. Jindal, "Compact Noise Models for MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, pp. 2051–2061, Sep. 2006.

[30] M. J. Deen, C. -H. Chen, S. Asgaran, G. A. Rezvani, J. Tao, and Y. Kiyota, "High-Frequency Noise of Modern MOSFETs: Compact Modeling and Measurement Issues," *IEEE Trans. Electron Devices*, vol. 53, pp. 2062–2081, Sep. 2006.

[31] V. Adamian, and A. Uhlir, "A Novel Procedure for Receiver Noise Characterization," *IEEE Trans. Instrum. Meas.*, vol. IM–22, pp. 181–182, Jun. 1973.

[32] V. Adamian, and A. Uhlir, "Simplified Noise Evaluation of Microwave Receivers," *IEEE Trans. Instrum. Meas.*, vol. IM–33, pp. 136–140, Jun. 1984.

[33] H. Rothe, and W. Dahlke, "Theory of noisy four poles," Proc. IRE, vol.44, pp. 811–818, June 1956.

[34] H. Fukui, "The Noise Performance of Microwave Transistors," *IEEE Trans. Electron Devices*, vol. ED-13, pp.329–341, Mar. 1966.

[35] J. Engberg, and T. Larsen, *Noise Theory of Linear and Nonlinear Circuits,* West Sussex, England, John Wiley & Sons Ltd. , 1995.

[36] H. Hillbrand, and P. H. Russer, "An efficient method for computer aided noise analysis of linear amplifier networks." *IEEE Trans. on Circuit Syst.*, vol. CAS-23, pp. 235–238, Apr. 1976.

[37] R. Sung, P. Bendix, and M. B. Das, "Extraction of High-Frequency Equivalent Circuit Parameters of Submicron Gate-Length MOSFETs," *IEEE Trans. Electron Devices*, vol. 45, pp. 1769–1775, Aug. 1998.

[38] J. Han, M. Je, and H. Shin, "A Simple and Accurate Method for Extracting Substrate Resistance of RF MOSFETs," *IEEE Electron Dev. Lett.*, vol. 23, pp. 434–436, Jul. 2002.

[39] Y. P. Tsividis, *O*peration and Modeling of the MOS Transistor, New York, McGraw-Hill, 1988.

[40] S. Venkataraman, B. Banerjee, C. -H. Lee, J. D. Cressler, J. Laskar, J. Papapolymerou, A. J. Joseph, and S. L. Sweeney, "The Extraction and Modeling of Intrinsic RF Noise Sources in 0.13 μm nMOSFETs," *IEEE MTT-S Int. Microwave Symp. Dig. 2005*, Jun. 2005.

[41] B. Jagannathan, *et al.*,"Self-Aligned SiGe NPN Transistors With 285 GHz f_{max} and 207 GHz f_T in a Manufacturable Technology," *IEEE Electron Device Letters*, vol.23, pp. 258–260, May 2002.

[42] B. A. Orner, *et al.*, "A 0.13 μm BiCMOS Technology Featuring a 200/280 GHz (f_T/f_{max}) SiGe HBT," *in Proc. IEEE BCTM 2003*, pp. 203–206.

[43] R. A. Pucel, W. Struble, R. Hallgren, and U. L. Rohde, "A General Noise De-embedding Procedure for Packaged Two-Port Linear Active Devices," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2013–2023, Nov. 1992.

[44] J. Laskar, and M. Feng, "An On-Wafer Cryogenic Microwave Probing System for Advanced Transistor and Superconductor Applications," *Microwave Journal*, vol. 36, pp. 104–114, 1993.

[45] J. Laskar, J. J. Bautista, M. Nishimoto, M. Hamai, and R. Lai, "Development of Accurate On-Wafer Cryogenic Characterization Techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 44, pp. 1178–1183, Jul. 1996.

[46] M. R. Murti, J. Laskar, S. Nuttinck, S. Yoo, A. Raghavan, J. I. Bergman, J. Bautista, R. Lai, R. Grundbacher, M. Barsky, P. Chin, and P. H. Liu, "Temperature-Dependent Small-Signal and Noise Parameter Measurements and Modeling on InP HEMTs," *IEEE Trans. Microwave Theory and Techniques.*, vol. 48, no. 12, pp. 2579–2587, Dec. 2000.

[47] F. H. Gaensslen, L. Rideout, E. J. Walker, and J. J. Walker, "Very small MOSFETs for low temperature operation," *IEEE Trans. Electron Devices.*, vol. ED-24, pp. 218–229, Mar. 1977.

[48] S. K. Tewksbury, "N-channel enhancement mode MOSFET characteristics from 10 to 300 K" *IEEE Trans. Electron Devices.*, vol. 28, pp. 1519–1529, Dec. 1981.

[49] G. Gildenblat, L. Colonna-romano, D. Lau, and D. E. Nelsen, "Investigation of Cryogenic CMOS Performance," *Proc. IEEE IEDM 1985,* pp. 268–271, 1985.

[50] W. F. Clark, B. El-Kareh, R. G. Pires, S. L. Titcomb, and R. L. Anderson, "Low Temperature CMOS - A Brief Review," *IEEE Trans. on Components, Hybrids, and Manufacturing Technology.*, vol. 15, pp. 397–404, Jun. 1992.

[51] F. Balestra, and G. Ghibaudo, "Brief Review of the MOS Device Physics For Low Temperature Electronics," *Solid-State Electronics*, vol. 37, no. 12, pp. 1967–1975, 1994.

[52] G. Ghibaudo, and F. Balestra, "Low Temperature Characterization of Silicon CMOS Devices," in *Proc. 20th Int. Conf. on Microelectronics*, Sep. 1995, pp. 613–622.

[53] B. Yu, H. Wang, C. Riccobene, H. -S. Kim, Q. Xiang, M. R. Lin, L. Chang, and C. Hu, "Nanoscale CMOS at Low Temperature: Design, Reliability, and Scaling Trend," in *Dig. Tech Papers VLSI Technology Symp.*, Apr. 2001, pp. 23–25.

[54] J. Y-C. Sun, Y. Taur, R. H. Dennard, and S. P. Klepner, "Submicrometer-Channel CMOS for Low-Temperature Operation," *IEEE Trans. Electron Devices*, vol. 24, pp. 19–27, Jan. 1987.

[55] S. Selberherr, "MOS Device Modeling at 77K," *IEEE Trans. Electron Devices.*, vol. 36, pp. 1464–1474, Aug. 1989.

[56] G. Gildenblat, and C. -L. Huang, "N-Channel MOSFET Model for the 60-300-K Temperature Range," *IEEE Trans. Computer-Aided Design.*, vol. 10, no. 4, pp. 512–518, Apr. 1991.

[57] M. J. Deen, "Digital Characteristics of CMOS Devices at Cryogenic Temperatures," *IEEE J. Solid-State Circuits*, vol. 24, pp. 158–164, Feb. 1989.

[58] P. Martin, M. Bucher, and C. Enz, "MOSFET Modeling and Parameter Extraction for Low Temperature Analog Circuit Design," *J. Phys IV France,* pp. 51–56, 2002.

[59] Y. Taur, and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, New York, 1998.

[60] M. W. Pospieszalski, S. Weinreb, R. D. Norrod, and R. Harris, "FET's and HEMT's at Cryogenic Temperatures - Their Properties and Use in Low-Noise Amplifiers," *IEEE Trans. Microwave Theory Tech.*, vo. 36, pp. 552–560, Mar. 1988.

[61] A. Siligaris, G. Pailloncy, S. Delcourt, R. Valentin, S. Lepilliet, F. Danneville, D. Gloria, and G. Dambrine, "High-Frequency and Noise Performances of 65-nm MOSFET at Liquid Nitrogen Temperature," *IEEE Trans. Electron Devices*, vol. 53, pp. 1902–1908, Aug. 2006.

[62] S. Venkataraman, B. Banerjee, C. H. -Lee, J. Laskar, and J. D. Cressler, "Cryogenic Small Signal Operation of 0.18 μm MOSFETs," in *Proc. IEEE SiRF 2007*, pp. 52 – 55, Jan. 2007.

[63] M. J. Deen, and Z. X. Yan, "DIBL in Short-Channel NMOS Devices at 77K," *IEEE Trans. Electron Devices*, vol. 39, pp. 908–915, Apr. 1992.

[64] R. S. Muller, T. I. Kamins, and M. Chan, *Device Electronics for Integrated Circuits*, Third Edition, John Wiley & Sons, 2002.

[65] E. Takeda, C. Y. Yang, and A. Miura-Hamada, *Hot-Carrier Effects in MOS Devices*, Academic Press, San Diego, CA, 1995.

[66] P. Heremans, R. Bellens, G. Groeseneken, and H. E. Maes, "Consistent Model for the Hot-carrier Degradation in n-channel and p-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, pp. 2194–2209, 1998.

[67] P. E. Cottrell, R. R. Troutman, and T. H. Ning, "Hot-electron emission in n-channel IGFETs," *IEEE Trans. Electron Devices*, vol. 26, pp. 520–533, 1979.

[68] K. K. Ng, and G. W. Taylor, "Effects of hot-carrier trapping in n- and p-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 30, pp. 871–876, Aug. 1983.

[69] K. -L. Chen, S. A. Saller, I. A. Groves, and D. B. Scott, "Reliability Effects on MOS Transistors due to Hot-carrier Injection," *IEEE Trans. Electron Devices*, vol. 32, pp. 386–393, 1985.

[70] F. -C. Hsu, and K. -Y. Chiu, "Temperature Dependence of hot-electron Induced Degradation in MOSFETs," *IEEE Electron Device Letters*, vol. 5, pp. 148–150, 1984.

[71] E. Takeda, A. Shimizu, and T. Hagiwara, "Role of Hot-hole Injection in Hot-carrier Effects and the Small Degraded Region in MOSFETs," *IEEE Electron Device Letters*, vol. 4, pp. 329–331, 1983.

[72] H. Gesch, J. -P. Leburton, and G. E. Dorda, "Generation of Interface States by Hot Hole Injection in MOSFETs," *IEEE Trans. Electron Devices*, vol. 29, pp. 913–918, 1982.

[73] C. Hu, S. C. Tam, F. -C. Hsu, P. -K. Ko, T. -Y. Chan, and K. W. Terrill, "Hot-electron Induced MOSFET Degradation - Model, Monitor, and Improvement," *IEEE Trans. Electron Devices*, vol. 32, pp. 375–384, Feb. 1985.

[74] M. Aoki, S. Hanamura, T. Masuhara, and K. Yano, "Performance and Hot-Carrier Effects of Small CRYO-CMOS Devices," *IEEE Trans. Electron Devices*, vol. 34, pp. 8–18, Jan. 1987.

[75] S. L. Von Bruns, and R. L. Anderson, "Hot-Electron-Induced Interface State Generation in n-Channel MOSFETs at 77 K," *IEEE Trans. Electron Devices*, vol. 34, pp. 75–82, Jan. 1987.

[76] J. Y. C. Sun, and M. R. Wordeman, "Degradation of 77-K MOSFET Characteristics Due to Channel Hot Electrons," *IEEE Trans. Electron Devices*, vol. 31, pp. 1970, Dec. 1984

[77] F. -C. Hsu, J. Hui, and K. -Y. Chiu, "Hot-electron Degradation in Submicron VLSI," *in IEDM Tech. Digest,* pp. 48–51, 1985.

[78] B. Doyle, M. Bourcerie, J. -C. Marchetaux, and A. Boudou, "Interface State Creation and Charge Trapping in the Medium-to-High Gate Voltage Range ($V_d/2 \geq V_g \geq V_d$) During Hot-Carrier Stressing of n-MOS Transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 744–754, Mar. 1990.

[79] M. Song, J. S. Cable, K. P. MacWilliams, and J. C. S. Woo, "Dependence of LDD Device Optimization on Stressing Parameters at 77 K," *in IEDM Tech. Digest,* pp. 223–226, 1990.

[80] M. Song, K. P. MacWilliams, J. S. Cable, and J. C. S. Woo, "Bias and Temperature Dependence of Hot Carrier Lifetime from 77 K to 300 K," *in IEDM Tech. Digest,* pp. 707–710, 1992.

[81] J. W. Ratkovic, R. C. Lacoe, K. P. MacWilliams, M. Song, S. Brown, and G. Yabiku, " New understanding of LDD CMOS hot-carrier degradation and device lifetime at cryogenic temperatures," *in IEEE Intl. Reliability Phys. Symp. Digest,* pp. 312–319, Apr. 1997.

[82] Z. Chen, K. Hess, J. Lee, J. W. Lyding, E. Rosenbaum, I. Kizilyalli, S. Chetlur, and R. Huang, "On the Mechanism for Interface Trap Generation in MOS Transistors Due to Channel Hot Carrier Stressing," *IEEE Electron Device Letters*, vol. 21, pp. 24–26, Jan. 2000.

[83] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors.* Boston, MA: Artech House, 2003.

[84] T. P. Ma and P. V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits.* New York: Wiley, 1989.

[85] S. Venkataraman, B. M. Haugerud, E. Zhao, B. Banerjee, A. Sutton, P. W. Marshall, C. -H. Lee, J. D. Cressler, J. Laskar, J. Papapolymerou, and A. J. Joseph, "Impact of Proton Irradiation on the RF Performance of 0.12 μm CMOS Technology," *IEEE 43rd Annual International Reliability Physics Symp. 2005*, Apr. 2005, pp. 356–359.

[86] B. M. Haugerud, S. Venkataraman, A. K. Sutton, A. P. Gnana Prakash, J. D. Cressler, G. Niu, P. W. Marshall, and A. J. Joseph, "The Impact of Substrate Bias on Proton Damage in 130nm CMOS Technology," *IEEE Nuclear and Space Radiation Effects Conf. Dig. 2005*, Jul. 2005.

[87] K. M. Murray *et al.*, *Nuclear Inst. and Methods*, vol. B56/57, p. 616, 1991.

[88] P. W. Marshall *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1958-1965, 1994.

[89] G. Niu, S. J. Mathew, G. Banerjee, J. D. Cressler, S. D. Clark, M. J. Palmer, and S. Subanna, "Total Dose Effects on the Shallow-Trench Isolation Leakage Current Characteristics in a 0.35μm SiGe BiCMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 46, pp. 1841-1847,Dec. 1999.

[90] Y. Li, J. D. Cressler, Y. Lu, J. Pan, G. Niu, R. A. Reed, P. W. Marshall, C. Polar, M. J. Palmer, and A. J. Joseph, "Proton Tolerance of Multiple-Threshold Voltage and Multiple-Breakdown Voltage CMOS Device Design Points in a 0.18 μm System-on-a-Chip CMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 1834–1838,Dec. 2003.

[91] D. L. Harame, S. J. Koester, G. Freeman, P. Cottrel, K. Rim, G. Dehlinger, D. Ahlgren, J. S. Dunn, D. Greenberg, A. Joseph, F. Anderson, J. -S. Rieh, S. A. S. T. Onge, D. Coolbaugh, V. Ramachandran, J. D. Cressler, and S. Subanna, "The revolution in SiGe: Impact on device electronics," *Applied Surface Science,* pp. 9–17, 2004.

[92] S. V. -Vandebroek, E. F. Crabbè, B. S. Meyerson, D. L. Harame, P. J. Restle, and J. M. C. Stork, "Design Issues For SiGe Heterojunction FETs," *in Proc. IEEE Conf. on Adv. Concepts in High Speed Semiconductor Dev. and Circuits,* pp. 425–434, Aug. 1991.

[93] M. Glück, T. Hackbarth, M. Birk, A. Haas, E. Kohn, and U. König, "Design and Fabrication of Si/SiGe n-type MODFETs," *Physica E Low-Dimensional Systems and Nanostructures,* pp. 763–767, Jul. 1998.

[94] U. König, M. Zeuner, G. Höck, T. Hackbarth, M. Glück, T. Ostermann, and M. Saxarra, "n- and p-Type SiGe HFETs and Circuits," *Solid State Electronics,* pp. 1383–1388, 1999.

[95] W. Lu, R. Hammond, S. J. Koester, X. W. Wang, J. O. Chu, T. P. Ma, and I. Adesisa, "High Performance 0.15 μm Self-Aligned SiGe p-MOS-MODFET's with SiN Gate Dielectric," *in IEDM Tech. Digest,* pp. 577–580, 1999.

[96] M. Zeuner, T. Hackbrath, G. Höck, D. Behammer, and U. König, "High-Frequency SiGe-n-MODFET for Microwave Applications," *IEEE Microwave and Guided Wave Letters,* vol. 9, pp. 410–412, Oct. 1999.

[97] S. J. Koester, K. L. Saenger, J. O. Chu, Q. C. Ouyang, J. A. Ott, M. J. Rooks, D. F. Canaperi, J. A. Tornello, C. V. Jahnes, and S. E. Steen, "80 nm gate-length $Si/Si_{0.7}Ge_{0.3}$ n-MODFET with 194 GHz f_{max}," *Electon. Lett.,* vol. 39, Nov. 2003.

[98] S. J. Koester, K. L. Saenger, J. O. Chu, Q. C. Ouyang, J. A. Ott, K. A. Jenkins, D. F. Canaperi, J. A. Tornello, C. V. Jahnes, and S. E. Steen, "Laterally Scaled $Si - Si_{0.7}Ge_{0.3}$ n-MODFETs with $f_{max} > 200\ GHz$ and Low Operating Bias," *IEEE Electron Device Letters*, vol. 26, pp. 178–180, Mar. 2005.

[99] M. Enciso, N. Zerounian, P. Crozat, T. Hackbrath, J. -H. Herzog, and F. Aniel, "HF Noise Performance and Modelling of SiGe HFETs," *in Proc. Intl. Conf. on Noise and Fluctuations,* pp. 287–290, 2005.

[100] M. Enciso, P. Crozat, T. Hackbrath, H. -J. Herzog, and F. Aniel, "Microwave Noise Performance and Modeling of SiGe-Based HFETs," *IEEE Trans. Electron Devices*, vol. 52, pp. 2409–2415, Nov. 2005.

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