DESIGN AND INTEGRATION OF HYBRID AND MONOLITHIC MICROWAVE POWER AMPLIFIERS FOR WIDEBAND APPLICATIONS USING GALLIUM NITRIDE TECHNOLOGY

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“Why?”

“Why not?”

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LIST OF SYMBOLS AND ABBREVIATIONS

ADS.....Keysight's Advanced Design System

AlN.....Aluminum Nitride

AuSn .....Gold Tin

CuW .....Copper Tungsten

DC-IV .....Direct-Current Current-Voltage

DC-MCW.....Direct-Current – Multi Contact Wafer

DPA.....Distributed Power Amplifier

DUT ..... Device Under Test

EM..... Electromagnetic

GaAs .....Gallium Arsenide

GaN .....Gallium Nitride

HEMT .....High Electron Mobility Transistor

HMIC .....Hybrid Microwave Integrated Circuit

LDMOS.....Laterally Diffused Metal Oxide Semiconductor

MMIC ..... Monolithic Microwave Integrated Circuit

NASA.....National Aeronautics and Space Administration

NDPA.....Non-Uniform Distributed Power Amplifier

NRC ..... National Research Council of Canada

PA .....Power Amplifier

PAE.....Power Added Efficiency

PDK.....Process Development Kit

P_{IN} .....Input Power

P_{OUT}..... Output Power

P_{SRC} ..... Source Power

SiC..... Silicon Carbide

SMD..... Surface Mount Device

SOLT..... Short Open Load Thru (calibration method)

TaN ..... Tantalum Nitride

TRL..... Through Reflect Line (calibration method)

TWA ..... Traveling-Wave Amplifier

TWTA..... Traveling-Wave Tube Amplifier

UC..... Unit Cell

UWBPA ..... Ultra-Wideband Power Amplifier

SUMMARY

The objective of this research is to compare and advance the predominant methods of realizing broadband microwave power amplifiers (PAs) up to 40 GHz with high efficiency using gallium nitride (GaN) technology. The studied architectures are based on the reactive/resistive matching approach and the traveling wave technique in both hybrid and monolithic microwave integrated circuits (MMICs). Important details of design development and integration are discussed, featuring discrete component descriptions, substrate material selections, additional matching techniques, and comparisons of both wirebonds and flip-chip bonds that are used for PA interconnections.

With a focus on improving the bandwidth and efficiency of the architectures mentioned above, the presented hybrid PA designs achieve state-of-the-art performance with commercially-available GaN power transistors. This work demonstrates the highest power added efficiency (27–48%) and widest bandwidth (1.0-11.5 GHz) for a multi-watt hybrid PA implementation.

To complement these novel hybrid PA designs and integration developments, broadband MMIC PAs were designed at higher frequencies. The results of device characterization and wideband modeling are presented for a new 0.15 μm GaN process in support of a 3-stage broadband MMIC PA design with reactive/resistive matching. Lastly, an ultra-wideband non-uniform distributed PA design is fabricated on a pre-release version of a new 0.14 μm GaN process. For the first time, a GaN MMIC PA with output power greater than 1 W and nearly 10% power added efficiency was successfully achieved from 2 to 40 GHz, surpassing previously-reported results.

CHAPTER 1:

INTRODUCTION

"Our astonishment at what has been accomplished would be uncontrollable were it not held in check by the expectation of greater miracles to come."

– Nikola Tesla, 1905

Ever since the days of the spark gap experiments, humans have been discovering and inventing new techniques to harness electromagnetic phenomena for the benefit of mankind [1]. Developments in the generation, amplification, transmission, and reception of high-frequency electromagnetic waves have unlocked an expansive set of applications for microwave technology. From the revolutionary emergence of terrestrial radio telegraphy [2] to the remarkable normalcy of a satellite video feed from across the globe, advancements in the wireless arts have been transforming the ways in which people communicate with one another for over a century.

Moreover, the utility of microwave radiation extends far beyond communication. This type of energy can interact with our environment in predictable patterns, thereby forming the basis for spectroscopy and remote sensing. The study of these interactions can both deepen our understanding of the universe around us [3] and enhance our quality of life here on Earth. Since their initial development in the 1930s for defense purposes [4], modern radar systems have found enduring success in aerospace, marine, and weather

applications. Because these systems usually require high levels of microwave power to function, there is naturally a strong interest in both novelty and improvement of devices that can offer high output power at high frequencies. It is the role of the power amplifier (PA) circuitry to realize these high-powered signals in a microwave system.

The primary objective of a PA design is to deliver the highest output power possible from a selected active device [5]. Similar emphasis is often placed on maximizing the power added efficiency (PAE) of a power amplifier design, as PAE represents how well the amplifier accomplishes the conversion from direct current (DC) and microwave input power to microwave output power. Another important PA metric is its power gain, which indicates the amount of signal amplification at a given level of output power. Some additional figures of merit describe the noise figure, matching quality, and degree of non-linearity. Depending on the intended application, these parameters can be included in PA design optimizations as well. Whatever the specific design goals may be, a PA must deliver power to a load across a range of operating frequencies.

The PA is at the heart of any communication system, and modern communication systems demand wideband performance. Increases in wideband power amplifier (PA) output power and large signal gain are critical for advancements in electronic warfare, next-generation wireless communication, and multi-band radar applications. Amplifier designs for these applications – and others, such as phased arrays and satellites – could benefit from increased bandwidth, reduced size, and improved efficiency. Two different technologies can enable us to meet the requirements of these high-performance applications: traveling-wave tubes and semiconductor devices.

Radar systems have historically employed traveling wave tubes for the required power amplification, but the tubes are large and heavy, require kV range supply voltages, have poor reliability, and often fail catastrophically [6]. Semiconductor technologies such as silicon-based laterally diffused metal oxide semiconductors (Si-LDMOS), gallium arsenide (GaAs), and gallium nitride on silicon carbide (GaN-on-SiC) have also been developed to address the challenges of high-power microwave amplification. Si-LDMOS is a mature semiconductor process that can deliver kW levels of output power, but it is currently limited to a maximum usable frequency of about 6 GHz [7]. While GaAs has excellent linearity characteristics and frequency response, it suffers from low power density and low breakdown voltage [8].

In contrast to Si-LDMOS and GaAs, GaN-on-SiC has an unprecedented combination of power density, thermal conductivity, and breakdown voltage. This technology alone has demonstrated high power and high-frequency operation over wide bandwidths in a solid-state amplifier [9]. Beginning in the late 1990s, significant investments in GaN technology – from both government [10] and industry [11] sponsors – have spurred massive research efforts, streamlined manufacturing processes, and sparked enormous commercial market growth. With Wolfspeed's announcement in April 2016 that its GaN-on-SiC process has demonstrated compliance with NASA reliability standards for satellite and space systems [12], GaN technology is poised to aggressively expand into this perfectly-suited market.

Because of their higher operating voltage and current density, GaN devices exhibit a relatively higher load impedance for a given power level [9] as compared to other semiconductor technologies. This lower transformation ratio to match a standard 50 Ω load

is a major asset in wideband microwave circuit design. The higher output power density (over 4.5 W/mm) provided by GaN process technology is supported by its SiC substrate, which can significantly improve the thermal performance of the device. By harnessing these characteristics of GaN technology, future innovations in broadband PA design can offer improvements in size and weight to existing applications, increase data transmission rates, and facilitate development of novel transmission encoding schemes. In addition to supporting wider bandwidths in high-power circuits, GaN high electron mobility transistors (HEMTs) can withstand severe impedance mismatches without failure [13]. Therefore, the use of GaN devices can provide a microwave system with a higher degree of interoperability, reliability, and simplicity. Considering these compelling benefits, this dissertation is concentrated on the design and integration of broadband microwave power amplifiers using GaN technology.

1.1 Background

To capitalize on the benefits of GaN technology, a microwave circuit designer must select an implementation method for bringing a design into reality. After the nascent years of microwave system development using waveguides, mechanical processing improvements enabled the fabrication of passive microwave circuits on planar dielectric substrates. When an active microwave component – such as a transistor – is bonded onto this passive structure, the resulting device is termed a hybrid microwave integrated circuit (HMIC). This hybrid circuit is contrasted by a monolithic microwave integrated circuit (MMIC), which has all of its passive and active elements integrated into a single chip by a

semiconductor technology process [14]. These two integration methods are complementary in many ways [15], as shown in Figure 1.

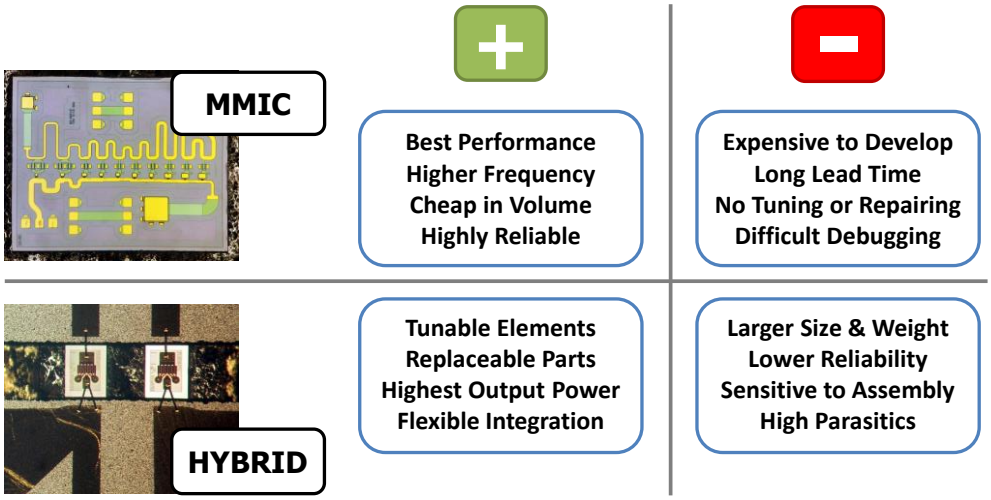


Figure 1 - MMIC and HMIC comparison

However, regardless of their individual characteristics, all MMICs will eventually become hybrids. An MMIC is of no use alone, as it must connect to other chips for bias, logic, thermal sinking, and other such functions. The distinction can be recognized by the degree of integration, and the lower parasitics can provide the MMIC with a larger bandwidth and higher frequency response. Yet, both HMICs and MMICs in GaN technology must contend with the effects of high thermal dissipation. This issue directly influences many design decisions, such as substrate material selection and die attach method. Given the substantial power density of GaN technology, the careful management of heat with prudent integration and packaging techniques can help to improve the performance of any GaN PA design [9].

Achieving multi-octave bandwidths in power amplifiers is particularly challenging due to several inherent properties of microwave transistors. The frequency-dependent gain roll-off, usually 4-6 dB/octave, must be compensated with additional circuitry to obtain a flat gain profile [16]. The input and output impedances of the transistor also vary with frequency, and they must be matched across the entire design bandwidth. Furthermore, to achieve higher output power levels with a given technology, the device's size must be increased. This increase in active periphery drives the transistor's impedances even lower. With such a high transformation ratio for operation in a 50 Ω environment, the quality of the match will suffer for a wideband design, reducing PAE and increasing the likelihood of thermal degradation.

Several circuit topologies have been developed to achieve broadband amplifier performance at microwave frequencies [16]. Each topology has its own methods and trade-offs to address these and other broadband design challenges. The main two topologies used in microwave PA design are reactive/resistive matching and the traveling-wave technique [17]. The reactive/resistive matching approach involves the use of reactive elements (capacitors, inductors, transmission lines) and resistors in the design of transistor matching networks [18]. A broadband PA using this approach will require a higher number of elements to achieve both the impedance transformation necessary for 50 Ω system operation and the gain compensation for a flat gain profile [16]. Reactive/resistive matching can yield better large-signal performance (i.e., higher output power, gain, and/or PAE) if the matching network design can tune the source and load to their optimal values

over the desired band. However, it is typically more limited in bandwidth than a traveling-wave design.

A traveling-wave amplifier (also known as a distributed PA) involves cascading several transistors together, as shown in Figure 2, and designing their interconnections as artificial transmission lines (ATLs). The gate and drain interconnection lines are optimized to enable in-phase addition of transistor currents at each cell and absorb the transistor capacitances for broadband operation [19]. While a traveling wave amplifier can realize an extremely wide bandwidth, it comes at the cost of reduced power gain and reduced output power density. When the transistor cells of a traveling-wave amplifier have different active peripheries, the design is said to be non-uniform. This adjustment in methodology can help to improve the output power and efficiency of a distributed amplifier design. With that in mind, this research is focused on enhancing the performance of two selected topologies – the reactive/resistive matching approach and the traveling wave technique – in both HMIC and MMIC implementations.

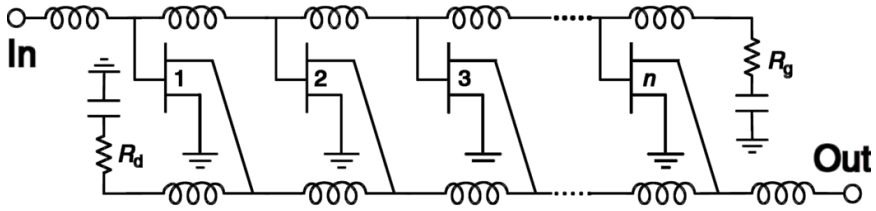


Figure 2 - Simplified diagram of a traveling-wave amplifier [17]

1.2 Recent Developments in Wideband PA Design

Microwave applications in the 1-40 GHz range – such as radar, wireless communication, and remote sensing – have an immense impact on our way of life.

Considering this impact, sustained research efforts have concentrated on improving the performance of the underlying technologies that enable these applications. Since the PA is an essential component of many microwave systems, many published works have focused on innovative PA designs in both HMIC and MMIC implementations.

Hybrid Microwave Integrated Circuit Power Amplifiers

With an aim of improving radar efficiency and range, several hybrid PA designs near X band have employed the reactive/resistive matching technique with GaN dies. Results have been reported from 1.6-14.1 W output power at 15-32% PAE and bandwidths in the 3-10 GHz range [20], [21]. This output power range is studied most often because a multi-watt PA module is typically selected as the "unit cell," or fundamental building block, of a high-power PA that uses many modules to achieve kilowatt levels of output power. It also represents the region of output power where thermal effects can begin to seriously degrade a device's performance. To mitigate this thermal degradation by physically spreading out the heat sources, a four-way Wilkinson division PA on AlN with four 1 mm-class GaN dies was designed in [22]. That publication reported measurements of 20% PAE and 8.5 W output power, giving a power density of 2.2 W/mm.

While increased output power and reduced thermal degradation are essential objectives in a GaN PA design, improvements in PAE and bandwidth are vital for driving the mobile broadband applications of tomorrow. A flip-chip hybrid design in [23] produced 1.8 W output power from 6.5-16 GHz at 17-39% PAE, featuring a wide bandwidth and high efficiency. However, the GaN dies required special processing, and device heating

becomes problematic because the flip-chip method of die attach creates a very poor thermal sink. Further improvements were reported in [24], where the design achieved a decade bandwidth and high PAE, but had an upper frequency limit of 4.1 GHz.

The best hybrid performance was published in [25], where 5 W output power and 20-33% PAE were measured over a 0.35-8 GHz bandwidth. Analysis of these previously-published results suggested that a multi-watt, ultra-wideband PA design using the reactive/resistive approach with commercial GaN dies above 10 GHz was unexplored for a hybrid implementation. Therefore, part of this work is devoted to the design of a reactively-matched multi-watt hybrid GaN PA covering the L-X bands.

Previously-published examples of an HMIC PA using the distributed approach at microwave frequencies are limited. When compared with an MMIC, the transistor interconnection parasitics can be large in a hybrid implementation, and device parasitics can be large for even the smallest singulated GaN HEMT die. Therefore, prior designs have concentrated on a lower frequency range, with [26] reporting 5-10 W output power and 20-50% PAE from 0.02-3 GHz. Since the published literature has not generally addressed the challenges of ultra-wideband distributed PA design near X band in a hybrid implementation, that area represents another focal point of this dissertation.

Monolithic Microwave Integrated Circuit Power Amplifiers

Significant research into the GaN MMIC implementation of reactive/resistive PAs in the X-Ku bands has been conducted, and the published results are summarized in the

comparison table of [27]. Five of these results cover a 100% relative bandwidth, from 6-18 GHz, which is a valuable range of operation for multi-band radar and electronic warfare applications. Further analysis of the results provides insight into the performance trade-off of output power, PAE, and bandwidth in a wideband GaN MMIC PA. As the output power of the reported MMICs increases from 2 W to 16 W, the average PAEs tend to decrease from 28% to 17%. In two other publications shown in [27], an increase of bandwidth to 6-20 GHz led to 2.5 W output power and 10% average PAE. Conversely, a decrease of bandwidth to 8-14 GHz led to 3.2 W output power and 41% average PAE. Another important facet to the performance trade-off described above is output power density, as it impacts the size and weight of the fabricated PA. A reduced physical footprint is beneficial in both commercial and military applications, so a piece of this work is allocated to improving the output power per die area in a multi-stage wideband GaN MMIC PA design.

Compared to HMICs, the use of a distributed approach in MMICs is demonstrated more frequently in publications. Most of these publications have targeted the 2-20 GHz band. The best reported PAs have achieved 10-20 W output power with 12-39% PAE over this band using GaN technology [28], [29]. However, few publications have addressed the additional challenges as frequency and bandwidth are increased. One such publication presented a 2-stage distributed MMIC using 100 nm GaN technology with output power of 0.5 W from 8-42 GHz [30]. The same author also reported 1 W output power from 6-37 GHz with 10% PAE in a dual-stage distributed MMIC design [31], representing the first time this level of output power had been achieved over such a wide band. Given these

previously published works, a portion of this research is dedicated to achieving multi-watt output power up to 40 GHz in a distributed GaN MMIC PA design.

Before any amplifier designs can be studied, we first need to have a device model that accurately represents the power transistor's performance. To better understand the fundamental relationships of PA design for large signal operation, Chapter 2 explores the different measurement techniques and challenges related to non-linear device characterization and modeling. In preparation for an MMIC PA design, the chapter concludes with the creation of a compact model for a new GaN transistor. Chapter 3 begins with the verification of a manufacturer's model for a commercially-available GaN device, and then presents the design, fabrication, assembly, and measurement of three different *hybrid* microwave PAs. Finally, Chapter 4 presents the design, fabrication, assembly, and measurement of three different *monolithic* microwave PAs. Large-signal PA characteristics will now be discussed to provide context for the upcoming measurement techniques and modeling results.

CHAPTER 2:

LARGE SIGNAL DEVICE CHARACTERIZATION

To attain broadband amplifier performance at microwave frequencies, it is imperative to understand and predict how an active device will behave under the expected range of operating conditions. Due to their parasitic reactances, active devices generally have low gain at microwave frequencies. Compensation of these parasitics is critical to obtain useable gain in a microwave amplifier [5]. Furthermore, any conductor used for interconnections has appreciable electrical length with respect to wavelength at microwave frequencies. Since quasi-static circuit theory is not valid under these conditions, transmission line theory is applied to include these interconnections as part of the circuit.

In a linear amplifier design, an active device is provided a simultaneous conjugate match at its input and output ports for optimal gain. Although preliminary power amplifier designs can often be obtained through modification of linear amplifier designs, PAs are typically operated under nonlinear conditions [5]. When a PA is driven with a large signal, or a signal of sufficient magnitude to cause bias variations or gain compression, the active device begins to behave in a nonlinear manner. Unfortunately, accurate predictions of device performance in a nonlinear region cannot generally be obtained from linear methods alone. This dilemma is what imposes the requirement of nonlinear device characterization and modeling in PA design. To help determine the optimal termination conditions for nonlinear operation, we use the load-pull technique.

2.1 Load-pull Technique

A power amplifier design is typically focused on achieving maximum output power (or PAE, or both) from an active device. The impedances required for optimal power or optimal efficiency can be significantly different from the impedances required for optimal gain [5]. The most prevalent method of determining the optimal large signal impedances for an active device is to perform a sequence of device measurements under large signal drive conditions for a range of swept impedance values. This process, known as *load-pull*, is widely employed for characterizing the nonlinear behavior of microwave transistors [33].

Figure 3 illustrates the value of the load-pull technique by comparing the output power of an amplifier under two different output impedance conditions: conjugate match and power match. Although gain is slightly lower, almost 2 dB of additional output power is realized from the active device when it is provided with an optimal power match. Consequently, to obtain the best large signal performance in a PA design, the transistor's output port is not presented with a linear conjugate match [5]. Instead, load-pull is used to determine the optimal matching conditions for the device.

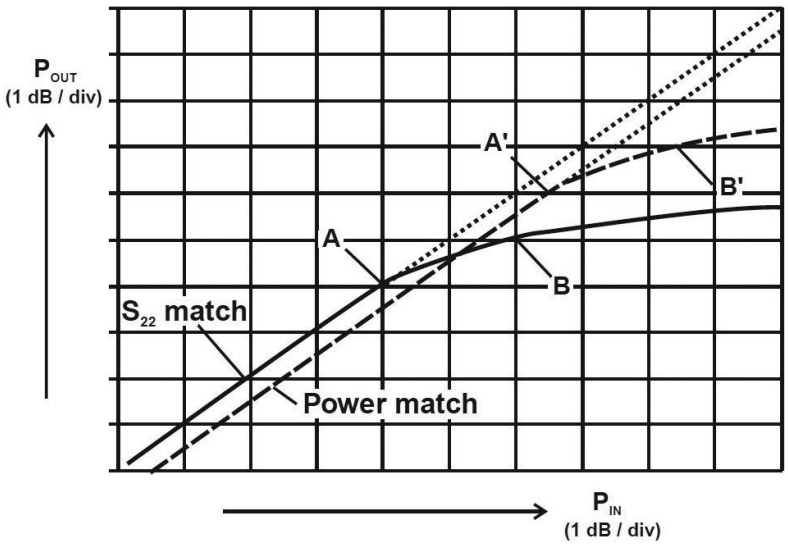


Figure 3 - Power and compression characteristics for different output matching conditions [5].

2.1.1 Theory of Operation

Load-pull measurement systems have evolved over time to improve accuracy, speed, and flexibility; but their underlying principle has remained the same: vary the impedance presented to a device under test (DUT), and measure the device performance over a range of excitation conditions [32]. The generic power wave block diagram in Figure 4 is annotated to help clarify the relationships and performance metrics defined below.

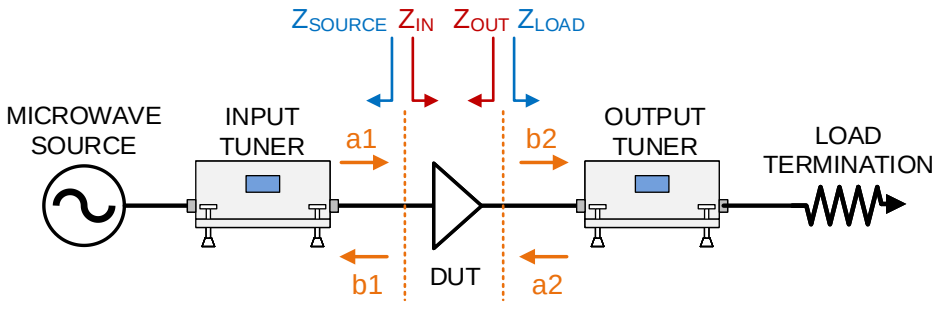


Figure 4 - Annotated power wave block diagram

The input reflection coefficient Γ_{IN} of the DUT, which is related to its input impedance Z_{IN}, is defined below in Equation 1. The input power P_{IN} (Equation 2) describes the power that is actually delivered to the DUT and amplified by the active device. Equation 3 defines the source power P_{SOURCE}, which is the power available from a microwave source with an internal impedance of Z_{SOURCE}. Lastly, Equation 4 describes the output power $P_{OUT,}$ or the power delivered by the DUT to the load impedance $Z_{LOAD.}$

$$\Gamma_{IN} = \frac{b1}{a1} \tag{1}$$

$$P_{IN} = \frac{1}{2}(|a1|^2 - |b1|^2) = \frac{1}{2}|a1|^2 * (1 - |\Gamma_{IN}|^2) \tag{2}$$

$$P_{SOURCE} = \frac{P_{IN}}{1 - \left|\frac{Z_{IN} - Z_{SOURCE}}{Z_{IN} + Z_{SOURCE}}\right|^2} \tag{3}$$

$$P_{OUT} = \frac{1}{2}(|b2|^2 - |a2|^2) = \frac{1}{2}|b2|^2 * (1 - |\Gamma_{LOAD}|^2) \tag{4}$$

Note that P_{SOURCE} (power available from the source) is always greater than P_{IN} (input power delivered to the DUT), except under perfect input matching conditions where $Z_{SOURCE} = Z_{IN}*$. With these definitions of power, we can now create several different ratios of power which describe specific gain relationships. The power gain G_P is the output power to input power ratio (Equation 5). In other words, power gain is the ratio of power delivered

into the load to power delivered into the DUT. This is contrasted by transducer power gain G_T, found in Equation 6, which is the ratio of output power to source power.

$$G_P = \frac{P_{OUT}}{P_{IN}} = \frac{|b2|^2 * (1 - |\Gamma_{LOAD}|^2)}{|a1|^2 * (1 - |\Gamma_{IN}|^2)} \tag{5}$$

$$G_T = \frac{P_{OUT}}{P_{SOURCE}} = \frac{|b2|^2 * (1 - |\Gamma_{LOAD}|^2)}{|a1|^2 * (1 - |\Gamma_{IN}|^2)} * \left(1 - \left|\frac{Z_{IN} - Z_{SOURCE}}{Z_{IN} + Z_{SOURCE}}\right|^2\right) \tag{6}$$

Lastly, we define power added efficiency (PAE) of the DUT as the ratio of power added to power consumed. As Equation 7 shows, the P_{IN} (not the P_{SOURCE}) must be known in order to accurately calculate PAE. P_{DC} is the total DC power consumed by the DUT, and linear quantities should be used for all values in Equation 7.

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}}\% \tag{7}$$

The primary goal of a load-pull system is to measure the quantities defined in Equations 1-7 [32] at every selected impedance condition. Impedance tuning is achieved using either passive mechanical tuners, active amplifier tuners, or a combination of both. A passive mechanical tuner uses the relative positioning of its internal passive elements to determine which part of the signal is transmitted through the tuner and which part of the signal is reflected back toward the signal source [33]. In this way, the magnitude and phase of the impedance at the DUT can be controlled. If fixture losses are minimized, a wide

range of impedances on the Smith Chart can be presented to the DUT. In contrast to the partial signal reflection of a mechanical tuner in a passive load-pull system, an active load-pull system injects a signal at a particular magnitude and phase to tune the impedance at the DUT [34]. Since an external amplifier is used for this active signal injection, the entire range of the Smith Chart can be presented to the device.

For characterization of power devices, a load-pull system will typically be configured to associate the impedance presented to the DUT with the measured large-signal parameters (e.g., output power, power added efficiency, power gain). Measurements are collected over a swept range of impedances, and the data are shown on the Smith Chart in the form of *load-pull contours*. These data are plotted for a specified large-signal performance metric, so each parameter (such as output power or PAE) has its own set of contours. The contours show how the behavior of the DUT changes with respect to impedance, and indicate the value of impedance required for optimal performance.

Load-pull data are most valuable when the measurements are collected at the desired operating conditions of the device. Biasing of the DUT is required, and the bias point for the device can be swept to measure the impact of reduced conduction angles on large-signal performance. The bias can be applied at any duty cycle, but the DC supply for the drain of a power device is often configured for pulsed operation with ~10% duty cycle. This technique mitigates the performance reduction and reliability issues that occur due to thermal degradation at high dissipated power levels. For depletion-mode devices (such as the GaN HEMTs discussed in this work), the bias voltage must first be applied at the gate,

and then at the drain, for safe operation. Therefore, pulse order and synchronization are critical for protecting the DUT from catastrophic damage during measurement.

In addition to configuring the bias, the drive conditions of the microwave signal must be defined. Load-pull contours are only valid for a particular frequency, so selection of the fundamental operating frequencies involves a tradeoff of measurement granularity and time. For each selected measurement frequency, the power level of the signal must also be chosen. Power amplifiers are almost always operated with some amount of gain compression to obtain higher output power and efficiency, so the source power of the microwave signal must be calibrated and controlled to enable load-pull measurements at the desired level of compression. The source power can also be swept during measurement to provide insight on how the amount of gain compression impacts the device performance.

Different configurations of laboratory equipment can be used to execute load-pull measurements, each with its own benefits and drawbacks. With this general understanding of the excitation conditions and impedance tuning requirements for load-pull measurements, the specific load-pull systems that were used for all large-signal measurements throughout this work can now be discussed.

2.1.2 Passive Load-pull Configuration with Power Sensor

This traditional load-pull method uses passive mechanical tuners to control the impedances at the DUT and a scalar power meter to determine the output power of the device. The diagram in Figure 5 identifies the main functional blocks of the measurement system [32], and the photo in Figure 6 depicts the laboratory equipment setup. A more

detailed description of the required hardware interconnections is provided in Appendix A.1.

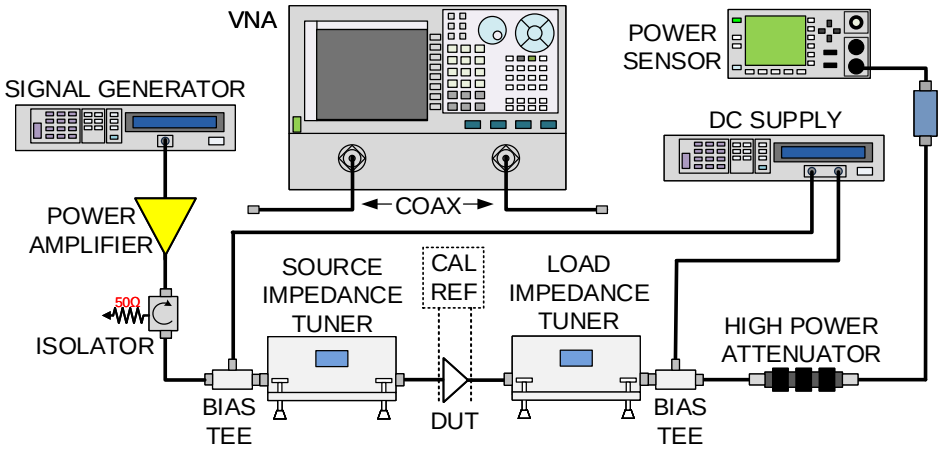


Figure 5 - Diagram of the power-sensor based passive load-pull system

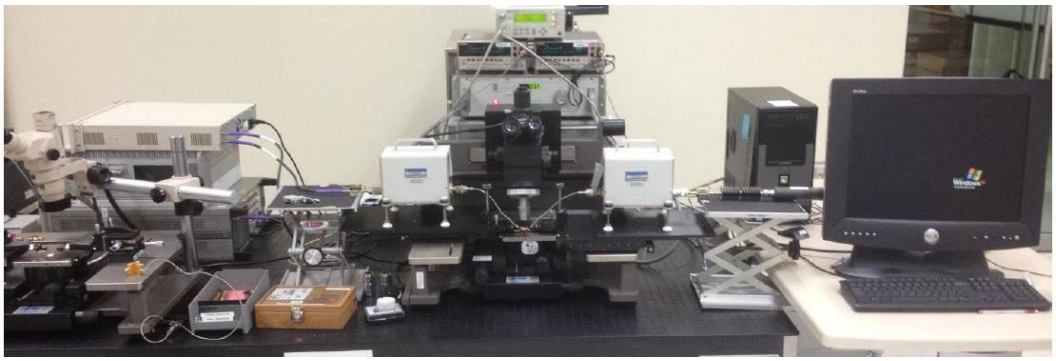


Figure 6 - Photograph of the laboratory equipment setup for the power-sensor based passive load-pull system

Biasing of the DUT is accomplished with external bias tees fed by DC supplies that are capable of sourcing the required currents at the required voltages. When the DUT is equipped with DC blocking capacitors, the external bias tees can be removed and bias can be applied directly to the DUT with wires or probes. After the laboratory equipment setup is finalized, the system is calibrated using the procedure described in Appendix A.2. Once

the calibration is complete, the vector network analyser (VNA) is no longer required for load-pull measurement.

2.1.3 Passive Load-pull Configuration with Vector-receiver

This upgraded passive load-pull method uses the same passive mechanical tuners and biasing setup as discussed in Section 2.1.2, but it also introduces directional couplers between the tuners and the DUT. The diagram in Figure 7 identifies the main functional blocks of the measurement system [32], and Figure 8 depicts the laboratory equipment setup. Directional couplers are connected to two receivers on the VNA, which enables direct measurement of the *a* and *b* waves at the input and output planes of the DUT. After the laboratory equipment setup is finalized, the system is calibrated using the procedure described in Appendix A.3.

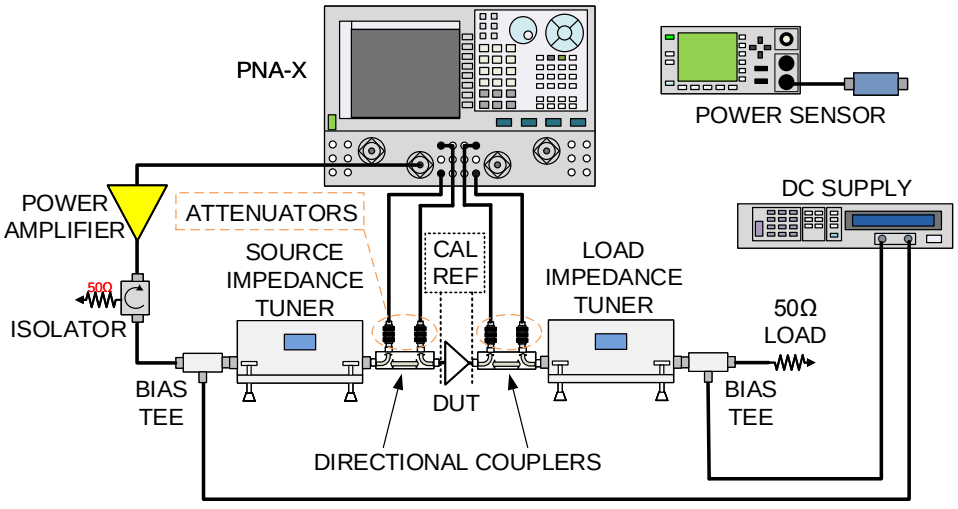


Figure 7 - Diagram of the vector-receiver based passive load-pull system

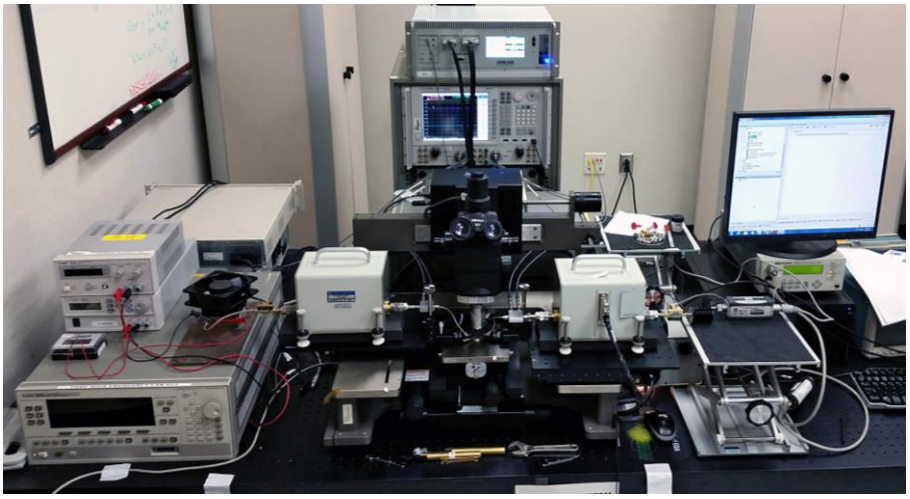


Figure 8 - Photograph of the laboratory equipment setup for the vector-receiver based passive load-pull system

While this load-pull configuration requires a network analyser during all measurements, it can accurately record both source power and input power at the DUT plane. Furthermore, the network analyser is frequency-selective, so the output power of the DUT can be accurately measured at a single frequency. These features represent significant improvements to the power-sensor based passive load-pull configuration, in which only the available source power is known, and the output power is measured simultaneously at all frequencies covered by the power sensor. Because of its input power measurement capability and frequency selectivity, the vector-receiver based passive load-pull configuration can provide a true measurement of PAE, which is a critical metric in nearly every microwave PA design.

2.1.4 Active Load-pull Configuration

Although passive mechanical tuners can handle high power and are less costly, there is no realistic way to overcome the losses introduced by the passive tuner itself and

the fixturing required to interface it with the DUT. In contrast to the passive load-pull configurations, no mechanical tuners are required in an active load-pull system. Instead, the active system uses high powered loop amplifiers to inject specific signals at the source and load. The diagram in Figure 9 identifies the main functional blocks of the measurement system [34], and Figure 10 depicts the laboratory equipment setup.

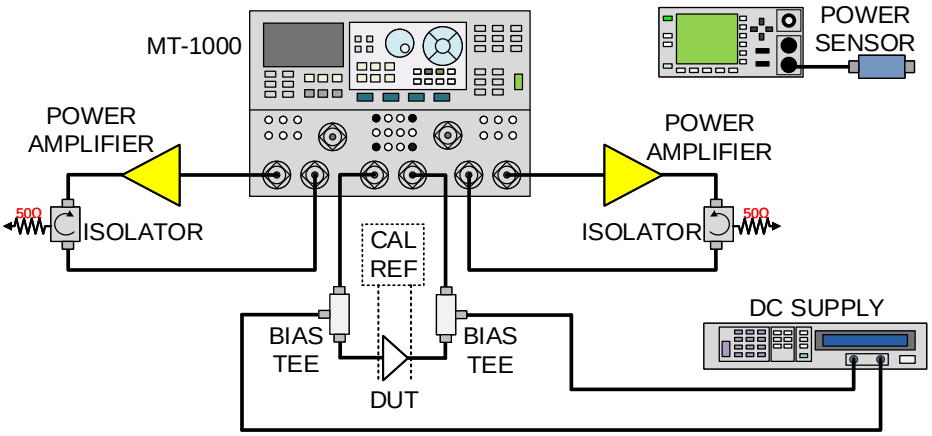


Figure 9 - Diagram of the MT-1000 active load-pull system

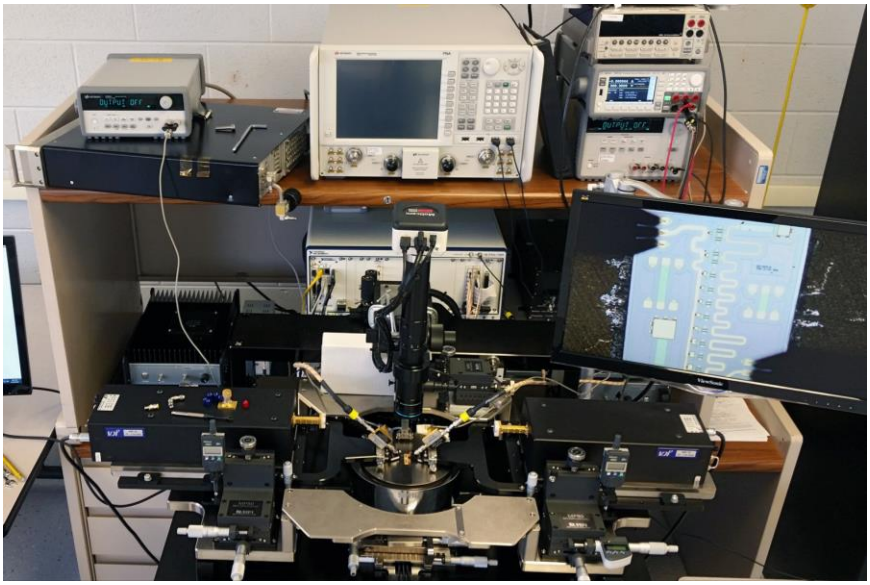


Figure 10 - Photograph of the laboratory equipment setup for MT-1000 active load-pull system

The active load-pull configuration achieves impedance tuning by using signal injection to manipulate the ratio between reflected signals and forward-traveling signals, thereby providing the desired impedance conditions at the DUT. After the laboratory equipment setup is finalized, the system is calibrated using the procedure described in Appendix A.4. While this type of load-pull configuration is very expensive, it provides the widest tuning range possible, flexible reconfiguration, and 100-fold reduction in measurement time.

The three load-pull system configurations discussed above – power-sensor, vector-receiver, and active – were available at various times for large-signal device characterization and PA performance verification measurements. All the large-signal measurement results presented throughout this dissertation were collected on one of these three measurement configurations. We will now examine how a load-pull system is used to verify the accuracy of a nonlinear device model for use in a PA circuit design.

2.2 Device Measurements

Many manufacturers of microwave power devices provide circuit designers with models to help predict the electrical performance of their transistors. These models are typically based on measurements of a unit cell, or a transistor with small active periphery. Microwave design software, such as Keysight ADS, can be used to access the models and determine optimal bias, impedance, and drive conditions to achieve the goals of the circuit. For any PA design, it is crucial to ensure that model simulations are consistent with measured data. Therefore, characterization of device samples and verification of device

models are essential to build confidence in the simulation results and increase the likelihood of a successful design. All of the work discussed in Chapter 3 and Chapter 4 used transistor models that were validated with both S-parameter and load-pull measurements. A 2x100 µm device fabricated on the NRC GaN150 process will now be used to provide details on device characterization measurements and present the creation of a non-linear device model.

2.2.1 Verification of Foundry PDK Models

Foundries often provide their device models in the context of a process development kit (PDK), which are developed for their specific semiconductor device fabrication process. An early version of a PDK for the NRC GaN150 process had been created for use in circuit design on that technology, and the kit included electrical models and layouts for standard passive and active components [35]. Prior to collecting any measurements, preliminary simulations were executed in ADS to provide insights on the operating conditions and expected behavior of the 2x100 µm device pictured in Figure 11. The NRC GaN150 HEMT nonlinear model was derived at V_{DS} = 20 V and V_{GS} = -3 V, which was considered the nominal starting point for investigation.

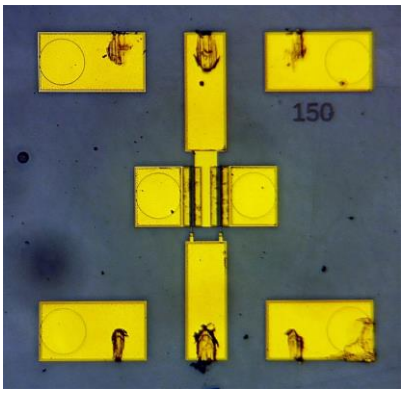


Figure 11 - Photograph of the NRC GaN150 2x100µm device used for characterization and modeling

The first measurement configuration consisted of a VNA with 150 µm pitch ground-signal-ground (GSG) probes, external bias tees, and 50 Ω coaxial cables. A short-open-load-thru (SOLT) calibration was completed to move the measurement plane to the probe tips. After the die was probed, a negative voltage of sufficient magnitude to put the device into a non-conductive region of operation was applied to the gate. Next, a small positive voltage was applied to the drain, and the current was monitored to ensure that a short circuit was not present. The drain voltage was then increased to the nominal starting point of 20 V, and the gate voltage was gradually increased until the channel began to conduct (as indicated by an increase in drain current). S-parameter measurements were then collected from 0.5-26.5 GHz for a swept range of gate voltages. The measurement setup was then recalibrated with on-wafer thru-line-reflect (TRL) standards, which moved the measurement plane to the gate and drain terminals of the device. This TRL calibration removed the effects of the probe pads and feed lines from the results, producing the most accurate measurement of device performance. The biasing procedure described above was

then repeated, and another set of S-parameter measurements were collected from 0.5-26.5 GHz for a swept range of gate voltages.

As expected, the measured data showed good agreement with the simulation results at a bias of V_{DS} = 20 V, V_{GS} = -3 V. Accurate results had been anticipated because the V_{DS} = 20 V, V_{GS} = -3 V bias condition had been specified as the nominal operating point for the NRC model. However, the model accuracy was impacted at other bias points, and the effects of interconnection parasitics were not fully captured in the model. As will be discussed in Section 4.1, the design goal with this GaN technology was to achieve wideband PA performance up to 18 GHz at a higher drain voltage. Therefore, this 2x100 µm transistor was chosen to undergo a more complete set of characterization measurements with the intention of using the collected data to generate a new electrical model for the device.

2.2.2 Device Characterization Measurements

A complete on-wafer characterization of a microwave transistor involves DC-IV, small-signal, large-signal, and noise parameter measurements over a range of operating temperatures [36]. Because this device will be used in a PA design at a specific bias point and tested at room temperature, a selected subset of the complete characterization measurements produced sufficient data to construct an accurate electrical model for use under these operating conditions. Specifically, noise figure was not measured, and the remaining measurements were collected at room temperature only.

Using the TRL calibration method and biasing sequence described above, the S-parameters of the 2x100 µm device were measured at CW from 0.5-26.5 GHz, over a swept DC bias of V_{GS} = -5 V : 0.1 V : -2 V and V_{DS} = 0 V : 1 V : 40 V. The DC-IV and small-signal measurement sequence was then repeated for pulsed bias duty cycles of 50% and 5% (100 µs period), from multiple quiescent bias conditions, with V_{GS} = -5 V : 0.1 V : -1 V and V_{DS} = 0 V : 1 V : 50 V. Finally, large-signal data were collected using the vector-receiver load-pull configuration described in Section 2.1.3. The measurement results were used to extract optimal P_{OUT} and PAE contours at 6, 12, and 18 GHz for a range of Class-AB bias points to complete the device characterization.

2.3 Modeling

Since the existing transistor model was optimized for a different bias point, the data collected during characterization measurements were used to extract a new transistor model for operation with a 28 V drain supply [37]. While there are many different modeling techniques, the three most common types in use today are physical, behavioral, and compact. Physical models are based on the underlying physics of the specific device technology. While they are valid over the largest operating range, physical models use complex equations which require longer simulation time, so this type of model is more suited for the transistor itself and not the full microwave circuit. Behavioral models are based on the measured responses of a component to a controlled input signal. Although development is easier for any component type (on-wafer, packaged, etc.), behavioral models are only applicable for the measured operating conditions, so this type of model

has reduced flexibility. Compact models are based on measurements of DC-IV and S-parameters which are then used to converge a formula-based transistor model with a reduced set of circuit parameters. The valid operating range of a compact model is somewhat reduced when compared with a physical model, and the modeling process is more involved when compared with a behavioral model (particularly for a packaged device). However, a compact model requires relatively straightforward measurements, needs less simulation time, and captures complex phenomena over a useful range of operating conditions. The compact model is an excellent choice when developing a model of a microwave transistor die for use in circuit design, so this technique was selected to create the electrical model for the NRC GaN150 2x100 μm device.

2.3.1 Nonlinear Device Model Creation

To extract the compact model, pulsed S-parameter and quasi-isothermal pulsed DC-IV data were collected for an on-wafer sample of the NRC GaN150 2x100 μm transistor. Load-pull measurements at 6, 12, and 18 GHz were also performed on the same device for model validation. Measurement system control and compact model extraction were accomplished with IVCAD software from Maury Microwave.

After the device measurements in Section 2.2.2 were completed, the modeling process began with the extraction of a linear model. The extrinsic parasitic elements R_g, L_g, C_{pg}, R_d, L_d, C_{pd}, R_s, and L_s, as defined in the compact model schematic in Figure 12, were determined by parameter optimization using the collected S-parameter data [38]. These extrinsic parameter values were selected such that the values of the intrinsic parameters C_{gs}, C_{gd}, G_m, G_d, C_{ds}, R_i, T_{au}, and R_{gd} were constant with respect to frequency.

During this procedure, the measured and modeled S-parameters were constantly compared to ensure agreement over the bandwidth of interest.

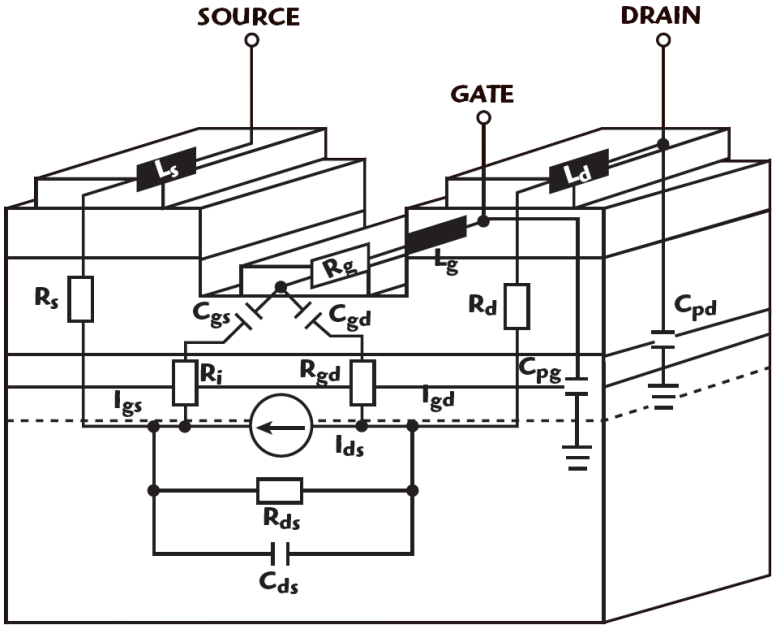


Figure 12 - Schematic of the compact transistor model used for the NRC GaN150 2x100 µm device

The modeling process was continued by using both continuous and pulsed DC-IV data to extract a nonlinear model. These measurements were required to determine the thermal impedance of the device, which enabled the compact model to predict the response of the device as a function of self-heating and baseplate temperature. The duty cycle of the pulsed measurements was configured to minimize the mean variation of device temperature, and the pulse width was configured to avoid temperature variations for the duration of the pulse.

To complete the modeling process, one-dimensional nonlinear capacitance models for C_{gd} and C_{gs} were extracted from the pulsed DC-IV and pulsed S-parameter

measurements. The value of C_{gd} heavily depends on the drain voltage, while the value of C_{gs} heavily depends on the gate voltage along the same RF load line [38]. Since C_{ds} exhibits only a weak voltage dependence in amplifier designs, it is treated as a linear element. Finally, the extracted compact model was simulated in ADS and compared with the measured data. The small-signal plots in Figure 13 and large signal load-pull contours in Figure 14 were used to validate the new model for design use.

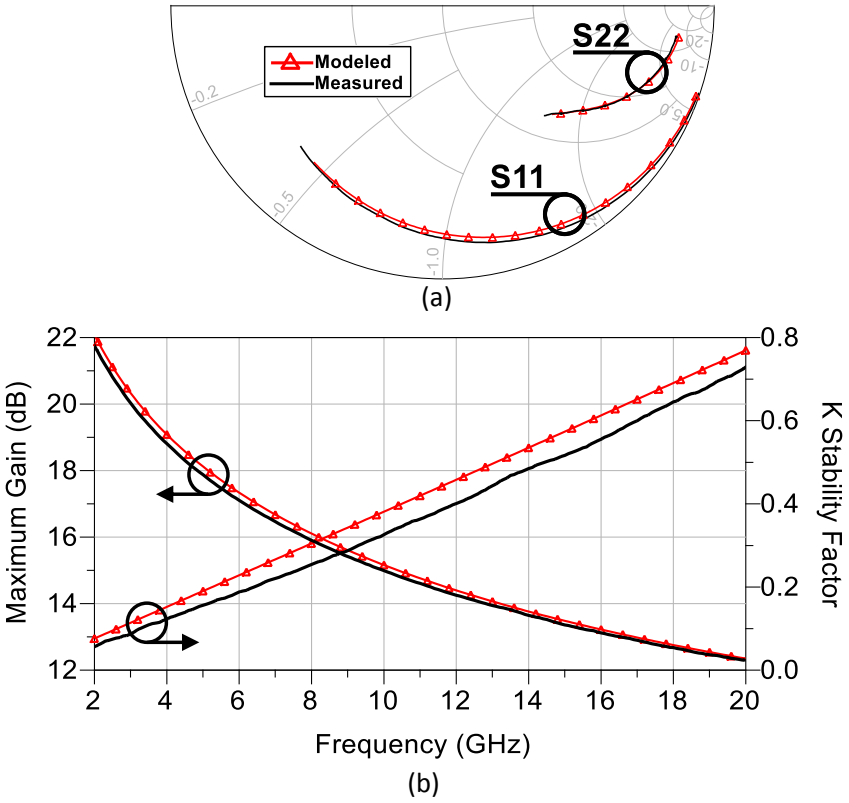


Figure 13 - Measured and modeled S-parameters comparing (a) S11 and S22, and (b) max gain and stability factor for a NRC GaN150 2x100 µm device at V_{DS} = 28 V

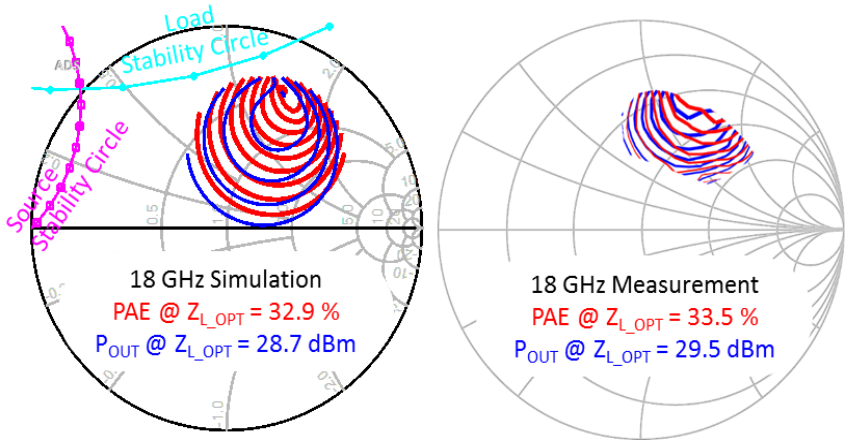


Figure 14 - Nonlinear model simulation and large signal measurement comparison for a 2x100 µm device at V_{DS} = 28 V, P_{IN} = 22 dBm, and *f* = 18 GHz

Load-pull results are provided at 18 GHz, the highest frequency at which the impedance tuners could function. The comparison plots show highly-correlated measurement and simulation results, indicating the efficacy of the newly extracted model. With the concepts and methods of large signal device characterization and modeling introduced, it is now possible to begin a power amplifier design. In the upcoming chapter, the manufacturer's device models will be applied in the development of several hybrid PA circuits. Then, in Chapter 4, the new model extracted above for the NRC GaN150 2x100 µm device will be used in the design of an MMIC PA.

CHAPTER 3:

HYBRID MICROWAVE GAN POWER AMPLIFIERS

By using large signal models from discrete device manufacturers, we can now focus on achieving cutting-edge performance from commercial power transistors in hybrid PAs. For a typical hybrid PA implementation, passive microwave circuits are fabricated on planar dielectric substrates, and active microwave components – in this case, GaN HEMTs – are bonded onto this passive structure. Hybrid PAs can enable faster design cycles, shorter production cycles, lower costs (for small quantities), and more flexible integration.

The first design presented in this chapter used multiple discrete GaN transistors with power-combining networks implemented on a low-loss substrate to achieve maximum efficiency and high output power at X band. The findings of this design were published in IEEE's International Conference on Microwaves, Communications, Antennas and Electronic Systems [39].

3.1 Hybrid Power Combining of Commercial Power Transistors

This hybrid configuration contained two commercially available TGF2023-01 GaN HEMT dies in parallel. The multi-die topology helped manage thermal constraints while increasing the total output power [22] by expanding the total circuit area and doubling the effective HEMT periphery, respectively. An overview of the PA architecture in Figure 15 shows the interconnections of the Wilkinson combiners, input matching networks, output matching networks, GaN devices, and wirebonds.

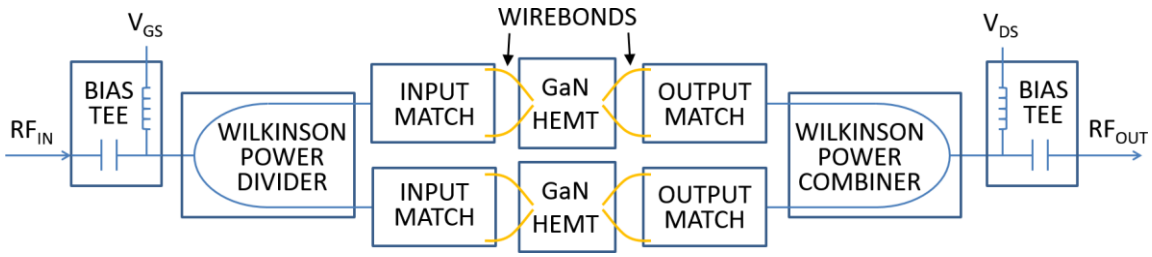


Figure 15 - Block diagram of hybrid multi-die PA architecture

Several characteristics of ideal microwave circuit substrates [40] – such as low dielectric loss and high dielectric strength – are particularly desirable for PAs, and a high thermal conductivity is essential to achieving good system efficiency in a high-power design [41]. With its thermal conductivity of 170 W/m·K, AlN can more quickly sink the excess heat generated by PA circuitry than many other substrate materials [42]. Given its excellent physical properties [42], 15 mil AlN was chosen as the substrate with 4.5 µm Au as the conductor for the power divider network designs, as shown in Figure 16.

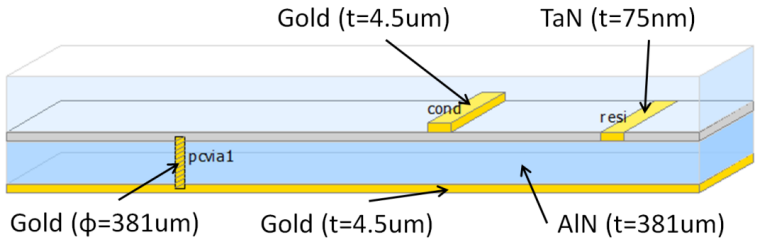


Figure 16 - Material stack-up for EM simulation of the power divider networks

3.1.1 Low-loss Wilkinson Power Dividers

To divide and recombine the power for the two dies, an equal-split Wilkinson divider [43] was designed and optimized in ADS. Thin-film TaN was used for the isolation resistors, and the final EM-simulated design had less than 0.1 dB insertion loss, over 20 dB isolation, and over 20 dB return loss as shown in Figure 17.

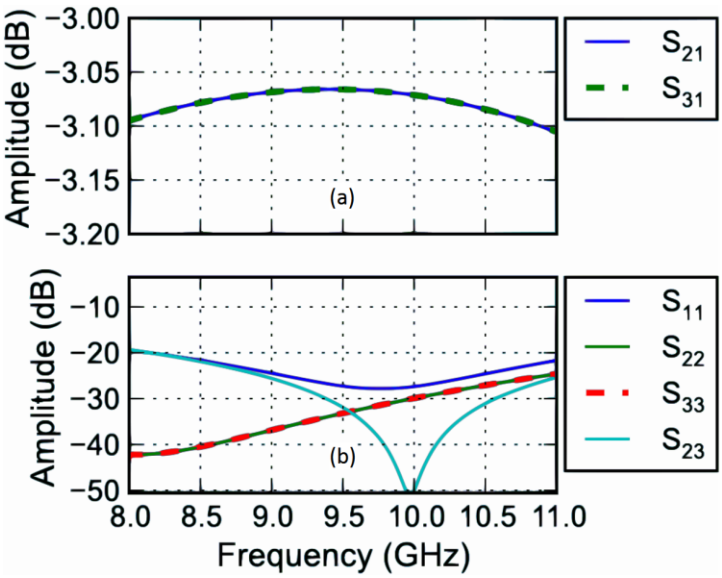


Figure 17 - EM-simulated (a) insertion loss and (b) isolation and return loss for the equal-split Wilkinson power divider design

3.1.2 Matching Network Design

To maximize output power and PAE, the 50 Ω impedance of the Wilkinson dividers must be transformed to present optimal large-signal impedances to the TGF2023-01 power transistor. Iterative load-pull and source-pull simulations were performed in ADS to determine the optimal impedances, and the passive power-sensor based load-pull configuration described in Section 2.1.2 was used to measure the TGF2023-01. The simulated optimal impedance values were then compared with measured data in Table 1. All simulations and measurements presented in Table 1 were performed at I_{DS} = 70 mA and V_{DS} = 28 V, with optimal impedance extractions at 10 GHz for a source power of 24 dBm at the GaN die.

Good agreement was observed for the optimal load impedances, as indicated by the load values in Table 1 and the load-pull contours in Figure 18. Because the impedance

tuning range of the measurement system was limited, the measured optimal source resistance seemed somewhat different than the simulated result. Since the tuner and fixture losses prevented the realization of any impedance with a $|\Gamma| > 0.8$ at 10 GHz, source-pull measurements could not be collected for source impedances near the edge of the Smith Chart. Although measurements taken at the edge of the Smith Chart are desirable, they are not required to verify the model in this case. The simulated contours in Figure 18(a) are very similar in shape and size to the measured contours in Figure 18(b), and the maximum P_{OUT} and PAE of the device are also in good agreement after correcting for the limited source impedance tuning range. Taken together, these data confirm the model's validity for use in circuit design.

Table 1 - Simulated and measured optimal large-signal impedances and device performance of the TGF2023-01 die at 10 GHz

Parameter	Simulated	Measured
$Z_{SOURCE,\ OPTIMAL}$	2.3 - j9.5 Ω	7.48 - j7.37 Ω
$Z_{LOAD,\ OPTIMAL\ (POUT)}$	15.6 + j11.0 Ω	13.47 + j12.79 Ω
$Z_{LOAD,\ OPTIMAL\ (PAE)}$	11.64 + j15.8 Ω	10.04 + j15.41 Ω
$P_{OUT,\ MAXIMUM}$	36.5 dBm	34.75 dBm
$PAE_{MAXIMUM}$	62%	52%

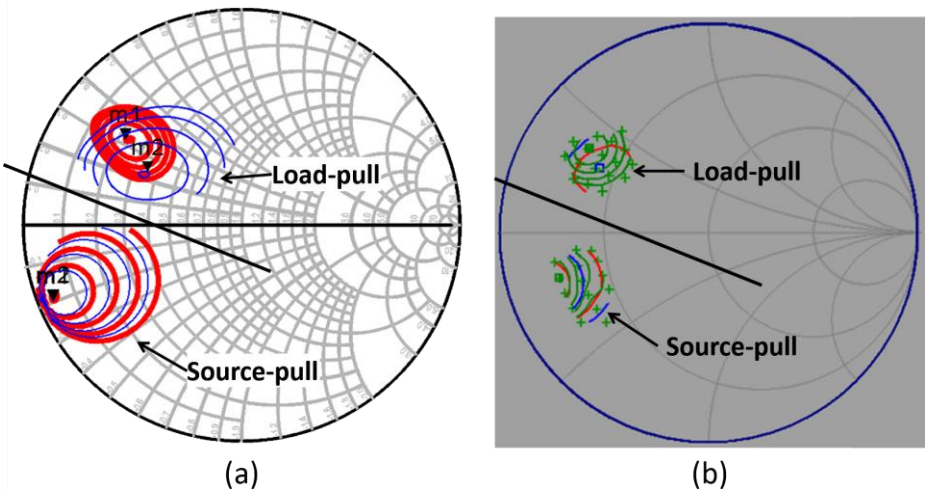


Figure 18 - (a) Simulated and (b) measured load-pull and source-pull contours for POUT and PAE

With these optimal impedances determined, the input and output matching networks were designed on the AlN substrate using double radial stubs and microstrip transmission lines. In HMICs, parasitics from interconnections (e.g., wirebonds, via holes) often limit the achievable performance. Circuit optimizations showed that a specific wirebond length at the gate would enable a better large-signal impedance match. However, the minimum realizable wirebond length was constrained by the height difference between the AlN substrate and GaN dies. Therefore, the metal carrier in Figure 19 was designed to include an integrated pedestal upon which the GaN dies would be mounted. The pedestal's dimensions were cut so that the bondpads of the mounted die would align in the z-direction with the patterned metal layer of the mounted matching networks. This carrier helped to reduce the minimum realizable wirebond length and provided an excellent heat sink for the dissipated power from the dies.

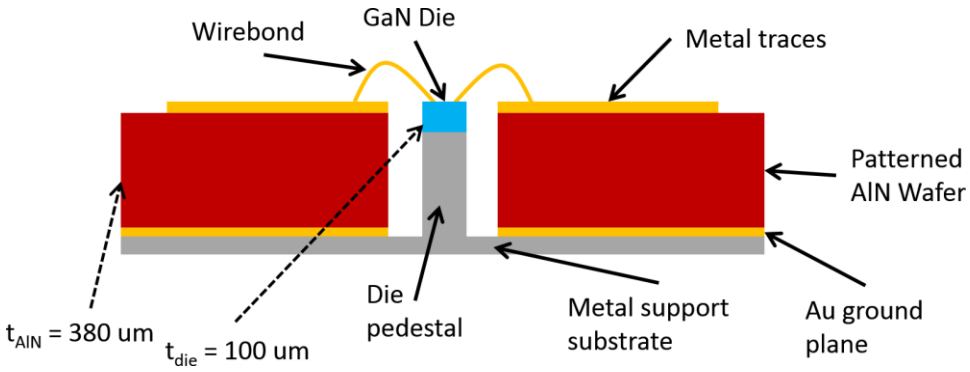


Figure 19 - Diagram of hybrid PA module assembly using metal carrier with integrated die pedestal

After optimization of the schematic level design, EM simulations were executed in Momentum on the full network layouts. These layouts were tuned until the EM simulation results were close to the schematic simulation results, at which time the mask was finalized and submitted for thin-film fabrication. After the completed wafers were diced, the microwave structures were ready for assembly into a hybrid X band PA.

3.1.3 Assembly and Measurements

The first step in PA assembly was affixing the GaN dies to the carrier. An 80% Au 20% Sn eutectic preform was used to attach the dies to the Au-plated pedestal on the metal carrier. Although this method of die attach required high heat, it provided the transistor with the lowest possible thermal resistance. Next, the input and output matching networks were affixed to the carrier with silver epoxy, providing a good thermal pathway to ground. Because silver epoxy is viscous until cured, choosing this material enabled precise alignment of the matching networks with the die bondpads in both x- and y-dimensions.

Lastly, 1-mil gold wires were wedge-bonded from the dies to the networks as shown in Figure 20 to complete assembly.

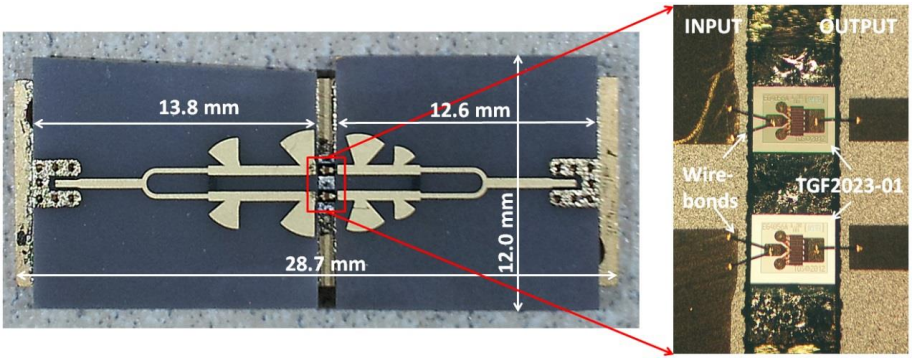


Figure 20 - Photograph of the fabricated and assembled PA with inset showing gold wirebonds

The fabricated and assembled circuit seen in Figure 20 was probed, biased, and tested for small-signal and large-signal performance. Plots of the small-signal reflection coefficients and linear gain for a -10 dBm input signal are found in Figure 21, which also shows traces for three different wirebond configurations for the input matching network to gate interconnection – double, single, and long. Initial PA measurements indicated an upwards frequency shift which was due to mechanical positioning limitations. The assembled circuit had the matching networks physically closer to the dies, which decreased the length (and, therefore, inductance) of the wirebonds. Since the desired large-signal performance can be partially targeted by tracking the small-signal input match, the frequency response was tuned with different configurations of IMN-to-gate wirebonds to achieve a peak output power of 38.1 dBm at 9.5 GHz.

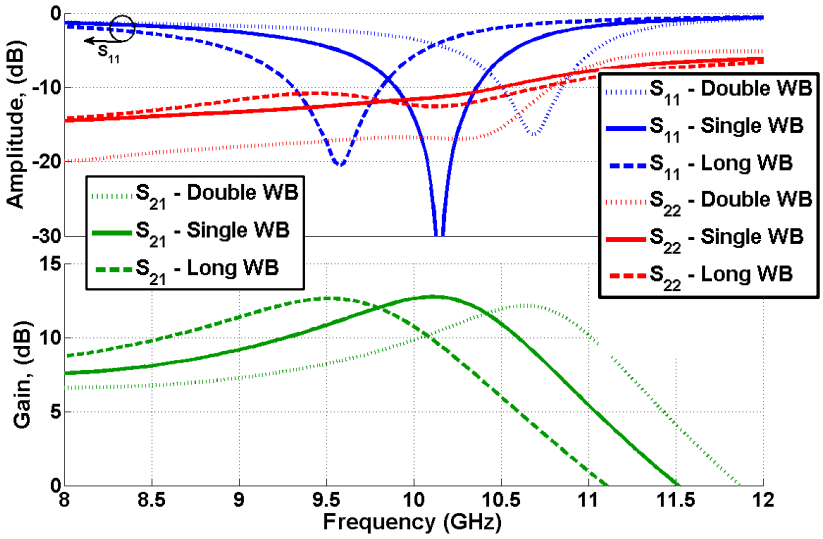


Figure 21 - Simulated and measured small-signal results

The large-signal measurements at 27 dBm source power are compared with simulations in Figure 22. The source power was then swept (up to the available maximum) at the peak power frequency, and Figure 23 shows both the simulated and measured performance. This design effectively mitigated thermal effects with its parallel-die configuration, AlN substrate, and use of WPDs. Although thermal degradation can be difficult to capture in simulation, pulsed modes of operation (unavailable at the time of measurement) would help to identify and address any thermal limitations.

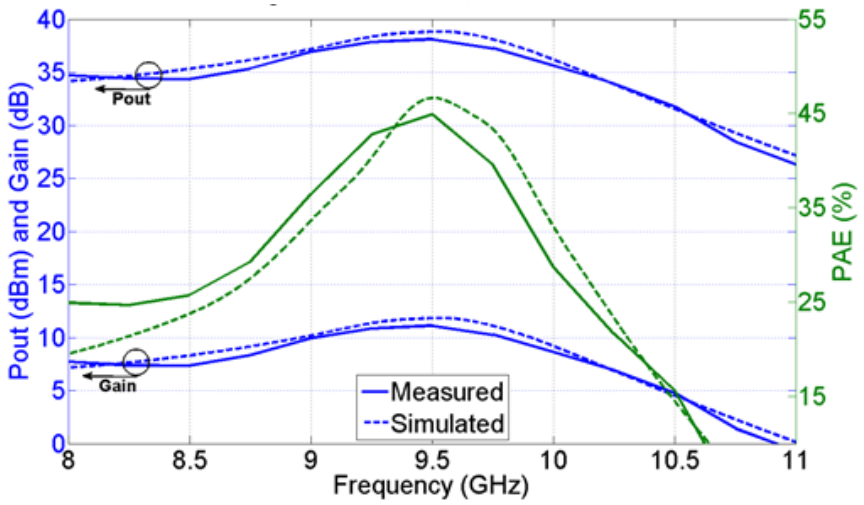


Figure 22 - Simulated and measured POUT, gain, and PAE vs. frequency results

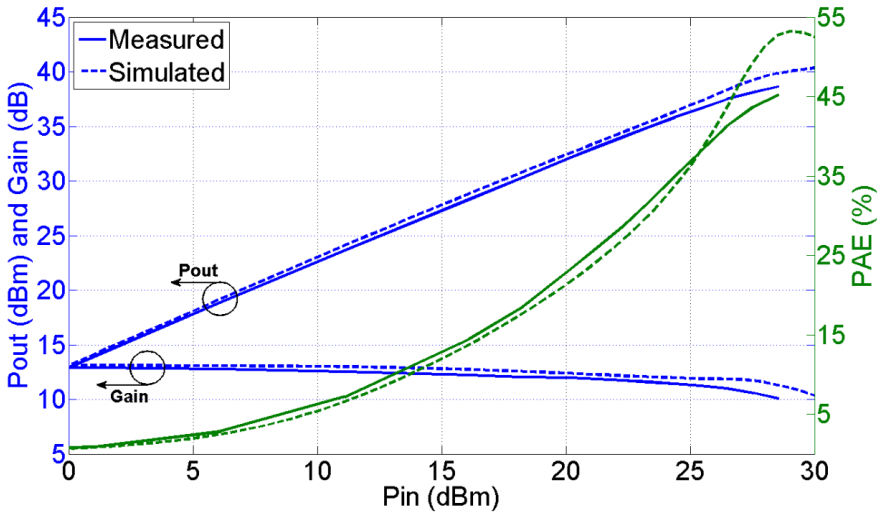


Figure 23 - Simulated and measured POUT, gain, and PAE vs. PIN at 9.5 GHz

Due to the hybrid approach, variations in wirebond topology and length enabled tuning of the operation frequency, which was captured in the small-signal response of the PA. A measured 38.1 dBm (6.5 W) output power and maximum PAE of 44% at 9.5 GHz is shown in Figure 23, corresponding to a 3.25 W/mm output power density. Although the PAE was relatively high and thermal effects were well mitigated, the bandwidth of this

Wilkinson-combined, reactively-matched PA was limited. To achieve a wider bandwidth in a hybrid implementation, the next PA employs the traveling wave technique.

3.2 Hybrid Broadband PA Implementation Using the Traveling Wave Technique

This portion focuses on achieving ultra-wideband performance from a hybrid distributed power amplifier (DPA) using discrete GaN devices. These efforts produced a 3-cell traveling wave design with state-of-the-art output power and PAE over the widest bandwidth for a hybrid DPA in GaN technology. The findings of this study were presented in IEEE's European Microwave Integrated Circuits conference [44].

3.2.1 Amplifier Topology and Design

The traveling-wave amplifier consists of three discrete 0.25 µm GaN HEMTs (CGHV1J006D), each with a saturated output power of 6 W at 10 GHz. ATLs were created along the gates and drains of these devices, as indicated in the DPA topology shown in Figure 24. The ATLs are shaped to absorb the input and output capacitances of the HEMTs into the interconnecting transmission line segments [16].

The chosen topology differs from a classical approach in several aspects. Firstly, while the gate ATL is terminated with a resistance, the drain termination was avoided to prevent significant losses in P_{OUT} and PAE. Instead, reducing the drain line Z_0 limited the backwards-traveling waves. Secondly, since discrete device periphery choices are limited, the gate line geometry was varied instead – in parallel with drain line optimization – to allow better P_{OUT} and PAE by improving the power distribution to the devices. Lastly,

capacitive coupling was used at the gates to reduce the effective capacitance absorbed into the gate ATL. The input capacitance of the devices would have limited the gate ATL cut-off frequency, so a series capacitor was included on each gate to trade lower gain for wider bandwidth. However, this trade-off has a diminished appeal if the capacitor sacrifices too much gain in the pursuit of greater bandwidth, as P_{OUT} and PAE will be reduced.

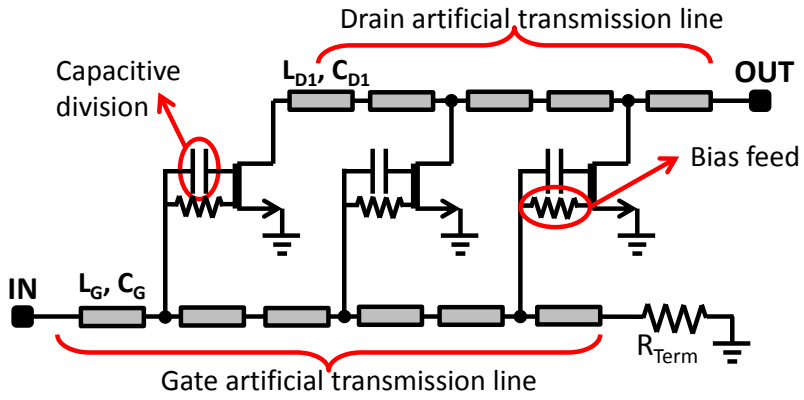


Figure 24 - Wideband distributed power amplifier schematic

Resistors in parallel with the series gate capacitors provided a bias path and assisted in achieving unconditional stability. In addition, the characteristic impedances of the drain and gate ATLs were chosen to be 25 Ω in order to present a more optimal impedance for maximum power and PAE at each die interface. The drain line impedance was gradually lowered towards the output to further improve the impedances seen by each die, while the gate line geometry was optimized in parallel for best performance. Tapered input and output connections were included for broadband 25 Ω to 50 Ω impedance transformation.

Choosing the right packaging for the GaN HEMTs is critical, as it is challenging to absorb the capacitance into a wideband ATL. The addition of a large wirebond inductance

to the already large device capacitance would have been severely detrimental to broadband performance. Thus, flip-chip bonds were selected for die interconnections to minimize parasitic inductance. AlN (15 mil) was chosen as the substrate to help with thermal management, as the flip-chip method only provided the Au bumps for a thermal sink (rather than the backside source contact). Finally, coplanar waveguide to microstrip transmission line transitions were included in the layout to enable probed measurements of the PA.

3.2.2 Assembly and Measurements

The fabricated and assembled PA, along with a zoomed-in view of the core components and their values, are shown in Figure 25. The first step in assembly was to flip-chip the three GaN dies onto the fabricated thin-film circuit. Next, silver epoxy was used in successive stages to attach the input resistors, capacitors, termination resistors, and DC blocking capacitors to the circuit board. Once the final round of epoxy was cured, the PA was ready for measurements.

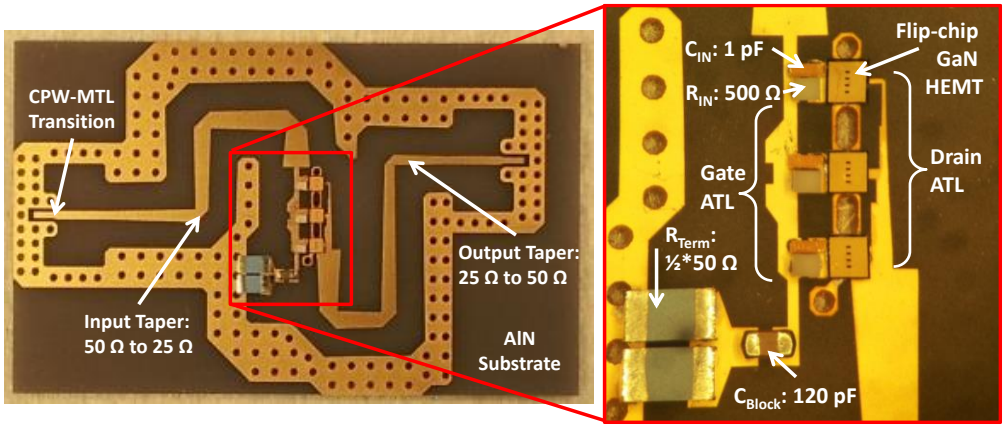


Figure 25 - Fabricated hybrid distributed power amplifier with assembly detail

The HEMTs were biased through probes and external bias tees for class AB operation, with V_{GS} = -2.3 V and V_{DS} = 35 V. The DPA was characterized under pulsed operation (10% duty cycle with 100 µs period), and Figure 26 shows the measured small-signal data. The PA was unconditionally stable, and it provided a small-signal gain of 9-14 dB from 0.4-8 GHz. The measured results were in good agreement with the simulations, except for a slight bandwidth reduction which was caused by the use of uniform gate capacitor values due to component availability. Although non-uniform gate capacitor values were originally specified in the design, the component manufacturer had difficulties sourcing them. Only one capacitor value was used at all three transistor gates, so the measured bandwidth was slightly lower than in simulation. There was also an unexpected degradation of input matching around 4 GHz, which was associated with the non-ideal gate line termination and parasitics of the surface mount devices.

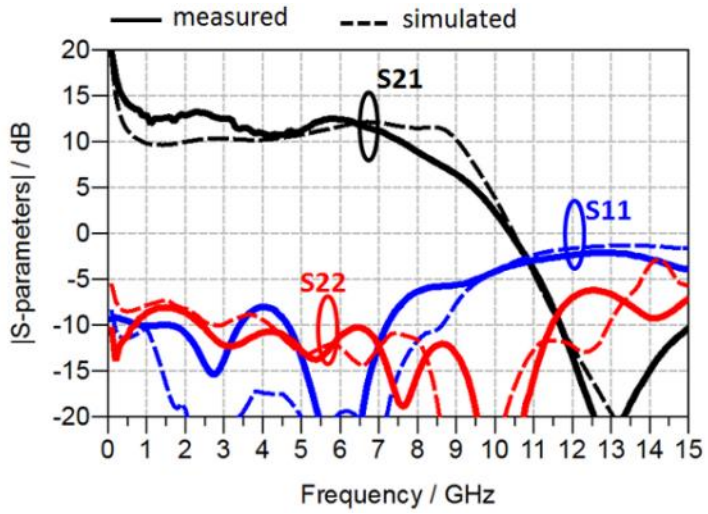


Figure 26 - Measured S-parameters under 10% duty cycle pulsed operation

For large-signal measurements, fixture losses were extracted and power levels were calibrated to the probe tip plane. The measurement plots in Figure 27 show that the amplifier reached 41 dBm P_{OUT} with 37% PAE at 5.5 GHz with 31 dBm (max available source power), and the measured response for swept input power is found in Figure 28.

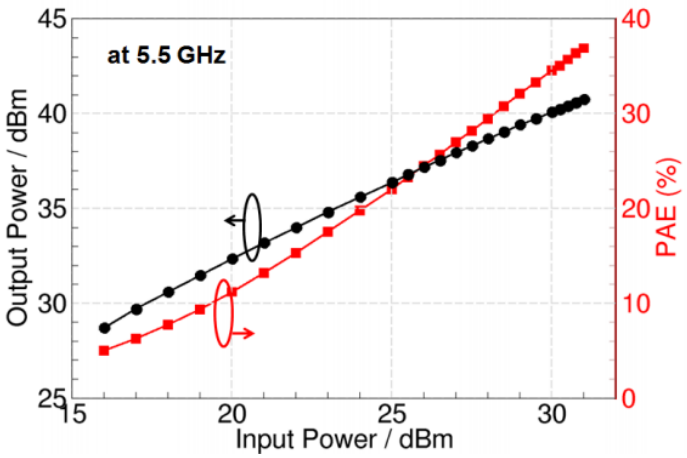


Figure 27 - Measured P_{OUT} and PAE at 5.5 GHz (10% duty cycle pulsed operation)

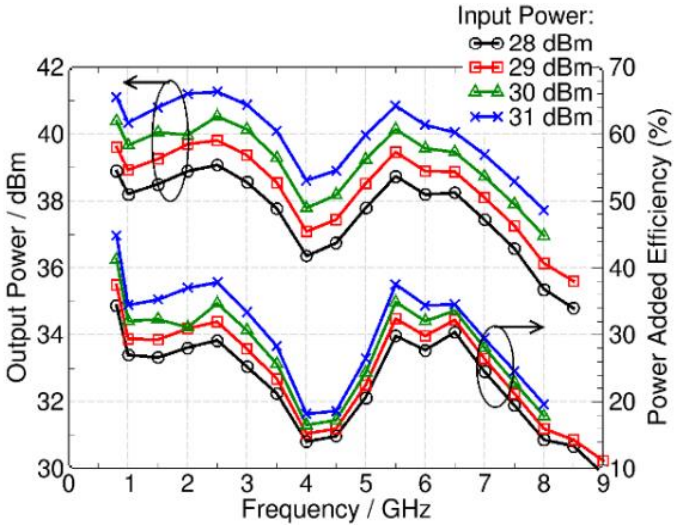


Figure 28 - Measured P_{OUT} and PAE from 1 to 9 GHz (pulsed with 10% duty cycle)

Excluding the reduced efficiency around 4 GHz, the amplifier provided more than 38 dBm output power and 20-30% PAE up to 8 GHz. The efficiency drop at 4 GHz was related to the previously-discussed matching degradation. With this performance, the presented traveling-wave PA achieved significant output power with high PAE and provided the widest bandwidth for a hybrid design, surpassing previously reported hybrid DPA results. Although a traveling-wave architecture can provide a very broad bandwidth, it is difficult to achieve the highest PAE using this technique. The final section of this chapter will now discuss another broadband hybrid PA design, but will emphasize the use of reactive/resistive matching to improve efficiency.

3.3 Ultra-wideband Hybrid PA with Reactive / Resistive Matching on Disparate Substrates

Continuing with broadband HMIC PAs, this study details the design of an ultra-wideband PA using a single discrete GaN transistor in a hybrid topology with multiple substrates. Targeting multi-watt output power and decade-plus bandwidth, the goal of this effort was to maximize PAE using the reactive/resistive matching technique. The findings of this work were published in IEEE's Microwave and Wireless Components Letters [45].

3.3.1 Amplifier Topology and Design

In the topology shown in Figure 29, a series RC network at the gate provided both stability and a bias path for a single Cree CGHV1J006D HEMT die. Appearing in series with the transistor's input capacitance, the series capacitor C_{SE} helped to extend the

bandwidth through capacitive division at the gate. A shunt resistor R_{SH} – connected to the input matching network with ribbonbond RB_{SH} – helped provide low frequency stability.

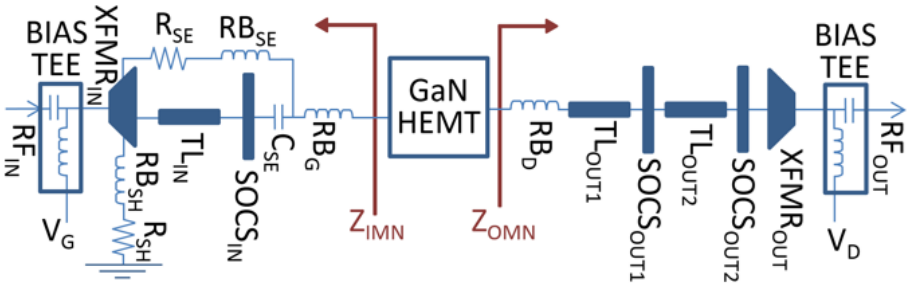


Figure 29 - Hybrid UWBPA schematic

To evaluate its large-signal performance, the transistor was first terminated with a conjugate match, and then iterations of load-pull and source-pull simulations were performed over a range of class AB bias conditions. The bias point and stabilization network values were chosen by optimizing the trade-off between bandwidth and unconditional stability. A drawback of the originally-proposed substrate was its limitation on maximum and minimum realizable characteristic impedance Z_0 for microstrip transmission lines. Lower impedance values were desired for the input matching network because of the low optimal input impedance of the GaN die, while simulations predicted the need for higher values in the output matching network. This was where the hybrid approach enabled the use of two different substrates for the input and output matching networks to optimize the ranges of available Z_0. Based on EM-simulated realizable Z_0 ranges, 10 mil RO3010 was selected for the IMN, and 30 mil RO3003 was chosen for the output matching network. The final values and design details are found in Table 2 for the named components in Figure 29.

Table 2 - Final hybrid UWBPA design parameters

Name	Parameter	Length (µm)	Width (µm)	Width (µm)	Notes
$XFMR_{IN}$	Impedance transformer	25000	207	1390	RO3010
TL_{IN}	Microstrip transmission line	150	1250	-	RO3010
$SOCS_{IN}$	Symmetric open circuit stubs	75	4990	-	RO3010
R_{SH}	Shunt resistor (SMD)	1520	750	-	100 Ω x 2
R_{SE}	Series resistor (SMD)	480	390	-	180 Ω
C_{SE}	Series single layer capacitor	635	635	-	1.5 pF
TL_{OUT1}	Microstrip transmission line	815	300	-	RO3003
$SOCS_{OUT1}$	Symmetric open circuit stubs	75	8450	-	RO3003
TL_{OUT2}	Microstrip transmission line	250	496	-	RO3003
$SOCS_{OUT2}$	Symmetric open circuit stubs	215	5510	-	RO3003
$XFMR_{OUT}$	Impedance transformer	24500	2970	1900	RO3003
RB_{SH}	Ribbonbond for shunt resistor	~ 4000	76	13	-
RB_{SE}	Ribbonbond for series resistor	~ 5500	76	13	-
RB_{G}	Gate ribbonbonds	~ 300	76	13	x 2
RB_{D}	Drain ribbonbonds	~ 300	76	13	x 2

The input matching network was comprised of a symmetric pair of open stubs and an impedance transformer. The 3.6 : 1 transformation ratio for a 50 Ω input match was quite high, and required large dimensions for the tapered line to remain resistive at lower frequencies. Thus, the input taper length was a tradeoff of increased lower-band reactance for reduced higher-band loss. Moreover, the bandwidth can be extended to higher frequencies by designing some mismatch into the input network at lower frequencies, where the transistor has extra gain. For broadband performance, the input return loss was optimized to gradually improve as the operating frequency increased. This gain compensation technique results in poorer return loss at the lower frequencies, but for a

given source power, it provides gain flatness across the entire band [16]. Since a low return loss may not be suitable for all systems, the use of a balanced architecture with Lange couplers and two identical PAs would significantly improve the return loss and nearly double the output power.

Similarly, the output matching network consisted of two symmetric pairs of open stubs, and two short sections of high impedance transmission lines. A transformer was then placed to deliver a wideband 50 Ω match. The output network substrate and 1.4 : 1 transformation ratio allowed for lower loss and smaller size, enabling the taper to remain resistive down to 1 GHz. To obtain the best PAE, it was critical to maintain an optimal large-signal output match across the entire operating band. Therefore, minimal gain compensation was designed into the output matching network.

Integration losses were kept to a minimum by optimizing the length and number of ribbonbonds, thus limiting their parasitic impact on the amplifier's performance. Geometric tolerances were estimated for the die pads, die placement, pedestal, and metal pullback, resulting in expected bond lengths ranging from 185-315 µm. Prior to beginning the PA design, different configurations of 3 x 0.5 mil bonds with 200-350 µm lengths in 50 µm steps were fabricated and measured. The collected data for the 250 µm long double ribbonbonds were imported into ADS for PA optimizations, and the final simulated input and output matching network impedances (including double ribbonbonds) are also found in Table 2. Masks of the finalized design layouts were purchased, and in-house fabrication of the matching networks was begun.

3.3.2 Fabrication and Assembly

The tools listed in Table 3 were used at the Georgia Tech IEN Cleanroom facility to create the passive planar microwave structures with photolithographic processing techniques. First, drilling of the vias was completed on a circuit board mill. Optimization of the entry/exit layer materials and drilling parameters helped to minimize any raised edges, but some of the copper surrounding the vias was deplanarized by the mechanical drilling process. Therefore, after all remaining processing steps were completed, the vias were filled with silver epoxy to ensure good conductivity. Once the metal surface was cleaned in the reactive ion etcher, Ti/Au was evaporated on the topside of the wafers to enable an Au wirebond connection from the matching networks to the GaN dies.

Table 3 - Facilities and tools used for microwave circuit fabrication and assembly

Fabrication	Fixturing	Assembly
GT Cleanroom	GTRI Machine Shop	MiRCTECH Lab
- Reactive Ion Etcher	- CuW Stock	- AuSn Preforms
- Spin Coater	- Cu-101 Stock	- Hotplate
- Mask Aligner	- Wire-cut EDM	- Wirebonder
- Evaporator	GT Cleanroom	- Au Wire & Ribbon
- Sputterer	- Electroplating Equipment	- Silver Epoxy
- Etching Station		GT Cleanroom
- Profilometer		- Forming Gas
- Dicing Saw		- Die Manipulator

The processing continued with the application of photoresist, mask aligning, UV exposure, developing, and finally metal etching. Several different chemicals were required

because of the Au/Ti/Cu metal stackup. Once the etch was complete, the wafer was diced with the dicing saw. Careful alignment was important because some of the fabricated samples were diced within 1 mil of the input networks' stubs to minimize bond lengths. Once diced, the networks were rinsed, dried, and prepared for attachment to the carrier.

Circuit planarity, also important in reducing parasitics, was achieved by varying the metal carrier thickness as shown in Figure 30. The varied carrier thickness was used to compensate for the differences among die, lumped component, and substrate heights. The transistor was then bonded to the integrated pedestal with an AuSn eutectic preform, while the input and output matching networks were silver epoxied to the carrier. The fully assembled amplifier is shown in Figure 31.

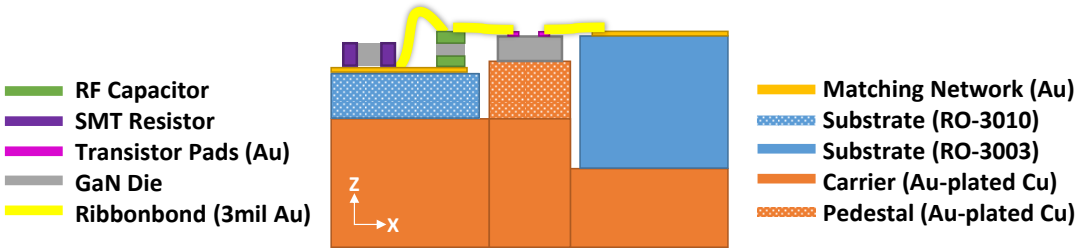


Figure 30 - Assembly diagram showing multi-level carrier with integrated pedestal

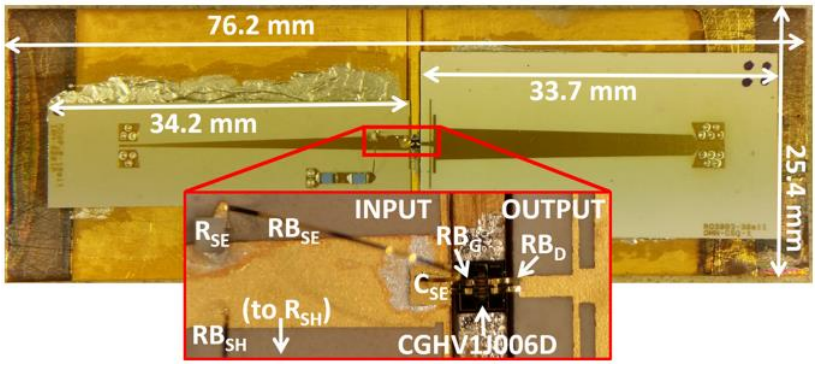


Figure 31 - Fully assembled hybrid amplifier with dimensions

3.3.3 Measured Results

Pulsed DC-IV data were collected over a range of gate and drain voltages to ensure device functionality and to configure the setup for class AB operation. Small-signal data were collected at the designed V_{DS} of 28 V and I_{DSQ} of 65 mA, and the measured amplifier was unconditionally stable (K > 1). The small-signal measurement results for this ultra-wideband PA are found in Figure 32, and the measurement results for P_{OUT} and PAE versus both source power and frequency are shown in Figure 33.

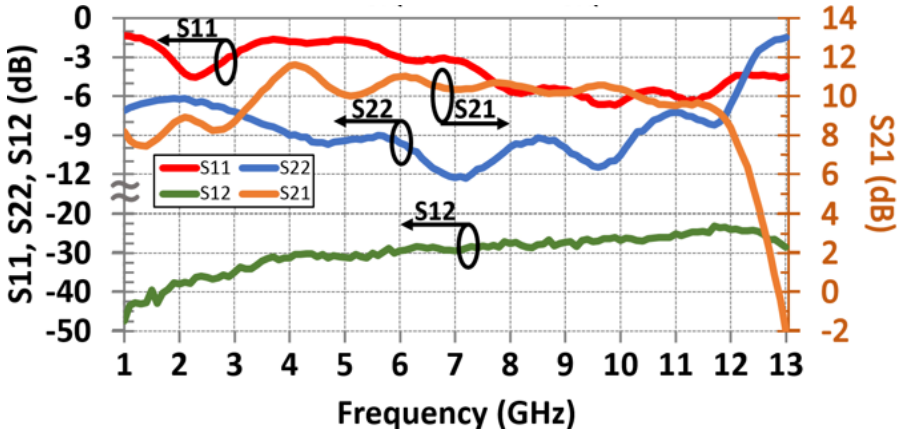
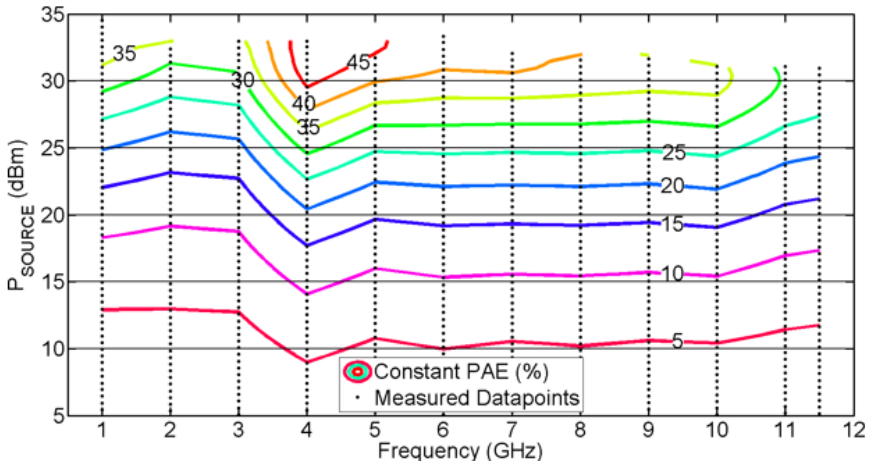
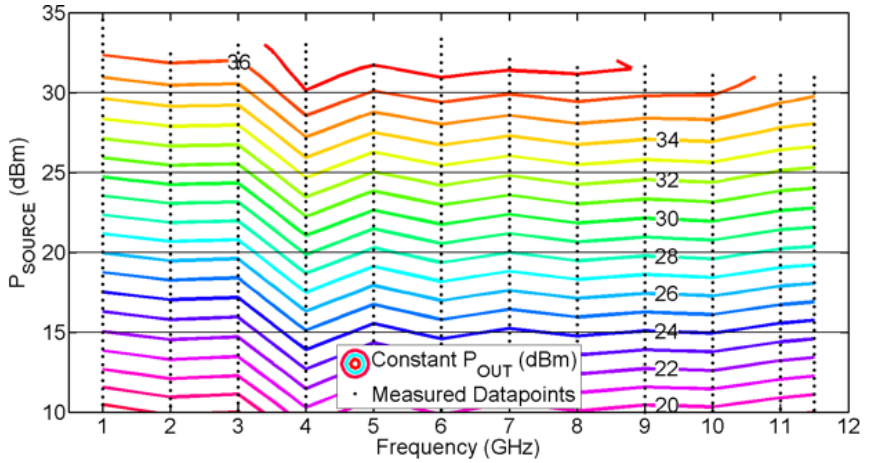


Figure 32 - Measured S-parameters of 1-11.5 GHz hybrid PA



(a)



(b)

Figure 33 - Measured (a) PAE and (b) P_{OUT} for swept source power and frequency

The contours in Figure 33 show that the gain compensation network is successful at leveling P_{OUT} without overdriving the amplifier. The input matching network determines the P_{IN} to the die at any in-band frequency by reflecting and absorbing a portion of the available source power. This aligns the gain compression points for 31 dBm source power such that the full bandwidth shows 3-5 dB of compression. The alignment is observed in Figure 33, as the P_{OUT} and PAE contours are relatively flat versus frequency for a given source power.

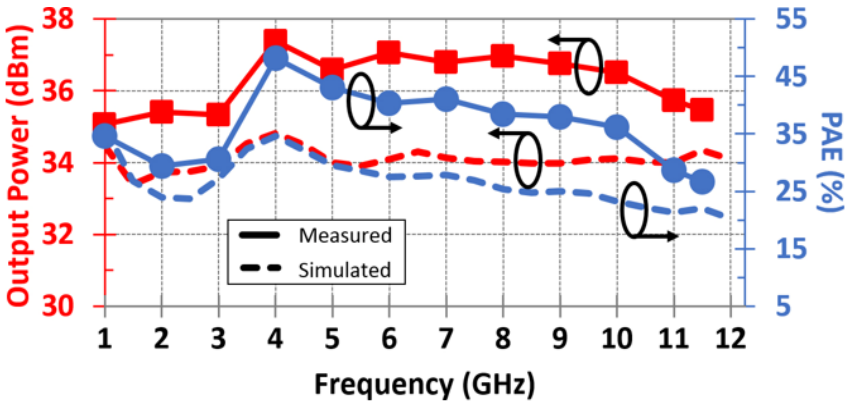


Figure 34 - P_{OUT} and PAE from 1 to 11.5 GHz at fixed source power of 31 dBm

Lastly, P_{OUT} and PAE plots versus frequency at 31 dBm source power are found in Figure 34. This PA delivered a CW P_{OUT} of 3.2-5.5 W at 27-48% PAE from 1.0-11.5 GHz. Choosing a hybrid implementation for this PA enabled a multi-substrate design, allowing optimal Z_0 ranges to be realized for each matching network. This flexibility helped to obtain state-of-the-art P_{OUT} and PAE over an ultra-wide bandwidth using a commercial GaN die. To the author's knowledge, this work demonstrated the widest bandwidth and highest P_{OUT} and PAE achieved by a hybrid design in the L-X bands.

The benefits of a hybrid amplifier – fast design cycle, short production cycle, and low cost in small quantities – certainly make it an appealing design option. However, as frequency is increased, component parasitics can cause significant performance degradation, which is why the designs presented in this chapter have focused on the L through X bands. To investigate broadband microwave PAs at higher frequencies, the next chapter studies designs implemented in an MMIC, which combines all components into a single chip.

CHAPTER 4:

MONOLITHIC MICROWAVE GAN POWER AMPLIFIERS

In contrast to a *hybrid* microwave integrated circuit, all of the passive and active elements in a *monolithic* microwave integrated circuit (MMIC) are integrated into a single chip by a single semiconductor technology process. This level of integration enables the matching circuitry to be located on-die, which lowers the device parasitics and decreases sensitivity to assembly. To take advantage of these benefits, the following MMIC designs focus on broader bandwidths, higher frequencies, or both.

4.1 Reactively Matched C-Ku Band MMIC PA

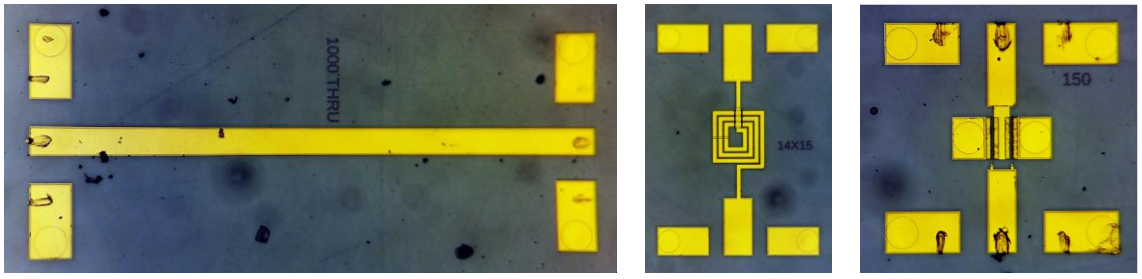
In order to improve the gain and power density of a multi-octave PA, this section first presents the modeling of a new GaN device, and then illustrates the use of that model in a broadband MMIC design. The objective was to create a multi-stage, reactively-matched PA design with multi-watt output power and broad bandwidth on a new GaN process by the National Research Council of Canada (NRC). The findings of this work were published in IEEE's European Microwave Conference [46].

4.1.1 NRC GaN150 Process Description and Sample Characterization

As GaN technology continues to advance, foundries research ways to improve their device performance. The NRC was developing their GaN150 process with 0.15 µm gate length on SiC substrate, and they provided early access to their foundry in collaboration on

this wideband amplifier effort. An early version of a PDK had been created for use in circuit design on their technology, and the kit included electrical models and layouts for standard passive and active components [35]. For any MMIC design, it is paramount to ensure that model simulations agree with measured data. Thus, sample characterization and model verification were vital to build confidence and improve the odds of first-pass design success.

Preliminary ADS simulations provided insights on the operating conditions and expected behavior of the photographed samples in Figure 35. Small-signal measurements (SOLT calibrated) were taken from 0.5-26.5 GHz and used to verify the microstrip transmission lines on the die, thus enabling the use of TRL calibration for improved accuracy of future measurements. S-parameter data was collected from 0.5-26.5 GHz (using both calibration methods) for the microstrip transmission line, resistor, and inductor samples fabricated with the GaN150 process.



(a) **(b)** **(c)**

Figure 35 - Photos of measured NRC GaN150 (a) MTL, (b) inductor, and (c) 2x100 µm HEMT samples

Obtaining accurate EM-simulated predictions of passive component behavior is contingent upon the careful definition of conductors, dielectrics, and other materials that

establish the EM environment. Based upon deduced GaN150 process characteristics, the substrate stack-up was developed for use with MMIC layout and EM simulations. The sample characterization data were then compared to both schematic and EM simulation results for several passive components from the PDK. Good agreement among the data, as shown in Figure 36 for a spiral inductor and Figure 37 for an MTL, helped to validate the stack-up definition and the closed-form schematic models for use in MMIC design.

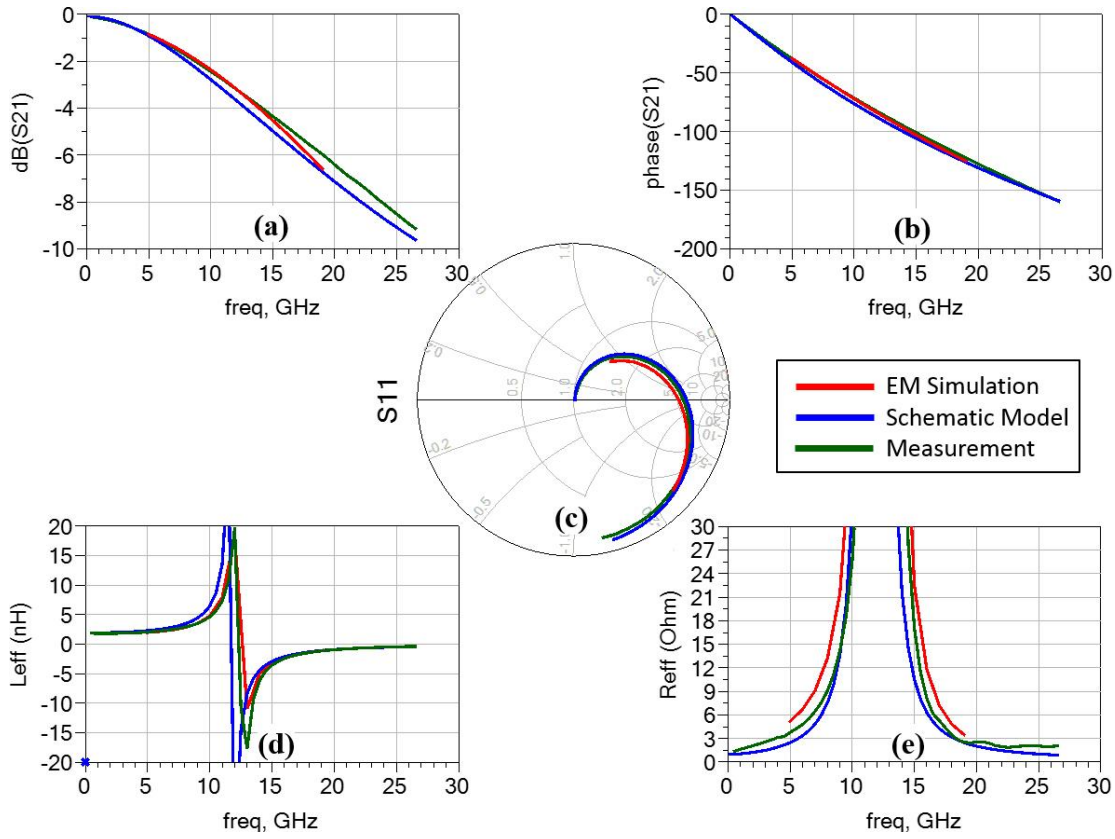


Figure 36 - Comparison of schematic model, EM simulation, and measured data for a NRC GaN150 spiral inductor

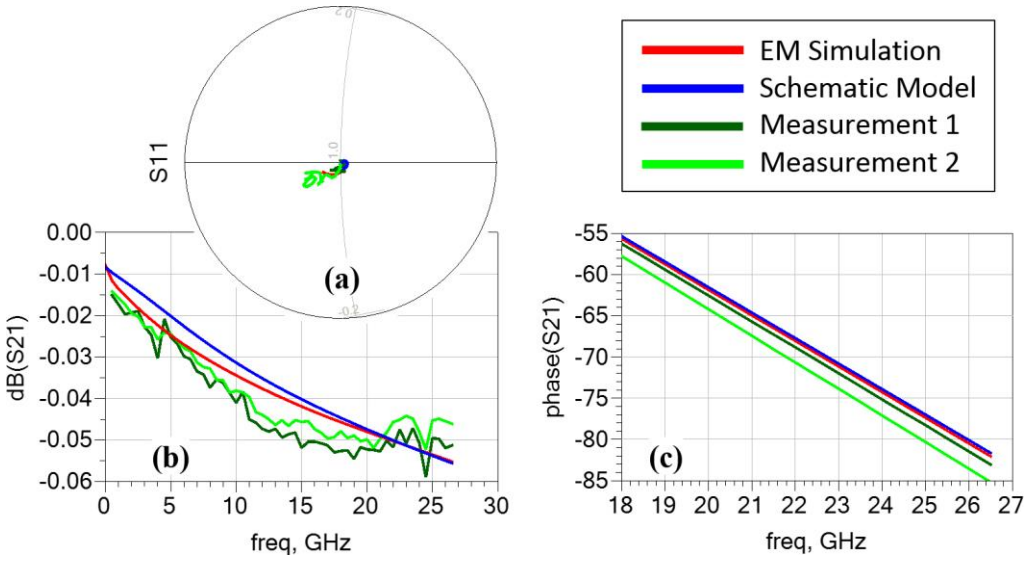


Figure 37 - Comparison of schematic model, EM simulation, and measured data for a NRC GaN150 1000 µm TL

4.1.2 3-Stage Corporate-Combined Broadband Design

The MMIC design uses reactive/resistive matching in a 3-stage corporate-combined topology. A simplified schematic of the amplifier topology is shown in Figure 38. The class-AB single-ended PA used a 2x100 µm device as the unit cell (UC), and is comprised of 8 UCs for the output stage (S3), 4 UCs for the driver stage (S2), and 2 UCs for the input stage (S1). Since the smallest sample device size of 2x100 µm was used to create the model, all stages use the same UC periphery. PAE can be improved in a future design iteration by using a smaller UC for the 1st and 2nd stage transistors. The 2nd and 3rd stages have 4 and 8 UCs, respectively, so the circuitry within the dashed lines is symmetric on the north and south sides of the die, as seen in Figure 38.

All matching elements and biasing circuitry, including input and output DC blocks, are integrated on the die. Each bias connection requires 1 mil diameter gold wirebonds

(WBs) and is named by its stage and function in Figure 38. Lumped metal-insulator-metal (MIM) capacitors were used in conjunction with microstrip lines and thin film resistors to create the input, output, and inter-stage matching networks. Parallel RC networks were connected in series to the gate of every UC for stability, and gain compensation was designed into the 1st and 2nd stages to provide relatively constant large-signal gain across the band.

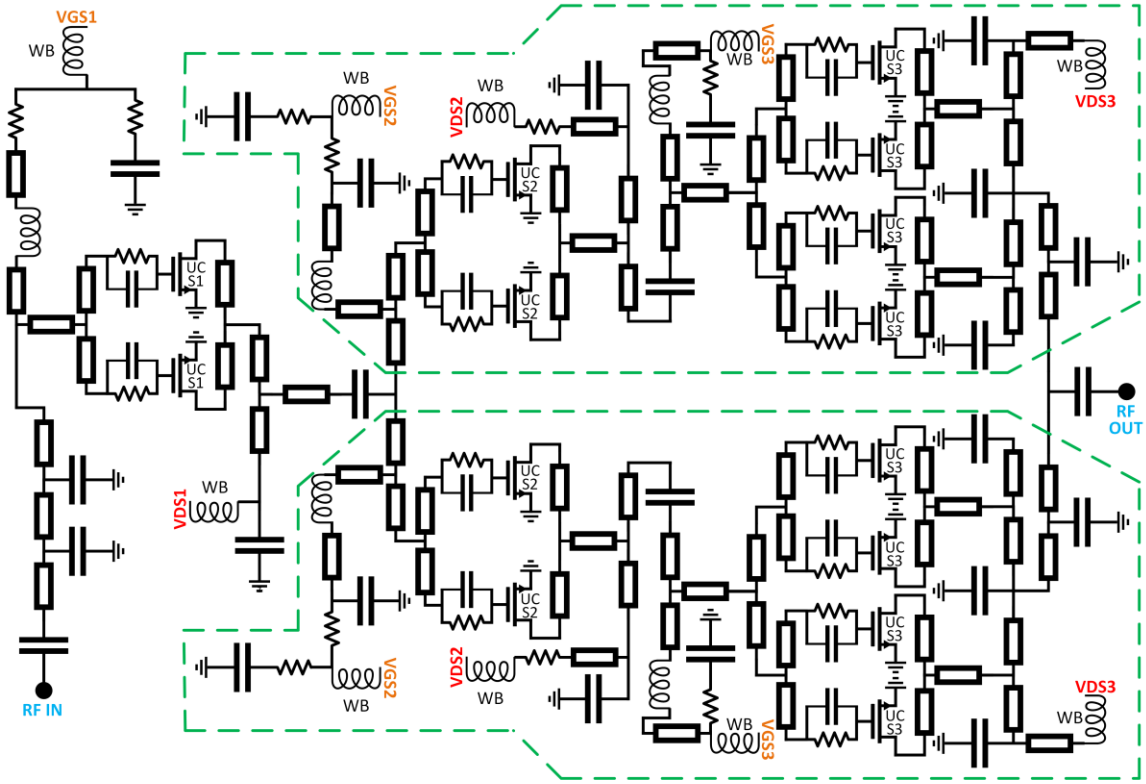


Figure 38 - Simplified schematic of the 3-stage PA design

The schematic-level design in Figure 38 was completed in ADS using PDK components. The transmission line elements were then iteratively replaced with EM-simulated networks, and nonlinear optimizations helped to recover the circuit response by compensating for parasitics. After full-network optimizations, the simulated PA

achieved a $P_{OUT} \geq 4$ W and 16.5 ± 0.5 dB gain from 6 to 18 GHz. The finalized PA MMIC layout that was submitted to NRC for fabrication is depicted in Figure 39.

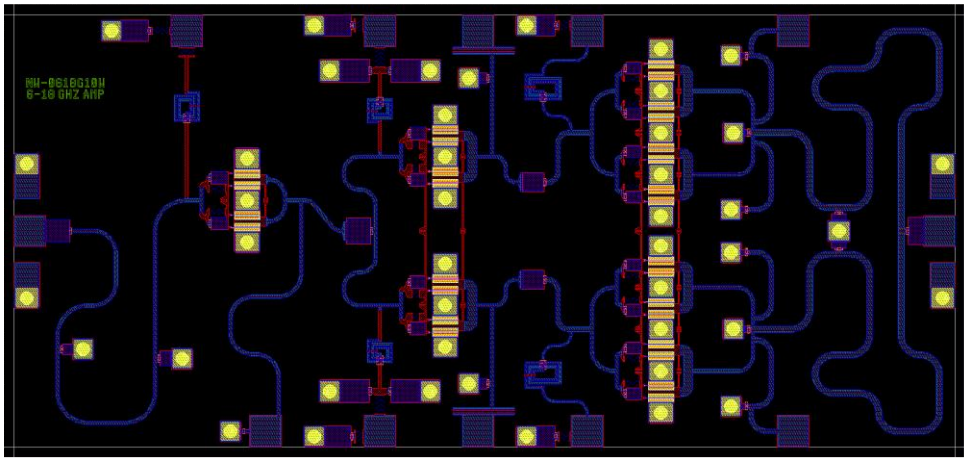


Figure 39 - C-Ku Band MMIC PA layout

4.1.3 Assembly and Measurements

After MMIC fabrication, the singulated dies must be affixed to a carrier and biased properly in order to take probed measurements as shown by the diagram in Figure 40. To decouple the bias lines and reduce parasitic WB inductance, 100 pF single-layer capacitors were also affixed to the carrier. Bias voltages were applied using 1 mil diameter Au wirebonds and DC-MCW probes. To minimize the required WB length, the 100 pF bypass capacitors were placed as closely as possible to every DC bias pad on the MMIC die.

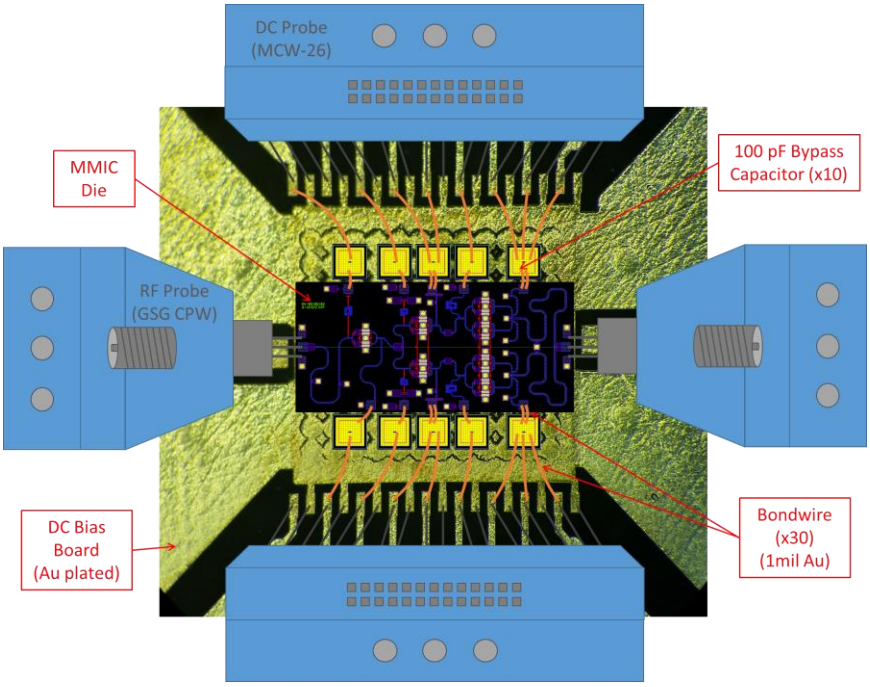


Figure 40 - Diagram of PA assembly and die probing for MMIC measurements

Initial testing ensured device functionality and established the quiescent point for class AB operation. This initial testing was followed by the collection of small-signal data. Finally, the load-pull system was characterized and calibrated for large-signal measurements to capture output power and efficiency performance. A photo of the fabricated, assembled, and measured PA device is found in Figure 41.

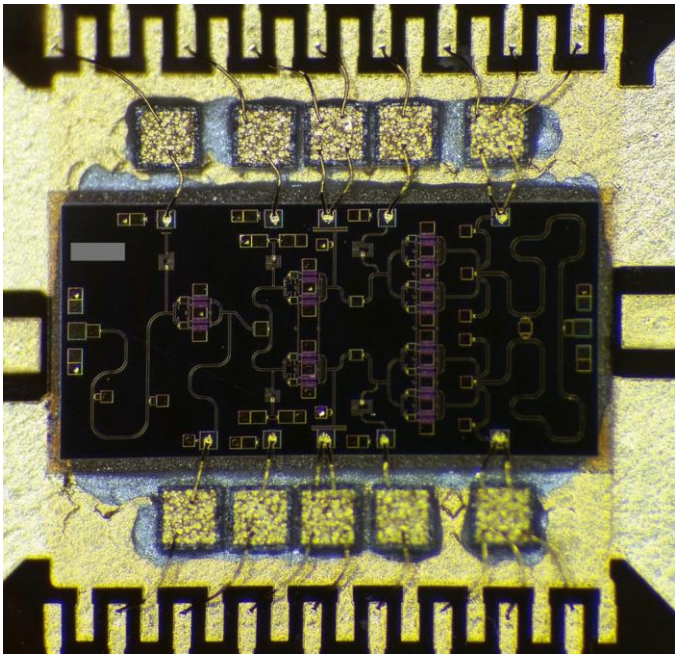


Figure 41 - Photo of the mounted MMIC PA with decoupling capacitors, gold WBs, and the DC multi-contact probe landing pads for biasing

The PA was biased at V_{GS} = -3.45 V and V_{DS} = 28 V, drawing 700 mA of quiescent drain current. Small-signal data were then collected from 0.1-25 GHz in 0.1 GHz steps under 10% duty cycle and 100 µs period pulse conditions. The response of the circuit depends on WB length for bandwidth selection. Based on ADS simulation results, adjustments in WB length and number were completed on the die-to-capacitor bias connections. The measured results are close to the simulated values as seen in Figure 42, except for some gain reduction at the upper band due to a shift in matching. This can be improved by introducing parasitic EM capacitor models in the next design iteration.

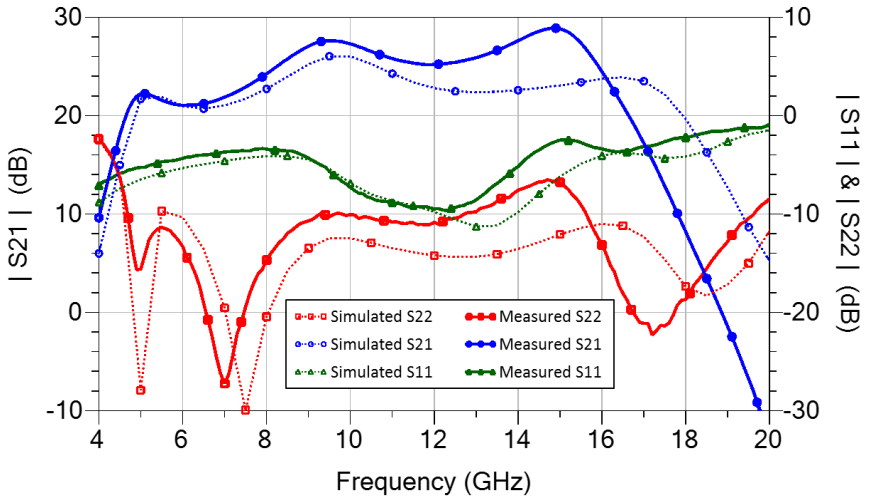


Figure 42 - S-parameter simulation and measurement results

After small-signal measurements, 50 Ω power sweeps from 5-19 GHz in 1 GHz steps were performed on the PA. Data were collected using a passive vector-receiver load-pull configuration, and the available equipment allowed only single-tone large-signal measurements up to 20 GHz. The swept frequency plot in Figure 43 was created for 20 dBm source power and the same pulsed conditions. Large-signal measurement results show the effects of the upper band reduction as noted in the small-signal results, but they are otherwise in agreement with simulation. At 20 dBm source power, the 16 GHz measurements in Figure 44 show 6.3 W output power and 18% PAE with 18 dB gain.

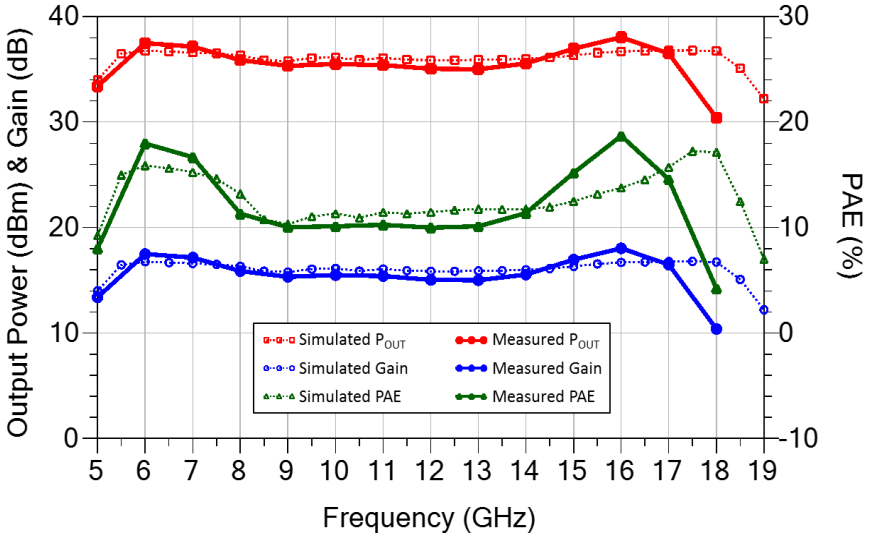


Figure 43 - Comparison of large signal swept frequency simulations and measurements at 20 dBm source power

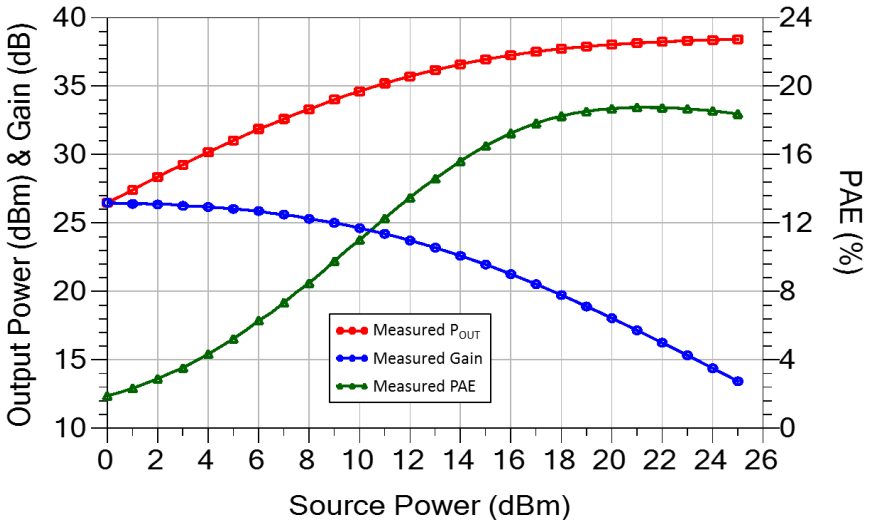


Figure 44 - 50 Ω power sweep measurement results at 16 GHz

The area of this 3-stage MMIC PA is 6.8 mm^2, which corresponds to a measured peak output power density of 0.92 W/mm^2. A comparison of previously published results for reactively matched MMIC PAs on GaN technology with output power ranging from 1 W to 20 W and ~100% fractional bandwidth in the C-Ku range is provided in Table 4.

The lowest and highest reported values are listed for output power, PAE, and saturated gain, along with the output stage periphery and total die area of each device.

Table 4 - Comparison of C-Ku Band GaN MMIC Reactively Matched PAs

Ref (#)	Stages (#)	Frequency (GHz)		P_{OUT} (dBm)		PAE (%)		$Gain_{SAT}$ (dB)		W_G* (mm)	P_{OUT}/W_G (W/mm)		Area (mm^2)	P_{OUT} Density (W/mm^2)	
		Low	High	Low	High	Low	High	Low	High		Low	High		Low	High
[46]	**3**	**6**	**17**	**35.2**	**38.0**	**10**	**18**	**15**	**18**	**1.6**	**2.07**	**3.94**	**6.8**	**0.48**	**0.92**
[47]	3	6	18	37.8	40.0	13	25	15	19	2.4	2.51	4.17	19.8	0.30	0.50
[48]	2	6	18	41.2	43.0	13	24	7.2	12.1	6.8	1.94	2.93	19.2	0.69	1.04
[49]	3	6	18	39.0	42.0	14	23	12	15	3.2	2.48	4.95	19.3	0.41	0.82
[50]	2	6	20	30.0	36.6	3	17	6	12	2.88	0.35	1.59	19.1	0.05	0.24
[27]	1	8	18	30.8	32.5	24	35	4.8	6.5	-	-	-	10.4	0.12	0.17
[51]	2	C†	Ku†	40.2	41.6	17	30	11†	15.5†	6.8	1.54	2.13	16.6	0.63	0.87
[52]	2	6	18	35.7	37.5	13	21	13.5	19.1	-	-	-	8.8	0.42	0.64

* Total transistor gate width of the power stage.
† Publication does not provide frequency values for band limits, only letters. Large signal gain was also not provided, so values were estimated from small-signal plots and stated compression point.

Both frequency magnitude and relative bandwidth are important factors to consider when comparing performance, as device characteristics are poorer at higher frequencies, and matching challenges are more difficult at wider bands. Hybrid implementations of wideband PAs are very large in comparison to MMICs, and other wideband techniques – such as distributed PAs – require a larger die area to achieve similar gain and output power.

In this section, a 2x100 µm HEMT fabricated on a new 0.15 µm GaN-on-SiC process from NRC was characterized and modeled for 28 V operation. Using that nonlinear model, a 3-stage reactively matched PA with 3.8 mm x 1.8 mm die dimensions was designed and fabricated. Large signal measurements showed an average of 5 W output power and

13% PAE over a 6 to 17 GHz bandwidth. Compared to previously published results found in Table 4, these results demonstrate the highest output power per die area for a 3-stage GaN MMIC PA of this bandwidth in this power range.

Continuing with reactively-matched MMIC PAs, this next design seeks to improve performance at even higher frequencies with a multi-stage Ka band PA using a new 0.14 µm GaN process.

4.2 Reactively Matched Ka Band MMIC PA

4.2.1 Cree G28V5 Process Description

One major challenge in GaN PA design at higher frequencies is the insufficient level of maximum available gain from existing foundry processes. Following the worldwide success of their V4 0.25 µm GaN process, Cree developed modifications for V5 to enable fabrication of 0.14 µm gate length HEMTs [53]. These changes led to useable device gain at higher frequencies when compared to previous process versions. The G28V5 process was in pre-release status at the time of this design, as the foundry was completing final development. Nonlinear model simulation results were confirmed by measurements of device samples, and passive components were also verified for design use. With an estimated 4.5 W/mm power density for this pre-release 0.14 µm GaN foundry process, the following study capitalizes on the improved gain at higher frequencies and targets a multi-watt MMIC PA design in the Ka band.

4.2.2 2-Stage Corporate-Combined PA Design

This MMIC used reactive and resistive matching elements in a corporate-combined 2-stage PA design to achieve 4 W output power in Ka band. After the schematic design was optimized, EM simulations were first executed for individual components, and then for groups of components. After each iteration, these models were imported back into the schematic, and the co-simulated circuit was reoptimized. Finally, EM simulations were executed on the full interconnected networks at fundamental and 2nd harmonic frequencies. The networks were also EM-simulated from DC to f_0 to ensure low frequency stability. These final EM models were imported back into the schematic as shown in Figure 45, and the large-signal simulation results appear in Figure 46. Due to limitations in available reticle area, DC biasing ground pads were omitted from the top-side of the die. The final MMIC PA layout that was submitted for fabrication is depicted in Figure 47.

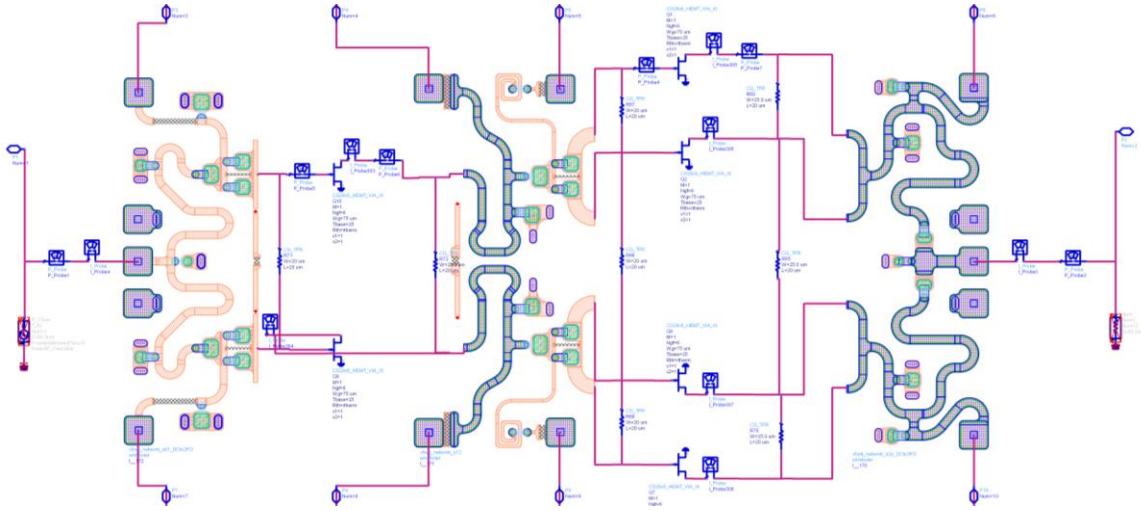


Figure 45 - Final schematic showing fully EM-simulated matching networks for the input, interstage, and output

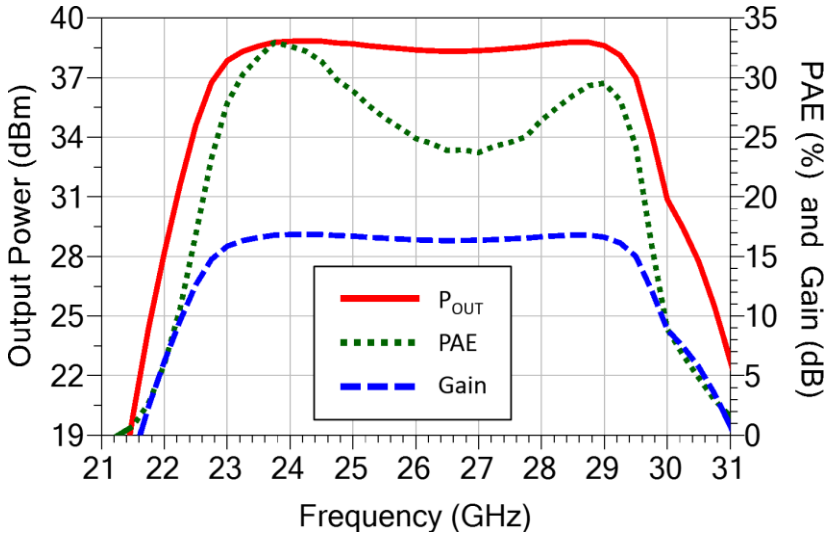


Figure 46 - Harmonic balance simulation results with EM-simulated networks for the 2-stage Ka band MMIC PA showing output power, PAE, and transducer gain

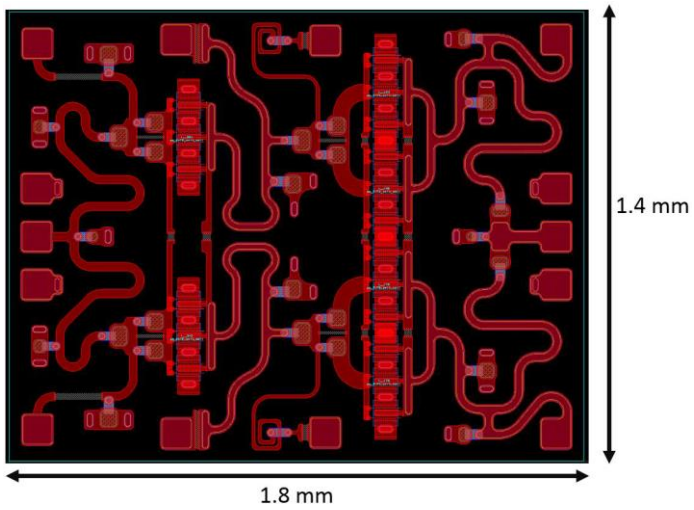


Figure 47 - Final layout of the 2-stage Ka band reactively-matched MMIC PA

The PA was designed using the Cree G28V5 0.14 µm GaN process and was fabricated on a pre-release foundry run. In preparation for measurements, the die will be mounted onto a carrier and biased for proper operation.

4.2.3 Assembly and Measurements

This MMIC fabrication run yielded many copies of the same design which were manufactured at the same time on the same process. These circumstances represented a suitable opportunity to evaluate the impact of process variations on the performance of this PA design. With measurement sequences planned for 20 PA dies, it was desirable to establish a rapid and repeatable method of probing the pads on a die. The design required DC bias voltages for the gate and drain to be applied to both sides of a singulated die for proper operation. Of course, connections at the RF input and RF output of a die were also necessary to measure that die's performance. At the same time, each die required good thermal grounding due to the expected levels of output and dissipated power in the design.

To resolve these constraints, the following biasing scheme was developed. The bias voltages were applied to each die with two custom DC-MCW probes. The needles were arranged in two rows, and each bias voltage used a GND | V_{DC} | GND format. This configuration is shown in the probing setup diagrams in Figure 48 and Figure 49. A CuW carrier with integrated grooves was fabricated so that the MMICs could be mounted within the grooves as depicted in Figure 50. Attaching the dies inside the groove with a eutectic preform enabled the GND needles on the DC-MCW probe to make good planar contact with the CuW carrier while also providing an excellent thermal sink for the die. Furthermore, this method enabled reuse of the DC-MCW probes if further testing on the MMIC with a biasing PCB were required.

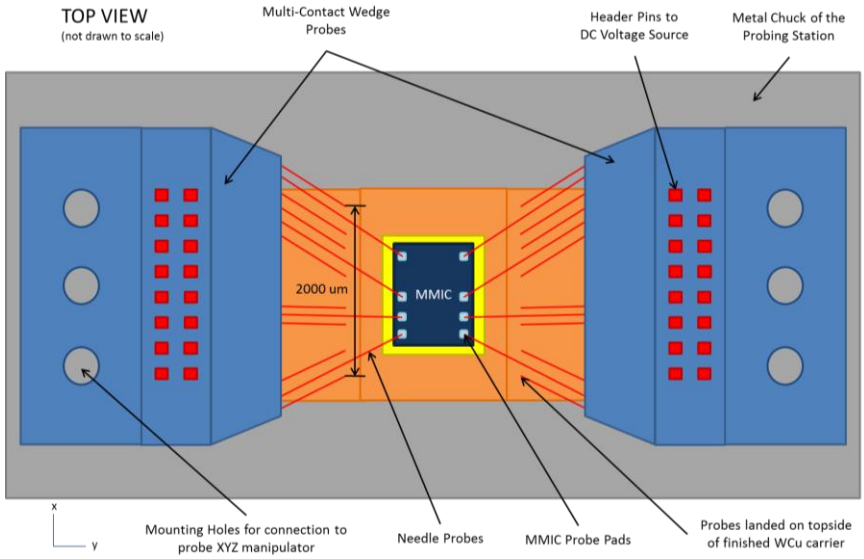


Figure 48 - Probing setup (top view) for DC biasing of the Ka band MMIC PA

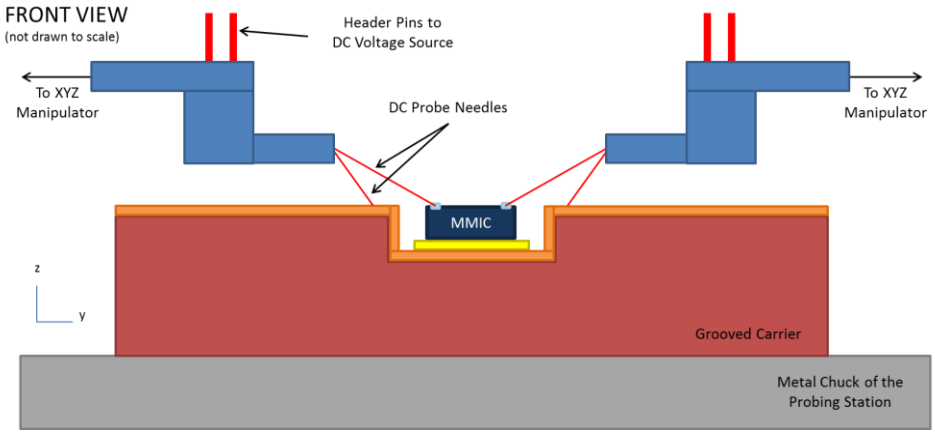


Figure 49 - Probing setup (front view) for DC biasing of the Ka band MMIC PA

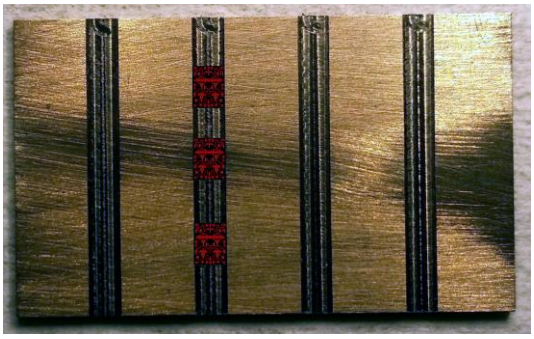


Figure 50 - Gold-plated CuW carrier with milled grooves for eutectic die attach

After the CuW carrier was milled and plated with gold, the MMIC die in Figure 51 was affixed inside the groove using an 80% Au 20% Sn preform in a eutectic die attach process. Several more dies were attached in a similar manner, and the assembled PA samples were now ready for performance measurements.

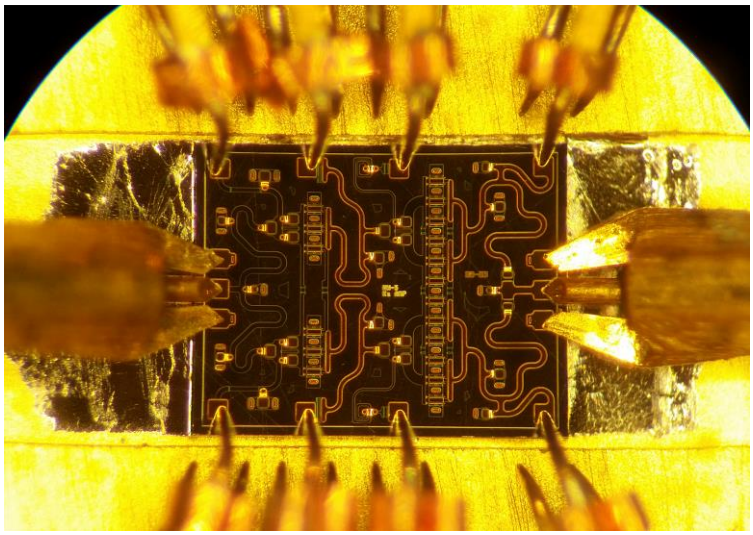


Figure 51 - Photo of a fabricated, probed, and measured Ka band MMIC PA

Although decoupling capacitors were integrated into the DC-MCW probe design, it was challenging to accurately predict or control the inductances of the probe tips. Furthermore, there was an additional increase in path length due to the GND needles landing on the carrier and not the die. Because of these issues, the measured performance of the tested samples was inconsistent with the simulation results. The small-signal results showed a reduced gain and modified output match. Large-signal measurements using a power meter setup were then executed for several bias points. While the achieved output power and bandwidth were relatively close to simulated values, the reduced gain had a negative impact on the measured PAE.

Since the bias probing method was likely limiting the performance of the die, a new sample was assembled using the wirebond and SLC approach for the DC connections as discussed in Section 4.1.3. This is a more labor-intensive and expensive method which required additional tooling and components. However, using this method allowed the capacitor locations and wirebond lengths to be individually controlled. The photograph in Figure 52 depicts the fully assembled sample. The DC-MCW probes were still used to apply bias to the wirebonds leading to the die, but the impact of the needle inductance became negligible because of the 100 pF bypass SLCs.

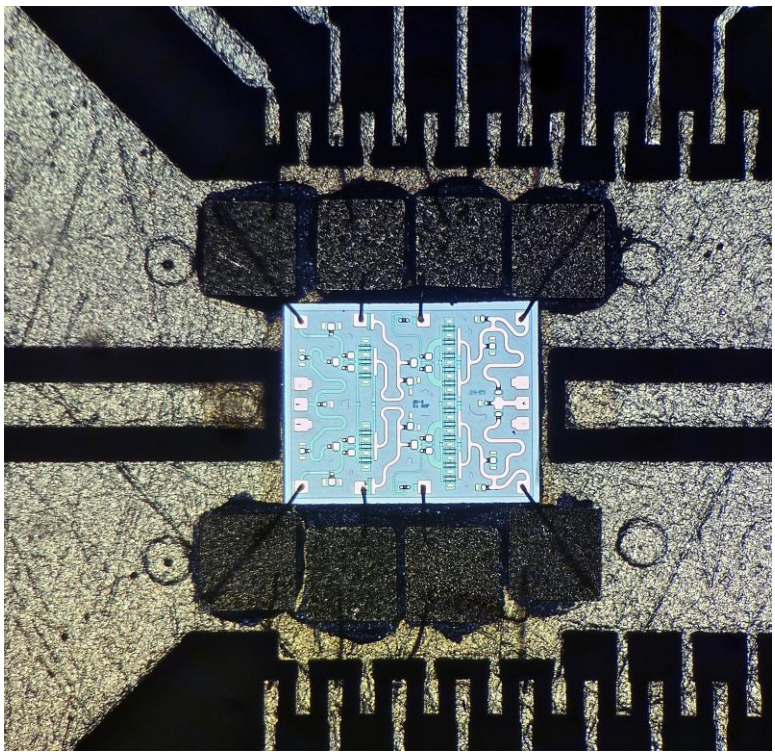


Figure 52 - Ka band MMIC PA sample assembled with wirebonds and single layer capacitors for DC bias connections

Small signal measurements of the new sample were collected at the nominal design bias point of V_{DS} = 28 V and I_{DSQ} = 250 mA. Measured results are plotted alongside the

simulated results in Figure 53, and their agreement is quite good. The new sample had a higher gain at a lower quiescent bias current, and it displayed return loss profiles that tracked the simulated values across most of the band.

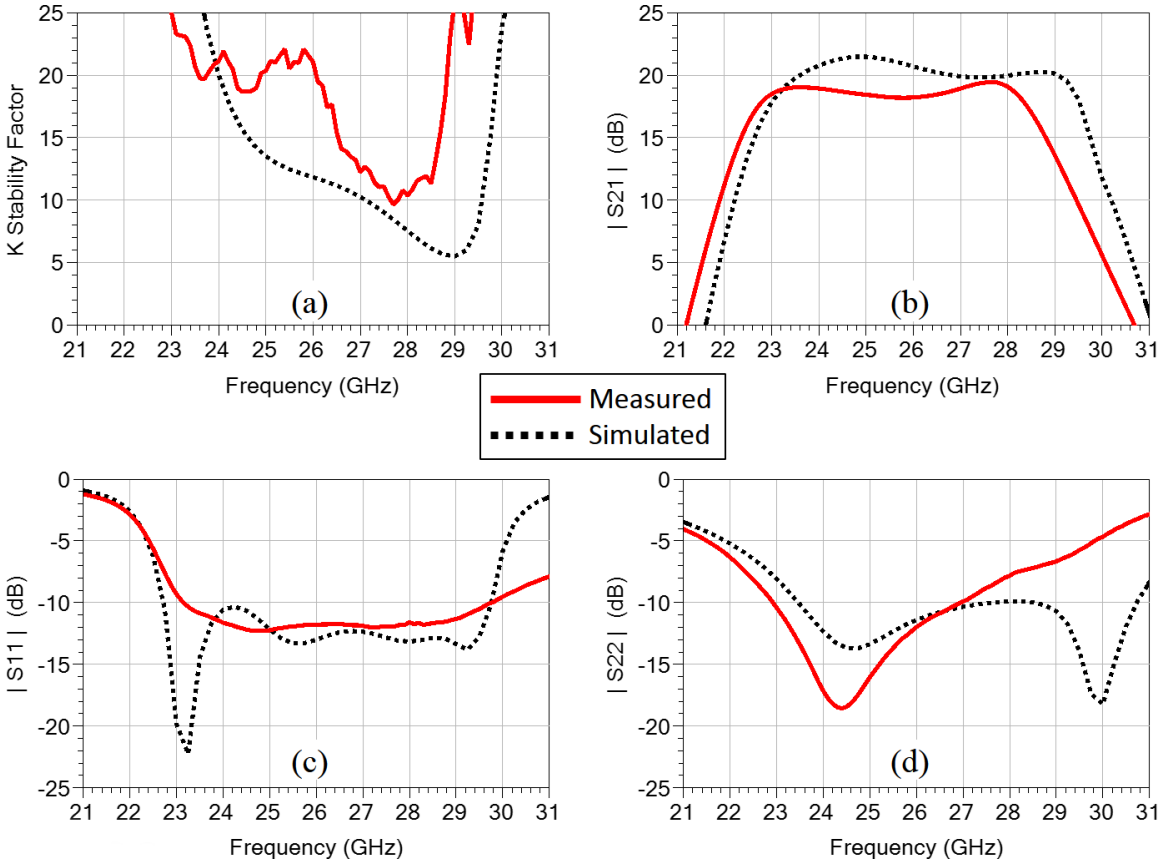


Figure 53 - Comparison of small signal simulation and measurement results for the Ka band MMIC PA

Following the small signal measurements, 50 Ω power sweeps were executed from 21 GHz to 30 GHz. The results shown in Figure 54 were collected with a source power of 25 dBm at a bias point of V_{DS} = 28 V and I_{DSQ} = 330 mA. Over 36 dBm of output power were measured from 22.5-28 GHz, with a peak PAE of 27% at 23 GHz. The results of the source power sweep at that frequency are plotted in Figure 55.

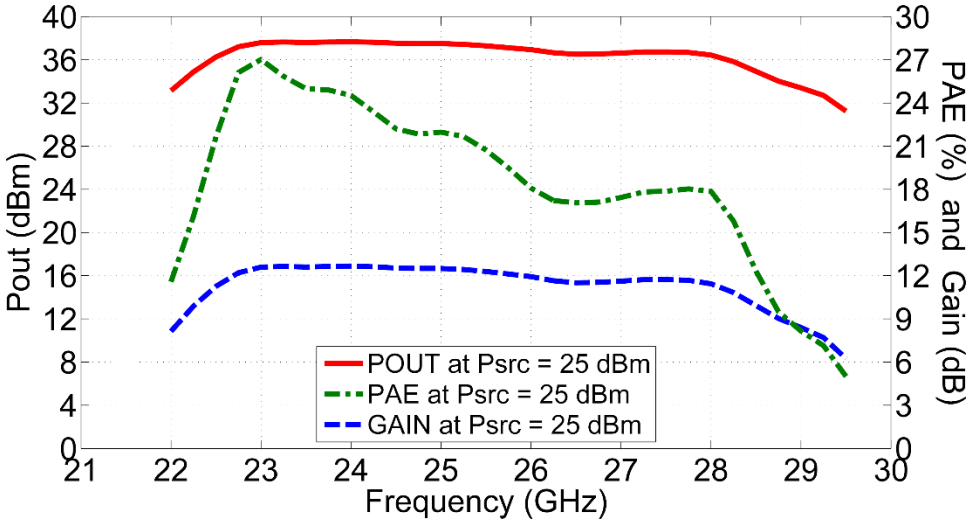


Figure 54 - Large signal measurements of the Ka band MMIC PA versus frequency at 25 dBm source power

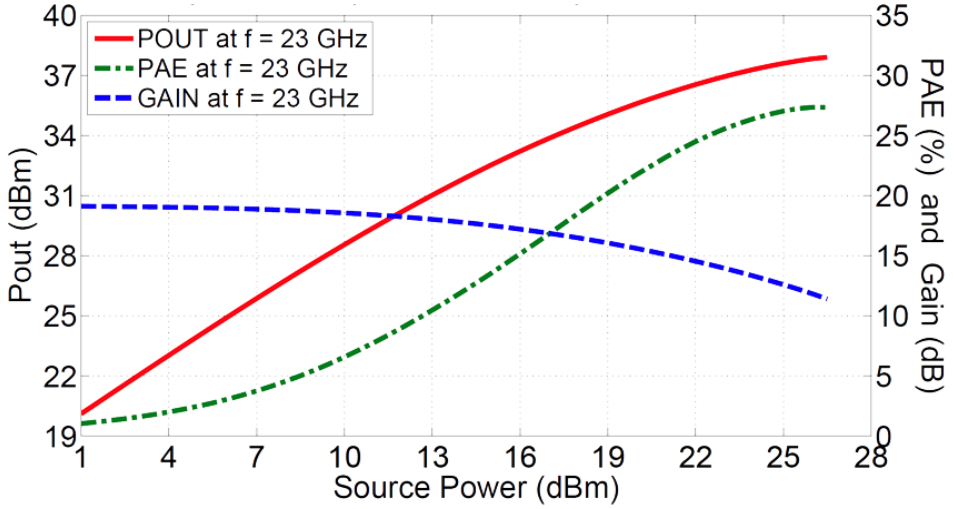


Figure 55 – Power sweep measurements of the Ka band MMIC PA at 23 GHz

With more than 4 W of output power and over 20% average PAE from 22.5-28 GHz in a 2.52 mm^2 die area, these results have demonstrated the efficacy of the reactive/resistive matching approach using an MMIC implementation for a Ka band PA design. The direct access to transistor feedpoints – which is an advantage afforded by an

MMIC implementation – serves to reduce parasitics, thereby enabling the realization of improved gain at higher frequencies.

In the final section of this chapter, the same G28V5 MMIC process is chosen for another amplifier implementation, but now the previously-discussed traveling wave technique will be employed to extend performance in an ultra-wideband PA design.

4.3 Non-uniform Distributed 2-40 GHz MMIC PA

To study ultra-wideband PAs at even higher frequencies and extend the performance of the previously published works discussed in Section 1.2, this MMIC design focuses on achieving high output power over the widest bandwidth by using the traveling wave technique. The results of this effort were under peer review for journal publication [54] when this dissertation was submitted.

4.3.1 Cree G28V5 Process Description

The same Cree G28V5 foundry process described in Section 4.2.1 was used again to take advantage of its increased gain at higher frequencies in comparison to prior versions of the process. Because the foundry was still completing final development, this 0.14 µm GaN-on-SiC process was in pre-release status at the time of this design.

4.3.2 Ultra-wideband 10-cell Traveling-Wave PA Design

This design utilized a non-uniform distributed power amplifier (NDPA) architecture, and the simplified topology shown in Figure 56 highlights the inter-

connections of the NDPA in schematic format. Although optimal impedances cannot be supplied to every NDPA cell, the distributed approach has an extremely broadband response, and several methods were used to improve the impedance matching at each device.

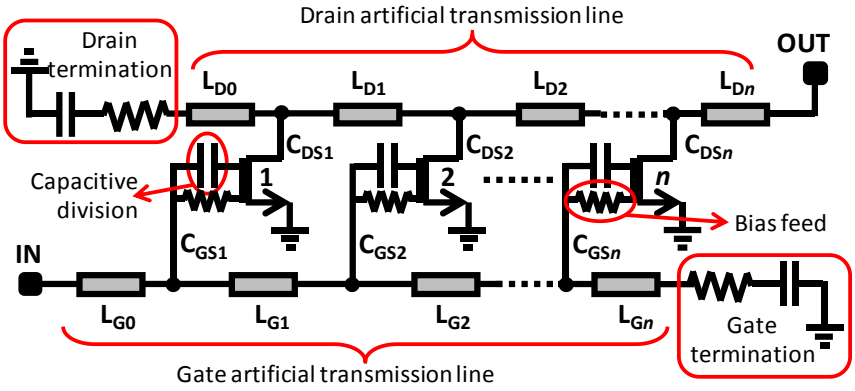


Figure 56 - Non-uniform distributed PA topology

The available G28V5 non-linear device model was used in load-pull simulations across the 2-40 GHz band to first evaluate the large signal performance of different HEMT peripheries, and then to determine the optimal power load of the selected unit cell devices. For such a wide bandwidth, a constant conductance G_{OPT} in parallel with a constant capacitance C_{OPT} can give an approximation for the conjugate of the optimal power load [55]. This $G_{OPT} \parallel C_{OPT}$ can then be used with the following equations from [55] to provide a starting point for NDPA design.

The optimal characteristic conductance $G_{CD(i)}$ for the i^{th} section of the drain artificial transmission line is:

$$G_{CD(i=1)} = G_{OPT(1)} \tag{8}$$

$$G_{CD(i\geq 2)} = \frac{{G_{OPT(1)}}^2}{G_D + G_{OPT(1)}} + \sum_{k=2}^{i} G_{OPT(k)} \tag{9}$$

where G_D is the conductance of the drain ATL termination and $G_{OPT(k)}$ is the optimal load conductance of the k^{th} transistor. The maximum overall output power P_{OUT} of an NDPA with n transistors can be estimated by Equation 10, where $P_{MAX(k)}$ denotes the maximum output power of the k^{th} transistor.

$$P_{OUT} = \left(\frac{G_{OPT(1)}}{G_D + G_{OPT(1)}}\right) \cdot P_{MAX(1)} + \sum_{k=2}^{n} P_{MAX(k)} \tag{10}$$

The selected 100 µm unit cell device has a simulated maximum small-signal gain of 12 dB at 40 GHz. Optimal large signal load impedance contours for this device are plotted at several frequencies in Figure 57. The marked trace represents an ideal (G_{OPT} = 2mS) || (C_{OPT} = -32 fF) power load condition, and is generally coincident with the contours over the full bandwidth. This ideal conductance was used in Equations 8, 9, and 10 to obtain initial values for design optimization.

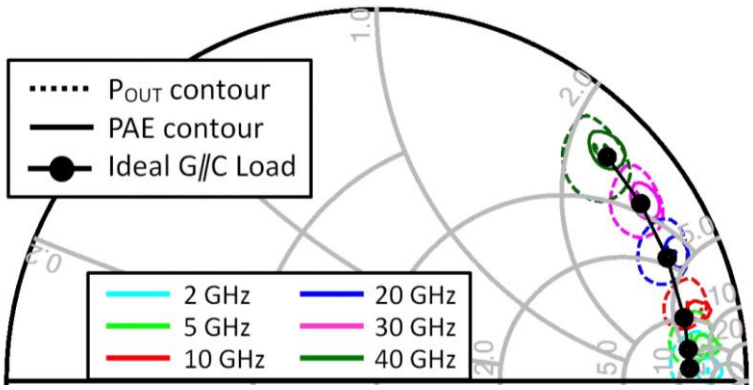


Figure 57 - Comparison of optimal power load impedance contours and a constant G||C load condition at select frequencies from 2-40 GHz

The NDPA layout in Figure 58 has been annotated to highlight the components included in the design. Non-uniform transistors arranged in a 10-cell single-stage configuration were connected by tapered gate and drain lines to provide more favorable large-signal impedances to the distributed transistors. Since the targeted bandwidth is extremely wide, the termination components listed in Table 5 were included at the ends of the ATLs. Transistors X_1 and X_2 each have a total gate periphery of 200 µm, while transistors X_3 through X_{10} each have a total gate periphery of 100 µm. This arrangement of non-uniform cells was determined to reach a suitable trade-off among the design parameters of gain, output power, and matching quality. The drain line length between each cell was optimized to absorb the output capacitances of the transistors and enable the in-phase addition of transistor currents.

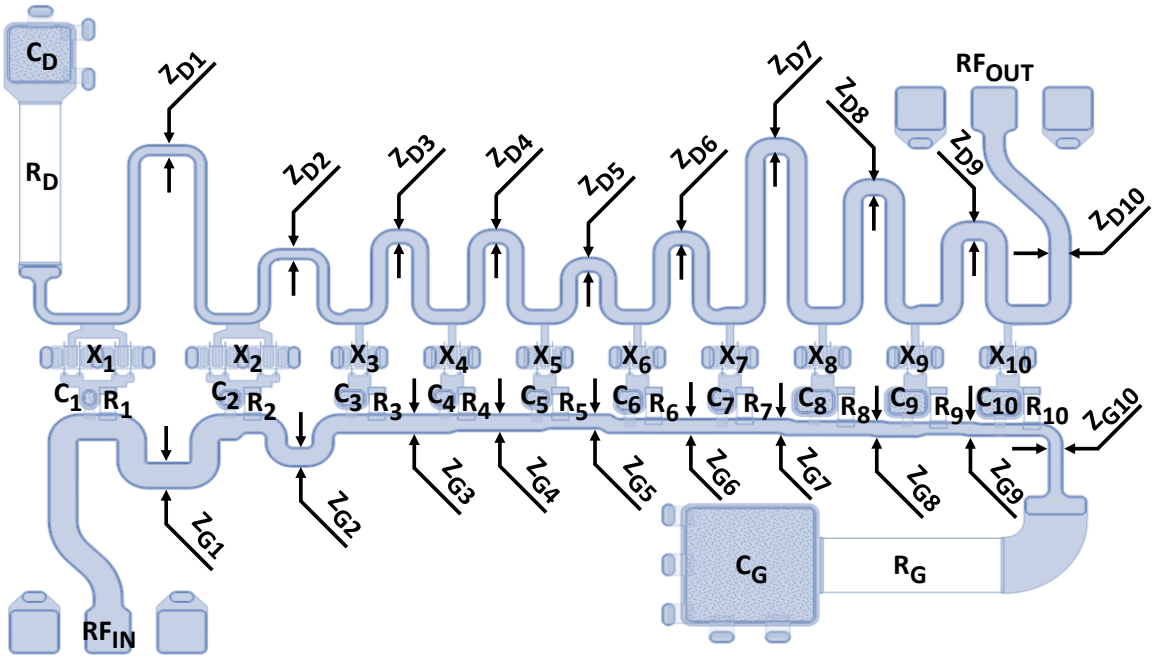


Figure 58 - Layout of 10-cell NDPA with annotated component references

Capacitive division at each of the transistor gates served to improve the gate line cut-off frequency by reducing the effective capacitance that was required to be absorbed into the gate ATL. This capacitive coupling represents a beneficial tradeoff of lower gain for wider bandwidth. However, this tradeoff could have diminished appeal if the capacitor sacrifices too much gain in the pursuit of greater bandwidth, as output power and PAE will be reduced. These series gate capacitors were tapered in size (increasing from C_1 to C_{10}) to better equalize the high frequency drive available at each cell's gate.

Table 5 - Artificial Transmission Line Termination Components

Component	Description	Value
R_G	Gate ATL Termination Resistor	35 Ω
C_G	DC Blocking Capacitor (Gate Termination)	11.2 pF
R_D	Drain ATL Termination Resistor	52 Ω
C_D	DC Blocking Capacitor (Drain Termination)	2.6 pF

Resistors R_1 to R_{10} were placed in parallel with the series gate capacitors C_1 to C_{10} to provide a DC bias path and assist in achieving unconditional stability. The gate and drain ATL geometries were designed to absorb the HEMTs' input and output capacitances into the interconnecting transmission line segments [17], enabling higher output power and PAE by improving the power distribution and impedance match for each cell. Instead of limiting the ATLs to a constant characteristic impedance (fixed width), a variable-width geometry was selected. The drain line characteristic impedance was gradually decreased towards the output by widening the transmission lines from Z_{D1} to Z_{D10}, while the gate line characteristic impedance was gradually increased towards the output by narrowing the transmission lines from Z_{G1} to Z_{G10}. These geometries were optimized in parallel for best performance, and helped improve the impedances seen by each die. To complete the ATL layouts, transitions were designed at the RF_{IN} and RF_{OUT} ports for 150 µm pitch ground-signal-ground (GSG) probes, enabling measurement of device performance.

The circuit was first simulated and optimized in ADS software using schematic components and models from the Cree PDK. Adjustments to the PDK were made to accommodate changes for the V5 pre-release process. EM simulations were executed using

ADS Momentum Microwave software on the full gate and drain line layouts. These EM-simulated networks – which included the tapered transmission lines, series capacitors, bias resistors, and termination components – were placed into the circuit schematic and connected to the appropriate non-linear HEMT models to simulate the final design performance. The simulation results are included with the measurement plots in Section 4.3.3 and show more than 1 W of output power and 6 dB of saturated gain at 10% PAE from 2-40 GHz. The final layout, which was submitted to Cree for fabrication, is found in Figure 58.

4.3.3 Assembly and Measurements

After the GaN fabrication process was completed, the singulated die was mounted onto a 40-mil thick Au-plated CuW carrier, and an 80% Au 20% Sn preform was used for eutectic die attach. A photo of the measured 2.2 mm x 1.8 mm die is found in Figure 59.

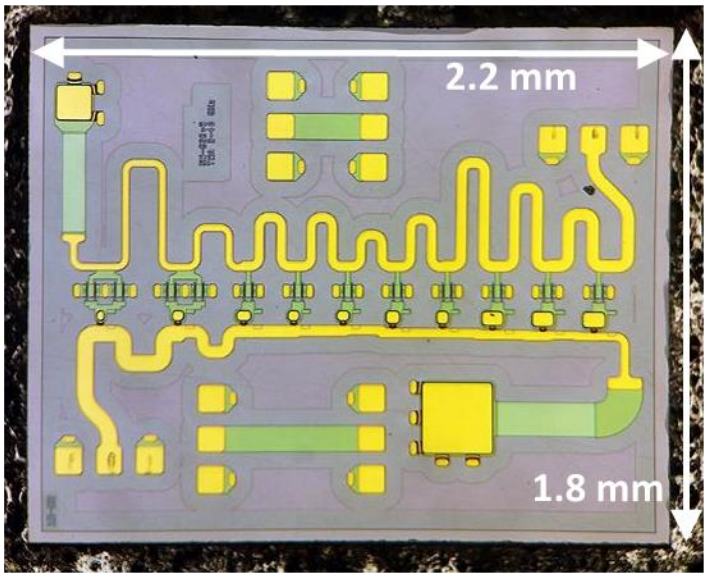


Figure 59 - Annotated photo of the fabricated and measured NDPA die

The MMIC NDPA was biased through GSG probes and external bias tees for class AB operation, with V_{DS} = 28 V and I_{DSQ} = 135 mA. Measurements were taken at room temperature using a 50 Ω vector network analyzer (Agilent N5244A) under small-signal excitation from 0.1-43.5 GHz. The measured NDPA was unconditionally stable, as shown by the K-factor and stability measure results in Figure 60.

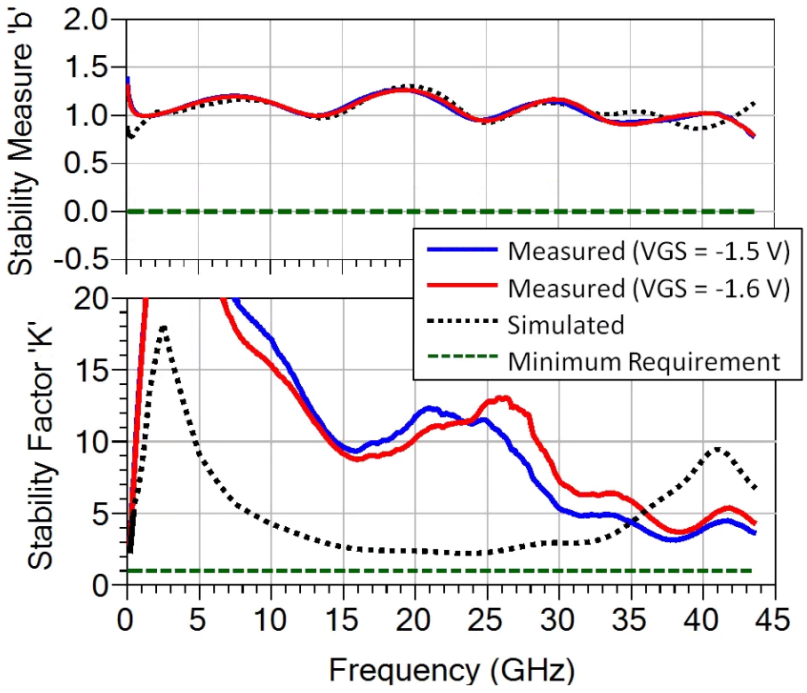


Figure 60 - Stability measure and stability factor, simulated vs. measured

The EM-simulated results obtained in ADS are compared with the measured S-parameter data for input and output return loss in Figure 61. Measurements show excellent agreement with the simulated response for the input matching. While a minor frequency shift is seen above 30 GHz for the output matching, the curves show very good agreement in the lower frequencies, with clear and consistent trends. Small-signal gain is plotted in Figure 62, showing the measured data at two bias conditions for comparison with

the simulated results. There is excellent agreement across most of the bandwidth, and an improvement in small-signal gain was measured above 35 GHz. As shown in Figure 62, the measured NDPA provided an average 8.5 dB small-signal gain from 2-40 GHz.

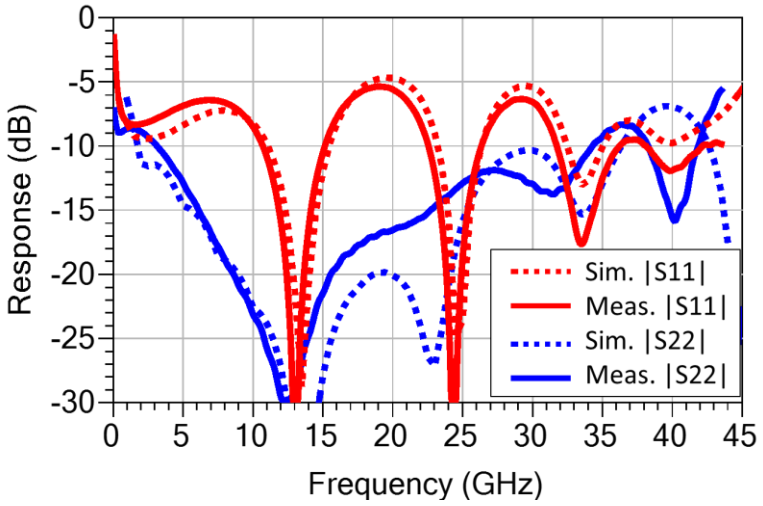


Figure 61 - Input and output return loss, simulated vs. measured

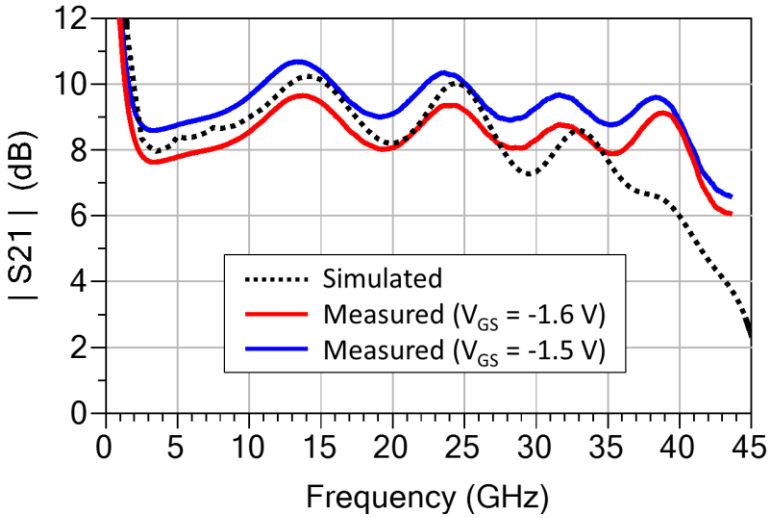


Figure 62 - Small-signal gain, simulated vs. measured

The measured improvement in small-signal gain above 35 GHz can be attributed to G28V5 process changes enacted after the initial development of the large signal device

model used in circuit simulations. This design was created for a pre-release process version which was not yet finalized at the time, so some deviation from the modeled performance could be expected. The effect can be observed in Figure 63, which compares the simulated and measured maximum gain of a stand-alone 4 x 100 µm device that was fabricated on the same reticle and wafer as the measured NDPA. Measurements showed a higher maximum gain at higher frequencies than was predicted by simulation, indicating that the NDPA could experience a similar change in performance.

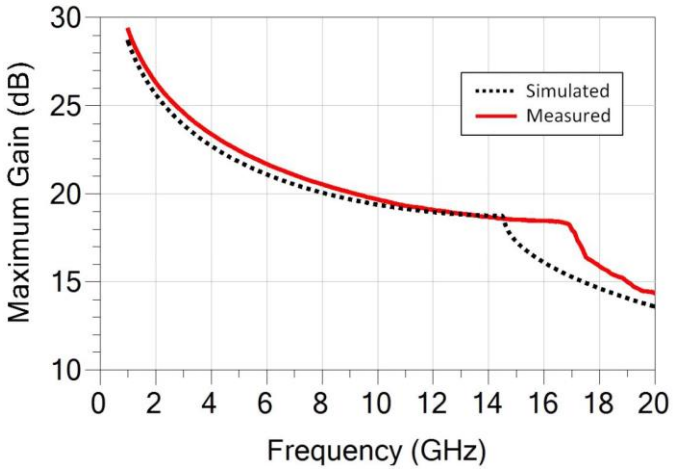


Figure 63 - Simulated vs. measured maximum gain for a 4x100 µm G28V5 device fabricated on the same wafer and reticle as the NDPA

After S-parameter measurements were completed, the NDPA was measured under large-signal drive conditions at room temperature with 50 Ω terminations. Multiple large-signal measurement methods and sequences were required to cover the full frequency band because of available laboratory equipment limitations and the extremely wide frequency response of this PA. All large-signal measurements below 18 GHz were collected using the Maury IVCAD vector-receiver based passive load-pull system shown in Figure 8, while

all large-signal measurements at 18 GHz and above were collected using the Maury MT-1000 active load-pull system shown in Figure 10. These load-pull systems were used to correct for measurement system impedance mismatches and present true 50 Ω loads to the DUT.

Signal power levels were calibrated at the plane of the probe tip, and source power sweeps were executed at 0.5 GHz steps across the band. The plots in Figure 64 show the measurement results at 26 dBm source power, demonstrating that the amplifier achieved an average of 31.5 dBm output power with an average 9% PAE and 5.5 dB gain across the S to Ka bands. These measurements show excellent agreement with the simulated responses for power, efficiency, and gain for nearly the entire design bandwidth. At frequencies above 35 GHz, the measured results show a performance improvement when compared to the simulated results due to the effect observed in Figure 63.

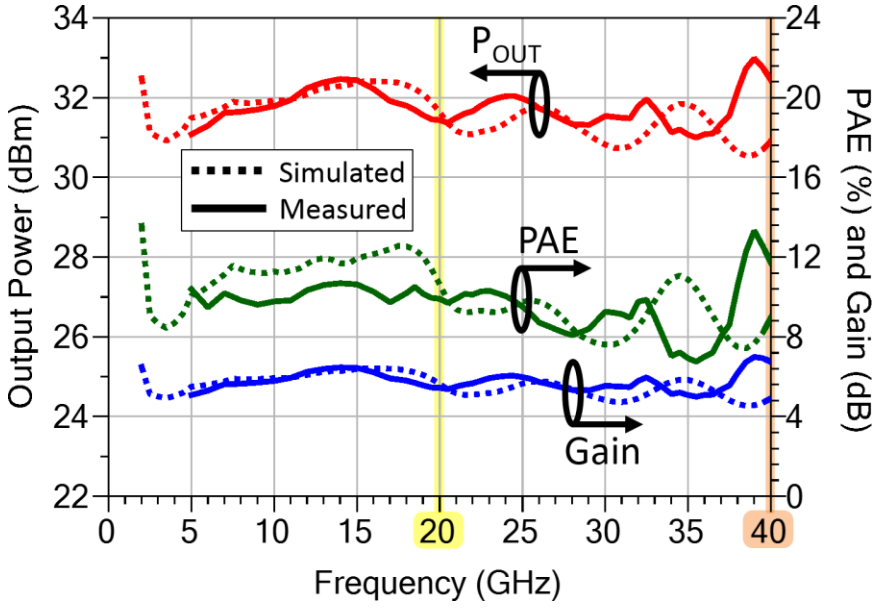


Figure 64 - NDPA large signal measurement results vs. frequency with 26 dBm source power

To further evaluate large signal performance, the swept source power measurement results at 20 GHz (mid-band, highlighted yellow in Figure 64) and 40 GHz (upper-band edge, highlighted orange in Figure 64) are shown in Figure 65 and Figure 66, respectively. The gain curves show some soft compression behavior in the lower regions of source power, and the output power curves indicate a saturated power greater than 2 W.

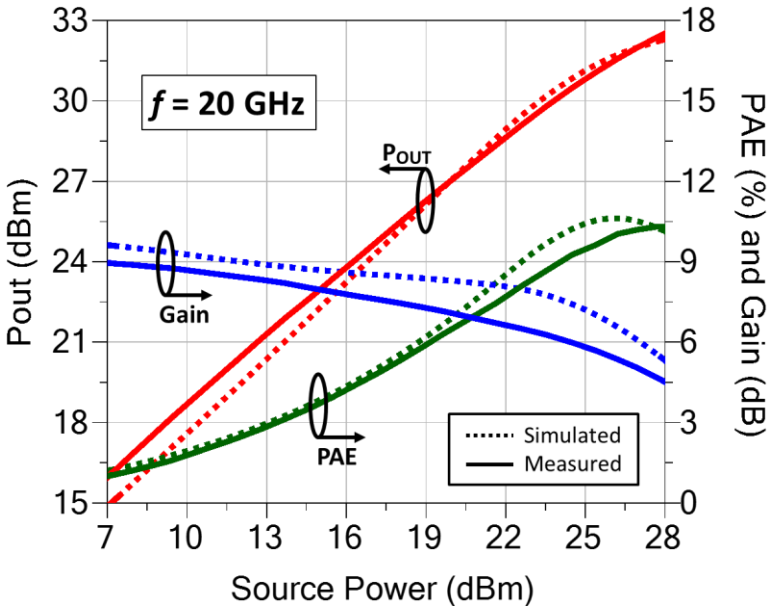


Figure 65 - Swept source power measurement results of the NDPA at 20 GHz

During measurements, the available range of source powers were limited depending on the operating frequency, as several different instrumentation amplifiers were required to measure such a wide bandwidth. For some frequencies, the maximum available source power was not enough to drive the NDPA to its peak PAE; this is evident in the 40 GHz results plotted in Figure 66. As seen therein, the PAE curve has not reached its highest value, indicating that higher PAE could be measured at an increased source power level.

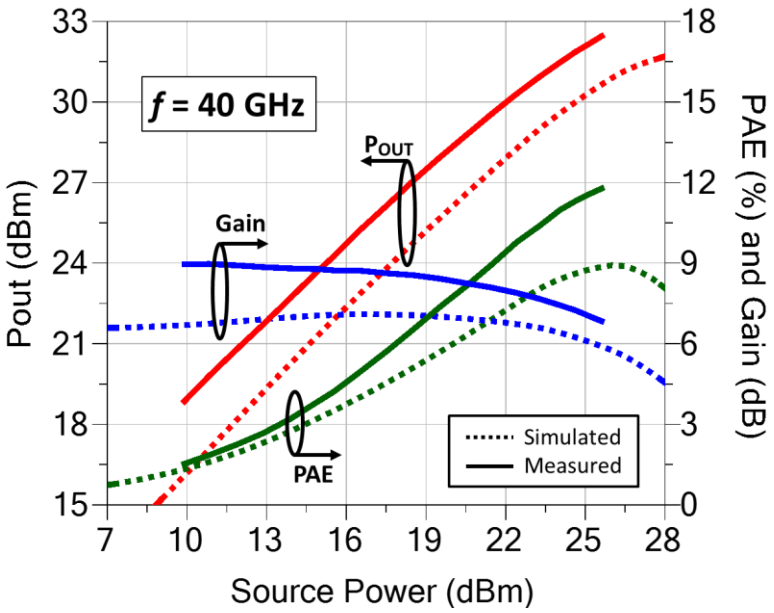


Figure 66 - Swept source power measurement results of the NDPA at 40 GHz

For comparison purposes, a summary of previously published results is found in Table 6. The highest output power achieved [56] corresponds to the publication with the lowest bandwidth in the table. While the work in [57] shows the largest bandwidth, that design was a low noise amplifier and therefore does not provide PAE or large signal gain data. Finally, the results in [31] and [58] are closest to the demonstrated performance, with this work exhibiting larger bandwidth and higher output power in a smaller die.

Table 6 - Comparison of Ultra-wideband GaN MMIC PAs

Ref (#)	L_{GATE} (μm)	Stages (#)	Frequency (GHz)		BW (%)	P_{OUT} (dBm)	PAE (%)	$Gain_{SAT}$ (dB)	Area (mm^2)
			Low	High	Relative				
[54]	**0.14**	**1**	**2**	**40**	**181**	**31 - 33**	**7 - 14**	**5 - 7**	**4.0**
[58]	0.2	1	2	32	176	NR* - 29	NR* - 16	NR* - 7.2	4.4
[30]	0.1	2	8	42	136	25.1 - 27	4 - 7	8 - 9.5	6.6
[31]	0.1	2	6	37	144	29.4 - 32.5	7 - 14	10 - 12.5	6.8
[56]	0.15	3	16	40	86	36.2 - 39.4	10 - 20	14.2 - 17.4	6.3
[57]	0.15	2	0.1	45	199	27.6 - 33	NR†	NR†	2.8

* Power measurements were provided only at 4 GHz in [58]; the broadband large-signal performance was not reported.

† The distributed amplifier design in [57] achieves 1 W over a broadband, but is focused on low noise and high linearity; therefore, the authors do not report PAE or saturated gain.

A GaN MMIC PA with output power greater than 1 W and nearly 10% PAE has been successfully demonstrated from 2 to 40 GHz for the first time. The presented measurement results agreed well with the simulation results. The design's ultra-wide bandwidth enables greater system design flexibility. To the best of the author's knowledge, the combination of bandwidth and output power performance of this GaN PA surpasses previously reported MMIC NDPA results.

The MMIC designs discussed in this chapter have focused on achieving improved PA performance at higher frequencies, over broader bandwidths, or both. The level of integration afforded by an MMIC implementation reduces both the component parasitics and sensitivity to assembly, so these circuits have shown better performance at higher frequencies in comparison to hybrid PAs. While MMICs are expensive to develop and require long lead times, they are economical in volume and can achieve the best results.

CHAPTER 5:

CONCLUSIONS

The power amplifiers presented here have explored different architectures with commercially-available GaN dies and newly-developed GaN devices manufactured on pre-released foundry processes. Various advancements in microwave power amplifiers have been achieved in the 1-40 GHz range. The design, fabrication, assembly, and measurement of innovative GaN PAs in both monolithic and hybrid implementations serve to augment our body of knowledge in wideband microwave amplifier circuitry.

Several HMIC implementations were successfully demonstrated using commercially-available GaN transistor dies in the following power amplifier designs:

- A multi-die amplifier was designed with GaN transistors on an AlN substrate using low-loss Wilkinson power dividers and eutectic die attachment to combat thermal effects. With a measured 38.1 dBm output power and 44% PAE at X band, this design established a baseline using the reactive/resistive matching technique.
- Multiple GaN transistors were used on an AlN substrate of an HMIC distributed power amplifier. This single-stage, 3-cell design included capacitive coupling, flip-chip bonding, and broadband impedance transformers to extend the achievable bandwidth. This HMIC PA demonstrated the widest bandwidth (0.4-8.0 GHz) for a distributed power amplifier in a hybrid implementation.

- In the final HMIC design, a GaN die was again used to obtain high power and high PAE over an ultra-wide bandwidth. The multi-substrate option allowed for optimization of the characteristic impedance ranges and material properties of each reactive/resistive matching network. This PA yielded the highest PAE (27–48%) and widest bandwidth (1.0-11.5 GHz) for a multi-watt hybrid design.

For amplifier designs at even higher frequencies, where parasitics become increasingly problematic, an MMIC implementation can enable the best possible performance from GaN technology. Several MMICs were successfully demonstrated in the following PA designs:

- An HEMT fabricated on a new 0.15 µm GaN-on-SiC process was characterized, and the measured data were used to create a new transistor model for 28 V operation. Then, a 3-stage MMIC PA was designed with the new model using the reactive/resistive matching technique. With a die size of 6.8 mm^2, this PA showcased the highest output power per die area for a 3-stage, C-Ku band MMIC design.
- Moving up in frequency, a 2-stage Ka band MMIC PA was designed and fabricated on a new 0.14 µm GaN-on-SiC process. With 4W of output power and 20% PAE in a 2.52 mm^2 die area, these results confirmed the efficacy of the reactive/resistive matching approach using an MMIC implementation for a Ka band PA design.
- Lastly, a NDPA design was implemented using the same 0.14 µm GaN-on-SiC process. For the first time, a GaN MMIC PA with output power greater than

1 W and nearly 10% PAE was successfully achieved from 2 to 40 GHz, surpassing previously reported MMIC NDPA results.

This research and previously-published studies indicate that better performance can be achieved by focusing on MMICs. However, market conditions and technical limitations demand continued improvement in HMICs as well. For any PA design, both frequency and bandwidth are important factors to consider when evaluating performance; device characteristics are poorer at higher frequencies, and impedance matching challenges are more difficult over wider bands. Compared to MMICs, hybrid implementations of broadband PAs are physically larger. Some wideband techniques, such as distributed PAs, require a comparatively larger die area to achieve similar gain and output power. As GaN-on-SiC technology continues to mature and its costs continue to fall, these devices will become more and more prevalent in both military and commercial applications.

5.1 Future Work

While the presented HMIC PAs have achieved state-of-the-art bandwidths using commercially-available GaN dies, these hybrid designs needed considerable area. To facilitate the integration of broadband hybrid PAs into a wider range of applications, future work should focus on size reductions of the hybrid matching networks. The microstrip impedance transformers in particular were quite long due to the bandwidths and transformation ratios required by the matching circuits. Optimized folding of the transformers, along with various other transformer taper curves, could be used to reduce the area or manipulate the aspect ratio of the board. Provided that the self-resonant

frequencies and losses of the component are acceptable, shunt lumped capacitors could be interconnected with inductive transmission lines for a reduced transformer footprint. If some decline in gain can be tolerated, a series gate resistor can raise the effective impedance required for a broadband match, thus relaxing the transformer's requirements. Alternatively, the choice of dielectric material could be guided by the in-substrate wavelength of the lowest frequency of interest. Keeping fabrication limitations in mind, the selected material could enable a shorter transformer at the cost of higher losses. This would be best suited for the input matching network, as increased losses in the output network should almost always be avoided.

Another area to further investigate for hybrid designs is a broadband balanced PA architecture. In this scenario, the transformer could be designed for a subset of frequencies in the higher range of the desired band. The layout would be smaller, but some reactance would be generated at the lowest frequencies in the desired band. This purposeful mismatch in the lower part of the band would help achieve the gain compensation necessary for a flat gain profile in a broadband PA. However, some microwave systems cannot handle high levels of reflection. To address the poor return loss created by the mismatch in the lower part of the band, two copies of the single-ended design could be combined into a balanced PA. The balanced architecture can be implemented with Lange couplers to achieve a roughly equal power split with a 90° phase shift over extremely wide bandwidths. This scheme would improve stability and return loss while nearly doubling the output power without increasing thermal degradation.

While GaN MMICs can achieve better performance than HMICs at higher frequencies, the typical lead time for GaN-on-SiC fabrication is longer than three months, and the total cost of a four wafer run can easily exceed $125,000. Using a combination of different MMIC dies with hybrid assembly techniques in the design of a PA should be explored to maximize the benefits and minimize the drawbacks of both implementations. Discrete GaN HEMT dies are readily available in the market, and other semiconductor processes need much shorter lead times. For example, the biasing and matching networks for a PA design could be manufactured using a passive GaAs process. This fabrication run would require less than half the time and a fraction of the cost in comparison to a GaN process. In addition, this method could increase the achievable frequency range and reduce variability in the matching network performance in comparison to an HMIC. However, interconnections from the GaAs matching networks to the pads of the GaN die would still be required. Because wirebonds would likely limit performance at higher frequencies, the lower parasitic inductance of flip-chip bonding makes it a more suitable interconnection method. The GaAs matching networks could be flip-chipped on top of the GaN HEMT die, which could use eutectic bonding for electrical and thermal grounding to a metal carrier. Either a bypass capacitor or another GaAs MMIC die could be mounted directly onto the carrier to provide bias connections for the flip-chipped GaAs matching network. Adjustments to the EM simulation environment should be the focus of initial analysis due to the proximity of a ground plane to the flip-chipped matching network. A passive GaAs MMIC with GaN HEMT die architecture may provide better performance than an HMIC

in a shorter timeframe and at a lower cost than a stand-alone GaN MMIC. Given these potential benefits, this architecture should be further investigated in future research.

APPENDIX A.

LOAD-PULL SYSTEM CONFIGURATION DETAILS

A.1 Passive load-pull Configuration with Power-sensor: System Setup

A high-frequency signal generator and an instrumentation power amplifier (if required) are configured to produce the desired source power at the plane of the DUT. An isolator is used at the output of the instrumentation amplifier to protect it from the high VSWR conditions created by the source tuner. It is often necessary to use a circulator with a high-power 50 Ω load due to the magnitude of the power reflected back toward the instrumentation amplifier. An attenuator is placed at the output of the load tuner to reduce the output power to an acceptable range for direct power sensor measurements. This attenuator should be sized to dissipate all of the output power of the DUT, plus a comfortable safety margin. Finally, a power sensor can be used to measure the power safely at that point in the system.

A.2 Passive load-pull Configuration with Power-sensor: Calibration

This measurement system is calibrated in three phases: tuner characterization, fixture de-embedding, and power calibration. Once the hardware is configured and the tuners have been initialized (i.e., set to a known home position), a network analyser is calibrated at the plane of the cable tips. The cables are then connected to the input of the source tuner and the output of the load tuner, and another calibration is performed at the plane of the DUT. For every desired load-pull measurement frequency, the impedance

tuners are individually stepped through their tuning ranges, and the resulting impedances are recorded. This in-situ characterization sequence accounts for the fixture losses between the tuners, and creates a mapping of each tuner's internal motor positions to the impedance values created at the plane of the DUT. The remaining input fixture losses are compensated by a 1-port S-parameter measurement of the *signal generator* | *power amplifier* | *isolator* | *bias tee* chain. The remaining output fixture losses are compensated by a 2-port measurement of the *bias tee* | *attenuator* chain, and a 1-port measurement of the power sensor. Once these data have been collected, the VNA is no longer required for load-pull measurement.

After all the hardware is reconnected, a THRU connection is made at the plane of the DUT, and the tuners are set to 50 Ω impedance. The signal generator is swept over a specified range of power at each desired frequency, and the power sensor measures the power at the output of the attenuator. This final calibration sequence determines the source power that is available at the plane of the DUT, and the system is now ready for large signal measurements.

A.3 Passive Load-pull Configuration with Vector-receiver: Calibration

Tuner characterization is accomplished as described in Appendix A.2, but additional fixture compensation is not required because the PNA-X is measuring the impedance at the DUT in real-time. The attenuators connected to the directional couplers must be sized such that the signal remains above the noise floor but does not drive the receivers into compression. Calibration of the receivers is completed with a 2-port

S-parameter calibration at the plane of the DUT. Power calibration is completed by a 1-port mechanical calibration at the output of the load tuner with a THRU connected at the DUT plane, followed by power sweeps at each desired frequency with the power sensor connected at the output of the load tuner. The power sensor is no longer required after the power calibration, and either the PNA-X or an external signal generator can be used to provide an input high-frequency signal. Once a 50 Ω termination with sufficient power handling capability is connected as the load, the system is ready to collect large signal data.

A.4 Active Load-pull Configuration: Calibration

Calibration of the MT-1000 active load-pull system begins with characterization of the loop amplifiers used for active signal injection. The control software for the MT-1000 system assists with the process by sweeping through the range of powers for each amplifier and setting the bounds for system operation. Next, a 2-port S-parameter calibration is required at the plane of the DUT for fixture compensation. Finally, a 1-port calibration is completed at the cable connected to the isolator of the loop amplifier on the load side. A power sensor is then connected to that cable, and power is swept and measured by the MT-1000 system to finish the amplitude calibration. After reconnecting the hardware, the system is ready for large-signal measurements.

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