Void Formation Study of Flip Chip in Package Using No-Flow Underfill

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***Abstract*—The advanced flip chip in package (FCIP) process using no-flow underfill material for high I/O density and fine-pitch interconnect applications presents challenges for an assembly process that must achieve high electrical interconnect yield and high reliability performance. With respect to high reliability, the voids formed in the underfill between solder bumps or inside the solder bumps during the no-flow underfill assembly process of FCIP devices have been typically considered one of the critical concerns affecting assembly yield and reliability performance. In this paper, the plausible causes of underfill void formation in FCIP using no-flow underfill were investigated through systematic experimentation with different types of test vehicles. For instance, the effects of process conditions, material properties, and chemical reaction between the solder bumps and no-flow underfill materials on the void formation behaviors were investigated in advanced FCIP assemblies. In this investigation, the chemical reaction between solder and underfill during the solder wetting and underfill cure process has been found to be one of the most significant factors for void formation in high I/O and fine-pitch FCIP assembly using no-flow underfill materials.**

***Index Terms*—Chemical reaction, flip chip, fine pitch, high I/O density, no-flow underfill, reliability, void formation.**

I. Introduction

FLIP CHIP in package (FCIP) technology has been widely used in high-performance device packaging solutions such as microprocessors, graphic devices, and high-speed memory applications for over a decade due to its advanced electrical, thermal, and form factor performance. Such performance requirements have narrowed the applicable assembly processes and notably underfill processes for high assembly yields with high reliability. It is well documented that underfills help to mitigate the effects of large coefficient of thermal expansion (CTE) mismatches between silicon chips and organic substrates [1]–[4]. The underfills reduce the strain on the solder joint interconnections, resulting in enhanced fatigue life for flip chip assemblies [5], [6]. Hence, underfill materials are used in flip chip assembly processes.

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The conventional assembly process for flip chip is based on a capillary flow underfill process. An alternate assembly process for low cost flip chip assembly is based on no-flow underfills [7]–[9]. The no-flow underfill materials containing fluxing agents and the underfills are deposited onto the substrate before a chip placement. Next, the chip is placed into the underfill causing squeeze flow of the underfill material during placement. The metallurgical solder interconnects are simultaneously achieved during reflow processing with underfill curing between a chip and a substrate. Therefore, several steps of conventional flip chip assembly processes can be eliminated using no-flow underfill material to save process time and cost compared to conventional capillary flow underfill process as illustrated comparatively in Fig. 1 [10].

Recently, a high-yield process was reported with high I/O density (over 3000 I/O) and fine pitch (down to 150 μm) for full area array FCIP interconnect structures comprised of high lead solder bumps with eutectic lead–tin solder interconnects using no-flow underfill [11]–[13]. The reported reflow process conditions were optimized for the high I/O, fine-pitch FCIP assemblies using five different no-flow underfill materials for robust electrical assembly yields. However, the developed high-yield assembly processes had a large number of voids which could cause reliability defects such as solder bridges and solder joint cracks possibly resulting early failure in thermal reliability [3], [14]–[16]. Typical underfill voiding patterns among solder joints are shown in optical micrographs of Fig. 2(a) and (b) of FCIP cross sections. In addition, a scanning acoustic microscopy (C-SAM) micrograph shown in Fig. 2(c) confirms multiple void areas in the underfill between the test FCIP and substrate assembled using no-flow underfill material.

The possible causes of void formation have been thoroughly investigated by several works. The research can be classified as studies of thermally induced voids and nonthermally induced voids. For thermally induced voids, Goenka *et al.* studied the determining factors affecting the formation and growth of voids in flip chip solder bumps using a theoretical investigation [17]. They also predicted the motion and coalescence of bubbles in flip chip solder bumps during the reflow process [18]. The source of void formation remained unidentified, and it was assumed that unidentified reactions caused bubble nucleation during the reflow process. Hurley *et al.* used experimental techniques to suggest a combined model for void formation with solder melting, underfill curing, and underfill volatilization in order to explain the mechanism of voiding in a flip chip device [19]. They suggested the void formation was mainly due to explosive boiling of uncured low-molecular weight components due to molecular components' volatilizations during reflow process. However, the experimental research could not inves-

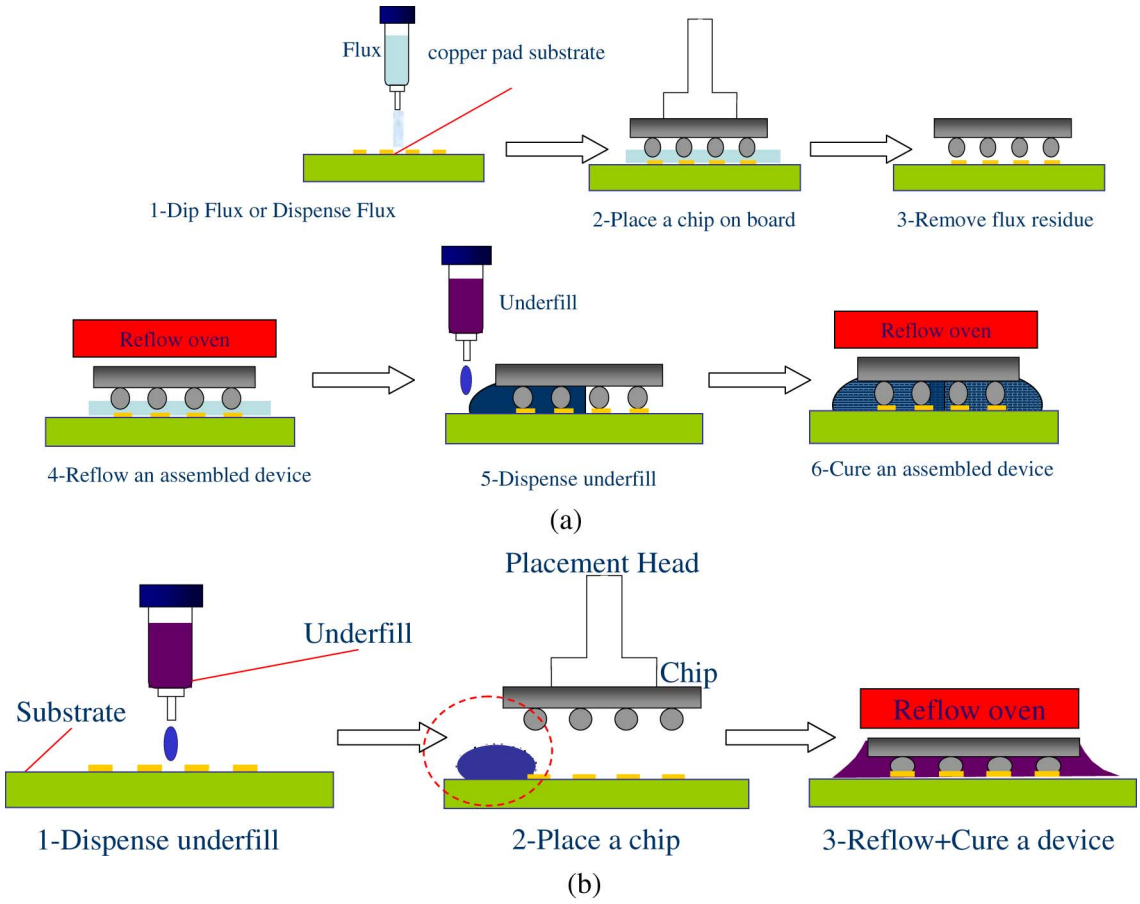


Fig. 1. Flip chip assembly process. (a) Conventional assembly process. (b) Hybrid no-flow assembly process.

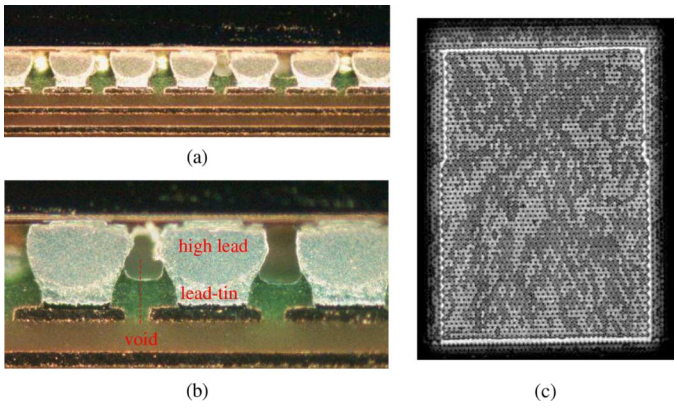


Fig. 2. Micrographs of FCIP built using no-flow underfill material under the reflow conditions of ramp rate: 2.1 °C/s, reflow time: 70 s, peak temp: 225 °C. (a) Cross-sectional view of flip chip solders joints (magnification: 100X). (b) Cross-sectional view of flip chip solders joints (magnification: 200X). (c) C-SAM analysis.

tigate the mechanism of uncured low molecular components formation, which generated the volatile out-gassing in flip chip assemblies.

Regarding nonthermal induced, Milner *et al.* studied the effect of substrate design and substrate features on flow induced void formation with commercial no-flow underfill materials [10]. They investigated the effect of pad geometry on the underfill void formation and found the underfill flow characteristics had a major effect. Colella *et al.* identified some significant factors influencing void formation in no-flow underfills including process design parameters such as underfill dispense pattern, placement parameters, and pad design [20].

These concepts of void formation and others will be included in this paper. This investigation of void sources and the understanding of the void formation mechanism are important steps toward reducing the underfill voiding in no-flow underfill assemblies. The ultimate goal is to establish a void-free assembly with high I/O, fine-pitch interconnects using no-flow underfill materials. Therefore, the effects of three plausible sources such as process conditions, material properties, and chemical reaction on the mechanism of voiding in FCIP assemblies are investigated using a systematic experimental approach with commercial no-flow underfills.

II. Experimental Approach

Three experiments were designed to investigate the plausible causes of void formation with FCIP using commercial no-flow underfills. These experiments were designed using the results from preceding studies with the effectiveness of cost and time due to a limited number of commercial FCIP TVs. A placement process void formation study, termed void formation study 1, was conducted to check the effect of underfill flow on the void formation. A material characteristics void formation study, termed void formation study 2, was performed to investigate whether one of the components in the no-flow underfill was

TABLE I
MATERIAL PROPERTY OF NO-FLOW UNDERFILL

Material property	Value
Glass Transition Temp. (Tg)	81 °C
Viscosity @ 25°C	3,100 cp
Flexural Modulus	2.6 GPa
Thermal Conductivity	0.18 W/mK
Coefficient of Thermal Expansion below Tg	190 ppm/°C
Cure condition	a standard SMT reflow incorporating at 150-170°C dwell prior to ramp up to reflow temperature

TABLE II
DESIGN MATRIX OF DOE FOR STUDY 1

Plasma pretreatment	Placement force	Placement dwell time
Plasma 1	Low (5N)	Low (0 sec)
Plasma 2	High (15N)	High (10 sec)

TABLE III
CONFIGURATION OF TEST VEHICLES USED IN THE STUDIES 1, 2, AND 3

Experiment	Test vehicle	Category	
Void formation study1	Test vehicle1-1	Bump material	97Pb-3Sn
		Chip size(mm)	< 10 x 10
		Bump count	3000 >
		Bump pitch	< 200μm
		Bump layout	Full area
		Substrate material	37Pb-63Sn
Void formation study2	Test vehicle 2-1	Die material	Glass cover
		Substrate size(cm)	1x1
		Substrate material	ENIG
		Underfill	No-flow underfill
	Test vehicle 2-2	Die material	Glass cover
		Bump material	37Pb-63Sn
		Substrate size(cm)	1x1
		Substrate material	ENIG
		Underfill	No-flow underfill
Void formation study3	Test vehicle 3-1 (FA10-4 substrate)	Die material	Glass cover
		Bond pad	copper
	Test vehicle 3-2 (FA10-4 die)	Bump material	37Pb-63Sn
		Passivation material	Nitride
		Chip size(mm)	10.16x10.16
		Bump count	1268
		Bump pitch	254 μm
		Bump layout	Full area
	Test vehicle 3-3 (FCIP substrate)	Die material	Glass cover
		Bond pad	37Pb-63Sn
	Test vehicle 3-4 (FCIP die)	Bump material	97Pb-3Sn
		Chip size(mm)	< 10 x 10
		Bump count	3000 >
		Bump pitch	< 200μm
		Bump layout	Full area

volatile and subsequently outgassed to form a void in the FCIP under reflow process conditions. A chemical reaction void formation study, termed void formation study 3, was conducted to understand how the no-flow underfill material reacted with the eutectic solder-plated substrate pads and the high lead solder bumps during the reflow process. This study also sought to find any possible chemical reaction that would cause underfill voiding.

A. Void Formation Study 1: Underfill Flow Induced Void Formation

The main objective of void formation study 1 is to determine the effects of the substrate pretreatment and chip placement process conditions on underfill flow as it impacts void formation in high I/O density, fine-pitch FCIP. The commercial no-flow underfill material, which showed the best performance in an assembly yield characterization, was selected for this void formation study 1 [12], [13]. The material properties of no-flow underfill used in this paper are shown in Table I. The process specifications of pretreatment, placement force, and placement dwell time are summarized in Table II. The placement force is defined as the applied force on a chip during the placement process, and placement dwell time is defined as the time the placed chip is held during a chip placement process. Since the chip placement speed, among the placement control parameters, was reported as an insignificant factor affecting underfill voids [20], the placement speed was not included in the design matrix for the void formation study 1.

Prior to the assembly process, all moisture was driven out of the boards with exposure to an isothermal environment at 125 °C for 3 h. This bake-out time was determined from a previous bake-out experiment and was sufficient to avoid moisture out-gassing of the boards [1], [21]. The plasma pretreatment for substrate surface cleaning was applied to the moisture-free FCIP test vehicle. The plasma 1 recipe was a plasma treatment using pure argon (Ar) for 10 min to remove contamination, and the plasma 2 recipe was a plasma treatment using 90% nitrogen (N_2) and 10% hydrogen (H_2) mixture for 10 min to activate the surface and change the surface energy.

The FCIP test vehicle (TV) 1-1 used in void formations study 1 is specified in Table III. The amount of underfill voiding was measured at different pretreatment and placement process conditions based on a full factorial design of experiment (DOE). According to the DOE shown in Table II, FCIP TVs were assembled using a commercial no-flow underfill and then were cured at an isothermal temperature of 130 °C for 1 h in a convection oven to eliminate the reflow process thermal impact on void formation. The impact of underfill flow on voids was determined by the area percentage of voids.

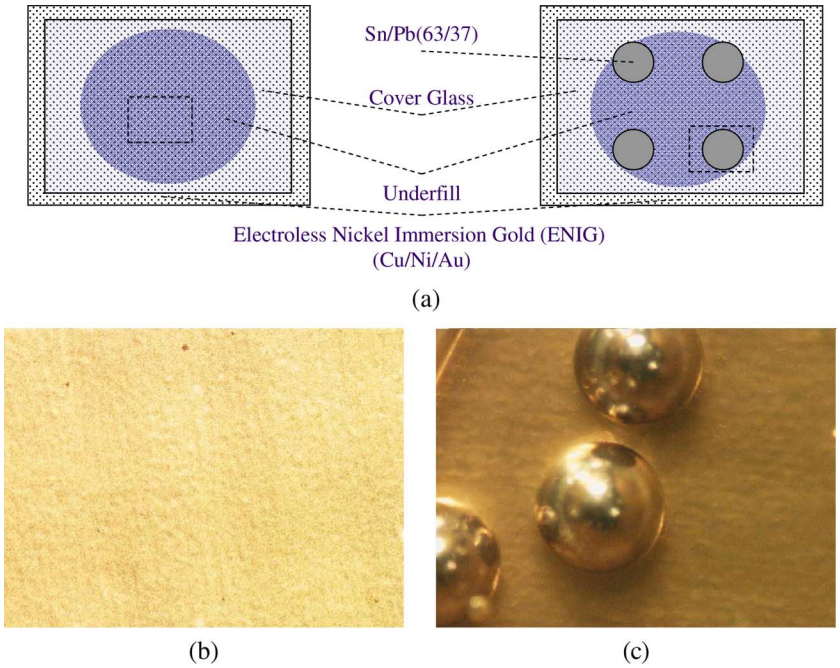


Fig. 3. Typical test vehicle in void formation study 2. (a) Schematic illustrations of TV2-1 and 2-2. (b) TV 2-1 without solder before heating. (c) TV 2-2 with solder bumps before heating.

B. Void Formation Study 2: Underfill Material Characteristic Void Formation

Void formation study 2 was designed to investigate whether the volatilization of uncured low-molecular weight components in no-flow underfill were the cause of voiding. The low-molecular weight components might be the main source for underfill voiding when exposed to higher temperatures above low molecular weight compounds boiling point during the reflow process.

Void formation study 2 used two test vehicles, designated test vehicle 2-1 and test vehicle 2-2. TV 2-1 consisted of a covered glass slide and an electroless nickel immersion gold (ENIG)-plated substrate. TV 2-2 consisted of a cover glass slide, four Sn/Pb (63/37) solder spheres, and an ENIG-plated substrate. A major difference between TV 2-1 and TV 2-2 is the presence of Sn/Pb (63/37) solder in the TV.

Prior to assembly, isopropyl alcohol (IPA) was applied to the surfaces of the test vehicles to clean them. After this cleaning process, the test substrates were baked at 125 °C for 3 h to avoid out-gassing from moisture on the substrate. Next, four solder spheres were placed on the ENIG substrate and a commercial no-flow underfill was dispensed onto the ENIG substrate. The solder spheres on the underfill deposited ENIG substrate covered with a glass cover slide is TV 2-2 as illustrated in Fig. 3. The presence of initial voids trapped by placing a glass cover on the underfill deposited substrate was inspected using an optical microscope. TV 2–3 assemblies used in this study had no voids induced by a glass cover placement as shown in Fig. 3.

The TV 2-1 and 2-2 were reflowed on a digital hotplate with a thermocouple attached to the ENIG substrate to measure the surface temperature of the TVs. Two test vehicles were placed next to a thermocouple coupon on the heated plate. The assembled TVs were reflowed from 100 °C preheating to 225 °C peak temperature which was held for 1 min to give enough time for solder wetting and underfill curing. The void formation behaviors of no-flow underfill material were observed during the reflow process under the optical microscope. Each test vehicle process was performed in replicates of three.

C. Void Formation Study 3: Chemical Reaction Void Formation Study

Void formation study 3 was designed to investigate the effect of chemical reactions between wetting molten solder and no-flow underfill using four test vehicles specified in Table III. The first test vehicle is TV 3-1 which consisted of a glass cover on an underfill deposited FA10-4 organic substrate with copper finished metallization as illustrated in Fig. 4(a). The stand-off gap height was controlled using polyimide taping of 200-μm thickness. Test vehicle 3-2 consisted of a glass cover and underfill deposited on a FA10-4 die as specified in Table III to confirm that Sn/Pb (63/37) has a strong impact on underfill voiding. Test vehicle 3-3 consisted of a glass cover and a FCIP organic substrate which had flip chip bond pads capped with a eutectic lead–tin (37–67) solder. A glass cover was put on the underfill deposited substrate with 200-μm standoff gap height using polyimide tape. Test vehicle 3–4 consisted of a glass cover on the underfill deposited FCIP die as specified in Table III to investigate the effect of high lead solder on underfill voiding at the lead–tin (37–67) solder reflow process condition. All four TVs were reflowed at the assembly process conditions specified in Table IV, which was used for achieving the high electrical yields with a flip chip assembly consisting of high lead solder bumps mounted on eutectic solder caps.

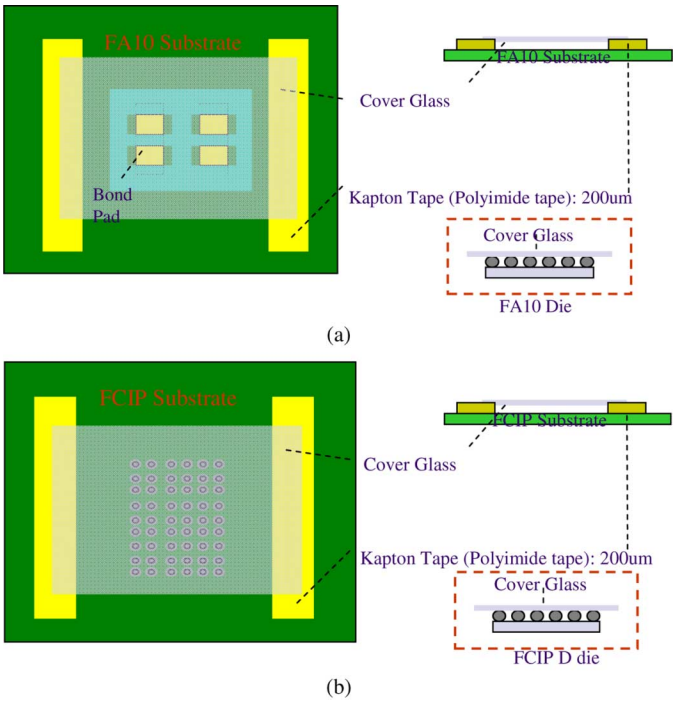


Fig. 4. Configuration of test vehicle for void formation study 3. (a) FA10-4 substrate TV (TV3-1) and die TV (TV3-2). (b) FCIP substrate TV (TV3-3) and die TV (TV3-4)

TABLE IV
REFLOW PROFILE FOR HIGH YIELD ASSEMBLY

Ramp rate	Soak temperature	Soak time	183°C >	Peak temperature
2.1 °C/s	140 ~ 170 °C	50sec	70 sec	225 °C

III. RESULTS AND DISCUSSIONS

A. Void Formation Study 1: Underfill Flow-Induced Void Formation

Fig. 5(a) shows a typical micrograph of a no-flow underfill voiding pattern among solder bumps under a particular reflow condition observed by planar cross-sectional analysis. Fig. 5(b) shows a typical scanned micrograph of no-flow underfill voiding using C-SAM. CSAM was used for quantitative analysis to compute the percentage of underfill voiding at different reflow conditions using image processing techniques. Post processing, the TVs were scanned using C-SAM, and an example scanned C-SAM image is shown in Fig. 6(a). The figure shows a grayscale pattern, where the darker gray and white regions indicate the regions of TVs containing underfill voids. The boundary of voiding area is shown in Fig. 6(b) as detected on the converted image. The image was converted to black and white using a commercial image processing program for further analysis. At the same time, the area of underfill voiding in the FCIP TV was calculated using the software, where white regions indicate regions of voids in the FCIP as shown in Fig. 6(c).

Percent area voiding is defined as the percentage of the void area over the area of the die. The percent area voiding of the FCIP TV using no-flow underfill at each process condition

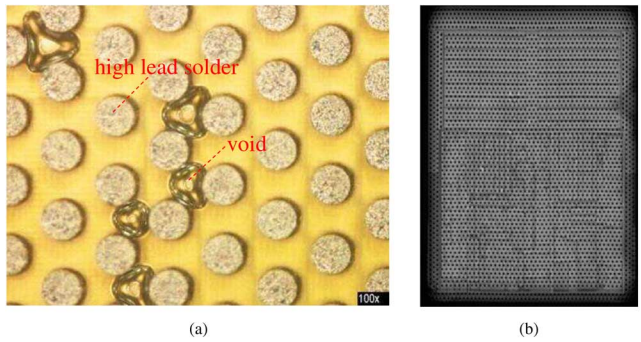


Fig. 5. Typical micrographs of an FCIP test vehicle built using no-flow underfill. (a) Planar cross-sectional micrograph of an FCIP. (b) C-SAM analysis.

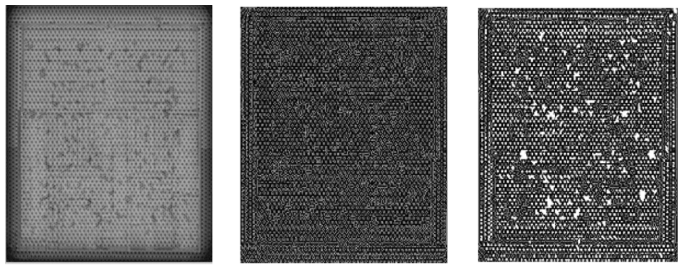


Fig. 6. Image processing for voids detection from C-SAM. (a) Original image. (b) Boundary of voids. (c) Detected voids.

TABLE V
RESULT OF VOID FORMATION STUDY 1

Order	Plasma pretreatment	Placement force	Placement dwell time	Voids (%)
1	1	1	2	0.385
2	2	1	1	0.570
3	2	2	2	0.487
4	2	2	2	0.706
5	2	1	1	0.000
6	1	2	1	0.071
7	1	2	1	0.000
8	2	2	2	0.702
9	1	1	2	0.215
10	2	1	1	0.567
11	1	2	1	0.060
12	1	1	2	0.432

was collected as shown in Table V. The percent area voiding of the FCIP ranged from 0.000% to 0.706%. analysis of variance (ANOVA) technique was applied to the collected data in void formation study 1 to determine the magnitude level of each process factor to underfill void formation [22]. The sign "+" represents the intensity of process factor on the underfill voiding. Thus, the magnitude of factors on underfill voids is described in Table VI according to statistical analysis. Besides, the primarily impacted plots, as shown in Fig. 7, indicate the relative effect of each design parameter on voiding for the no-flow underfill.

As a result, the plasma cleaning process might be a statistically moderate factor influencing the amount of underfill voiding. Placement dwell time appeared as a notable factor on the amount of underfill void formation. Placement force did not appear to be a major factor in void formation. A high value

TABLE VI
SUMMARY OF VOIDING RESULTS SIGNIFICANCE

	cleaning	force	time
p-value	++	0.887	+

\+ = <0.10 ANOVA p-value
++ = <0.05 ANOVA p-value
+++ = <0.01 ANOVA p-value

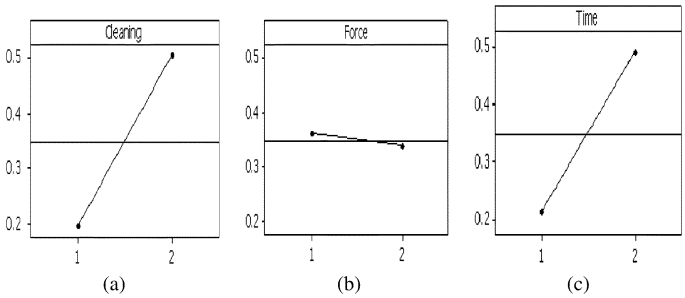


Fig. 7. Main effect plots on void. (a) Cleaning versus void. (b) Force versus void. (c) Dwell time versus void.

for placement dwell time increased the amount of void area. A detailed consideration of the results is necessary to explain the mechanism behind the statistical analysis. For example, the plasma 1 recipe using Argon gas is commonly used to remove contamination or micro-size particles on the surface, eventually achieving smoother surface. Therefore, TVs exposed to plasma 1 have fewer voids due to the laminar flow of underfill. On the contrary, the 90% nitrogen and 10% hydrogen mixture, used widely in the package industry as pretreatment, was selected for the plasma 2 recipe. Nitrogen was employed to promote the performance of wetting by activating the surface and hydrogen is for etching process. Thus, the roughness of TVs exposed to plasma 2 might be increased preventing the flow of underfill due to typical hydrogen etching characteristics thus causing an increased number of voids [23].

The effect of placement dwell time on voids can be explained only with further research. The current void formation study was designed narrowly to identify whether the underfill flow affects a large number of voids in high I/O, fine-pitch FCIP assemblies not subject to a reflow process.

The percentage of voiding induced by underfill flow was lower than 0.0706%, as shown in Table V, whereas the current high yield assembly process resulted in approximately 65% voiding [12]–[14]. Thus, the underfill flow is not believed to induce the high percent area of void without a thermal effect such as the reflow process. The underfill flow-induced voiding pattern (as an example shown in Fig. 6) which formed among solders is not desirable for long-term reliability [20]. That is, the void percentages between high and low parameter levels in all three cases were not sufficient to account for the process induced voids. Hence, underfill flow-induced void design parameters generally have only minor effects on underfill voiding for the configuration studied.

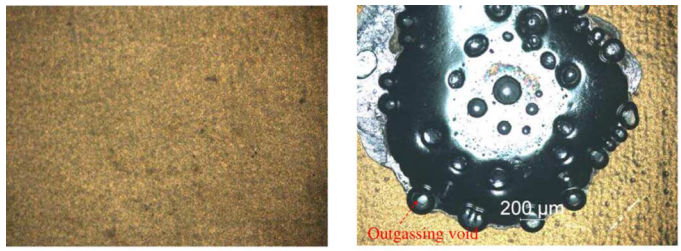


Fig. 8. Typical micrographs of void formation study 2. (a) TV 2-1 without solder after heating. (b) TV 2-2 with solder bumps after heating.

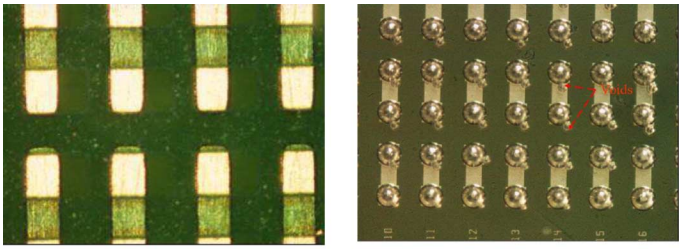
B. Void Formation Study 2: Effect of Underfill Material Characteristic on Void Formation

The no-flow underfill was evaluated in void formation study 2 to investigate whether an underfill material has a volatile component which can potentially expand creating voids during the reflow process. Furthermore, the effect of solder melting on underfill voiding was examined as shown in Fig. 8. Two micrographs of void formation study 2 compare TV 2-1 and TV 2-2 comparatively after reflow process (see Fig. 8). Test vehicle 2-1, consisting of a glass cover slide on the underfill deposited substrate without lead–tin solder, did not show any voids after the reflow process. A thermally activated volatile component such as a low molecular weight polymer component would tend to out-gas once a critical temperature is reached. Voids should appear in test vehicle 2-1 after the reflow process in order to validate the hypothesis that some uncured volatile components out-gas due to exposure of the components to high temperature above the volatile components' boiling point. Therefore, the result using TVs 2-1 indicated that the reflow process has a process window for any low-molecular weight components such that they fully participating in the underfill cure process and do not out-gas.

On the contrary, a significant amount of underfill voiding was detected around a merged Sn/Pb (63/37) solder sphere on the TVs 2-2, which had four small Sn/Pb (63/37) solders on the underfill-deposited ENIG substrate. The size of the underfill voids around the solder spheres was observed to be an average of average 200 μm. Thus, the potential existence of low-molecular weight volatile components within the no-flow underfill material is not the sole source for underfill voids. Solder ball reflow is required for voiding to occur. The reflow process of solder balls during the no-flow underfill material is necessary for underfill voiding to occur near Sn/Pb (63/37) solder based on void formation study 2. That is, this void formation study indicated that the presence of voids was strongly dependent on the presence of solder within the no-flow underfill material during the reflow process.

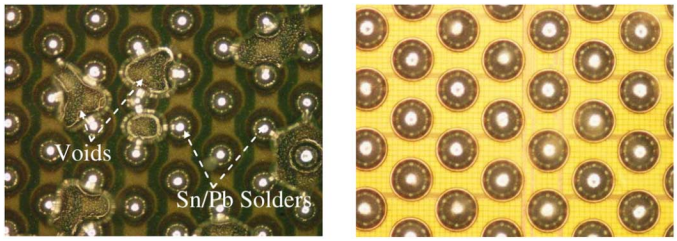
C. Void Formation Study 3: Effect of Chemical Reaction on Void Formation

The test vehicles were assembled and the assembled parts were inspected via a microscope to confirm void-free assemblies in the TV prior to the reflow process. The assembled TVs were reflowed in a convection reflow oven at the controlled reflow process conditions specified in Table IV, selected based on yielding a robust interconnect for high lead solder bumps and



(a) (b)

Fig. 9. Micrographs of FA10-4 TV. (a) TV3-1, FA10-4 substrate. (b) TV3-2, FA10-4 die.



(a) (b)

Fig. 10. Micrograph of a FCIP substrate and die. (a) TV3-3, FCIP substrate with lead-tin solder cap. (b) TV3-4, FCIP die high lead solder bumped on.

an eutectic solder cap FCIP test vehicle system using no-flow underfill materials.

After the robust reflow process was completed, TV 3-1, which consists of a glass cover slide on the no-flow underfill deposited FA10-4 substrate, did not show any voids as shown in Fig. 9(a). However, the optical micrograph of TV 3-2, which consists of a glass cover slide on no-flow underfill deposited a FA10-4 die, showed voids around every eutectic Sn/Pb (63/37) solder bump as shown in Fig. 9(b).

Furthermore, a large number of voids on the TV 3-3 (FCIP substrate), which consists of a glass die and organic substrate with eutectic Sn/Pb (63/37) solders bonding pads, was observed as shown in Fig. 10(a). However, no voids were detected on the TV 3-4 (FCIP die), which consists of a glass cover slide on the high lead solder balls bumped FCIP die as shown in Fig. 10(b) after the reflow process. The reflow process conditions were mainly designed for eutectic Sn/Pb (63/37) solder wetting for the interconnection of the high lead solder bumps (Sn/Pb-3/97) on the eutectic caps (Sn/Pb-63/37). Therefore, the evidence of void formation study 3 demonstrates that the interaction of solder melting, no-flow underfill fluxing, and no-flow underfill curing has a strong effect on underfill voiding.

Indeed, solder melting is influenced by the flux agents in a no-flow underfill. The fluxing agent removes the oxide layer on both surface of the solder bumps and metal pads during the reflow process. Such fluxing capability mainly depends on the functionality and concentration of fluxing agents, and surface finished material status. In general, carboxylic acid is used for organic acid based fluxing agents in no-flow underfills, as it simultaneously reacts with the solder oxide and with the epoxy ring during the underfill cure process as shown in Fig. 11 [25].

Similarly, the organic acid-based fluxing agents in the no-flow underfill participate in underfill curing without eutectic solder

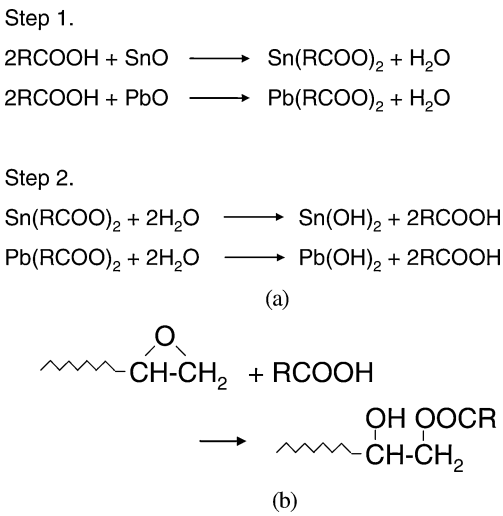


Fig. 11. (a) Possible fluxing mechanism for organic acid-based fluxes and (b) their reaction with oxirane of epoxy resins.

melting. If solder is present during the no-flow underfill cure process, the fluxing agents simultaneously participate in the underfill curing process and the fluxing function near the eutectic solder balls. In other words, some amount of fluxing agents directly participate in underfill curing, and some portion of the fluxing agents, which remove oxidation around solders bumps, are restored to fluxing agents. Then the restored fluxing agents around solder bumps are exposed to temperatures above their boiling temperature due to solder melting endothermic reaction and are less likely to participate in the underfill curing process due to partially cured underfill material. The endothermic reaction results in heat energy concentration around the solder surface. The concentrated heat energy instantly provides to the potential nucleation sites causing underfill voiding during the reflow process using high reflow parameters for high yields with high I/O density, fine-pitch flip chips.

IV. Conclusion

This paper investigated the plausible sources of underfill voiding during the assembly process development of a high I/O density, fine-pitch flip chip assembly. This paper used several specially designed test vehicles and a commercial no-flow underfill material to study the voiding process. Structured experimentation focused on the effects of reflow process parameters, the no-flow underfill materials, test vehicle material, the chemical reaction between the solders and no-flow underfill, and no-flow underfill cure. The results of the void formation studies showed that the chemical reaction between the eutectic lead–tin (Pb37/Sn63) solder interconnection system and no-flow underfill during solder reflow process is a main cause of underfill voiding in the FCIP assemblies. In addition, the studies have shown that the placement process parameters such as pretreatment on the substrate, placement force, and placement dwell time contribute little to the amount of void formation.

The findings in this study contribute to a fundamental understanding of void formation in the no-flow underfill and can be

used to establish design guidelines for the development of advanced no-flow underfill materials systems and for the development of high I/O, fine-pitch flip chip assembly process for high-yield and long-term thermomechanical reliability.

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