Final Report for HYPRES, Inc.

"Cryogenic High-Gain, Wideband, SiGe HBT Digital Amplifier"

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1 Introduction

In order to interface the superconducting electronics (SCE) based on rapid single flux quantum (RSFQ) logic with room temperature electronics, which needs much higher switching energies than offered by SCE, and without significant degradation in the signal to noise ratio (SNR), an intermediate cooled (e.g., 77K) amplifier was proposed based on SiGe HBTs [1]. The performance of SiGe HBTs improves with cooling [2,3] and hence SiGe is ideally suited for this application. The output data rate from the SCE is between 0.2 Gbps and 20 Gbps, and therefore the analog bandwidth of the intermediate amplifier needs to be at least 15 GHz [4]. Since IBM's 120 GHz peak f_T process (7HP) should provide the required bandwidth [5], we initially used IBM's 7HP SiGe process for the wideband amplifier design, but have also completed secondary designs using IBM's 8HP SiGe technology, both of which are described.

1.1 Accomplishments

- We have designed, simulated, and taped-out multiple versions (7HP + 8HP) of the SiGe digital amplifier circuit, along with associated debug circuits.
- These SiGe digital amplifier circuits display usable bandwidth in excess of 20 GHz and mid-band gain >50 dB upon full post-layout parasitic simulation, in principle meeting the required specifications.
- Preliminary 7HP/8HP dc and ac transistor measurements at low temperature on transistors at low temperatures were performed to quantify the device-level performance of the respective technologies.
- The 7HP SiGe amplifier was fabricated, and functionality has been demonstrated, with complete characterization on-wafer at Georgia Tech down to cryogenic temperatures.
- The 7HP SiGe amplifier die were delivered to Hypres for placement in their package and measurement inside their superconducting system application.
- The 8HP version of the amplifier was designed and is still in fabrication. It will be tested at a later date.

2 Circuit Design & Layout

2.1 7HP Version #1

The wideband digital amplifier contains three differential amplifier cells with transimpedance loads. Transimpedance load has very low input impedance, thus suppressing the Miller effect and also causing gain peaking, thereby improving the bandwidth [6]. An emitter-follower precedes each of the gain stages. The input is matched to 50-Ohm. The output buffer is a simple emitter follower stage capable of driving a 50-Ohm load. Due to the 50-Ohm matching at the output the total power consumption is high in the output buffer. This power consumption can be dramatically minimized by matching the output of the amplifier to the input of the succeeding ECL logic, which has much higher input impedance.

The three stages of the amplifier are DC-coupled to each other and to the I/O buffers, enabling cascading of these stages. The overall mid-band gain of the amplifier is ~43 dB. We do plan to enhance the gain to obtain ECL voltage levels at the output in our future designs. Fig. 1 shows the representative schematic of the three stages of the amplifier. Fig. 2 shows the layout of the overall design. We have also included individual stages of the amplifier in this tape out for further analysis.

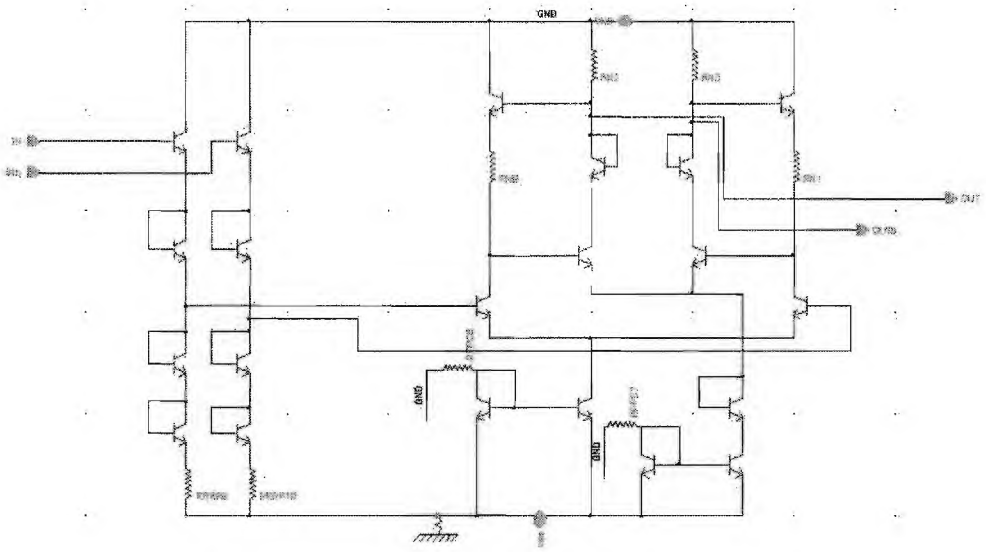

Fig. 1. Schematic of stages 1 and 3 of the amplifier.

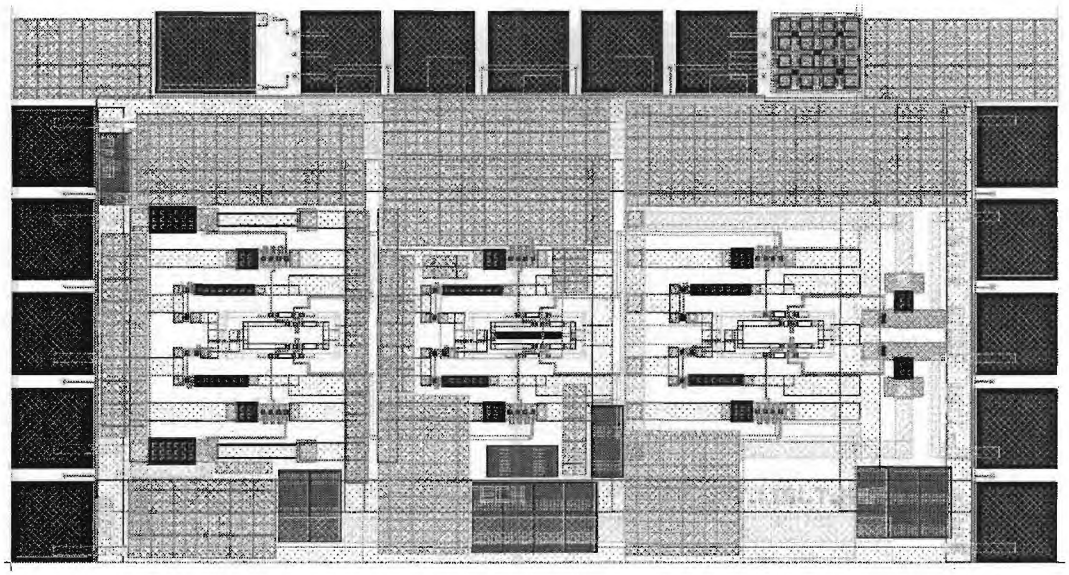

Fig. 2: Amplifier layout showing all 3 stages.

2.2 7HP Version #2

In order to improve the overall performance of the amplifier from the previous design the output buffer was changed from a simple emitter follower stage to a differential pair, which has a better gain and also introduces lesser gain peaking than an emitter follower [7,8]. An extra emitter follower stage was added in between the stages to improve the isolation between stages [9]. The design of the core stages were maintained the same as the previous design. Driving a 50-ohm load has limited the extent to which we can decrease power dissipation. Right now the power dissipation stands at about 0.3W/channel (slightly higher than design #1).

The layout of all the stages of the amplifier has been dramatically shrunk from the previous design (Fig. 3). While the core amplifier area has been reduced dramatically, the total area is still limited by the size of the bonding pads. The total area of the amplifier has been reduced from 0.87x1.67 mm^2 to 0.975x1.125 mm^2. The pos-parasitic circuit simulation results are summarized in Table 1.

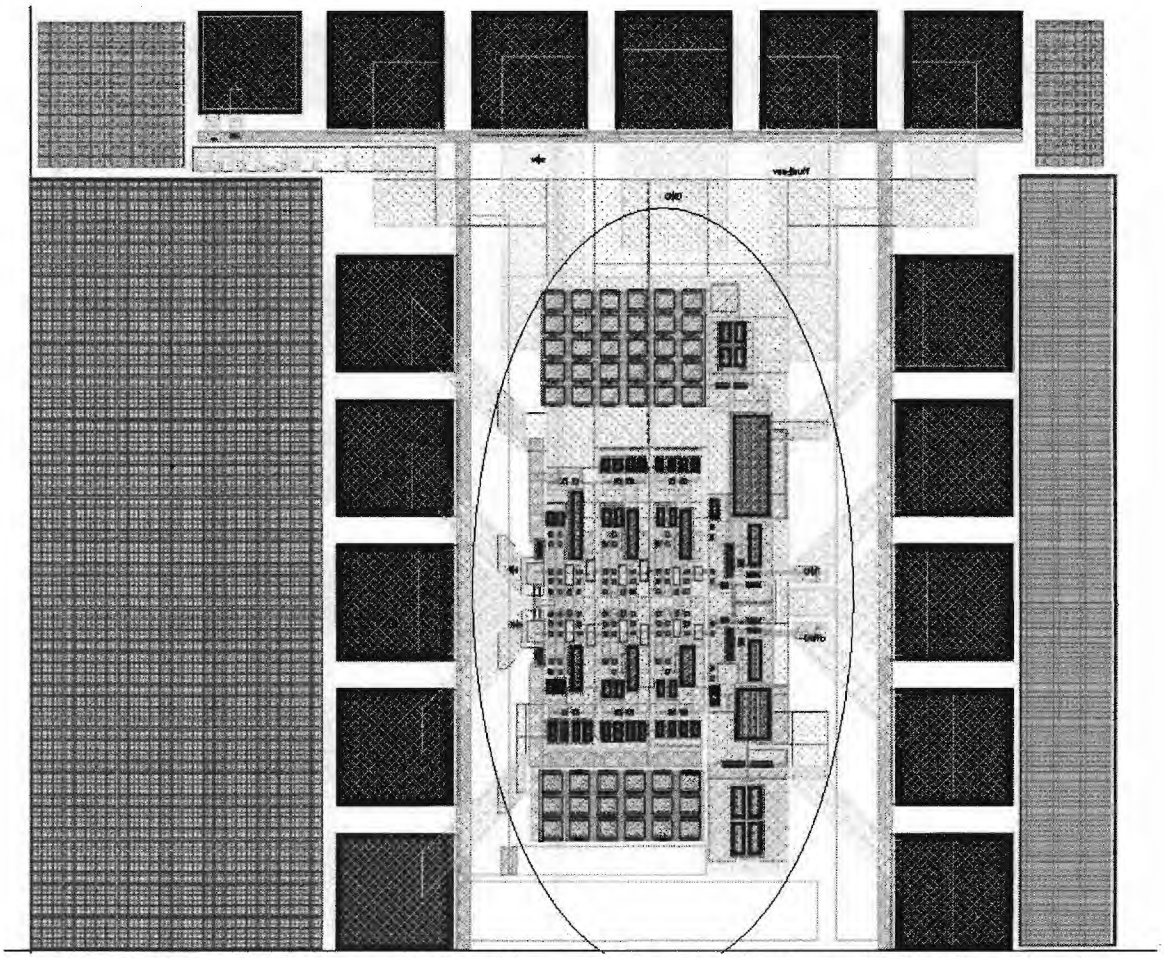

Fig. 3: Layout of the new design (the amplifier core is shown inside the ellipse).

Table 1: Post parasitic extraction simulation results (all at room temperature).

Parameter	August run	November run

Bandwidth (-3 dB)	>19 GHz	>21 GHz
Power consumption	<0.25 W/channel	< 03 W/channel
Small–signal mid-band gain	>43 dB	>52 dB
Input/output match	50-ohm	50-ohm
Supply voltage	-5V	-5V
Differential output voltage	>300mV	>500mV
Max. differential input voltage (for linearity)	<4mV	<4mV

2.3 Circuit Measurement Results

The post-fabricated 300K measurement results of this SiGe 7HP amplifier are summarized in the following paper [10]. Die have been delivered to Hypres for measurements at cryogenic temperatures.

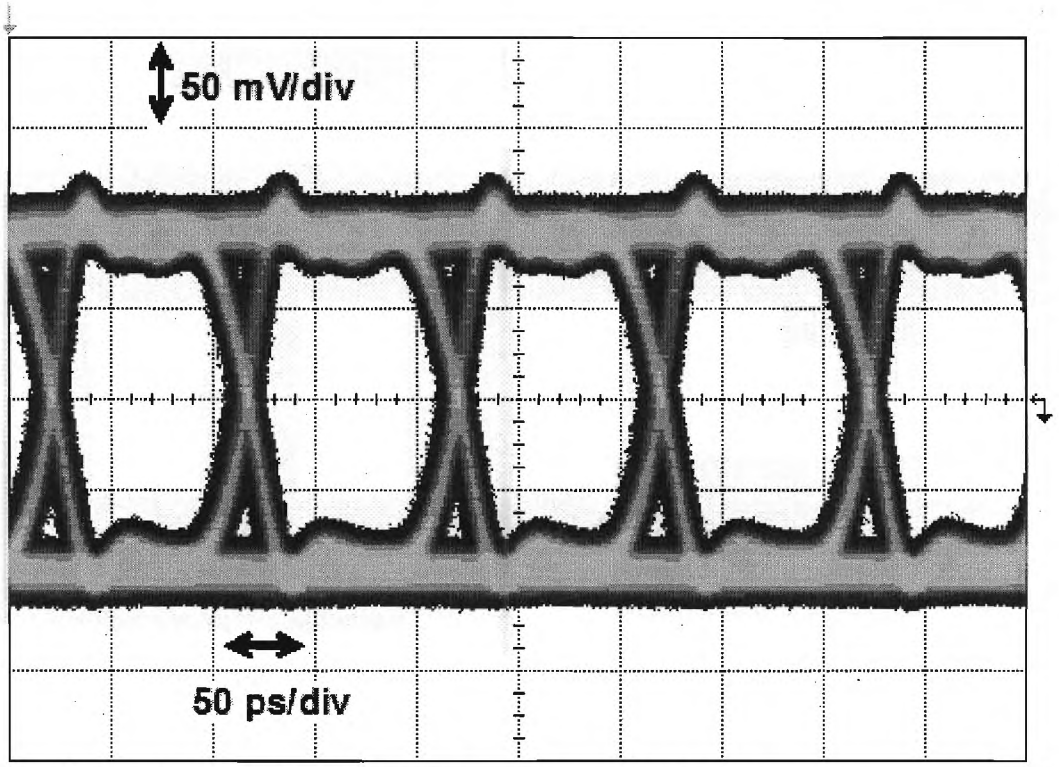

Fig. 4: Eye diagram of the amplifier operating at 10 Gb/s (our measurement limit).

Table 2: Measured 300K performance of the SiGe amplifier.

SUMMARY OF THE SIGE LIMITING AMPLIFIER CHARACTERISTICS

S_{21} Bandwidth (3dB)	> 24 GHz
Differential Gain (S_{21})	> 42 dB
S_{11}, S_{22} 0-30 GHz	< -10 dB
Differential Output Voltage	~370 mV_{pp} at 50 Ω Load
Simulated Sensitivity	< 12 mV_{pp} at BER = 10^{-9}
Power supply	-5 V
Power consumption (including output buffer)	~550 mW
Die Area	0.945 × 0.720 mm^2

2.4 8HP Version #1

As a follow-on demonstration, IBM SiGe 8HP (@00GHz HBTs) was used to design a 40G limiting amplifier with >30dB gain, with and without automatic offset correction, and featuring alternate output buffer schemes (Cherry-Hooper and simple diff pair) with a < 900uVrms input referred noise. That circuit is still in fabrication.

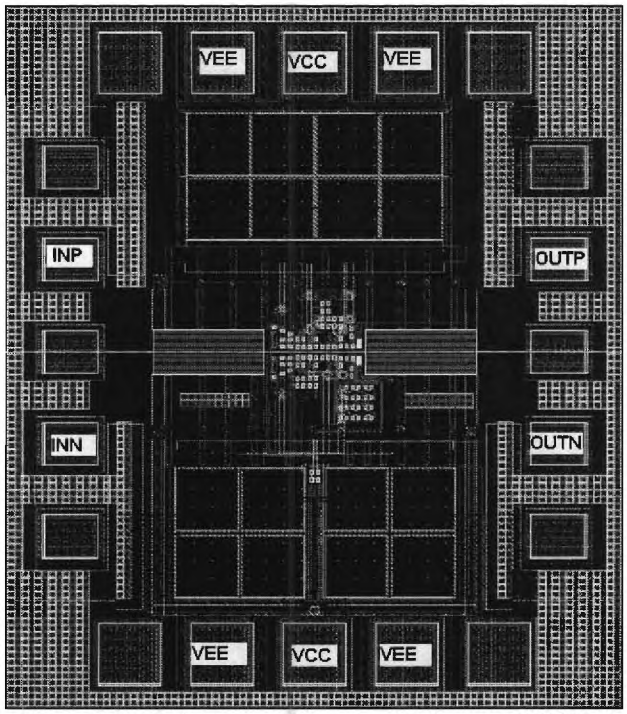

Fig. 5: 8HP layout of the 40 Gb/sec amplifier.

3 Transistor Characterization at Cryogenic Temperatures

Full ac/dc device characterization of 7HPand 8HP SiGe HBTs have been completed during this project. SiGe HBT with device geometry of 0.2 x 2.56 μm^2 was chosen as the representative device of this technology generation. Various dc measurements were made across the temperature range of 300K to 82K on this device. Fig. 4 shows the Gummel characteristics of this device from this technology at 300K and 82K with collector-base voltage (V_{CB}) set to 0V. The gradient of the collector current (or transconductance) increases with cooling, making the device attractive for high gain analog applications at low temperatures.

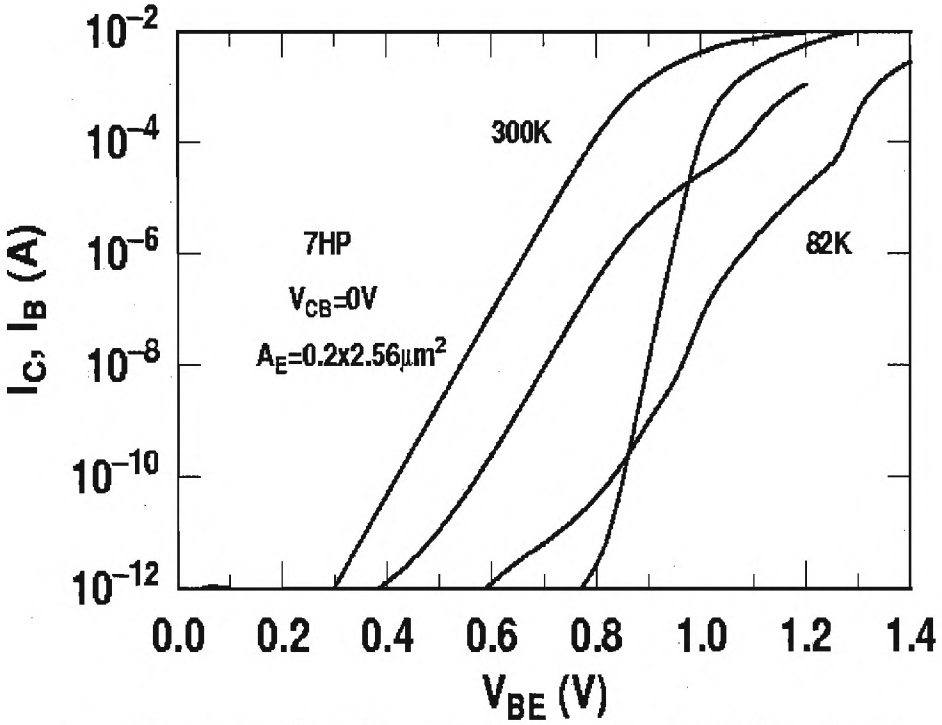

Fig. 4: 7HP SiGe HBT Gummel characteristics at 300K and 82K.

The current gain (β) increased monotonically with cooling. The peak beta at 82K was more than 1900 (Fig. 5). The peak cut off frequency (f_T) at 85K was in excess of 120 GHz (Fig. 6).

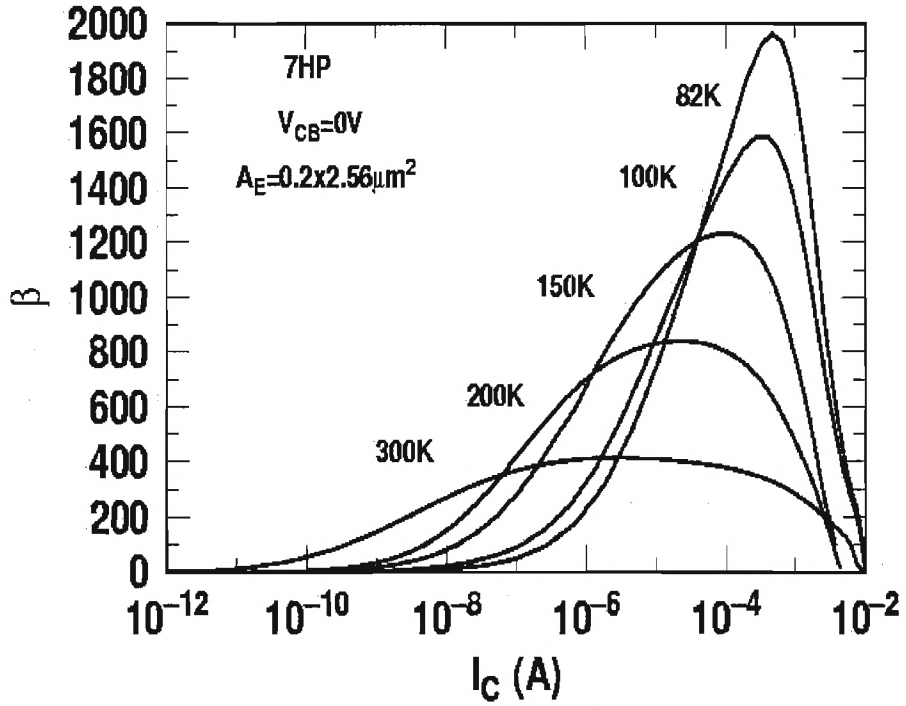

Fig. 5: 7HP current gain as a function of collector current density.

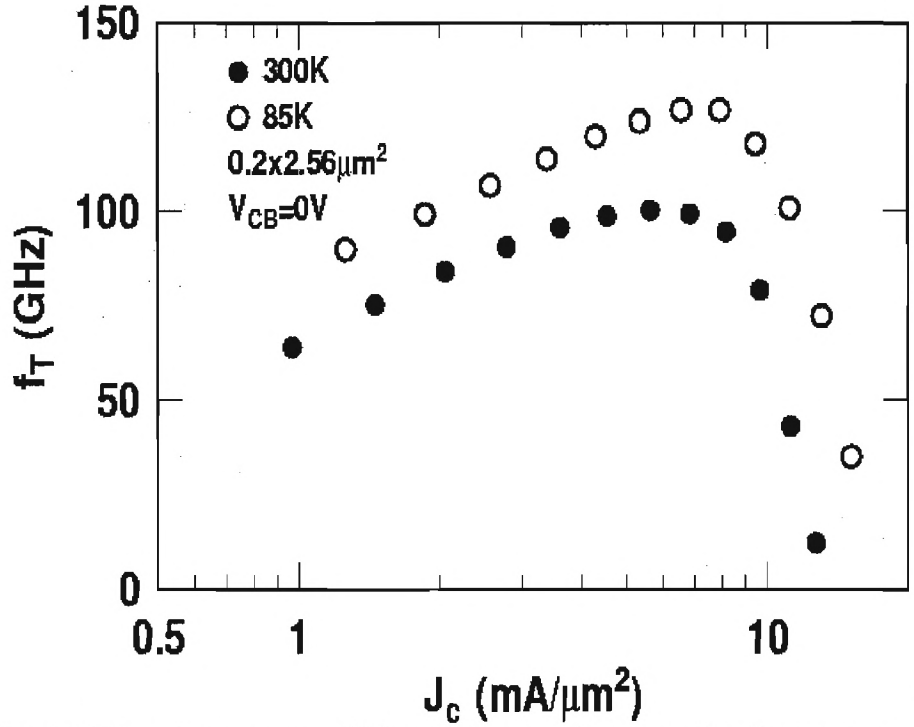

Fig. 6: 7HP unity gain cut-off frequency as a function of collector current.

References

[1] D. Gupta, A.M. Kadin, R.J. Webber, I. Rochwarger, D. Bryce, W. Hollander, Y. Yim, Channakeshav, R.P. Kraft, J.-W. Kim, and J.F. McDonald, "Integration of

Cryocooled Superconducting Analog-to-Digital Converter and SiGe Output Amplifier", *IEEE Trans. Appl. Supercond.*, vol. 13, pp. 477-483, June 2003.

[2] J. D. Cressler, E. F. Crabbé, J. H. Comfort, J. Y.-C. Sun, and J. M. C. Stork, "An epitaxial emitter-cap SiGe-base bipolar technology optimized for liquid-nitrogen temperature operation," *IEEE Electron Device Lett.*, vol. 15, pp. 472-474, November 1994.

[3] J. D. Cressler, E. F. Crabbé, J. H. Comfort, Johannes M. C. Stork, and J. Y.-C. Sun, "On the profile Design and Optimization of Epitaxial Si- and SiGe-Base Bipolar Technology for 77 K Applications – Part II: Circuit Performance Issues," *IEEE Transactions on Electron Devices*, vol. 40, pp. 542-556, March 1993.

[4] M. Neuhauser, H.M. Rein, and H. Wernz, "Low-noise, high-gain Si-bipolar preamplifiers for 10 Gb/s optical links–Design and realization," *IEEE J. Solid-state Circuits*, vol. 31, no. 1, pp. 24-29, 1996.

[5] A. Joseph, D. Coolbaugh, M. Zierak, R. Wuthrich, P. Geiss, Z. He, X. Liu, B. Orner, J. Johnson, G. Freeman, D. Ahlgren, B. Jagannathan, L. Lanzerotti, V. Ramachandran, J. Malinowski, H. Chen, J. Chu, M. Gordon, P. Gray, R. Johnson, J. Dunn, S. Subbanna, K. Schonenberg, D. Harame, R. Groves, K. Watson, D. Jadus, M. Meghelli, and A. Rylyakov, "A 0.18 um BiCMOS technology featuring 120/100 GHz fT/fmax HBT and ASIC compatible CMOS using copper interconnect," Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp. 143-146, 2001.

[6] K. Ohhata, T. Masuda, E. Ohue, and K. Washio, "Design of a 32.7-GHz Bandwidth AGC Amplifier IC with Wide Dynamic Range Implemented in SiGe HBT," *IEEE J. Solid-state Circuits*, vol. 34, no. 9, pp. 1290-1297, September 1999.

[7] G. Georgiou, *et al*, "Effect of output buffer on 40Gb/s limiting amplifiers designed with InP HBT technology", *IEEE MTT-S Digest,* pp. 2269-2272, 2003.

[8] W. Pohlmann, "A silicon-bipolar amplifier for 10 Gbits/s with 45 dB gain," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 551-556, May 1994.

[9] H. -M. Rein, and M. Moller, "Design considerations for very-high-speed Si-bipolar IC's operating up to 50 Gb/s," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1076-1090, August 1996.

[10] R. Krithivasan, J.P. Comeau, W.-M.L. Kuo, Y. Lu, J.D. Cressler, and A.J. Joseph, "A 24 GHz Broadband SiGe HBT Limiting Amplifier," *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 208-211, 2005.