Process Modeling of InAs/AlSb Materials for High electron Mobility
Transistors Grown by Molecular Beam Epitaxy

A Dissertation
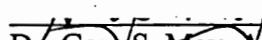Presented to
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By

Gregory Edward Triplett, Jr.

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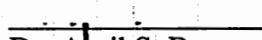School of Electrical and Computer Engineering

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Process Modeling of InAs/AlSb Materials for High electron Mobility
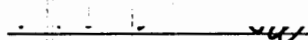Transistors Grown by Molecular Beam Epitaxy

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DEDICATION

This thesis is dedicated in memory of my dad.

ACKNOWLEDGEMENT

This research work would not be possible without blessings from God. I first give thanks to Him for all that I have accomplished. I recognize my advisors and dissertation committee members for all their support and guidance over the years. My gratitude exceeds this acknowledgement. I also thank the research staff and fellow group members for many technical discussions. I especially acknowledge my family and friends for their timely moments of motivation and support. This accomplishment is theirs as much as it is mine.

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Chapter 1 Problem Description

Semiconductor materials systems that demonstrate potential for ultra-high (~THz) frequency, low noise, and low-power applications are especially attractive, and much research and development effort is directed towards those systems. An example application is passive millimeter wave (PMMW) imaging, which is useful for concealed weapon detection, visibility during adverse weather conditions, and remote sensing of earth resources. High frequency and low noise electronics are important for PMMW imaging as well as for improving space-based and portable communication capabilities. Alternatives solutions are also needed for fully integrated low light imaging systems, where the high-speed and low power are important for digital signal processing performance. Future functions require low noise, low power consumption devices and circuits needed for high data rate transmission, lightweight power supplies, and extension of battery lifetimes. This also includes circuit components such as limiters and filters for enhanced control.

Device structures consisting of pure InAs layers present the opportunity to operate in the THz range by utilizing their extraordinary transport properties (electron mobility, electron saturation velocity). The ~6.1Å semiconductor materials (AlSb, GaSb, InAs) have drawn much interest due to their small lattice mismatch enabling the production of pseudomorphically-grown InAs-based structures and fully integrated functional systems. The 6.1Å family exhibits favorable valence and conduction band alignments, which offer flexibility in device design. Without the need to dope the epitaxial layers, both type-I and type-II structures are attainable. This system boasts a large conduction band offset

between InAs and AlSb. This offset provides superior electron charge confinement in AlSb/InAs/AlSb quantum well structures. Current performance of 6.1Å device structures, however, fall short of material expectations [1]. Several aspects, including but not limited to, device design, growth, and fabrication contribute to the less-than-projected frequency performance. For this reason, this study explores the material growth process during critical stages of production and examines the properties of 6.1Å-based structures produced via molecular beam epitaxy.

Synthesizing high-quality 6.1Å mixed-anion device heterostructures by molecular beam epitaxy (MBE) presents several manufacturing challenges. The most noted obstacle is the propensity for anion intermixing across the heterointerfaces that introduces defects that diminish structural and transport properties. Moreover, the impact that structural variations exhibit on device performance parameters is not well understood. If properties of the 6.1Å compound semiconductor "family" are to be realized, precise control of the growth process at the heterointerface is necessary, and the facility to manipulate device structures is essential. The use of MBE is advantageous for the production of 6.1Å device structures. MBE is flexible and can be configured to achieve the desired control to within one atomic layer (3Å) for the growth of thin epi-layers. Heterostructure devices that are sensitive to thickness variations are frequently synthesized using this growth method [2]. The quality of interfaces is also critical in many device structures, particularly when it involves the semiconductor material systems of interest. With better control over the interface, MBE affords the opportunity to achieve 6.1Å device structures with excellent structural and transport properties. Device structures, such as high electron mobility transistors, are sensitive to the quality of heterojunction. Transport properties have been

observed to fluctuate with the growth of the heterojunction. The use of MBE also offers real time *in-situ* process monitoring. A "live" look at the process during critical stages of growth (i.e. the interfaces) presents an interesting perspective. To date, there exists a limited ability to evaluate the interfaces and the quality of the device structures *in-situ*. Typical methods of characterization are performed post-growth and impose MBE system idle time to assess material properties. The use of real time diagnostic tools available through MBE is the key for understanding the process and enhancing run-to-run quality control.

The foremost difficulty with producing high-quality 6.1Å device heterostructures involves the mixed-anion (As/Sb) heterojunction. Anion intermixing across the heterojunction impacts many structural and device performance parameters including band alignment, interfacial roughness, material quality of the subsequent layer, and transport properties. A complete understanding of the formation and influence of the mixed-anion heterojunction is necessary to produce high-quality 6.1Å structures. In the next section, the 6.1Å material system and production issues are described.

1.1 The 6.1A Semiconductor Family

The 6.1Å semiconductor material system and device structures under investigation are comprised of InAs, GaSb, and AlSb. Interest in this semiconductor family remains primarily with bulk InAs material properties that possess a small energy gap (E_g=0.354 eV), high electron-mobility (μ>30,000 cm^2/V/s), and high electron saturation velocity (v_{sat}=4x10^7 cm/s). AlSb and GaSb, in comparison to InAs, exhibit

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larger energy gaps and inferior transport properties. Selected properties for InAs, GaSb, and AlSb are provided in Table 1.

Table 1. Properties of the 6.1Å Semiconductor Family

Semiconductor	Lattice constant	Energy gap	Electron affinity
InAs	6.059Å	0.354eV	4.9eV
GaSb	6.094Å	0.726eV	4.06eV
AlSb	6.1353Å	1.6eV	3.6eV

The 6.1Å semiconductor family has drawn a great deal of interest for the large conduction band offsets between AlSb and InAs (1.35 eV) and small lattice mismatch (<1.2%). Various semiconductor materials and their properties are illustrated in Figure 1.
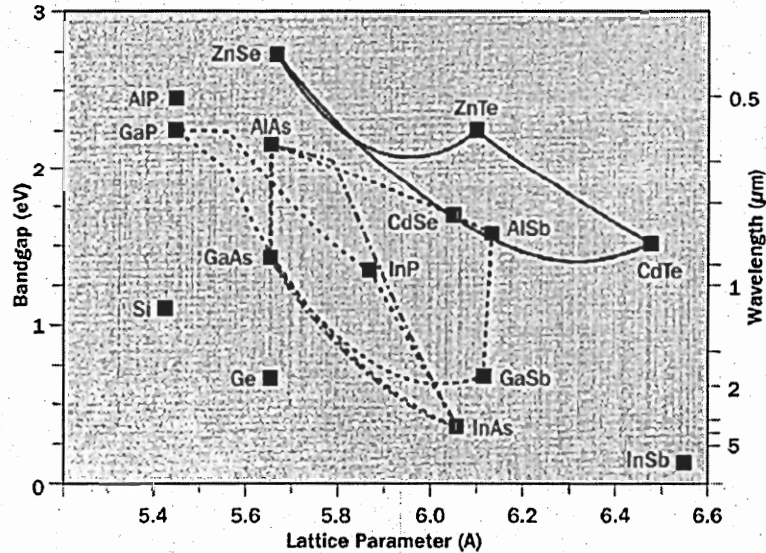
Figure 1. Semiconductor materials

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A large conduction band offset offers carrier confinement and allows high carrier densities and mobilities to be achieved. Because of the band alignments and small lattice mismatch among these materials, various device structures can be explored with interesting quantum properties. For example, both type-I and type-II structures can be achieved with the 6.1Å semiconductor family. By varying composition, the following can be produced: straddling type-I band alignments (AlSb/GaSb), type-II staggered band alignment (AlSb/InAs), and type-II broken band alignments (GaSb/InAs). The energy band alignments are presented in Figure 2.
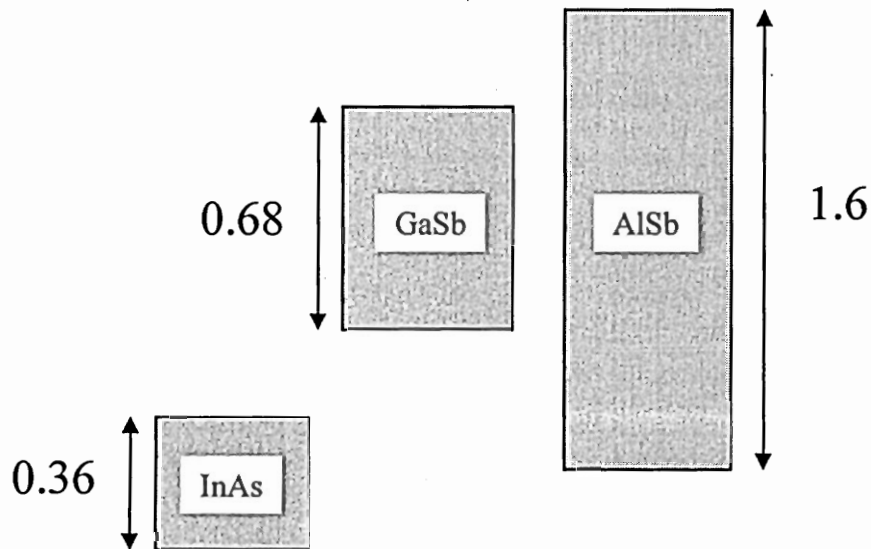
Figure 2. Energy band alignments for InAs, GaSb and AlSb (300 °K)

Unique to these material systems is the range of band alignments that can be accomplished without considerable differences in bulk lattice spacing at the interface,

which is not characteristic of most material systems. As a result, the crystalline quality of these structures can be retained without the effects of severe lattice deformation.

The bulk lattice properties in the 6.1Å family allow the design of unique device structures. Small lattice mismatch permits the implementation of pseudomorphically grown structures. It is expected that the transport properties of bulk InAs are achievable in 6.1Å structures, unlike InAs layers grown lattice-matched to InP where gallium fractionally substitutes for indium in order to compensate for the 3.2% mismatch. An $In_xGa_{1-x}As$ quantum well grown lattice matched to InP demonstrates a significant reduction in electron mobility, which decreases with increasing gallium composition. In contrast, increasing indium composition in $In_xGa_{1-x}As$ layers grown on InP enhances the strain in the layer and leads to growth instability. The same condition holds for $In_xAl_{1-x}As$ layers grown on InP. It therefore becomes fitting to synthesize pure InAs between suitable lattice-matched barriers, thereby taking full advantage of the high electron-mobility and electron saturation velocity of InAs.

1.2   AlSb/InAs/AlSb Quantum wells

InAs exhibits the second highest electron-mobility (InSb being first) among semiconductor materials. Structures that exploit the transport properties of InAs include single and multi-quantum well structures for HEMT and laser applications. However, InAs transport properties in AlSb/InAs/AlSb quantum wells are strongly dependent on the atomic-scale features of the heterointerface. One of the first studies of AlSb/InAs/AlSb single quantum wells explains that the inverted interface, InAs-on-AlSb, is especially influential on the carrier density and electron-mobility [3]. The AlSb-on-

InAs interface, on the other hand, has very little impact in determining the transport properties. The influence of the interface on the growth of the following layer is considerable. Therefore, optimization of the transport properties of AlSb/InAs/AlSb single quantum well structures involves the study of the InAs-on-AlSb interface, its formation, and quality of the InAs quantum well.

The bonding configuration at the interface is key to synthesizing high-quality 6.1Å heterostructures. There are two atomic arrangements possible at the InAs-AlSb interface: AlAs-like bonds or InSb-like bonds. If AlAs-like bonds exist at the interfaces in AlSb/InAs/AlSb quantum well structures, lower electron-mobility ($\sim 10^2$-10^3 cm^2/V/s) is the result. InSb-like bonds, however, reproducibly yield higher electron-mobility ($> 10^4$ cm^2/V/s). It has been argued that InSb-like bonds facilitate a smoother transition from AlSb to InAs compared to AlAs-like bonds. However, the extent of interfacial roughness is best defined by the abruptness of the interface, as opposed to the bonding configuration.

AlAs-like interfaces are synthesized using arsenic exposure to AlSb. These interfaces are atomically rough, since reduced mobility values are characteristic of this configuration. Brar, et al [4] observed that InAs epi-layers grown on AlAs-like interfaces exhibit higher dislocation density than epi-layers grown on InSb-like interfaces. This increase in dislocation density is in agreement with the increase in electron carrier concentrations observed in InAs/AlSb HEMT structures with AlAs interfaces at the inverted interface.

InSb-like interfaces, on the other hand, are realized using an extended antimony soak and the deposition of an indium monolayer at the InAs-AlSb interface. These

interfaces are smoother and produce significantly higher mobility than AlAs interfaces. Deposition of an indium monolayer at the heterointerface serves as a barrier for ensuing arsenic. Although previous work [5] suggest more indium is necessary for the InAs-AlSb transition, Nosho, et al. suggest that an indium monolayer is insufficient to make up for the compositional difference between InAs and AlSb and 1.25 monolayers of indium effectively transitions AlSb to InAs. The general difference between InSb and AlAs interfaces, besides the constituents, is the bulk lattice constants, where the mismatch from the 6.1Å material system is ~7% and ~6% for AlAs and InSb, respectively. A more distinguishing feature involves the strain states between AlAs and InSb. In the (001) growth direction, InSb bonds on AlSb undergo tensile strain. In contrast, AlAs bonds on AlSb experience compressive strain. The strain states at this critical phase potentially lead to instabilities during growth of the subsequent layer (the InAs channel) that are accompanied by an increase in structural imperfections. In review, it is apparent from transport and structural analyses that the difference between the two distinctive configurations is pronounced.

1.3 Device Structure

High electron mobility transistors (HEMTs) are advantageous for low voltage, high frequency applications. They exhibit superior electron transport properties compared to other device structures. Advantages of a HEMT include high transconductance, high output resistance, and small source resistance. HEMTs are semiconductor devices with low noise and high Gain·BW characteristics. The usefulness of HEMT devices is appropriate for amplifier, receiver, and detector applications.

In silicon field effect transistors (FETs), a conducting channel is formed between two intentionally-doped regions. The channel region is also doped to generate charged carriers. In contrast, HEMTs utilize a unique feature, the heterojunction, which improves carrier confinement and electron-mobility values. A HEMT structure is illustrated in Figure 1.
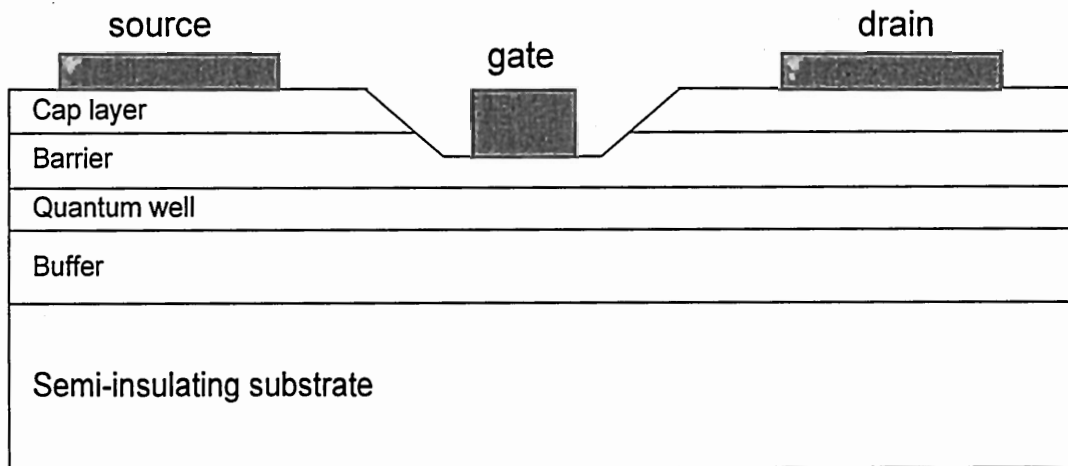
Figure 3. Cross section of a High electron mobility transistor (HEMT) structure

In a HEMT structure, the conduction carriers are physically separated from the donor impurities, which supply the electrons and reside in a lower energy state, confined by an energy barrier (the conduction band offset). During transistor operation, the charged carriers travel from the source to the drain by way of the channel region. The conduction carriers become subject to impurity scattering in the channel. Because the conduction carriers are separated from the donor impurities in a HEMT structure, the effects of impurity scattering are reduced and higher electron mobility values are attainable. Success of the first HEMT, an AlGaAs/GaAs based device, has stamped its

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place in electronic circuitry because of the improved device performance. The 6.1Å semiconductor family (AlSb, GaSb, InAs) enhances the opportunity to perform band engineering and takes advantage of the excellent transport properties of InAs. In the AlGaAs/GaAs HEMT structure, band offsets at the AlGaAs/GaAs interface are modified with increasing aluminum composition. Unfortunately, reduced electron mobility also accompanies increasing aluminum composition. In comparison, benefits of the 6.1Å material systems in HEMT structures are a larger (1.35eV) conduction band offset and a higher mobility channel (InAs) that can be pseudomorphically grown on AlSb.

1.4 Challenges

The expectations of the InAs/GaSb/AlSb material systems have yet to be realized. Several obstacles attribute to the lack of ultra-high frequency operation in 6.1Å transistor structures. The critical issues deal with control during epitaxy and post-growth device fabrication. Secondary issues involve the band alignments of InAs sandwiched between AlSb barriers. The valence band alignments, in particular, between InAs and AlSb lack sufficient hole confinement and contribute to significant gate leakage current in transistor structures. This degrades the device performance at high frequencies. Moreover, the small energy gap of InAs falls victim to impact ionization. This also influences transistor gate leakage current. Overcoming the interference that impact ionization presents requires thinner InAs layers between AlSb barriers. As the InAs layer thickness is reduced, the electron ground state in the quantum well is "squeezed" upwards. Unfortunately, thinner InAs layers exhibit reduced electron mobility values as a result of interfacial roughness scattering [6].

The imperfections initiated at the heterojunction exhibit residual effects. Following the growth of the InAs/AlSb interface, kinetics and surface chemistry impacts the growth of subsequent layers and ultimately influence the electronic properties of the structure. Where the InAs and AlSb layers meet, atoms exchange across the interface to create non-abrupt transitions. The characteristics of this interface are highly unfavorable because they lead to non-uniformity, growth instability, and degraded electronic properties.

Ideally, InAs should be grown on 6.1Å crystal structures. Its transport properties can be optimized under these conditions. Its bulk lattice constant inhibits the ability to achieve pseudomorphically-grown binary InAs layers involving more technologically mature GaAs (7% mismatch) and InP (3.2% mismatch) based systems. Even so, the strain-induced modulations during initial InAs growth on AlSb are carried over into the subsequent layer and effect electronic properties of the structure. Conveniently, the desired improvement for InAs-based structures becomes attainable through further development of the fabrication process of 6.1Å structures.

The attraction to the InAs/AlSb/GaSb material systems has prompted numerous studies [7-9]. Still, questions remain regarding the importance of the inverted heterojunction. Several studies demonstrate that the inverted heterojunction has considerable influence on the structural features and transport properties in the InAs quantum well [4, 10-12]. Unfortunately, the ability to produce thin, coherent InAs layers on AlSb involves greater control over interface formation. The motivation for using thin (<10nm) InAs layers between AlSb barriers remains the reduction in impact ionization- a benefit from squeezing the ground electron states up to higher energies. On the other

hand, an existing drawback to employing thin InAs layers continues to be the reduction in electron mobility, which is coupled to the electron saturation velocity and high frequency device performance.

Formation of the inverted interface remains considerably difficult to control, owing to numerous reasons, including anion exchange, a process where anions (As, Sb) on opposite sides of the heterojunction exchange lattice sites and create heterogeneous transitions. This phenomenon and its effects have been well documented [4, 6, 11, 13-22]. In short, the challenges for improving these device structures are linked to precise control during the synthesis of several critical monolayers. Therefore, exploring the growth process at the inverted interface presents the opportunity to fine-tune the fabrication process for the improvement of InAs/AlSb HEMT structures.

The focus of this research deals with a critical phase during the molecular beam epitaxy growth of these structures: formation of the InAs-on-AlSb interface. Several studies explore one MBE process parameter at a time and then analyze the device structures. The experiments in this study were performed using statistically designed experiments, a technique for determining the significance and facilitating the modeling of several selected MBE process parameters. InAs/AlSb HEMT structures were the test vehicles. X-ray diffraction and Hall measurements were used to determine the structural and electronic properties of the HEMT structures. Neural network modeling was employed with the purpose of developing relationships between properties of device structures and the MBE growth process. Formation of the inverted interface was examined in real-time through the use of reflection high-energy electron diffraction (RHEED). Using a unique approach, the RHEED data was analyzed using principal

component analysis (PCA) and used to train a neural network. RHEED-based modeling presents the opportunity to detect changes in the MBE growth process enabling run-to-run process control. RHEED and atomic force microscopy were also used to observe the surface roughness of the inverted interface, prior to growth of the InAs quantum well. Other facets of this research involve various HEMT structures and doping schemes for modulating the conductivities in these structures.

The results from in-situ and ex-situ analysis techniques are used to identify several noteworthy features of InAs/AlSb HEMT growth via MBE. One deals with the importance of MBE process parameters during the growth of the inverted interface. Another is the growth regime for improved InAs/AlSb-based HEMT structures. The last involves an effort to understand particulars about the growth process. This study highlights the impact of MBE growth process on material properties and demonstrates new techniques for understanding the growth of heterostructure devices.

1.5 Outline for this thesis

The remainder of this thesis is dedicated to the challenges that should be overcome for production of integrated circuitry consisting of the 6.1Å material systems. Chapter 2 describes the studies performed to date and the design and growth issues that remain. Chapter 3 provides the experimental approach employed and the analytical techniques used to characterize these device structures. The results and evaluations are discussed in Chapter 4, which include the process models developed. The impact of the growth process on the device performance parameters and the structural properties are

summarized in Chapter 5. This thesis is concluded by the recommendations for future work in Chapter 6.

Chapter 2 Literature Review

The 6.1Å (InAs, GaSb, AlSb) compound semiconductor material system has been under intense study, largely due to unique properties that demonstrate potential for low-noise and millimeter wave applications. Producing mixed-anion and mixed-cation heterostructures presents numerous challenges, particularly at the heterointerface. The difficulty with producing near-perfect InAs-AlSb heterostructures is recognized, and improving results reflect a better understanding of how to manipulate these structures. Still, several aspects of InAs/AlSb device manufacturing require further insight. These areas involve, for example, the intermixing of anions at the heterojunction and the origin of charge in unintentionally doped InAs/AlSb structures. Alternative approaches for investigating these issues are also essential to the development InAs/AlSb heterostructures. This chapter describes the methods, latest advances, and future goals for controlling and understanding the properties of these structures.

The ideal properties of InAs-AlSb heterostructures are attractive for device applications. Specifically, the electronic properties of pure InAs, including electron mobility and electron saturation velocity, are desirable for high frequency and low power applications. Electron mobility, a measure of electron scattering in a semiconductor, influences field-effect transistor source/drain resistance. Electron saturation velocity, which describes the maximum rate at which electrons travel in a semiconductor, determines operational frequencies. Unfortunately, the most beneficial aspect of the InAs-AlSb material system - the transport properties of the InAs quantum well layer- is very sensitive to the InAs/AlSb device structure and its fabrication process. The specific

issues surveyed in this chapter include: (1) the impact of structural variations on the transport properties, namely sheet charge and electron-mobility; and (2) microscopic processes that occur during formation of the heterojunction. The following sections describe recent advances and the current status of epitaxial growth of InAs/AlSb device structures.

2.1 Epitaxy of InAs-AlSb structures

The roadmap for improving InAs/AlSb heterostructure device technology begins with enhanced control over the fabrication process, which will result in increased device functionality and improved performance. The simultaneous exchange of cations and anions at the InAs/AlSb heterojunction during growth further complicates device production and places stringent requirements on semiconductor fabrication systems. The challenge with heterostructure growth continues to be unintentional incorporation of atoms from one side of the heterojunction into the other, which is observed in InAs/AlSb device structures. As a result, the boundary between InAs and AlSb is difficult to distinguish. More importantly, the electronic properties and energy band alignments are affected by such exchange. Therefore, the production of InAs/AlSb heterostructures demands precise control of the growth process, otherwise, variations in device structure and electronic properties are observed.

2.1.1 Molecular Beam Epitaxy

The most common growth method for InAs/AlSb heterostructures is molecular beam epitaxy (MBE), which is described in detail in chapter 3. MBE allows epitaxy

control to within one atomic monolayer. The MBE growth sequences by which InAs-AlSb heterojunctions are formed have been examined extensively [3, 4, 12, 15, 16, 19, 20, 23]. Still, the challenge in producing ideal heterojunctions remains unsolved. In addition, controlling the charge in InAs/AlSb heterostructures is also a critical issue. As the charge in the InAs/AlSb structures is reduced, the electron-mobility follows. Resolving issues such as these will improve the frequency performance of InAs/AlSb devices. The following sections describe InAs/AlSb heterostructure growth via molecular beam epitaxy and the challenges with manipulating the device structure.

2.1.2 Interfacial Bonding

The transport properties of InAs-AlSb heterostructures depend a great deal on the heterointerface, in which there are two basic bonding configurations: InSb-like and AlAs-like. When InSb-like bonds are formed at the inverted heterojunction, electron mobility values for 15nm InAs quantum well structures are high ($\sim 10^4$ cm^2/V-s), and the sheet charge densities are reproducibly $\sim 10^{12}$ /cm^2 [3]. In contrast, AlAs-like bonds at the inverted interface produce structures with lower electron mobility ($\sim 10^2$ - $\sim 10^3$ cm^2/V-s) and higher sheet charge densities ($\sim 10^{13}$ /cm^2). These results suggest that AlAs-like bonds contribute substantially to sheet charge and impede electron transport along the inverted interface.

Ideally, the growth sequence of InSb and AlAs interfaces differs by only two monolayers. For example, when forming InSb bonds, the AlSb layer is terminated with antimony and followed by the deposition of one monolayer of indium. Then InAs growth

is initiated. Forming AlAs bonds is quite the opposite. Covering the surface with aluminum on AlSb, which is then followed by arsenic exposure, produces AlAs-bonds. The growth sequence is reversed for AlSb-on-InAs, i.e., covering the growth surface with indium followed by antimony exposure forms InSb bonds. The growth sequence for InSb bond-like structure at the InAs-on-AlSb interface is illustrated in Figure 4.
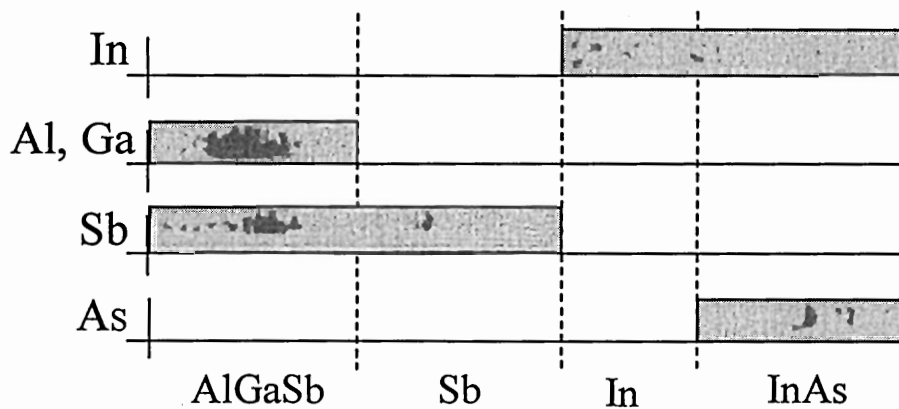
Figure 4. Growth sequence at the InAs-on-AlSb interface for InSb bond-like structure

Numerous reports cite the influence that interfacial bonding exhibits on both mobility and sheet charge in InAs-AlSb quantum well structures. Still, it remains unclear what mechanisms drive the distinctions in electron mobility. Likewise, the range of electron populations accumulating in the well is difficult to explain. Analysis becomes more complex for reasons that include sensitivity of transport properties with respect to interfacial bonding on both sides of the quantum well and the device structure. The next section describes the sensitivity of the transport properties with respect to modifications in InAs-AlSb device structures.

2.2 Two-Dimensional Electron Gas

An attribute of the ~6.1A semiconductor material system is the large conduction band offset (1.35 eV) between InAs and AlSb. When InAs is sandwiched between AlSb barriers, a deep quantum well is formed. A large band offset allows substantial charge to be stored and reduces the carrier's ability to escape the well. Charge is accumulated in the quantum well when carriers move from higher energy states outside the well to lower energy states inside the quantum well. In AlSb/InAs/AlSb quantum well structures, the electron charge that is transferred to the conduction band minimum in the InAs well becomes spatially separated from the AlSb clad layers. As a result, the carriers accumulate and reside in the quantum well. Because of the energy barrier on both sides of the well, the carriers are confined to movement in two dimensions only. Therefore, they travel in one direction- along the quantum well. The accumulated electron population in the quantum well is a "termed two-dimensional electron gas" (2-DEG) because it exists in only two dimensions. The carrier velocities and mobilities in quantum well structures depend on the material in the well. In AlSb/InAs/AlSb well structures, considerable 2-DEG charge concentrations ($\sim 10^{12}$ /cm^2) are observed. High electron mobilities (30,000 cm^2/V/s) are also consistent with InAs bulk material.

2.2.1 Electron Charge Compensation

A requirement for digital logic and analog circuitry is the availability of both depletion-mode and enhancement-mode transistor operation. Implementation of InAs/AlSb device structures for complex circuitry is predicated on the reduction of accumulated charge in the transistor channel layer. Unfortunately, the 2-DEG values in

unintentionally doped InAs/AlSb structures produced via MBE are especially high ($\sim 10^{12}$ /cm^2). Consequently, transistors developed from unintentionally doped structures operate in depletion-mode exclusively. One goal is to reduce the charge transferred to the quantum well so that the channel is non-conducting when no bias is applied. To date, enhancement-mode operation is not achievable without instituting doping schemes that simultaneously degrade electron mobility and device operation.

The electron population in non-intentionally doped AlSb/InAs/AlSb quantum wells cannot be explained by the background doping of InAs. Recent studies have examined the origins of charge in the InAs/AlSb system [23-29]. The sources of charge in these structures are numerous, and control is inadequate. The list of charge contributors includes bulk donors in adjacent AlSb barriers, surface donors, and interface donors along the well. Each is related to the epitaxy process, device structure, or energy band offsets. Reduction of 2-DEG values has been demonstrated through modifications of the device structure; however, the residual charge remains too high for the development of enhancement-mode devices.

2.2.2 Surface and Bulk Donors

Surface donors account for the largest contribution of charge transferred to the quantum well. In one relevant study, Nguyen, et al. [24] found the electron population in the InAs quantum well to be sensitive to the thickness of the top barrier. When the top AlSb barrier is increased to several hundred angstroms, the charge in the quantum well is reduced. So, as the channel layer is displaced further away from the surface, the fermi-level pinning of the cap layer is lower and a reduction in electron population is observed.

In a later study by Nguyen, et al. [29], the surface layer was also found to influence the electron population. Again, the surface donor contributions depend on the pinning position of the Fermi level. In this case, Fermi level pinning is dictated by the composition of the surface layer. For InAs-AlSb structures, GaSb or InAs are typically used as cap layers because: (1) AlSb is highly reactive when expose to the atmosphere; (2) both GaSb and InAs provide good lattice matching with AlSb; and (3) both GaSb and InAs are useful for forming metal contacts. Since the electron affinity of InAs is greater than that of GaSb, the fermi level for InAs is deeper in the conduction band. Therefore, the use of InAs as the cap layer considerably reduces the surface charge transferred to the quantum well. Figure 5 shows the energy band alignment of InAs/AlSb quantum wells and the impact of the cap layer.
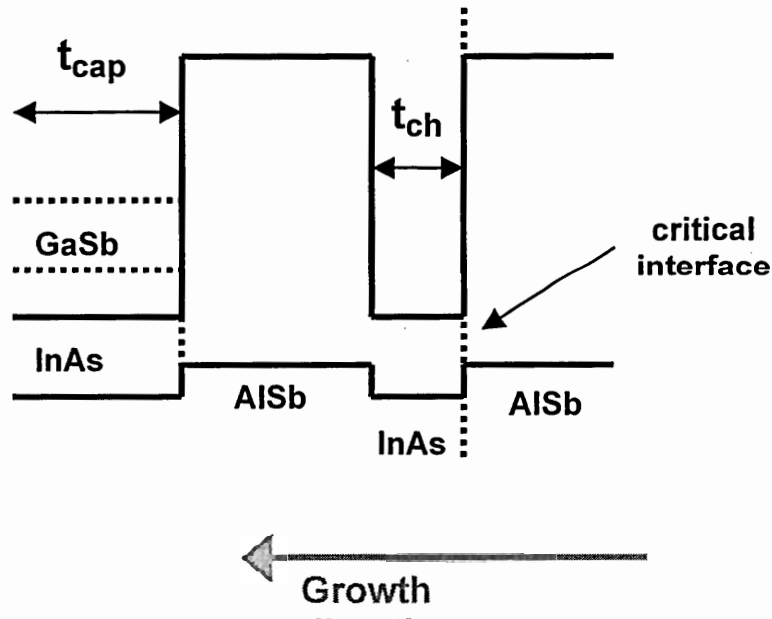
Figure 5. Energy band diagram of an InAs/AlSb quantum well

The bulk donors from AlSb barriers also account for a significant portion of electrons in the quantum well. The bulk donors are defect-oriented and are influenced by the growth process or quality of starting material. Producing defect-free AlSb layers presents a challenge. The bulk donors are influenced by the process environment, AlSb growth parameters, and purity of the constituents Moreover, suitable semi-insulating substrates are lacking. As a result, the crystal quality of AlSb layers is improved using thick buffer layers or smoothing superlattices. While much improvement is desired regarding the crystal quality of AlSb, researchers focus on understanding and controlling the charge in these structures.

A study by Shen, et al. [28] describes the contribution of defects (Al_{Sb}) in AlSb barriers. The energy level for Al_{Sb} defects was determined to be 0.45 eV above the AlSb valence band maximum, which lies above the InAs conduction band minimum. Accordingly, it is energetically favorable for electrons originating from Al_{Sb} defects to transfer to the quantum well. To address this contribution, the InAs conduction band minimum can be raised above the Al_{Sb} antisite defect level by decreasing the well thickness (t_{ch} in figure 5). According to Shen, et al., the critical layer thickness is ~63Å for the InAs quantum well. A tradeoff in electron-mobility is observed when the InAs layer thickness is modified so as to compensate for undesirable charge in the quantum well. The reasons for this tradeoff remain unknown.

It has been determined that the interface also contributes charge to the quantum well [3, 23, 28]. There are two distinct bonding configurations achievable at the heterointerface, and empirical data challenges the explanation that each configuration is comparable and not expected to produce large differences in 2-DEG values. With InSb-

like interfaces, AlSb/InAs/AlSb single quantum well structures exhibit 2-DEG values on the order of $\sim 1 \times 10^{12}$ /cm^2. In comparison, AlAs interfaces produces 2-DEG that is as much as four times that ($\sim 4 \times 10^{12}$ /cm^2) in structures with InSb-like interfaces. Reasons for this anomaly have been associated with interface Tamm states [23], yet models do not corroborate empirical data. This conundrum stems from the reduction in electron-mobility and how it surprisingly follows reduced 2-DEG values. In this instance, Tamm states are associated with the discontinuity between the potentials at the heterointerface and are considered to influence the valence band alignments. As reports remain purely speculative, physical interpretation of the interface donors in this area is highly desired.

2.3 Microscopic Processes at the Heterojunction

The growth of InAs/AlSb heterostructures requires particular attention at the heterointerfaces. It is clear that interfacial bonding influences the transport properties (i.e. electron-mobility and 2-DEG). Still, as questions remain regarding the source of charge in the well and its equivalent impact on electron mobility, studying the growth mechanisms during heterointerface formation presents an arena to glean more information regarding InAs/AlSb structures. The growth mechanisms affect strain, structural properties, transport properties, and more noticeably, surface morphology. Investigating these microscopic processes is complicated because it requires in-situ process monitoring of the growth surface. Interaction with the processes environment is a clear drawback for reasons that include interference with surface kinetics. Prospective tools for analyzing the growth process include RHEED, a typical accessory in MBE systems. RHEED is noninvasive, however, RHEED data analysis is intensive and time

consuming. This section describes the mechanisms that drive intermixing at the heterojunction and methods used to examine them.

2.3.1 Anion Intermixing

An ideal InAs/AlSb interface is difficult to synthesize. As long as the heterointerface consists of distinct cations and anions, the ability for atoms to exchange across the interface exists. Ultimately, anion intermixing (or anion exchange) governs these interfaces that influence transport, structural, and optical properties. The basis for understanding anion intermixing includes the ability to control stoichiometry as well as preserve structural properties that enhance the performance of high frequency, low power devices. Accordingly, control of anion intermixing remains the objective for As/Sb structures.

Numerous studies illustrate the disorderly nature of anion exchange reactions [18, 21, 22, 30-32]. Standard test structures for studying this phenomenon are superlattices, where repeatable observations at each interface is expected to provide evidence that relates process parameters or atomic/molecular species to exchange behavior. In these structures, segregation, diffusion, and incorporation are the principal processes for anion intermixing. Segregation is the spontaneous process of separating atoms from the sub layer. Diffusion describes the transfer of those atoms into the subsequent layer. In the end, the incorporation of the diffused atoms give rise to non-linear, graded profiles in the following layer. Temperature, atomic/molecular species, and surface states affect the individual processes, thus making analysis of anion intermixing a major undertaking.

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The critical stage of InAs/AlSb growth is the growth sequence at the heterointerface. Employing InSb-like interfaces brings about desirable electron mobilities in AlSb/InAs/AlSb well structures. The issue of anion intermixing provides insight into the relationship between electron transport and the heterojunctions.

Recent studies of anion intermixing and electron transport in As/Sb heterostructures support the critical role of the inverted interface. Observations by Tuttle, et al. [3] demonstrate that the MBE shutter sequences at the bottom interface influences electron-mobility in AlSb/InAs/AlSb quantum wells. Reports that follow describe anion exchange reactions during the growth of As/Sb heterostructures. Also using MBE, Bennett et al. [32] studied As/Sb heterostructures and observed strong relationships between anion intermixing and substrate temperature, with stronger intermixing for As-for-Sb compared to Sb-for-As. In another study, Xie, et al. [21] described the arsenic for antimony exchange and also demonstrated a correlation between temperature and arsenic incorporation. Anion intermixing was observed for substrate temperatures as low as 300°C. According to these studies, the dominant anion exchange reactions at As-on-Sb interfaces correspond with the significant interface in AlSb/InAs/AlSb quantum wells. Since the optimum growth temperatures for InAs/AlSb structures are higher than 300°C, the temperature-related mechanisms that drive exchange reactions appear unavoidable.

2.3.2 RHEED Observations

Anion exchange reactions are typically examined using post-growth analytical techniques such as transmission electron microscope (TEM), cross-sectional scanning tunneling microscope (CS-STM), or x-ray diffraction (XRD). A comprehensive

exploration of these growth processes should include real-time in-situ surface analysis as well. The techniques listed assess the end result of anion intermixing rather than the means. Taking into consideration the criteria for real-time surface analysis during growth, the non-invasive nature of RHEED lends usefulness to this technique for observing anion exchange reactions.

RHEED is a tool for studying anion exchange reactions that is not generally employed. Instead, MBE crystal growers utilize RHEED for determining deposition rates, surface reconstructions, and substrate de-oxidation. While RHEED itself is not difficult to implement, the information from RHEED can be too complex to analyze. RHEED images of the growth surface consist of numerous features including patterns, spots, lines, linewidth, and intensities, to name a few. Improved heterostructure growth benefits from the development of models that explain the non-linear behavior of RHEED image properties. The potential of RHEED for monitoring anion exchange was demonstrated by Collins, et al. [18]. The anion exchange reactions during the exposure of InAs to antimony overpressure were apparent through the intensity profiles of the specular spot. Reproducible data could be achieved as long as the antimony flux and species were consistent from run to run. This demonstrated RHEED as a potential avenue for controlling MBE heterostructure growth and run-to-run process control.

In the next chapter, the experimental apparatus and the analytical techniques are described. The experimental approach includes the used of designed experiments, in-situ diagnostic tools, and optical and electrical characterization techniques. The methods in which the experimental results are analyzed are also described.

Chapter 3 Methodology

The relationships between the properties of ~6.1Å HEMT structures and the process parameters can be very complex and non-linear. The ability to synthesize precisely ~6.1Å HEMT structures depends a great deal on the process environment and the growth dynamics. A systematic approach to studying these relationships provides the opportunity to examine the effects of the process environment and concentrate on particulars of the growth process. Moreover, it supports the development of process models that describe these relationships and provides insight into the intricacies of ~6.1Å HEMT structure growth. In this study, ~6.1Å HEMT structure fabrication is examined through the use of experimental, analytical, and modeling techniques such that a greater understanding of the influence of the process parameters is gained. The following sections describe the experimental methods and the techniques employed for data acquisition and analysis.

3.1 Experimental approach

Production of ~6.1A heterostructures can be tedious, depending on the complexity of the device structure. Not only do the optimum process conditions for individual layers differ, but special attention must also be directed toward the arsenide/antimonide junction [3]. For structures that contain distinct constituents on opposite sides of the heterojunction, enhanced control during growth is highly desirable. Therefore, a crystal growth method, such as molecular beam epitaxy, that exhibits superior control during epitaxy down to one atomic layer is essential for ~6.1Å heterostructure growth. An added

benefit to using molecular beam epitaxy is the *in-situ* process-monitoring tool available. Reflection high-energy electron diffraction (a customary component on MBE systems) provides real-time surface evaluation during epitaxy without interfering with the growth process.

The complexity inherent in producing ~6.1Å heterostructures also involves subtle changes in growth dynamics (particularly at the heterointerface), which influence the physical properties of the structure. The driving forces for these subtle changes remain uncertain. Moreover, the ability to suppress these changes using controllable process parameters is lacking. The use of designed experiments is especially useful for identifying these important process parameters that influence the properties of these structures. The following section describes the experimental approach employed, which consists of the following techniques: molecular beam epitaxy, reflection high-energy electron diffraction, and statistical experimental design.

3.1.1 Molecular Beam Epitaxy

Fabricating InAs/AlSb device structures requires precise control over the growth process. The inability to manipulate the formation of critical heterojunctions shows up in variations of device structure and electronic properties. A widely used and recognized growth method that exhibits enhanced control down to an atomic monolayer is molecular beam epitaxy (MBE). MBE is capable of producing complex, multi-layer electronic device structures containing a mixture of semiconductor II-VI and III-V compounds. Once considered unsuitable for mass production, MBE is now present in high production environments. Resulting from improved designs, existing MBE technology now offers

the capability to synthesize complex, multi-layer compound semiconductor device structures on 6" wafers. Figure 6 illustrates an MBE system.
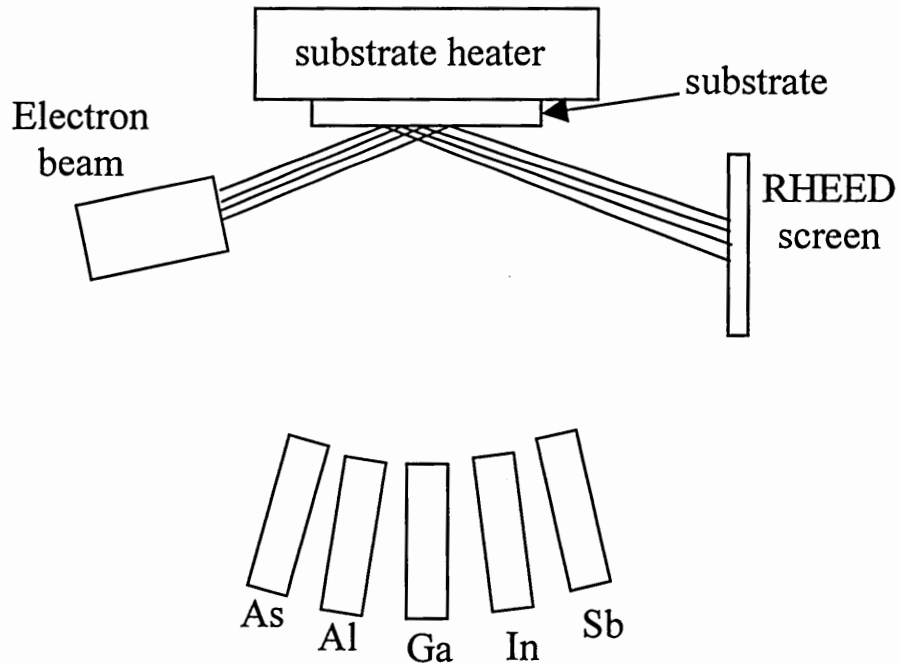
Figure 6. Schematic of a Varian Gen-II MBE system.

An MBE system is comprised of a large vacuum chamber that can achieve pressures down to $\sim 10^{-11}$ Torr. Ultra-high vacuum is achieved using large-volume ion pumps, turbo-molecular pumps, or cryogenic pumps. The vacuum chamber pressure is important because it influences the mean free path of atoms/molecules in the process environment. At lower chamber pressures, molecular beams can travel much farther without experiencing collisions with other particles before being deposited on the substrate material. Attributes of lower chamber pressure include low contamination and command over material deposition. A relatively low growth rate compared to faster crystal growth techniques, i.e. the Czochralski method, is characteristic of MBE systems.

Device structures can be grown atomic layer by atomic layer at a growth rate of several microns per hour (μm/hr).

The main components of an MBE system contain the source shroud and the substrate assembly. These sections are located on opposite sides of the main growth chamber. A source shroud, which contains numerous ports for MBE cell mounting, typically consists of effusion cells, dopant cells, and/or bulk evaporator and cracker units. MBE cells are essentially thermal sources that have enclosed thermocouples, heater filaments, and a crucible that contains elemental material in bulk form. When in operation, power is applied to the heater filaments in the MBE cell and thermal energy is transferred from the crucible to the bulk material. Once sufficient thermal energy is transferred to the bulk material, bonds are broken and molecular beams are produced. The magnitude of the molecular beams is primarily a function of temperature, elemental material, and material volume in the crucible. The rate of material deposition can be expressed as:

$$GR \cong A \exp{^{Ea/kT}} \qquad (1)$$

where GR is growth rate, A is a constant, Ea is activation energy, k is Boltzmann's constant (1.3806×10^{-23} J K^{-1}), and T is temperature in Kelvin. Bulk evaporators and crackers are larger volume cells that have internal valves, which permit beam flow and determine beam magnitude. Dopant cells, which have significantly smaller volumes, are used to tailor the carrier concentrations of the epi-layers. Typical MBE cell operation is in the 400-1200°C range.

On the source shroud, MBE cells are numerous and operating temperatures are high. Therefore, cooling is required and is normally accomplished using flowing liquid nitrogen and/or ethanol glycol throughout the source shroud. The bulk evaporators and crackers are particularly large and use two separate temperature zones, so additional and exclusive cooling is required for these cells.

The substrate assembly is used for mounting the substrate material for epitaxial growth. It consists of a substrate block holder, thermocouple, and substrate heater. The substrate block holder is located directly in front of the substrate heater without making contact and is rotated during epitaxy. The thermocouple is placed behind the heater - free from impinging beams. This extends the thermocouple lifetime and promotes measurement repeatability. Substrate assembly rotation increases film uniformity across the wafer.

Mounted directly in front of each cell port is a pneumatic shutter. The opening and closing of these shutters determines beam flow. The molecular beams travel from the cell port and impinge on a substrate, which is mounted on the substrate assembly located directly across from the source shroud (Figure 6). The experiments in this study were accomplished by controlling the temperatures, valve positions, and MBE shutter sequences. The shutters remained closed for idling cells and cells that were not in use.

3.1.2 Reflection High-Energy Electron Diffraction (RHEED)

A customary diagnostic feature on MBE systems is reflection high-energy electron diffraction (RHEED). A RHEED system provides in-situ, real time evaluation of crystal growth. MBE crystal growers have benefited significantly from this technique. For

example, substrate-cleaning procedures have been established and deposition rates can be calculated based on RHEED observations.

The RHEED system employed in this study consists of a 10-keV electron beam, a green phosphor screen, and a CCD imager. The electron beam strikes the substrate surface at a glancing angle ($<2°$) and reflects to the phosphor screen, which displays the diffraction pattern. The 12-bit digital CCD camera is used to capture RHEED images displayed on the screen. The diffraction pattern contains qualitative and quantitative information about the growth surface. Such information about the growth surface includes strain, lattice spacing, and deposition rate. In attempt to glean more from RHEED observations and growth of ~6.1A heterostructures, RHEED images and specular spot intensities were recorded during the formation of the inverted interface in InAs/AlSb structures without rotating the substrate assembly.

3.1.3 Statistical Experimental Design

MBE has numerous controllable process parameters. They include, but are not limited to: shutter sequence, soak times, flux pressure, and growth rates. Optimizing the conditions for heterostructure growth is a major undertaking. The traditional method, where one factor is examined at a time, is not the most efficient method of exploration. The ideal operating condition is unlikely to be found in this manner. The use of designed experiments is a means for successfully and efficiently exploring the parameter space. Designed experiments have several advantages. A notable attribute of designed experiments is the determination of statistical significance. Not only can main effects be identified, but important interactions can also be estimated. When studies merely

compare a few samples, the results are not usually significant or generalizable. In contrast, the use of designed experiments optimally determines the experimental trials, and the results can be rigorously analyzed. Overall, designed experiments provide an efficient, reliable, and systematic approach.

The selection of a specific experimental design is based primarily on the experimental objective. The goals of this study were to (1) identify the process parameters that influence the properties of ~6.1Å HEMT structures; and (2) develop models that describe the MBE process. Accordingly, factorial and central composite experiments were employed. These designs support the development of process models over the parameter range.

3.2 Analytical Techniques

The task of examining process conditions and their effects on the properties of heterostructures calls for individual samples for each operating condition. Many studies employ superlattice structures that contain several experimental trials per sample. Superlattice structures are useful for recognizing trends at a series of heterojunctions. However, the ability to relate electronic properties to process conditions in superlattice structures is unfeasible. In this study, a HEMT structure was fabricated for each process condition. Thus, the electronic properties as well as the structural characteristics could be associated with specific MBE process conditions. The analysis techniques employed in this study were used to determine electronic and structural properties, as well as analyze and represent information from RHEED observations for the development of process models. The following sections describe these techniques.

3.2.1 Hall measurements

An important electronic property in ~6.1Å heterostructures is the electron mobility in InAs quantum wells. A customary technique for determining electron mobility is Hall analysis. Because of its simplicity and low-cost, it is the most commonly used characterization technique in semiconductor fabrication facilities. This technique determines sheet density (n_s), bulk carrier density (n, p), electron mobility (μ), and sheet resistance (R_s) in semiconducting samples. The electronic properties are measured using a combination of measurements. The resistivity measurement determines the sheet resistance, and the Hall measurements determine the electron mobility and sheet density. To perform Hall analysis, four ohmic contacts are formed on the corners of the sample. Figure 7 illustrates Hall sample configuration.
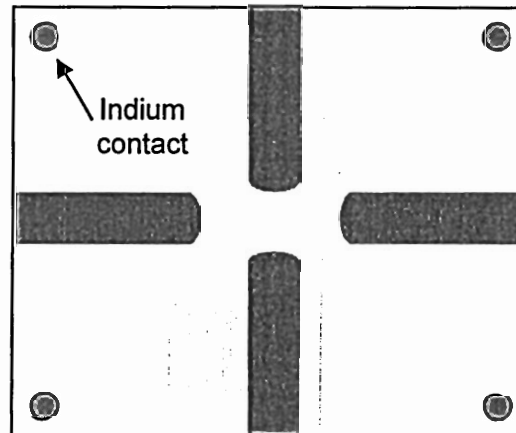
Figure 7. Hall sample configuration using van der Pauw technique

The resistivity is measured by applying direct current (dc) into nodes (1) and (2) and measuring the voltage from nodes (3) and (4). This process is repeated for the other combinations. The sheet resistance is determined using the equations

$$R_A = (R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21})/4 \qquad (2)$$

$$R_B = (R_{32,41} + R_{23,14} + R_{14,23} + R_{41,32})/4 \qquad (3)$$

$$\exp(-\pi\,R_A/R_S) + \exp(-\pi\,R_B/R_S) = 1 \qquad (4)$$

Based on the sheet resistance calculated, the electron mobility and sheet density can be determined. Hall measurements are performed by measuring the voltage on a diagonal set of contacts while supplying dc current into the remaining set of contacts. These measurements are performed in the presence of a magnetic field. The equations below are used to calculate electron mobility and sheet density.

$$V_a = V_{24P} - V_{24N} \qquad \text{\{current is applied to (1) and flows out of (3)\}} \qquad (5)$$

$$V_b = V_{42P} - V_{42N} \qquad \text{\{current is applied to (3) and flows out of (1)\}} \qquad (6)$$

$$V_c = V_{13P} - V_{13N} \qquad \text{\{current is applied to (2) and flows out of (4)\}} \qquad (7)$$

$$V_d = V_{31P} - V_{31N} \qquad \text{\{current is applied to (4) and flows out of (2)\}} \qquad (8)$$

If $(V_a + V_b + V_c + V_d)$ is positive, sample is p-type, otherwise the sample is n-type.

$$p_s = 8 \times 10^{-8}\, IB/[q(V_a + V_b + V_c + V_d)] \qquad (9)$$

$$n_s = |8 \times 10^{-8}\, IB/[q(V_a + V_b + V_c + V_d)]| \qquad (10)$$

$$n = n_s/d,\; p = p_s/d \qquad (11)$$

$$\mu = 1/qn_sR_S \qquad (12)$$

where *I* is dc current, *B* is the value of uniform constant magnetic field intensity, and *d* is thickness of the conducting layer. In this study, *d* represents the width of the quantum well. In this study, the electronic properties in InAs/AlSb HEMT structures produced by molecular beam epitaxy were measured using Hall measurements.

3.2.2 X-ray analysis

Evaluating the structural properties of pseudomorphically-grown ~6.1Å heterostructures is instrumental to improving the growth of these structures. X-ray analysis determines the crystalline properties, which can be used to assess the quality of InAs/AlSb HEMT devices. In this study, structural analysis was performed using x-ray diffraction (XRD), a non-destructive technique that provides qualitative and quantitative information about the individual layers.
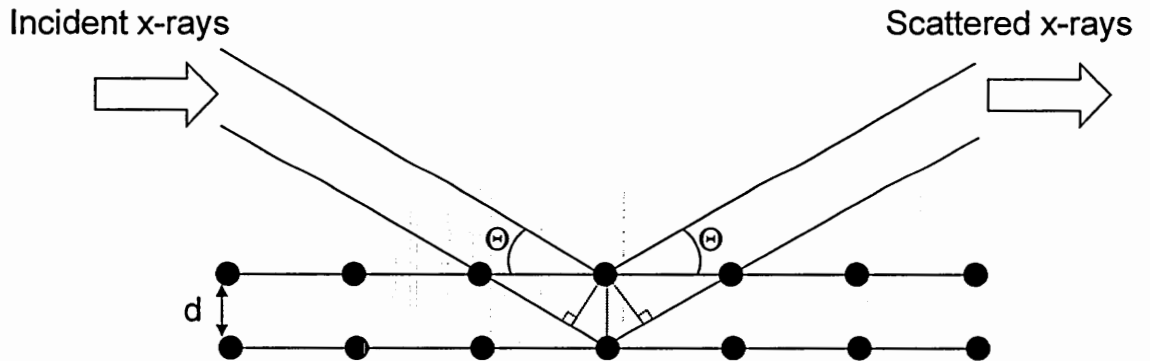
Figure 8. Incident and scattered x-rays on a lattice

XRD is a powerful technique for analyzing the crystal structure in semiconductor materials. The essence of XRD is the use of x-rays that strike the surface and undergo

scattering and absorption. Diffraction measurements occur when the scattered x-rays add up in phase (figure 8). According to the Bragg law (Equation 13),

$$n\lambda = 2d \sin \theta \qquad (13)$$

strong diffraction is observed when the incident and diffraction angle are equal, and the path difference between the two beams is an integral number of wavelengths ($n\lambda$). X-rays from $CuK\alpha$-lines ($\lambda = 1.54056\text{Å}$) are employed in this study. The separation of reflecting planes determines d. Theta (Θ) is the angle between the incident and reflecting plane. The x-ray peak characteristics are dependent on the number of plane waves collected and the quality of the semiconductor material. In thin samples, the peak width is broader compared to the peak width for thicker samples. Likewise, the peak width is narrower for samples with superior crystalline quality.

X-rays penetrate deeply into the sample and provide information on the complete structure. Several techniques available through XRD allow particular structural features to be examined in detail. The most commonly employed measurement is the rocking curve scan, which provides information regarding the following structural features: film quality, composition, film thickness, and lattice matching. Rocking curves scans are performed using symmetric reflections, such as the (004) plane.

Another valuable measurement is reciprocal space mapping (RSM), which gives information on strain in the structure. RSM show spreads and relationships between peaks. RSM can be used to analyze tilt, relaxation, and lattice mismatch, which are all

key elements to understanding the growth of these structures. RSM requires the use of asymmetric reflections for determining in-plane strain.

In this study, rocking curve and RSM scans from symmetric/asymmetric reflections were used to examine the impact of the process conditions on the structural properties of ~6.1Å heterostructures. The structural properties studied include composition, strain, lattice spacing, and thickness.

3.2.3 Principal component analysis

Directly comparing the RHEED signals resulting from different process conditions provides limited information about the physical properties of the structure including the quality of the interface. Likewise, developing a model based on a time series of RHEED intensity oscillations consisting of hundreds of data points is impractical. Principal component analysis (PCA) is a method that can help overcome some of these difficulties. PCA compresses multivariate data into principle components (PCs), which represent the primary components of the variance in the signals [33].

The PCA technique allows the RHEED data to be used to develop process models. Since RHEED generates voluminous data arrays, the ability to reduce the dimensionality of RHEED data has practical implications. Some promising applications include in-situ characterization of structures being produced, as well as the detection of drift in the process environment. The application of PCA on multivariate RHEED data affords the identification of significant changes in the growth process. PCA transforms the original, sizeable data arrays into new variables, which are uncorrelated. The new variables are termed principle components (PCs). They are ordered such that the first few

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components account for most of the variation in the original data set and the last few contain the least.

In this study, subtle differences in the formation of the inverted heterojunction and the impact on the physical properties are of interest. RHEED observations are recorded to study the formation of the heterojunction and the resultant changes in growth process. The variance in the various RHEED signals can be used to gain more knowledge about the heterojunction. PCA is particularly useful in this approach as it concentrates on the variances of the RHEED data array. If x is a vector of p random variables (such as a RHEED time series signal), the first task is to determine a linear function, $\alpha_1'x$, of the elements of x that exhibits the maximum variance. Here, α is a vector of p constants, where p is the number of data points in the RHEED signal. The variable, $\alpha_k'x$, is the kth PC. This is mathematically expressed as:

$$\alpha_1'x = \alpha_{11}x_1 + \alpha_{12}x_2 + \ldots + \alpha_{1p}x_{1p} = \sum_{j=1}^{p}\alpha_{1j}x_j. \qquad (14)$$

Then, another linear function, $\alpha_2'x$, which is uncorrelated with $\alpha_1'x$ is determined that represents the maximum variance. This process is repeated until p PCs are found.

In order to find the PCs, consider a vector x that consists of p random variables. Let Σ be the covariance matrix of x. The covariance matrix is the matrix whose (i,j)th element is the covariance between the ith and jth elements of x when $i \neq j$. When $i=j$, the (i,j)th element is the variance of the jth element x. For $k = 1,2, \ldots, p$, the kth PC is given by

$$z_k = \alpha_k' x \hspace{5cm} (15)$$

where α_k is an eigenvector of Σ corresponding to its kth largest eigenvalue λ_k. If α_k is chosen to have unit length (i.e., $\alpha_k' \alpha_k = 1$) as described above, then the variance of $z_k = \lambda_k$. Generally, if these eigenvalues are ordered from largest to smallest, then the first few PCs will account for most of the variation in the original vector x. In this formulation, each of the sequences of RHEED intensity values is the x vector, and p represents the number of intensity values. As many as p PCs can be found; however, the remaining PCs can be discarded if the variation in x is represented by for the first few PCs.

PCA was performed on a data array of RHEED signals recorded at the specular spot. Each signal represented consecutive intensity values during formation of the critical heterojunction. Before PCA was performed on the data, one hundred (100) consecutive intensity values for each RHEED signal were selected, beginning at the end of the antimony soak on the AlSb sublayer. The first few PCs were selected that account for a majority of variance in the RHEED signals. These PCs were subsequently used as inputs for a multi-layer neural network, which is described in the next section

3.2.4 Neural network modeling

Complex relationships exist between film growth conditions and physical properties of a semiconductor material or structure. The relationships are not well understood, but can be modeled empirically using artificial neural networks. Neural networks represent a powerful tool that is useful for mapping relationships between non-linear or noisy data sets.

Neural network modeling affords many useful capabilities that are beneficial to compound semiconductor fabrication. The advantages of using neural networks include, but are not limited to, the following: non-linearity, adaptivity, input-output mapping, evidential response, fault tolerance, and neurobiological analogy [34]. This study benefits from the non-linearity and input-output mapping capabilities of neural networks. Whereas linearity can be represented using standard regression models, applications such as compound semiconductor fabrication, stock market analysis and voice recognition are inherently non-linear. They benefit specifically from the capabilities of neural networks. Neural networks are advantageous from a financial and technological standpoint. Understanding the relationships between MBE process conditions and thin film properties is critical to the improvement of compound semiconductor fabrication. The MBE process models developed in this study are developed using this method.

A neural network can be described generally as a machine that models the way in which the brain performs a task or function. It has found great use in computational tasks, including modeling, signal processing, and pattern recognition. Neural networks are finding widespread use because of their ability to learn and generalize. For example, a neural network can learn from input data and provide a reasonable output from data not encountered during the learning process. Neural networks have previously been demonstrated to be an effective tool for modeling the effects of MBE process conditions on film qualities [35].

Artificial neural networks are crudely modeled after the human brain. Like the brain, artificial neural networks operate in an efficient manner. With their parallel-like structure,

they contain processing elements (neurons) with many interconnections between them. A diagram of a typical neural network is shown in Figure 9.
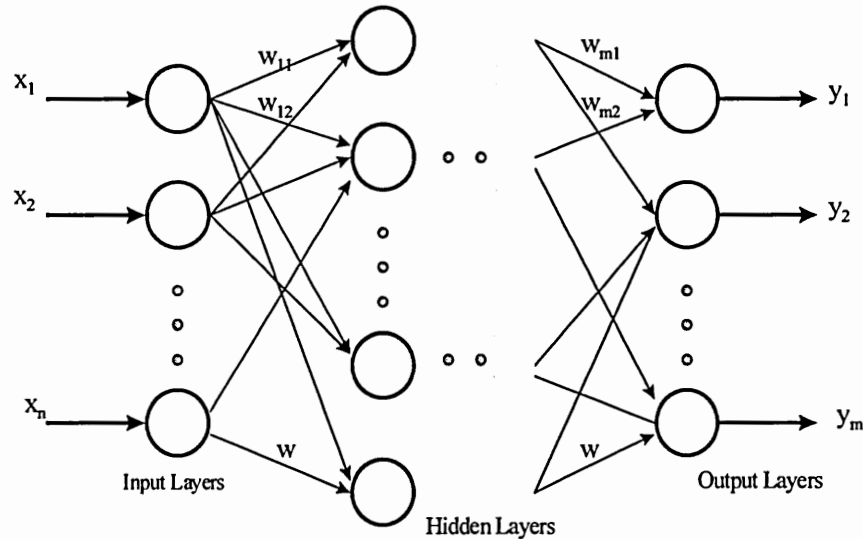
Figure 9. Diagram of neural network

A neural network is comprised of at least three basic layers: (1) input, (2) hidden, and (3) output. It can mimic or "learn" the relationships between the input and output. This is accomplished by training of the neural network with a set of training examples. In this study, the network inputs represent the MBE process conditions, and the outputs represent the responses to be modeled. The neurons contained in each layer are interconnected in such a way that information about the relationships between the input and output is stored in the weights between connections.

The basic elements of the neuron are the connection, the adder, and the activation function (Figure 10). The connecting links between the neurons are known as synapses. The synapses are characterized by the weights assigned to them. The adder determines

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the weight or strength of a neuron by summing the weights of its input signals, or synapses. As the network is trained, the weights of synapses are adjusted so that the network output approaches the desired output. The activation function serves to limit or "squash" the amplitude of the output of the neuron to some finite value.
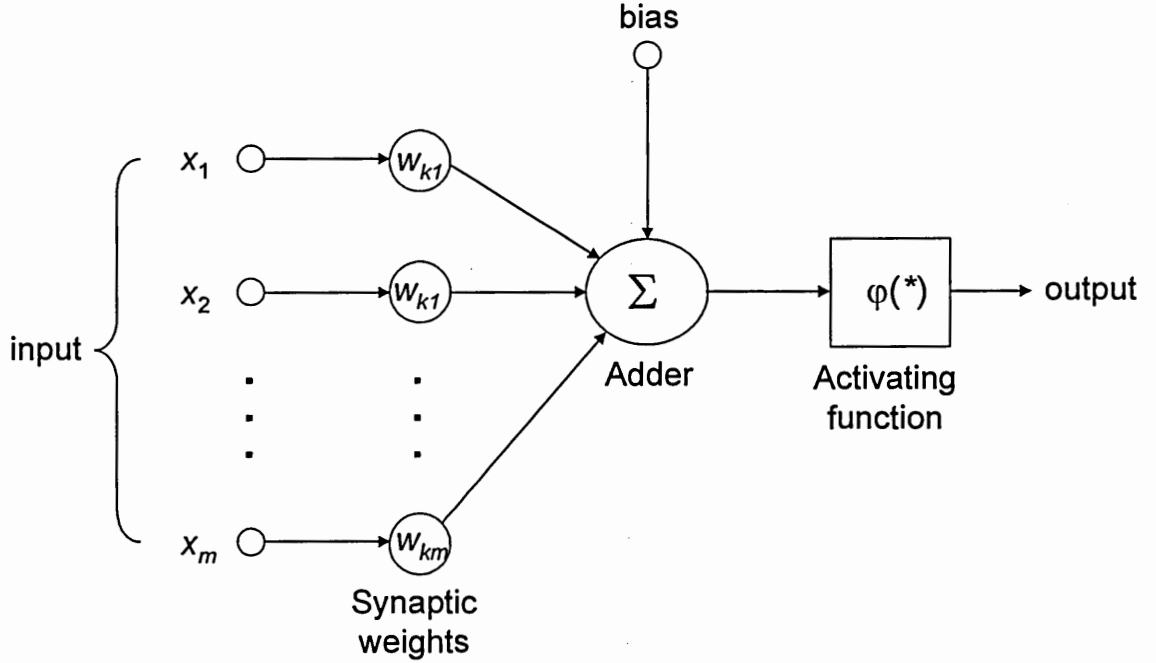
Figure 10. Model of a neuron

The models presented herein were developed using the error back-propagation (BP) algorithm [34]. This learning algorithm uses two passes, both forward and backward computations. To begin the learning process, weights of the neurons are randomized and a set of training examples is passed through the neural network. The outputs of neurons in the lth layer become inputs to the neurons in the next layer k. The internal activity level $s_j^{(l)}(n)$ for neuron j in layer l is

$$s_j^{(l)}(n) = \sum_{i=0}^{p} w_{ji}^{(l)}(n) o_i^{(l-1)}(n) \qquad (16)$$

where $o_i^{(l-1)}(n)$ is the function signal of neuron i in the previous layer $(l-1)$ at iteration n, $w_{ji}^{(l)}(n)$ is the synaptic weight of neuron j in layer l that is fed from neuron i in layer $l-1$, and p is the number of neurons in the lth layer. For $i{=}0$, $o_0^{(l-1)}(n) = -1$ and $w_{j0}^{(l)}(n) = \theta_j^{(l)}(n)$, where $\theta_j^{(l)}(n)$ is the threshold applied to neuron j in layer l. Then, the output signal of neuron j in layer l is

$$o_j^{(l)}(n) = \begin{cases} \dfrac{1}{1+\exp[-s_j^{(l)}(n)]}, & 1 \le l < L \\ y_j(n), & l = L \end{cases} \tag{17}$$

where $x_j(n)$ is the jth element of the input vector in the first hidden layer (i.e., $l{=}1$), and L denotes the last layer. The output of the network, $y_k(n)$, is then compared with the desired response, $d_k(n)$, and the error signal is generated. The error signal is mathematically expressed in equation 16:

$$e_k(n) = \tfrac{1}{2} [\, d_k(n) - y_k(n)]^2 \tag{18}$$

where $e_k(n)$ is the error of neuron k at time step n. This error signal is used to apply a corrective adjustment to the neuron. The error signal is minimized using the generalized delta rule based on the gradient descent approach. The expressions for the weight changes (i.e., "deltas") of the output layer and other layers are:

$$\delta_j^{(L)}(n) = [\hat{y}_j - y_j^{(L)}(n)]y_j(n)[1 - y_j(n)] \tag{19}$$

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$$\delta_j^{(l)}(n) = o_j^{(l)}(n)[1 - o_j^{(l)}(n)]\sum_k \delta_k^{(l+1)}(n)w_{kj}^{(l+1)}(n) \qquad (20)$$

Once the outputs of the last layer are calculated, weights are updated by the deltas for each node calculated from the output layer and back-propagated to the input layer. The generalized delta rule is:

$$\Delta w_{ji}^{(l)}(n) = [w_{ji}^{(l)}(n) - w_{ji}^{(l)}(n-1)] \qquad (21)$$

$$w_{ji}^{(l)}(n+1) = w_{ji}^{(l)}(n) + \eta \delta_j^{(l)}(n)o_i^{(l-1)}(n) + \alpha \Delta w_{ji}^{(l)}(n) \qquad (22)$$

where n is the number of iterations, η is the *learning rate*, and α is the *momentum*. The learning rate is a constant that represents the rate at which a weight will be changed along its slope to the minimum error. The momentum coefficient is a constant that includes a portion of the previous weight change. The momentum coefficient, generally ranges between 0 and 1, may have the benefit of preventing the learning process from terminating in a shallow local minimum on the error surface.

When the network is fully trained, appropriate weights, w_{kj}, are derived such that the network output represents the relationship between the inputs and outputs of the data set. Networks are typically trained and tested with 75% and 25% of the data set, respectively.

Chapter 4 Results/Evaluations

Exploring the growth of 6.1Å structures will lead to a greater understanding of the issues that impact mobility in InAs-AlSb quantum well structures. As described in Chapter 1, some key concerns include the microstructural quality of the As/Sb heterojunction interface and the tremendous impact of the interface on the growth of subsequent InAs channel layers. In these pseudomorphically grown structures, the transport properties are sensitive to interface bonding [13] and quantum well properties [28]. The relationships between the former and the latter are unclear. This study is comprised of several experiments aimed at revealing parameters that affect the properties of these structures. The parameters under study were controlled within the MBE process environment. They include substrate temperature, overpressure, doping, shutter sequence, and composition. The importance of the InAs-on-AlSb heterojunction in InAs/AlSb device structures has been previously identified. Empirical models that describe these structures would be useful for optimizing electronic properties. In this study, *in-situ* process monitoring was used to acquire real-time data during the formation of these interfaces. The experiments were designed for eventual modeling of the growth process.

It is demonstrated in this chapter that the properties of these structures are dominated by a few monolayers at the InAs-on-AlSb interface. The process conditions at the InAs-on-AlSb interface prove to be influential. Using RHEED, the growth process was examined via specular spot intensities. The RHEED data was analyzed using PCA and used to demonstrate the feasibility of RHEED as a characterization tool. RHEED data was used to predict thin film properties.

MBE process conditions were also explored to achieve a range of conductivities in 6.1Å HEMT structures. Results are presented that demonstrate the relationships of the process parameters to the properties of 6.1Å HEMT structures. The HEMT structures are analyzed, and the optimum process conditions are identified. Process models developed using neural networks. The models are used to make inferences about the growth process, predict film properties, and distinguish between the most influential MBE process parameters.

The following sections describe experiments performed using a Varian Gen-II MBE system. The experiments can be categorized as follows: interfacial roughness at the inverted interface, RHEED analysis of the inverted interface, the growth of unintentionally-doped and Be-doped structures, and the impact of buffer/barrier characteristics on HEMT properties. HEMT structures are characterized using XRD, Hall measurements, and RHEED.

4.1 Interfacial Roughness

Studying interfacial roughness in these structures is challenging. The reactivity of AlSb when exposed to atmosphere complicates the morphological study of the InAs-on-AlSb surface. Consequently, cap layers are required to shield the antimony sublayer from oxygen contamination that immediately degrades the surface. Common approaches for examining mixed-anion (cation) interfaces employ superlattice structures that are analyzed using optical or cross-section-capable characterization techniques. While superlattice structures overcome oxygen contamination issues, areal images of the interface are unattainable using this approach. In the present study, thin (≤5 ML) InAs

layers serve as the protective barriers as surface roughness of the inverted interface is analyzed.

Previous studies describe atomic-scale roughness at the interface and compositional profiles in subsequent layers resulting from anion exchange and segregation [36, 37]. In a recent study, Nosho, et al. [38] described the formation of nanowires during MBE-growth of InAs/GaSb superlattices. Using cross-sectional scanning tunneling microscopy (XSTM), periodic nanowires were observed that exhibited widths of 120 nm for several microns in length. Similar observations were seen in the As/P system [30]. Yang, et al. exposed InP buffers to an arsenic flux that produced nanowires with an average height of 1.9 nm. In this section, experiments were performed using thin (≤ 5 monolayers) InAs protective layers. Micron-long InAs quantum wires with estimated widths ranging from 160 nm to 210 nm were observed.

4.1.1   Experimental Technique

Epitaxial layers were grown using Group-V (As$_4$, Sb/Sb$_2$) stabilized growth conditions, where the growth rates for AlSb, GaSb, and InAs were 2.0 μm/hr, 1.0 μm/hr, and 0.5 μm/hr, respectively. Structures were grown on ¼-GaAs (001) substrates and rotated during epitaxy. The growth temperatures were determined with reference to the de-oxidation temperature of GaAs (~580°C). This test structure consisted of the following (from cap layer to substrate): InAs protective layer / 200-nm Al$_{0.66}$Ga$_{0.33}$Sb / (5-nm AlSb / 5-nm GaSb) X15 / 2-μm AlSb / 300-nm GaSb / 200-nm GaAs buffer / semi-insulating. After growth of the Al$_{0.66}$Ga$_{0.33}$Sb layer, antimony impinged on the surface for twenty seconds, until the antimony valve and shutter were simultaneously

closed. Three monolayers of indium were then deposited on the surface, followed by an arsenic exposure of flux $As_4 = 7 \times 10^{-6}$ Torr. In the second experiment, the same structure was produced, followed by the growth of two additional InAs monolayers. The InAs protective layers for the experiments were targeted at three and five monolayers, respectively. After the protective layers were deposited, samples were cooled, promptly removed from the MBE system, and characterized using AFM.

4.1.2   Results

AFM measurements were performed on small sections from the samples. The images appear in Figures 1a and 1b. Scan sizes were limited to 10 x 10 μm. The AFM measurements show a mean surface roughness of 1.45 nm and 2.039 nm for interfaces with three and five ML InAs protective layers, respectively. The formation of micron-long quantum wires with estimated widths ranging from 160 nm to 210 nm was observed. These results are comparable with widths in [38] and average height in [30]. The difference in average surface roughness is accounted for by the difference in cap layer thickness.

Since the growth of heterostructures is subject to the effects of both in-plane strain at the interfaces (owing to lattice mismatch) and the exchange of anions/cations across heterointerface, it is not surprising that nanoscale undulations appear at the InAs-on-AlSb interface. In the InP/InAs system that experiences a 3.2% lattice mismatch, the formation of nanowires was driven primarily by the exchange of anions across the heterointerface [30]. For the InAs-on-$Al_xGa_{1-x}Sb$ interfaces shown in Figure 11, the

indium-terminated surface inhibits the exchange of impinging arsenic with the sublayer [39].
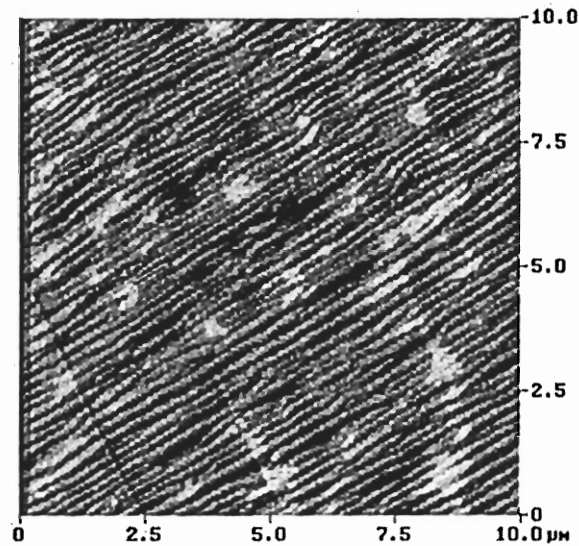
(a)
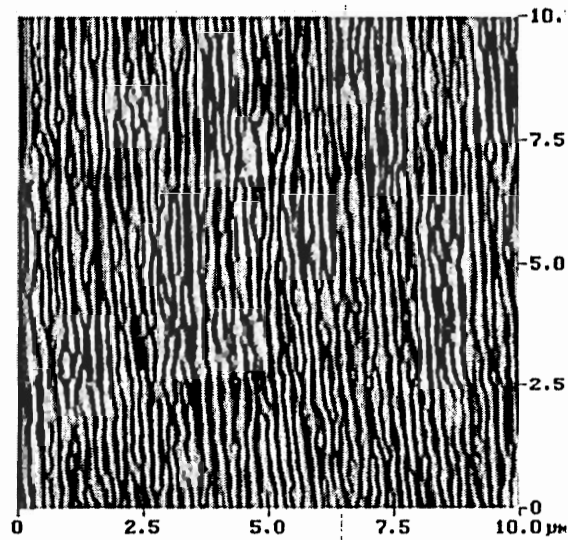
(b)

Figure 11. AFM results for structures with: (a) 3 ML of InAs; (b) 5 ML of InAs

Smoothing of the antimony-sublayer was performed using extended antimony soak times [20] prior to the deposition of indium. Similar HEMT device structures were produced at these growth conditions, and x-ray diffraction (XRD) reciprocal space maps confirmed

relaxation of the buffer layers. Hall measurements of those structures demonstrated high electron mobility [39].

The thin InAs protective layers in these structures should be under tensile strain, since the buffers exhibit larger lattice spacing. This is not supported by the strain analysis of identical structures (section 4.5.3). These structures show signs of antimony segregation into the InAs layer. As long as antimony segregates from the sublayer and becomes incorporated into the subsequent InAs layer, the resulting $InAs_xSb_{1-x}$ layer is subjected to compressive strain that is proportional to the antimony composition. Kaspi reported that antimony surface riding is inversely proportional to the distance from the As/Sb interface [40]. Similarly, these thin (<5 monolayers) InAs layers should contain antimony.

The consequences of thin InAs protective layers on $Al_xGa_{1-x}Sb$ in this study include enhanced strain at the interface - due to a greater mismatch between $Al_xGa_{1-x}Sb$ - and an Sb-rich InAs layer (<5.4%). As a result of the lattice mismatch, the InAs-on-$Al_xGa_{1-x}Sb$ becomes deformed during the initial stages of growth, stemming from considerable sublayer-anion incorporation [30] and anisotropic stress relaxation [41]. The induced strain generated from antimony incorporation into the subsequent layer is relieved in a single direction and spontaneously produces periodic undulations in as few as 3 ML of InAs growth. RHEED images recorded during this interfacial growth sequence show no sign of surface roughening from arsenic exposure on indium-terminated surfaces, as suggested by streaky (2 x 4) arsenic-stabilized patterns.

Investigating the induced surface roughness at the inverted interface of InAs/$Al_xGa_{1-x}Sb$ HEMT structures presents an opportunity to refine their growth, thus

improving device performance. The surface roughness results show evidence that strain relief at the InAs-on-$Al_xGa_{1-x}Sb$ interface produces undulations that subsequently transform during continuous InAs layer growth and longer arsenic flux exposure. Nanowires were formed whose average heights and widths were comparable to those seen in As/P and As/Sb systems.

4.2 RHEED Analysis of Inverted Interface

RHEED is a diagnostic tool that allows *real-time* monitoring of the growth surface. With a strong dependence on the quality of the inverted interface, the properties of MBE-grown InAs-AlSb heterostructures vary with process conditions. Therefore, the use of RHEED is a practical approach for studying the relationships between the process conditions and the physical properties in these structures.

The most common analyses of MBE-grown structures are performed post growth. These techniques including XRD, CS-STM, TEM, and Hall analyses to describe the structural and electronic properties. Still, uncertainties regarding the growth dynamics at critical interfaces and throughout critical layers remain. By employing RHEED during the growth of mixed-anion structures, real time data can be obtained that leads to a better understanding of the growth process. In this section, RHEED data is used to develop process models. RHEED specular spot intensities were recorded during formation of the InAs-on-$Al_xGa_{1-x}Sb$ heterointerface.

4.2.1 Experimental Technique

The test structure and growth technique are equivalent to those described in Section 4.1.1. After the deposition of indium at a given substrate temperature, arsenic flux impinged on the surface for the remainder of RHEED data acquisition. MBE process conditions and ranges examined at the inverted heterojunction consist of the following: indium concentration deposited (1-2 ML); substrate temperature (460°-520°C); and arsenic overpressure ($1.4*10^{-6} - 7 \times 10^{-6}$ Torr). In the figures below, RHEED specular spot intensities were organized by substrate temperature and indium concentration. The RHEED signals at time t=0 refer to the beginning of indium deposition on $Al_xGa_{1-x}Sb$ sub layer. The dash line represents opening of the arsenic shutter.

-▲- 460 1-ML with 1.4e-6
-⊖- 460 1-ML with 2.8e-6
-□- 460 1-ML with 4.9e-6
-◇- 460 1-ML with 7e-6
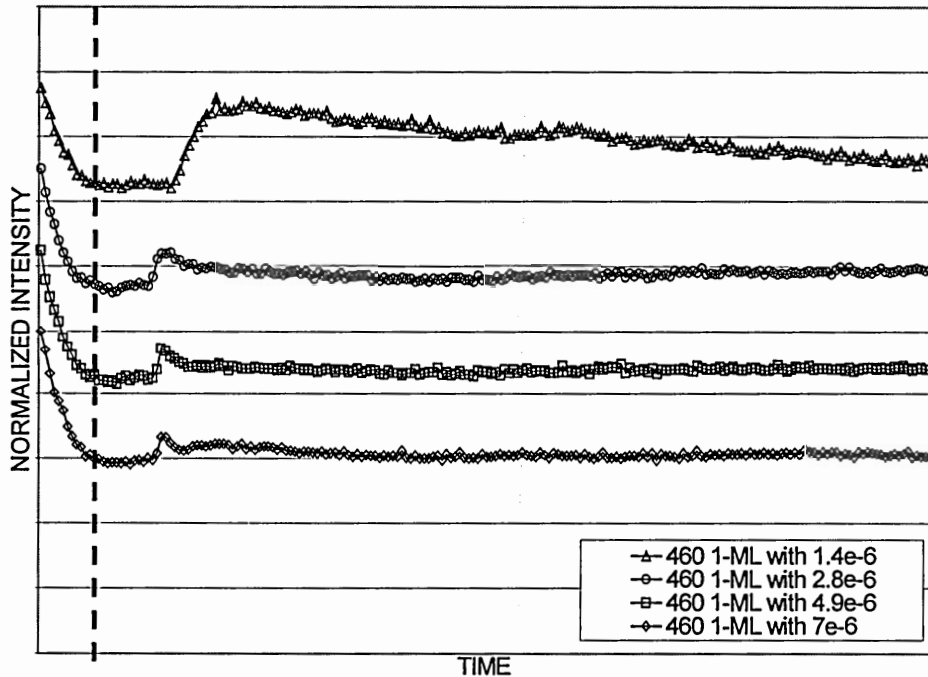
(a) Ts=460°C, 1-ML of indium
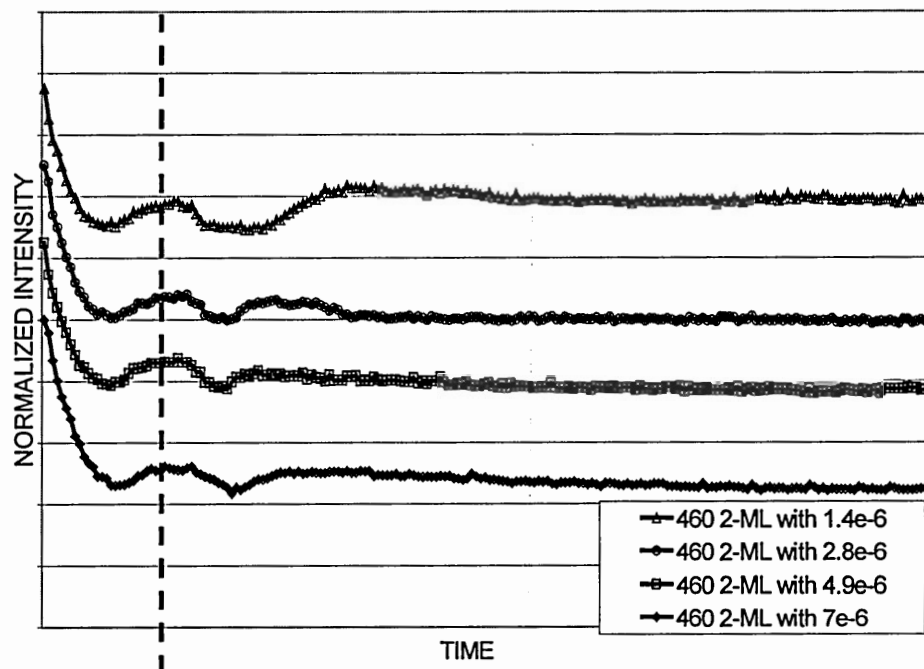
(b) Ts=460°C, 2-ML of indium
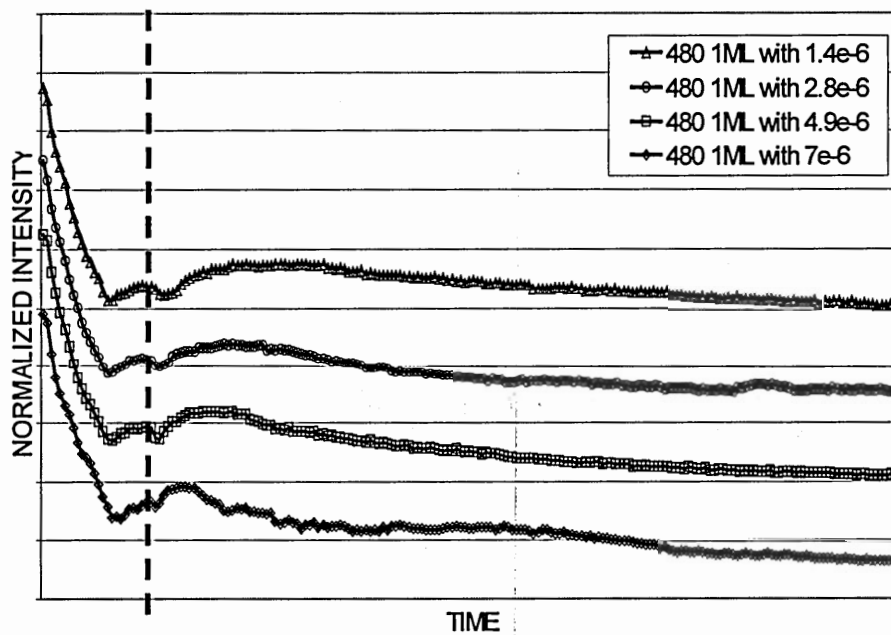
(c) Ts=480°C, 1-ML of indium
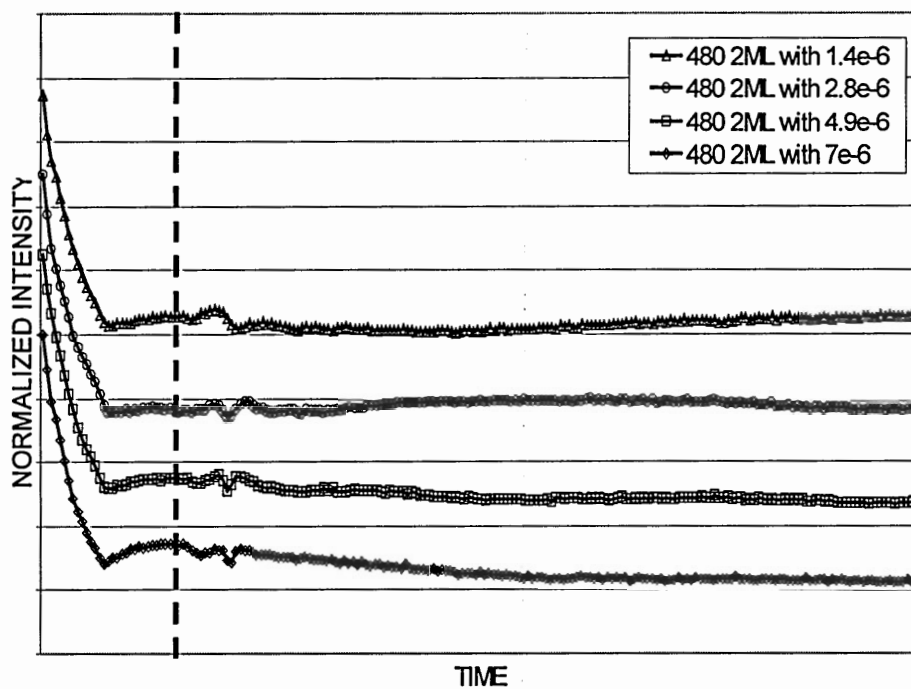
(d) Ts=480°C, 2-ML of indium
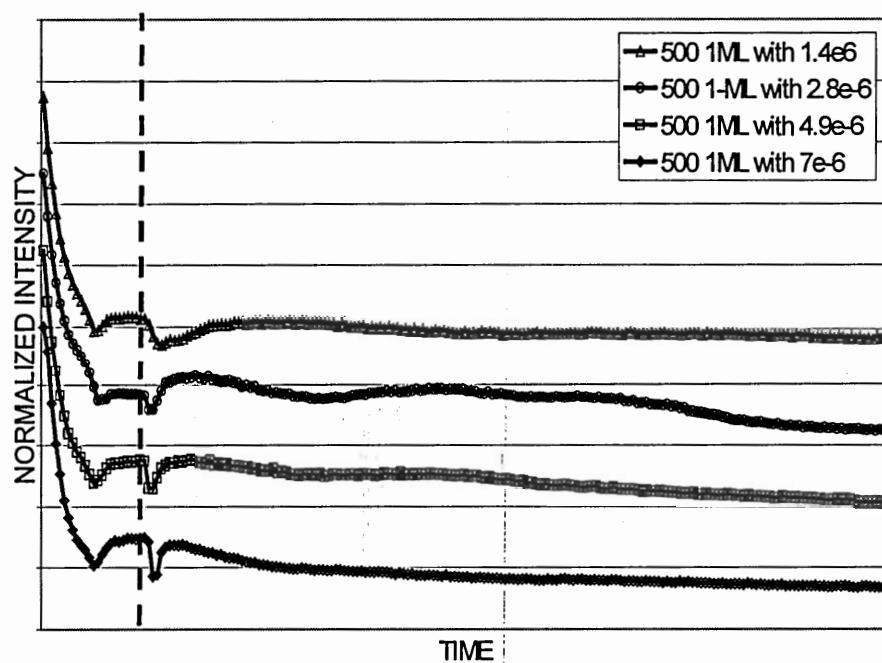
(e) Ts=500°C, 1-ML of indium

64
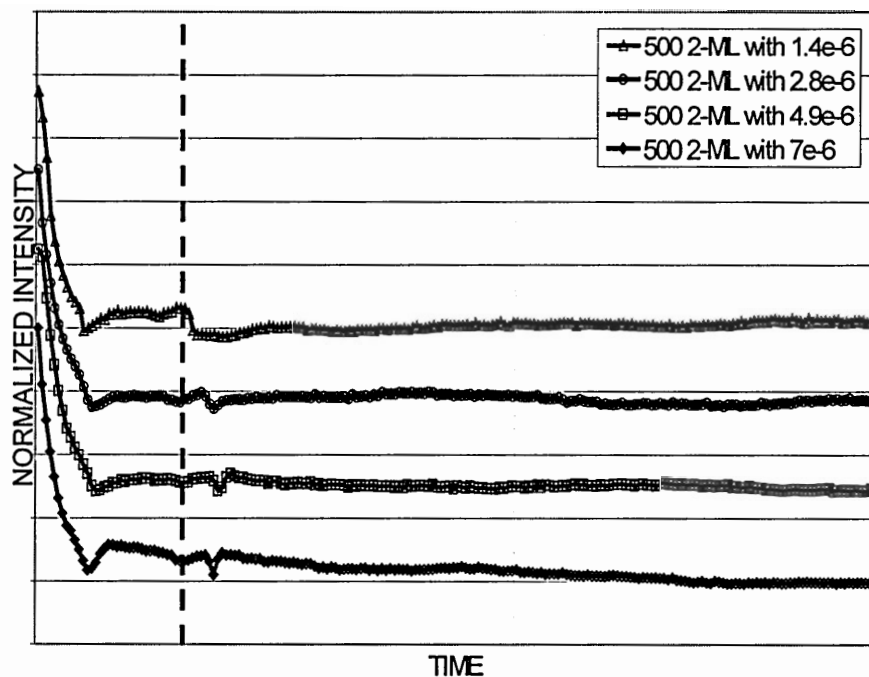
(f) Ts=500°C, 2-ML of indium
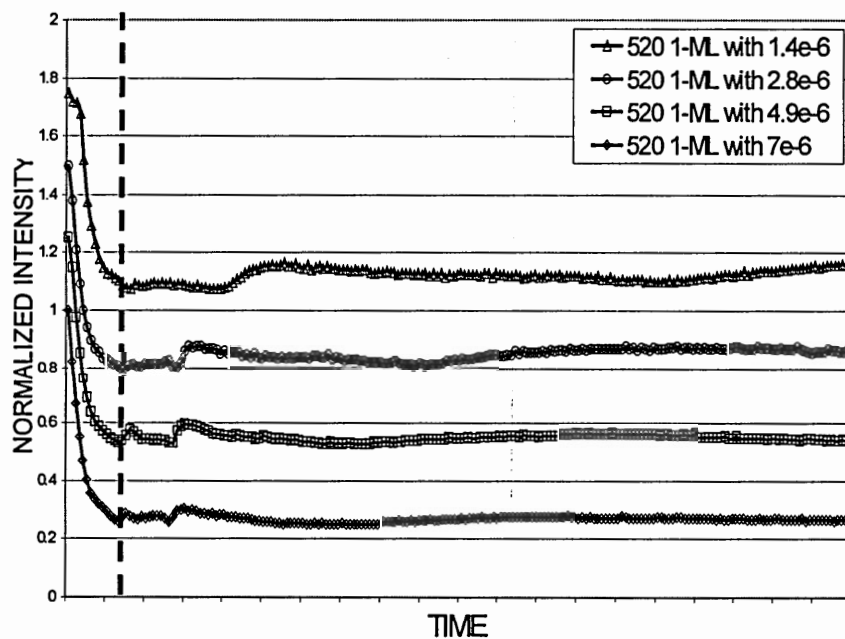
(g) Ts=520°C, 1-ML of indium

(h) Ts=520°C, 2-ML of indium
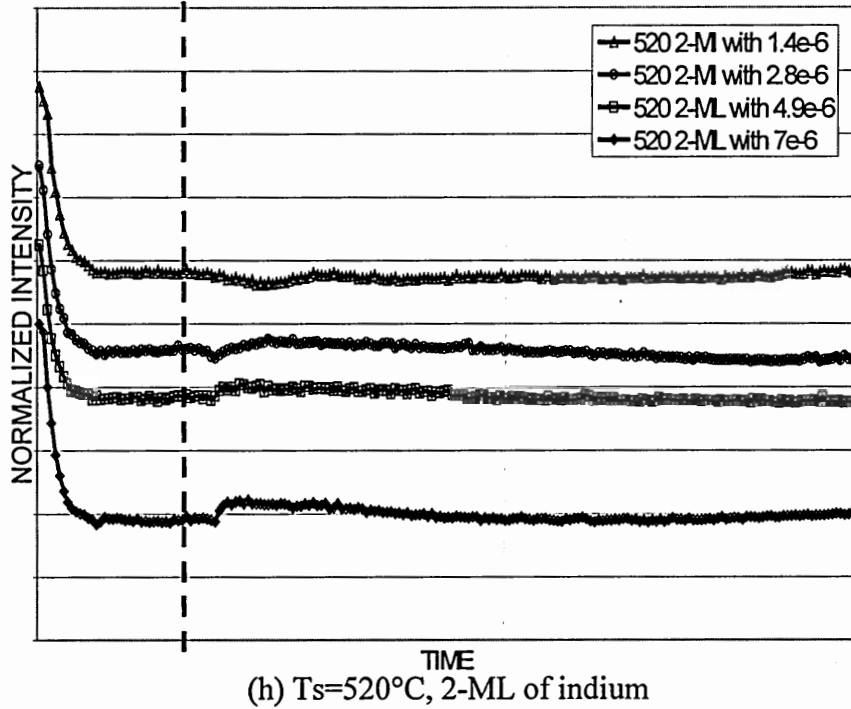
Figure 12. RHEED specular spot intensities for varying indium barrier thickness, substrate temperature and arsenic overpressure (a-h). The dashed line indicates when the arsenic shutter opened.

4.2.2 Arsenic overpressure

Arsenic overpressure is required for InAs crystal growth. At the InAs/AlSb interface, impinging arsenic atoms interact with the sublayer. This behavior results in a non-linear interfacial profile that affects the physical properties. Furthermore, arsenic that is diffused into the sublayer impacts the transport properties in InAs quantum well structures. The RHEED observations confirm that for 1-ML of indium deposited at substrate temperatures (460-520°C), the surface roughens with higher arsenic overpressure. The figures also illustrate that increasing arsenic flux and substrate temperature, as suggested by a continual decrease in specular spot intensity, stimulates roughening.

The uptake of indium by arsenic is observed through the simultaneous increase in intensity when the arsenic shutter opens. This sudden rise in intensity is dependent on arsenic overpressure. After this initial bump, the time it takes the intensity to return to its initial value decreases with increasing overpressure. This confirms that: (1) the exchange (or conversion) process is slower for lower arsenic overpressure; and (2) arsenic diffuses further into the sublayer with increasing overpressure. During the growth of InAs/AlSb structures, high arsenic-to-indium flux ratios produce high quality InAs layers. For instance, the InAs/AlSb HEMTs produced in this thesis were grown with arsenic overpressure, $P_{As} = 7.0 \times 10^{-6}$ Torr for an InAs growth rate of 0.5ML/s. This study recommends the use of lower arsenic overpressure at the InAs-on-AlSb interface.

4.2.3 Indium barrier thickness

Indium deposited at the InAs/AlSb interface serves to promote InSb bonds, which results in higher electron mobility for AlSb/InAs/AlSb quantum wells [3]. More specifically, indium-stabilized nucleation at the heterojunction produces smoother films [42]. As a barrier for impinging arsenic atoms, indium can be used to create abrupt InAs/AlSb heterojunctions. In this thesis, the RHEED observations confirm a rougher growth surface for interfaces with 2-ML(s) of indium compared to those with 1-ML. Higher concentrations of indium appear to lead to the onset of three-dimensional growth. However, it is also observed that indium desorption is enhanced at higher substrate temperature. Therefore, the amount of indium deposited at the heterojunction for the formation of an abrupt interface varies according to the growth temperatures of the InAs

layer. This is in agreement with Schaffer, et al. [42], who observed a dependence on substrate temperature for InAs nucleation on GaAs.

4.2.4   Substrate temperature

The influence of substrate temperature on surface characteristics at critical heterojunctions is important. In relation to InSb bond formation, temperature impacts indium surface coverage at the InAs/AlSb interface, thereby affecting the transport properties in the InAs quantum well. In the RHEED experiments performed, decreasing specular spot intensity is observed with increasing substrate temperature. Clearly, surface roughening is stimulated by substrate temperature. At 460°C for all arsenic overpressures, oscillatory behavior was observed that appears similar in nature to observations of layer-by-layer anion stabilized growth. These oscillations confirm the uptake of deposited indium by impinging arsenic. This is less apparent at higher substrate temperatures. The differences among the intensity profiles at higher substrate temperatures are less pronounced, proving that substrate temperature is an overriding process condition. For the growth of abrupt InAs/AlSb heterojunctions, the substrate temperature corresponsd with the preservation of indium that prevents the diffusion of ensuing arsenic flux.

4.3   Unintentionally doped HEMT structure

Barriers to reproducible devices exist when growing structures with mixed anion interfaces. In these structures, As/Sb interfaces are known to be affected by anion

intermixing and exchange [5, 43]. Reasons for this are not yet well understood and are related to growth processes and structural properties. Likewise, the charge in these quantum well structures is difficult to control and also related to the quality of the epilayers and interfaces. These issues are addressed by examining the growth of unintentionally doped structures. In this set of experiments, RHEED data and MBE process conditions are used to model the electron mobility in InAs/AlSb HEMT structures. Predictive models are developed using neural networks. It is demonstrated that information about the quality of the As/Sb mixed interface is present in the RHEED data, and this data can be used to model device performance parameters.

4.3.1   Experimental Technique

The test vehicle in this study was an InAs-$Al_{0.66}Ga_{0.33}Sb$ HEMT structure developed in previous experiments. The HEMT structure is shown in Figure 13.

GaSb layer 3nm

AlSb 17nm

InAs 15nm

$Al_{0.66}Ga_{0.33}Sb$ 200nm

AlSb (5nm)

GaSb (5nm)

AlSb 2um

GaSb 300nm

GaAs 200nm

GaAs substrate

Superlattices (15x)
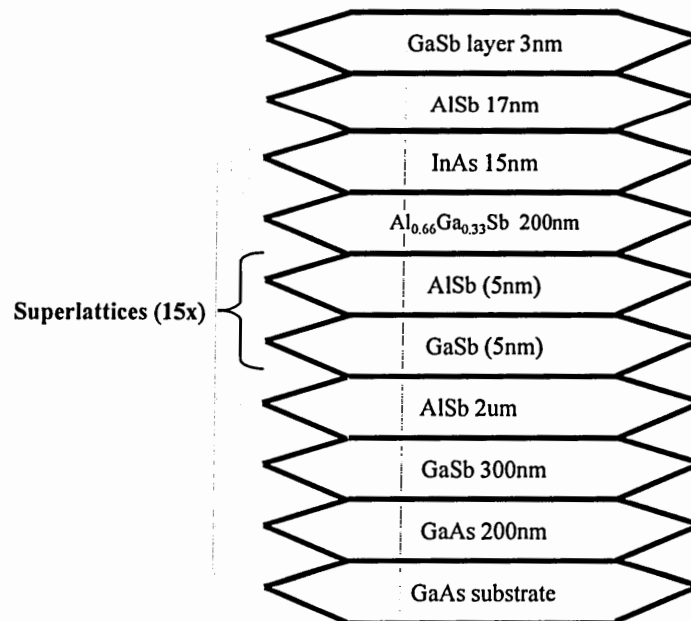
Figure 13. InAs-AlGaSb based HEMT test Structure

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The structure from cap layer to substrate consists of the following: 3-nm GaSb / 17-nm AlSb / 15-nm InAs / 200-nm $Al_{0.66}Ga_{0.33}Sb$ / (5-nm AlSb / 5-nm GaSb) X15 / 2-µm AlSb / 300-nm GaSb / 200-nm GaAs buffer / GaAs substrate. The HEMT structures were grown on one-quarter of 2"-GaAs (100) undoped substrates. Samples were mounted in indium-less *EPI* substrate assemblies. Experiments were performed under Group-V stabilized conditions, where the growth rates for In, Ga, and Al were 0.5, 1.0, and 2.0 µm/hr, respectively. Arsenic tetramers (As_4) and antimony dimers/monomers (Sb_2/Sb) were used in these experiments. All samples were rotated during growth, except when RHEED specular spot intensities were recorded during the formation of the InAs-on-AlGaSb interface. The growth temperatures were determined using the deoxidation temperature of GaAs substrates (~580°C). The experiments focus on the formation of the inverted InAs-on-AlGaSb interface. At this interface, a twenty-second Sb soak, followed by indium deposition, preceded InAs channel growth. The Sb soak was used to saturate the surface sites with Sb atoms, so that an InSb-like bonding configuration could be formed.

4.3.2   Experimental Design

Since the conversion of the inverted interface into InSb-like bonds is required for high electron mobility, the growth conditions before and during the growth of the InAs channel are critical [3]. Typically, Sb soaks or deposition of one indium monolayer are used to form the InSb-like bonds. Previous work [5] describes the amount of indium

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necessary to create a smooth InAs/AlSb interface. This report suggests that more than one indium monolayer is required to make up for the compositional difference in the two reconstructions. In an attempt to illuminate the impact of In on the bond configuration of the interface, channel growth temperature and indium barrier thickness at the interface are varied. A statistically designed experiment is used. This design is a 2^2 factorial central composite circumscribed (CCC) experiment requiring eleven runs [44]. Table 2 shows the factors, ranges and units of the parameters studied.

Table 2. Input factors, range and units

Input factors	Range	Units
Indium barrier	3 to 15	Å
Channel temperature	445 to 490	°C

4.3.3 Characterization

For each experiment, 5 x 5 mm Hall samples in the clover-leaf van der Pauw pattern were produced and measured at a magnetic field intensity of 3020 Gauss. Hall measurements were taken at temperatures of 300 °K and 77 °K. RHEED signals were recorded for each experiment, beginning with the Sb soak on the AlGaSb layer (Figure 14).
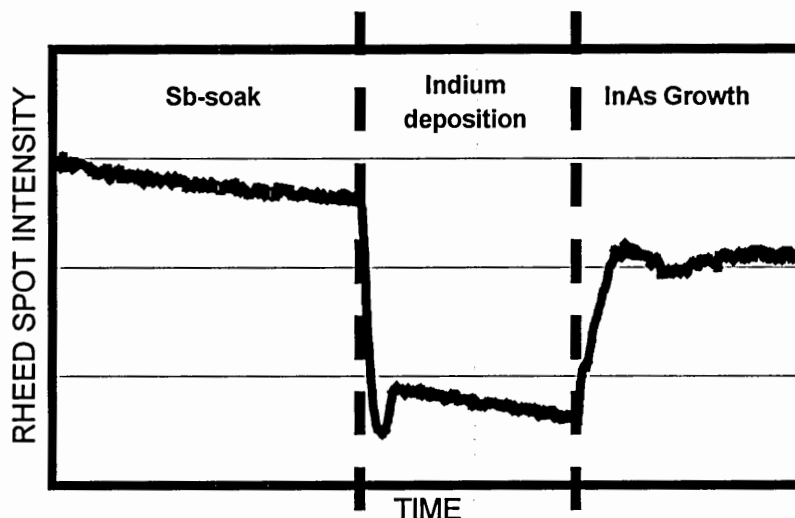
Figure 14. Reflection high-energy electron diffraction (RHEED) signal acquired during the growth of the InAs/AlSb interface

4.3.4 RHEED Analysis

The RHEED signals are the intensity oscillations observed at the specular spot of the "1X" side of 1 X 3 AlSb Group V-stabilized RHEED pattern. The RHEED data includes intensity oscillations at interface, as well as during the growth of the subsequent InAs layer. The process conditions and the results are provided in Table 2.

Table 3 Growth parameters and 300 °K and 77 °K Mobility Results

INDIUM BARRIER (Å)	CHANNEL TEMP = 460 °C+	77 °K MOBILITY (cm^2/V/s)	300 °K MOBILITY (cm^2/V/s)
15	-15	95038	24773
3	30	106792	29356
17.48	7.5	135367	24259
15	30	80257	25716
3	-15	91439	28520

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Table 3 (cont'd)

9	39.31	98921	24797
1.3	7.5	101738	31954
9	7.5	137729	28188

4.3.4.1   Neural network modeling

The relationships between film growth conditions and electron transport are not well understood, but can be modeled empirically using neural networks. Neural networks have previously been demonstrated to be an effective tool for modeling the effects of MBE process conditions on film qualities [35]. The process models presented are developed using this method.

During network training, inputs represent RHEED data, and the outputs represent the electron mobility. The models presented are developed using the error back-propagation (BP) algorithm [35], which is described in Chapter 3. Recall that the input data is first passed through the network using a random set of weights. The output of each neuron is a weighted sum of its inputs, filtered by a sigmoidal "squashing" function. At the final layer, the network outputs and training data are compared, and the mean-squared-error between then is calculated. The error is fed back into the network, where the weights are re-adjusted to minimize the output error. Networks are typically trained and tested with 75% and 25% of the data set, respectively.

4.3.4.2   Principle Component Analysis

Directly comparing the RHEED signals resulting from different process conditions does not provide information about electron transport or the quality of the interface. Likewise, developing a model based on a time series of RHEED intensity oscillations consisting of hundreds of data points is challenging. As described in Chapter 2, principle component analysis (PCA) is a method that can help overcome some of these difficulties. PCA compresses the RHEEED data into principle components (PCs), which represent the primary components of the variance in the signals [33]. This section describes the method used to analyze the RHEED signatures.

Before PCA was performed on the data, one hundred consecutive intensity values for each RHEED signal were selected beginning with the initiation of the indium deposition. Six PCs were selected, accounting for 99% of the variance in the RHEED signals. The PCA based neural network achieved a 100:6 data reduction ratio while losing less than 1% of the variability in the RHEED signals. These PCs were subsequently used as inputs for a multi-layer neural network, and the electron transport data remain the responses. Neural network process models wer`e developed for 300 °K and 77 °K electron-mobility. The structures and results of the RHEED process models are provided in Table 4.

Table 4 RHEED process models

	300 °K	77 °K
NN Structure	6-5-2-1	6-4-6-1
Training error (%)	0.22	0.46
Testing error (%)	3.78	9.68

4.3.4.3 RESULTS

Results from the experiments contain excellent room temperature electron-mobility of up to 32,000 cm^2/V/s. The process models indicate that the RHEED signals contain information about the quality of the interface as well as the subsequent InAs channel. This makes sense because RHEED patterns are based on reflections from the growth surface, and surface roughness will alter the intensities of the diffraction pattern. This change in the specular spot intensity is observed in the RHEED data. As the indium monolayer(s) are deposited on the Sb-sublayer, the specular spot intensity decreases rapidly. For longer indium soak times, the intensity values reach a point of saturation until the As shutter opens. Once the As shutter opens commencing InAs growth, the intensity increases. As for the RHEED pattern, it changes from a "1X" to a "4X" when the indium soak begins. Afterward, the "4X" changes to a "2X" when InAs growth initiates. The "2X" and "4X" reconstructions (Figures 15a, 15b) can be associated with In- and As-rich growth regimes, respectively.

The low temperature results demonstrate a correlation with both indium barrier thickness and temperature, whereas the room temperature results showed a correlation with temperature, only. However, the room temperature model exhibited better accuracy than the low temperature model. This can be attributed to higher sensitivity of the electron mobility to the quality of the interface at lower temperature. [6, 20]. When the indium barrier is thick, the surface becomes saturated with indium, which protects the underlying Sb-sublayer from the ensuing As flux. In addition, too much indium may accumulate on the surface. When the indium barrier is thin, the interface is affected, possibly roughened, as indium desorbs from the interface exposing the Sb-sublayer. With

the Sb-sublayer exposed, anion exchange occurs at the interface, where roughness scattering dominates electron-mobility.

(a)   (b)
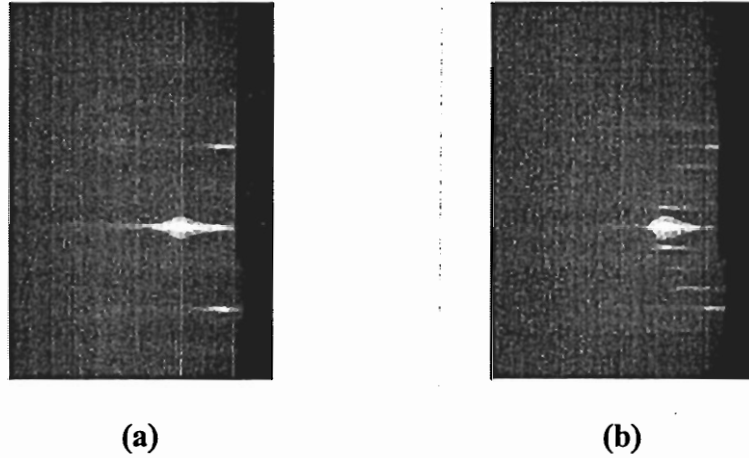
Figure 15 RHEED image from (a) InAs growth - "2X" and (b) Indium deposition on Sb-sublayer - "4X"

A designed experiment was used to examine interface formation and its effect on device performance parameters. RHEED was used to monitor the interface formation of AlGaSb-InAs-based HEMTs, which were characterized using high- and low-temperature (300 °K and 77 °K) Hall measurements. PCA was performed on the RHEED data, and the PCs were chosen to account for 99% of variance were used as inputs for a multi-layer back-propagation neural network. The PCA-based process models exhibited testing error less than 4% and 10% for 300 °K and 77 °K electron-mobility, respectively.

4.3.5 Interface Process Conditions-Mobility Analysis

The data analyzed in this section was generated from experiments described in section 4.3.2. The statistically designed experiments and results are provided in Table 3. Disregarding the **outlier**, these experiments produced test structures with average 300

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°K mobility above 20,000 cm2/V/s. They also produced low temperature mobility that encompassed a range of 90,000 cm2/V/s.

4.3.5.1 Results

Neural network process models were developed for each response. Growth conditions (temperature, indium barrier thickness) were inputs to the neural network, and the responses (electron mobility at 300 °K and 77 °K) were outputs. The network structures and results are provided in Table 5. Plots of the growth conditions and responses generated by the process models are provided in Figure 16. The room temperature mobility model indicates a strong correlation with temperature. The electron mobility is inversely proportional to substrate temperature during formation of the interface.
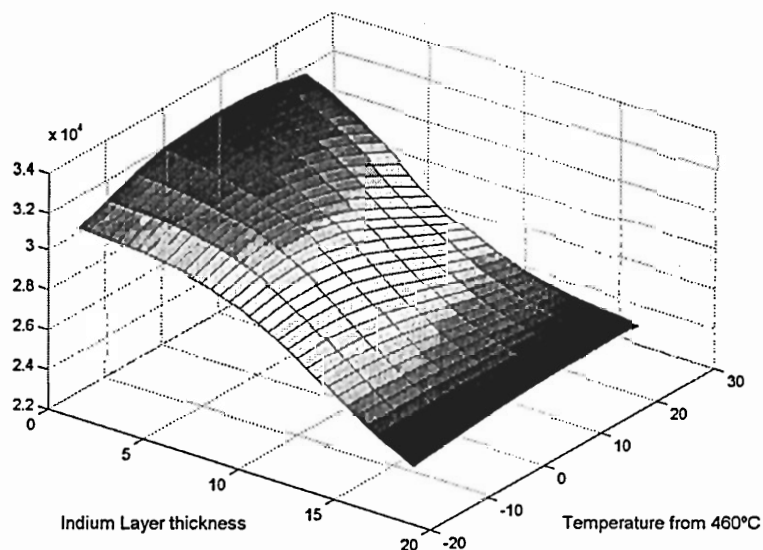
(a)
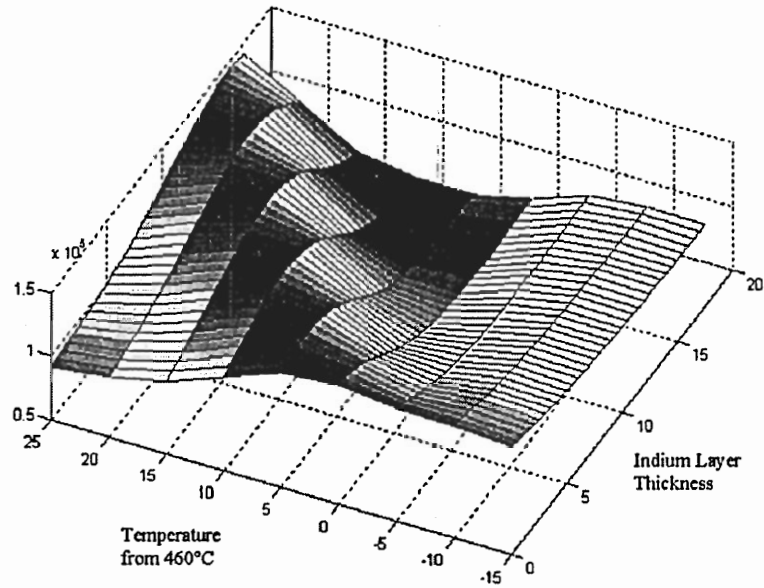
(b)

Figure 16. Models based on growth conditions (a) 300 °K mobility (b) 77 °K mobility

Table 5. Growth condition process models

	GC 300 °K	GC 77 °K
NN Structure	2-2-1	2-2-4-1
Training error (%)	0.23	0.48
Testing error (%)	5.35	6.55

The indium barrier thickness does not appear to have an effect on the room temperature mobility. Depositing multiple monolayers of indium at the interface seems illogical since it leaves the interface metal rich, except the results do not invalidate these experiments. It may be that room temperature electron transport measurements are not sensitive enough to explore the impact of both indium and temperature on the interface formation. However, it is certain that substrate temperature plays a role in the amount of indium retained on the growth surface.

Low-temperature electron transport is sensitive to the quality of the interface [6, 36]. Interfacial roughness scattering has been responsible for the decrease in electron mobility at low temperature. The low-temperature electron transport presented demonstrates a correlation with both temperature and indium barrier thickness. The low-temperature model (Figure 16b) reveals maximums in two particular regions: (1) the thick indium barrier at higher temperature, and (2) the thin indium barrier at lower temperature. It is possible that there is little difference in the quality of the interface between these two regions. In region (1), indium desorbs at higher temperatures, thus creating an interface similar to those formed in region (2). However, when the indium barrier is thick at lower temperature, multiple layers of indium can exist, which are converted to InAs by the ensuing As flux. The model also illustrates that when the indium barrier is thin, low temperature mobility is inversely proportional to increasing temperature, suggesting that interface is affected, possibly roughened, as indium desorbs from the surface. When indium is desorbed so as not to protect the underlying Sb layer, anion exchange can occur, thus creating AlAs-bonds at the interface. The low-temperature model is effective in illuminating indium's role as a function of substrate temperature on interface formation.

4.3.6 Interface Process conditions-strain analysis interface formation

The channel (InAs) strain in these structures can vary according the buffer layer characteristics. Since the buffer is grown on GaAs, thick layers are required to accommodate the large lattice mismatch. The strain is also sensitive to the interfacial properties. Defect-rich interfaces can provide immediate strain relief, but the mobility is

then affected. Studying the relationships among the process conditions, strain, and electron mobility is useful for identifying the optimum process conditions and physical limitations for producing high mobility InAs/AlSb HEMT structures.

Using reciprocal space mapping (RSM) available through x-ray diffraction, the strain was determined in the HEMT structures described in Table 3. RSM from symmetric (004) and asymmetric planes (115) were measured. Because strain is accurately measured by accounting for tilt in the channel layer, RSM from the (004) plane were examined and revealed that tilt was not present in these structures. Hence, the asymmetric scans were used to determine the strain in these structures. The strain data is plotted with corresponding electron mobility in Figure 17.
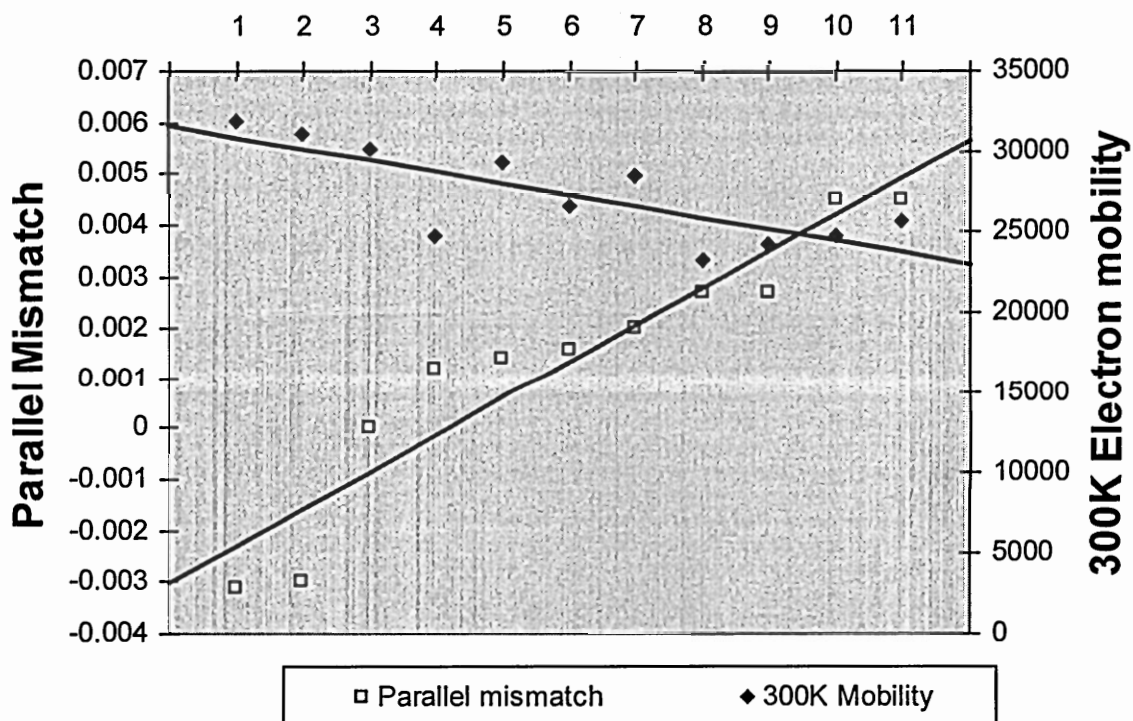
Figure 17. Plot of strain vs. electron mobility in InAs/AlSb HEMT structures

The results show that the mobility values increase with increasing bulk lattice spacing in the InAs channel. For samples exhibiting mobility higher than 30,000 cm2/V/s, the bulk lattice spacing is large than InAs freestanding lattice constant. This shows that antimony is incorporated in the channel. Using neural networks, process models were developed. The network structure is described in Table 6. The network inputs include channel mobility and process conditions at the interface. The model predicted the strain test data within 0.2% error. The strain is relieved as more indium is deposited at the interface. For tensile-strained InAs layers, electron mobility is higher.

Table 6. Neural network structure for InAs channel strain

	GC and Mobility
NN Structure	3-2-1
Training error (%)	0.18
Testing error (%)	0.17

4.4 Be-doped HEMT Structure

Intrinsic sheet charge levels in unintentionally doped AlSb/InAs/AlSb quantum wells are reproducibly $\sim 10^{12}$ /cm^2. While these levels are suitable for depletion-mode operation, realizing enhancement-mode devices ultimately depends on the ability to significantly reduce sheet charge. In an effort to limit carrier accumulation in the InAs quantum well, molecular beam epitaxy (MBE) process conditions, including substrate temperature, Be-doping density, and doping plane spacing above the quantum well were

varied during growth of InAs-Al$_x$Ga$_{1-x}$Sb high electron mobility transistor (HEMTs) structures.

The sheet charge originates from several sources including bulk InAs, the surface, and background impurities of the AlSb barriers [23, 24]. Despite control over epi-layer growth and material properties, high levels of charge accumulation are consistently observed. Minimizing the charge transferred to the quantum well without compromising the device structure is inherently difficult. In several studies that concentrated on the charge in unintentionally doped AlSb/InAs/AlSb quantum wells, the sources of charge were addressed individually and yielded slight improvement [24, 26-28, 45]. The tradeoff is a reduction in electron mobility.

Difficulties in controlling the charge remain unresolved. The InAs and AlSb epi-layers, as well as the heterointerface, remain dependent on the growth conditions and can vary from system to system. Moreover, the impurity charge in Al$_x$Ga$_{1-x}$Sb barriers transferred to 15-nm InAs quantum wells arguably attribute to oxygen contamination (deep donor levels) [45] and Sb-antisites, (Sb$_{Al}$, deep acceptors) [25]. The solution for achieving low charge in AlSb/InAs/AlSb quantum wells in all likelihood requires repressing the donors in the Al$_x$Ga$_{1-x}$Sb barriers. In a study by Zhao, et al. [46], the charge in MBE-grown InAs-AlSb heterostructures was successfully reduced by modulation doping of the top barrier using beryllium, and enhancement-mode n-channel transistor operation was demonstrated. Be-doping was employed to produce acceptor-like impurities in the AlSb barrier such that the donor-like defects were compensated, in effect, reducing the number of carriers readily available to transfer to the lower energy states in the quantum well. In a more recent study [47], decreases in sheet charge were

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achieved with increasing Be-sheet doping levels in AlSb barriers of AlSb/InAs/AlSb quantum well structures. Appropriately, this thesis explores process conditions during MBE growth of modulation-doped InAs-Al_xGa_{1-x}Sb HEMT structures such that the relationships between the process conditions and transport properties are established.

Utilizing a full factorial statistical experimental, the ranges for Be-doping (0 to $2e12$ /cm^2), substrate temperature (350-420°C), and separation above the quantum well (60 to 80 Å) were examined. Relationships between MBE process conditions and transport properties in Be-doped InAs-Al_xGa_{1-x}Sb HEMT structures were established. Among the process parameters investigated, substrate temperature during Be-doping was the most significant process parameter. Substrate temperature and sheet charge exhibited an inversely proportional relationship. The lowest charge and corresponding mobility achieved were $6.6*10^{10}$ /cm^2 at 6,000 cm^2/V/s, respectively.

4.4.1 Experimental Technique

The experiments were performed using the MBE system described in Chapter 3. The epitaxial layers were produced under Group-V (As$_4$, Sb/Sb$_2$) stabilized growth conditions, where the growth rates for Al, Ga, and In were 1.25 um/hr, 0.5um/hr, and 0.5um/hr, respectively. Experiments were performed on semi-insulating ¼-GaAs (001) substrates that were rotated during epitaxy. The growth temperatures were determined using the deoxidation temperature of GaAs substrates (~580°C). The test vehicle in this study was an InAs/Al_xGa_{1-x}Sb HEMT structure. The structure from cap layer to substrate consisted of the following: InAs (1.5nm); In_xAl_{1-x}lAs, where x=0.4 (7nm); Be-doped AlSb (12.5nm); InAs (10nm); AlSb (8nm); Al_xGa_{1-x}Sb, where x=0.60 (200nm); AlSb

(1.5um); and GaAs (200nm). The process conditions and ranges examined are listed in Table 7.

Table 7 Process parameters and ranges

Process Parameter	Range	Units
Be-doping (N_s)	0 to 2e12	/cm^2
Substrate temperature (T_s)	350 to 420	°C
Separation from the InAs quantum well (d)	60 to 80	Å

The experiment was carried out using a 2^3 full-factorial experimental design plus 8 additional trials [44]. The samples were analyzed using conventional Hall measurements at room temperature. For each trial, 5 x 5 mm Hall samples in the clover-leaf van der Pauw pattern were produced and measured at a magnetic field intensity of 3020 G. The Hall results (Table 7) from the experimental design include a wide range of electron-mobility (1k – 22k cm^2/V/s) and carrier density ($6.6 \times 10^{10} - 2.9 \times 10^{12}$ /cm^2).

The experimental data was analyzed using analysis of variance (ANOVA) tables, which determined the statistical significance of the MBE process parameters as they related to the transport properties. ANOVA tables (Tables 7, 8) were generated for sheet charge and electron mobility. The minimum acceptable confidence level was 90%. First-order response surface models were produced that accounted for greater than 95% and 91% of the variance in the data sets for electron mobility and sheet charge, respectively. The regression equations are as follows:

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$$\mu_n = 11788 - 1433*[(Ns - 1.5e+12)/5e+11] - 7240*[(Ts - 385)/35] + 1381*[(d - 70)/10] \quad (23)$$

$$n_s = 1.18e+12 + 3.67e+10*[(Ns - 1.5e+12)/5e+11] - 1.07e+12*[(Ts - 385)/35]$$

$$+ 1.72e+10*[(d - 70)/10] \quad (24)$$

The r-square values for mobility and sheet charge are 0.956 and 0.913, respectively. The surface models (Figure 18) illustrate the dependence of electron-mobility and sheet charge on the MBE process conditions.

Table 8. MBE Process Parameters and Transport Properties

Be-doping ($/cm^2$)	Temperature (°C)	Separation (Å)	Mobility ($cm^2/V/s$)	Sheet charge ($/cm^2$)
1.5e12	385	70	7938	5.1e11
1.5e12	420	80	4819	1.48e11
1.5e12	420	60	711	1.8e11
0	420	-	11506	7.01e11
1.5e12	350	60	17438	2.2e12
0	350	-	20660	1.74e12
5e11	420	80	8975	4.29e11
5e11	350	80	21128	1.75e12
2e12	350	60	18368	2.96e12
2e12	350	80	19048	2.58e12
1e12	420	60	6026	1.21e11
1e12	350	60	19604	1.27e12
2e12	420	80	6038	6.6e10
1e12	350	80	21897	2.12e12
1e12	420	80	10146	2.72e11
2e12	420	60	1683	7.66e10

Table 9 Anova Table for Electron Mobility

Process parameters	Degrees of Freedom	Sum of squares	Mean square	F-ratio	Significance
BE	1	77298752	77298752	22.08	0.0007
T	1	711053809	711053809	203.10	0.0000
D	1	18695755	18695755	5.34	0.0412
BE*T	1	20977029	20977029	5.99	0.0324
BE*D	1	4901520	4901520	1.40	0.2616
T*D	1	2001979	2001979	0.57	0.4654

Table 10 Anove Table for Sheet Charge

Process parameter	Degrees of Freedom	Sum of squares	Mean square	F-ratio	Significance
BE	1	$3.187e+22$	$3.187e+22$	0.26	0.6214
T	1	$1.277e+25$	$1.277e+25$	103.40	0.0000
D	1	$2.004e+22$	$2.004e+22$	0.16	0.6947
BE*T	1	$1.519e+24$	$1.519e+24$	12.31	0.0049
BE*D	1	$1.545e+22$	$1.545e+22$	0.13	0.7302
T*D	1	$1.068e+22$	$1.068e+22$	0.09	0.7741

(a)

(b)

87

(c)

(d)

88
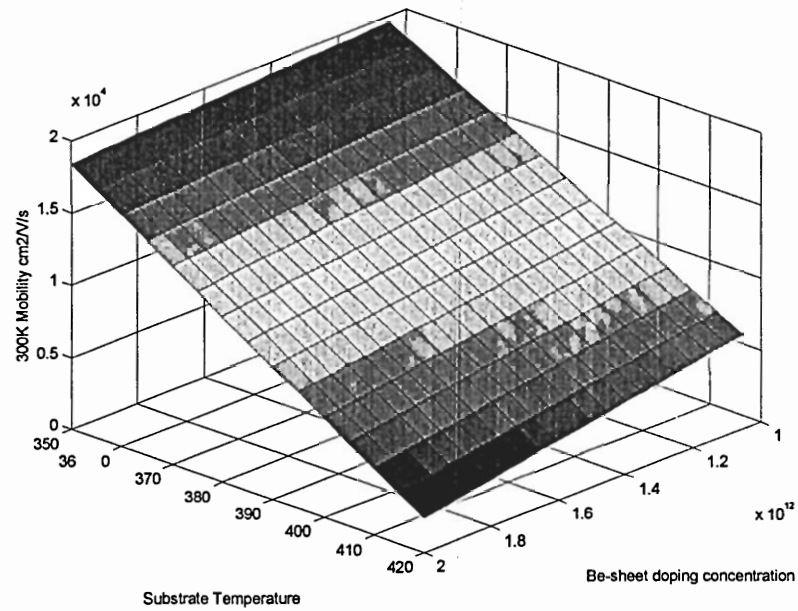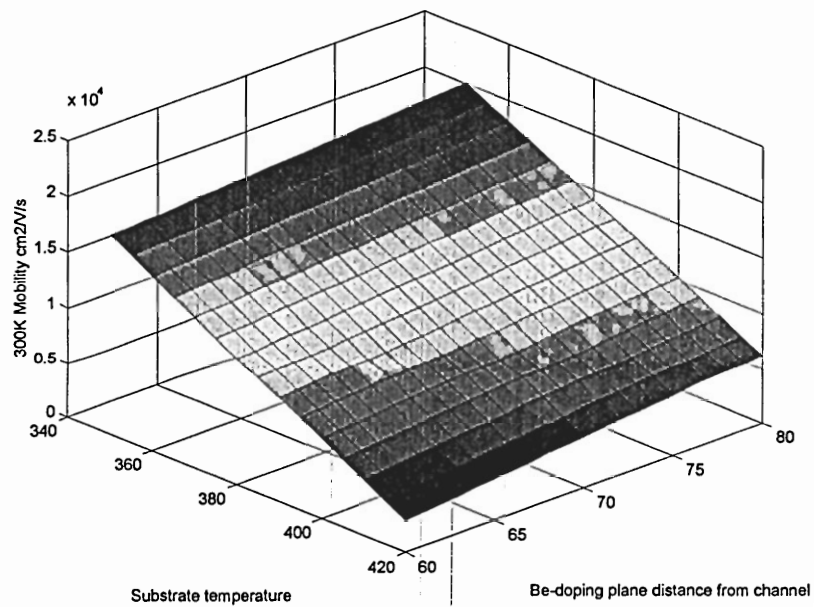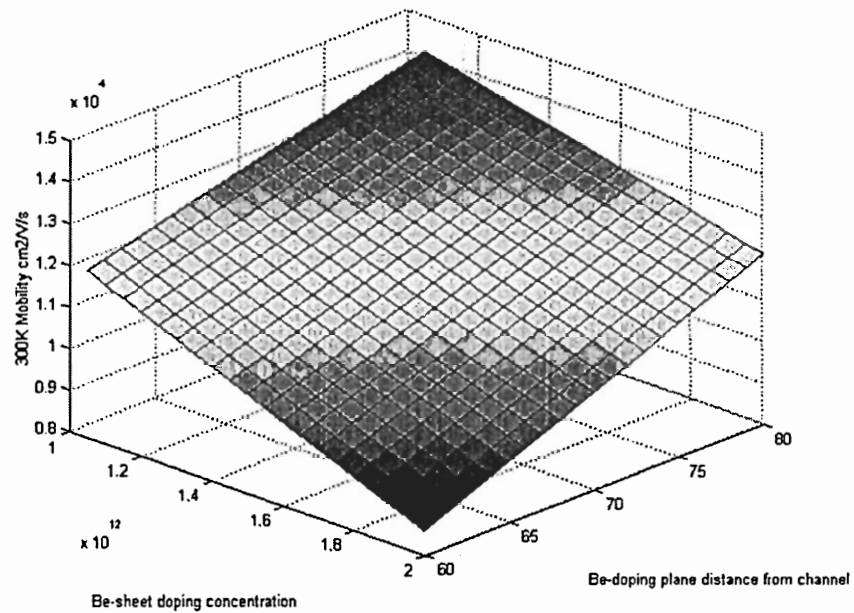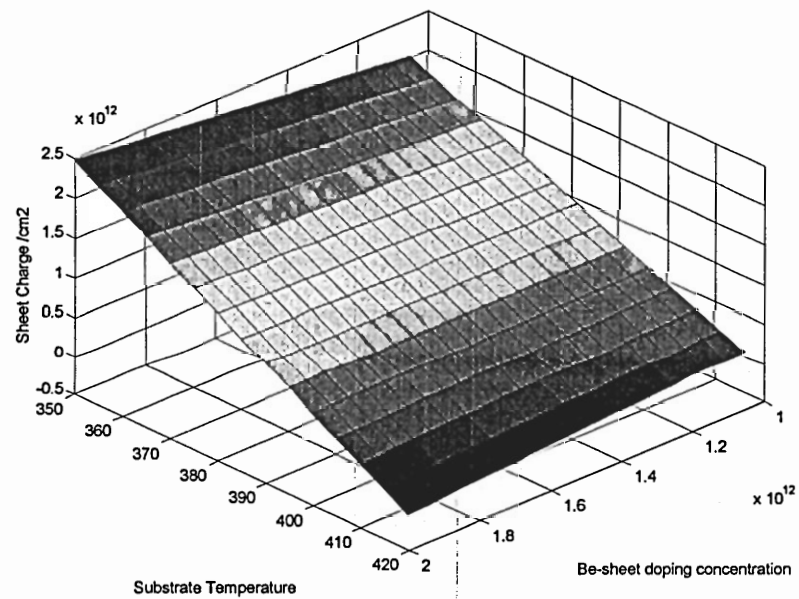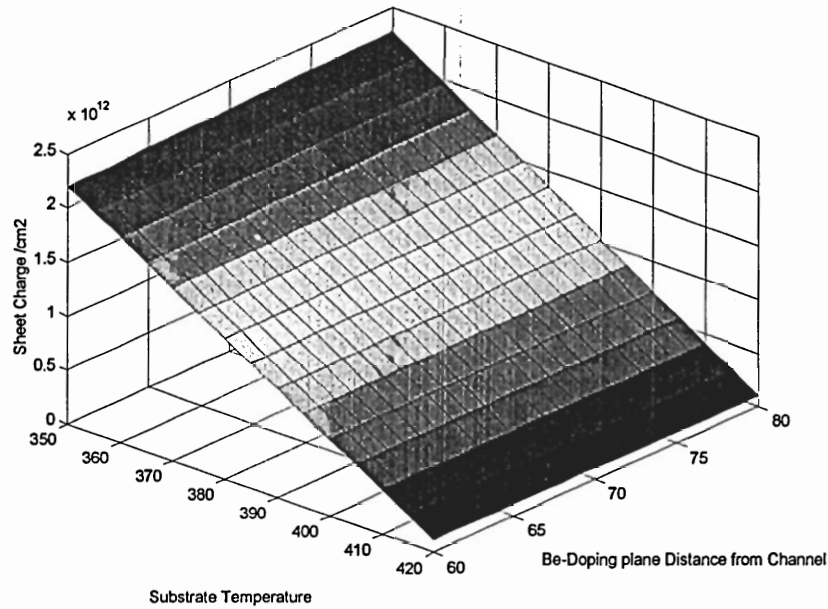
(e)

Figure 18. Regression models for (a) mobility vs. temperature and sheet density (b) mobility vs. temperature and distance (c) mobility vs. distance and sheet density (d) sheet charge vs. temperature and sheet density (e) sheet charge vs. temperature and distance.

The network structure for sheet charge and mobility are described in Tables 11 & 12. The network inputs include the process conditions substrate temperature, doping concentration, and doping plane distance from the channel. The model predicted the charge and mobility within 7% and 1% error, respectively.

Table 11. Neural network structure for sheet charge

	Growth Conditions
NN Structure	3-6-1
Training error (%)	0.01
Testing error (%)	6.75

Table 12. Neural network structure for mobility

	Growth Conditions
NN Structure	3-4-1
Training error (%)	0.15
Testing error (%)	0.11

4.4.2 Discussion

The experiments presented demonstrate that the modification of charge in InAs-$Al_xGa_{1-x}Sb$ quantum well structures can be achieved. Owing to the acceptor impurity levels in Be-doped barriers, the charge transferred to the quantum well was reduced to lower levels ($\sim 10^{10}/cm^2$), in InAs-$Al_xGa_{1-x}Sb$ quantum well structures. The highest mobility HEMT structure produced had a mobility of $\mu=21,897$ $cm^2/V/s$ with corresponding sheet charge of $N_s=2.12 \times 10^{12}$ $/cm^2$. In contrast, the lowest sheet charge and corresponding mobility were $N_s=6.6 \times 10^{10}$ $/cm^2$ and $\mu=6,038$ $cm^2/V/s$, respectively. The process conditions exhibiting significance values less than 0.05 in the ANOVA tables demonstrate correlations with HEMT structure transport properties. Among the MBE process parameters explored, substrate temperature was the most significant, as it relates to both sheet charge and mobility in the InAs quantum well. As illustrated by the response surfaces in Figure 18 (d, e), increasing substrate temperature during Be-doping substantially reduced the sheet charge. Unfortunately, the electron-mobility values exhibited a similar trend (Figure 18 a, b). The ANOVA tables and the first-order response surface models show evidence that considerable changes in the sheet charge levels can be

achieved by adjusting substrate temperature during modulation doping of beryllium in InAs-Al$_x$Ga$_{1-x}$Sb quantum well structures.

The results at higher substrate temperature (420°C) show that higher Be-sheet doping concentration (2.0x10^{12} /cm^2 compared to 1.0x10^{12} /cm^2) yield lower sheet charge values, which is in agreement with the observations reported by Kadow, et al. These authors observed similar trends in mobility. Data from a subset of samples presented in Table 8 are plotted in Figure 19. This plot illustrates the relationship between Be-sheet doping concentration and electron density for samples grown at 420°C. The doping plane displacement was 8 nm above the well.

The growth temperatures reported by Kadow, et al., however, are higher than those examined in this thesis. Kadow shows a near linear relationship between Be-sheet doping concentration and electron density. Similarly, these results demonstrate the impact of Be-sheet doping on electron density. This data also shows mobility reduction with electron density, which suggests that the screening of defects is critical in these structures. The quantum wells examined in this thesis are thinner in comparison to previous reports [46, 47]. It is expected that Be-sheet doping will exhibit a distinctive effect on the conductivity in wider wells. A study examining the sensitivity of InAs well thickness and Be-doping is forthcoming.
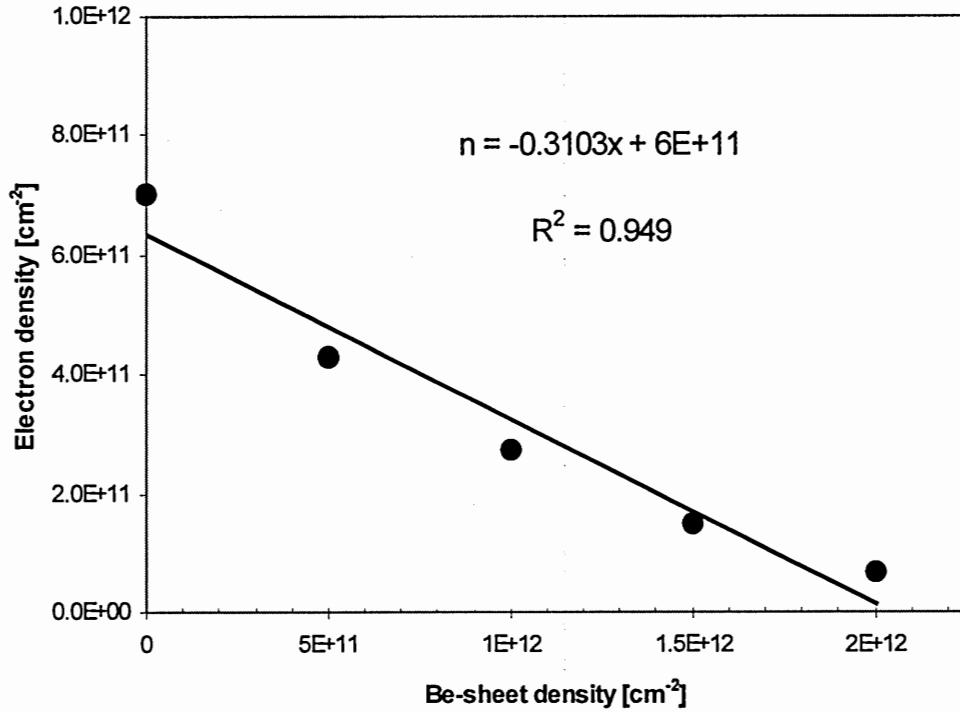
Figure 19. A plot of electron density vs. Be-doping density for samples grown at 420°C. The linear fit accounts for 95% of the variance.

Figure 20 shows that at lower substrate temperature (350°C), higher Be-doping concentration results in increased levels of charge accumulation in the InAs quantum well. This increase in electron density should be correlated with an increase in defect density. Yet, these results suggest that the unintentional background impurities in these structures depend greatly on temperature. Specifically, as substrate temperature is decreased, the defects increase, negating the effects of the Be-doping.
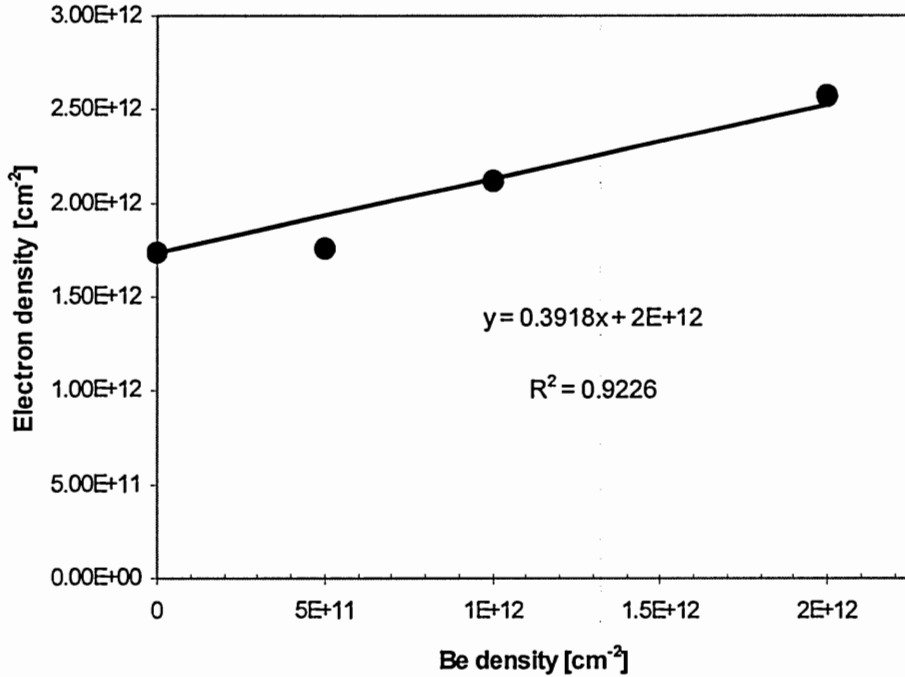
Figure 20. A plot of electron density vs. Be-doping density for samples grown at 350°C. The doping plane is 8-nm above the Well. The linear fit accounts for 92% of the variance.

Sheet-doping plane displacement from the channel appears significant only as it relates to the differences in charge accumulation in the InAs quantum well as the doping plane concentrations vary between 2.0×10^{12} /cm^2 and 1.0×10^{12} /cm^2. Figure 21 includes data from samples grown at 350°C with a doping plane displacement 6 nm above the well. Specifically, the results indicate that for lower doping plane concentrations, improvement ($\Delta = 8.5 \times 10^{11}$ /cm^2) is achieved when the doping plane is closer to the channel. Alternatively, deeper positioning into the barrier is favored for higher doping plane concentrations ($\Delta = 3.8 \times 10^{11}$ /cm^2). By determining the intercept between the linear functions (Figures 20 and 21), it is determined that the critical Be-sheet concentration is N_s=1.85e12 /cm^2 for samples grown at 350°C. This data point represents electron density that is shared for the doping-plane displacements examined in this thesis. In the same

way, the critical Be-sheet concentration for samples grown at 420°C is N_s=1.5e12 /cm^2. Below these limits, the electron density is lower in structures where doping planes are closer to the well.
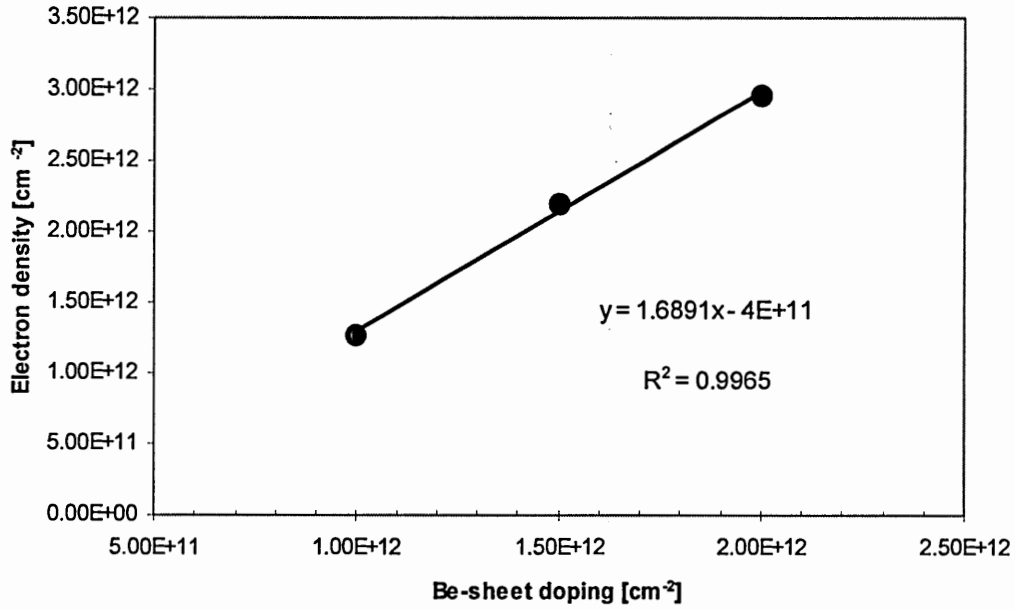
Figure 21. A plot of electron density vs. Be-doping density for samples grown at 350°C. The linear fit suggests a larger influence of doping plane displacement.

In summary, modulation doping of beryllium in AlSb barriers is sensitive both to the process conditions and presumably affects the acceptor levels, which ultimately counteract high donor-like impurity levels found in AlSb barriers. The unintentional background impurities in these structures have a strong dependence on substrate temperature, which can negate the effects of Be-doping in the barriers [46, 47]. Clearly, the carrier density and mobility are interrelated, as they are proportional to each other.

4.5 HEMT Structure with 6.12Å AlGaAsSb Composite Buffer Layer

The technology to vary the conductivity in InAs/AlSb structures is in its early stages. In the previous section, conductivities were studied using Be-doping in the barrier. Be-doping modifies the conductivity; however, screening effects degrade the mobility. An alternative is to vary the band alignments, which is accomplished by adjusting composition in the layers adjacent to the well. In these experiments, the AlSb barriers were grown with arsenic and gallium compositions, producing a bulk lattice constant of 6.12Å. One challenge is to control composition over a range of growth temperatures. Harmand, et al. [2] observed a 4% increase in arsenic mole fraction as the substrate temperature varied from 450-510°C for $Al_xGa_{1-x}As_ySb_{1-y}$ barriers grown by MBE. As the composition changes, so do the quantum properties, including conductivity. Appropriately, this study consists of an experimental design that explores substrate temperature for the barrier and buffer layers adjacent to the quantum well. The impact of the cap layer thickness was also examined.

In this study, the $Al_xGa_{1-x}As_ySb_{1-y}$ barriers were calibrated for a bulk lattice constant of 6.12Å, where x=0.8 and y=0.016. This bulk lattice spacing corresponds with that of AlSb. The calibration samples were grown at 500°C. Arsenic/antimony flux ratio was determined empirically. Arsenic incorporation in the $Al_xGa_{1-x}As_ySb_{1-y}$ samples was confirmed using XRD rocking curves scans from the (004) plane.

A 2^3 full factorial (CCC) experimental design was used to perform the experiments. The substrate temperature during the growth of the buffer and barrier layers were varied (450°C - 500°C) and the cap layer thickness were varied (15Å – 60Å). The test vehicle from cap to substrate was as follows: InAs cap, (varied); $Al_xGa_{1-x}As_ySb_{1-y}$ barrier,

150Å; InAs channel, 100Å; $Al_xGa_{1-x}As_ySb_{1-y}$ buffer, 1μm; AlSb nucleation layer, 2000Å; GaAs buffer layer, 2000Å; GaAs substrate (SI). The growth parameters and results are provided in Table 13. The samples were characterized using Hall measurements and XRD rocking curve measurements.

Table 13. Experimental Design and Results for $Al_xGa_{1-x}As_ySb_{1-y}$ barriers, As=1.6%

Buffer Growth Temperature (°C)	Barrier Growth Temperature (°C)	Cap Layer Thickness (Å)	Mobility	Sheet Charge	Arsenic Composition
432.95	475	37.5	1479	2.69E+11	0.91%
450	450	15	6482	2.56E+11	0.34%
450	500	15	40	1.15E+12	0.71%
450	450	60	5945	3.83E+11	0.40%
475	432.95	37.5	7623	1.34E+11	1.17%
475	475	37.5	5135	9.23E+10	1.27%
475	475	37.5	5738	1.08E+11	1.17%
475	517.05	37.5	696	2.95E+11	0.71%
475	475	75.35	3705	3.16E+11	0.84%
500	450	15	10335	2.43E+11	0.93%
500	500	15	1360	9.37E+10	3.10%
500	500	50	9237	1.90E+11	1.72%
500	500	50	9727	1.75E+11	2.03%
500	450	60	10420	2.01E+11	2.79%
500	500	60	9200	1.33E+11	2.60%
517.05	475	37.5	7285	1.79E+11	1.92%

4.5.1 Mobility analysis

Mobilities as high as 10k cm^2/V/s were measured, which is acceptable for 100Å thick InAs quantum wells. For constant buffer temperatures, the electron mobility decreases with increasing barrier growth temperature (Figure 22). As the arsenic mole fraction changes, so do the quantum properties. Figure 22 illustrates the impact of barrier temperature on electron mobility for samples with 15Å cap layers. As previously described, the transport properties are strongly influenced by the process conditions.
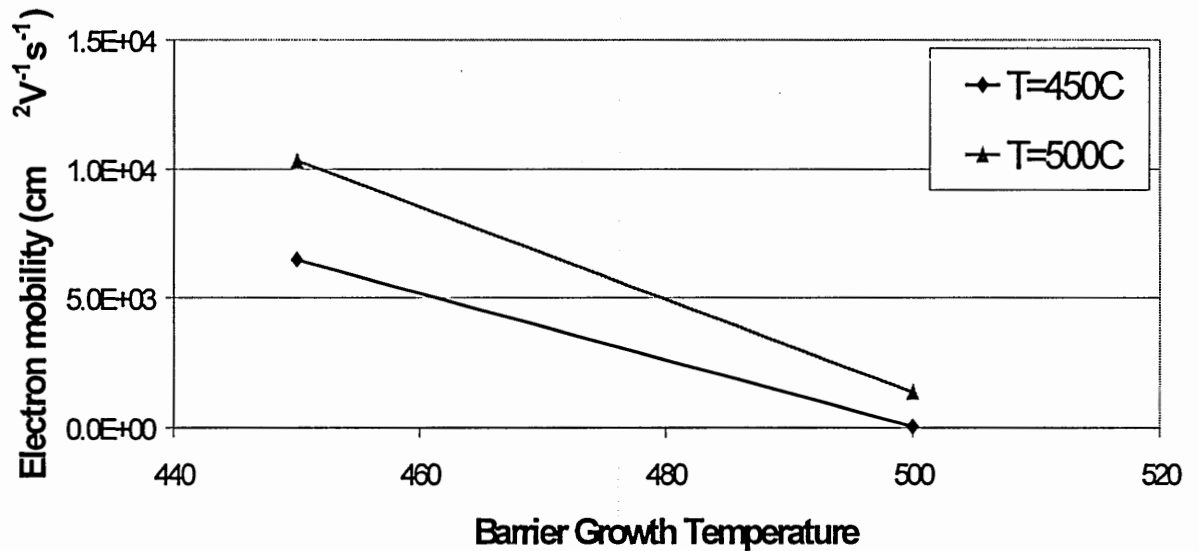
Figure 22. Plot of electron mobility vs. barrier growth temperature for samples with 15Å cap layer.

4.5.2 Carrier density analysis

Carrier density is a property that is challenging to examine. For unintentionally doped samples, the origins and respective magnitudes of free carriers are unclear. In this study, the 2-DEG values vary from 10^{10} to 10^{12} /cm2. There is no correlation between the process conditions and the carrier density. Neither is there a clear relationship between

the 2-DEG and electron mobility. The understanding of charge in these structures would benefit from additional designed experiments.

4.5.3 Strain analysis

The structural properties in these samples were determined using XRD. The results show that the arsenic fraction varies from 0.4% to as mush as 3% for the range of temperatures studied (figure 23). There is also a relationship between the process conditions and arsenic composition.
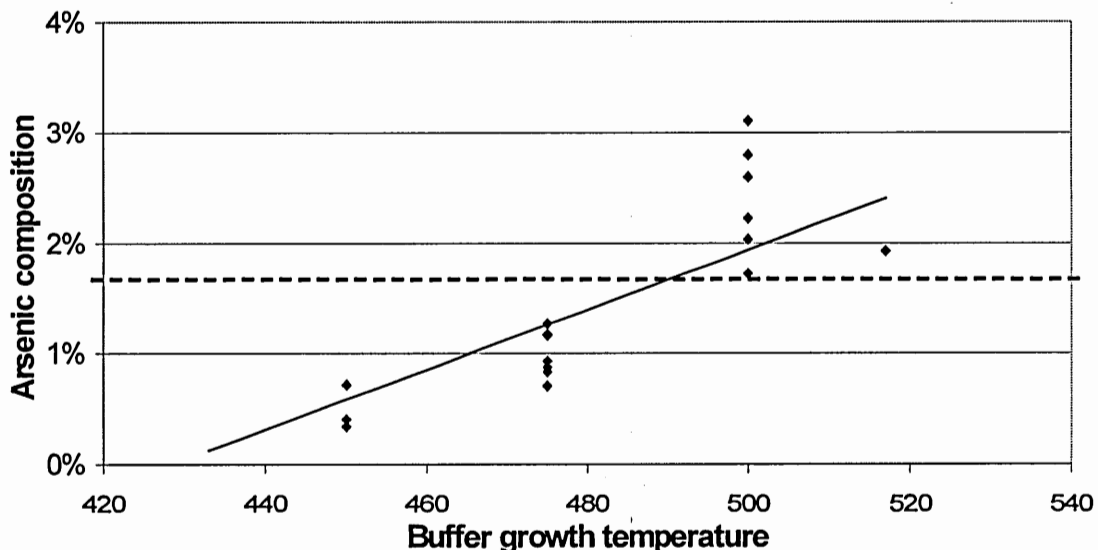
Figure 23. Plot of arsenic composition versus buffer growth temperature for samples with target lattice spacing of 6.12Å. The dotted line represents target arsenic composition

Samples produced at lower buffer growth temperature exhibit reduced arsenic composition. Likewise, higher buffer growth temperatures exhibit the highest arsenic composition. The dependence on substrate temperature shows that antimony desorption is energetically driven. Equally, arsenic atoms are preferentially incorporated with

increasing substrate temperature. The variance of values for unvarying buffer growth temperature reflects the contribution of the cap layer and barrier growth temperature.

4.6 HEMT Structure with 6.06Å AlGaAsSb Composite Buffer Layer

In this study, the $Al_xGa_{1-x}As_ySb_{1-y}$ barriers were calibrated for a bulk lattice constant of 6.06Å, where x=0.8 and y=0.14. The substrate temperature during the growth of the buffer and barrier layers were varied (450°C - 500°C) and the cap layer thickness were varied (15Å – 60Å). A 2^3 full factorial (CCC) experimental design was used to perform the experiments. The test vehicle from cap to substrate was as follows: InAs cap, (varied); $Al_xGa_{1-x}As_ySb_{1-y}$ barrier, 150Å; InAs channel, 100Å; $Al_xGa_{1-x}As_ySb_{1-y}$ buffer, 1µm; AlSb nucleation layer, 2000Å; GaAs buffer layer, 2000Å; GaAs substrate (SI). The growth parameters and results are provided in Table 14.

Table 14. Experimental Design and Results for $Al_xGa_{1-x}As_ySb_{1-y}$ barriers, As=14%

Buffer Growth Temperature (°C)	Barrier Growth Temperature (°C)	Cap Layer Thickness (Å)	Mobility	Sheet Charge	Arsenic Composition
500	500	15	12	-2.65E+12	15.75%
500	450	15	2039	7.74E+10	15.85%
450	450	60	4272	7.83E+10	9.52%
500	450	60	2017	6.94E+10	16.32%
475	475	75.35	1043	7.27E+10	11.93%
450	450	15	2060	1.11E+11	10.00%
517.05	475	37.5	3291	4.31E+10	15.47%
450	500	15	14	2.78E+12	10.20%

Table 14 (cont'd)

432.95	475	37.5	5	1.12E+13	9.71%
500	500	60	170	2.59E+11	14.13%
475	432.95	37.5	2274	7.64E+10	9.52%
475	517.05	37.5	36	-1.50E+12	11.83%
450	500	60	47	-2.85E+12	-
475	475	37.5	-	-	10.87%
475	475	15	-	-	12.41%

4.6.1 Mobility analysis

The mobility in these structures was measured up to 4,200-cm^2/V/s, which is lower than the values measured in the previous section. Like the data produced in the previous section, the barrier growth temperature has a notable effect on electron mobility. At higher barrier growth temperatures, the mobility decreases substantially. Figure 24 illustrates the impact of the barrier growth temperature.
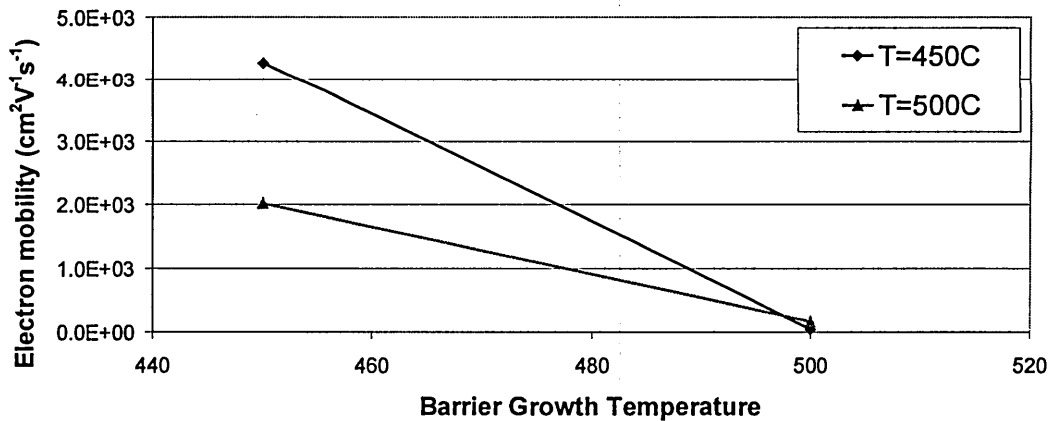
Figure 24. Plot of electron mobility vs. barrier growth temperature for samples with 15Å cap layer.

4.6.2 Carrier density analysis

Just as in section 4.5.2, the 2-DEG values vary (10^{10} to 10^{13} /cm^2). There is no correlation between the process conditions and the carrier density. A relationship between the 2-DEG and electron mobility is not obvious. Some the samples in this study were p-type (indicated by the negative sheet charge values). The reasons for this are unclear.

4.6.3 Strain analysis

The arsenic mole-fraction in these structures ranges from 9% to 16%. Like the results in the section 4.5, the data shows a dependence on the buffer growth temperature.
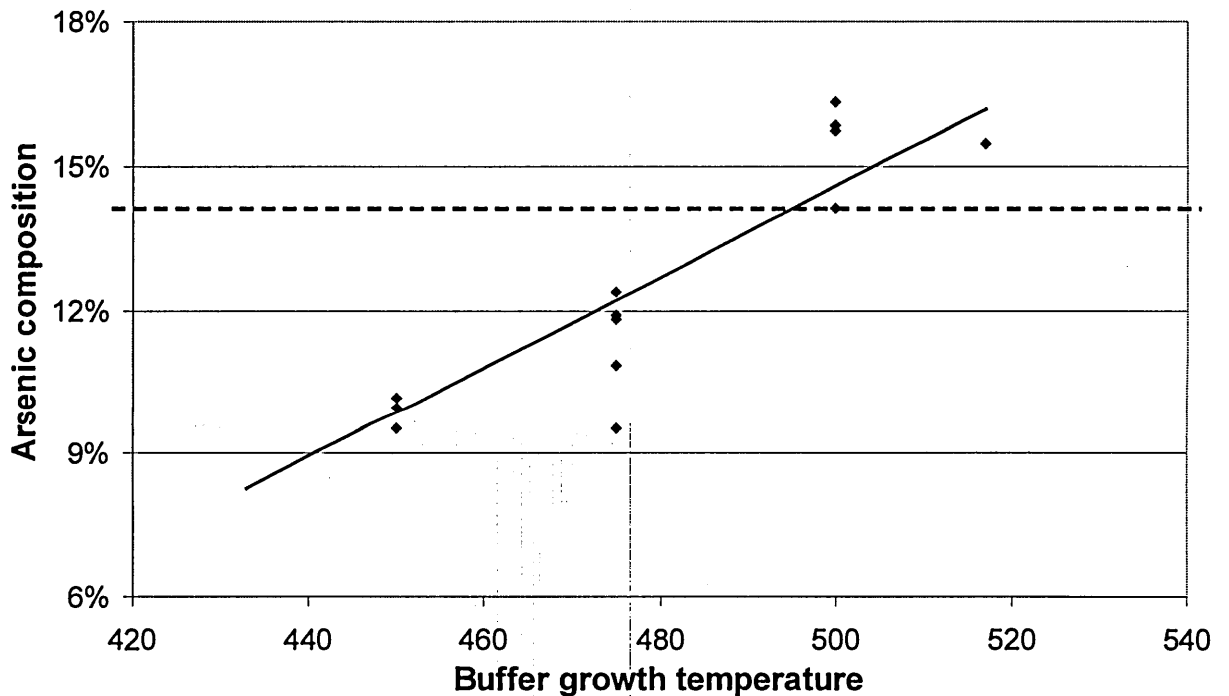
Figure 25. Plot of arsenic composition versus buffer growth temperature for samples with target lattice spacing of 6.06Å. The dotted line represents target arsenic composition

At higher substrate temperature, arsenic incorporation increases. The lowest values were produced using lower growth temperatures. The variance observed in these samples is greater than those reported in Section 4.5. This is attributed to the higher arsenic flux required during the growth of these structures.

Chapter 5 Conclusions

This study proves that process conditions at select stages during MBE growth greatly influence the physical properties of InAs/AlSb HEMT structures. It is illustrated in Chapter 4 that not only relationships between the process conditions and thin film properties exist, but also associations among the electronic and structural properties can be formed. This effort also demonstrates that these complex relationships can be examined and modeled using neural network techniques. The contributions presented are a useful reference for the design and growth of InAs/AlSb HEMT structures.

The study and optimization of the device performance parameters, as well as structural properties in InAs/AlSb HEMT structures, was a motivating factor for this research. Because several properties, including electron mobility, are unique features of InAs/AlSb structures, it is imperative to understand the factors that influence them. For this reason, an *in-situ* diagnostic tool (i.e., RHEED) was employed for the evaluation of critical stages during the growth of complex device structures. RHEED-based neural network models were developed that predicted electron mobility values with less than 4% error. Since RHEED is an optical technique, it presents a unique opportunity to observe, but not interact with the growth process. RHEED experiments at the heterointerface illustrate distinctively how the process conditions affect the surface as material growth is switched from AlSb to InAs. These experiments show that this interface is critical for reasons involving transport properties, material quality, and quantum characteristics. Precise control of this switchover is relevant for producing quality device structures.

RHEED monitoring demonstrates promise for predicting device performance parameters, thus potentially enhancing MBE run-to-run control.

Correlations among the MBE process conditions and structural and electronic properties in InAs/AlSb HEMT structures were examined by means of designed experiments. The experimental and modeling results suggest that appropriate MBE process conditions can be chosen to achieve desired electronic properties for the design of InAs/AlSb integrated circuitry. The experimental results demonstrate the range of values attainable by varying process conditions. Mobilities as high as 32,000 cm^2/V/s and carrier densities as low as $6e10^{10}$/cm^2 were observed in the HEMT structures. The empirical models highlight the impact of select process conditions on the physical properties studied. The models developed help identify the optimum growth conditions within the parameter ranges studied. The results of this study provide a baseline for further development of InAs/AlSb HEMT structures. Moreover, the impact of process conditions on strain and composition is applicable for the design and synthesis of multi-quantum well structures, where the control of mixed-anion mole fractions is required.

5.1 Device Performance Parameters

In this thesis, several influential factors of the transport properties in InAs/AlSb structures were observed and confirmed. The most notable is the heterointerface - the AlSb-to-InAs switchover- that has an immediate consequence on the growth of the subsequent InAs channel layer. Other factors include doping and barrier layer composition, where the effects vary with the process conditions, namely temperature. It is demonstrated that the design and synthesis of InAs/AlSb structures require that these

factors be controlled appropriately. Because the electronic properties are attractive in these structures, the focus is primarily on understanding the electron mobility and carrier density, as wells as the parameters that affect them.

5.1.1 Carrier density

This study demonstrates a range of mobilities and carrier densities; however, no carrier density relationships were observed with the process parameters or other physical properties in unintentionally doped structures. This thesis demonstrates that the InAs-to-AlSb crossover has a negligible effect on excess carriers and that other factors dominate the high donor levels in these structures. Correlations are observed in structures with intentional doping. Carrier density in the quantum well was reduced because modulation doping of beryllium in the AlSb barrier counteract high donor-like impurity levels found in AlSb barriers. This research proves that the carrier density in InAs/AlSb structures can be effectively reduced for the design and implementation of enhancement-mode InAs/AlSb transistors. The process models provide the conditions for achieving levels below those observed in unintentionally doped structures.

5.1.2 Carrier mobility

Mobility values in the InAs/AlSb HEMT structures produced were as high as the theoretical limit for bulk InAs, which indicates the quality of samples grown by MBE. The experiments show that electron transport is subject to quality of the InAs-on-AlSb heterointerface, where substrate temperature, anion exposure, and indium concentration drive the transition. It is also shown that strain relief affects electron transport in these

structures. Because the quality of the InAs quantum well layer is measured by its transport, the ideal process conditions are selected according to the best-observed mobility values. In the list below, all of the experiments performed are considered. The results suggest the following:

- The AlSb-to-InAs switchover is sensitive to the process conditions.

- The decrease in electron mobility as the carrier density reduces demonstrates that the screening of defects is critical in these structures. The optimal mobility values for enhancement mode devices do not correspond with InAs bulk properties.

- Strain states in the channel are important as it relates to the transport properties.

As the motivation for investigating these structures, mobility is found to be sensitive to changes in the growth process. This study demonstrates that the production of structures with excellent transport properties require the optimization of several parameters including those studied in this thesis.

5.2 Physical Interpretation

Critical stages during growth prove to affect the structural properties in these structures. The study of the heterointerface revealed that the process conditions at the switchover have a direct consequence on the subsequent layer. The quality of the interface is important as it relates to the growth of the rest of the structure.

5.2.1 Interfacial roughness

The interface is roughened by anion exchange. RHEED data shows that the interface is sensitive to temperature, antimony exposure, indium concentration deposited, and arsenic overpressure. These are all adjustable parameters while the interface is formed. The AFM images taken at the InAs/AlSb interface illustrate nanoscale roughness as the InAs layer is grown. This presumably affects the quality of the subsequent layer.

5.2.2 Channel quality

In these structures, antimony desorbs from the sublayer and incorporates into the InAs channel. Using XRD, the lattice spacing of the InAs channel was measured and found to be related to electron mobility in the channel. Structures were found to be InAs(Sb), where higher amounts of antimony resulted in higher mobility values.

Chapter 6 Recommendations & future work

The design and synthesis of InAs/AlSb HEMT structures will benefit from a greater understanding of leakage current in these structures. The structural specifics and process conditions that influence leakage current should be studied. Based on the influence of strain in these structures, graded buffer layers should also be explored as starting material for eventual HEMT growth.

The development of empirical models, such as those in this thesis, provides a reference for implementing alternative device structures. Still, much work is needed in the selection of parameters for simulating the quantum properties in InAs/AlSb structures. Long term goals involve the matching of theoretical models with empirical results.

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SUMMARY

This research demonstrates process modeling of InAs/AlSb HEMT structures produced by MBE using neural network technology. The process models developed employ MBE process conditions to predict HEMT structure metrics. This research effort enhances the ability to: (1) better understand the MBE growth process for these particular, complex structures; and (2) achieve reproducible results. The performance of InAs/AlSb structures depend greatly on the ability to control the physical properties in thin films produced via MBE. Therefore, the influence of the process conditions on these properties should be realized. The approach used in this research involves using carefully designed experiments and in-situ diagnositc techniques to evaluate thin film quality. The experiments in this thesis demonstrate the range of transport properties attainable and the significance of the parameters studied.