A Programmable Δ - Σ Modulator Using Floating Gates

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A Programmable Δ - Σ Modulator Using Floating Gates

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SUMMARY

A programmable Δ-Σ modulator using floating gates is presented. Floating gates are used to accurately set the feed-forward and feedback gain coefficients which allow for tunability of the modulator noise transfer function. The modulator is designed to be able to run in sub-threshold, therefore providing low power consumption. The design of the G_m-C integrator is presented and a technique for improved linearity and novel common mode feedback is presented. Experimental results for the improved G_m-C integrator are shown. A Δ-Σ modulator test structure was fabricated in a 0.5μm CMOS process. Experimental results are shown for 2^{nd} and 3^{rd} order modulators. Design improvements are then presented for the next version of the modulator.

CHAPTER I

INTRODUCTION

The objective of the proposed research is to create a low-pass continuous-time Δ-Σ modulator that has tunable feed-forward and feedback gain coefficients. Floating gates will be employed to allow for the tunability of the coefficients. The currents of floating gate transistors can be programmed to a high level of accuracy, and this in turn will translate to a high level of accuracy for the feed-forward and feedback gain coefficients [19]. The proposed modulator has many advantages over traditional Δ-Σ modulator implementations. The typical noise sources associated with switched-capacitor Δ-Σ modulators, charge injection and slew rate, are not present in the proposed modulator. The proposed modulator will have a completely programmable Noise Transfer Function (NTF) which is not possible in traditional switched-capacitor implementations.

1.1 Previous work on Δ-Σ Modulators Involving Floating Gates

Traditional Δ-Σ modulators use capacitive ratios to set the feed-forward and feedback gain coefficients. One of the problems with this is approach is that once the circuit is fabricated the capacitor ratio is fixed and can not be changed. The downside of this is any nonidealities that occur from layout and fabrication cannot after words be adjusted for.

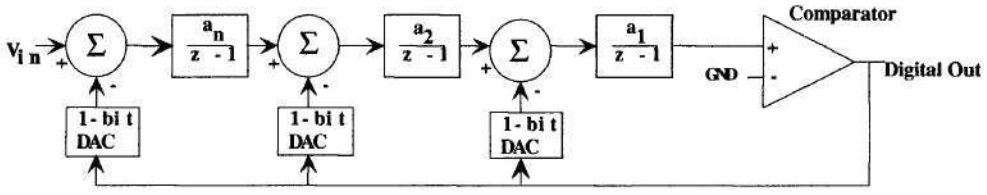

Figure 1: Traditional Δ-Σ modulator architecture using discrete time representation. In this model the circuit is analyzed as a discrete time system and uses ideal components. The circuit provides a good understanding of the modulator but fails to include any of the critical nonidealities that occur such as charge injection and slew rate limitations.

Recently research has been begun on using floating-gate circuits to emulate the capacitor ratio feedback found in switched capacitor Δ-Σ modulators [9]. The work done in [9] focuses on using programmable voltage sources called electronic potentiometers or EPOTs [18]. Using floating-gate circuits in the form of EPOTs allows for the feedback coefficients to be tuned to achieve the desired values. However, the feed-forward gain is still comprised of switched-capacitor circuit elements that have fixed capacitor ratios, illustrating the lack of tunability for the feed-forward coefficients. Nonetheless, the ability to finely adjust the feedback coefficient is still a very positive step in the right direction towards complete tunability.

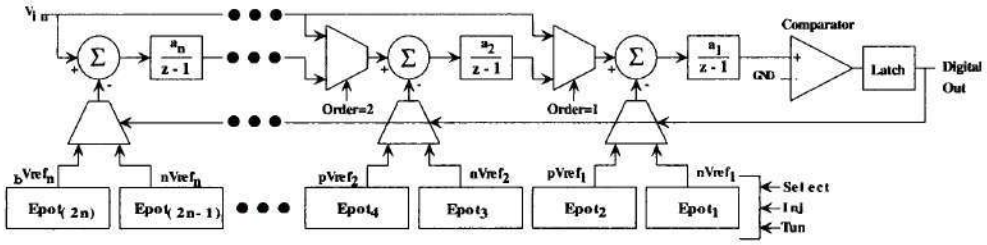

Figure 2: Current research done on Δ-Σ and floating gates involves using EPOT elements to accurately set the feedback gain coefficients. While this provides some tunability the modulator still suffers from the standard noise sources of switched-capacitor Δ-Σ modulators.

The EPOT switched-capacitor implementation shown in Fig. 2 still suffers from some of the problems associated with switched-capacitor Δ-Σ modulators. The switching of the capacitors from one potential to another creates the problem of charge injection in the modulator [4]. This charge injection creates a large amount of unwanted noise that carries into the signal of the modulator output. Large capacitors are needed on the first integration stage to reduce the effect of $\frac{KT}{C}$ noise in the system. Depending on noise specifications, a large amount of die area might be used for the input capacitors. Another problem is the amount of power that is used by the modulator. Each op-amp used in a switched-capacitor integrator block must have a high enough slew rate to meet the desired specifications [8]. This means large amounts of current are required for each stage of the modulator, greatly increasing the total power usage. While the EPOT Δ-Σ modulator provides added tunability to aid in optimizing performance, it still retains all of the above

negative issues: unwanted noise, slew rate limitations and no tunability of the feed forward coefficients. This research will try to show that there exists a better way to make a Δ-Σ modulator using continuous-time elements and the programmability of floating-gates.

CHAPTER II

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER DESIGN

The key building block of the continuous-time Δ-Σ modulator is the G_m-C integrator stage. It is the G_m-C integrator that enables the noise to be shaped away from the baseband. Traditionally in Δ-Σ design the integrator has been built with switched-capacitor elements. Recently more work has gone into designing continuous-time integrators for Δ-Σ modulators. This chapter presents a G_m-C continuous-time integrator with improved linearity and a new, novel form of common-mode feedback.

2.1 Traditional Subthreshold Design

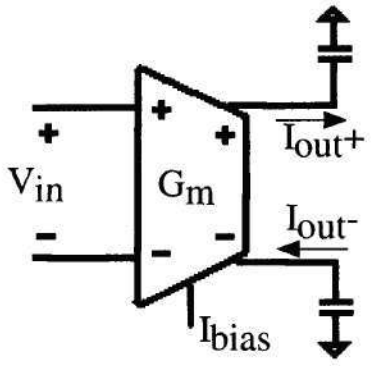

Figure 3: Differential G_m-C integrator. The differential voltage V_{in} is converter to a differential current I_{out+} and I_{out-} by the transconductance G_m. The bias current I_{bias} sets the value of G_m.

The G_m-C integrator works by converting a differential input voltage into a differential output current that is then integrated by a load capacitor. The capacitor transforms the output current into an output voltage by the standard I-V relationship of a capacitor,

$$I_{out} = C\frac{dV_{out}}{dt} \tag{1}$$

Integrating and replacing I_{out} by $G_m V_{in}$ shows that the output voltage is an integration of the input voltage, where

$$V_{out} = \int G_m \frac{V_{in}}{C} dt \tag{2}$$

Equations (1) and (2) are implemented in the operational transconductance amplifier, OTA, seen in Fig. 4. The OTA of consists of a bias transistor M_5, an input differential pair, M_1 and M_2, and an output stage. The transconductance, G_m, of the stage is proportional to the amount of current in the bias transistor. The equation for G_m varies depending on whether the circuit operates in the above-threshold region or in sub-threshold [6].

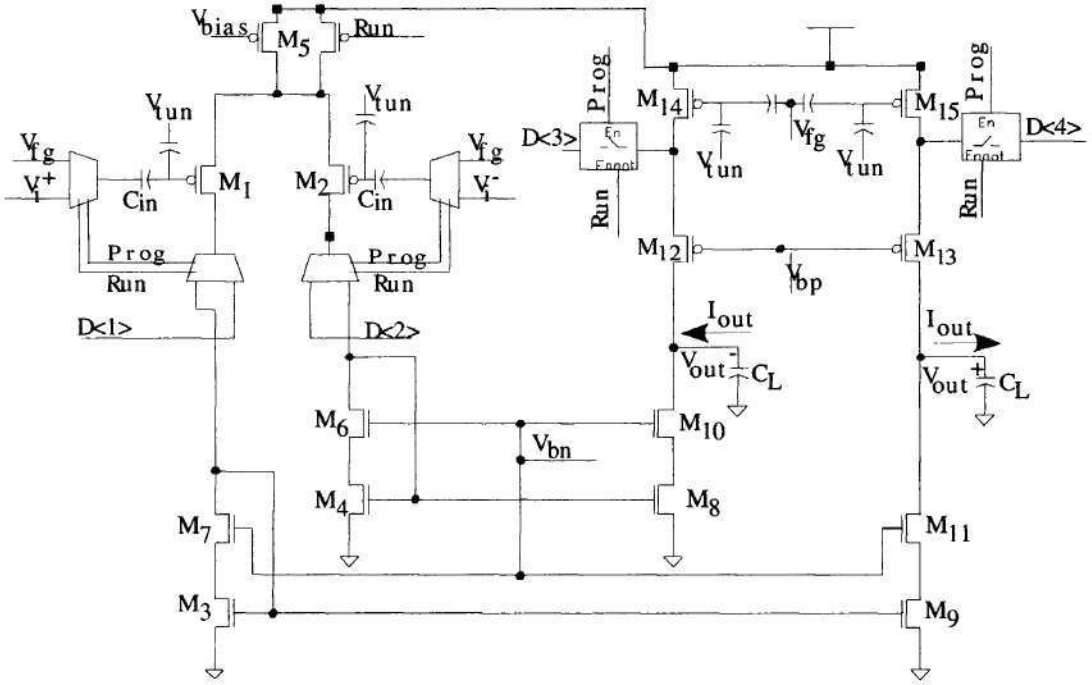

Figure 4: Operational Transconductance Amplifier circuit used in the Δ-Σ modulator. Transistors M_1 and M_2 create a differential input pair with floating gate capacitance degeneration to provide increased linearity. M_3 supplies the bias current and is set by a floating gate. The floating gate transistors attached to the gates of M_{14}, M_{15} are used to set the bias current in the output stage of the modulator to a current that is half the bias current. Common mode feedback is provide by the circuit shown in Fig. 9 which controls the bias current provided by M_5.

The bias current for the OTA will be set by a floating-gate that is attached to transistor M_{16} of the common-mode feedback, CMFB, circuit shown in Fig. 9. This current in turn sets the bias current of the OTA through transistor M_3. The floating gate will be programmed to accurately set the gate voltage of transistor M_{16} so that a precise bias current can be

Table 1: Transistor sizes for OTA of Fig. 4

$\mathbf{M}_1$	$\frac{12\mu}{1.2\mu}$	$\mathbf{M}_9$	$\frac{3\mu}{1.2\mu}$
$\mathbf{M}_2$	$\frac{12\mu}{1.2\mu}$	$\mathbf{M}_{10}$	$\frac{3\mu}{1.2\mu}$
$\mathbf{M}_3$	$\frac{3\mu}{1.2\mu}$	$\mathbf{M}_{11}$	$\frac{3\mu}{1.2\mu}$
$\mathbf{M}_4$	$\frac{3\mu}{1.2\mu}$	$\mathbf{M}_{12}$	$\frac{6\mu}{1.2\mu}$
$\mathbf{M}_5$	$\frac{3\mu}{3\mu}$	$\mathbf{M}_{13}$	$\frac{6\mu}{1.2\mu}$
$\mathbf{M}_6$	$\frac{3\mu}{1.2\mu}$	$\mathbf{M}_{14}$	$\frac{6\mu}{1.2\mu}$
$\mathbf{M}_7$	$\frac{3\mu}{1.2\mu}$	$\mathbf{M}_{15}$	$\frac{6\mu}{1.2\mu}$
$\mathbf{M}_8$	$\frac{3\mu}{1.2\mu}$		

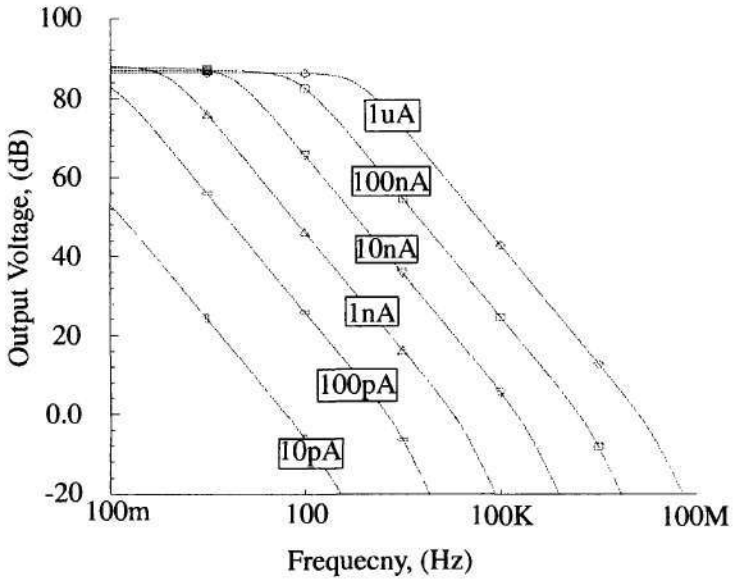

Figure 5: SPICE simulation AC magnitude curves of the differential voltage gain of the OTA with varying bias currents. Starting from the left the bias currents are 10pA, 100pA, 1nA, 10nA, 100nA, 1uA. The 0dB frequency crossings go from 75Hz to 15MHz. The dominant pole is determined by R_oC_L and the 0dB crossing is determined by G_m/C_L

achieved [1, 7]. Through charge injection and tunnelling, charge can be added and removed from the gate of the transistor in a controlled manner allowing the biasing current to be set to an arbitrary value. The T-gates that are attached to the differential pair transistors gates and drains in Fig 4 are used for the programming of those transistors. During programming mode the T-gates allow the programming interface to isolate the individual transistors so that the gate and drain voltage can be individually controlled allowing accurate tunnelling and injection [19]. In run mode the T-gates connect the transistors with the rest of the OTA and act as ideal wires. The parasitics introduced by the T-gates are minimal when operating at frequencies below 10MHz.

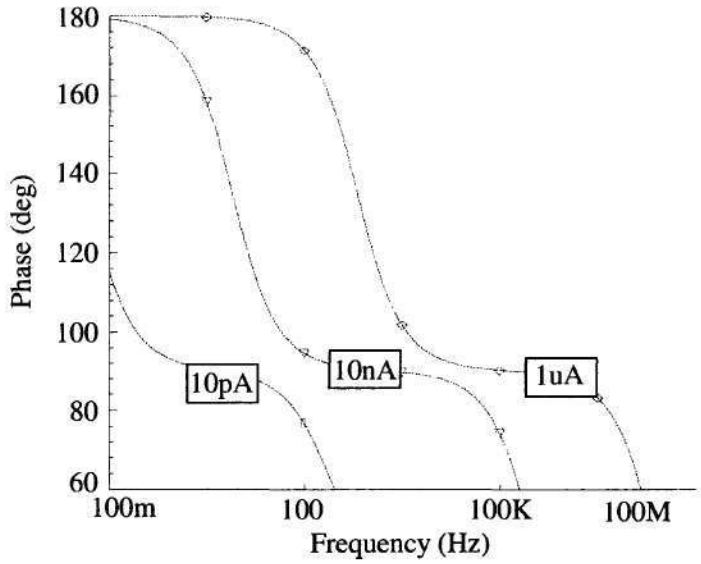

Figure 6: SPICE simulation AC phase curves of the OTA showing phase response for the bias values of 10pA, 10nA, 1uA. These are the phase curves for the related AC magnitude plots in Fig. 5

The programmability of the bias current translates to an ability to set the transconductance of the OTA to any desired G_m value. The ability to vary the transconductance allows for the AC frequency response to be tuned to the desired response. Figure 5 shows the various frequency responses obtained using the tunable floating-gate current. Since the

OTA works in conjunction with the load capacitor to represent an ideal integrator, the optimal operating frequency for the OTA would be when the phase shift is 90^o. This can be seen in Fig. 6 where the phase is plotted for three of the curves in Fig. 5. Therefore, the input frequency to the modulator will help to determine what transconductance value to use so that an optimal integration behavior can take place.

The time constant for the dominant pole and the equation for the 0dB cross-over frequency are as follows:

$$\tau = G_m R_o^2 C_L \tag{3}$$

$$\textit{Unity Gain Bandwidth} = \frac{G_m}{C_L} \tag{4}$$

The output stage is cascoded so that the output resistance increases by $G_m R_o{}^2$. A larger output resistance causes the dominant pole to move to lower frequencies. The overall effect is to cause the phase to be 90^o for a larger frequency spread while still maintaining the same 0dB crossing frequency, (4).

2.2 Linearity Issues

In standard operational amplifiers the transconductance of the amplifier is not constant, as the input amplitude varies, the transconductance of the OTA is modified. This is a problem for G_m-C circuits because a fixed G_m value is necessary to obtain linear results from the integrator. The non-linearity in the transconductance is due in part to the non-linear voltage to current relationship of the MOSFET [6]. In subthreshold the differential pair I-V relationship can be expressed using the hyperbolic tangent function. For small values of input voltage the output current is linear, but as the input voltage increases, the current becomes non-linear for large values of positive and negative voltage. For above threshold operation the differential pair I-V relationship does not distill to as simple a function as in the subthreshold case.

There have been many methods proposed to create a more linear OTA, [6, 11, 10]. Some of the circuits designed include using source degeneration on the input differential pair so

that the transconductance becomes proportional to the degeneration resistance [6, 11]. Another method involves using a cross-coupled differential pair along with the standard differential pair to try to cancel out the non-linearities of the amplifier [10]. One problem with the above solutions is that they increase the complexity of the circuit, and in some cases they are not easily tunable to different transconductance values. In this research improved linearity is obtained by using floating gate transistors on the input differential pair.

As has been shown in [13, 14], floating gates can be applied to differential input transistors to program out any threshold mismatch that occurs. The addition of the floating gates and the additional capacitor needed can be seen on transistor M_1 and M_2 in Fig. 4. Ideally the input differential transistors should be exact matches of each other. But due to processing variations and the layout of the circuit this is usually not the case. The mismatch has many negative effects including a voltage offset on the input and an increase in the non-linearity of the circuit. The floating gates allow for charge to be applied to the gates of the input differential pair so that their voltage thresholds match one another. This will allow for better performance than in the before programmed state.

The input differential pair transistors M_1 and M_2 are augmented with floating gates on their inputs for a twofold benefit. They allow for the removal of threshold-voltage mismatches between the input differential pair and they provide an increase in the linearity of the G_m-C integrator.

In subthreshold the main source of mismatch is voltage threshold mismatch, as shown in the I-V equation for a subthreshold MOSFET with the source referenced to the substrate,

$$I = I_{th}\frac{W}{L}\delta \exp\left[\kappa\left(\frac{V_g - V_{th} + \Delta V_{th}}{U_T}\right)\right]. \tag{5}$$

To remove the V_{TH} offset the floating-gate transistors are programmed to either add or remove charge to cancel out the effect of the V_{TH} error [13, 7, 14].

At transistor M_1 the floating gate input capacitance, C_{FG}, will create a capacitively coupled voltage division to occur at the gate of transistor M_1. The equation can be found

to be

$$V_{FG} = \frac{C_{FG}}{C_T + C_{FG}} V_{in} + V_{charge} \tag{6}$$

where V_{FG} is the voltage after the capacitive divider, C_T is the total capacitance seen at the node including the floating-gate capacitance, gate oxide capacitance, tunnelling capacitance and parasitic capacitance. V_{charge} is the charge that is stored at the output of the capacitively coupled node. By using floating-gate programming techniques it is possible to change V_{charge} so that it cancels out the ΔV_{th} error,

$$V_{th,eff} = V_{th} - (V_{charge} - \Delta V_{th}). \tag{7}$$

The removal of the ΔV_{th} error will be maintained over temperature and will help reduce mismatch error if the differential pair are taken to current biases that are above-threshold.

For subthreshold currents the differential pair has a transfer function that is in the form of the hyperbolic tangent [6]. By having a capacitive divider at the input to each differential transistor, (6), the linear region of the hyperbolic tangent is expanded,

$$I^+ - I^- = I_{ref}\left[\tanh\left(\frac{\kappa C_{FG}(V^+ - V^-)}{2U_T C_T}\right)\right]. \tag{8}$$

The linear range of (8) can be calculated to be,

$$LinearRange = \frac{2U_T}{\kappa}\frac{C_T}{C_{FG}}, \tag{9}$$

where U_T is the thermal voltage and κ is derived from the ratio of the depletion capacitance to the total capacitance of the transistor channel. The fabricated modulator has a C_{FG} of 30fF and a M_1 of size 12um/1.2um.

The effects of this increase in linearity can be seen in Fig. 7 with summarized results in Table 2. Using SPICE simulations a floating-gate capacitance of 30fF causes a reduction in the third harmonic magnitude of over 10dB for only a 4dB reduction in fundamental frequency magnitude. The use of floating gates for improving linearity is a natural choice due to the face that floating gates are already being used in other areas of the circuit.

Experimental data was also taken from a fabricated test IC, Fig. 14, that shows the improved linearity resulting from using floating-gate capacitors on the input differential

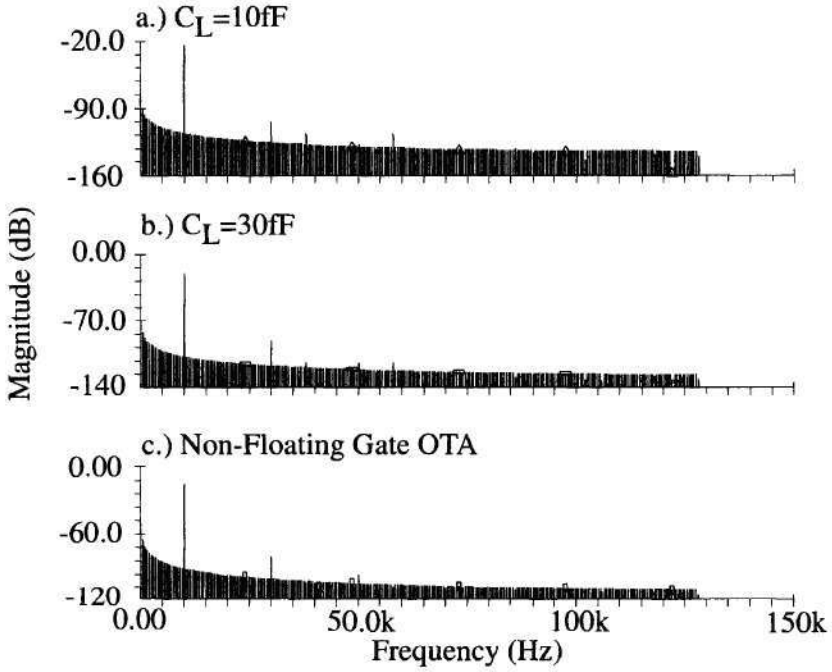

Figure 7: SPICE simulation frequency spectrum plots of the output voltage of OTA for different values of floating gate input capacitance. V_{in}=1mV, I_{bias}=100nA and C_L=100pF. Input transistor W/L is 12u/1.2u The top spectrum is for C_L=10f, the middle is C_L=30f, and the bottom plot is for a standard OTA without the improved linearity of input floating gates. The various frequency points of the spectrums are summarized in Table 2

Table 2: Analytical Results of Fig. 7 Showing Effects of Increasing Linearity Using Input Floating-Gate Transistors, Voltage Output Magnitudes are Listed at the Key Frequencies: 1st Harmonic @10KHz, 3rd Harmonic @30KHz and 5th Harmonic @50KHz

FG Capacitance	Fundamental	3rd Harmonic	5th Harmonic
No FG capacitance	−15.54dB	−80.1dB	−96.3dB
C_{FG} = 30fF	−19.43dB	−90.63dB	−113dB
C_{FG} = 10fF	−24.15dB	−103.9dB	−127.5dB

pair. The experimental results are shown in Fig. 8. As the input capacitance gets smaller the differential gain becomes less and the linear range improves. For input capacitances of 20fF, 60fF and 120fF the resulting differential gain was 40.01V/V, 60.77V/V and 95.75V/V respectively. It can be extrapolated from this data that to get an even larger linear range either the input capacitance can me made smaller or the input differential pair transistors can be made larger so that their gate capacitance is increased.

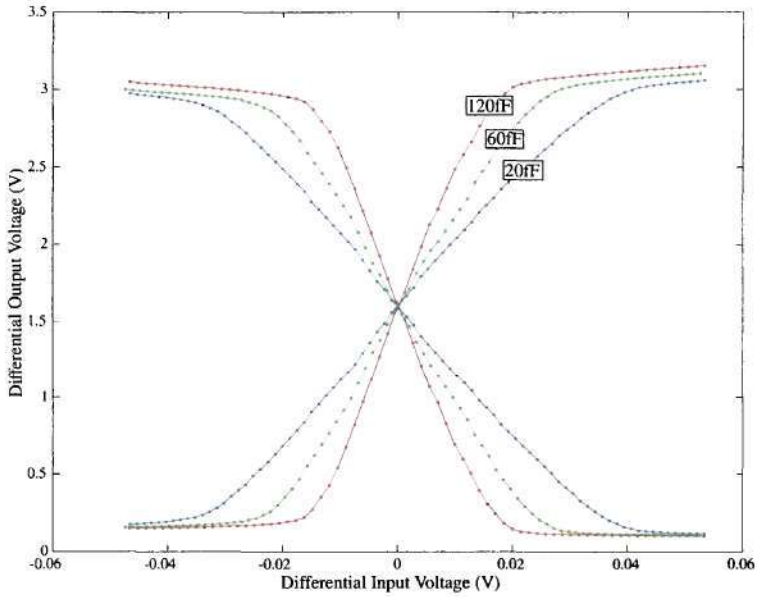

Figure 8: Experimental DC differential input sweep for the OTA circuit with varying C_{in} values–20fF, 60fF and 120fF. Measured DC gains are 40.01V/V, 60.77V/V and 95.75V/V respectively. The gain is a function of the capacitance C_{in} connecting the differential input to the floating-gate node.

2.3 Common Mode Feedback

A fully differential OTA lacks the common mode rejection as found in single ended amplifiers [5]. Additional circuitry is required for the OTA in Fig. 4 to provide common-mode feedback. Two different types of common mode feedback are being attempted in this research. The first approach, seen in Fig. 9 is a traditional approach [4] that uses two auxiliary differential pairs, M_{20-21} and M_{22-23} to sense the differential output voltages. For differential changes in the output no change occurs in the common feedback circuit because the differential pairs change in opposite but equal amounts. Any common mode change in the output voltage

causes the average voltage at the gates of M_{20} and M_{23} to be different than the reference voltage applied to gates M_{21} and M_{22}. The CMFB circuitry therefore adjusts the bias transistor of the OTA, M_3, through the mirror transistor of the CMFB circuit, M_{24}, so that the common mode voltage of the output returns to mid-rail. The bias transistor M_{16} sets the bias current for the entire OTA, in this application it will be a floating-gate transistor allowing the bias current to be accurately programmed.

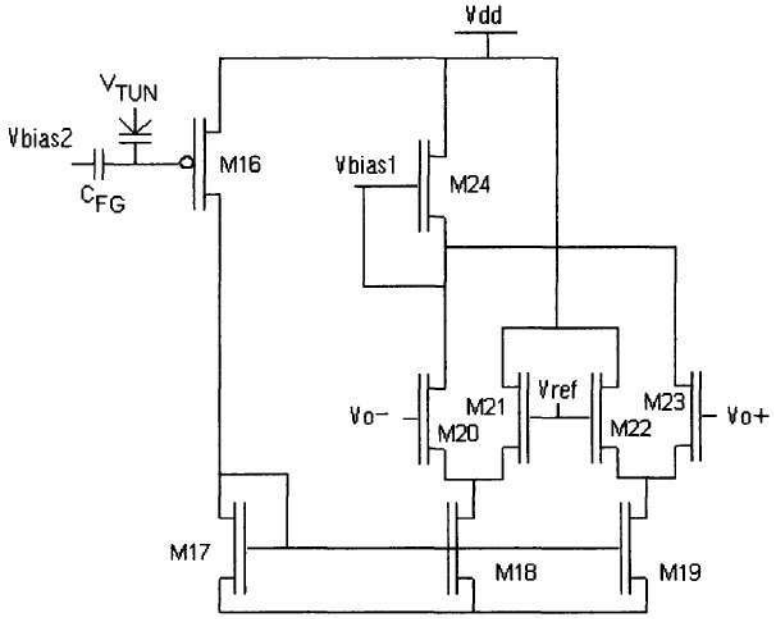

Figure 9: Traditional common mode feedback circuit used with the OTA of Fig. 4. Transistor M_{16} is a floating-gate transistor and sets the bias current for the entire OTA. The current that flows through M_{16} is ideally the same current that will flow through M_3. The two differential input pairs act to keep the common mode voltage of the OTA equal to the value of Vref applied to the gates of M_{21} and M_{22}. The bias transistor M_3 of Fig. 4 is controlled by the mirrored gate voltage of M_{24}.

One of the disadvantages of this approach is the nonlinearity of the CMFB circuit. Because the CMFB circuitry is composed of differential pairs it suffers from the same linearity issues as discussed previously concerning the input differential pair to the OTA. When the output voltage swing becomes large, the CMFB will contain nonlinear distortion which will then be reintroduced into the OTA circuit. Attention must also be paid to the stability of the common mode feedback loop to make sure it does not go unstable since it can be treated as an additional high gain amplifier loop.

The second form of common mode feedback is a new approach that uses capacitively coupled floating gates on the output legs of the amplifier [17]. A schematic of this can be seen in Fig. 10. The complete OTA with floating gate CMFB is shown in Fig. 11. The floating-gate node at $Vbias3$ is programmed so that the current in the output legs is equal to half of the bias current set by transistor N_5. This sets the output voltage in DC to be at half the rail voltage. Any differential change in the output voltages causes no change in the output stage voltage because as in the traditional common mode feedback the differential voltage change causes opposite but equal magnitude voltage changes to couple through the capacitors. In differential mode the gates of transistors N_8 and N_9 are at AC ground causing the output legs to look just like the output legs of Figure 4 except for the difference of not being cascoded.

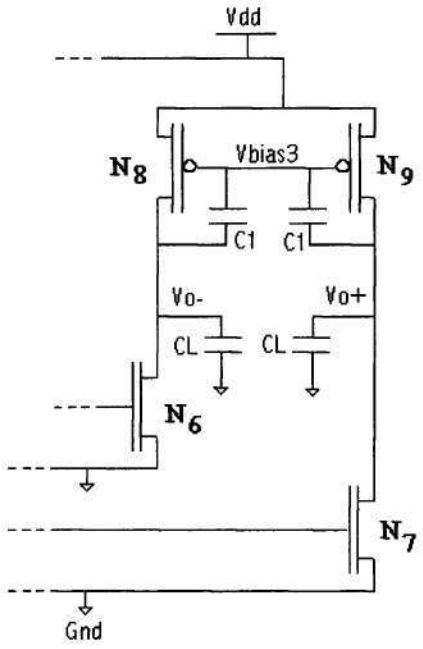

Figure 10: New approach for common mode feedback that uses floating gates on the output legs of the OTA in Fig. 4. Any differential change in the output voltage causes no change on the capacitively coupled node $Vbias3$. Any common mode change will cause the voltage seen at $Vbias3$ to change until the output voltage returns to the original value the bias current was programmed for. The complete OTA circuit can is shown in Fig. 11

A common-mode change in output voltage can be examined more simply by looking at what happens to just one leg of the output stage. Take for example the OTA output leg

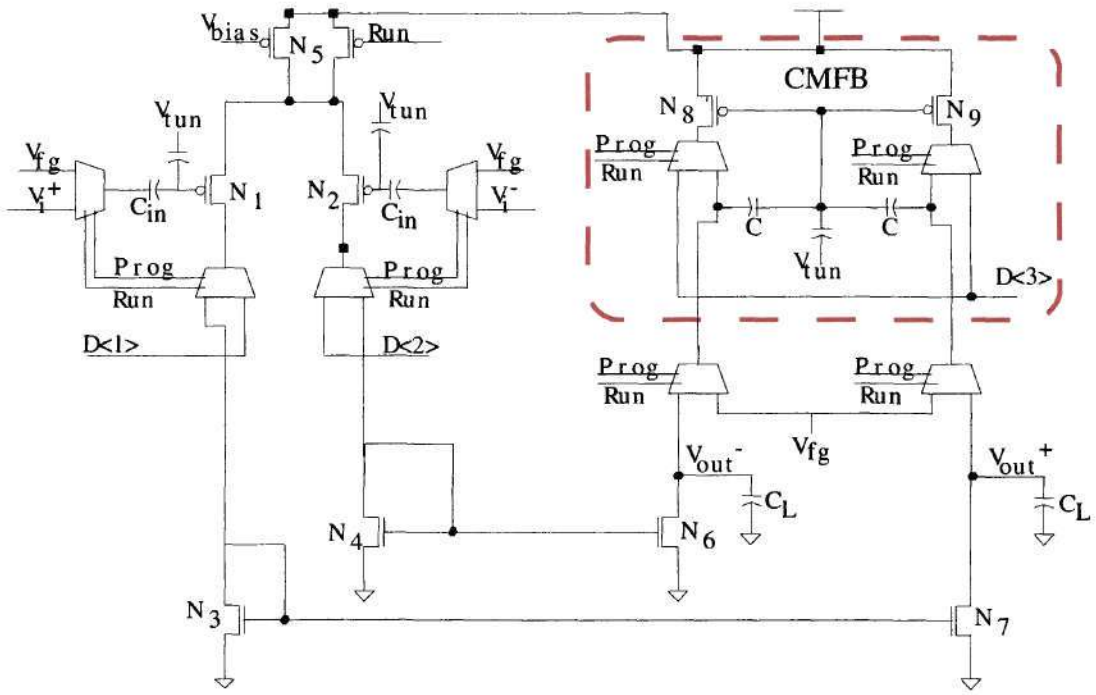

Figure 11: OTA of Fig. 4 using the proposed CMFB techniques from Fig. 10.

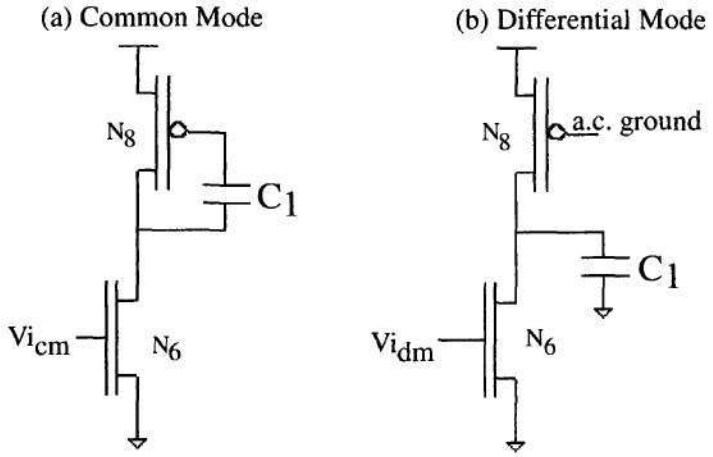

Figure 12: A closer inspection of the behavior of the floating gate common mode feedback circuit found in Fig. 10. The behavior of the output leg when a differential signal is applied to the input of the output leg can be seen in Fig. (b). In Fig. (a) a common-mode signal is applied to the input of the output leg causing the common-mode feedback transistor to behave as a diode connected transistor with a capacitive divider between C_1 and the gate capacitance of transistor N_8.

that produces the voltage Vo- containing transistors N_8 and N_6 of Fig. 10. If the voltage Vo- increases in voltage from mid rail the change in voltage is capacitively coupled through capacitor C_1 to the gate of N_8. The increase in voltage on the gate causes less current to flow through the drain of N_8 and this in turn lowers the voltage Vo- to mid rail. The operation can be viewed as a negative feedback loop. The small signal differential mode and common mode gain equations have been derived in [17] and are presented below,

$$A_{dm} = \frac{V_o}{V_i} = \frac{g_{m6} g_{m2} R_{out}}{g_{m4}\left(1 + \frac{sC_{gs,mirror}}{g_{m4}}\right)\left(1 + sC'_L R_{out}\right)} \tag{10}$$

$$\frac{V_o}{V_{cm}} = \frac{g_{m6}}{g_{m8}\kappa_{out} + s\left(\frac{C_L + C_{gs8}}{C + C_{gs8}}\right)} \cdot \left(\frac{1}{sC_{gs,m} + g_{m4}}\right) \cdot \frac{g_{m2}}{\left(1 + 2\kappa_{in}\left(g_{m2} - sC_{gs2}\right) r_{ds5}\right)}. \tag{11}$$

Where C'_L is the load capacitance plus floating gate CMFB capacitance, $C_{gs,m}$ is $C_{gs,4}$+$C_{gs,6}$ and R_{out} is $r_{ds,6} \parallel r_{ds,8}$.

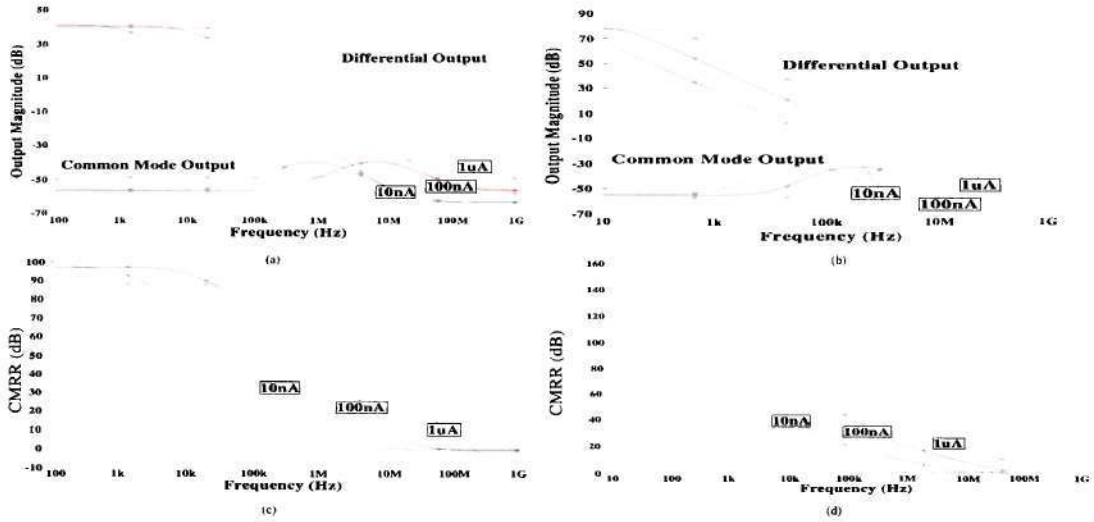

Figure 13: SPICE simulation results of small signal common-mode and differential-mode response of (a) OTA with new floating-gate CMFB, Fig. 11 and (b) OTA with traditional CMFB, Fig. 4. The plot shows data for three values of OTA bias currents–10nA, 100nA and 1μA. SPICE simulation results of CMRR versus frequency of (c) Fig. 11 and (d) Fig. 4. Plot shows data for three values of OTA bias currents–10nA, 100nA and 1μA.

A comparison of the frequency responses of the two CMFB circuits can be seen in Fig. 13. Both circuits have similar differential-mode and common-mode frequency responses. The

traditional design has greater differential mode gain because the output stage is cascoded thus making it's gain many orders of magnitude greater. The common-mode rejection ratio (CMRR) is also plotted in the figure for both OTAs. As can be seen in plots Fig. 13(c) and Fig. 13(d) the CMRR for the floating gate CMFB is close to the performance of the traditional OTA when the increased gain due to the cascoded output of the traditional OTA is taken into account.

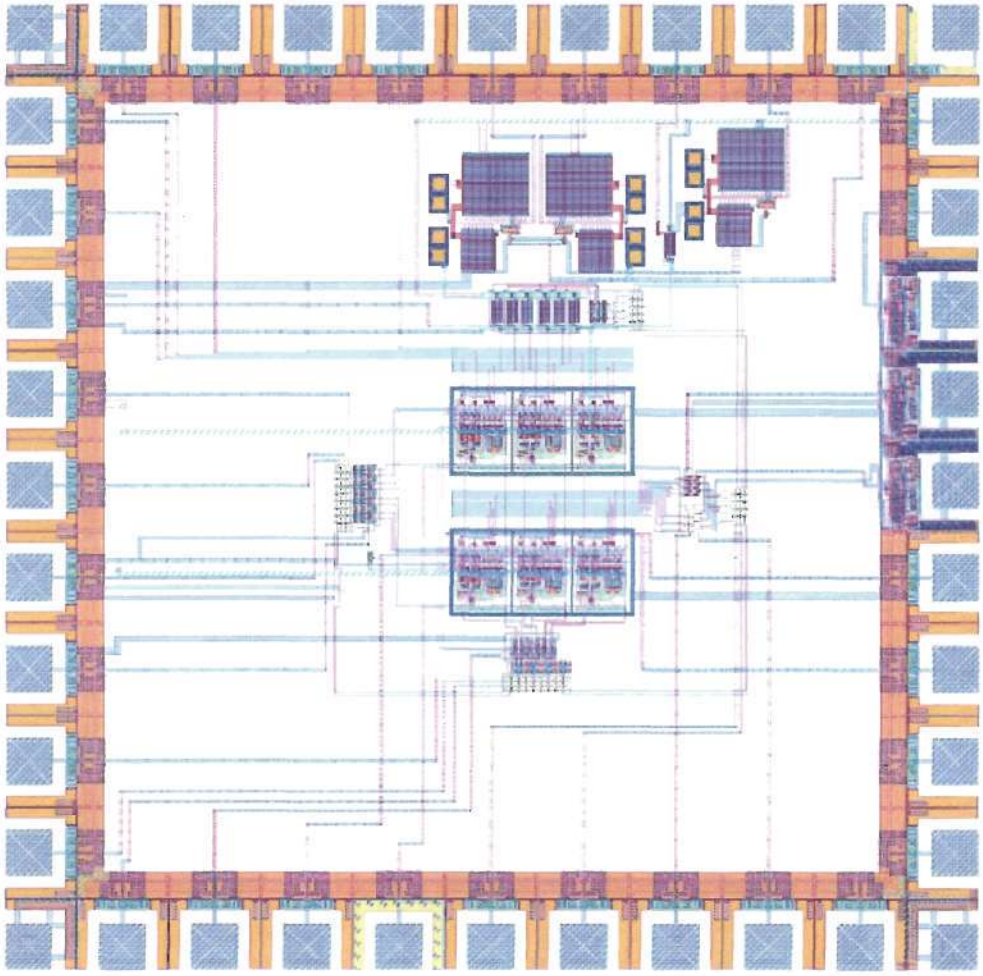

Figure 14: Fabricated test IC containing OTA test structures to obtain experimental test results for the proposed increased linearity technique and for the novel floating-gate CMFB. The IC was fabricated in 0.5μm CMOS using a double poly, four metal process. Chip area is 1500μmx1500μm.

A test circuit was fabricated to obtain experimental results for the new techniques of

CMFB and improving linearity. The IC was fabricated by MOSIS in AMI's 0.5μu CMOS, double poly, four metal process. A top level layout picture is shown in Fig. 14. Multiple OTAs were included in the test structure with different size differential pair input capacitances and with the two different types of CMFB. Experimental results for the improved linearity have already been shown in Fig 8.

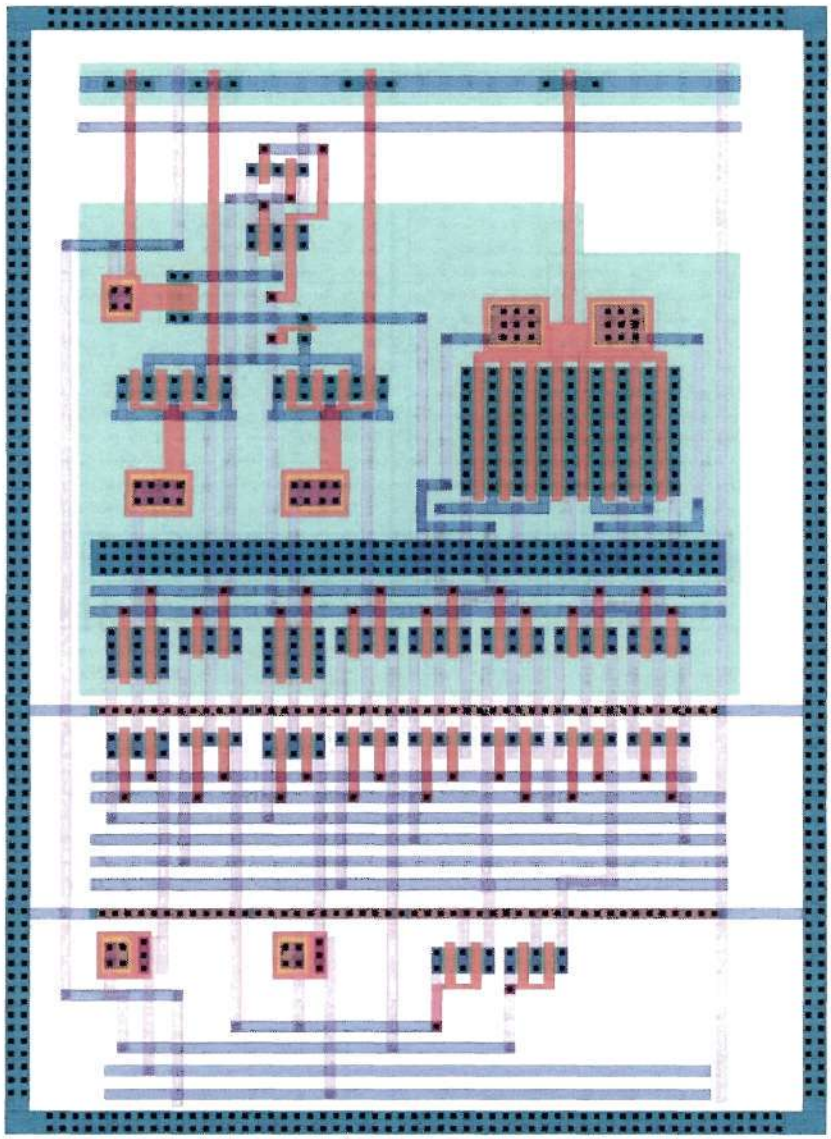

Figure 15: Layout picture of individual OTA cell used in layout of Fig. 14. A guard ring surrounds the OTA to help isolate it from substrate noise. The layout shown is of an OTA with the novel floating-gate CMFB.

The experimental results for floating-gate CMFB are shown in Fig. 16. The plot displays the results from a common-mode DC sweep for three different bias currents: 4nA, 40nA and 120nA. As seen in the figure the common-mode output voltage does vary around the desired output voltage of 1.55V. The errors are thought to come from layout mismatch of the OTA output legs. Because there is one floating gate for N_8 and N_9 it is not possible to adjust for any mismatch in the output legs of the OTA. If two floating gates were used instead of one the error should be reduced. Experimental results for the traditional CMFB can be seen in Fig. 17. The results show how the common-mode output voltage of the OTA can be easily set by changing the value of Vref and how the OTA automatically sets the output voltage to the desired value.

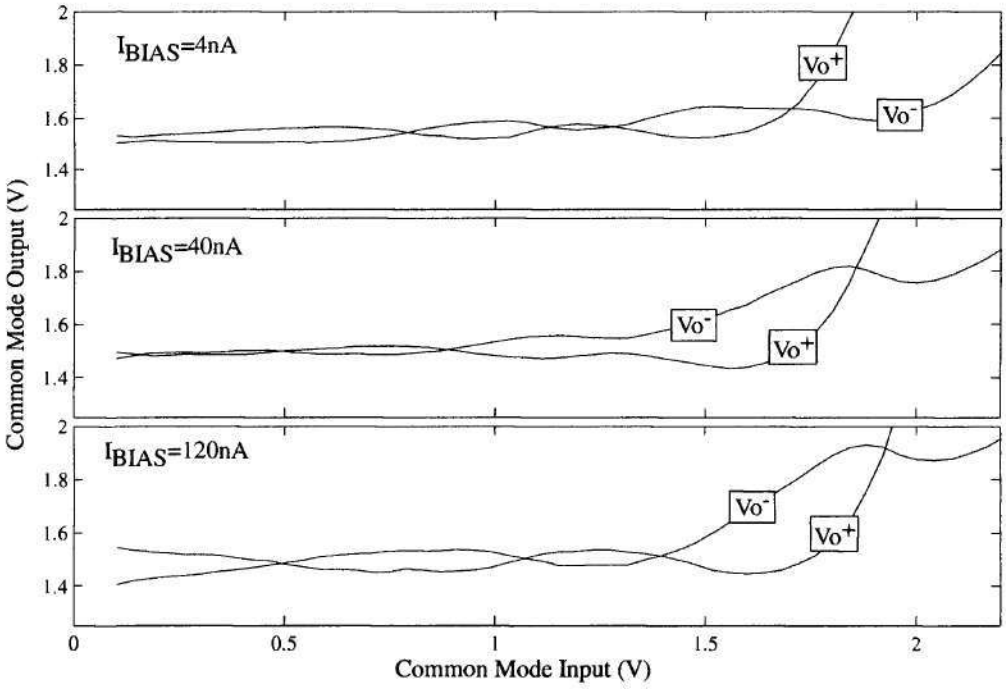

Figure 16: Common-mode DC sweep plots for floating-gate CMFB as seen in Fig. 11. Three values of bias currents are used–4nA, 40nA and 120nA. Output common-mode voltage is held at 1.55V.

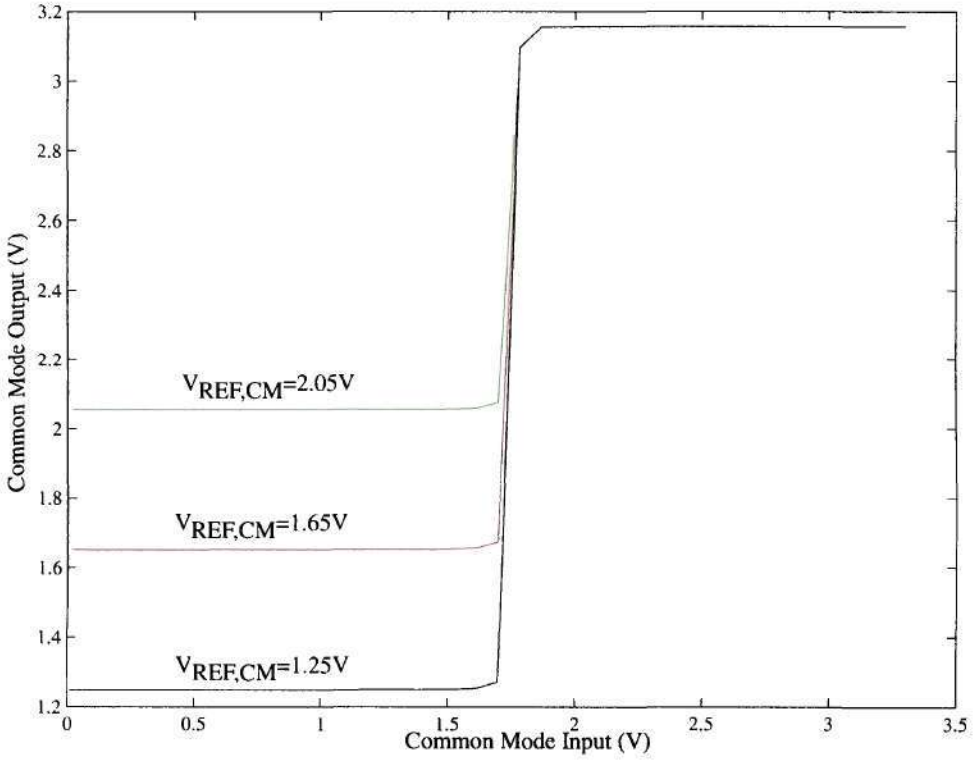

Figure 17: Common-Mode DC sweep plots for floating-gate CMFB as seen in Fig. 4 For the three different data sets the reference voltage Vref is changed. The experimental data shows how the common-mode of the OTA tracks what the desired common-mode output is set to.

CHAPTER III

DESIGN OF THE Δ-Σ MODULATOR

3.1 Top Level Overview

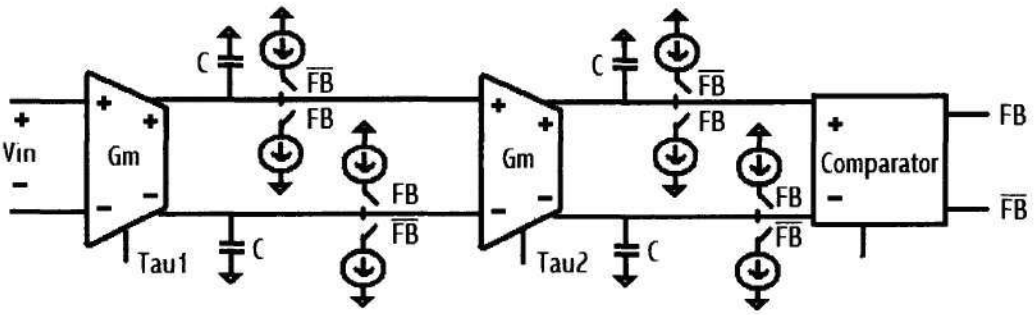

Figure 18: Top level model of the proposed Δ-Σ modulator. The basic building blocks are the Gm-C integrating structures, the switchable current sources, and the comparator. The G_m of the integrators is controlled by Tau_1 and Tau_2 which are set by I_{BIAS1} and I_{BIAS2}. I_{BIAS1} and I_{BIAS2} are programmable by floating gates. All four current switches for each modulator stage have equal current values and are set by a single floating gate.

The Δ-Σ modulator consists of three main elements: G_m-C integrating blocks, 1-bit current DACs and a comparator. For the proposed architecture the g_m-C integrating structures are arranged in the traditional cascade of integrator (COI) structure found in [5, 8]. Each integrator block integrates the previous ones output voltage until the last integrator's output is applied to the comparator. The high or low digital output of the comparator, which is the output of the modulator, is then returned back to the current DACs which subtract current from the integrator output nodes. The system has been designed to operate in subthreshold current ranges. The modulator works on the principle of negative feedback to reduce the total error in the feedback to zero. The block level layout of the modulator is shown in Fig. 18. The order of the modulator is determined by the number of integrating stages in the modulator. In the proposed research the modulator will be able to be scaled

up to a fourth order modulator. A switching network will allow for integrating blocks to be added or subtracted so that the modulator can go from a first order system to a fourth order system.

3.2 1-bit Current DAC

The feedback gain of the Δ-Σ modulator is realized by adding or subtracting current at the output voltage node of the G_m-C integrator. In this research, the adding and subtracting of current is performed by a series of NMOS and PMOS current mirrors that are turned on and off depending on if current needs to be sourced or sinked from the node. The current mirror configuration can be thought of as a 1-bit current DAC because it converts the digital modulator output, Fb and $\bar{\text{Fb}}$ into current being applied back to the output node voltages of the integrators.

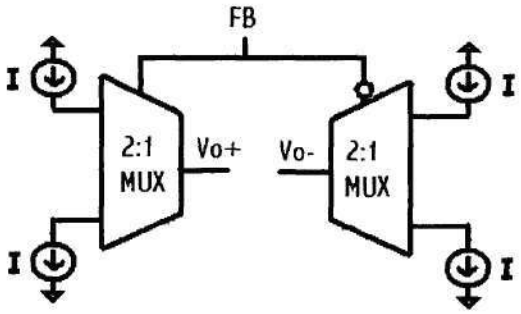

Figure 19: High level block diagram of the 1-bit current DAC. Each output voltage can be thought of as being attached to a 2:1 MUX. FB determines whether the MUX adds or subtracts current at the output voltage node. All of the currents are of the same value.

There are four current mirrors for each integrator. There is a NMOS and PMOS current mirror on each differential output voltage. When the positive input to the comparator is greater than the negative input $\bar{\text{Fb}}$ is high and Fb is low. The opposite is true for when the negative input is greater than the positive input. The bias current is provided transistor M_{25} which is a floating-gate transistor. Because M_{25} is just setting a bias it can be treated as a current source.

In simulating floating-gate circuits two approaches can be taken. If the floating-gate is providing a dc bias with no ac signal passing through, it can be model in SPICE by

applying a voltage source to the gate of the transistor to obtain the necessary current. If the floating-gate is being used in an ac signal path, such as in the differential input pair, another approach must be taken. For these cases it is necessary to provide the dc bias to the transistor but still allow an ac signal to go through it. To simulate this a very large resistor, 1TΩ, is connected to the floating-gate node. The other end is connected to a dc bias. The voltage from the bias source will bias the gate of the transistor but because it is nor directly attached to the node, the node will be able to responde to a transient signal. The large resistance allows for the voltage to be transferred to the the gate but stops any current from being sourced to the voltage bias supply.

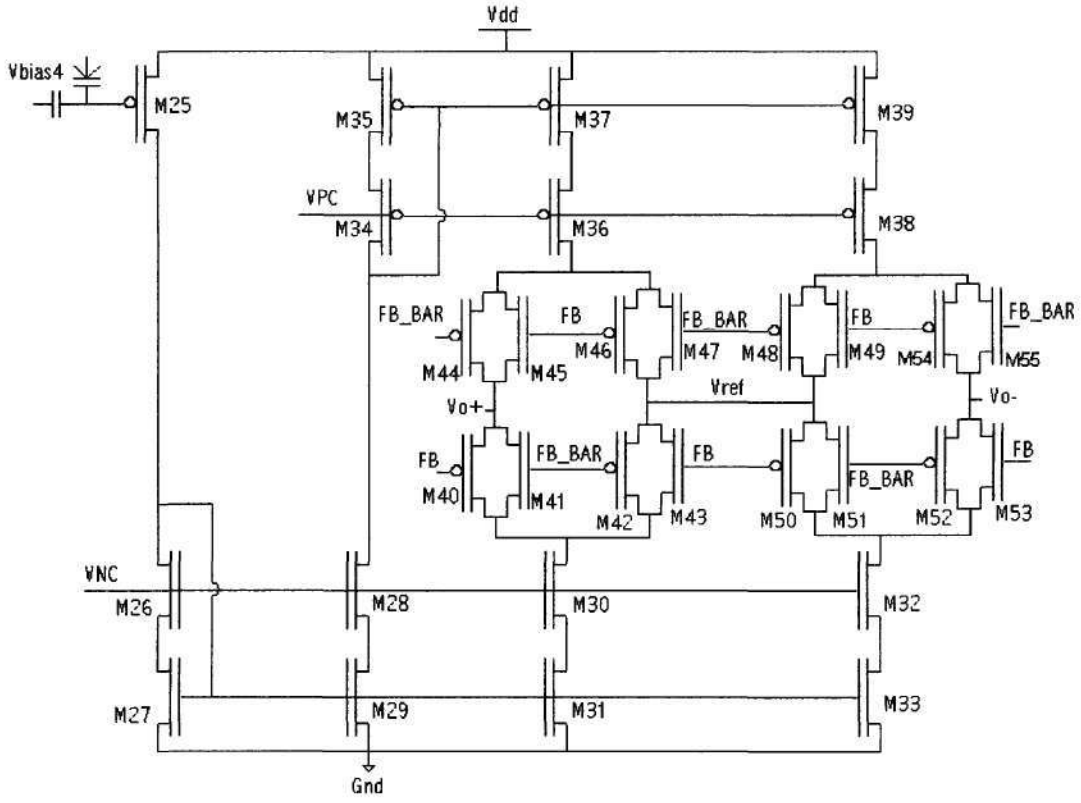

Figure 20: Current DAC used to realize the negative feedback in the Δ-Σ modulator. T-gates are used to turn the current either on or off for each output voltage node. When any of the current mirrors are not applying current to the output voltage node they are switched through another T-gate that sets the drain voltage of that current mirror to Vref, half of VDD. All of the current mirrors for each integrator have the same current which is set by the floating-gate transistor M_{25}. VNC and VPC are the cascode voltage biases.

The current feedback attempts to make the positive and negative nodes of the integrator

equal to each other. If one voltage is greater than the other, current is subtracted from the larger node and current is added to the smaller node voltage until the two nodes are equal. An example of how the current DAC works is next. If the positive output voltage becomes greater than the negative output voltage the comparator makes $\bar{Fb}$ go high and Fb go low. The NMOS current mirror for the positive voltage node will be turned on to remove current from the positive voltage node and the PMOS current mirror for the negative voltage node will be turned on so that the voltage increase. This is negative feedback because it is forcing the output voltage nodes to become equal to each other, reducing the error. The other two current mirrors that are not being used, the PMOS mirror attached to Vo+ and the NMOS mirror attached to Vo- are set to Vref, where Vref is half of VDD. The unused current mirrors are set to Vref so that the drain voltage fluctuation that occurs when the mirror is turned back on are minimized. If the mirror was not set to vref while it off it's output voltage would go to another voltage that might not be close to the output voltage. This is a problem because when it turns back on there would be a large voltage difference across the drain and source of the transistor. This in turn would produce an unnecessary transient because of the quick change of voltage across the capacitance of the T-gate and the load capacitance. By setting the mirrors that aren't used to the half rail voltage the spiking is minimized when the mirror is turned on because the output voltage of the mirror is already close to the half rail voltage value.

The feedback back DAC waveform and the matching of the feedback current are important to take into account because they can degrade the performance of the modulator if care is not taken during the design [3]. Using cascode transistors helps to increase the matching of the current from mirror to mirror because the cascode transistors fix the voltages on the drain of the mirror transistors to be the same. Because there is no variation between drain voltages the early effect is reduced and the currents should be matched. Fb and $\bar{Fb}$ should have the same pulse width and should be matched as closely as possible in rise and fall times.

3.3 Comparator Structure

Traditionally in Δ-Σ modulators the 1-bit quantizer consists of a comparator and a latch which is controlled by the clocking signal, Fig. 21. It is the latching of the comparator that allows for the modulator to be oversampled. An interesting issue that arises due to the modulator being continuous-time is what happens when the clocking frequency for the latch goes to infinity, or simply put, not clocking the modulator at all. This is not an option in switched-capacitor modulators due to the necessity of all of the components needing to be clocked. However for continuous-time Δ-Σ modulators it is a question that does not currently have an answer. In switched capacitor circuits stability is increased in the modulator by using a multi-bit comparator on the output. This increases the complexity of the circuit by a large degree. By using an unclocked comparator in a continuous-time Δ-Σ modulator the possibility exists to achieve the benefits of a multi-bit comparator with a standard 1-bit unclocked comparator.

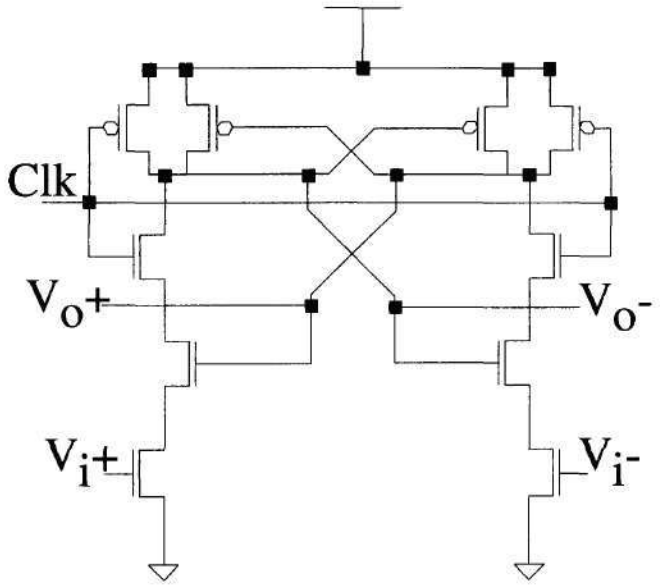

Figure 21: Traditional latched comparator.

The proposed Δ-Σ modulator will contain two interchangeable comparator structures. One is a standard latched comparator that is controlled by a clock signal [5]. The other comparator structure is an unclocked comparator, see Fig. 22. This will cause the system

to run at the speed dictated by the comparator. This raises the question of what to do with the modulator output? Because the output of the modulator will be unlocked a standard FFT cannot be used to determine the spectral content of the output. It is proposed that one way to analyze the data is to let the digital output represent the continuous derivative of the modulated input signal. In order to reconstruct a representation of the input using the modulator output it will be necessary to perform a integration of the output. This should hold true for a 1^{st} order modulator, but modulators of higher order will have derivatives of higher order in the digital output spectrum thus making them much more difficult to reconstruct at this time. Further analysis and an attempt at reconstructing the unlatched digital output stream is in section 4.4 which discusses the experimental results for the unlatched comparator.

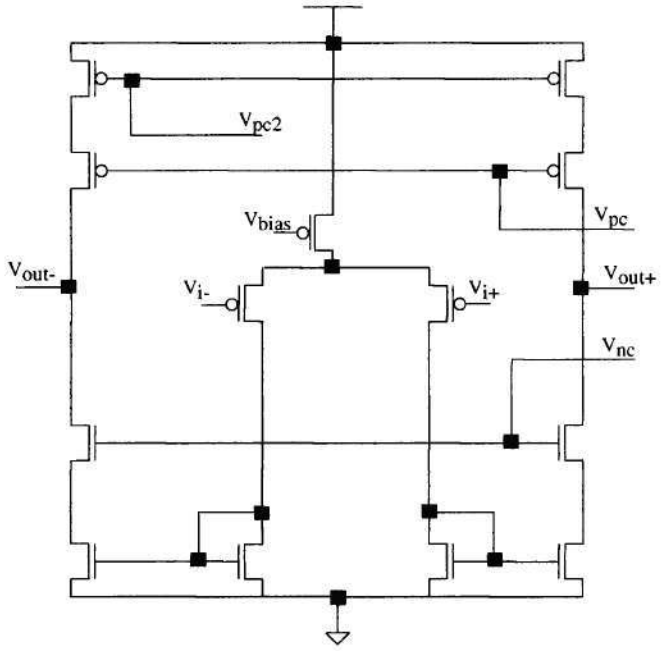

Figure 22: Unlatched comparator used for testing the modulator in an unclocked state. This is a standard differential Op-amp that is designed to run in an open loop state and to have a very large differential gain.

3.4 SPICE Simulation Results

SPICE simulations were performed using the Cadence suite of software. The simulations were performed to verify the proof-of-concept of the modulator and to ensure proper operation for the desired bias currents. A 1^{st} order modulator was simulated to ensure general operation of the design. The output spectrum can be seen in Fig. 23. The SPICE simulation shows that for a bias current of 600nA, a feedback current of 250nA and a sampling frequency of 5MHz an output spectrum is produced that has a dominant peak at the fundamental frequency and only one other peak at the 3^{rd} harmonic peak. It can be hypothesized that if a smaller input voltage were to be used the 3^{rd} harmonic would be reduced by a larger amount. This is because an input voltage of 100mV is getting close to where the OTA will be out of the modulators linear range.

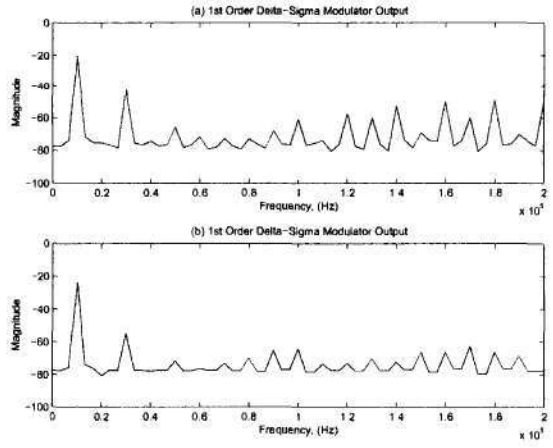

Figure 23: Output frequency spectrums for the 1^{st} order modulator. Plot (a) has no floating-gate capacitance at the input. Plot (b) has 30fF floating-gate capacitors on the input differential pair. I_{bias} was 600nA, feedback DAC current was 250nA and Vin was 100mV at 10KHz, Fs=5MHz. The traditional CMFB circuit was used for these simulations. Notice the large decrease in 3^{rd} harmonic magnitude compared to the small decrease in fundamental frequency magnitude.

SPICE simulation were also done for a 2^{nd} order modulator. However this simulation uses non-optimized coefficient values. This simulation was performed to make sure that a second order section would modulate correctly. Because of the long simulation times required for each SPICE simulation optimization of the coefficient values was performed using a high level model in Simulink, this is discussed further in the section on high level

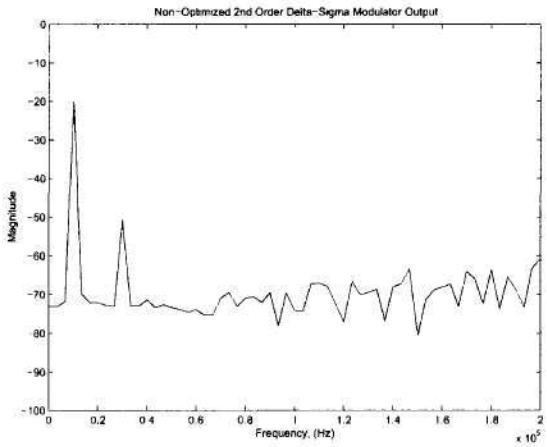

Figure 24: Output frequency spectrum for 2^{nd} order modulator. The simulation was performed to ensure the proper operation of the modulator

modelling, section 5.1. By using an accurate high level model it is possible to get a faster understanding of the behavior of the modulator over the entire feed-forward and feedback coefficient ranges.

CHAPTER IV

EXPERIMENTAL Δ-Σ MODULATOR MEASUREMENTS

Using the circuit topology presented in Fig. 18 an experimental Δ-Σ integrated circuit was fabricated. A test setup was designed to enable accurate testing of the modulator. Experimental results for a 2^{nd} and 3^{rd} order modulator were then taken along with other supporting measurements. Experimental results for the modulator with the unclocked comparator were also taken.

4.1 Test Setup

A 4^{th} order modulator was fabricated in the AMI 0.5μm process provided through the MOSIS service. The process is a standard CMOS double poly, four metal process. The modulator was designed so that the order of the modulator could be changed from a 1^{st} order to a 4^{th} order modulator through the use of digital selection logic. The layout of the test IC is shown in Fig. 25. Care was exercised to minimize the clock and digital signal lines from the analog portions of the modulator. Guard rings were placed around all critical analog components so that substrate noise from the clocked signals could be reduced. A separate analog and digital ground, AGND and DGND, as well as sperate analog and digital supply rails, AVDD and DVDD, were also employed. The modulator output was passed through an inverter string buffer to ensure a clean digital output that would be less distorted from parasitic board and package capacitance. The differential integrator outputs of each integration stage are passed to buffered output pins so that the integration outputs can be observed.

The test setup for measuring the experimental modulator is shown in Fig. ??. The fabricated IC is placed on a custom fabricated PCB, Fig. 28, that enables the IC to interface with the programming board, the FPGA and the input signal to the modulator. The fabricated PCB in shown in greater detail in Appendix A. The programming for the

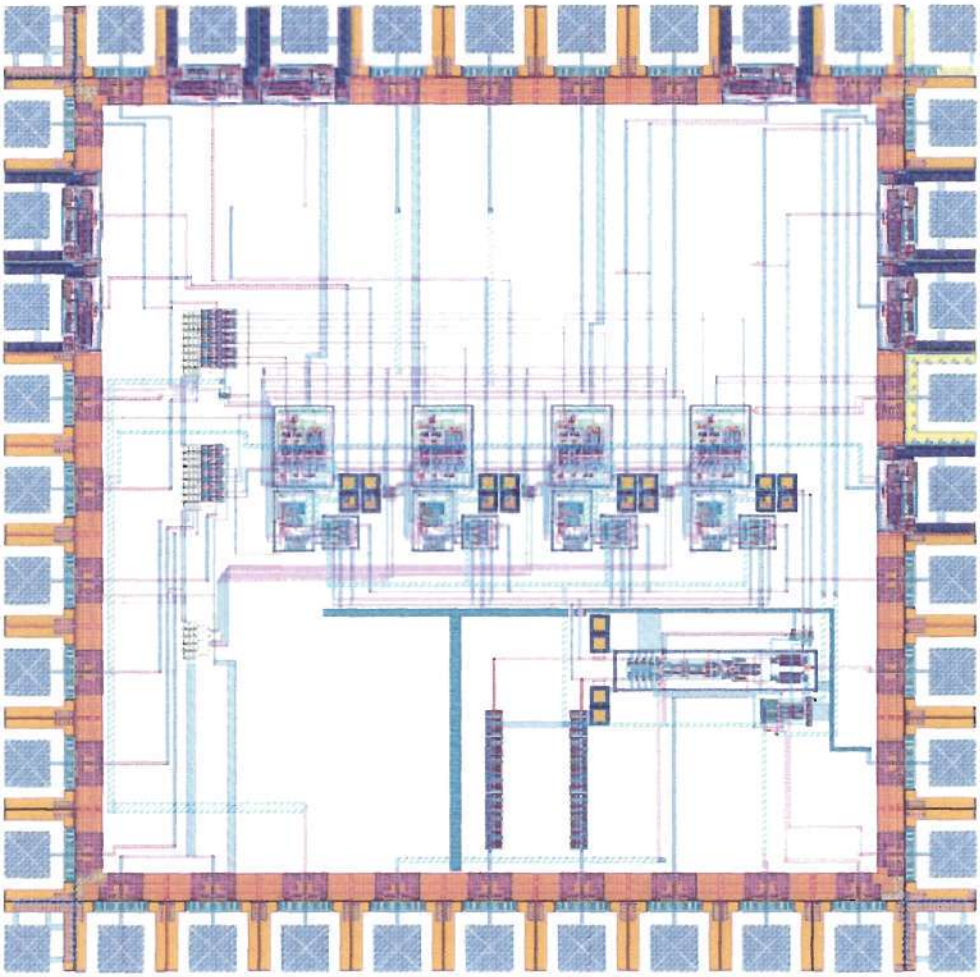

Figure 25: Layout for a Δ-Σ modulator that is scalable from a 1^{st} to a 4^{th} order modulator. The modulator is fabricated in a standard 0.5μm process using double poly and four metal layers. Chip area is 1500μmx1500μm

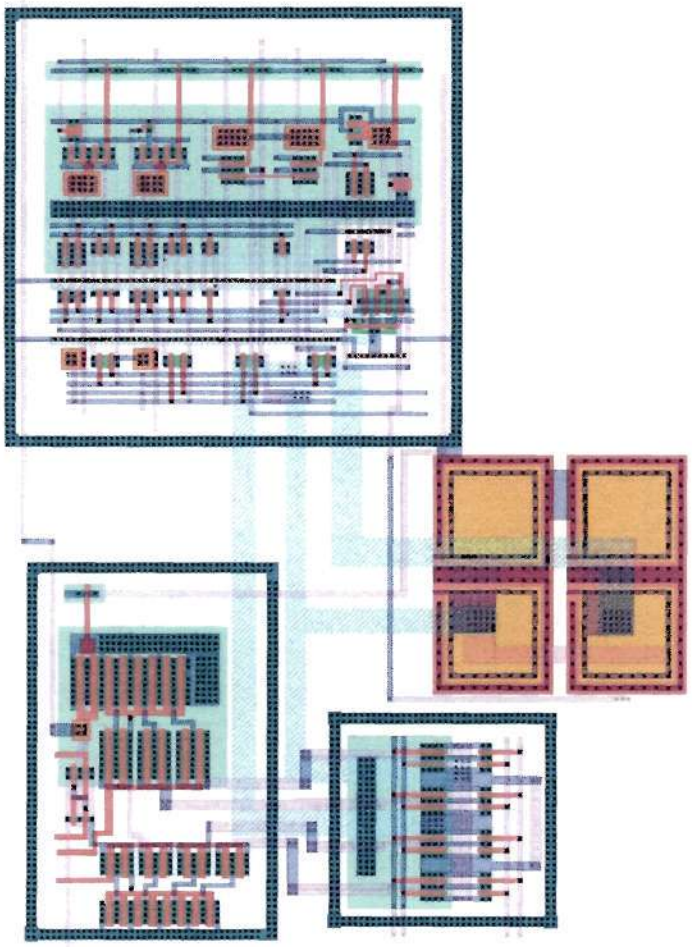

Figure 26: Zoomed in image of individual integration and feedback circuit layout. Four of these cells make up the entire Δ-Σ modulator shown in Fig. 25. The upper left cell is the OTA. Below the OTA is the current mirror DAC block and next to that cell are the switches for the current DAC. The capacitors can be seen next to the cells.

floating-gates on the modulator and the bias voltages for the modulator are provided by the programming board. This is a generic PCB that was designed by our research group to aid in the programming of floating-gates [19]. The programming board not only aids in programming but it also contains auxiliary DACs that are used to provide the needed bias voltages to the modulator.

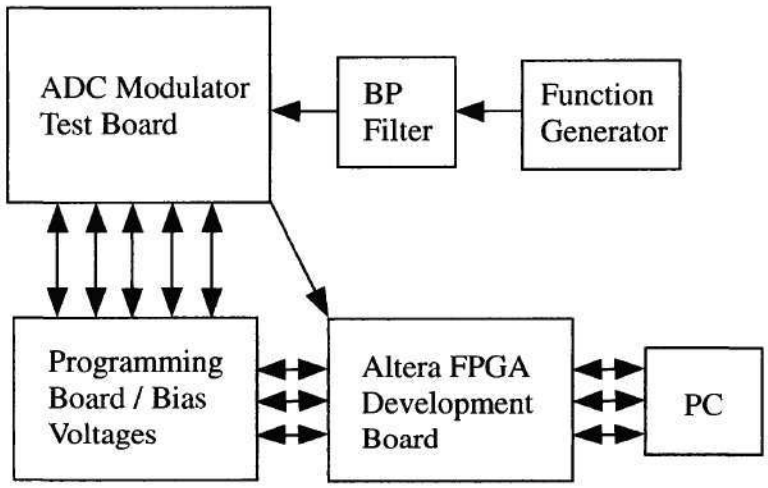

Figure 27: Test setup for characterizing modulator. The PC controls the FPGA board through an ethernet connection. The FPGA board controls the programming board and also supplies the clock for the comparator and samples the digital output stream of the modulator. The programming board is used to program the floating gate elements and also provides voltage biases for the modulator. The input sine wave signal is passed through a bandpass filter to remove any distortion in the input signal before it is passed into the input of the modulator.

The FPGA connects to both the programming board and directly to the custom PCB that houses the modulator. The FPGA interface with the programming board controls the programming for the floating-gates and provides the digital logic signals used for controlling the modulator behavior and structure. The FPGA interface that connects directly to the custom PCB is used for providing the modulator clock signal and for retrieving the digital modulator output. The FPGA that is used is an Altera Stratix evaluation board and all of the routines used are stored on the processor in a combination of VHDL and C code. The PC allows for an easy interface for controlling the interaction of the FPGA and the rest of the system through the MATLAB software. After the FPGA obtains the digital output the data is retrieved by MATLAB and post-processed so that the output spectrum can be

analyzed and data measurements performed.

The input signal for the modulator is provided from a function generator whose output sine wave is passed through a bandpass filter to remove any impurities from the signal. The bandpass filter is a continuous time discrete IC from MAXIM and the filter is built on a standard bread-board that has an aluminum ground shielding surrounding the entire board.

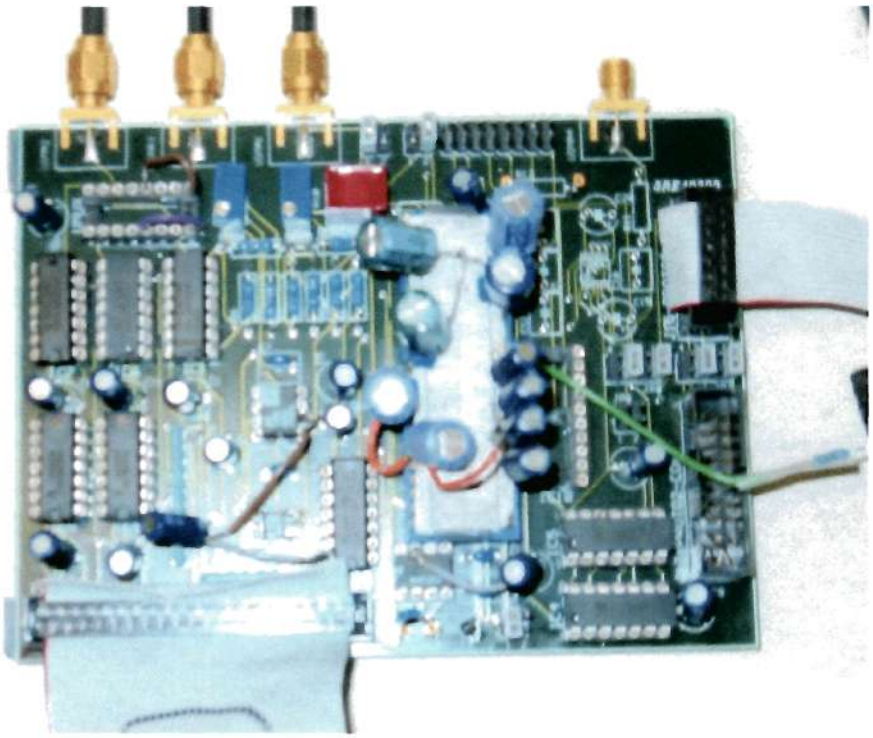

Figure 28: Picture of fabricated PCB designed for testing experimental modulator. The modulator IC can be seen in the middle of the board. Notice the large number of capacitors that were added after fabrication to aid in the reduction of bias voltage noise.

The test setup for characterizing the performance of the modulator is not an ideal setup. If resources were unlimited the modulator would be tested using probes to an unbonded IC with clean bias voltages, the function generator would be an ideal sine wave with a noise floor of -150dB and all of the testing would take place in a noise free environment. Unfortunately this is not the case. The function generator that was available for testing was not a high quality audio band signal generator, instead it was a standard direct digital synthesis function generator that had a poor noise floor and also had linearity issues caused

by spurious harmonics. The bias voltages for the modulator were initially incredibly noisy with over 100mV of random noise on the voltage. After the addition of large capacitors soldered directly to the IC the noise was dropped to 30mV, an improvement but still too much noise. The additional capacitors can be seen in Fig. 28. The addition of the capacitors reduced the noise floor of the modulator 5dB down to -97dB.

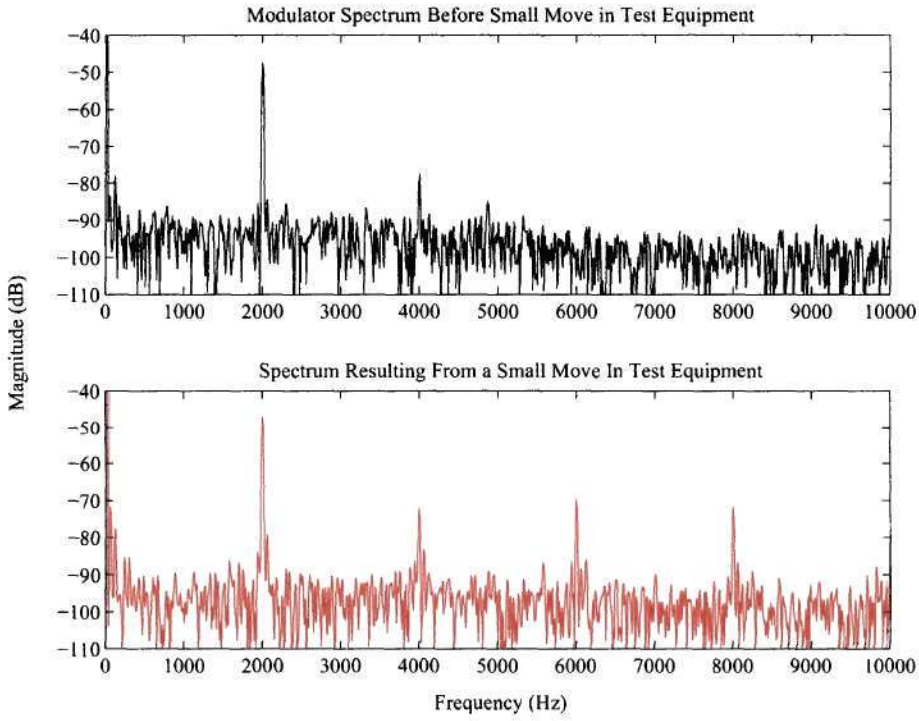

Figure 29: Two modulator output spectrums showing the results of moving the test equipment on the testing table. The top spectrum is before a move in the equipment and the bottom graph is the resulting spectrum after the move. From this data it can be seen that there are large sources of environmental noise that are degrading the performance of the modulator

The custom PCB that houses the modulator is shielded by a grounded box coated with aluminum foil to help reduce noise from the environment. The shield does improved performance but there is still a large quantity of environmental noise in the test set up area. Figure 29 shows the results of what happens to the modulator output spectrum when a small move in equipment on the testing table occurs. The effects of environment noise are very obvious in this figure. However, at this time it is still a matter of trial and error to find the optimum position of the equipment to achieve the best results. Another problem is

Table 3: 2^{nd} Order Modulator Experimental Results

Parameter	Value
F_{in}	2kHz
Bandwidth	8kHz
Max. SNR	59.2 dB
Max. SINAD	50.27 dB
Dynamic Range	$\approx$ 50 dB
Noise Floor	-97 dB

that the spectrums are not always continuously repeatable. It may be possible to get two successive modulator output spectrums to appear similar but over time the noise changes for the worse and shifting the equipment is needed again to lower the noise floor. The current test setup is adequate for proving the functionality of the modulator but it is not practical for trying for achieve optimum experimental data.

4.2 2^{nd} Order Results

A second order modulator was tested using the setup described in the above section. Figure 30 shows the entire modulator output spectrum and the desired noise shaping behavior of the modulator. Figure 31 displays the desired 8kHz band of interest that the data is data taken for. Experimental results for the 2^{nd} order modulator output is shown. The input frequency is 2kHz, the clock frequency is 2MHz and the bandwidth used for calculating SNR and SINAD is 8kHz. The dynamic range of the modulator is shown in Fig. 32. The maximum SINAD value is 50.27dB and that is achieved for an input voltage of 51.5mV. The results from the experimental measurements are summarized in Table 3. The idle channel noise floor is shown in Fig. 33.

From Fig. 31 it is visible that there is a large undesired 2^{nd} harmonic in the output spectrum. Because of the differential nature of the G_m-C integrator there should only be odd harmonics in the output spectrum. The second order harmonic is thought to be the result of inaccuracies in the floating-gate programming of the differential pair, M_1 and M_2, and the output leg transistors M_{13} and M_{15}. Any mismatch in currents produces an unbalance in the G_m-C integrator which in turn causes the even harmonics to appear. It is also thought the second harmonic can also be due to mismatches in feedback DAC pulse

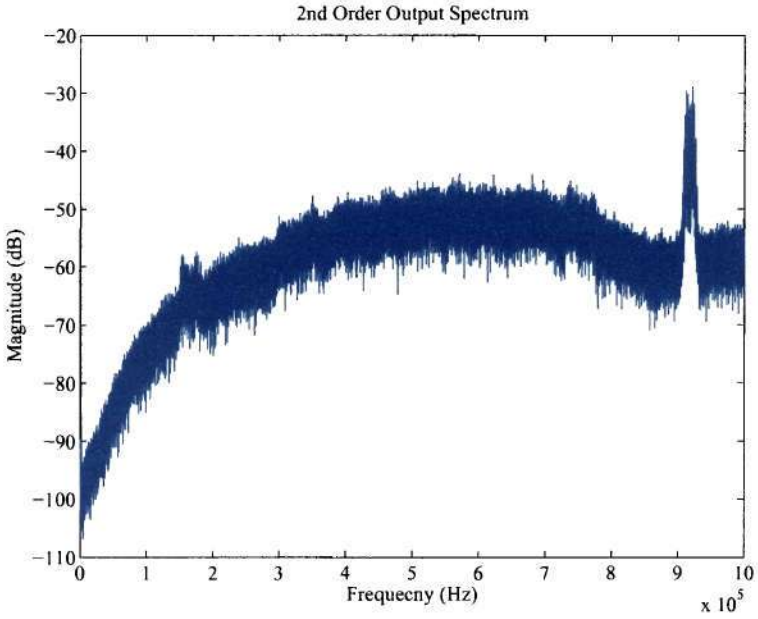

Figure 30: Output spectrum of 2^{nd} order modulator. The noise shaping of the quantization error is clearly present in this figure. The sampling frequency of the modulator is 2MHz

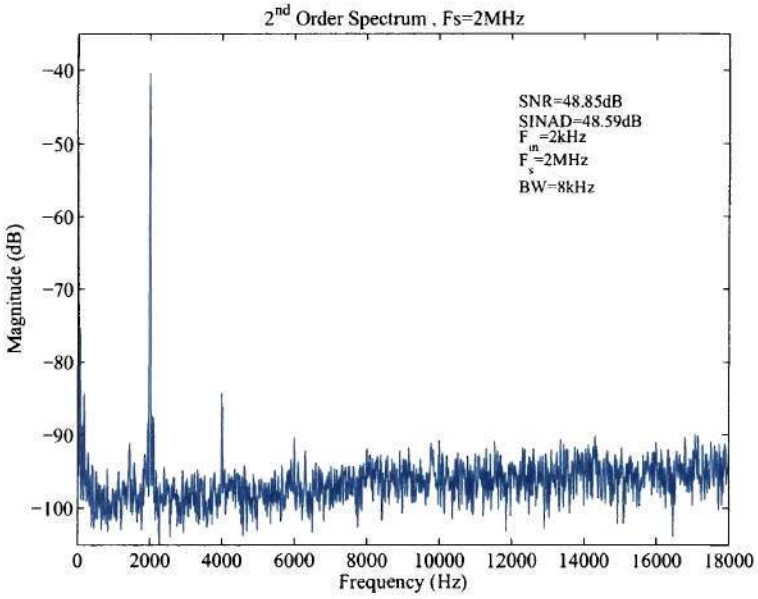

Figure 31: Output spectrum of 2^{nd} order modulator. The input integrator's bias current is 100nA and second integrator's bias current is 1uA. The feedback current values for the first and second integrator are 40nA and 100nA respectively. This plot shows results for an input voltage of 30.5mV

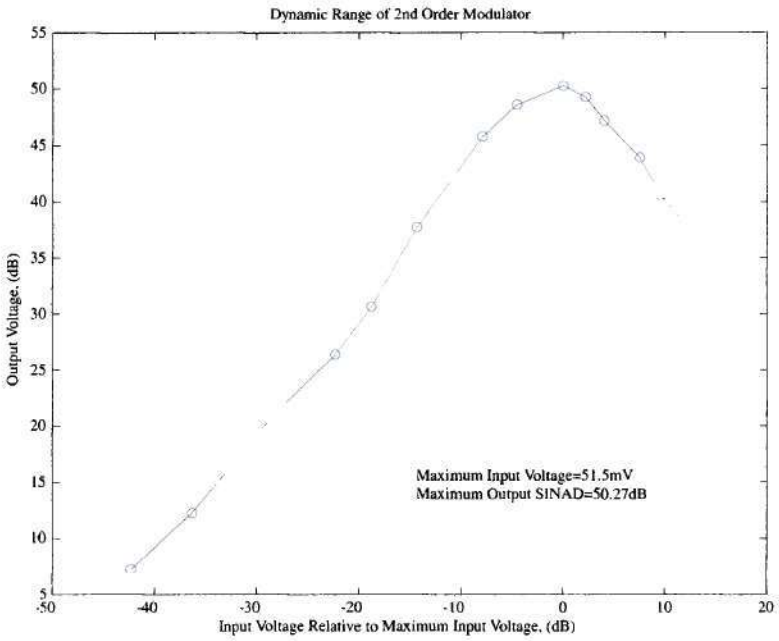

Figure 32: Dynamic range results for the 2^{nd} order modulator. Maximum SINAD is achieved at 50.27dB for an input voltage of 51.5mV with bandwidth of 8kHz.

shapes and magnitudes [3].

The improvements that result in increasing the matching between the differential pair currents can be seen in the output spectrums shown in Fig. 34. The improvement were made for an output spectrum that was consistently providing the same output spectrum over numerous multiple data sets. So it is determined that the tuning of the differential pair does aid in reducing the harmonics. However, for larger input signal amplitudes the tuning only causes a minor improvement and still leaves the offending second harmonic. It is believed that in these cases the mismatch current in the layout of the OTA output legs and the mismatch of currents in the 1-bit DAC play a large role in creating the error. For larger amplitudes the odd harmonics are also present but reduced from what they would have been without the addition of the floating gate input capacitance. It can be concluded that further decreasing the size of the floating-gate input capacitor would result in an increased reduction of the size of the odd harmonics.

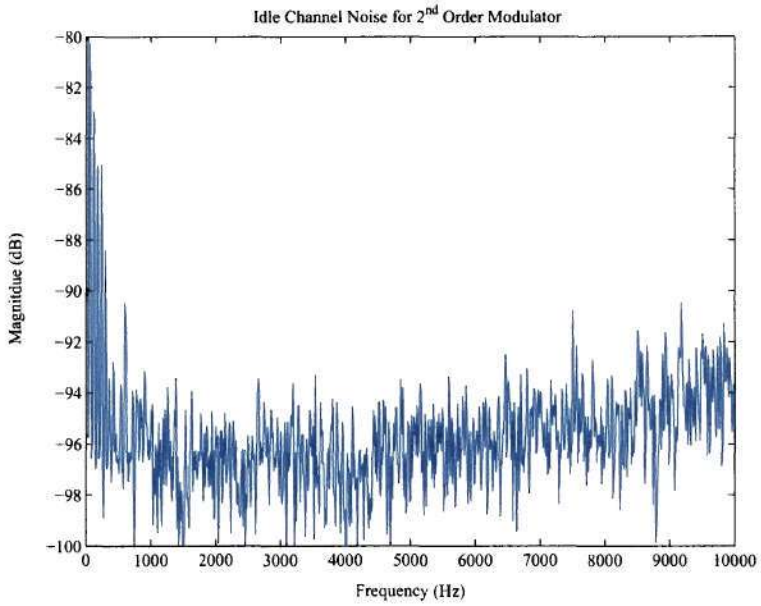

Figure 33: Noise floor for output spectrum of the 2^{nd} order modulator.

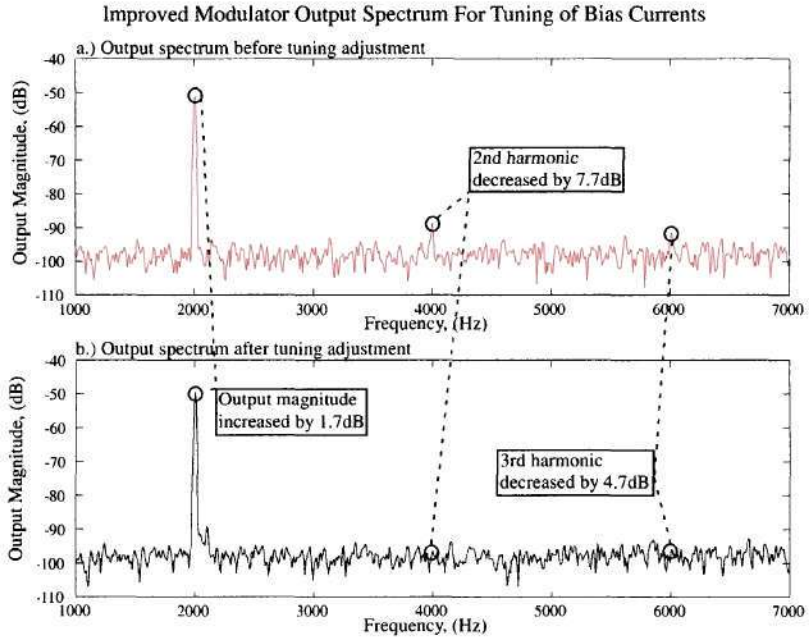

Figure 34: An increase in the differential pair matching reduces the 2nd and 3rd harmonics shown in spectrum (a) to where they almost vanish in spectrum (b). A slight increase in the fundamental frequency magnitude also occurs.

Table 4: 3^{rd} **Order Modulator Experimental Results**

Parameter	Value
F_{in}	2kHz
Bandwidth	8kHz
Max. SNR	50.2 dB
Max. SINAD	40 dB
Dynamic Range	$\approx$ 50 dB
Noise Floor	-97 dB

4.3 3^{rd} Order Results

A third order modulator was tested using the setup described in the above section. Figure 35 shows the modulator output spectrum and the desired noise shaping behavior of the modulator. Experimental results for the 3^{rd} order modulator output are shown in Table 4. The input frequency is 2kHz, the clock frequency is 2MHz and the bandwidth used for calculating SNR and SINAD is 8kHz. The dynamic range of the modulator is shown in Fig. 36. The maximum SINAD value is 40.27dB and that is achieved for an input voltage of 40mV. The results from the experimental measurements are summarized in Table 4. The idle channel noise spectrum for the 3^{rd} order modulator is shown in Fig. 37.

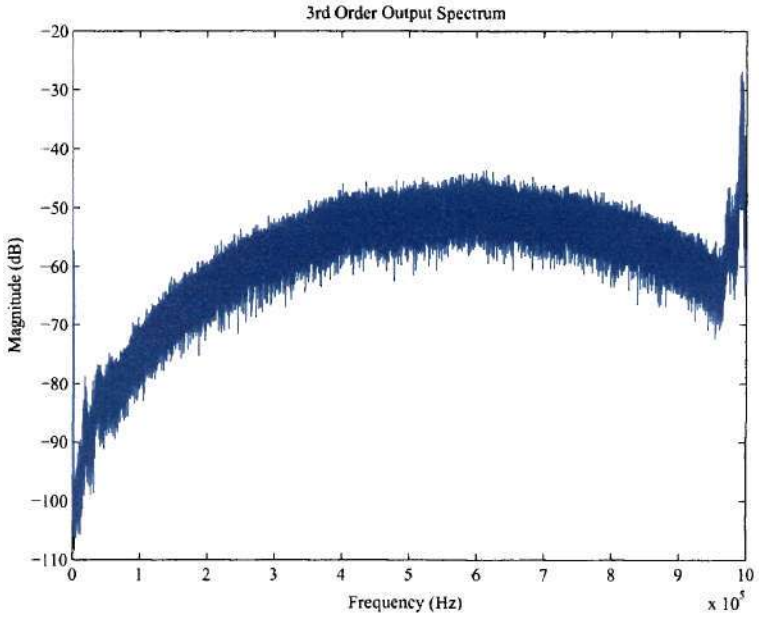

Figure 35: Output spectrum of 3^{rd} order modulator. The sampling frequency is 2MHz and the signal input frequency is 8kHz.

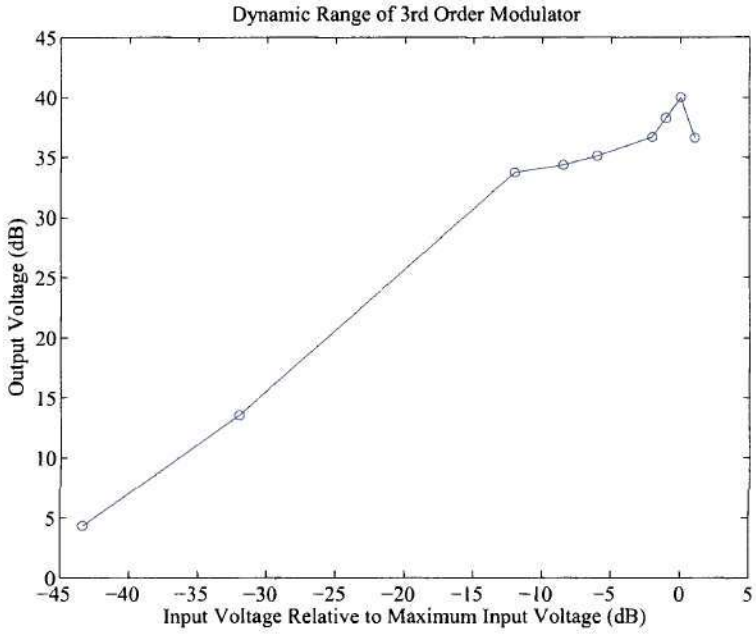

Figure 36: Dynamic range plot for 3^{rd} order modulator. The maximum SINAD value of 40dB is achieved for an input voltage of 40mV which is referred to as overload value for the modulator.

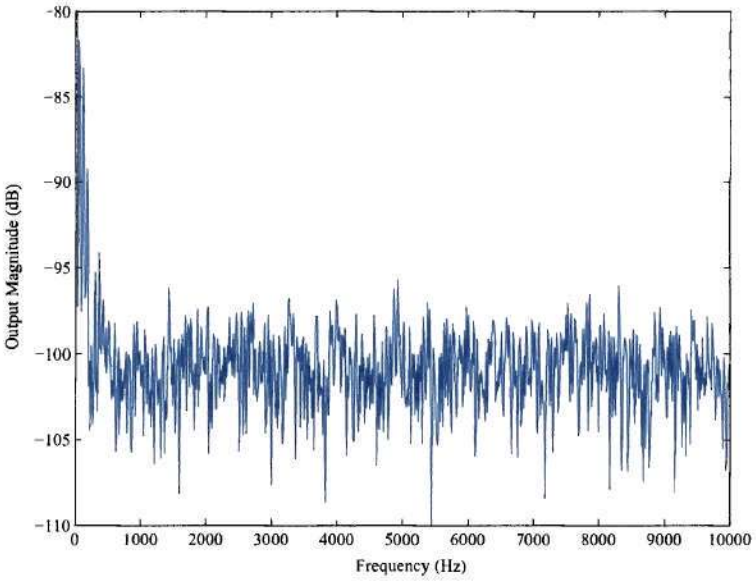

Figure 37: 3^{rd} Order Noise floor

During one of the testing sessions of the modulator an error occurred while programming the DAC bias currents and instead of being programmed to the values in Table 7 they were all programmed to around 1μA. The resulting output spectrum is shown in Fig. 38. The noise transfer function for this modulator is very impressive and would ideally be what is desired, down to -145dB at 0Hz. However, there is a problem. The DAC feedback current values are so large they completely overpower the current output generated by the input feed forward signal thus greatly diminishing the magnitude of the input signal. The input signal magnitude for the shown modulator was 30mV but the output spectrum has an output signal magnitude of only -95dB.

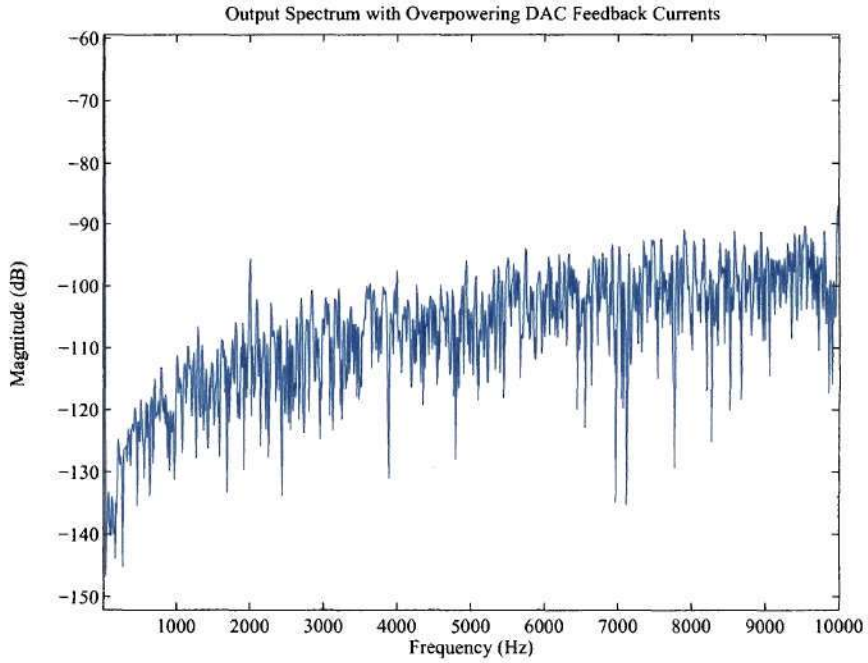

Figure 38: 3^{rd} order modulator output spectrum for the same modulator coefficients used for the results in Table 4 except that the DAC bias currents are all set to 1μA. The noise transfer function, (NTF), is much more ideal but the signal transfer function, (STF), has been distorted. The input signal that is shown in the figure is a 30mV input signal which is much larger than the -90dB showing up in the output spectrum.

In fact the entire signal transfer function (STF) was distorted from it's ideal all pass behavior. The STF now has a high pass behavior that follows the shape of the noise spectrum, but instead of flatting out at 0dB the STF flattens out at -80dB. Therefore, any signal passed through the modulator is attenuated by -80dB. So while the NTF is greatly

Table 5: Summary Of Harmonic Magnitudes For Fig. 39

VNC	VPC	1^{st} Harmonic	2^{nd} Harmonic	3^{rd} Harmonic
1.25V	1.85V	−51dB	−75dB	−80dB
1.15V	1.95V	−52dB	−82dB	−94dB
1.05V	2.05V	−53.5dB	−90dB	−95dB
0.95V	2.15V	−51dB	−89dB	−78dB
0.85V	2.25V	−52B	−85dB	−93dB
0.75V	2.35V	−60dB	−70dB	−65dB

improved for these coefficient values, the STF is so poor that it reduces the benefit of the great noise shaping. The noise shaping in Fig. 38 shows that the noise floors in Fig. 37 and Fig. 33 are not reaching the theoretical noise floor limitations. The limitations on the noise floor will be caused by the thermal noise of the entire modulator. It appears that the quantization noise still dominates the noise floor for the modulator outputs.

For the 3^{rd} order modulator an investigation was performed into the effects the cascode bias voltages, VNC and VPC, have on the modulator output spectrum, the results can be seen in Fig. 39. Intuitively one would expect that as the cascode bias voltages are reduced to their minimum values the harmonic distortion should also decrease because a larger voltage swing is being allowed at the output of the modulator allowing a more linear behavior. The maximum and minimum output swings for the OTA are $2V_{VDS(Sat)}$ and as the V_{gs} of the cascode transistor is reduced the $V_{VDS(Sat)}$ for that transistor is also decreased, thus increasing the signal swing. Therefore the cascode bias voltages should be set at the minimum voltage values of $2V_{TH}+V_{VDS(Sat)}$ to achieve the least amount of distortion caused by clipping of the output signal. Cascode bias voltages of less than the minimum voltage result in the output transistors operating in the ohmic region thus degrading the behavior of the OTA, this is shown in Fig. 39(f). The results of Fig. 39 are summarized in Table 5.

4.4 Modulator with Unlatched Comparator Results

The output spectrum for the 1^{st} order modulator when running in the unclocked mode of operation can be seen in Fig. 40. The modulator output consists of well defined high and low states and a half-rail, midrange state. The output seen in Fig. 40 is a quantized version

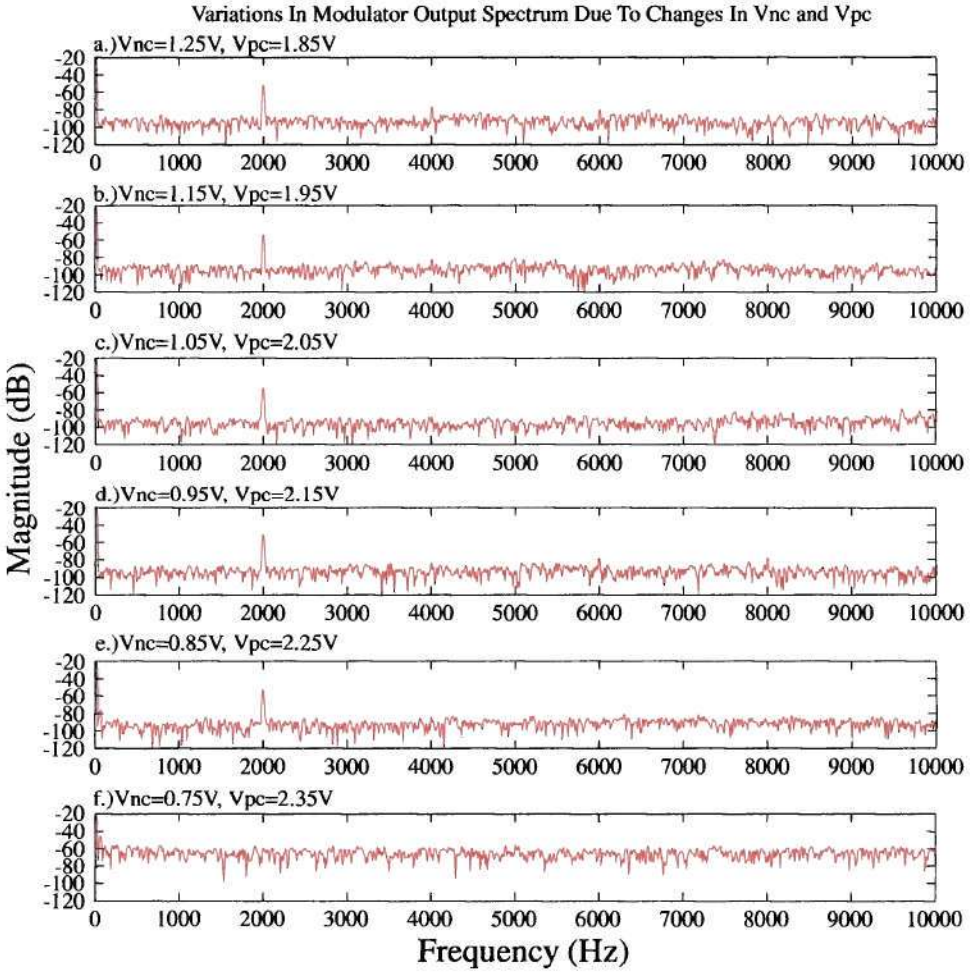

Figure 39: This figure shows the effect of changing the PFET and NFET cascode bias voltages on the OTA, VNC and VPC. As the cascode voltage is reduced/increased to the minimum cascode bias voltage the harmonic distortion decreases because a larger output signal swing is allowed. Once the cascode bias voltage goes past the minimum bias voltage the output transistors go out of saturation an the modulator stops working.

of the data recorded from the modulator output. The high and low values were quantized to be +1 and -1. If the signal value was around the half rail voltage it was determined to be 0.

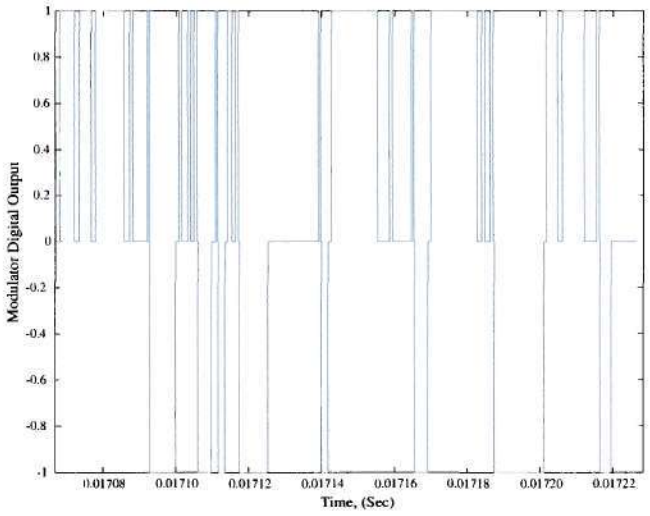

Figure 40: 1^{st} order modulator output when comparator is operated in the unclocked mode of operation. The output has been cleaned up and quantized to consist of three different levels, +1, 0, 1.

At first glance the data looks that it does consist of the derivative steps that were predicted in the unlatched comparator section, section 3.3. However, upon attempting to reconstruct the output into an analog signal no meaningful data was extracted. The reconstruction approach for the 1^{st} order modulator consisted of either adding, subtracting or doing nothing to the reconstruction signal for each time step. Initially the signal starts at 0, then for the next time step if the modulator output is +1 a voltage step is added to the output signal, if the modulator output is -1 a voltage step is subtracted form the output signal and if the modulator output is 0 then the reconstructed voltage remains constant for the time step. Other analysis techniques were performed on the modulator output data to see if any frequency content could be extracted but none of the other attempts proved useful.

There is a possible reason as to why the unclocked modulator output is corrupted. The hypothesis is that the output is buffered through a string of digital inverters which is causing

the corruption. The digital buffer works well for the latched modulator because the output is purely digital. However, for the unlatched case the comparator output being returned back to the current DACs is not the same as the signal coming out of the IC to be analyzed. The digital buffer is very unstable for mid-rail voltages therefore it will cause any internal comparator output to be either railed high or low and not be a true representation of the comparator output. This problem will need to be corrected for the next version of the modulator.

CHAPTER V

HIGH LEVEL MODELLING

5.1 Using SIMULINK For High Level Modelling

While the EPOT Δ-Σ modulator was being created, one issue that become obvious was that there needed to be an efficient way to take advantage of the ability to program the feedback coefficients. There are many equations that deal with performance of Δ-Σ modulators but most of these take a simplified discrete time approach to the solution, see the Δ-Σ modulator section in [5] for a complete listing of sampled time design equations. These equations provide coefficient values for the ideal discrete time system they are modelling but fail to account for the many different sources of noise and nonlinearities. There are many continuous-time discrepancies such as slewing and charge injection that need to be taken into account. One approach to finding optimal feedback coefficients would be to run SPICE simulations for every possible combination and determine from those results what the best coefficients values would be. But this is an impractical procedure when it takes one simulation almost 24Hrs to get enough data to extract adequate frequency results.

The solution that was decided upon was to use MATLAB and SIMULINK to create a high level model that could quickly determine the optimal values of feedback coefficients. This form of high level modelling has already been attempted in [2] to varying degrees of success. Using SIMULINK it was possible to create a high level model that efficiently recreated a Δ-Σ modulator that included all of the important sources of noise. Changes were made to the model presented in [2] because the slew rate modelling needed refinement and the model failed to include charge injection and. The main op-amp sources of error were included: non-infinite gain, limited bandwidth, and limited slew rate. Charge injection and KT/C noise were also included. Using this model it was possible to simulate thousands of coefficient possibilities in the amount of time it would take SPICE for just one simulation.

Since the proposed continuous-time Δ-Σ modulator will have both feed forward and

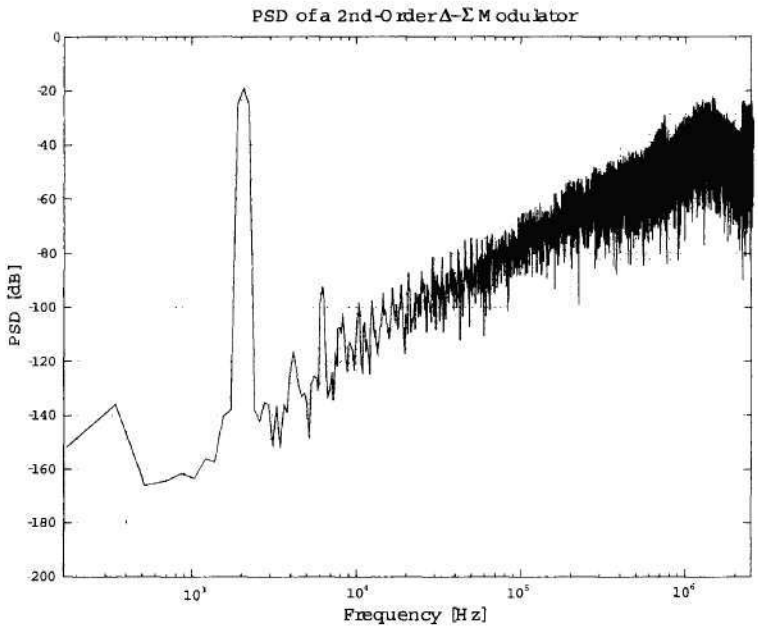

Figure 41: SIMULINK simulation results for 2^{nd} order modulator.

feedback variable coefficients it was a high priority to create a high level model to help find the optimal coefficient values for the modulator in a practical amount of time. It was possible to work off of the same basic structure as the EPOT modulator high level model, but some modifications were needed. Because the continuous-time modulator does not use switched-capacitor circuits, charge injection and slew rate will not be sources of noise. The main source of error to be modelled is the nonlinearity of the G_m-C integrator block. This takes the form of a hyperbolic tangent curve. The ability to model the *tanh* functions effect on the system will determine the reliability of the results obtained from simulations,

$$I^+ - I^- = I_{ref}\left[\tanh\left(\frac{\kappa C_{FG}(V^+ - V^-)}{2U_T C_T}\right)\right], \tag{12}$$

where C_{FG} and C_T are OTA model parameters for the floating gate input capacitance on the input differential transistor pair.

With the ability to run thousands of different coefficient combinations it becomes possible to construct contour plots showing the change in SNR with respect to different coefficient values. The plots help to show were plateaus are formed and where similar SNR is achieved

Table 6: 2^{nd} Order Optimal Coefficient Values

BiasName	Value
1st Integrator Bias	100nA
2nd Integrator Bias	1uA
1st Feedback DAC	40nA
2nd Feedback DAC	100nA

Table 7: 3^{rd} Order Optimal Coefficient Values

BiasName	Value
1st Integrator Bias	50nA
2nd Integrator Bias	200nA
3rd Integrator Bias	400nA
1st Feedback DAC	90nA
2nd Feedback DAC	300nA
3rd Feedback DAC	300nA

for multiple coefficient combinations. Figure 42 shows a series of contour plots for varying the feedback coefficients with fixed feed forward values. As the plots progress from Fig. 42(a) to Fig. 42(c) it can be seen how a plateau gradient is formed where the SNR is approximately constant for varying values of the feedback coefficients. Using the simulation data and analyzing the gradient plots allows for optimal coefficients to be chosen. The coefficients for the 2^{nd} and 3^{rd} order modulators are presented in Table 6 and Table 7.

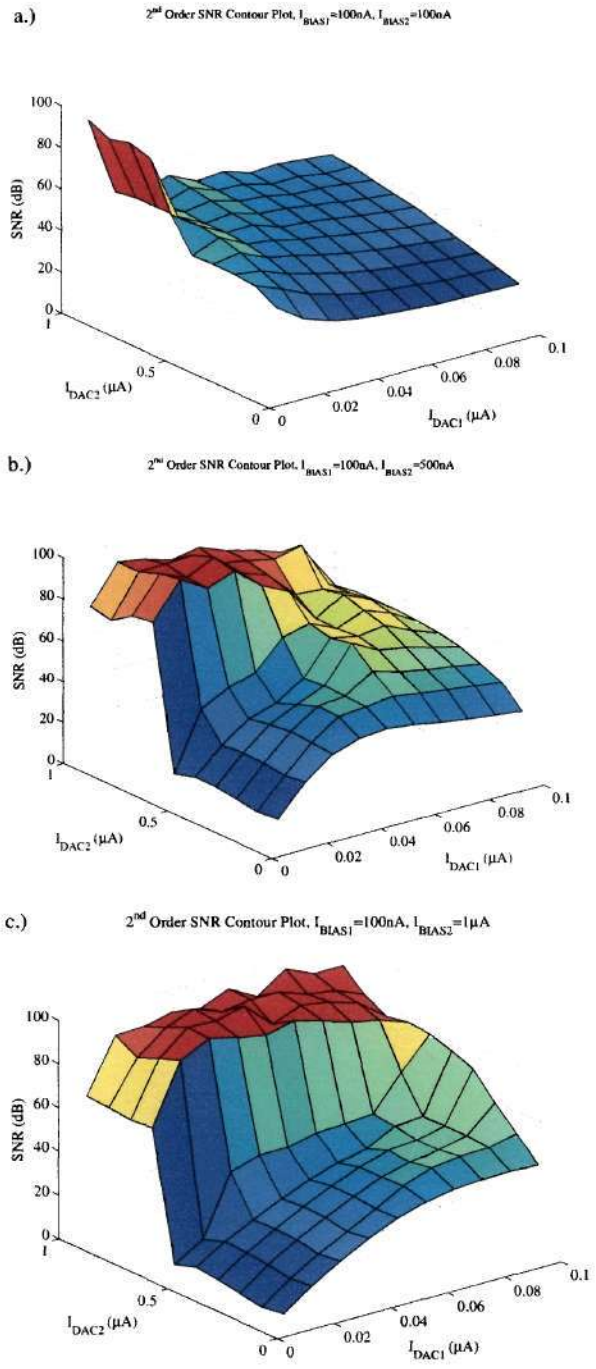

Figure 42: Contour plots showing the gradients obtained by varying the feedback coefficient values of a 2^{nd} order modulator. All three plots have varying feedback current DAC values. In plot (a) I_{BIAS1} and I_{BIAS2} are both equal to 100nA. In plot (b) I_{BIAS1} and I_{BIAS2} are equal to 100nA and 500nA respectively. For plot (c) I_{BIAS1} and I_{BIAS2} are equal to 100nA and 1μA

CHAPTER VI

CONCLUSION

A continuous-time Δ-Σ modulator was designed, fabricated and shown to work up to 4^{th} order. During the process an OTA with improved linearity and floating-gate CMFB was also designed, fabricated and tested. The experimental results showed the improvement obtained in linearity with a floating-gate differential pair. The floating-gate CMFB was also shown to work. The idea of using the modulator in an unclocked, asynchronous behavior was tested. It was found that due to the digital buffering of the modulator output the signal was distorted so much so that it was not possible to obtain any meaningful results. To aid in the programming of the modulator a high level SIMULINK model was constructed to allow for the ability to compare numerous different coefficient settings to determine optimal results. Overall this work proved the feasibility of a continuous-time floating-gate modulator and opened the door for future work to be performed. One possible extension of this work is to apply it to a continuous-time bandpass Δ-Σ modulator. With the programmability of the floating-gates the bandpass modulator's noise transfer function could be tuned to cover a wide range of frequencies. This would allow the modulator to change it's frequency band of operation depending on what frequency the desired signal was in.

The research presented in this thesis represents the first time a continuous-time Δ-Σ modulator has been designed with floating-gates controlling the feed-forward and feedback gain. The use of floating-gates makes this work very novel because it allows the feed-forward and feedback gain coefficients to be programmed allowing the noise transfer function to be modified. The 3^{rd} order experimental results show that just using discrete analysis to work out the modulator behavior is not correct. Z-transform analysis states that a 3^{rd} order Cascade-of-Integrator modulator is unstable [5]. But that is clearly not the case from the experimental data shown in the previous section. Another first for this research is the use of a unlatched comparator for the 1-bit quantization.

Three papers were submitted to ISCAS 2004 on the research presented in this thesis. They are as follows:

- "A Programmable Coefficient Continuous-Time A/D Δ-Σ Modulator" [16].
- "A 0.5um CMOS Programmable Discrete-Time Δ-Σ Modulator Using Floating-Gate Elements" [15].
- "Fully Differential Floating-Gate Programmable OTAs with Novel Common-Mode Feedback" [17].

6.1 Future Work

- Increase linearity of OTA
- Improve feedback current DAC
- Improve unlatched comparator structure and fix output buffering problem
- Fabricate new modulator using the above improvements
- Improve testing environment to aid in reducing noise

From the experimental data presented in this work it is clear that the linear range of the modulator still needs to be increased. Because of this the linearity on the differential pair will be increased. This will either be achieved by decreasing the size of the floating gate capacitor or by increasing the size of the input differential transistors. Both options will result in an improved linearity but it is yet to be seen which one is the optimal solution. A third option along the same line as the other two is to add an additional capacitor connected to ground at the floating gate node of the input differential pair. However, while this will again improve the linearity there will now be an additional parasitic capacitance at the input node that will only detract in performance.

More work is going to be done on the matching of currents and matching of switching effects of the current feedback 1-bit DAC. The addition of floating-gates and improved design techniques should aid in the matching of the currents. A literature survey of PLL

charge pump designs is being performed to see what can be gained by employing designs from that area. The purpose being that the charge pump that is connected to the output of a digital phase/frequency detector (PFD) of a PLL is very similar to the current DAC that is implemented in this research. The PLL charge pump switches on an off sourcing and sinking current sources to add or remove charge on an integrating capacitor whose voltage is then used to control the VCO of the system, this behavior is just like that of the 1-bit current DAC.

The comparator for the unlatched operation of the modulator needs to be improved upon to allow for a faster behavior. The comparator presented in this research was not optimized for the desired performance due to time constraints in getting the first IC fabricated. The output buffer stage used for the clocked modulator needs to be analyzed more carefully when the modulator is set to run in the unclocked state. The reason is that the buffered output, if it does come out in three different states would not be passed out properly from the digital buffer that is currently used. This is giving a distorted modulator output that is causing the output to be unanalyzable.

All of the above improvements will be implemented in a new Δ-Σ modulator. The second version of the modulator should be a step towards obtaining better experimental results. The IC presented in this work was more of a proof-of-concept IC and now that the concept has been proven the modulator design needs to be optimized and fabricated. Along those same lines it will also be necessary to redesign the test board and make attempts at improving the testing environment. The new test board will have less auxiliary components on the board and will be designed to have a clean reference and power signals.

6.2 Distribution of Work

The Δ-Σ modulator work using EPOTs discussed in Chapter I was done with Angelo Pereira. Angelo originally started the work and had fabricated one chip before I joined the research group. After joining, Angelo and I sent out a revised chip using the EPOT structures. A conference paper was submitted to ISCAS2004 detailing the revised modulator with new results.

The high level modelling of the Δ-Σ modulator using SIMULINK was also done in conjunction with Angelo Pereira. This work was started after I had joined the group and the work was split between the two of us. The beginning structure of this work was taken from [2].

The research work on the design of G_m-C integrators was done in partnership with Ravi Chawla. Both Ravi and myself were in need of a G_m-C block for our different application. Ravi used it in G_m-C based filters while I used it in the modulator. The research was a joint effort and test chips were sent out with the various G_m-C elements and common-mode feedback schemes so that characterization could take place. Testing of the G_m-C integrator was performed by Ravi, Guillermo Serrano, myself and Angelo. The results of the integrator with novel CMFB were submitted in a conference paper to ISCAS2004 [17].

All of the work on the research and design of the continuous-time Δ-Σ modulator has been done by myself with insightful comments and discussions being provided by my advisor Dr. Paul Hasler. The testing of the modulator was performed by Angelo and myself. Angelo was very helpful in the test board design and in writing the VHDL and C interface code.

APPENDIX A

PCB TEST STRUCTURE DESIGN

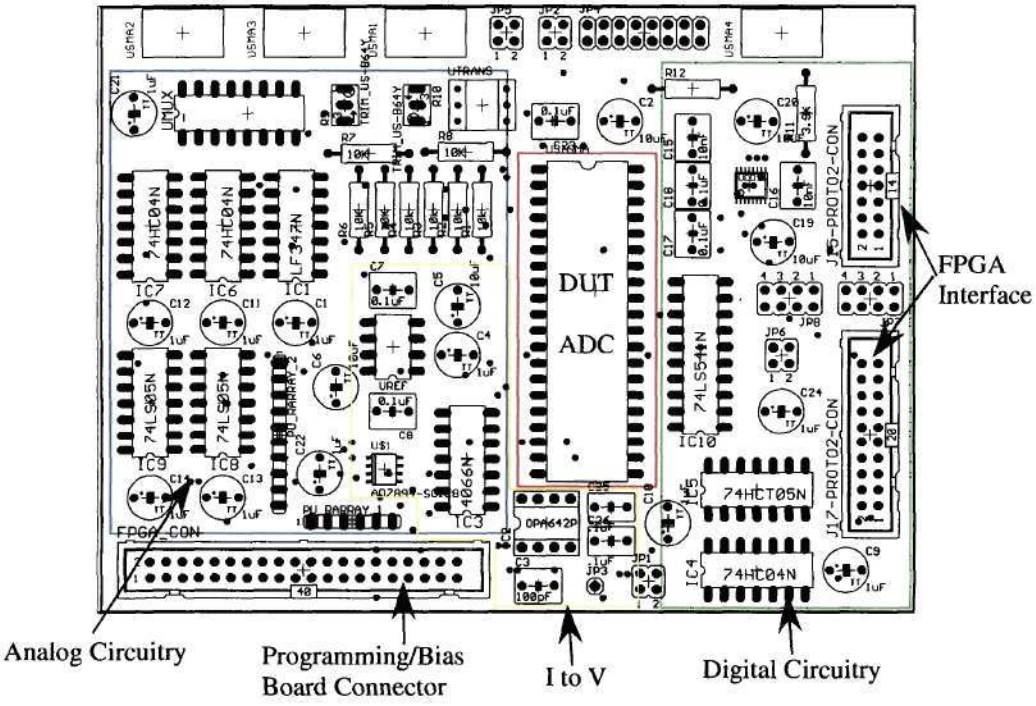

Figure 43: Test board designed for Δ-Σ modulator

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