Simultaneous Switching Noise Measurements

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Abstract

Simultaneous switching noise (SSN) has become a major bottleneck in high speed system design. For future systems, modeling of SSN can be complex due to the thousands of interconnects that need to be analyzed. This paper presents measurement and analysis of simultaneous switching I/O noise for a CMOS ASIC test chip packaged in a HyperBGA package and mounted on a printed wiring board (PWB). The measurements were done under several different variable conditions and the results were analyzed. The data measured will be used for model to hardware correlation.

Introduction

Current complementary metal oxide semiconductor (CMOS) microprocessors and application-specific integrated circuits (ASICs) have hundreds of inputs/outputs (I/Os) switching within one cycle time. When the noise generated by all the simultaneous switching circuits approaches the noise tolerance of a static CMOS circuit, the integrity of the output signal is degraded. Therefore proper prediction and accurate measurement of the level of simultaneous switching noise (SSN) in a packaged electronics system has become one of the most important issues in high speed systems. This paper discusses measurement results for a SSN experiment.

Test Vehicle Description

1) The CMOS ASIC test chip measured 10.9mm on a side and was designed by IBM using the CMOS6SF 0.18μm ASIC logic family circuit library. The controlled collapse chip connection (C4) flip-chip technology was used to attach the test chip to the HyperBGA package. The C4's are 101μm in diameter on a 225μm pitch.

2) The IBM HyperBGA package measured 32×32mm. This organic package had 4 power distribution layers. The cross section of the power distribution planes in the HyperBGA package is shown in Table 1 and the layout of HyperBGA package is shown in Fig. 1.

TSR	Ground
V1	Solid plane 2.5V
GND	Ground
V2	Split plane 3.3V+1.5V

Table 1. Cross section of the power distribution planes in the HyperBGA package.

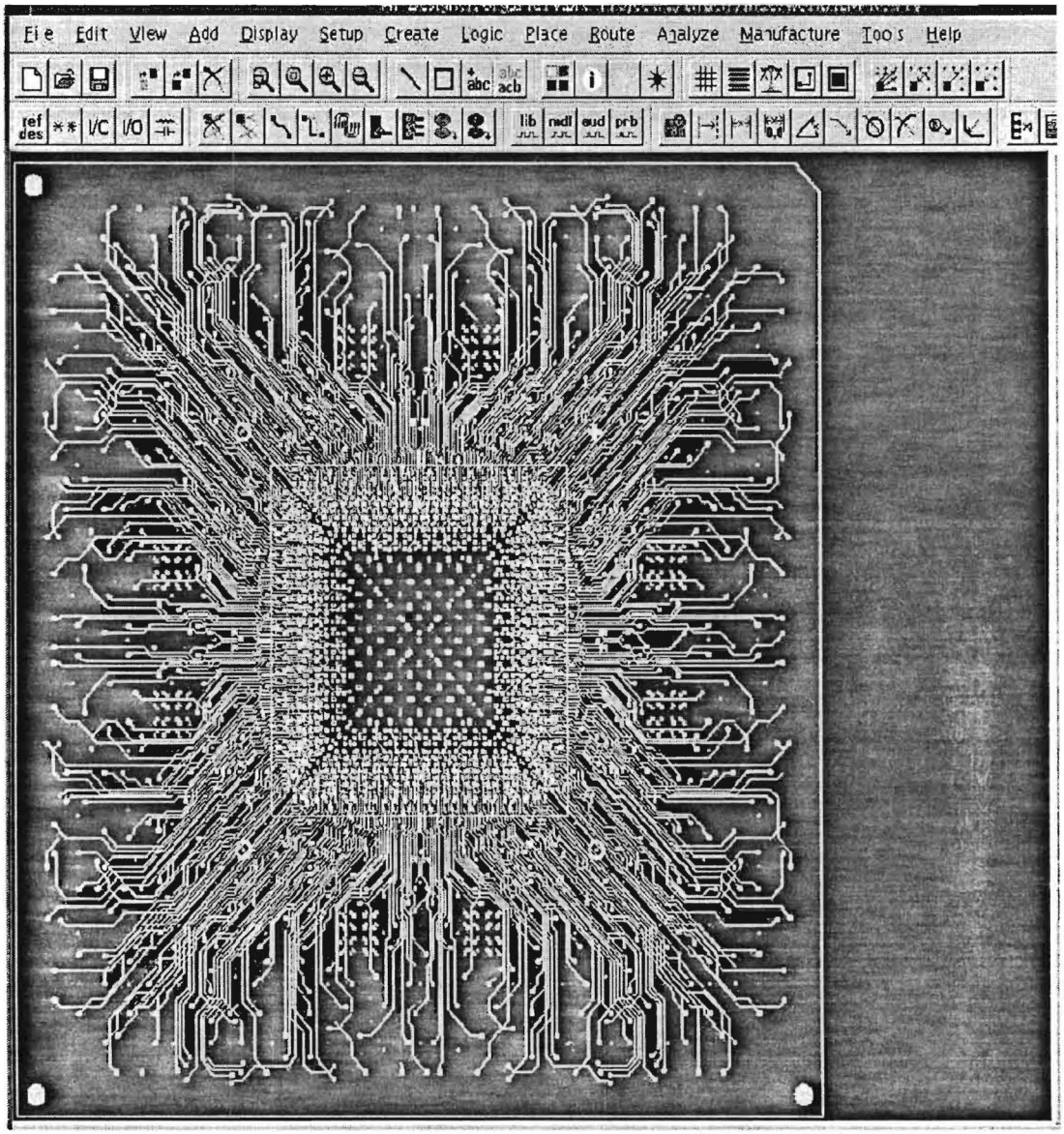

Fig. 1. Layout of HyperBGA package

The V1 plane provides 2.5V to the core logic and I/O circuits. The V2 plane is split into four quadrants along two diagonal lines. Three of them, left, top, right, are connected to 3.3V. The bottom plane is connected to 1.5V. All the quadrants of the V2 plane supply power to the I/O circuits. The structure of the test vehicle is shown in Fig. 2.

3) The Saranac PWB measured 45×30cm, which had two GND planes, two 2.5V planes, two 1.5V planes, two 3.3V planes and eight signal layers. The dielectric used was FR-4. The cross section of the power distribution planes in the Saranac PWB is shown in Table 2 and the layout of the Saranac PWB is shown in Fig. 3 where S3, S5, S7, S9, S10, S12, S14, and S16 are signal layers.

V2GND	Full layer Ground Plane
V4PLANE	Full layer plane V1 = 2.5V
V6PLANE	Full layer plane V2 = 1.5V
V8PLANE	Full layer plane V3 = 3.3V
V11PLANE	Full layer plane V4 = 2.5V
V13PLANE	Full layer plane V5 = 1.5V
V15PLANE	Full layer plane V6 = 3.3V
V17PLANE	Full layer Ground Plane

Table 2. Cross section of the power distribution planes in Saranac board.

The first four planes, V2GND to V8PLANE, provide the power supply to the modules located on the right side. The next four planes, V11PLANE to V17PLANE, provide the power supply to the modules located on the left side. There are vias connected between the two ground planes, V2GND and V17PLANE. But there are no connections between corresponding voltage planes. For instance, there is no connection between V4PLANE and V11PLANE. The board under test had only one module mounted on the right side so that only top four layers were powered by DC voltages, 1.5V, 2.5V and 3.3V separately. The different voltages were used to provide power to different parts of the chip under test. The core logic of the ASIC was connected between 2.5V and ground. There were three different I/O types on the chip, which were powered by 1.5V, 2.5V and 3.3V. There were 40 decoupling capacitors mounted on the board with values: 20μF×0, 0.47μF×5 and 0.01μF×5. The parasitic resistance, R_E, and parasitic inductance, L_E, for each capacitor are shown in Table 3.

C	R_E	L_E
20μF	1 Ω	10 nH
0.47μF	0.1 Ω	1 nH
0.01μF	0.1 Ω	1 nH

Table 3. Parasitic resistance and inductance values for each capacitor.

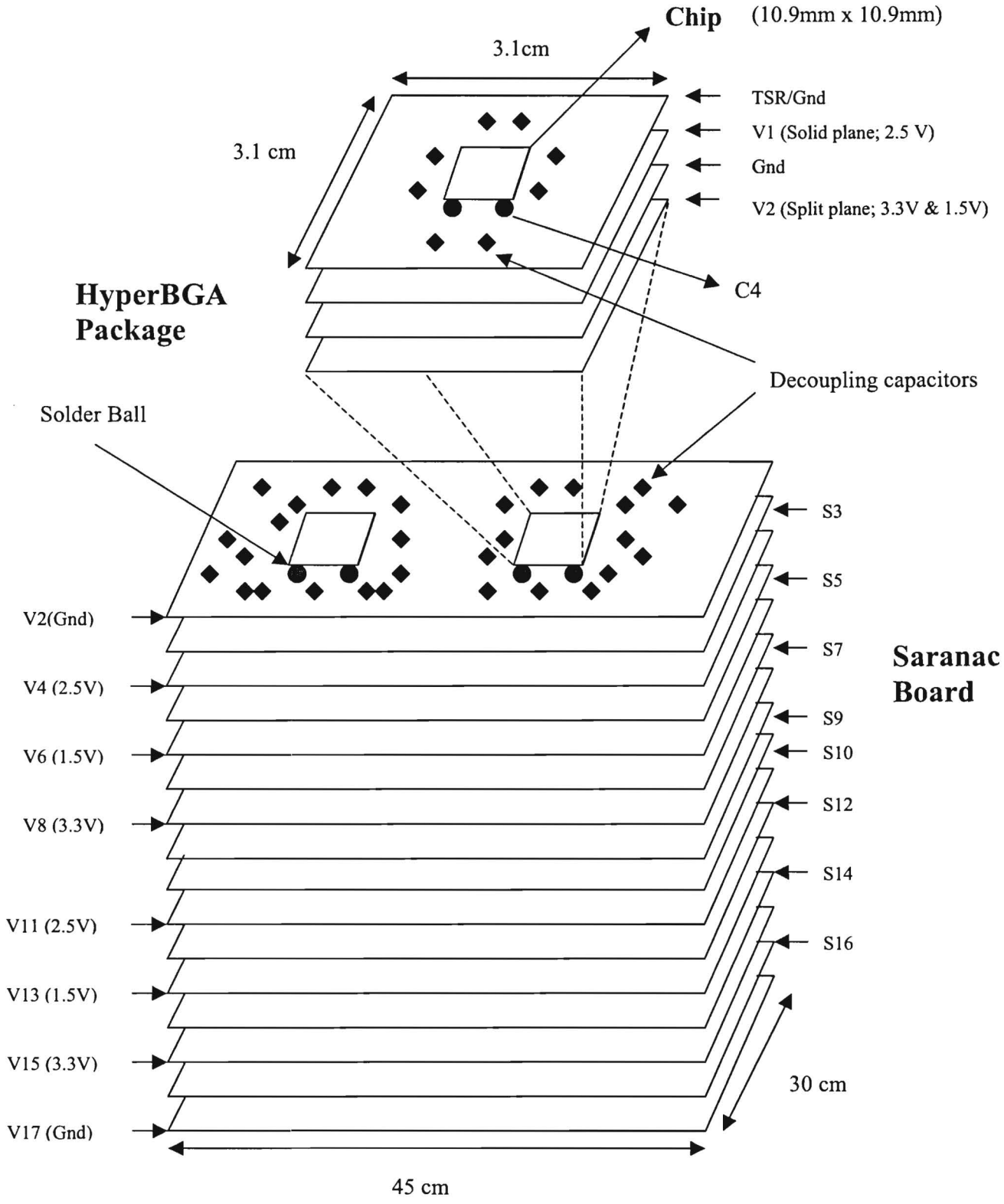

Fig. 2. Structure of Test Vehicle.

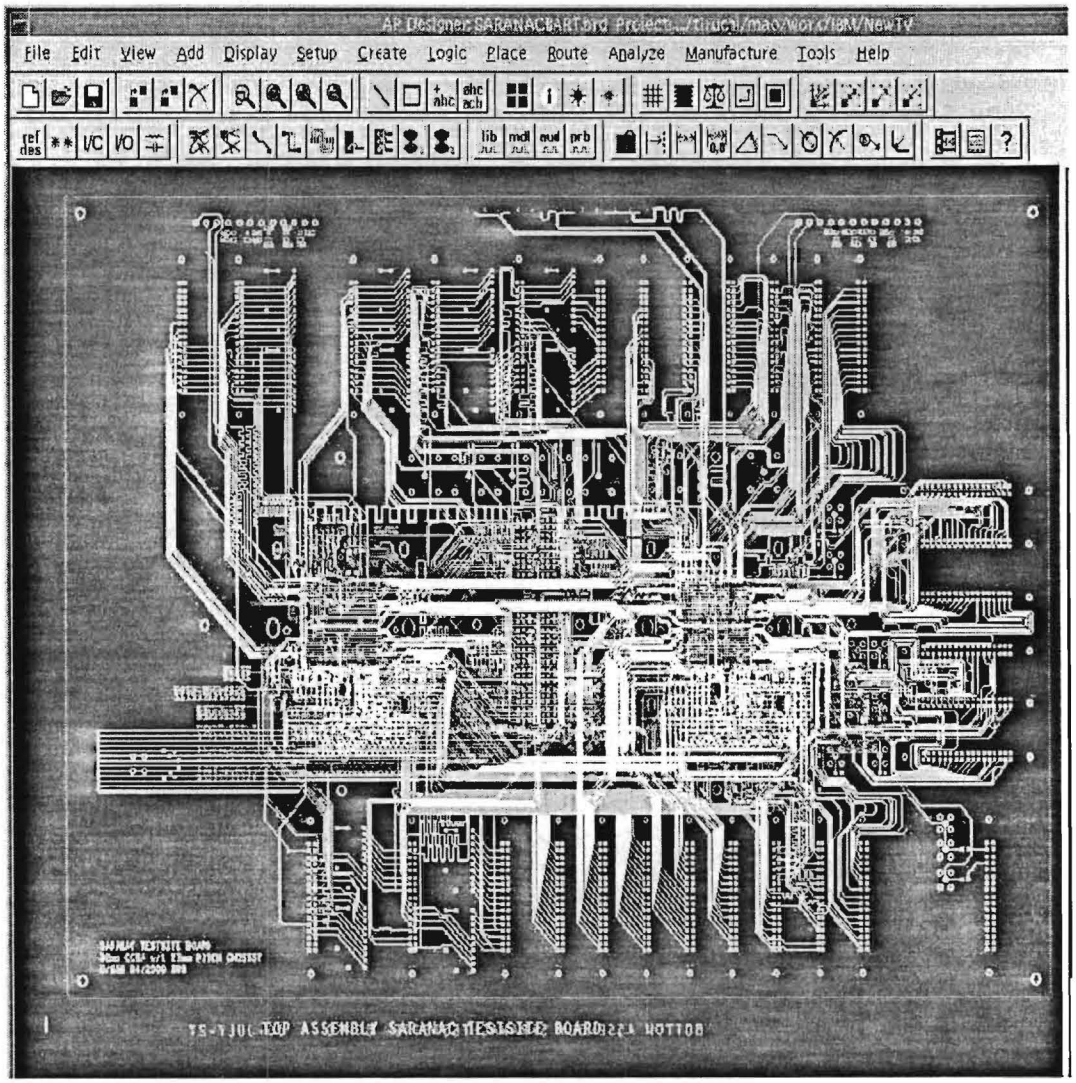

Fig. 3. Layout of Saranac PWB.

Measurement

The system was powered using three different voltages namely, 1.5V, 2.5V and 3.3V. The ASIC accepts both the clock and input signals and controls the I/O drivers to switch individually. The adjustable pulse, which is used as Phase-2 clock of the ASIC, was generated by HP8130A pulse generator. The control signal from the HP82000 tester was used by the logic circuits inside the ASIC. The logic circuits in the ASIC enable the I/O drivers to either always stay low/high or switch according to the input clock. The command input through a parameter file where the switching action of every I/O driver is specified was executed by the HP82000 tester. The signal was measured using a Tecktronix probe on the load board and the waveform was displayed on the screen of a Tek11801 Tecktronix Digital Sampling Oscilloscope. The interface between oscilloscope and HP workstation makes it easy to save the time domain waveform directly to a specified directory with a specified file name.

The measurement steps were as follows:
1) Clock signal was tuned by varying the period and rise time.
2) The appropriate parameter files were executed to control the logic signal of HP82000 Tester based on the I/O drivers that needed to be switched or kept quiet.
3) The probe was moved to the place where the noise was to be measured. The time scale and voltage scale of the oscilloscope was tuned to a suitable level.
4) The waveform was saved to a file.
5) The above steps were repeated by changing the conditions, such as using different probe and using different decoupling capacitors.

The first measurement done was called WQL standing for walking quiet line. The probe, which was attached onto a moving deck, touched the quiet I/O site. Then, the deck and probe were moved along the 3.3V I/O driver array to measure WQL noise at different I/O locations. The measurement for WQL is automated which took 4~5 hours to complete. The noise saturation measurement was also done. The main idea of this measurement was to keep one of the 3.3V I/O drivers quiet and switch the I/O drivers in the vicinity. The number of switching drivers was started from 1 and stopped until all the 3.3V I/O drivers switched simultaneously. The data was saved every time the number of I/O driver increased. The object for this measurement was to see the saturation of noise as the number of switching circuit increases. Next, the measurement of simultaneous switching I/O noise was done. The idea was that when all 3.3V I/O drivers switch, current is drawn from V2 plane of the package and V8 plane of the Saranac board. The transmission line on the S3 plane that is sandwiched between V2Gnd and V4Plane is driven by the 3.3V I/O drivers. In this way, the voltage disturbance is induced between V2Gnd and V4Plane.

The several variables considered for I/O switching noise measurements were as follows.

a) Different clock/switching speed with different rise time.
There were three different clock/switching speeds such as 25MHz, 50MHz and 100MHz with two different rise time, 0.7ns and 1.4ns.

b) Different I/O drivers switching.

There were two cases: One was to switch all 3.3V I/O and keep other I/Os quiet. The other was to switch all 2.5V I/O and keep other I/Os quiet.

c) Different decoupling capacitors setup.

There were 40 capacitors around the module. Four different decoupling capacitors setups were used namely,

I. All the capacitors included on the board.
II. All the capacitors included on the board except 10 capacitors valued 20μF.
III. All the capacitors included on the board except 10 capacitors valued 20μF and 15 capacitors valued 0.47μF.
IV. All the capacitors removed from the board.

d) Different measurement sites.

The four capacitor sites were chosen. The two capacitor sites among them are close to the module and the other two capacitor sites were close to the edge. Based on APD design files, there were seven signal lines related to 3.3V I/O drivers in a S3 signal layer underneath C31 capacitor site and there were six signal lines related to 2.5V I/O drivers in a S3 signal layer underneath C28 capacitor site while there were no signal lines related to 3.3V I/O and 2.5V I/O drivers in a S3 signal layer underneath C16 and C11 capacitor sites. The measurement sites were as follows.

I. C31 (20μF) that is connected between 2.5V and ground. It is close to the module.
II. C28 (20μF) that is connected between 3.3V and ground. It is close to the module.
III. C16 (0.47μF) that is connected between 2.5V and ground. It is close to the edge and near DC supply.
IV. C11 (0.47μF) that is connected between 3.3V and ground. It is close to the edge and near DC supply.

e) Different probes.

Two types of probes were used namely, SD-14 and P6248. The SD-14 is a high impedance active probe with 3.0GHz bandwidth and P6248 is a differential probe with 1.7GHz bandwidth.

Next the file name was designed to represent all the variable above, so that the file name was self-explainable. Files in the SD14 directory have an additional _SD14_ label on the front end of the filename. Files in the P6248 directory do not have a _P6248_ label on the front end of the filename, but they were taken with the P6248 probe. The following example is very useful for understanding file names;

(Example file name) wql_C31_40_3.3_100_.7ns_.xplot

1) wql_: Since a program similar to WQL skew program was used, so this tag was automatically added.
2) C31_: It means that the probe is placed where C31 is located. The other choices were C28, C16, C11, J21.5 and J22.17. The J21.5 and J22.17 are selected for measuring active I/O driver outputs.

3) 40_: It means 40 capacitors were removed from the load board. The other choices include 25 which stands for all 20μF and 0.47μF capacitors being removed, 10 which stands for all 20μF capacitors being removed and 0 which stands for no capacitors being removed.
4) 3.3_: It means all the 3.3V I/O drivers were switching and the others kept quiet. The other choice was 2.5 that stands for all 2.5V I/O drivers were switching and the others kept quiet.
5) 100_: It means phase 2-clock speed is equal to 100MHz. The other choices were 50_, 25_ and 1M that stand for 50MHz, 25MHz and 1MHz respectively.
6) .7ns_: It means 0.7ns rise time on Phase 2 clock. The other choice was 1.4ns for the rise time.
7) .xplot : It means file extension of the Unix application "Xplot" which is a screen plot software used for post-processing.

Based on this information, I/O simultaneous switching noise measurements were performed during June 20 and June 21, 2001. On June 20, P6248 differential probe was used to do all the measurements. On June 21, SD14 probe was used to do all the measurements. All the data were ftped to the IBM drop box. The waveform in Fig. 4 was named wql_SD14_C28_40_3.3_50_.7ns_.xplot which has the meaning that SD14 probe is used at C28 site and all the 40 capacitors were removed and all 3.3V I/O drivers were switching and the clock was running at 50MHz with rise time 0.7ns. The noise voltage was measured between 3.3V and GND since C28 capacitor was connected between 3.3V and GND. The x-axis is time and the y-axis is voltage in this plot.

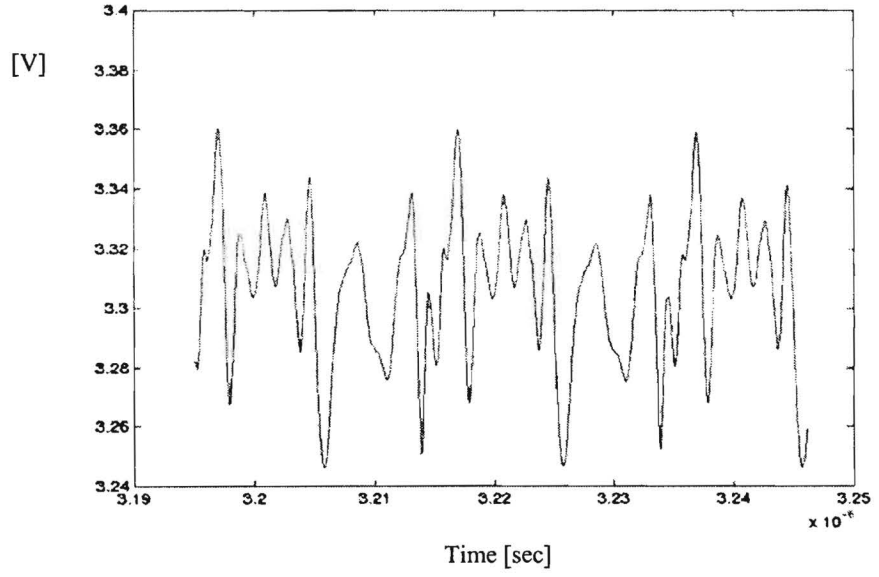

Fig. 4. Simultaneous Switching Noise (SSN) example.

Results and Discussion

First, for the C31 and C28 sites that were close to the module and under which there were some signal lines related to I/O drivers in a S3 signal layer, four SSN voltages are plotted together for comparison with the waveform from I/O driver output in Fig.5. In this figure, all the 3.3V I/O drivers were switching and the others kept quiet with 50MHz phase 2-clock speed whose rise time is 0.7nsec at C31 site. The noise voltage was measured between 2.5V and GND since C31 capacitor was connected between 2.5V and GND. The 4 files for this figure are wql_C31_0_3.3_50_.7ns.xplot, wql_C31_10_3.3_50_.7ns.xplot, wql_C31_25_3.3_50_.7ns.xplot, and wql_C31_40_3.3_50_.7ns.xplot. It should be mentioned that the noise amplitude must be multiplied by 10 in this measurement due to P6248 measurement setup. Hence, the maximum noise voltage swing was around 55mV while the minimum noise voltage swing with all capacitors was around 14mV in this case. The frequency of noise was 50MHz. It is clear that SSN becomes larger as the number of removed capacitors is increased in Fig. 5. The same conclusion is also true for Fig. 6 in which 3 SSN voltages are plotted together for comparison. In this figure, all the 2.5V I/O drivers were switching and the others kept quiet with 50MHz phase 2-clock speed whose rise time is 0.7nsec at C28 site. The noise voltage was measured between 3.3V and GND since C28 capacitor was connected between 3.3V and GND. The 3 files for this figure are wql_C28_0_2.5_50_.7ns.xplot, wql_C28_10_2.5_50_.7ns.xplot, and wql_C28_25_2.5_50_.7ns.xplot. In this case, the maximum noise voltage swing was around 40mV while the minimum noise voltage swing with all capacitors was around 8mV. The frequency of noise was also 50MHz.

Second, for C16 and C11 sites that were close to the edge of Saranac board and under which there were no signal lines related to I/O drivers in a S3 signal layer, four SSN voltages are plotted together for comparison with the waveform from I/O driver output in Fig. 7. In this figure, all the 3.3V I/O drivers were switching and the others kept quiet with 50MHz phase 2-clock speed whose rise time is 0.7nsec at C16 site. The noise voltage was measured between 2.5V and GND since C16 capacitor was connected between 2.5V and GND. The 4 files for this figure are wql_SD14_C16_0_3.3_50_.7ns.xplot, wql_SD14_C16_10_3.3_50_.7ns.xplot, wql_SD14_C16_25_3.3_50_.7ns.xplot, and wql_SD14_C16_40_3.3_50_.7ns.xplot. In this case, the maximum noise voltage swing was around 56mV while the minimum noise voltage swing with all capacitors was around 10mV. The frequency of noise was 50MHz. Like C31 and C28 cases, SSN becomes smaller as the number of removed capacitors is decreased. The same conclusion is also valid for Fig. 8 in which four SSN voltages are plotted together for comparison. In this figure, all the 2.5V I/O drivers were switching and the others kept quiet with 50MHz phase 2-clock speed whose rise time is 0.7nsec at C11 site. The noise voltage was measured between 3.3V and GND since C11 capacitor was connected between 3.3V and GND. The 4 files for this figure are wql_SD14_C11_0_2.5_50_.7ns.xplot, wql_SD14_C11_10_2.5_50_.7ns.xplot, wql_SD14_C11_25_2.5_50_.7ns.xplot, and wql_SD14_C11_40_2.5_50_.7ns.xplot. In this case, the maximum noise voltage swing was around 36mV while the minimum noise voltage swing with all capacitors was around 8mV. The frequency of noise was also 50MHz. It is important to note that all these measurements were on the board. The noise voltages in the ASIC are typically larger than the measurements on the board.

Summary

In summary, SSN voltage becomes larger as the number of removed capacitors is increased regardless of the capacitor site under which there are signal lines related to I/O drivers in a S3 signal layer or not. The maximum noise voltage swing ranged between 36mV and 56mV and the minimum noise voltage swing with all capacitors included ranged between 8mV and 14mV for these cases. Hence, the importance of the role of decoupling capacitors for suppressing SSN can be proved through these SSN measurements. These noise measurements will be used to validate the modeling techniques being developed with support by the Semiconductor Research Corporation under contract number 99-NJ-735.

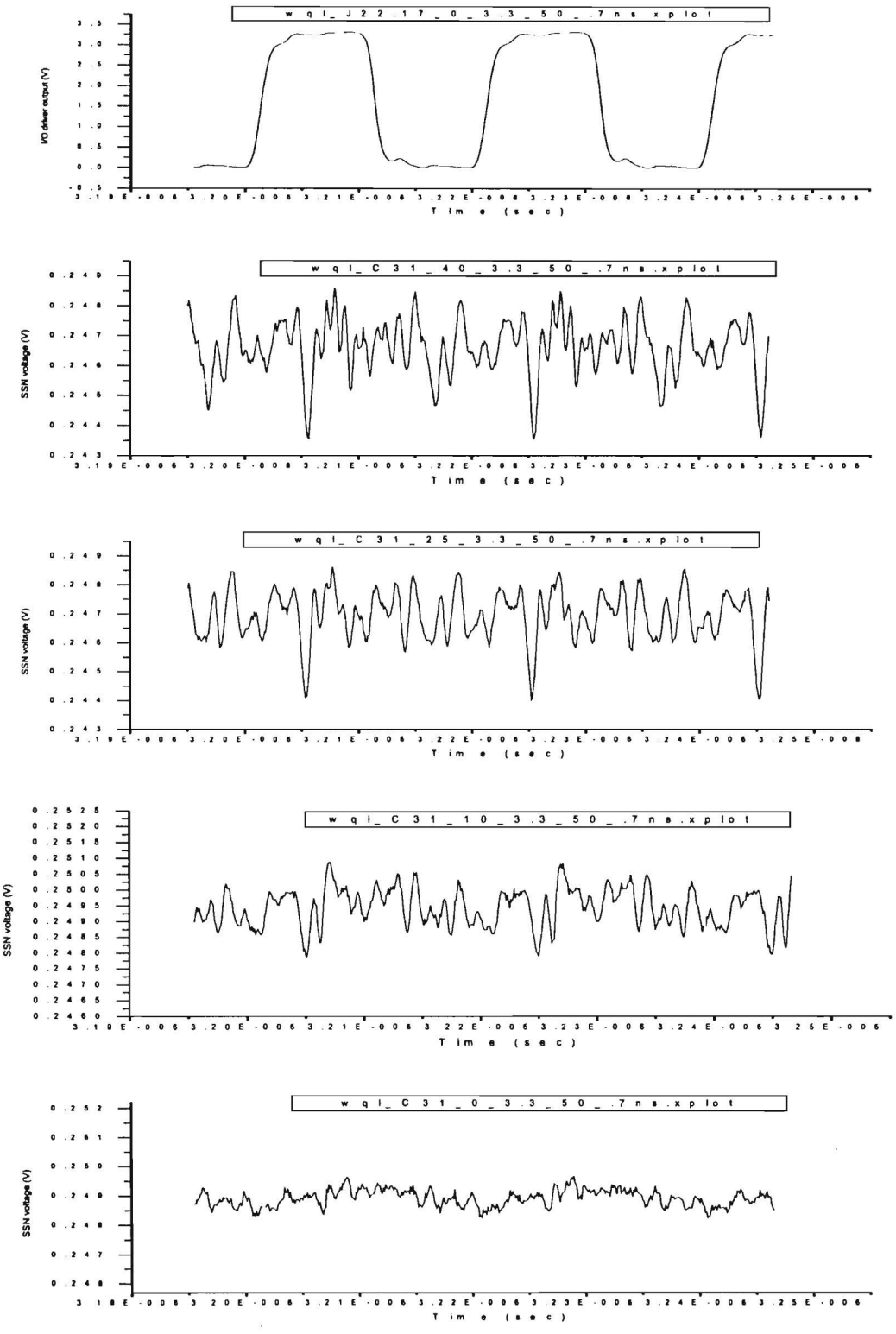

Fig. 5. Simultaneous Switching Noise voltages at C31 capacitor site when all the 3.3V I/O drivers are switching and others kept quiet with 50MHz phase 2-clock speed whose rise time is 0.7nsec.

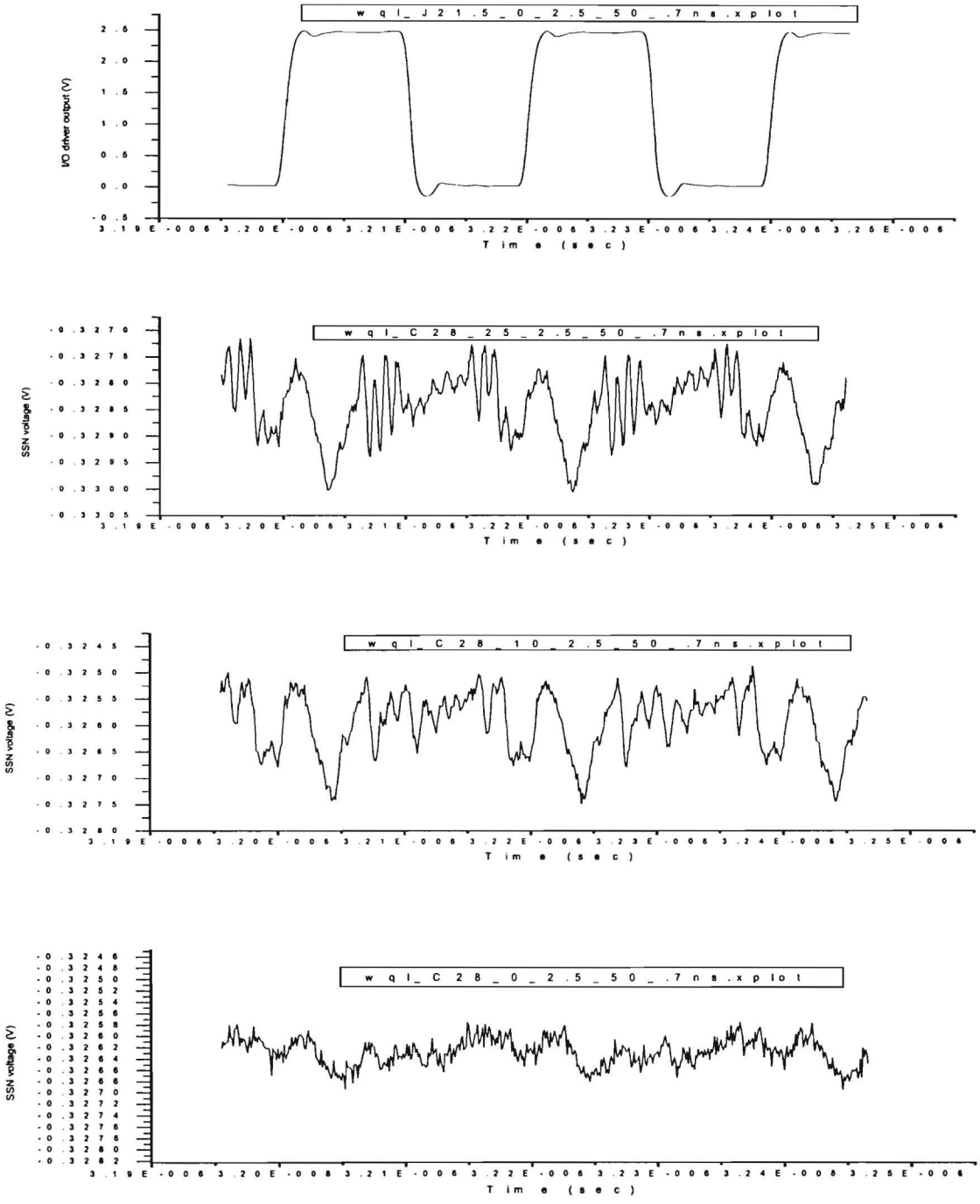

Fig. 6. Simultaneous Switching Noise voltages at C28 capacitor site when all the 2.5V I/O drivers are switching and others kept quiet with 50MHz phase 2-clock speed whose rise time is 0.7nsec.

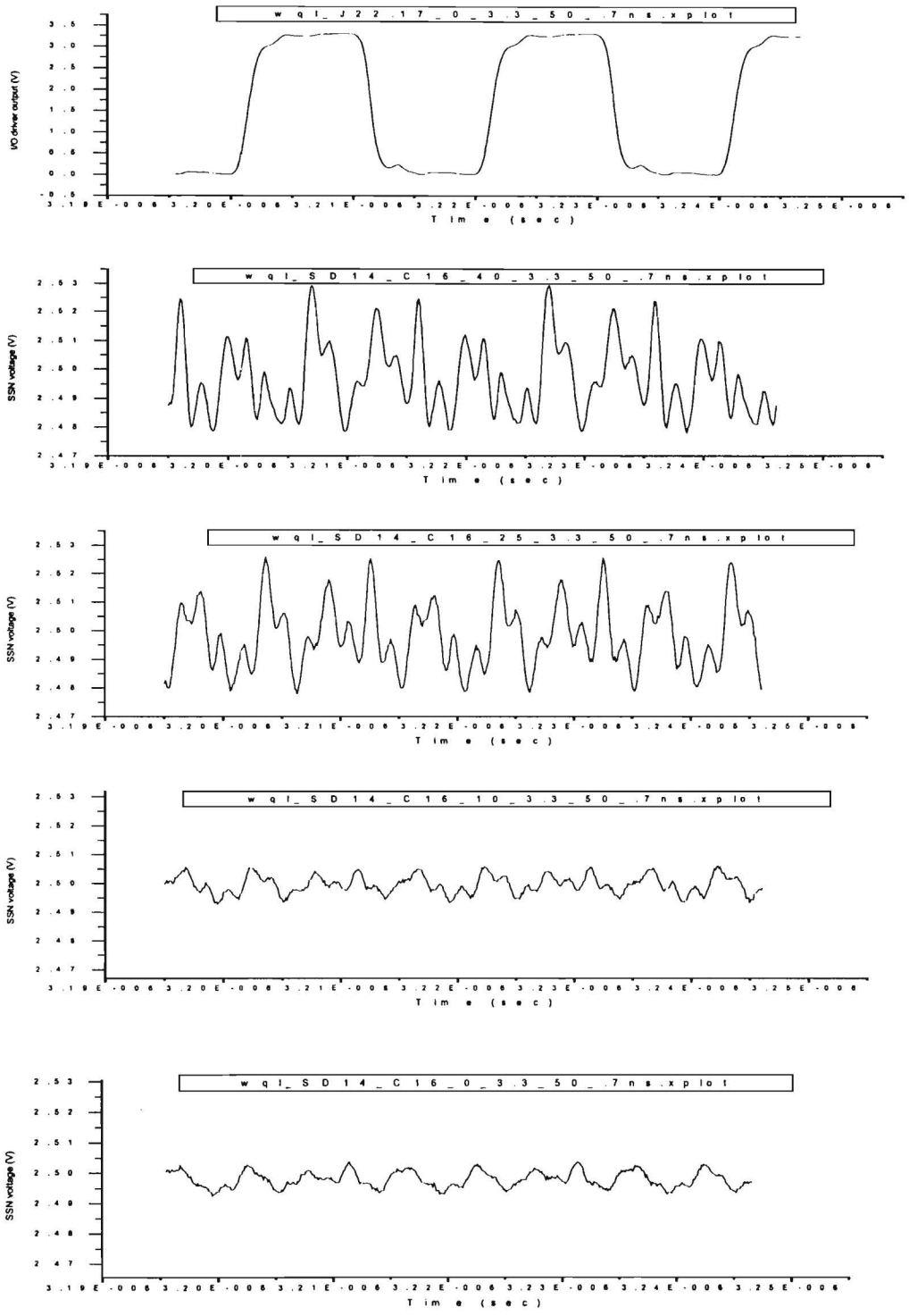

Fig. 7. Simultaneous Switching Noise voltages at C16 capacitor site when all the 3.3V I/O drivers are switching and others kept quiet with 50MHz phase 2-clock speed whose rise time is 0.7nsec.

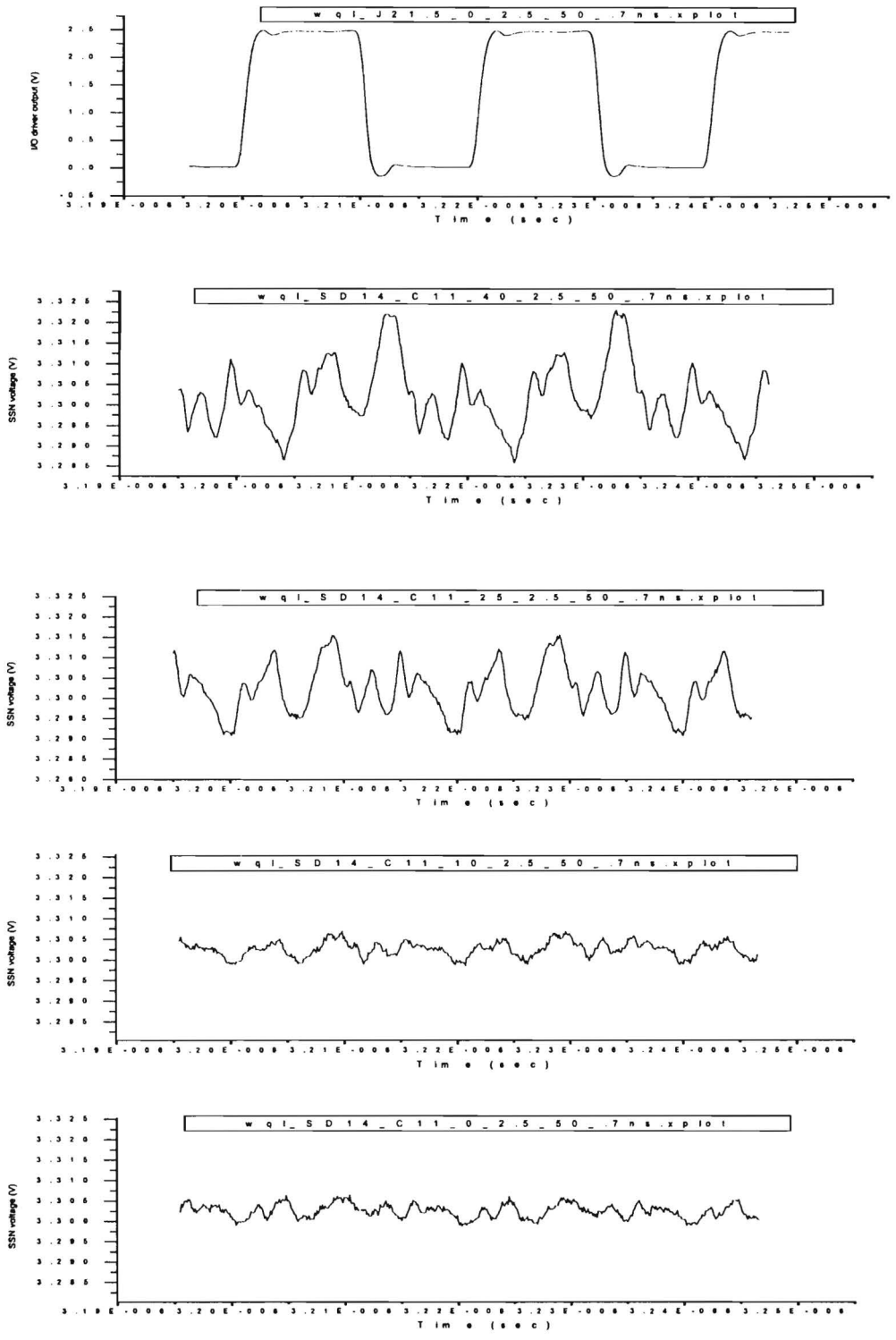

Fig. 8. Simultaneous Switching Noise voltages at C11 capacitor site when all the 2.5V I/O drivers are switching and others kept quiet with 50MHz phase 2-clock speed whose rise time is 0.7nsec.

Modeling of Field Penetration Through Planes in Multi-layered Packages

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Abstract-- This paper describes a method for analyzing the field penetrating through planes in package power distribution networks. This field can cause excessive noise in the system at resonant frequencies of the package. The effect has been quantified both in the time and frequency domain and compared with measurements. General guidelines have been suggested to suppress this noise by varying the material and physical parameters of the planes.

Index Terms—Field Penetration, simultaneous switching noise, power distribution noise

I. Introduction

As the clock frequency of high performance microprocessors and ASICs increase into the gigahertz region with high demand for power, the power distribution network can play a critical role in the design of the system. The power distribution network includes the chip, package and board where each level in the system hierarchy contributes to parts of the system response. A commonly used power distribution network in high

performance packages are multilayered power/ground planes, such as in printed wiring boards, multi-chip modules and single-chip modules. A major concern in the design of such modules is power supply noise which appears as a voltage fluctuation on the power distribution network when groups of circuits switch simultaneously. The current transients caused by the switching circuits excite cavity modes in the power distribution network causing power supply noise, a detailed discussion of which is available in [1].

It is clear from [1] that modeling power planes using equivalent lumped inductors, or inductive networks can give erroneous results for computing power supply noise, since the model may only account for the effect of slower current transients. However, for fast current transients, the power distribution network should be treated as a dynamic electromagnetic system in which waves can propagate between the power/ground planes. Various methods have been adopted to model the power/ground pairs by researchers in the packaging community, such as the Finite Difference Time Domain (FDTD) [5], two dimensional discrete transmission line model [6] and partial-element equivalent circuit (PEEC) [7]. Cavity mode solution for modeling the power/ground pair as a planar microwave circuit has also been studied in [1], [8], [9]. This method is based on a modal solution where the cavity formed by the power and ground planes is analyzed using a double infinite series consisting of cavity modes. Details on truncating the series that retains the passivity of the circuit are discussed in [1]. In [1], the equivalent circuit consisting of resonator sub-circuits is achieved by linearizing the solution to obtain frequency-independent inductor, capacitor and resistor elements. Various parameters in the model have been optimized in [8], [9] to analyze the frequency response of the plane pair to minimize impedance.

In all the methods that have been applied to analyze multi-layered power distribution networks containing planes, the plane-pairs have always been assumed to be isolated from each other [1], [5], [6], [7]. For example, in [1] the effect of conductor loss is included in the solution by changing the wave number k to a complex number. For a single plane pair, the skin effect is then assumed to be dominant and the solution is extended to multi-layered structures by assuming zero coupling between the plane layers. However, in the steady state, when the planes resonate, substantial coupling between the plane layers can occur through the magnetic fields penetrating the solid conductor where the level of penetration depends on the conductor thickness and conductivity of the planes. With the increase in clock frequency for present and future microprocessors, the package resonance frequency can overlap with the clock frequency causing coupling between the layers. This effect is a steady state effect which can cause a problem when the microprocessor performs an operation continuously over many clock cycles. The modeling and analysis of the field penetrating through power/ground planes is the subject of this paper. A modeling method has been discussed in this paper which is an extension to [1] and [11] where a perturbational solution has been used to capture the field penetration effect. The results have been compared with measurements and used to analyze its effect on a switching microprocessor.

The organization of this paper is as follows: In Section II, the modeling of voltage coupling between neighboring plane pairs is described and the method is extended to multiple layers. In Section III, the modeling method has been applied to a test structure and compared with measurements. In Section IV, the effect of field penetration for a switching microprocessor has been discussed using frequency and time domain

simulation. In Section V, two important parameters, namely, the metal thickness and metal conductivity of the planes are optimized to suppress the field penetration effect. Finally, Section VI describes the conclusion.

II Modeling of Field Penetration through Planes

In [1] and [8], two planes of dimension '$a \times b$' separated by a distance T as shown in Fig.1 have been analyzed as a cavity resonator. In Fig.1 the parameter T is the thickness of the dielectric. The figure also shows two ports, namely, port 'i' and port 'j'. Each port consists of two regions, one on the top plane and the other on the bottom plane. Each region represents a surface, with the two surfaces separated by the dielectric thickness T. The area of these surfaces at the port location is small and can be viewed as pad location where measurement can be made. Using the cavity modes, the impedance between ports 'i' and 'j' can be represented in the form:

$$Z_{ij} = j\varpi\mu T \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{(k_{mn}^2 - k^2)ab} f(x_i, y_i) f(x_j, y_j) \qquad (1)$$

where

$$f(x_i, y_i) = \cos\frac{2m\pi x_i}{2a} \sin c\frac{m\pi t_{xi}}{2a} \cos\frac{2n\pi y_i}{2b} \sin c\frac{n\pi t_{yi}}{2b}$$

In Eq. (1) (x_i, y_i) and (x_j, y_j) are the coordinates of the port locations, (t_{xi}, t_{yi}) and (t_{xj}, t_{yj}) are dimensions of the ports, $k = k' - jk''$ with $k'' = \varpi\sqrt{\mu\varepsilon}(\frac{\tan\delta}{2} + \frac{r}{2T})$ which accounts for the conductor and dielectric losses, $k_{mn}^2 = (\frac{m\pi}{2})^2 + (\frac{n\pi}{2})^2$ where m,n are propagating modes in the cavity, μ, ε are the permeability and permittivity of the

medium, respectivly, $\tan\delta$ is the loss tangent of the dielectric material, r is equal to $\sqrt{2/\varpi\mu\sigma}$ in which σ is the conductivity of the metallization, ϖ is the angular frequency and Z_{ij} is the impedance between the i^{th} and j^{th} ports.

The above equation has been derived directly by solving Maxwell's equations and assuming magnetic wall at the edges. This analytical solution captures the propagation and reflection of radial waves between the power planes [1]. Efficient methods for reducing the model complexity and for stacking planes have also been described in [1], [2]. In [3], this method has been applied to develop SPICE models for simulating the noise generated by output drivers switching simultaneously.

The modeling methods in [1], [2], [3] are based on the assumption that skin effect is dominant and hence the field cannot penetrate the solid planes. The plane pairs are therefore assumed to be completely isolated from each other since the skin depth is a small fraction of the metal thickness at high frequencies as shown in Fig.2. Though this assumption is valid for thick planes with high conductivity metallization, thin planes with low conductivity metallization are sometimes used to supply power to the chip. When this happens, magnetic fields can penetrate through solid conductors. Since a plane pair acts as a cavity resonator with high quality factor (low loss), a small amount of energy leaking into the cavity can take a long time to decay. Hence, over time, a switching microprocessor can couple a significant amount of energy into the layers above. The maximum coupling of energy occurs at resonance, as will be shown later in the paper.

In this section, Eq. (1) is modified to enable the magnetic field to penetrate the solid conductor. The solution procedure starts with the computation of the electrical field

in cavity I composed of plane V1 and GND1 as shown in Fig. 2. The electric field can be described in cavity I as [4]

$$E_{cav1,z} = \frac{j\varpi\mu J_s}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{\varepsilon_m^2\varepsilon_n^2}{k_{mn}^2 - k^2}\cos\frac{m\pi x_i}{a}\cos\frac{n\pi y_i}{b}\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b} \tag{2a}$$

$$E_{cav1,x} = E_{cav1,y} = 0 \tag{2b}$$

where only a vertical z-directional electric field is assumed to exist in the cavity due to the small dielectric thickness 'T'. In Eq. (2), a vertical delta current source J_s is assumed to excite the cavity to mimic a switching circuit. By evaluating the curl of the electric field in Eq. (2), the magnetic field in cavity I can be expressed as

$$H_{cav1,x} = \frac{J_s}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{\varepsilon_m^2\varepsilon_n^2}{k_{mn}^2 - k^2}\frac{n\pi}{b}\cos\frac{m\pi x_i}{a}\sin\frac{n\pi y_i}{b}\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b} \tag{3a}$$

$$H_{cav1,y} = \frac{J_s}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{\varepsilon_m^2\varepsilon_n^2}{k_{mn}^2 - k^2}(-\frac{m\pi}{a})\sin\frac{m\pi x_i}{a}\cos\frac{n\pi y_i}{b}\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b} \tag{3b}$$

In Eq. (3), the magnetic fields are along the transverse direction. Assuming initially that the ground plane GND1 is a perfect conductor, the current density at the bottom of plane GND1 can be computed as

$$J_{per\_GND1,x} = \frac{J_s}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{\varepsilon_m^2\varepsilon_n^2}{k_{mn}^2 - k^2}(-\frac{m\pi}{a})\sin\frac{m\pi x_i}{a}\cos\frac{n\pi y_i}{b}\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b} \tag{4a}$$

$$J_{per\_GND1,y} = \frac{J_s}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{\varepsilon_m^2\varepsilon_n^2}{k_{mn}^2 - k^2}(-\frac{n\pi}{b})\cos\frac{m\pi x_i}{a}\sin\frac{n\pi y_i}{b}\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b} \tag{4b}$$

$$J_{per\_GND1,z} = 0 \tag{4c}$$

where the currents in Eq. (4) are obtained from Eq.(3) through the boundary condition $\vec{J}_{per\_GND1} = \hat{n} \times \vec{H}_{cav1}$ with $\hat{n}$ being the unit outward vector normal to the surface of plane GND1. Since the magnetic fields are in the transverse direction, the induced currents at the bottom of plane GND1 flow in the transverse direction. The current computed in Eq. (4) is a surface current which cannot penetrate the conductor, since the conductor is assumed to be perfect with infinite conductivity.

If the center conductor plane GND1 in Fig. 3. is assumed to have a finite conductivity, the current through the cross section of the conductor has the form:

$$\vec{J}_{non\_GND1}(z) = \vec{J}_0 e^{-\gamma z} \tag{5}$$

where $\vec{J}_{non\_GND1}$ is the distribution of the current across the cross section of the non-ideal conductor and the parameter γ is related to the metal conductivity and frequency through the equation

$$\gamma = (1+j)\sqrt{\frac{\varpi \mu_0 \sigma_c}{2}} \tag{6}$$

where σ_c is the metal conductivity and ϖ is the angular frequency. In Eq.(5), the unknown constant $\vec{J}_0$ can be computed by assuming that the total current in the non-ideal conductor GND1 is equal to that in the perfect conductor. This assumption which is a perturbational solution can be represented in the form:

$$\int_0^t \vec{J}_{non\_GND1}\, dz = \vec{J}_{per\_GND1} \tag{7}$$

where t is the thickness of the plane GND1. By combining Eq. (5) and Eq. (7), the constant $\vec{J}_0$ can be computed as

$$\vec{J}_0 = \frac{\gamma}{1-e^{-\gamma}} \vec{J}_{per\_GND1} \tag{8}$$

Hence, for a thickness 't', the current density at the top of plane GND1 can be obtained by combining Eq. (5) and Eq. (8) as

$$\vec{J}_{GND1,top} = \frac{\gamma e^{-\gamma}}{1-e^{-\gamma}} \vec{J}_{per\_GND1} \tag{9}$$

The current designated by Eq. (9) flowing at the top of the plane GND1 acts as the source of coupled noise in the quiet cavity II composed of planes V2 and GND1 in Fig. 3. Since the current and electric field in a conductor are related by

$$\vec{J} = \sigma_c \vec{E} \tag{10}$$

the electric field at the top of plane GND1 can be computed as:

$$\vec{E}_{GND1\_top} = \frac{\nu}{\sigma_c} \vec{J}_{per\_GND1} \tag{11}$$

where the constant $\nu = \frac{\gamma e^{-\gamma}}{1-e^{-\gamma}}$.

In Eq. (11), since the current is in the transverse direction on the plane, the electric field is along the transverse direction. Using the boundary condition that the tangential electric field is continuous at an interface, the electric field computed in Eq. (11) is the field at the bottom surface of cavity II.

Since the field distribution in cavity II is not known, the variation of the electric field in cavity II can be described as

$$\vec{E}_{cav2} = \frac{\nu}{\sigma_c} \vec{J}_{per\_GND1} f_{mn}(z) \tag{12}$$

where $f_{mn}(z)$ is an arbitrary function with a maximum of '1' at the bottom surface of cavity II and a minimum of '0' at the top surface of cavity II. This is based on the assumption that the electric field decays to zero at the top of cavity II. This can be extended to 'n' cavities in a multi-layered structure where the function $f_{mn}(z)$ is assumed to be zero at the top surface of the n^{th} cavity, which is equivalent to the electric field decaying to zero at the top of the n^{th} cavity. It is important to note that Eq. (12) is a perturbational solution to the electric fields which is a good approximation, as will be justified later through measurement.

Since the fields in cavity II have to satisfy the wave equation, substitution of Eq. (12) into the wave equation leads to

$$(\frac{\partial^2}{\partial z^2} + C_{mn}^2) f_{mn}(z) = 0 \tag{13a}$$

where

$$C_{mn}^2 = k^2 - (\frac{m\pi}{a})^2 - (\frac{n\pi}{b})^2 \quad \text{and}$$

$$f_{mn}(z)=\begin{cases}1; & z=0\\ 0; & z=T\end{cases} \tag{13b}$$

For two plane pairs, as shown in Fig.3, the solution of Eq. (13) is

$$f_{mn}(z)=\frac{-\sin[C_{mn}(z-T)]}{\sin(C_{mn}T)} \tag{14}$$

Applying the divergence condition $\nabla\cdot\vec{E}=0$ in the source free cavity II region to calculate the vertical and transverse components of the electric field and integrating over the thickness of the cavity, the voltage in cavity II, V_{cav2}, can be derived as

$$V_{cav2}=\frac{J_s\nu}{ab\sigma_c}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{-\varepsilon_m^2\varepsilon_n^2k_{mn}^2}{(k^2-k_{mn}^2)^2}\cos\frac{m\pi x_i}{a}\cos\frac{n\pi y_i}{b}\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b} \tag{15}$$

which leads to the transfer impedance between port 'i' in cavity I and port 'j' in cavity II as

$$Z_{ij}=\frac{A}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{-\varepsilon_m^2\varepsilon_n^2k_{mn}^2}{(k^2-k_{mn}^2)^2}\cos\frac{m\pi x_i}{a}\cos\frac{n\pi y_i}{b}\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b} \tag{16}$$

In Eq. (16), (x_i,y_i) is the coordinate of the excitation port in cavity I. Similarly, (x_j,y_j) is the coordinate of the coupled port in cavity II. The parameter A is a function of the metal thickness 't' and conductivity 'σ_c' of plane GND1 given by $A=\frac{\nu}{\sigma_c}$. In Eq. (16) $\frac{k_{mn}^2}{(k^2-k_{mn}^2)^2}$ is a frequency-dependent factor that determines the poles of the system. The primary difference between Eq. (1) and Eq. (16) is that the latter equation contains 2nd order poles which give rise to sharper peaks in the response at the resonant frequencies of the structure.

Through a similar procedure, the method can be extended to multiple plane pairs containing more than two cavities. As an example, consider a three plane pair structure consisting of a homogeneous dielectric as shown in Fig. 4. The three cavities in the multi-layered structure are formed by planes V1, GND1, V2 and GND2 in Fig. 4. Assuming a current excitation in cavity I, the transfer impedance between the excitation port '*i*' in cavity I and the measured port '*j*' in cavity III can be computed as

$$Z_{ij} = \frac{1}{j\varpi\mu}\frac{A^2}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{-\varepsilon_m^2\varepsilon_n^2 k_{mn}^2}{(k^2-k_{mn}^2)^{5/2}}\frac{k^2}{\sin(C_{mn}T)}\cos\frac{m\pi x_i}{a}\cos\frac{n\pi y_i}{b}\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b} \quad (17)$$

Details on the derivation of Eq. (17) have not been discussed in this paper since the coupled voltage beyond the second cavity is typically small due to the factor A^2. Therefore, the leakage of energy beyond one plane pair can be ignored in most realistic structures.

III Model to Measurement Correlation

The model for the impedance derived in Eq. (16) was compared with measurement on a ceramic test vehicle. The test vehicle consisted of three planes as shown in Fig. 5a. with lateral dimensions of a=47.53 mm and b= 47.53 mm. Tungsten metallization was used with metal thickness t=12 μm and conductivity $\sigma_c = 0.67\times10^7$ s/m. The dielectric medium was homogeneous with permittivity $\varepsilon_r = 9.8$ and thickness T=150 μm. The source port and coupling port were located at x= 5.52 mm, y= 43.46 mm and x= 42.41 mm, y= 4.24 mm, respectively. The scattering parameter S12, which denotes the transmission and coupling of energy between the ports, was measured using an HP8510B vector network analyzer. The correlation between the model and

measurement is shown in Fig. 5b which shows good agreement. As can be seen, substantial coupling (-20 to –30 dB) occurs at the resonant frequency of the structure with the first two resonant peaks coupling the maximum voltage. As expected, the amplitude of the coupled energy between the plane pairs decreases as frequency increases, which can be attributed to skin effect that reduces the amplitude of the current penetrating the conductor.

The effect of resonance on the distribution of current in the center conductor in Fig. 5 can be illustrated by plotting Eq. (5) as a function of the metal thickness across the center of the conducting surface at two frequencies, namely a frequency far from resonance and a frequency at resonance. This is shown in Fig. 6 at f=0.4 GHz (far from resonance) and f=2 GHz (resonance frequency). In Fig. 6a, the current density across the cross section of the center conductor is minimum. However, in Fig. 6b.substantial current density exists across the cross section of the conductor. In addition, the current density shows a standing wave pattern with maximum penetration at specific points along the surface of the center conductor.

IV.Simulation of a Microprocessor Application

In this section, the effect of coupling between plane pairs for a gigahertz microprocessor application is discussed.

Consider the test case of a ceramic single chip module shown in Fig.7a. The chip measures 2 cm × 2 cm and is mounted on a ceramic package of size 4.8 cm × 4.8 cm. Three planes are used to supply power to the chip which is similar in cross section to Fig. 5a. where the top plane is the voltage plane for the core and the bottom plane is the

voltage plane for the I/O. The center plane serves as the common ground for the voltage plane V1 and V2. The separation between the planes is T=150 μm and the plane thickness t=10 μm. Tungsten was used as the metallization with conductivity $\sigma = 0.67 \times 10^7$ (s/m). The space between the planes was filled with a dielectric with permittivity $\varepsilon = 9.8\varepsilon_0$.

Consider groups of circuits within the microprocessor core switching simultaneously. They are powered by the top two planes in the package. These circuits are represented as '*' in Fig. 7a. where each group of circuits is a 10 A current source, for a total of 50 A for the microprocessor. A field point is also shown in Fig. 7a. between the center and bottom plane at which the coupled noise is measured. The coupling between the five sources and the field point is shown in Fig. 7b, which was computed using Eq. (16). In Fig. 7b, superposition has been used whereby the individual response from the five sources have been computed and added together. As can be seen in Fig.7b, maximum coupling occurs at 2 GHz.

Consider next a switching frequency of 2GHz for the microprocessor core which translates to a period of 0.5 ns with rise time and fall time of 62.5 ps as shown in Fig. 8a. When the microprocessor core switches for two cycles, it couples energy into the I/O power supply as shown in Fig. 8b. This was computed using the frequency response in Fig. 7b. with the source current defined in Fig. 8a. From Fig. 8a, the maximum coupled noise for two switching cycles is ± 100 mv. However, when the core switches for 30 cycles, more coupled noise can be generated in the system. The coupled energy in Fig. 9b gradually increases during the initial 5ns, reaches a steady state and gradually decreases after the core stops switching. It is interesting to note that the I/O power supply bounces

± 400 mV in the steady state which is large and therefore cannot be ignored. Moreover, the coupled energy lasts for 5ns even after the core has stopped switching due to the high quality factor of the cavity. Both these effects can deteriorate the functioning of future microprocessors operating at gigahertz frequencies. In addition, the interconnect I/Os in the package operating at high frequencies can also cause coupling between plane layers.

It is important to note that the penetration of the magnetic field induces varying magnitudes of coupled voltage at different positions of the field point. The coupled voltage exhibits a standing wave pattern across the plane surface consisting of peaks and nulls. The peak locations lead to the maximum coupling of energy resulting in large voltage fluctuations.

V. Suppression of Coupled Noise

The coupled noise between plane pairs discussed in this paper is undesired and needs to be suppressed.

In [1] and [9], optimization methods have been proposed to minimize the impedance between ports by varying the position of the excitation and coupled ports. Since Eq.(1) and (16) contain similar cosine factors that capture the position of the ports, these optimization methods can be applied to minimize the coupling between power planes.

An alternate method for minimizing coupling is by varying the metal conductivity 'σ_c' and metal thickness 't' which occur in Eq. (16). To show the effect of conductivity on coupling, the structure in Fig. 7 was simulated with two different metallizations, tungsten ($\sigma_c = 0.67 \times 10^7$ s/m) and copper ($\sigma_c = 5.81 \times 10^7$ s/m). It can be observed from

the comparison in Fig. 10 that the plane with copper metallization has much smaller trans-impedance as compared to the plane with tungsten metallization. Since the conductivity is at the denominator of Eq. (16), the scaling factor would be smaller for higher conductivity metal. Since copper has higher conductivity, the attenuation constant $\alpha = \sqrt{\pi f \mu \sigma_c}$ (real part of γ) is larger which results in a smaller depth of penetration of the magnetic field and current in the center plane.

Another important parameter in the scaling factor A in Eq. (16) is the thickness of the metal plane 't'. To demonstrate its effect, the structure in Fig. 7 was simulated with varying thickness by assuming tungsten as the metallization. The results are shown in Fig. 11 where a larger metal thickness results in better isolation between plane pairs.

The coupled noise can also be suppressed by reducing the quality factor Q of the cavity. This can be achieved by reducing the dielectric thickness between the planes or by increasing the loss tangent of the dielectric material.

An alternate method which is not related to the impedance in Eq. (16) is to use decoupling capacitors to reduce the impedance of the planes, which has not been discussed in this paper.

VI. Conclusion

This paper discusses a method for modeling the effect of field penetration through planes in package power distribution networks. The correlation between measurement and computation demonstrates the validity of the approach. The effects of penetrating fields have been computed both in the frequency and time domain, for a microprocessor that switches continuously over many cycles. Based on the analysis, large coupled noise

was generated in the system due to the coupling between the plane layers, in the steady state. Methods to reduce this noise were suggested by using thick planes with high conductivity metal. Since the modeling method is an extension of the cavity resonator method for a single plane pair, the solution retains its analytical representation. Hence, multiple plane layers can be analyzed using this method.

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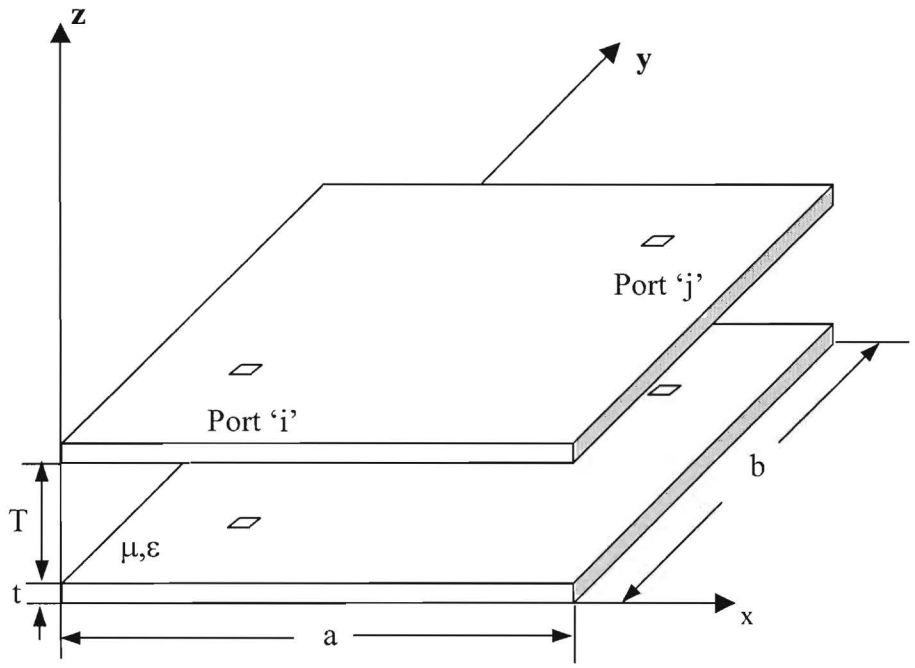


Fig.1 Power plane pair modeled as a cavity

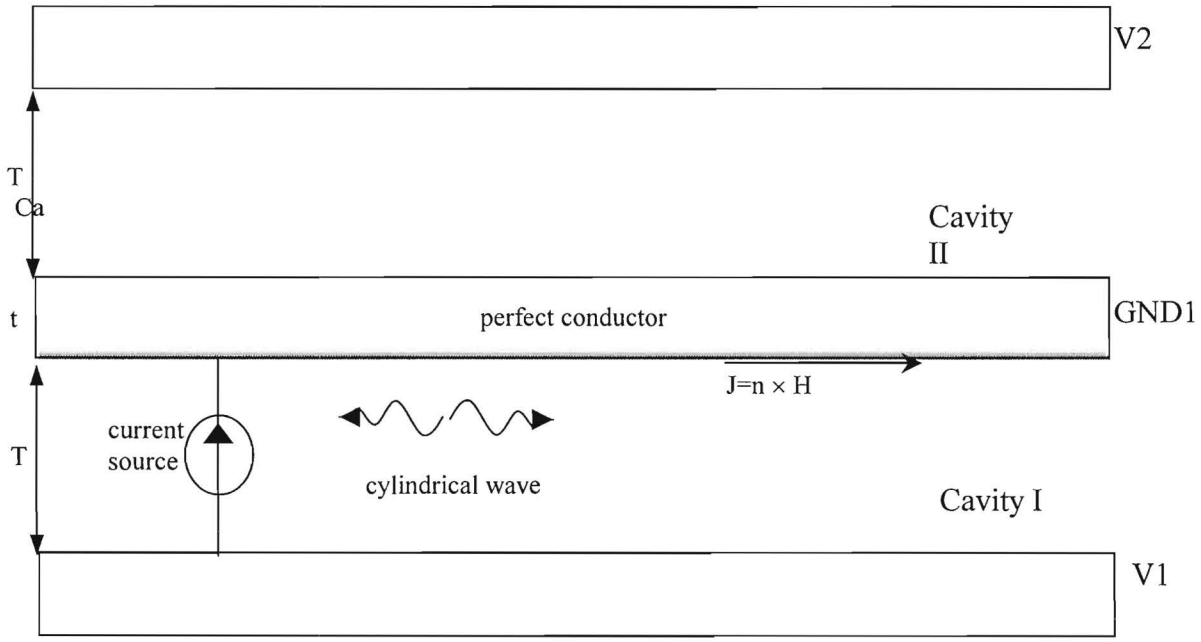


Fig.2 Three-layer package planes constructed with high conductivity metal (perfect conductor)

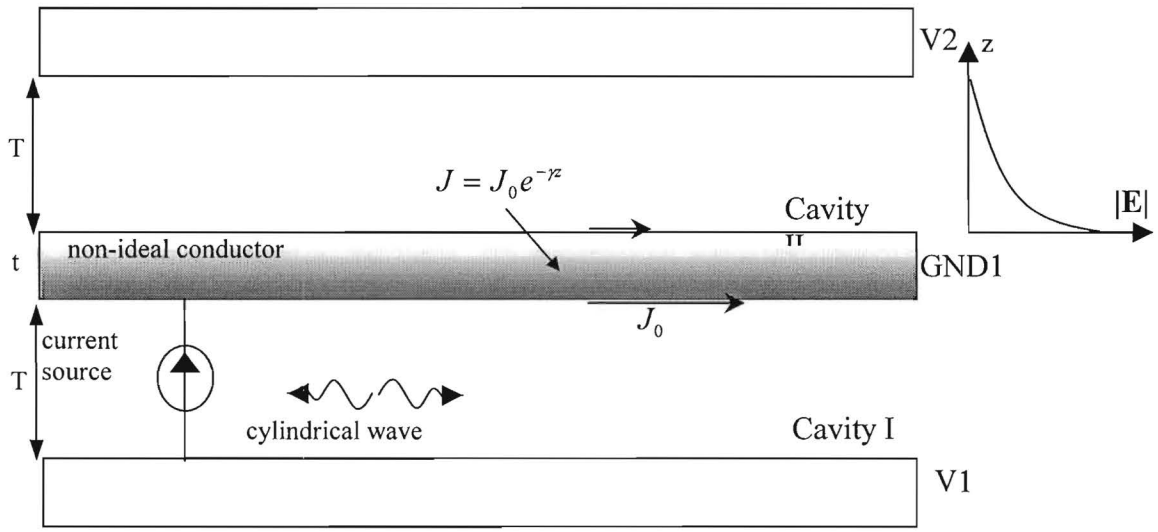


Fig.3 Three-layer package planes constructed with non-ideal conductor

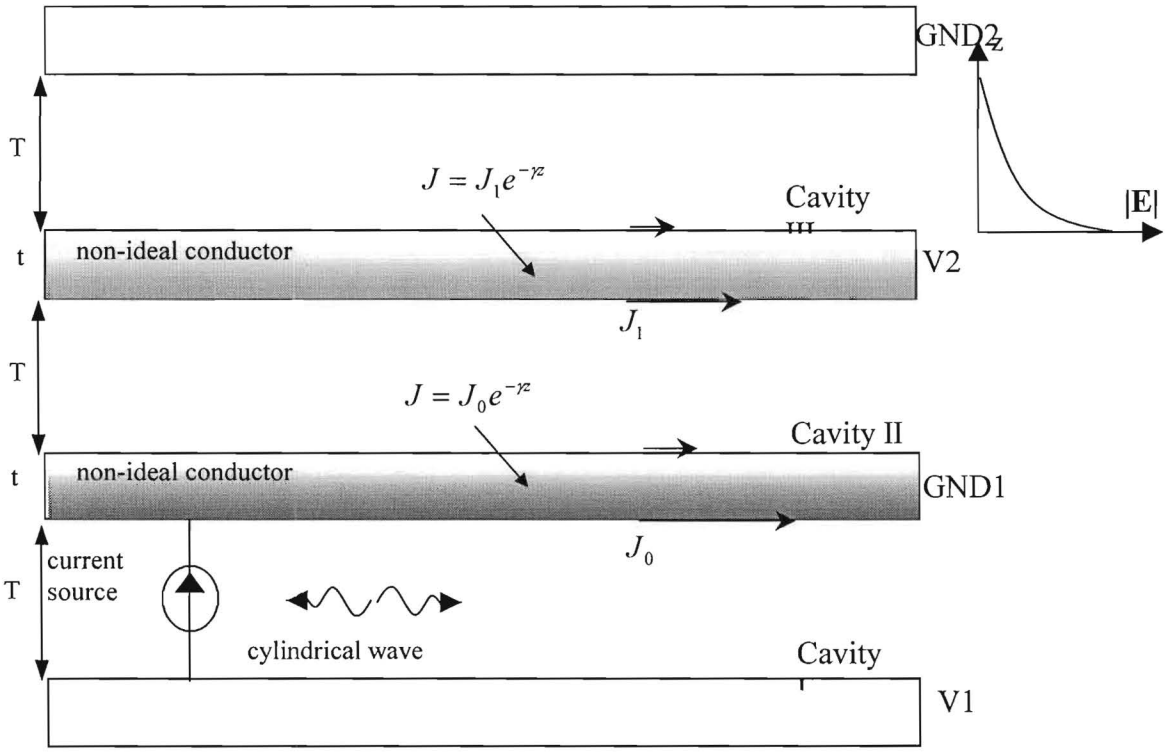
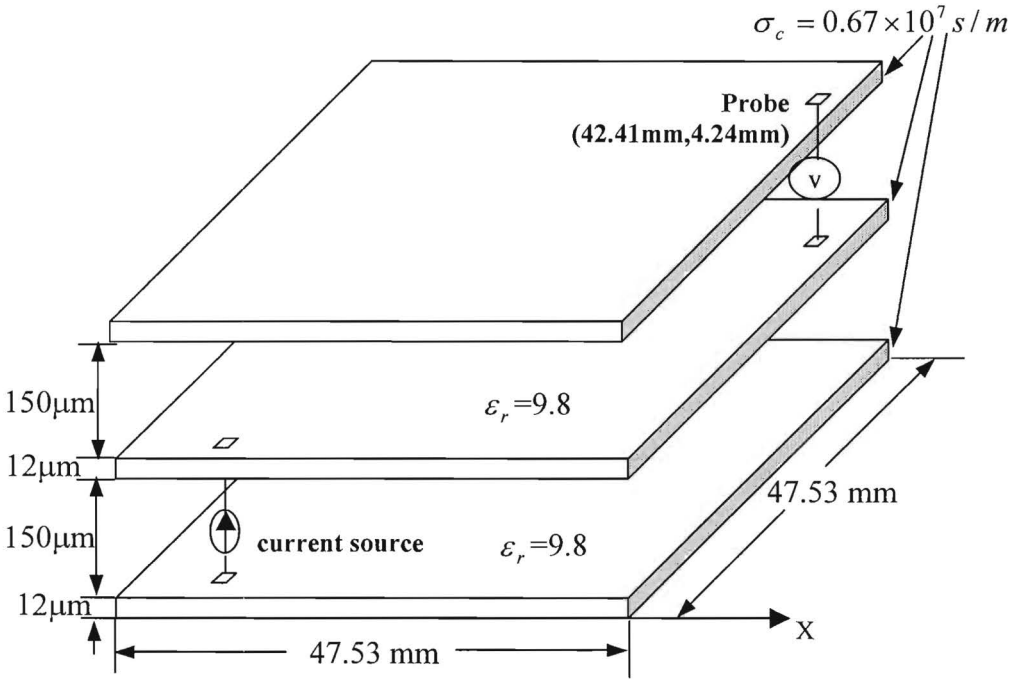
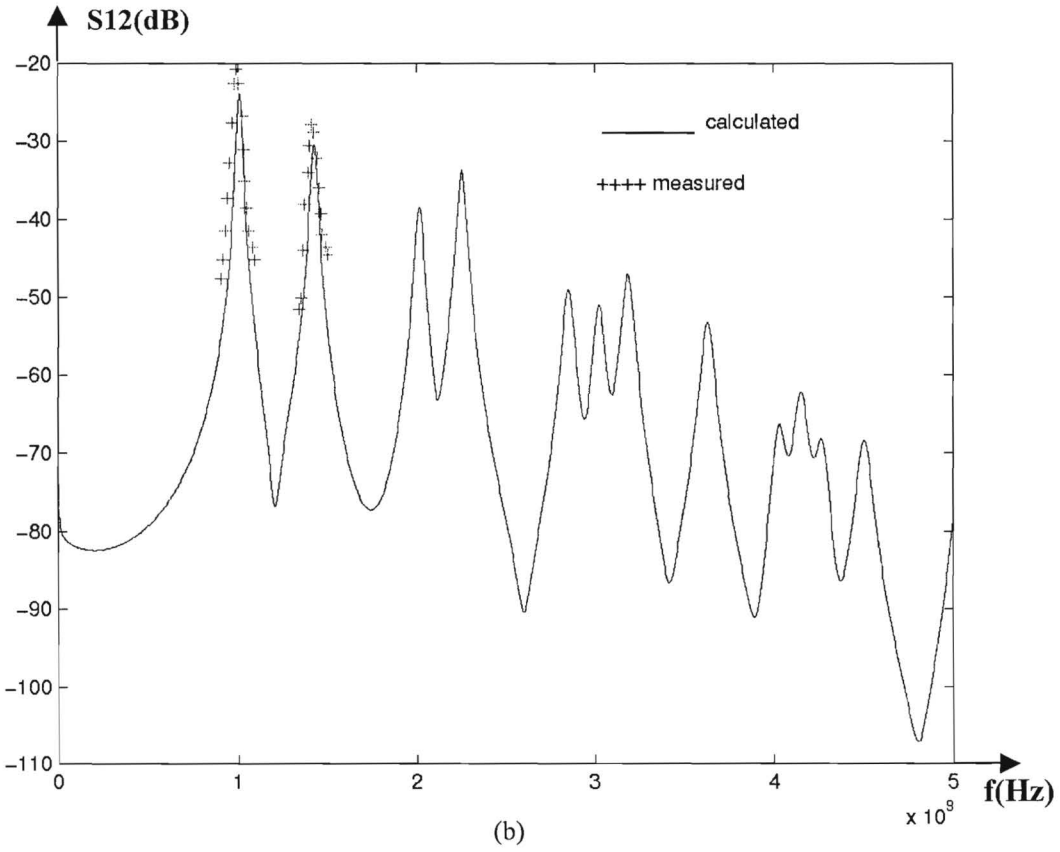


Fig.4 Four-layer package constructed with non-ideal conductor

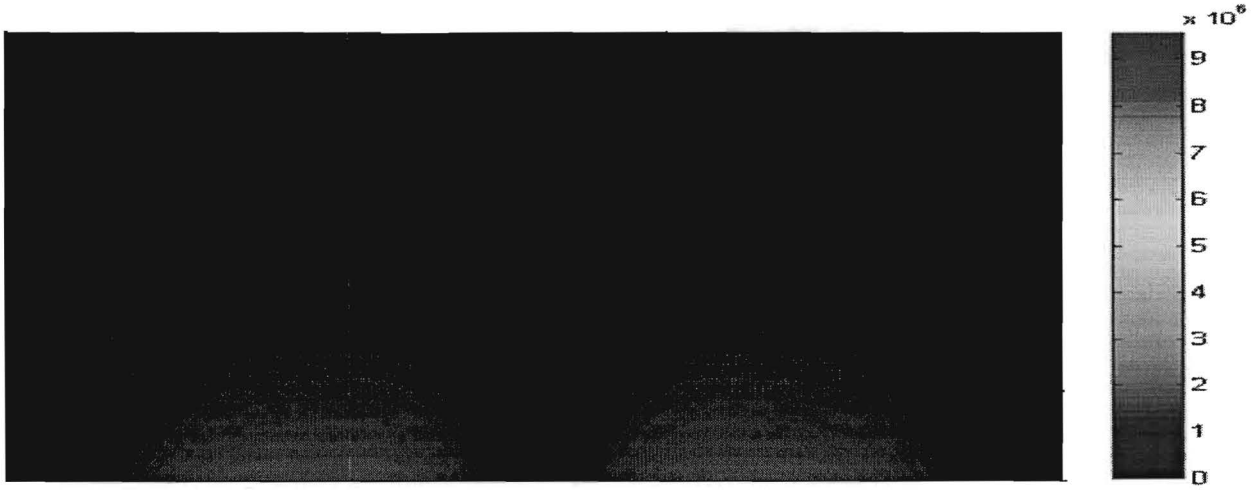


(a)

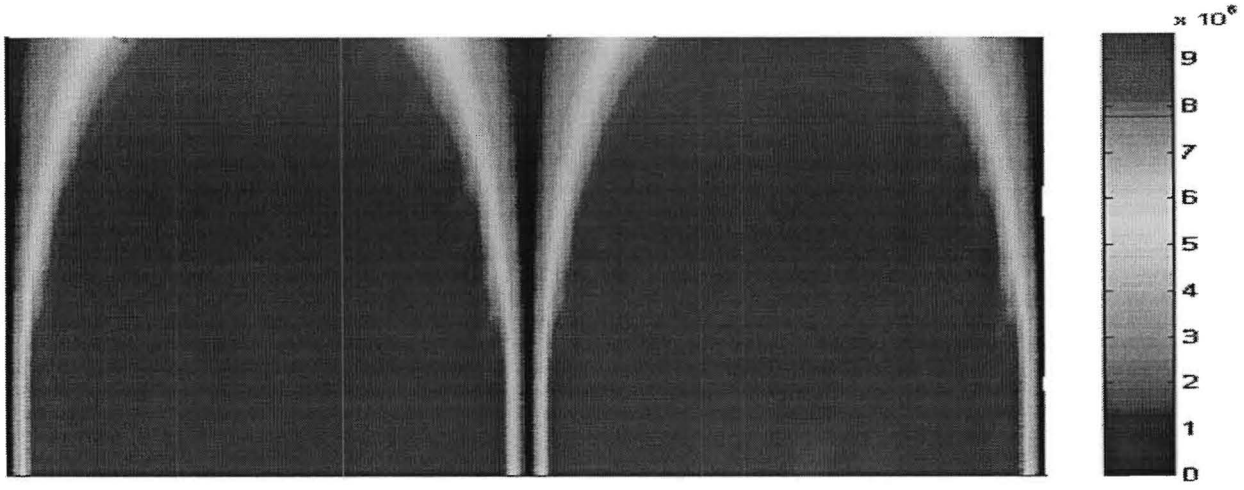
Fig.5 Measurement to model correlation a)Cross section of test vehicle b) Comparison between simulation and measured data


S12(dB)
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
0
1
2
3
4
5
x 10^9
f(Hz)
calculated
++++ measured

(b)

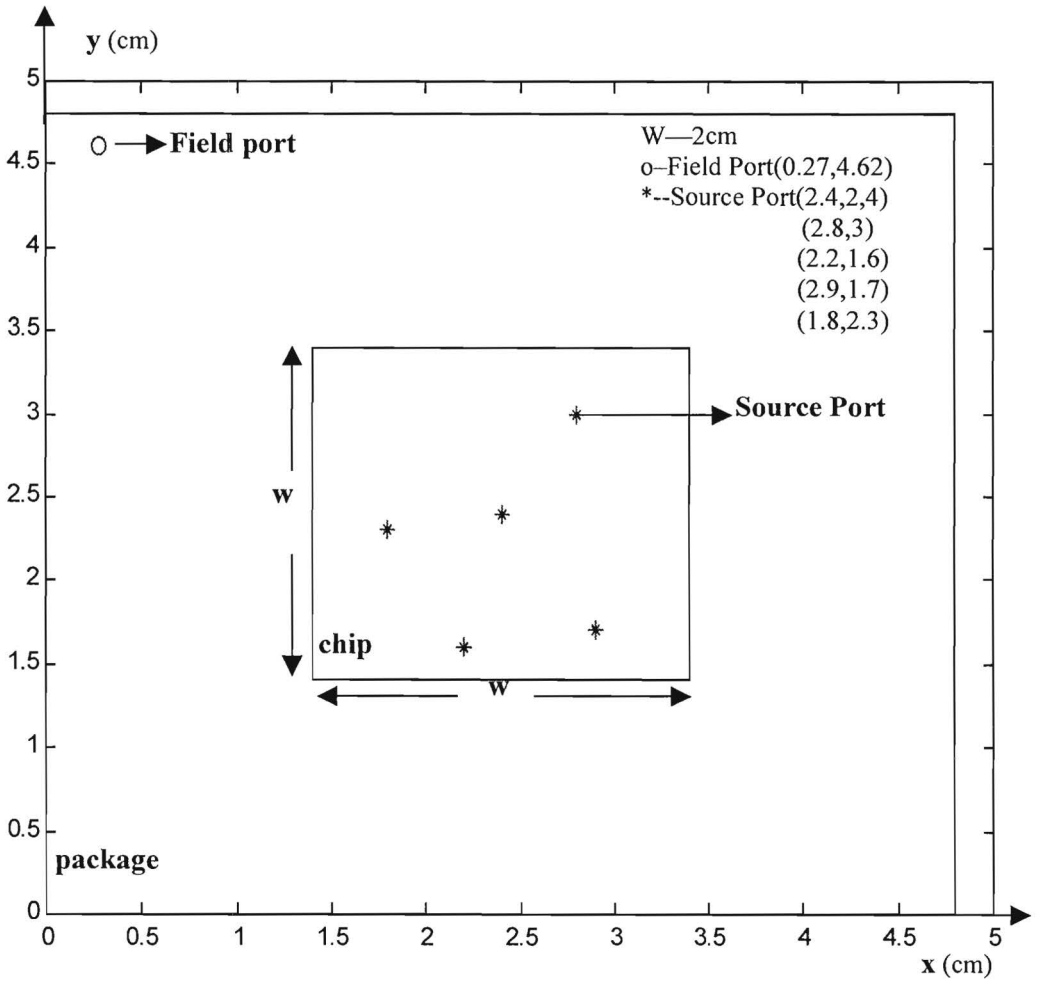


(a)



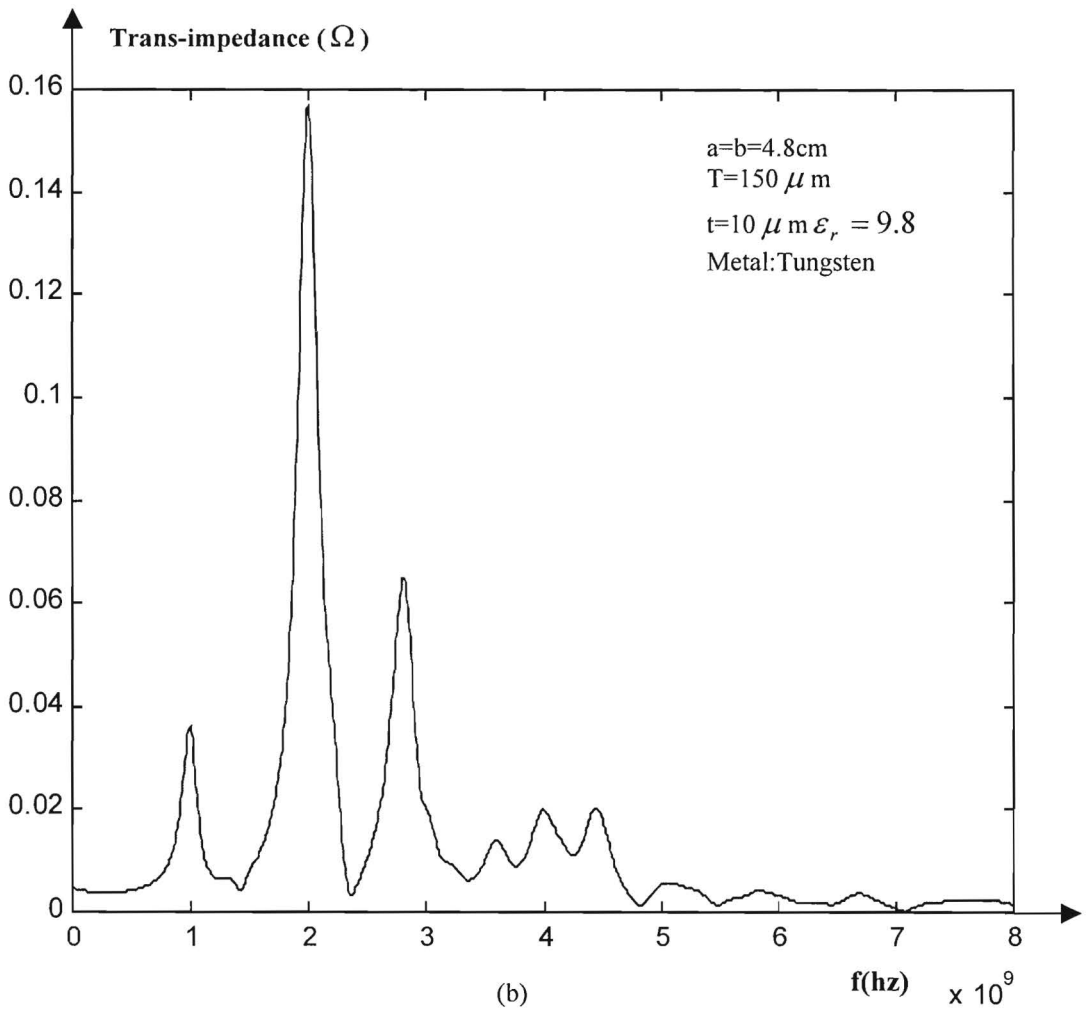
(b)

Fig.6. Current distribution in the cross section of GND1 plane a) f=0.4 GHz b) f=2.0 GHz

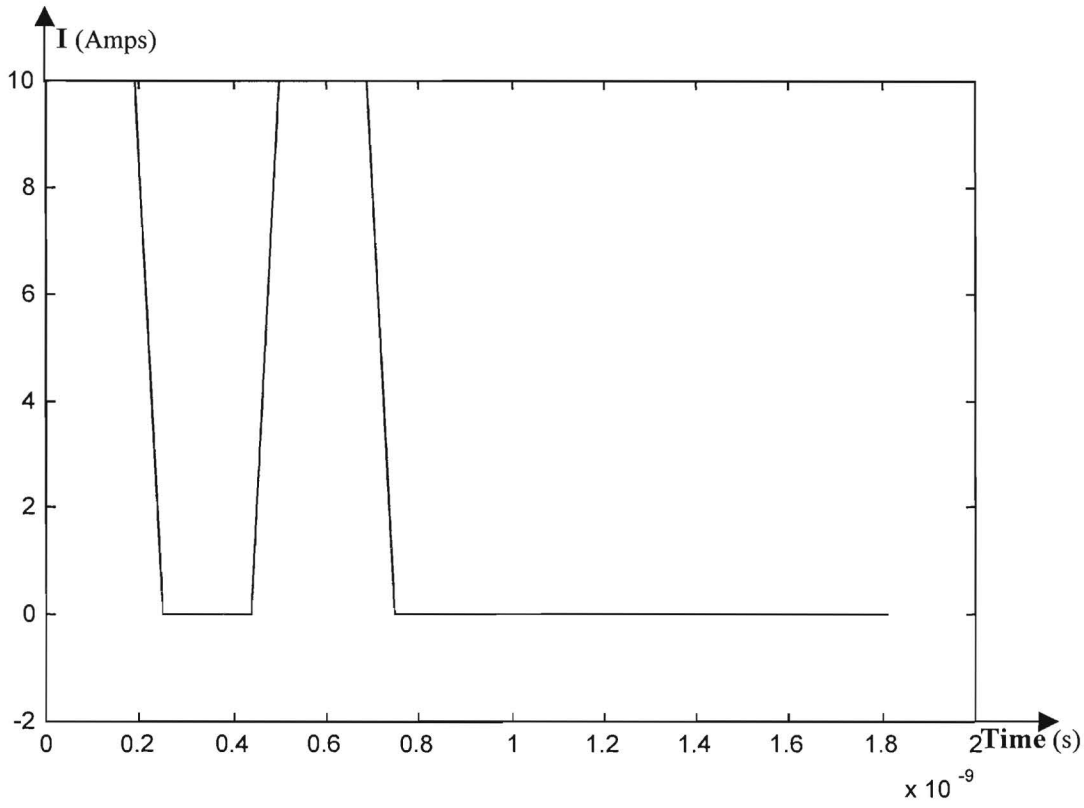


(a)

Fig. 7. Microprocessor package a)Top view of the single chip module
b) Trans-impedance Vs frequency

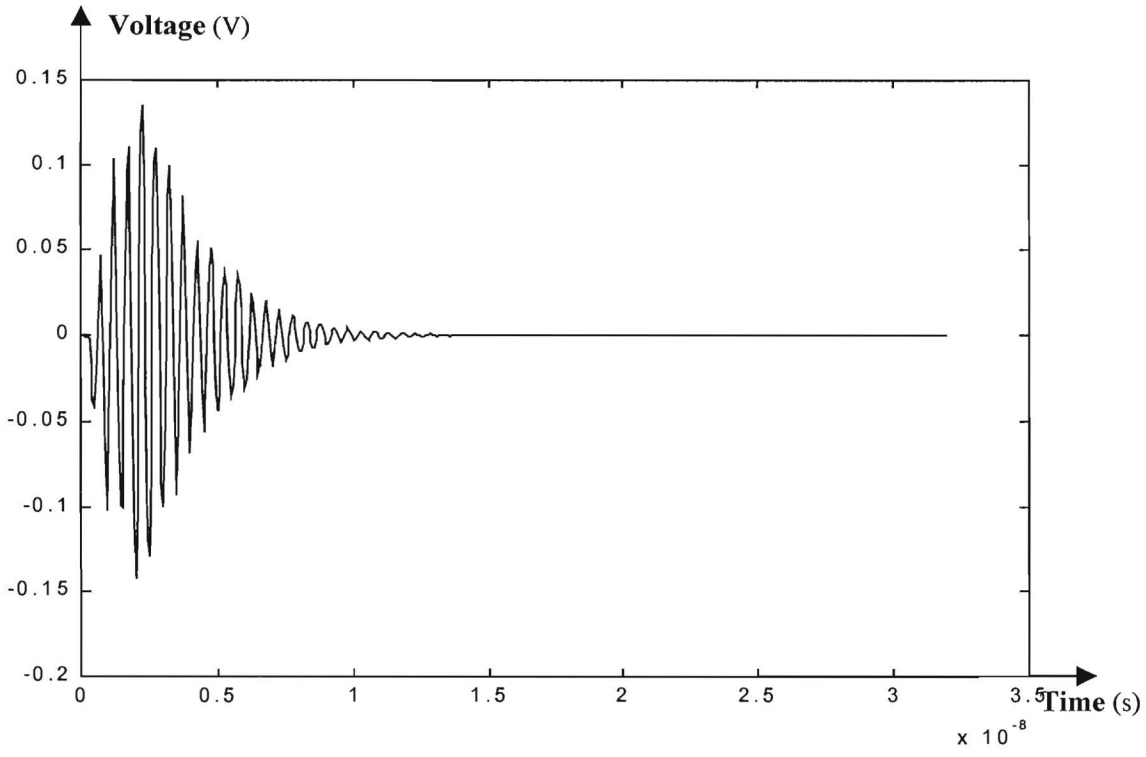

Trans-impedance (Ω)
0.16
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
a=b=4.8cm
T=150 μ m
t=10 μ m ε_r = 9.8
Metal:Tungsten
0
1
2
3
4
5
6
7
8
f(hz)
x 10^9

(b)

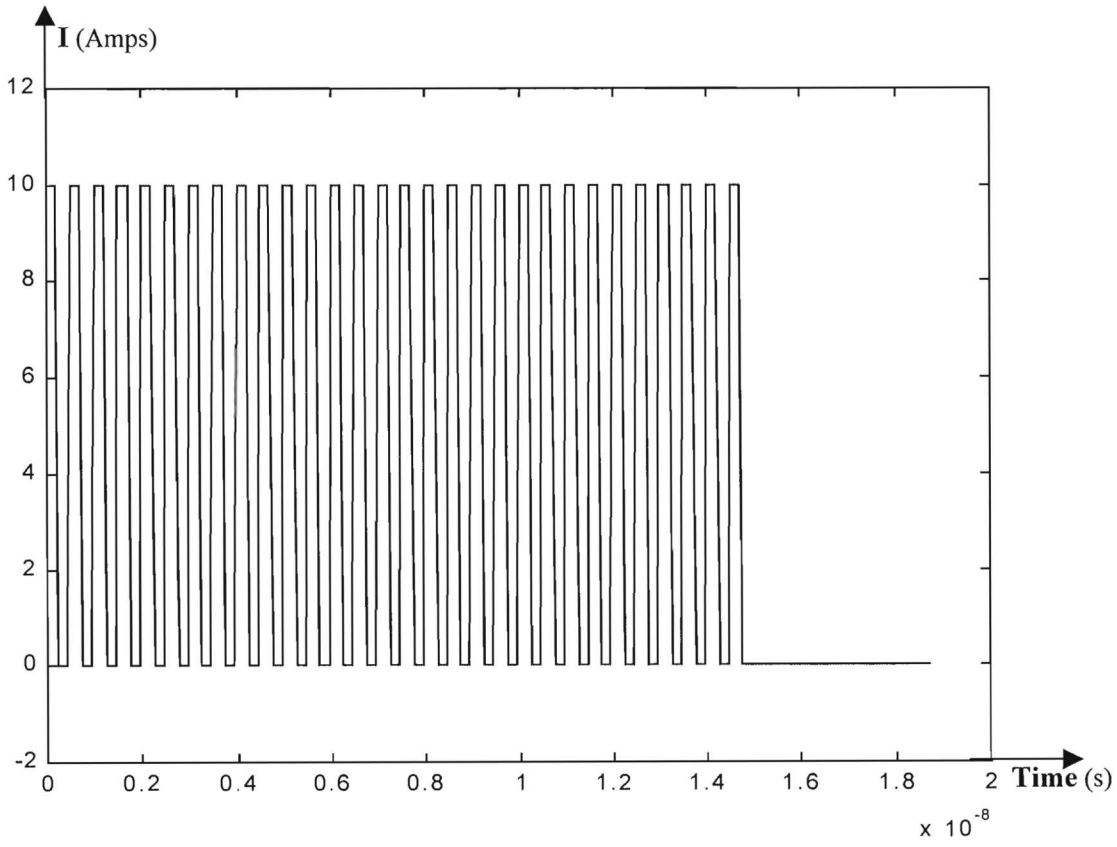


(a)

Fig 8 Excitation and voltage fluctuation for 2 switching cycles
a)source waveform b)coupled voltage

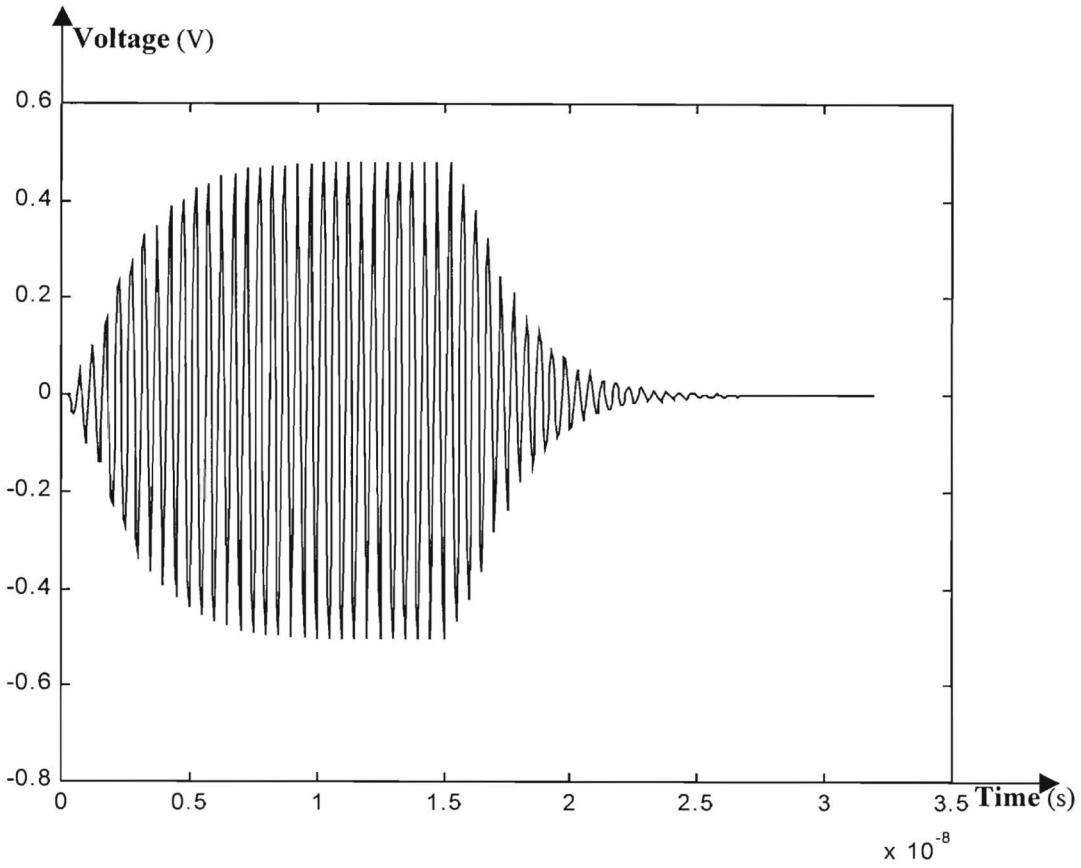


(b)



(a)

Fig.9 Excitation and voltage fluctuation for 30 switching cycles
a)source waveform b)coupled voltage



(b)

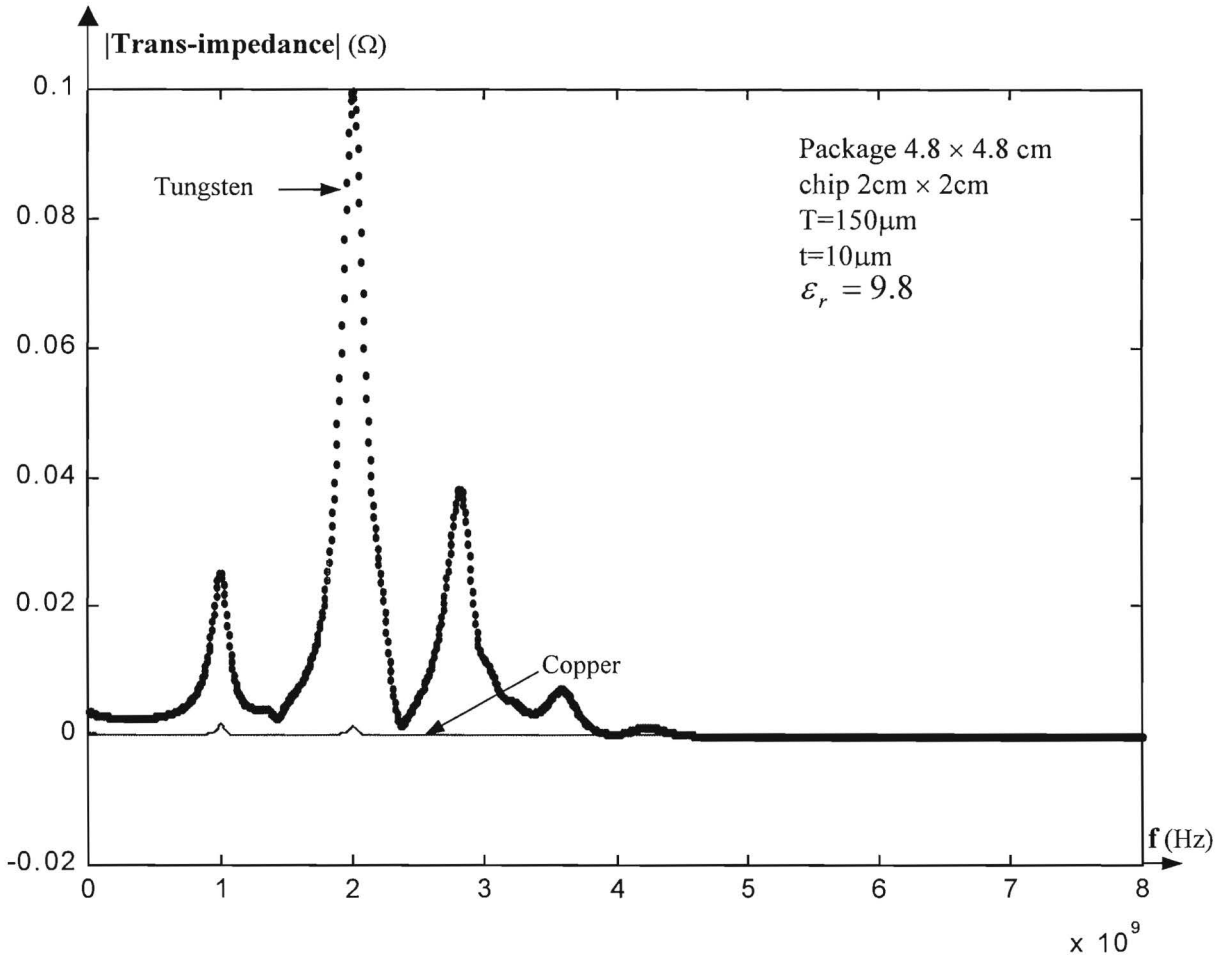


Fig. 10 Effect of metal conductivity

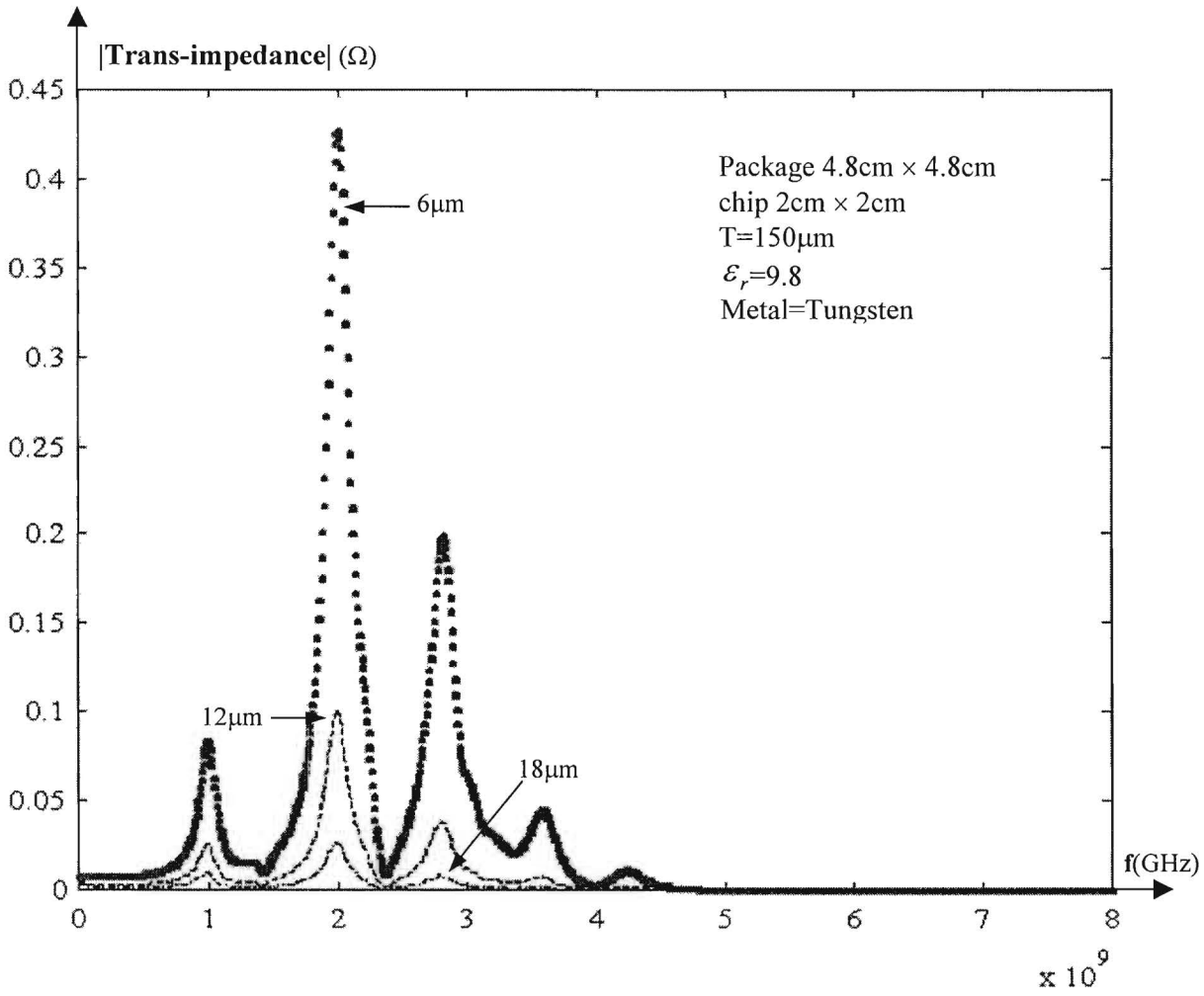


Fig. 11. Effect of metal thickness on trans-impedance

Modeling and Simulation of Core Switching Noise for ASICs

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Abstract

This paper presents simulation and analysis of core switching noise for a CMOS ASIC test vehicle. The test vehicle consists of a ceramic ball grid array (CBGA) package on a printed circuit board (PCB). The entire test vehicle has been modeled by accounting for all the plane resonances using the cavity resonator method. The models included both the on-chip and off-chip decoupling capacitors. Using both time domain and frequency domain simulations, the role of plane resonances on power supply noise for fast current edge rates has been discussed. The models have been constructed to amplify certain parts of the test vehicle during simulations.

I. Introduction

There has been much speculation in the design community about the role of plane resonances on core switching noise. In the past, partial element equivalent circuit (PEEC) based approaches have been used as illustrated in [1]. This approach used an inductive network to model the via inductances and the partial lateral inductances of the planes. However, as packages and boards become thinner with enough vias to reduce the vertical inductance, it is expected that plane effects will start dominating the core switching noise. In [2], the authors have provided an extensive analysis of the mid-frequency noise generated in multi-chip modules (MCM). The arguments in [2] are based on physics

based models that provide insight into the behavior of the MCM power delivery system. Since the models are physics based, the models have been simplified during analysis.

In [3], a method was presented for modeling planes. Though this paper provides insight into the cause and effect of plane resonances, it does not provide much detail on its importance for a complex system. Though [2] provides a methodology for modeling multi-layered packages, the modeling approach is physics based and is customized to a specific MCM. This paper, however, presents a more generic approach that is applicable to a menu of ASICs (Application Specific Integrated Circuits) supported in a semiconductor foundry.

In this paper an entire CMOS test vehicle has been modeled using the cavity resonator method [4] where both the vias and planes have been modeled. The primary goal of this paper is to demonstrate the frequency beyond which the plane effects need to be considered. In addition, the amount of noise generated by the planes (in the absence of via inductance) has been quantified for multi-gigahertz packages. Finally, a modeling method is presented that preserves the passivity of the circuit during core switching noise simulations of large networks.

Though commercial tools based on Finite Difference Time Domain (FDTD) and Partial Element Equivalent Circuit (PEEC) can analyze the structures discussed in this paper, the authors believe that the method that has been presented is ideally suited for the pre-layout analysis of multi-layered packages and boards. This analysis can be used to optimize the package cross-section prior to physical layout.

II. Test Vehicle Description

The test structure that was modeled consists of a multi-layered CBGA package and PCB. Fig. 1 shows the details of the plane layers and the decoupling capacitors in the test set-up. A CMOS ASIC test chip was mounted on the CBGA package through controlled collapse chip connections (C4) and the CBGA package was attached to the board through solder balls. The CMOS ASIC test chip measured 9 mm on a side and was fabricated with IBM's CMOS5L process technology. The test chip contained 766 C4 flip-chip pads; 468 signal, and 298 divided between voltage and ground. The pads were arranged on a 230.4 um pitch.

Signal, voltage, and ground C4's were six rows deep on the chip periphery. Each voltage-ground pair serviced seven signal I/O cells. An array of voltage and ground C4's provided power to the core logic. The core voltage C4's were placed on a 921.6 um pitch with ground C4's interstitially placed between the voltage C4's on the same pitch. The test chip and four 32nF decoupling capacitors were mounted on a 32mm CBGA package. The CBGA package had six power and ground mesh planes, three signal distribution layers, and two pad layers. The module was mounted in the center of a 9x11 inch test card. The card had eight signal layers, and six voltage and ground layers. Decoupling capacitors were mounted on the card, as shown in Fig. 1. The test vehicle was powered with a 3.3V supply on one corner of the PCB.

III. Modeling Plane Layers

In the past, the inductance of the package power distribution has been the major contributor to core logic switching noise. Hence, the test structure in Fig. 1 was previously modeled based on three dimensional package inductance models using the PEEC method discussed in [1]. Reduction techniques were then used to create an equivalent lumped inductance model. This modeling approach captured the peak inductive noise, and the resonant noise due to the LC tank circuit formed by the package inductance and the chip capacitance. Hence, the edge effects from planes were not modeled since it was not considered to be dominant due to the relatively slow speed of the ASIC test chip.

In [3], the importance of modeling radial waves between plane pairs has been discussed. It has been speculated that the plane resonances can dominate the core noise for fast chips on packages/boards with negligible vertical via inductance. To verify the speculation, the test vehicle in Fig. 1 was re-modeled to account for the plane resonances. In [3], [4], a method has been presented for modeling planes. This method uses a cavity resonator model to represent a plane pair as an electromagnetic system. This method was then extended to multiple plane pairs under the skin effect approximation which allows each plane pair to be modeled separately and recombined during simulation [3], [4]. The cavity resonator model has been used in this paper, which has been briefly described in this section for a single plane pair. It is important to note that multiple plane layers have

been represented using an equivalent plane pair in [2]. However, in this paper, a more extensive model has been used that enables the simulation of noise on every plane pair.

Consider a plane pair, as shown in Fig. 2. The structure can be modeled as an electromagnetic system by assigning ports to the structure. Ports represent positions on the plane pair where either a current source exists or a voltage is to be measured.

The impedance matrix between the ports can be computed as [3]:

$$Z_{ij}(\omega) = j\omega\mu d \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{\varepsilon_n^2 \varepsilon_m^2}{(k_{mn}^2 - k^2)ab} f(x_i, y_i, x_j, y_j) \quad (1)$$

where

$$f(x_i, y_i, x_j, y_j) = \left(\cos\frac{m\pi x_i}{a} \operatorname{sinc}\frac{m\pi t_{xi}}{2a}\right) \cdot \left(\cos\frac{n\pi y_i}{b} \operatorname{sinc}\frac{n\pi t_{yi}}{2b}\right)$$

$$\cdot \left(\cos\frac{m\pi x_j}{a} \operatorname{sinc}\frac{m\pi t_{xj}}{2a}\right) \cdot \left(\cos\frac{n\pi y_j}{b} \operatorname{sinc}\frac{n\pi t_{yj}}{2b}\right)$$

$k = k' - jk''$ with $k' = \omega\sqrt{\varepsilon\mu}$ and

$k'' = \omega\sqrt{\varepsilon\mu}\,(\tan\delta + r/d)/2$,

$k_{mn}^2 = (m\pi/a)^2 + (n\pi/b)^2$,

$r = 1/\sqrt{\pi f \mu\sigma}$ the skin depth,

δ is the dielectric loss angle,

m, n are the propagating modes,

(x_i, y_i), (x_j, y_j) are the co-ordinates of the port locations, and

(t_{xi}, t_{yi}), (t_{xj}, t_{yj}) are the dimensions of the ports.

The impedance matrix in equation (1) can be rewritten as [4]:

$$Z_{ij}(\omega) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{N_{mni} N_{mnj}}{1/j\omega L_{mn} + j\omega C_{mn} + G_{mn}} \quad (2)$$

where $L_{mn} = d/(\omega_{mn} ab\varepsilon)$,

$C_{mn} = ab\varepsilon/d$,

$G_{mn} = (ab\varepsilon/d)\,\omega_{mn}\,(\tan\delta + (\sqrt{2/\omega_{mn}\mu\sigma})/d)$,

and $N_{mni}=\varepsilon_n\varepsilon_m \cos\frac{m\pi x_i}{a}\ \mathrm{sinc}\frac{m\pi t_{xi}}{2a}\ \cos\frac{n\pi y_i}{b}\ \mathrm{sinc}\frac{n\pi t_{yi}}{2b}$.

The conductance G_{mn} can be approximated as $G_{mn}=(\ ab\varepsilon/d^2\ )\sqrt{2\omega_{mn}/\mu\sigma}$ for low dielectric loss ($\tan\delta<<r/d$) substrates. In equation (2), each propagating mode is represented as a parallel resonant circuit. The port response is, therefore, represented as the summation of infinite modes. In equations (1) and (2), the ground plane in Fig. 2 is assumed to be an equipotential surface in [3]. To account for the potential variation across the ground plane, the circuit as shown in Fig. 3 was constructed by separating the reference nodes [4].

The circuit in Fig. 3 is a passive circuit and meets all the passivity conditions. Since the CBGA package and board in the test set-up consist of multiple plane layers, each plane pair in the structure was first modeled seperately using the above method and combined together in SPICE using the skin effect approximation described in [3]. This enabled the construction of a multi-layered stack-up for the test vehicle described in Fig. 1. For the package planes, a total of 9 modes were used which corresponds to frequency bandwidth of 4.3 GHz. Similarly, 49 modes were used to model the PCB planes which supports a bandwidth of 2.39 GHz. The modes represent m, n values in equation (1). The frequency bandwidth used was considered to be sufficient for the ASIC described in Fig. 1.

With the resonator model that included the cavity resonances of the planes, the following test cases were simulated: i) core noise with only the package model, ii) core noise with the package model and on-chip capacitance, iii) core noise with the package and PCB models integrated, where the PCB model included decoupling capacitors, iv) core noise using the model in iii) containing decoupling capacitors mounted on the package and v) core noise using the model in iv) with the on-chip capacitance included. Using this approach, the importance of each part can be assessed.

IV. Core Switching Noise using the Package Model

The CBGA package alone was modeled and simulated to understand the effect of the package planes on core noise. The ports on the chip area of the package were defined as shown in Fig. 4.

Five ports for ground and four ports for Vdd were defined for the C4 locations in the core area of the chip, as shown in Fig. 4. The same number of grounds and Vdds were defined for the vias connecting from the planes to the solder balls. The ground planes and Vdd planes were connected together using through vias at the C4 locations. The chip was powered at the bottom of the package by connecting an ideal voltage source to the solder ball locations between Vdd and ground. A current source as shown in Fig.5 was connected between ports 5 and 9 in Fig. 4 to emulate the on-chip switching activity of the circuit. The fluctuation on the ASIC power supply was observed between ports 18 and 19 in Fig. 4. Vias, C4s and solder balls were modeled with lumped inductors of 15pH, 10pH and 10pH, respectively. The inductances for the C4s and solder balls were based on the number of these structures in parallel at each port location. Similarly, the via inductance was derived using the PEEC method for a group of vias in parallel per layer, at each port location. No decoupling capacitors were included in the simulation model. The model was first simulated using the current source in Fig. 5 with 1ns rise time (t_r) and 9ns fall time (t_f).

The simulation result for the voltage fluctuation between ports 18 and 19 is shown in Fig. 6. In Fig. 6, the oscillatory waveform was produced by the package plane resonances and the deep valleys in the waveform were caused by the inductances of vias, C4s and solder balls. It can be clearly seen that the noise due to the plane resonance is trivial compared to the noise due to the inductances in this simulation.

The same simulations were repeated with faster current sources. The results with a current source of 0.5ns rise time and 4.5ns fall time and a current source of 0.1ns rise time and 0.9ns fall time are shown in Figs 7 and 8, respectively. The simulation results show that the noise contribution due to the planes increases with faster current sources, suggesting that the source excites the plane resonances. The plane contribution is almost equal to the inductive contribution in Fig. 7 and the main contribution to the noise is from the plane in Fig. 8. In Figs 7 and 8, the sharp peaks are due to high frequency noise. From Fig. 8, clearly the CBGA package in the CMOS5L Test Vehicle cannot support a 100 ps edge rate (without on-chip capacitance) since the noise is almost equal to the logic swing. This, however, can be a very myopic view since only a small part of the entire system, namely the package, has been considered.

V. Core Noise with Package and On-chip capacitance

Using a current source with 0.1ns rise time and 0.9ns fall time, the package model was simulated using an on-chip capacitor of 32nF with a series resistance of 6.3mΩ. Fig. 9 shows the result. The on-chip capacitance decreases the noise substantially. However, around $\pm$ 25 mV of residual high frequency noise exists in the package in the steady state due to the plane resonances. This noise can increase with larger current sources.

From Figs 7,8,9, it is apparent that for fast current edges, the cavity modes in the package planes need to be modeled, if the package alone is considered. Clearly, the on-chip capacitance has a dominant effect on the noise.

VI. Core Noise with Package and PCB

The test vehicle in Fig. 1 including the CBGA package and board layers was modeled and the simulations were repeated by observing the voltage variation between ports 18 and 19. Fig. 10 shows the test board and the port locations for the ideal power supply, decoupling capacitors and solder balls. The position of the CBGA package is also shown in the figure. Three kinds of decoupling capacitors as shown in Table 1 were used on the PCB. In Table 1, R_E and L_E indicate parasitic resistance and parasitic inductance of a decoupling capacitor, respectively.

Table 1 Decoupling capacitors used on the PCB

	C	R_E	L_E
C_1	47nF	0.1Ω	1nH
C_2	10nF	0.1Ω	1nH
C_3	20μF	1Ω	10nH

In Fig. 10, the Vdd planes and ground planes were shorted together using ideal vias at the decoupling capacitor locations. Inductances for the vias and solder balls were not included in this simulation to amplify the plane resonances. The current source shown in Fig. 11 was used for the switching activity. The current source had the same rise time of 1ns as before. However, the fall time and period were changed to 1ns and 50ns, respectively. The goal of the longer period was to enable sufficient time for all the oscillation to die down prior to the next switching event. Three test cases were simulated.

In the first test case, no capacitors were included on the PCB. In the second test case, all the capacitors were assumed to be ideal and included on the PCB. In the final test case, all the PCB capacitors with parasitics were included in the simulation. These test cases were used to understand the effectiveness of the PCB capacitors in suppressing core switching noise. The simulation results for the differential voltage between ports 18 and 19 on the top surface layer of the CBGA package are shown in Fig. 12. Since ideal vias and solder bumps with no inductance were used in the simulation model, the noise contribution in Fig. 12 is produced by the planes.

In Fig. 12, the oscillatory waveform is caused by the radial waves between planes. The oscillation consists of a high frequency component modulated on a low frequency component. From the period of the low frequency oscillations, it is clear that they are caused by the PCB planes. In Fig. 12, as expected, the parasitics of the capacitors increase the noise as compared to ideal decoupling capacitors. However, the capacitor parasitics help in attenuating the steady state noise as compared to a bare PCB, as shown in Fig. 12. Comparing Figs 6 and 12, it is clear that for a 1ns rise time current source, the PCB planes have a significant effect on the core switching noise. Hence for this current source, modeling the PCB planes is far more critical than modeling the package planes. From Fig. 12, it can be seen that the parasitics of the capacitors degrade the performance of ASIC and the steady state noise attenuates faster as compared to the case with no decoupling capacitors.

VII. Core Noise with Package, PCB and On-chip Capacitance

An on-chip capacitance of 32 nF with a series resistance of 6.3mΩ was included into the integrated package and PCB models as discussed in the previous section. The PCB model included the parasitics of the decoupling capacitors. The model was simulated by monitoring the voltage between ports 18 and 19, the results of which are shown in Fig. 13. The inclusion of the on-chip capacitance decreased the 140mV peak noise in Fig. 12 to 80 mV in Fig. 13. In addition, the high frequency oscillations have been smoothened. However, the oscillations after the switching activity which are produced by the PCB planes still exist at a frequency of ~100MHz.

VIII. Core Noise with Package, PCB, On-chip Capacitance and Package Capacitance

Four module capacitors of 32nF each with R_E=0.1Ω and L_E=50pH were next included into the package models. They were connected to the package planes outside the die area at a distance of 5mm from the die edge, one on each side of the die. The via inductance from the capacitors to the package planes were assumed to be negligible. The simulated result is shown in Fig. 13. The inclusion of the module capacitors had little effect on the noise in Fig. 13 which can be attributed to the large lateral inductance of the planes from the capacitor to the ASIC. Since the vias were assumed to be ideal short circuits, the inductance to the PCB capacitor, was smaller as compared to the inductance to the package capacitors. Hence, the package capacitors in Fig. 13 did not reduce the switching noise.

From Figs 12 and 13, it is clear that both the on-chip capacitance and the PCB planes have a significant impact on the core noise. This is for the current sources in Figs 5 and 11. With faster current sources, it has been speculated from Figs 7 and 8 that the package planes can have a significant impact on core noise. To answer this question, the models have been analyzed in the frequency domain in the next section.

IX. Importance of on-chip capacitors

The frequency response of the entire system was computed using the transient simulation models in Figs 2 and 3. The results are shown in Fig. 14. The model included the CBGA package and board plane layers and the board decoupling capacitors. No inductances for vias, C4s and solder balls were included in the model. The simulations were conducted with an on-chip capacitance of 32nF and series resistance of 6.3mΩ. The simulation was next repeated without any on-chip capacitor. The self-impedance between ports 18 and 19 is shown in Fig. 14. The figure shows three curves namely, i) the response of only the on-chip capacitor, ii) the response without the on-chip capacitor and iii) the response of the entire system. In Fig. 14, the second peak for the entire system response is caused by the chip-package resonance caused by the on-chip capacitance resonating with the planes and decoupling capacitors. The frequency at which this occurs is the intersection point between curves i) and ii) as shown in Fig. 14.

From Fig. 14, beyond 500 MHz, the on-chip capacitance dominates the frequency response and hence completely suppresses all the plane resonances caused by the package. From Fig. 14, it can be concluded that the bandwidth to be supported by the package and board is from DC – 500MHz for the test vehicle in Fig. 1.

Assuming the same cross section, the self-impedance frequency response between ports 18 and 19 for various on-chip capacitors is shown in Fig. 15.

The chip-package resonance can be clearly seen in all the cases where the resonance shifts to a lower frequency as the on-chip capacitance is increased. For an on-chip capacitance of 500nF, the chip-package resonance occurs at a very low frequency indicating that the bandwidth to be supported in the package and board is < 190MHz. This is shown in Fig. 16, where the chip-package resonance frequency has been plotted for various on-chip capacitances using the test vehicle described in Fig.1. From Fig. 15, it is clear that since the package planes have resonances above 1GHz, they are completely suppressed by the on-chip capacitance, if the on-chip capacitance exceeds 30nF.

The current ASIC trend of large on-chip intrinsic and added thin-oxide decoupling capacitance will continue into the future. This being the case, the package can be modeled as an inductance network by accounting for only the vertical via inductances and can be connected to a PCB network containing all the plane resonances, as described in this paper. The model also includes the C4 and solder ball inductances. This modeling approach is valid for future ASICs, as illustrated in Fig. 17.

X. Conclusion

In this paper a CBGA package on a test board was simulated for computing the core switching noise. Initially, the core noise produced by the CBGA package alone was investigated. It was observed that the inductance of vias, C4s and solder balls contributed the maximum towards core noise and the effect of the package planes was insignificant for the 0.5μm CMOS process used in this paper. However, it was also observed that the effect of the plane resonances in the package dominated the response as the technology moved towards higher performance. Next, the entire test vehicle including the CBGA package and board was modeled and the effect of decoupling capacitors on the noise was investigated. It was seen that the parasitics of on-board decoupling capacitors degraded

the performance of the system. Finally, the frequency response of the test vehicle was analyzed with various on-chip capacitors. The simulation results showed that on-chip capacitors completely dominated the response beyond 190MHz (for on-chip capacitance of 500nF), suggesting that the package planes have little contribution towards core switching noise. Based on this observation, a method that simplified the models was suggested that accounted for the package vertical inductances and the PCB lateral resonances and vertical inductances.

XI. Acknowledgements

This work was supported by the Semiconductor Research Corporation under contract number 99 – NJ – 735.

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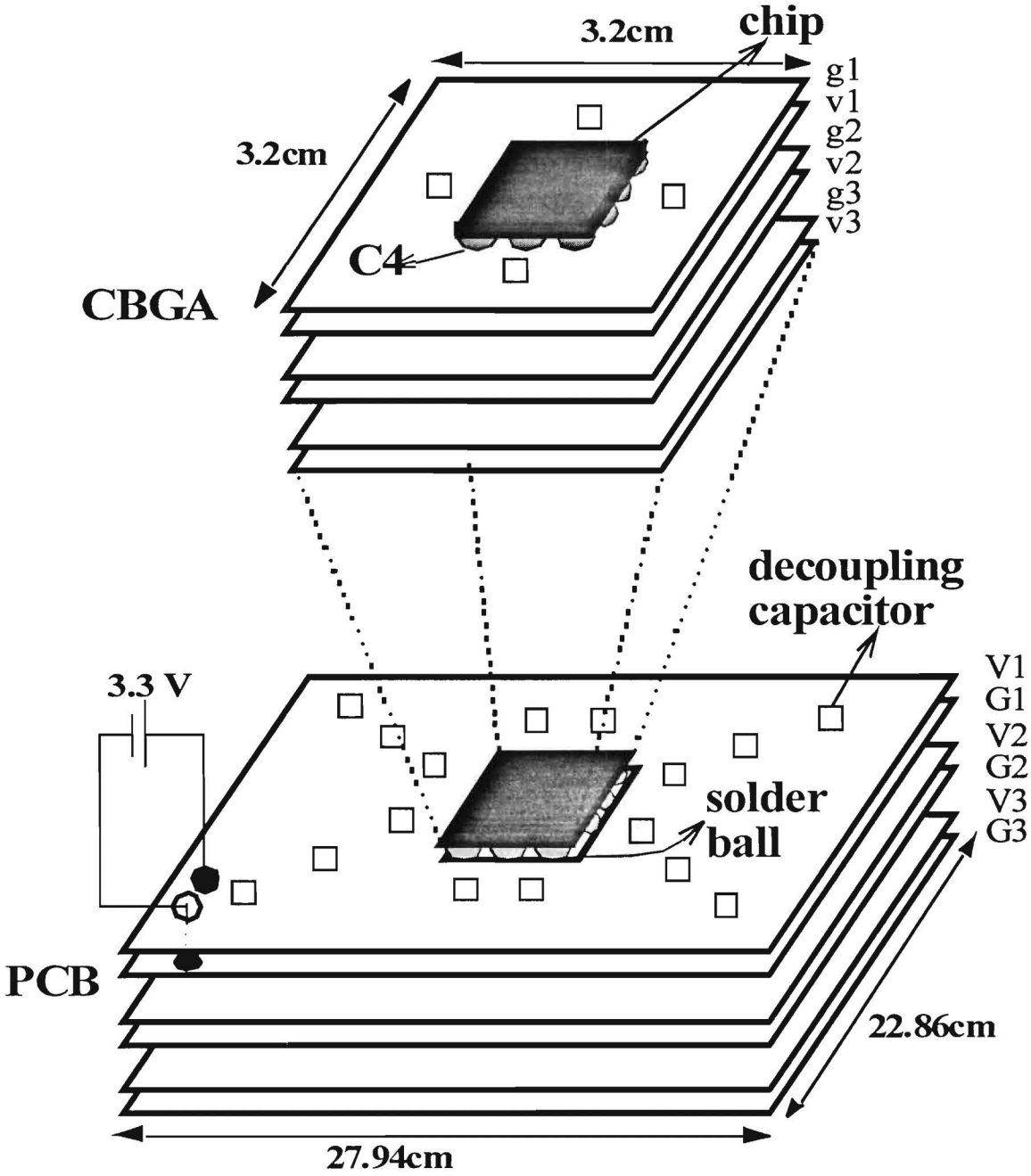


Fig. 1 Core Switching Noise Test Vehicle

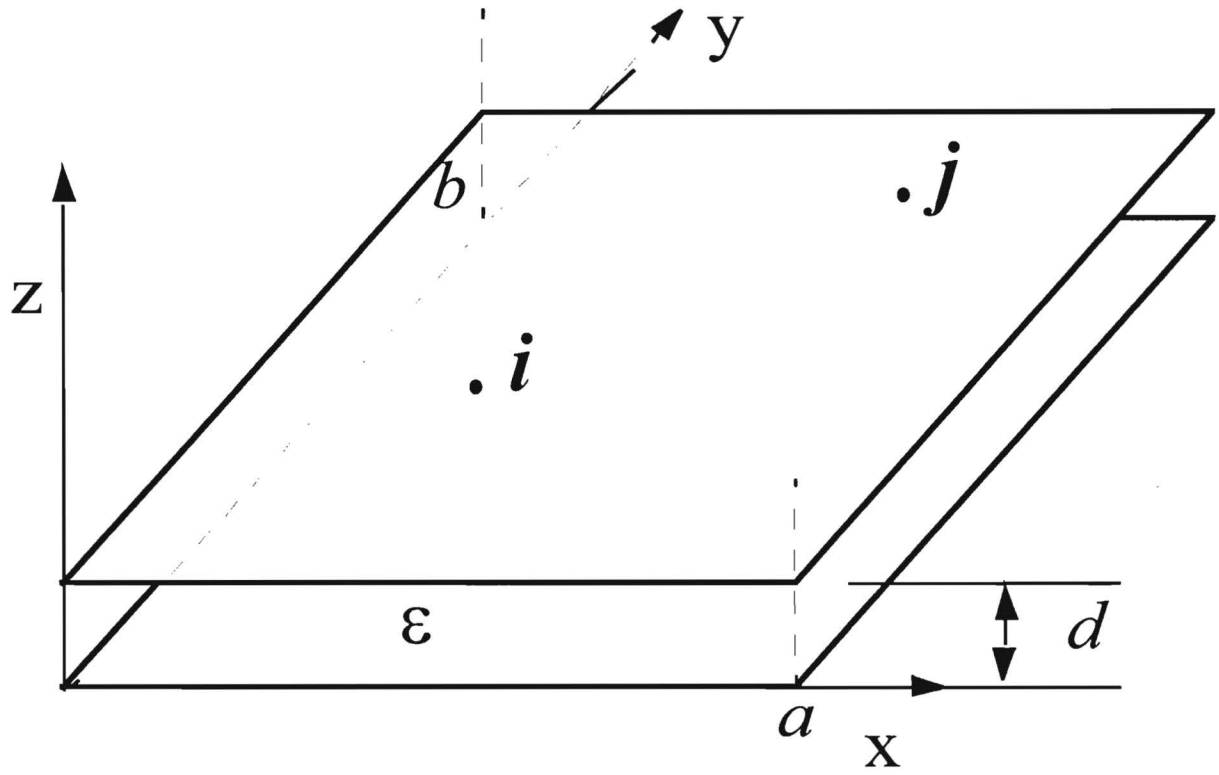


Fig. 2 Plane Pair

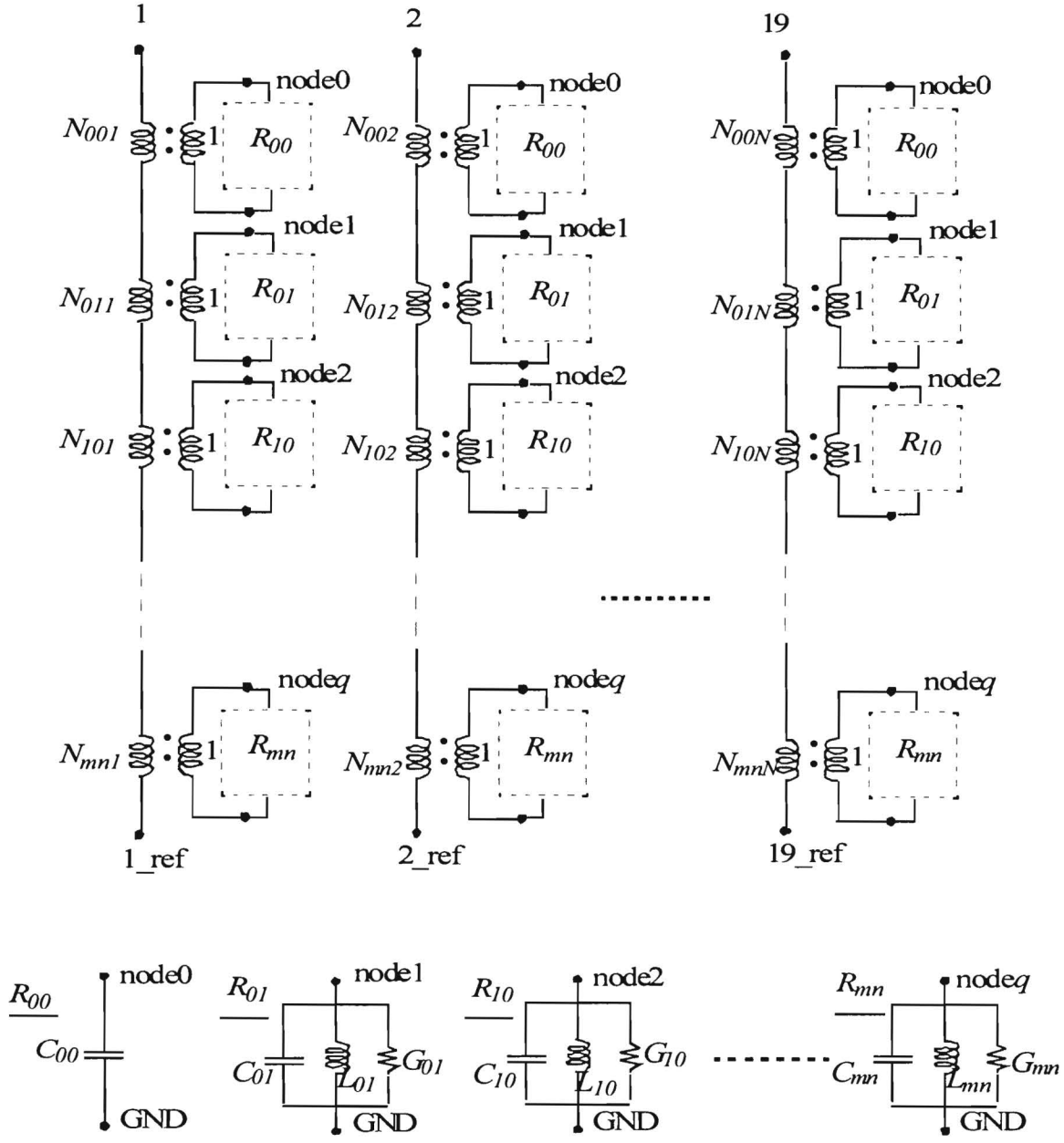
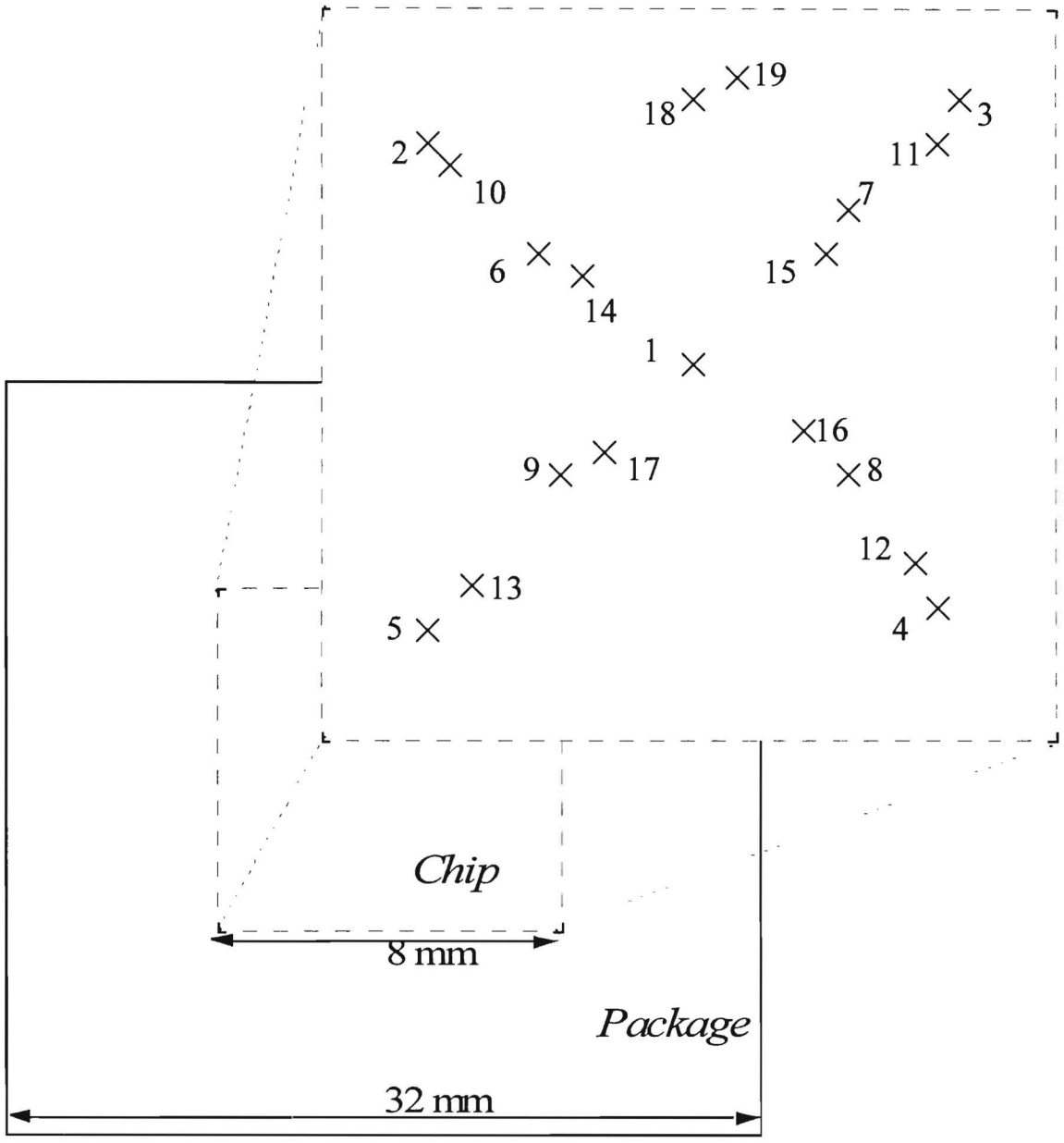


Fig. 3 Equivalent Circuit for a Plane Pair.



1-5 : ports for ground vias connected between C4s and g1 through g3
6-9 : ports for Vdd vias connected between C4s and v1 through v3
1, 10-13 : ports for ground vias connected between solder balls and g3
14-17 : ports for Vdd vias connected between solder balls and v3
18, 19 : ports for differential voltage measurement, ground on g1 and Vdd on v1

Fig. 4 Port locations on the package

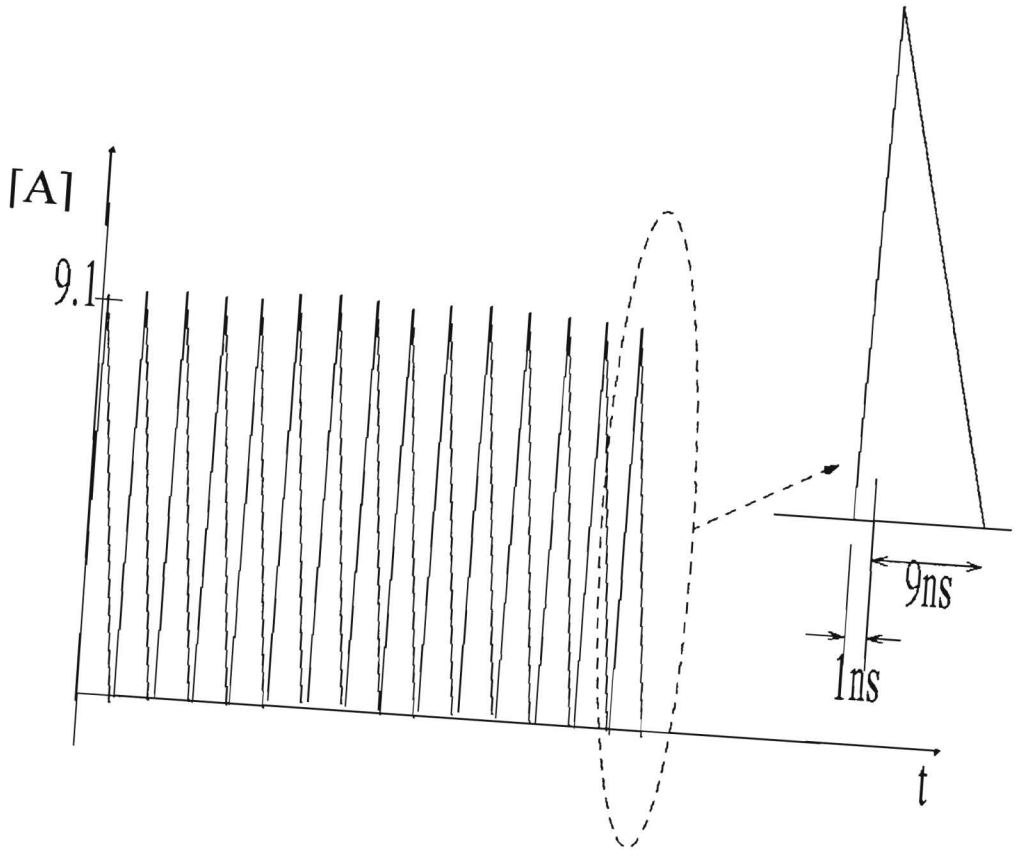


Fig. 5 Current Source 1

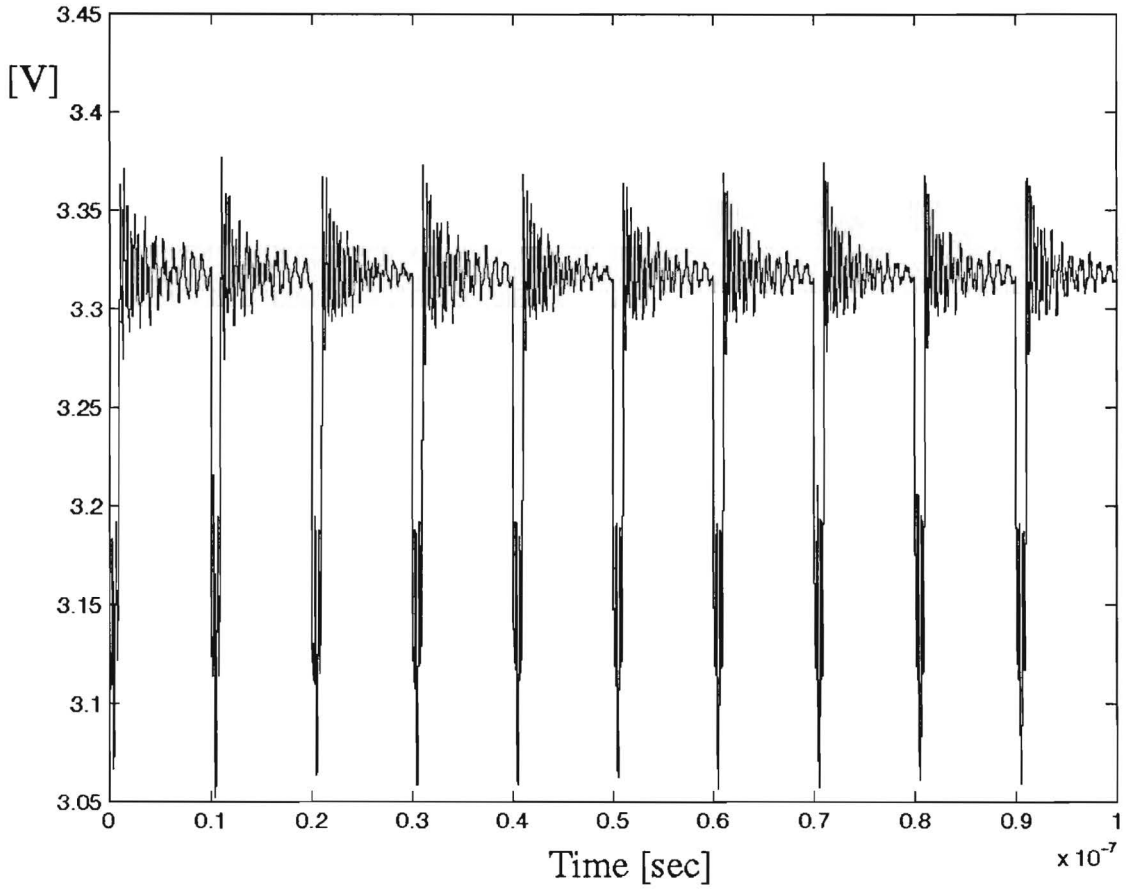


Fig. 6 Core noise due to package : t_r = 1ns, t_f = 9ns

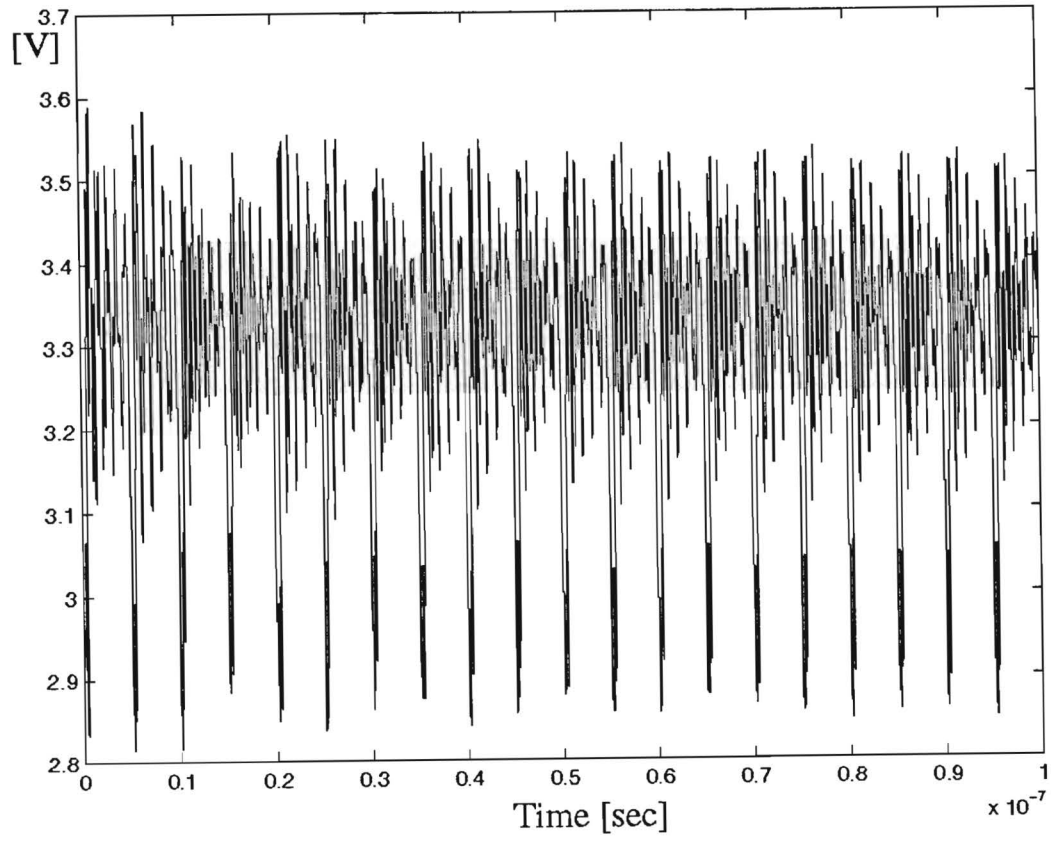


Fig. 7 Core noise due to package only: $t_r = 0.5$ns, $t_f = 4.5$ns

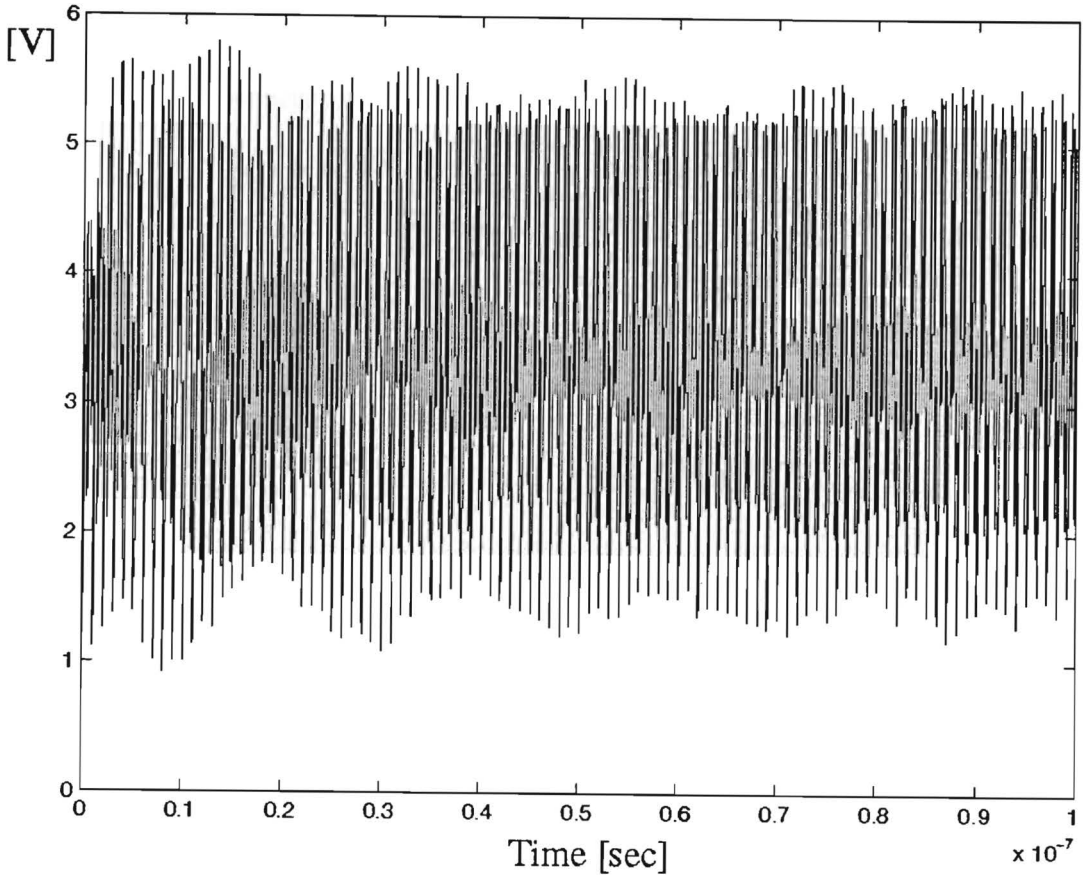


Fig. 8 Core noise due to package only: $t_r = 0.1$ns, $t_f = 0.9$ns

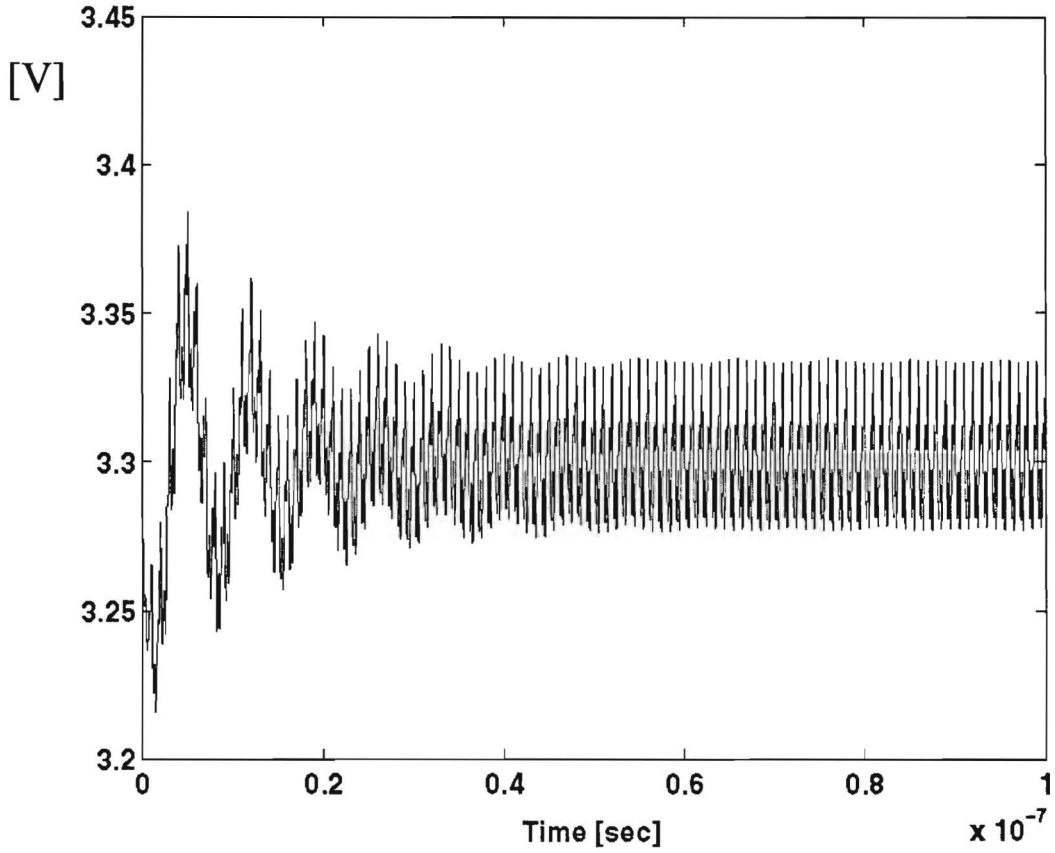
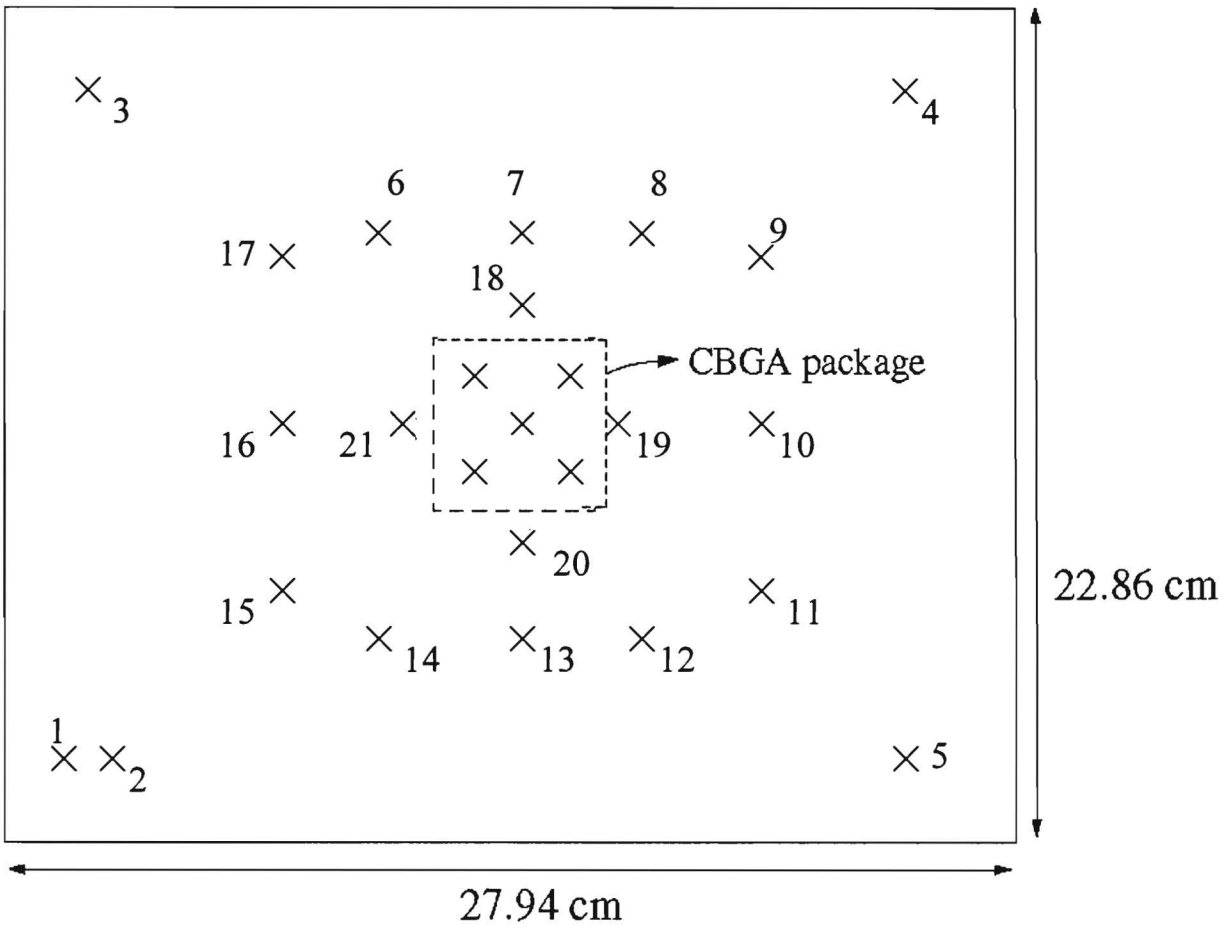


Fig. 9 Core noise due to package with on-chip capacitance



1: Port for the ideal power supply
2-17: Ports for decoupling capacitors of types C_1 andC_2
18-21: Ports for decoupling capacitors of type C_3

Fig. 10 Port locations on the PCB

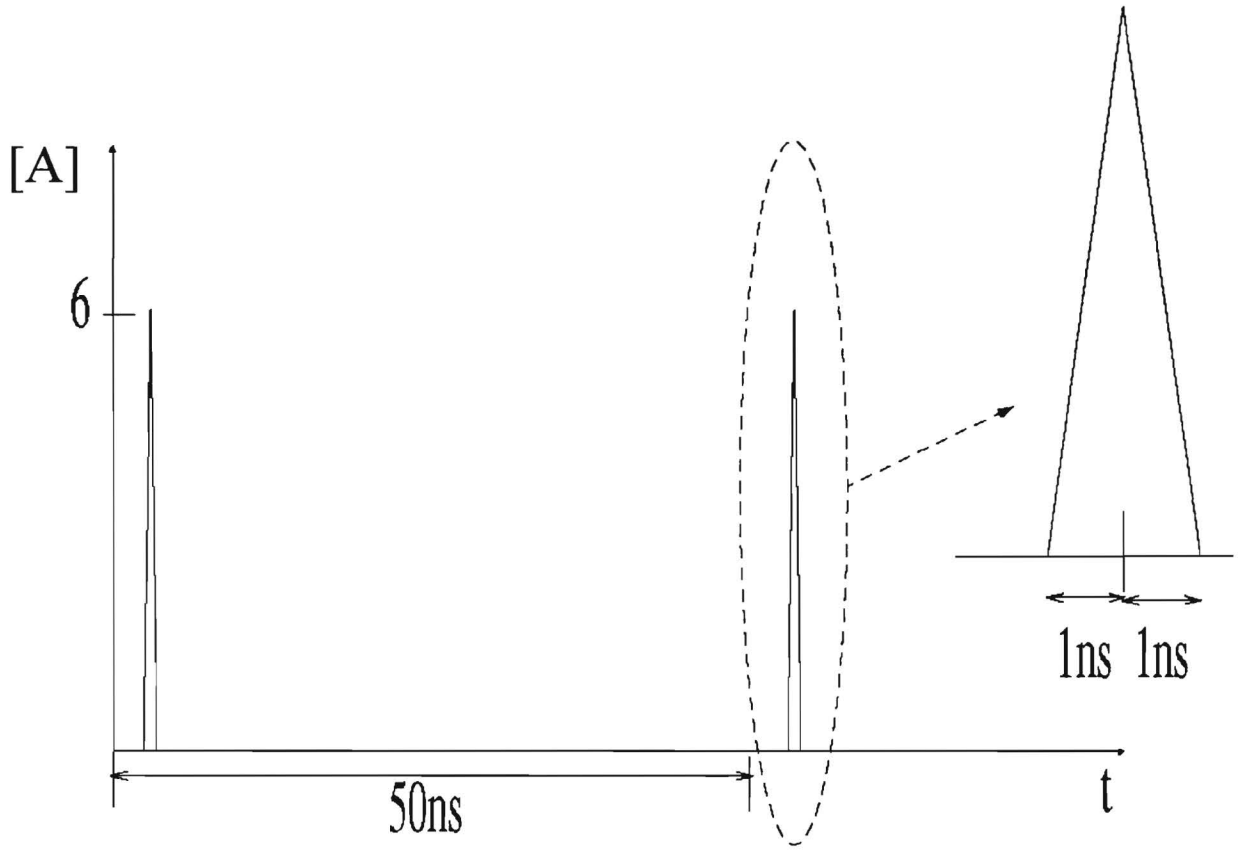


Fig. 11 Current source 2: t_r=1ns, t_f=1ns

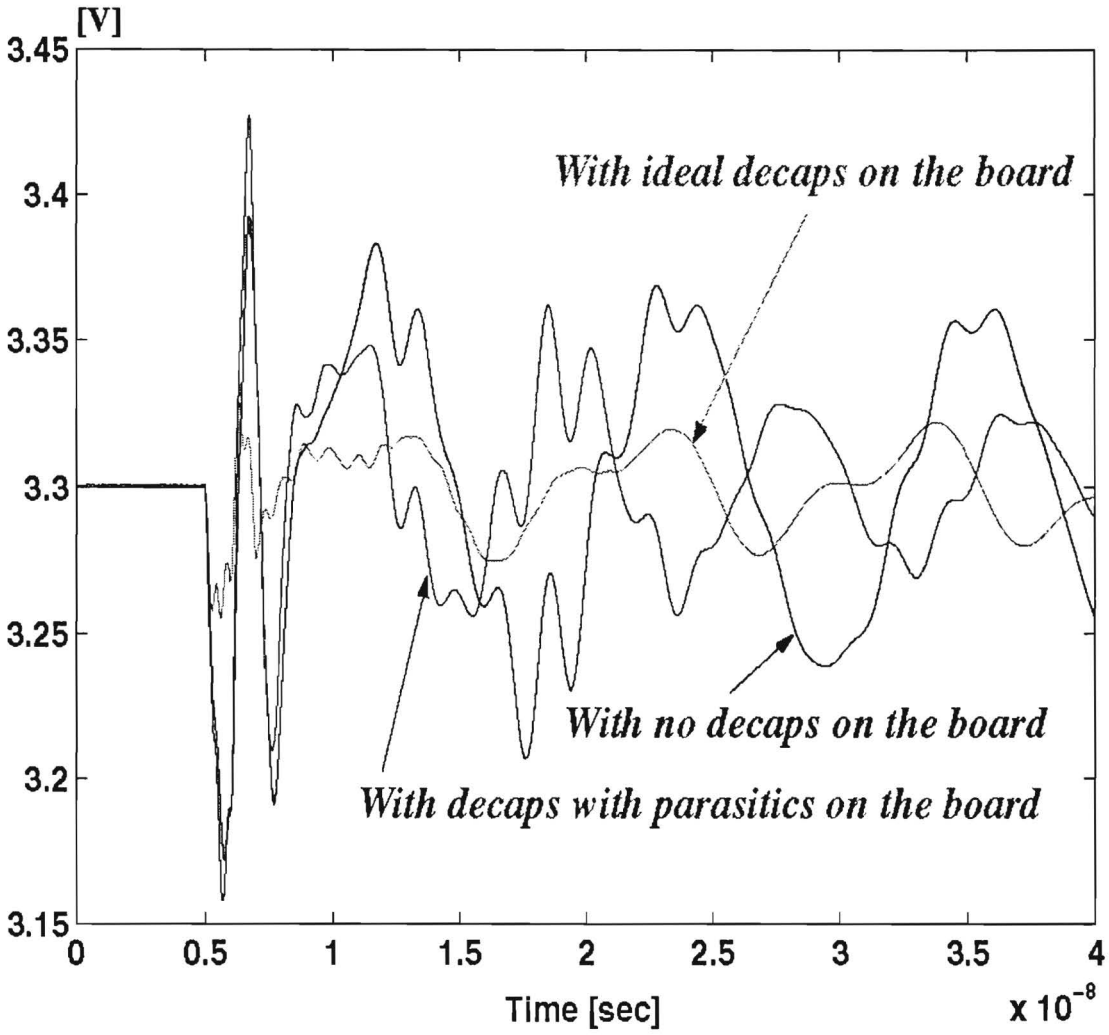


Fig. 12 Core noise with the package and PCB

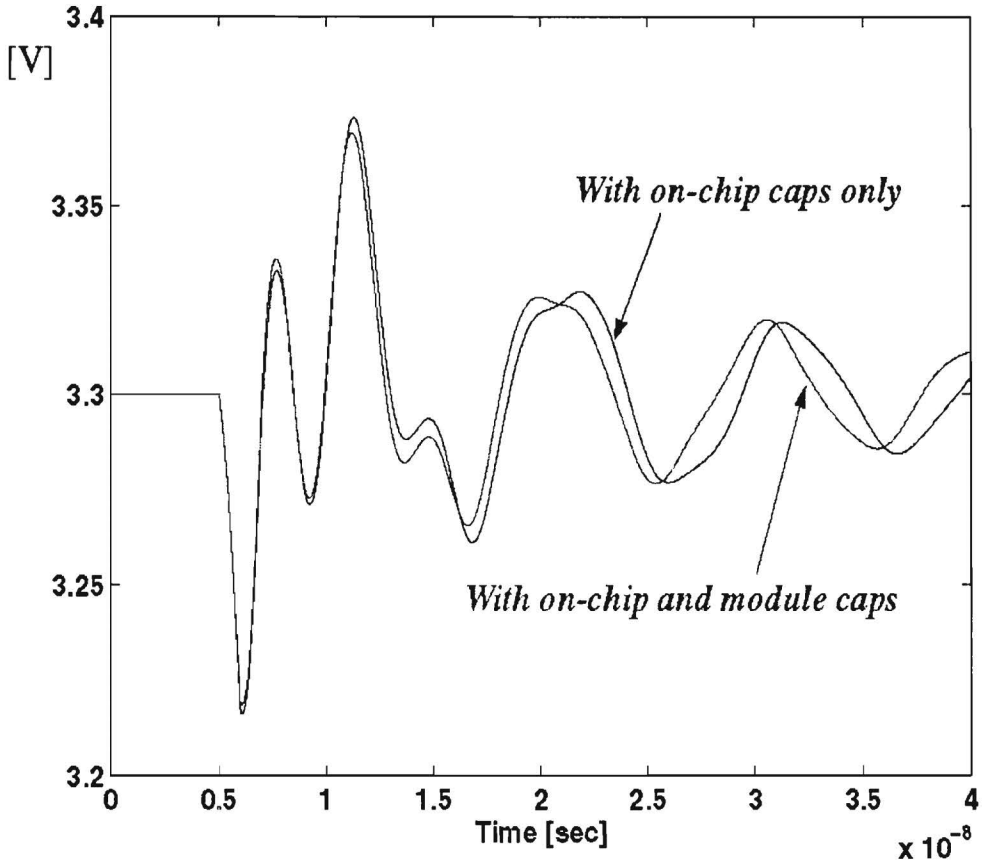
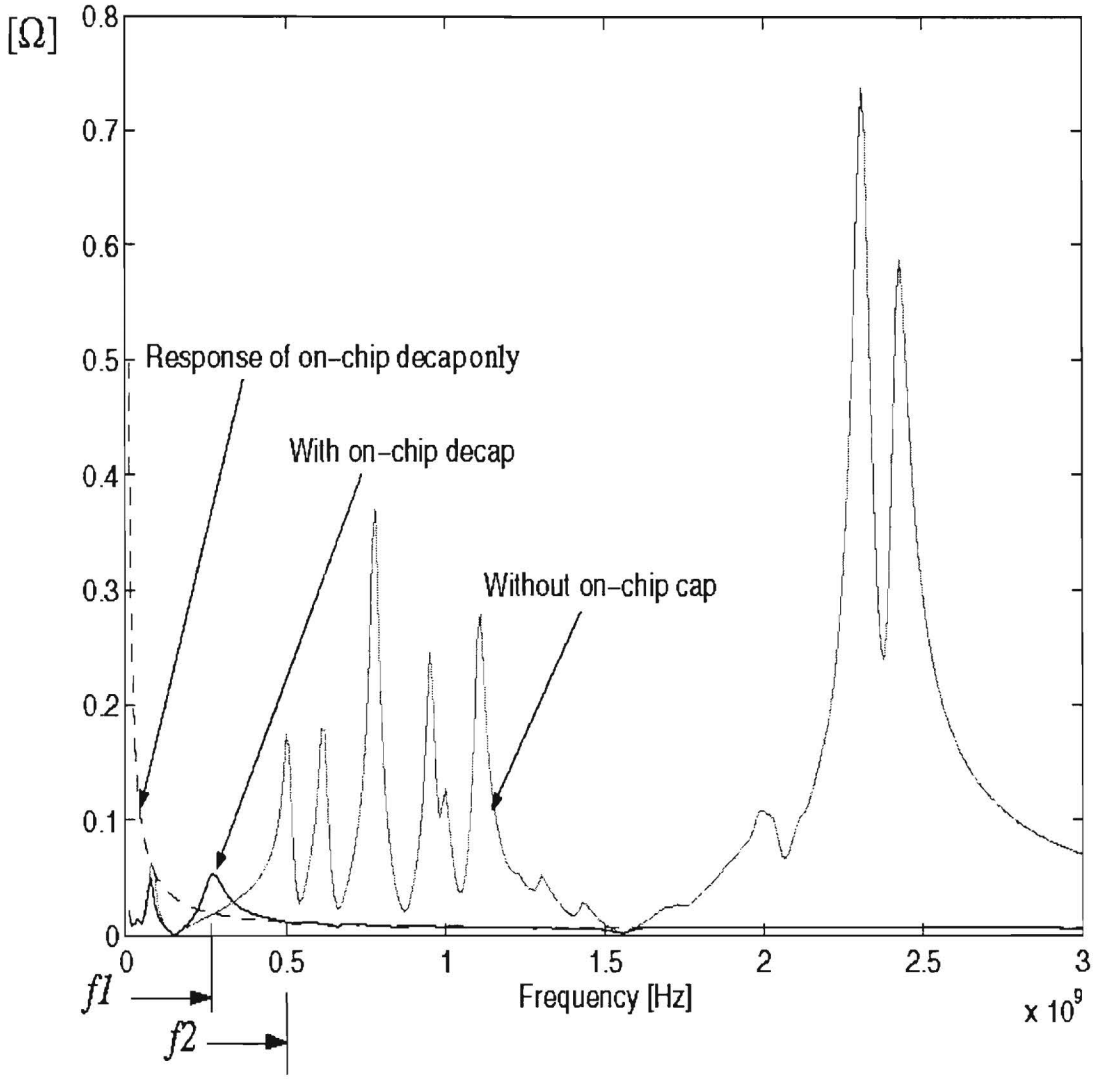


Fig.13 Core noise for the test vehicle



f1: chip-package resonance, *f2*: bandwidth to be supported

Fig. 14 Chip-package resonance

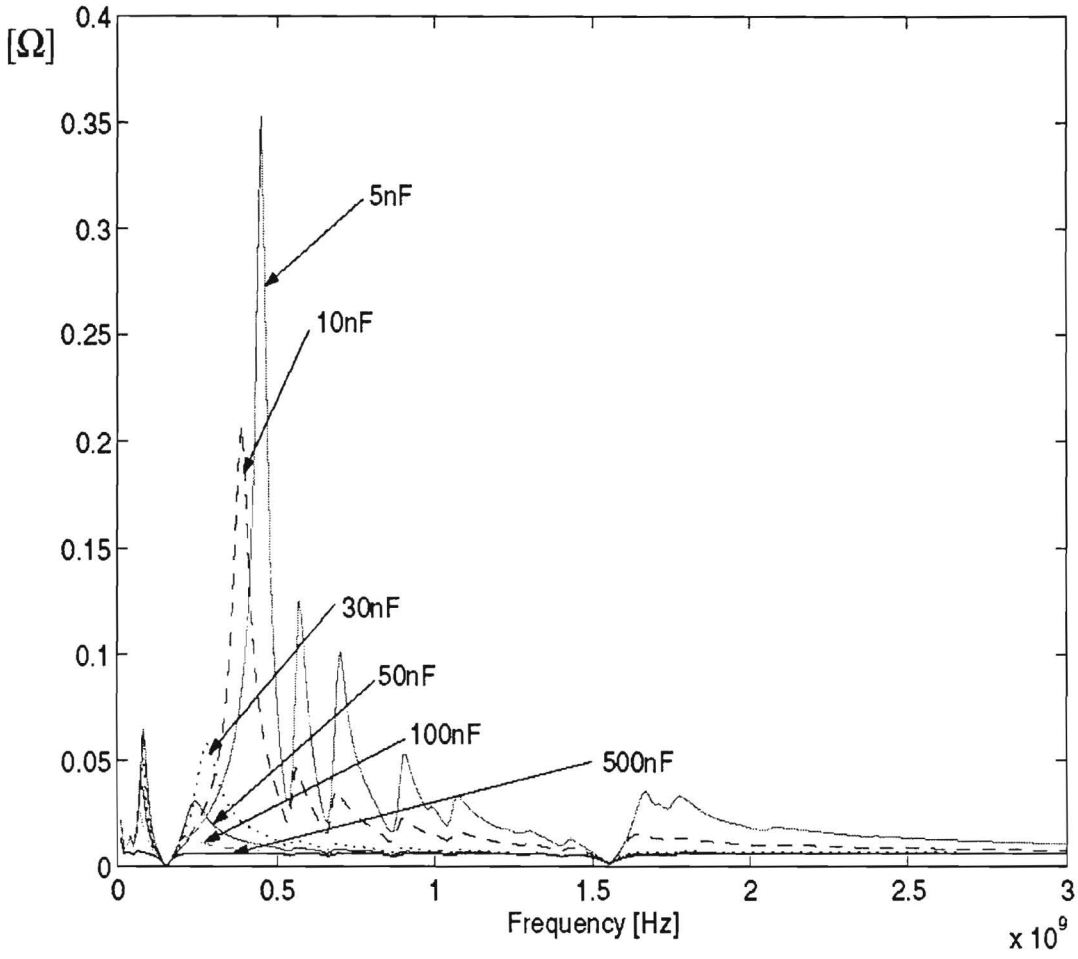


Fig. 15 Chip-package resonance shifts with larger on-chip capacitance values

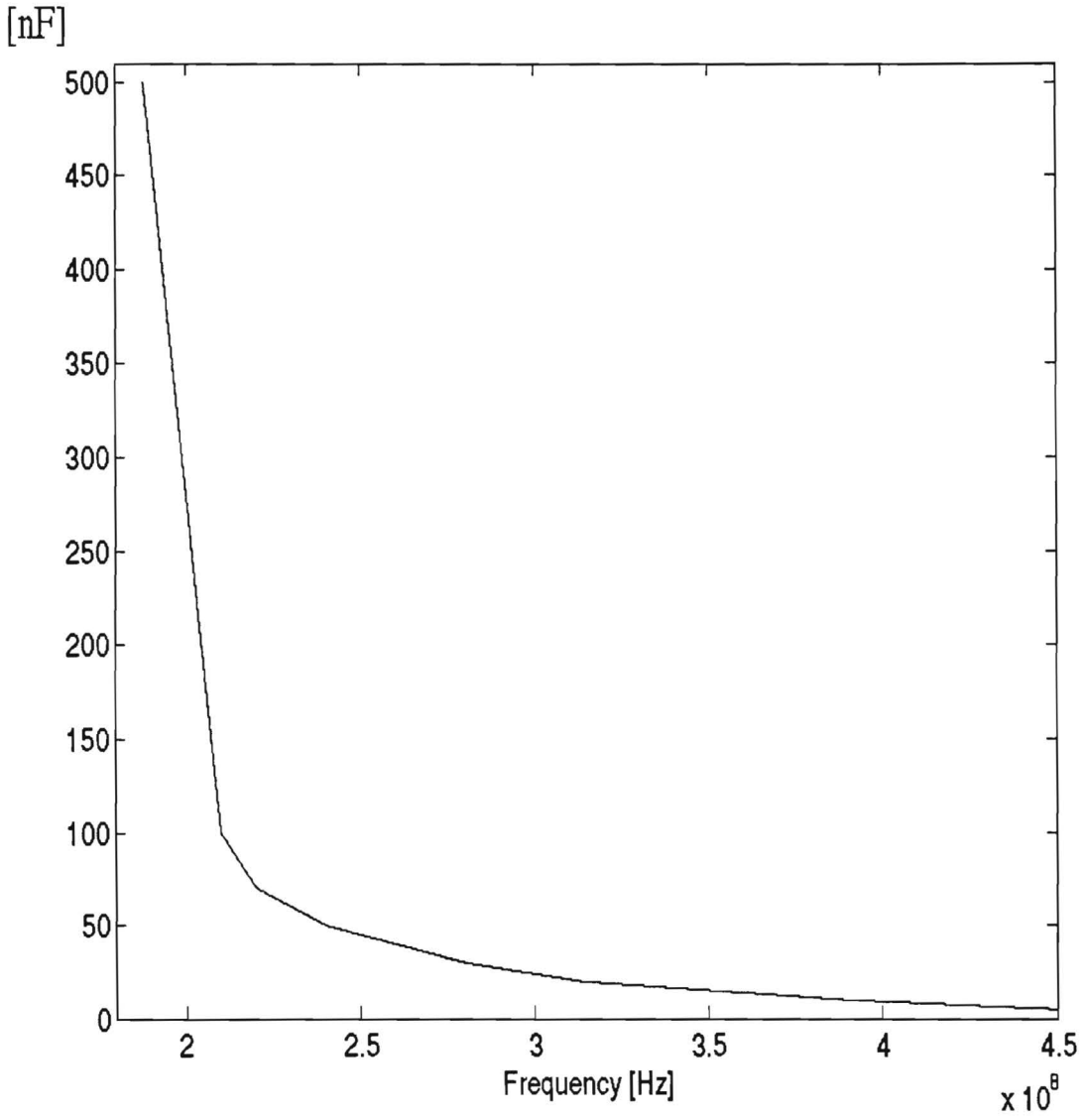


Fig. 16. On-chip capacitance vs. chip-package resonance

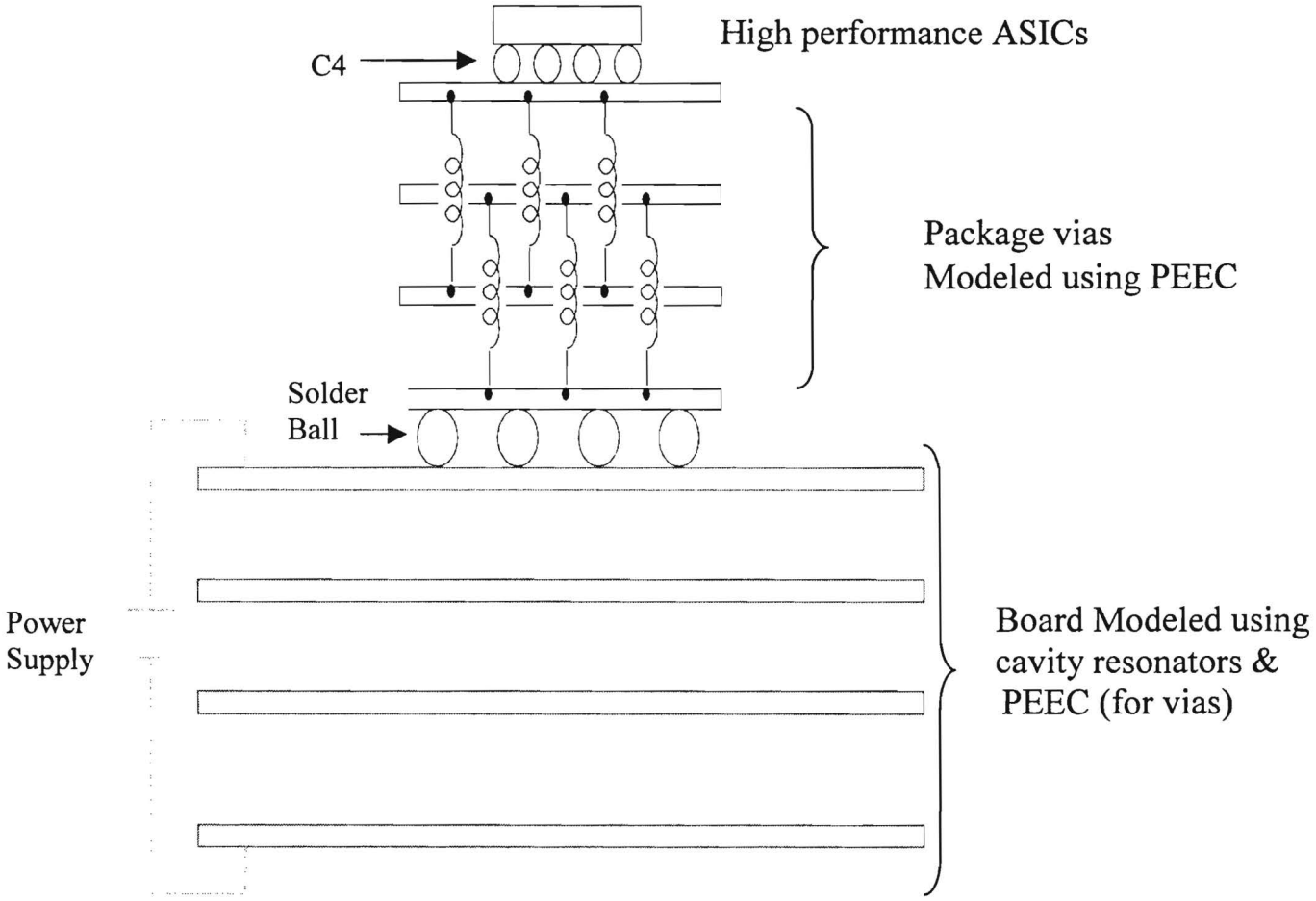


Fig. 17 Modeling of the package and board for future generation

E-21-F05 #5

I. Deliverable Name, Associated Task ID and Task Title

Deliverable Name: Algorithms for simulating I/O noise in multi-layered packages for transmission lines in the presence of non-linear drivers

Associated Task ID: The Design of the Power Delivery System for Next Generation Gigahertz Packages

Task Title: The Design of the Power Delivery System for Next Generation Gigahertz Packages

II. Summary/Abstract

Digital devices play an important role in Signal Integrity analysis. Commercial transistor level driver models are usually very complicated and require lots of memory for simulation. Therefore simulations involving these drivers take up huge memory and time. The objective of the research work is to model non-linear active digital drivers by using less memory and increase the simulation speed by a factor of 10X – 100X as compared to transistor level models. In addition to these objectives, the developed models should capture sensitive effects such as cross talk, simultaneous switching noise and reflected noise without any compromise on accuracy.
This report discusses a systematic method for developing behavioral models of transistor level digital circuits. These models have been combined with models of linear networks for computing power supply noise and cross talk.

III. Technical Results and Data

Modeling Methodology: The method is best described using an example provided by IBM which is the encrypted driver "bt3350pd_c.inc" available in a spice format. The idea behind the modeling technique is to get a relation between the output current I_o and the output voltage V_o of the driver for a given input pulse. Figure 1 shows the driver connected to a supply voltage Vdd of 3.3 volts, at the output of the driver a voltage source is connected and the current is monitored at the output of the driver.

The output current I_o of the driver can be expressed in terms of the output voltage using the relation $\boldsymbol{I_o(t) = w_1(t).\ F_1(t) + w_2(t)\ .F_2(t)}$, where $w_1(t)$ and $w_2(t)$ are time varying weighting functions and $F_1(t)$ and $F_2(t)$ are functions that relate the output current to the output voltage when the driver input is HIGH and LOW respectively. The functions $F_1(t)$ and $F_2(t)$ can be evaluated by connecting a piece wise linear voltage source at the output of the driver and examining the output current for both driver input HIGH and LOW respectively, as shown in Figure 2,. The rise times of the voltage should be around the rise time of the input pulse. This allows the determination of the functions F_1 and F_2 accurately.

The functions F_1 and F_2 can be expressed as $A.V_o+B$ and $C.V_o+D$ respectively, where A, B, C, D are constants and V_o is the output voltage. To determine the time varying weighting functions, two equations are required. Therefore, the driver output is terminated with two different loads for measuring the driver output current and voltage. The two loads that are usually preferred are Impedance (usually the load the driver drives) and impedance of the voltage source (usually the power supply of the driver). Once the values of the current and voltage at the output of the driver are obtained, the following relation can be used to determine the weighting functions

$$\begin{bmatrix} w_1 \\ w_2 \end{bmatrix} = \begin{bmatrix} F_{1a} & F_{2a} \\ F_{1b} & F_{2b} \end{bmatrix}^{-1} \begin{bmatrix} I_a \\ I_b \end{bmatrix}$$

In the above equation, F_{1a} and F_{2a} are determined by the first load and F_{1b} and F_{2b} are determined by the second load. Similarly I_a and I_b are the output currents for the two loads. For one complete cycle the weighting functions are as shown in figure 3.

Validations: Once the weighting functions are calculated, the driver can be terminated with different loads at the output to validate the modeling methodology for load independence. Figure 4 shows the driver

connected to a 100 ohm resistor, the input pulse to the driver has a rise and fall time of 1 ns and a period of 20 ns. The voltage across the resistor has been modeled. The blue curve is from the model and the red curve is from the encrypted IBM macro-model. Figure 5 shows the driver with 25ohm resistive termination. Again, accurate match is obtained between the (blue) modeled output and the (red) transistor level IBM model.

Spice Macro-Model: The results described are from MATLAB. To ensure ease of use, the modeling methodology described can be captured using a spice macro-model. The spice macro-model contains voltage dependent voltage sources and voltage dependent current sources. A brief description of the spice net-list for the above model is shown below:

```
*** Spice macro-model for the IBM driver

**** Sub-circuit call for the driver
.subckt driver out gnd

**** Defining the weighting functions as PWL voltage source
Vw1 1 gnd PWL <.V1 T1 V2 T2.....>
Vw2 2 gnd PWL < V1 T1 V2 T2 .....>

**** Defining the Function F1 with a voltage dependent voltage **** source
E_fun1 n1 gnd out gnd 1
.....
.....
**** Defining the Function F2 with a voltage dependent voltage **** source
E_fun2 n2 gnd out gnd 1
.....
.....
**** Driver output node with a volatge dependent current
**** source
F_fun1 out gnd .....
.....
. ENDS (driver)
```

Spice Macro-Model validations: To validate the accuracy of the spice macro-model, the driver was connected to transmission lines of different impedances to verify load independence. Figure 6 shows the driver connected to a 25ohm transmission line which is terminated by a 10 pF capacitance. The driver is given an input pulse of 1ns rise time and a period of 20 ns. The voltage across the capacitancor has been monitored. The red curve is from spice macro-model and the yellow curve is from the IBM transistor model. The results match very accurately. The spice model took 4 seconds where as the encrypted transistor model took 84 seconds for simulation, resulting in a speed-up of 20X.

The second validation used the same scenario, but the transmission line had a characteristic impedance of 200 ohms. Figure 7 shows the voltage across the 10 pF capacitancor, red curve is from spice macro-model and yellow is from the transistor level IBM driver model.

Figure 8 shows the scenario where 3 drivers are driving 3 transmission lines of 50 ohm impedance. Two drivers were given an input pulse of 1ns rise time and 20 ns period and the third driver was kept quiet. The transmission lines were all terminated with a 10pf capacitance. The voltage across the capacitor of the quiet transmission line was monitored to check the accuracy of the model for capturing the cross-talk waveforms. The results show very good correlation.

Extension of the method to Multiple ports: The examples described earlier only described a 2-port circuit with the driver having only an input and output port For capturing effects such as power supply noise, the Vdd and Gnd ports should also be included in the functions F_1 and F_2. The functions F_1 and F_2 relate output current to both output voltage and voltage at port Vdd. Therefore, F_1 and F_2 are of the form $A.Vdd +$

B.Vout + C, where A, B and C are constants. Accordingly in the spice macro-model the functions F_1 and F_2 should be modified so that they can capture the change in supply voltage Vdd. Figure 9 shows a test case where the driver was connected to a plane pair with six ports. The models for the planes were developed as part of the earlier deliverables in this project.

The driver was connected at port 1 and the transmission lines were terminated at port 6. The power supply was connected at port 4. Figure 10 shows the voltage across the capacitor and the plane noise at ports P1 and P3. The results between the spice macro-model and the transistor model correlate very well.

Conclusion: The modeling methodology described used piece wise linear approximation functions for capturing the non-linear characteristics of the driver. This modeling methodology has many advantages such as: 1) Accuracy. This was shown through good correlation with the transistor level model, 2) Speed. The spice macro-model was 20X to 200X faster than the transistor level models depending on the type of termination, 3) Low memory. The macro-model required less memory compared to the transistor level model and 4) Compatibility. The models were compatible with the plane models developed as part of this project.

IV. Figures

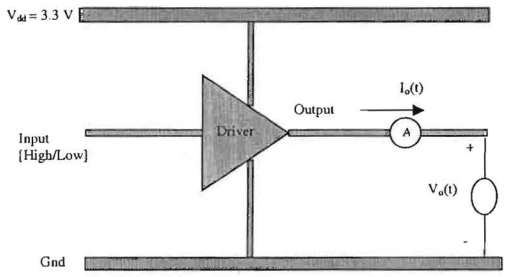


Figure 1 IBM driver

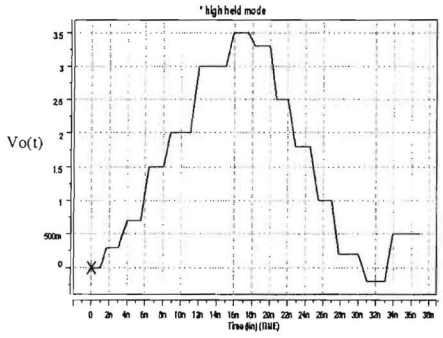
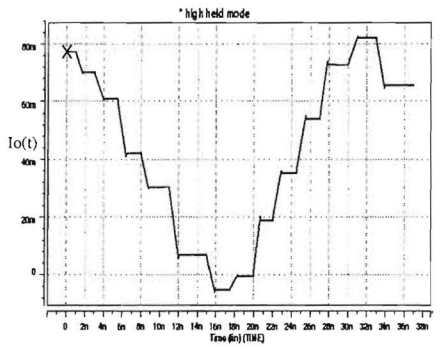


Figure 2 voltage source at the driver output



Driver output current for Input HIGH

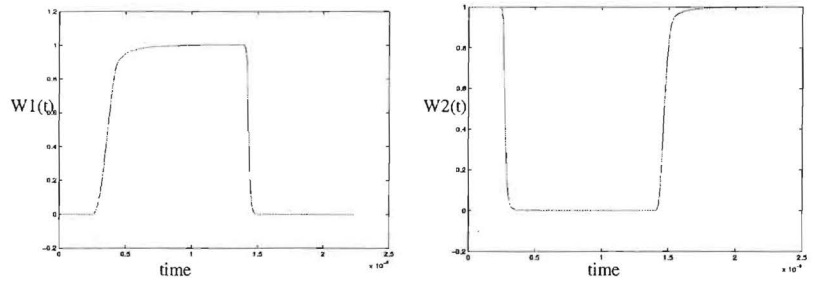


Figure 3 Weighting functions

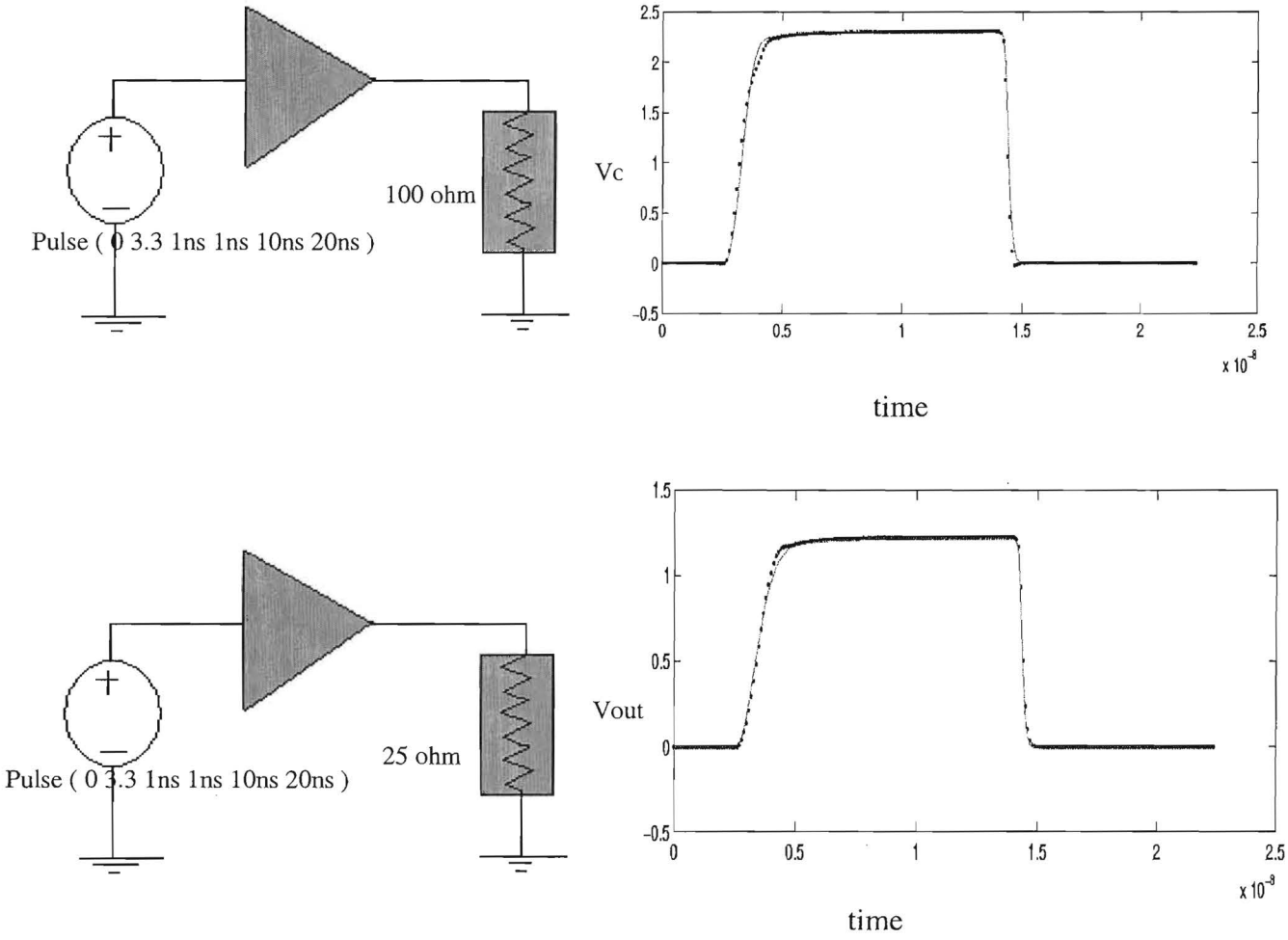


Figure 4: Validation with 100 ohm resistance and Figure 5: Validation with 25 ohm resistance

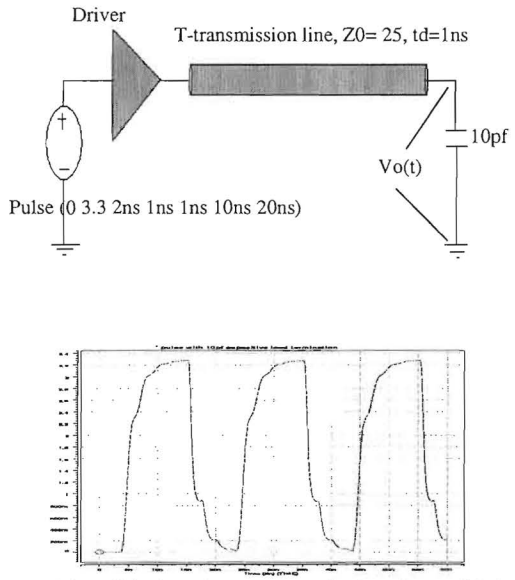


Figure 6 Spice model validation for a transmission line of 25 ohm impedance

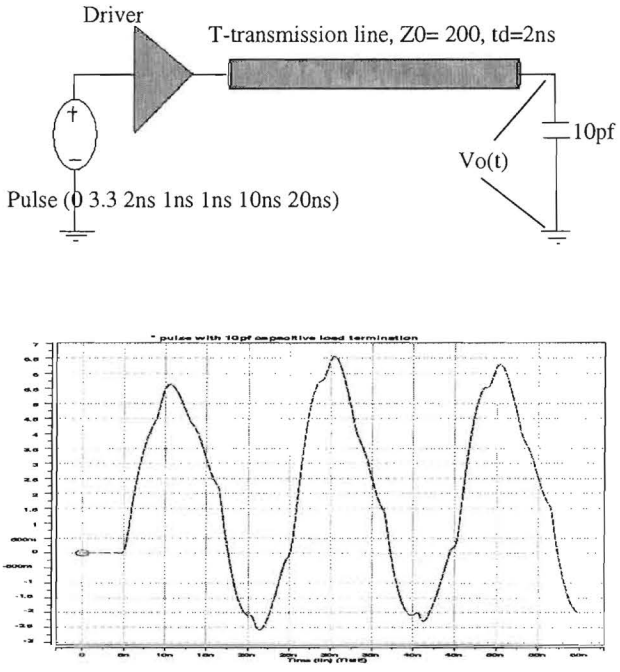


Figure 7 Spice model validation for a transmission line of 200 ohm impedance

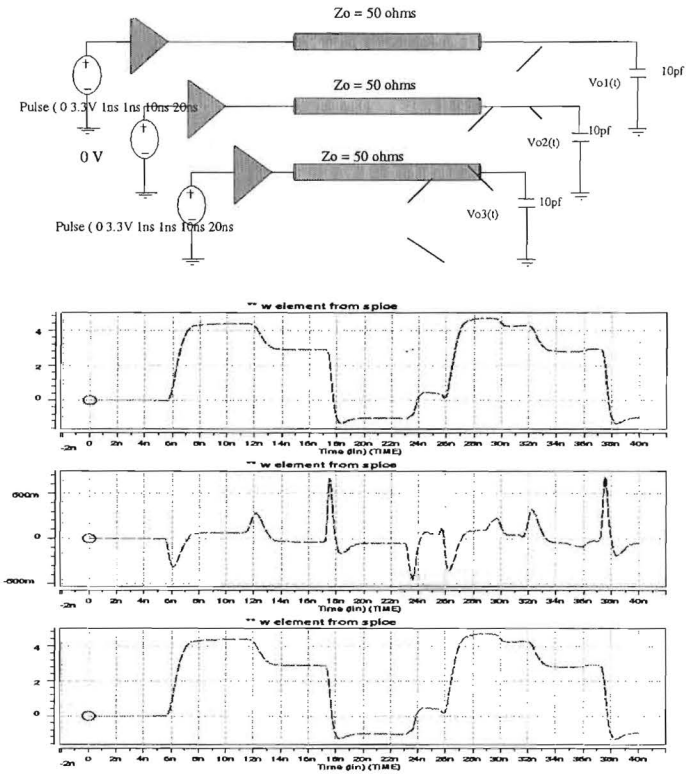


Figure 8 Cross talk validation

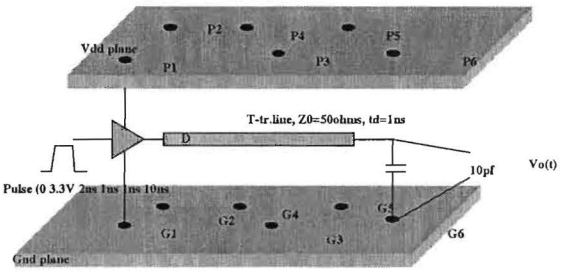


Figure 9 Driver connected to a plane pair

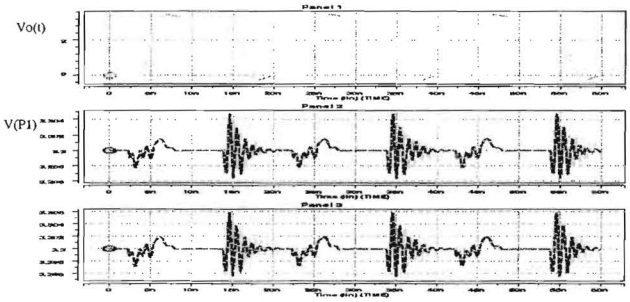


Figure 9: Driver Connected to a Plane Pair and Figure 10: Waveforms of the power supply noise