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SPONSORED PROJECT INITIATION

Date: June 9, 1977

Project Title: Compressor Research Facility System Review and Software Design

Project No: A-2000

Project Director: Ms. E. W. Martin

Sponsor: Cadre Corporation; Atlanta, Ga. 30340

Agreement Period: From 5/18/77 Until Approx. 7/17/77

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Amount: \$20,377

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Sponsor Contact Person (s):

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(thru OCA)

Defense Priority Rating: None

Assigned to: Radar Instrumentation Laboratory (School/Laboratory)

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Date: November 1, 1977

Project Title: Compressor Research Facility System Review and Software Design

Project No: A-2000

Project Director: Ms. E. W. Martin

Sponsor: Cadre Corporation; Atlanta, Ga. 30340

Effective Termination Date: 7/18/77 (Contract Expiration)

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- ☐ Final Fiscal Report
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NOTE: Follow-on project is A-2053.

Assigned to: Radar Instrumentation Laboratory. (School/Laboratory)

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ENGINEERING EXPERIMENT STATION
Georgia Institute of Technology
Atlanta, Georgia 30332

FINAL TECHNICAL REPORT
on EES/GIT Project A-2000

COMPRESSOR RESEARCH FACILITY
SYSTEM REVIEW AND SOFTWARE DESIGN

Edited by

E. W. Martin

Contributors

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Prepared For

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2845 Clearview Place
Atlanta, Georgia 30340

under

Standard Industrial Agreement 5-18-77

JULY 1977

Standard Industrial Agreement
dated 5-18-77
CADRE CORPORATION
2845 Clearview Place
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A-2000 Final Technical Report
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

COMPRESSOR RESEARCH FACILITY
SYSTEM REVIEW AND SOFTWARE DESIGN

edited by

E. W. Martin

ABSTRACT

This Final Technical Report summarizes efforts conducted under EES Project A-2000. The goal of the investigation was for EES to familiarize themselves with the Compressor Research Facility being built by Cadre Corporation and to identify specific areas in which EES personnel could provide research and development assistance to Cadre. Subsequent to review of the current Cadre Computer hardware and software capabilities and requirements, EES began descriptions of several software system modules which could be supplied by Georgia Tech. The result of this effort was the definition of two tasks to be proposed by EES as follow-on work which would support the total CRF endeavor. The Task definitions are herein contained.

Monitor Computer Software Development Task

A description of and manpower requirements for seven tasks on the monitor computer in the CADRE Corporation's Compressor Research Facility are described below. The tasks are: (1) ADDS 880 CRT Interface, (2) Data Link Study, (3) Timing System, (4) Command String Processor and Graphics Preprocessor, (5) Real-Time System, (6) Reports and Documentation, and, (7) Miscellaneous tasks. Figure 1 is a simplified critical path method network which shows the relationship between the tasks.

It is understood in the following discussion that all software design will result in a Software Design Document which must meet with CADRE's approval before any coding begins. In addition, final documentation will include a set of detailed design notes, copies of all current programs with their internal documentation, a test plan, and a user's guide, all of which will conform to CADRE's specifications.

1. ADDS 880 CRT Interface Task

The current Modcomp handler being used with the ADDS (Applied Digital Data Systems) 880 CRT assumes that it is a conventional teletype and does not permit the usage of special features on the machine, such a page mode, protected fields, and automatic spacing. CADRE would like to implement these special features for test operator programs. The purpose of this task is to supplement Modcomp's handler with a subroutine interface which will allow the operator to use these special features on the ADDS 880. The page mode, for example, must permit local editing of the contents of the CRT screen; that is, several changes can be made on the screen before any of the data is transmitted back to the operating program.

Two and one-half man-months of effort will be required to complete the subroutine interface task. This time can be broken into sub-tasks as follows:

1. Two man-weeks to design the subroutine interface;

2. Four man-weeks to code the interface;
3. Two man-weeks to test the handler;
4. Two man-weeks for documentation.

2. Data Link Study Task

The purpose of the data link study is to determine the best method for implementing intertask communications between the various Modcomp computers on the system. The need arises because all of the messages for the four Modcomp II computers with shared memory come through the same data link.

Two types of communications should be considered:

1. High-priority messages (such as alarm conditions), which need to cause an immediate change in the control flow of the program; and,
2. Low-priority messages, which ideally should not be allowed to interfere with normal program execution.

In other words, what is needed is a mechanism which will notify a task that a message has come for it, or which will activate a task (including loading, if necessary) from another operating system. This mechanism needs to be able to assign priorities to messages and to handle alarm conditions.

At least three possible indirect solutions to the problem will be studied, as well as any others which may look promising:

1. Have the message task for each of the computers relinquish control until a bit is set in a specified location in shared memory;
2. Issue a hardware interrupt for all messages;
3. Use the relinquish-until-bit-set scheme for low-priority messages and the hardware-interrupt scheme for high-priority messages and alarms.

WORD 2

| | | | | | | | | | | | | | | | |
|----------|-----|----|----|----|----|---|---|---|---|-----------|----|----|----|----|----|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 200 | 100 | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 | 20 | 10 | 8 | 4 | 2 | 1 |
| BCD Days | | | | | | | | | | BCD Hours | | | | | |

Time-of-day information will then be available to any program on the monitor computer by means of the Modcomp-supplied Fortran-callable "TIMDAT" subroutine.

It is understood that the timing system program must execute as efficiently as possible, since it is serviced at the hardware interrupt level, ahead of any tasks. By no means can it require more than one millisecond to complete, since this is the rate at which the data in the input registers is being updated.

The timing system program task will require approximately six man-weeks of effort to complete, including:

1. Two man-weeks for a study of the various alternatives available for handling the task;
 2. Two man-weeks for the design of the program;
 3. One man-week for program coding; and,
 4. One man-week for program checkout and documentation.
4. Command String Processor and Graphics Preprocessor Task, and
 5. Real-Time System Task

Because these two tasks are closely interrelated, they will be treated together. The goal of both tasks is to provide CADRE personnel with an easy-to-use, engineering-oriented graphics language for programming eight Ramtek 9200 color display units. These color CRT's will be used to convey system status to the test operator during tests in the Compressor Research Facility.

The command string processor and graphics preprocessor will accept a Fortran program with graphics instructions for a desired display as input and produce three separate Fortran programs as output. One program will execute pre-test in the monitor computer to generate and store the fixed part (background) of the display in image mode on disk. The second and third programs (the real-time system) will execute once per second during the test. One of these programs will run on the data acquisition computer and will gather together all the real-time variables needed for the display. The other program, on the monitor computer, will output the Ramtek instructions necessary to generate the variable (foreground) part of the display.

An estimated nine man-months will be required to complete these two tasks as follows:

1. Two man-months for program design;
2. One and one-half man-months to code the processor which will generate three Fortran programs from the user's source program;
3. One-half man-month to code a symbol processor routine which will translate ten mnemonic symbols (such as "VALVE") into a combination of twelve "pure" Ramtek-type instructions (such as "VECTOR"), and which will be able to accept new symbol definitions;
4. Two man-months to code an instruction processor routine which will translate any of twelve "pure" Ramtek-type instructions into Ramtek-acceptable code, along with the appropriate arguments;
5. One-half man-month to code a routine which will generate point plots. Input will consist of an array of values. The routine will perform scaling and draw axes, in addition to plotting the points;

6. One-half man-month to derive a set of procedures which will perform task-related chores such as executing the program to generate the fixed portion of the display, retrieving the object code from the Ramtek memory, and storing the image form on disk;
7. One man-month for program checkout;
8. One man-month for documentation.

6. Reports and Documentation

In addition to task documentation described above, the following reports and documentation will be needed at the approximate manpower requirements listed below:

1. Progress meetings with CADRE, one day per week during the first four months of effort, for a total of seventeen man-days;
2. Narrative reports, four hours every two weeks for one year, for a total of thirteen man-days;
3. Final documentation, which will provide CADRE with a complete User's Manual for the ADDS 880 Interface and the Graphics Preprocessor; one man-month.

These three phases of documentation will thus require a total of approximately 2.5 man-months.

7. Miscellaneous Tasks

Besides the time allocated for the six tasks outlined above, additional time will be required to accomplish the following tasks:

1. Three man-months of training on and familiarization with the Modcomp system (one man-month for each of three programmers);
2. One-half man-month to establish a useful procedure file; and,

3. One man-month for system generation (Sysgen) attempts to create a computer system streamlined for the needs of CADRE.

Although the total requirement of four and one-half man-months of effort for these three tasks may seem like quite an overhead, it is felt that time invested in these tasks will greatly pay off in increased programmer productivity and increased system flexibility.

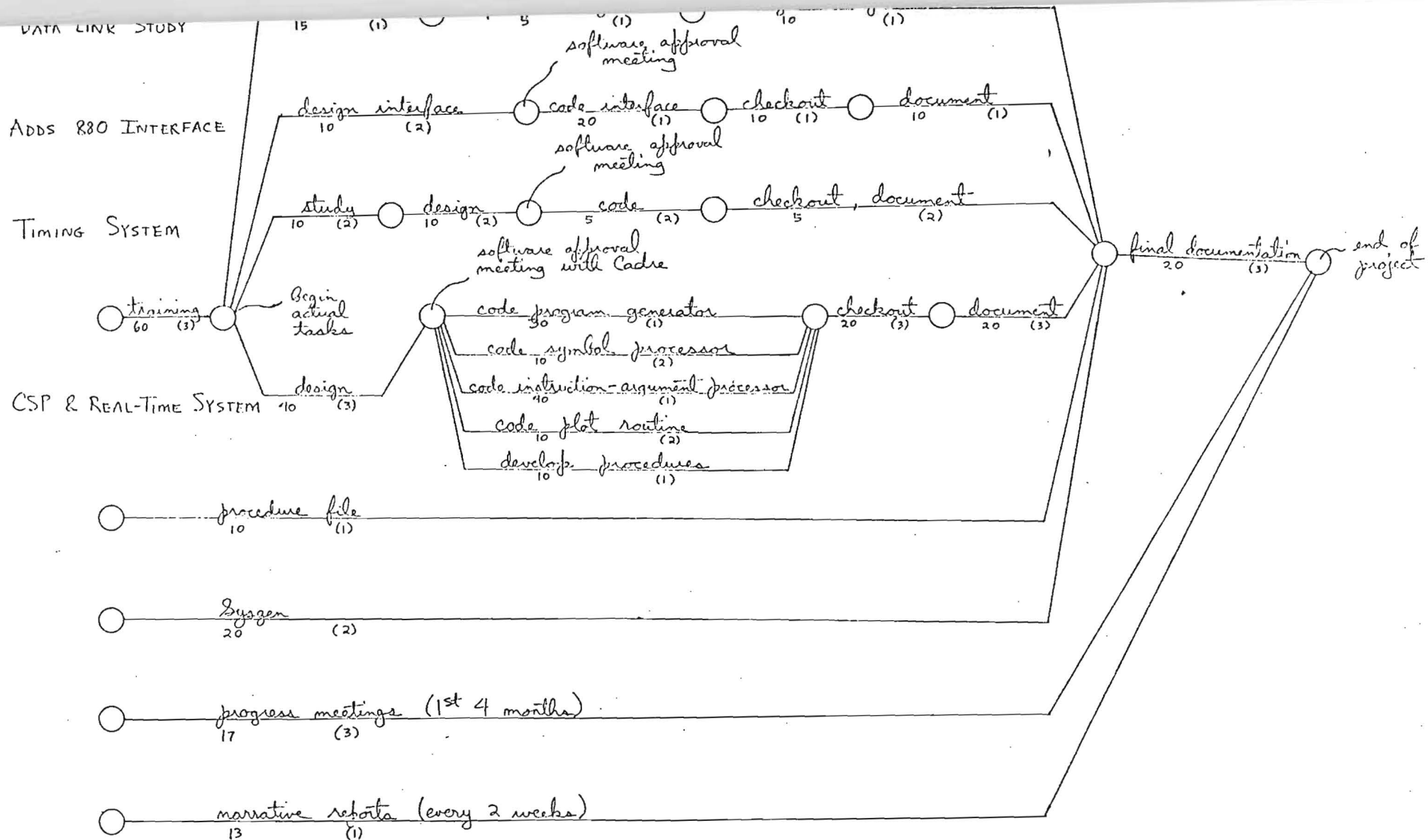


FIGURE 1. MONITOR COMPUTER SOFTWARE DEVELOPMENT PLAN

FCC Software Development Task

The sequence for development of software design and coding of the Facility Control Computer in the Compressor Research Facility is described below in terms of seven sub-tasks. The sub-tasks are: (1) Review of Software Functional Specification, (2) Overall Software design, (3) Timing Considerations/software, (4) Extraction of Drive Models for Simulation Testing, (5) Module Software Design, (6) Module Coding, and (7) Integrated Testing. Figure 1 shows the relationships between sub-tasks and the estimated time and manpower requirements for each sub-task.

1. Overall Software Requirements

The Overall Software Requirements sub-task for the Facility Control Computer (FCC) will include itemization of the inputs and outputs of the FCC and the timing requirements associated with them. It will also show the desired relationships between the input and output variables in either analytic, logical, or verbal form, and will specify limiting conditions such as allowable acceleration levels. It will not contain scales of measured variables, but will list those variables for which scales must later be specified. The existing CADRE document No. 78-107-0040, entitled, "Variable Speed Drive Control" will be the primary source of information. This itemization will provide the basic data necessary for software design in a format readily usable by the software designers.

Also in this sub-task, the logical components of the software package will be identified, their functions defined, the intra-module interfaces defined, and a detailed overall description of methodology will be developed including time considerations for use when integrating the modules into the overall FCC software package. The output of the overall software design will be a document containing the above information in a form which can be used directly by personnel developing the individual modules. An overall block diagram will be included in the documentation. It is anticipated that a design review will be held at CADRE upon completion of this phase.

2. Timing Considerations/Software

The second sub-task in the top-down software development process is to design, code, implement, and test the overall software control algorithm. It is the opinion of the project team that a timing control module for the FCC software will serve this purpose. The availability of the timing control module to the designers of the individual modules will permit the identification of timing requirements internal to each module. After individual modules are coded, implemented, and tested on a stand-alone basis, they may be interfaced with the timing control module and further tested for performance within the real-time environment. The timing control module will be developed in such a manner as to permit testing on stand-alone basis with no other modules implemented, testing with any number of modules, testing with any combination of modules, and inclusion in the final software package. Documentation for the timing control module will be prepared and delivered as discussed below.

3. Extraction of Drive Model for Simulation Testing

Several simulations have been used to model the response of the electro-mechanical devices associated with conversion of 60 cycle power to variable-frequency power and the prime drive motors for the compressor research facility chamber. The primary simulation currently existing at CADRE contains such a model of the drive system, but it is the result of a series of sequential modifications and, as such, is somewhat unwieldy; it also contains simulation of additional features not needed for this task. It is proposed as sub-task 3 that the portion of that simulation needed for verification of the algorithms for control of the frequency converting and driving electro-mechanical devices be extracted from the CADRE simulation, reprogrammed in an orderly fashion, and interfaced for use on one of the MODCOMP II computers for checkout of the resulting FCC software. It will serve primarily as a check on the speed control module implementation, but will also provide additional check capability for other modules.

4. Module Software Design

Individual module designs comprise the next phase of the FCC software development. The modules include the facility executive, the emergency shut-down model, the speed control module, the PLC control module, the drive control parameter input module, the facility parameter input module, the limit checking module, and the data output module. The design of each module will include the following steps:

1. Description of all functions to be performed;
2. Interrelationship of all these functions and the interfaces external to the module (including a general flow chart); and,
3. Methodology for implementation within the particular hardware environment.

Documentation covering the module design will be provided including the above information in a format consistent with CADRE's requirements.

5. Module Coding

Upon completion of the design for all the modules, the coding, implementation, and testing process will begin. Based on results of module design, FORTRAN code will be developed for the MODCOMP II computer designated as the Facility Control Computer. At this time, it is not anticipated that assembly language coding will be required to meet any of the timing requirements; however, assembly language coding can be delivered if required (with appropriate cost adjustments made to include the additional time required for assembly language coding and implementation). The code will be established in program files on the MODCOMP II, compiled/assembled, tested within the timing and functional constraints of the overall system. Documentation consistent with CADRE's standards will be delivered covering the coding, implementation procedure, and the results of tests.

6. Integrated Testing

Upon the completion of software design and coding for all modules, integrated testing will be performed. In this sub-task, all modules will be integrated into the timing control module and tested in conjunction with the facility drive system simulation developed in sub-task 3 above. One purpose of top-down software development is to reduce the possibilities of error due to oversight and, therefore, reduce the effort necessary to repeat any portion of the development process. However, it is recognized that there is room for error in any software development process and iteration between testing, designing and coding may be required in some cases. The cost estimates given herein were made assuming some iteration will occur.

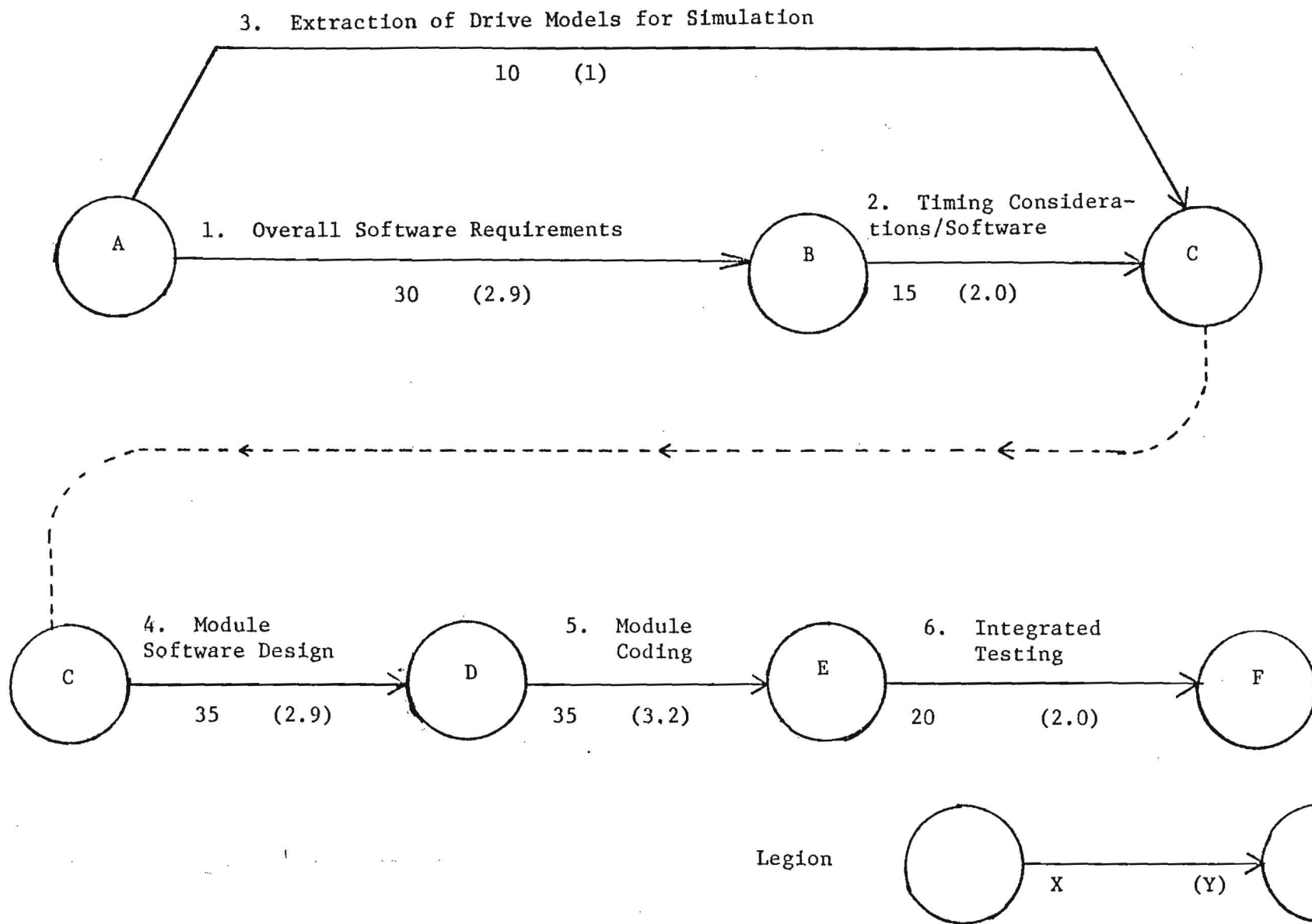


Figure 1. FCC Software Development Plan

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