INTEGRATED, DYNAMICALLY ADAPTIVE SUPPLIES FOR LINEAR RF POWER AMPLIFIERS IN PORTABLE APPLICATIONS

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Biranchinath Sahu

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INTEGRATED, DYNAMICALLY ADAPTIVE SUPPLIES FOR LINEAR RF POWER AMPLIFIERS IN PORTABLE APPLICATIONS

APPROVED:

Prof. Gabriel A. Rincón-Mora, Chairman

Prof. Phillip E. Allen

Prof. J. Stevenson Kenney

Prof. W. Marshall Leach

Prof. Paul A. Kohl

Date Approved: November 4, 2004

Dedicated to my parents

PREFACE

This research focuses on the design and development of a high-efficiency linear radio frequency (RF) power amplifier (PA) with a dynamically adaptive power supply and bias current control targeted for state-of-the-art and next generation, high-performance wireless handsets. The use of spectrally efficient modulation schemes, e.g., code-division-multiple-access (CDMA) and wide-band CDMA (WCDMA) has resulted in challenging requirements of a highly linear PA while maximizing its efficiency over a wide loading range for longer battery life. In this work, an integrated circuit primarily consisting of a noninverting, dynamic, buck-boost converter is conceived and experimentally verified. The approach adopted is to develop circuit techniques that allow use of a low-cost, complementary metal-oxide-semiconductor (CMOS) process while ensuring the design to be operational in a low voltage environment permitted by the threshold voltages of transistors. The functionality of the overall system is verified over a wide range of input supply voltage 1.4 – 4.2 V, which enables the design to be useful over a wide spectrum of portable power sources, e.g., single cell Li-ion battery, double cell nickel cadmium (NiCd) and nickel metal hydride (NiMH) batteries, and the promising alternative of direct-methanol fuel cell (DMFC). The dissertation is organized as a logical sequence of efforts that has gone into the design and development of the linear, efficient RF PA system with dynamically adaptive supply and bias current control.

Chapter 1 introduces the role of portable power management in modern handheld devices and the importance of highly efficient linear RF PAs. The requirements imposed by wireless standards are briefly discussed, which is followed by introduction of various linearity and efficiency specifications pertinent to PA design. The characteristic of portable power sources, rechargeable batteries and DMFC are described in this section.

Various power supply circuits used in portable devices are introduced and compared. Lastly, the chapter concludes by identifying and defining the research objective.

Chapter 2 discusses various PA circuit topologies highlighting their efficiency and linearity aspects. State-of-the-art linearization and efficiency enhancement techniques are critically analyzed pertaining to their suitability for handheld applications, where circuit complexity and low-cost are of prime importance. A comparative evaluation of the linearization and efficiency-enhancement methods is offered. A novel, power-tracking PA with both supply voltage and bias current control is developed and its characteristics are analyzed. The use of buck-boost converter for supply voltage control is adopted to maximize the battery voltage range.

In Chapter 3, various switching regulator topologies suitable for both step-up and -down conversion have been analyzed and compared. Because of its suitability towards IC implementation with minimal number of external components, the single inductor non-inverting buck-boost converter was selected as the adaptive power supply for the PA. The buck-boost converter was analyzed and various system design considerations are offered in this chapter. An intuitive, non-mathematical procedure for deriving small-signal models of the converter is also described, which can be readily extended to other converter topologies. Analysis of converter transfer function for various loading conditions and converter power loss analysis have also been derived in this chapter.

Chapter 4 deals with prototype implementation and experimental verification of the power-tracking PA system developed at the end of Chapter 2. The primary goal of prototyping is to verify the system functionality and subsequently identify potential improvements, which are addressed and implemented in the IC solution. The design details and experimental results of the noninverting buck-boost converter discussed in Chapter 3 are presented in this chapter. Experimental results of a CDMA PA with a power-tracking buck-boost power supply operating at 915 MHz center frequency and 27 dBm peak output power is offered.

Chapter 5 brings about the concepts and extensions made to the basic buck-boost converter to achieve high efficiency over wide loading conditions. The modified buck-boost converter operating in pulse-width modulation (PWM) mode is discussed. An

adaptive on time based pulse-frequency modulation (PFM) mode converter operating in discontinuous conduction-mode (DCM) suitable for maintaining high efficiency during light-loading conditions is presented. Overall, by operating the converter in dual-mode, not only higher system efficiency is maintained throughout the PA loading range but also the controller's quiescent power dissipation is lowered, which improves the PA's standby performance. The concept of spread-spectrum clocking used for reducing the peak-value of switching noise in a buck-boost converter and its implication on CDMA-based wireless systems is discussed.

Based on the conclusions of prototype implementation and subsequent circuit improvements developed in Chapter 5, the details of power management system design and circuit blocks of the buck-boost converter are discussed in Chapter 6. A top-down design approach is followed for deriving specifications for the individual building blocks from the top-level system requirements. The circuit blocks whose design, implementation and experimental results offered are: error amplifier op-amp, PWM and PFM comparators, triangular waveform generator, bandgap reference, supply voltage adaptive on time generation for PFM, and dynamic gate/base bias for the RF PA.

Chapter 7 details the system the experimental evaluation of the adaptive supply IC and WCDMA PA system. The buck-boost converter IC was tested individually for its performance specifications. Later, the IC is used as an adaptive supply for a discrete HBT PA and overall system was tested with a 1.96 GHz HPSK modulated signal with 3.84 MHz bandwidth, as specified by the WCDMA standard. Finally, a summary of the performance specifications of the system as well as those targeted are discussed and illustrated in a table.

Chapter 8 provides a summary of the research presented in the dissertation and conclusions derived thereof. The concepts developed and adopted in the design of the integrated power management system are discussed. The implications of the research on the current and future market demand of linear RF PAs and development of their power management systems is highlighted. The chapter ends with recommendations for future work in this area, addressing the issues of calibration and integration with the transceiver system in a real-word application platform.

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I express my deepest sense of gratitude and thanks to Prof. Gabriel A. Rincón-Mora for allowing me to work with him for my Ph.D. dissertation. His advice, suggestions, and encouragement throughout my doctoral research have been a lifetime learning opportunity and experience. The energy and enthusiasm he infuses during each and every discussion over the entire program has been instrumental in successful completion of this dissertation. His insightful and thought-provoking comments in every possible opportunity have been immensely helpful, not only for the graduate experience, but will also be of tremendous help in my future endeavors. The fine art of intuitive analysis and design of analog integrated circuits from a system perspective that I learned over the years working with Prof. Rincón-Mora is the hallmark of my graduate education at Georgia Tech.

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fellow colleagues for enriching my graduate school experience at Georgia Tech. The association with Georgia Tech Analog Consortium has not only helped to broaden my analog integrated circuit exposure, but it also provided a platform for reaching out to the other frontiers of analog and RF technology. The help of Margaret H. Boehme, our administrative support, during my graduate research is gratefully acknowledged. Graduate school without friends is always devoid of an important facet of life. All of those whom I met inside and outside the Georgia Tech campus, inside and outside the work environment, deserve a special mention for their generous and brave smiling faces in spite of many different obstacles, which inspired me to march towards a goal, which once the famous Robert Frost termed as "Miles to go before I sleep."

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GLOSSARY

2G/3G	Second Generation/ Third Generation
ACPR	Adjacent Channel Power Ratio
ACLR	Adjacent Channel Leakage Power Ratio
BER	Bit Error Rate
BJT	Bipolar Junction Transistor
BS	Base Station
BW	Bandwidth
CCM	Continuous Conduction Mode
CDMA	Code Division Multiple Access
CTAT	Complementary to Absolute Temperature
DAC	Digital-to-Analog Converter
DAT	Distributed Active Transformer
DCM	Discontinuous Conduction Mode
DMFC	Direct Methanol Fuel Cell
EDGE	Enhanced Data Rate for GSM Evolution
EER	Envelope Elimination and Restoration
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
EVM	Error Vector Magnitude
GaAs	Gallium Arsenide
GSM	Global System for Mobile Communications
HBT	Hetero-junction Bipolar Transistor

HPSK	Hybrid Phase Shift Keying
InP	Indium Phosphite
IC	Integrated Circuit
ICMR	Input Common Mode Range
IF	Intermediate Frequency
LAN	Local Area Network
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDO	Low Dropout
LDR	Load regulation
LHP	Left-half plane
LINC	Linear Amplification with Nonlinear Control
LNR	Line regulation
NADC	North American Digital Cellular
OFDM	Orthogonal Frequency Division Multiplexing
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MS	Mobile Station
NPR	Noise Power Ratio
OCQPSK	Orthogonal Complex Quadrature Phase Shift Keying
OQPSK	Offset Quadrature Phase Shift Keying
PA	Power Amplifier
PAR	Peak-to-Average Ratio
PCB	Printed Circuit Board
PDF	Probability Density Function
PM	Phase Margin
PMU	Power Management Unit
PTAT	Proportional to Absolute Temperature
PWM	Pulse Width Modulation
PFM	Pulse Frequency Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency

RHP	Right-half plane
SEPIC	Single-ended Primary Inductance Converter
SiGe	Silicon-Germanium
SOP	System-on-Package
SIP	System-in-Package
SOC	System-on-Chip
UGF	Unity-gain frequency
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VLSI	Very Large Scale Integration
VRM	Voltage Regulator Module
WCDMA	Wideband Code Division Multiple Access

SUMMARY

Energy-efficient radio frequency (RF) power amplifiers (PAs) are critical and paramount to achieve longer battery life in state-of-the-art portable systems, e.g., cellular phones and multimedia terminals with wireless connectivity, because they typically dominate the power consumption of such devices. The conflicting requirements of higher linearity and increased power efficiency impose an enormous challenge for the PA designers. While many complex schemes are employed to improve the linearity of PAs in base-station applications, handheld devices typically require a different approach, where circuit complexity and form-factor of the device are crucial. When a dedicated power supply is used for the PA, incorporating smart power management functions in the converter supply provides unique possibility of prolonging battery life without any significant increase in circuit complexity, when compared to other approaches requiring RF and intermediate frequency (IF) signal processing.

In this research, a high efficiency linear RF PA with a dynamically adaptive supply and bias current control targeted for code division multiple access (CDMA) and wideband CDMA (WCDMA) is conceived, simulated and experimentally demonstrated with a discrete PCB-level design as well as in integrated circuit (IC) form. The efficiency of the PA is improved by dynamically adjusting its supply voltage and bias current, there by minimizing the quiescent power drained from the source. The supply voltage of the PA is derived from the battery by a noninverting synchronous buck-boost switching regulator, because of its flexible functionality and high efficiency. Investigations conducted in this research concluded that changing the PA supply voltage and current by tracking the input power, instead of following the complete envelope in large bandwidth

wireless applications, can be achieved by a converter with a lower switching frequency and consequently higher light-load efficiency, which translates to prolonged battery life. Experimental results of the discrete prototype implementation of the linear PA system with dynamically adaptive supply shows *more than four times improvement in average efficiency* over a fixed-supply PA.

The dynamically adaptive power management system for a WCDMA RF power amplifier is designed, simulated and experimentally evaluated. AMI's 0.5-μm CMOS process technology through MOSIS is utilized for the fabrication of the integrated system. The integrated buck-boost converter was experimentally verified for functionality with a wide input voltage range, 1.4 – 4.2 V, the lower value of which is limited by the threshold voltage of the process technology and input common-mode range (ICMR) requirements of low-voltage circuits. The converter IC generates an output voltage of 0.4 – 5 V in pulse width modulation (PWM) mode from an input supply of 1.8 – 4.2 V with a maximum output current of 330 mA, while exhibiting a peak efficiency of 90 %. The converter operating in pulse frequency modulation (PFM) mode generates an output voltage of 0.5 V with 50 mA load current, while accurately controlling the output ripple voltage to less than 25 mV over an input supply range of 1.4 – 4.2 V using adaptive on time control. A top-down design approach was followed for deriving the circuit specifications from the system requirements and subsequently various circuit blocks were designed and developed for low voltage operation.

A 25-dBm, 1.96 GHz center frequency, 3.84 MHz baseband bandwidth hybrid-phase-shift-keying (HPSK) modulated WCDMA RF PA is experimentally demonstrated with a dynamically adaptive integrated CMOS dual-mode buck-boost supply and bias current control IC. The dual-mode (i.e., PWM and PFM) converter increased the battery life performance of the PA system as much as *five times* compared to a fixed-supply system and *twice* compared to a converter operating in only PWM control, assuming that the PA remains in active mode for 2 % of the total time and remains in the standby mode otherwise. The experimental PA system developed in this research is verified for functionality and performance over a 1.8 – 4.2 V supply voltage range, rendering its suitability for single-cell state-of-the-art Li-ion batteries and two-cell stacked low-cost

NiCd/NiMH battery, thus providing a truly generic and low voltage solution. Furthermore, the low voltage circuit design techniques developed in this research are also applicable beyond the realm of integrated power management applications and can be used in the general arena of analog integrated circuit design.

CHAPTER I

INTRODUCTION

In the next generation, high-performance, portable hand-held devices there is a great interest in accommodating the challenging demands of high-speed data transmission, e.g., software, screen technology, and data-processing bandwidth [1]. Consequently, the higher bandwidth and increased power requirement at the antenna in these systems demand efficient power management solutions to prolong battery life. The power amplifier (PA) in a portable radio frequency (RF) transmitter drives the load (antenna) with sufficient energy such that the resulting electromagnetic signals reach the base station with higher power level than the noise floor. Energy-efficient PAs are critical to increase battery life in state-of-the-art RF transceivers used in portable communication devices, e.g., cellular phones, because they typically dominate and determine the power consumption characteristics of such devices. Unlike the second-generation (2G) systems employing Global Systems for Mobile Communications (GSM) where nonlinear PAs are used, the spectrally efficient digital modulation schemes, e.g., code-division-multiple-access (CDMA), require linear PAs to preserve the fidelity of the transmitted signal without causing unnecessary interference in the adjacent channels.

Linearity of a PA is typically achieved by increasing its bias current, thereby drawing more power from the supply for a fixed output power and consequently degrading its power efficiency. On the other hand, PAs exhibiting high efficiency are nonlinear in nature [2]. Therefore, the design of an energy-efficient PA remains an extremely challenging frontier in wireless communication research. This chapter brings about the role and requirements of energy-efficient linear PAs in the domain of portable

power management with the aim of improving battery life in feature-rich handheld devices. The performance specifications of RF PAs, especially linearity and efficiency are introduced. A brief summary of state-of-the-art rechargeable batteries and the highly promising fuel cells are also discussed, while presenting an overview of dynamically adaptive power supplies. The objectives of the research are then identified according to the state-of-the-art and future portable market demands for wireless handsets using CDMA and Wide-band CDMA (WCDMA) wireless standards.

1.1 Role of Efficient Linear RF Power Amplifiers in Portable Applications

Portable devices with wireless connectivity require a radio frequency transmitter to send information to the nearest base station, which subsequently resends the data to the desired destination via another wired or wireless network. In the wireless transmitters, the RF PA is the final interface between the baseband and RF signal processing components and the antenna. Figure 1.1 offers a simplified block-level schematic of a radio transmitter employing a digital modulation scheme. The baseband in-phase (I) and quadrature-phase (Q) data are modulated to generate an intermediate frequency (IF) signal, which is subsequently amplified by a variable gain amplifier (VGA). The resulting signal is processed through a band pass filter (BPF) and up-converted into an RF signal by using a mixer and a local oscillator. The PA amplifies the modulated RF signal and increases the transmitted signal power level at the antenna such that faithful reception is accomplished at the base station. The variable gain amplifiers, by adjusting their gains, control the signal level at the PA input, thereby ultimately controlling the antenna power level.

Conceptually, the role of a PA appears to be rather simple, to amplify the input signal and to deliver the resulting power to the antenna. However, RF PAs are extremely critical components in the radio transmitters used in the wireless communication systems because they determine the final quality of the waveform. The PA in a RF transmitter drives the load (antenna) with sufficient energy to ensure the resulting electromagnetic signals reach the base station with enough strength, that is to say, well above the noise

level. This must be done with minimum distortion to the RF signal to prevent spurious signals from interfering with other channels. Therefore, the RF PAs used in transmitters require very high linearity to preserve modulation accuracy and limit the spectrum re-growth. PAs typically dissipate more power than any other circuit block in a mobile radio [3]. The PA is therefore a key block, as far as cost, power consumption, reliability, and system performance requirements are concerned [2].

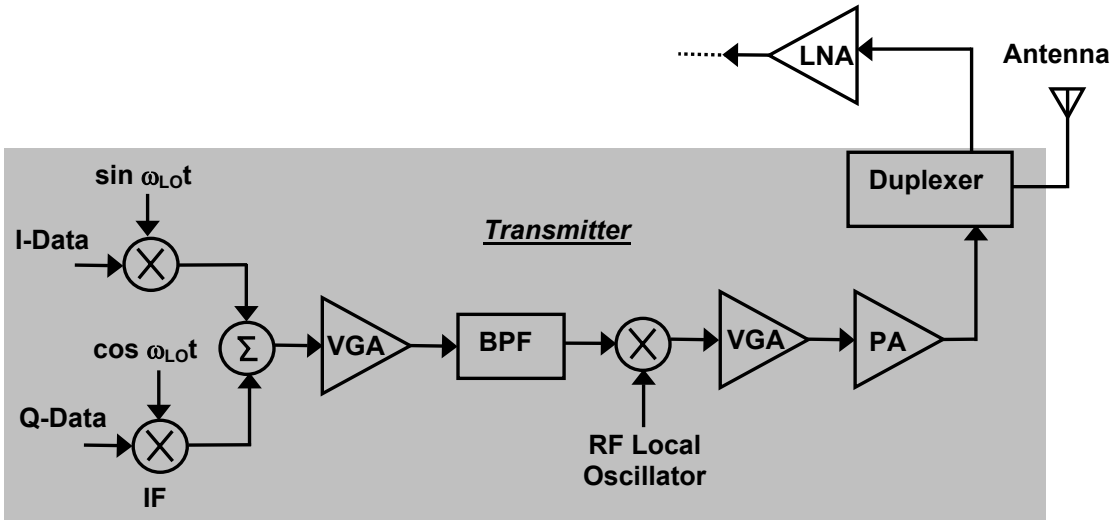


Figure 1.1. Block-level representation of a typical wireless handset transmitter section with a digital modulation scheme.

To improve operational time of a battery-powered wireless transceiver, it is desirable to have a transmitter section that works at its highest possible efficiency. Unfortunately, as one strives to increase power efficiency by operating the PA in different regions of its load-line, the output distortion produced by the solid-state device nonlinearities often becomes excessive and a limiting factor for the overall design. Nonlinear PAs achieve higher efficiency at the expense of degraded linearity. The required linearity level desired for the PA is highly dependant on the application environment. Wireless standards employing modulation schemes with constant envelope RF signals, e.g., GSM, use nonlinear PAs because the information is transmitted in the phase of the signal, and accurate transmission of amplitude is therefore not required. On

the other hand, advanced modulation formats targeted for the third generation wireless schemes, e.g., EDGE, and WCDMA use non-constant envelope RF signals to achieve higher spectral efficiency. In these applications, information is transmitted in both the amplitude and the phase of the waveform; therefore, linearity as a performance specification of RF PAs is the first and foremost requirement.

Achieving the desired level of linearity, while improving the efficiency of the RF PA remains a challenging frontier in wireless research. Fundamentally, an RF amplifier can be operated with high efficiency by biasing the active device with low quiescent current, which results in clipping of the signal waveform and degraded linearity. Generally, linearity is achieved at the expense of degraded efficiency and nonlinear PAs are more power efficient than their linear counter parts. Two different approaches are pursued, depending on system complexity and cost advantages, to achieve higher efficiency while maintaining required linearity level demanded by the application. An inherently efficient nonlinear PA with an added linearization circuit is used to improve the linearity level, while a linear PA with an efficiency enhancement circuit is used to increase the efficiency.

1.2 Role of Portable Power Management

The unprecedented growth of cellular technology and infrastructure around the globe has resulted in a surge in the demand for handheld devices incorporating color screens, games, multimedia, cameras, personal information management systems, etc. It is predicted that in 2006 the number of smart phones, convergent devices with extensive voice and data capabilities, should be larger than the number of notebooks shipped in a year and far outnumber devices with single functionality, e.g., digital still cameras and personal digital assistants (PDAs) [4].

As data, voice, and ubiquitous computational technologies become available in a single hand-held device, a number of design challenges arise. Multiple wireless standards, video games, mobile-internet, and audio functionalities are starting to become available in a single multimedia terminal. While the power consumption grows with every added functionality, the end user expects the same or comparable battery life.

Power management of multimedia portable terminal has evolved over the years leading to many innovations [5], but mainly for optimized voice-only applications [6]. The new technical challenges primarily due to the unprecedented integration of multitude of functionalities have spurred wide spread research interest around the globe focusing on prolonging battery-life in portable devices. Since improvements in battery's technology has not kept up the pace with the portable demands driving it, the thrust remains on squeezing more life out of the same battery by using efficient power management techniques through smart innovative solutions, which exploit the capabilities of high-volume integrated circuit (IC) technologies.

Virtually all state-of-the-art electronic systems require some form of power conversion. The trend towards low power and portable equipment has further driven the technology and need for converting power efficiently. Today's portable, hand-held devices use a number of supply voltage levels for different parts to operate them with higher efficiency, thereby improving the system's battery run-time. Typically, the system's power management unit (PMU) comprises a number of converters, both switching and linear regulators, to generate these various supplies from available power sources. Figure 1.2 shows a typical block diagram representation of a handheld device and its power supply model [7]. Generally, the digital circuits are operated with their lowest possible supply voltage, as permitted by technological constraints, while display and other interface functions require a higher supply. The PA is operated with a higher supply than the other parts of the analog/RF sub-block to deliver the required power with a lower current level, thereby minimizing the power losses in the current flowing path and achieving higher efficiency. The power management of portable devices like cellular phone is much more complicated than simply turning on the radio to make a call or turning on the charger to charge the battery. In state-of-the-art CDMA systems, as many as eleven separate power supplies are being used to elongate battery life by optimizing the operation of circuit building blocks with different supply voltages [8].

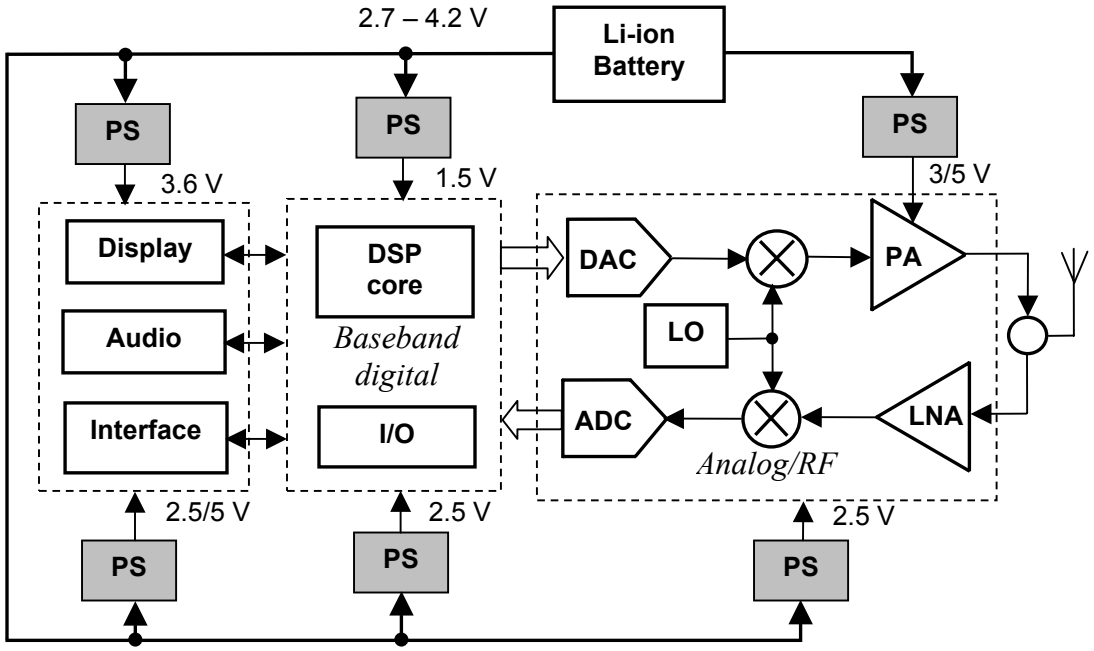


Figure 1.2. Block diagram representation of various power supply units in a wireless handset [7].

As handheld systems evolved into multi-media and multifunction solutions, their power management units have necessarily become more complex. Utilizing the system's operating state information and dynamically adjusting the power supply for various blocks to save power has become the corner-stone in the new paradigm of intelligent and smart power management systems. Irrespective of higher complexity, the manufacturer's ability to differentiate portable products in the consumer market with longer battery life, even at slightly higher cost, is the driving force behind innovations in power saving architectures. The ever-improving integration capabilities leading up to system-on-chip (SOC) and system-on-package (SOP) solutions have also been instrumental in reducing the overall cost. The "smartening" of power management electronics, combined with the increasing maturity of new technologies for energy storage and displays, promises to keep the feature-rich portable devices on a steep growth curve for the foreseeable future [4].

1.3 Wireless System Considerations

Classical power amplifier design techniques frequently ignore signal characteristics, instead focusing on transistor performance and circuit design techniques. However, with the emergence of digital wireless communication systems, an understanding of modulation theory is also required to fully characterize the power amplifier performance with the modulated carrier for the optimum linearity-efficiency trade-off [9]. Two important characteristics of spectrally efficient CDMA and WCDMA wireless schemes are highlighted in this section and their implications on the overall system from the efficiency and linearity perspective is addressed in the following paragraphs.

1.3.1 High Peak-to-Average Ratio (PAR)

Time domain CDMA signal exhibits large peak-to-average ratio (PAR) [3]. A representative time domain CDMA signal and its envelope are shown in Figure 1.3. The PA is normally designed and biased such that the signal peaks incur no or very limited clipping to meet the linearity specifications of a wireless standard in which the PA is targeted for use. In the valleys of the signal envelope, because of the smaller voltage swing and consequently higher power loss, the PA efficiency degrades. Intuitively, to prolong battery life, the PA should therefore be operated with high efficiency throughout the base-band signal envelope (e.g., peaks, valleys, and intermediate points).

Figure 1.4 illustrates the input to output power transfer function of a typical PA, highlighting the operating point in both linear and nonlinear regions of operation. When the amplifier is biased to operate in the linear region of the transfer function, the peak amplitudes of the signal waveform experience little clipping. On the other hand, operating in the nonlinear region of the transfer function produces clipping of the output signal waveform since the PA is saturated. As a result, the PA output signal contains unwanted harmonics, in addition to the fundamental component, thereby creating both in-band as well as out-of-band distortion.

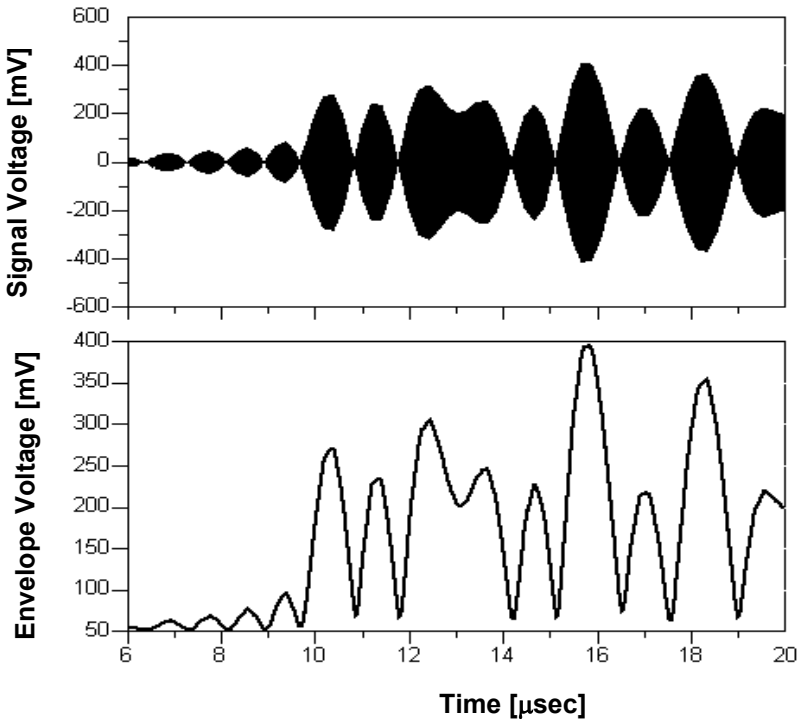


Figure 1.3. Time domain CDMA waveform and its envelope, illustrating high peak-to-average ratio characteristics.

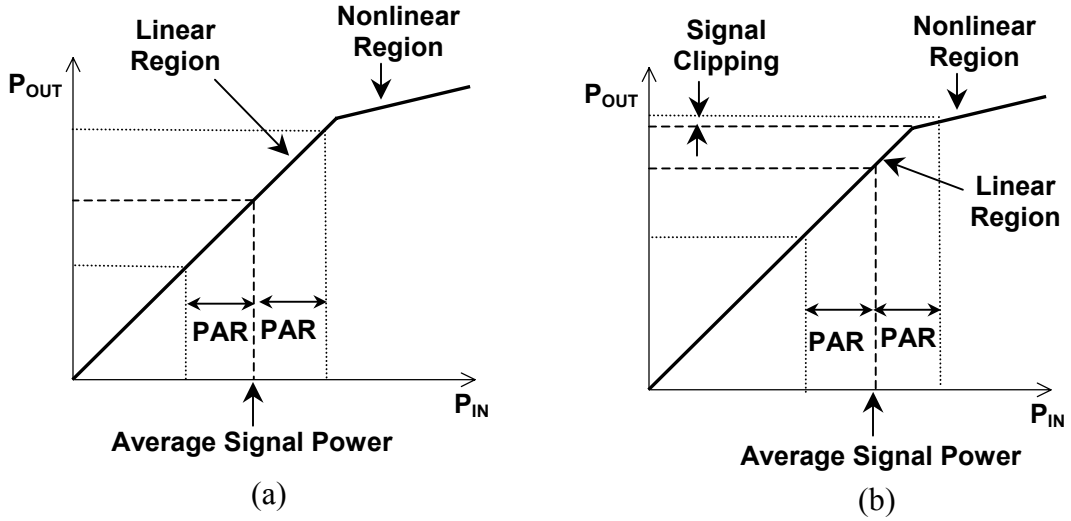


Figure 1.4. Illustration of the peak-to-average signal implication on the PA (a) linear operation, (b) operation with clipping.

While the PA amplifies a single-tone sinusoidal signal, to achieve linear operation the operating point is selected such that peak value of the instantaneous signal remains within the limit set by the boundary of linear and nonlinear operating regimes. To amplify a high peak-to-average ratio signal having an instantaneous maximum same as that of the single-tone signal, the operating point remains unchanged. Consequently, while the quiescent power in the active device remains the same, the useful average output power is less, which degrades the PA efficiency.

1.3.2 Power Control

Power control is essential to the operation of a CDMA/WCDMA system [10]. When all the mobile stations send signal of equal power level, the base station (BS) receives a much stronger signal from a mobile station (MS) that is closer to the base station than the mobile station that is far way. Since all the users share the same RF band, each user looks like random noise to other users. The power of an individual user, therefore, must be carefully controlled so that no one user is unnecessarily interfering with others who are sharing the same frequency band. Another objective of power control is to maximize channel capacity. WCDMA uses fast closed-loop power control, where based on the power a base station receives, it commands the mobile station to adjust its transmission power such that the received power from all the mobile station is equal. In the CDMA and WCDMA architecture, transmitted power can be adjusted up or down by 1dB in every 1.25 ms and 666 μs, respectively, as requested by the base station [11]. The handset may enter or exit data-transmission mode every 10 ms [11].

Figure 1.5 shows the transmitted power usage probability density for CDMA applications [3], [12] in an urban and suburban environment. Unlike GSM, the dynamic range of transmitter power is large for CDMA-based wireless communication systems, which creates additional challenges in realizing an energy-efficient PA solution. To achieve high average efficiency, for improved battery life, the power amplifier must be operated with high efficiency across the loading condition. Any additional circuit either used for achieving linearity or improving efficiency should exhibit high efficiency across the output power range of the PA.

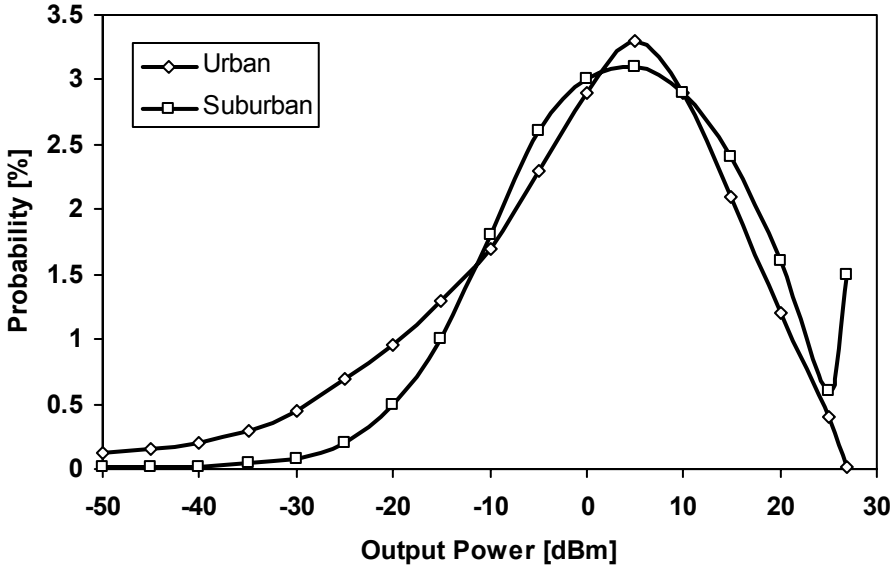


Figure 1.5. Probability curves for transmit power level in urban and suburban environments [3], [12].

1.4 RF PA Performance Specifications

1.4.1 Linearity

All radio systems must generate minimum possible interference to the other systems; they must therefore maintain their signal transmission within the bandwidth allocated to them and not radiate significant energy outside of it. Linear modulation schemes are defined as those in which information is transmitted in both the amplitude and the phase of the RF signal. The envelope of the RF signal thus varies with time and must therefore be preserved to retrieve the information content of the original message signal. Linearity of an RF PA is measured in terms of both in-band and out-of-band undesired signal generation, and the specifications relating these nonidealities are presented in the following subsections.

(a) Adjacent Channel Power Ratio: Adjacent channel power ratio (ACPR) is a measure of the degree of signal spreading into adjacent channels caused by nonlinearities in the

power amplifier. Figure 1.6 shows a representative output spectrum of an RF PA with the main channel and adjacent channels illustrating the ideal signal and the distorted signal with in-band and out-of-band distortions. ACPR is the result of out-of-band signal distortion and is defined as the power contained in a given bandwidth (BW_2) at an offset frequency (f_o) from the center frequency (f_c), divided by the power in a bandwidth (BW_1) around the channel center frequency (f_c).

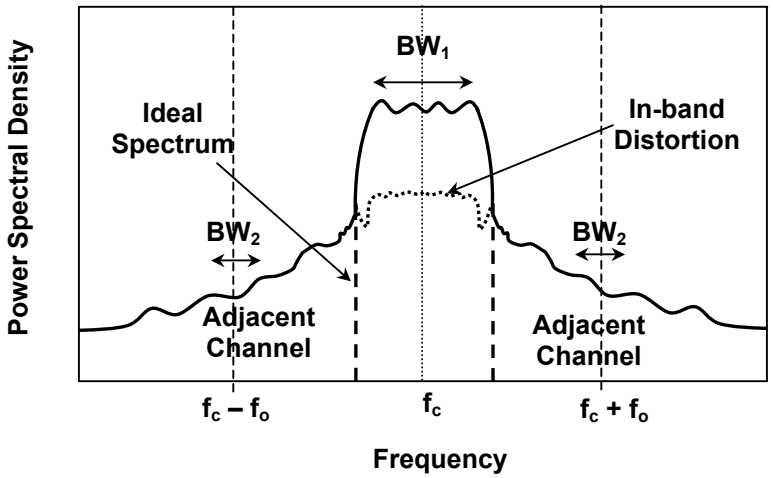


Figure 1.6. Spectrum of the ideal transmitted modulated signal and the distorted signal illustrating ACPR and in-band distortion.

(b) Noise Power Ratio: Noise power ratio (NPR) is a measure of the unwanted in-channel distortion power caused by the nonlinearity of the power amplifier. NPR is defined as the ratio between noise-power-spectral-density of a white noise signal passing through the amplifier, measured at the center of the notch, to the noise-power-spectral-density without the notch filter, where the amplifier is driven at the same power level in each case [13]. Figure 1.7 provides a graphical representation of noise power ratio, which is essentially the result of the in-channel distortion caused by the nonlinearities in an RF PA. Generally, it is measured for multi-carrier amplifiers such as the ones used in base stations.

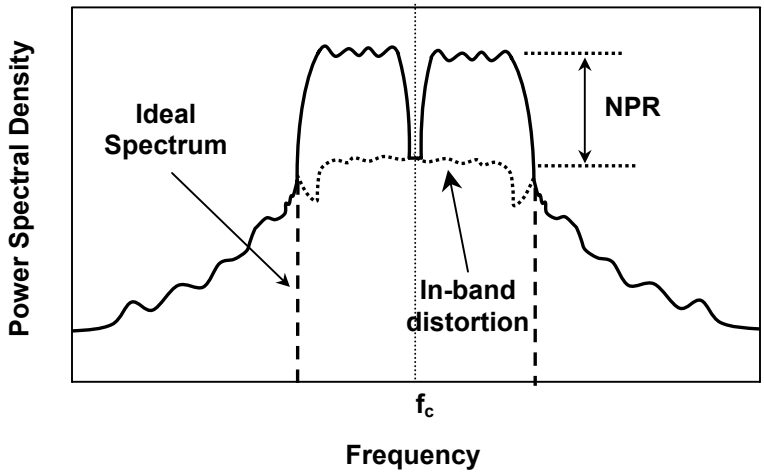


Figure 1.7. Illustration of noise power ratio of an RF PA because of in-band signal distortion.

(c) Error Vector Magnitude: For vector-modulated signals, the digital bits are transmitted onto an RF carrier by varying the carrier's magnitude and phase such that at each data clock transition the carrier occupies any one of the several specific locations on in-phase (I) versus quadrature-phase (Q) plane. Each location encodes a specific data symbol, which consists of one or more data bits and the pattern is known as *constellation diagrams*. Figure 1.8 shows the constellation diagrams of OQPSK and QPSK modulation schemes [14]. OQPSK is employed in CDMA-IS95 mobile handsets while WCDMA mobile units use hybrid phase shift keying (HPSK) modulation, which is a variant of QPSK where two successive transitions through origin are not allowed. Because of fast envelope fluctuations in QPSK, the high frequency components removed during the filtering process for adjacent channel interference in a cellular system can be regenerated by nonlinearities in an amplifier. However, since the fast phase transitions are absent in OQPSK modulation scheme, the PA can be operated further inside the gain compression region where it is nonlinear, thereby yielding a higher efficiency.

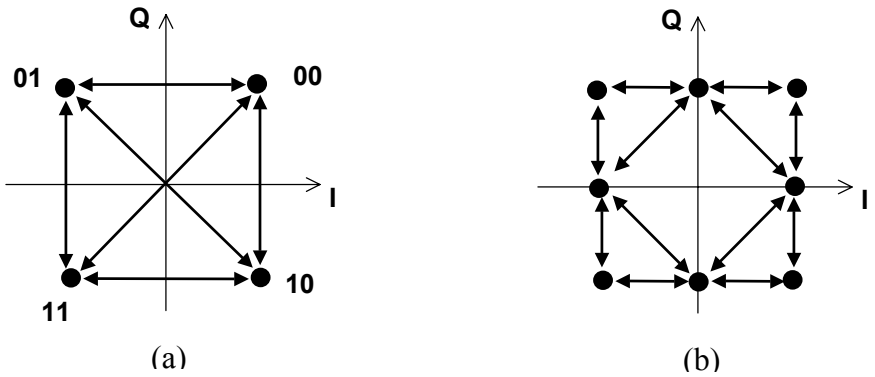


Figure 1.8. Constellation (state) diagram of (a) QPSK, and (b) OQPSK modulation schemes.

At any time instant, the transmitted signal's amplitude and phase can be measured. The corresponding ideal reference phasor can be calculated, given knowledge of the transmitted data stream, the symbol clock timing, and baseband filtering parameters. The error vector magnitude (EVM) is defined as the scalar distance between the two phasor end points, reference and measured signals. Figure 1.9 shows the conceptual representation of EVM and related quantities. The error vector is a complex quantity, containing both magnitude and phase components [13]. EVM is measured as the root-mean-square (rms) value of the error vector when the symbol clock transition occurs. Typical EVM figures are in the range of 5–15% [9].

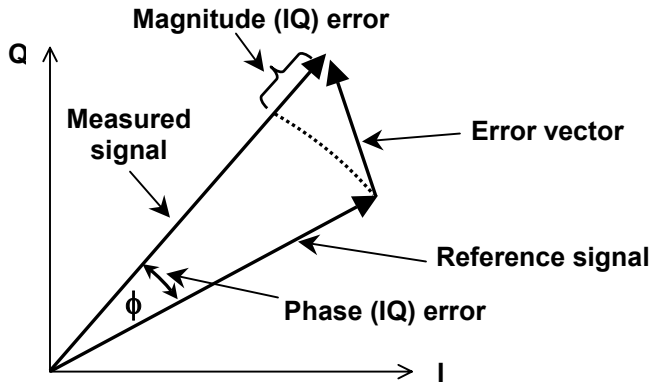


Figure 1.9. Illustration of error vector magnitude (EVM) and related quantities.

The waveform quality metric *Rho* (ρ) is another measure of the fidelity of the transmitted signal, which is typically used in CDMA systems. It is the measure of correlated power, which is computed by removing frequency, phase and time offsets, and performing a cross correlation between the corrected measured and the ideal reference to the total transmitted power [16]. If the transmitted signal matches perfectly with the reference signal, correlation is one-to-one yielding a *Rho* of 1.00. A waveform quality factor of 0.98 or better typically represents a high quality transmission [9]. In practice, EVM has been demonstrated to be a more sensitive gauge of waveform quality than *Rho*, since the latter is seen to vary approximately from 0.98 to 0.99 while the former varies from 3% to 10% [17].

1.4.2 Efficiency

The efficiency of an RF PA, as a figure-of-merit, is often expressed by different specifications, which are briefly explained in the following subsections.

(a) Drain/Collector Efficiency: The drain/collector efficiency of an RF PA is defined as the ratio of output RF power (P_{RF_OUT}) to the input supply power (P_{SUPPLY}) and is given by

$$\eta_{DRAIN} = \frac{P_{RF\_OUT}}{P_{SUPPLY}}. \tag{1.1}$$

(b) Power-Added Efficiency: The power-added efficiency (PAE) of an RF PA considers the gain of the amplifier and is defined as the ratio of the difference of output RF power (P_{RF_OUT}) and input RF power (P_{RF_IN}) to the input supply power (P_{SUPPLY}) and is given by

$$\eta_{PAE} = \frac{P_{RF\_OUT} - P_{RF\_IN}}{P_{SUPPLY}}. \tag{1.2}$$

(c) Average Efficiency: Drain or power-added efficiency represents a realistic figure of merit only when the PA is operated at its peak output power. However, in portable environments, especially CDMA-based systems, the PA transmits its peak-rated power for a fraction of the total time and mostly operates with a 20-30 dB power back-off. Therefore, average efficiency, where the probability distribution of the PA loading profile is taken into account, is seen as a true figure of merit for evaluating battery life.

The average energy efficiency of the PA is defined as the ratio of average output power to the average input power and is given by [3]

$$\eta_{AVG} = \frac{\int_0^{P_{RF\_OUT,max}} P_{RF\_OUT}\, \mathrm{Prob}(P_{RF\_OUT})\, dP_{RF\_OUT}}{\int_0^{P_{RF\_OUT,max}} P_{SUPPLY}(P_{RF\_OUT})\, \mathrm{Prob}(P_{RF\_OUT})\, dP_{RF\_OUT}}, \tag{1.3}$$

where P_{RF_OUT} is the output power, $\mathrm{Prob}(P_{RF\_OUT})$ is the probability of output power P_{RF_OUT}, and $P_{SUPPLY}(P_{RF\_OUT})$ is the supply power required at P_{RF_OUT}. This quantity is the realistic measure of the effectiveness of the PA in converting the battery-stored energy into transmitted energy.

1.5 Portable Power Sources

Today's portable devices are smaller and more powerful than ever, but the batteries remain the major roadblock in further miniaturization [18]. Manufacturers are capable of producing smaller notebooks, cellular phones, and personal digital assistants (PDAs), but cumbersome state-of-the-art power sources make the smaller packages impractical. Direct Methanol Fuel Cell (DMFC) technology, although at its early infancy, promises to be an alternative power source for portable applications due to its potentially superior energy density, and suitability of integration with rest of the system onto same silicon wafer [19]. In this section, characteristics of rechargeable batteries and DMFC fuel cells are reviewed and the design considerations they superimpose on the design of a power management unit (PMU) are highlighted. For complete utilization of the power

source before recharging a battery or adding more fuel into a fuel cell, the PMU should be designed to be functional over the entire terminal voltage profile of the power sources. For flexibility and generality, the solution is desired to be compatible with power sources having different voltage profiles.

1.5.1 Rechargeable Batteries

The discharge characteristics of a Lithium-ion (Li-ion), and a Nickel Metal Hydride (NiMH) and Nickel Cadmium (NiCd) battery cells are shown in Figures 1.10(a) and 1.10(b), respectively. A single Li-ion cell battery has a terminal voltage of 4.2 V when fully charged and approximately 2.7 V just before it is fully discharged. NiMH and NiCd cells offer a voltage profile that is 1.8 V in the fully charged state and an end-of-life voltage of 0.9 V.

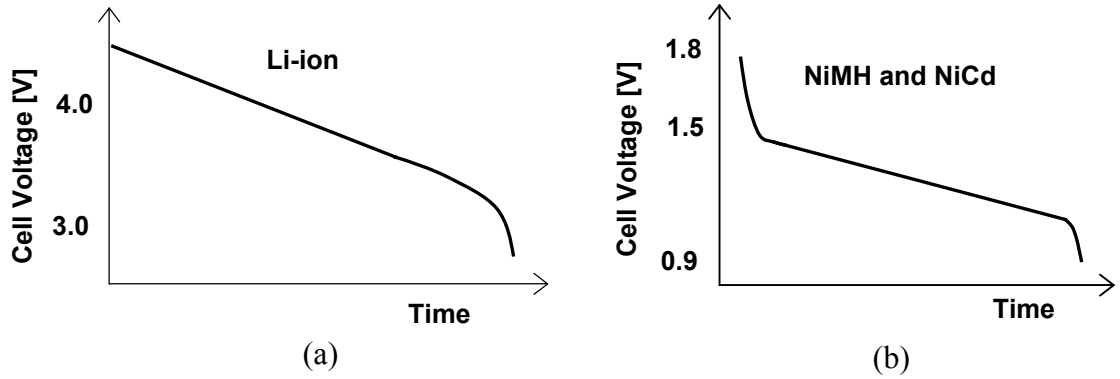


Figure 1.10. Approximate discharge characteristics of (a) Li-ion and (b) NiMH and NiCd batteries [20].

Energy capacity of a given battery is defined by its energy density, which is generally expressed in two ways [20]. The *gravimetric energy density* of a battery is a measure of how much energy a battery contains with respect to its weight, and it is typically expressed in Watt-hours/kilogram. The *volumetric energy density* of a battery is a measure of how much energy it contains in comparison to its volume, and it is typically expressed in Watt-hours/liter. A comparison of energy densities offered by state-of-the-

art batteries is offered in Table 1.1. Because of its higher volumetric energy density and gravimetric energy density, products from Li-ion cells powered are much lighter than the others without sacrificing runtime. However, Li-ion cells typically have higher effective series resistance (ESR), which limits the peak current delivered by the battery and increases power dissipation. The charging circuitry for NiMH and NiCd cells is simpler than that for Li-ion cell. Overall, NiCd offers the best cost-performance value of any rechargeable battery [20].

Table 1.1. Comparison of energy densities of rechargeable batteries [20].

Cell Type	NiCd	NiMH	Li-ion
Gravimetric energy density (W-hr/kg)	55	50	90
Volumetric energy density (W-hr/liter)	180	140	210

1.5.2 Micro-Fuel Cells

Fuel cells are electrochemical devices that convert the chemical into electrical energy [21]. A direct methanol fuel cell (DMFC), based on the chemical reaction of methanol and air, is considered promising because of its capability to store more energy (1 kWh) compared to a Li-ion cell (100Wh) [22]. Increasing battery drain current because of complex applications is the driving force behind the development of energy sources based on fuel cell technology. To manufacture miniaturized fuel cells to match these applications, one of the most interesting paths is to combine planar technology developed for semiconductor devices with silicon micro-machining techniques. Prototypes reported using this approach have demonstrated an energy rate of 1 W at an operating voltage of 3 V with a total volume of 20 cm^2 [19].

The output terminal voltage of a full cell varies significantly with load current. Useful work (electrical energy) is obtained from a fuel cell only when a reasonable current is drawn, but the actual cell potential is decreased from its equilibrium potential

because of several irreversible losses, the details of which is beyond the scope of this dissertation, and can be found in [21]. Figure 1.10 depicts an approximate terminal voltage profile of a single fuel cell, which varies from 1.2 V to 0.2 V, the nominal of which is 0.7 V.

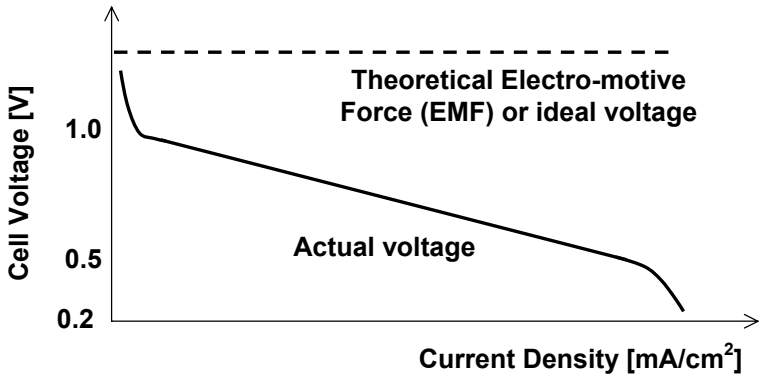


Figure 1.11. Ideal and actual fuel cell voltage/current characteristic [21].

Apart from the power sources described above, other non-conventional energy sources (e.g., vibration, thermal, nuclear, and wireless transmission of power) are being considered as potential energy sources for future portable applications. However, they remain far from becoming viable solutions.

1.6 Introduction to Dynamically Adaptive Power Supplies

Power supplies are ubiquitous building blocks in portable applications, where they efficiently and accurately transform a given battery supply into different voltage levels for their respective loads. Depending on the load requirements, the output voltage of the power supply can be lower or higher than the battery voltage, and they are termed as step-down (buck) or step-up (boost) power supplies, respectively. Figure 1.12 presents a generic power supply circuit, which consists of one or more pass elements with their respective filter components, resistive divider network, and error amplifier connected in a negative feedback configuration. The feedback loop ensures that two voltages at the input of the error amplifier (V_{CON} and V_{FB}) are equal thereby generating output voltage V_{OUT}

depending on the control signal (V_{CON}) and the feedback resistors' ratio. Most integrated power supplies use a bandgap reference voltage as the control signal for the feedback loop, thereby generating a constant output voltage V_{OUT} from input supply V_{IN}.

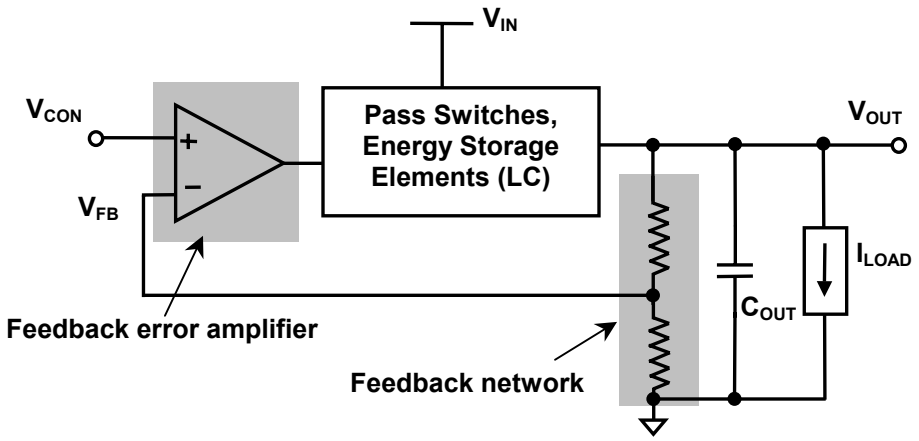


Figure 1.12. Schematic of a generic power supply circuit.

Dynamically adaptive power supplies are the conventional power supply circuits but with their output voltage being varied as a function of time. In principle, any power supply can be used as an adaptive supply provided it is stable under different operating conditions, and the circuit's bandwidth is sufficiently large to track a variable control signal. The primary requirements of power supplies in portable applications are high energy-efficiency, low cost, small size, and low noise.

1.6.1 Power Supply Specifications

Power supply circuits are characterized to quantify their ability to transform an input supply voltage into desired voltage levels as required by their loads. It is desired to have a power supply that incurs minimal power loss so that the input power is effectively transformed into useful power by the load. At the same time, the output voltage of a power supply must be well controlled, during both steady-state and transient circumstances. Several relevant basic performance matrices are explained in the following subsections.

(a) Efficiency: The efficiency of a power supply circuit is defined as the ratio of the output power delivered to the load (P_{OUT}) and the input power drawn from the power source (P_{IN}), and is given by

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}, \tag{1.4}$$

where P_{LOSS} represents the power lost in the supply circuitry. Regulators are always designed to dissipate minimal power and therefore achieve high efficiency. In portable applications, high efficiency power supplies are desired to maximize the battery life.

(b) Line Regulation: Line regulation (LNR) is the ability of a power supply circuit to maintain a constant output voltage as supply voltage changes and it is defined as the variation of its output voltage with a change in its input voltage for a specific loading condition. It is given by

$$LNR = \frac{V_{OUT}|_{V_{IN\_MAX}} - V_{OUT}|_{V_{IN\_MIN}}}{V_{OUT}|_{V_{IN\_MIN}}}, \tag{1.5}$$

where $V_{OUT}|_{V_{IN\_MAX}}$ and $V_{OUT}|_{V_{IN\_MIN}}$ are the output voltages of the regulator with maximum and minimum rated input supply voltages, respectively.

(c) Load Regulation: Load regulation (LDR) is the ability of a power supply circuit to maintain a constant output voltage as load current changes and is defined as the variation of its output voltage with a change in load current for a constant supply voltage. It is given by

$$LDR = \frac{V_{OUT}|_{I_{LOAD\_MAX}} - V_{OUT}|_{I_{LOAD\_MIN}}}{V_{OUT}|_{I_{LOAD\_MIN}}}, \tag{1.6}$$

where $V_{OUT}|_{I_{LOAD\_MAX}}$ and $V_{OUT}|_{I_{LOAD\_MIN}}$ are the output voltages of the regulator with maximum and minimum rated load currents, respectively.

(d) Bandwidth: The bandwidth of a power supply essentially refers to the open-loop bandwidth of the converter's feedback loop. In a given application, a change in loading conditions for the power supply affect its output voltage until the feedback loop responds to adjust control parameters in the loop to correct for the voltage shift. Similarly, converter's output voltage of the converter does not instantaneously reach its target value as desired by the control signal. A faster feedback loop ensures that the power supply circuit responds to load or control voltage changes to maintain the required output voltage with minimum error.

(e) Transient Response: Transient response of a power supply generally refers to the time required by the circuit to respond to load changes. However, in dynamic supplies, the converter's output voltage is varied with a change in its control signal. Therefore, the terms load transient response and control transient response are used to represent load and control signal change characteristics of the power supply. A faster transient response is typically achieved with a larger feedback loop bandwidth. While bandwidth is defined for small-signal perturbations, transient response represents a generic term including large signal event, e.g., slew rate. In practice, during a transient event the converter's response time is initially limited by its slew rate limitations, and subsequently the loop bandwidth comes into play while the output voltage settles down.

1.6.2 Power Supply Circuit Classification

Conventional power supplies used in battery-operated, portable applications can be classified into three categories: (a) Linear regulators (b) Switching regulators, commonly known as *dc-dc converters*, and (c) Switched–capacitor circuits, also known as *charge-pumps*. In the following subsections, these three types of voltage regulators are introduced and their characteristics are described briefly.

(a) Linear Regulators: Linear regulators, also called *series regulators*, use a pass switch between the input supply voltage and the regulated output voltage [23]. The term "series" is derived from the fact that the pass element is connected in series between the input supply and load [24]. An error amplifier controls the switch resistance with respect to a reference voltage. The blocks are arranged in a feedback configuration to maintain constant output voltage irrespective of the loading conditions. Figure 1.13 shows the simplified schematic of a linear regulator with a PMOS pass transistor (MP) used as a variable resistor, which works linearly to maintain the output at its desired level. When the output voltage approaches that of the input supply, the pass transistor operates in the triode region, and the linear regulator is said to be operating in dropout mode. Linear regulators of this genre are commonly known as Low Dropout (LDO) regulators [23].

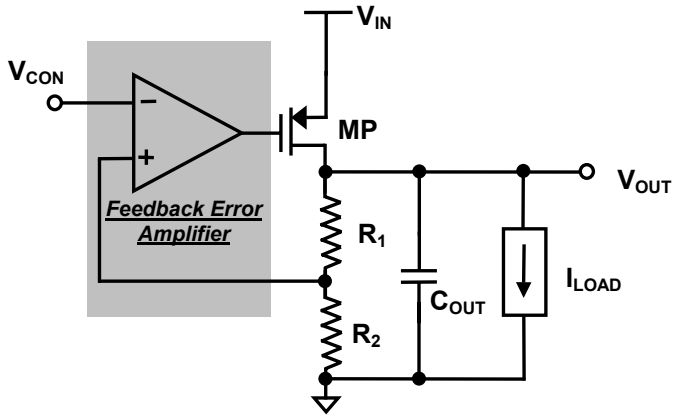


Figure 1.13. Schematic of a linear regulator.

Assuming the current in the feedback resistors and the error amplifier is much smaller compared to the load current, the power loss in a linear regulator is equal to the product of the voltage drop across the regulator ($V_{IN} - V_{OUT}$) and the load current. Hence, its efficiency depends on the difference of input and output voltage and is given by the expression

$$\eta_{LR} = \frac{V_{OUT}\, I_{LOAD}}{V_{OUT}\, I_{LOAD} + (V_{IN} - V_{OUT}) \times I_{LOAD}} \approx \frac{V_{OUT}}{V_{IN}}. \qquad (1.7)$$

Therefore, a linear regulator can only be efficient in applications that require an output voltage that is close to the input voltage, which may be incompatible with the voltage required for the load. Furthermore, the output voltage in a linear regulator must be always less than its supply voltage because of the voltage drop in the pass transistor.

(b) Switching Regulators: Switching regulators are mixed-signal circuits having both digital and analog blocks in the feedback loop. An analog error signal is fed back and digitally gated at a certain frequency rate to produce discrete voltage pulses [22]. Output capacitors and inductors filter these digital pulses into a regulated output voltage. A unique advantage of switching regulators lies in their ability to convert a given supply voltage with a known voltage range to virtually any desired output voltage, with no "first-order" limitation on efficiency. This is true regardless of whether the output voltage is higher (*boost* application) or lower than the input voltage (*buck* application). Figure 1.14 shows the simplified schematic of a buck-type switching regulator.

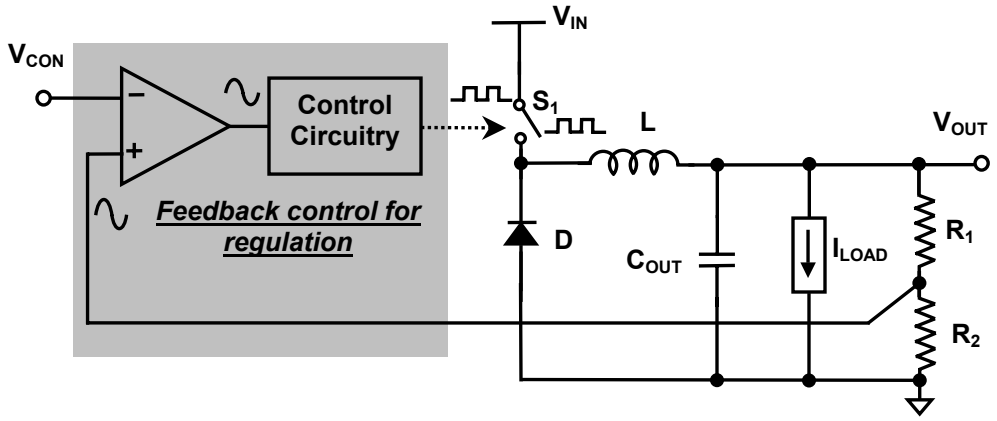


Figure 1.14. Schematic of a step-down switching regulator with a simplified feedback control circuit.

Considering the basic components of a switching regulator, the inductor and capacitor are ideally reactive elements and therefore dissipate no power. The switch is either "on", thus ideally not having voltage dropped across it while current is flowing, or "off", in which case no current flows. Since either voltage or current are always zero, the power dissipation is theoretically zero. The diode has a finite voltage drop while current flows though it, and thus dissipates some power. However, with the diode replaced by a "synchronous switch" having zero-voltage drop across it, the switching regulator ideally does not dissipate any power. In practice, inductors have resistance and their magnetic cores are not perfect either, thus dissipating power. Capacitors have resistance, and as current flows in and out of them, they dissipate power. Switches, which are implemented as transistors, have a finite voltage drop across them as they conduct current thereby dissipating power. Similarly, switches cannot be turned-on and off instantaneously, thereby having finite voltage and current overlap during transitions ultimately dissipating power.

The primary limitations of switching regulators are their output noise, electromagnetic interference (EMI) emissions, complexity, and use of external components. Switching regulators generate ripple currents in their input and output capacitors. As a result, voltage ripples and noise on the converter's input and output, referred to as *conducted* noise, is produced because of the resistance, inductance, and finite capacitance of practical capacitors. Often, there are also ringing (oscillation) voltages in the converter due to parasitic inductances in components and PCB traces, and an inductor which creates a magnetic field that is not perfectly contained within its core – all these contribute to *radiated* noise. Noise is inherent to the operation of a switching regulator and is generally kept within the system specifications with proper component selection, printed circuit board (PCB) layout, and if required, additional input and output filtering [25].

(c) Switched-Capacitor Regulators: Switched-capacitor converters, also known as charge pumps, are widely used in low power ICs, where a voltage higher than or of opposite polarity to the input voltage is needed. Unlike a switching regulator, a switched-capacitor

converter requires no magnetic components –the inductor is essentially replaced by an additional capacitor and a few switches. Figure 1.15 illustrates the basic principle of operation of a switched-capacitor voltage doubler. In principle, the capacitors are pre-charged in parallel and then connected in series with the input supply, thus generating an output voltage higher than the supply voltage.

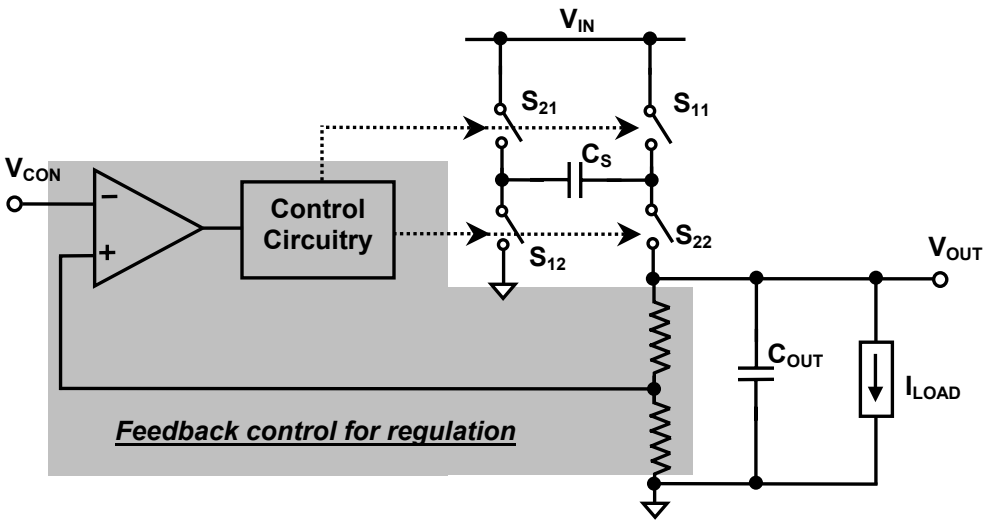


Figure 1.15. Schematic of a switched-capacitor voltage doubler and its respective control circuit.

Switches S_{11} and S_{12} are closed during one interval of the switching period, charging capacitor C_S to input voltage V_{IN}. During the other interval of the switching period, switches S_{21} and S_{22} are turned on and the voltage across capacitor C_S is placed in series with the input to generate an output voltage that is higher than the input. When the two switching intervals are equal, the output voltage is twice the input voltage and hence the circuit is known as a *voltage doubler*.

To generate an accurate output voltage, a simple switched-capacitor voltage converter can be regulated in three different ways. The most straightforward method is to follow the switched capacitor circuit with a low dropout (LDO) regulator, which provides the regulated output with a lower ripple voltage compared to that of an unregulated switched-capacitor converter. Figure 1.15 shows one possible scheme where the output

voltage is regulated by varying the ratio of on time to the total switching period (known as *duty cycle*) of the switches, which is similar to that used in inductance-based switching regulator. This approach is highly nonlinear and requires long time constants to maintain good regulation [24]. The most effective method for achieving regulation in a switched-capacitor converter is to use an error amplifier to control the on-resistance of one of the switches [24]. Although the theoretical efficiency of switched-capacitor converters is 100%, in practical applications switch resistances, equivalent series resistance (ESR) of capacitors, and the inherent switched-capacitor resistance [given by $1/(fC_S)$, where f is the switching frequency of the converter] degrade the efficiency.

A comparative evaluation of various power supply circuits is presented in Table 1.2, which concludes that switching regulators, in spite of their higher complexity and noise, are best suited for power supplies in PA driven portable applications because of their high efficiency and large power handling capability.

Table 1.2. Comparative evaluation of basic power supply circuits.

Parameters	Linear Regulator	Switching Regulator	Switched- Capacitor Regulator
Efficiency	Low	High	Medium
Power Rating	Medium	High	Medium
Size (PCB Real Estate)	Compact	Large	Moderate
Cost and Complexity	Low	High	Medium
Noise	Low	High	Medium

1.6.3 Efficiency and Bandwidth Perspective in Adaptive Switching Regulators

The power loss in a switching regulator is the sum of the conduction and the switching losses. Conduction loss is dependent on load current –the higher the load current, the higher is the conduction loss. On the other hand, switching loss is proportional to the switching frequency, which is normally independent of loading conditions. Under light loads, the efficiency of the converter is dictated by its switching losses; therefore, a lower switching frequency should be used during low loading

conditions to achieve high overall converter efficiency. Unfortunately, the size of the external inductor and capacitor increase with lower switching frequency, if the ripple voltage is to remain low for accuracy, which is inconsistent with low external component count and cost-effective system-on-chip (SOC) solutions for portable applications.

Figure 1.16 shows the typical feedback loop configuration of a switching regulator in pulse width modulation (PWM) control highlighting its key elements and their respective frequency responses. The location of poles and zeros of the switching converter's power stage depend on its functionality (step-up or -down) and feedback variables, e.g., output voltage, inductor current, used in the controller for output regulation. Typically, the feedback compensation network in a dc-dc converter is designed to maximize the bandwidth while still ensuring a stable operation.

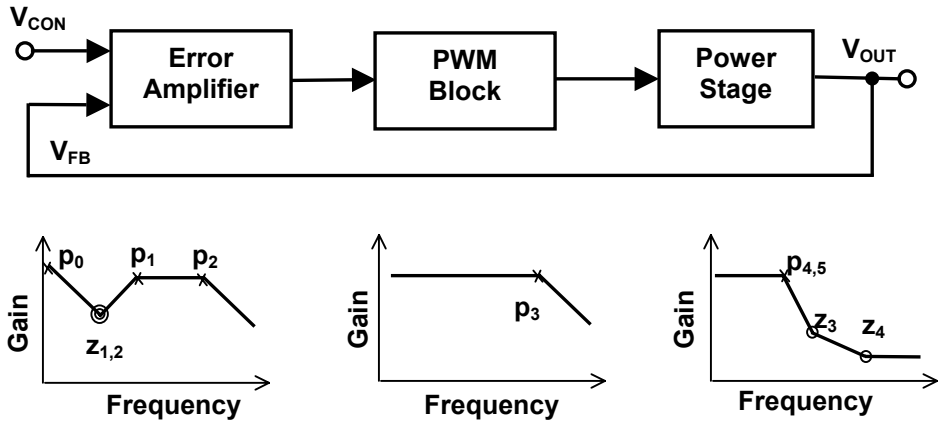


Figure 1.16. Block diagram of a switching regulator illustrating key building blocks along with their representative frequency responses.

The bandwidth of a dc-dc converter's feedback loop is limited to one-tenth of the switching frequency [27] such that sufficient gain roll-off is achieved at the switching frequency to desensitize the effect of converter's switching noise on the feedback control loop operation. For a wider bandwidth, the converter switching frequency must be increased, which increases switching losses, and consequently lowers light-load efficiency. In boost and buck-boost converters operating with continuous inductor current

[continuous-conduction mode (CCM)], the right-half plane (RHP) zero must be designed to reside at a higher frequency with respect to the desired unity-gain frequency (UGF), which can be accomplished by selecting a smaller power inductor value. For a fixed switching frequency, having a smaller inductor results in larger peak-to-peak inductor current, which in turn increases the root-mean-square (rms) current rating of the power switches and induces more conduction losses in the current-flowing path. The trade-offs just mentioned are summarized in Table 1.3.

Table 1.3. Summary of trade-offs involved in designing a wide-bandwidth and high-efficiency switching converter.

Considerations	Higher switching frequency	Lower switching frequency
Light-load Efficiency	Decreases	Increases
Bandwidth	Increases	Decreases
External components' size	Decreases	Increases

1.7 Research Objective

The objective of this research is to design and develop an integrated, energy-management framework for linear RF PAs in portable applications capable of operating from a power source with wide variation in supply voltage. The above goal is targeted to fulfill the state-of-the-art requirements of a single-cell Lithium-ion battery, low-cost NiMH and NiCd batteries, while anticipating the future market potential of other portable power sources, e.g., fuel-cells. The efficient linear RF PA is realized by a dynamically adaptive supply voltage and bias current control scheme such that the quiescent power consumption of the PA is adjusted with its transmitted output power, thereby maximizing the system efficiency, and ultimately prolonging battery life. The concepts are developed for CDMA and WCDMA wireless systems, but can be extended to other schemes with similar characteristics, e.g., large output power dynamic range, high peak-to-average ratio, etc. The challenges in realizing such a system are offered below.

(a) Linear RF PA over a wide dynamic range: Generally, the PA nonlinearity is at its worst when the amplifier operates at its peak output power. The PA is therefore operated at a power back-off to meet the linearity specification required by industry standards, which essentially implies a higher quiescent power loss and consequently a degradation in power efficiency. The presence of undesired voltage ripple at the PA supply rail modulates its transconductance, which creates in-band and out-of-band distortion of the transmitted RF signal. Therefore, maintaining the PA's linearity performance when it transmits RF signals with lower signal strength requires accurate power supplies with small ripple voltages.

(b) High efficiency over wide loading conditions: With the PA output power dynamic range varying over 80 dB in a CDMA/WCDMA system, the energy-management framework must be efficient throughout the loading conditions to maximize transformation of battery power into useful transmitted RF power. With a fixed bias (supply voltage and current), the PA is designed to meet the linearity at peak output power exhibits degraded efficiency as the transmitted power is reduced. Unfortunately, power supplies designed for peak-efficiency at a maximum power have low efficiency for low output power, and the load-independent switching power losses dominate the converter's total efficiency performance. Therefore, maintaining high efficiency over wide loading conditions is an increasingly challenging task, and it warrants scrutiny when designing for longer battery life.

(c) Fast response, output slew rate, and settling: As the PA output power is dynamically adjusted with the RF transmitter entering and exiting various operational modes (e.g., high-speed data, multimedia, voice only, etc.), the energy management system must be able to quickly adapt to these changes such that the PA performance is not compromised. While a converter with extremely fast transient response seems to be an intuitive solution for such an applications, efficiency, accuracy, and supply voltage considerations decipher other challenges, which mandates the adaptation a balanced approach to meet the various targets in a cost-efficient manner.

(d) Wide supply voltage range: To maximize the battery energy in state-of-the-art portable sources, power supplies with both step-up and -down capabilities are best suited for a portable environment. For example, in a Li-ion cell (4.2 – 2.7 V) powered application the required output voltage (say, 3.0 V) can be higher or lower than the supply voltage, thereby requiring a buck-boost supply. The higher end of supply voltage defines the process technology suitable for designing the IC. When a process technology is selected considering the higher supply voltage range, threshold voltage of the devices present a bottleneck to achieve the desired input and output dynamic range while the system is operated at the lower end of the input supply. These challenges require development of building blocks with low voltage circuit design techniques.

Performance of the PA is extremely important for the overall transmitter and should meet the system specifications with the power management system in place. The overall system must meet the ACPR requirements over its entire power range. The key specifications the power amplifier in CDMA and WCDMA applications [28], [29], are listed in Table 1.4. The frequency bands used by CDMA IS-95 for transmitting RF signals are in the range of 824-849 MHz and 1850-1910 MHz, while WCDMA mobile stations use 1920-1980 MHz frequency band.

Table 1.4. Key specifications of CDMA IS-95 and WCDMA power amplifiers in portable handsets.

Specification	CDMA IS-95[1]	WCDMA[2]
Base band signal BW	1.25 MHz	3.84 MHz
PA maximum transmit power	28 dBm	27 dBm
PA typical transmit power	–10 to +15 dBm	–10 to +15 dBm
Modulation	OQPSK	QPSK
1st ACPR @ 995 KHz, 30 KHz BW[1] @ 5 MHz, 3.84 MHz BW[2]	–44 dBc	 –32 dBc / –50 dBm
2nd ACPR @1.98 MHz, 30 KHz BW[1] @10 MHz, 3.84 MHz BW[2]	–60 dBc	 –42 dBc / –50 dBm

1.8 Summary

In this chapter, the role of efficient, linear RF PAs to meet the linearity requirements and maximize battery life in state-of-the-art CDMA and WCDMA wireless portable systems is established. With convergence of multitude of functionalities, e.g., voice, data, imaging, etc., in a single device, smart power management systems continue to play a crucial role in the growth and evolution of portable applications. The RF PA, being the power-hungry block in a radio transceiver and operating with a output power dynamic range over 80 dB, maintaining high efficiency over a wide loading conditions while achieving desired linearity specifications (ACPR and EVM) is critical for optimal battery usage. Since the state-of-the-art batteries exhibit a wide variation in their terminal voltages, power supplies with both step-up and -down capabilities are essential to utilize the entire battery energy.

A comparative evaluation of power supply circuits reveals that switching regulators, irrespective of their complexity and noise, are best suited for PA-driven applications because of their high power conversion efficiency and large output power handling capability. Typically, dynamically adaptive supplies require a higher switching frequency to achieve larger bandwidth, but at the expense of their light-load efficiency. Power converters operating at a higher switching frequency need smaller external components (inductors and capacitors), which is conducive towards portable systems. The objectives of the research with the goal of realizing an energy-efficient linear RF PA with a dynamically adaptive supply and bias current control scheme are then identified. Subsequently, the challenges of the research, e.g., maintaining PA's linearity over a wide dynamic range, achieving high efficiency, and requirement of low voltage design techniques to operate the system under a wide supply range are discussed.

This chapter essentially forms the background for evaluating various PA system architectures suitable for CDMA/WCDMA handsets, which is discussed in the next chapter. The concepts developed in this dissertation can be extended to other application areas of linear RF PAs, e.g., IEEE 802.11 based wireless local area networks (LANs) employing orthogonal frequency division multiplexing (OFDM) modulation scheme and third generation (3G) wireless platform, Enhanced Date for GSM Evolution (EDGE).

CHAPTER II

EFFICIENT LINEAR RF POWER AMPLIFIER DESIGN

The key to improving battery life in portable applications with radio transmitters for wireless connectivity, e.g., code-division-multiple-access (CDMA) modulation based cellular phones, orthogonal-frequency-division-multiplexing (OFDM) based wireless local area network (WLAN) assisted handheld devices, is to operate the power-hungry PA with a linearity that is just enough to meet the required specification, while minimizing the power drained from the battery. In a portable environment, the circuit complexity is a major design consideration, where both the silicon and printed circuit board (PCB) real estate are crucial, not to mention the increase in cost with each additional external component. Therefore, design and development of linearization or efficiency enhancement schemes for PAs must be evaluated with respect to the additional complexity they impose on the system design.

In this chapter, classification of RF PAs and the associated linearity-efficiency trade-offs are reviewed. Various PA linearization and efficiency enhancement techniques are categorized and evaluated with respect to their applicability for battery-powered wireless handsets. In essence, development of an efficient linear RF PA is considered based on two different paradigms: (a) using an inherently efficient non-linear PA with a linearizing circuit, or (b) having a linear PA with additional circuitry for efficiency enhancement. A comparative evaluation of the efficiency enhancement and linearization techniques is also offered. Finally, a novel linear RF PA scheme with dynamically adaptive supply voltage and bias current control is proposed and its characteristics are presented.

2.1 RF PA Topologies

Figure 2.1 shows the typical output stage of a MOS RF PA, which consists of an output transistor, an RF choke, and input and output impedance matching networks. The behavior of this amplifier is defined by the portion of total time for which the output (drain) current flows in the transistor, knows as *conduction angle*, and its input signal drive. Depending on the biasing conditions the output current flow in a transistor can be for the complete cycle or a part of it when subjected to an input sinusoidal signal. If the transistor remains in the saturation region for the entire cycle of the input signal, its conduction angle is 360^0.

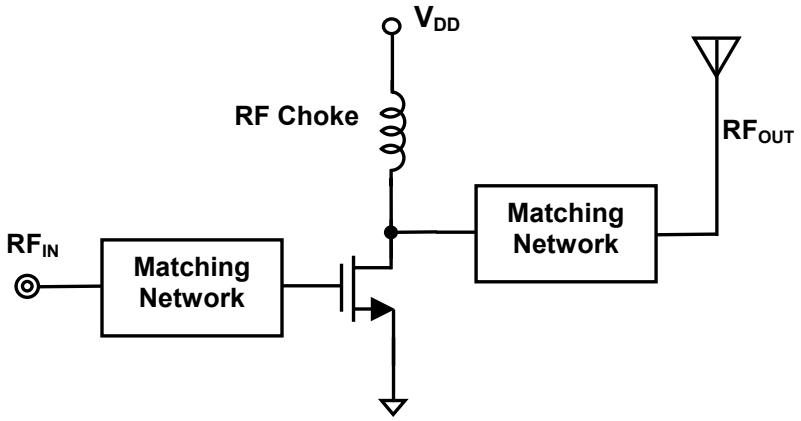


Figure 2.1. Simplified output stage of an MOS RF PA.

Figure 2.2 shows the load-line characteristics of a MOS RF PA, highlighting the quiescent points in class A, AB, and B mode of operation. For a small input RF signal, the amplifier as shown in Figure 2.1 can operate as class A, AB, B, or C depending on its conduction angle, which is determined primarily by its gate bias. A class A amplifier is the one in which the operating point and input signal level are chosen such that the drain current flows at all the times, yielding a 360^0 conduction angle. The transistor therefore operates in the linear potion of its characteristics and hence the output signal suffers minimal distortion. A class-B amplifier is biased such that there is no quiescent current flow, and the transistor conducts only when input signal is present. A class-AB amplifier

is a compromise between the two extremes of class-A and class-B operation. In class C operation, the operating point is selected such that there is no current flow in the transistor for more than half of the input sinusoidal signal cycle.

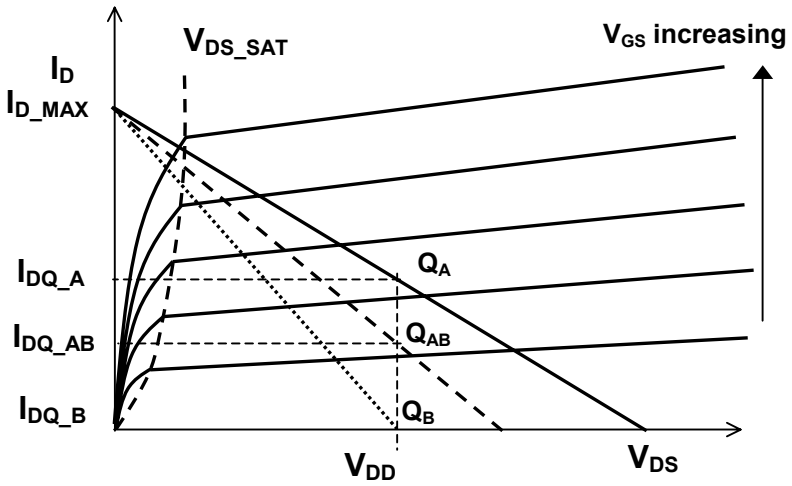


Figure 2.2. Load line in MOS RF PA for Class-A, -AB and -B modes of operation.

For class-A, -AB, -B, and -C amplifiers, the PA efficiency is improved by reducing the conduction angle, and thereby lowering the quiescent power dissipation, which however comes at the expense of a lower output power. Alternatively, a transistor can be operated as an on-off switch by increasing its gate overdrive. In a switch-mode circuit, the transistor operates either in the linear or cut-off region with its output reaching the power supply rail and ground, respectively. The amplifier's output does not contain any information about the amplitude of the signal, and therefore it is not suitable for linear amplification. Since the voltage and current in a switch-mode amplifier overlap for a tiny fraction of the total time, it incurs a lower power loss. Therefore, efficiency of a switching-mode circuit is improved but at the expense of linearity. The classifications of power amplifiers based on conduction angle and input signal drive described in this section is summarized in Figure 2.3 [30].

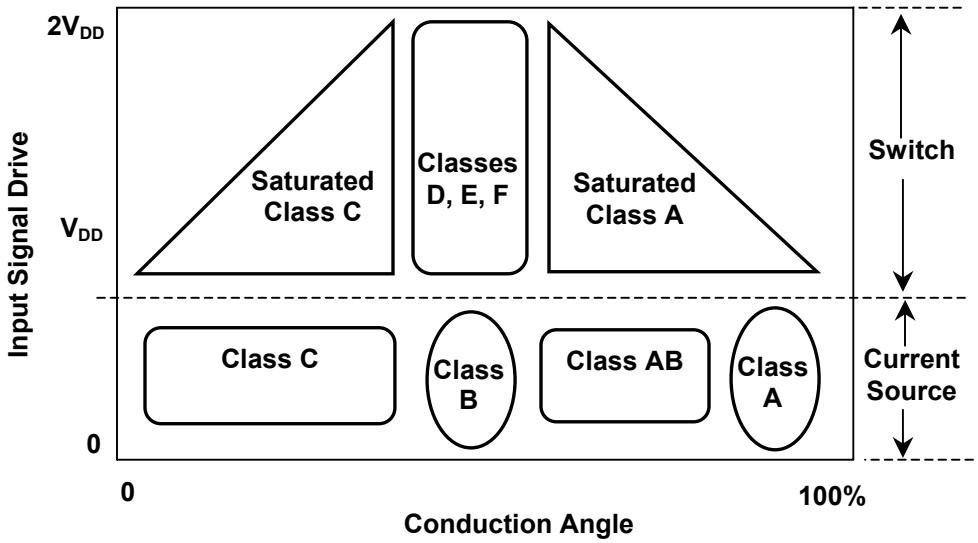


Figure 2.3. Classical definition of RF PAs based on conduction angle and input signal overdrive [30].

The gate overdrive of an RF PA essentially determines the trade-off between its linearity and efficiency. When the output transistor is biased in class-A configuration, its drain voltage V_D is an amplified version of the RF input signal RF_{IN}. The power dissipated in the transistor (P_D) is the product of drain voltage (V_D) and drain source current (I_D). With an increase in overdrive, ideally, the output transistor operates as a switch with no overlap between V_D and I_D, yielding zero power loss P_D. With no power lost in the transistor, all the power from the dc supply is transferred to the output, resulting in a theoretical efficiency of 100 %. However, in a practical RF PA, there are losses due to the overlap of drain current and voltage, as well as the finite on-resistance of the output transistor.

A summary of various classes of PA operation and their maximum theoretical efficiency values are offered in Table 2.1. A class-A and -B amplifier exhibits a maximum theoretical efficiency of 50 % and 78.5 %, respectively. An amplifier in class-C mode shows a maximum theoretical efficiency of 100 %, which is same as that for switch-mode amplifiers.

Table 2.1. Summary of RF PA classification and characteristic based on their operation.

Class	Conduction Angle	Max. Theoretical Efficiency	Comments
A	360^0	50 %	▪ Linear amplifiers, minimum distortion ▪ Degraded efficiency at the expense of higher linearity
AB	180^0 - 360^0	50 % < η< 78.5 %	▪ Most commonly used mode ▪ Good compromise between output power, efficiency, gain and linearity
B	180^0	78.5 %	▪ PA self biases when driven with RF power ▪ Good efficiency over a large output power at the expense of linearity
C	$<180^0$	100 %	▪ Minimal time in active region for better efficiency ▪ Zero output power at zero conduction angle with peak efficiency
D, E, F	$<180^0$	100 %	▪ Switch-mode amplifiers (D, E) ▪ Harmonic control for better efficiency (F)

Table 2.2 presents a systematic representation of the efficiency degradation for Class-A and -B PAs while amplifying a variable envelope RF signal. As discussed in Section 1.3, state-of-the-art, spectrally efficient modulation schemes transmit information in both the amplitude and phase of the RF signal, leading to complex signal waveforms with high peak-to-average ratios. When a PA amplifies these signals with complex envelopes, its efficiency decreases compared to the single-tone sinusoidal signal amplification, since the PA is operated in a power back-off mode so that signal peaks do not experience any clipping. For a class-A amplifier the input supply power remains constant even if the output power reduces, therefore the efficiency decreases linearly. For the amplifiers operating in class-B mode, the current drawn from the power supply reduces proportionately with output voltage. Therefore, the efficiency decreases linearly with output voltage, which is square-root function of the output power. Briefly, complex

signal amplification in class-A and -B PAs is a linear and a square-root function of the output power, respectively.

Table 2.2. Efficiency comparison of class A and B PAs for single-tone and variable envelope signal amplification.

Parameters	Class A	Class B
DC input power ($P_{IN} = V_{DD} I_{SUPPLY}$)	$\frac{V_{DD}^2}{R}$	$\frac{V_{DD} \cdot 2V_{OUT}}{\pi R}$
Output power ($P_{OUT} = V_{OUT} I_{OUT}$)	$\frac{V_{OUT}^2}{2R}$	$\frac{V_{OUT}^2}{2R}$
Maximum efficiency (η_{MAX})	$\frac{V_{OUT}^2}{2V_{DD}^2}$	$\frac{\pi V_{OUT}}{4V_{DD}}$
Efficiency at back-off power ($V_{OUT} < V_{DD}$) (Single-tone sinusoidal signal)	$\eta_{MAX} \frac{P_{OUT}}{P_{OUT\_MAX}}$	$\eta_{MAX} \sqrt{\frac{P_{OUT}}{P_{OUT\_MAX}}}$
Peak efficiency ($V_{OUT} = V_{DD}$) (Single-tone sinusoidal signal)	50 %	78.5 %
Peak efficiency (CDMA signal with 5 dB peak-to-average ratio)	15.8 %	44.2 %

2.2 Linearization Techniques of RF PAs

Linearization techniques are targeted to improve the linearity of a PA with the use of additional signal processing circuitry. Most linearization techniques are used for improving peak power efficiency; however, little attention is normally given to their applicability in a system operating with a large output power variation. Because of their complexity and higher cost, linearized RF PAs are commonly used in wireless base-station environments [31]. Moreover, base-stations are likely to be operated at their peak output power for a much longer duration than mobile stations, where the output power varies significantly, especially in communication systems with inherent power control schemes. State-of-the-art linearization techniques can be broadly classified into various categories depending on the methodology adopted to realize the linear PA. In some cases,

a combination of several techniques [30] is used to achieve further linearity improvements, especially when the targeted application environment demands stringent specifications. Various linearization schemes are briefly discussed in the following subsections.

2.2.1 Direct Feedback

The simplest and most obvious technique to improve the amplifier's linearity is to use negative feedback, which is widely pursued in the design of low frequency analog circuits. Direct feedback is a familiar enough concept, but its implementation at RF and microwave frequencies is not beneficial and sometimes not practically feasible because of stability and time causality conflicts [2]. Therefore, most linearization techniques use indirect feedback, which are reviewed in the following subsections.

2.2.2 Envelope Feedback

Figure 2.4 illustrates a simplified block-level representation of the PA linearization scheme employing envelope feedback. The main idea of envelope feedback is to control the gain of the PA – one way is to change the bias current of the transistor. If the amplifier operates well below the saturation region where the output is linearly proportional to its input power, the feedback loop forces the output envelope to replicate the input envelope, and substantial improvement in spectral density is attained. However, the envelope feedback scheme is not effective in the region of device operation where the output power is saturated (the output power remains unchanged even if input power increased) and, as a result, the envelope swings into the gain compression (nonlinear) regime.

The error amplifier's bandwidth must be two orders of magnitude greater with respect to the bandwidth of the envelope signal [2] for proper operation. Furthermore, the linearization accuracy is greatly affected by the accuracy and linearity of the envelope detectors. In addition, the nonidealities of the feedback loop, e.g., offset of the error amplifier, can lead to AM-PM distortion of the overall system.

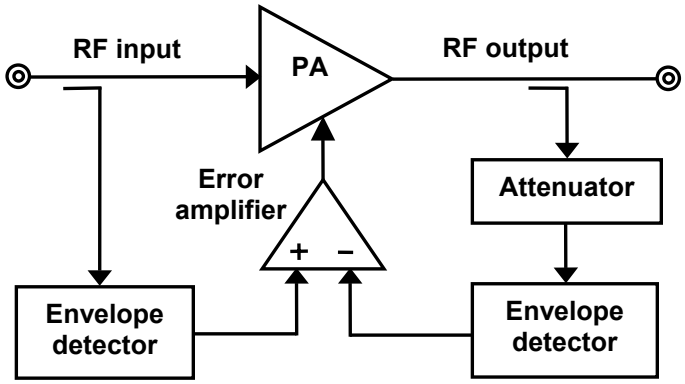


Figure 2.4. Linearization of an RF PA using envelope feedback.

2.2.3 Polar Loop Feedback

Polar feedback linearization scheme is a logical extension of the simple amplitude feedback scheme, where both amplitude and phase correction are performed. Although it looks simple from the block-level schematic, the practical difficulties associated with measuring differential phase changes at microwave signal frequencies poses significant challenges in its practical circuit implementation. Therefore, in almost all realizations, some form of down conversion or sampling is used to accomplish phase correction.

Figure 2.5 shows a block diagram of a basic polar loop system [33], which addresses both phase and amplitude distortion with two separate feedback loops. The output of the RF PA is attenuated and down converted using a local oscillator and mixer. The envelope of the incoming intermediate frequency (IF) signal and down-converted RF output are compared and subsequently the bias condition of the PA is adjusted via one of the error amplifies in a negative feedback loop. Similarly, the phase of the RF output is compared with the incoming IF with necessary phase correction and subsequently up-conversion is performed using a voltage-controlled oscillator (VCO). Obviously, the linearization scheme considers the system-level implementation rather than just the amplifier. The key issues arise from the bandwidth requirement of both amplitude and phase amplifiers.

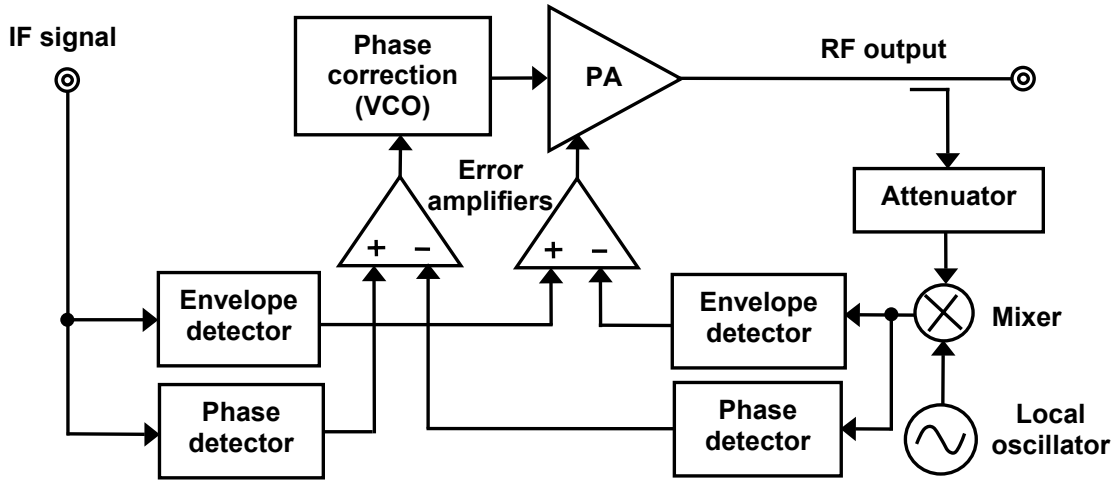


Figure 2.5. Linearization of an RF PA using polar signal feedback.

A polar feedback loop linearization scheme without down conversion of the RF signal has been used for enhanced data rates for GSM evolution (EDGE) system [34]. The amplitude error is derived from the difference between the reference (incoming) and feedback (output) signal envelopes. The detected phase error is the actual phase between RF reference and feedback signal. A delay line is inserted in the reference path so that phase comparison for the correct signal sequence takes place.

2.2.4 Cartesian Feedback Loop

The use of quadrature modulation schemes and the availability of the baseband signal in many of the current wireless systems offer the benefit of processing in-phase (I) and quadrature-phase (Q) signals in well-matched paths. Therefore, the problems of different bandwidth and signal processing requirements for magnitude and phase paths in the polar loop implementation can be eliminated by processing the I- and Q- signals.

Figure 2.6 shows the simplified schematic of an RF PA linearization scheme using Cartesian feedback [6]. The separate I- and Q-signal inputs are filtered binary symbol sequences, which are fed through differential correcting amplifiers into vector modulators that generate the actual RF signal. The amplified RF signal from the PA output is coupled and down converted, and the retrieved I- and Q-signals are compared

with the original signals. The accuracy of the system greatly depends on the gain and bandwidth of the error amplifiers and the linearity of the down converter demodulators.

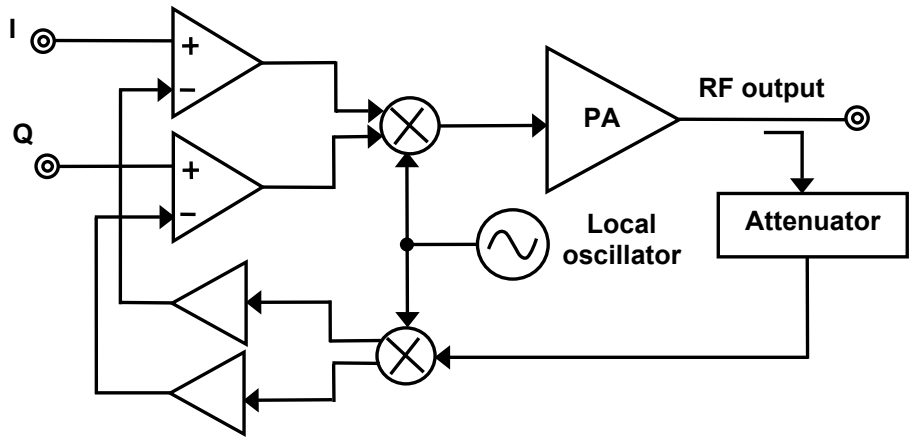


Figure 2.6. Linearization of an RF PA using Cartesian feedback.

The symmetry of gain and bandwidth in the two quadrature-signal-processing paths reduces the possibility of introducing AM-AM and AM-PM errors at the output. With DSPs as the centerpiece of many digitally modulated transceivers, digital linearization schemes are possible, but performance of ADCs present a major bottleneck in the process of closed-loop linearization. Like the polar feedback scheme, Cartesian feedback also warrants a system level approach to the problem of linearization. A comprehensive treatment of Cartesian feedback linearization system is found in [35].

2.2.5 Predistortion

Predistortion can be viewed as an open-loop linearization technique. Although it suffers from the problem of accuracy, like any other open-loop systems, the bandwidth and stability limitations are absent. Figure 2.7 illustrates the simplified schematic of an RF PA linearization scheme using analog predistortion technique. The predistorter has the inverse function of the PA. Since the characteristic of the PA can change over time,

the predistorter transfer function must be modified simultaneously to compensate for the PA fluctuation, which leads to the concept of adaptive predistortion.

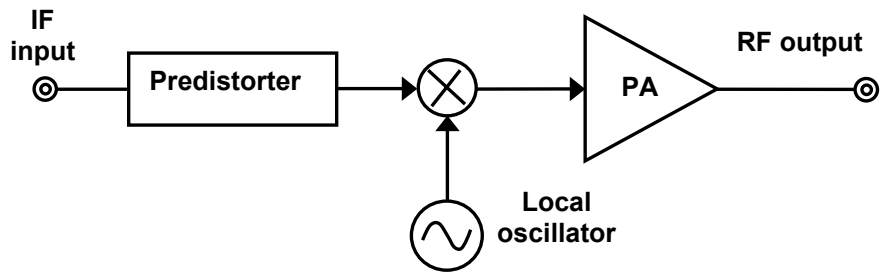


Figure 2.7. Linearization of an RF PA using predistortion method.

Adaptive predistortion addresses the problem of accuracy, drift, and aging effects by modifying the transfer function of the predistorter from the initially measured nonlinear PA characteristics. Figure 2.8 illustrates a digital implementation of an adaptive predistorter using Cartesian feedback mechanism. In the normal operation, the system operates as an open-loop predistorter, with the lookup table providing a preprogrammed I-Q output pair for each input envelope sample, which contained appropriate phase and amplitude correction. The system has an offline adaptation mode, where it behaves as a closed-loop Cartesian correction loop and the lookup table is simultaneously programmed for a particular signal environment [2].

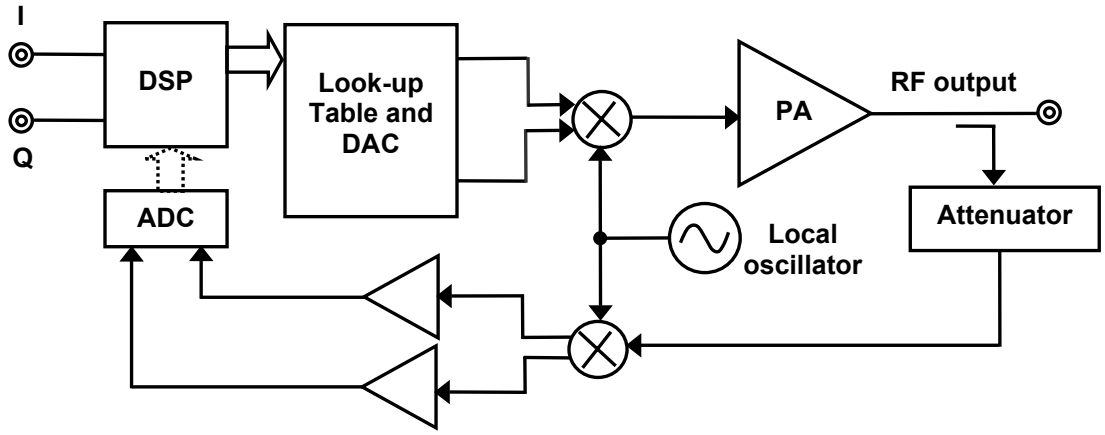


Figure 2.8. Digital adaptive predistortion system.

In an RF system, the already existing DSP can be used for the linearization system. Although the peak-power efficiency is increased by operating the PA in its gain compression region where it exhibits higher efficiency, this method suffers from the inability to operate with reasonable power efficiencies at low PA output power levels, especially when the transmitter power varies over a large range.

2.2.6 Feedforward System

Figure 2.9 illustrates the basic schematic of an RF PA using a feedforward linearization scheme. The radio frequency signal is divided in two parts, one portion of the input signal is amplified through the main PA and the other part of the signal is processed through a delay element. The amplification error in the main PA is amplified through an auxiliary error amplifier. Finally, the output of both the main PA and error amplifier are combined together to generate the actual output signal.

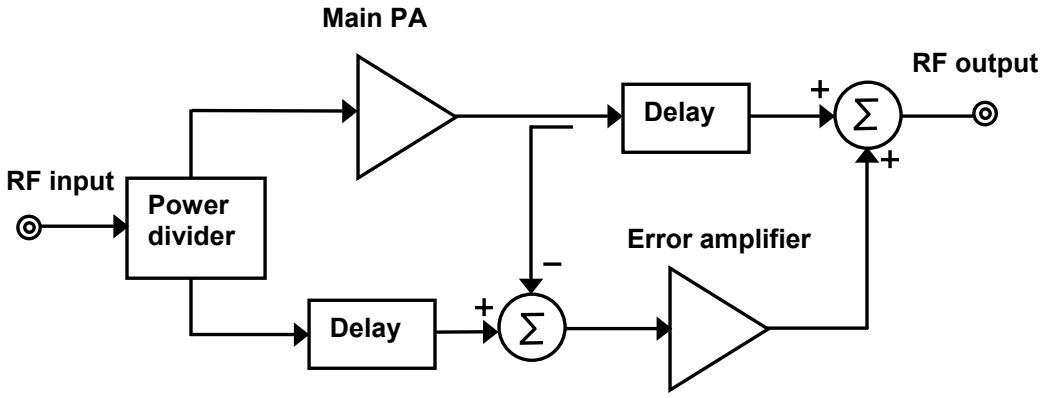


Figure 2.9. Simplified schematic of feedforward PA scheme.

Feedforward correction does not degrade the gain of the amplifier. This is in contrast to the feedback system where the linearity is achieved at the expense of gain. Gain-bandwidth is conserved in the range of interest and correction is independent of the magnitude of the amplifier delays within the system. Moreover, the basic feedforward configuration is unconditionally stable. The error amplifier needs to process only the main amplifier distortion information and hence can be of much lower power than the

main amplifier. Thus, it is likely that a more linear and lower noise error amplifier can be designed.

The changes in device characteristics with time and temperature are not compensated, however. The open-loop nature of the feedforward system does not permit it to assess its own nature and correct for the time variations in the system components; therefore, performance of the system is expected to degrade with time. The matching between the circuit elements in both amplitude and phase must be maintained to a very high degree over the correction bandwidth of interest. The circuit complexity of the feedforward scheme is therefore greater than that of the feedback system, particularly with the requirement for a second (error) amplifier, which leads to higher cost and larger silicon area. In addition, the efficiency of the overall system is significantly degraded because two amplifiers are used.

2.2.7 Linear Amplification with Non-linear Components

The concept of linear amplification with nonlinear control (LINC) is rather straightforward. Also known as out-phasing amplifier (originally developed by Chireix in 1930s [9]), the circuit operates by resolving an amplitude- and phase-modulated signal in two separate *constant envelope* signals, which are applied to highly efficient and nonlinear PAs, whose outputs are the summed together to reconstruct the amplified output signal. A simplified schematic of a LINC system is shown in Figure 2.10.

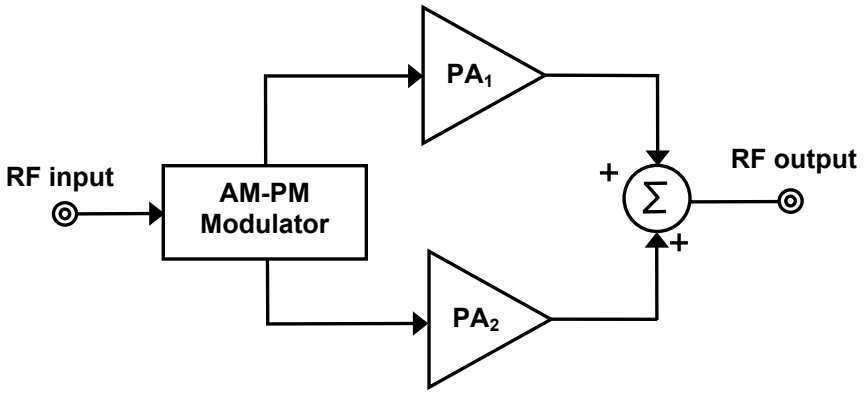


Figure 2.10. Schematic of linear amplification with nonlinear components (LINC) scheme.

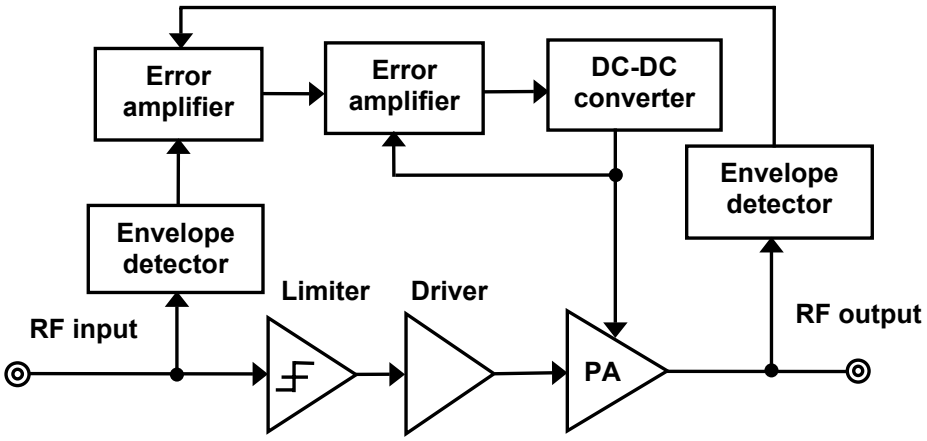
In a LINC scheme, since each amplifier is operated with high efficiency, the overall system efficiency could be potentially higher. In practice, the matching conditions of the two amplifying paths are difficult to achieve and maintain due to process variation, thermal drift, component aging, and transition of channels [9].

2.2.8 Envelope Elimination and Restoration

The Envelope Elimination and Restoration (EER) technique [36] combines a nonlinear RF PA with an envelope amplifier, the schematic of which is shown in Figure 2.11. The envelope amplifier is built with a pulse-width modulated (PWM) buck converter. While EER achieves high peak-power efficiency, the necessarily high switching frequency converter results in lower efficiency at power back-off because of higher switching losses. To suppress the 4^{th}-order harmonics in the envelope amplifier, the desired converter bandwidth must be four times the envelope bandwidth [37], [38]. Assuming that the unity-gain frequency of the converter is limited to one-fifth of its switching frequency, numerical values of the DC-DC converter's bandwidth and switching frequency for CDMA and WCDMA applications are given in Figure 2.11.

Although EER shows improvement in peak-power efficiency [36], because of the high converter switching frequency requirement and consequently higher switching losses, light-load converter efficiency is degraded, thereby decreasing overall system efficiency. Other challenges in designing an integrated circuit implementation of the EER scheme are: (a) an RF delay line is required for accurate recombination of the envelope signal and the constant amplitude RF signal because of the delay mismatch in the envelope and RF signal amplification paths, (b) difficulty in detecting and restoring low power envelope signals (–80 dBm), (c) substantial AM-to-PM conversion in active limiters at high frequencies corrupts the RF signal phase [39], and d) the envelope detector and dynamic converter supply must be linear. At present, the Kahn EER technique has only been shown for a 30 KHz base-band applications {North American Digital Cellular (NADC) applications} using a delta modulated envelope amplifier [40]. Recent result [41] using a delta-modulated buck converter operating up to a switching

frequency of 200 MHz show a high-efficiency CDMA RF PA, but its applicability over the entire output power dynamic range has not been reported.



	CDMA IS-95	WCDMA
Baseband BW	1.25 MHz	3.84 MHz
Converter BW	5 MHz	15.36 MHz
Switching frequency	25 MHz	76.8 MHz

Figure 2.11. Kahn envelope elimination and restoration scheme and requirements of the dc-dc converter for CDMA IS-95 and WCDMA specifications.

2.2.9. Comparative Evaluation of PA Linearization Techniques

A summary of state-of-the-art linearization schemes highlighting their key advantages and disadvantages is presented in Table 2.3. The feedback, polar and Cartesian systems are complex and require a complete transmitter level implementation. Adaptive predistortion and linear combination with nonlinear component (LINC) schemes are attractive alternatives, because they improve the peak power efficiency by using a nonlinear PA, but complexity of the overall system undermines the advantages. Feedforward systems are even more complex and not suitable for a portable handset

environment. EER is more appropriate for the integrated power management domain; however, the necessity of high switching frequency power supplies needed for high base-band bandwidth systems remains a bottle neck to achieve high efficiency over wide loading conditions.

Table 2.3. Comparative evaluation of PA linearization schemes.

	Advantages	Disadvantages
Envelope feedback	• Simple	• AM-PM distortion problem
Polar feedback	• Both amplitude and phase correction are possible	• Requires overall system consideration • Complex circuit and signal processing requirement
Cartesian feedback	• Linearity depends on the feedback mixer, which is easier to achieve at lower power level	• Requires overall system consideration • Complex circuit and signal processing requirement
Analog Predistortion	• Simple	• Requires good PA characterization • Performance degradation due to aging, drift and process variation
Digital Predistortion	• Compensates for process variation and drift	• Overall system needs to be considered for linearization
LINC	• Theoretically provides a high efficiency platform	• Lossy on-chip power combining • Matching difficulties
Feed forward	• Absence of stability problem and gain reduction	• Difficulty in matching and loss-less delay implementation • Drift and variation in process and over time • Reduced efficiency due to extra PA
EER	• High peak-power efficiency	• Large converter BW and higher switching frequency results in degraded light-load efficiency • Stringent requirement of detector linearity, limiter phase distortion, and delay mismatch

2.3 Efficiency Enhancement Techniques

2.3.1 Doherty Amplifier

Figure 2.12 shows the schematic of a Doherty amplifier configuration. The principle behind the Doherty Amplifier is to use one main PA and an auxiliary PA. At maximum output power, both PAs contribute to the output. When the input drive level decreases to typically half the maximum combined power, the auxiliary PA shuts down. Since the main amplifier is operated close to its gain compression region where it is efficient, the overall efficiency of the system is improved.

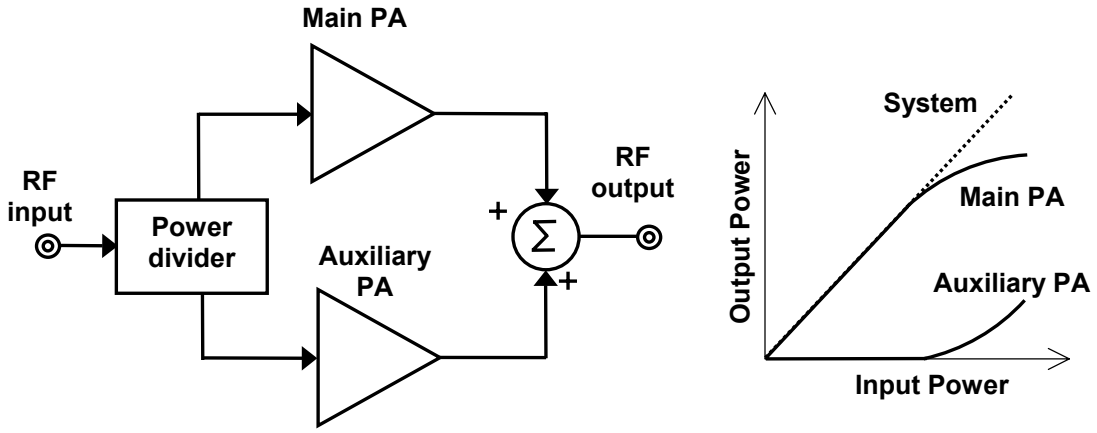


Figure 2.12. Basic Doherty amplifier configuration.

Recent works in the Doherty amplifier with extended power range [42], [43], have been demonstrated using microstrip power-division and combination networks. However, integrated circuit realization of the scheme requires the use of on-chip power division and combination schemes, which are inherently lossy because of the increased metal resistance at high frequencies (skin effect) and substrate coupling [44].

2.3.2 Efficiency Enhancement of Linear Power Amplifiers

Efficiency of linear power amplifiers is improved by dynamically varying the bias point, thereby reducing the quiescent power dissipation in a PA as output power decreases. Linear PAs with dynamic supplies have been investigated with bias control at

the input and output of the amplifier (gate/base and drain/collector in MOSFET's and BJT's, respectively [45]-[49]). A theoretical evaluation the efficiency enhancement resulting from dual-bias control is reported in [50] and experimental results for a similar architecture have been demonstrated in [51]. All of these schemes can be broadly classified in two categories: (a) envelope-follower PA, and (b) envelope-tracking PA.

(a) Envelope-Follower PAs:

The block diagram representation of an envelope follower PA is shown in Figure 2.13, where the supply voltage and/or current of the PA are changed dynamically by following the complete envelope. The supply voltage is adjusted dynamically by a boost converter [45], [47] only when the required supply voltage is greater than the battery voltage. To vary the bias current with constant supply, the gate voltage of the PA is changed according to the envelope signal [44], and a theoretical dual bias (both supply voltage and bias current) control scheme is proposed in [50]. By following the envelope completely, the peak-load efficiency of the system is improved. However, higher bandwidth requirement and subsequently higher switching frequency (same as in the EER scheme presented in Figure 2.11) result in lower converter efficiency at light loads. Like in the EER scheme, an RF delay line (equal to the delay of envelope signals while amplified through the converter, which is of the order of microseconds) is required; introducing resulting delay mismatch issues [52] makes this scheme unattractive for IC implementation.

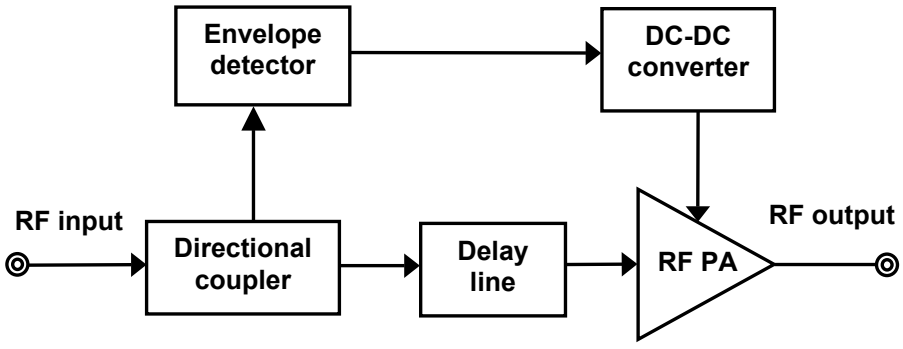


Figure 2.13. Generalized functional block diagram of the envelope-follower linear PA.

(b) Envelope–Tracking PA:

To mitigate the requirement of an RF delay line and overcome the problems of delay mismatch, instead of following the envelope completely, the supply voltage is adjusted dynamically using a buck converter according to the root-mean-square (rms) value of the envelope signal [48]. A generalized block diagram of such a scheme is shown in Figure 2.14. Since the converter does not follow the complete envelope, loop bandwidth and consequently switching frequency can be lower than what is required for the EER and the envelope follower technique, thereby achieving high efficiency over wide-loading conditions and consequently longer battery life. However, with the highly variable nature of the batteries used in portable applications, the buck-converter supplied systems [51] cannot be operated at their peak performance when the required supply is higher than the battery voltage.

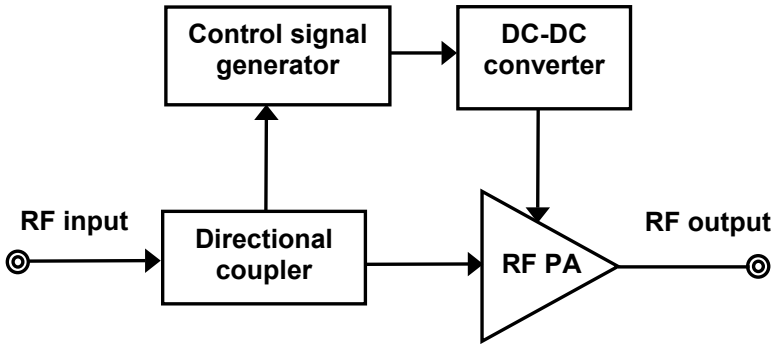


Figure 2.14. Generalized functional block diagram of envelope-tracking linear PA.

2.3.3. Comparative Evaluation of Efficiency Enhancement Techniques

A summary of state-of-the-art efficiency enhancement schemes highlighting their key advantages and disadvantages is presented in Table 2.4. The Doherty configuration is not suitable for an IC implementation with state-of-the-art on-chip power division and combination schemes, which are inherently lossy. While the envelope follower PA approach achieves high peak-power efficiency, the higher converter bandwidth requirement and consequently higher converter switching frequency results in a lower

efficiency during light loading conditions. On the other hand, envelope-tracking PA is realized with a lower converter bandwidth, which can be achieved by a power supply with a lower switching frequency and potentially higher efficiency over the transmitter's output power dynamic range. Therefore, envelope-tracking scheme is the most suitable technique to improve the average efficiency of the system by operating the PA and its associated efficiency-enhancement circuitry with high efficiency over wide loading range.

Table 2.4. Comparative evaluation of PA efficiency enhancement schemes.

Technique	Advantages	Disadvantages
Doherty PA	• High efficiency over loading range	• Lossy power combining and dividing networks • Complexity of multiple PAs
Envelope-follower PA	• Close to peak power efficiency	• Large converter BW and higher switching frequency results in degraded light-load efficiency • Detector linearity requirement and delay mismatch
Envelope-tracking PA	• Lower converter BW and lower switching frequency results in higher light-load efficiency	• Low peak power efficiency (but average efficiency is what matters for battery life!)

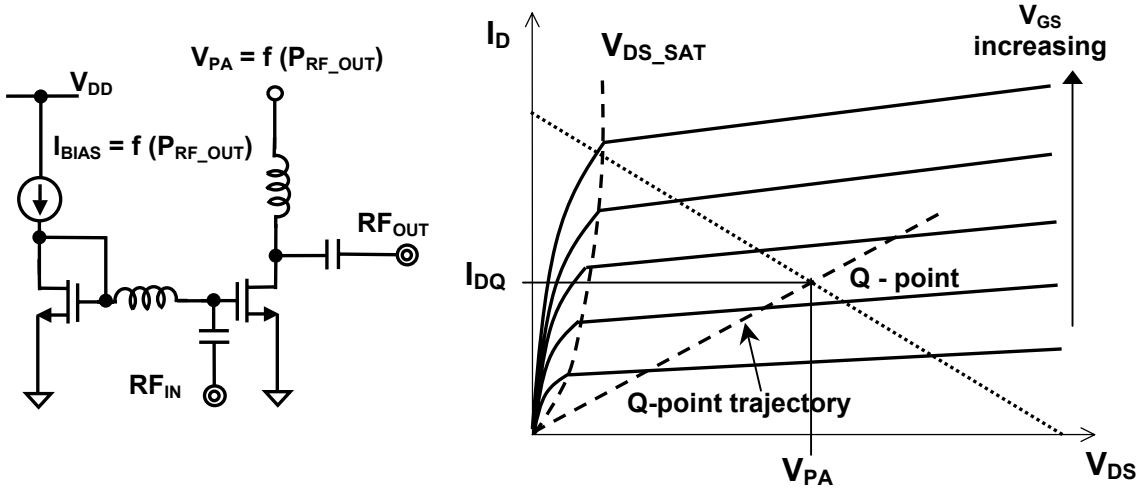
2.4 Proposed Power-Tracking, Dual-Bias Controlled Linear RF PA

PA linearization and efficiency enhancement schemes reviewed in the preceding section offer unique challenges and opportunities to realize energy-efficient linear RF PAs for high-performance, battery-powered handheld devices. PAs with dynamically adaptive supplies (e.g., EER, envelope-follower and envelope-tracking) present an avenue for improving battery life, from the system power management perspective, since the already existing power supply can be replaced with a smart, dynamically adaptive supply. At the same time, predistortion approaches can be used along with dynamic

supplies to further improve the efficiency performance of the PA. In this section, a new dynamically adaptive PA system is introduced, where both the supply voltage and the bias current are adjusted, depending on the power transmitted by the PA.

2.4.1 System Description

Figure 2.15 (a) illustrates the basic principle of operation of the proposed power-tracking PA system. For peak-power, its dc operating point is selected based on the maximum allowed supply voltage and the bias current required to achieve the specified linearity. As the PA output power decreases, its supply voltage and bias current are reduced such that the linearity is well within the specification. Figure 2.15 (b) shows the operating point of the PA for peak power and its trajectory of operating points with transmitted RF power. In essence, at a lower RF power level, the quiescent power is reduced, resulting in efficient transformation of battery power into useful transmitted signal power.



(a) (b)

Figure 2.15. (a) Simplified schematic of a MOS PA with dynamic supply voltage and bias current adjustment and (b) its operating point trajectory.

Figure 2.16 shows the schematic of the proposed energy-efficient linear RF PA system with dynamically adaptive supply voltage and bias-current control. The bias current of a transistor is adjusted by changing the potential at its gate/base, which is also used as the input port for the input RF signal. The power detector senses part of the RF input power to be amplified by the PA using a directional coupler. The power detector's output generates a control signal for the dc-dc converter and bias generator, which control the PA's supply voltage and bias current, respectively. As the input power for the PA increases, the power detector senses higher power, thereby generating a control signal, which ultimately increases the PA supply voltage and its gate/base bias voltage to yield a higher drain/collector bias current.

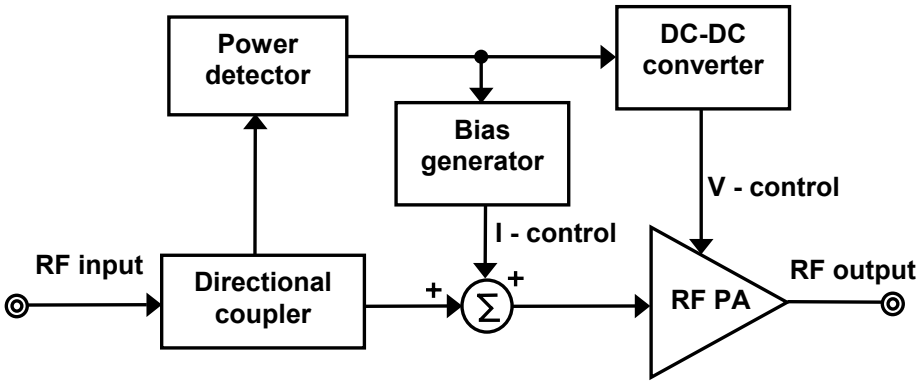


Figure 2.16. Functional block diagram of the proposed power-tracking, dual-bias controlled linear RF PA as a stand-alone solution.

The control signal for the dynamic supply and bias signal can also be generated from the base-band processor as digital data, which can be converted back to an analog signal using a digital-to-analog converter (DAC). While the generation of the control signal using the PA's input signal is suitable for a stand-alone PA, obtaining control signal from the base-band processor is attractive towards complete system implementation of the radio transceiver. Figure 2.17 shows a block diagram of the proposed scheme targeted for a transmitter environment. In the wireless systems with inherent power control mechanisms, e.g., CDMA and WCDMA, the base-band processor

monitors the transmitter's output power a dedicated power control loop. Moreover, the base-station sends information to the mobile station to increase or decrease its output power as required. Therefore, the baseband processor possesses all the necessary information to generate the required control signal, which is representative of the transmitted power.

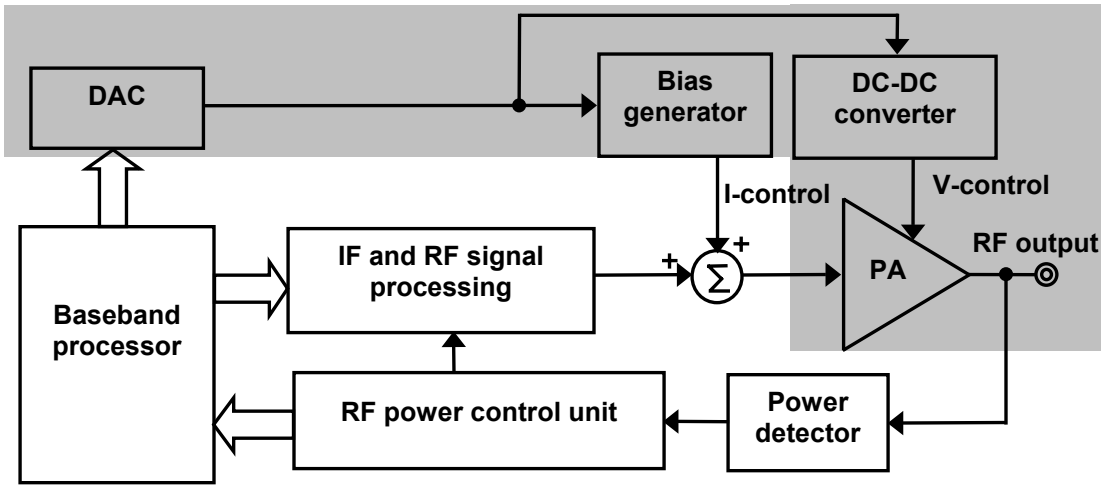


Figure 2.17. Functional block diagram of the proposed power-tracking, dual-bias controlled linear RF PA within the complete transmitter.

2.4.2 Efficiency Improvement Analysis

The transistor operating in class-A configuration exhibits higher linearity. In this section, efficiency improvement due to both supply voltage and bias current control over only supply voltage and only bias current control for a class-A amplifier is derived and compared. Subsequently efficiency enhancement for class-B and -AB amplifiers is discussed.

For a class-A amplifier with a nominal supply voltage V_{DD} and a peak output voltage V_{OUT} supplied to a load R_L, the quiescent current I_{DQ} is given by

$$I_{DQ} = \frac{V_{DD}}{R_L}. \tag{2.1}$$

The efficiency of a class-A amplifier is the ratio of output power ($V_{OUT}^2/2R_L$) to the power drained from the supply ($V_{DD}I_{DQ}$), and is given by

$$\eta_A = \frac{V_{OUT}^2}{2V_{DD}^2}. \tag{2.2}$$

(a) Varying the Supply Voltage: When the supply voltage of an amplifier is adjusted with its output power, at any time supply voltage (V_{SUPPLY}) is equal to the peak value of its output voltage V_{OUT}. Since the bias current remains constant, which is given by Equation (2.1), the quiescent power drawn from the supply is given by

$$P_{IN\_VS} = V_{SUPPLY} \times I_Q = \frac{V_{OUT}V_{DD}}{R_L}. \tag{2.3}$$

The efficiency of a class-A amplifier with only supply voltage adjustment is the ratio of output power ($V_{OUT}^2/2R_L$) to the power drained from the supply P_{IN_VS} and is given by

$$\eta_{A\_VS} = \frac{V_{OUT}}{2V_{DD}}. \tag{2.4}$$

Therefore, the efficiency of a PA with a dynamic supply varies linearly with output voltage in contrast to that of a conventional class-A amplifier where the efficiency varies with the square of the output voltage.

(b) Varying the Bias Current: For a bias current variation scheme, the optimum value of quiescent current is given by

$$I_{DQ\_OPT} = \frac{V_{OUT}}{R_L}. \tag{2.5}$$

The efficiency of a PA with bias current control is the ratio of output power ($V_{OUT}^2/2R_L$) to the power drained from the supply ($V_{DD}V_{OUT}/R_L$) and is given by

$$\eta_{A\_OB} = \frac{V_{OUT}}{2V_{DD}}. \tag{2.6}$$

Therefore, the efficiency characteristic varies linearly with output voltage, which contrasts to a conventional class-A amplifier, where the efficiency varies with the square of the output voltage.

(c) Variation of both bias current and supply voltage: When both the supply voltage and bias current of the PA are adjusted, termed as dual bias (DB) control in this text, the supply voltage V_{SUPPLY} is equal to its peak output voltage V_{OUT}, while bias current is equal to V_{OUT}/R_L. Therefore, the input power drawn by the PA from the supply is given by

$$P_{IN\_DB} = V_{SUPPLY} \times I_{DQ} = \frac{V_{OUT}^2}{R_L}. \tag{2.7}$$

The efficiency of a class-A power amplifier with both supply voltage and bias current control can be written as

$$\eta_{A\_DB} = \frac{V_{OUT}^2/2R_L}{V_{OUT}^2/R_L} = \frac{1}{2}. \tag{2.8}$$

The efficiency variation plots under only supply voltage control, only bias current control, and both supply voltage and bias current adjustments for a class-A amplifier are given in Figure 2.18. While the efficiency degrades linearly with output power for only supply voltage or bias current control, adjustment of both the supply voltage and bias

current enables the PA to operate at its theoretical maximum efficiency of 50 % in class-A configuration.

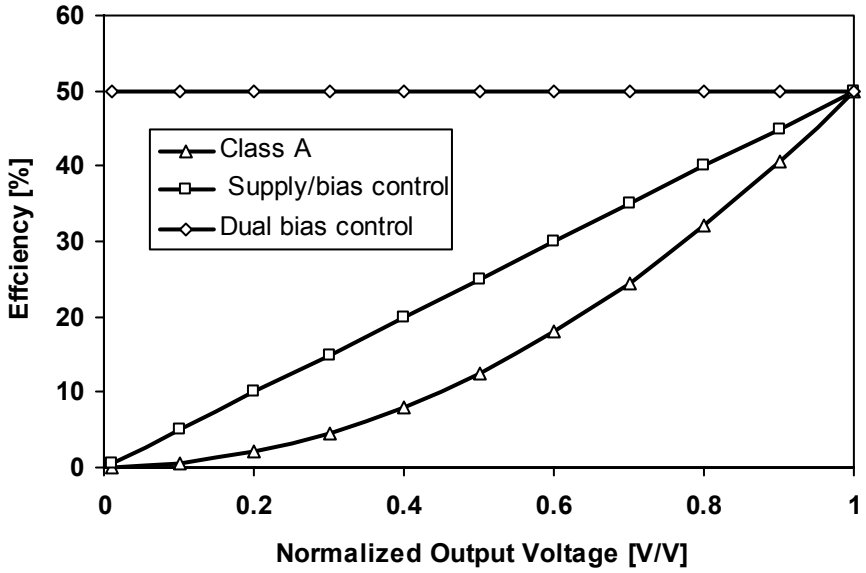


Figure 2.18. Efficiency enhancement plots of an RF PA under various bias control schemes on a class-A amplifier.

The bias current of a class-B amplifier is zero. In the presence of an input signal, the input supply power is the product of average current drawn from the supply and its terminal voltage, and is given by

$$P_{IN\_B} = V_{DD} \times \frac{2V_{OUT}}{\pi R_L}, \tag{2.9}$$

yielding a power efficiency

$$\eta_B = \frac{\pi V_{OUT}}{4V_{DD}}. \tag{2.10}$$

When the supply voltage of a class-B amplifier is adjusted with its output power, at any time supply voltage (V_{SUPPLY}) is equal to the peak value of its output voltage V_{OUT}. Therefore, the PA efficiency remains constant at 78.5 % as long as the supply voltage is adjusted to be equal to the peak output voltage V_{OUT}. An amplifier operating in class-AB configuration yields power efficiency in between the two limits set by class-A and -B operation.

2.4.3 Effects of Supply Voltage and Bias Current Adjustments on PA

The effects of supply voltage and bias current adjustment on the input matching and gain characteristics of the PA are analyzed from the transistor's small-signal model (without the high frequency parasitic elements, for simplicity), as shown in Figure 2.19. The model parameters, e.g., capacitances, transconductance, and output resistance, depend on both the supply voltage and bias current, and therefore affect the amplifier's matching and gain characteristics. The output matching of the last stage of a PA is designed to achieve maximum power transfer, where the bias conditions change even under normal conditions, and therefore is not analyzed.

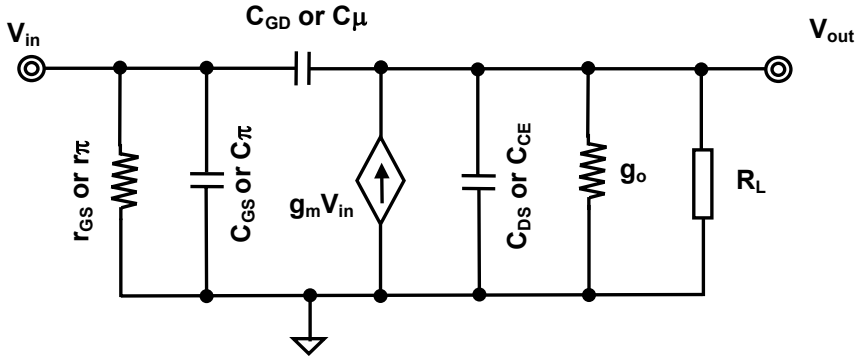
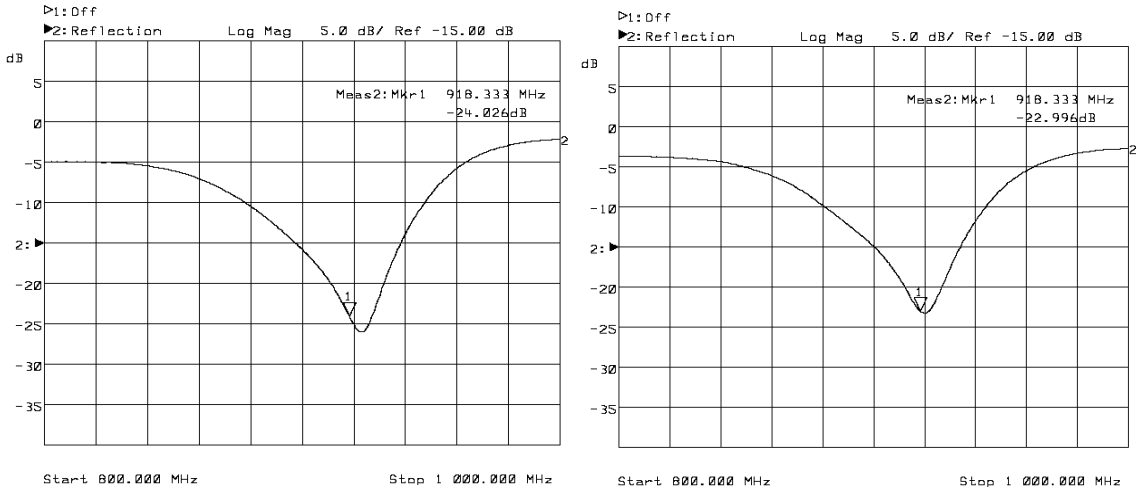


Figure 2.19. Simplified small-signal model of an MOS or bipolar transistor without parasitic elements.

The input matching network of a PA is designed using linear (s-parameters) methods, with S_{11} representing its input-matching characteristic. Figure 2.20 shows the

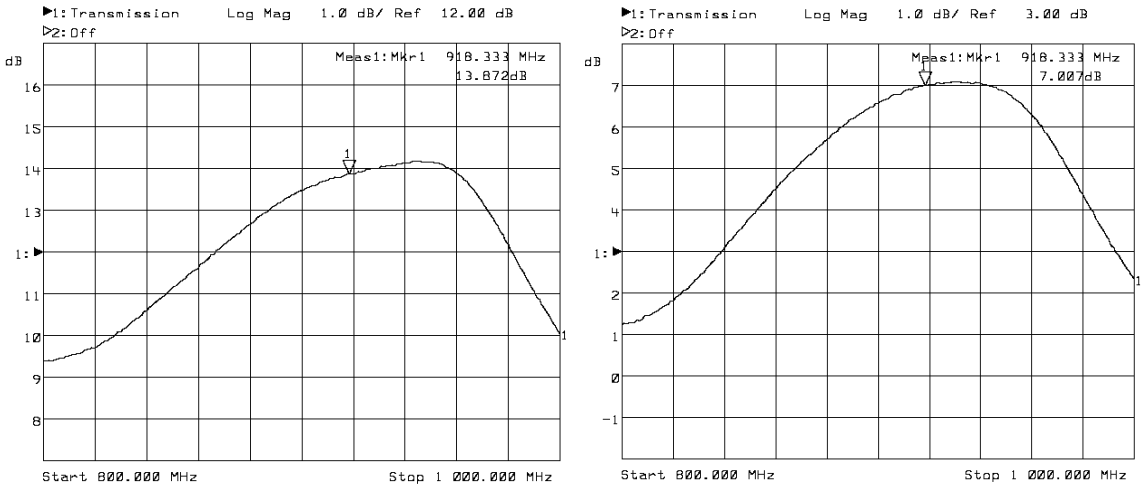
measured S_{11} parameters of a laterally-diffused-metal-oxide-semiconductor (LDMOS) N-channel PA having center frequency of 915 MHz with both bias current and supply voltage adjustments. The reflection coefficient (S_{11} parameter) degrades from –24 to –22 dB, it however remains below typical values (–10 to –15 dB) for the two extreme bias conditions of the PA in a dynamically adaptive system.



(a) (b)

Figure 2.20. Input matching characteristics of an LDMOS PA with bias current and supply voltage variation. The S_{11} parameter of the PA with (a) V_{DD} = 3.6 V, I_D = 300 mA, and (b) V_{DD} = 0.5 V, I_D = 40 mA.

The amplifier's gain is given by the product of its transconductance (g_m) and the resistance seen by the transistor at its output node. The transconductance varies linearly with the collector current for a bipolar transistor and as a square-root function of the drain current for a MOS device. Figure 2.21 shows the measured transmission coefficient (S_{21} parameter) of an LDMOS PA with bias current and supply voltage change under the two extremes of the operating conditions: (a) supply voltage of 3.6 V with bias current of 300 mA, and (b) supply voltage of 0.5 V with bias current of 40 mA. As expected, the amplifier's gain reduces from 14-dB to 7-dB between the two extreme operating conditions in a dynamically adaptive system.



(a) (b)

Figure 2.21. Power gain variation of a LDMOS RF PA with supply voltage and bias current adjustment. The S_{21} parameter of the PA with (a) V_{DD} = 3.6 V, I_D = 300 mA, and (b) V_{DD} = 0.5 V, I_D = 40 mA.

Since the PA's gain is a strong function of its bias current compared to supply voltage, accurate adjustment of bias current is required to achieve a desired gain such that the transmitter's target output power by can be achieved by settling the input power level. For a given bias current, a larger than required supply voltage results in unnecessary power loss, thereby degrading the efficiency, while a lower supply voltage results in clipping of the output signal, and consequently degrading the linearity of the PA.

2.4.4 Effect of Power Supply Ripple

Power supply ripple is inherent to switching regulators and it is therefore critical to evaluate its effects on the load (the PA, in this case). The effect of supply voltage variation on the transconductance of a MOS transistor (g_m) can be observed from the expression given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = k' \frac{W}{L}\left(V_{GS} - V_T\right)\left(1 + \lambda V_{DS}\right), \tag{2.11}$$

where k_n' is the transconductance parameter, W/L is the width/length ratio of the transistor, $(V_{GS} - V_T)$ is the gate overdrive voltage, λ is the channel-length parameter, and V_{DS} is the drain to source voltage. Consequently, the variation in supply voltage affects the amplifier's transconductance. In the following text, the effect transconductance variation due to a ripple on the PA power supply for a single-tone and spread-spectrum signal (e.g., CDMA) amplification is analyzed. Although the switching ripple of a dc-dc converter is composed of many harmonics, for simplicity, the ripple is approximated as a first-order harmonic.

(a) Single-tone signal: The PA supply voltage in the presence of a ripple (approximated as a first-order harmonic) is expressed as

$$V_{DD}(t) = V_{DD\_AVG} + V_R \cos(\omega_s t), \tag{2.12}$$

where V_{DD_AVG} is the average PA supply voltage, V_R is the output ripple amplitude, and $\omega_s (= 2\pi f_s)$ is the angular frequency in radians/sec, and f_s is converter's switching frequency. When an input sinusoidal signal given by the expression

$$v_{in}(t) = V_{IN} \cos(\omega_o t), \tag{2.13}$$

where V_{IN} is the amplitude of the signal, $\omega_o (= 2\pi f_o)$ is the angular frequency of the RF signal in radians/sec, and f_o is the RF signal frequency, is amplified by the PA its output waveform is expressed as

$$v_{out}(t) = g_m(t)\, R_{out}(t)\, v_{in}(t), \tag{2.14}$$

where $R_{out}(t)$ is the output resistance seen by the transistor at its drain as a function of time.

Replacing V_{DS} in the expression for g_m given by Equation 2.11, with Equation 2.12, the output signal can be expressed as

$$v_{out}(t) = k' \frac{W}{L}\left(V_{GS} - V_T\right) R_{out}(t) V_{IN} \cos\omega_o t \left\{\left(1 + \lambda V_{DD\_AVG}\right) + \lambda V_R \cos\omega_s t\right\}. \qquad (2.15)$$

The first and second terms of the expression given by Equation (2.15) represents the fundamental and harmonic content of the output signal, respectively. The multiplication effect of the input RF signal frequency (f_o) and power supply ripple frequency (f_s) results in harmonics at the sum ($f_o + f_s$) and difference ($f_o - f_s$) of the two frequencies. The ratio of the signal amplitude for the fundamental component to that of the harmonic content, known as *harmonic suppression* (HS), is given by

$$HS = \frac{V_{harmonic}}{V_{fundamental}} = \frac{\lambda V_R / 2}{1 + \lambda V_{DD\_AVG}}. \qquad (2.16)$$

The harmonics of the output signal, the location of which depends on the relative frequencies of the supply ripple and RF signal, create interference in the adjacent channels as well as inside the channel, thereby corrupting the useful information. Therefore, the harmonic content of the output signal must be suppressed below a certain level with respect to the fundamental component such the system's linearity specifications are satisfied. A smaller harmonic content in the output signal generated due the power supply ripple is desirable, which ultimately yields a lower value of harmonic suppression.

Figure 2.22 conceptually illustrates the effect of power supply ripple on the PA's output signal spectrum. For a single-tone signal with center frequency f_o, when processed by an amplifier with a power supply having a ripple frequency f_r, there are unwanted harmonics at the frequencies $f_o - f_s$ and $f_o + f_s$. Figure 2.23 shows the measured output spectrum of an RF PA with a power supply ripple frequency of 6 MHz amplifying a 915 MHz signal. As expected from the analysis, harmonics are observed around the center

frequency (f_o) at an offset equal to the ripple frequency (f_s) with an harmonic suppression of –42 dB.

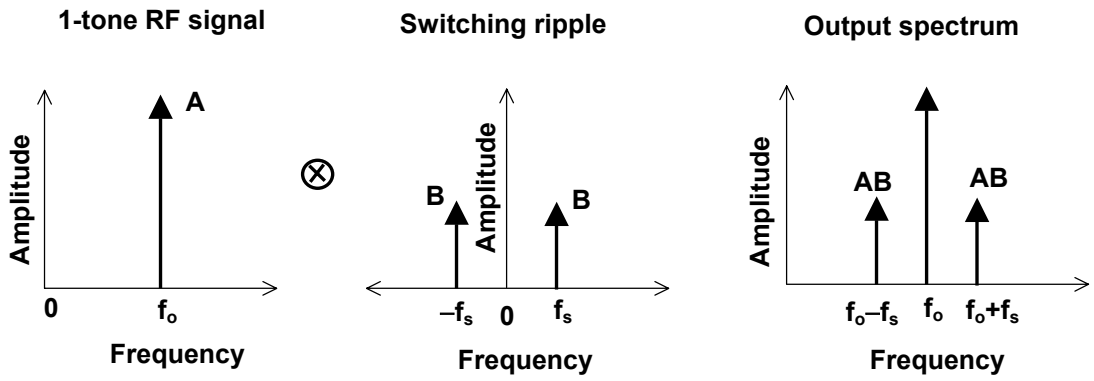


Figure 2.22. Effect of the power-supply ripple voltage on single-tone signal amplification.

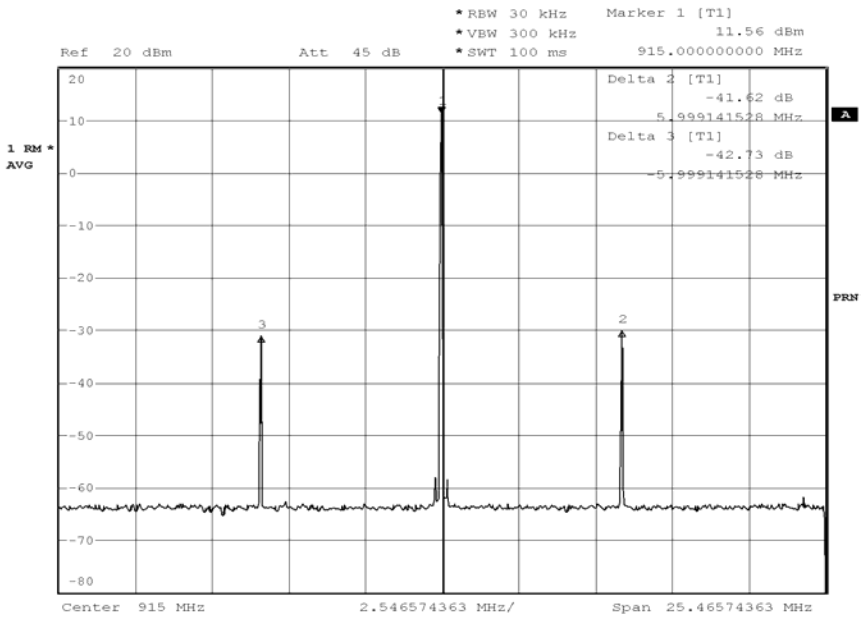


Figure 2.23. Measured single-tone signal amplification in the presence of a 6 MHz power supply ripple.

Figures 2.24 and 2.25 show the variation of the measured and estimated values of harmonic ripple suppression as a function of the average supply voltage and peak-to-peak ripple voltage, respectively. With a higher average voltage, the same peak-to-ripple creates harmonics of lower amplitude compared to the signal content of fundamental frequency. Alternatively, for a given average supply voltage a higher peak-to-peak ripple generates harmonics of larger amplitude.

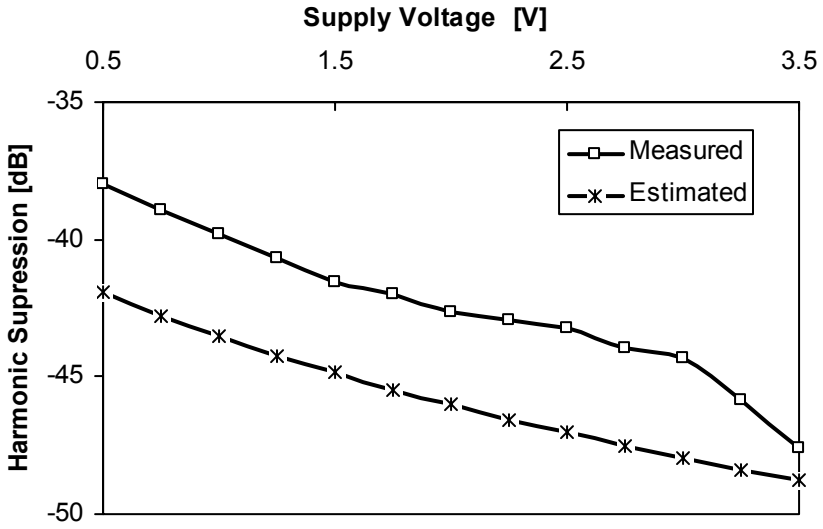


Figure 2.24. Comparison of the measured and first-order estimated harmonic suppression as a function of supply voltage.

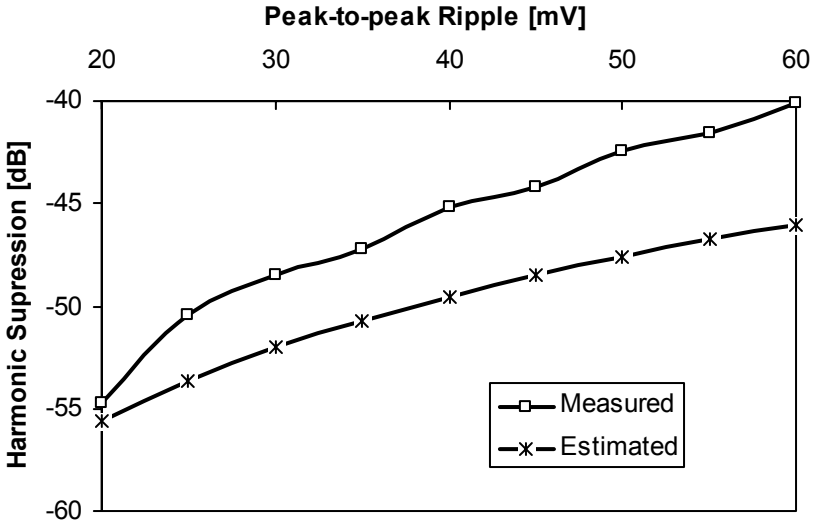
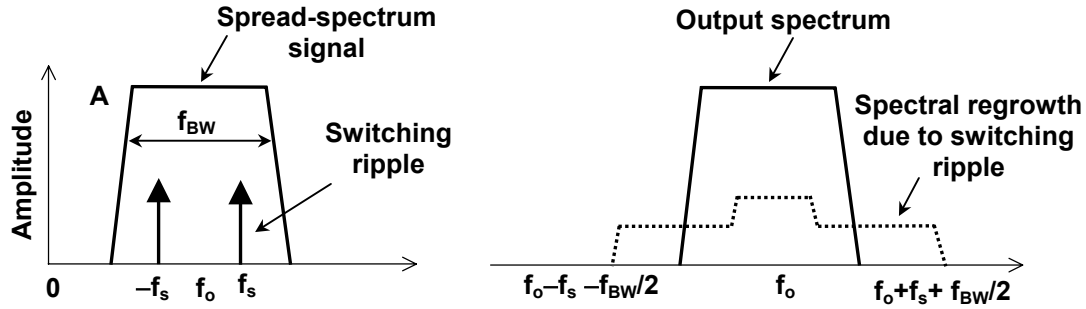


Figure 2.25. Comparison of the measured and first-order estimated harmonic suppression as a function of peak-to-peak ripple voltage in the supply.

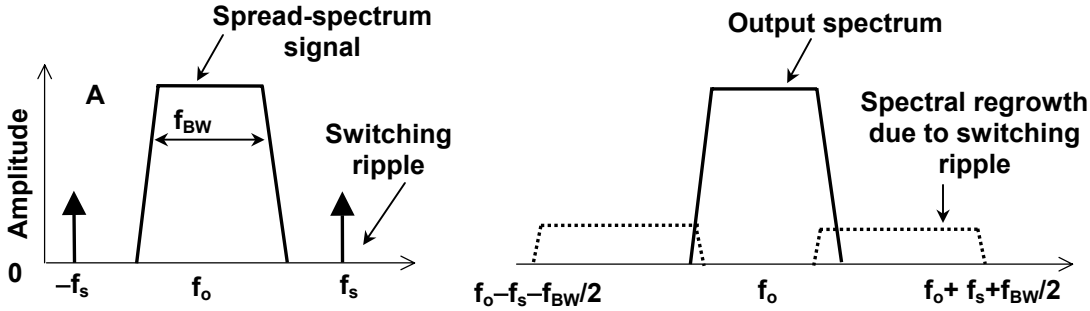
For the estimated harmonic suppression, a constant channel-length modulation parameter (λ), extracted from the measured DC characteristic of the LDMOS transistor is used in the calculation. In practice, an RF PA while transmitting output power operates in a large signal manner, which implies variable dc bias conditions. Since the parameter λ is dependant on dc bias conditions, where as it is assumed as constant in this case, for simplicity, and an approximate first-order model is used in the estimation, an error up to 6 dB (50 %) is observed between estimated and measured values. However, the trend of harmonic suppression closely matches with the estimated trend.

(b) Spread-spectrum signal: Unlike single-tone signal amplification, the effect of ripple voltage for spread-spectrum RF signal is distributed across a bandwidth. Mathematical analysis of the effect of ripple voltage on the PA output can be cumbersome and therefore a qualitative explanation is provided in this section. Figure 2.26 conceptually demonstrates the multiplication of RF signal with a switching supply ripple inside, and outside the RF channel, creating spectral regrowth (side-lobes) both inside and outside the channel. Since the switching-ripple spectrum is spread over a smaller band compared to the signal spectrum, the spectral regrowth bandwidth is same as the RF signal bandwidth.

Figure 2.26(a) shows the resultant output signal spectrum when the power supply ripple frequency lies within the baseband bandwidth of the RF signal. The side-lobes generated due to the multiplication of the RF signal and the ripple overlap with each other inside the channel space itself, consequently affecting the in-band linearity of the PA. As a result, the accuracy of transmitted signal degrades, which is typically measured by error vector magnitude (EVM) specification of the PA. On the other hand, when the switching ripple frequency falls outside the baseband bandwidth of the RF signal as shown in Figure 2.26(b) the side-lobes do not overlap with each other creating out-of-band spectral regrowth, which is reflected as a degraded adjacent channel power ratio (ACPR) of the PA. In both cases, spectral regrowth due to the switching ripple voltage along with the inherent nonlinearity of the PA contribute to the overall in-band and out-of-band nonlinearity.



(a) Case I: $f_s < f_{BW}/2$

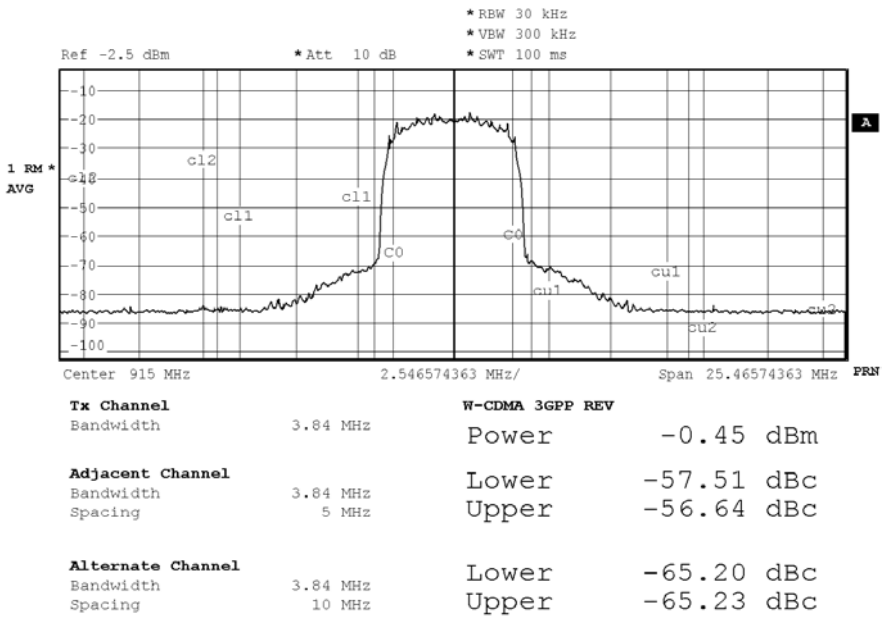


(b) Case II: $f_s > f_{BW}/2$

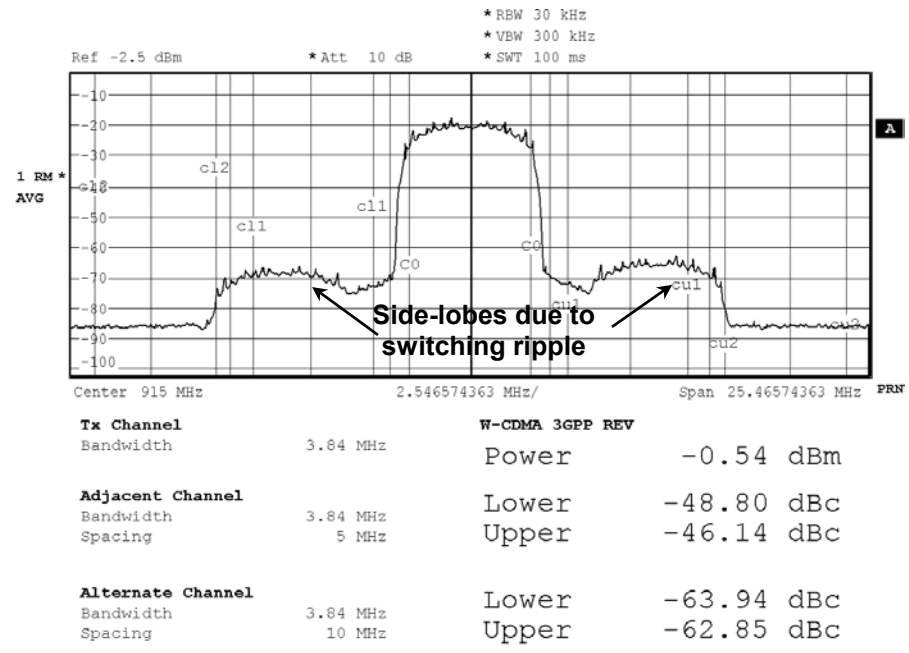
Figure 2.26. Power supply ripple effect on the spread-spectrum signal amplification by the RF PA with ripple frequency (a) within baseband bandwidth, and (b) outside baseband bandwidth.

Figure 2.27 shows the measured output spectrum of a 915 MHz RF PA with 3.84 MHz baseband bandwidth hybrid phase shift keying (HPSK) signal with and without a supply ripple of 6 MHz switching frequency. The power supply ripple, for measurement purpose, was adjusted to 42 dB below the fundamental signal level (Figure 2.23). As seen in Figure 2.27(b), the spectral regrowth is observed at an offset frequency of 6 MHz from the center frequency of 915 MHz with the harmonic power level remaining 42 dB below the channel power level. The spectral regrowth due to the switching ripple yielded a 10 dB degradation of adjacent channel leakage ratio of the PA. For a given application, the PA and its dynamic supply voltage ripple must be designed such that the overall spectral

regrowth due to the inherent nonlinearity of the PA and supply voltage ripple remains below the requirements specified by the standard.



(a)



(b)

Figure 2.27. Measured output spectrum of a PA with a 915 MHz center frequency and 3.84 MHz HPSK signal (a) without power supply ripple, (b) with power supply ripple of 6 MHz.

2.4.5 Effect of Power Supply Transient Response

Any dynamically adaptive power supply requires a finite time to adjust its output voltage from one level to the other with a change in its control signal. Transient response of the power supply is determined by its slew-rate limitations for large signal step, while bandwidth of its feedback control loop determines the response time for a small control step change. During the transition, if the converter's output voltage is not sufficient for the PA's signal swing (insufficient head-room), the RF transmitted signal is clipped, resulting in distortion and out-of-band spectrum regrowth. Overall, the PA performance is degraded, which in turn affects the fidelity of the RF transmitter.

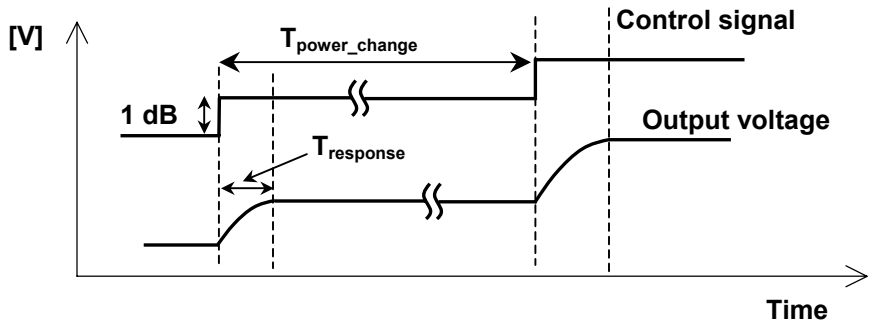


Figure 2.28. Illustration of the power supply's transient response during a PA's supply voltage adjustment.

Since the gain and linearity (ACPR/ACLR for CDMA/WCDMA and EVM) specifications of a PA are measured for a given power level, its performance during a transient power-level change requires monitoring other performance parameters. In a radio transmitter, the PA's performance degradation during a transient step is reflected to a system level specification, in terms of the accuracy of the transmitted data for a given time period, e.g., bit error rate (BER). The test setup requires a mobile transmitter and a base station with implementation of closed-loop power control mechanism. When the base station requests a change in power level, the mobile station responds accordingly while sending a control signal to dynamically adjust the PA's supply voltage and bias current. For a given time interval, the degradation of measured BER for a transmitter with

and without dynamic supply adjustments can be used to gauge the transient performance and effects on the PA, and consequently on the RF transmitter.

2.5 Summary

This chapter introduced various classes of PA circuit topologies highlighting the linearity efficiency trade-offs in their operations. State-of-the-art PA linearization schemes and efficiency enhancement techniques have been reviewed considering their applicability to realize a cost-effective solution for battery-powered, portable hand-held devices. Based on the discussions presented earlier, following the complete envelope and changing the supply voltage and current requires a high bandwidth dc-dc converter, which is achieved by a higher switching frequency, and thereby exhibiting poor light-load efficiency. Instead, controlling the supply voltage and current based on the change in power level in the system, termed as *power-tracking*, requires lower converter bandwidth, which can be achieved by selecting lower switching frequencies and thus maintaining high efficiency over a wide-loading range.

A novel, power-tracking, dual-bias controlled PA scheme is proposed and its characteristics are presented. Changing the supply voltage and bias current simultaneously, essentially combines the efficiency improvements in supply voltage or bias current adjustment schemes. As expected, the variation in bias current results in a variable gain PA, which requires automatic gain compensation circuitry to implement the transmitter's output power dynamic range. The ripple voltage inherently associated with any switching power supply results in a linearity degradation of the PA, and therefore should be carefully designed to keep the overall nonlinearity within the specified limits. This chapter essentially forms the background for design and implementation of an efficient PA targeted for CDMA and WCDMA modulation scheme. In the next chapter, analysis and design considerations of an adaptive buck-boost converter suitable for dynamic supply of an RF PA is presented.

CHAPTER III

DYNAMICALLY ADAPTIVE BUCK-BOOST SUPPLY

The supply voltage required for the proposed power-tracking, efficient, linear PA can be higher or lower than the battery voltage depending on the application-related parameters, e.g., the transmitter's output power level, PA technology, and the battery type used, thereby requiring a buck-boost converter. In other applications, e.g., the 3.3 V I/O can be provided by a highly efficient buck-boost converter, which allows the Li-ion battery to be drained to its lowest level [53] thereby utilizing its entire voltage profile (4.2 – 2.7 V). Furthermore, in USB applications [54], a constant 5 V supply is often required, while the input voltage varies from 4.5 to 5.25 V, which requires a buck-boost supply. Apart from PA-driven platforms, application-specific components in a system-on-chip (SOC) may require different supply voltages as operating conditions and workload [55]-[58] vary in an effort to minimize the energy drained from the battery. Since the battery voltage varies significantly, to operate these devices at peak performance levels, irrespective of the battery condition, the supply voltage needs to be transformed into a higher or lower voltage level dynamically, *on-the-fly*.

Several circuit topologies can be used to accomplish the buck-boost power conversion. In portable applications, lower cost and smaller size are key design requirements, which necessitate minimal use of external components. In switching regulators, the passive energy-storage elements, i.e., filter inductor, and input and output capacitors are off-chip, which increase the printed circuit board (PCB) real estate and thereby overall system cost. In this chapter, circuit topologies for buck-boost voltage conversion are reviewed and their suitability for low voltage, portable environments is

evaluated. The noninverting, synchronous buck-boost converter is chosen, considering its suitability for IC implementation since it uses minimum number external inductors and capacitors compared to other topologies. In addition, this chapter presents analysis and small-signal modeling of the basic buck-boost converter followed by system design considerations and power loss analysis.

3.1 Regulator Topologies

The circuit topologies with buck-boost conversion capabilities, suitable for adaptive power supply of a PA, considered and evaluated in this section are: (a) Flyback converter, (b) Boost/Linear regulator combination, (c) Single-ended-primary-inductance converter (SEPIC), (d) Inverting, buck-boost converter, (e) Cuk converter, and (f) Noninverting, buck-boost converter.

3.1.1 Flyback Converters

Figure 3.1 shows the power stage schematic of a Flyback converter [27]. During the on time of switch M_1, energy is stored in the transformer and the output capacitor sources the load current. During the off time of the switch, the stored inductor energy is delivered to the output capacitor and the load through diode D_1. The circuit is used in both continuous- and discontinuous-conduction mode, and the output voltage is regulated by either voltage- or current-mode control.

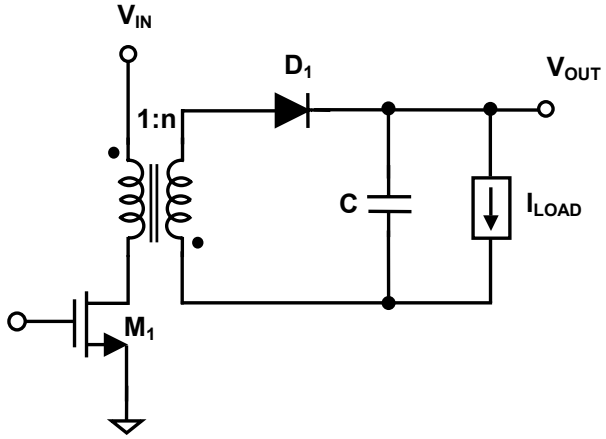


Figure 3.1. Schematic of a Flyback converter.

The only disadvantage of this topology is the use of an external transformer, which not only adds extra PCB space but also increases overall cost. With state-of-the-art IC fabrication processes, realization of transformers with large current capabilities and acceptable quality factor remains a distant dream. The fundamental limitation imposed by the series resistance of on-chip inductors, which is due to the physical constraints of the metal layers like size and conductivity, leads to unacceptable power losses, i.e., lower efficiency.

3.1.2 Boost/Linear Regulator Combination

Figure 3.2 illustrates the schematic of a boost converter cascaded by a linear regulator [59] to achieve buck-boost conversion. By controlling the boost converter and the linear regulator simultaneously, or independent of each other, the desired output voltage is obtained. Overall, system efficiency can be improved by allowing the linear regulator to track the boost converter output voltage, at least in the region of operation when the converter is required to step-up the voltage. However, in the low output voltage region, the linear regulator has to step-down the voltage from the boost converter's output. The limitations of such a scheme lies with the poor efficiency of a linear regulator when the difference between its input and output voltage is large.

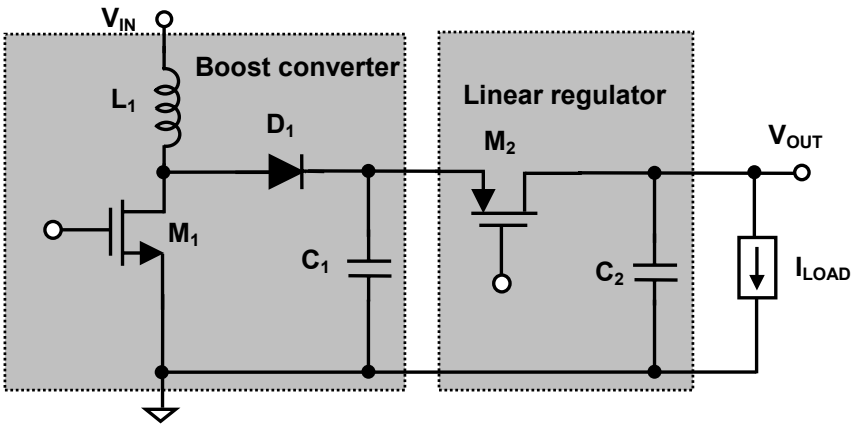


Figure 3.2. Schematic of a boost converter with a series linear regulator for realizing buck-boost conversion.

3.1.3 Inverting Buck-Boost Converter

The power stage schematic of an inverting buck-boost converter [27] is shown in Figure 3.3. The inverting buck-boost converter topology is the simplest, in terms of circuit complexity. However, as the name suggests, the polarity of the output voltage is opposite to the input supply voltage. An output voltage with the same polarity as the supply can be generated by interchanging the battery terminals, which prevents the same battery to power up other circuits in the system thus not facilitating single-cell operation. Therefore, an inverter is required for polarity inversion either at the input or at the output of the converter. Using an inverter at the output is better because of the lower current-carrying requirements of the output, especially during boost-mode operation.

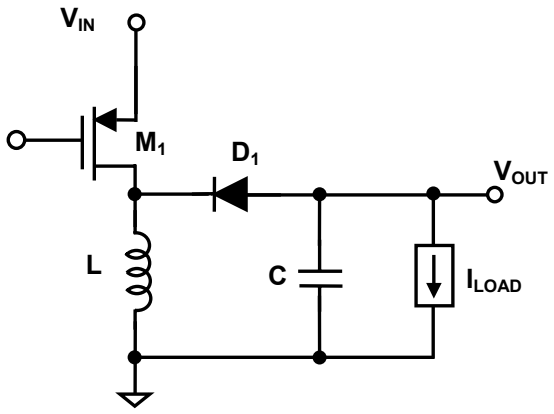


Figure 3.3. Schematic of an inverting buck-boost converter.

Figure 3.4 presents a charge-pump implementation of an inverter circuit topology. The energy transfer capability of the charge pump is limited by the capacitor values used, which are normally external off-chip components. The overall system complexity is evidently higher increased with the addition of the charge-pump inversion circuitry. Furthermore, since efficiency of the charge pump is lower than switching regulator which overall system efficiency is degraded.

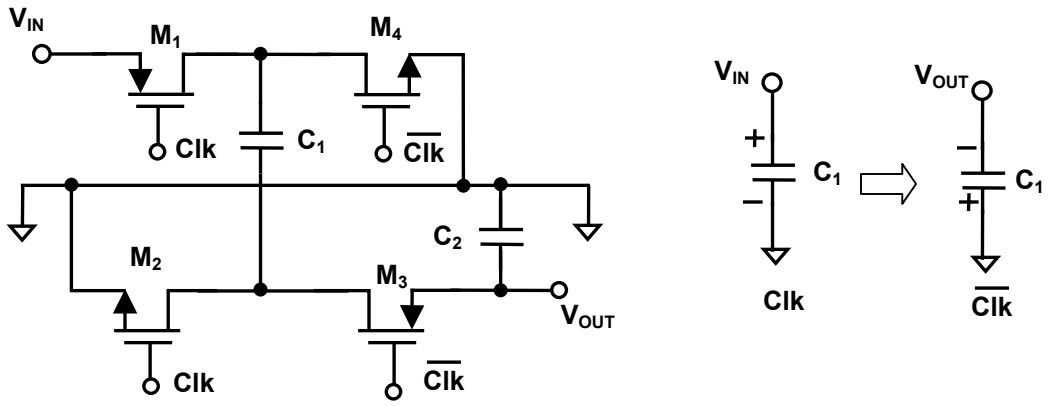


Figure 3.4. Schematic of a charge-pump inverter.

3.1.4 Cuk Converter

Figure 3.5 shows the schematic of a Cuk converter [27]. Similar to the inverting buck-boost converter, it also suffers from the output voltage polarity inversion problem, which requires an additional inverter circuit for system solutions. Unlike other converters Cuk converter uses current capacitive energy transfer from the input to the output. When transistor M_1 is open, capacitor C_1 is charged through diode D_1. When transistor M_1 is switched on, the diode is reverse biased, and capacitor C_1 is now connected to the output via inductor L_2 and capacitor C_2, which act as a filter.

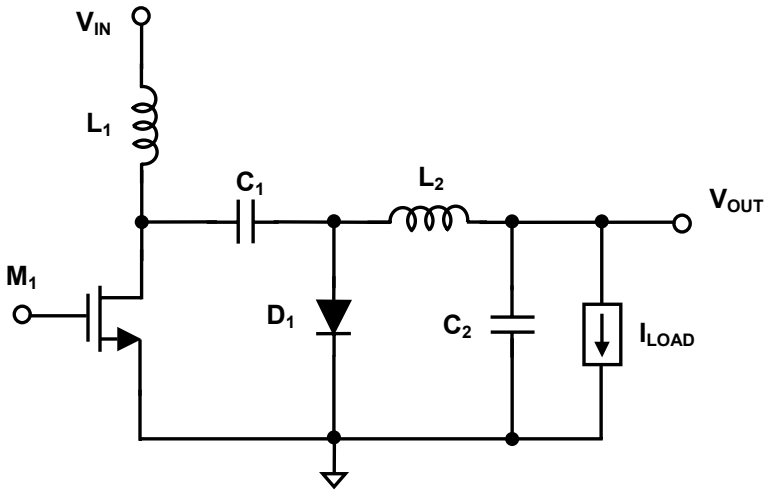


Figure 3.5. Schematic of Cuk converter.

The advantage of Cuk converter, though, lies in the fact that the currents drawn from both the input decoupling capacitor and output capacitor are not sharp square waves, which results in lower noise and EMI. However, it uses two inductors and two capacitors, which are external and therefore not recommended for a low cost portable environment.

3.1.5 Single-Ended-Primary-Inductance Converter

The Single-Ended-Primary-Inductance Converter (SEPIC) topology [27], as shown in Figure 3.6, is essentially an extension of a boost converter. In a boost converter (without capacitor C_1 and inductor L_2), input voltage V_{IN} has to be lower than the output voltage V_{OUT}; otherwise, diode D_1 is forward biased, providing a direct current-flowing path from input to output. By inserting a capacitor between input and output, the dc component is blocked. Inductor L_2 provides a known potential to the positive terminal of diode D_1. From a portable application's perspective, the SEPIC topology is not only bulky because of the additional inductor capacitor pair, but also more costly due to the external components requiring more PCB real estate, not to mention their additional cost.

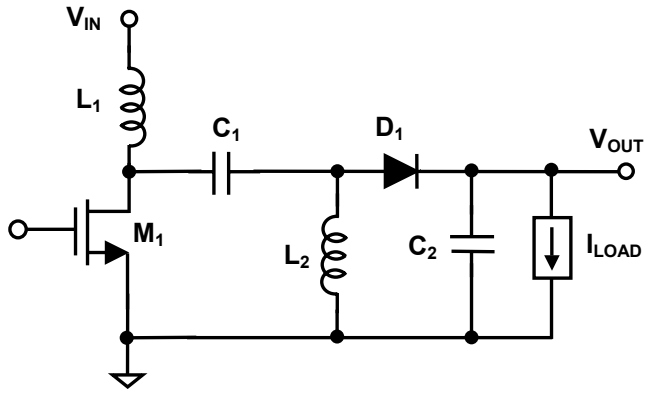


Figure 3.6. Schematic of a single-ended-primary-inductance converter.

3.1.6 Noninverting Buck-Boost Converter

A noninverting buck-boost converter is essentially a cascade combination of a buck converter followed by a boost converter, where a single inductor-capacitor is used for both [27], [60], as shown in Figure 3.7. Its ability to work over a wide range of input voltage to generate both higher and lower voltages with one inductor/capacitor pair makes this topology an attractive choice [60]. Since the input and output capacitor currents in the noninverting buck-boost converter topology are square waves in nature, they create more ripple and electromagnetic interference (EMI). However, by using low equivalent series resistance (ESR) and equivalent series inductance (ESL) ceramic capacitors, switching ripple can be minimized in order to meet the system requirements.

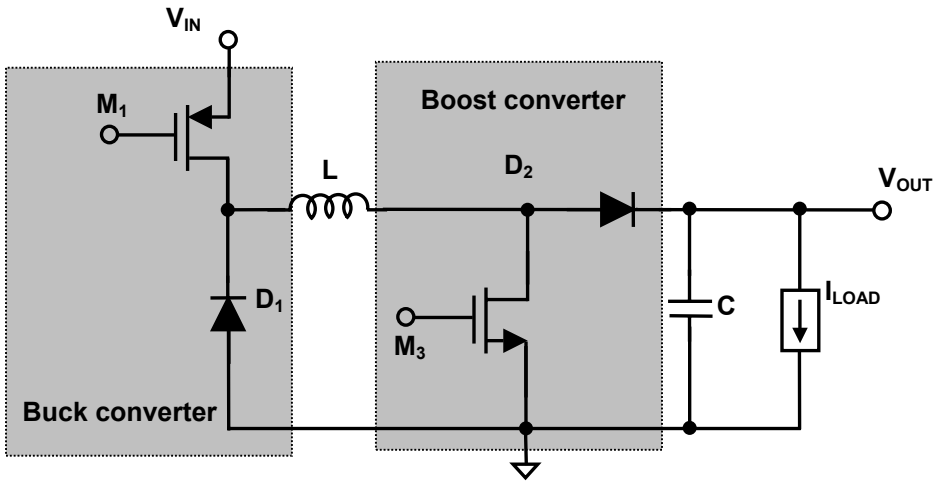


Figure 3.7. Schematic of a noninverting buck-boost converter.

A comparative evaluation of the various circuit topologies considered in this section is offered in Table 3.1 The trend in portable applications is to use the topologies that require low external component count and cost-effective system-on-chip (SOC) designs. Because SEPIC uses two inductors and two capacitors to transform energy from the battery to the load, the single-inductor, non-inverting buck-boost converter, irrespective of its complexity, is the most suitable topology for a portable, cost-effective, low-power environment. While the reported design in [61] is claimed to be the power

industry's first buck-boost dc-dc converter [62], it's ability to respond to dynamically adaptive reference control signal has not been reported. Furthermore, the minimum output voltage of the converter is 2.5 V, which is not suitable for applications requiring lower supply voltages.

Table 3.1. Comparative evaluation of regulator topologies suitable for noninverting buck-boost conversion.

Topology	Complexity	Efficiency	External components
Flyback converter	Low	Low	Transformer and single capacitor
Inverter plus inverting buck-boost converter	High	Medium	Single inductor, two capacitors
Inverter plus Cuk converter	High	Medium	Two inductors, two capacitors
Boost converter plus linear regulator	High	Low	Single inductor, two capacitors
SEPIC Converter	Low	High	Two inductors and two capacitors
Noninverting buck-boost converter	High	Medium	Single inductor, single capacitor

3.2 Noninverting, Synchronous Buck-Boost Converter

3.2.1. Circuit Topology and Operation

For low voltage and low power implementations, the efficiency of a buck-boost converter is improved by replacing the rectifier diodes with switches because of a smaller voltage drop across switches compared to the diodes, which results in a synchronous converter topology. The schematic of a synchronous buck-boost converter power stage is shown in Figure 3.8. The notations used for the schematic are as follows: V_{IN} is the input supply voltage, V_{OUT} is the steady state output voltage, I_{LOAD} is the output load current, L is the inductor value, C is the capacitor value, and R_{C_ESR} is the equivalent-series resistance (ESR) of the capacitor.

During the period T_{ON} of the cycle, switches MP_1 and MN_1 are on and the input voltage is impressed across the inductor. Since the load current is instantaneously

provided by the output shunt capacitor during this interval, the capacitor voltage (output voltage) decreases. During the other interval of the switching period (T_{OFF}), switches MN_2 and MP_2 are turned on and the inductor energy is transferred to the output, providing both the load current and charging the output capacitor. There is a time delay (known as *dead-time*) between turning off MP_1 MN_1 and turning on MN_2 MP_2 to prevent shoot-through current and avoid unnecessary power loss associated with it. During this period, the inductor current flows through body diodes D_2 and D_4, from transistors MN_2 and MP_2, respectively. The duty cycle (D) of the converter is given by

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T}, \tag{3.1}$$

where T is the switching time period of the converter. By adjusting either the switch-on or -off periods or both, the desired output voltage is obtained from the converter. The relation between input voltage, output voltage, and duty cycle is derived in the following subsection.

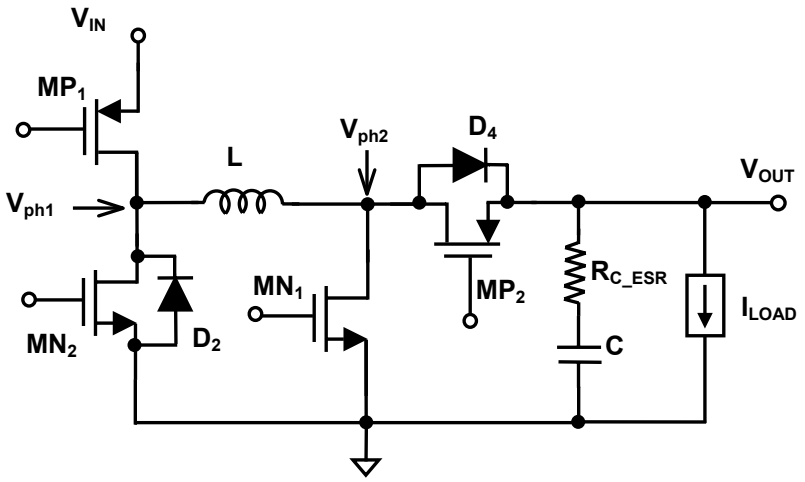


Figure 3.8. Schematic of a noninverting, synchronous buck-boost converter.

Figure 3.9 shows the key voltage and current waveforms of the converter operating with inductor current flow all the time, which is knows as *continuous-conduction mode*. The node voltage V_{ph1} is switched between V_{IN} and ground when MP_1 and MN_1 are on, while node voltage V_{ph2} is switched between V_{OUT} and ground when MP_2 and MN_2 are on. During the dead-time, node voltage V_{ph1} reaches below ground by a diode voltage drop. Similarly, V_{ph2} node voltage goes higher than V_{OUT} by a diode voltage drop during the dead time.

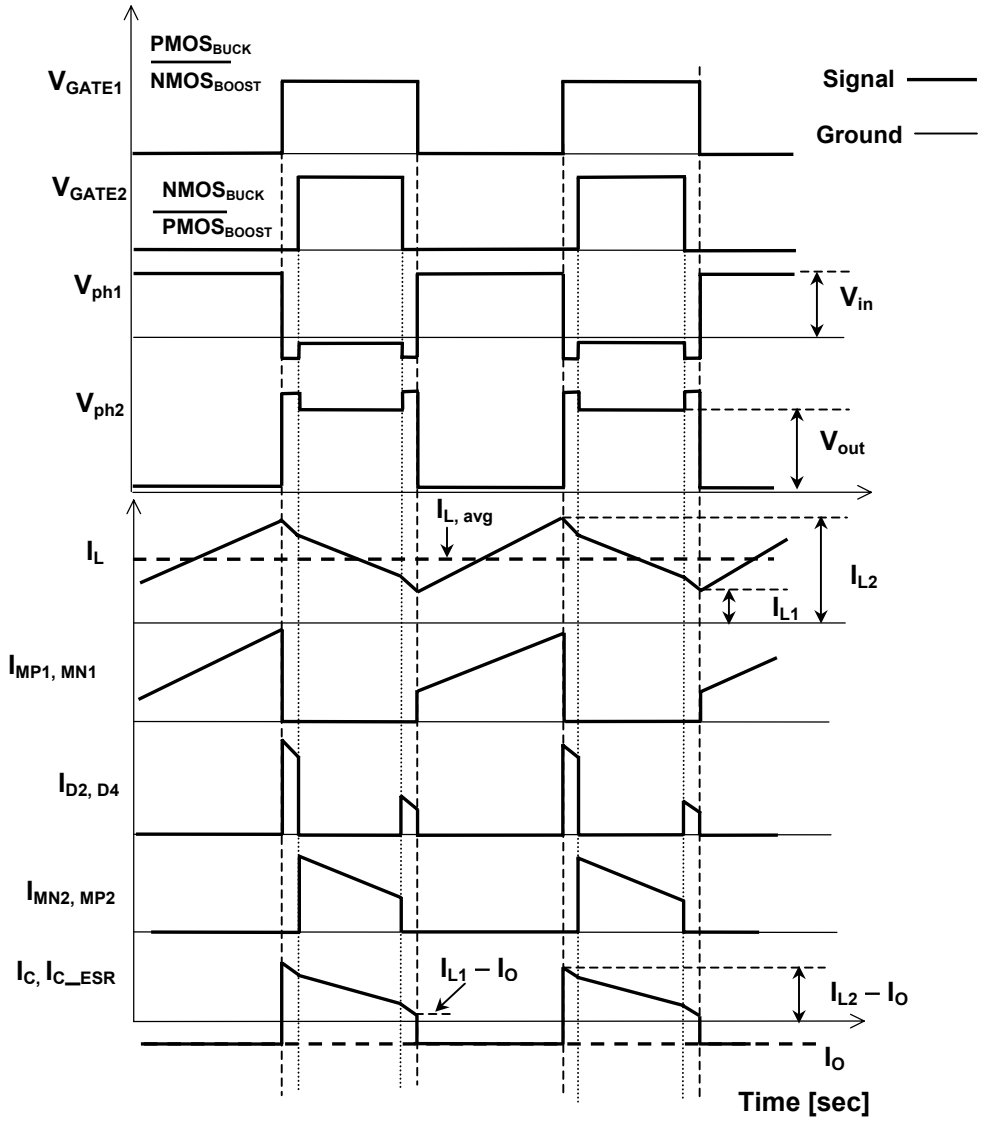


Figure 3.9. Key waveforms of the non-inverting, synchronous buck-boost dc-dc converter.

The current flowing through transistors MP_1 and MN_1 is same as the inductor current during on period, while MP_2 and MN_2 carry a current equal to the inductor current during off period. The body diodes conduct during the dead-times, which is shown as narrow pulses in Figure 3.9. The output capacitor provides load current during converter's on period, which is represented by a negative current. During the off period, the difference of inductor and load currents flows into the output capacitor.

3.2.2 Steady-State Analysis

Since node V_{ph1} is connected to V_{IN} for DT time over a period of T, the average voltage is given by

$$V_{ph1,avg} = DV_{IN}. \tag{3.2}$$

Similarly, the average node voltage of V_{ph2} can be given by

$$V_{ph2,avg} = D' V_{OUT}, \tag{3.3}$$

where D' is the complementary of duty cycle, and is equal to 1–D. Under steady-state operating condition (dc), the inductor can be treated as a short circuit, and the average voltage of V_{ph1} and V_{ph2} are therefore equal, which is expressed as

$$DV_{IN} = D'V_{OUT}, \tag{3.4}$$

yielding the ratio of output-to-input voltage given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D}. \tag{3.5}$$

For a duty cycle of 0.5, the output voltage is equal to the input voltage. When the duty cycle is less than 0.5, the output voltage is lower than the input (*buck mode*) and for duty

cycles greater than 0.5, the output voltage is higher than the input (*boost mode*). Figure 3.10 shows a graphical representation of the output-to-input voltage ratio of the buck-boost converter highlighting buck- and boost mode-operation region as a function of duty cycle.

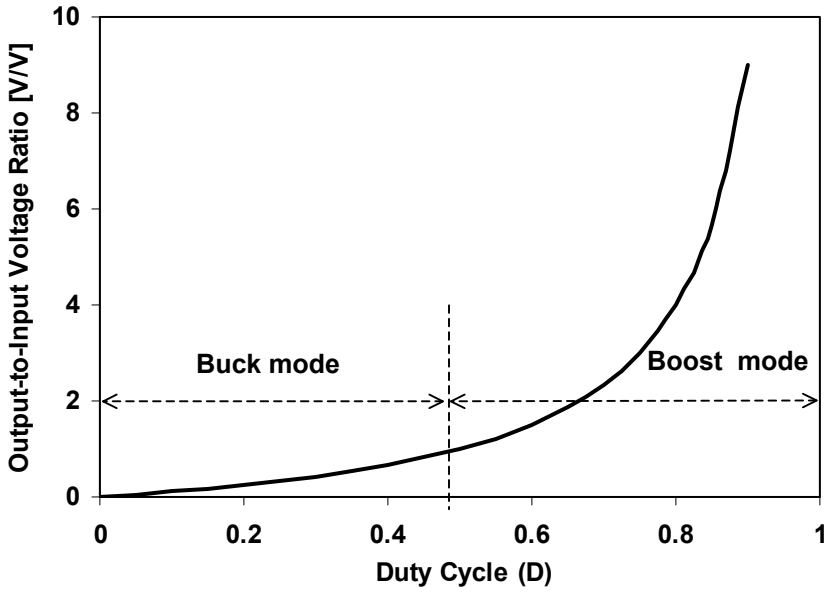


Figure 3.10. Output-to-input voltage ratio of a noninverting buck-boost converter as a function of its duty cycle.

Alternatively, the output-to-input voltage ratio can also be derived using inductor volt-second balance during the on- and off-times of the switches. During T_{ON} period, input voltage V_{IN} is impressed across the inductor, causing a ramp current flowing into it, the peak value of which (I_P) given by

$$I_P = \frac{V_{IN} T_{ON}}{L}. \tag{3.6}$$

Similarly, during T_{OFF} period, output voltage V_{OUT} is impressed across the inductor, which causes a negative but equal peak-to-peak ramp current to flow through the inductor given by

$$I_P = \frac{V_{OUT} T_{OFF}}{L}. \tag{3.7}$$

The output-to-input transfer function given by Equation 3.2 can also be obtained from Equations 3.1, 3.6, and 3.7.

3.2.3 Implications of a Dynamic Output Voltage

For low output voltages below the threshold voltage of the PMOS (MP_2 in Figure 3.8), the transistor never conducts current, leaving only the body diode (D_4) as the switch, which results in asynchronous operation of the converter. Because of larger voltage drop across the body diode compared to switch, the converter's power efficiency decreases. A transmission gate, as shown in Figure 3.11, is a parallel combination of a PMOS and an NMOS transistor with complimentary logic inputs to their gates. It is used in place of the PMOS boost transistor (MP_2), which ensures synchronous operation. For output voltages below the threshold voltage of a PMOS, the NMOS switch conducts current and, for higher output voltages, the NMOS transistor turns-off while PMOS device is the working switch. For intermediate output voltages, both PMOS and NMOS devices in the transmission gate conduct current during the switching interval in which the inductor is connected to the output node.

Figure 3.12 presents a plot that illustrates the operating regions of the transmission gate transistors. There exists a region, especially when supply voltage is low enough for the NMOS device to switch on and the output voltage is not sufficient enough to switch on the PMOS transistor, where the output current flows through body diode (D_4). The time period for which the converter operates in this mode is dependent on the input and output voltage ranges of a given application. The transmission-gate approach offers an cost effective solution the buck-boost converter where external

schottkey diodes are used to achieve low output voltage operation, since the additional power switch can be implemented on chip.

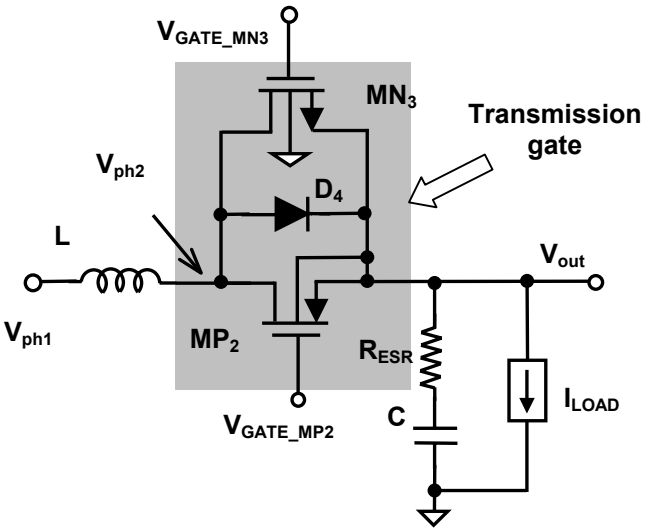


Figure 3.11. Schematic of the transmission gate output stage of the buck-boost converter for dynamic output voltage considerations.

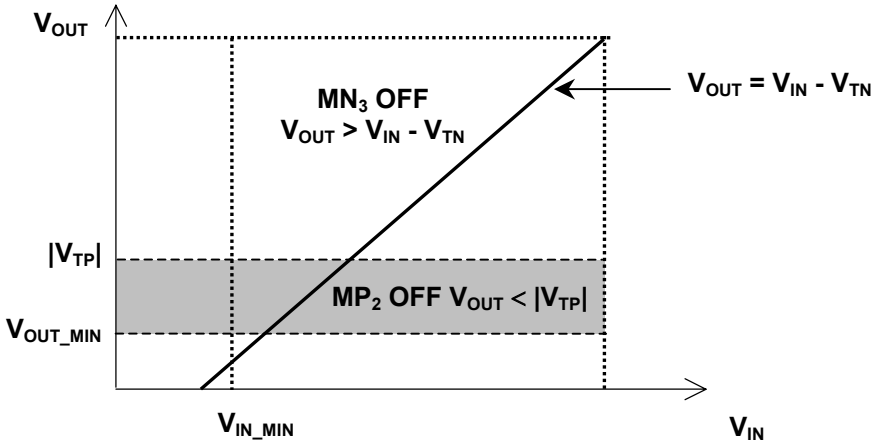


Figure 3.12. Illustration of the effects of low supply voltages on the operation of the buck-boost converter with a transmission-gate output stage.

3.3 Small-Signal Modeling and Analysis

Feedback control system is employed in dc-dc converters to regulate the output voltage regardless of the changes in input voltage and loading conditions. To design their feedback control loops, an equivalent small-signal model of the power stage is required that is valid for small-signal perturbation of the duty cycle at a lower frequency compared to the converter's switching frequency. To model the nonlinear power stage of these converters, techniques such as state-space averaging and circuit averaging [27], [63]- [66] have been used extensively. However, the derivation is mathematically complex and difficult to relate to the circuit's intuitive operation, which is important to the design and implementation of integrated circuits. In this section, a time-averaged model for a synchronous buck-boost converter power stage is introduced with precise one-to-one mapping with the physical operation of the circuit.

3.3.1 Small-Signal Model with Respect to Duty Cycle

When the duty cycle changes (e.g., from steady-state value **D** to **D + d,** where **d** is a small change in the duty cycle), the following changes occur in the circuit, which can be directly associated with the small-signal model. Upper-case letters (e.g., V_{OUT}, V_{IN}, D, etc.) are used to represent steady-state values and lower-case letters (e.g., v_{out}, v_{in}, d, etc.) are used for small-signal (ac) parameters throughout the text.

Since node $\mathbf{V_{ph1}}$ **(**which is equal to $\mathbf{DV_{IN}}$ in steady-state) is connected to $\mathbf{V_{IN}}$ for an interval **dT** more often in period **T**, the node voltage increases to $\mathbf{V_{ph1} + dV_{IN}}$, which is represented by a voltage source $\mathbf{dV_{IN}}$ in the small-signal model [shown in Figure 3.13]. Since node $\mathbf{V_{ph2}}$ is connected to ground for an interval **dT** more often in period **T** (and to $\mathbf{V_{OUT}}$, **dT** interval less often), the node voltage decreases to $\mathbf{V_{ph2} - dV_{OUT}}$. This decrease in voltage is represented by a voltage source $\mathbf{dV_{OUT}}$ of opposing polarity. Inductor current $\mathbf{I_L}$ flows into the output node **d** times less than in steady state, which is represented by a current source $\mathbf{dI_L}$ flowing out of output node $\mathbf{v_{out}}$. Because of the increase in voltage across the inductor, there is a net increase in inductor current ($\mathbf{i_{in1}}$). Part of this current $\{\mathbf{(D^{/}–d)\ i_{in1}}$, which is approximately equal to $\mathbf{D^{/}i_{in1}}$, since both **d** and $\mathbf{i_{in1}}$ are small quality resulting in their product even smaller, flows into the output node.

Therefore, the net current "$\mathbf{D'i_{in1} - dI_L}$" flowing into the output node increases the output voltage to $\mathbf{V_{OUT} + v_{out1}}$. Due to the increase in output voltage, node voltage $\mathbf{V_{ph2}}$ increases by $\mathbf{(D'-d)v_{out1}}$, approximates as $\mathbf{D'v_{out1}}$ since both **d** and $\mathbf{v_{out1}}$ are small quantities, which reduces the inductor current from $\mathbf{i_{in1}}$ to $\mathbf{i_{in}}$, and ultimately settles down the output voltage increase to $\mathbf{v_{out}}$. The equivalent circuit model shown in Figure 3.13 (a) represents these parameters.

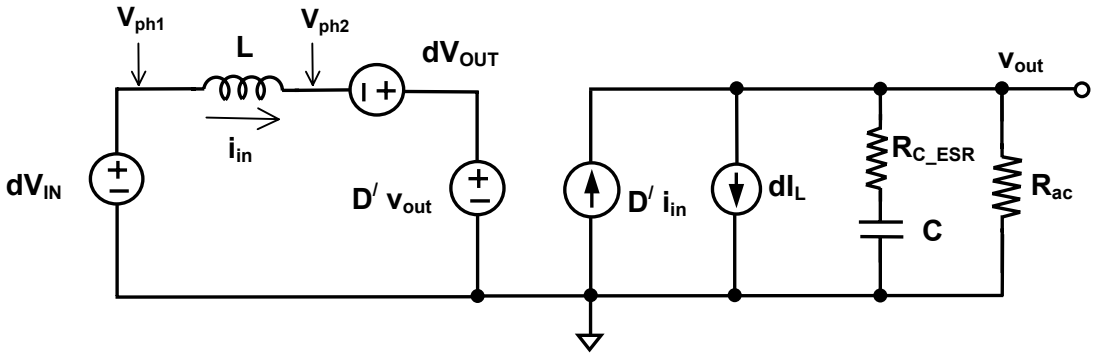


Figure 3.13. Time-averaged small-signal model of the buck-boost converter power stage with respect to a change in duty cycle.

The derivation of control-to-output transfer function from the small-signal model described earlier is straightforward, and therefore a detailed derivation is not presented here. The control-to-output transfer function, without the effect of the output capacitor's ESR (R_{C_ESR}), is given by

$$\frac{v_{out}}{d} = \frac{V_{OUT}}{DD'}\left(\frac{1-\dfrac{s}{(D'^2V_{out}/DLI_O)}}{1+\dfrac{s}{D'^2R_{ac}/L}+\dfrac{s^2}{D'^2/LC}}\right), \tag{3.8}$$

which is consistent with the equation for the inverting buck-boost converter [27]. The dc gain of the transfer function is dependent on the output voltage and duty cycle. The

second-order denominator implies existence of complex conjugate poles, while the numerator signifies a right-half plane (RHP) zero.

The decrease in output voltage, instead of the steady-state increase predicted by Equation (3.5) when the duty cycle is slightly increased can be seen as an *opposing feed-forward effect*, which is the physical meaning of a right-half plane (RHP) zero. The physical origin of a RHP zero in a circuit (e.g. miller-compensated two-stage operational amplifier [67]) can also be explained as a combination of two parallel gain paths having opposite polarity. The RHP zero is located at a frequency where the gains of both the paths are equal. From the small-signal model as shown in Figure 3.13, it is seen that current sources "$\mathbf{D'i_L}$" and "$\mathbf{dI_L}$" flow into the output node, but with opposite polarity, and can be equated to determine the location of the RHP zero, as given in Equation (3.8).

The existence of the RHP zero is inherent in the converter topologies where an increase in duty cycle causes a decrease in the time interval for which current flows into the output node, thereby discharging the output voltage (opposite feed-forward effect of increasing duty cycle). By using alternate switching control mechanisms (e.g., tri-state boost converter [68]), where the time interval for which output current flows into output node is made independent of the duty cycle increase, the RHP zero is eliminated.

3.3.2 Small-Signal Model with Respect to Line (Input) Voltage Change

When the input voltage changes from $\mathbf{V_{IN}}$ to "$\mathbf{V_{IN} + v_{in}}$," the following changes occur in the power stage (Figure 3.8). Node voltage $\mathbf{V_{ph1}}$ increases by $\mathbf{Dv_{in}}$ and can be represented by a voltage source [Figure 3.14]. Due to the increase in the voltage across the inductor, the inductor current increases by $\mathbf{i_{in1}}$, part of which flows into the output node as $\mathbf{D'i_{in1}}$, increasing the output voltage by $\mathbf{v_{out1}}$. The increase in output voltage increases the node voltage $\mathbf{V_{ph2}}$ by $\mathbf{D'v_{out1}}$, which reduces the inductor current increase to $\mathbf{i_{in}}$, and an output voltage increase of $\mathbf{v_{out}}$. These parameters are represented in the equivalent circuit model shown in Figure 3.14.

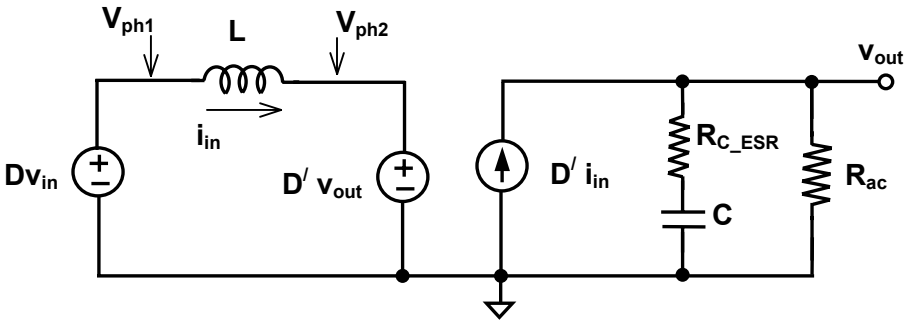


Figure 3.14. Time-averaged small-signal model of the buck-boost converter power stage with respect to a change in line (input) voltage.

The line-to-output transfer function, without considering R_{C_ESR}, is given by

$$\frac{v_{out}}{v_{in}} = \frac{D}{D'}\left(\frac{1}{1+\frac{s}{D'^2 R_{ac}/L}+\frac{s^2}{D'^2/LC}}\right). \tag{3.9}$$

Unlike control-to-output transfer function, the dc gain of a line-to-output transfer function depends on only the converter's duty cycle. The complex conjugate poles are located in the same frequency as for the control-to-output transfer function, while there is no right-half plane zero.

Equations 3.8 and 3.9 are compared with a standard second-order transfer function in [67], and the expression for dc gain, poles and zeros are presented in Table 3.2. Also, the effect of the output capacitor ESR, which introduces a left-half plane (LHP) zero in both the transfer functions is shown. The absence of RHP zero in the line-to-output transfer function can be explained from the fact that with small rise in input voltage only an increase in the current flowing into the capacitor is observed. On the contrary, with a duty cycle increase although inductor current increased, the current flow into the capacitor decreased initially before a net increase is observed, which is responsible for the RHP zero phenomenon.

Table 3.2. Small-signal transfer function parameters of the noninverting buck-boost converter.

	Change in duty cycle	Change in line voltage	Units
DC Gain	V_{out} / DD'	D / D'	-
Center frequency	$D' / 2\pi\sqrt{LC}$	$D' / 2\pi\sqrt{LC}$	Hz
Denominator Q	$D'R_{ac} / \sqrt{L / C}$	$D'R_{ac} / \sqrt{L / C}$	-
Right-half plane zero	$D'^{2}(V_{out} / I_{O}) / 2\pi DL$	∞	Hz
Left-half plane zero	$1 / 2\pi R_{C\_ESR} C$	$1 / 2\pi R_{C\_ESR} C$	Hz

3.3.3 Transfer Function Analyses under Different Loads

The load at the converter output can vary significantly according to the application. To design the converter's control-loop compensation to be stable across all loading conditions, the transfer function (derived earlier in Subsection 3.3.1) is analyzed for two extremes: (a) a pure current source load with high ac output impedance and (b) a simple resistive load with relatively low impedance, which is equal to the resistor value itself. For loads of equal current, the ac impedance (R_{ac}) modulates the quality factor (Q-factor) of the second-order denominator of the control-to-output transfer function [Equation 3.8] between the two extremes just identified.

The gain and phase plots comparing the control-to-output transfer function frequency response for the two loads are presented in Figure 3.15. A converter with 2.2 μH inductor (L) with 47 μF output capacitor (C) having a ESR (R_{C_ESR}) of 70 mΩ operating with a duty cycle (D) of 0.75 supplied from 3 V input and loaded by a 10 Ω resistive and 0.4 A current-sink load with ac resistance (R_{ac}) of 1 MΩ are used for the plots. For a resistive load, an increase in the output voltage directly translates to an increase in the load current, thereby absorbing the extra energy during the peak, which is ultimately reflected as degraded quality (Q)-factor that is observed as a lower peaking in the bode plot. For a current-sink load, an increase in the output voltage does not affect its current (because of its high impedance); consequently, its Q and peaks are higher. The

real part of the complex-conjugate poles, the right- and left-half plane (capacitor ESR zero) zeros remain unchanged under both loading conditions.

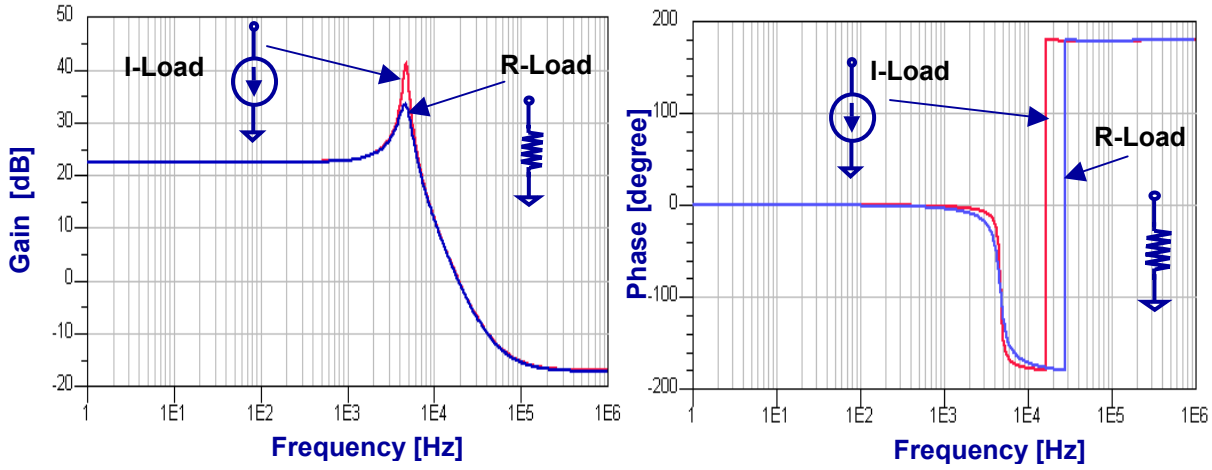


Figure 3.15. Power stage frequency response of the noninverting buck-boost converter with respect to change in duty cycle.

3.4 Power Stage Design

3.4.1 Selection of Power Inductor

A buck-boost converter designed to generate a variable output voltage from a wide input supply range operates at its maximum duty cycle (D_{MAX}) when the output voltage is at its maximum (V_{OUT_MAX}) with the minimum input supply voltage (V_{IN_MIN}). Consequently, considering a finite voltage drop of V_{SW} across the power switches (in Figure 3.8) and using Equation 3.5 the converter's maximum duty-ratio is given by

$$D_{MAX}= \frac{V_{OUT\_MAX} + 2V_{SW}}{V_{IN\_MIN} + V_{OUT\_MAX} - 2V_{SW}}. \qquad (3.10)$$

Since the inductor is connected to the output node (Figure 3.8) for a time of (1-D)T over the total time T, the average output current (I_{LOAD}) is equal to (1-D) times the average inductor current (I_{L_AVG}). Therefore, the average current flow in the inductor reaches at

its maximum under the conditions of maximum load current (I_{LOAD_MAX}) and duty cycle, which is given by

$$I_{L\_AVG\_MAX} = \frac{I_{LOAD\_MAX}}{1 - D_{MAX}}. \tag{3.11}$$

The value of peak-to-peak inductor current ripple (ΔI_L) is selected such that the inductor current remains continuous, and therefore must be a fraction of the maximum average inductor current and the power inductor value is selected accordingly. When the converter operates with its maximum duty cycle, the difference of input voltage and switch voltage drops is impressed across the inductor for a time interval equal to $D_{MAX}T_S$, which is described by the following equation

$$L\frac{\Delta I_L}{D_{MAX}T_S} = V_{IN} - 2V_{SW}, \tag{3.12}$$

where T_S is the converter's switching period. Rearranging the parameters in Equation 3.12, the value of the power inductor is calculated as

$$L = \frac{(V_{IN} - 2V_{SW})D_{MAX}}{f_S \Delta I_L}, \tag{3.13}$$

where f_S is the switching frequency of the converter, which is given by the inverse of time period. The inductor current, under maximum duty cycle and loading conditions, has a dc value of $I_{L\_AVG\_MAX}$ with a triangular waveform of peak-to-peak value ΔI_L. Therefore, the peak current rating of the inductor is given by

$$I_{L\_MAX\_PEAK} = I_{L\_MAX\_AVG} + \frac{\Delta I_L}{2}, \tag{3.14}$$

and root-mean-square current rating is given by

$$I_{L\_RMS\_MAX} = \sqrt{I_{L\_AVG\_MAX}^2 + \frac{\Delta I_L^2}{12}}. \tag{3.15}$$

3.4.2 Selection of Output Capacitor

In a buck-boost converter, the function of output capacitor is to store the inductor energy when both the components are connected, and later provide the load current when inductor is disconnected from the output node. Due to the charging and discharging of the output capacitor, its terminal voltage changes during the switching period yielding a ripple voltage. When the converter operates with its maximum duty cycle and load current, the drop in the output capacitor's terminal voltage (ΔV_{OUT_CAP}) is given by

$$\Delta V_{OUT\_CAP} = \frac{I_{LOAD\_MAX} D_{MAX}}{f_S C_{OUT}}. \tag{3.16}$$

Since there is no inductive element between the output diode (switch) and the capacitor, large instantaneous surge currents flowing in and out of the output capacitor generate an output ripple voltage that is dependent on its ESR and equivalent series inductance (ESL), which is a parasitic element in series with the capacitor. Assuming the capacitor has a small ESL, which is typically the case for ceramic capacitors, output ripple voltage due to its ESR (ΔV_{OUT_ESR}) is given by

$$\Delta V_{OUT\_ESR} = I_{C\_PEAK} R_{C\_ESR}, \tag{3.17}$$

where I_{C_PEAK} is the peak-to-peak capacitor current, which is from $-I_{LOAD\_MAX}$ to ($I_{L\_MAX\_PEAK} - I_{LOAD\_MAX}$), effectively equal to $I_{L\_MAX\_PEAK}$.

The total ripple voltage is due to discharging of the output capacitor when it provides the load current, and instantaneous current flow through its ESR and is given by

$$\Delta V_{OUT} = \Delta V_{OUT\_CAP} + \Delta V_{OUT\_ESR} = \frac{I_{LOAD\_MAX} D_{MAX}}{f_S C_{OUT}} + I_{C\_PEAK} R_{C\_ESR}. \quad (3.18)$$

For a given targeted value of output ripple, the output capacitor and its desired ESR can be estimated from Equation 3.18.

3.4.3 Selection of Input Capacitor

Similar to its output, the instantaneous value of current flowing in and out of the input capacitor is high in noninverting, buck-boost converters. Similar to the discussion offered for the output capacitor, assuming the capacitor has a small ESL, the maximum input ripple voltage (ΔV_O) is given by

$$\Delta V_{IN} = \Delta V_{IN,CAP} + \Delta V_{IN,ESR} = \frac{I_{IN\_MAX} D_{MAX}}{f_S C_{IN}} + I_{C\_PEAK} R_{C\_ESR}. \quad (3.19)$$

For a given targeted value of input voltage ripple, the output capacitor and its required ESR can be estimated from Equation (3.19).

3.5 Control Loop Design

3.5.1 Control Scheme and Frequency Compensation

While other controlling schemes, such as peak-current, average-current mode pulse width modulation (PWM) architectures [69]-[70] can be used for closed-loop control, voltage mode was considered for this design because of its simplicity -no inductor current information is required. Voltage-mode control enjoys popularity in the industry for simple, point-of-load dc-dc converter applications [71].

Figure 3.16 shows the schematic of a voltage mode PWM control scheme for the noninverting, buck-boost converter. The error amplifier's output is compared with a fixed frequency sawtooth signal by the PWM comparator to generate digital pulses that controls the switching on and off of the power transistors such the feedback node (V_{FB})

and control node (V_{CON}) voltages at the error amplifier's output are equal. The feedback voltage is related to the converter's output voltage by the feedback resistors. For a given control voltage, an increase in output voltage results in a increase in the feedback node voltage, which decreases the error amplifier's output voltage. As a result, the gate signal pulse widths of power switches MP_1 and MN_1 decreases, thereby reducing the converter's duty cycle and ultimately decreasing the output voltage to its desired value. Similarly, a decrease in the output voltage increases the error amplifier's output voltage, consequently increasing the dutycycle such that conveter's output voltage reaches its desired value.

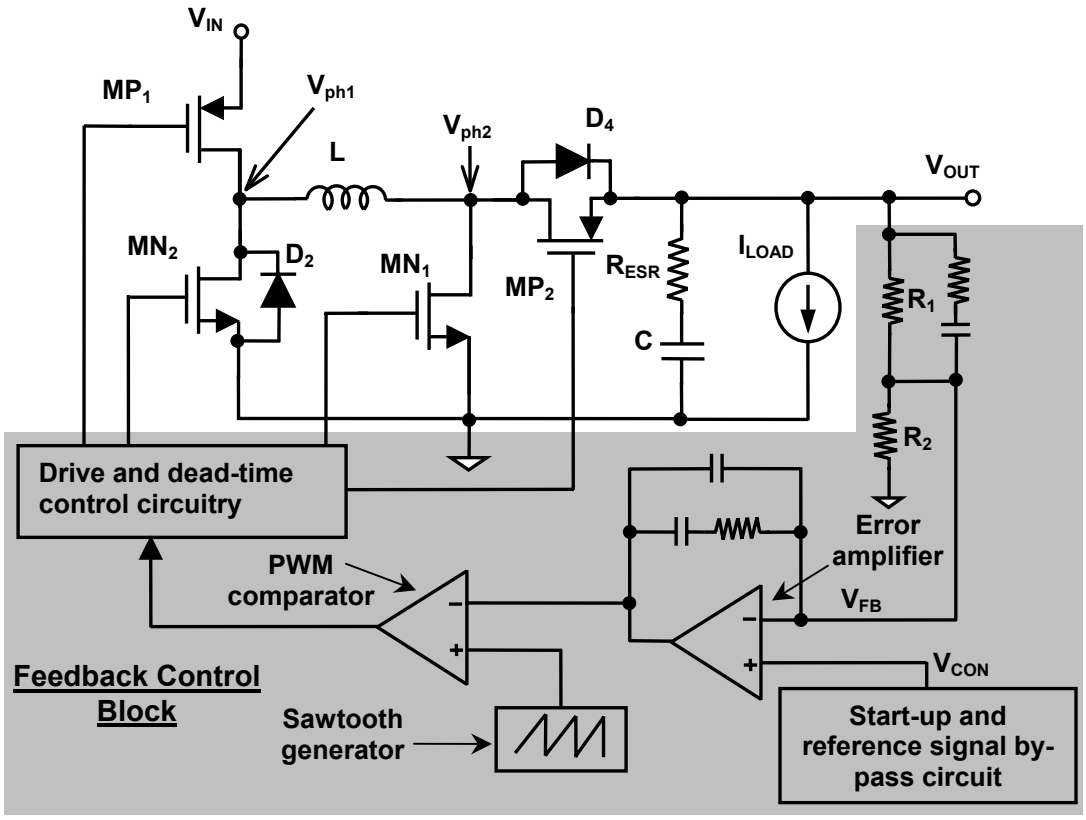


Figure 3.16. Voltage-mode PWM controlled, non-inverting, synchronous buck-boost dc-dc converter.

As with any other circuit operating with negative feedback, unless it is inherently stable (e.g., single-pole systems), frequency compensation is required for stable operation of the converter. Similar to the boost converter, the right-half plane (RHP) zero limits the unity-gain frequency (UGF) of the closed-loop performance of the buck-boost converter. Therefore, the RHP zero is designed to reside far beyond the UGF, in other words at higher frequency. Considering the expression given in Table 3.2, the RHP zero is at the lowest frequency when the duty cycle is at its peak, which corresponds to the highest output voltage value. For a specified V_{OUT}, load current $I_{LOAD,}$ and input voltage V_{IN} combination, a smaller inductor pushes out the RHP zero, but increases the peak-to-peak ripple current in the inductor. A higher inductor current not only results in larger peak-current rating requirements for the switching devices, but also induces more rms power losses in the current-flowing path. Once the RHP is located at a higher frequency compared to the UFG of the loop, the compensation design depends on the location of the left-half plane (LHP) zero arising as result of the ESR of the output capacitor. Feedback-loop compensation design for the two cases, (a) when the ESR zero is located within the desired UGF and (b) when the ESR zero is far from the desired UGF, have been explained in [72]-[73].

As explained earlier in Section 3.3, the control-to-output transfer function poles and zeros vary with the duty cycle. Figure 3.17 shows the frequency responses of the buck-boost converter's power stage for two duty cycle values. The dc gain of the converter's power stage is larger for a higher duty cycle. In addition, the complex conjugate poles due to the power inductor and output capacitor and the RHP zero occur at a lower frequency compared to a lower duty cycle operation of the converter. Therefore, the error amplifier's compensation network is designed for the worst-case conditions when the poles and zeros occur at the lowest frequencies, which occurs for maximum duty cycle condition.

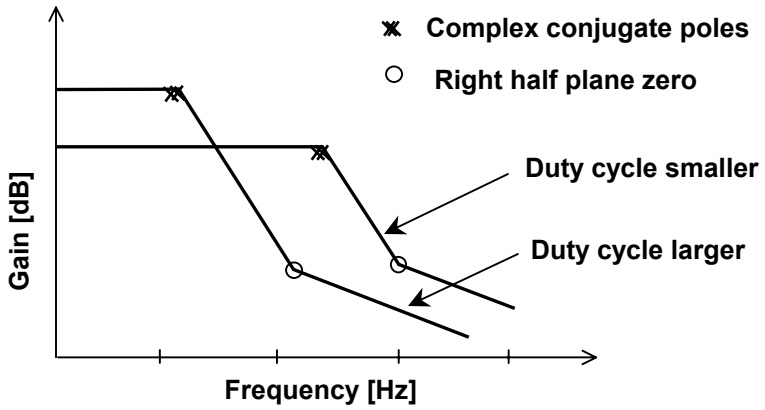


Figure 3.17. Frequency response of the buck-boost converter's power stage for two duty cycle values.

3.5.2 Duty-Cycle Limiting

During start-up and transient events (load and control signal), duty cycle changes between extreme limits, i.e, zero and unity. For example, during start-up, the converter's reference voltage can be higher than the sensed feedback voltage. Consequently, the error amplifier's output goes to the positive rail, in other words, equal to or greater than the peak sawtooth voltage, which results in the PWM comparator's output reaching the negative rail throughout the entire switching period. Transistors MP_1 and MN_1 (Figure 3.16) are therefore turned on, impressing the input voltage across the inductor. The inductor current never flows into the output during this interval; therefore, the output voltage remains unchanged. However, the inductor current continues to increase until the resistance of its path limits it, but such a high current can damage the inductor and power switches, even before reaching the limit, especially if it is sustained. Simplistically, this phenomenon is avoided by choosing the positive rail supply voltage of the error amplifier to be less than the peak value of the sawtooth waveform, as shown in Figure 3.18, thereby limiting the duty cycle to less than unity. The disadvantage of limiting the error amplifier's output voltage is that it requires an additional supply voltage for the error amplifier, which is lower than the peak value of the sawtooth waveform.

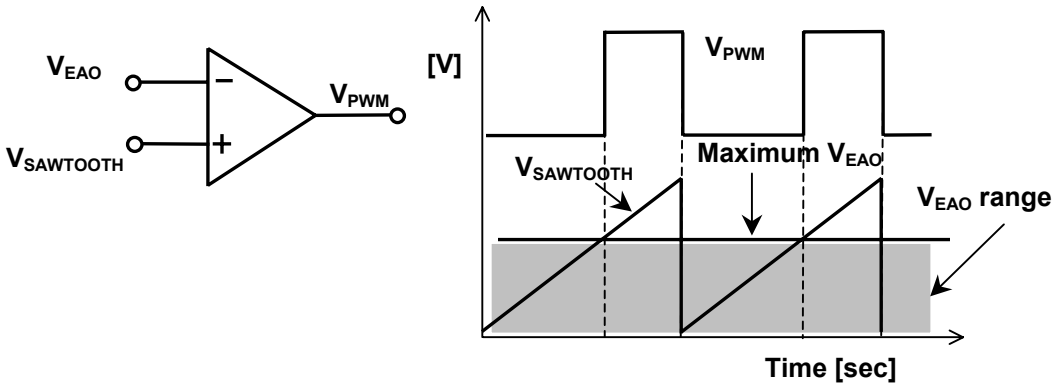


Figure 3.18. Duty-cycle limiting of the buck-boost converter with restricted error amplifier supply voltage.

Alternatively, the error amplifier's output can be clamped to a voltage lower than the peak sawtooth voltage such that the converter is prevented from operating with a duty cycle of unity. In a low-supply voltage environment, the dynamic range of the sawtooth signal itself is limited and designing an error amplifier with even lower supply voltage is challenging. Figure 3.19 illustrates the schematic an alternate circuit and its waveforms, where the converter's duty cycle is limited through proper processing of the PWM signal, having a predefined maximum duty-cycle signal (V_{DC_MAX}). The limiting duty-cycle signal is generated by comparing the sawtooth signal with a dc voltage V_{DCL}.

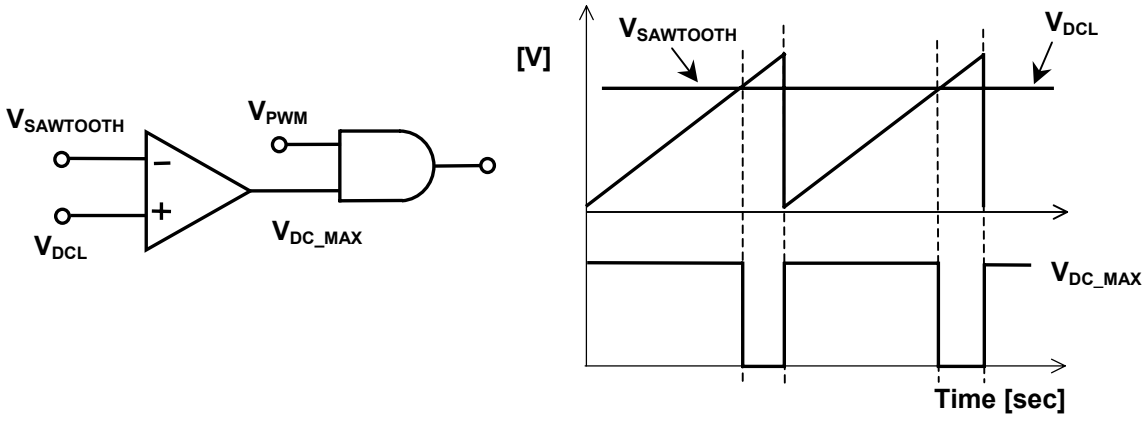


Figure 3.19. Duty-cycle limiting in a buck-boost converter for low supply voltage environment.

3.5.3 Dead-Time Control

Dead-time control in synchronous converters is required to prevent "shoot-through current" losses, which is an unnecessary power loss resulting when the rectifier and pass transistors are both conducting current simultaneously briefly "shorting" the supply to ground. The goal of dead-time control circuit is to convert an input duty-cycle waveform into two non-overlapping clock waveforms. A simple fixed-delay dead-time control scheme and relevant waveforms are shown in Figure 3.20. The input PWM signal is delayed by a fixed time and directly used as gate drive signal (V_{GATE1}) for the buck PMOS transistor. With V_{GATE1} transitioning from low to high, the node voltage V_{PH1} changes from V_{IN} to ground due to the body-diode conduction, which is sensed and used to turn the buck stage synchronous NMOS switch on. The synchronous rectifier is turned off when the actual PWM signal transitions from high to low, and after a certain delay the PMOS pass transistor in turned on. The boost stage NMOS pass transistor's and PMOS synchronous rectifier's gate signals are the inverse gate signals for buck stage PMOS pass transistor and NMOS synchronous rectifier, respectively.

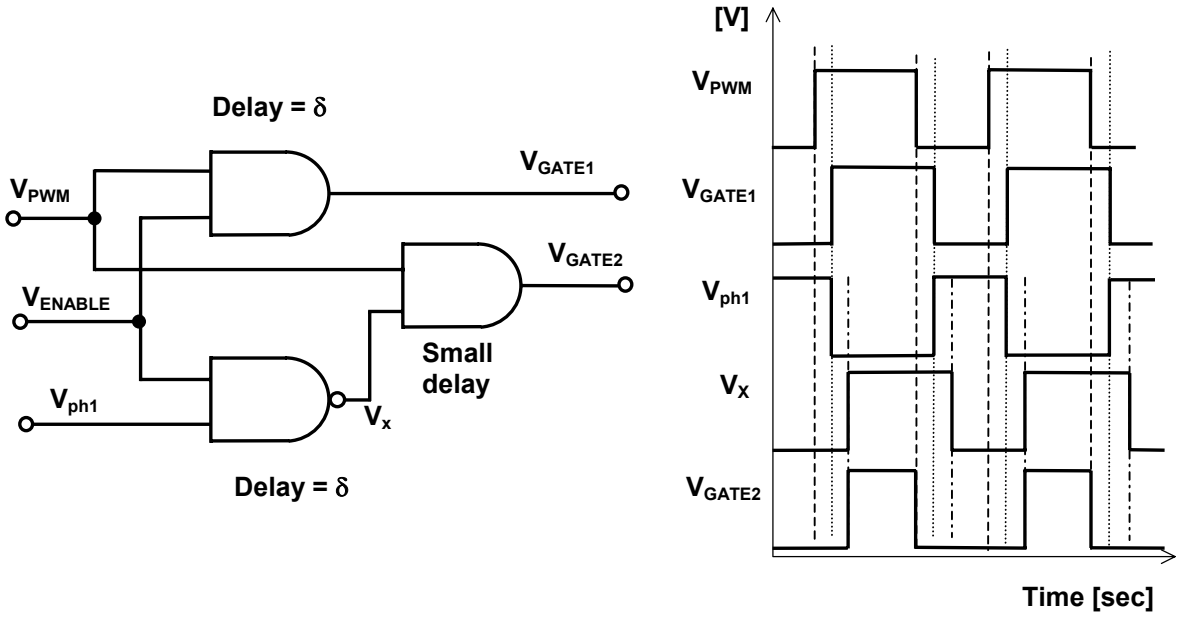


Figure 3.20. Fixed dead-time control and its relevant waveforms for the buck-boost converter.

3.5.4 Start-Up Circuit

To reduce transient surges during a power-on sequence, and prevent catastrophic failures, a start-up circuit as shown in Figure 3.21 is incorporated into the design of the converter. When the supply is turned on, the comparator's output is high and the voltage at its negative input node is slowly increased, which is dependent on resistance R_1 and capacitance C_1. During this period, the slowly charging terminal voltage of capacitor C_1 is used as the control signal for the converter, thereby slowly building up its output voltage. After capacitor C_1's node voltage reaches a predetermined threshold, depending on the supply voltage and resistances R_3 and R_4, the comparator's output goes low and the actual external control signal is used for the dc-dc converter. Resistance R_2 along with C_2 act as a noise filter to provide a clean control signal for the buck-boost converter.

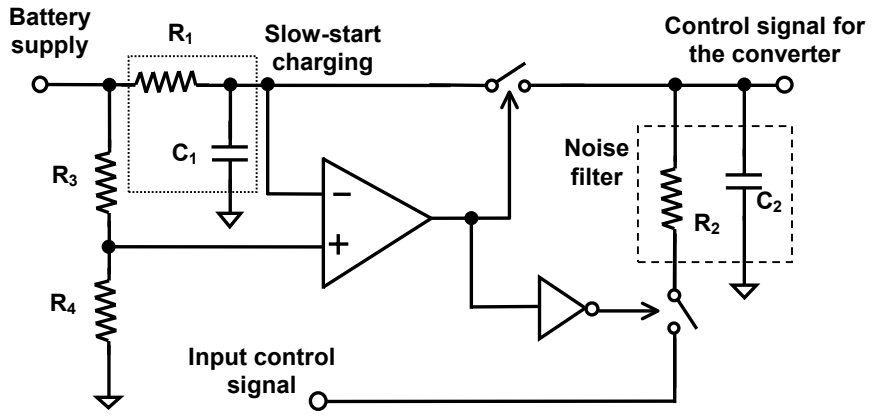


Figure 3.21. Slow-start circuit schematic suitable for the buck-boost converter.

3.6 Buck-Boost Converter Power Losses

Theoretical estimation of power losses in the converter is essential to estimate and improve efficiency performance by using power-saving techniques. Power losses in a switching converter are classified in two categories: conduction and switching losses. Current flow through non-ideal power transistors, filter elements, and interconnections results in conduction power losses.

To avoid "shoot-through" current, dead-time control schemes are adopted in almost all synchronous converter topologies. However, during the dead time, the current flows through the diodes resulting in higher power losses because of the inherent larger voltage drop (V_{ON} equals to 0.6 – 0.7 V), which is referred as body-diode conduction losses. The dead-time control circuits must therefore be optimally designed for higher efficiency, while avoiding "shoot-through." As for any switching converter topology, the switching nodes incur power losses due to the overlap of voltage and current in the switching devices. This loss is dependent on load current, node voltage swing, and converter switching frequency. Similarly, power losses result when charging and discharging the gate capacitances of the power switches, which is referred as gate-drive loss.

Mathematical expressions for the various power loss mechanisms in switching converters are found in [27], [74]-[75]. The power loss equations for a buck-converter given in [75] are extended for the buck-boost converter, which are presented in Table 3.3. Various notations used in the table are as follows: I_L, $I_{L,rms}$, and ΔI_L are the average, root-mean-square (rms), and peak-to-peak inductor current, respectively, t_{dead} is the dead time, R_{DS} is the transistor's on resistance, V_{DIODE} is the body-diode voltage drop, R_{L_ESR} is the equivalent series resistance of the inductor, I_{LOAD} is the load current, f_s is the switching frequency, C_{ISS} is the input capacitance of the switching transistor, t_X and t_Y are the voltage and current overlap time during switching on and off at V_{ph1}/V_{ph2} nodes, respectively, V_{GATE} is the NMOS gate-drive voltage, and k is the core loss factor of the inductor.

Table 3.3. Summary of power losses in the buck-boost converter.

Mechanism	Expression
CONDUCTION LOSSES	
Buck-PMOS and Boost NMOS	$DI_{L,rms}^2 (R_{DS\_PMOS} + R_{DS\_NMOS})$
Buck-NMOS and Boost PMOS	$\left(1 - D - \frac{2t_{dead}}{T_S}\right) I_{L,rms}^2 (R_{DS\_NMOS} + R_{DS\_PMOS})$
Body diodes	$\left(\frac{2t_{dead}}{T_S}\right) I_{L,avg} V_{DIODE}$
Inductor resistive loss	$I_{L,rms}^2 R_{L\_ESR}$
Capacitor ESR loss	$\left(DI_{OUT}^2 + (1-D)\frac{\Delta I_L^2}{12}\right) R_{C\_ESR}$
SWITCHING LOSSES and CORE LOSSES	
V-I overlap for V_{ph1}	$I_L V_{IN} t_X f_s$
V-I overlap for V_{ph2}	$I_L V_{OUT} t_Y f_s$
NMOS gate-drive losses	$2C_{ISS\_NMOS} V_{GATE}^2 f_s$
PMOS gate-drive losses	$C_{ISS\_PMOS} (V_{IN}^2 + V_{OUT}^2) f_s$
Core loss	$k I_{L,peak}^2 f_s$

3.7 Summary

In this chapter, various converter topologies suitable for noninverting buck-boost conversion are evaluated considering usage of minimum external component count and suitability for on-chip integration, which are the key requirements in portable applications. Noninverting synchronous buck-boost converter, with its four power switches and single inductor/capacitor pair offers the most attractive solution since the

power transistor can be implemented in a single chip and uses less number of external components when compared to other topologies. A transmission gate modification of the boost-stage synchronous PMOS transistor is proposed to enable the circuit to operate efficiently operation under low output voltage conditions. An intuitive analysis of the small-signal model of the converter based on the circuit operation, which avoids mathematically complex state-state approach, is offered. The control-to-output transfer function of the converter's power stage shows complex conjugate poles and a right-half plane zero.

The power stage design considerations presented in this chapter include selection of power inductor value under the maximum duty cycle and load current conditions. Similarly, the output capacitor is selected to meet the ripple voltage specifications of the converter. The converter's feedback control loop is compensated for the poles and zeros for maximum duty cycle and load current when the RHP zero occurs at the lowest frequency. The requirements and circuit topologies of duty cycle limiting circuit to the prevent the converter from catastrophic failure, dead time control to avoid "shoot-through" power loss and, start-up circuit to minimize initial transients are discussed. Finally, the power losses in a buck-boost converter are derived. Essentially, this chapter outlines the design equations and considerations for building a prototype system, which is addressed in the following chapter.

CHAPTER IV

PROTOTYPE CDMA RF PA WITH A POWER-TRACKING, DYNAMICALLY ADAPTIVE BUCK-BOOST SUPPLY

This chapter presents the prototype implementation and experimental results of the proposed linear RF PA with a power-tracking, dynamically adaptive, buck-boost supply for CDMA handsets. In CDMA IS-95 standard, the power changes from one level to the other at a much slower rate compared to the baseband envelope signal of 1.23 MHz (1 dB in 1.2 msec). Therefore, as discussed earlier in Chapter 2, adaptation of the supply voltage and bias current as a function of the RF power (termed as *power-tracking*) can be achieved with a converter with a lower switching frequency. A lower switching frequency converter essentially leads to higher light-load efficiency, thereby enabling the system to operate with a high efficiency over wide loading conditions and consequently increasing the battery life.

Typically, a PA is operated with its highest possible supply voltage that is limited by technology limitations especially break down voltage. By using a higher supply voltage, the PA undergoes a larger signal swing at its output, thereby delivering its peak output power with a lower current, and consequently minimizing the power losses in the current-flowing path. Therefore, in a low voltage portable environment, a noninverting buck-boost converter is essential to operate the RF system at its peak performance level throughout the battery voltage span, from a freshly charged to a fully discharged condition. The design, implementation, and experimental results of a discrete buck-boost converter prototype targeted for the dynamic supply of the PA are also presented in this chapter.

4.1 System Implementation

Although the conceptual representation of the proposed system is explained in Chapter 2, for completeness, the schematic of the PA system implemented as a discrete prototype is shown in Figure 4.1. The overall system is partitioned in three separate modules based on functionality and external components requirement. The directional coupler, power detector, and dynamic bias voltage generation circuit are implemented as one module. A prototype voltage-mode buck-boost converter is built on a separate board and a commercial PA is used to evaluate the system.

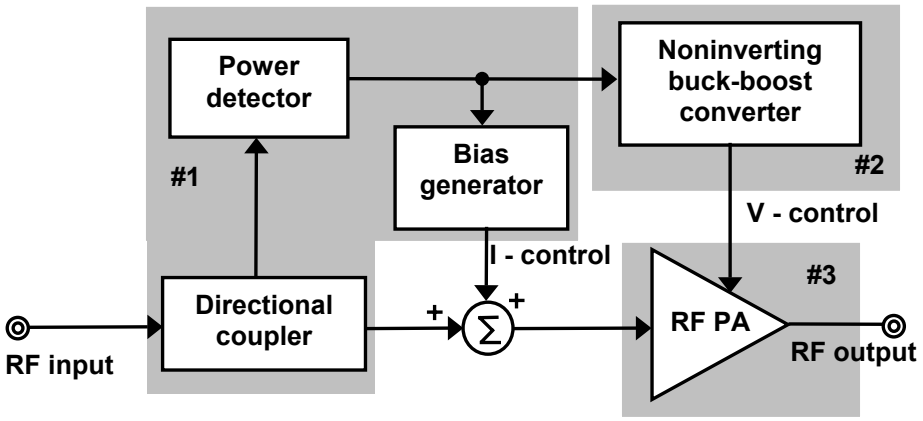


Figure 4.1. Schematic of the prototype CDMA PA system.

An evaluation board of an LDMOS PA using California Eastern Laboratory's (CEL) NE5520279A [76] operating in class-A/AB configuration is used for the prototype system. The schematic of the circuit used for generating the dynamic gate bias in the prototype PA system is shown in Figure 4.2. At any given instant, a control signal that sets the output of the buck-boost converter is impressed across resistance R_{BIAS_PA}, which is also proportional to the PA's load-line resistance [2] in the prototype implementation. The amplifier forces MN_1's source voltage to be equal to the control voltage, thereby setting a proportional current through MP_1. This current is reflected in MP_2 (current mirror MP_1 and MP_2) and flows through MN_2, which generates the desired gate voltage for the PA, MN_3. As the RF input power changes, the directional coupler's output voltage

that is used as a control signal for the converter and dynamic bias circuit also changes, thereby adjusting PA's supply voltage and bias current. In an integrated circuit, the control voltage, resistor R_{BIAS_PA} and the current mirrors can be suitably scaled down.

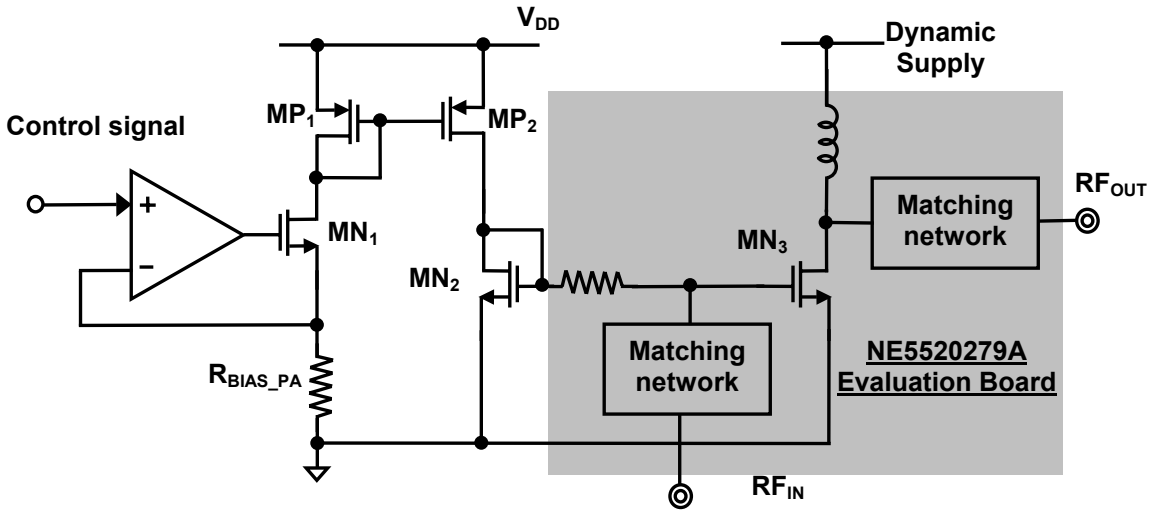


Figure 4.2. Schematic of RF PA along with its dynamic gate bias circuit.

A micro-strip, branch-line directional coupler [77] with coupling coefficient of 5 dB was designed and fabricated on a printed-circuit board (PCB), having a thickness 0.032 inches, permittivity (ε_r) of 4.8, and a loss tangent (tan δ) of 0.022. A commercial power detector (LTC 5505-2 from Linear Technology [78]) is used to detect the input RF power. The power detector's output voltage was suitably scaled using a gain-control circuit to generate the desired control signal for the dynamic converter and bias control block.

4.2 Noninverting Buck-Boost Converter Design

4.2.1 Specifications

The maximum output voltage and load current for the buck-boost converter is established from the supply voltage and bias current required by the PA to supply its maximum output power (27 dBm, in this case) while maintaining the desired linearity

{adjacent channel power ratio (ACPR) and error vector magnitude (EVM)} specifications. Since the PA characteristic is strongly dependent on its design, prior knowledge of its specifications is required while designing the adaptive power supply. For the PA used in the prototype, it is experimentally determined that a maximum supply voltage of 3.6 V and a quiescent current of 320 mA is sufficient to deliver 27 dBm of output power while exhibiting -45 and -65 dBc of first and second ACPR, respectively. A switching frequency of 500 kHz is chosen for the converter to use a smaller power inductor and output capacitor. A maximum ripple voltage of 100 mV is specified to limit the harmonics due to switching ripple to 40 dB below the RF signal level. Since the switching ripple lies inside the CDMA baseband bandwidth, a degradation in EVM expected, while the ACPR remains unaffected. These specifications of the buck-boost converter are summarized in Table 4.1.

Table 4.1. Prototype buck-boost converter specifications.

Parameter	Value
Input voltage	2.5 – 3.2 V
Output voltage	0.4 – 4.0 V
Load current	0.05 – 0.8 A
Ripple voltage	≤ 100 mV
Switching frequency	500 kHz

A theoretical estimation of the variation of supply voltage and bias current of the PA with RF power based on a supply voltage of 3.6 V and bias current of 320 mA for the peak RF power of 27-dBm is presented in Figure 4.3. As the RF power is decreased, ideally, the control signal decreases such the ratio of PA supply voltage and load current remains same as that is designed for the peak-power conditions. However, the transistor's supply voltage cannot be reduced to any arbitrarily small value, since the dynamically adaptive supply poses a minimum output voltage set by its minimum duty cycle. Furthermore, the transistor must be kept in the saturation region, even for a low output power, to obtain acceptable gain and linearity. Even if the desired supply voltage

calculated based on the signal swing falls below this limit, the PA supply voltage is kept at 0.4 V in this design.

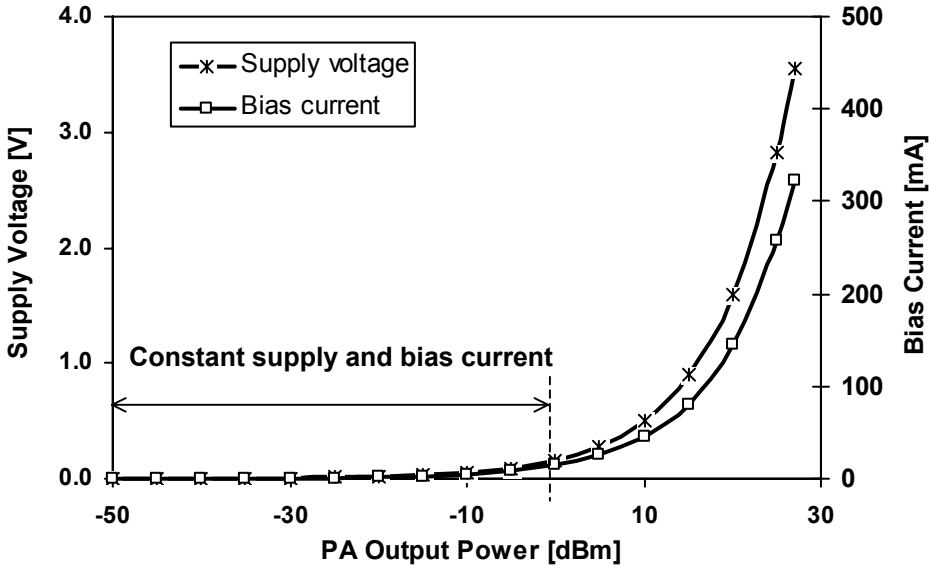


Figure 4.3. Approximate loading profile (supply voltage and bias current) of the CDMA RF PA with output voltage variation of –50 to 27 dBm.

4.2.2 Implementation

The design approach for a voltage-mode buck-boost converter presented earlier in Section 3.5 is used to implement the buck-boost converter as a dynamic supply for the PA. Figure 4.4 shows the schematic of the converter along with its component parameters. In this section, selection of power stage components of the converter is discussed followed by error amplifier compensation design.

A 2.2 μH power inductor and a 47 μF output capacitor with equivalent series resistance (ESR) of 70 mΩ were chosen for the prototype converter power stage, defining the peak inductor current to 3.0 A (peak-to-peak ripple current 1.5 A) and the output ripple voltage to 200 mV maximum, with a switching frequency of 500 kHz. For a constant switching frequency, a smaller inductor results in a higher inductor and switched peak-current ratings, which require a larger capacitor to achieve the same specified

output ripple voltage. A lower output ripple is critical for the overall system performance because any noise in the converter output directly couples to the PA output, which consequently increases spurious out-of-band distortion and degrades in-band modulation accuracy. Since large instantaneous values of current flows in and out of the output capacitor, assuming its ESL is small, the majority of the ripple is due to the ESR of the capacitor; hence, an output capacitor with a smaller ESR value is desirable.

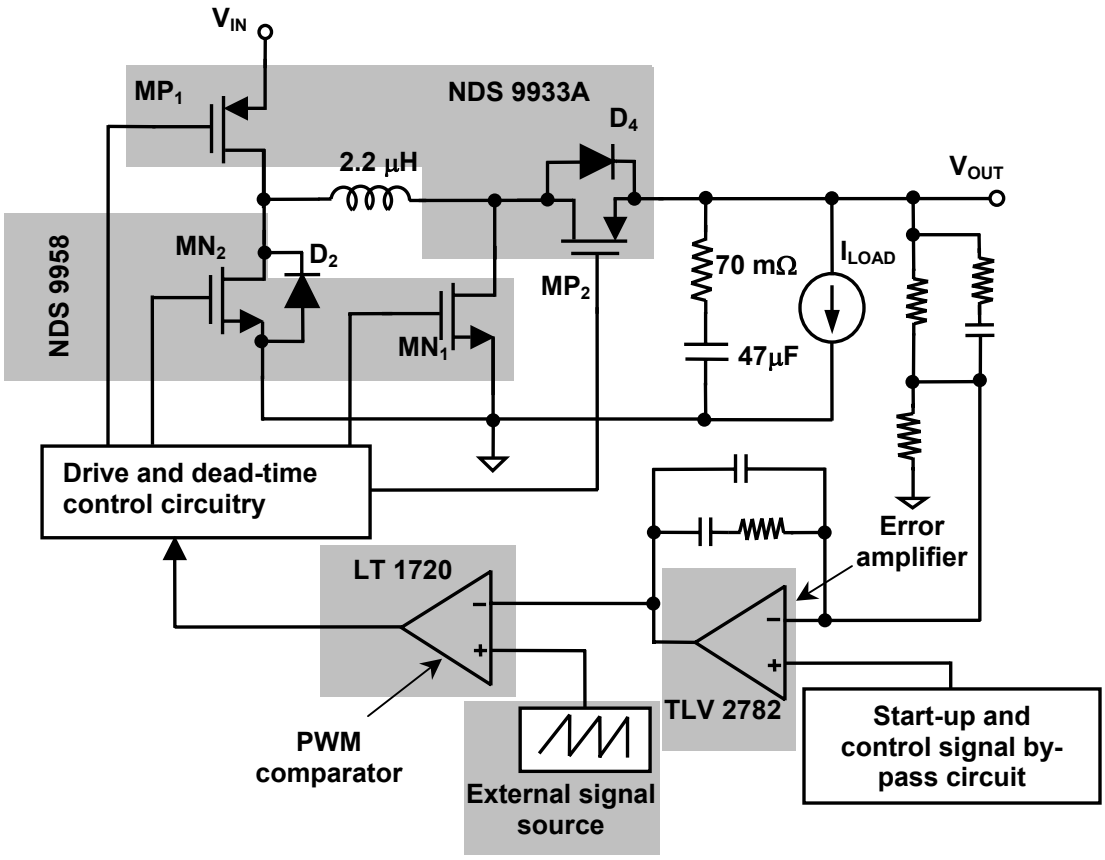


Figure 4.4. Voltage-mode, non-inverting, synchronous buck-boost dc-dc converter implementation.

The peak current rating of the power transistors is equal to the peak inductor current (3.0 A, in this case). The maximum average current flowing through the power switches is the product of maximum duty cycle (D_{MAX}) and corresponding maximum

average inductor current ($I_{L\_AVG\_MAX}$). Fairchild Semiconductor's NDS9933A dual-PMOS and NDS9958 dual-NMOS transistors are chosen for the prototype.

In continuous-conduction mode (CCM), the buck-boost converters' power-stage small-signal response shows a pair of complex-conjugate poles (related by inductor L, capacitor C, and duty cycle D), a right-half plane (RHP) zero (related by inductor L, duty cycle D, steady-state output voltage, and load current), and a left-half plane (LHP) zero (due to the ESR of the capacitor). The detailed derivation of the small-signal model is illustrated earlier in Section 3.3. Since the duty cycle varies dynamically to generate a time-varying output voltage, locations of the poles and RHP zero change. Therefore, the error amplifier's frequency compensation scheme is designed for the maximum value of the duty cycle, which results in the lowest pole and RHP zero frequencies.

The converter is designed to be stable for a maximum duty cycle of 0.75 and to achieve a closed-loop, unity-gain frequency (UGF) of 20 kHz. The LC-double poles, capacitor-ESR zero, and RHP zero are calculated (using expressions in Table 3.2) to be 3.912 kHz, 48.37 kHz, and 30.143 kHz, respectively. The DC gain of the power stage and PWM modulator are 26.58 dB and –12.04 dB (corresponding to a peak sawtooth voltage of 4 V), which results in a total open-loop DC gain of 14.54 dB.

A Type-III compensation scheme [72]- [73] is chosen, along with the component values as shown in Figure 4.5. The transfer function of the error amplifier is given by

$$A_{ea}(s) = \left[\frac{1}{sR_4(C_1 + C_2)}\right]\left[\frac{[s(R_4 + R_3)C_3 + 1][sR_2C_2 + 1]}{[sR_3C_3 + 1][sR_2(C_1 \parallel C_2) + 1]}\right]. \tag{4.1}$$

Resistors R_4 and R_5 set the closed loop gain of the feedback controller given by

$$\frac{V_{OUT}}{V_{CON}} = 1 + \frac{R_4}{R_5}. \tag{4.2}$$

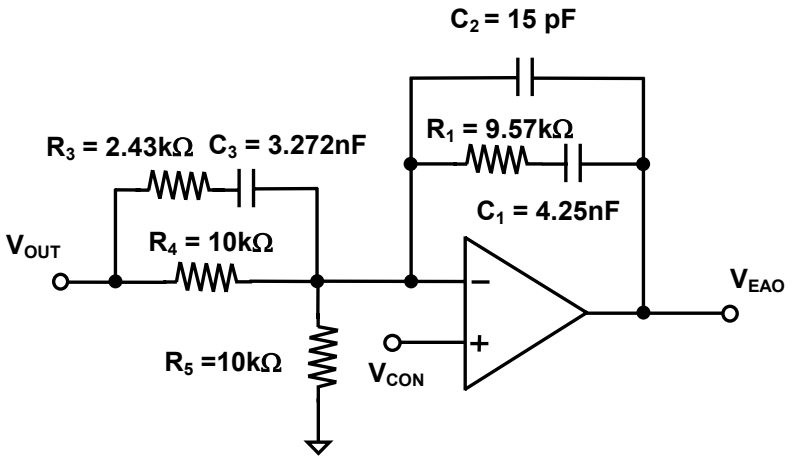


Figure 4.5. Type-III network (2-zeros and 3-poles) designed for compensating the buck-boost converter.

Two zeros [from R_1C_1, and the other from $(R_4 + R_3)\ C_3$] are added at the same frequency as the LC double pole to compensate for the gain and sharp phase change. Assuming C_1 is much larger than C_2, capacitor C_1 is selected to ensure the open-loop gain of the system (modulator, LC filter, and error amplifier) is 0 dB at the UGF. The values of R_3 and C_3 are chosen to place a pole at about one fifth of the switching frequency, 100 kHz in this design. Capacitor C_2 sets the high frequency pole and ensures 20 dB/dec roll-off (detailed expressions can be found in [73]).

The simulated gain and phase plots of the control-to-output transfer function of the power-stage and with error amplifier compensation network are shown in Figure 4.6. From the gain plot, it can be seen that the open-loop gain with error amplifier compensation crosses 0 dB at 20 KHz yielding the desired unity-gain frequency (UGF) for which the loop was designed. Corresponding phase plot shows a phase margin (PM) of 30^0. With the loop phase response crossing zero at a frequency of 100 KHz, corresponding gain plot shows –10 dB, which is the gain margin of the feedback loop.

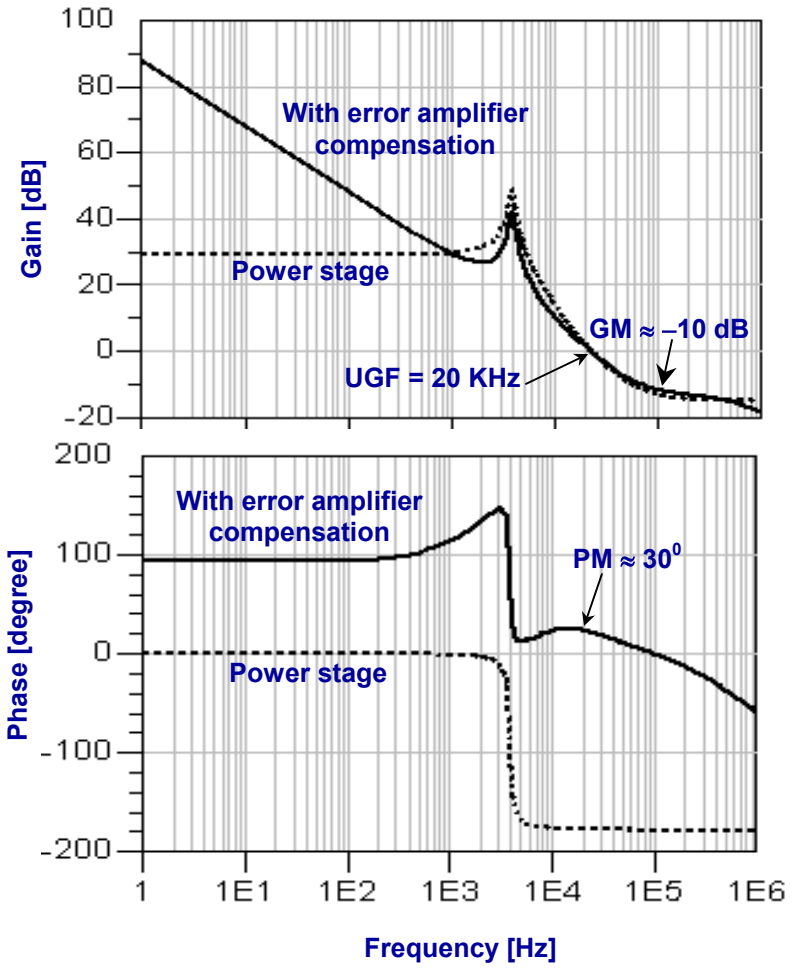


Figure 4.6. Gain and phase plots of the open-loop control-to-output transfer function of the buck-boost converter with and without the error amplifier compensation network.

A fixed dead-time control scheme is used in the prototype for generating non-overlapping clock-signals to prevent "shoot-through" current, which is an unnecessary power loss resulting when the rectifier (MN_2 and MP_2) and pass transistors (MP_1 and MN_1), as shown in Figure 4.4, conduct simultaneously. The duty cycle of the converter was limited to less than unity by choosing the error amplifier's positive rail supply smaller than the peak sawtooth voltage, which prevents MP_1 and MN_1 to be switched-on for a long time during the converter start-up and thereby eliminating the possibility of damaging the transistors $MP_1$and MN_1 and inductor L. A slow-start circuit described

earlier in Section 3.5 was incorporated in the prototype to reduce the initial transients and prevent potentially catastrophic failures. After the converter completes the start-up sequence, the control signal from the RF detector enables the reference signal for the converter. The research contributions resulting from the design and implementation of the dynamic buck-boost converter described in this section is reported in [79].

4.3 Experimental Results – Prototype Buck-Boost Supply

The prototype converter designed in the previous section was assembled in a printed-circuit board (PCB) and tested for both functionality and performance. The following paragraphs present the experimental results of the prototype converter. The node voltage V_{ph1}, output-ripple voltage, and inductor current waveforms shown in Figure 4.7 illustrate the functionality of the converter. Since no overlap is observed between the gate drive signals for the PMOS and NMOS transistors of the buck stage as shown in Figure 4.8, correct functionality of the dead-time control scheme was concluded.

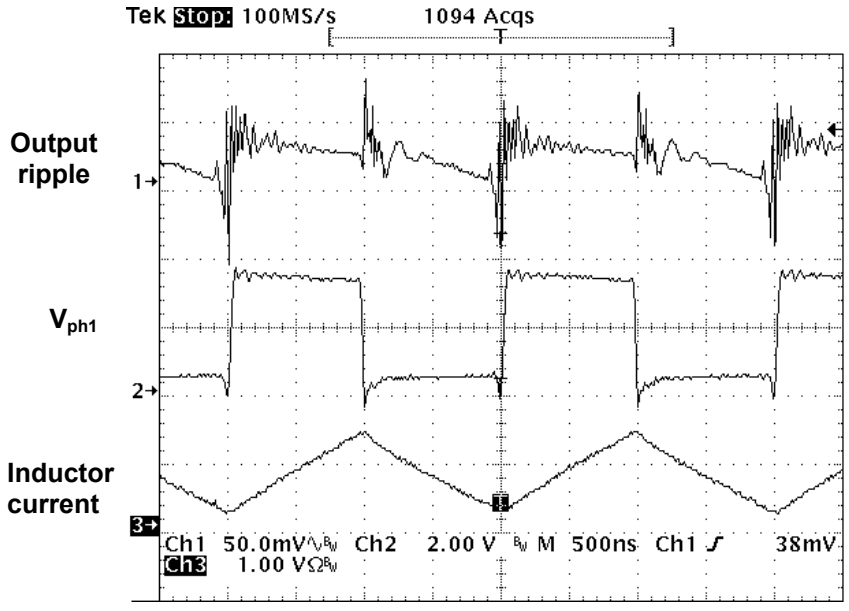


Figure 4.7. Experimental buck-boost converter waveforms: output ripple, node voltage $V_{ph1,}$ and inductor current waveforms.

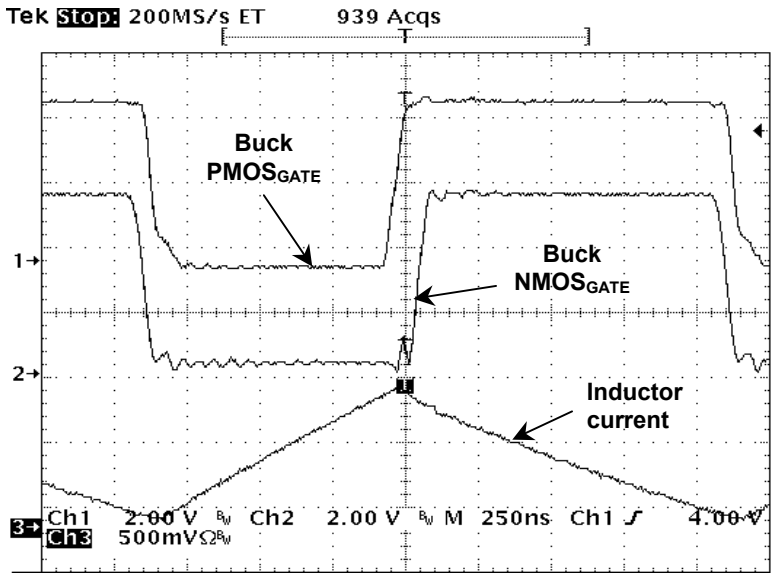


Figure 4.8. Experimental buck-boost converter waveforms: gate drive signals illustrating dead-time control.

Figures 4.9 illustrate the variation of percentage error in the output voltage with a maximum of 2.8 % at 0.4 V when loaded with a current source of 0.4 A. The error in the output voltage is attributed to the finite loop gain of the control loop limited by the error amplifiers dc gain, the parasitic resistance in the switching-current-flowing path and the offset voltage of the error amplifier. Since the absolute value of the error voltage is the same for equal load currents, with a higher output voltage the percentage error decreases. Finite dc gain of the converter's feedback loop results in a gain error, which along with the error amplifier's offset voltage are multiplied by the closed-loop gain of the converter, resulting in an error at the output.

Figure 4.10 shows the output peak-to-peak ripple with the output voltage with a maximum of 275 mV for a load current of 0.65 A at an output voltage of 4.0 V. The ripple in the output is the result of peak-to-peak ripple current flowing through the ESR and ESL of the output capacitor. For constant load currents, although the average inductor current is constant, ripple inductor current increases for higher output voltages (larger duty cycles). For resistive loads the load current increases with higher output

voltages, leading to higher peak-to-peak ripple currents and consequently higher ripple voltage.

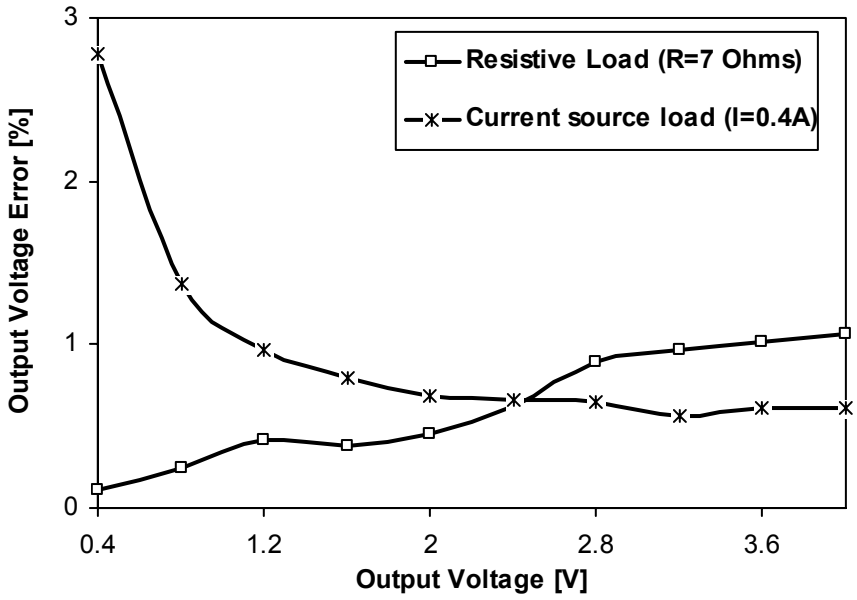


Figure 4.9. Percentage output voltage error of the prototype dynamic buck-boost converter.

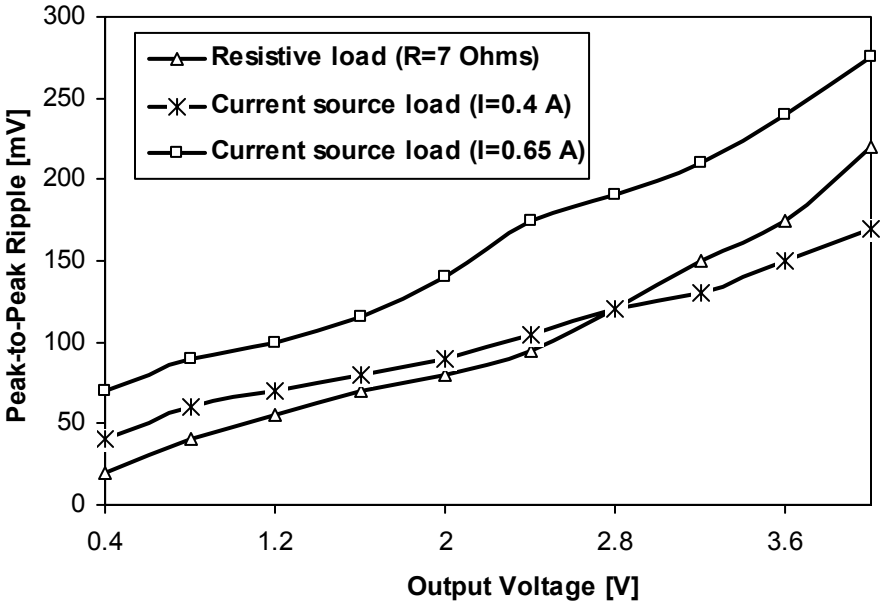


Figure 4.10. Peak-to-peak ripple voltage of the dynamic buck-boost converter prototype.

Although the maximum peak-to-peak ripple voltage was estimated theoretically for a maximum load current of 0.8 A, the prototype converter's ripple was measured up to 0.65 A because of higher power losses and resulting heat dissipation in the converter. The error between the estimated ripple of 172 mV for a 0.65 A load at 4.0 V output voltage and measured 275 value of mV can be attributed to several factors. Due to a lower power efficiency of the converter, the actual current flow through the capacitor's ESR is higher than the estimated value. Furthermore, because of the sharp current transition in the output capacitor in a buck-boost converter, the measured ripple also contains voltage spikes due to effective series inductance (ESL) of the capacitor and oscilloscope probes leads, the contributions of each part is not easily separable. In addition, the actual ESR value of the capacitor is measured to be 100 mΩ as opposed to the data sheet specifications of 70 mΩ.

Efficiency curves of the converter at various load currents and different output voltages are presented in Figure 4.11, showing higher efficiency at higher load current and output voltage. The converter shows lower efficiency compared to other state-of-the-art power supplies because of the discrete switches used in the prototype are not customized for low voltage applications - they have a much higher on resistance due to their reduced gate drive. The primary objective of the prototype implementation was to verify the functionality of the dynamic converter and therefore it was not optimized for higher efficiency. For the same output power but with higher current and lower voltage, conduction loss is more than with the lower current and higher voltage combination, resulting in degraded efficiency. Like other switching converters, the switching losses due to the gate drive charging and discharging is dominant at light loading conditions. Theoretical estimation of the converter efficiency for an output voltage of 3.6 V exhibits a reasonable match with the experimental results, as shown in Figure 4.12.

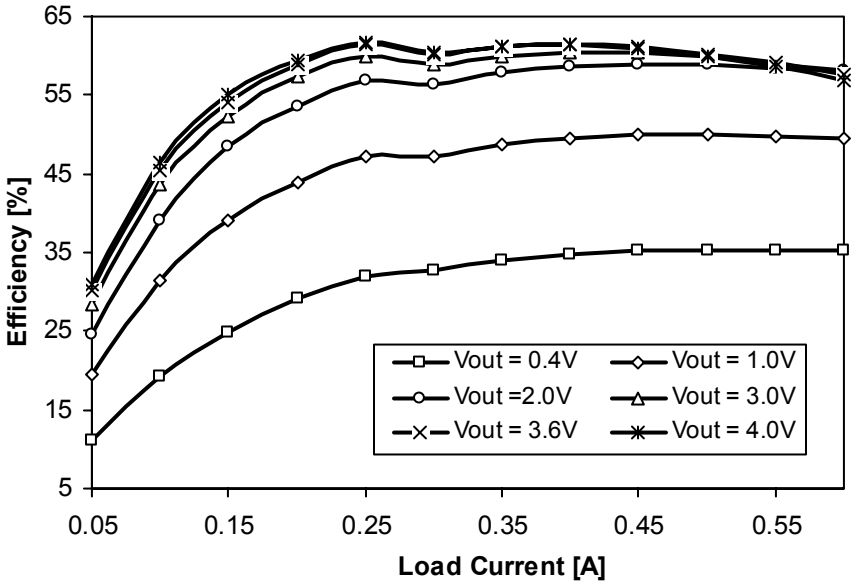


Figure 4.11. Efficiency curves of the buck-boost converter prototype.

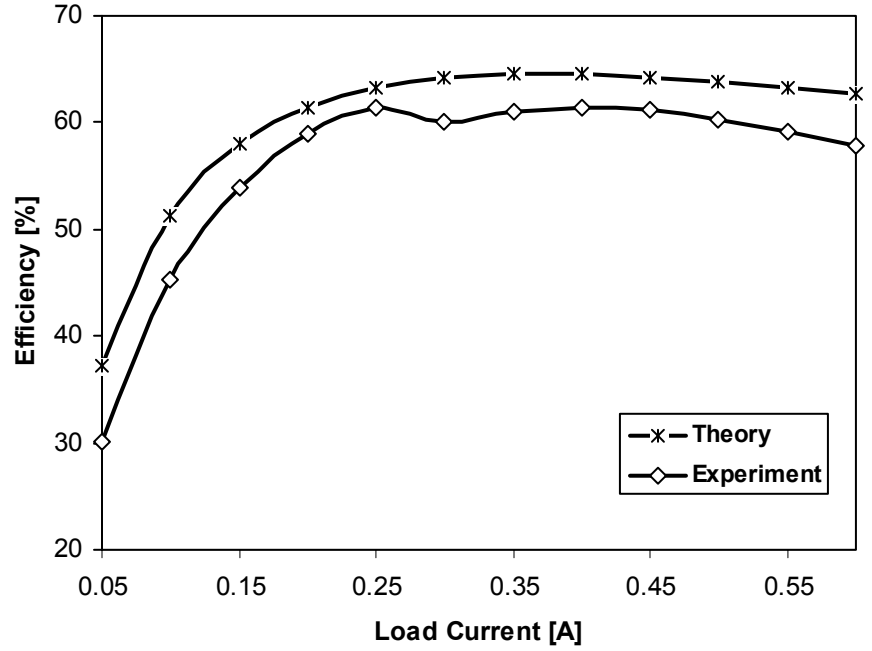


Figure 4.12. Comparison of theoretical and experimental efficiency results for output voltage of 3.6 V generated from an input supply of 3.0 V.

The measured line (LNR) and load (LDR) regulation of the buck-boost converter prototype are 0.3 % and –1 %, respectively. Figure 4.13 shows the change in output voltage with a step change in the control signal. The converter takes approximately 300 μsec to reach 4.0 V, from its initial condition of 0 V. Therefore the converter is suitable for use as a dynamic supply for a power amplifier CDMA IS-95 application, where in the worst-case a 1-dB power change (approximately a step control voltage of 10 %) occurs in 1.2 msec.

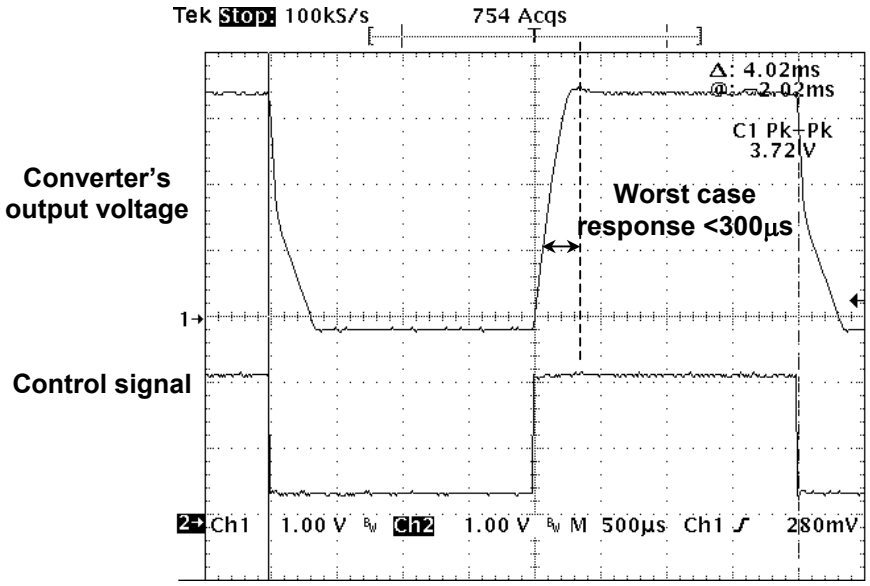


Figure 4.13. Prototype buck-boost converter's response to a worst-case step change in control signal

Figure 4.14 shows the transient response of the output voltage with a step change in load current of 0.5 A. The output voltage exhibits a transient and steady-stage error of 40 and 50 mV, respectively, and a response time of 200 μsec. Although the converter was not designed to meet any load transient response specification, its the ability to settle the about voltage for a load step illustrates the stability of its feedback control loop. The experimental results of the converter are compared with the targeted values in Table 4.2. All the target specifications are met by the converter except the output ripple voltage

because of the higher value of output capacitor ESR used in the prototype than that is expected from theoretical considerations.

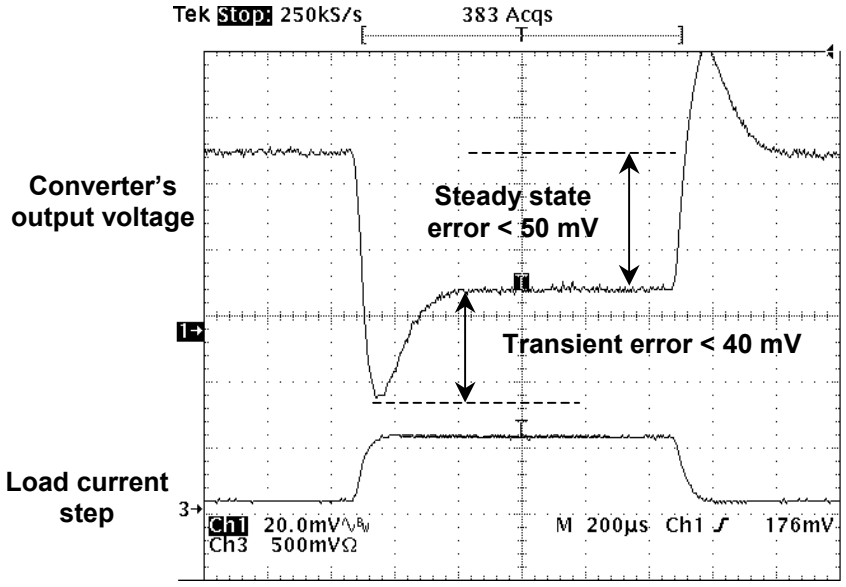


Figure 4.14. Prototype buck-boost converter's response to a 0 to 0.5 A step-change in load current.

Table 4.2. Experimental results of the prototype buck-boost converter.

Specifications	Target	Experimental
Input voltage	2.5-3.2 V	2.4-3.4 V
Output voltage	0.4-4.0 V	0.4-4.0 V
Output voltage accuracy	-	0.5-3 %
Peak-to-peak ripple	≤ 100 mV	≤ 275 mV
Line regulation (Range: 2.4-3.4 V)	-	≤ 0.3 %
Load regulation (Range: 0.05-0.6 A)	-	≤ -1.0 %
Efficiency	-	10-62 %
Worst case response to reference signal	≤ 300 µsec	300 µsec
Response to load step change	≤ 300 µsec	200 µsec

4.4 Experimental Results – Prototype CDMA PA System

The prototype PA system was tested with a CDMA IS-95 signal, for a center frequency of 915 MHz and a 1.23 MHz base-band signal bandwidth. Figure 4.15 shows the measured RF output spectrum of the PA with a dynamically adaptive supply voltage and bias current delivering a channel power of 25.8 dBm at the spectrum analyzer input. The power loss in the connector from the PA output to the spectrum analyzer output was measured to be 1.2 dB, which implies the actual PA output power of 27 dBm.

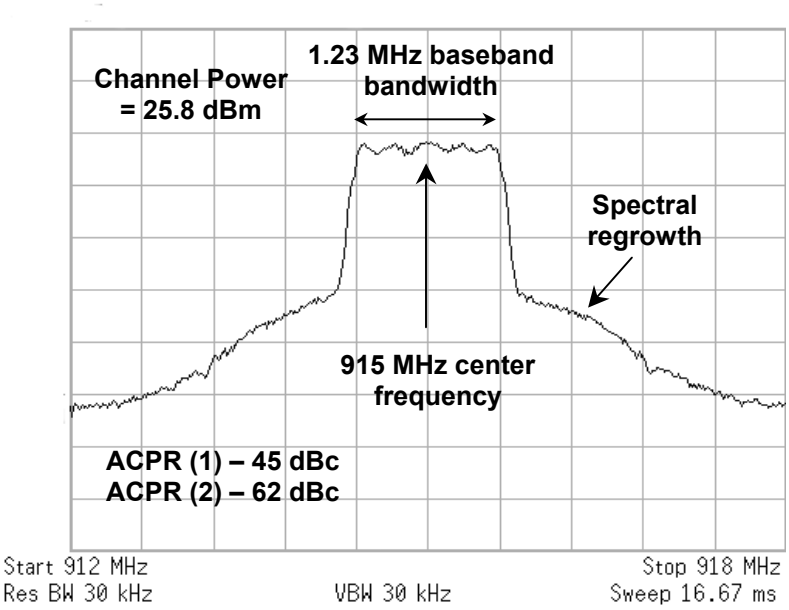


Figure 4.15. Measured output spectrum of the RF PA showing channel power in a 1.23 MHz bandwidth with a 915 MHz center frequency.

Out-of-band linearity of the PA in CDMA applications is measured by adjacent channel power rejection (ACPR), which is defined as the ratio of power in a specified bandwidth at an offset from the center frequency to the channel power. In the CDMA IS-95 standard, the first ACPR is measured as the ratio of the power in 30 kHz bandwidth at an offset of 885 kHz from the center frequency to the power in 1.23 MHz channel bandwidth. Similarly, the second ACPR is measured as the ratio of the power in 30 kHz

BW at an offset of 1.98 MHz from the center frequency to the channel power. Variations of the first and second ACPR for the PA using fixed and dynamic supplies are presented in Figure 4.16, which shows that out-of-band linearity of the PA is not significantly degraded with the dynamic supply. The first and second ACPR values at the peak output power are less than –44 dBc and –60 dBc, respectively, and remains within the specification limits throughout the output power range, thereby satisfying the CDMA IS-95 requirements. The degradation of ACPR values at low power is attributed to the noise floor of the measurement system.

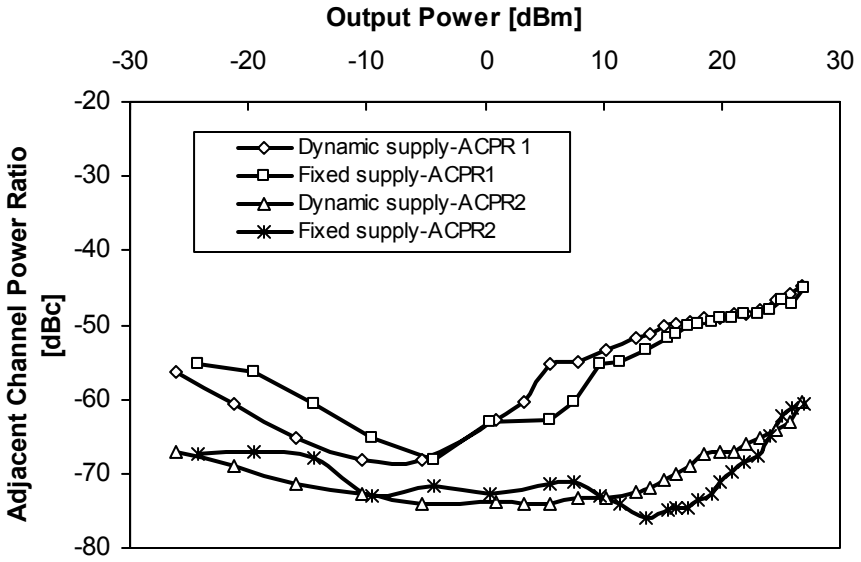


Figure 4.16. First and second ACPR comparison of the dynamic- and fixed-supply PA.

The gain characteristics of the dynamic- and fixed-supply PAs are presented in Figure 4.17. At lower output power levels, the dynamic-supply PA shows a smaller gain because of the lower drain bias current and consequently decrease in the transistor's transconductance, which is consistent with the measured S_{21} parameters of the PA presented in Chapter 2. In a practical system environment, the gain of the last stage of the PA can be calibrated with the driver stages and the variable gain amplifiers to achieve the necessary dynamic range of the transmitter output power.

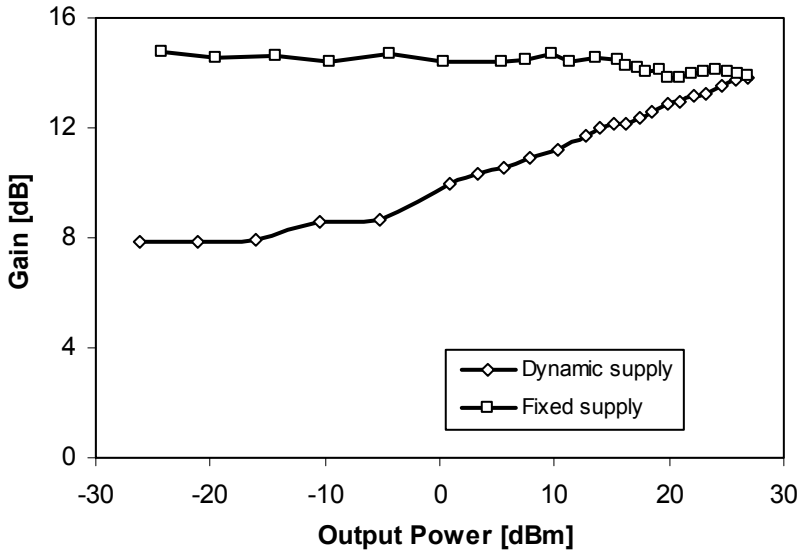


Figure 4.17. Gain comparison of the dynamic- and fixed-supply PA.

Modulation accuracy of digitally modulated signals, e.g., CDMA, is expressed using error vector magnitude (EVM), which is the scalar distance between the ideal reference signal and the measured signal. Since the converter used in the prototype system has a switching frequency of 500 kHz, the switching ripple falls within the transmitting channel bandwidth of 1.25 MHz around the carrier center frequency. To investigate the effect of switching power supply ripple on the in-band linearity of the prototype PA, EVM of the RF output signal was measured at various power levels. The EVM measurement plot and the output signal constellation of the dynamically adaptive PA system at its maximum output power is shown in Figure 4.18, highlighting a maximum overall rms error of 5.8 %. The overall EVM numbers obtained for the dynamic supply PA along with the fixed supply PA and a commercial CDMA PA (MAX2264) for different output power levels are shown in Figure 4.19, which imply that the ripple in the PA's power supply marginally degrades the EVM but remains within an absolute value of 6 %. At peak output power, although the output ripple of the converter increases due to a higher load current, its effect on EVM is slightly greater than the fixed supply PA, but well below the commercial CDMA PA.

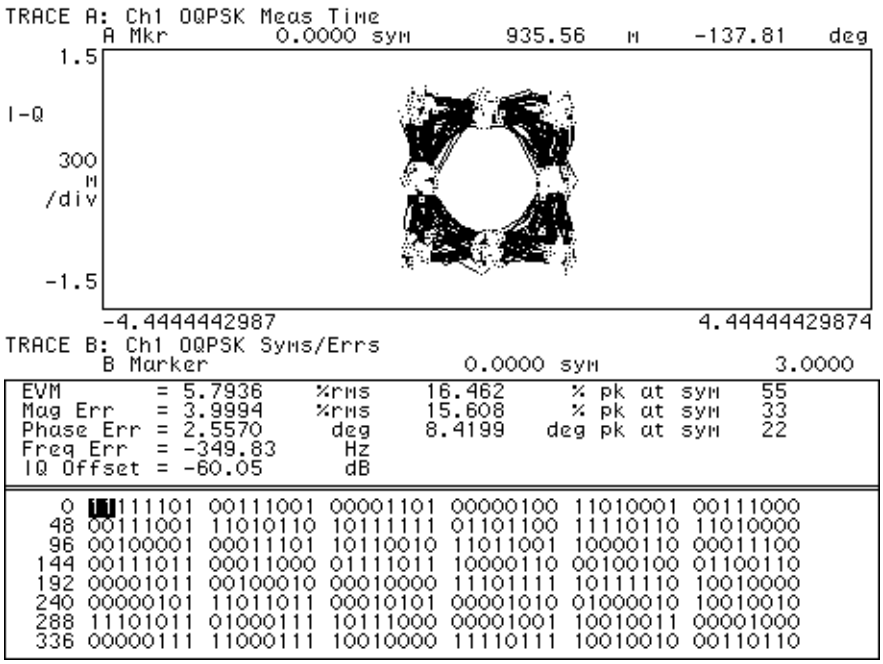


Figure 4.18. Measured error vector magnitude and constellation of the OQPSK CDMA signal at the maximum PA output power of 27 dBm.

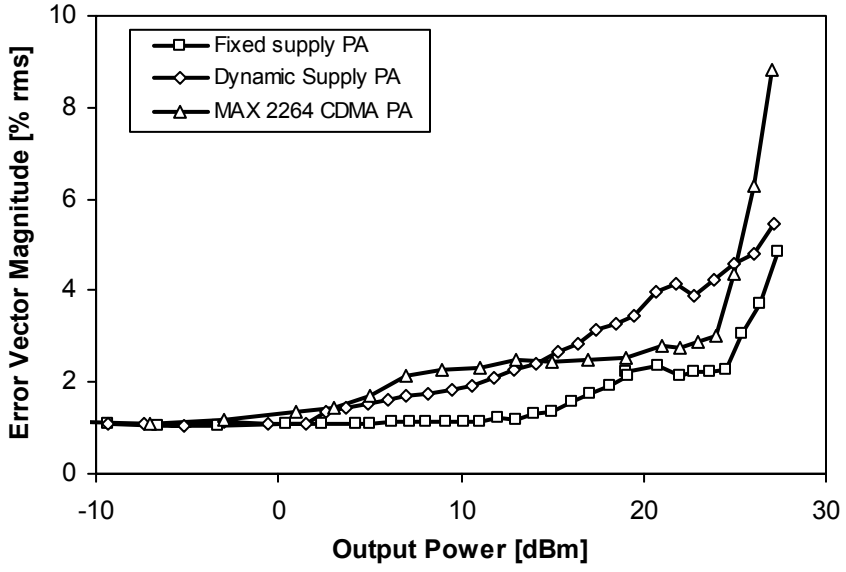


Figure 4.19. Error vector magnitude (EVM) results comparison of the dynamic- and fixed-supply PA.

To verify the dynamic response capabilities of the system for CDMA IS-95 specifications (transmit power is adjusted by 1 dB every 1.2 msec, as requested by the base station), a step stimulus was applied to the converters' control to adjust the PA's supply from 2.95 V(output power of 26 dBm) to 3.6 V (output power of 27 dBm). From the experimental results shown in Figure 4.20 it is seen that the converter responds to the worst-case power adjustment within 5% of its target value in less than 200 μsec. Although the calculated 1-dB step is for a change from 3.2 to 3.6 V, a higher step was chosen to ensure that the converter is guaranteed to respond, as per requirement, well within the specified time limit. The ACPR and EVM performance of the dynamic supply PA during the transient period was not possible to quantify because these tests are performed at a given power, which is adjusted manually from a RF source. Transmitter level system specification, e.g., bit error rate (BER), may be used to gauge the performance of the PA during the transient step-change, which requires a complete system level-investigation.

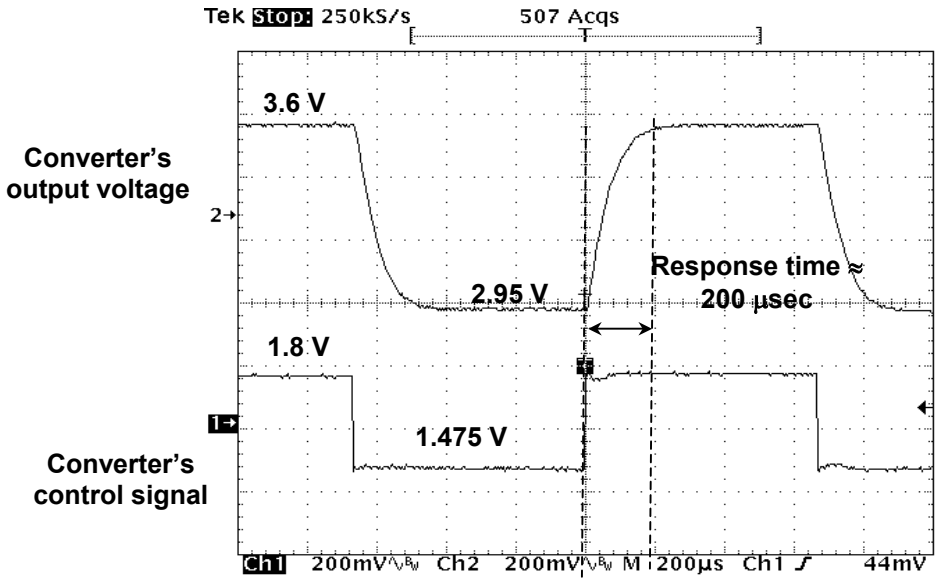


Figure 4.20. Dynamic converter's response to a worst-case power adjustment from 26 to 27 dBm with a corresponding change in its output voltage from 2.95 to 3.6 V.

Drain efficiency, which is the ratio of RF output power to the input supply power, is the measure of the PA's ability to convert battery power into usable RF power at the transmitter antenna. Therefore, all the discussions offered in this section are with respect to drain efficiency. Efficiency curves for the power amplifier with fixed and dynamic supplies are illustrated in Figure 4.21, which shows that the PA with the dynamically adaptive supply exhibits higher efficiency at back-off power.

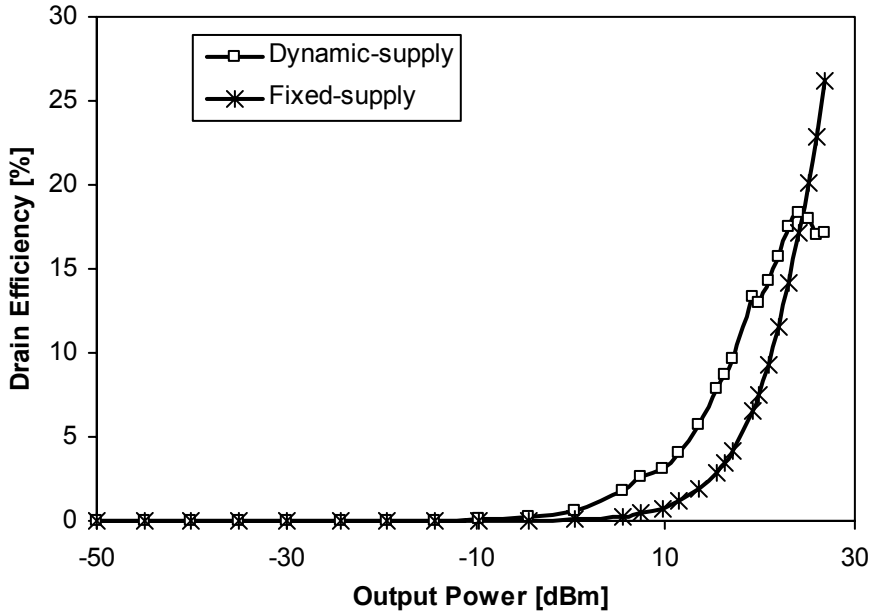


Figure 4.21. Drain efficiency comparison of the fixed- and dynamic-supply PAs.

In the low output power range (i.e., less than –10 dBm), the efficiency curves (in Figures 4.21 are not distinguishable, because the overall system efficiency degrades to very small values. However, while the input supply power for the fixed-supply PA remains constant at lower output power, the dynamic-supply PA tracks the input RF power to adjust both the voltage and current, resulting in reduced input supply power. Figure 4.22 shows the input supply power plots of the fixed- and dynamic-supply PAs.

To estimate the battery life improvement, input supply power is multiplied with probability density function (PDF) of the output power as described earlier in Chapter 1 to generate the weighted input supply power curves. Consequently, the weighted input

supply power profiles for both fixed- and dynamic-supply PAs are shown in Figure 4.23. Clearly, the average input supply power, which is equal to the area under the weighted input power curve, for the dynamic-supply PA is significantly lower than that of the fixed-supply PA for same average output power. The weighted average efficiency of the dynamic-supply PA [calculated using Equation 1.3] is *4.43 times greater* than the fixed-supply scheme, which translates into a battery life improvement depending on the percentage of transmitter power consumed by the PA stage.

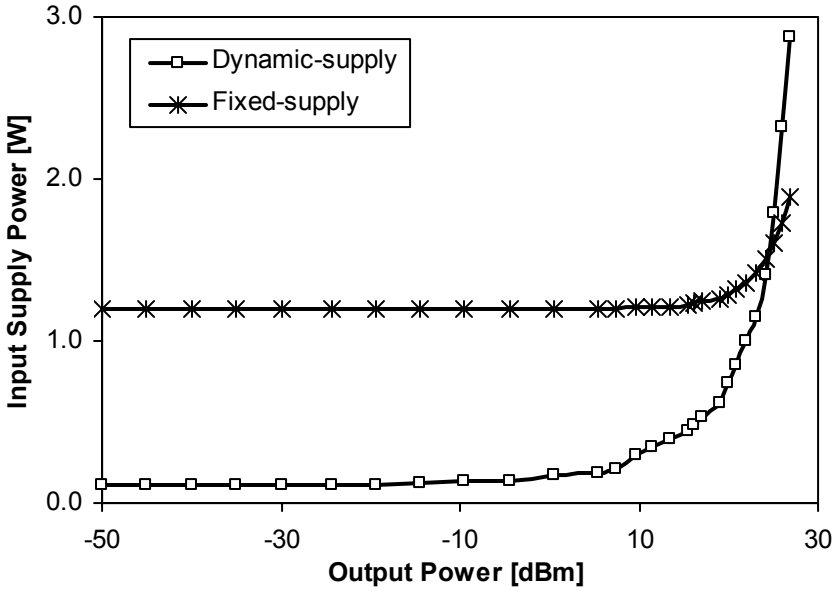


Figure 4.22. Input power comparison of the dynamic- and fixed-supply PAs.

This average efficiency enhancement of the dynamic-supply PA with respect to fixed-supply PA is compared with other results reported in the literature in Table 4.3. The proposed prototype system in this work delivers comparable performance with respect to the other systems, but it also operates at peak system performance with a close-to fully discharged battery, not to mention its inherent improved battery life performance. Since the buck-boost converter supplied LDMOS PA operates with a lower supply voltage and current than the boost converter supplied GaAs MESFET PA [45] under light loading conditions, a higher average efficiency is achieved. On the other hand, the converter used

in the prototype, which was designed for functionality and not optimized for efficiency, showed an efficiency of 10 – 65 % over 0.4 to 4 V output, compared to the high efficiency buck converter used in [51], resulted in a lower average efficiency of the prototype system.

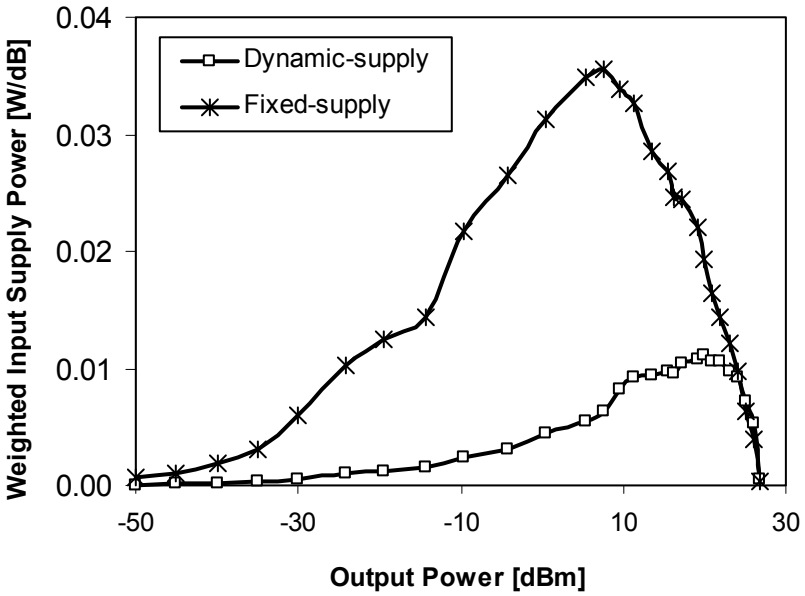


Figure 4.23. Weighted input power comparison of the dynamic- and fixed-supply PAs.

Table 4.3. Comparison of the proposed and reported efficiency enhancement schemes.

Scheme	Fixed supply PA efficiency	Dynamic supply PA efficiency
Buck converter supplied AlGaAs/InGaAs MESFET PA [51]	2.2 %	11.2 %
Boost converter supplied GaAs MESFET PA [45]*	3.89 %	6.38 %
Buck-boost converter supplied LDMOS PA [80]	**1.53 %**	**6.78 %**

* Output power probability distribution profile used in [45] is not the same.

Further improvement in the system efficiency can be obtained by using a buck-boost converter with high efficiency over wide loading range. At the same time, the overall system efficiency can also be improved by using a PA with higher peak-power efficiency of the PA, irrespective of its type (e.g., GaAs HBT/MESFET, SiGe HBT, etc.). A PA with higher peak-power efficiency can be operated with higher efficiency over its loading range with a dynamic supply scheme, thereby improving overall system efficiency.

4.5 Summary

A 27-dBm linear prototype PA for CDMA signals with a dynamically adaptive buck-boost converter supply using an LDMOS transistor is presented. A prototype buck-boost converter is described whose output voltage is dynamically adjustable (on the fly) from 0.4 to 4.0 V, while supplying a load current up to 0.65 A from an input supply of 2.4–3.4 V. The worst-case response times of the converter itself for a 0.4 to 4 V step and a load-current step of 0 to 0.5 A are less than 300 and 200 μsec, respectively, yielding only an output transient error voltage of 40 mV. The maximum measured output error voltage error and peak-to-peak ripple are 2.8 % and 275 mV, respectively. The measured ripple is higher than the desired ripple because of the output capacitor used in the prototype has a higher ESR than the estimated value. The prototype converter was designed for its functionality and not optimized for efficiency. The converter's efficiency can be improved by using power transistors with lower on-resistance values.

The prototype PA system with a dynamically adaptive buck-boost converter and bias control circuit showed an average efficiency improvement of *4.43 times* in system compared to a class-AB PA with fixed-supply voltage, while maintaining the linearity (ACPR) requirements of CDMA IS-95 specifications. Due the power supply ripple voltage in the dynamic-supply PA, its overall error vector magnitude (EVM) degrades marginally over the EVM of a fixed-supply PA. The dynamically adaptive buck-boost converter's response to a worst-case power adjustment of 1 dB in 1.25 msec is within 200 μsec, which means the converter can adjust the supply voltage of the PA dynamically. The transient power level change capability of the system and its effect on the PA

performance was not tested in this implementation, since it requires a complete transmitter level test set-up with a closed-loop power control scheme. With the increased demand for high efficiency RF PAs in portable wireless applications, dynamically adaptive, buck-boost converter supplied PA play a pivotal role in maintaining peak performance, irrespective of the battery condition, while maximizing battery life. The next chapter discusses a high performance buck-boost converter, especially high efficiency over wide loading conditions and lower quiescent current in standby mode, with which the average efficiency of the PA can be further improved.

CHAPTER V

HIGH PERFORMANCE, BUCK-BOOST ADAPTIVE SUPPLY

The performance of the dynamically adaptive buck-boost power supply presented in Chapter III and its prototype experimental results presented in Chapter IV is improved by including several features, which are described in this chapter. The converter's power efficiency is increased by using a modified control scheme such that the converter can transition from and to buck, buck-boost, and boost mode *on-the-fly*, depending on the input battery voltage and required output voltage. While operating in either buck or boost mode the converter eliminates unnecessary switching losses associated with two of its four switches, which would have otherwise incurred power losses in the converter operating only in buck-boost mode for all ranges of input and output voltages.

Switching regulators operating with fixed-frequency, pulse width modulation (PWM) scheme suffer from a low power efficiency under light loading conditions when the converter's switching losses dominate its overall power consumption. Pulse-frequency modulation converter operation, where the converter switching frequency scales with the load current, results in higher light-load efficiency. Therefore, a constant on time, pulse-frequency modulation (PFM) control scheme is considered for low load efficiency enhancement. As the supply voltage varies, the converter's on time is adjusted adaptively to achieve an accurate peak-to-peak ripple voltage, which is critical to minimize spectral regrowth of an RF PA where the converter is used as a dynamic supply. A PFM mode converter with a load dependent switching frequency not only reduces the energy drained from the battery during light-load operation but it also draws

low quiescent current during standby mode because of lower complexity of the control circuit.

To improve converter's power efficiency, adaptive and predictive dead-time control schemes are discussed in this chapter. The applicability of spread-spectrum clocking for reducing the noise in a switching regulator when used as a dynamic supply of a CDMA/WCDMA RF PA system is also discussed. This chapter essentially outlines several performance enhancement techniques and evaluates their suitability as it pertains to the integrated circuit design of a dynamically adaptive power supply system for CDMA/WCDMA mobile handsets with a wide variation in supply voltage.

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5.1 PWM Control with Buck, Buck-Boost, and Boost Mode Operation

5.1.1 Motivation

In a synchronous buck-boost converter, four switches are turned on and off during each switching cycle to generate the regulated output voltage, which can be higher or lower than the input voltage. Any input supply can be transformed into a lower or higher voltage using a step-down or -up converter, respectively, and either scheme requires only two switches to operate in a given switching period. Figure 5.1 presents a graphical representation of the output-to-input voltage ratios of buck, buck-boost, and boost converters with variation in the duty cycle, which shows that an output voltage generated by buck-boost conversion can be accomplished by boost-mode, thereby operating two switches at any given time period. Similarly, an output-to-input voltage ratio of less than unity can be obtained by a buck-mode operation, which also uses two switches as opposed to four in the buck-boost mode. Therefore, switching losses associated with the additional two transistors can be eliminated for all loading conditions except the overlap band, where buck-boost mode operation is necessary. However, the converter must be able to seamlessly transfer from one mode to the other, generating the required output voltage *on-the-fly*, while also supplying the load current.

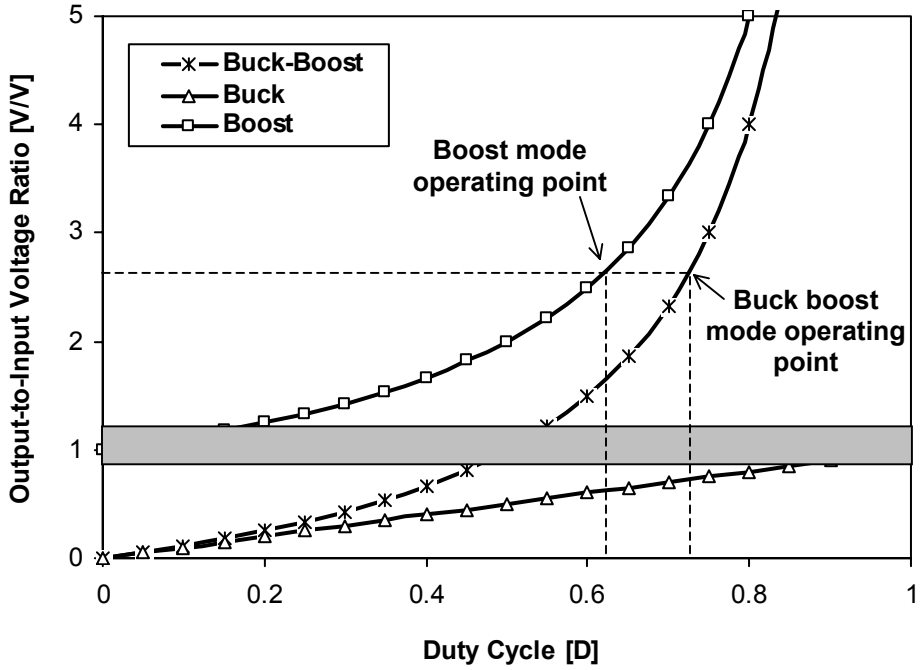


Figure 5.1. Output-to-input voltage ratio in buck/buck-boost/boost mode of operation and their band overlap.

5.1.2 Control Scheme and Operation

Figure 5.2 shows the schematic of the PWM mode buck-boost converter with a control scheme capable of operating the converter in buck, buck-boost, and boost mode. The basic noninverting synchronous buck-boost converter, described earlier in Chapter III, operates with four switches (MP_1, MN_1, MP_2, and MN_2), turning on and off to generate the desired output voltage. For output voltages less than the threshold voltage of a PMOS, transistor MP_2 does not turn on, during which time its body diode conducts and incurs higher power losses. Additional switch MN_3, which along with MP_2 comprises a transmission gate, is specifically added such that the converter operates in a synchronous manner as long as the input supply is at least one NMOS threshold voltage higher than the output voltage. For an interval of the switching period, transistors MP_1 and MN_2 are switched on, thereby storing energy in the inductor's magnetic field. In the other interval, the stored inductor energy is transferred to the output capacitor. By adjusting the switching intervals, an output voltage higher or lower than the input supply is obtained.

Intuitively, any output voltage can be generated using either a buck or a boost converter, which requires only two switches to be operational. In [81], a control method is proposed where an external buck/boost signal is provided to the converter such that the power supply operates in either buck or boost mode. However, this scheme is not suitable for dynamically adaptive systems generating variable output voltages, while transitioning through different modes because of the inherent delay associated with the decision process to transfer the converter from one mode of operation to the other.

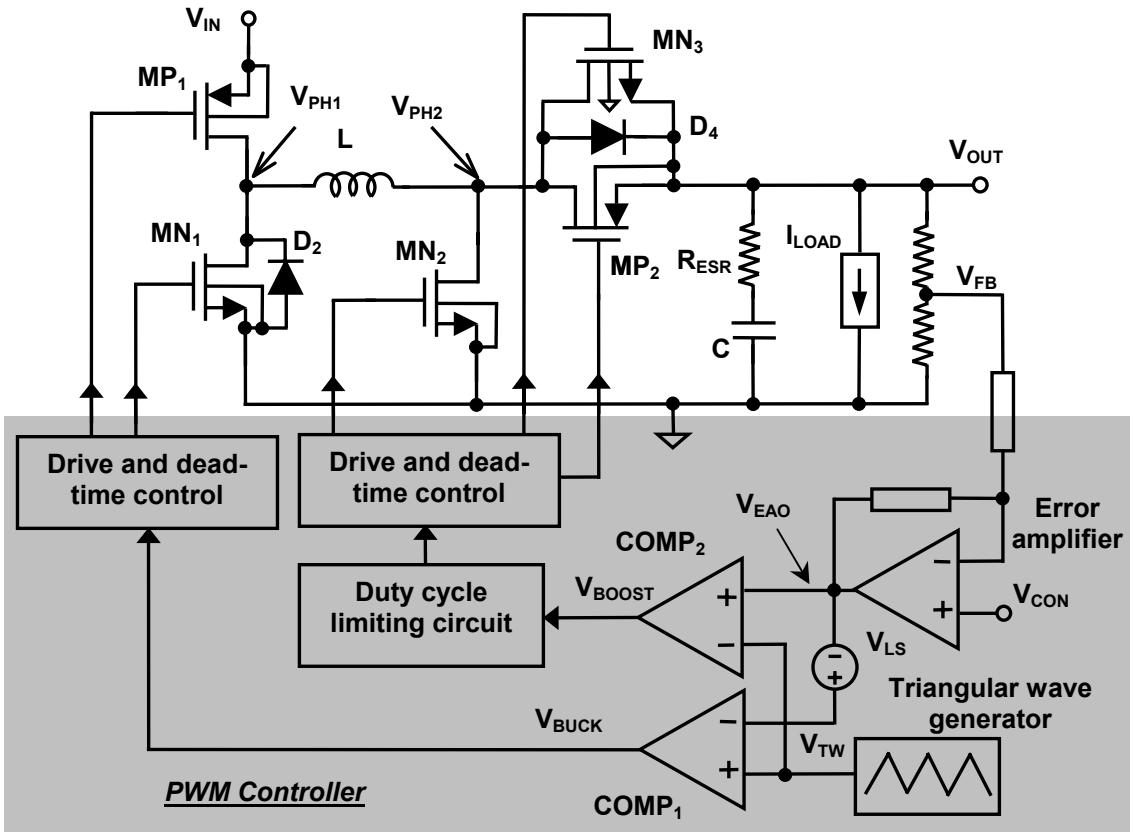


Figure 5.2. Block diagram of the modified buck-boost converter with buck, buck-boost, and boost mode operation.

Modified control schemes described in [82]- [83], are suitable for generating a dynamically adaptive output voltages, the operation of which is as follows. The basic

idea is to control the operation of the power switches based on the error amplifier's output. When the error amplifier's output lies in a certain region of the PWM triangular wave, only buck-stage switches are activated and the inductor is permanently connected to the output node. Similarly, for a higher value of error amplifier's output the boost switches are activated, while the inductor is connected directly to the input supply. In the buck (step-down) mode, switch MN_2 is open while MP_2 and MN_3 are closed. Similarly, for boost operation, MN_1 is open while MP_1 is closed.

The feedback control block in Figure 5.2 shows the functional diagram used to realize the above operation. To adaptively control the transition between buck and boost regions, the error amplifier's output voltage (V_{EAO}) is level-shifted by V_{LS} for comparison with the triangular wave signal (V_{TW}) to control buck switches MP_1 and MN_1. On the other hand, the error amplifier's output voltage (V_{EAO}) is directly compared with V_{TW} to control boost switches MN_2, MN_3, and MP_2. If level-shift voltage V_{LS} is equal to the triangular wave generator's peak-to-peak voltage, the converter operates either in the buck or in the boost region. However, designing the level-shift voltage to be equal to the triangular wave generator's peak-to-peak voltage is not practical in an IC environment because of the process variation and tolerance. Furthermore, the input offset voltage inherently associated with the comparators contribute towards the inaccuracies, even if shift voltage V_{LS} is trimmed to be equal to the triangular wave generator's peak-to-peak output signal. Therefore, an overlap between buck and boost mode is deliberately established to account for any instability that might arise in a situation where the output voltage cannot be generated either in buck or boost mode.

Figure 5.3 offers several key waveforms of the circuit operating in the intermediate buck-boost region, where all the switches of the converter are operational. The total switching period (Ts) is comprised of four subintervals. During interval T_1, MP_1 and MN_2 are turned on and the input voltage is applied across the inductor, yielding a rise in inductor current I_L. In period T_2, switches MP_1, MP_2, and MN_3 are turned on, while MN_2 is switched-off. Inductor current I_L continues to rise; assuming the output voltage V_{OUT} is less than input supply voltage V_{IN}, which would otherwise have a falling slope. In interval T_3, MN_1 is turned on while MP_1 is turned off, allowing the inductor to

freewheel close to ground and have a downward slope in the current. In interval T_4, switches MP_1, MP_2, and MN_3 are turned on resulting in an inductor-current rise with the same slope as that in interval T_2.

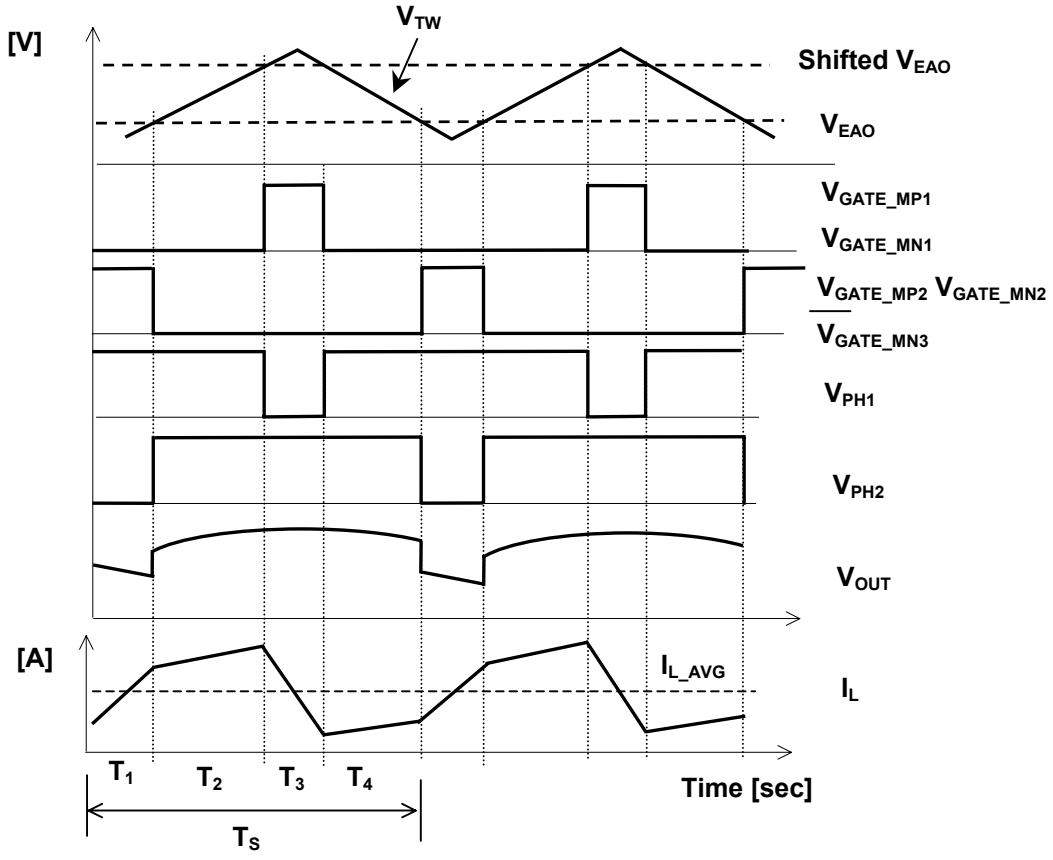


Figure 5.3. Key waveforms of the modified noninverting buck-boost converter operating in buck-boost mode.

The output-to-input transfer function of the converter operating in the buck-boost mode can be derived intuitively using the approach adopted in Section 3.2. With the buck-stage switches operating with a duty cycle D_{BUCK} the node voltage of V_{ph1} is equal to D_{BUCK} times V_{IN}. Similarly, the boost-stage switches operating with a duty cycle of D_{BOOST}, the node voltage of V_{ph2} is equal to 1-D_{BOOST} times V_{OUT}. Under dc conditions, the inductor can be treated as a "short- circuit," thereby V_{ph1} is equal to V_{ph2}. Therefore,

the output-to-input transfer function of the converter operating in the intermediate buck-boost mode is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{D_{BUCK}}{1 - D_{BOOST}}, \tag{5.1}$$

where D_{BUCK} is the duty cycle of the converter's buck stage and is given by

$$D_{BUCK} = \frac{T_1 + T_2 + T_4}{T_S}, \tag{5.2}$$

and D_{BOOST} is the duty cycle of the converter's boost stage given by

$$D_{BOOST} = \frac{T_1}{T_S}. \tag{5.3}$$

When the converter operates in only buck mode, D_{BOOST} is equal to zero, yielding the transfer function for a buck converter. Similarly, when the converter operates only in boost mode, D_{BUCK} is equal to unity yielding the transfer function for a boost converter.

5.2 Implications of Low Supply Voltage

For a given supply voltage, a buck-boost converter cannot generate any arbitrarily high output voltage while supplying a given load current. The on-resistances of power transistors (R_{DS}), the inductor's effective series resistance (R_L), and the load resistance (R_{LOAD}), modeled as the ratio of output voltage and load current in the steady-state (V_{OUT}/I_{LOAD}), set a maximum limiting value of duty cycle beyond which the converter's output voltage decreases even if the duty cycle is increased. Intuitively, beyond this inflection point an increase in duty cycle and subsequent rise in inductor current leads to higher voltage drop across the resistances in the current carrying path. Consequently, a lower volt-sec across the inductor refers to less energy transfer from the

input, to the output resulting in the converter's inability to generate a higher output voltage. A mathematical relationship pertaining to maximum duty cycle consideration is derived in the following text.

Considering the resistance of the inductor and power switches' on resistance, the rise in the inductor current rise for a given duty cycle D in continuous conduction mode is given by

$$\Delta I_L(+) = \left(\frac{V_{IN} - I_L R_L - 2\, I_L R_{DS}}{L} \right) \times D\, T_S, \tag{5.4}$$

and the inductor current fall in the time period $(1-D)T_S$ is given by

$$\Delta I_L(-) = \left(\frac{V_{OUT} + I_L R_L + 2 I_L R_{DS} - V_{IN}}{L} \right) \times (1-D) \times T_S. \tag{5.5}$$

Invoking inductor volt-second balance and equating Equations 5.4 and 5.5, the output voltage of the converter is given by the expression

$$V_{OUT} = \frac{V_{IN} - I_L (R_L + 2R_{DS})}{1-D}. \tag{5.6}$$

Substituting the value of inductor current $I_L = \frac{I_{LOAD}}{1-D} = \frac{V_{OUT}}{R_{LOAD}(1-D)}$, the expression for output voltage can be written as

$$V_{OUT} = \frac{V_{IN}}{(1-D) + K/(1-D)}, \tag{5.7}$$

where K is a non-ideality factor arises due to the finite on resistance of the power devices and inductor resistance given by

$$K = \frac{2R_{DS} + R_L}{R_{LOAD}}, \tag{5.8}$$

which can also be written as

$$K = \frac{I_{LOAD}(2R_{DS} + R_L)}{V_{OUT}}. \tag{5.9}$$

From Equation (5.7), the critical value of duty cycle beyond which the output voltage starts decreasing is determined by

$$K = (1 - D_{CRIT})^2 \Rightarrow D_{CRIT} = 1 - \sqrt{K}, \tag{5.10}$$

yielding a maximum value of output voltage

$$V_{OUT,MAX} = \frac{V_{IN}}{2(1 - D_{CRIT})}. \tag{5.10}$$

The value of K given by Equation (5.9) essentially denotes the fraction of output voltage drop in the power switches' and inductor's resistances if current equal to the load current flows through them. Figure 5.4 shows the output-to-input voltage ratio of the buck-boost converter operating in boost mode with finite switch and inductor resistances. As the resistance value increases, the maximum value of conversion ratio and duty cycle decreases, which is consistent with the explanation of reduced volt-sec transfer offered earlier in this section.

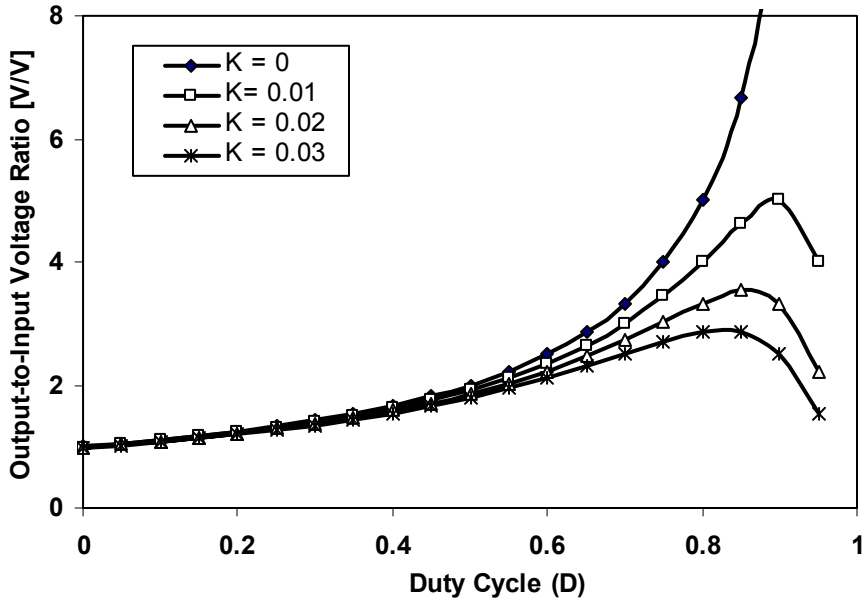


Figure 5.4. Output-to-input voltage ratio of the boost converter with power switches and inductor resistances.

From system design perspective, once the maximum duty cycle is determined, based on the minmum input and maximum output voltages, the power switch-on and series inductor resistance should be kept below the critical value given by Equations 5.8 and 5.9. This problem becomes signficant under a low voltage envirorment, when the converter operates in boost mode, which is when the buck-stage transistor (MP_1) is connected in series with the inductor. When the supply voltage is decreased to a level when it becomes comparable to a PMOS threshold voltage, which is typically higher than NMOS threshold voltage, a significantly larger size switch (may not be practical considering die size and cost limitations) is required, not to mention the lower transconductance of PMOS devices because of lower hole mobility compared to electrons in NMOS devices.

Furthermore, a maximum duty cycle value for the converter must be imposed, which should also be accurately controlled to achieve proper converter operation. Figure 5.5 shows a zoomed version of the output-to-input transfer characteristic, illustrating the existence of two duty cycle values (D_L and D_H) generating a given output voltage from an input supply. These two values exist on either side of the critical (maximum) value of

duty cycle, which means accurate setting of maximum duty cycle is necessary to prevent the converter to reach D_H, instead of operating at D_L. Parameter tolerance due the process variation in integrated circuit environment presents significant challenges in setting up this limit precisely, without any trimming.

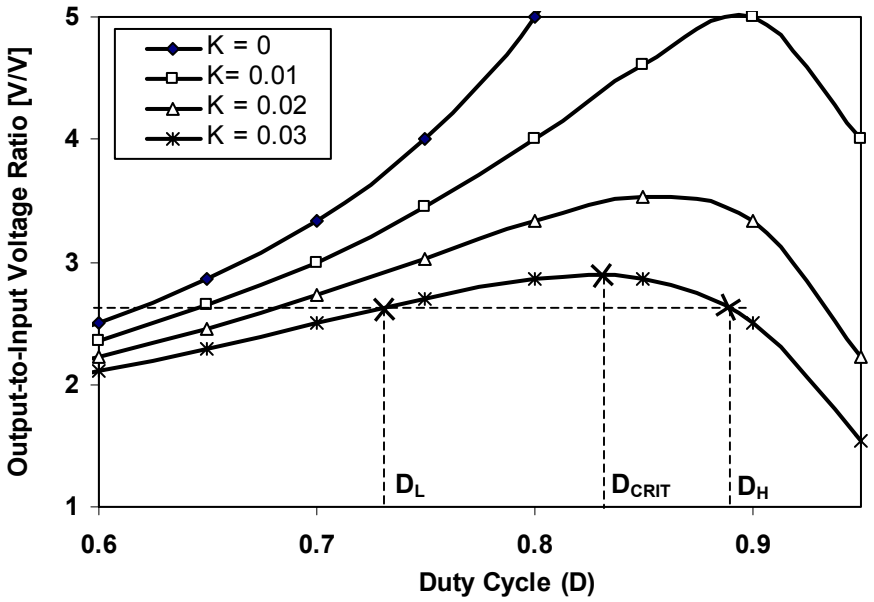


Figure 5.5. Zoomed output-to-input voltage ratio plot of the boost converter in presence of nonidealities illustrating the existence of two operating points for a given voltage conversion ratio.

When the converter operates with the undesired value of duty cycle D_H, instead of D_L, the input (inductor) current increases resulting in a higher powerloss and thereby degraded efficiency. Furthermore, as the converter feedback loop increases the duty cycle from D_H, attempting to generate a higher voltage, the output voltage actually decreases, which would otherwise increase if the converter were operating with a duty cycle D_L. Therefore, precise control of the maximum duty cycle is critical to achieve proper operation. An alternate to accurate duty cycle control is to limit the inductor current to a maximum value, which requires additional overhead and complexity in the form of current-sensing circuitry. The converter operating points D_L and D_H can be differentiated

from each other by their respective inductor current values. A higher duty cycle refers to a higher peak and average inductor current. Therefore, setting a peak inductor current limit corresponding to the critical duty cycle value D_{CRIT}, the converter can be prevented from reaching the prohibited operating state D_H. However, in a low supply voltage environment, the actual values of D_L and D_H can be very close to each other, which essentially superimposes the requirement of a precise peak-current control scheme. In essence, either duty cycle or peak-current control requires accurate control to prevent the converter from reaching the undesired operating point.

5.3 PFM Control with Adaptive On-Time Control

5.3.1 Motivation

The smartening of power management systems in portable applications demand power supplies to maintain high efficiency over loading conditions and consume very little quiescent current, thereby maximizing the utilization of battery energy. While high efficiency during actual loading conditions improves the operation time, a lower quiescent current during no-load operation of the converter improves its standby performance. The actual battery life improvement in such a system depends on the energy savings in both loading conditions and standby operation.

PWM converters, usually designed to achieve high efficiency at full-loads, unfortunately suffer from several drawbacks as their load current is reduced. Their switching losses, because of higher operating frequency, dominate the total power consumption during light loads. Reducing the switching frequency in an attempt to minimize switching losses, however, results in higher ripple currents in the power stage, not only degrading the converter's peak-to-peak ripple but also increasing its conduction losses. Moreover, the converter's switching frequency cannot be arbitrarily scaled down because of the limited current ratings of the power switches, inductor and filter capacitor. Additionally, because of the controller's circuit complexity, its quiescent current consumption is high, which adversely affects its no-load efficiency.

Therefore, the strategy for improving the light load efficiency not only requires a lower switching frequency but also a mode-hopping controller with low quiescent-current

usage. Pulse-frequency modulation (PFM) control with discontinuous conduction mode (DCM) [84] is used to improve the light-load efficiency of power supplies. A plethora of commercial dc-dc controllers [85]- [87] reap the benefits of PFM control during low loads and pulse-width modulation (PWM) control while delivering high power.

In the reported literature, either peak-inductor current [88] or constant on-time control [89], are used to define the on time of a switching regulator. Peak inductor current control requires additional current sensing circuitry, which not only results in additional power losses and lower efficiency, especially during heavy loading conditions, but also increases circuit complexity. Alternatively, a constant on-time scheme eliminates the current sensing, but suffers both steady-state ripple and average output voltage inaccuracies, when operated in a wide supply voltage environment. A constant on time results in a variable peak inductor current, and consequently variable energy transfer from the input to the output in one switching cycle [84], yielding a inaccurate ripple as well as average output voltage. Therefore, an adaptive on-time control is developed in this section where the goal is to equalize the energy transfer from the input to the output, irrespective of the supply voltage variation, thereby maintaining an accurate peak-to-peak ripple and average output voltage.

5.3.2 Operation and Control Scheme

For the PA application considered in this dissertation, the converter's output voltage is maintained at 0.5 V with a load current of approximately 50 mA during low power mode. Therefore, the buck-boost power supply is designed to operate only in buck-mode when operating in PFM, where transistor MN_2 is off while MN_3 and MP_2 are on (Figure 5.2). Accordingly, the schematic of the control loop for PFM control and its key waveforms are shown in Figure 5.6 and 5.7, respectively. During the on-time of the converter, transistor MN_1 is turned on, and the difference of input and output voltages is applied across the inductor, thereby raising its current and storing energy in its magnetic field while supplying the load current and charging the output capacitor. Subsequently, the inductor current is freewheeled to zero through the synchronous switch MN_1, during

which period the stored inductor energy is transferred to the output capacitor. Now both the switches remain off and the output capacitor provides the load current.

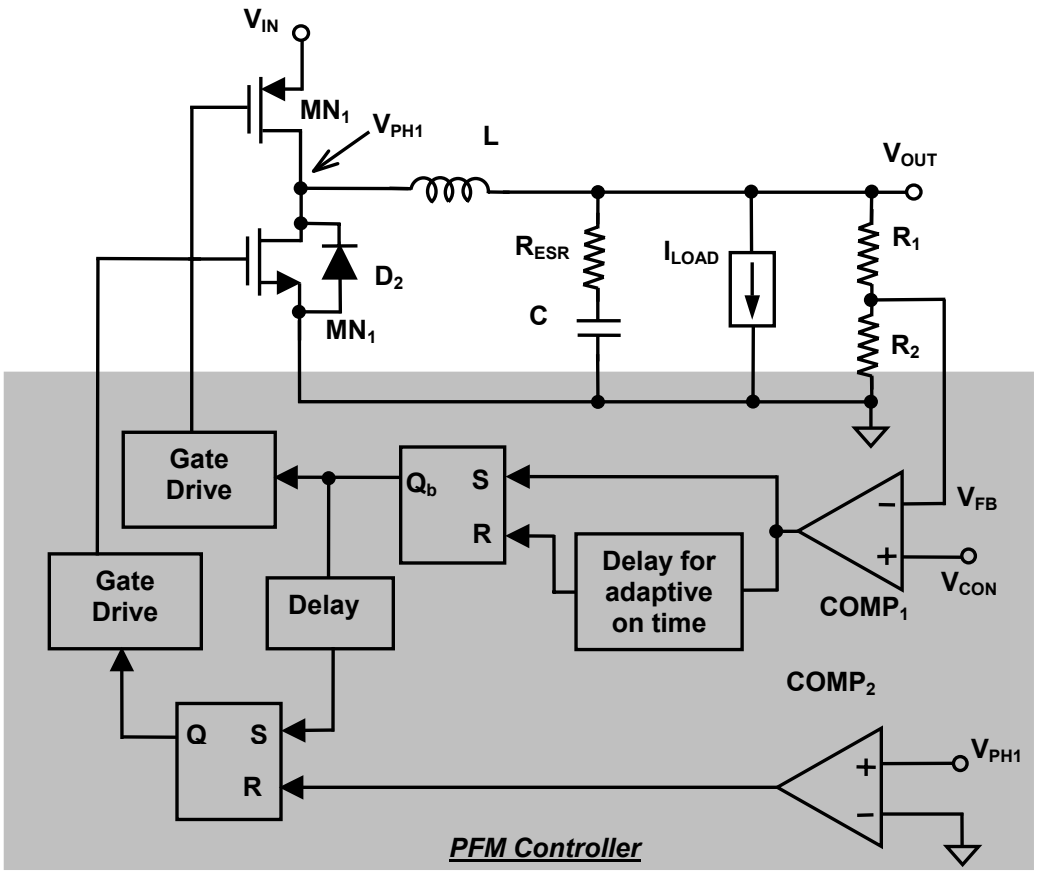


Figure 5.6. Block diagram of the PFM controller with buck operation.

In steady state, when the feedback sense voltage, which is derived from the output voltage by the feedback resistive divider, decreases below the control signal for the converter, the output of $COMP_1$ goes from low to high. The state of the complimentary output Q_b of the D flip-flop changes from high to low, thereby turning on the PMOS transistor M_1. During the on time (T_{PMOS}), inductor current rises up to I_{L_PEAK}, and therefore stores energy in the inductor's magnetic field and charges the output capacitor while providing load current, which is actually much smaller compared to the full load current. After a programmable delay generated internally, resetting of the SR latch

changes the gate-drive signal for transistor MP_1 from low to high, ultimately turning it off.

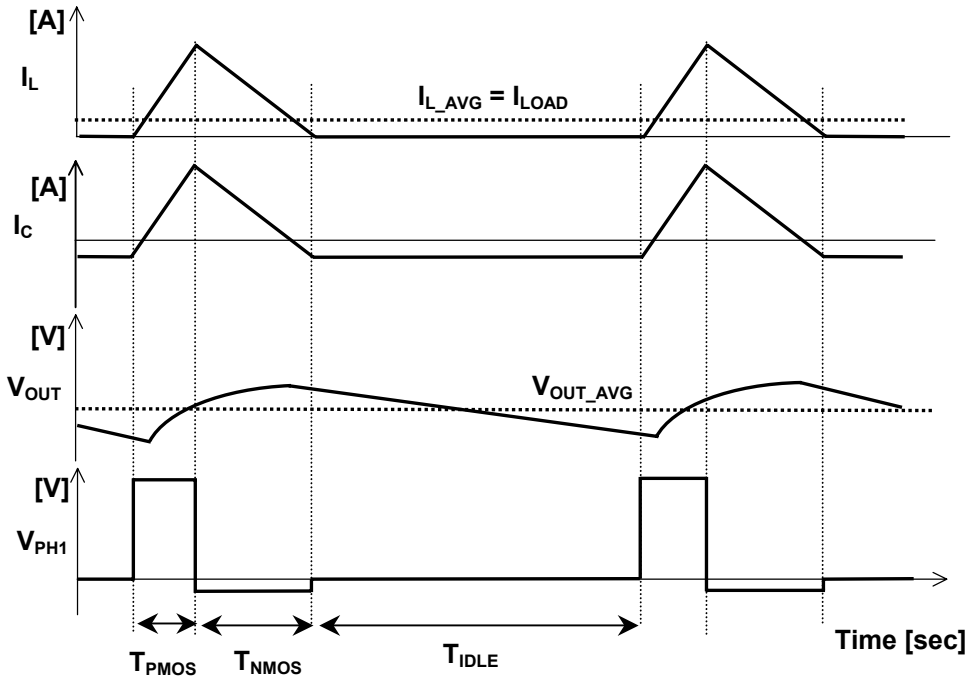


Figure 5.7. Buck-boost converter's PFM mode steady-state waveforms.

An intentional delay between turning off of the buck-stage PMOS pass switch (MP_1) and turning on of the synchronous NMOS device (MN_1) is introduced to avoid "shoot-through" current from the power supply to ground, which constitutes unnecessary power losses. After MP_1 turns off, the output of the second latch traverses from low to high, thereby turning MN_1 on. The inductor current decays during this period freewheeling through MN_1 and combination of the output capacitor and the load. When the current through MN_1 starts flowing in the negative direction the phase node voltage V_{PH1} changes from a negative to a positive value, which is detected by comparator $COMP_2$. The output of $COMP_2$ resets the flip-flop and ultimately switching off MN_1, thereby preventing negative inductor current, consequently avoiding unnecessary power loss and discharging of output capacitor.

During the third interval of a given switching period, both power switches (MP_1 and MN_1) are off and the inductor current is zero. The output capacitor provides the full load current during that period, thereby discharging the capacitor and decreasing the output voltage. The switching cycle repeats when the capacitor terminal voltage is discharged below the desired level, as established by the control signal and the feedback resistor ratio. The load-independent gate drive switching losses are reduced, if not eliminated in the converter. Output regulation is maintained when the energy delivered through the inductor is equal to the energy dissipated by the load.

5.3.3 Design Equations

In this section, the relationship between the on and off time of the converter, energy transferred from input supply to the output load in one switching burst, and resulting output voltage ripple are derived. During time $T_{PMOS,}$ when transistor MN_1 in turned on, the inductor current slews at the rate of

$$\frac{di_L}{dt} = \frac{V_{IN} - V_{OUT}}{L}, \tag{5.11}$$

and eventually reaches its peak value, I_{L_PEAK}, at the conclusion of the PMOS conduction interval. During the NMOS conduction, node V_{PH1} is connected to ground and the energy stored in the inductor is released to the output. The inductor current slews down from I_{L_PEAK} to zero at the rate of

$$\frac{di_L}{dt} = \frac{-V_{OUT}}{L}. \tag{5.12}$$

The device MN_1 is ideally switched off when inductor current reaches zero. At that time node voltage V_{PH1} ring up to output voltage V_{OUT} and the circuit idles with zero inductor current while the output capacitor provides the load current.

The total charge delivered through the inductor in each burst cycle is calculated by integrating the area under the inductor current waveform and is given by

$$Q_L = \frac{1}{2} I_{L\_PEAK} \left(T_{PMOS} + T_{NMOS} \right). \tag{5.13}$$

In the PFM scheme described in this section, the NMOS switching time interval is uncontrolled, but can be related to T_{PMOS} by invoking volt-second balance relationship across the inductor given by

$$T_{NMOS} = \frac{V_{IN} - V_{OUT}}{V_{OUT}} \times T_{PMOS}. \tag{5.14}$$

Therefore, the charge stored in the inductor is expressed as

$$Q_L = \frac{1}{2} \frac{T_{PMOS}^2 \left(V_{IN} - V_{OUT} \right) V_{IN}}{V_{OUT} L}. \tag{5.15}$$

For regulation to be maintained the total charge stored in the inductor must be equal to the charge consumed by the load, which is given by

$$Q_L = I_{OUT} T, \tag{5.16}$$

where T is the sum of three switching intervals (T_{PMOS}, T_{NMOS}, and T_{IDLE}) in PFM operation with discontinuous-conduction mode (DCM).

Since the load current is small during PFM mode operation, the worst-case output voltage ripple is estimated considering the total charge delivered through the inductor is absorbed by the output capacitor, which is given by

$$\Delta V = \frac{Q_L}{C}. \tag{5.17}$$

Therefore, for a given output voltage, the peak inductor current value or MP_1 on time should be chosen carefully such that the ripple voltage requirement is satisfied.

5.3.4 Adaptive On-Time Control

For a given output voltage, a constant on time designed for the high-end of the input supply (4.2 V) results in a lower peak-current and thereby lower stored energy in the inductor when operated with lower-limit of the supply (1.4 V). A lower energy transfer to the output in one cycle essentially results in a higher switching frequency to maintain voltage regulation, which defeats the advantage of using PFM control. Conversely, an on time designed for the lower supply voltage yields a higher peak current when operated at the highest supply voltage, thereby resulting in a larger output voltage ripple.

For a given input voltage (V_{IN}), output voltage (V_{OUT}), inductor (L), capacitor (C), and output ripple (ΔV) combination, using Equations 5.11, 5.15, and 5.17, the peak inductor current I_{L_PEAK} is expressed as

$$I_{L\_PEAK} = \sqrt{\frac{2C\Delta V}{L}\left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)}. \tag{5.18}$$

Unfortunately, in a wide supply voltage environment, a constant on-time control method results in a variable inductor current and output ripple voltage. Therefore, to maintain an accurate ripple voltage, the converter's on time should be adaptively changed with supply voltage, given by

$$T_{ON}(T_{PMOS}) = \sqrt{\frac{2LC\Delta V\, V_{OUT}}{V_{IN}(V_{IN} - V_{OUT})}}. \tag{5.19}$$

Figure 5.8 presents conceptual development of adaptive on time scheme for PFM control and relevant timing diagram. A variable current source depending on the input supply voltage and output voltage is used to charge a capacitor. The capacitor's rising

voltage is compared with a threshold voltage to generate a delay, which is essentially used as the on time for the converter. The higher the supply voltage, the larger is the charging current for the capacitor, which charges it faster resulting in a smaller delay, and vice versa.

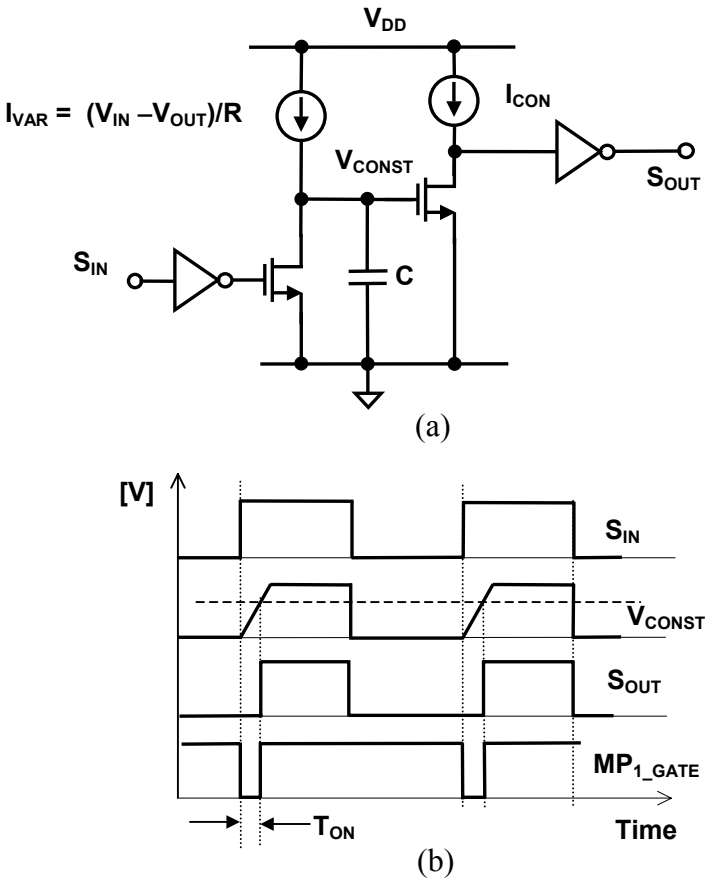


Figure 5.8. (a) Conceptual representation of adaptive on time generation for PFM control, and (b) timing diagram.

The time required for charging a capacitor (T_{CHARGE}) up to a constant voltage (V_{CONST}), using a current source (I_{VAR}) generated by applying to the difference of input and output voltage across a resistor R is given by

$$T_{CHARGE} = \frac{V_{CONST}\, C}{I_{VAR}} = \frac{V_{CONST}\, RC}{V_{IN} - V_{OUT}}. \tag{5.20}$$

To maintain a constant peak inductor current, irrespective of the supply voltage, the required on time of the converter needs to be same as the charging time of the capacitor and is given by

$$T_{ON} = \frac{L\, I_{L\_PEAK}}{V_{IN} - V_{OUT}} = \frac{V_{CONST}\, RC}{V_{IN} - V_{OUT}}. \tag{5.21}$$

Therefore, choosing suitable values of V_{CONST}, R and C, a supply voltage dependant on time for the converter can be generated.

5.3.5 Asynchronous Versus Synchronous Switching in PFM

In PFM control, use of asynchronous and synchronous switching scheme depends on the actual loading, and input and output supply voltage conditions. Figure 5.9 shows the inductor current waveform in synchronous and asynchronous operation under PFM control. While the inductor current rises with the same slope in both modes, it falls at a higher rate in asynchronous mode compared synchronous mode because of the higher voltage drop in the body diode with respect to the synchronous switch resistance. Therefore, the net charge transfer from the input supply to the output capacitor, which is the area under the plots, is lower for asynchronous operation.

Due to the energy lost during body diode conduction, the asynchronous converter needs to switch more often compared to the synchronous converter to maintain its output voltage regulation, thereby incurring more power losses. On the other hand, the additional comparator used in synchronous operation for negative inductor current sensing incurs quiescent power loss. Therefore, for a given load current, if the power loss in the body-diode is higher than the quiescent power loss of the comparator, synchronous operation should be used. Relevant mathematical expressions pertaining to the above explanation are derived in the following text.

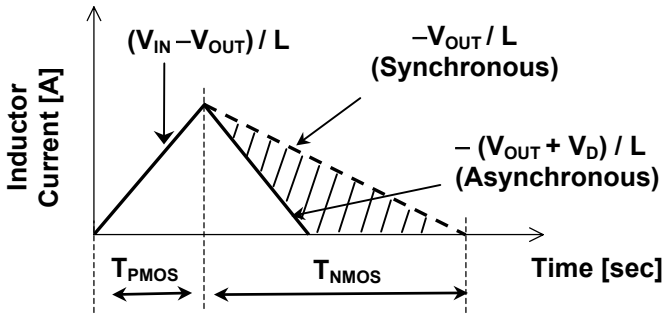


Figure 5.9. Inductor current waveform of one switching cycle with asynchronous and synchronous operation in PFM control.

Assuming the voltage drop across switches is smaller than the body-diode voltage drop, and invoking inductor volt-sec balance, the net energy transferred from the input supply to the capacitor for one cycle in asynchronous switching mode is given by

$$Q_L = \frac{1}{2}\frac{T_{PMOS}^2 (V_{IN} - V_{OUT})(V_{IN} + V_D)}{(V_{OUT} + V_D)L}. \tag{5.22}$$

The charge lost in the body diode (Q_{BD}) during one burst of energy transfer is shown in the shaded area of Figure 5.9 and is equal to the difference of the energy stored in the inductor for synchronous [Equation (5.15)] and asynchronous mode [Equation (5.22)] and is expressed as

$$Q_{BD} = \frac{1}{2}\frac{T_{PMOS}^2 (V_{IN} - V_{OUT})}{V_{OUT} L}\left(1 - \frac{1 + \frac{V_D}{V_{IN}}}{1 + \frac{V_D}{V_{OUT}}}\right). \tag{5.23}$$

The overhead associated with synchronous switching is the quiescent current of the zero inductor current sensing comparator. Consequently, the charge drained from the

supply is the product of quiescent current I_{Q_COMP} and PFM-mode switching period T_S, which is given by

$$Q_{COMP} = I_{Q\_COMP} T_S . \tag{5.24}$$

The limiting criterion for asynchronous and synchronous switching depends on the PFM-mode switching period, which in turn is dependant on the load current. When the power loss due to the comparator exceeds the body diode conduction loss, which depends on the converter's switching frequency, asynchronous switching is preferred. For the same operating conditions, a higher load current refers to a higher switching frequency in PFM mode operation resulting in higher body-diode conduction losses compared to the comparator's quiescent power loss. Therefore, depending on the converter's loading condition, synchronous or asynchronous switching can be used to optimize the power efficiency.

5.4 Advanced Dead-Time Control Schemes

5.4.1. Motivation

In most switching power supplies, the second highest power loss is the body-diode loss of a synchronous rectifier [90]. The disadvantage of fixed dead-time control is the introduction of a delay time margin that is sufficient to prevent potentially catastrophic shoot-through over the entire application, i.e., over supply voltage range, and process and temperature variations. Fixed dead-time control results in a non-optimal solution, since the body diode conduction time can be significantly varied over process, temperature, and devices in an integrated circuit solution. Therefore, alternate schemes e.g., adaptive and predictive dead-time control circuits are considered in this section.

5.4.2. Adaptive Dead-Time Control

The main advantage of adaptive dead-time control is real time turn-on and turn-off delay adjustment of the power switches that changes over temperature and process parameters such that an optimal dead-time is achieved for higher efficiency [90]. This

scheme utilizes the state information of the power switches to control the turn-on and -off of the two gate drivers. Adaptive gate-drive control provides an optimal solution when the controller has access to the actual gate/switch node information, which is possible when the power switches are integrated in the same die as the control circuitry. For high-power applications with external power switches, the available external sense signal is not the same as the actual gate signal responsible for turning the transistor on or off because of the additional delays associated in the signal sense path parasitic inductance and capacitance. Therefore, adaptive dead-time control, when used in a discrete solution, still requires additional delays similar to fixed dead-time control resulting in extra power losses. Unlike the buck-boost converter described in Chapter III, since the modified PWM controller generates two separate signals for buck and boost-stage, their respective synchronous rectifier's gate-drive signals must therefore be derived from the PWM signal. In the following paragraphs, adaptive dead-time schemes suitable for buck- and boost-stage of the buck-boost converter are described.

(a) Buck stage: For the buck-stage power switches, the PWM signal's rising edge controls the turn-off action of MP_1 and its falling edge controls the turn off of MN_1. After MP_1 is turned off, the synchronous rectifier in turned-on after the node voltage V_{PH1} transitions from high to low because of MN_1's body diode conduction. The turning on action of MP_1 is controlled by sensing the actual gate-drive signal of synchronous rectifier MN_1. Figure 5.10 shows the logic-level schematic of the dead-time control circuit for the buck stage. When the PWM signal transitions from low to high, transistor MP_1 is turned-off after a finite time, depending on the gate-drive and signal logic delay. As MP_1 turns-off, the body-diode conducts, pulling down the V_{PH1} node to one diode drop below ground, which enables the logic for the transistor MN_1 to turn on. Transistor MN_1 is turned off when PWM signal transitions from high to low and MP_1's is turned on after MN_1's gate drive signal changes its state from high to low.

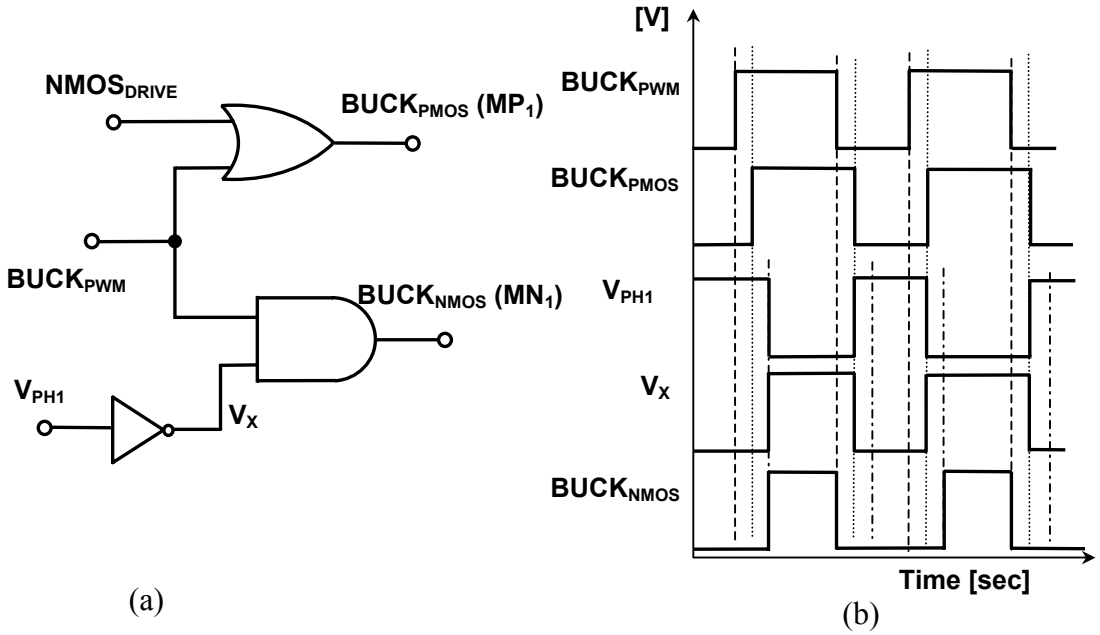


Figure 5.10. (a) Logic-level representation of the adaptive dead-time control circuit for the buck stage of the PWM buck-boost converter and (b) its timing diagram.

(b) Boost stage: For the boost-stage power switches, the PWM signal's rising edge controls the turn-off action of synchronous rectifiers MP_2 and MN_3, while its falling edge controls the turn off of the main switch MN_2. The main switch MN_2 in turned on by sensing the actual gate-drive signal of synchronous rectifier MP_2. The synchronous rectifies in turned on after node voltage V_{PH2} transitions from high to low because of MP_2's body diode conduction. The turning on action of MP_1.Figure 5.11 shows the logic level schematic and time diagram of the dead-time control circuit for the boost stage. When the PWM signal transitions from low to high, transistor MP_2 is turned off after a finite time depending on the gate-drive and signal logic delay, which enables the logic for the transistor MN_2 to turn on. The transistor MN_2 is turned off when PWM signal transitions from high to low and subsequently MP_2 is turned on after MN_2's gate drive signal changes its state from high to low. The switching signal for the transmission gate NMOS transistor MN_3 is complimentary of the logic for MP_2.

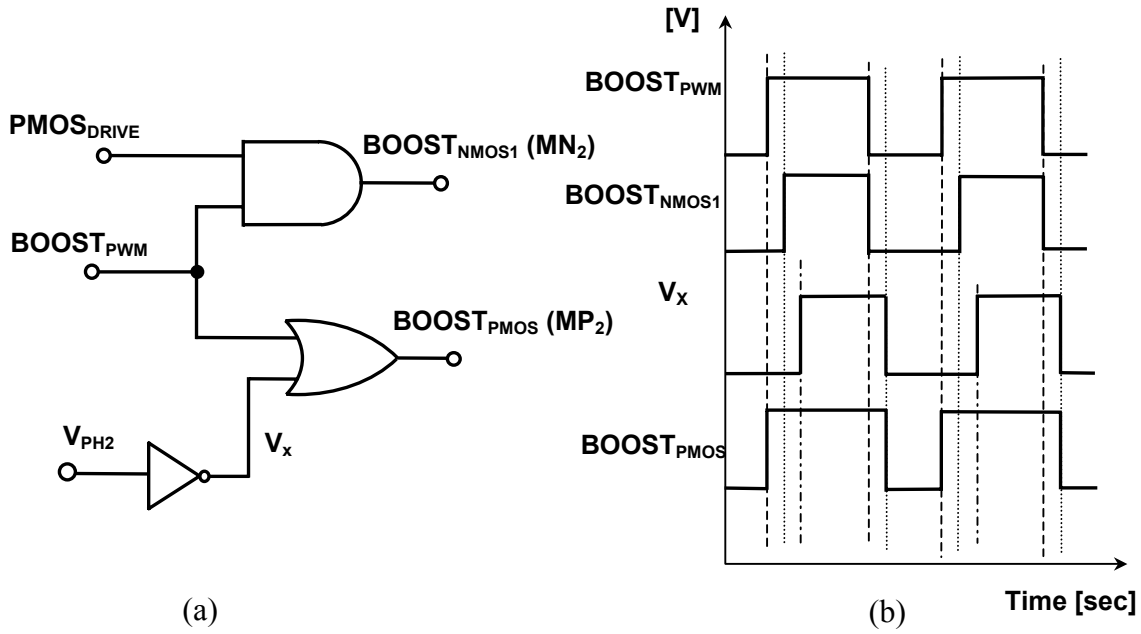


Figure 5.11. (a) Logic-level representation of the dead-time control circuit for the boost stage of the PWM buck-boost converter and (b) its timing diagram.

5.4.3. Predictive Dead-Time Control

In adaptive dead-time control, where current switch states are used to set the delay times, inherent delays associated with the feedback loop path may cause inadvertent body-diode conduction. In predictive dead-time control [90], the dead time is continuously adjusted by a digitally controlled feedback loop based on the information from the previous switching cycle. The benefits of this control technique are especially promising in processor power and multiphase voltage regulator module (VRM) applications. In a portable power management system, since converters operate at their peak power for a small percentage of the total time, additional circuit complexity for predictive dead-time control and use of integrated power switches makes adaptive dead-time control an effective solution because the actual gate signals of the power transistors can be sensed.

5.5 Switching Noise Reduction Using Spread-Spectrum Clocking

Switching noise and electromagnetic interference (EMI) are inherent to the operation of dc-dc converters. However, their effects can be reduced such that it does not create an unwanted interference in the overall system operation. Noise due to the ripple of a switching converter is seen at its switching frequency, as a fundamental tone, and at multiples of the switching frequency, as harmonics. The noise in the power supply of an RF PA in a wireless system contributes to both the in-band and out-of-band distortion components because of this effect, thereby affecting the fidelity of transmitted signal.

The idea behind spread-spectrum clocking is to vary the converter's switching frequency in a pseudo-random manner [88], [91] such that the switching noise and its harmonics spread out into multiple frequencies rather than residing about a single switching frequency and its harmonics as in the case for fixed switching frequency converters. Spreading the noise power into multiple frequencies essentially reduces the peak noise power at a given frequency, thereby improving the overall signal-to-noise ratio. The implication of spreading the switching noise frequency is illustrated in Figure 5.12, where the harmonic suppression with spread spectrum clocking (B) is lower than fixed switching frequency scheme (A).

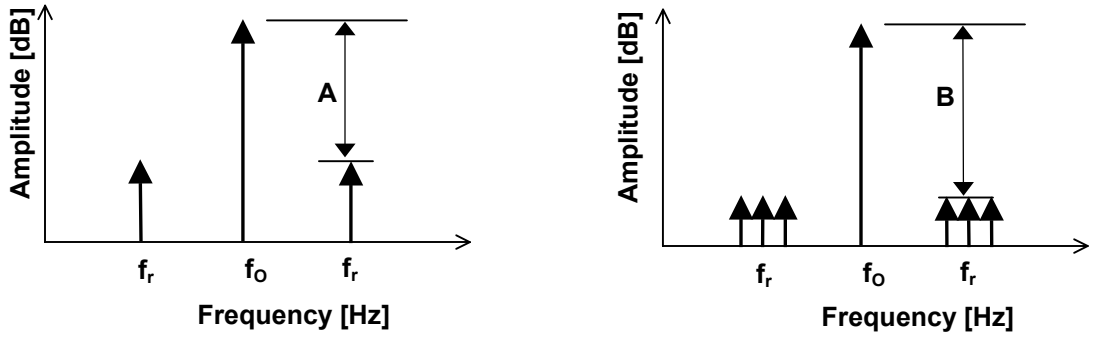


Figure 5.12. Illustration of the single-tone RF PA output: (a) without spread-spectrum clocking, and (b) with spread-spectrum clocking.

Unfortunately, for wideband systems such as CDMA/WCDMA with 1.25/3.84 MHz channel bandwidth the switching ripple has to spread across a wider bandwidth to achieve an improvement in the harmonic suppression and resultant distortion. For instance, a switching frequency of one MHz with +/-10 percent variation would spread the fundamental component of switching noise in a 200 kHz band around one MHz offset from the RF center frequency. The spectral regrowth due to the switching noise would now spread across an additional 200 kHz band inside the 3.84 MHz WCDMA channel bandwidth, which is much smaller compared to single-tone signal amplification. Therefore, in a wideband RF system, the converter's switching frequency needs to be spread across a larger frequency range (comparable to channel bandwidth) to reap the full benefits of pseudo-random switching. To realize such a wide spectrum, the converter needs to operate with a much higher nominal switching frequency, which results in higher switching losses and consequently degraded power efficiency.

5.6 Summary

This chapter describes a high performance buck-boost converter with buck, buck-boost, and boost mode operation to eliminate unnecessary switching losses. For a low supply voltage environment, in the high duty cycle operation region, a given output voltage can be generated by operating the converter in two duty cycles. Therefore, accurate control of maximum value of duty cycle is required to prevent the converter reaching from the undesired duty cycle state, thereby achieve proper operation of the converter. For light-loading conditions, the buck-boost supply can be operated in a adaptive on-time PFM control to maintain accurate peak-to-peak ripple while minimizing power losses with a lower switching frequency and quiescent current compared to fixed-frequency PWM control. Adaptive dead-time controls are suitable for maintaining optimal dead-time in an integrated circuit solution over process, temperature variation, since the actual gate node signals of the power switches are sensed and feedback to control the dead-times. An analysis of spread-spectrum clocking as a noise reduction scheme reveals its applicability for low bandwidth system, e.g., 200 kHz in Global System for Mobile communication (GSM). However, no apparent benefit is seen for

wireless systems with higher channel bandwidth, e.g., 1.23 MHz in CDMA and 3.84 MHz in WCDMA, because of the requirement of spreading the switching frequency over a larger bandwidth. The performance enhancements, i.e., separate buck, buck-boost, and boost PWM mode operation, adaptive on-time PFM control, adaptive dead-time controls, described and developed in this chapter are utilized in the integrated circuit design of the dynamically adaptive RF PA power management system described in the following chapter.

CHAPTER VI

INTEGRATED CIRCUIT DESIGN

Single-cell lithium-ion (Li-ion) batteries (4.2 – 2.7 V) or, alternatively stacked nickel metal hydride (NiMH) and nickel cadmium (NiCd) cells (3.6 – 1.8 V), including state-of-the-art direct methanol fuel cells (DMFCs), offer a source with large variation in its terminal voltage. In a generalized solution, suitable for a variety of power sources, all the control and drive circuitry of the dynamically adaptive regulated supply need to operate at the minimum available input voltage to maximize battery life, i.e., to operate throughout the life of the battery. The major challenges of low voltage operation are achieving the desired input common-mode range (ICMR) and output voltage swing. Typically, amplifiers with complementary input stages are used to achieve a wide ICMR, where both stages are operational at intermediate input common-mode signals and separately for input signal levels close to either the input-supply rail or ground. However, when the input supply is smaller than the sum of the threshold voltages of a PMOS and a NMOS transistor in a CMOS process, both the differential pairs stop functioning when the input common-mode signal sits at an intermediate value because of insufficient source voltages. Furthermore, circuit-design technique, e.g., cascoding for achieving higher dc gain, is prohibited in low voltage environments because of headroom limitations. Appropriate circuit topologies must therefore be developed to meet the design objectives.

The theoretical headroom for low voltage operation is a transistor stack of one diode connected device and one current source/sink device. The voltage drop in a diode-connected device equals to gate-source voltage, which is the sum of threshold voltage

(V_T) and one saturation voltage drop (V_{DS_SAT}). In practice another saturation voltage, is required for the circuit to operate with some ICMR, yielding the minimum supply voltage requirement equal to the sum of V_T and three times of V_{DS_SAT}. For the AMIS 0.5-μm CMOS process (available through MOSIS) used in this design, the PMOS and NMOS devices have threshold voltages of 0.95 V and 0.75 V, respectively. Therefore, all the circuit building blocks are targeted for functionality and performance at a minimum supply of 1.4 V, which is three times the saturation voltage (V_{DS_SAT}) of 150 mV plus PMOS threshold voltage of 0.95 V. The higher limit of the supply voltage is determined by the process technology, 5 V for 0.5-μm. A 4.2 –1.4 V input supply range is selected, which ensures single-cell Li-ion and low-cost two-cell NiCd and NiMH battery operation. Given a process technology with a 0.5 V nominal threshold voltage, the circuit blocks and hence the system can be functional for a supply voltage of as low as 0.95 V, which is close to the requirement of a low-cost single-cell NiCd/NiMH operation.

In this chapter, development, design, relevant simulation, and experimental results of various circuit building blocks of the integrated dynamically adaptive, radio-frequency (RF) power amplifier (PA) power management system is presented. Critical specifications for each circuit block are derived from the system requirements by following a top-down design approach. Based on these derived specifications and technology parameters, suitable topologies are then developed and designed. All the circuit blocks designed are simulated across process technology corners and over a temperature range of –40 to 125^{o} C.

6.1 Linear RF PA Power Management System

6.1.1. The System

The schematic of the RF PA power management (PMU) unit with a simplified signal processing circuitry in the transmission path is shown in Figure 6.1. The baseband signal processor sends a control signal via a digital-to-analog converter (DAC) to the dynamically adaptive buck-boost power supply, which ultimately adjusts the RF PA's supply voltage. The same control signal is also used to adjust the transistor's bias current with a dynamic bias circuit. In a RF transceiver with inherent power control schemes,

e.g., code-division-multiple-access (CDMA)/wide-band CDMA (WCDMA), the signal processor is updated with the transmitted RF power information via a dedicated control loop. Therefore, is it assumed that a control signal for a given output power can be generated by the processor and DAC. As the PA output power decreases from its peak level, the supply current and bias current are reduced such that the PA meets its desired linearity specifications, thereby minimizing the quiescent power dissipation and ultimately improving battery life.

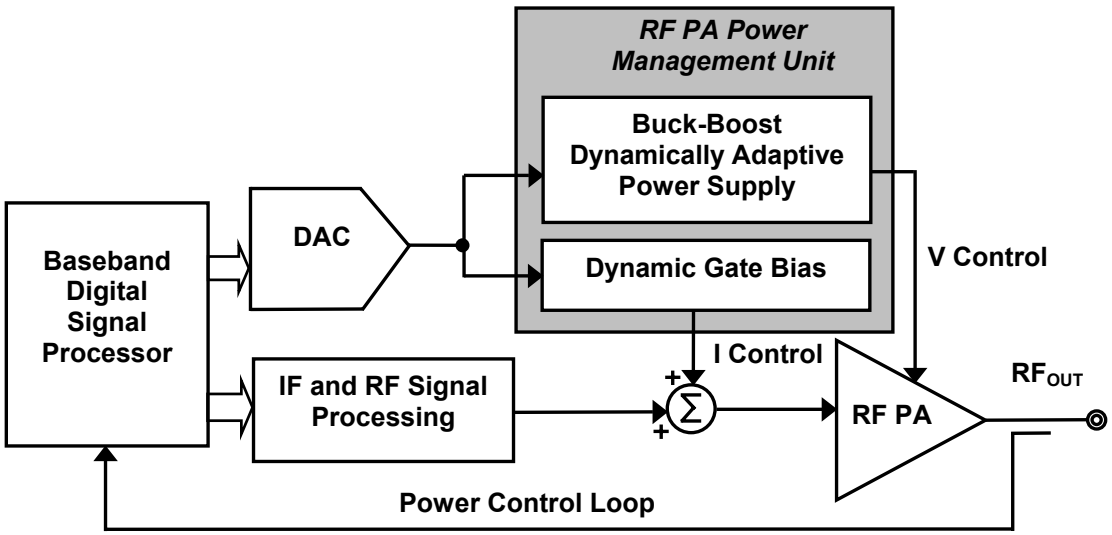


Figure 6.1. Simplified system-level representation of the dynamically adaptive RF PA power management system.

6.1.2 Adaptive Power Supply Design Considerations

The critical design requirements of the converter are: (a) to maintain the desired output voltage accuracy (dc, steady-state ripple, and transient response), (b) to respond to 1-dB control-signal changes, as requested by the base station, and (c) to maximize power efficiency over the entire output voltage and current range. The output ripple in the supply voltage is responsible for both in-band linearity (error vector magnitude- EVM) and out-of-band spectral regrowth (adjacent channel power rejection- ACPR), depending on the switching frequency and baseband bandwidth of the RF signal. On the other hand,

a finite delay in tracking the control signal by the converter's output results in unwanted clipping of the output RF signal, ultimately translating into out-of-band spectral regrowth. The accuracy and transient response trade-offs are critical for the PA system to operate within the in-band and out-of-band linearity specifications required by the wireless standard. The PA specifications and resulting constraints are carefully considered to optimize the dynamic converter's operation, the details of which are offered in the following subsections.

(a) PWM/PFM Operation: Using a simplified model, the output power transmitted to the load is given by ratio of the square of peak output voltage (V^2) to the load resistance (R) seen by the power transistor at its output, where V is the voltage swing of the transistor's drain node. As the output power decreases, the dynamically adaptive system proportionately reduces the output voltage and bias level. A supply voltage range of 5 – 0.5 V translates to an output power variation of 27 – 7 dBm, yielding a power control range of 20 dB, below which the PA supply and bias current are unchanged. Figure 6.2 conceptually illustrates the two regions of operation (i.e., A and B). Therefore, the converter is operated in two separate modes: (a) with high output power capability and fast enough to respond and track 1-dB step changes is the control signal, and (b) with low power capability without the need for fast response (since the output voltage is kept at a constant value).

Pulse-width modulation (PWM) control is suitable for the high power mode because it is both accurate and relatively fast. In PWM mode of a conventional buck-boost converter, all the four switches are functional, which results in unnecessary switching losses. Considering the output voltage requirement of 0.5 – 5.0 V and a Li-ion battery supply of 2.7 – 4.2 V, it is evident that the converter can be operated in either buck or boost mode, where only two of the four switches are functional. The modified converter's detailed operation is described earlier in Chapter 5.

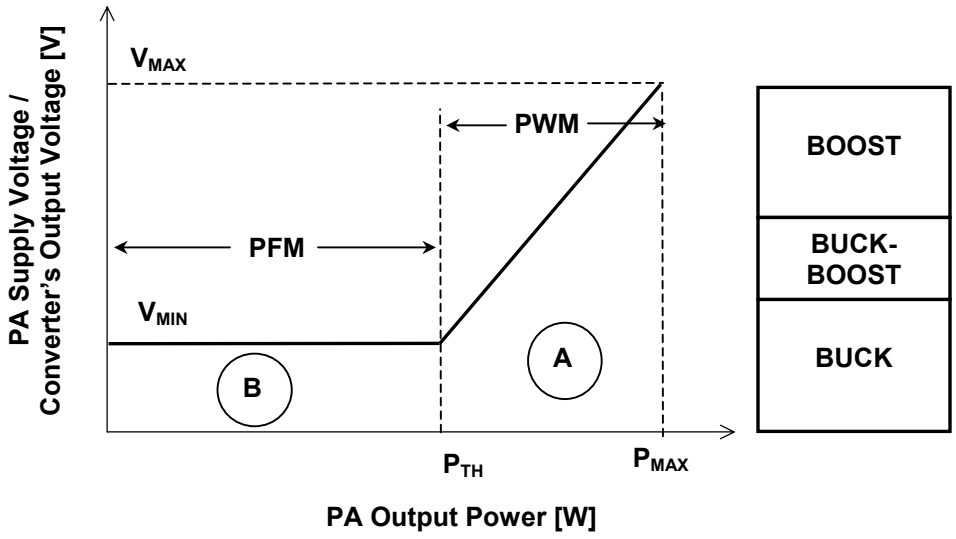


Figure 6.2. Adaptive supply's output voltage profile and illustration of a dual mode (PWM/PFM) converter operation.

A constant on time pulse-frequency modulation (PFM) scheme is adopted for the light load conditions because of its higher efficiency, owing to a lower switching frequency and lower quiescent current flow requirements. The converter can be operated in PWM mode throughout the loading range, but the switching losses incur poor light-load efficiency and consequently shorter battery life. Figure 6.3 shows the schematic of a non-inverting, synchronous buck-boost converter with dual-mode control. The two controllers, voltage-mode PWM and PFM are selected by an enable/disable signal (MODE). While one controller is in operation, all the circuits in the other controller are switched-off to reduce quiescent-current power losses. Signal MODE can either generated by sensing the converter's control signal and a threshold voltage level, or obtained from the signal processor, which tells the converter to switch from one mode the other depending on transmitter's output power level. In this research, it is assumed that an external signal generated by the digital signal processor is available to control the power supply's operation mode.

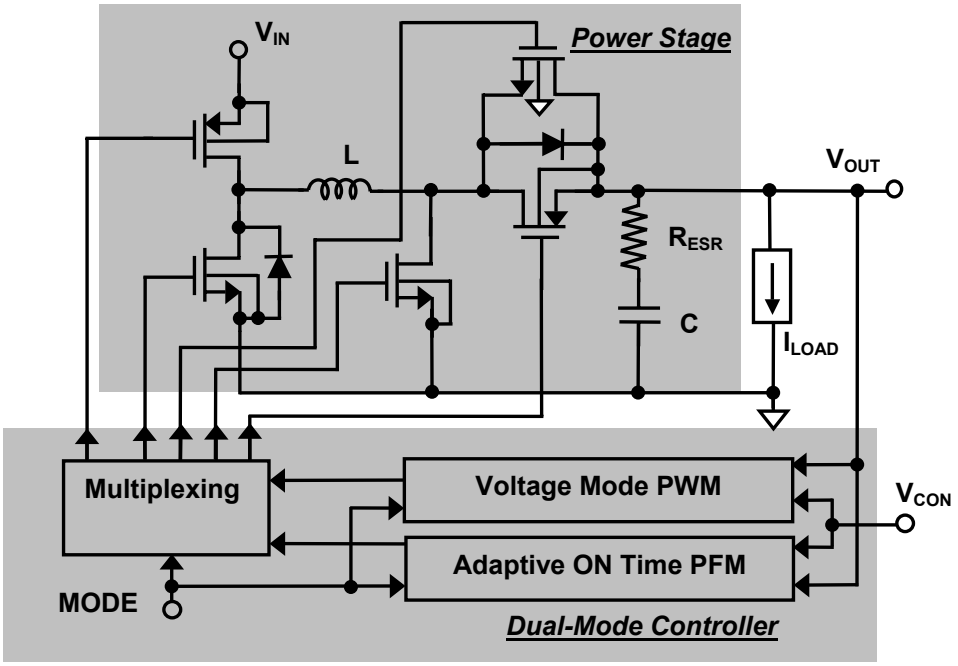


Fig. 6.3. Schematic of the dual-mode, buck-boost converter.

(b) Performance Trade-offs in a Buck-Boost Converter: In a PWM-controlled buck-boost converter operating in the boost mode, the control loop is compensated to achieve a unity-gain bandwidth that is below the right-half plane (RHP) zero, which is inversely proportional to the converter's power inductor value (similar to the description for a buck-boost converter provided in Chapter III). Increasing the converter's bandwidth requires a high frequency RHP zero by choosing a smaller inductor, which increases the ripple current and therefore requires a larger output capacitor to meet the output voltage ripple specification. A larger output capacitor requires more current and therefore energy to be transferred from the input supply to change its terminal voltage from one level to the other, thereby yielding a longer control-to-output transient response time. Moreover, the steady-state output voltage accuracy of the converter is affected by the error amplifier's input offset voltage in the control loop. Since MOS devices' matching is worse than bipolar transistors, in a standard CMOS process, realization of a low offset amplifier requires complex offset cancellation schemes, thereby increasing the complexity of the circuit.

6.1.3 Calibration Requirement and Alternate Control Strategies

Adjustment of the bias current and supply voltage of the PA, however, changes the transistor's transconductance, which results in a variable gain, that is dependant on its output power. In a practical implementation, the PA gain needs to be adjusted with the other components in the signal transmission chain, e.g., drivers and variable gain amplifiers (VGAs) to achieve the desired output power dynamic range. An open-loop approach with a look-up table can be adopted to implement such a system, where, for a given RF output power, its corresponding input power and control signals are stored in the DSP's memory –these are based on the experimentally predetermined gain characteristic of the PA. Along with the VGAs, the PA is dynamically programmed to achieve the transmitter's output power dynamic range. However, like any other open-loops scheme, this architecture suffers from time-dependent performance drifts resulting in accuracy degradation. The accuracy can be improved by incorporating an automatic calibration procedure implemented in a closed-loop feedback manner like, the Cartesian feedback predistortion system [2], where the look-up table parameters are updated during start-up. However, the system complexity is increased due to the additional components used for its adaptation.

Evaluating the circuit complexities, e.g., look-up table based open-loop or closed-loop gain adjustment requirements, steady-state accuracy and transient response trade-offs in a buck-boost converter, control schemes alternate to the continuous tracking of supply voltage and current are considered. One way to operate the PA system is to introduce a systematic offset at the converter's output voltage such that, at any given time, the PA supply voltage is 1-dB higher than the desired voltage level to achieve its specified linearity. Therefore, the transient response requirements of the converter are simplified; however, it still requires a calibration scheme similar to the exact continuous control. Alternatively, a two- or there-step approach is considered where the power management system adjusts the supply voltage and current in discrete steps. These approaches greatly simplify the calibration and transient response requirements of the power converter and associated control circuitry. Figure 6.4 conceptually illustrates these alternate control schemes with respect to the accurate continuous-control method. A

summary of the calibration schemes' complexity along with the dynamic converter's accuracy and control-step transient requirement is offered in Table 6.1. Further discussions on these approximate control schemes with experimental results and their implications on the PA system efficiency are offered in Chapter 7.

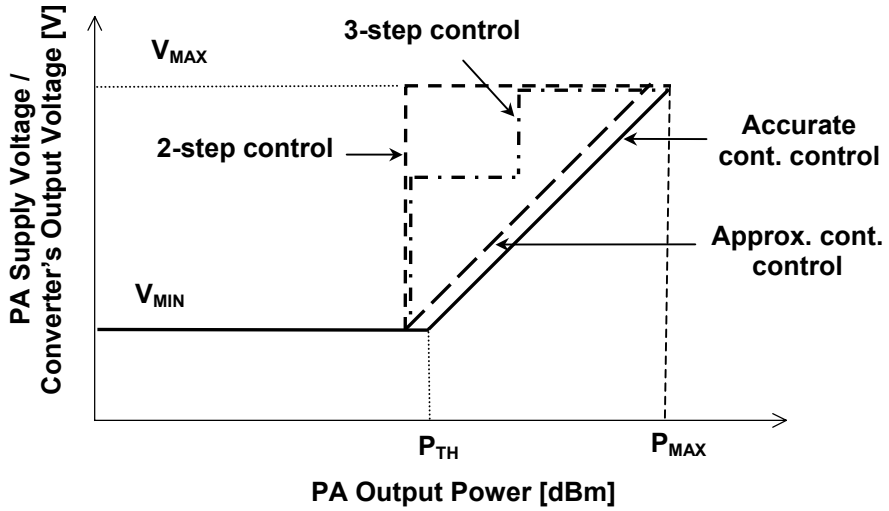


Figure 6.4. PA supply voltage variation profile with transmitter output power for alternate control schemes.

Table 6.1. Gain calibration and dynamic converter's accuracy and transient response requirements for various control schemes.

Scheme	Calibration requirement	Converter's transient response	Converter's output accuracy
Accurate continuous control	Complex	Fast	Accurate
Accurate continuous control	Complex	Fast	Accurate
Approximate continuous control	Complex	Moderate	Moderate
Discrete two-step control	Simple	Moderate	Moderate
Discrete three-step control	Simple	Moderate	Moderate

6.2 Dynamically Adaptive Buck-Boost Supply System Design

6.2.1. System Specifications

A maximum output voltage of 5 V is selected for the integrated buck-boost converter for the dynamically adaptive system developed in this research to be suitable for state-of-the-art PAs fabricated in various processes, e.g., SiGe, LDMOS, GaAs. A maximum load current of 300 mA at the output voltage of 5.0 V, is chosen resulting in converter's power rating of 1.5 W. A minimum output voltage of 0.5 V is selected such that the PA is accurately biased in the saturation region when the RF transmitted power is low.

Peak-to-peak ripple voltages of 100 mV at 5 V output and 20 mV at 0.5 V output are chosen to limit the RF PA output spectral regrowth 40 dB below the channel power level to meet the linearity requirements. Since the effect of supply ripple voltage is dependent on the PA characteristics, the PA must therefore be characterized experimentally or accurately simulated before selecting the ripple performance of its dynamic supply. To simplify the accuracy and transient response requirements, the converter was designed to adaptively adjust the RF PA's voltage level 1-dB higher than the required level (Figure 6.4). Therefore, the converter is specified to respond within 200 μsec of a 1-dB change in the control signal under worst-case operating conditions. For a buck-boost converter operating in boost mode, the worst-case condition occurs when the input supply voltage is at its minimum with maximum output voltage and load current, which yields the RHP-zero. The converter is specified for a bandwidth of 30 kHz under the worst-case operating condition just mentioned. Furthermore, depending on the control-step change the inductor current may slew from its previous value to the required value, thereby transferring the required charge from the input supply to the output capacitor that allows the converter's output to reach its desired regulated output voltage level.

In the PFM mode, the converter is designed for an output voltage of 0.5 – 0.75 V with a maximum ripple voltage of 20 mV over the entire supply voltage range of 1.4 – 4.2 V. Although, the converter is targeted for a load current of 50 – 100 mA during low power mode, it can provide a maximum current of 300 mA. The derived specifications of

the dynamically adaptive buck-boost supply in PWM and PFM mode operation are summarized in Table 6.2.

Table 6.2. Integrated, dynamically adaptive buck-boost supply's specifications in PWM and PFM mode.

Performance	Unit	Target
Input supply voltage	V	1.4 – 4.2
PWM Mode		
Control voltage range	V	0.1 – 1
Output voltage range	V	0.5 – 5
Load current range	A	0.05 – 0.3
Output ripple (peak-to-peak)	mV	≤ 100
Output voltage accuracy	%	5
1- dB control-step response	μsec	≤ 200
Unity gain frequency (maximum duty cycle)	kHz	> 30
Switching frequency	MHz	≈ 1
Efficiency (Peak load)	%	> 90
PFM Mode		
Control voltage range	V	0.1
Output voltage range	V	0.5
Load current range	A	0.05 – 0.1
Output ripple (peak-to-peak)	mV	≤ 20
Output voltage accuracy	%	5
Efficiency	%	> 80

6.2.2. Power Stage Design

(a) Output Filter Inductor and Capacitor Selection: The output inductor in a boost converter is chosen to establish the inductor ripple current. At the same time, a smaller is desired to push the right-half plane (RHP) to a higher frequency. For the minimum input supply (V_{IN_MIN}) of 1.4 V and maximum output voltage (V_{OUT_MAX}) of 5 V with a 0.5 A load current (I_{LOAD}), the converter's maximum duty cycle (D_{MAX}) in boost mode is calculated as 0.77 from the expression given by

$$D_{MAX} = 1 - \frac{V_{IN\_MIN} - 2V_{SW}}{V_{OUT\_MAX} + 2V_{SW}}, \tag{6.1}$$

where V_{SW} is the voltage drop due to the switches' on resistances (assumed to be 100 mV). Assuming a peak-to-peak inductor current ripple (ΔI_L) of 1 A, the minimum value of the inductor is estimated to be 0.97 μH from the following expression

$$L_{MIN} = \frac{(V_{IN\_MIN} - 2V_{SW})D_{MAX}}{f_{SW}\Delta I_L}, \tag{6.2}$$

where f_{SW} is the switching frequency of the converter (nominal value of 1 MHz). Similar buck-boost converter described in Chapter III, the output peak-to-peak ripple voltage (ΔV_O) of the converter in boost mode is given by

$$\Delta V_O = \frac{I_{LOAD\_MAX}D_{MAX}}{f_{SW}C} + I_{PEAK}R_{C\_ESR}, \tag{6.3}$$

where I_{PEAK} is the peak inductor current and R_{C_ESR} is the equivalent series resistance (ESR) of the capacitor. A total ripple voltage of 50 mV is divided between the ESR component (30 mV) and the output capacitor (20 mV) to yield an output capacitor of 20 μF with an estimated ESR of 10 mΩ. Similarly, an input capacitor of 47 μF with an ESR of 5 mΩ is chosen to limit the input supply ripple within 50 mV.

(b) Power Switches Requirements: The design of the power switches in an integrated buck-boost converter is driven by the efficiency and functionality, especially in a low-supply voltage environment. The total resistance of a power switch is due to the device's on resistance, metal interconnect and bond-wire resistances. Typically, the device resistance dominates over the other two. However, for an extremely small device resistance, the metal and bond wire resistances can be a significant part of the overall resistance.

As discussed earlier in Chapter 5, to generate an output of 5 V with load current of 0.5 A from a 1.4 V input supply with a duty cycle of 0.8, the ratio of device resistances and effective load resistance is given by

$$K = \frac{2R_{SW} + R_L}{R_{LOAD}} \leq (1-D)^2 = 0.04. \quad (6.4)$$

With an equivalent load resistance R_{LOAD} (equal to the ratio of output voltage V_{OUT} and load current I_{LOAD}) of 10 Ω and assuming an inductor dc series resistance (R_L) of 100 mΩ, the switch resistance (R_{SW}), which consist of device resistance R_{DS}, metal resistance R_M and bond-wire resistance R_{BW}, the value of R_{SW} is calculated to be less than 150 mΩ. Allocating 50 mΩ to metal and bond wire resistances, the desired device resistance is estimated to be less than 100 mΩ.

6.2.3. PWM Control Loop Design

The PWM mode control scheme is described earlier in Section 5.1. However, for completeness, the control loop schematic consisting of the error amplifier, PWM comparators, and the triangular wave generator is shown in Figure 6.5. During steady-state operation, the negative feedback loop operates in such a way that the positive terminal of the error amplifier is equal to its negative terminal voltage. Therefore, by changing the error amplifier's positive terminal voltage (V_{CON}), the converter's output voltage can be programmed. The error amplifier's output and its level-shifted version are compared with a triangular wave signal to control the boost and buck switches, respectively. The boost comparator's output is further processed for limiting the duty cycle to a maximum value of 0.85 for proper converter operation. Finally, the resultant logic signal is fed to the dead control and drive circuit, ultimately switching the power transistors on and off. The high and low values of the triangular wave are controlled by reference signals generated from a bandgap reference circuit, which is not shown in the schematic for simplicity.

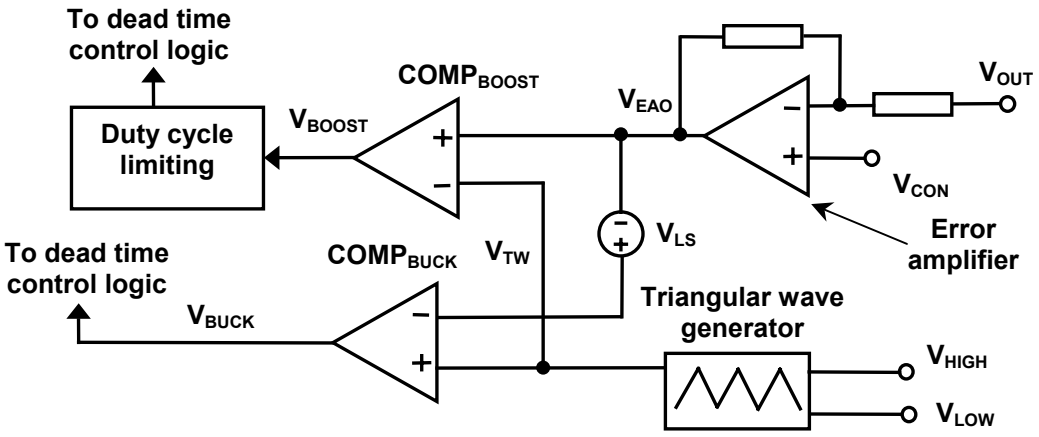


Figure 6.5. Schematic of the voltage-mode PWM controller for the buck-boost converter.

(a) Compensation Network Design: The time-averaged small-signal model of the boost converter [27] is used for designing the compensation network. For the converter to be stable across supply and loading conditions it is compensated for worst-case conditions. For a boost converter, it occurs while generating the maximum output voltage from the minimum input (maximum duty cycle) and providing maximum load current, where the RHP zero caused by the inductor is at the lowest frequency. The compensation network design procedure is described earlier in Section 4.2. For a maximum duty cycle of 0.8 and triangular wave generator's peak-to-peak signal of 300 mV, the uncompensated feedback loop has an open-loop gain of 16.77 dB with complex-conjugate LC filter poles at 7.2 kHz and RHP zero at 64 kHz. A 2-zero and 3-pole, type III network (Figure 6.6) with zeros at the filter pole frequency, one pole at origin and two other poles below the switching frequency of the converter is used to compensate the PWM control loop, yielding a unity-gain frequency of 35 kHz and a phase margin of 30 degrees. Figure 6.7 shows the resulting open-loop gain Bode plot of the converter along with power stage and compensation network.

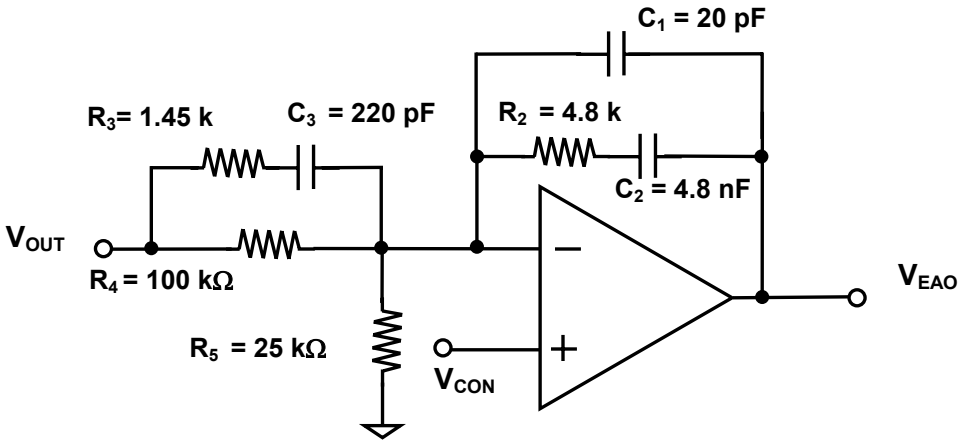


Figure 6.6. Error amplifier with the compensation network component values.

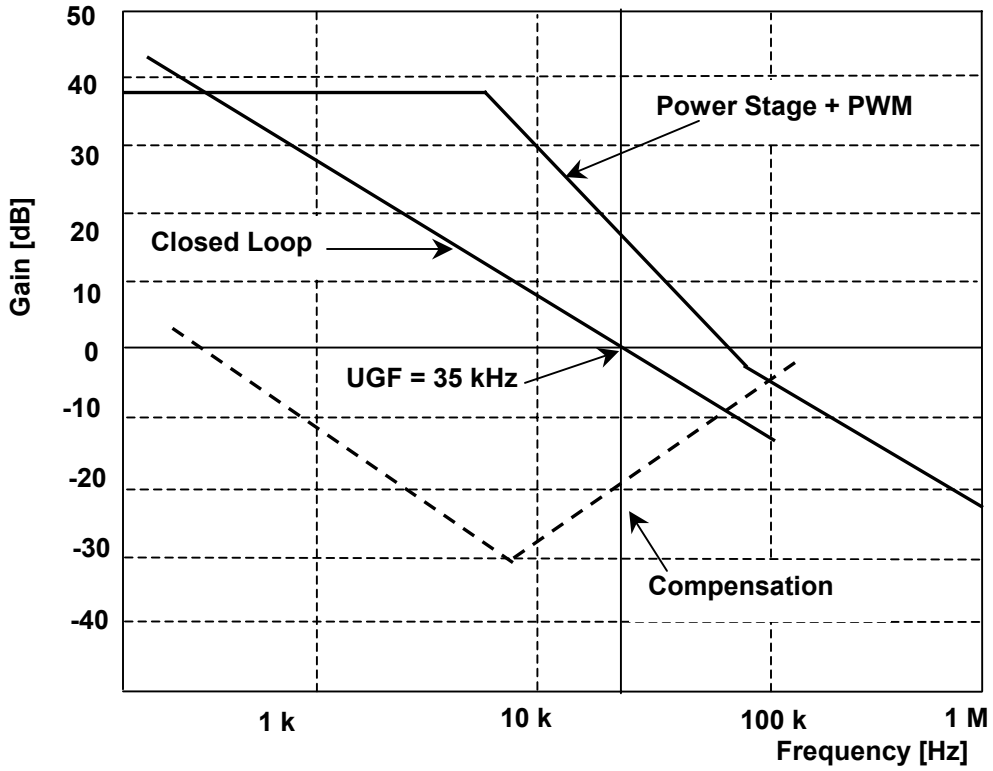


Figure 6.7. Line Bode diagram of the power stage and PWM generator, error amplifier compensation, and closed-loop transfer function of the buck-boost converter.

(b) Error Amplifier Op-amp: With a 1.4 V minimum supply, the control signal (V_{CON}) at the error amplifier's input is selected in the range of 0.1 – 1 V to generate a 0.5 – 5 V output voltage, which yields a closed-loop gain (A_{CL}) of five. In the presence of the op-amp's input offset voltage (V_{OFFSET_OPAMP}) and finite open-loop gain (A_{OL}), the converter's steady-state output voltage error (ΔV_{DC}) is given by

$$\Delta V_{DC} = \Delta V_{OFFSET\_OPAMP} + \Delta V_{GAIN\_ERROR} = \left| V_{OFFSET\_OPAMP} \times A_{CL} \right| + \left| \frac{V_{CON}}{\beta(1 + A_{OL})} \right|, \quad (6.5)$$

where ΔV_{OFFSET_OPAMP} and ΔV_{OFFSET_OPAMP} are error due to the offset voltage and gain error, respectively, and β is the feedback ratio, which is the ratio of output to control voltage.

A lower control signal range requires a higher closed-loop gain of the converter, which implies a smaller input offset voltage requirement for the error amplifier op-amp to achieve the same accuracy obtained with a lower closed-loop gain. Therefore, the idea is to maximize the input dynamic range by having an amplifier with close-to-rail input common-mode range (ICMR). The op-amp's dc gain is targeted to be greater than 60 dB to limit the converter's steady-state output voltage gain error to less than 5 mV because of the amplifier's gain error. The unity-gain frequency and phase margin of the op-amp are not specified since the error amplifier is compensated as a part of the overall feedback loop and is not designed to be stable as a standalone module. However, the design must ensure that the parasitic poles of the amplifier lie beyond the desired unity-gain frequency such that sufficient phase margin (greater than 30^0) is achieved.

(c) PWM Comparator: The PWM comparators should be functional over 300 mV peak-to-peak signal amplitude of the triangular wave generator, which is compared with the error amplifier's output voltage to generate digital pulses. The signal delay in the converter's feedback path contributes to a phase margin degradation of the overall loop response. The phase shift (φ in radians) due to feedback path propagation delay (t_{PD}) at the loop unity gain frequency (f_{UGF}) is given by

$$\varphi = 2\pi f_{UGF} t_{PD} . \tag{6.6}$$

For a 100 kHz unity-gain frequency and a phase degradation of 5 degrees, the total feedback path delay is estimated to be 140 nsec. Allocating a delay of 40 nsec to gate-drive and logic circuits, the comparator's propagation delay is estimated to be less than 100 nsec. Since the PWM comparator is subjected to a triangular wave stimulus, its response characteristic is different compared to a square wave stimulus for which the propagation delay is defined (details given in Appendix I). The comparator's dc gain is specified to be greater than 60 dB to achieve a resolution of 1 mV.

When a comparator is used inside the feedback control loop, its offset voltage is not critical because the loop automatically adjusts the error amplifier's output to yield the correct duty cycle. In the modified control scheme (described in Section 5.1), the PWM comparator's offset voltage may or may not affect the converter's operation region, depending on their relative changes. When both the comparators' offset-voltages have the same magnitude and polarity, the PWM operation remains unchanged. When the offset voltages cancel each other, the intermediate buck-boost region decreases. Conversely, when the offset voltages add to each other the intermediate buck-boost region increases as shown in Figure 6.8 (b), thereby decreasing the converter's efficiency.

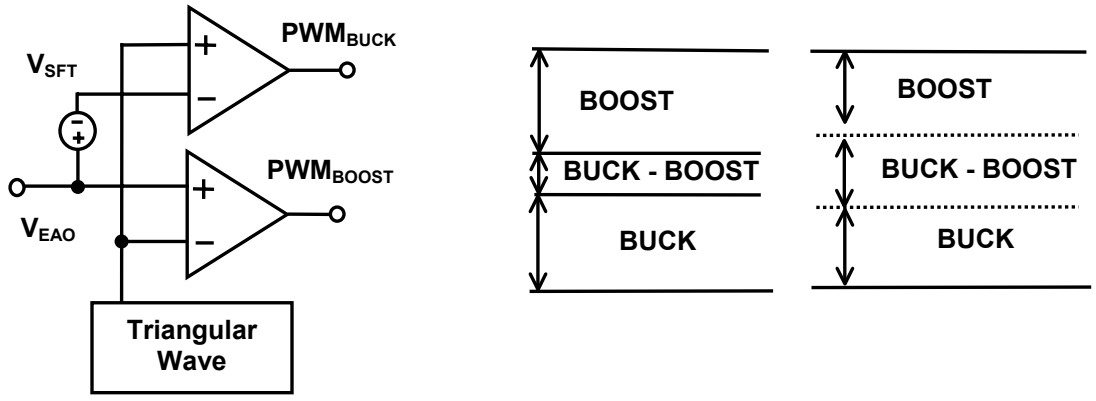


Figure 6.8. (a) Simplified schematic of the PWM block, (b) regions of operation under ideal conditions, and (c) modified region of operation under comparators with input-referred offset voltage.

By selecting a level-shift voltage of 270 mV with a triangular wave signal of 300 mV, each comparator can have a worst-case offset of 10 mV, effectively yielding an actual level-shift voltage at the comparator's input to either 290 mV or 250 mV.

(d) Triangular Wave Generator: The gain contributed by the PWM triangular wave in the feedback loop is equal to the reciprocal of its peak-to-peak voltage [72]-[73] and is given by

$$\text{Gain}_{\text{PWM}} = \frac{1}{V_{\text{PP\_TW}}}, \tag{6.7}$$

where V_{PP_TW} is the peak-to-peak signal amplitude of the triangular wave. A large peak-to-peak signal is desired to minimize the effect of switching noise on the system operation. However, in a low input supply of 1.4 V, a 300 mV nominal amplitude is selected taking into account the ICMR limits of NMOS input stage PWM comparator. A worst-case variation of 50 mV is allowed on the triangular wave signal by designing the PWM compensation network accordingly. The frequency of the signal generators is specified to be 1 MHz with a ± 20 % variation, for which the power stage is designed.

(e) Bandgap Reference: The reference signal for the maximum and minimum value of the triangular wave generator over supply voltage range, 1.4 – 4.2 V is provided by a bandgap reference circuit. A bandgap voltage of 1.21 ± 0.1 V is used for the high-side reference (V_{HIGH}) and the low-side reference signal (V_{LOW}) is generated with respect to V_{HIGH} such that a difference of 250 mV is maintained throughout the input voltage. The bandgap reference also generates a first-order, zero-temperature coefficient (TC) reference current of 2 μA, which is distributed for biasing various circuit blocks throughout the chip.

6.2.4. PFM Controller Design

The schematic of the PFM controller illustrating its key building blocks is shown in Figure 6.9. The PFM comparators, used for output voltage regulation and V_{PH1} sensing to detect negative inductor current in discontinuous-conduction mode (DCM) and the adaptive on-time generation circuit constitute key analog components in the PFM controller. The edge-triggered SR flip-flops should be designed for appropriate setup time, hold-time, and propagation delay with respect to minimum pulse-width for proper feedback loop operation.

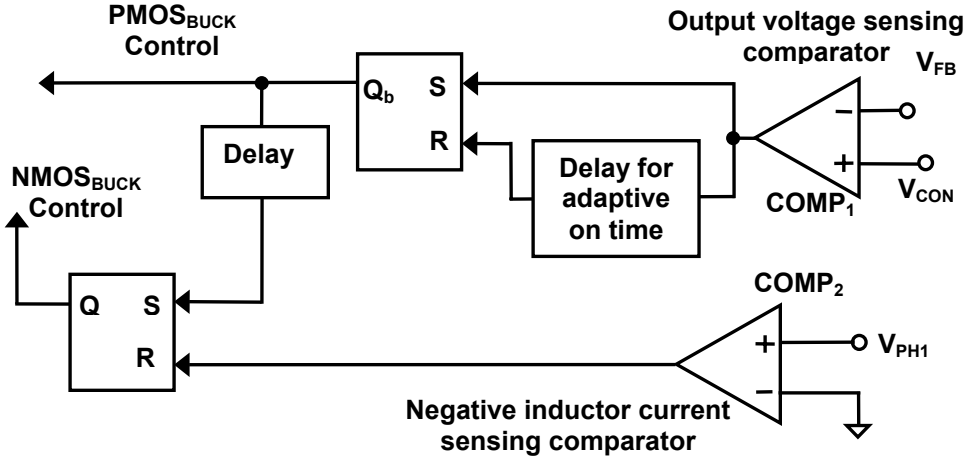


Figure 6.9. Schematic of the PFM controller.

(a) PFM Comparator: The comparator, $COMP_1$, for output voltage regulation is specified to have a input common-mode range (ICMR) of 50 – 150 mV, which is 50 mV about the desired feedback voltage of 100 mV for 500mV output voltage (closed-loop feedback gain of five). On the other hand, the comparator used for determining inductor current direction change from a positive to negative by sensing V_{PH1} node voltage, $COMP_2$, needs to be functional over a common-mode range of –50 to 50 mV for sensing zero voltage. Therefore, both comparator's ICMR specifications are combined into one to generate an ICMR requirement of –50 to 150 mV. Similar to the PWM comparator, the comparator's dc gain is specified to be greater than 60 dB to achieve 1 mV resolution.

The comparator's maximum propagation delay is specified to be less than 100 nsec with a 10 mV overdrive voltage accurate output voltage regulation and not allow the inductor current to reach a large negative value, thereby degrading the converter's PFM mode power efficiency. Although both the comparators are ideally required to have very small offset voltage, a maximum of 10 mV is specified, which however directly affects the converter's output ripple voltage. In the PA system, since the dynamic converter is programmed for a higher output voltage than the actual requirement, a maximum steady-state error of 50 mV is allowed without affecting the system functionality and performance.

(b) Adaptive ON Time Delay Circuit: To limit the peak-to-peak ripple voltage of 20 mV, the converter's required on time for 500 mV output voltage from a 1.4 – 4.2 V input supply with a 1 μH inductor and 20 μF output capacitor (calculated earlier for the PWM controller) is calculated from Equation 5.19. Figure 6.10 shows the desired on time of the controller over its supply voltage range to maintain an accurate output ripple voltage. Appropriate circuits must therefore be developed such that the converter's on time adjusted (trimmed) for a given supply voltage results in the desired on times for other supply voltages.

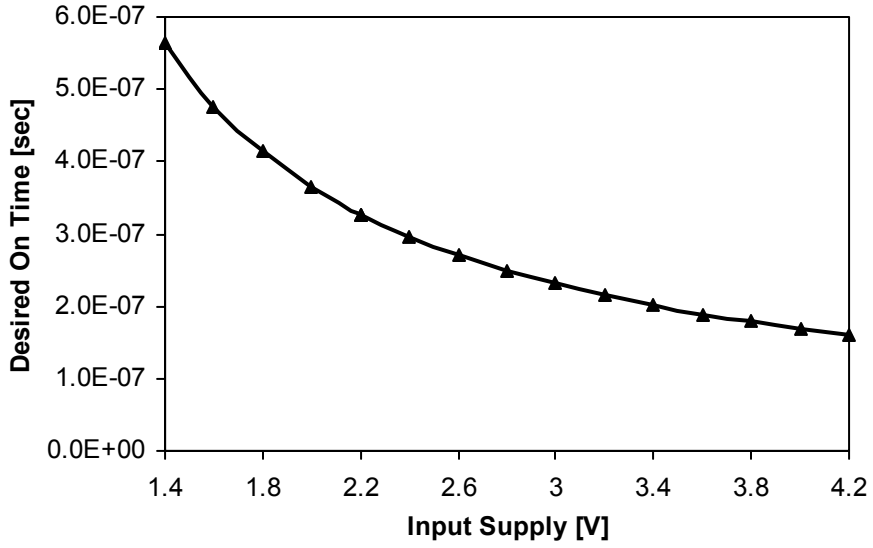


Figure 6.10. Desired on time of the PFM controller over the input supply voltage range.

6.3 Power Transistor and Gate Drive Circuit Design

6.3.1 Design Considerations

The motivation behind integrating power switches onto the same die with the control circuits is to reduce the number of external components, and thereby minimize the overall system size and cost. The switch resistance of a MOS transistor operating in the linear region is given by

$$R_{DS\_ON} = \frac{1}{k'\left(\frac{W}{L}\right)(V_{GS} - V_T)V_{DS}}, \tag{6.8}$$

where k' is the transconductance parameter given by the product of μ and C'_{ox}, μ is the mobility of the majority carrier (electron/hole), C'_{ox} is the gate oxide capacitance per unit area, W/L (width/length) is the aspect ratio, V_{GS} is the gate to source voltage, and V_T is the threshold voltage of the MOS device. Due to the higher mobility of electrons compared to holes and lower threshold voltage, a given switch resistance can be realized with a smaller aspect ratio, and hence a lower device area by using a NMOS transistor. However, implementing a NMOS transistor for the high-side buck switch suffers from two limitations: (a) due to the low supply voltage headroom, and (b) technology constraints in a low cost, N-well CMOS process, which are explained in the following paragraphs.

(a) Low Supply Headroom and Bootstrap Driver: Use of a NMOS transistor for the high-side switch necessitates a gate drive circuit that is referenced to the device's source. In battery-powered applications where a suitable direct gate drive signal for the NMOS is not available, bootstrapped circuits are commonly employed [74]. Figure 6.11 shows the schematic of a circuit for driving a high-side NMOS switch. When the PWM signal goes high to turn the MOSFET on, the level shift circuit's output goes low, thereby enabling the gate driver that actually turns the transistor on. The gate charge is taken from the bootstrap capacitor, C_{BST}. As the switch turns on, its source voltage swings to the positive

input rail, V_{IN}. At turn off, the PWM signal goes low tuning on the level shift circuit. As the NMOS gate discharges, its drain-to-source voltage increases and its source transitions to ground. During the off time of the transistor, the bootstrap capacitor, C_{BST}, is charged to a voltage level equal to the difference of input voltage V_{IN} and diode drop V_{DIODE}, through the bootstrap diode, D_{BST}.

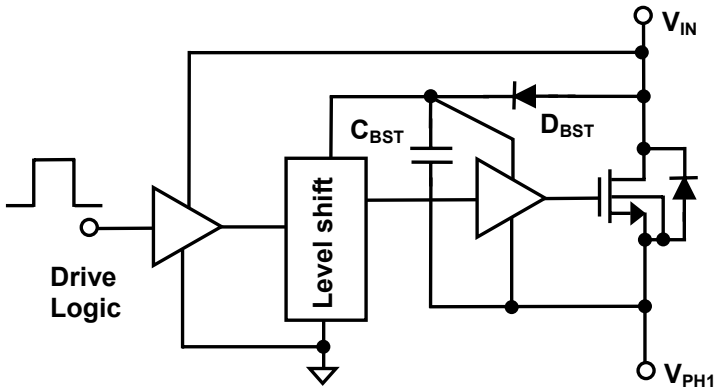


Figure 6.11. Schematic of the bootstrap circuit for the NMOS high-side drive.

The bootstrap scheme works satisfactorily for relatively higher supply voltages. Unfortunately, as input supplies get lower, the bootstrap capacitor is charged to a lower voltage value. For a 1.4 V input supply with a 0.7 V drop across the integrated diode, the bootstrap capacitor is charged to 0.7 V. which is not sufficient to turn the NMOS device on, rendering this arrangement unsuitable for low supply voltage environments. Moreover, the bootstrap capacitor is external and typically of the order of μF, which increases the external component count, board space, and overall system cost. An external Schottky diode can be used in place of the integrated diode for a lower voltage drop, which however defeats the purpose of moving closer to a system-on-chip (SOC) solution.

(b) Technology Constraint in an N-well CMOS Process: Figure 6.12 shows the body diodes of the main switch and synchronous rectifier when implemented as discrete and integrated solutions. Also, shown is the high-side body diode conduction when inductor

current goes negative in a synchronous converter operating in continuous-conduction mode. In a N-well CMOS process, bulk of all the NMOS devices are connected to a common substrate potential, generally to ground. Therefore, unlike a discrete circuit implementation, there is no body-diode from V_{PH1} node to the input supply, V_{IN}, in an IC implementation. Therefore, during the dead time between the low-side switch turning off and high-side switch turning on, there is no direct path for the inductor current to flow. In order for the inductor to sustain the current during this period of uncertainty, the node voltage V_{PH1} has to undergo a drastic transient, which would otherwise have been clamped by the high-side body diode. To avoid any potential catastrophic failure arising out of the transient event just mentioned, external Schottky diode may be used across V_{PH1} and V_{IN}, which increase the number of external component count, thereby defeating the goal of realizing a low cost, integrated solution.

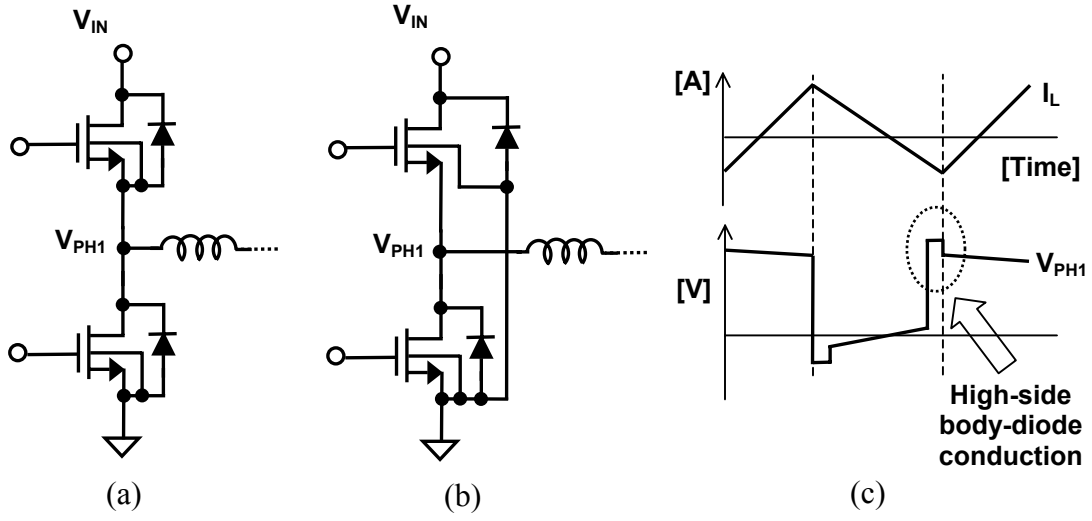


Figure 6.12. High-side NMOS transistor's body-diode in (a) discrete implementation, (b) n-well integrated circuit implementation. (c) Illustration of the high-side body diode conduction for negative inductor current in continuous-conduction mode

Therefore, to design an integrated solution without external Schottky diodes, a high-side switch is implemented using a PMOS device although it requires a larger die-area. The trade-offs for such an implementation lie in the die-area versus external component count. In a low voltage environment, a NMOS high-side switch cannot be

used for functionality considerations, unless a separate higher drive voltage is generated internally, which however increases the system complexity.

6.3.2 Integrated Circuit Design

The power transistors' aspect ratios are computed to realize 100 mΩ on resistance requirement derived earlier. The gate drive circuits are essentially cascaded inverters designed to charge and discharge the gate capacitances of the power switch while optimizing the propagation delay, power dissipation, and die area. Theoretically, minimum delay is achieved by sizing the driver stage 2.723 (≈e) times smaller the loading stage [80]. However, to optimize size and power consumption, typically a ratio of 5 – 10 is used in practice, since the delay variation with the ratio of driver size shows a broad optimum. While all other gate drivers are supplied from the input voltage, the logic level of the boost PMOS synchronous driver needs to follow the output voltage to completely turn it off. Therefore, the boost PMOS gate driver is powered from the output voltage. However, since the output voltage varies dynamically and can be different from the input supply, a level-shift supply voltage is required to translate the controller logic level, which is powered from the input voltage to the driver's input logic level. Figure 6.13 shows the schematic of the logic level-shift circuit along with the device dimensions. Figure 6.14 shows the power switches' dimensions and their respective gate drive circuits designed for the integrated buck-boost converter's power train.

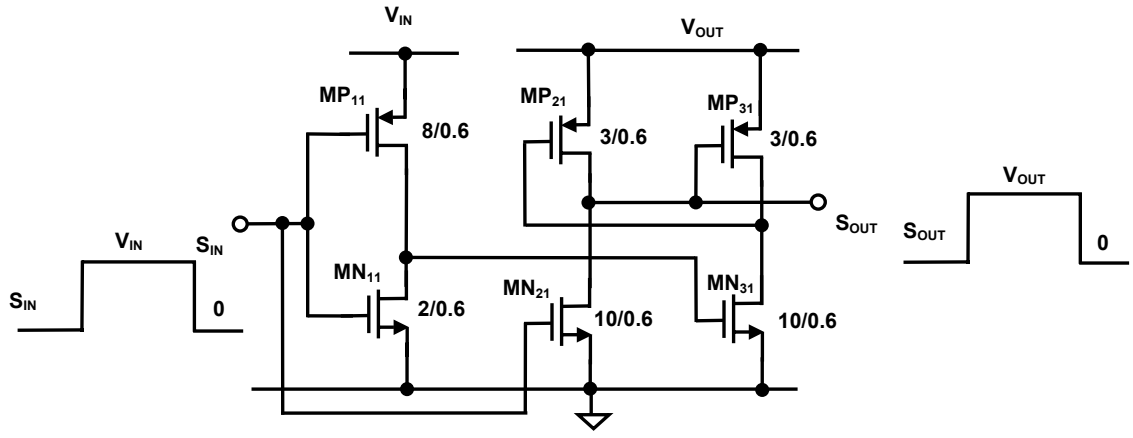
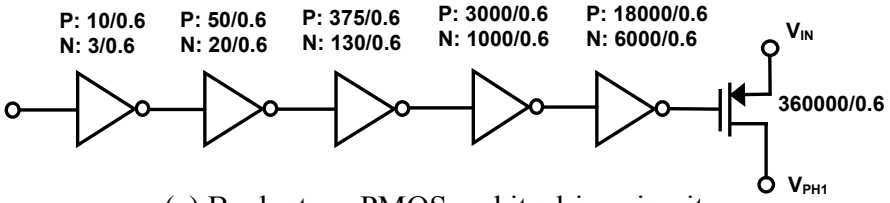
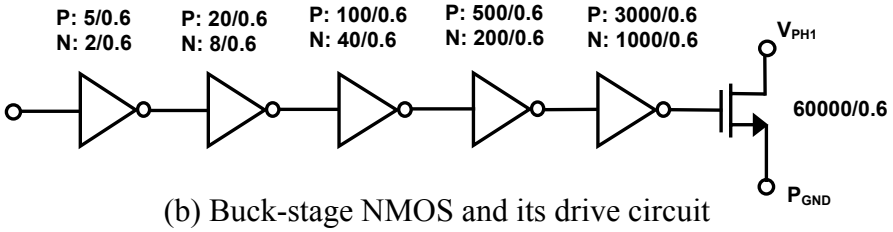


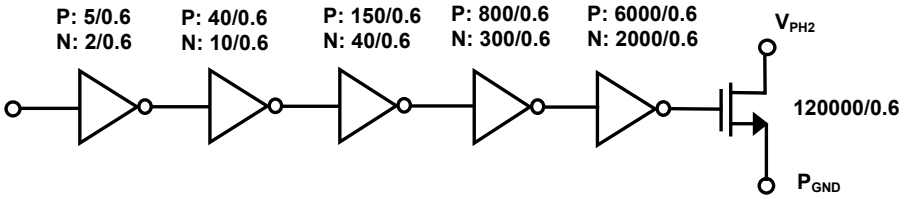
Figure 6.13. Schematic of logic-level converter (level-shifter) circuit (device sizes are in μm).



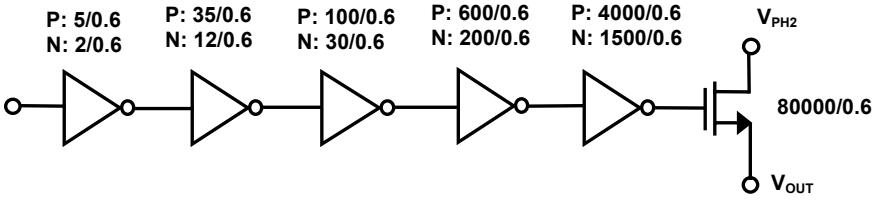
(a) Buck-stage PMOS and its drive circuit



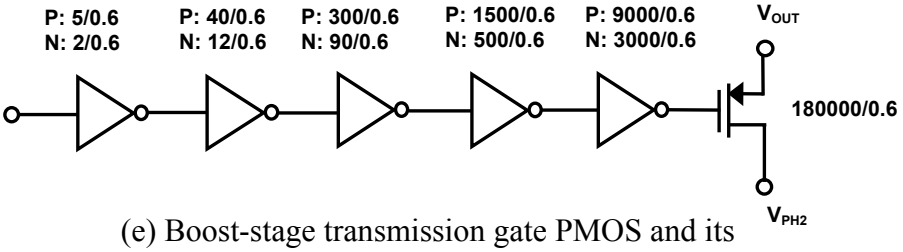
(b) Buck-stage NMOS and its drive circuit



(c) Boost-stage NMOS and its drive circuit



(d) Boost-stage transmission gate NMOS and its drive circuit



(e) Boost-stage transmission gate PMOS and its drive circuit

Figure 6.14. Schematic of the power transistors and their drive circuits with their respective aspect ratios and dimensions (in μm).

Table 6.3 offers the simulated device on-resistances of the power transistors for the two extremes of the supply voltage for which the design is targeted for use. An accurate extraction of the devices' on-resistance from the measured data was not possible since the experimentally measured data contained additional parameters due to the metal interconnect and bond wire resistances.

Table 6.3. Simulation results of the buck PMOS switch on-resistance.

Drive voltage	Unit	Target	Simulation	Worst-case sim.
BUCK PMOS				
1.4 V	mΩ	≤ 100	234.5	60.57 – 910
4.2 V	mΩ		28.24	18 – 43
BUCK NMOS				
1.4 V	mΩ	≤ 200	124	75 – 212
4.2 V	mΩ		62	44 – 84
BOOST NMOS				
1.4 V	mΩ	≤ 100	67. 72	37.2 –106
4.2 V	mΩ		31.23	22 – 41.6
BOOST PMOS				
1.4 V	mΩ		470	122 –1820
4.2 V	mΩ	≤ 100	56.5	37.2 – 87.4
BOOST NMOS T-Gate				
1.4 V	mΩ	≤ 100	102	68 – 127
4.2 V	mΩ		46.88	33 – 62.5

Table 6.4 offers the simulated and experimental gate drive propagation delays of the gate drive circuits for the power transistors. The boost-stage transmission gate NMOS transistor's drive's performance was not measured, since the gate of the device was not available for testing. Except the boost PMOS stage, all the other gate drive circuits' measured data match well with the simulated values. The mismatch in PMOS gate drive measured data from the simulated value is due to the higher gate resistance of the power device. While all the other power transistors' poly-silicon gates were connected through a metal layer around their peripheries for lower gate resistances, the boost-stage PMOS

device's gate had only poly-silicon due to a layout error. The higher poly resistance essentially delayed the charging and discharging or the actual gate node of the power MOSFET, which resulted in a higher than expected gate drive propagation delay. Figure 6.15 graphically illustrates this phenomenon.

Table 6.4. Simulation and measurement results of the drive stage propagation delays.

Drive voltage	Unit	Target	Simulation	Worst-case sim.	Exp
BUCK PMOS					
1.4 V	nsec	≤ 20	16	8 – 36	16.5
4.2 V	nsec	≤ 20	3.4	2.69 – 4.84	3.14
BUCK NMOS					
1.4 V	nsec	≤ 20	10	8 – 16	12.21
4.2 V	nsec	≤ 20	2.6	2.28 – 3.53	3.42
BOOST NMOS					
1.4 V	nsec	≤ 20	9	5 – 14	6.46
4.2 V	nsec	≤ 20	2.9	2.28 – 3.53	3.73
BOOST PMOS					
1.4 V	nsec	≤ 20	32	11.7 –101	170
4.2 V	nsec	≤ 20	2.2	1.6 – 2.9	110
BOOST NMOS T-Gate					
1.4 V	nsec	≤ 20	20	7 –29	CT
4.2 V	nsec	≤ 20	3.5	2.5 – 6	CT

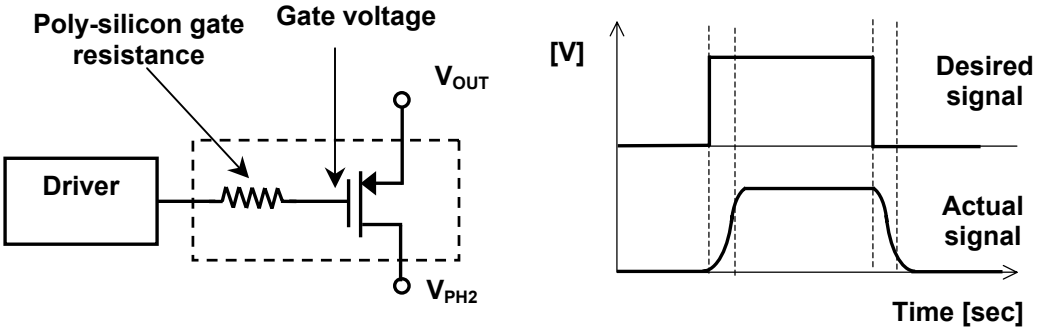


Figure 6.15. Illustration of the additional propagation delay in the boost-stage PMOS transistor resulting from higher gate resistance.

6.4 Error Amplifier Op-Amp

6.4.1 Topologies

The simplest circuit architecture, a NMOS input stage differential pair with a simple current mirror load, as shown in Figure 6.16(a) suffer seriously from input common-mode voltage limitations. Using a low voltage current mirror load as shown in Figure 6.16(b) can circumvent this handicap. However, in an N-well process since the bulk of the NMOS devices are connected to ground, the transistors are subjected to bulk-bias effect, which increases their threshold voltage. This problem is specifically prevalent under a variable supply voltage environment, where the gate potential of the mirror transistors track the supply voltage for a given bias current, thereby also changing the source potential of the level shift transistor. Folded cascode type architecture [as shown in Figure 6.16(c)] is typically used to further improve the common-mode range of the amplifier with NMOS input stage. However, the resulting ICMR is not sufficient to achieve the desired specification of 0.1 –1 V and therefore requires additional circuitry to convert the desired ICMR to workable range of the circuit topology under discussion.

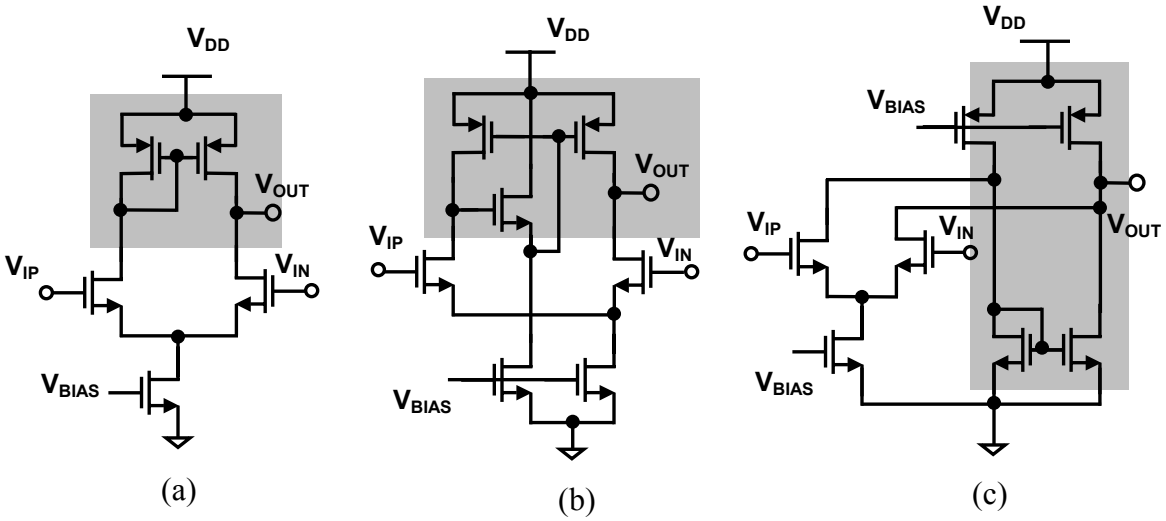
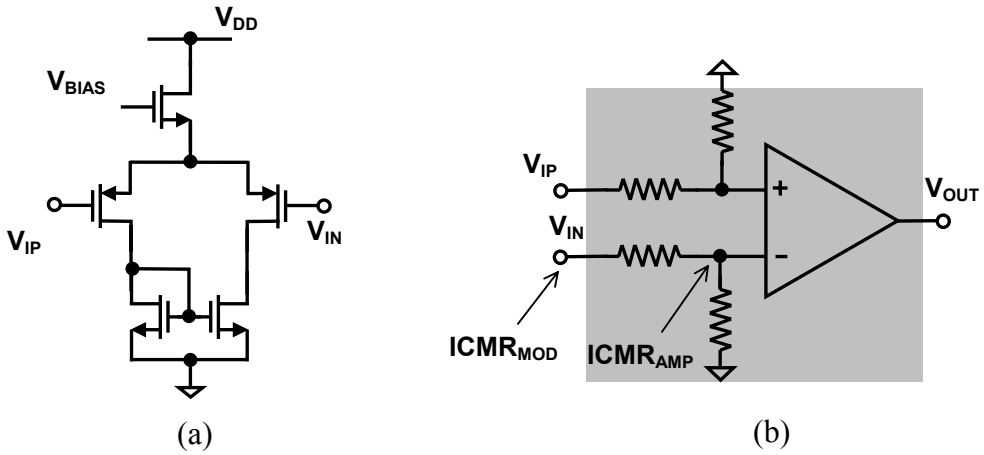


Figure 6.16. NMOS input stage differential amplifiers with (a) a simple current mirror load, (b) a low voltage current mirror load, and (c) folded mirror load architecture.

Figure 6.17(a) shows an amplifier with a PMOS input stage. Modifications similar to the NMOS differential input stage amplifier explained earlier can be extended to the PMOS input stage as well to improve the ICMR. Figure 6.17(b) illustrates the schematic of a circuit with PMOS input stage amplifier with attenuation resistors. The resistors are used to satisfy the amplifier's common-mode requirement, while still being able to use a larger actual input signal. The limitation of such an approach is low input offset requirement of the main amplifier compared to the top-level module, where the former is smaller by the attenuation factor of the resistive divider.



(a) (b)

Figure 6.17. (a) PMOS transistors differential input stage and (b) increasing the ICMR of the PMOS input stage with a resistive divider.

A complementary pair input stage with level shift resistors [93]-[94] as shown in Figure 6.18 offers an alternative way to realize large ICMR when the supply voltage is less than the sum of PMOS and NMOS transistors' threshold voltages. When the input signal has a common-mode range close to the supply rail, the NMOS differential pair operates. Conversely, the PMOS input differential pair operates when the input signal is close to the ground. As the input common-mode signal is increased above the ground level, the current sources (I) push more current into the resistors thereby yielding a higher voltage drop across them. Therefore, the input signal shifted down with a common-mode voltage drop (across the resistors) such that the actual input for the PMOS differential pair remains within its common-mode range. When the input signal is at the mid-level,

the current source and sinks carry maximum current shifting the input signal up and down such that both the PMOS and NMOS input pairs operate upon the input signal. For a higher input common-mode signal, the level-shift current reduces and only NMOS input pair remains operational. The disadvantages of such a scheme are circuit complexity with complementary input pairs, gain variation with input common-mode signal and resulting compensation requirement to ensure stable operation over supply voltage, process and temperature corners.

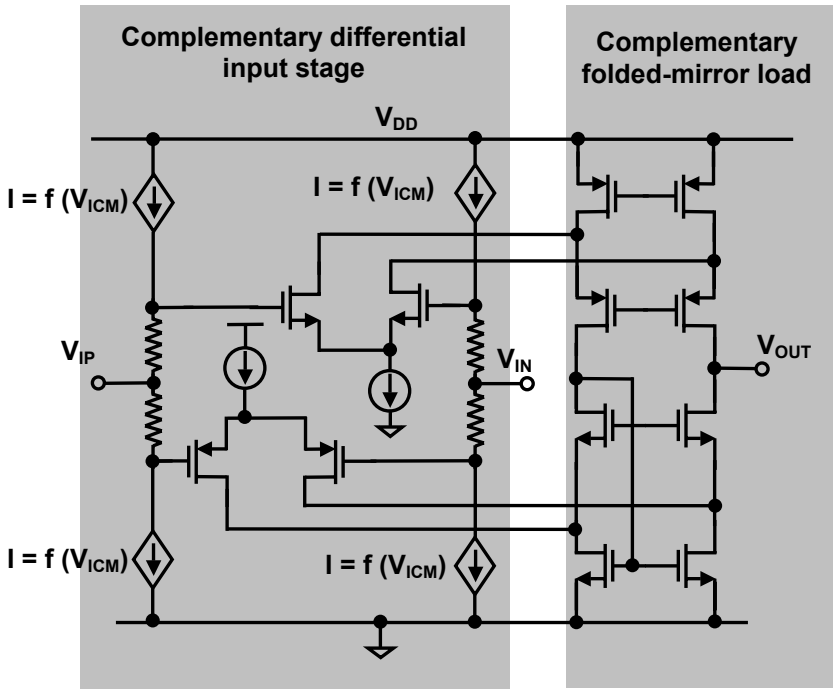


Figure 6.18. Complementary (PMOS and NMOS) pair input stage with level shifting resistor divider to realize a large ICMR op-amp.

Figure 6.19 presents the principle of operation of a close-to-rail ICMR op-amp with only one differential pair circuit [95]. An auxiliary amplifier along with two level shifting circuits using current mirrors and resistors are used in a negative feedback configuration to establish the common-mode signal of the main amplifier by producing adaptive voltages across the resistors. The circuit described in [95] uses a fixed common-mode reference voltage (V_{CM_REF}), which is suitable for a constant supply voltage.

However, for a variable supply voltage environment, which is 1.4 – 4.2 V for this design, the common-mode reference signal must track the supply voltage for the circuit to be functional. A simple reference signal, which tracks the power supply voltage is generated with the circuit (shaded) shown in Figure 6.19, ensures close-to-rail input signal operation over a wide supply voltage variation.

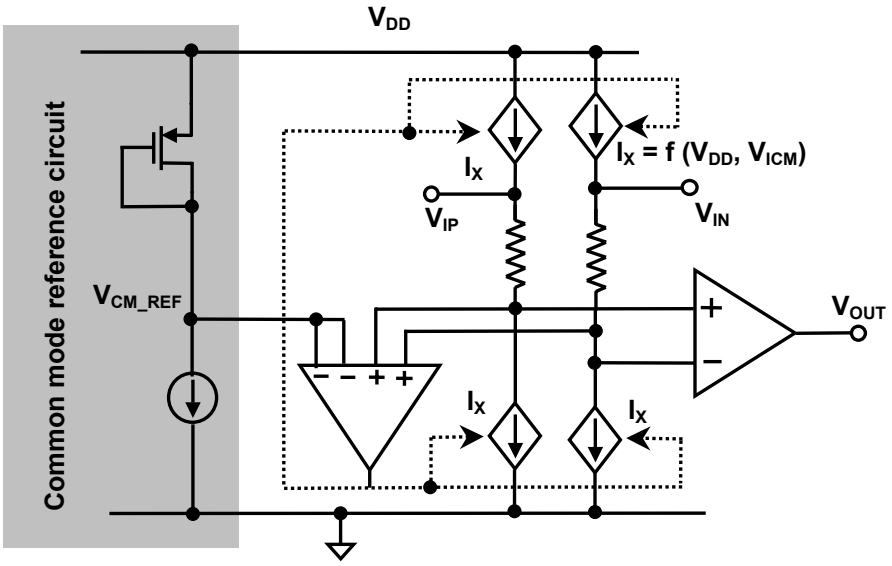


Figure 6.19. Supply voltage dependant, adaptive input common-mode feedforward based amplifier with PMOS input stage.

6.4.2 Slow-Start Circuit

Slow-start is essential for switching converters to avoid initial transients and potentially catastrophic failures. When the converter is powered on, the slow-start circuit slowly increases the reference control signal, which otherwise would have been determined by the external control voltage. The concept of realizing a slow-start with the error amplifier [96] is shown in Figure 6.20. At any instant, the lower of the two voltages V_{CON} and V_{SLOW} is actually used by the differential pair to control the feedback node voltage, V_{FB}. As the converter is switched on, the gate voltage (V_{SLOW}) of auxiliary differential pair transistor MP_{13} is slowly increased from zero at a rate depending on the current source, I_{CHARGE}, and the slow start capacitor, C_{SS}. The feedback node voltage

follows V_{SLOW} until it increases higher than V_{SLOW}, when V_{CON} takes over as the controlling input of the differential pair. After slow start, the capacitor is charged to the positive supply rail, effectively disabling the auxiliary input transistor MP_{13} from interfering with the normal operation of the differential pair transistors MP_{11} and MP_{12}.

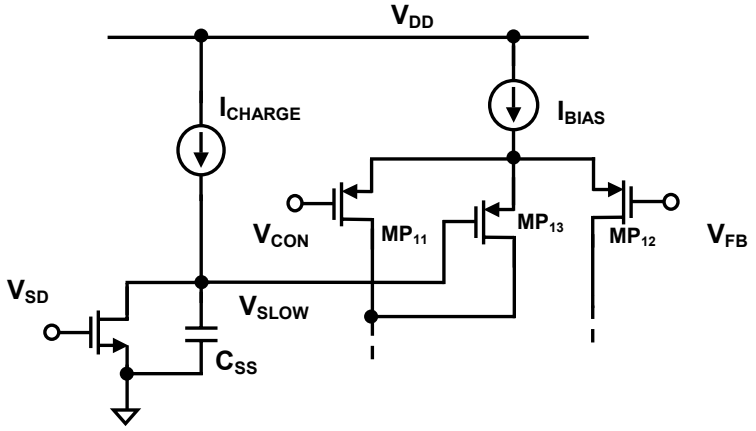


Figure 6.20. Illustration of the slow-start circuit as a part of the error amplifier [96].

6.4.3 Integrated Circuit Design

Figure 6.21 shows the complete schematic of the error amplifier op-amp consisting of three sub-blocks: biasing and enabling circuit, input common-mode adaptation circuit, and the main amplifier. The biasing transistor current mirrors MN_{B1} and MN_{B2} sets the current in the tail current sink transistor MP_{23}, and common-mode adaptation amplifier's tail-current sink MP_{15} via diode-connected mirror transistor MP_{B1}. The transistor MP_{C1} along with the biasing transistor MN_{B3} generates the reference voltage for the common-mode adaptation circuit.

Transistors MP_{11}, MP_{12}, MP_{13}, and MP_{14} form the input differential pairs of the common-mode adaptation circuit with current mirror loads MN_{11} and MN_{12}. The amplifier directly drives the gate of level shifting current sinks MN_{13}, MN_{14} and current sources MP_{17}, MP_{18} via transistors MN_{15} and MP_{19}. Resistors R_1 and R_2 generate the required level shift voltages depending on the current forced through them.

Compensation capacitor C_C is used to stabilize the common-mode adaptation loop. The shifted input signal is fed into the main amplifiers input pairs MP_{21} and MP_{22} with current mirror loads MN_{21} and MN_{22}. Common source amplifier transistors MN_{31} with current sink load MP_{31} is used as the second stage of the main amplifier for additional gain. The transistor's aspect ratios, level-shift resistors and compensation capacitor values of the design are given in Table 6.5.

Table 6.5. Component parameters of the designed error amplifier.

Sub-circuit	Component	Value
Main amplifier	$(W/L)_{MP21, MP22, MP23}$	16 × (4.5 μm / 1.8 μm)
	$(W/L)_{MN21, MN22}$	4 × (9 μm / 3 μm)
	$(W/L)_{MP24}$	12 × (12 μm / 3 μm)
	$(W/L)_{MN31}$	4 × (9 μm / 3 μm)
	$(W/L)_{MP31}$	6 × (12 μm / 3 μm)
Common-mode adapter	$(W/L)_{MP11, MP12, MP13, MP14}$	4 × (4.5 μm / 1.8 μm)
	$(W/L)_{MN11, MN12}$	4 × (4.5 μm / 1.8 μm)
	$(W/L)_{M15}$	10 × (12 μm / 3 μm)
	$(W/L)_{MN13, MN14, MN15}$	4 × (4 μm / 3 μm)
	$(W/L)_{MP16, MP17, MP18}$	4 × (16 μm / 3 μm)
	R	180 kΩ
	C_C	25 pF
Dynamic common-mode reference and bias generation	$(W/L)_{MNB1, MNB2, MNB32}$	4 × (5 μm / 5 μm)
	$(W/L)_{MPB1}$	2 × (12 μm / 3 μm
	$(W/L)_{MPC1}$	6 μm / 3 μm
	I_{BIAS}	2 μA ± 20%

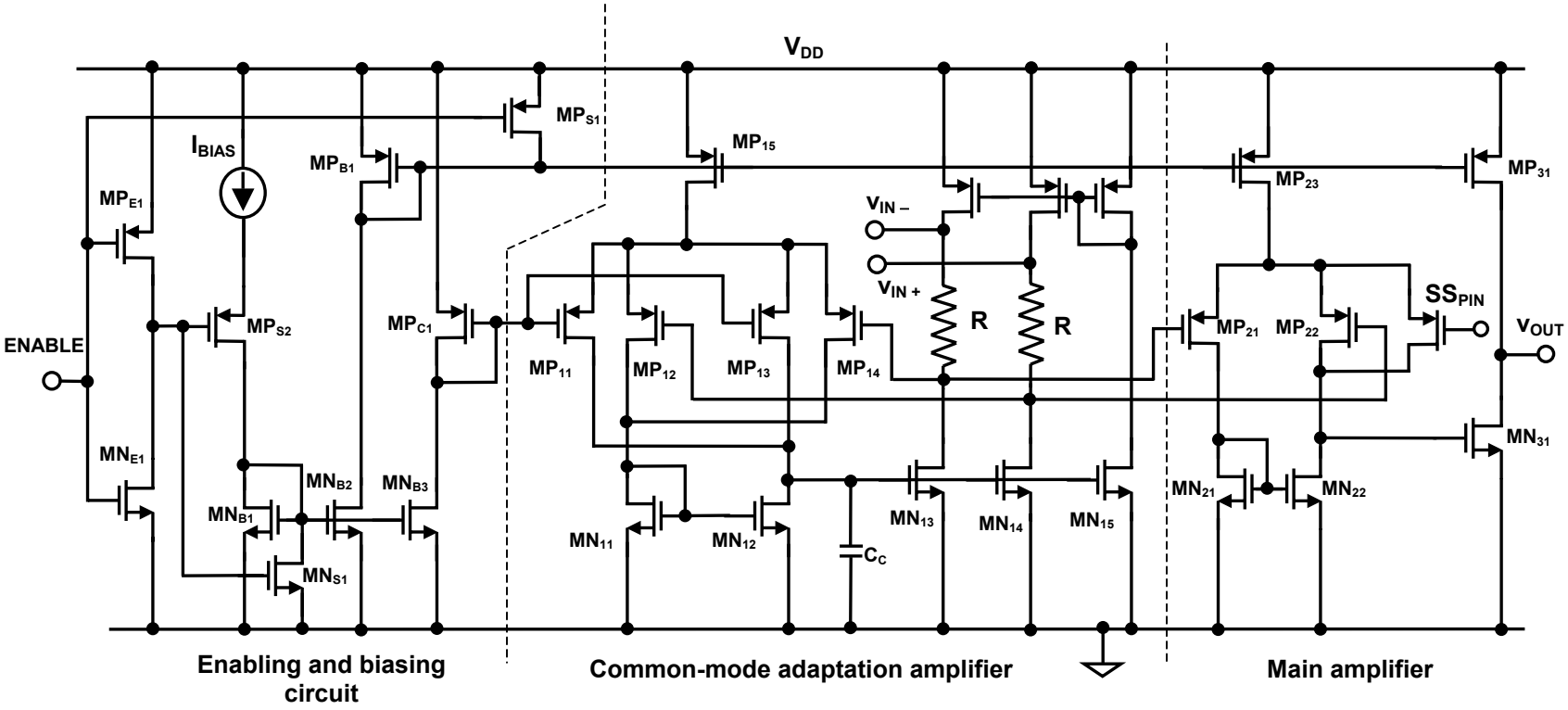


Figure 6.21. Complete schematic of the error amplifier op-amp with large input common-mode range (ICMR).

6.4.4 Simulation and Measurement Results

Table 6.6 presents nominal and worst-case simulation results and measured characteristic of the op-amp designed for the error amplifier in the buck-boost converter. The experimental results of the op-amp match with the expected values from simulation and meet the target specification for the two extremes of supply voltage with an ICMR range of 0.1 – 1 V, which crucial to achieve a converter output voltage of 0.5 – 5 V. The amplifier's measured dc gain was greater than 60 dB, thereby yielding a maximum gain error of 1 mV and consequently having converter's output voltage error of less than 5 mV.

Table 6.6. Simulation and measurement results of the error amplifier op-amp.

Specification	Unit	Target	Simulation	Worst-case sim.	Exp
V_{DD} = 1.4 V					
Quiescent current	μA	≤ 70	36	30 – 45	40
Power Dissipation	mW	≤ 0.1	0.05	0.04 – 0.06	0.056
DC Gain	dB	≥ 60	78 – 83 dB	76 – 92	≥ 60
ICMR	V	0.1 – 1	0.1 – 1.3	0.05 – 1.3	0.1 – 1.0
Output swing	V	0.93 – 1.27	0.15 – 1.29	0.13 – 1.29	0.1 – 1.3
Input offset voltage	mV	≤ 10	0.28 – 0.33	-0.2 – 0.5	≤ 5
CMRR	dB	≥ 60	75	58 – 140	≥ 60
PSRR @ dc	dB	≥ 60	80	52 – 142	≥ 60
V_{DD} = 4.2 V					
Quiescent current	μA	≤ 70	44	40 – 65	55
Power Dissipation	mW	≤ 0.21	0.18	0.17 – 0.27	2.31
DC Gain	dB	≥ 60	78 – 83 dB	76 – 92	≥ 60
ICMR	V	0.1 – 1	0.1 – 1.3	0.05 – 4.0	0.1 – 4.0
Output swing	V	0.93 – 1.27	0.15 – 4.1	0.13 – 4.07	0.1 – 4.15
Input offset voltage	mV	≤ 10	0.28 – 0.33	-0.2 – 0.5	≤ 5
CMRR	dB	≥ 60	86	58 – 140	≥ 60
PSRR @ dc	dB	≥ 60	120	52 – 142	≥ 60

6.5 PWM Comparator

6.5.1. Circuit Topology

An NMOS input differential stage is chosen for the PWM comparator to achieve a 300 mV ICMR under 1.4 V minimum supply voltage with nominal NMOS and PMOS threshold voltages of 0.75 and 0.95 V, respectively. As discussed in subsection 6.4.1, a differential pair with simple and level-shifted current mirror loads is not suitable for realizing large ICMR. Therefore, a folded mirror load is chosen for the comparator's input differential pair.

For 1 mV resolution and 100 nsec propagation delay a two stage architecture is used where the first stage amplifies a small differential input signal followed by a differential-to-single ended stage that transforms the amplified input signal into a logic high or low. Depending on the load capacitance, a number of buffer (inverter) stages are used to improve the drive capability of the comparator. Figure 6.22 illustrates a simplified representation of the three-stage comparator circuit [67] typically used to achieve higher resolution with smaller propagation delay. Since a low gain stage refers to a higher input offset voltage, the transistors in the preamplifier stage must be designed and laid out with the goal oaf maximizing their matching and thereby reducing their mismatch related offset.

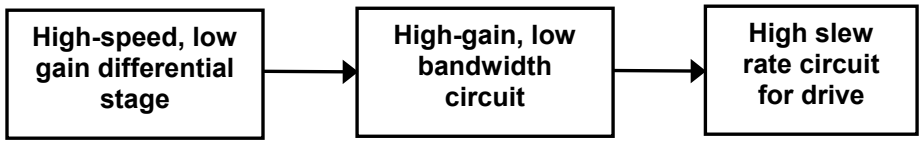


Figure 6.22. Conceptual representation of the low voltage, high resolution, fast comparator circuit [67].

6.5.2 Integrated Circuit Design

Figure 6.23 shows the PWM comparator's complete circuit schematic. The biasing current mirrors MN_{B1} generate required voltages for the differential input stage's current sink, MN_{13}, and second amplifier stage's current sink, MN_{23}. The folded mirror transistors for the differential input stage, MP_{11} and MP_{12}, are biased through diode

connected transistor MP_{B1} and MN_{B2}. Transistors MP_{E1}, MN_{E1}, MN_{S1}, MP_{S1}, and MP_{S2} are used to enable or disable the comparator depending on its requirement in active or sleep mode operation of the switching regulator.

Transistors MP_{11} and MP_{12} form differential input stage with MN_{14} and MN_{15} as diode connected loads resulting in a low gain but fast transient response circuit due to a small output impedance ($1/g_m$) and consequently yielding a high-frequency dominant pole. The comparator's second stage consists of input differential pairs MN_{21} and MN_{22} with current mirror loads MP_{21} and MP_{22}. Transistors MN_{31} and MP_{31}, and MN_{41} and MP_{41} form simple digital inverter circuits for driving capacitive loads. The transistor's aspect ratios of the PWM comparator design are offered in Table 6.7.

Table 6.7. Component parameters of the two-stage comparator.

Sub-circuit	Component	Value
Bias and enable/disable circuit	$(W/L)_{MNB1, MNB2}$	15 μm / 5 μm
	$(W/L)_{MPS1, MPS2}$	10 μm / 0.6 μm
	$(W/L)_{MNS1}$	5 μm / 0.6 μm
	$(W/L)_{MPE1}$	4.5 μm / 0.6 μm
	$(W/L)_{MNE1}$	1.5 μm / 0.6 μm
Preamplifier differential input stage	$(W/L)_{MN11, MN12}$	10 × (30 μm / 5 μm)
	$(W/L)_{MP11, MP12}$	30 × (20 μm / 5 μm)
	$(W/L)_{MN14, MN15}$	2 × (3.6 μm / 2.4 μm)
	$(W/L)_{MN13}$	20 × (15 μm / 5 μm)
Differential-to single-ended amplifier stage	$(W/L)_{MN21, MN22}$	16 × (8 μm / 2 μm)
	$(W/L)_{MP21, MP22}$	16 × (7.2 μm / 2.4 μm)
	$(W/L)_{MN23}$	30 × (15 μm / 5 μm)
Buffer stages	$(W/L)_{MN31}$	1.5 μm / 0.6 μm
	$(W/L)_{MP31}$	5 μm / 0.6 μm
	$(W/L)_{MN41}$	6 μm / 0.6 μm
	$(W/L)_{MP41}$	2 × (10 μm / 0.6 μm)

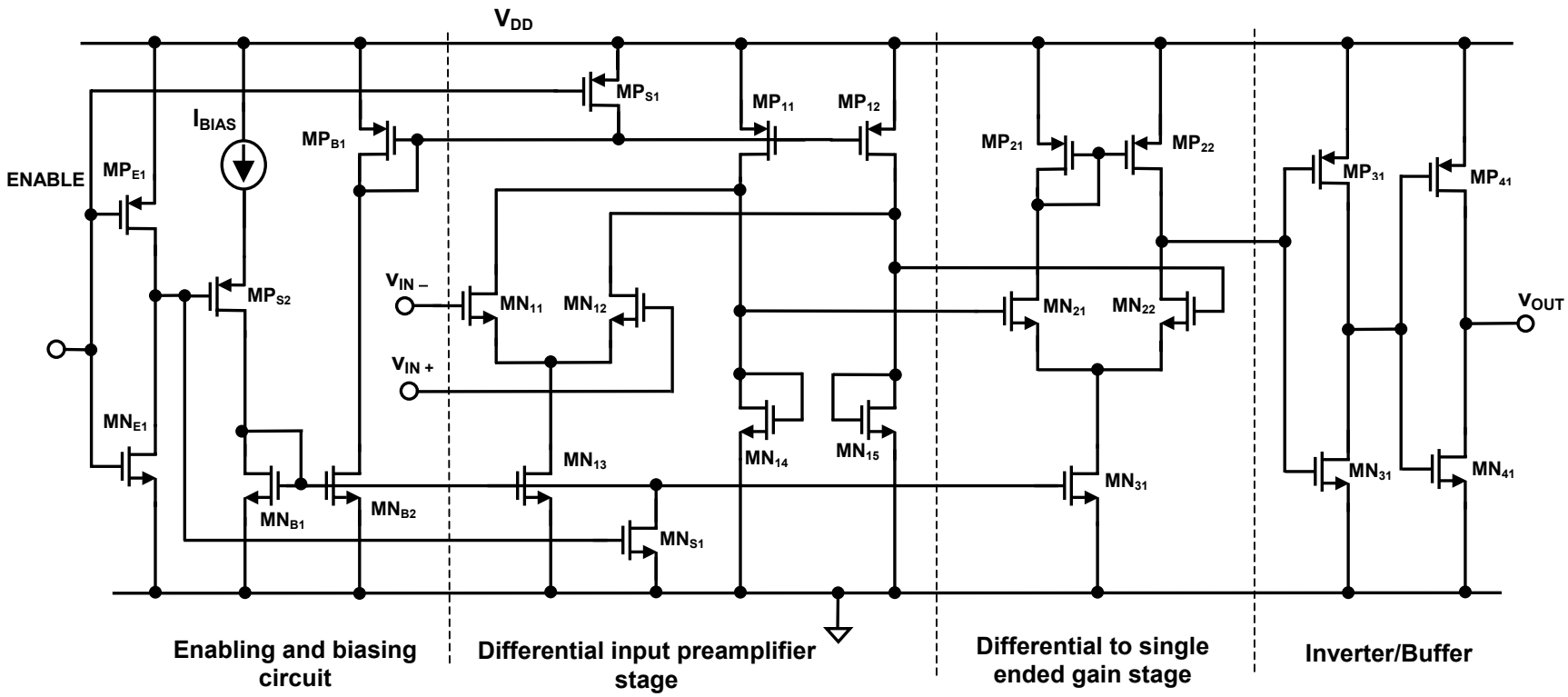


Figure 6.23. Complete schematic of the high speed, two-stage comparator circuit.

6.5.3 Simulation and Experimental Results

A summary of the simulation and experimental results of the comparator circuit for the two extremes of the supply voltages (1.4 and 4.2 V) is offered in Table 6.8. The comparator's propagation delay in both simulation and experimental IC is measured with a 10 mV overdrive step signal. In the experimental IC additional buffer circuits are used to drive the oscilloscope probe and other parasitic capacitances, therefore the core comparator's propagation delays could not be measured (marked as CT in Table 6.8).

Table 6.8. PWM comparator's simulation and experimental results summary.

Specification	Unit	Target	Sim	WC Range	Exp.
Supply Voltage = 1.4 V					
Quiescent current	μA	≤ 200	141 – 146	112-172	CT
Power Dissipation	mW	≤ 0.28	0.21	0.157 – 0.24	CT
ICMR	V	0.95 – 1.25	0.93 – V_{DD}	0.92 – V_{DD}	0.9 - V_{DD}
Load capacitance	fF	100 ± 20 %	100± 20 %	100± 20 %	50 pF
Propagation delay (t_{PLH})	nsec	≤ 100	49 – 48	35 - 89	CT
Propagation delay (t_{PHL})	nsec	≤ 100	59 – 56	43 -114	CT
Input offset voltage	mV	≤ 20	2	0.5 – 10	< 5
t_{PHL} with drivers	nsec		95		110
t_{PHL} with drivers	nsec		85		90
Supply Voltage = 4.2 V					
Quiescent current	μA	≤ 200	173.9 –173	138 – 220	CT
Power Dissipation	mW	≤ 0.84	0.73	0.58 – 0.924	CT
ICMR	V	0.95 – 1.25	0.85– 1.25	0.83 – V_{DD}	0.9 - V_{DD}
Load capacitance	fF	100 ± 20 %	100± 20 %	100± 20 %	50 pF
Propagation delay (t_{PLH})	nsec	≤ 100	65 – 56	37 – 92	CT
Propagation delay (t_{PHL})	nsec	≤ 100	61 – 58	39 – 91	CT
Input offset voltage	mV	≤ 20	-0.8	-1.2 – -0.4	< 5
t_{PHL} with drivers	nsec		88		90
t_{PHL} with drivers	nsec		100		110

However, since simulated and measured propagation delays of the comparators along with the drives match reasonably well, the core comparator's performance is expected to be within its desired specifications. Since the comparator was part an IC with other circuit blocks, its experimental quiescent current and power dissipation were not verified with simulation results.

6.6 Triangular Wave Generator

6.6.1 Circuit Topology

The basic principle used in the triangular wave signal generator is to charge and discharge a capacitor with a current source and sink, respectively, the schematic of which is shown in Figure 6.24. When the capacitor voltage is below V_{HIGH}, the output of the comparator $COMP_2$ remains at a logic low, which results turns the switch S_1 on through the SR flip-flop and inverter logic. The current source I charges capacitor C, thereby increasing its terminal voltage V_{TW}.

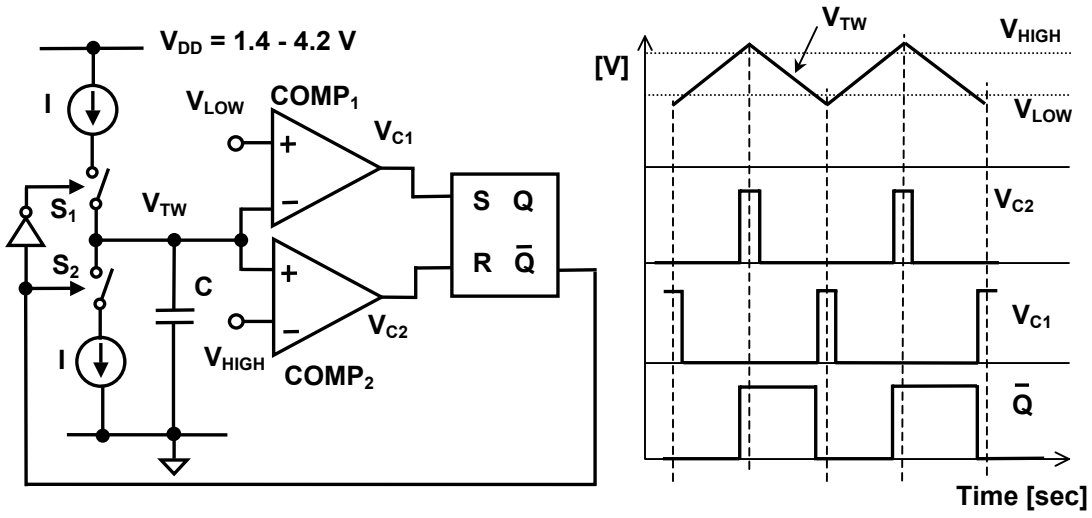


Figure 6.24. Basic principle of the triangular wave generator.

When the capacitor voltage increases above V_{HIGH}, the output of comparator $COMP_2$ goes high, which resets the SR flip flop, ultimately turning S_1 off and S_2 on.

During this interval, the current sink through switch S_2 discharges the capacitor. When V_{TW} goes below V_{LOW}, output of the comparator C_{COMP1} goes high, thereby setting the SR flip flop and ultimately turning S_2 off and S_1 on. The time-period (switching frequency) of the triangular wave can be changed by adjusting (trimming) either the charging and discharging current I, or capacitor C.

6.6.2 Integrated Circuit Design

Figure 6.25 shows the circuit schematic of the triangular wave generator with the current sources and controlling switches implemented with transistors. The circuit for comparators $COMP_1$ and $COMP_2$ is the same as the PWM comparator described earlier in Section 6.5. Transistors MP_1 and MN_1 form the current source and sink to charge and discharge the capacitor C enabled by switching transistors MP_{S1} and MN_{S1}, respectively. The bias current I_{TW} is established in MP_1 via transistors MN_2 and MP_2. While switches MN_{S1} and MP_{S1} control the current sources, additional switches MN_{S2}, MP_{S2} and MN_{S2} are used to improve the current mirror accuracy.

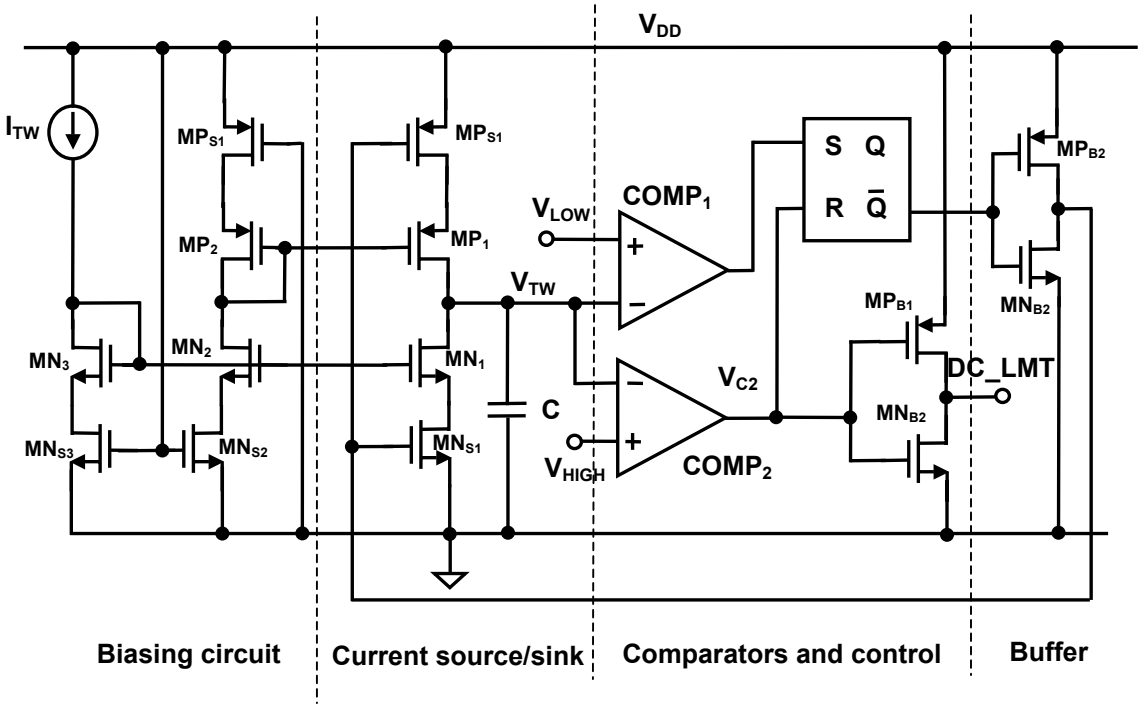


Figure 6.25. Complete schematic of the triangular wave generator.

The current source and sink enabling switches swiches are plaed close to the power supply and far from to the output node V_{TW} to mizimize the effect of charge injection error on triangular wave due to the turning on and off of the control switches. The duty cycle limit signal DC_LMT required by the boost stage is generated from the output of comparator $COMP_2$ using an inverter consists of transistors MN_{B1} and MP_{B1}, thereby eliminating the need of another comparator circuit. The duty cycle limit signal generated from this design is correlated with the triangular wave signal. However, the duty cycle is not accurately controlled from process and supply voltage variations, since the comparator delay changes. Table 6.9 offers the component parameters of the design.

Table 6.9. Component parameters of the triangular wave generator.

Component	Value
$(W/L)_{MN1, MN2, MN3}$	4 × (15 μm / 3 μm)
$(W/L)_{MP1, MP2}$	8 × (22.5 μm / 3 μm
$(W/L)_{MPS1, MPS2}$	4 × (50 μm / 0.6 μm)
$(W/L)_{MNS1, MNS2}$	4 × (15 μm / 0.6 μm)
$(W/L)_{MNB1, MNB2}$	10 μm / 0.6 μm
$(W/L)_{MPB1, MPB2}$	3 × (10 μm / 0.6 μm)
I_{TW}	20 μA
C	20 pF

6.6.3 Simulation and Experimental Results

Table 6.10 presents the simulation and measurement results of the triangular wave generator circuit. All the other measured results except the duty cycle limit (DC_LMT) match reasonably well with the simulated values. An exact value of the maximum duty cycle value is critical to prevent the converter to reach the undesired operating point, the details of which is discussed earlier in Section 5.1. In a low supply voltage environment, a given output voltage can be generated with two duty cycle values, distinguished from each other by corresponding inductor currents. For the higher duty cycle, the inductor current is larger and with further rise in the duty cycle the output voltage drops, which is

undesired for proper converter operation. For a higher input voltage operation, the duty cycle limit is generally not a problem, since the converter is operated with a lower duty cycle. The experimental results marked CT, were not verified since several circuits in the chip were power-on simultaneously by one enable control signal.

Table 6.10. Summary of the simulated and measured results of the triangular wave generator.

Specification	Unit	Target	Sim.	Worst-case Sim.	Exp.
Supply voltage = 1.4 V					
Quiescent current	μA	≤ 500	342	284 – 408	CT
Power dissipation	mW	≤ 0.7	0.478	0.397 – 0.578	CT
V_{OUT} (Trough)	V	≤ 0.96	0.953	0.953 – 0.968	0.91
V_{OUT} (Peak)	V	≥ 1.24	1.248	1.236 – 1.254	1.32
Frequency	MHz	≥ 0.9	1.03	0.96 – 1.12	1.04
DC_LMT	%	0.75 ≤ X ≤ 0.90		0.86 – 0.89	0.91
Supply voltage = 4.2 V					
Quiescent current	μA	≤ 500	406	336 – 503	CT
Power Dissipation	mW	≤ 2.1	1.71	1.41 – 2.1	CT
V_{OUT} (Trough)	V	≤ 0.96	0.958	0.956 – 0.964	0.92
V_{OUT} (Peak)	V	≥ 1.24	1.252	1.241 – 1.257	1.3
Frequency	MHz	≥ 0.9	1.1	1.09 – 1.21	1.23
DC_LMT	%	0.75 ≤ X ≤ 0.90		0.83 – 0.88	0.94

6.7 PFM Comparator

6.7.1 Circuit Topology

To design for the PFM comparator's ICMR specification of –50 to 150 mV a PMOS differential input stage is selected. For a lower ICMR value of –50 mV, a folded-mirror load [Figure 6.26(a)] can be used. Alternatively, since the PMOS devices have higher threshold voltages than the NMOS threshold voltage in the 0.5-μm n-well CMOS

process technology of this design, a simple current mirror load is used by connecting the input PMOS pairs' bulk to power supply. Therefore, the input pairs' threshold voltages is increased due to bulk-bias effect and consequently yielding a lower ICMR limit of less than –50 mV, which is expressed as

$$\mathrm{ICMR}_{\mathrm{LOW}} = \mathrm{V}_{\mathrm{TN}} + \mathrm{V}_{\mathrm{DS\_DSAT}} - |\,\mathrm{V}_{\mathrm{TP}}\,|, \tag{6.9}$$

with a nominal value of V_{TN} = 0.75 V and $|V_{TP}|$ = 0.95 V. The use of folded mirror architecture is avoided due to its relatively higher quiescent power dissipation, circuit complexity, and extra transistor-matching requirement that is critical to minimize input offset voltage.

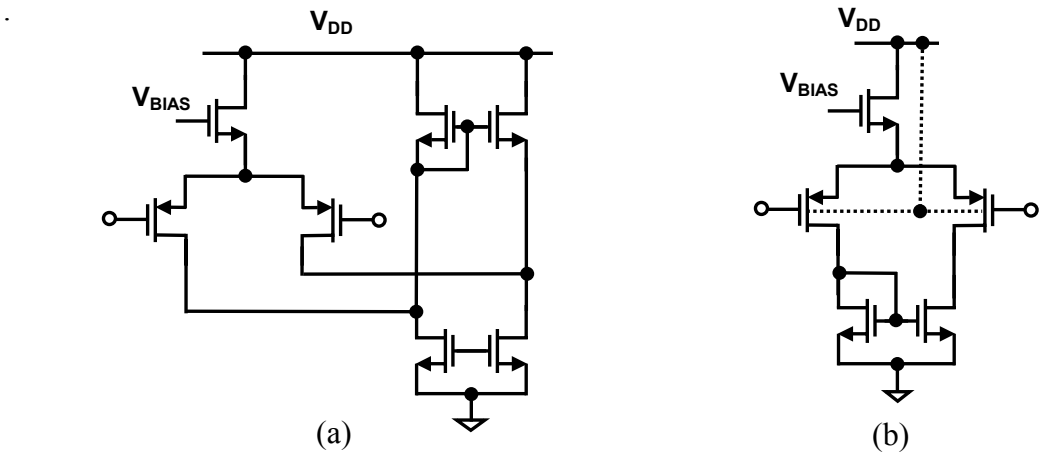


Figure 6.26. PMOS input stage with (a) folded-mirror load (b) current mirror load with input transistors' bodies connected to power supply for extending the ICMR below ground.

6.7.2 Integrated Circuit Design

Figure 6.27 shows the complete schematic of a standard two-stage comparator [67]. The biasing transistor current mirrors MN_{B1} sets the bias current in the differential input stage's tail current source MP_{13} and second stage's bias current source MP_{21} through diode-connected transistor MP_{B1} and biasing transistor MN_{B2}. Transistors MP_{E1},

MN_{E1}, MN_{S1}, MP_{S1}, and MP_{S2} are used to enable or disable the comparator depending on its requirement during active or sleep mode operation of the switching regulator. Transistors MP_{11} and MP_{12} form input pairs of input differential stage with MN_{11} and MN_{12} current mirror load. The second stage of the comparator consists of common source amplifier transistor MN_{21} with MP_{21} as a current source load. Transistors MN_{31} and MP_{31}, and MN_{41} and MP_{41} are simple digital inverter circuit used to drive capacitive loads. The component sizes of the designed comparator are given in Table 6.11. The buffer circuit's dimensions are same as those used for the PWM comparator.

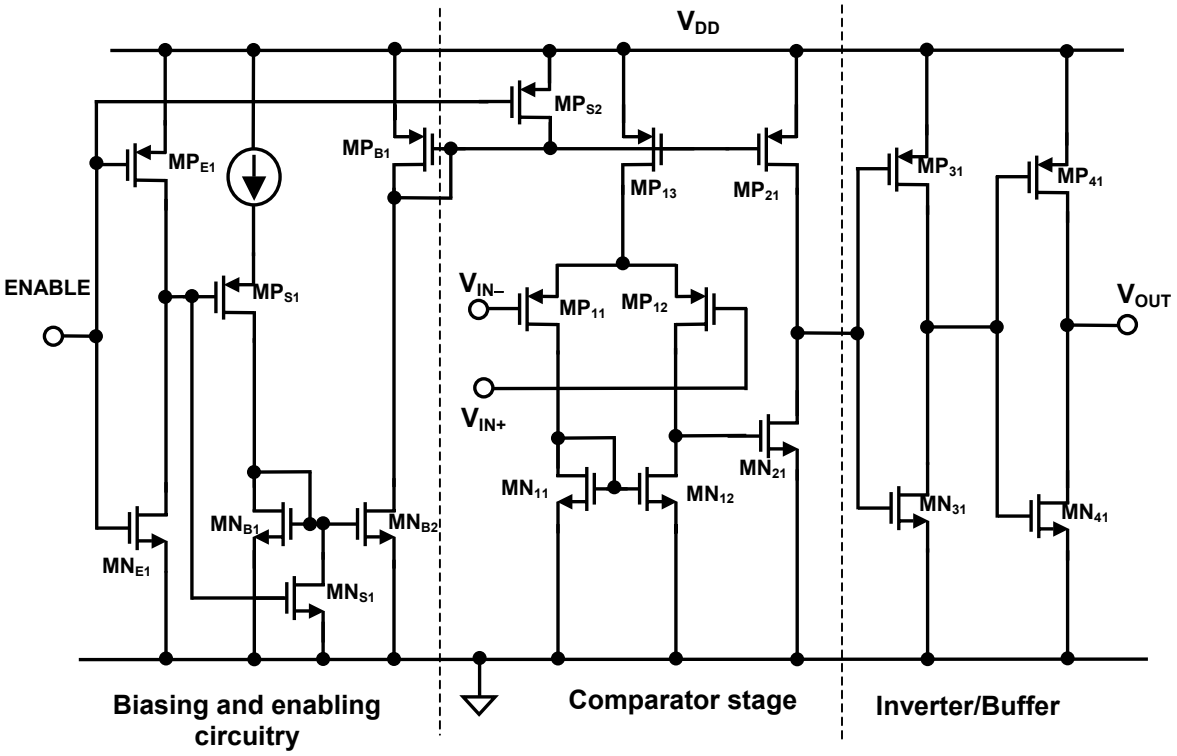


Figure 6.27. Complete schematic of the PFM comparator circuit.

Table 6.11. PFM comparator's component parameters.

Sub-circuit	Component	Value
Bias and enable/disable circuit	$(W/L)_{MNB1, MNB2}$	4 × (5 μm / 3 μm)
	$(W/L)_{MPS1, MPS2}$	10 μm / 0.6 μm
	$(W/L)_{MNS1}$	5 μm / 0.6 μm
	$(W/L)_{MPE1}$	4.5 μm / 0.6 μm
	$(W/L)_{MNE1}$	1.5 μm / 0.6 μm
Two-stage comparator	$(W/L)_{MN11, MN12}$	8 × (7.2 μm / 2.4 μm)
	$(W/L)_{MP11, MP12, MP1SS}$	16 × (12 μm / 2.4 μm)
	$(W/L)_{MPB1}$	32 × (12 μm / 3 μm)
	$(W/L)_{MPB2}$	20 × (12 μm / 3 μm)
	$(W/L)_{MN23}$	4 × (7.2 μm / 2.4 μm)

6.7.3 Simulation and Experimental Results

A summary of the simulation and experimental results of the comparator circuit for the two extremes of the supply voltages (1.4 and 4.2 V) is offered in Table 6.12. The comparator's propagation delay in both simulation and experimental IC is measured with a 10 mV overdrive step signal. In the experimental IC additional buffer circuits are used to drive the oscilloscope probe and other parasitic capacitances, therefore the core comparator's propagation delays could not be measured (marked as CT in Table 6.12). However, since the comparator's simulated and measured propagation delays with the drives match reasonably well, the core comparator's performance is expected to be within its desired specifications. Since the comparator was part an IC with other circuit blocks, its quiescent current and power dissipation was not experimentally verified.

Table 6.12. Summary of PFM comparator's simulation and measurement results.

Specification	Unit	Target	Simulation	Worst-case Sim.	Exp.
Supply voltage= 1.4 V					
Quiescent current	μA	100	66.09	51.08 – 78.8	CT
Power dissipation	mW	0.14	0.092	0.071 – 0.11	CT
Load capacitance	fF	100 ± 20 %	100 ± 20 %	100 ± 20 %	50 pF
Propagation delay (t_{PLH})	nsec	≤ 150	46	37 – 91	CT
Propagation delay (t_{PHL})	nsec	≤ 150	115	69 – 149	CT
Input offset voltage	mV	≤ 10	0.017	-0.041 – 2.1	≤ 5 mV
ICMR	mV	-50 – 150		-60 – 180	-50 –175
t_{PLH} with drivers	nsec		99		100
t_{PLH} with drivers	nsec		146		150
Supply voltage = 4.2 V					
Quiescent current	μA	100	77.88	65.28 – 93.72	CT
Power dissipation	mW	0.42	0.327	0.274 – 0.393	CT
Load capacitance	fF	100 ± 20 %	100 ± 20 %	100 ± 20 %	50 pF
Propagation delay (t_{PLH})	nsec	≤ 150	88	78 - 146	CT
Propagation delay (t_{PHL})	nsec	≤ 150	80	56 - 119	CT
Input offset voltage	mV	≤ 10	-0.02	-0.045 – - 0.015	≤ 5 mV
ICMR	mV	-50 – 150		-60 mV – 2.98 V	-50 mV – 2.95 V
t_{PLH} with drivers	nsec		146		150
t_{PLH} with drivers	nsec		116		130

6.8 Variable Delay Generator for PFM

6.8.1 Integrated Circuit Design

A generalized concept for adaptive on time with variable input and output voltage targeted for PFM control is earlier described in Section 5.4. For dynamic supply of a PA in this design, the output voltage of the converter in PFM mode is approximately 500 mV. Since the output voltage is close to the threshold voltage of an NMOS transistor, its

gate-to-source voltage is used as a measure of the actual output voltage to establish an input supply and output voltage dependent current, which is required for adaptive on-time generation for the buck-stage PMOS in PFM control. Accordingly, the schematic of the circuit adopted in this design is shown in Figure 6.28.

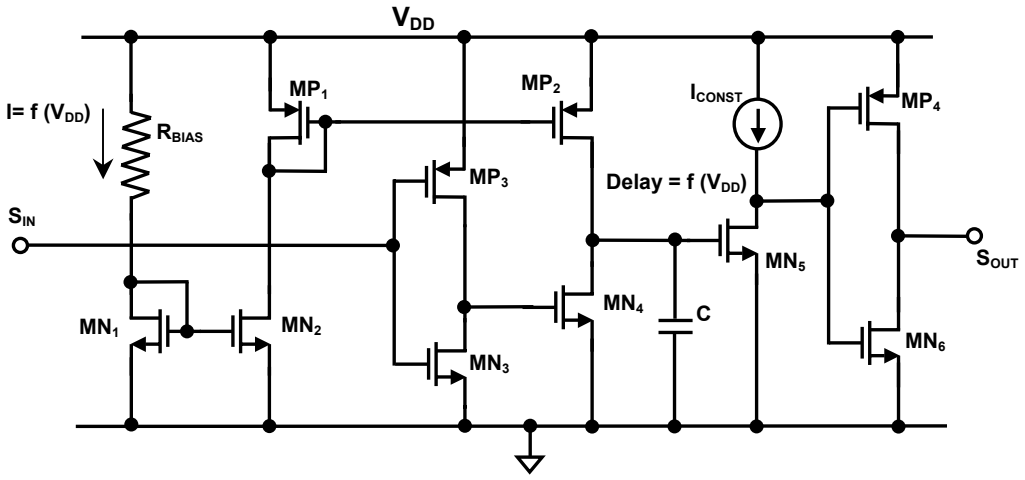


Figure 6.28. Complete schematic of the adaptive on time circuit for the PFM controller.

Using large aspect ratios for the transistors MN_1 and MN_2 such that they operate in sub-threshold region, an approximate difference of input and output voltage is established across the bias resistor, R_{BIAS}. The resulting current is mirrored through transistors MN_2, MP_1, and MP_2 to charge the capacitor C. When the capacitor is charged beyond the trip point of the inverter circuit consisting of MN_6 and current source I_{CONST}, its output state changes. For a higher supply voltage, a larger current is established through the resistor R_{BIAS}, which in turn flows through MP_2 and charges the capacitor faster yielding a smaller delay. Alternatively, a lower supply voltage establishes a smaller current resulting in longer delay or on time. In the IC developed in the research, R_{BIAS} designed such that it can be trimmed to achieve the specified on time.

6.8.2 Simulation and Experimental Results

Figure 6.29 presents the simulated and measured on time of the circuit with supply voltage change, which shows that for the worst-case resistance and capacitance values the on time varies almost twice from one corner to the other. The measured plot was generated for a trimmed $R_{BIAS,}$ which matches well with the target specifications.

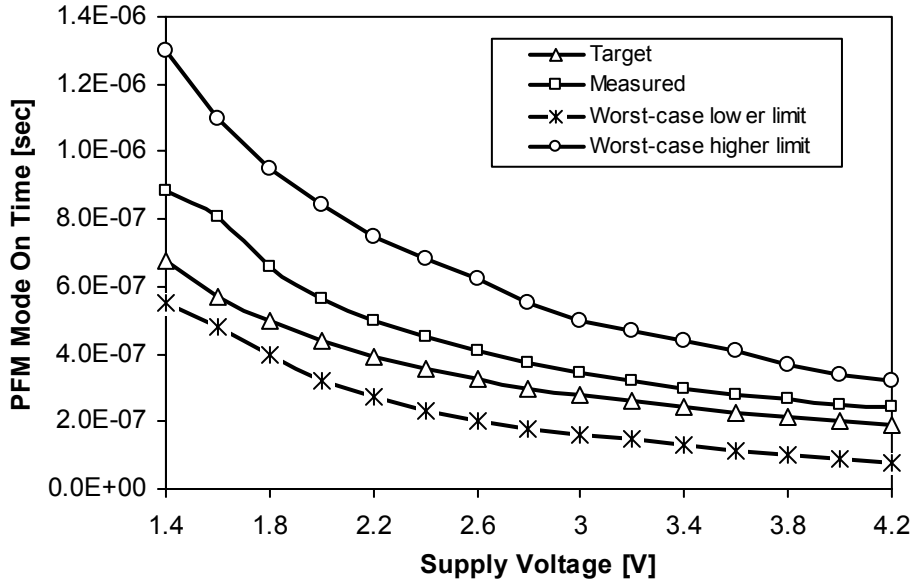


Figure 6.29. Simulated and measured on-time characteristic of the adaptive on-time circuit with supply voltage variation.

6.9 Bandgap Reference Circuit

6.9.1 Circuit Topology

Bandgap references are widely incorporated in all stand-alone ICs to generate reference voltages and bias currents for different circuit blocks independent of supply voltage and temperature variation. As identified earlier, the buck-boost power supply IC requires reference voltages for the triangular wave generator. A plethora of circuit topologies available for bandgap reference, a comprehensive review of them can be found in [24], [67], [96]. For a minimum supply voltage of 1.4 V, and N-well CMOS

process technology, Figure 6.30 shows the schematic of the conceptual representation of the circuit [97] used in this design illustrating its basic principle of operation.

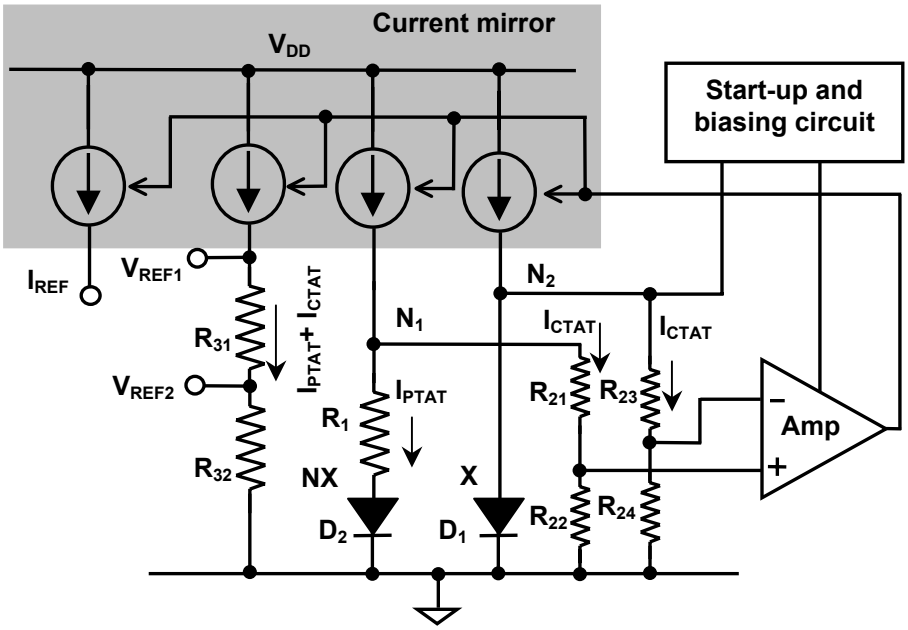


Figure 6.30. Conceptual representation of the low voltage bandgap reference circuit.

In an N-well CMOS process technology, the diodes D_1 and D_2 are implemented using the p-substrate, n-well and p^+-diffusion (used for PMOS), with p-substrate and n-well connected to the ground together. These diodes (D_1 and D_2) having area ratio 1: N along with R_1 form the base-emitter voltage (V_{BE}) loop of the bandgap circuit. The node voltages N_1 and N_2 are shifted down by resistors R_{21}, R_{22}, R_{23}, and R_{24} such that input signal to the amplifier, A, remains within its input common-mode limits. During normal operation, the positive and negative input voltages of the amplifiers are same (assuming no input offset and high open-loop gain), which forces the node voltage N_1 and N_2 to be equal. Therefore, the current flowing through the current sources is equal to the sum of currents through the diodes and level-shift resistors and is given by

$$I_{REF} = \frac{V_{BE}}{R_2} + \frac{V_T \ln N}{R_1}, \tag{6.10}$$

where N is the diode area ratio, V_T is the thermal voltage (kT/q ≈ 26 mV), and resistance R_2 is the summation of level-shift resistances R_{21} and R_{22}, which is also equal to summation of R_{23} and R_{24}. The current through diodes is a proportional-to-absolute-temperature (PTAT) current, while a complementary-to-absolute-temperature (CTAT) current is established through the level-shift resistors. The reference current flows through a resistor R_3, which is equal to the summation of R_{31} and R_{32} to generate a reference voltage (V_{REF}) and is given by

$$V_{REF} = I_{REF} R_3 = \left(\frac{V_{BE}}{R_2} + \frac{V_T \ln N}{R_1} \right) \times R_3 . \tag{6.11}$$

By selecting the diode area ratio N and resistors R_1, R_2, and R_3 appropriately, the desired reference voltage, inclusive of the bandgap voltage of 1.21 V, and reference current are generated.

6.9.2 Integrated Circuit Design

Figure 6.31 shows the complete schematic of the bandgap reference circuit with the amplifier, start-up circuit, and the core reference component. The core reference block is described earlier and for brevity not explained in this section. Transistors M_{C1}, M_{C2}, M_{C3}, and M_{C4} form the current sources carrying reference currents in the bandgap circuit. Transistors MP_{11} and MP_{12} form differential input pairs of the amplifier with MN_{11}, MN_{12}, MN_{13}, MN_{14}, MP_{13} and MP_{14} forming folded load mirrors, while MP_{15} is used as a tail current source biasing the differential pair. The transistors MP_{S1}, MP_{S2}, MP_{S3}, and MN_{S1} constitute the start-up circuit for the bandgap. When powered-on the gate potential of transistors MP_1 and MP_2 is close to the ground potential, thereby turning the transistors on and pushing current into the low impedance of the bandgap core and the amplifier. As the amplifier starts carrying current, the feedback loop becomes functional

stabilizing the reference current and generating the required bandgap voltage. Transistor MN_{S1} is sized such that at maximum supply voltage is current sinking capability is lower than the current established through MP_{S3} after start-up. Therefore, after the bandgap is started and subsequently reference voltage and current are established by the circuit, the gate voltage of MP_{S1} and MP_{S2} are pulled closer to the V_{DD} thereby turning them off. The component parameters and transistor sizes of the design are given in Table 6.13.

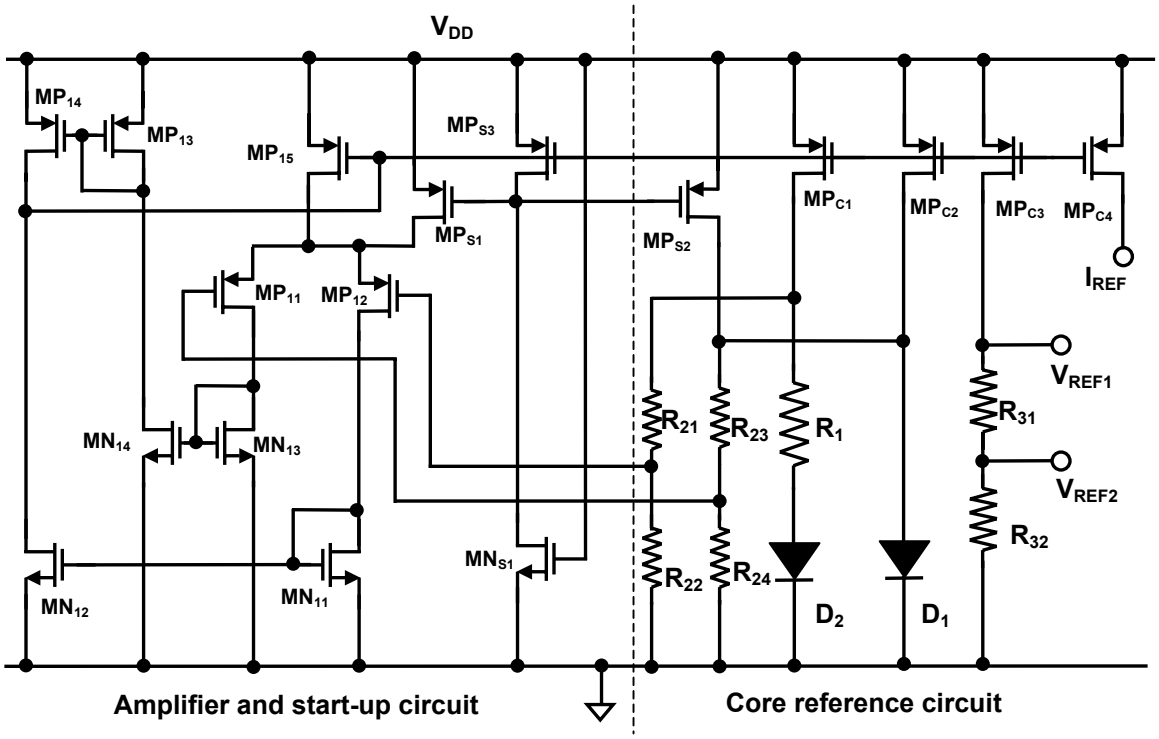


Figure 6.31. Complete circuit schematic of the bandgap-based voltage and current reference.

Table 6.13. Component parameters of the bandgap reference circuit.

Sub-circuit	Component	Value
Core bandgap circuit	$(W/L)_{MPC1, MPC2, MPC4}$	4 × (40 μm / 20 μm
	$(W/L)_{MPC3}$	16 × (40 μm / 20 μm)
	D_1	1.5 μm × 3.0 μm
	D_2	16 × (1.5 μm × 3.0 μm)
	R_{21}, R_{23}	300 kΩ
	R_{22}, R_{24}	180 kΩ
	R_1	45 kΩ
	R_{31}	125 kΩ
	R_{32}	155 kΩ
Low voltage amplifier and bias circuit	$(W/L)_{MP11, MP12}$	8 × (20 μm / 5 μm)
	$(W/L)_{MN11, MN12, MN13, MN14}$	4 × (10 μm / 5 μm)
	$(W/L)_{MP11, MP12}$	4× (10 μm / 5 μm)
	$(W/L)_{MP13}$	16× (10 μm / 5 μm)
Start-up circuit	$(W/L)_{MPS1, MPS2}$	10 μm / 0.6 μm)
	$(W/L)_{MPS3}$	40 μm / 20 μm
	$(W/L)_{MNS1}$	1.5 μm / 1 mm

6.9.3 Simulation and Experimental Results

Figure 6.32 shows the measured line regulation performance of the untrimmed experimental bandgap reference circuit, which is approximately 5 mV/V. Figure 6.33 shows a zoomed plot of the line regulation performance to demonstrate the minimum supply requirement for the bandgap to be 1.35 V. When the supply voltage is reduced below the minimum value, the reference goes into drop out mode. Figure 6.34 shows the reference current generated from the bandgap circuit, which varies from 2.7 – 3 μA over the supply voltage range, 1.4 – 5 V.

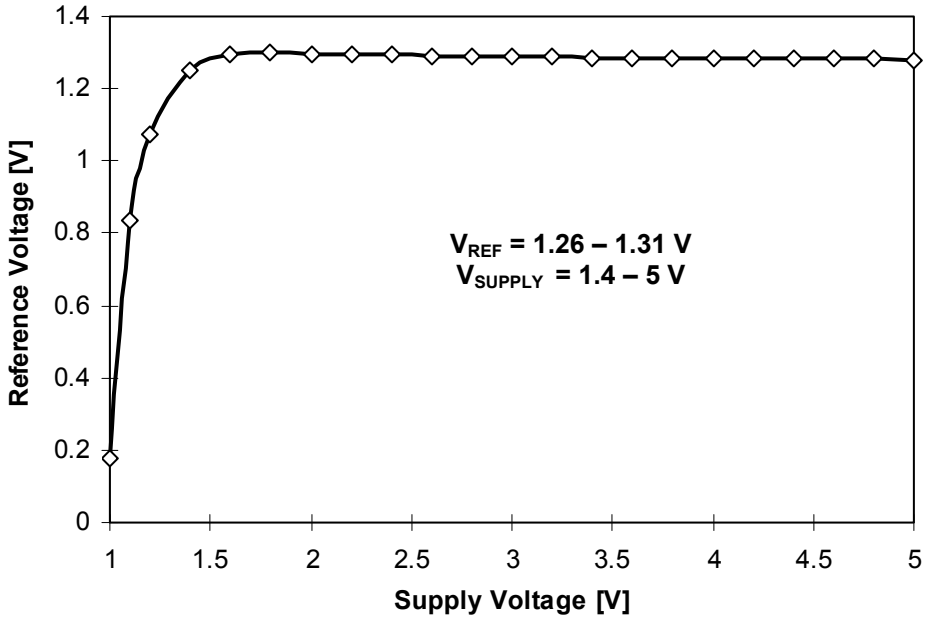


Figure 6.32. Measured line regulation performance of the bandgap reference.

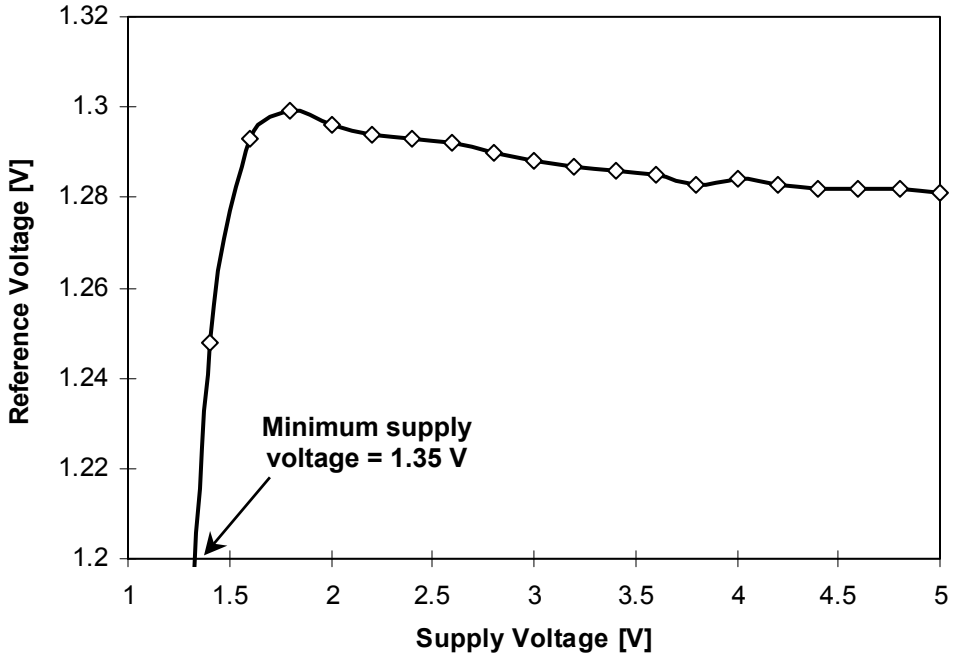


Figure 6.33. Measured minimum input supply voltage for the bandgap reference.

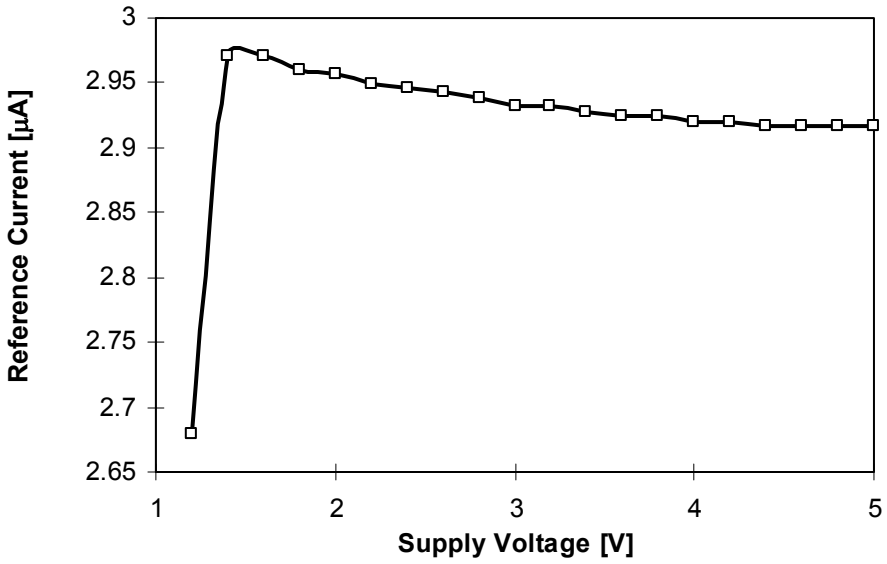


Figure 6.34. Measured reference current generated from the bandgap circuit.

Figure 6.35 shows the measured supply current of the bandgap circuit, which varies from 35 – 45 μA over the supply voltage of 1.4 – 4.2. The increase in supply current at higher voltage is primarily due to the channel length modulation of the amplifier transistors. The variation of the untrimmed bandgap voltage for an input supply of 1.4 V over a temperature range of 30 –125 ^{0}C changes between 1.1 and 1.28 V as shown in Figure 6.36, yielding a temperature coefficient of 0.82 mV/ ^{0}C. Higher precision can be obtained by trimming the resistors used in the circuit; however, since in this design the absolute value is not critical, trimming is avoided. The fluctuation of bandgap voltage over temperature is attributed to the measurement errors. Figure 6.37 illustrates the start-up characteristic of the bandgap as the input voltage is slowly increased from zero to the minimum supply voltage of 1.35 V.

A summary of the simulation and measured results of the bandgap reference circuit presented in this section is given in Table 6.14. The measured values of reference voltages and currents are well within the worst-case limits obtained from the simulation. However, the experimental results of the circuits meet the target specifications, as evident from the data presented in Table 6.14.

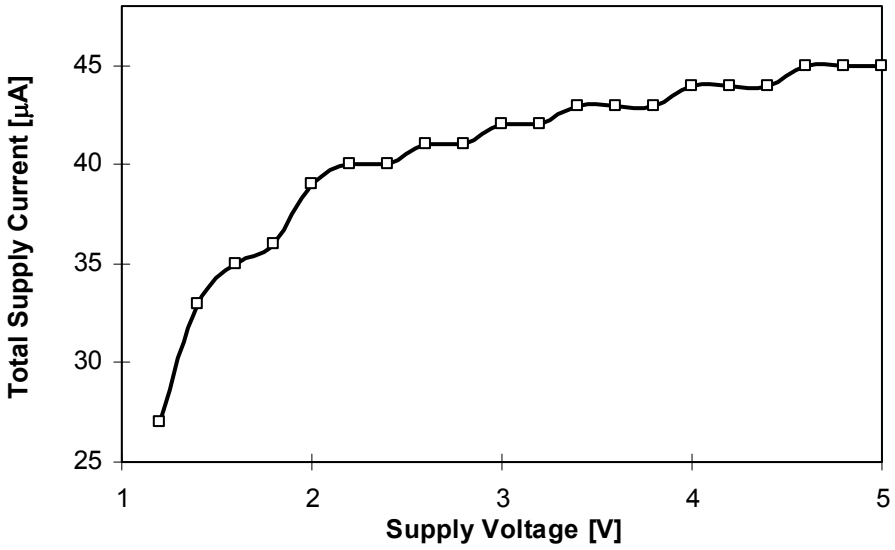


Figure 6.35. Measured supply current drawn by the bandgap reference.

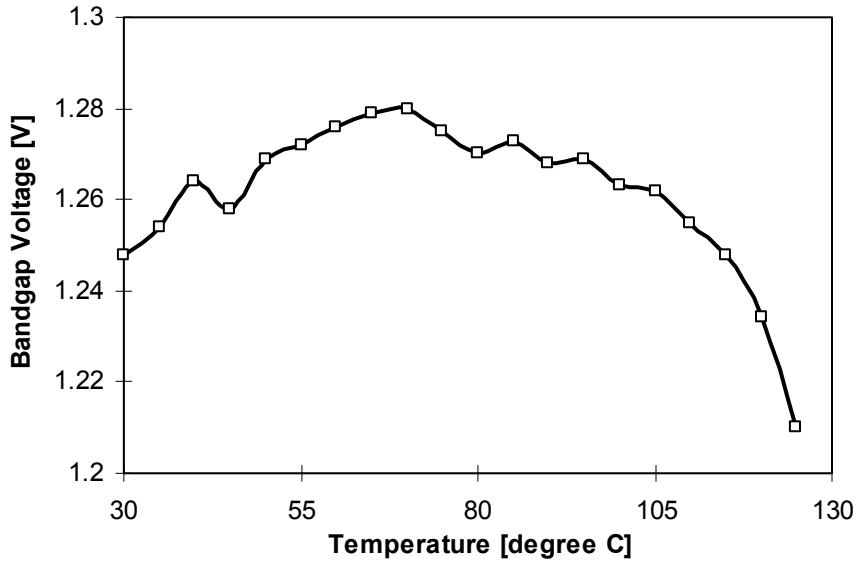


Figure 6.36. Measured temperature characteristics of the bandgap reference for an input supply of 1.4 V.

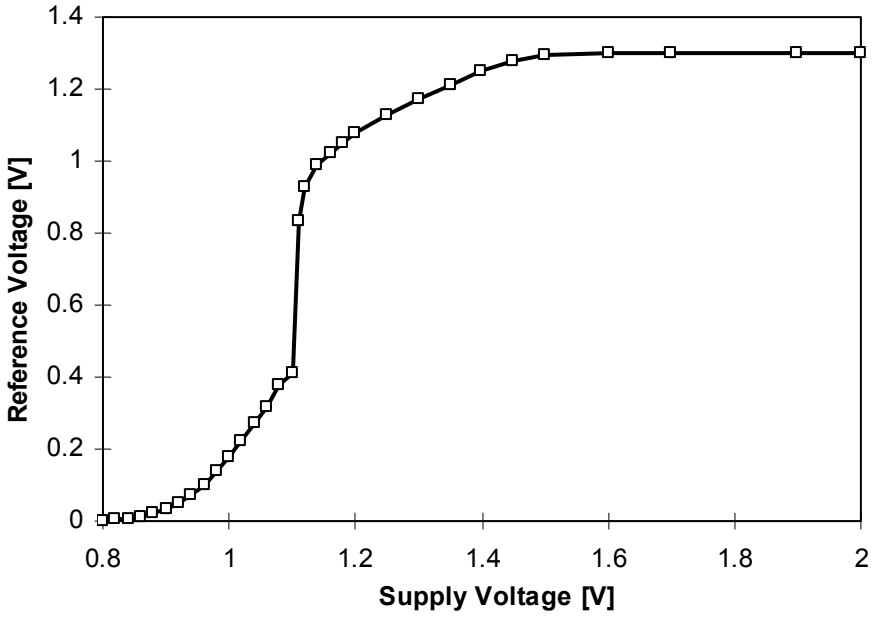


Figure 6.37. Measured start-up characteristic of the bandgap reference circuit.

Table 6.14. Simulation and measurement results summary of the bandgap reference.

Spec.	Unit	Target	Simulation	Worst-case Sim.	Exp.
V_{DD}	V	1.4 – 4.2	1.4 – 4.2	1.4 – 4.2	1.35 - 5
I_Q	μA	≤ 50	40 – 45	29.15 – 51.93	30 – 46
PD	mW	≤ 0.21	0.05 – 0.19	0.04 – 0.0218	0.039 – 0.27
V_{REF_1}	V	1.22 ± 0.05	1.224	1.186 – 1.255	1.213 –1.299
V_{REF_2}	V	1.0 ± 0.05	1.005	0.989 – 1.038	1.01 – 1.082
I_{REF}	μA	2.5	2.567	1.8 – 3.7	2.7 – 2.97

6.10 PA Dynamic Gate/Base Bias Circuit

6.10.1 Circuit Topology

The dynamic gate bias circuit for an MOS PA or base bias circuit for a BJT/HBT PA is essentially a voltage-to-current converter, the schematic of which is shown in Figure 6.38. The negative feedback loop consisting of the transconductance amplifier and transistor MP_{31} with resistor R_{BIAS} ensures the positive terminal of the amplifier equals to

its negative terminal voltage, V_{CON}. Therefore, the current through transistor MP_{31} is given by the ratio of the control voltage, V_{CON} and bias resistor, R_{BIAS}. MP_{31}'s current is mirrored through MP_{41} to generate the actual bias current for the PA. Since the control signal for the dynamic bias circuit is same as that is used for the buck-boost power supply, the amplifier needs to have an input common-mode range (ICMR) of 0.1 – 1 V.

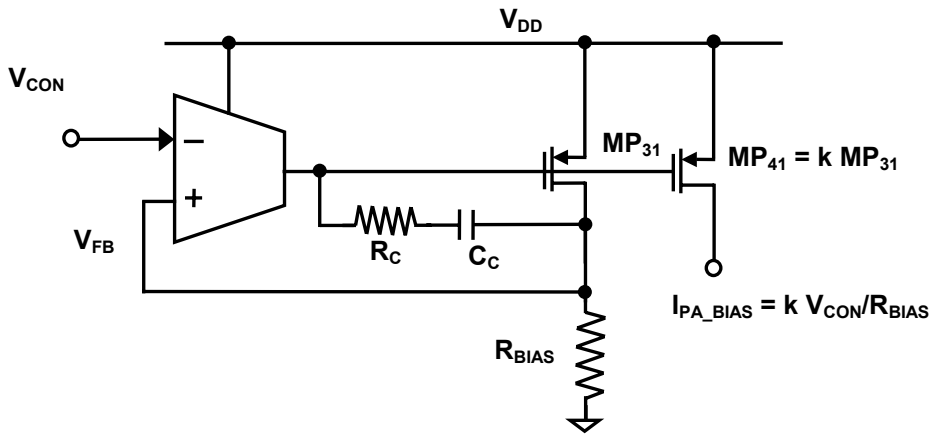


Figure 6.38. Schematic of the dynamic gate (base) bias circuit for MOS (BJT/HBT) RF PA.

6.10.2 Integrated Circuit Design

The critical element of the dynamic biasing circuit is the transconductance amplifier with close-to-rail ICMR. Figure 6.39 shows the dynamic bias circuit schematic, where the biasing and enabling circuit, and common-mode adaptation circuit are same as those described in the error amplifier op-amp design earlier in Section 6.4. MP_{21} and MP_{22} constitute the main amplifier differential pairs with MN_{21}, MN_{22}, MN_{23}, MN_{24}, MP_{24}, MN_{25} folded-mirror loads. The output drives the current mirrors MP_{31} and MP_{41} with R_{BIAS} forming the load resistance for the common source amplifier MP_{31}, whose output is feedback to the common-mode adaptation circuit. Capacitor C_C is used for Miller compensation while the function of R_C is to cancel the right-half plane (RHP) zero due to C_C. The transistor's aspect ratios and compensation component values of the design is presented in Table 6.15.

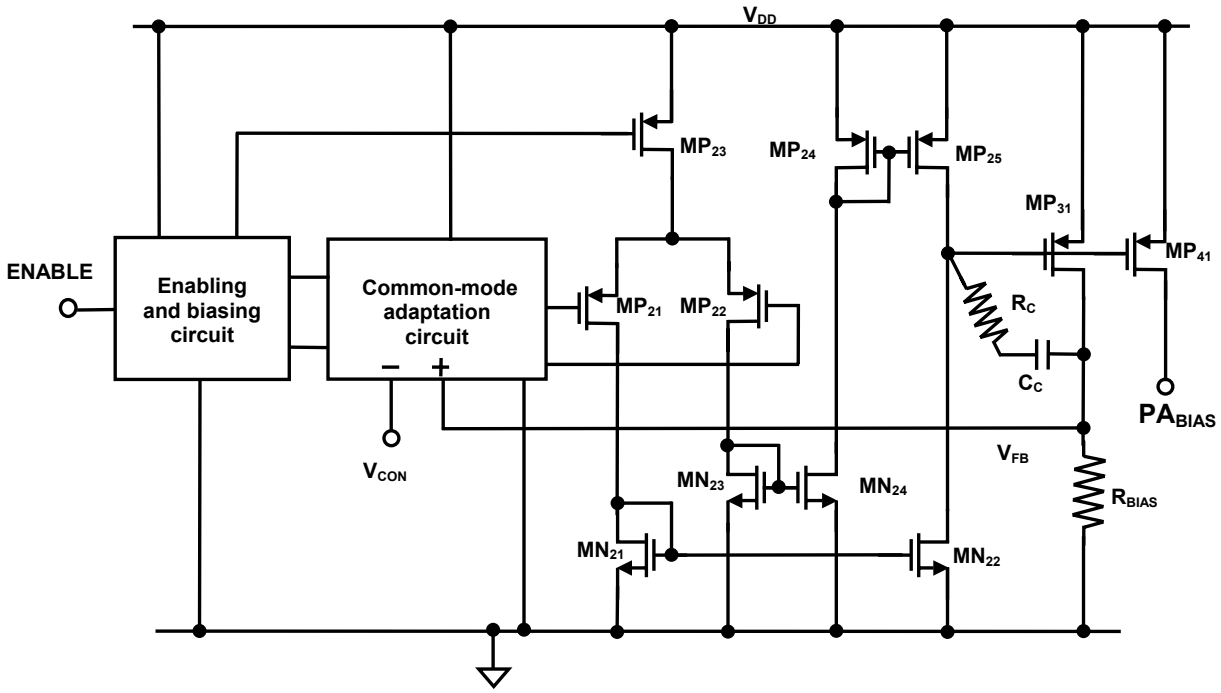


Figure 6.39. Schematic of the dynamic bias circuit.

Table 6.15. Component parameters of the dynamic bias circuit.

Sub-circuit	Component	Value
Transconductance amplifier stage	$(W/L)_{MP11, MP12}$	4 × (9 μm / 1.8 μm)
	$(W/L)_{MN11, MN12, MN13, MN14}$	4 × (4.5 μm / 3 μm)
	$(W/L)_{MP14, MP15}$	4 × (16 μm / 3 μm)
	$(W/L)_{MP13}$	12 × (6 μm / 3 μm)
Mirror transistors and compensation	$(W/L)_{MP31}$	72 μm / 1.2 μm
	$(W/L)_{MP41}$	50× (72 μm / 1.2 μm)
	C_C, R_C	10 pF, 25 kΩ
	R_{BIAS}	40 kΩ

6.10.3 Simulation and Measurement Results

Figure 6.40 shows the measured feedback node error voltage with the control signal for 1.4 and 5 V input supply voltage. The error voltage essentially consists of gain error due to finite open-loop dc gain and input offset voltage of the transconductance amplifier. As expected, for 5 V input supply, the common-mode adaptation circuit does not operate on the input signal for the control voltage range of interest, 0.1 – 1 V. Therefore, the only error is attributed to the amplifier's offset voltage. On the other hand, for a 1.4 V input supply, as control voltage increases beyond 200 mV, the common-mode adaptation circuit operates on the input signal. The mismatch on the level-shifting current mirrors and resistors combined with the main amplifier's input offset results in the overall error in the feedback voltage. For the control voltage range of interest, the error remains with in 10 mV as required by the system.

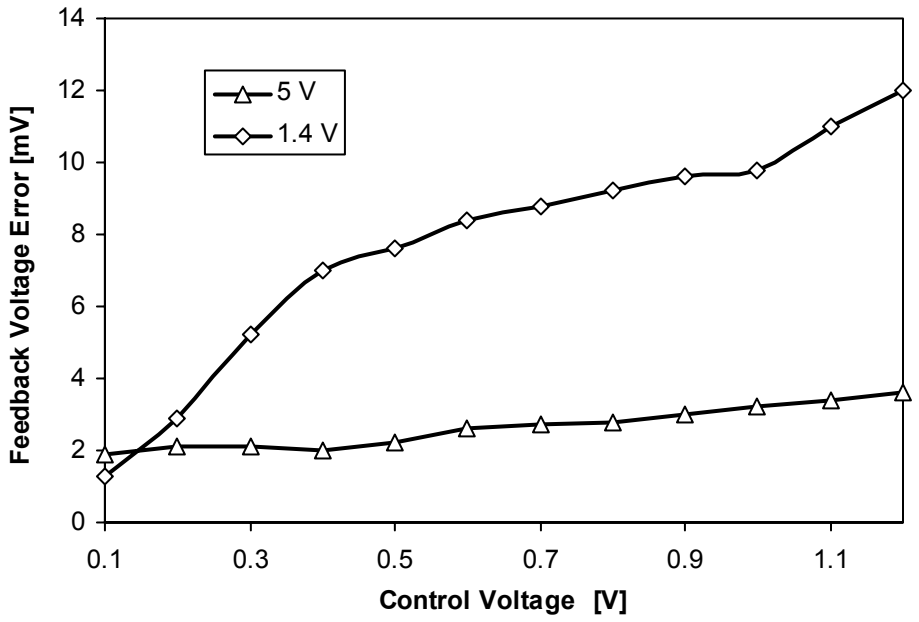


Figure 6.40. Measured feedback node error voltage compared to the control voltage of the dynamic bias circuit.

Figure 6.45 shows the PA bias current percent error with control voltage, which shows a maximum of 5 % at lower end of the control signal. A higher bias current error

essentially degrades the power efficiency, while a lower current may not be sufficient enough to meet the desired linearity level. For optimal performance, accurate bias current is desired, which however requires amplifier's offset voltage compensation and trimming of current mirrors that increased circuit complexity.

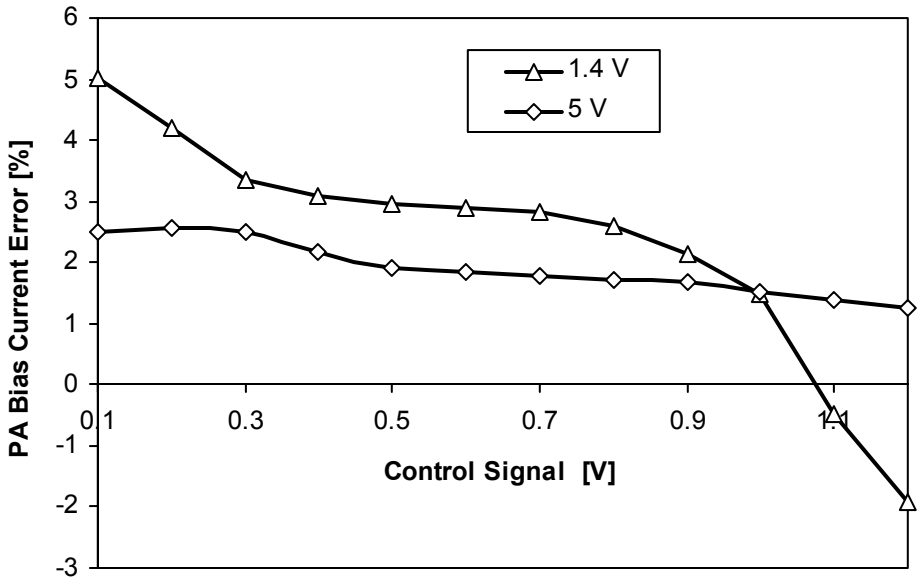


Figure 6.45. Measured accuracy of the dynamic bias circuit's output current.

Figure 6.46 shows the 0.1 – 1 V control-step transient response of the dynamic bias circuit while monitoring its feedback node voltage, which is also the voltage impressed across the bias resistor. The feedback node voltage closely follows the control step signal without any ringing or oscillation thereby ensuring the stability of the feedback loop. A summary of simulation and measurement results of the PA dynamic bias circuit is offered in Table 6.16, which essentially demonstrated the experimental results match well the simulated values. The PA bias current, however, deviates from the specified values because of channel length modulation and transconductance amplifier's offset voltage at the higher and lower end of the supply voltage, respectively.

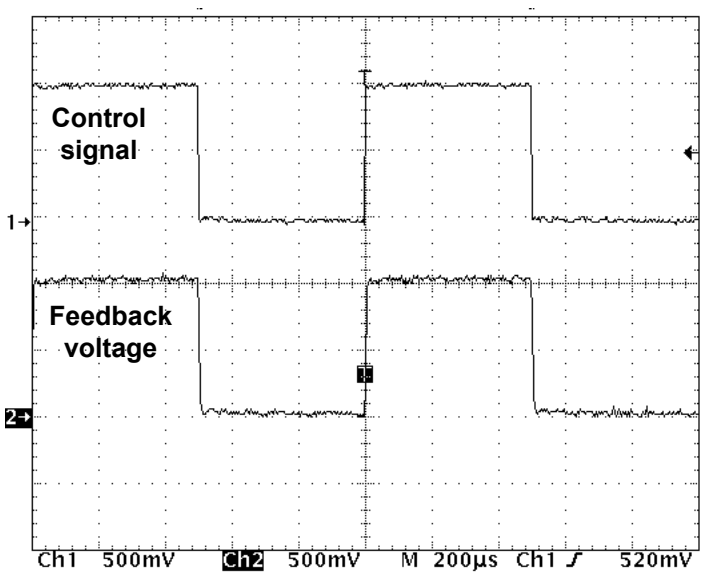


Figure 6.42. Measured 0.1 – 1 V control-step transient response.

Figure 6.16. Summary of simulation and experimental results of the PA dynamic bias generation circuit.

Specification	Unit	Target	Sim.	Worst-case sim	Exp.
Supply voltage	V	1.4 – 4.2	1.4 – 4.2	1.4 – 4.2	1.4 – 5
Control voltage	V	0.1 – 1	0.1 - 1	0.1 - 1	0.1 –1.2
Mirror current	mA	0.125 – 1.25	0.114 – 1.23	0.113 – 1.28	0.116-1.48
Power dissipation	mW	≤ 0.1 – 5	0.16 – 5.17	0.16 – 5.38	CT
Control step response	µs	≤ 20	1.4 – 2.3	1.2 – 2.3	≤ 5

6.11 Summary

In this chapter, development, design and experimental results of various circuit building blocks of the dynamically adaptive buck-boost power supply and dynamic gate (base) bias circuit of the RF PA is presented. Specifications for each circuit are derived from the system requirements by following a top-down approach. The limitations of low supply voltage on the use of bootstrap gate drive circuits and N-well process technology

constraints on availability of body diode for an integrated solution requires the use of a high-side PMOS switch, even at the expense of large die area. While simple inverter-based gate drive circuits are used for driving all the power switches, the synchronous boost PMOS drive is provided from the output.

A 0.1 – 1 V ICMR, close-to-rail, error amplifier op-amp is designed and experimentally verified with higher than 60 dB dc gain over the 1.4 – 4.2 V supply voltage range. Similarly, 0.9 – 1.3 V ICMR PWM comparator and -50 – 150 mV ICMR PFM comparator designs with 100 nsec propagation delay for 10 mV of overdrive voltage have been experimentally verified. Other circuit blocks, e.g., triangular wave generator and adaptive on-time circuits are also experimentally verified for the PWM and PFM controller, respectively. The low voltage bandgap circuit designed exhibits reference voltage of 1.23 – 1.29 V and current reference of 2.7 – 2.9 μA over 1.4 – 5 V input supply, rendering its suitability for the reference inputs for the triangular waveform generator and biasing of other circuit blocks. The experimental results of PA dynamic gate (base) bias circuit with a trimmed resistor yielded 5 % accuracy of the desired current over its control voltage range. The circuit blocks are now assembled into an integrated system, the details of which is described in the next chapter.

CHAPTER VII

INTEGRATED BUCK-BOOST SUPPLY AND EFFICIENT WCDMA RF PA SYSTEM

This chapter presents the assembly of various circuit building blocks described in Chapter 6 into an integrated system. Simulation results illustrating full-chip functionality of the system are described followed by floor planning and system layout considerations. Experimental performance of the buck-boost integrated supply is then described. Subsequently, the power supply and bias control IC is used to realize a high efficiency 1.96 GHz WCDMA RF PA, and the performance of the PA system is presented.

7.1 Integrated Buck-Boost Supply

The dual-mode, dynamic, noninverting, buck-boost power supply and PA gate bias circuit are assembled into one system, the schematic of which is shown in Figure 7.1. Apart from the blocks described in Chapter 6, a bias generator and a unity-gain buffer are also incorporated in the system implementation. The bias generator essentially takes an input reference current from the bandgap circuit and generates bias currents for various analog circuit blocks, e.g., error-amplifier, triangular wave generator, PWM comparators, etc. The unity-gain buffer provides isolation between the control signal input and the error amplifier input while ascertaining a minimum delay for fast control steps. The architecture of the unity-gain buffer is similar to the error amplifier op-amp with close-to-rail input common-mode range (ICMR). Miller compensation scheme is used to stabilize the amplifier for unity-gain.

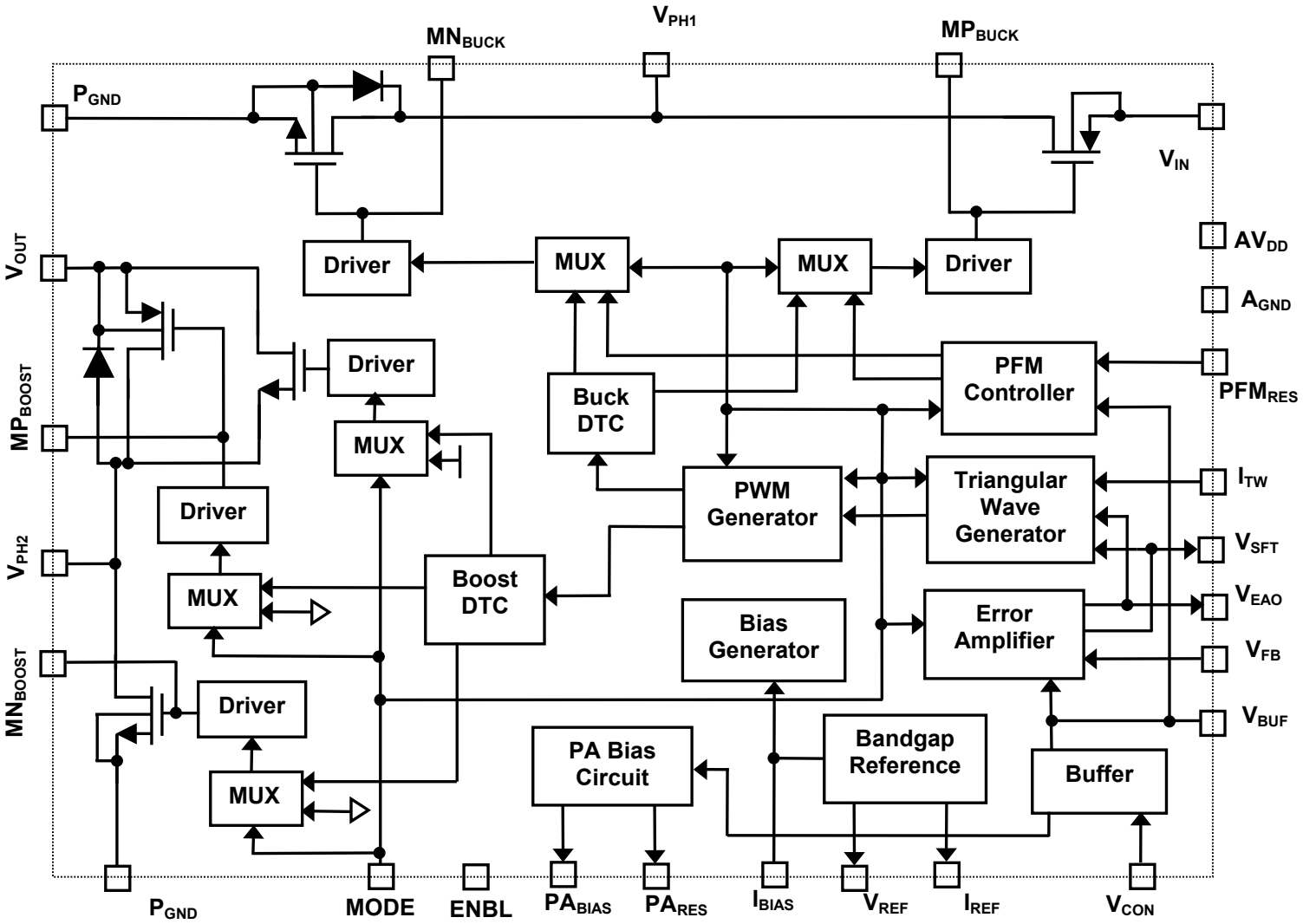


Figure 7.1. Integrated dynamic buck-boost converter and PA gate-bias system.

The full-chip buck-boost converter was verified for functionality and performance before the circuit was laid out and submitted for fabrication. Figure 7.2 shows the buck-boost converter system indicating the integrated circuit and discrete external components. Except the power inductor, output capacitor, input bulk capacitor, slow-start charging capacitor and frequency compensation network, all other blocks are integrated onto one chip.

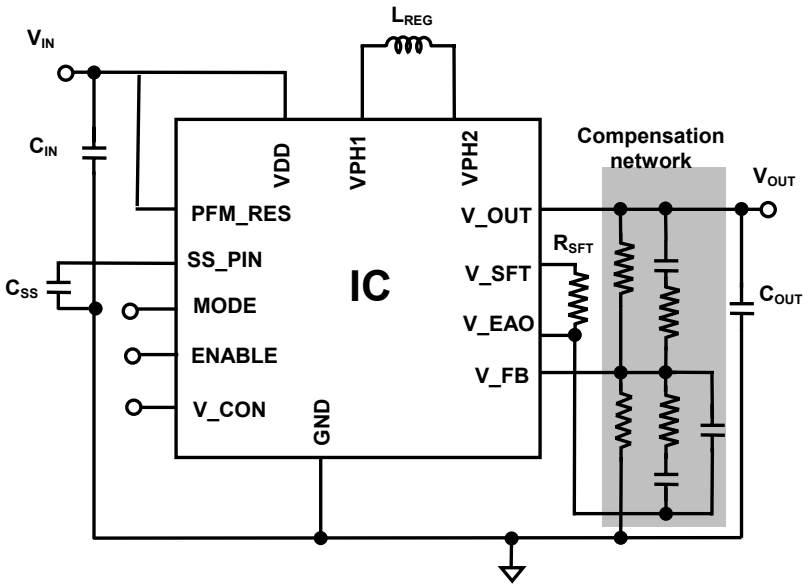


Figure 7.2. Schematic of the chip-level integrated system with its respective external passive components.

As with the individual circuit blocks, the transistor-level full-chip converter circuit is simulated for key functionalities using Cadence Spectre simulation environment. Figure 7.3 shows a representative plot of simulation results with key waveforms, e.g., inductor current, output voltage illustrating the converter's functionality in PWM mode. The output ripple voltage is within 18 mV when a 5 V steady-state output voltage is generated from a 1.5 V input supply with a load resistance of 15 Ω. Figure 7.4 depicts the worst-case control step response, which is simulated with a 0.9 – 1 V step signal at the control input of the converter while monitoring its output voltage and inductor current. The transient response plot illustrates the converter's stability under the

extreme duty cycle environment for which the compensation circuitry is designed. The converter's output voltage changes from 4.5 to 5 V within 200 μsec with a 1.5 V supply.

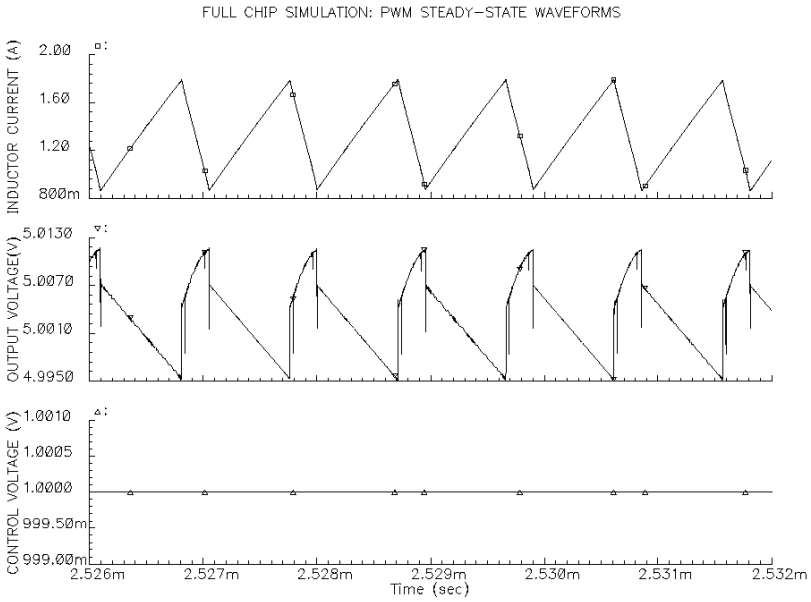


Figure 7.3. Full chip PWM mode simulation results - Steady-state waveforms (V_{IN} = 1.5 V, V_{OUT} = 5 V).

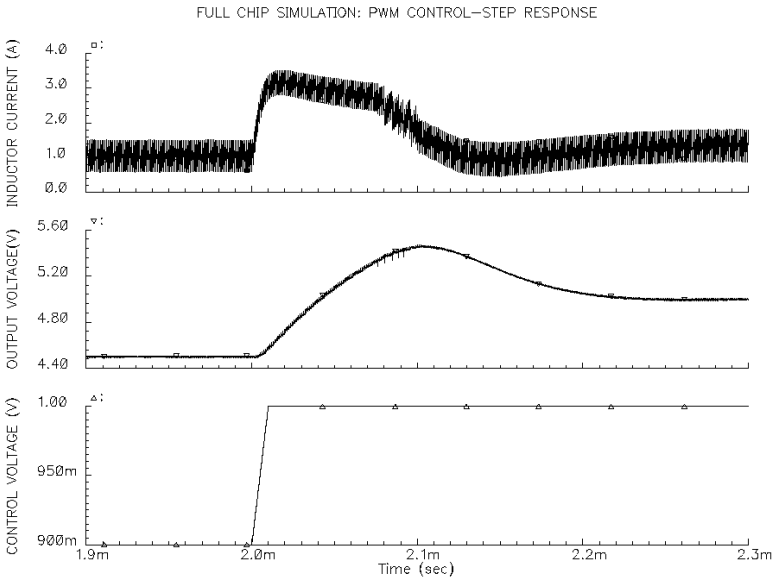


Figure 7.4. Full chip PWM mode simulation result: Transient control-step response.

Figure 7.5 shows the representative steady-state waveform illustrating the functionality of the converter operating in PFM control with an output voltage of 0.5 V having a peak-to-peak ripple of 13 mV generated from an input supply of 3.0 V. The output ripple voltage in PFM mode is critical to minimize signal distortion, especially when the transmitted power is low. Since the output voltage and loading conditions of the converter in PFM mode remains at a constant level, it is not simulated for a transient control-step response.

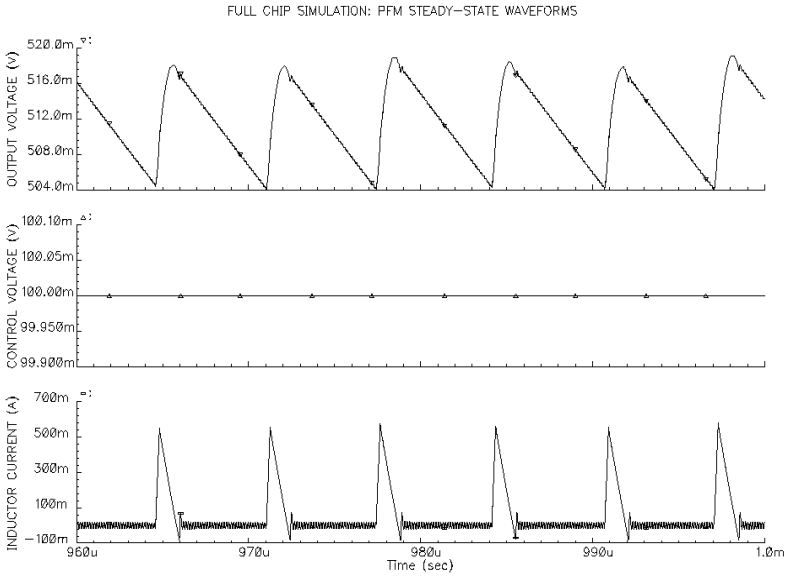


Figure 7.5. Full chip PFM mode simulation result: Steady-state waveforms.

7.2 Chip Layout

Switching regulators with power MOSFETs integrated with other analog blocks in a standard N-well CMOS process must be carefully laid out with sufficient substrate and well contacts to prevent latch-up and mitigate noise coupling using guard rings whenever necessary. The floor plan of the dynamically adaptive buck-boost converter and gate (base) bias circuit for the PA is shown in Figure 7.6. The power transistors and gate drive circuits are placed on two sides of the die to minimize their switching noise on analog circuit blocks. Guard rings in the form of N^+ and P^+ diffusions are connected to

the supply voltage and ground, respectively, isolating the switching area from the non-switching components on the die.

The bandgap reference circuit, being the most sensitive noise prone block, is placed at one corner of the die along with other circuit block, e.g., error amplifier, buffer, bias generator and the PA bias circuit. Other circuit building blocks of the controller, e.g., triangular waveform generator, PWM comparators are separated from the sensitive blocks using guard rings.

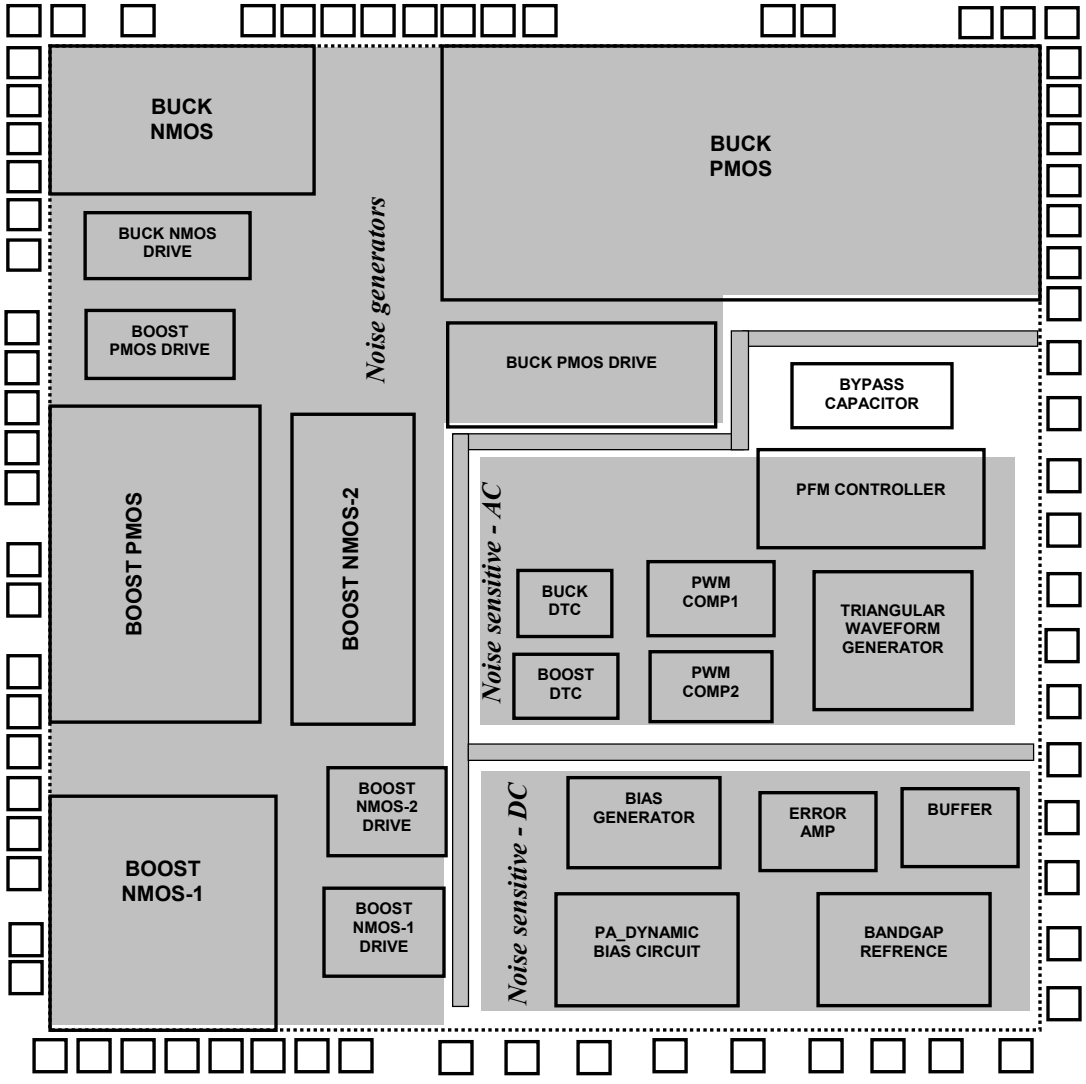


Figure 7.6. Integrated system floor plan.

The layout of a power transistor, due to its sheer size and instantaneous body diode conduction during the dead time, is laid out with integrated back-gate contacts [98]. Figure 7.7 illustrates the concept of integrated P^+ diffusion contact inside the N^+ source area of an NMOS transistor. Although the effective source area is more than the drain area with the integrated back-gate contact, still it is more compact with respect to laying out two separate fingers and inserting a column of back-gate contact in between them. Similarly, in a PMOS device patches of N^+ diffusion are created inside the P^+ source area to create back-gate contact.

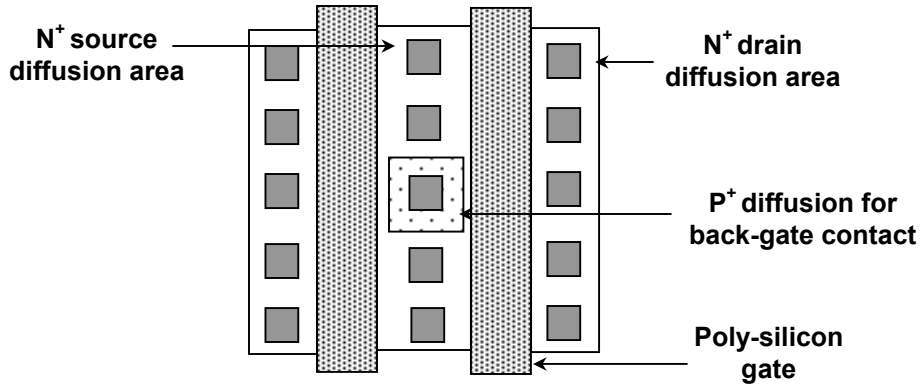


Figure 7.7. Illustration of integrated back-gate contact of an NMOS transistor.

Critical devices, e.g., input differential pairs and their load mirrors are laid out in cross-coupled common-centroid geometry with dummy devices to minimize mismatch related errors, thereby achieve better input-referred off-set performance. Realizing the accuracy requirements and critical nature of the bandgap circuit, all of its components in were laid out in cross-coupled, common centroid geometry.

7.3 Experimental Results of the Integrated System

Figure 7.8 shows the die photograph of the integrated system fabricated using AMI's 0.5 μm CMOS process technology through MOSIS. The dimension of the chip is 3.8 mm × 4.2 mm, out of which the converter's power switches consume approximately 60-70 % of the total chip area. Multiple pads and bond wires are used for input, output,

phase nodes and ground paths of the chip to support the required current. A LCC 52 pin ceramic package was selected for the die to have access to various nodes in side the chip for testability requirements.

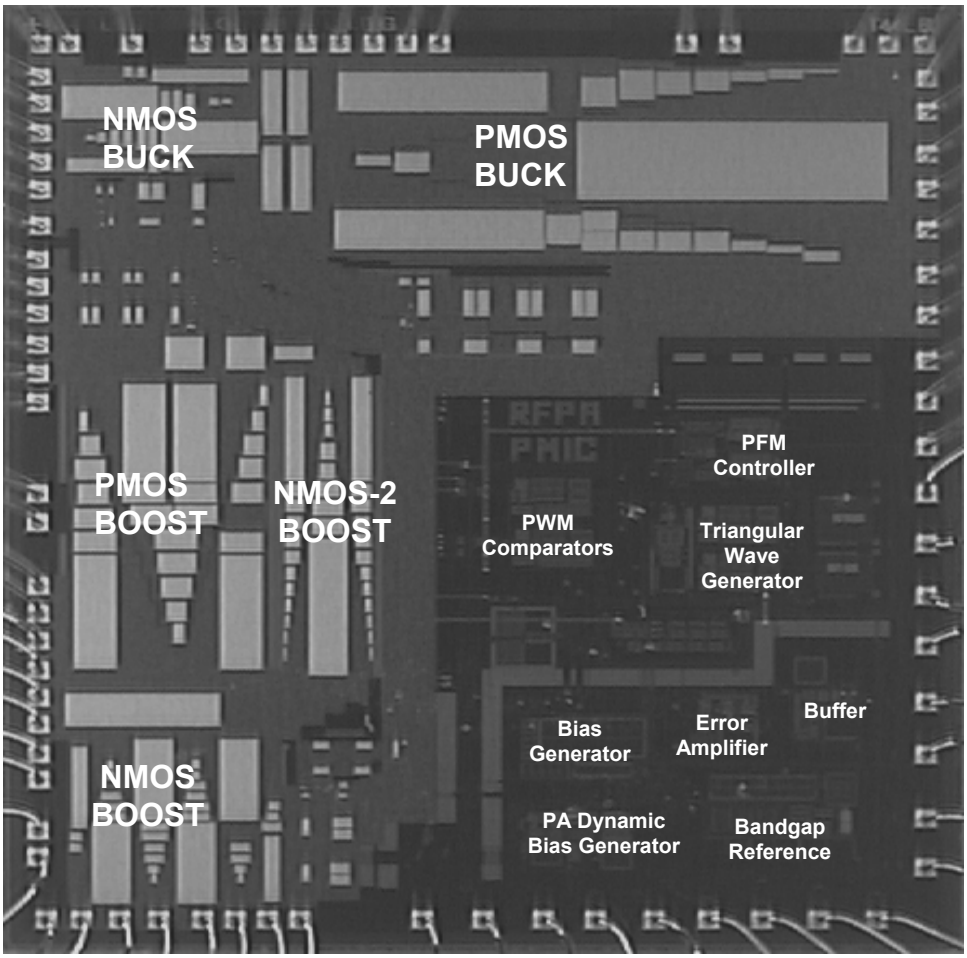


Figure 7.8. Die plot of the buck-boost converter and PA dynamic gate bias control chip.

Figure 7.9 shows the pin diagram of the chip with functionality of each pin is described in Table 7.1. Multiple pins, with each pin being connected to two pads in the die, are allocated to the nodes in large current carrying paths to minimize unwanted series resistance and inductance.

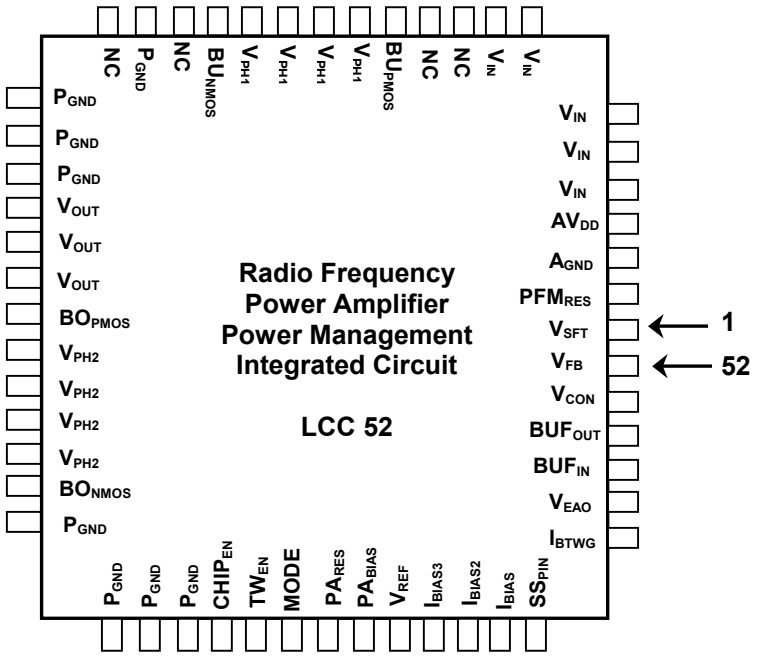


Figure 7.9. Pin diagram of the buck-boost converter and bias control chip.

Table 7.1. Pin description of the buck-boost converter and bias control chip.

Pin	Description	Pin	Description
1	Shifted error amp output	39	PWM/PFM mode
2	PFM mode resistor trim	40	PA Bias resistor
3	Analog ground	41	PA bias current
4	Analog supply	42	Bandgap reference voltage
5-9	Input supply	43	Reference current 1
12	Buck PMOS gate	44	Reference current 2
13-16	V_{PH1} node	45	Input bias current
17	Buck NMOS gate	46	Slow start
19, 21-23	Power ground	47	Triangular wave generator bias
24-26	Output node	48	Error amplifier output
27	Boost PMOS gate	49	Buffer input
28-31	V_{PH1} node	50	Buffer output
32	Boost NMOS gate	51	Input control signal
33-36	Power ground	52	Feedback Node
37	Chip enable		
38	Triangular wave enable		

The IC was soldered onto a printed circuit board (PCB) along with the external passive components. Appropriate guidelines, e.g., minimizing the length of power traces, proper ground connections [99]-[100], were followed for designing the PCB to minimize the effect of switching noise on the converter's operation. Experimental results of the integrated buck-boost supply operating in PFM and PWM mode, and relevant discussions are offered in the following subsections.

7.3.1 PFM Mode Results

Figure 7.10 presents the experimental gate drives, V_{PH1} node and inductor current waveforms of the buck-boost power supply IC operating in PFM mode with discontinuous conduction mode (DCM) operation. Figure 7.11 shows a close-in plot of the gate drive signals and inductor current illustrating turning off of the synchronous NMOS transistor when inductor current starts to change its direction from a positive to a negative value. Both these plots are presented to illustrate the converter's functionality.

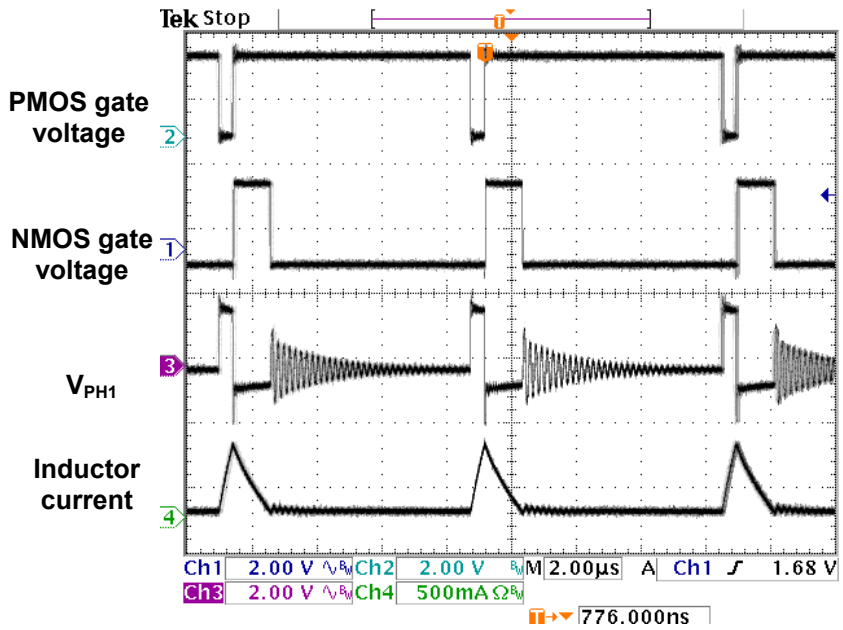


Figure 7.10. Experimental buck-boost converter IC PFM mode functionality: Power transistors' gate voltage, V_{PH1} node, and inductor current waveforms.

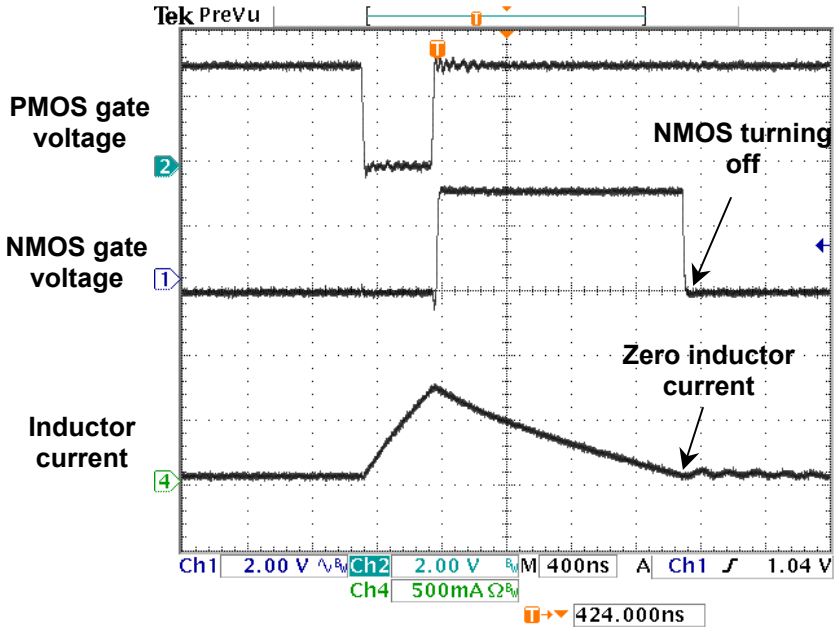


Figure 7.11. Experimental buck-boost converter IC results: Synchronous NMOS turning off when the inductor current becomes zero.

Figure 7.12 shows a representative experimental waveform of the PFM converter with gate drive and output peak-to-peak ripple waveform from an input supply of 3.2 V with the desired 0.5 V average steady-state voltage. The converter's ripple voltage remains with in the specification of 20 mV, as evident from the plot. After the converter IC's functionality is verified, the adaptive on time scheme is compared with a fixed on time system, the variation of which is shown in Figure 7.13.

Figure 7.14 compares the peak-to-peak output ripple voltage of the converter in fixed and adaptive on time control. For a given on time, as the supply voltage increases the peak inductor current also increase. Therefore, the energy transferred from the input source to the output capacitor during the on time increases resulting in a higher peak-to-peak output ripple. Figure 7.15 shows the average output voltage of the converter operating in fixed and adaptive on time control schemes. Since the PFM controller is operated based on the lower value of the output voltage in a given switching period, a higher output ripple essentially results in a larger average output voltage in fixed on time control as the input supply voltage is increased.

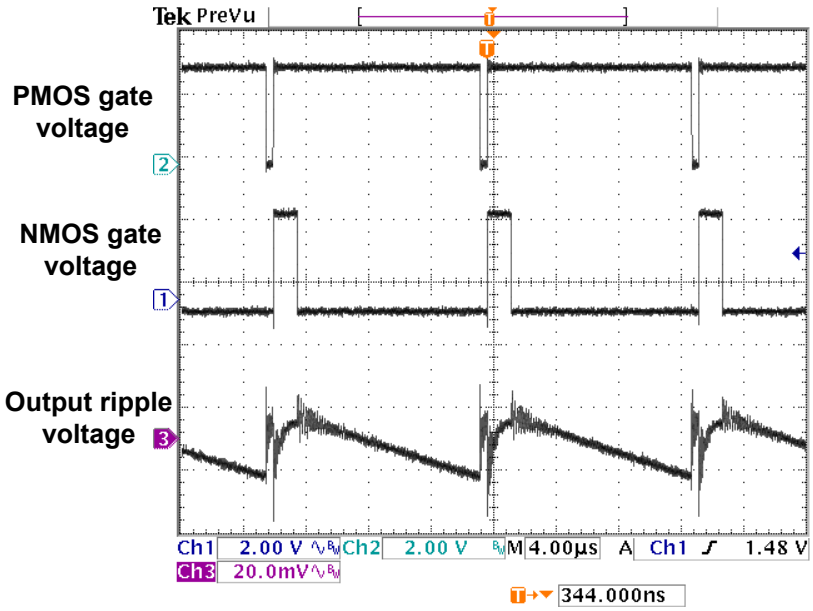


Figure 7.12. Experimental buck-boost converter IC results: Gate drive and output ripple voltage waveforms.

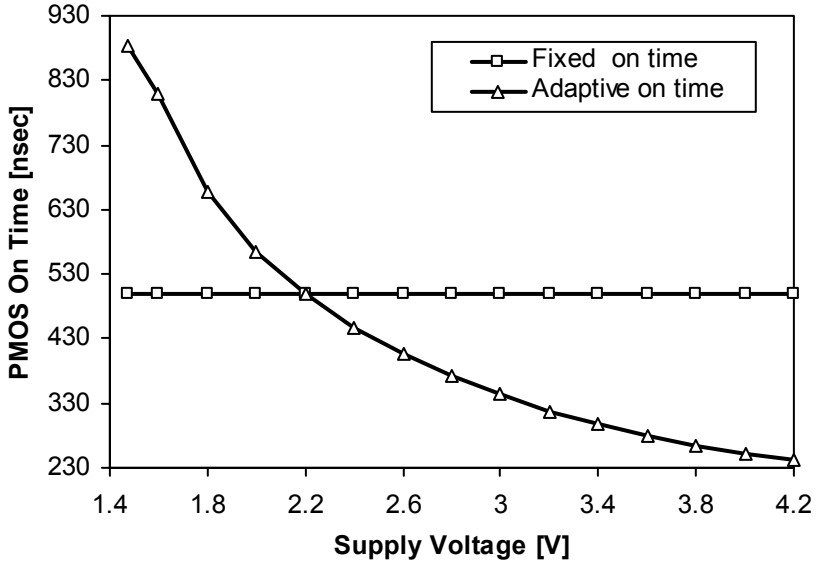


Figure 7.13. Fixed and adaptive on time of the experimental buck-boost converter IC in PFM mode.

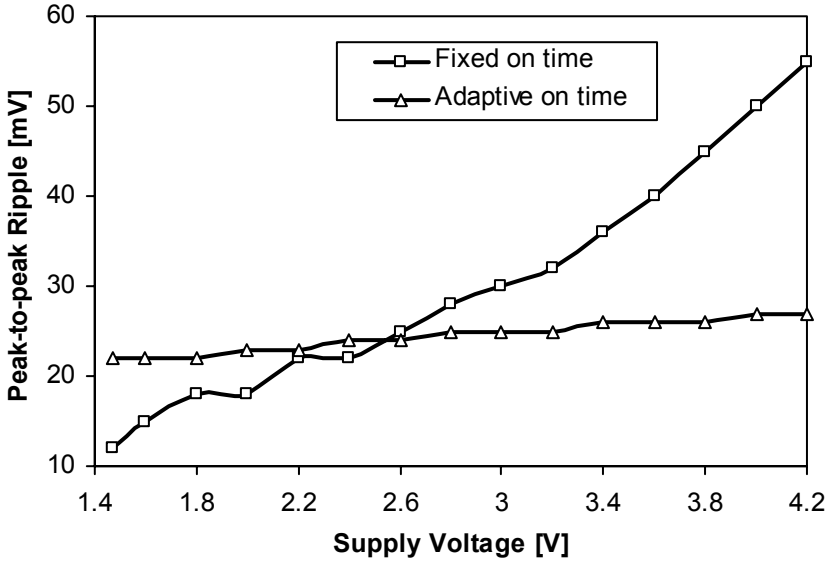


Figure 7.14. Experimental peak-to-peak output voltage ripple of the buck-boost converter IC for fixed and adaptive on time PFM mode control.

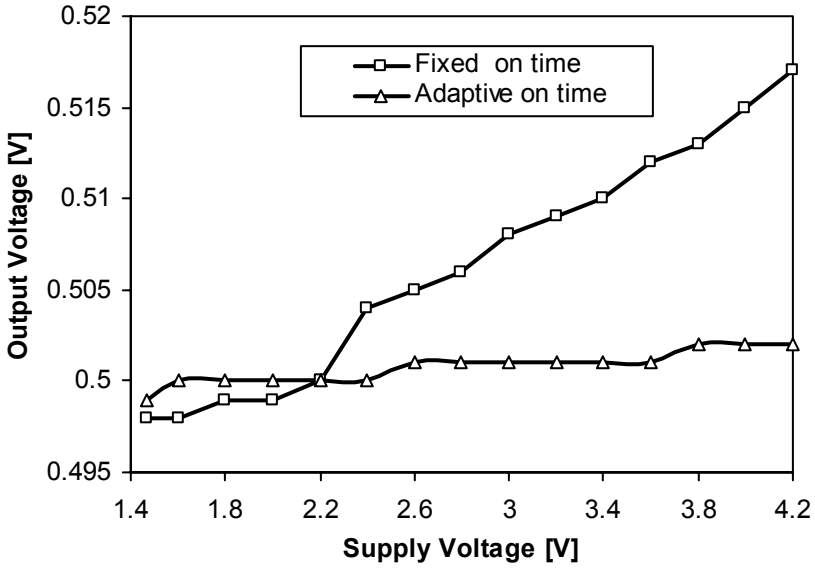


Figure 7.15. Experimental average output voltage of the buck-boost converter IC for fixed and adaptive on time PFM mode control.

Figure 7.16 shows the variation of the converter's switching frequency in fixed and adaptive on time controls. With an increase in supply voltage, a higher energy is transferred from the input to the output due to larger peak inductor current in a fixed on time control. Hence, the load current also takes longer time to discharge the output capacitor. Therefore, the switching frequency of the converter decreases to maintain the output voltage regulation. Alternatively, with adaptive on time control, the energy transferred to the output capacitor remains almost identical in every switching cycle irrespective of the input supply voltage. Therefore, the converter is turned on in equal time intervals resulting in an approximately constant switching frequency over supply voltage range. When the input supply goes below 1.5 V having an output voltage of 0.5 V, the PMOS transmission gate transistors remains off and the NMOS transistor's gate drive approaches its threshold voltage level. During this period, the PMOS body diode conducts current from input to the output, resulting in higher power loss, which means the power transistors are switched more frequently to maintain regulation resulting in a higher switching frequency.

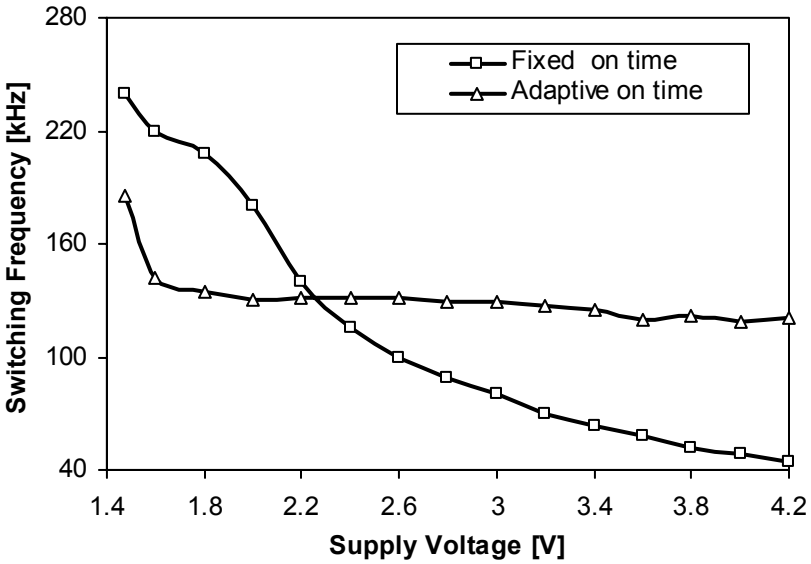


Figure 7.16. Measured switching frequency of the buck-boost converter IC for fixed and adaptive on time PFM mode control.

Figure 7.17 shows the measured efficiency characteristic of the buck-boost converter IC operating in PFM with discontinuous-conduction mode (DCM). For adaptive on time control, the efficiency degradation at higher supply voltage is attributed to higher switching losses, since power transistor's and drive circuit's gate capacitances are charged to and discharged from a higher voltage. For a lower supply voltage the efficiency improves because of a reduced switching losses. However, when the gate-drive for the transmission-gate NMOS device gets smaller, its on resistance becomes larger, thereby incurring higher conduction loss. As the supply voltage is decreased even further, the body diode of the boost PMOS transistor conducts, which further degrades the efficiency. The fixed on time scheme yields a lower efficiency at higher supply voltage due to a larger peak inductor current, consequently yielding a higher conduction loss. On the contrary, the efficiency loss at lower supply voltage compared to the adaptive on time control is attributed to a higher switching frequency of the converter.

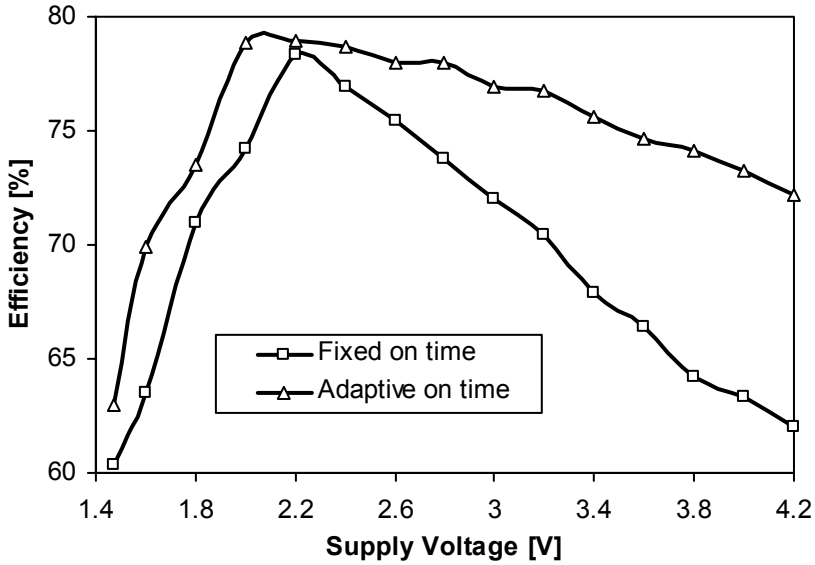


Figure 7.17. Measured efficiency characteristics of the buck-boost converter IC in fixed and adaptive on time PFM control.

Figure 7.18 shows the measured load transient characteristic of the PFM mode converter. As the load is increased from 50 to 300 mA, the average output voltage drops approximately 15 mV for a nominal output voltage of 500 mV due to load regulation. The output voltage remaining unperturbed after the load transient illustrates the converter's feedback loop stability.

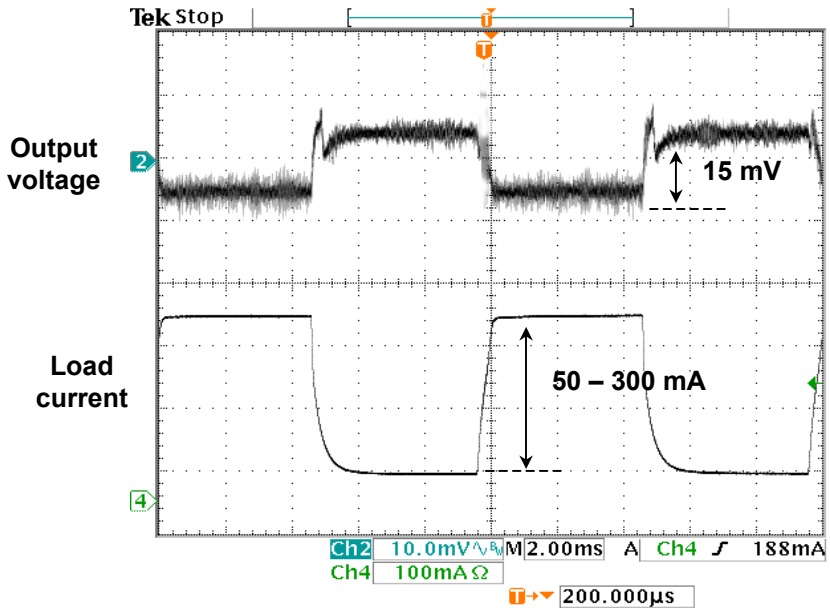


Figure 7.18. Experimental load-step response of the PFM-mode converter with adaptive on time control.

Experimental results of the converter in PFM mode operating are compared with the targeted values in Table 7.2, which shows that the measured results match reasonably well with the targeted and simulated values. The measured efficiency values are lower than the simulated values, since the parasitic resistances were not modeled in the simulation. The peak-to-peak ripple voltage is slightly higher than the simulated values, because the adaptive on-time circuit generated a larger on time across supply voltage variation when compared to the simulated values.

Table 7.2. Experimental buck-boost converter's PFM mode results summary.

Specification	Unit	Target	Sim.	Expt.
V_{IN} = 1.4 V (1.45 V Expt)				
Output voltage	V	0.5	0.515	0.499
Peak-to-peak ripple	mV	≤ 20	20	22
Efficiency	%	≥ 80	54	63
V_{IN} = 3.0 V				
Output voltage	V	0.5	0.515	0.501
Peak-to-peak ripple	mV	≤ 20	22	25
Efficiency	%	≥ 80	83.56	76
V_{IN} = 4.2 V				
Output voltage	V	0.5	0.512	0.502
Peak-to-peak ripple	mV	≤ 20	25	27
Efficiency	%	≥ 80	81.52	72.255

7.3.2 PWM Mode

The full-chip integrated converter was tested functional for buck operation. However, due to a missing metal layer in the layout of the boost stage PMOS transistor's poly gate the actual gate-drive signals of the boost stage NMOS transistor and synchronous PMOS transistor overlapped with each other leading to shoot-through, and consequently damaging the power switches. Therefore, the buck-boost and boost mode operation of the integrated system was experimentally verified with a two-chip solution, a controller chip and another chip with integrated power transistors. The dead-time control for the boost stage was realized using discrete logic gates in a PCB, while all other blocks are used from the two designed test chips.

Figure 7.19 shows the V_{PH1}, V_{PH2} node voltages and inductor current waveforms the experimental PWM controlled converter operating in the intermediate buck-boost region of operation. Figure 7.20 shows the output ripple and inductor current waveforms of the converter operating in the boost mode. Both these figures are presented to illustrate the functionality of the buck-boost converter.

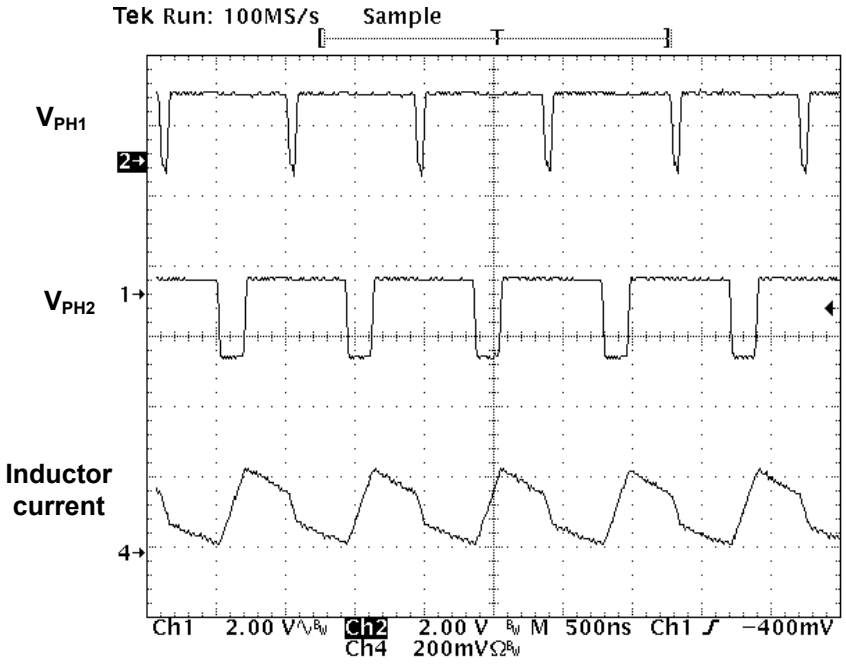


Figure 7.19. Experimental buck-boost converter waveforms in buck-boost mode: V_{PH1}, V_{PH2}, and inductor current.

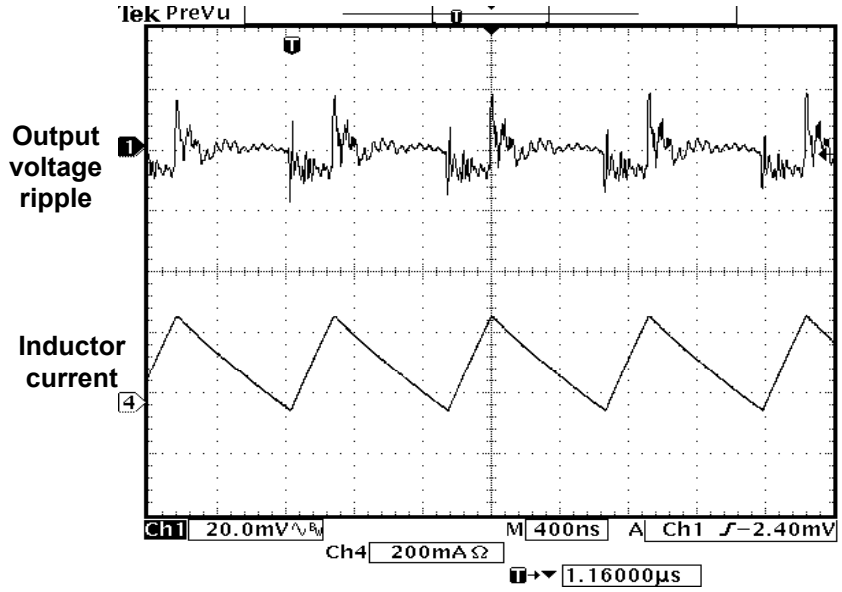


Figure 7.20. Experimental buck-boost converter waveforms in boost mode: output ripple and inductor current.

Figure 7.21 illustrates the variation of percentage error in the output voltage as the dynamic converter's output voltage varies. The absolute value of error voltage does not change considerably with output voltage, which is reflected as a decreasing percentage error with higher output voltage. Most part of the error is due to the error amplifier's offset voltage, while other factors, e.g., finite loop gain of the control loop, and the parasitic resistances in the switching-current-flowing path contribute to the error voltage.

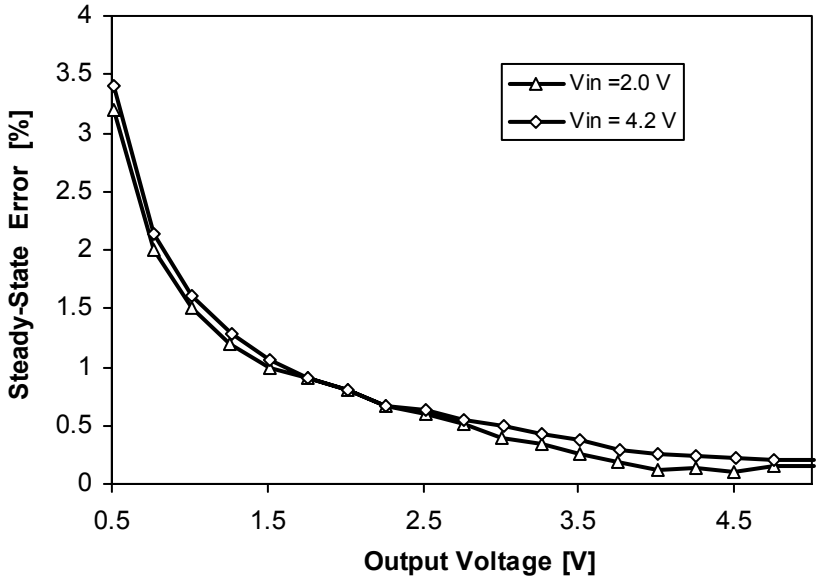


Figure 7.21. Percentage output voltage error of the integrated dynamic buck-boost converter (V_{OUT} = 2.5 V, R_{LOAD} = 15 Ω).

Figure 7.22 illustrates the peak-to-peak ripple voltage variation of the integrated dynamic converter with variation in its output voltage. The ripple in the output is as a result of peak-to-peak ripple current flowing through the ESR and ESL of the output capacitor. For a constant load current, although the average inductor current is constant, ripple inductor current increases for higher output voltages (larger duty cycles). For resistive loads, with higher output voltage the load current increases, leading to higher peak-to-peak ripple currents, and consequently higher ripple voltage.

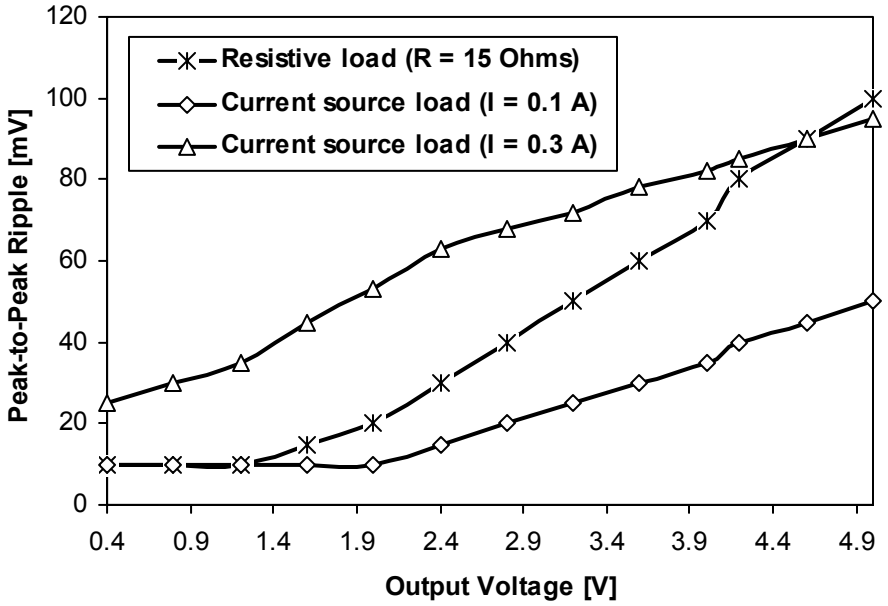
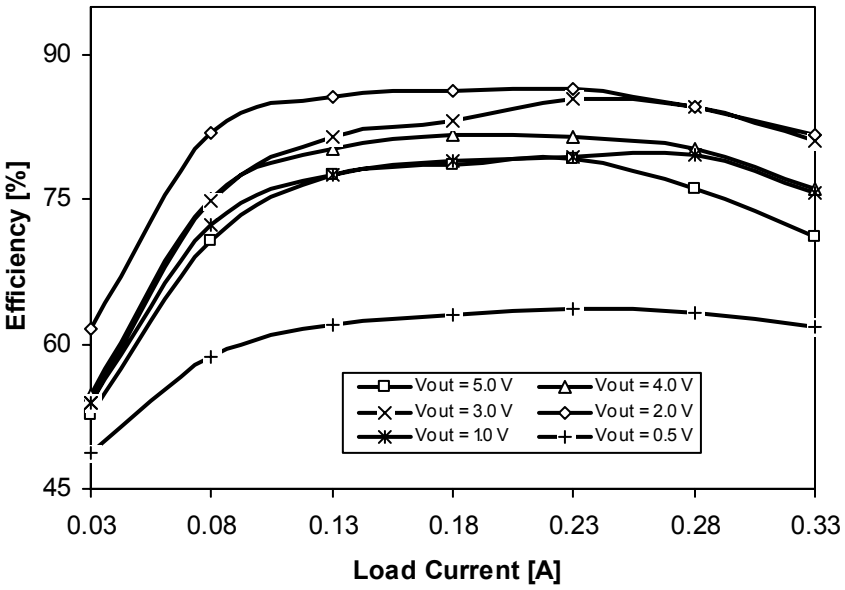
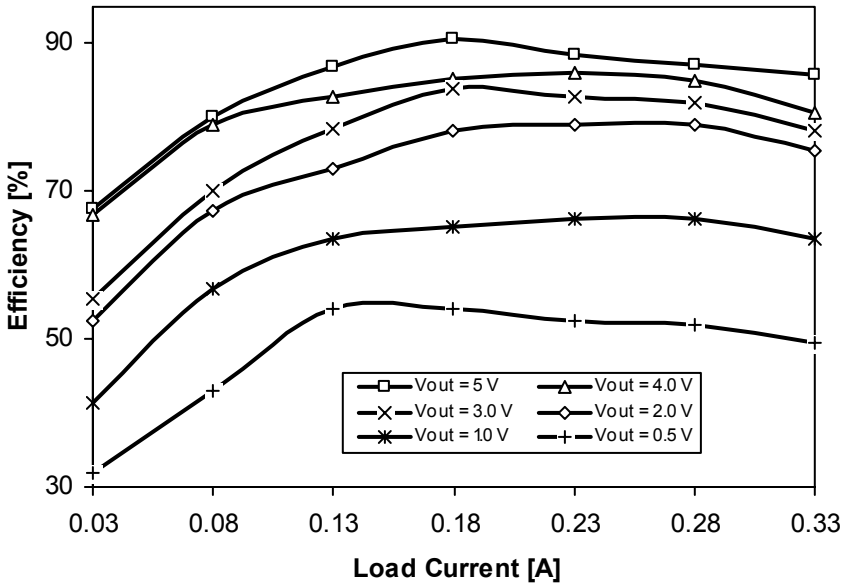


Figure 7.22. Peak-to-peak ripple voltage of the integrated dynamic buck-boost converter's output.

Efficiency curves of the converter at various load currents and different output voltages for input supplies of 2.5 and 4.2 V considering the two extremes of Li-ion battery operation (2.7 – 4.2 V) are presented in Figure 7.23. With a 2.5 V input supply, as the output voltage increase the controller adjusts the converter's operation from buck to buck-boost and ultimately to boost mode. For a constant load, with the output voltage increasing from 0.5 to 1 V output power also increases, while the power losses are not significantly altered, thereby yielding a higher efficiency. However, as the converter transits from buck-boost to boost mode while output voltage changing from (2 to 3 V), the buck-stage PMOS switch remains completely on carrying the total input current that increases with a higher output voltage, subsequently yielding higher power loss and degrading the converter's efficiency. Unlike 2.5 V input supply voltage, the converter's efficiency monotonically increases with higher output voltage for 4.2 V input supply.



(a)



(b)

Figure 7.23. Measured efficiency characteristic of the integrated buck-boost converter (a) V_{IN} = 2.5 V and (b) V_{IN} = 4.2 V.

Figure 7.24 shows the variation of output voltage of the integrated converter with changing load current for different input supply voltages. For a given output voltage (2.5 V in this case) with a constant load current, a higher supply translates to lower input current subsequently generating a smaller voltage drop due to the parasitic resistances in the current carrying path. With a 1.4 V input supply, as the load current is increased from 30 to 330 mA, the converter's output voltage (2.5 V nominal) shows a 40 mV drop, which translates to a load regulation performance of 1.6 %. For the maximum load current of 330 mA, the output voltage changes by 38 mV as the input supply is varied from 4.2 to 1.4 V translating to a line regulation performance of 1.36 %.

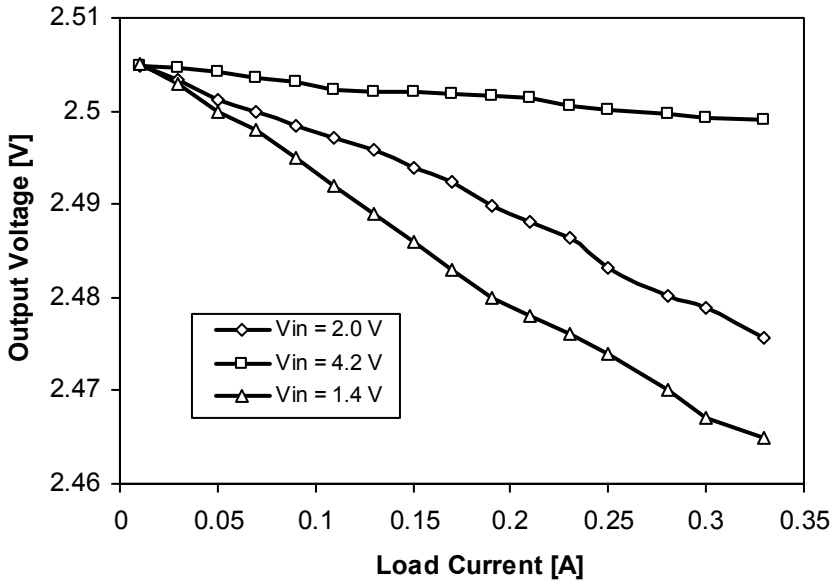


Figure 7.24. Measured load (LDR) and line regulation (LNR) characteristics of the integrated buck-boost converter.

The integrated buck-boost converter was not targeted for fast load transient response, which is typically achieved using a larger output capacitor. Nevertheless, the converter was tested with a load step to evaluate its transient performance. Figure 7.25 shows the integrated converter's output voltage drop of less than 50 mV for a load step of 50 – 250 mA in 100 μs, illustrating its stability under load transient events.

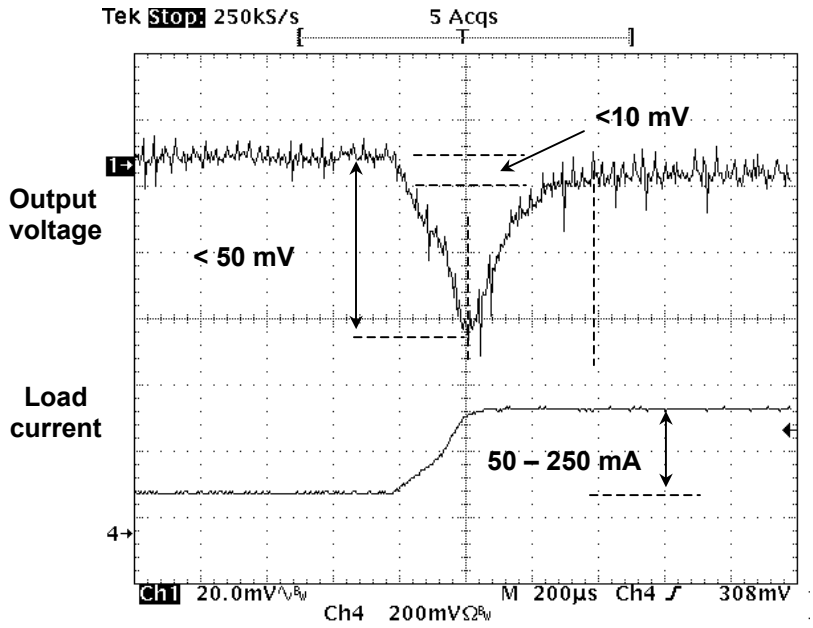


Figure 7.25. Measured load transient response of the integrated buck-boost converter.

The dynamic converter was tested for its control signal to output voltage transient response under the worst-case conditions. The feedback loop, compensated for stability in the boost mode, suffer from a lower unity gain frequency in buck-mode with the input supply and output voltage are at their minimum, when power-stage's open loop gain is at lowest while the dominant pole location remains unchanged. Figure 7.26 shows the buck-mode control transient response of the integrated converter. The converter's output voltage changes from 0.5 – 1 V, for a 0.1 – 0.2 V control-step with in 100 µsec. Recall that the converter is designed to operate 1-dB higher than the desired voltage level such that the output voltage does not fall insufficient while responding to control steps of 1-dB in 666 µsec. Figure 7.27 shows the control-step transient response of the converter with the minimum supply voltage of 1.4 V. The output voltage changes from 0.8 – 3.0 V with a control signal change of 0.16 – 0.6 V within 100 µsec. A 1-dB step control step approximately changes by 10 % from the previous value; therefore these control steps used in the measurement represent far worse conditions.

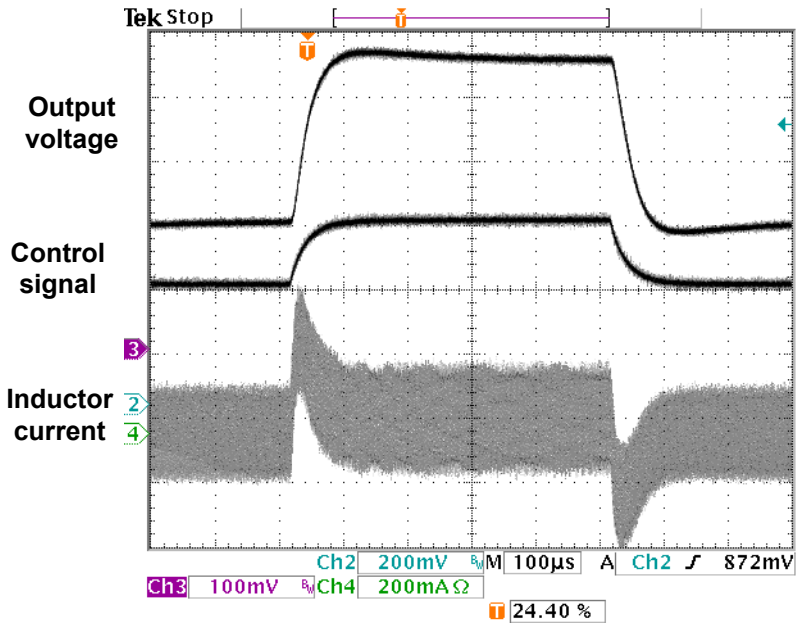


Figure 7.26. Control step-response of the buck-boost converter operating in buck-mode with 1.4 V input supply.

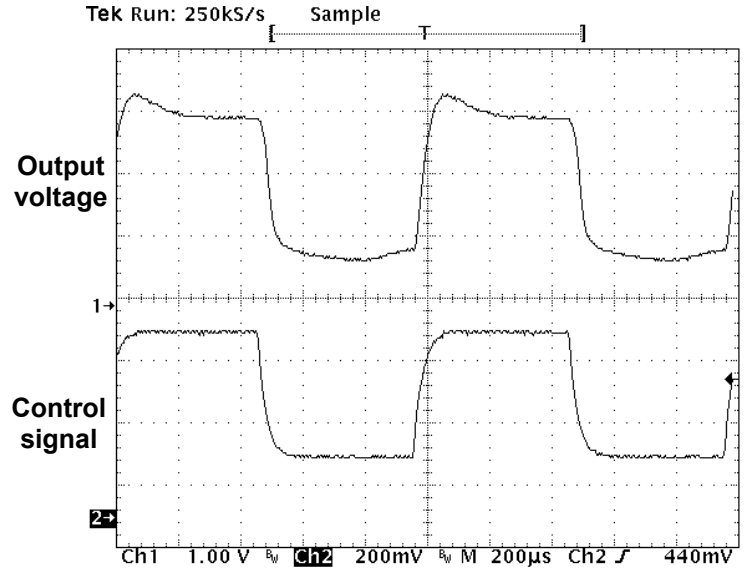


Figure 7.27. Control step-response of the buck-boost converter transitioning through buck, buck-boost, and boost mode with a 1.4 V input supply.

The integrated buck-boost converter's experimental results for an input voltage of 2.0 V in PWM control are summarized in Table 7.3, which shows the experimental converters' performance meets the targeted values. The discrepancy in simulated and measured peak-to-peak ripple voltage mostly arises from the effective series inductance (ESL) of the output capacitor and parasitic inductance of the current carrying path. Since the current flowing into the capacitor is in form of a square wave with fast rising and falling edges, ripple voltage must be carefully measured, since the oscilloscope probe inductance and grounding bounce related noise contributes to the ripple waveform. It was concluded that, the printed circuit board (PCB) for the integrated converter required further optimized for a better ripple performance so that a fair comparison with the simulated value could be made. However, since the experimental result met the target requirement, another PCB was not designed. While the simulated efficiency value only considered device resistances, bond wire and metal resistances contributed to extra power losses, ultimately yielding a lower measured efficiency of the converter.

Table.7.3. Summary of the integrated buck-boost converter's experimental results.

Parameters	Unit	Target	Simulation	Expt.
PWM Mode (V_{IN} = 2.0)				
Control voltage range	V	0.1 – 1	0.1 -1	0.08 - 1
Output voltage range	V	0.5 – 5	0.5 –5	0.4- 5
Load current range	A	0.03 – 0.3	0.03 – 0.3	0.03 – 0.33
Output ripple (peak-to-peak)	mV	≤ 100	≤ 35	≤ 100
Output voltage accuracy	%	5	-	3.5
Line regulation @ 2.5 V output	%	2	-	1.4
Load regulation @ 2.5 V output and 0.3 A load	%	2	-	1.6
Worst case control-step response	μsec	≤ 200	-	≤ 200
Switching frequency	MHz	1	-	1.05
Efficiency (Peak load)	%	> 90	82	72

7.4 WCDMA RF PA System

The performance of the integrated buck-boost supply and dynamic gate bias circuit are evaluated in the system environment using a 1.96 GHz WCDMA RF PA. The available evaluation board from Sirenza Microdevices with hetero-junction bipolar transistors [101] is selected because of its suitability for low voltage operation and flexibility of modifying the circuit board to incorporate the dynamic bias control circuits. The schematic of the test system is shown in Figure 7.28. HBT_1 constitute the RF power amplifier while HBT_2 and HBT_3 forming the biasing circuitry. For testing purpose, a current mirror ratio of 1: 200 is achieved between HBT_2 and HBT_1 using a variable emitter resistor R_{BIAS}. In an integrated circuit implementation, the current mirror ratio can be achieved by designing two transistors with specified ratio of their emitter areas. Transistor HBT_3 is used to provide base current for the main transistor HBT_1, thereby allowing the dynamic bias circuit to provide only the required collector current for HBT_2. For MOS based PAs and their biasing circuits, only the current mirror transistors are required, since these devices do not draw any gate current under dc operating conditions.

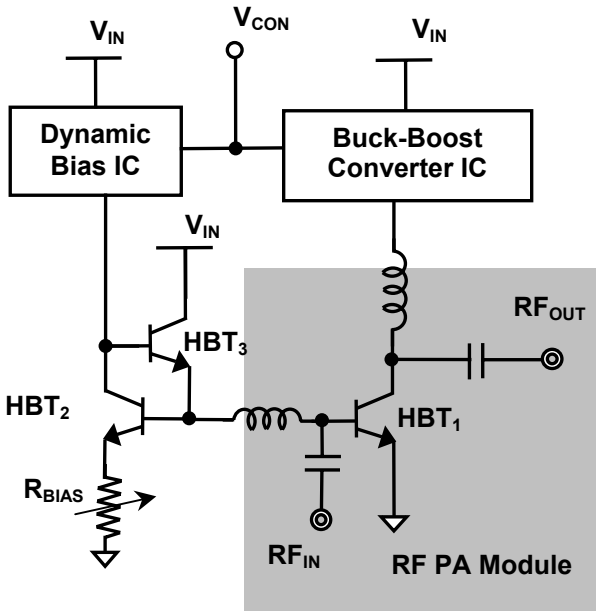
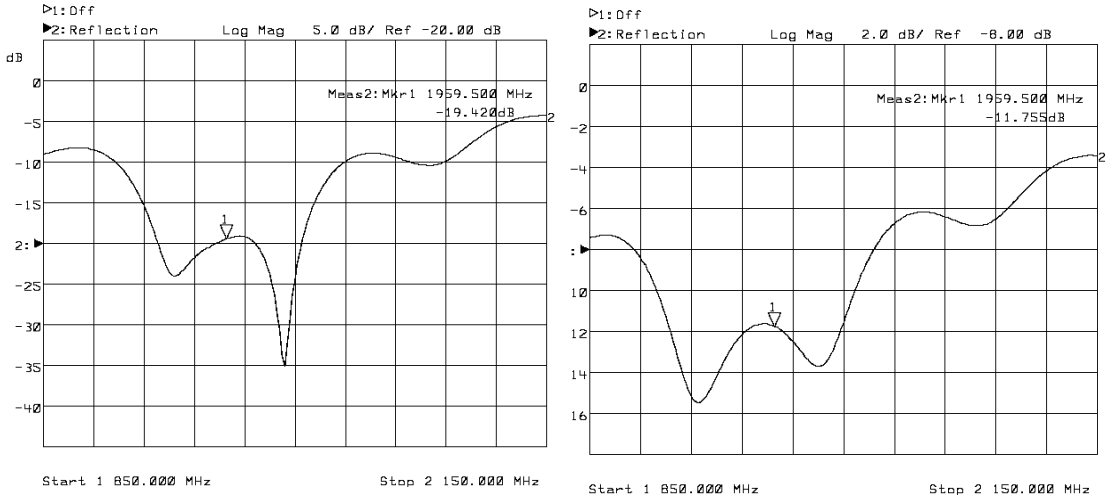


Figure 7.28. Schematic of the HBT RF PA with a dynamically adaptive buck-boost supply and gate-bias circuit.

The input matching characteristics of the 1.96 GHz HBT RF PA under two extreme operating conditions under which the dynamically adaptive system operates is shown in Figure 7.29. For the peak power of 25 dBm the PA is biased at a collector voltage of 4.5 V with 220 mA of collector current established through the transistor. Alternatively, during low output power the transistor is operated with a collector emitter bias voltage of 0.5 V and collector bias current of 25 mA. Although the input matching degraded from –19 dB to –11 dB, it remains within the typical minimum requirements of –10 dB.



(a) (b)

Figure 7.29. Input matching characteristics of the 1.96 GHz HBT RF PA with bias current and supply voltage adjustment. The S_{11} parameter of the PA with (a) V_{DD} = 4.5 V, I_D = 220 mA and with (b) V_{DD} = 0.5 V, I_D = 25 mA.

The power gain characteristics of the 1.96 GHz HBT RF PA under two extreme operating conditions under which the dynamically adaptive system operates is shown in Figure 7.30. As expected, the power gain of the transistor degraded from higher to lower current, since the transconductance of the device changes with it bias current. The power gain variation of the dynamic supply PA needs to be taken into account while calibrating the transmitter with the automatic gain control circuits.

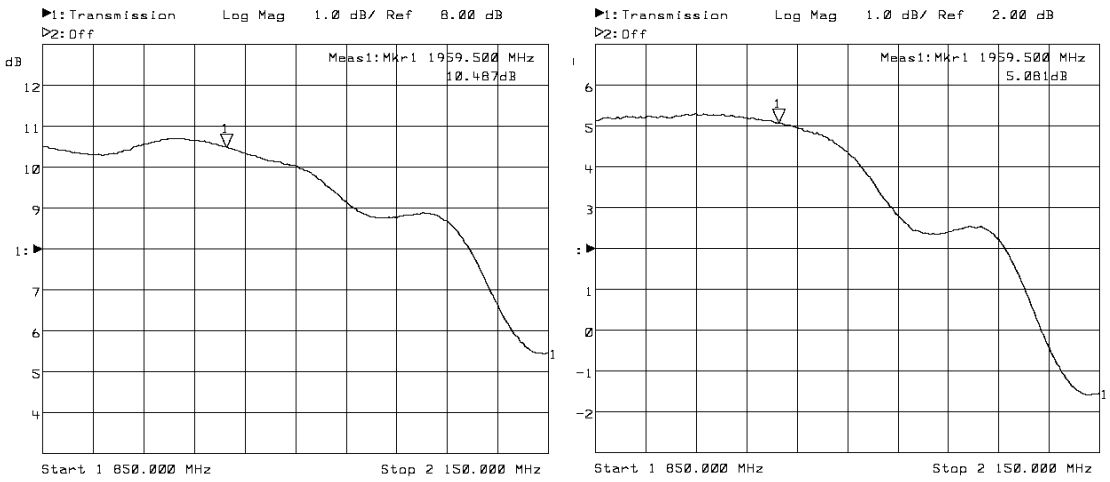


Figure 7.30. Power gain variation of the 1.96 GHz HBT RF PA with supply voltage and bias current adjustment. The S_{21} parameter of the PA with (a) V_{DD} = 4.5 V, I_D = 220 mA and with (b) V_{DD} = 0.5 V, I_D = 25 mA.

7.5 PA System Experimental Results

The dynamically adaptive system is tested with a 1.96 GHz center frequency, 3.84 MHz bandwidth hybrid phase-shift keying (HPSK) modulated wideband code division multiple access (WCDMA) signal. The out-of-band signal regrowth due to the nonlinearity of the PA and supply voltage ripple is expressed as adjacent channel leakage ratio (ACLR), which is defined as ratio of signal power in a 3.84 MHz bandwidth at 5 MHz offset from the center frequency to the channel power. Similarly alternate channel power is defined as the ratio of signal power in a 3.84 MHz bandwidth at 10 MHz offset from the center frequency to the channel power. Figure 7.31 shows the measured output spectrum of the RF PA with dynamic supply and bias control at its peak power of 25 dBm (22.5 dBm output power at the spectrum analyzer with 2.5 dBm attenuation from the PA output to the spectrum analyzer input). The adjacent and alternate channel leakage ratios of the PA are –35 and –58 dBc, respectively, satisfying the WCDMA requirements.

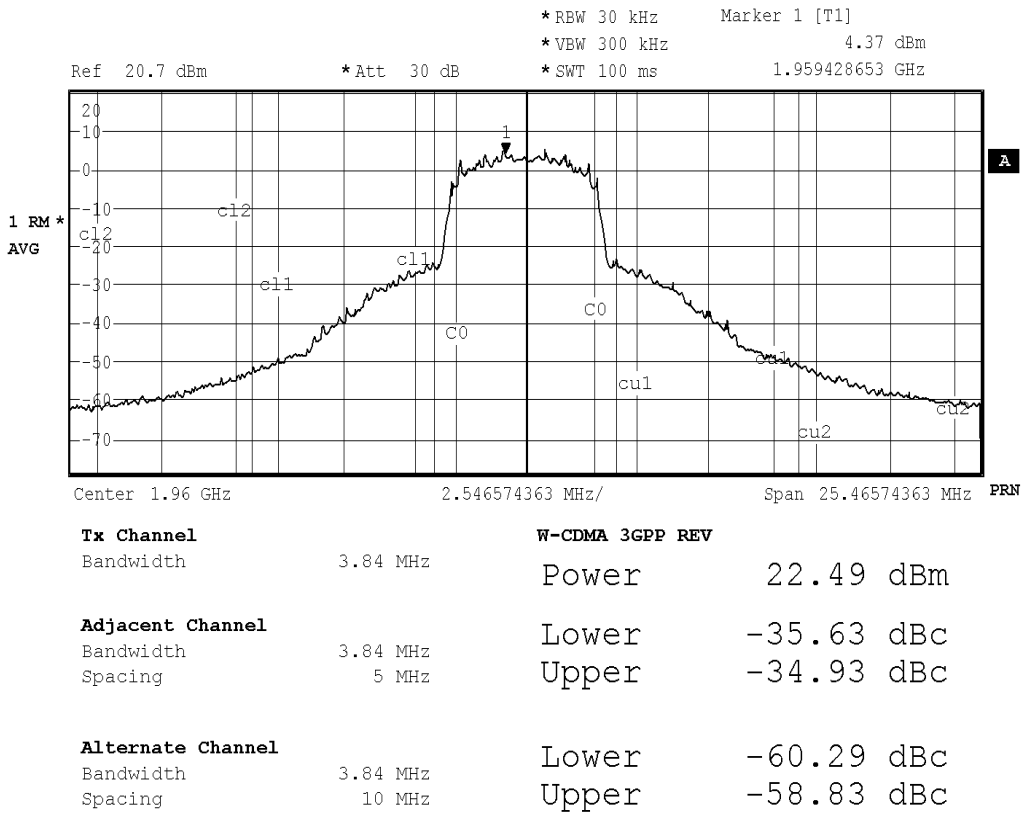


Figure 7.31. Output spectrum of the experimental PA with dynamically adaptive buck-boost supply and bias current control.

Variations of the adjacent channel leakage ratio of the dynamic supply PA is compared with a fixed supply PA as shown in Figure 7.32. Since the PA was operated with close to the optimal supply and bias control in the dynamic system to achieve higher efficiency, although the ACLR is degraded with respect to a fixed-bias system, it remains well below the specified limit of –35 dBc. The alternate channel leakage ratio values of the fixed- and dynamic-supply PA are plotted in Figure 7.33. Unlike the adjacent channel leakage ratio, the PA nonlinearity due to dynamic bias does not significantly affect the alternate channel leakage ratio. However, the dynamic supply PA exhibits a marginally higher alternate channel leakage ratio mostly attributed to the power supply ripple. The dynamic supply PA meets the alternate channel leakage ratio specifications of -48 dBc in a WCDMA system. Both the adjacent and alternate leakage ratios degrade as RF output

power is lowered when the RF signal level approaches the noise floor of the spectrum analyzer.

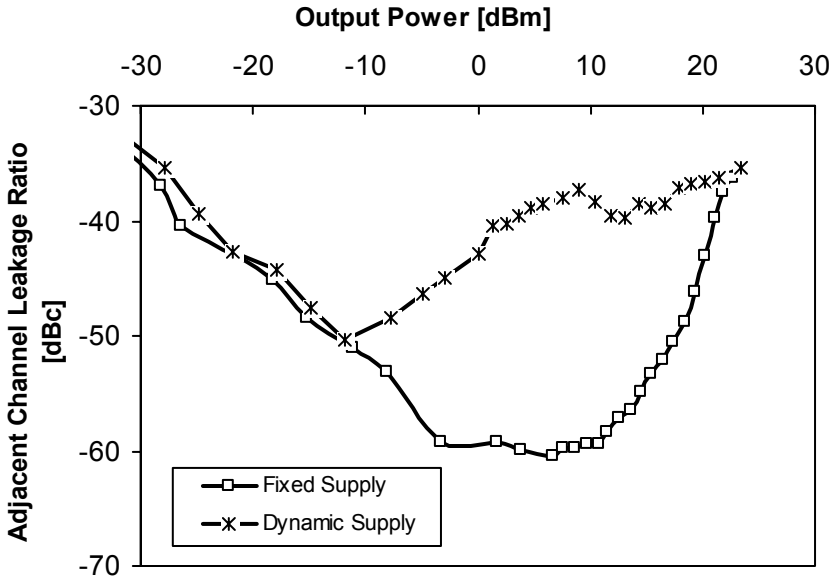


Figure 7.32. Comparison of adjacent channel leakage ratio of the dynamic- and fixed- supply PA.

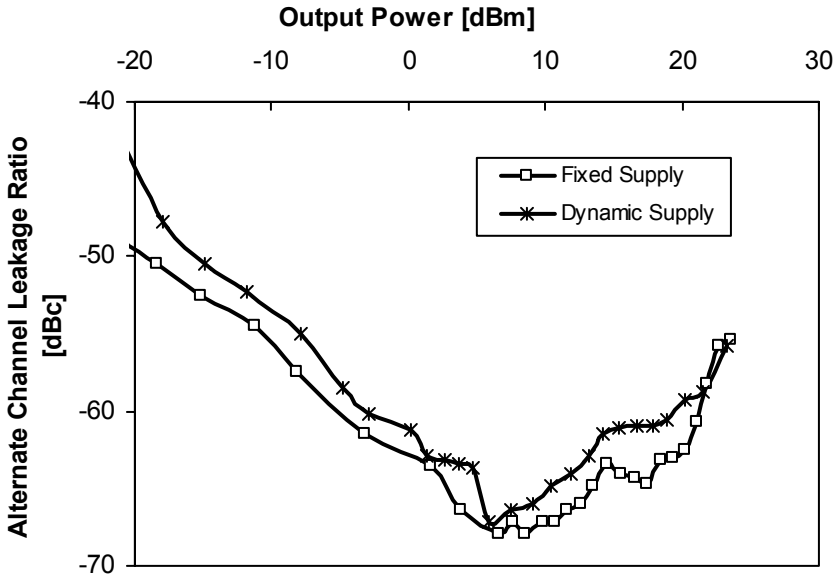


Figure 7.33. Comparison of alternate channel leakage ratio of the dynamic- and fixed- supply PA.

Figure 7.34 shows the power gain of the dynamic supply PA, which varies from 10 dB to 4 dB as the bias condition changed from 4.5 V, 220 mA to 0.4 V, 25 mA, due the dependence of transistor's transconductance on bias parameters. As the output power decreases below 0 dBm, the PA's bias condition remain unchanged, which is reflected as the power gain remains constant in the low power region.

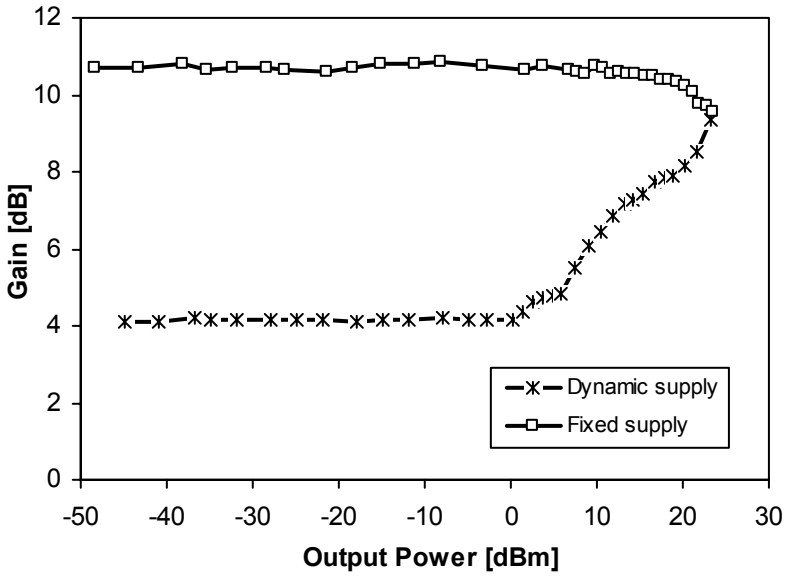


Figure 7.34. Power gain of the dynamic- and fixed- supply PA.

Modulation accuracy of digitally modulated signals, e.g., WCDMA is expressed using error vector magnitude (EVM), which is the scalar distance between the ideal reference signal and the measured signal. Since the dynamic buck-boost power supply has a switching frequency of 1 MHz, the switching ripple falls within the transmitting channel bandwidth of 3.84 MHz around the carrier center frequency. To evaluate the effect of switching power supply ripple on the in-band linearity of the PA system, EVM of the RF PA was measured at various power levels using a QPSK modulated signal. A representative EVM plot and the output signal constellation of the dynamically adaptive PA system at its maximum output power is given in Figure 7.35 showing an overall rms error of 8.7 %.

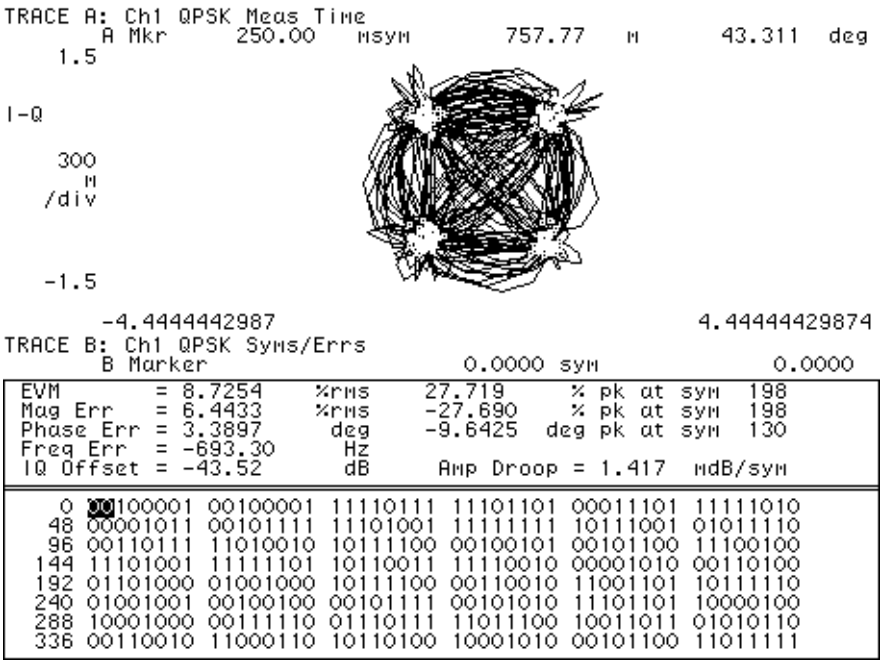


Figure 7.35. Error vector magnitude (EVM) plot of the WCDMA RF PA with a dynamically adaptive buck-boost supply and bias control IC.

The overall EVM numbers obtained for the dynamic supply PA along with the fixed supply PA are shown in Figure 7.36, which infers that the ripple in the PA's power supply degrades the EVM but remains within a factor of 8 –10 %. At peak output power, although the output ripple of the converter increases due to a higher load current, its effect on EVM is slightly greater than the fixed supply PA but remains below typical specifications of 10 % or less. The EVM of the PA is essentially reflected on to the system level specifications, e.g., bit-error rate (BER) of the RF transmitter. For high performance system with stringent EVM requirements, using either a larger inductor or output capacitor, or both, can further lower the ripple voltage of the dynamic supply, which however comes at the expense of degraded control-signal response.

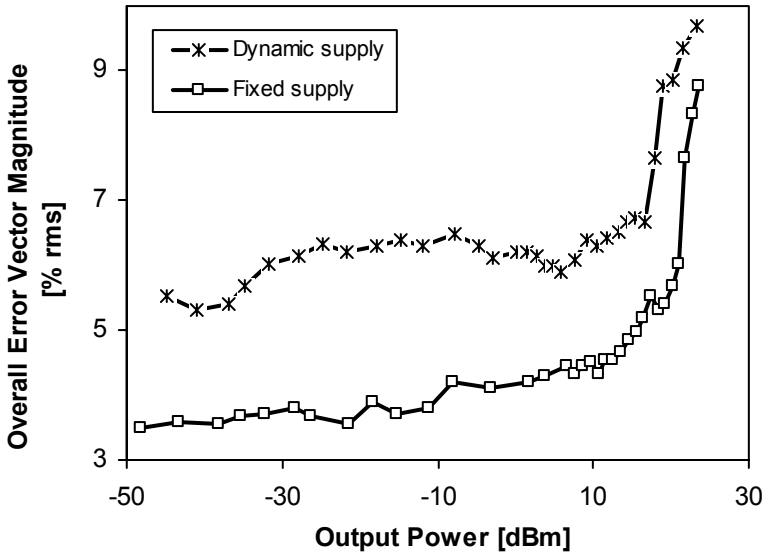


Figure 7.36. Error vector magnitude (EVM) of the dynamic- and fixed-supply PA with QPSK-modulated signal.

Drain efficiency, which is the ratio of RF output power to the input supply power, is the measure of PA's ability to convert battery power into usable RF power at the transmitter antenna. Therefore, all the discussions offered in this section are with respect to the drain efficiency. Efficiency curves for the power amplifier with fixed supply and dynamic supply are illustrated in Figure 7.37, which shows that the PA with dynamically adaptive supply exhibits higher efficiency at back-off power. The converter, when operated with PFM mode exhibits marginally higher efficiency compared to the PWM mode converter, which however is not clearly distinguished in the plot. Figure 7.38 shows the input supply power of the PA operating with fixed and dynamic supply. As seen from the plot with a fixed supply for higher PA output power the input supply power increases, which suggests that the current drawn by the PA is dependent on the input signal drive concluding a class-AB operation.

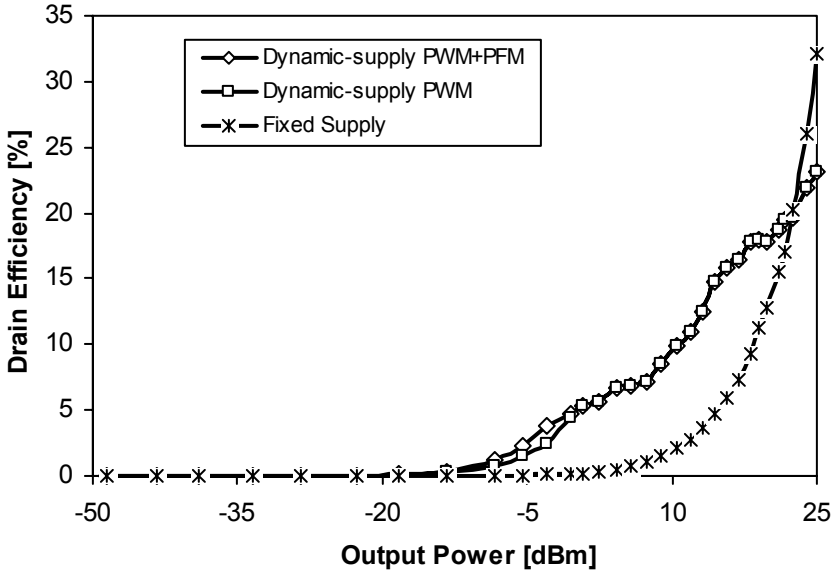


Figure 7.37. Drain efficiency of the dynamic- and fixed-supply WCDMA PA.

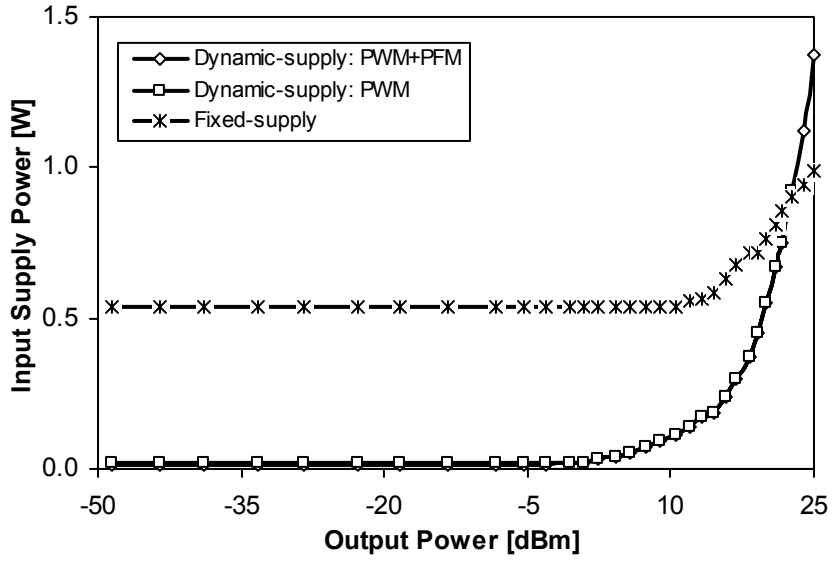


Figure 7.38. Input supply power of the dynamic- and fixed-supply PA.

To estimate average efficiency of the PA system while in active transmission mode, weighted input supply power profiles for both fixed-supply and dynamic-supply PA are shown in Figure 7.39. Clearly, the average input supply power, which is equal to the area under the weighted input power curve, for the dynamic-supply PA is much smaller than that of the fixed-supply PA for same average output power. The average efficiency of the dynamic-supply PA with PWM and PFM mode converter [calculated using Equation (1.3)] is *seven times greater* than the fixed-supply scheme, which translates into a battery life improvement depending on the percentage of transmitter power consumed by the PA stage and time period for which the PA actively transmit RF power.

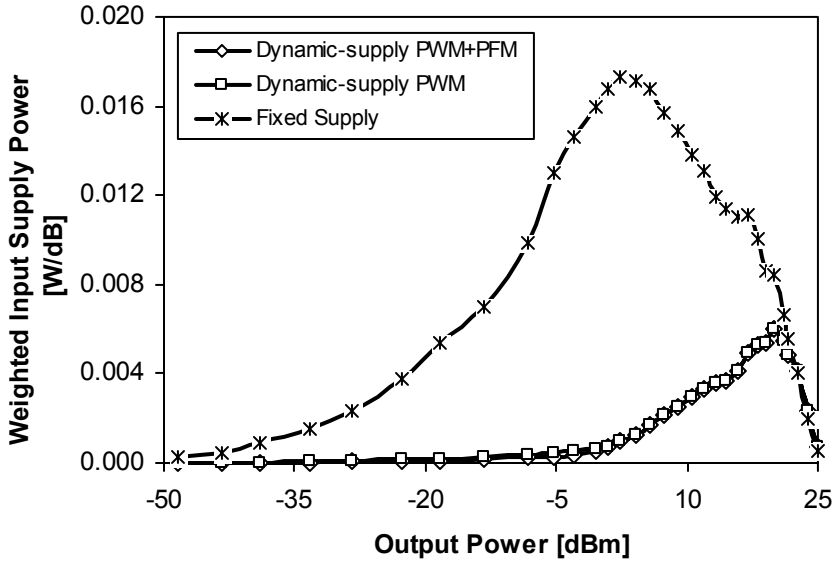


Figure 7.39. Weighted input power comparison of the dynamic- and fixed-supply PA.

The efficiency enhancement of the experimental HBT PA with dynamically adaptive buck-boost converter supply and bias current control IC is compared with other results reported in the literature as given in Table 7.4. The integrated system described in this chapter offers better performance compared to others, but it is also to operate at peak

system performance with a battery close-to fully discharged, not to mention its inherent improved battery life performance. The increased in average efficiency of the PA with integrated buck-boost converter compared to the discrete prototype described earlier is attributed to the higher power efficiency of the converter itself.

Table 7.4. Comparison of the reported efficiency enhancement scheme using dynamic supplies and this work.

Scheme	PA maximum output power	Fixed supply PA efficiency	Dynamic supply PA efficiency
Buck converter supplied AlGaAs/InGaAs MESFET PA [51]	28 dBm	2.2 %	11.2 %
Boost converter supplied GaAs MESFET PA [45]*	26 dBm	3.89 %	6.38 %
Buck-boost converter supplied LDMOS PA presented in Chapter 4	27 dBm	1.53 %	6.78 %
Integrated buck-boost converter supplied HBT PA	25 dBm	1.95 %	13.67 %

* Output power probability distribution profile used in [45] is not the same.

7.6 Battery Life Improvement

The average efficiency of the PA system considering the probability distribution of the output power discussed in the previous section only presents the information when the PA actively transmits RF power. To evaluate actual battery life improvement due to the dynamically adaptive system, standby performance of the converter needs is considered. Therefore, the total average power (P_{avg_tot}) drained from the battery is given by

$$P_{avg\_tot} = P_{stdby} \times (1 - D_{active}) + P_{avg\_active} \times D_{active}, \quad (7.1)$$

where P_{stdby} is the standby power consumed by the power supply control circuit that remain active even if the PA does not transmit any power, P_{avg_active} is the average power

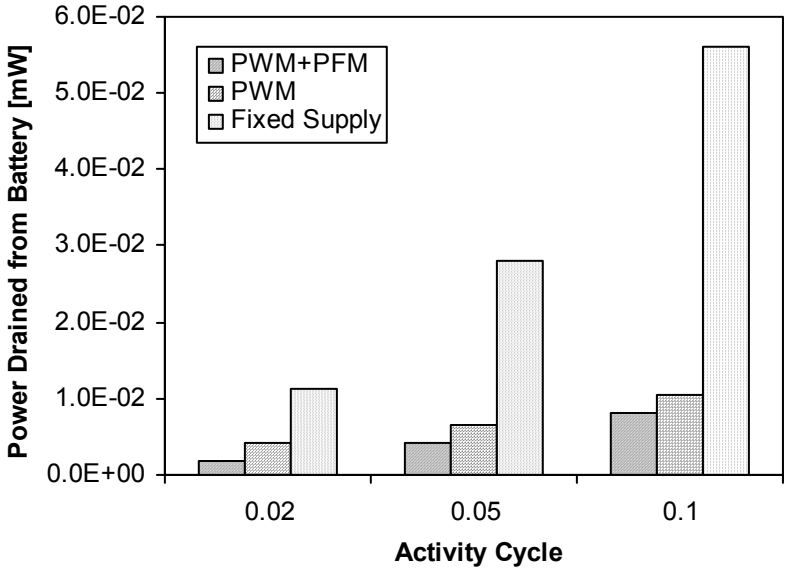
consumed by the system when the PA is transmitting RF power. D_{active} is the fraction of total period for which the PA is operational, which is referred as *activity cycle* henceforth in the discussion. The battery life (in hours) system is computed as the ratio of batter capacity to the total average power (including active power and standby power), and is given by

$$\text{Battery Life [Hours]} = \frac{\text{Battery Capacity[mWh]}}{\text{Total Average Power[mW]}}. \tag{7.2}$$

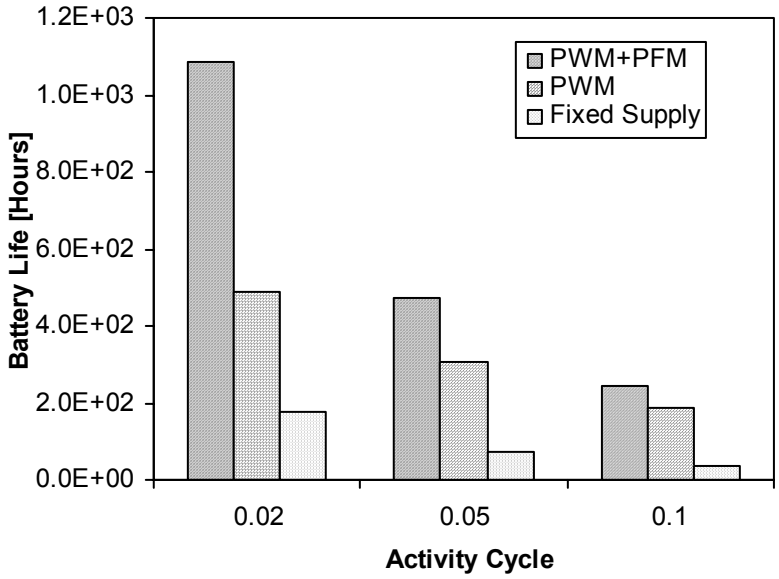
The calculation of the exact battery life improvement is complicated by the fact that a battery capacity is typically specified in mAh, while its terminal voltage varies considerably as the load current changes. To obtain a relative estimate of the battery life improvement and for simplicity, a battery with constant energy of 2000 mWh [1.5 V with 800 mAh] is considered in this discussion. Experimentally obtained standby (quiescent) currents of 100 μA and 1 mA are used in the calculation for PFM and PWM mode standby power, respectively. As evident from Equation 7.1, the total average power drawn by the PA depends on the *activity cycle* of the PA. Accordingly, using the average active power and standby power of the system, the total power drained from the battery are calculated for the dynamically adaptive system with both PWM and PFM control, only PWM control, and the fixed-supply system.

Figures 7.40(a) and 7.40(b) show bar graphs of the total average power drawn and battery life of the systems, respectively, for dynamic supply operating in both PWM and PFM, only PWM, and fixed supply PA system with variation in activity cycle. For a lower activity cycle, while the PA does not transmit any power, its dynamically adaptive converter remains active dissipating quiescent power for its control circuits. Since the converter operating in PFM mode has a lower quiescent current, its total average power consumption is less than the converter operating in PWM mode throughout the power range. Consequently, for lower activity cycle, the dual-mode converter exhibits almost twice battery life with the converter operating in PWM mode throughout. However, as the PA remains active more time, the effect of standby power on the overall system

power and battery life decreases. Therefore, depending on the portable device's activity cycle, dual-mode converter can significantly prolong the battery life.



(a)



(b)

Figure 7.40. (a) Power drained from the battery and (b) battery life of the dynamic- and fixed-supply PAs for various activity cycles.

Recalling the discussion in Chapter 6, continuous 1-dB adjustment of supply voltage and bias current of the PA requires a complex gain calibration scheme with characterization of the PA for a number of operating points and subsequent utilization of the information to realize the converter's dynamic range. Alternate control methods with two and three discrete steps simplify the calibration process, which however degrades the system efficiency. Figures 7.41 and 7.42 show the input and weighted input power profiles of the alternate control methods just described and the continuous 1-dB step method. Average efficiencies of the approximate controlled systems are calculated using the procedure outlined earlier and the results are presented in Table 7.5. Clearly, the continuous 1-dB control method shows a higher efficiency compared to the approximate schemes, since the supply voltage and current of the PA are kept at the minimum for the former case yielding a higher efficiency across its loading conditions. Especially, in the power range of 10 – 25 dBm, where the output power and its respective probability density is high, the contribution towards average efficiency of the PA is larger compared to the low power region (less than -10 dB). Therefore, for higher average efficiency, the PA system needs to operate with high efficiency over the region where the contribution of average power (product of output power and probability distribution) is larger.

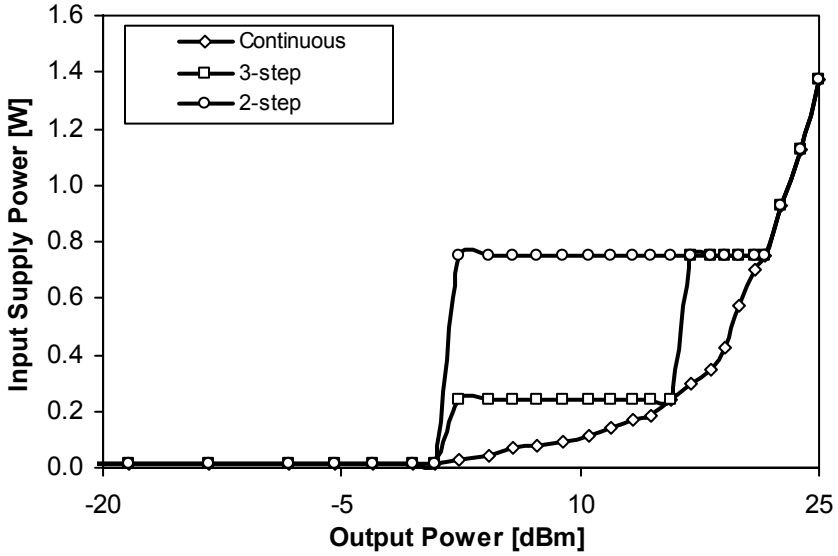


Figure 7.41. Input power profiles of the continuous 1-dB, discrete two- and three-step control schemes.

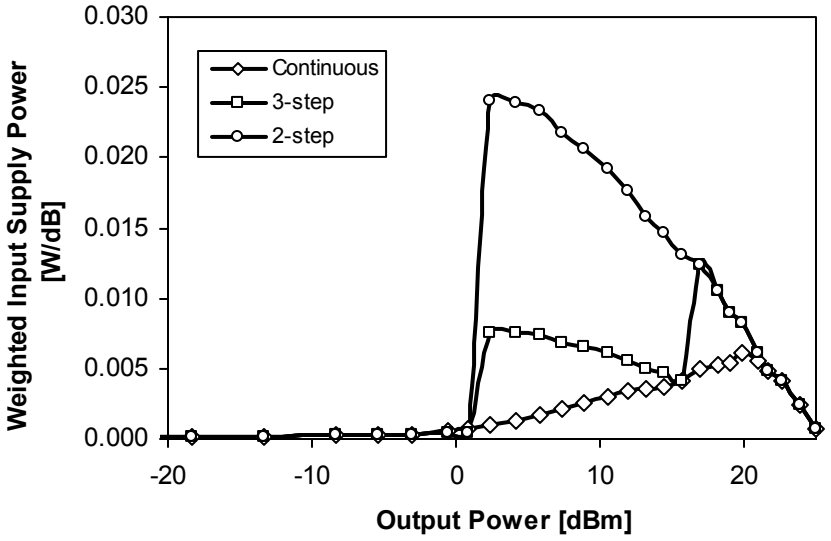
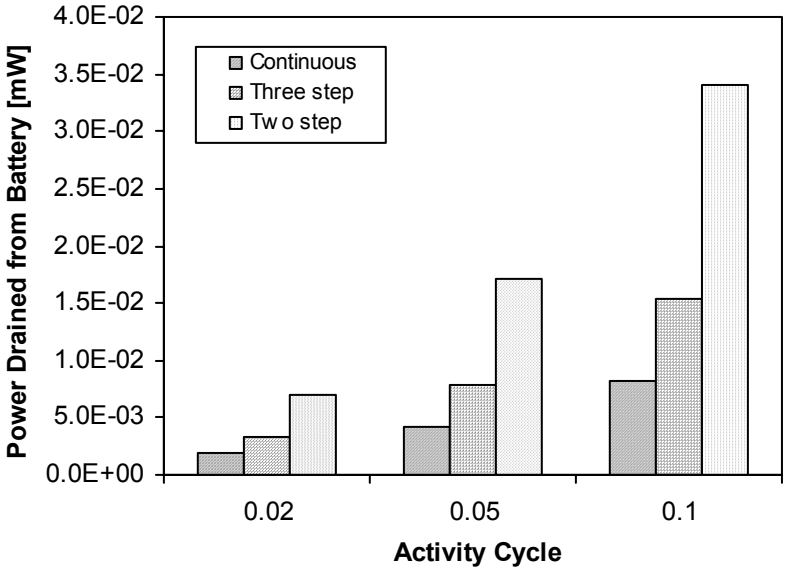


Figure 7.42. Weighted input power profiles of the continuous 1-dB, discrete two- and three-step control schemes.

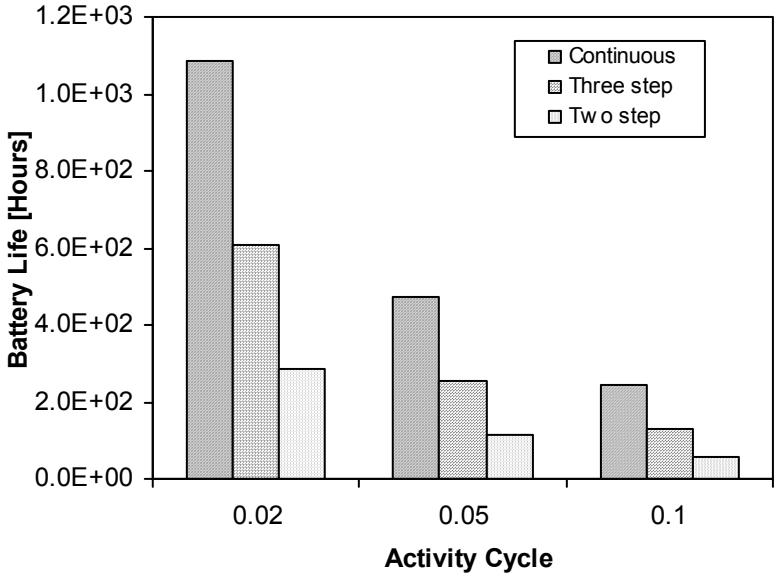
Table 7.5. Comparison of the average efficiency of various control schemes.

Control scheme	Average Efficiency
1-dB continuous control	13.61 %
3-step discrete step control	7.87 %
2-step discrete step control	3.224 %

Figures 7.43 (a) and (b) show bar graphs of the total average power drawn and battery life of the systems, respectively, for the alternate control schemes with variation in activity cycle utilizing the dual-mode converter with PWM and PFM operation. As expected, the continuous 1-dB control scheme outperforms both the approximate control methods in terms of lower power consumption and consequently higher battery hours.



(a)



(b)

Figure 7.43. (a) Power drained from the battery and (b) battery life for alternate control methods for various activity cycles.

7.7 Summary

This chapter discusses the full-chip verification results of the integrated buck-boost converter, followed by system layout issues. Power transistors are laid out with integrated back-gate contacts and placed on one side of the die to minimize their switching noise effect on sensitive analog circuits. The analog blocks are laid out in cross-coupled, common-centroid geometry to improve the matching of key components, e.g., input pairs, current mirror loads, etc. to achieve low input offset voltage. The experimental buck-boost converter in PFM mode is verified with an output voltage of 0.5 V with 50 mA load current yielding a maximum peak-to-peak ripple voltage of 25 mV over an input supply range 1.4 – 4.2 V. The converter exhibits an efficiency of 70 – 88 % in the PFM mode. It is also verified that the converter with adaptive on time control exhibits accurate output ripple voltage over the supply range while yielding a higher power efficiency compared to the fixed on time control method.

The integrated buck-boost converter, except power inductor, input and output capacitors, error-amplifier compensation network and a variable resistor for buck-boost converter's operation region adjustment, was successfully operated in buck-mode operation. As described earlier in Chapter 6, the boost stage PMOS transistor's poly-silicon gate was not connected with metal around its periphery resulting in a higher gate resistance and consequently larger gate-drive propagation delay. Therefore, with external logic gates and using separate controller and power transistors' chips, the buck-boost and boost mode operation of the power supply was experimentally verified for functionality and performance. The buck-boost converter in PWM mode generated 0.4 – 5 V of output voltage with a maximum load current of up to 330 mA from an input supply of 1.8 – 4.2 V, exhibiting a maximum power efficiency of 90 %. Since the available gate drive for the buck stage PMOS pass transistor reduced at lower supply voltages and consequently the on resistance of the power switches increase, a maximum output voltage of 3.5 V with 300 mA load was generated from a 1.4 V supply.

With the integrated buck-boost power supply, the dynamic gate bias circuit, and discrete HBTs, a 1.96 GHz, 3.84 MHz baseband bandwidth, 25 dBm WCDMA RF PA was implemented. Experimental results of the PA system with a HPSK modulated signal

show adjacent and alternate channel power ratios of less than –35 and –48 dBc, respectively, thereby satisfying the targeted system requirements. The error vector magnitude (EVM) performance was measured with a QPSK modulated signal, since the vector network analyzer was not equipped with an HPSK demodulator. The overall EVM remained less than 10 % throughout the PA output power dynamic range. The dynamically adaptive system showed an average efficiency of 13.67 % compared to an amplifier biased with fixed current and supply voltage, which yielded an average efficiency of 1.9 %. Depending on the activity cycle (defined as the ratio of the time for which the PA is actively transmitting and receiving information to standby mode) of the PA, the average power during active mode and standby system power contribute to the total average power consumption and consequently influence the battery life. Assuming the PA is active for 2 % of the total time and 98 % remains in standby mode, and powered from a 2000 mWh (1.5 V with 800 mAh) battery capacity, the dual-mode (PWM+PFM) converter shows five times increase in battery life compared to fixed supply PA and twice that of the only PWM-mode converter supply PA. The PA system is verified for functionality and performance over the supply voltage range of 1.8 – 4.2 V, which includes the state-of-the-art single cell Li-ion battery (2.7 – 4.2 V) and its low cost equivalent of two-cell NiMH and NiCd batteries (1.8 – 3.6 V). In essence, the proposed novel dynamically adaptive PA power management system is successfully realized for both functionality and performance using a low-cost CMOS process. Next chapter concludes the work presented in this dissertation while summarizing the challenges and original research contributions.

CHAPTER VIII

CONCLUSIONS

A novel, energy-efficient linear RF power amplifier with a power-tracking, dynamically adaptive buck-boost power supply and bias current control scheme is conceived and experimentally demonstrated in this research as a discrete PCB-level prototype implementation and an integrated solution in a low-cost CMOS process. The power-tracking solution enables the use of a converter without the need for fast transient response, which is accomplished by a low switching frequency converter, consequently maintaining high efficiency over a wide loading range. The use of a dual-mode buck-boost converter, operating in pulse-width modulation (PWM) at high power and pulse-frequency modulation at low power region, offers a power supply solution with high efficiency over the output power range of the PA, not to mention the buck-boost converter's inherent ability to operate across the entire battery voltage range.

This chapter offers a summary of challenges faced and solutions proposed while realizing an energy-efficient linear RF PA for portable handheld devices targeted for code-division-multiple-access (CDMA) and wide-band CDMA (WCDMA) wireless environment. The experimental results are demonstrated for a CDMA/WCDMA wireless platform; however, the design concepts are applicable to other application environments, e.g., IEEE 802.11 based wireless LANs, 3G wireless system EDGE, etc. having a wide variation of transmitter power. The following subsections present summary of original contributions of this research followed by recommendations on possible future work.

8.1 Challenges

The primary objective of this research was to develop and design an efficient linear RF PA targeted for CDMA/WCDMA mobile handsets suitable for state-of-the-art single cell Li-ion/NiMH/NiCd batteries. The motivation is to increase battery life of PA-driven applications by designing a low-cost, integrated system with smart power management functions, especially for the feature-rich handheld devices having simultaneous voice, data, and imaging capabilities. Linear PAs are critical in state-of-the-art wireless systems employing non-constant envelope modulation, where information is transmitted both in the magnitude and in the phase of the RF signal. Preserving in-channel signal fidelity and minimizing out-of-band spectral regrowth is key to a functional cellular system. Unfortunately, linearity and efficiency are two orthogonal specifications of an RF power amplifier. High efficiency is achieved at the expense of reduced linearity and vice versa. Moreover, the variation of transmitter power over a wide dynamic range further complicates the problem, since the power efficiency of a PA, normally designed to meet the system requirements at its peak power, degrades significantly at lower power levels while it exhibits a linearity more than what is required. Optimizing the PA operation with respect to acceptable linearity while maximizing its efficiency clearly presents an attractive solution to one the complicated and challenging frontiers of portable RF research.

The design of a dynamically adaptive power supply comes with additional obstacles with regard to accuracy and control-to-output transient response. For a given inductor value and subsequent inductor ripple current, a larger capacitor is required to reduce the peak-to-peak output ripple voltage. While a large capacitor is beneficial for load transient response providing fast charge to mitigate load-demand, its control-to-output transient response is degraded since it requires a higher energy being transferred from the input source for its voltage level to increase. For an RF PA the ripple voltage requirement is critical since the ripple voltage influences both in-band and out-of-band signal fidelity, and must therefore be well controlled for satisfactory system operation.

To improve the light-load power efficiency and standby performance of the system, switching regulators typically use pulse-frequency modulation (PFM) control,

where the switching frequency is lower than a fixed frequency pulse-width modulation (PWM). A constant on-time PFM control is preferred over a peak-inductor current control scheme, since the latter requires expensive current-sensing or -estimation techniques. Unfortunately, in a constant on-time scheme, as supply voltage varies, the peak inductor current changes, which results in a variation of the peak-to-peak ripple and average output voltage. When the converter is used as a dynamic supply for the PA, the ripple voltage must be well controlled to meet the linearity specifications of the PA. Therefore, the converter's on time needs to be adjusted as supply voltage changes to maintain an accurate output ripple voltage.

State-of-the-art portable batteries exhibit a wide variation in supply voltages (e.g., single-cell Li-ion: 4.2 –2.7 V, NiMH/NiCd: 1.8 – 0.9 V). Developing generalized power management system solutions capable of operating across wide supply voltage range (1.4 – 4.2 V) need to have functional circuits at the lower end of supply voltage while withstanding breakdown limits higher supply voltage limit. Unfortunately, process technology available for this research, with a high supply voltage limits, e.g., 0.5 μm with 5 V, has transistors with relatively large threshold voltages in the order of 0.7 ~ 0.95 V. Therefore, low voltage circuit design techniques must be employed to meet the input common-mode range (ICMR) requirement.

8.2 Original Research Contributions

The original contributions of this research are in the area of efficient linear RF PAs suitable for low-voltage, battery-powered radio systems and in the domain of integrated power management. However, the concepts developed can also be utilized in power management IC designs targeted for other portable applications and in the general area of low voltage analog IC design. The contributions are classified in three domains: (a) design of energy-efficient linear RF PAs, (b) ultra-low voltage non-inverting, buck-boost dc-dc converter with high efficiency over a wide loading range, and (c) low-voltage and low-power analog circuits. The specific contributions are briefly summarized in the following paragraphs.

A. Power-Tracking, Dual-Bias Linear RF Power Amplifier

In wireless communication systems with a wide range of power control, e.g., CDMA and WCDMA, the system need to operate with high efficiency over wide loading conditions to achieve high energy efficiency. Most of the reported techniques in the literature attempt to improve peak-power efficiency, which is of course beneficial for systems operating mostly at peak power. In this research, it is proposed and experimentally verified that changing both the supply voltage and bias current of the PA as a function of its average transmitted power, instead of the instantaneous signal envelope, can be accomplished with a converter with a lower bandwidth, which implies a lower switching frequency and consequently higher light-load efficiency. The main limitation of such an approach is the gain variation of the PA; however, in a system environment the PA can be calibrated with the drivers and variable gain amplifiers to maintain the transmitter's output power range.

B. Buck-Boost Converter Supplied Linear RF PAs for Low Voltage Environment

In addition to improving the system's energy efficiency by operating individual components with higher efficiency, battery life can further be improved by utilizing entire battery voltage range. Today's portable power sources exhibit a wide terminal voltage profile as a function of time (e.g., single-cell Li-ion battery: 4.2 V – 2.7 V, two-cell NiCd/NiMH: 3.6 V – 1.8). The in typically operated at its highest possible supply voltage, limited by its breakdown voltage limitations, to deliver the required power with a lower current thereby minimizing power loss in the current flowing path and consequently achieve higher efficiency. Therefore, the required supply voltage for the PA in power-tracking system can be higher or lower than the battery voltage, which necessitates the use of a buck-boost converter. This research experimentally demonstrates a high-efficiency linear RF PA system with a low voltage, dynamically adaptive buck-boost converter, thereby enabling the system to operate from a wide supply voltage power source.

C. Integrated Power Management Frame Work for Linear RF PAs

This research also contributed in the successfully realizing an integrated circuit consisting of a dual-mode buck-boost converter and dynamic gate bias circuit for a PA in a low cost CMOS process to implement an energy-efficient WCDMA linear PA. The IC is fully functional with a minimum supply voltage of 1.4 V, while it was successfully applied to realize a 25-dBm WCDMA PA for a supply voltage of a 1.8 – 4.2 V. The design covers most of the state-of-the-art rechargeable batteries. The converter can be used for alternate portable power sources, fuel cells, which are however not experimentally validated in this research.

D. A Power-Supply-Adaptive Constant ON Time PFM Control for Accurate Peak-to-Peak Ripple Voltage

Energy-efficiency of portable handheld devices is not reflected by their peak-power efficiency and the probability of the loading profile must therefore be considered while evaluating battery life. Especially in CDMA/WCDMA mobile stations, where the transmitter power varies from –50 dBm to 27 dBm, dynamic adjustment of supply voltage and current over the entire range is practically not possible, and therefore below a certain output power the supply voltage and bias current is kept constant. Under low output-power, the efficiency is degraded due to excessive switching losses if the converter is operated in PWM mode, which is primarily designed for the peak-power target. For maintaining high efficiency under light loads, the converter voltage is regulated with a PFM controller having constant on time control. The on time is dynamically adjusted with supply voltage with the aim of keeping the peak inductor current constant, thereby optimizing the converter's switching frequency and output voltage accuracy.

E. Low Voltage, Dual-Mode Buck-Boost Converter IC with Wide Output Voltage

A top-down approach to the design of a dual-mode, buck-boost power supply IC primarily deigned for PWM operation in high power mode while changing to PFM mode during low power operation is developed for low supply voltage systems. The limiting

values of power switches resistance and its effect on the requirement of accurate duty cycle control are derived for generating a high output voltage with a certain load current from extremely low supply voltages. An experimental dual-mode converter CMOS IC was demonstrated for functionality for a input supply of 1.4 V; however the designs can be extended to other process technologies with the minimum voltage of $V_T + 3\ V_{DS\_SAT}$.

F. Low Voltage Buck-Boost Converter without External Schottky Diodes

When the dynamic converter's output voltage is below the threshold voltage of the a PMOS transistor, the output synchronous switch of a buck-boost converter remains off. Under this condition, the load current is delivered through the body diode, thereby incurring significantly higher power losses compared to synchronous switch operation. An external Schottky diode, because of its smaller on voltage drop, is typically used to improve the efficiency. In this research, by introducing a transmission gate synchronous switch (PMOS and NMOS connected in parallel), the buck-boost converter is operated with high efficiency, except for a small region of input-output voltage combination. This solution however increases the die area in an integrated circuit environment, while reducing one external component and associated cost with respect to PCB real estate and assembly.

G. Design and Development of Operational Amplifier With Large Input Common-Mode Range For Wide Supply Voltage Range

Operational amplifiers as error amplifier in the PWM switching regulator and voltage-to-current converter for dynamic gate bias generation in an RF PA require large ICMR to accurately control the converter's output voltage and PA's bias current over a wide range, respectively. With a supply voltage less than the sum of threshold voltages of PMOS and NMOS, use of complementary pair without any modification is not possible. This handicap is overcome by using a dynamically adaptive supply voltage dependant common-mode feedforward circuit to adjust the common-mode input signal for the main amplifier while keeping the differential signal unchanged.

H. Intuitive, Non-Mathematical Small-Signal Modeling for Switching Converter

An intuitive approach to small-signal modeling and analysis of switching converters is developed. The converter's model is developed based on the circuit's operation without navigating through complex mathematical formulations, e.g., state space matrix formulation. The simplified approach is appropriate for analog circuit designers involved in power management IC design and can be found useful in a *pedagogic* environment.

Table 8.1 summarizes the original contributions of the research presented in this dissertation. Research work presented in this dissertation has led to the publication and submission of several journal papers and conference papers, the list of which is given in Appendix –II.

8.3 Future Work

The concepts proposed and demonstrated in this dissertation can be extended to other PA-driven portable applications, e.g., wireless local area networks (LANs), with large transmitter power dynamic range. Portable systems are becoming more complex with their increase in functionality, thereby draining more power from the battery. Therefore, intelligent power management techniques, e.g., the one proposed and experimentally demonstrated in this dissertation, are expected to play a crucial role in the future portable handheld devices. Some of the possible extensions of this research are presented in the following subsections.

A. Efficient RF Transmitter System

The effect of converter's finite transient response while adjusting the PA voltage as a function of the output power can be evaluated by measuring transmitter's system performance, e.g., bit error rate (BER). Therefore, a complete transmitter implementation using the dynamically adaptive PA system is a logical future extension to the research presented in this dissertation.

Table 8.1. Summary of original research contributions.

System/Circuit	Area	Details
Energy-Efficient Linear RF PA	Efficiency enhancement	Power-tracking, dynamically adaptive dual-bias controlled linear RF PA
	Low voltage implementation	Power-tracking, buck-boost converter supplied PA
	System design	Design considerations for CDMA portable applications
		Calibration approach for RF transmitter using look-up table and variable gain RF PA
	Experimental linear RF PA	915 MHz center frequency 1.23 MHz baseband bandwidth CDMA RF PA with an adaptive supply and bias control
		1.96 GHz center frequency 3.84 MHz baseband bandwidth WCDMA RF PA with an adaptive supply and bias control IC
Noninverting Dynamically Adaptive Buck-boost Converter	Analysis and modeling	Intuitive non-mathematical time-averaged small-signal modeling
		Voltage mode design considerations and power loss analysis
	Low output voltage capability	Transmission-gate based synchronous rectification and output voltage enabled PMOS gate drive circuit
	Accurate peak-to-peak and average output voltage PFM	Conceptual development of supply voltage adaptive on-time adjustment in DCM operation
	Low voltage dual-mode converter	A top-down design approach of a PWM/PFM mode buck-boost converter IC with low supply voltage
		Determination of limiting values of switch resistance and accurate duty cycle control for proper converter operation
		Buck-boost power supply IC with dual-mode operation
Low Voltage Analog Circuits	Large ICMR op-amp	Power-supply tracking input common-mode reference voltage feedforward
Low voltage circuit design practices (amplifier, comparator, and reference topologies)		

Along with the high efficiency linear RF PA proposed and experimentally demonstrated in this dissertation, gain calibration, power control, and IF/RF signal-processing circuits can be combined to realize an efficient dynamically adaptive RF transmitter. Either an open-loop look-up table based approach or a closed-loop automated calibration scheme can be employed to realize the total dynamic range of the transmitter power.

B. Integrated Buck-Boost Converter with PA

With the semiconductor industry always looking for higher integration moving towards compact and low cost solutions, integrating the PA with the buck-boost converter can be pursued. Realizing an efficient PA in CMOS technology in itself offers several challenges, e.g., non-availability of high-Q passives for matching, lower breakdown voltages as feature size reduces. In a single-well CMOS process, isolation of the RF signal path from the switching transistor's harmonics can also be quite challenging. Nevertheless, successful realization of integrated CMOS PAs [102]-[105] have been reported in the literature. Although the CMOS PAs do not exhibit high efficiency when compared to GaAs, InP solutions, they can be combined with the dynamically adaptive efficiency enhancement system presented in this dissertation to leverage the advantage of a low cost process leading up to the realization of a low-cost solution.

C. Combined Efficiency Enhancement and Linearization Techniques

Incorporating linearization scheme, e.g., predistortion, seems a logical extension to improve the PA system efficiency further. If a closed-loop calibration technique is used in the RF transmitter implementation, there is no additional hardware is required to incorporate predistortion.

D. Dynamic Compensation and Digital Controlled Buck-Boost Converter

As required by the PA and elsewhere in a battery-powered environment, a non-inverting buck-boost converter critical to generate an output voltage that is higher or

lower than the battery voltage, *on-the-fly*, for higher efficiency and having the ability to operate the system at its peak performance even with a battery that is close to fully discharged. The compensation of the feedback control circuit in a dynamic output voltage environment imposes new challenges since the locations of complex conjugate poles and RHP zero change with frequency. Typically, the converter is compensated for stability considering the worst-case conditions while optimizing its feedback bandwidth. However, as the operating conditions the converter's feedback loop is no longer optimally compensated, which degrades the converter's performance.

Digital control for power ICs, although at its early infancy compared to the matured and well-established analog control, promises to offer flexibility like any other digital systems using a software programming. Recently reported literature [106]-[107] discusses the feasibility of digital control for switching regulators. However, the circuit complexity and therefore higher cost remains a major bottleneck before digital control is used in low cost portable systems.

8.4 Summary

A high-efficiency linear RF PA with a dynamically adaptive buck-boost power supply and bias control scheme is developed and experimentally demonstrated in this dissertation using discrete PCB level implementation as well as integrated circuit solution. The contributions of this research include the concept of power-tracking dual-bias control scheme, its ability to be operational over a wide supply voltage range with the use of a buck-boost converter. In the integrated circuit implementation, the use of a pulse-frequency mode controller with adaptive on-time control enables the PA to meet its linearity and improve standby performance of the system with lower quiescent current flow. The buck-boost converter supply and PA gate bias control ICs developed in this research demonstrates the suitability of the use of low–cost standard CMOS process technology for integrated power management of RF PAs. Low voltage circuit design techniques are used in IC design to achieve large dynamic range of converter's output voltage (0.5 – 5 V) from a minimum input supply of 1.4 V. The above functionality is

achieved by having an error-amplifier with input common-mode range (ICMR) of 0.1 -1 V throughout the input supply range of 1.4 -4.2 V.

This underlying conclusions of this research state that for maximizing the battery energy, both bias current and supply voltage must be adjusted, which however comes at the expense of higher complexity in the form of gain calibration circuits. Solutions with dynamic supply and bias control performed in discrete-steps can be used at the expense of a lower efficiency with simpler gain adjustment circuits. The optimal solution considering both complexity and efficiency lies in between the continuous control and discrete-steps. However, with the integration capabilities of state-of-the-art process technologies, complex circuits can be realized in smaller die areas. As the functionality in the PA-driven applications increases, solutions with longer battery life will eventually standout in the market place. Therefore, the supply voltage and bias currents of the RF PA with approximate 1-dB control, irrespective of its complexity, is expected to play a pivotal role in the future power management systems of RF PAs, because of its ability to achieve higher average efficiency and consequently longer battery life.

APPENDIX – I

Relationship between propagation delay with a step input and with a triangular wave drive

Consider a comparator with a single pole transfer function given by the expression

$$H(s) = \frac{H_0}{1 + \frac{s}{\omega_c}}, \tag{A1.1}$$

where H_0 is the DC gain of the comparator and ω_c is the dominant pole. For a step-input stimulus the comparator's output voltage is given by

$$V_{OUT}(t) = H_O V_{IN}\left[1 - \exp\left(-\frac{t}{t_c}\right)\right]. \tag{A1.2}$$

For a minimum input drive voltage equal to the resolution of the comparator (V_{IN_MIN}), its propagation delay is given by

$$t_p = t_c(\ln 2) = 0.693\, t_c, \tag{A1.3}$$

When a triangular wave input signal is used to drive one input of the comparator, its response can be is modeled by the following expression:

$$V_{OUT}(t) = \frac{V_{IN\_RAMP}}{T_r}\left[H_0 t - \frac{H_0}{\omega_c}\left\{1 - \exp\left(-\frac{t}{t_c}\right)\right\}\right]. \tag{A1.4}$$

In a comparator with triangular wave as its drive signal, to achieve the same propagation delay ($t_p = 0.693\ t_c$) as with a step input signal the following relationship holds true.

$$\frac{V_{IN\_RAMP}}{T_r} H_0 \left[t_p - \frac{1}{\omega_c} \left\{ 1 - \exp\left(- \frac{t_p}{t_c} \right) \right\} \right] = \frac{V_{IN\_MIN} H_0}{2}, \qquad \text{(A1.5)}$$

which yields

$$\frac{V_{IN\_RAMP}}{T_r} 0.193\, t_c = 0.5\, V_{IN\_MIN}. \qquad \text{(A1.5)}$$

Assuming the ramp signal rises to its required level in half the time as the propagation delay, the amplitude of the ramp signal is related to the resolution of the comparator by the expression:

$$V_{IN\_RAMP\_MIN} = 0.897\ V_{IN\_MIN}, \qquad \text{(A1.6)}$$

which signifies that the peak value of the ramp must rise to 1.8 times the minimum step-input voltage within the propagation delay of the comparator to achieve same propagation delay.

APPENDIX – II

LIST OF PUBLICATIONS

A. Published/Accepted

[1] **B. Sahu** and G.A. Rincón-Mora, "A high-efficiency linear RF power amplifier with a power-tracking, dynamically adaptive buck-boost converter supply," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no.1, pp.112-120, 2004.

[2] **B. Sahu** and G.A. Rincón-Mora, "A low voltage, dynamic, non-inverting, synchronous buck-boost converter for portable applications," *IEEE Transactions on Power Electronics*, vol. 19, no., pp. 443-452, 2004.

[3] **B. Sahu** and G.A. Rincón-Mora, "System-level requirements of DC-DC converters for dynamic power supplies of power amplifiers," *Proceedings of the IEEE Asia-Pacific Conference on ASICs*, pp. 149-152, 2002.

[4] **B. Sahu** and G.A. Rincón-Mora, "Adaptive power management of linear RF power amplifiers in mobile handsets – An integrated system design approach," Accepted for publication in the *IEEE Asia-Pacific Microwave Conference,* 2004.

[5] **B. Sahu** and G.A. Rincón-Mora, "A high-efficiency, dynamic, buck-boost power supply IC for portable applications," Accepted for publication in the *IEEE International Conference on VLSI Design*, 2005.

B. Projected

[6] **B. Sahu** and G.A. Rincón-Mora, "An intuitive approach to small signal modeling of switching regulators in continuous-conduction mode," Submitted to the *IEEE Transactions on Circuits and Systems (TCAS) - I*, 2004.

[7] **B. Sahu** and G.A. Rincón-Mora, "A low voltage, CMOS, pulse frequency mode step-down switching regulator with adaptive on-time control," To be submitted to the *IEEE Transactions on Circuits and Systems-II*, 2004

[8] **B. Sahu** and G.A. Rincón-Mora, "A low voltage, high-efficiency, dual-mode, dynamically adaptive, buck-boost power supply solution in standard CMOS process," To be submitted to the *IEEE Journal on Solid-State Circuits*, 2004.

[9] **B. Sahu** and G.A. Rincón-Mora, "An efficient WCDMA RF power amplifier with dynamically adaptive CMOS supply voltage and bias current control IC," To be submitted to the *IEEE Transactions on Microwave Theory and Techniques*, 2004.

[10] **B. Sahu** and G.A. Rincón-Mora, "Ultra low-voltage op-amp with high ICMR," To be submitted to the *IEE Electronic Letters*, 2004.

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VITA

Biranchinath Sahu was born and brought up in the village of Nodhana, in the state of Orissa in India. He attended the Maharaja Krushna Chandra (M.K.C.) High School and Maharaja Purna Chandra (M.P.C.) College, both situated in Baripada, India, for his secondary and higher secondary education, respectively. In 1993, he was enrolled in the premier engineering college in Orissa, University College of Engineering at Burla near the famous Hirakud dam, which is the longest earthen dam in the world. In 1997, he graduated with the Bachelor of Engineering (B.E.) degree in Electrical Engineering with highest percentage of marks among all the students in the entire university earning him a University Gold Medal for Academic Excellence. He was placed among the top fifty students in the all India competitive entrance examination, Graduate Aptitude Test in Engineering (GATE), for admission into the graduate programs in India.

After a brief work experience at the Power System Automation Group at Larsen and Toubro Limited in India, during that period he was also selected for the highly competitive Indian Engineering Services, he started his graduate program in Electrical Engineering in the Indian Institute of Technology (IIT), Kanpur, in July 1998. Upon successful completion of the Master of Technology (M.Tech.) degree in Electrical Engineering in January 2000, he started working for the VLSI CAD group in the Microelectronics Division of Lucent Technologies in Bangalore, India.

The burning desire of higher education and the quest of technical knowledge drove him towards the Ph.D. program at the Georgia Institute of Technology in Spring 2001. His graduate research at Georgia Institute of Technology has resulted in the publication of several journal and conference articles in the area of integrated power

management targeted for CDMA and WCDMA power amplifiers. During the graduate program, he worked one summer for Analog Devices, Inc., in Wilmington, MA, on the design and simulation of delta-sigma converters in Global System for Mobile Communication (GSM) codec. He also served as Senator in the Student Government at the Georgia Institute of Technology for the academic year 2001-2002 representing the School of Electrical and Computer Engineering. Upon graduation, he has accepted a full-time position with Silicon Laboratories, Inc. in Austin, Texas.