DESIGN AND RELIABILITY OF HIGH DYNAMIC RANGE RF BUILDING BLOCKS IN SOI CMOS AND SIGE BICMOS TECHNOLOGIES

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DESIGN AND RELIABILITY OF HIGH DYNAMIC RANGE RF BUILDING BLOCKS IN SOI CMOS AND SIGE BICMOS TECHNOLOGIES

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Dedicated to the Divine's Creation

BLISS, LOVE & JOY

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SUMMARY

The objective of the proposed research is to understand the design and reliability of RF front-end building blocks using SOI CMOS and SiGe BiCMOS technologies for high dynamic-range applications. This research leads to a comprehensive understanding of dynamic range in SOI CMOS devices and contributes to knowledge leading to improvement in overall dynamic range and reliability of RF building blocks.

While the performance of CMOS transistors has been improving naturally with scaling, this work aims to explore the possibilities of improvement in RF performance and reliability using standard layouts (that don't need process modifications). The total-ionizing dose tolerance of SOI CMOS devices has been understood with extensive measurements. Furthermore, the role of body contacts in SOI technology is understood for dynamic range performance improvement. In this work, CMOS low-noise amplifier design for high linearity WLAN applications and its integration with RF switch on the same chip is presented. The LNA and switches designed provide state-of-the-art performance in silicon based technologies.

Further, the work aims to explore applications of SiGe HBT in the context of highly linear and reliable RF building blocks. The RF reliability of SiGe HBT based RF switches is investigated and compared with CMOS counterparts. The inverse-mode operation of SiGe HBT based switches is understood to give considerably higher linearity.

A significant portion of this research has been published in peer-reviewed literature [7, 36, 38, 72, 73. 74, 75, 76].

CHAPTER 1

INTRODUCTION

1.1 Motivation

Radio-frequency (RF) front-end is a key building block in any wireless or communication system. A typical RF front-end includes an RF switch for transmit and receive mode switching, low-noise amplifier on the receive side, and power amplifier on the transmit side. The push for increasingly higher data rates, low-cost technology, and compact design drives much of the demand in wireless and supporting technologies that comprise the front-end. The challenging RF circuits, in particular, the RF front-end prove to be a limiting factor in reducing bandwidth, dynamic range, and sensitivity of the wireless communication system.

The basic topology of a RF transceiver is shown in Figure 1. A crucial component of the transceiver architecture is the RF front-end. For example, the power handling capability of the RF switch limits the amount of power that can be transmitted through the system. Moreover, the insertion loss of the switch also adds to the noise-figure of the receiver. The LNA has a direct impact on the receiver signal-to-noise ratio (SNR) and thus can restrict the maximum data rate, receiver sensitivity, and other receiver parameters. For wireless receivers, the SNR limits the minimum detectable signal and therefore limits the receiver dynamic range.

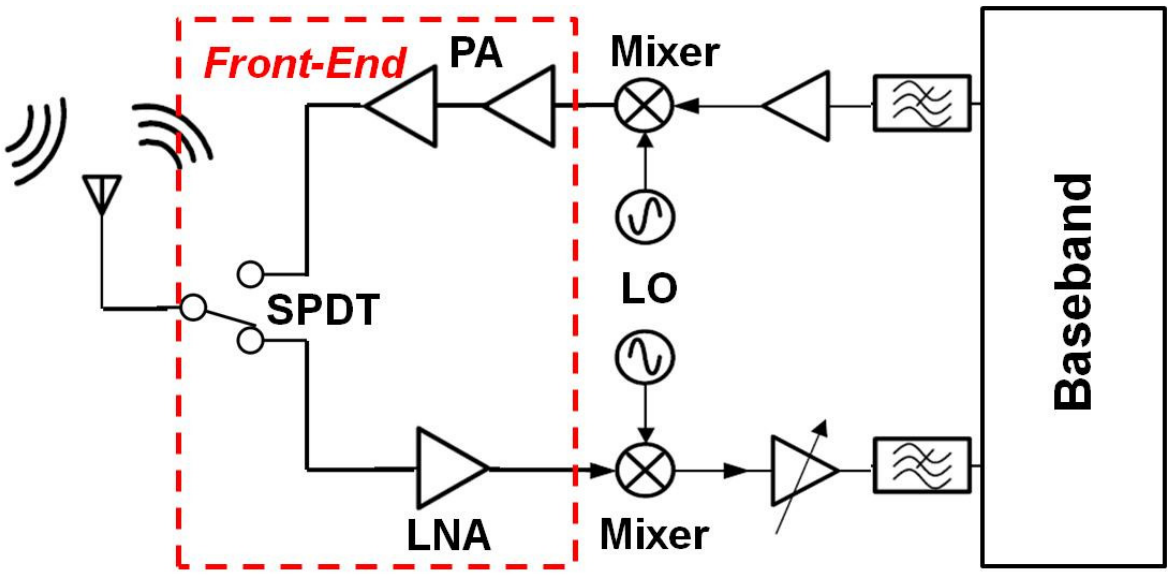


Figure 1. Block diagram of a typical wireless transceiver depicting the RF front-end.

"Dynamic Range" is defined as the power spanning from minimum to maximum usable signal levels in any wireless communication system. In a RF transceiver or front-end, the upper bound of dynamic range is typically limited by the functional block distortion characteristics and the lower bound is limited by the noise floor (or noise figure) of the system, as illustrated in Figure 2.

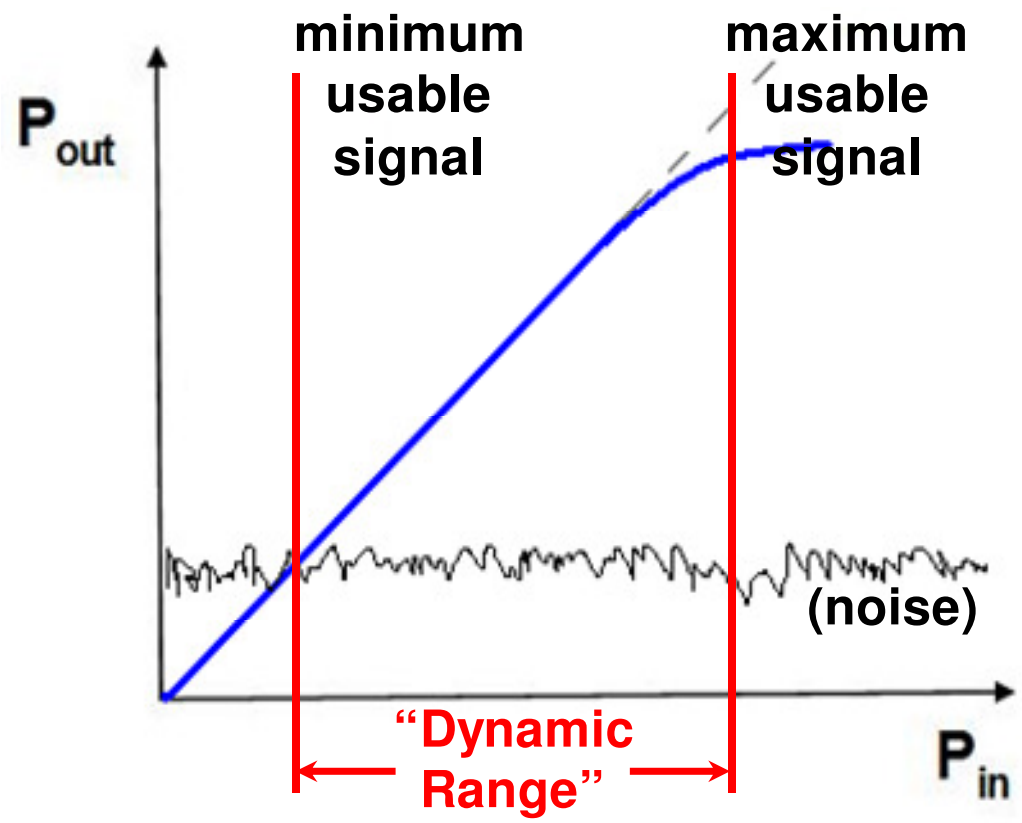


Figure 2. Dynamic range of a typical transceiver or wireless communication system.

1.2 Technology

CMOS technology has, in recent years, emerged as a genuine contender for RF and analog applications. These markets have traditionally been outside the scope of the relatively low-cost silicon-based technologies, and have been dominated by III-V and SiGe BiCMOS technologies. With the need for low-power and low-cost wireless solutions for consumer electronics, the historical demand for compound semiconductors and high-performance processes has been largely reduced for consumer applications. Instead, the focus of industry has moved towards using CMOS technology for analog baseband and RF front-end modules by integrating multiple functions on the same chip

and package, using System-on-Chip (SoC) and System-on-Package (SoP) approaches, respectively. CMOS technology allows the integration of digital functionalities which can control high-frequency and high-speed analog circuits and digital compensation for non-ideal effects.

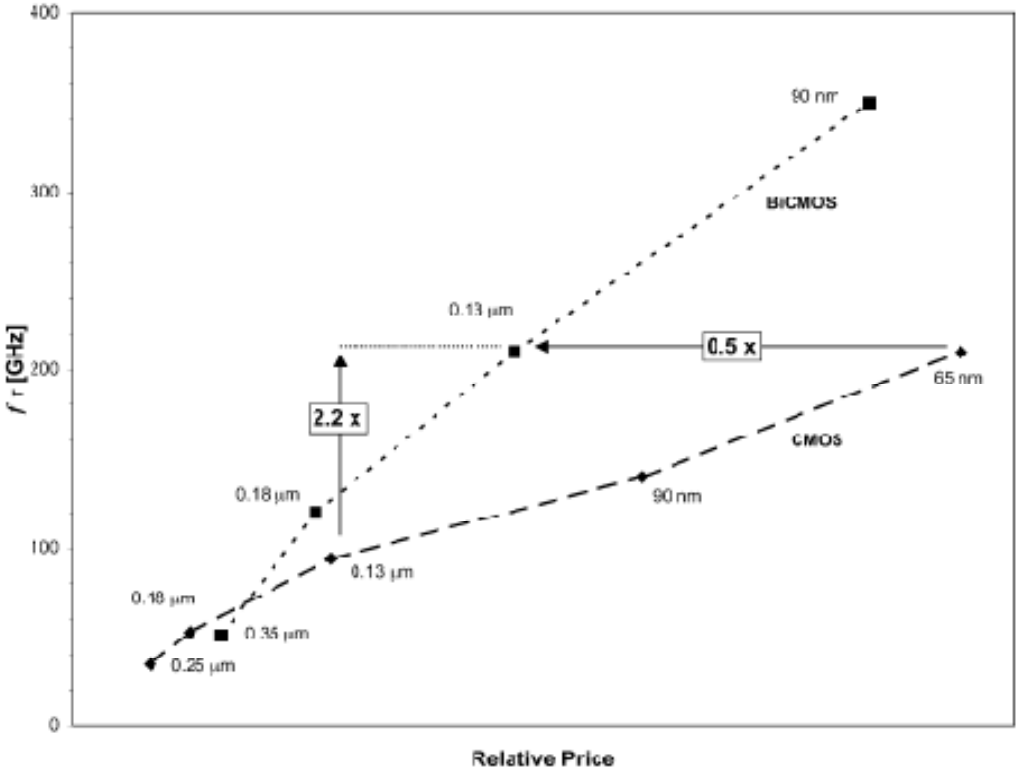


Figure 3. Illustration of price-performance comparison between BiCMOS (HBTs) and CMOS (NFETs) [12].

RF-CMOS remains the optimal choice for low-cost RF applications where the SiGe HBT performance is not fully required, due to thr lower mask count in CMOS process. A typical RF-CMOS technology can be considered primarily as an enhancement on the base of digital CMOS with improved RF models, design automation, and passive

devices built from the existing base process. There may be additional process adders (masks) to improve the FET performance from a RF standpoint. Typically, higher resistivity or SOI substrate is another enhancement introduced in the RFCMOS process relative to the base CMOS technology. High-performance features such as MIM capacitor, thick analog metal for inductors, high-gain FETs, hyperabrupt varactors, etc., are modularly introduced and can be utilized with appropriate cost-performance tradeoff considerations. Integrating a bipolar transistor with CMOS adds masks and processing steps which necessarily raises the cost of producing the wafer. Figure 3 compares the relative cost and performance of BiCMOS and CMOS technologies by looking at the of the NFET and SiGe NPN for various technology nodes [12].

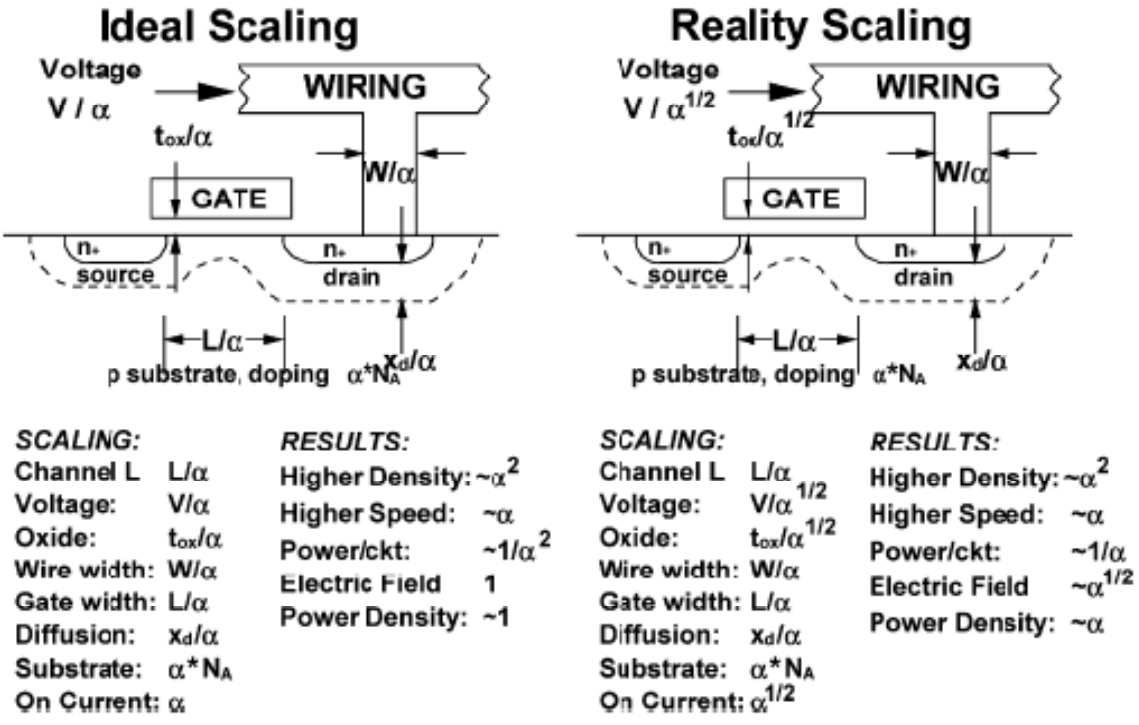


Figure 4. CMOS scaling parameters showing the concepts of “ideal” and “real” scaling [12].

Figure 4 summarizes the "ideal" and "real" CMOS scaling methodology. All dimensions of the device are scaled with the same scaling factor 'α' in ideal scaling methodology to ensure that the electric field remains constant from one generation to the other. The reality scaling guidelines in Figure 4 illustrate the two departures from ideal scaling methodology i.e. supply voltage (V_{DD}) and gate-oxide thickness (t_{ox}). Thus, both performance and density increase but at a cost of the power density.

As a result of CMOS, the high-frequency performance of CMOS devices has undergone considerable improvement, resulting in devices with peak cutoff frequency (f_T) currently greater than 450 GHz [1]. This impressive improvement in speed provides RF enablement to a simple digital CMOS technology, while being a low-cost adder. A combination of process innovations and lithographic scaling has been used to improve CMOS performance. These innovations include SOI substrates, strained silicon layers for mobility enhancement, double gated devices and fully-silicided or metal gates [2, 3]. Among available choices, SOI technology provides added advantages over bulk CMOS technology by minimizing parasitic, improving isolation, decreasing leakage, improving short-channel effects, and enhancing single event upset (SEU) tolerance. This performance improvement, combined with high-density integration capability, cost effectiveness and process maturity makes SOI CMOS technology attractive for integrating both RF front-ends and base-band analog/digital circuitry onto a single chip.

In this thesis, we evaluate two commercially available CMOS technologies from IBM. While the 65 nm CMOS technology is evaluated more from a radiation standpoint [72, 73], the 180 nm bulk and SOI CMOS technologies are used to design RF front-end circuits [75, 76].

The operation of SOI CMOS devices in the floating-body and body-tied mode has been thoroughly investigated for digital applications. In the digital world, the body-tied operation was used to control the floating-body effects in digital logic, where the transistors showed kink-effect [4]. In addition to the area penalty, the high-frequency performance of body-contacted SOI CMOS devices is degraded due to additional parasitic from different body-contacting schemes. However, as is demonstrated in Chapter 2, an auxiliary benefit of using body-contacting schemes has been the simultaneous improvement in the total-dose radiation tolerance of SOI CMOS devices, which to date has been largely ignored in the literature due to the widely perceived performance shortcomings in body-contacted SOI devices. In the present context, different body contacts refer to the T-body, and H-body orientations for accessing the thin silicon body [Figure 5].

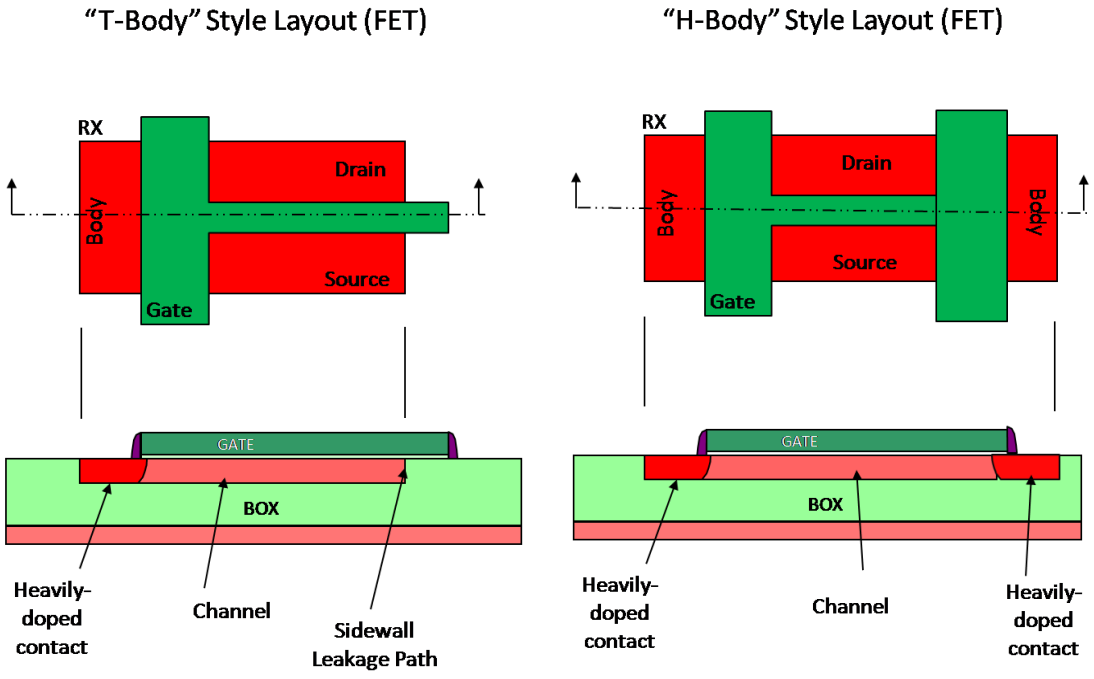


Figure 5. Top view schematic and cross-section of two widely used body contacting schemes in SOI MOSFETs.

The impact of floating-body effects on the analog performance of SOI devices has also been investigated before [5]. It was found that third-order harmonic distortion and noise are very sensitive to floating-body induced kink or deviation of output conductance and a body tie was necessary to maintain comparable distortion performance with the bulk counterparts. With aggressive scaling, however, the linearity performance of the transistors degrades (as will be shown). It is therefore logical to revisit the use of body contacts in a state-of-the-art SOI CMOS technology (45 nm), to quantitatively assess the impact of generational scaling and role of body contacts for improved high-frequency performance. The significance of using body-contacts to maintain a fixed body potential in these devices is explored from a dynamic range standpoint. The addition of body contacts to the compact layout of the 45 nm n-MOSFETs degrades the linearity at lower bias. Finally, improved understanding of the linearity should potentially lead to better circuit design for high dynamic-range using SOI CMOS technology, which is clearly relevant to a number of small-signal and large-signal circuits.

1.3 Switch and LNA Design

Multi-standard radio integration requires complex transmit/receive switching capabilities as highlighted in Section 1.1. Key switch performance parameters include not only insertion loss and isolation, but power handling capability as well. Typical switch performance parameters and their importance is highlighted below and illustrated in Figure 6:

- **Insertion Loss** (dB) is the measure of power lost due to the switch. A higher insertion loss implies lower overall power amplifier efficiency. The insertion loss of a switch is proportional to the on-resistance (R_{on}) of the FET.
- **Isolation** (dB) is the measure of power coupled form one node to the other. Higher isolation is required to protect LNA while PA is transmitting. This parameters is proportional to the off-capacitance (C_{off}) of the FET.
- **Power Handling P1dB** (dBm) of the switch can be converted to the drain to source breakdown voltage (BV_{DSS}) of the FET. A large number of FETs are stacked to handle the large peak voltage swing. For example, in a typical GSM environment, the peak voltage can be up to 30V under 6:1 mismatch.

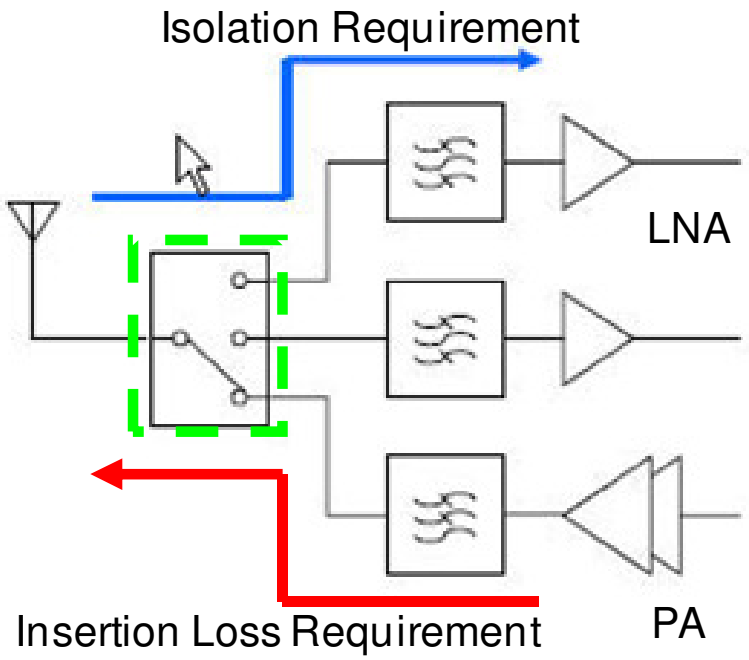
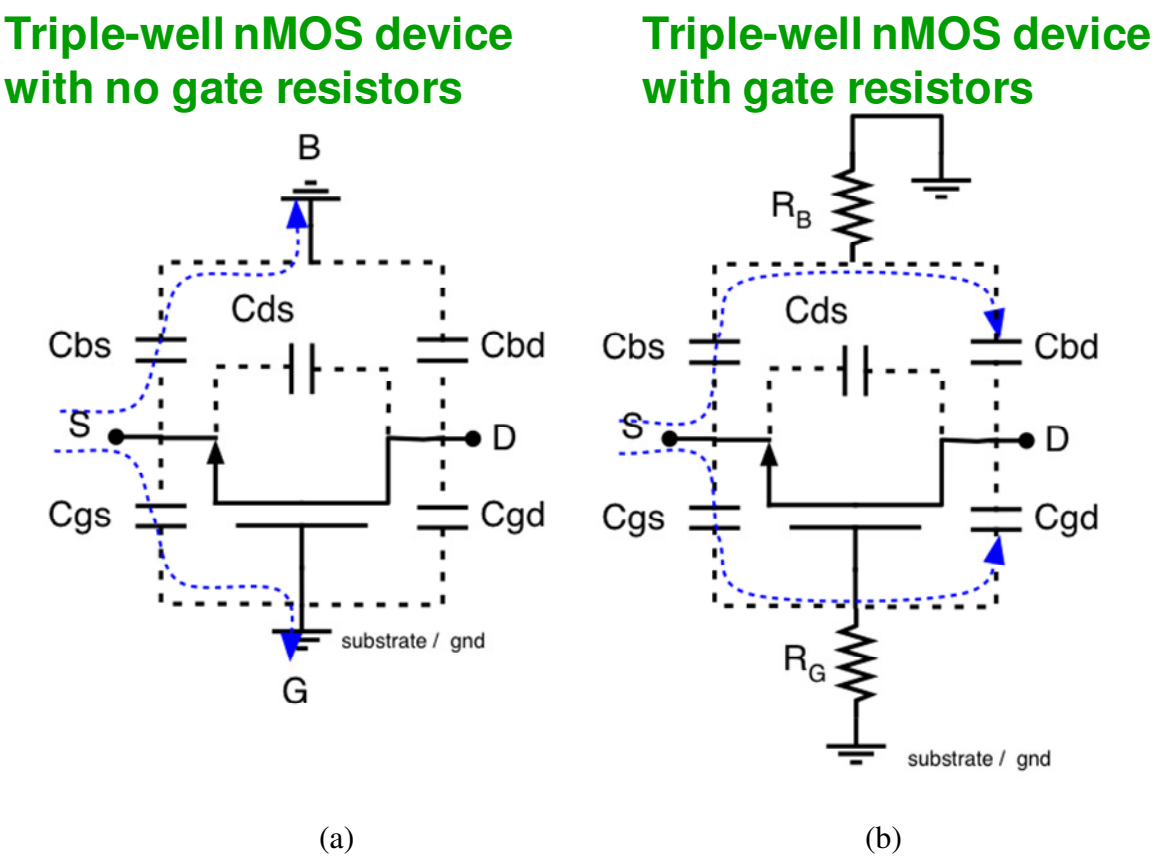


Figure 6. Section of a RF front-end, highlighting the key performance metrics for a front-end switch.

High linearity and constant group delay over modulation bandwidth in RF switches are critical to ensure that the amplitude and phase information of the modulated signal is maintained, and to prevent intermodulation distortion. While the addition of body contacts may be crucial for high linearity RF amplifiers on SOI, floating body devices are generally used in RF switch design to minimize the C_{ds} [8]. SOI technology is particularly interesting for RF switch design since parasitic junction capacitances are lower than the bulk CMOS technology. However, high linearity performance can be achieved in bulk CMOS switches (as will be demonstrated here) by layout optimization and careful treatment of parasitic in the switch design and layout, without any design rule violations, as demonstrated in Chapter 4. Triple-well CMOS devices are generally added to a standard technology to improve switch insertion loss. The trade-off of using a triple-well technology is better understood by a comparison of parasitic capacitances between a standard n-MOSFET device and an isolated triple-well device as shown in Figure 7 [9].

In addition, SiGe HBT technology is rapidly entering the world of wireless and radar applications, particularly at higher frequencies. RF switches have been realized in SiGe BiCMOS technology by incorporating diode-connected HBTs as series elements, and pMOS pull-up transistors to act as shunting elements [10]. Due to higher non-linearity in SiGe HBTs compared to CMOS transistors, systems with high linearity or dynamic range requirements typically employ CMOS-based RF switches. However, when the SiGe HBT is operated in inverse-mode as a switch, it is shown in Chapter 4 that considerable improvement in linearity and compression point of the switch is obtained. The proposed circuit enables a wide variety of RF and mm-wave applications where high power levels are needed.



(a) (b)

Figure 7. Comparison of (a) non-isolated switch and (b) triple-well isolated n-MOSFET switch with floating body [9].

Currently, the majority of front-end radar and wireless modules use p-HEMT based switches, which are fabricated on III-V technologies [11]. The idea of a high dynamic range silicon-based RF switch with high power handling capability is clearly desirable for low-cost integration. Even though we show that high linearity can be achieved in both CMOS and SiGe HBT based switches, the high RF power handling capability and robustness of silicon-based switches has not been addressed in the literature. Both CMOS and SiGe-BiCMOS based switch designs are investigated and compared for their power handling capability under RF stress in Chapter 5. Improved

understanding of the breakdown mechanism will potentially lead to better design of CMOS switches operating under high power conditions, clearly relevant to a number of large-signal circuits.

The learning from improved linearity in body-contacted devices is applied to SOI low-noise amplifiers in Chapter 6. The LNA design involves tradeoffs between noise-figure (NF), gain, power dissipation, input matching, and linearity in the output signal. The standard cascode topology design is applied to LNA design using both floating-body and body-contacted devices at 5 GHz. The floating-body device based LNA delivers state-of-the-art performance with sub-1.0 dB noise figure, while maintaining high linearity. The body-contacted FET LNA performance is compared with the floating-body LNA. Due to the extra gate resistance and better control of body potential relative to source, the body-contacted FET based LNA is seen to have higher NF, but marginally better intermodulation performance. The improvement in the intermodulation performance is explained using third-order derivatives of DC characteristics, also used in Volterra analysis.

Due to extensive CMOS scaling (sub-100 nm) and integration of the RF transceiver with the baseband, it has become extremely difficult to integrate the RF front-end on the same chip to obtain the desired performance. Thus, a standalone front-end module is typically used, which includes performance critical blocks such as the RF switch, the low-noise amplifier on the receive side, and the power amplifier on the transmit side. This approach necessitates RF front-end modules with switch and LNA functionality on the same chip, for use with WLAN chipsets. WLAN front-ends have been historically dominated by GaAs platforms because of their superior high power

handling capability and semi-insulating substrate. Owing to low mobility, high substrate conductivity, low breakdown voltage, and various parasitic parameters of CMOS processes, it is very challenging to design CMOS switches and LNA to simultaneously achieve low-insertion loss, high isolation, wide bandwidth, high power handling and low-noise comparable to their GaAs counterparts. In Chapter 7, the first implementation of a single-chip fully-integrated SP3T and LNA front-end on 0.18 μm CMOS is reported for 802.11b/g WLAN applications at 2.5 GHz. The integrated solution includes on-chip dc blocking, bypass-mode, matching network and ESD protection and drives the die-size (0.64 mm^2) towards a low-cost, fully-integrated solution.

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CHAPTER 2

THE ROLE OF BODY CONTACTS IN SOI

2.1 Introduction

In this chapter, we discuss the role of body contacts in mitigating total ionizing damage in SOI CMOS technology. Ionization damage in semiconductor devices is initiated when electron-hole-pairs (ehps) are generated along the track of secondary electrons emitted via photon-material interactions. Protons and other charged particles also generate ehps that lead to ionization damage. The total amount of energy deposited by a particle that results in ehp production is commonly referred to as total ionizing dose (TID). The typical unit of TID is rad, which denotes the energy absorbed per unit mass of a material. The possible physical processes leading to the creation of ionization defects are depicted in Figure 8 below. Since electrons have much higher mobility than holes in oxides, they are rapidly swept out of the dielectric [12].

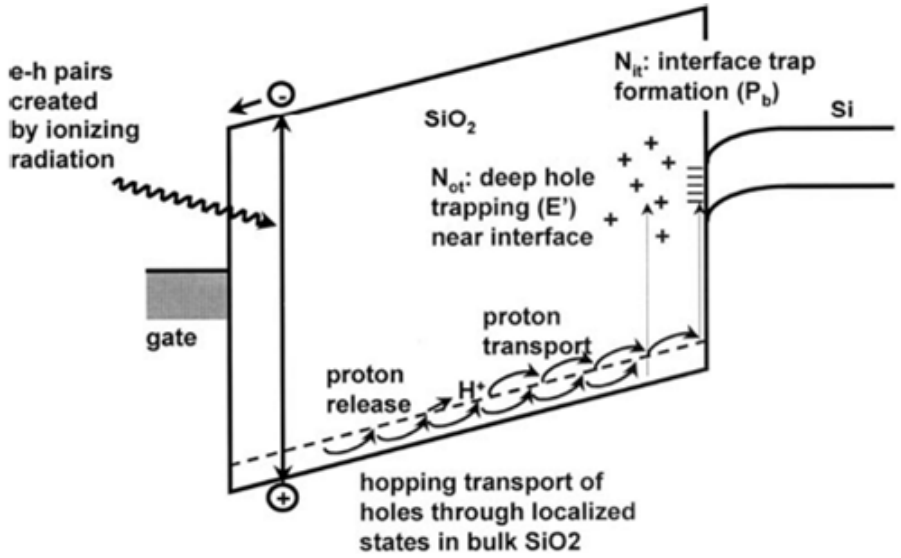


Figure 8: Major processes responsible for inducing TID damage in MOSFET [13].

In modern CMOS technologies, susceptibility of gate oxide to radiation-induced damage is reduced primarily due to the fact that defect buildup in gate oxides scales with t_{ox} [14]. Gate oxide hardness trends have continued to be observed in 0.25µm (t_{ox} = 6nm), 0.18µm (t_{ox} = 3.2nm), and 0.13µm (t_{ox} = 2nm) respectively [15], [16]. However, defect buildup in thicker isolation oxides is the major cause of radiation-induced degradation in modern CMOS devices. The STI oxide thickness is typically greater than 300nm in advanced CMOS technologies. The thick buried oxide (BOX) in SOI technologies is also susceptible to radiation damage.

2.2 Radiation Reliability

Advances in CMOS technology have enabled system-on-a-chip applications through the integration of analog and radio-frequency (RF) circuit blocks with conventional digital CMOS. This combination of a traditional digital CMOS technology with RF-optimized process elements (e.g., n- and p-channel transistors, passive elements, and thick top metal) is commonly termed RF-CMOS. Importantly, RF-CMOS transistors typically employ very large numbers of gate fingers (50 – 200) in order to boost transconductance and frequency response to >200 GHz levels. A combination of new materials, strain-engineering, and lithographic scaling is used to further improve performance to support demanding RF circuit functions [17]. The scaling trends in digital CMOS have a strong influence on the RF CMOS roadmap. For example, the f_{MAX} scaling and broadband noise can benefit from the lower resistance of fully silicided gates, but the flicker (*1/f*) noise may require added attention as new gate materials are introduced.

RF-CMOS on SOI technology provides additional advantages over bulk RF-CMOS,

by decreasing leakage and improving short-channel effects. In the RF context, SOI helps by minimizing parasitics and also improves device-to-device isolation at high frequencies. From a radiation perspective, SOI is known to enhance single event upset (SEU) tolerance. This performance improvement, coupled with its high-density integration capability, cost effectiveness, and process maturity, makes RF-CMOS on SOI technology attractive for integrating both RF front-ends and base-band analog/digital circuitry onto a single chip for emerging space-based systems.

The proton tolerance of 180 nm and 130 nm bulk CMOS technology has been previously studied from both *dc* and RF standpoints [18, 19]. High-quality ultra-thin gate oxides in aggressively-scaled CMOS technologies are known to exhibit reduced sensitivity to total dose irradiation. However, isolation-oxide and buried-oxide damage (in CMOS on SOI) can potentially impact the total dose tolerance. The total dose radiation response of partially depleted RF-CMOS on SOI transistors has been investigated using X-ray and proton sources [20]. Although the radiation tolerance of a 90 nm SOI technology has been reported [21], the radiation response of more advanced SOI CMOS technology nodes has not been understood, especially from a RF standpoint. The total ionizing dose-induced degradation mechanisms in high-gate-finger-count 65 nm RF-CMOS on SOI devices are investigated for the first time. Both S-parameters and *dc* characteristics are employed to characterize the radiation damage and understand the underlying damage mechanisms in 65 nm SOI devices. The devices selected were laid out as multi-finger structures and padded out to enable on-wafer high-frequency measurements.

2.2.1 Experimental Details

Strain-engineered, partially-depleted RF-CMOS on SOI devices are investigated here for total ionizing dose radiation tolerance. The stress memorization technique (SMT) has been applied to a fully-integrated 65 nm RF-CMOS on SOI technology, complete with high Q on-chip inductors and capacitors, to enable system-on-chip integration of RF blocks with digital blocks [22]. A relaxed pitch layout for the RF devices yields peak f_t of 360 GHz and 260 GHz for the nFET and the pFET, respectively [23]. Fully silicided (FUSI), low resistance polysilicon gates were used with a thermally grown gate oxide of thickness 1.05 nm. The devices are designed for an operating V_{DD} of 1.0 V using a dual-well CMOS technology on p-type SOI substrate. For our analysis, we used 60 nm gate length, standard threshold voltage nFETs.

The devices selected were laid out as multi-finger structures and padded out to enable on-wafer high-frequency measurements. An Agilent 4156C Semiconductor Parameter Analyzer was used to perform *dc* device characterization at room temperature. For two-port S-parameter measurements, an Agilent E8361B network analyzer was used for RF measurements up to 40 GHz, both before and after irradiation. The conventional open-short de-embedding technique was used on the raw S-Parameters of the devices to de-embed the effects of pad parasitics. All measurements were performed at room temperature before and after the devices were exposed to a given proton radiation dose. These devices were also packaged into 28-pin DIP packages for cumulative total ionizing dose radiation testing. The *dc* characteristics of the devices were measured at room temperature. All terminals were grounded for nominal bias conditions, while the gate was biased at 1.0 V (V_{DD}) for worst-case conditions during exposure. The *dc* characteristics of

the devices were measured immediately after each cumulative dose was reached. All irradiated devices were of a multi-finger geometry, with different total width (1 µm, 2 µm, and 4 µm) and number of gate fingers.

Two separate ionizing radiation experiments were conducted to analyze the role of shallow-trench isolation in the device response. First, the samples were irradiated with 63 MeV protons at Crocker Nuclear Laboratory, at the University of California at Davis. A five-foil secondary emission monitor calibrated against a Faraday cup was used for dosimetry measurements. The radiation source (Ta scattering foils) was located several meters upstream of the target, and this established a beam spatial uniformity of about 15% over a 2.0 cm radius circular area. Beam currents from about 10 nA to 50 nA allow testing with proton equivalent gamma doses up to 2 Mrad(SiO_2). The dosimetry system has been previously described and is accurate to about 10% [24]. Additionally, devices were irradiated on-chip with all terminals floating using a 10 keV X-ray source at Vanderbilt University. A dose rate of 31.5 krad(SiO_2)/s was used to obtain equivalent gamma doses up to 2 Mrad(SiO_2). Since radiation damage can depend on device bias conditions during exposure, the results obtained from 10 keV X-ray exposure with floating terminals may not represent worst-case conditions. While X-ray exposure of packaged devices would be better to compare the response with proton radiation, packaging related electro-static discharge (ESD) issues allowed only floating terminal conditions in this experiment.

2.2.2 Impact on DC performance

Figure 9 shows typical I_D-V_{GS} transfer characteristics as a function of total accumulated dose for a 120-finger nFET with width and length dimensions of *W/L*=1.00/0.06 µm, after 63.5 MeV proton exposures. Even though we show the off-state leakage degradation in a 120-finger nFET, the device with 20-fingers also showed considerable degradation in off-current. Observe that the off-state leakage current is significantly degraded, even at a low V_{DS} of 50 mV. Thus, the impact ionization-induced floating-body effect (also referred to as 'total-dose latch' or 'snap-back effect') in these SOI devices can be ruled out [25]. Moreover, this effect is known to be more pre-dominant in fully-depleted SOI transistors [26, 27].

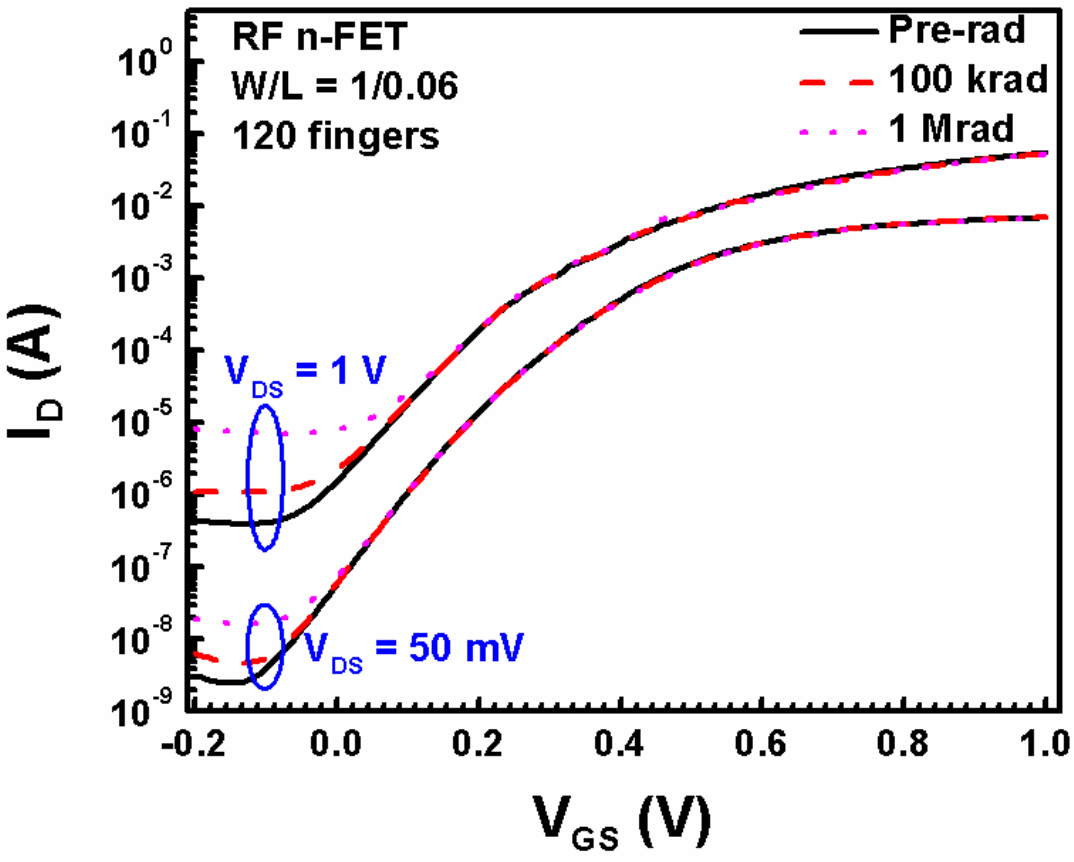
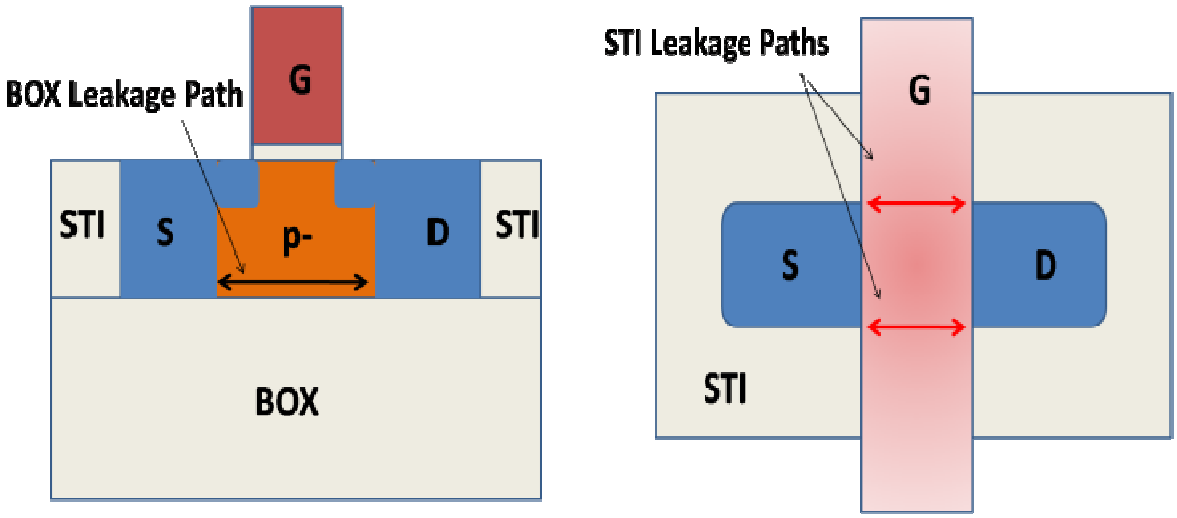


Figure 9. Transfer characteristics of the devices at different accumulated dose points for 63 MeV protons.

There are two possible radiation-induced parasitic conduction paths which can induce off-state leakage degradation consistent with what we observe. As shown in Figure 10(a), hole trapping in the much thicker buried-oxide (BOX) layer could result in a sheet of mobile electrons at the bottom of the active silicon layer, thus causing radiation-induced back-channel conduction between the source and drain, which reach to the BOX in these partially-depleted devices. On the other hand, the increase in radiation-induced leakage could potentially be a manifestation of a parasitic inversion channel where the gate overlaps the shallow trench isolation (STI), as shown in Figure 10(b).



(a) (b)

Figure 10. Possible radiation-induced leakage paths along the (a) surface of BOX, (b) STI sidewalls.

In Figure 11, it is observed that the same device has more off-state leakage degradation when the gate was biased at 1.0 V (V_{DD}) during exposure. The effect of parasitic inversion channel along the STI is aggravated in nFETs since one applies a positive front-gate bias during irradiation [28]. Moreover, one would expect the BOX

surface channel to be insensitive to front-gate bias during exposure. This result is highly suggestive of a STI-induced degradation mechanism in these multi-finger RF-CMOS devices, because each finger adds extra parasitic conduction paths along the STI edge, thereby contributing to the observed total radiation-induced leakage enhancement. These conduction paths may enhance the total drain current at high drain bias and make the floating body effect more pronounced, as shown in Figure 11.

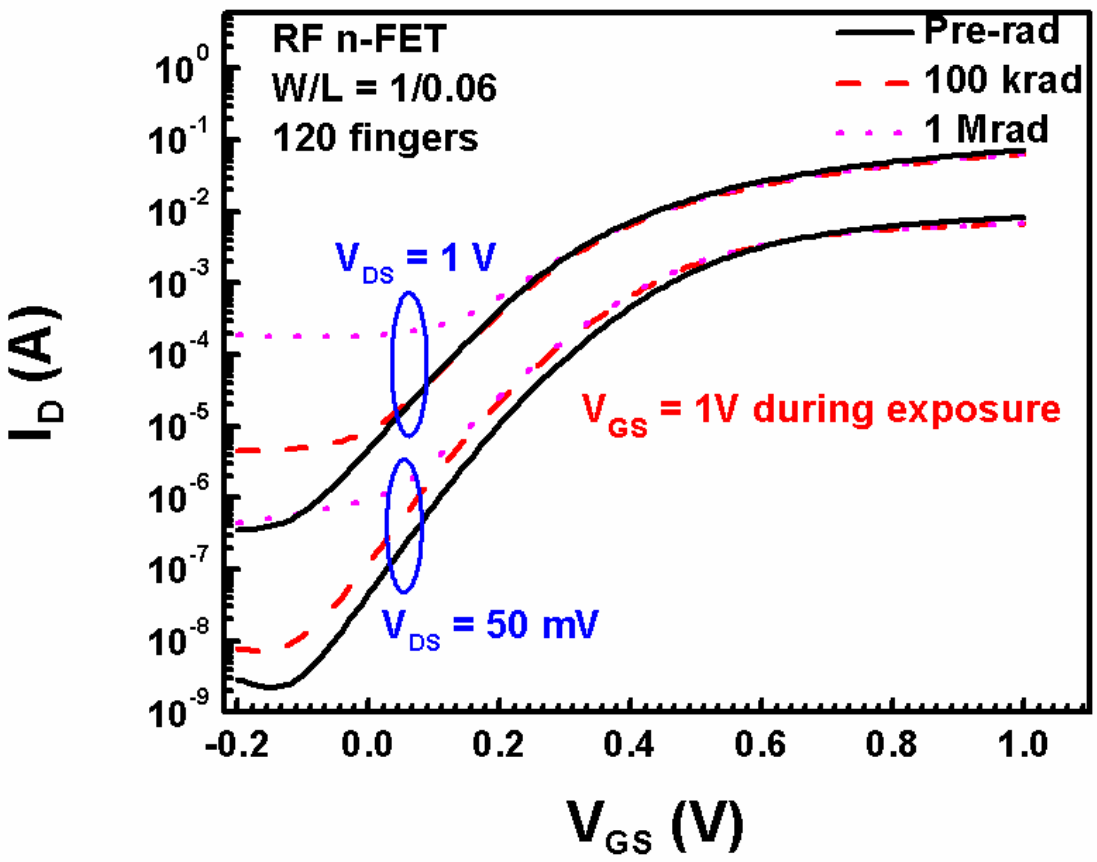


Figure 11. Enhanced degradation in off-state leakage when gate was biased at 1.0 V during proton irradiation.

Figure 12 shows the normalized change in off-state leakage as a function of accumulated dose. The enhancement in degradation with applied gate-bias during

irradiation is clearly visible. This is because each additional finger creates extra parasitic conduction paths along the STI edge, thus contributing to the total radiation-induced leakage enhancement. Additionally, it is shown that the damage can be reduced by decreasing the number of fingers. This reduction can be achieved by increasing the width of each finger, while maintaining the same total width of the device. However, gate resistance may start to dominate the small-signal RF response for longer finger-widths, thus reducing the RF figures-of-merit of the transistor.

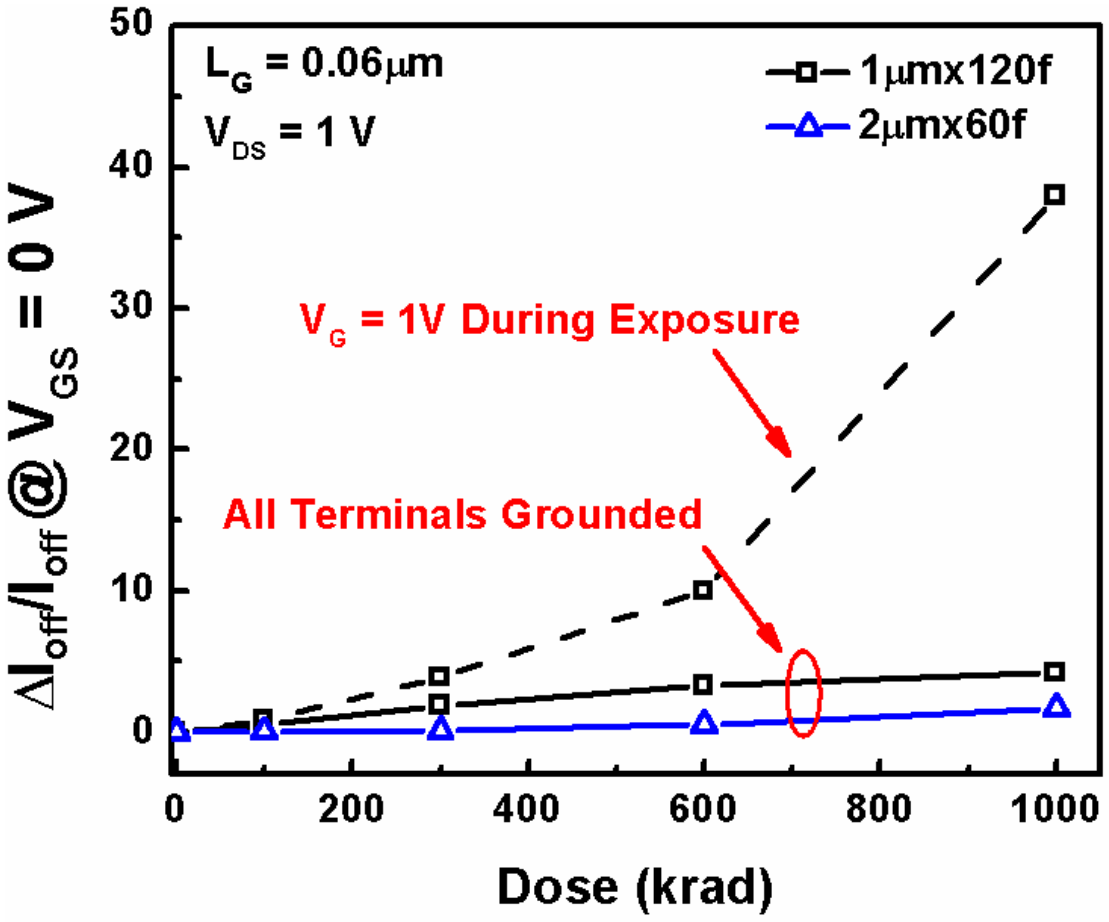


Figure 12. Normalized change in off-state leakage as a function of total accumulated proton dose.

Interestingly, the T-body contact eliminates the STI edge from only one end of the channel, while an H-body contact results in a completely edgeless device. We observed negligible degradation of a T-shaped body-contacted device, as shown in Figure 14. The effect of sidewall leakage at one end of a T-body contacted device is observed at a cumulative dose of 600 krad(SiO_2). Additionally, the back-gate characteristics of irradiated T-body devices indicate the presence of trapped charge in the buried oxide (Figure 14), which has negligible impact on the front-gate characteristics of the device in Figure 13.

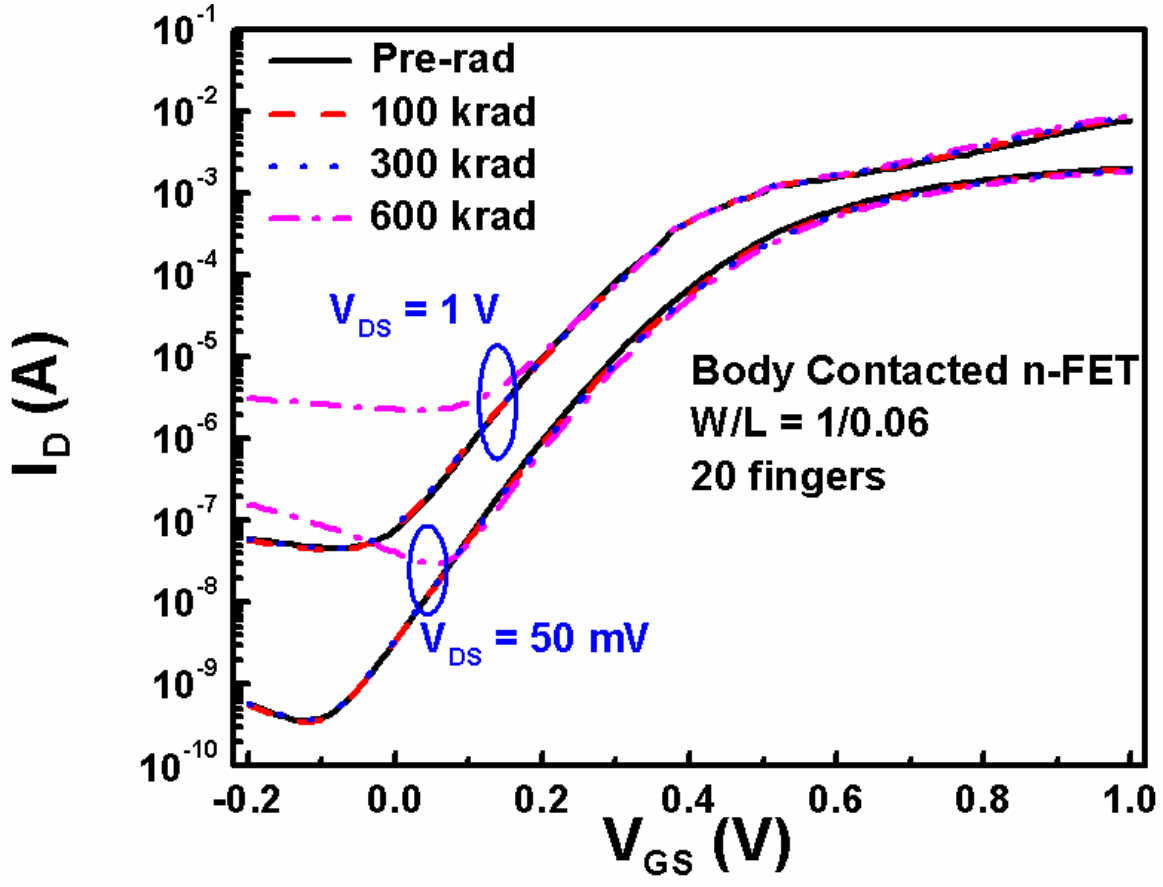


Figure 13. Transfer characteristics of a body-contacted device at different accumulated proton doses.

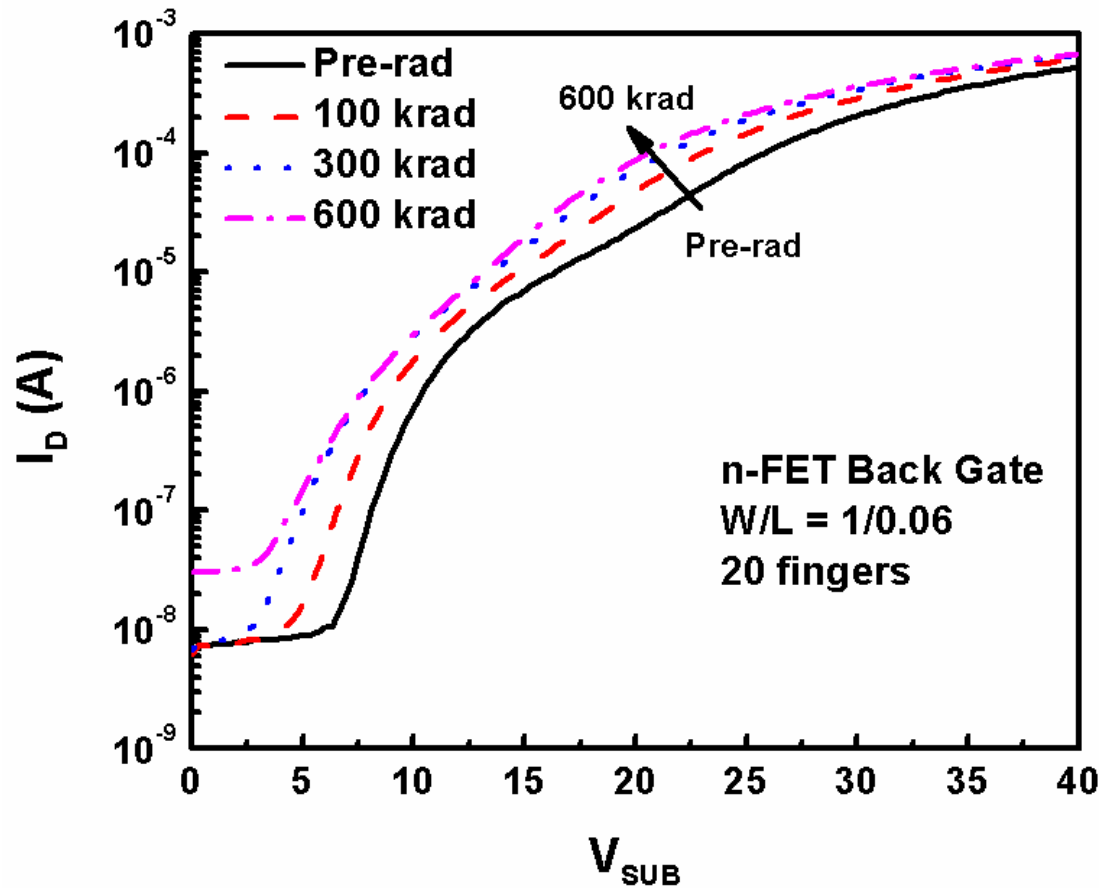


Figure 14. Back-gate characteristics of body-contacted device at different accumulated proton doses.

Radiation tolerance of edgeless devices (no STI) and H-gate topology available in a 90 nm SOI CMOS technology has been analyzed [21]. It was observed there that even though the back-gate threshold voltage was shifted due to BOX charge accumulation, the front-gate characteristics of the transistor remained unaffected up to a total dose of 300 krad. Thus, the observed radiation damage is understood to be dominated by an STI parasitic conduction path.

2.2.3 Impact on RF Performance

To achieve better RF performance (i.e., peak f_T and f_{MAX}), finger width in a multi-finger device plays a key role. Cut-off frequency (f_T) is seen to scale very well with inverse gate length, and is independent of finger width to a certain minimum value. This minimum value is dictated by the technology node, when the parasitic capacitance, C_{gs} and C_{gd}, dominate the device f_T, as indicated in equation (1) below:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \qquad (1)$$

A strong indicator of usable power-gain of the transistor is its f_{MAX}. f_{MAX} has a peak value at some optimum width, above which it is limited by physical gate resistance, and below which it is limited by parasitic losses in the FET structure, as shown in equation (2). The optimum device width shrinks as the unit gate resistance increases with smaller gate length in advanced technologies [12].

$$f_{MAX} = \frac{f_T/2}{\sqrt{g_{ds}(R_g + R_i + R_s) + 2\pi f_T R_g C_{gd}}} \qquad (2)$$

The total dose radiation tolerance is shown here to be worse for smaller finger width devices. This result potentially represents a fundamental tradeoff between achievable RF performance and total dose radiation tolerance. Moreover, high finger count is required for acceptable power-gain, which degrades the total dose tolerance due to extra parasitic conduction paths along the sidewalls of each finger. If the designer decides to use devices with longer finger width to accommodate total dose tolerance in

the circuit, the resulting lower power-gain or f_{MAX} of the device will impose a penalty on the achievable RF performance.

As discussed in Section 1.3.1, body-contacts can mitigate the effect of STI sidewall conduction. However, body contacting schemes come not only with an added area penalty, but with extra gate polysilicon strapping around the active region of the device. This gate polysilicon around the edges adds extra parasitic capacitance between gate-source (C_{gs}) and gate-drain (C_{gd}), respectively, thus degrading the high frequency performance of the device. Hence, the choice between longer finger width devices and body-contacted devices for total dose tolerance will depend on the technology performance and desired circuit specifications.

2.3 Impact on Linearity

To enable integration of scaled CMOS in wideband communication systems, it is important to ensure that the linearity of these scaled devices will be able to satisfy the expected demands of high P1dB compression point and low IMD product. It is shown in Figure 15 that the linearity of CMOS devices worsens with scaling. The 180 nm channel length n-MOSFET has the highest IIP3, followed by the 130 nm and 65 nm devices, respectively. However, the device noise-figure is expected to improve with CMOS scaling [12]. It is therefore important to investigate the impact of scaling on overall dynamic range of scaled CMOS devices.

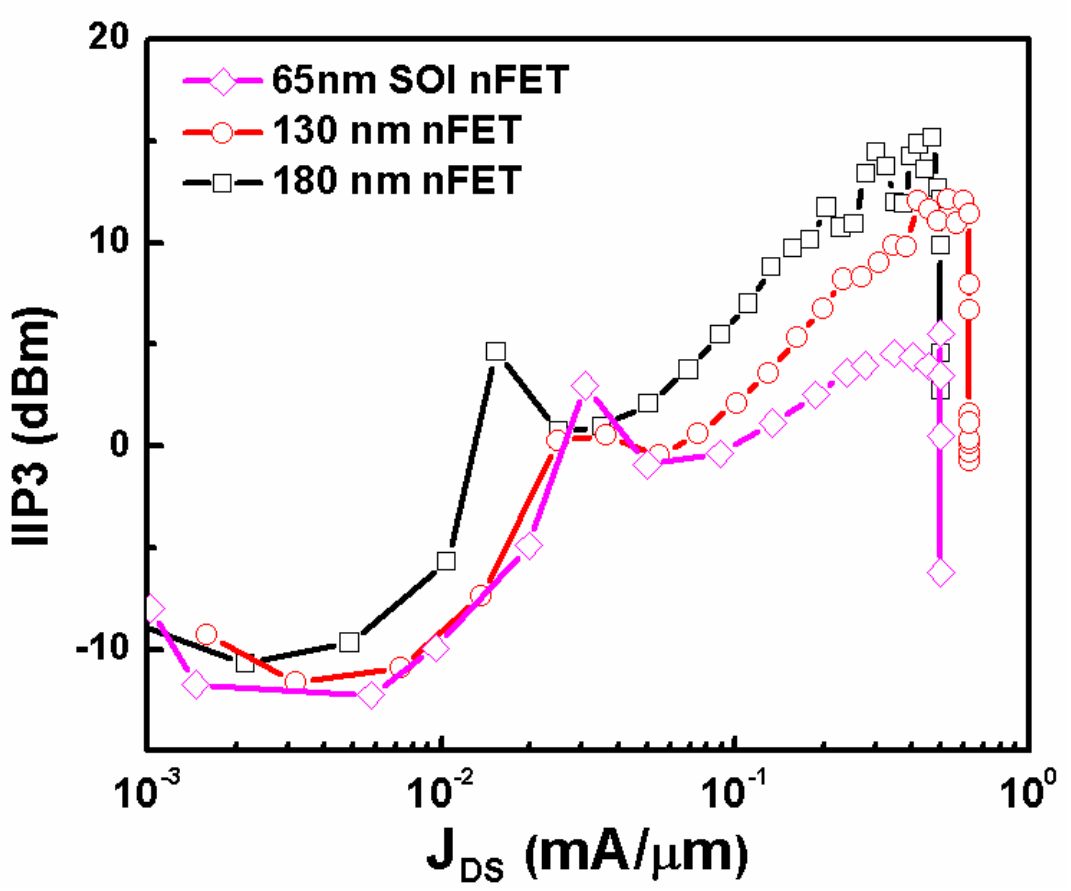


Figure 15. Impact of CMOS scaling on the device linearity.

Device linearity in the state-of-the-art, commercially available 45 nm SOI CMOS technology is investigated. As shown in Figure 16, the floating-body device linearity is compared with two different body-contacted devices. The notched-T body contacting scheme is used to reduce the extra gate-to-source and gate-to-drain capacitance in a T-body device, while controlling the body potential. The floating-body device provides the highest linearity in this technology. The body potential was tied to the ground during the linearity measurements of body-contacted devices. It should be noted that the body-contacted devices have a longer channel length (56 nm) than the floating-body device (40 nm), which may potentially be the reason for improved linearity in body-contacted

devices. However, the use of body-contacting schemes for high dynamic range LNA design will be investigated in Chapter 6.

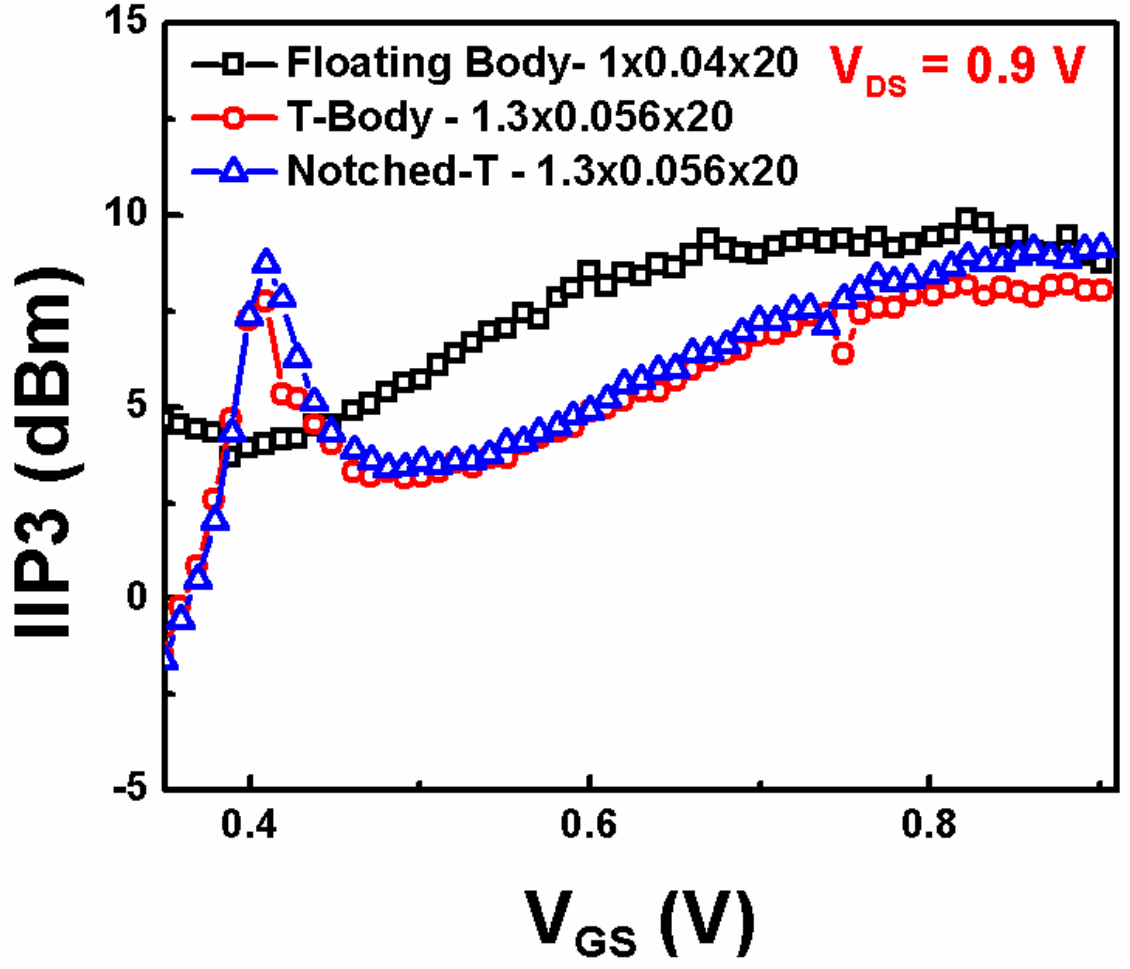


Figure 16. Comparison of linearity between floating-body and body-contacted devices in a 45nm CMOS on SOI technology.

CHAPTER 3

INTEGRATED S-PARAMETER AND LINEARITY CHARACTERIZATION

3.1 Introduction

A new and simpler linearity characterization approach is described, in which the power levels of the fundamental and the IM3 products are measured using a network analyzer, thus eliminating the need for the spectrum analyzer. The network analyzer used is capable of performing power sweeps at the desired frequencies along with S-parameter measurements. Measurements were performed on MOSFETs in a commercially-available 0.13 µm SiGe BiCMOS technology using this novel test setup. Harmonic balance simulations and IP3 analysis are performed to validate the measured results.

Figure 17 shows the block diagram of a conventional two-tone measurement setup. The two-tone signal is obtained by power combining the two RF signal generators which supply the fundamental and the second tone, respectively. Figure 18 shows the block diagram of the proposed setup. The measurement setup uses the power sweep feature of the network analyzer to measure non-linear distortion across bias in both transistors and integrated circuits. The setup shown in Figure 18 eliminates the need for a spectrum analyzer and an additional RF signal generator. Thus, the setup facilitates easy integration of linearity measurements with S-parameter measurement setup with minimal cost overhead.

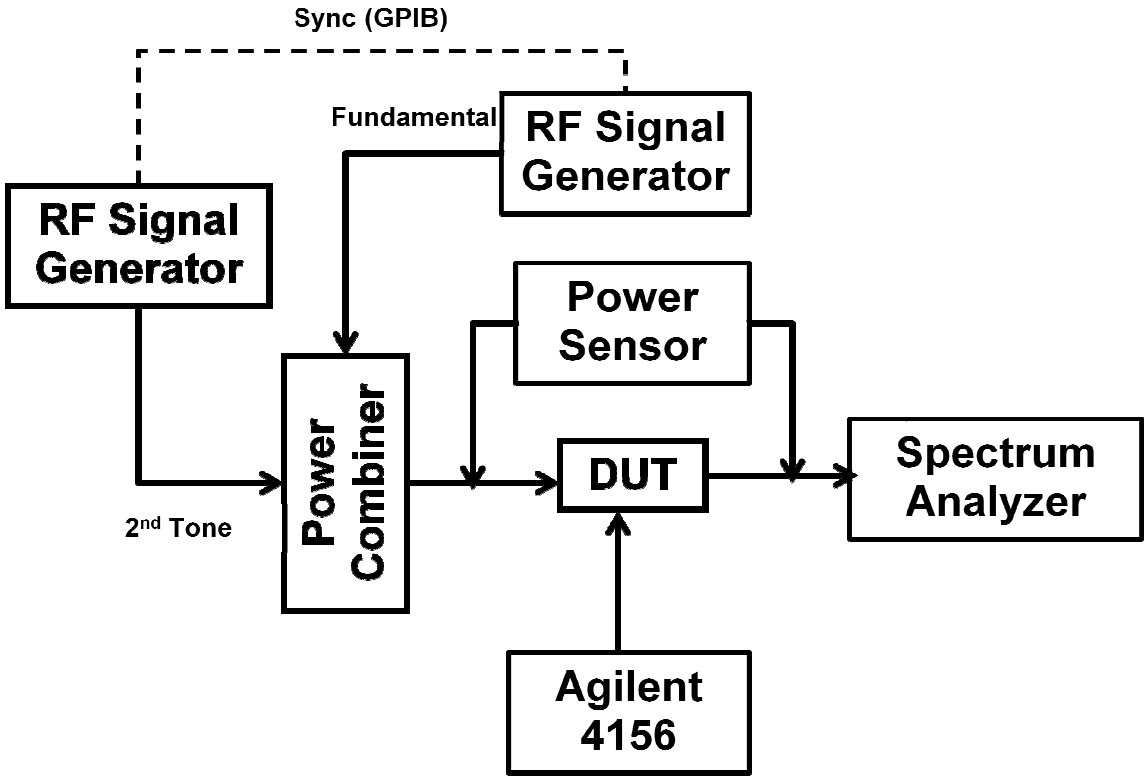


Figure 17. Block diagram of a conventional two-tone linearity measurement setup with spectrum analyzer.

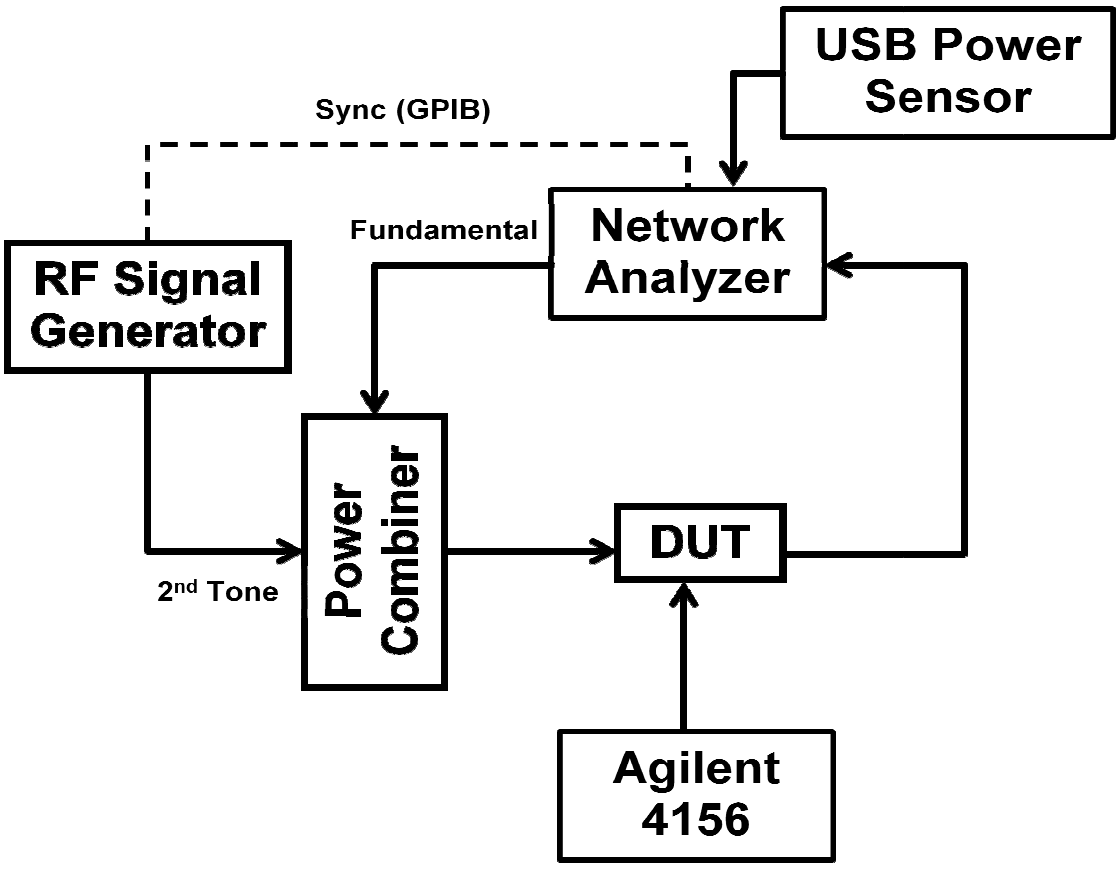


Figure 18. Block diagram of the test-setup proposed for two-tone linearity measurements integrated with S-parameter measurements.

The continuous-wave (CW) signal at the fundamental frequency is provided by the network analyzer. The network analyzer (here, an Agilent PNA E8361C) is synchronized in the time-domain with an external Analog Signal Generator, which provides the CW signal for the second tone. The signals are then fed into a power combiner and a two-tone signal is obtained at the input of the DUT. The device or circuit is biased using an Agilent 4156 Parameter Analyzer or with external DC supplies. The network analyzer is used to measure the power of the fundamental frequency, 2^{nd} tone,

and third-order harmonics at the output of DUT. The power sensor (Agilent U2002H) used for the power calibration is connected to the USB port of the network analyzer.

3.2 Measurement Results

Source power calibration is performed at four different frequencies (i.e., fundamental, 2^{nd} tone, IM3 low and IM3 high) using the power sensor. The output is received at the network analyzer. Four separate channels are set up in the network analyzer to receive the fundamental, 2^{nd} tone, IM3 low, and IM3 high signals, respectively. The source and receiver power calibration for each of these frequencies are loaded onto their respective channels. When the DUT is biased and input RF power is applied as a two-tone signal, the output power sweep for all four frequencies (channels) are then measured. For linearity characterization, minimum channel length n-MOSFETs with maximum supply voltage of 1.5 V and a total width (W) of 64 µm was chosen from a 0.13 µm SiGe BiCMOS technology for validation purposes [29]. The peak cut-off frequency (f_T) performance and transconductance of the device are shown in Figure 19. The fundamental frequency chosen for the linearity analysis is 9.5 GHz, with 10 MHz spacing for the 2^{nd} tone. The input power on the device was swept from -27 dBm to -15 dBm. IIP3 was measured as a function of gate bias (V_{GS}) at four different drain bias values (0.6 V to 1.5 V).

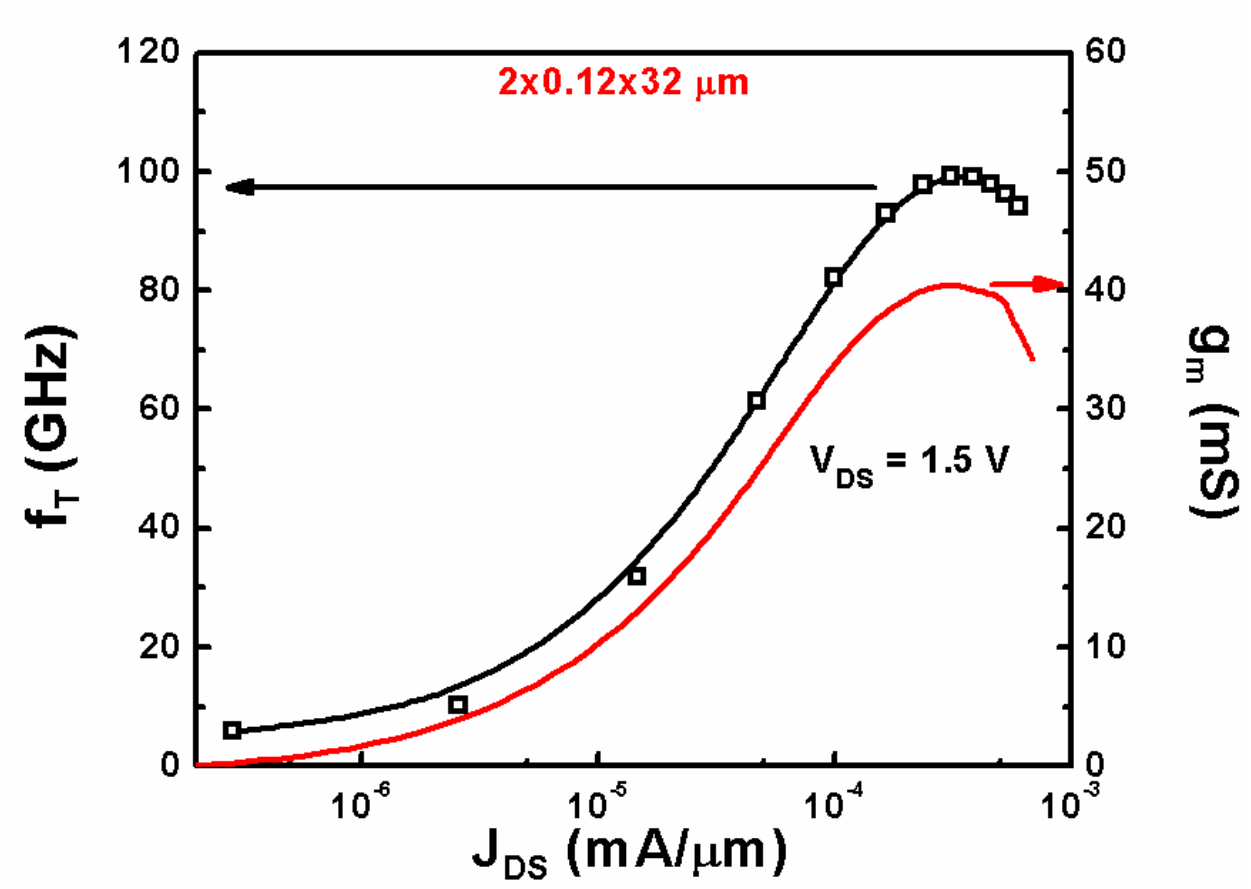


Figure 19. Peak f_T performance of the device under test and its correlation with g_m.

Figure 20 shows the measured power sweep on the device at a fixed bias. The IP3 point was extrapolated from the experimental P_{out} and IM3 curves and approximate 1:3 slope ratios were obtained, as expected. The measured IIP3 and OIP3 values are also shown in Figure 20.

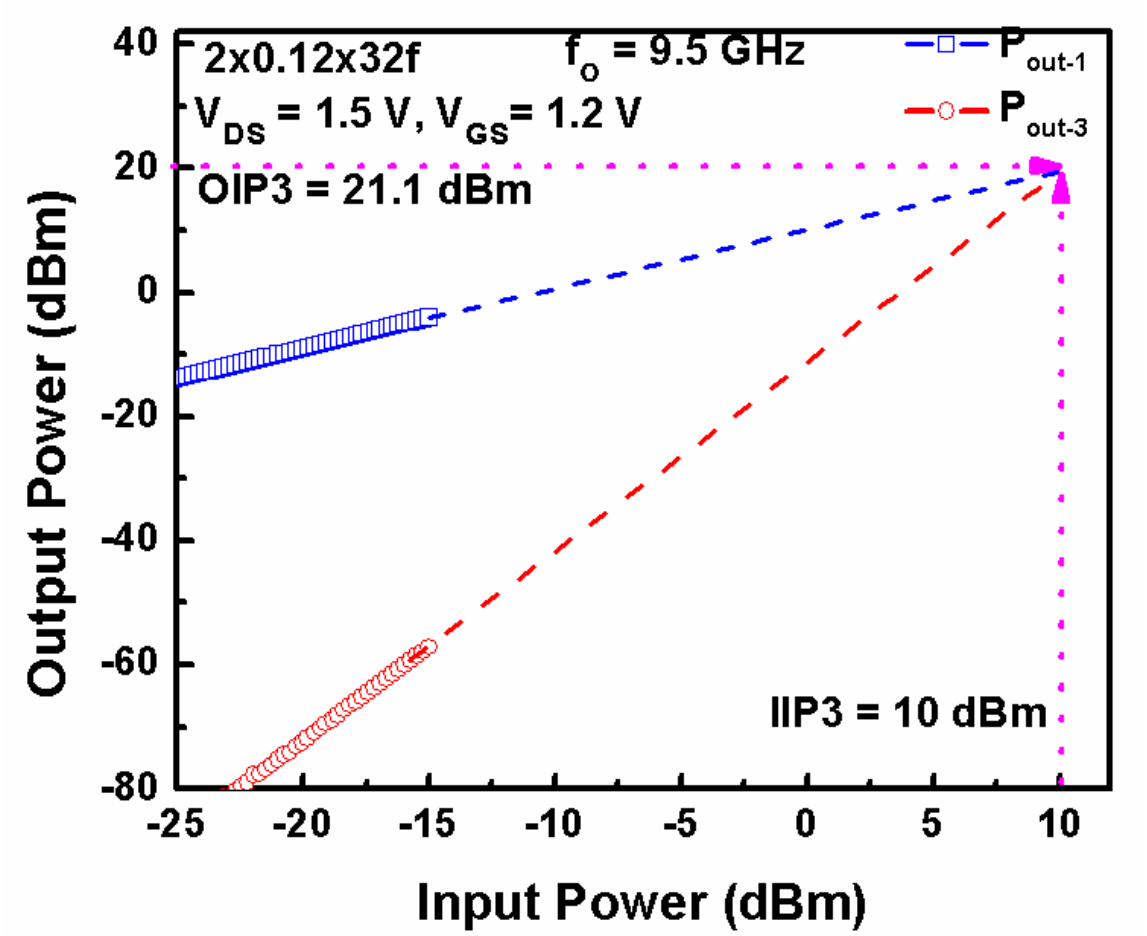


Figure 20. Measured fundamental and third-order harmonics for the device. IIP3 and OIP3 are extrapolated for a fixed bias.

Figure 21 shows IIP3 obtained from measurements at four different V_{DS} values ranging from 0.6 V to 1.5 V. At each of these V_{DS} values, the gate voltage was swept from 0.2 V to 1.5 V. With V_{DS} increasing from 0.6 to 1.5 V, IIP3 increases by a large factor, particularly at higher V_{GS}. The measured value of $K3g_m$ (third-order derivative of I_D with respect to V_{GS}) is plotted in Figure 22 to explain the "sweet spot" and V_{GS} dependence of IIP3. The zero $K3g_m$ point corresponds closely to the sweet spot (maximum linearity) of IIP3 for V_{DS} = 1 V.

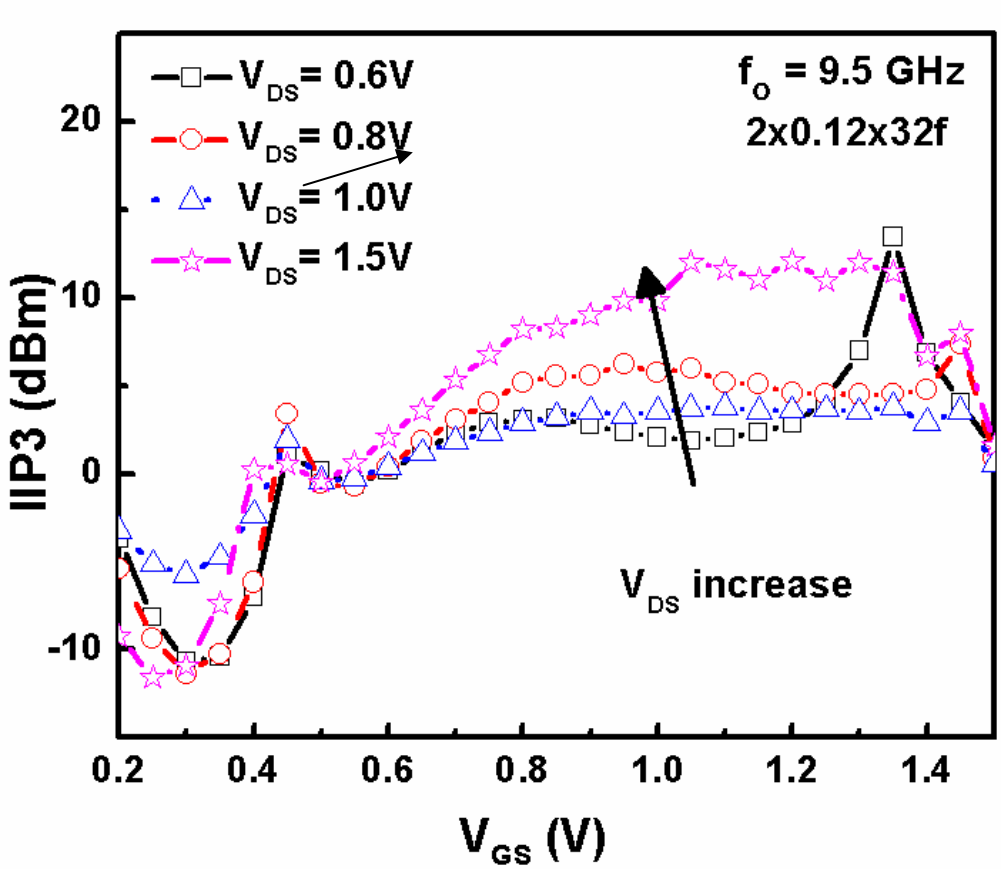


Figure 21. Measured bias dependence of IIP3 as a function of gate voltage, at different drain voltages.

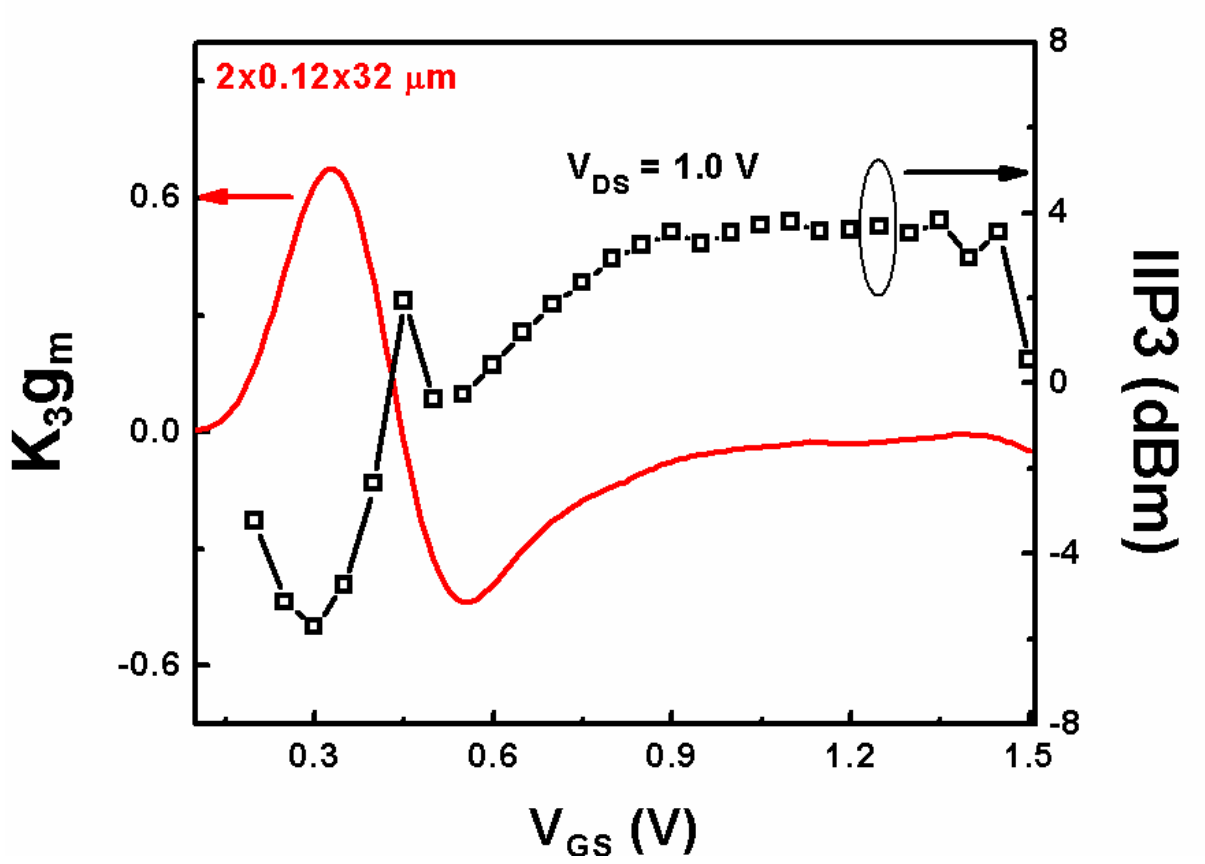


Figure 22. K3g_m and its correlation with linearity sweet spot.

3.3 Simulations and Calculations

The harmonic balance (HB) technique was used for simulating distortion in the devices. For simulating analog and RF circuits, harmonic balance offers frequency-domain analysis, and is typically the method-of-choice for linearity simulations. The direct solver method was used for HB simulations, with a fine bias step size (10 mV). This method allows one to minimize the oscillations in the extraction of third-order derivatives, which is necessary for understanding the nonlinear response of transistors. For a fundamental frequency of 9.5 GHz, IIP3 was calculated by extrapolating the P_{out} and IM3 terms at -27 dBm, assuming 1:3 slopes. Figure 23 shows the IIP3 dependence on

bias obtained from the harmonic balance simulations, using the standard design kit compact models. It is observed that the simulation results are in agreement with the measured data using our new simplified linearity measurement setup.

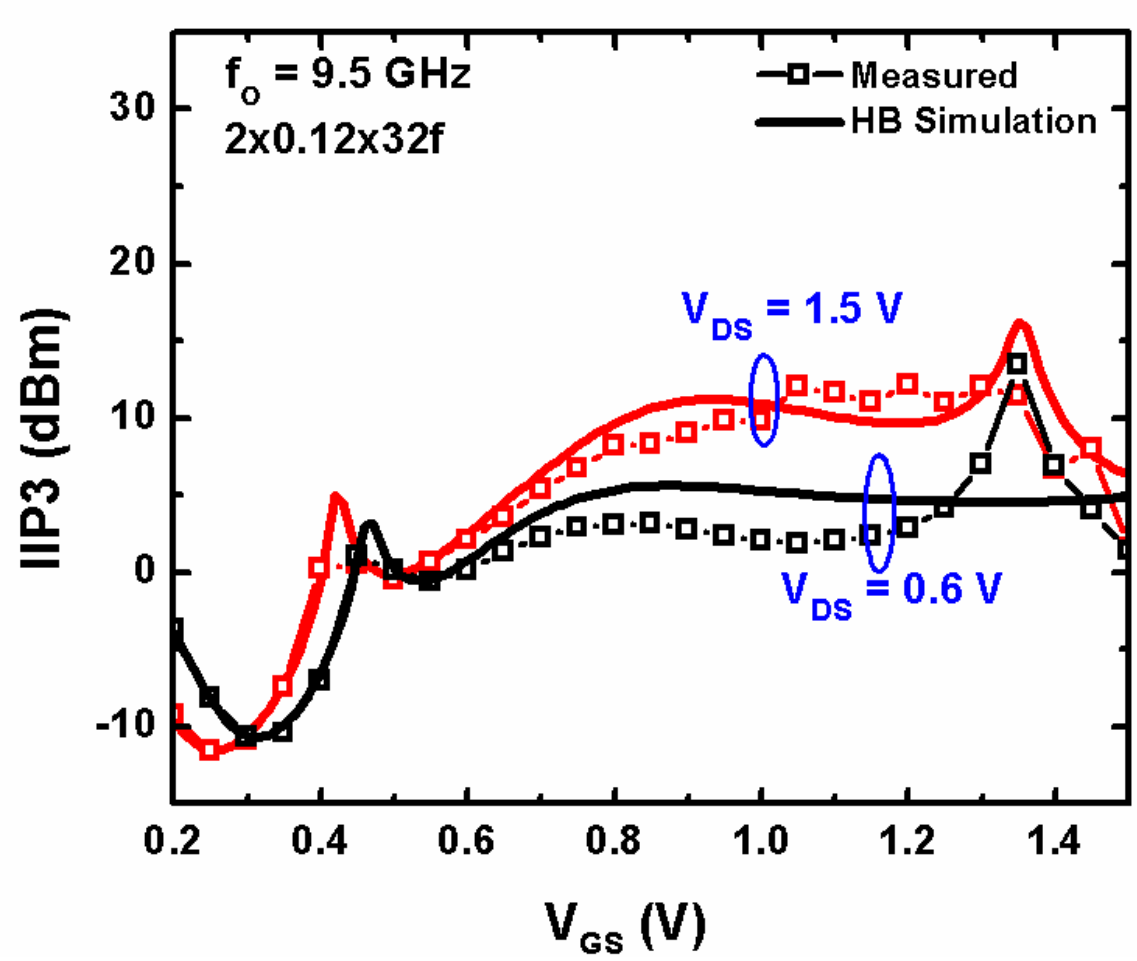


Figure 23. Comparison of measured IIP3 with harmonic balance simulations run using ADS simulation tool.

This integrated approach to measure linearity and S-parameters is currently used in the lab to characterize a number of devices and circuits.

CHAPTER 4

HIGH LINEARITY SWITCH DESIGN

4.1 CMOS Switch Design

In this chapter, we explore RF single-pole single throw (SPST) n-MOSFET switch designs in a commercially available 0.35 μm SiGe BiCMOS technology (5PAe), particularly used for power-amplifier (PA) applications. The focus of this work is to design high linearity, low-loss switches for integration with PA in wireless front-end applications. The challenge is to design a low loss switch using a longer channel length technology (0.35 μm), while maintaining adequate isolation, and pushing for higher linearity.

The SPST switches were designed using the topology highlighted in Figure 24. To improve insertion loss, an isolated triple-well n-MOSFET device is used as the series switch. The isolated p-well is achieved by floating the deep n-well of the triple-well n-MOSFET device, reducing parasitic losses by increasing the effective substrate resistance in the body of the device. The shunt n-MOSFET device increases isolation while only minimally degrading the insertion loss. Both the source and drain of the device were held at the same *dc* potential, and therefore only leakage current is dissipated, enabling these switches to consume virtually no power. As shown in the schematic in Figure 24, the 20 kΩ resistors on the gate and body of the device isolate the gate and body nodes from RF ground, thus improving the insertion loss of the switch. However, the switch isolation is

degraded due to these floating nodes, allowing RF power to leak from the source to the drain, even when the switch is in the off state.

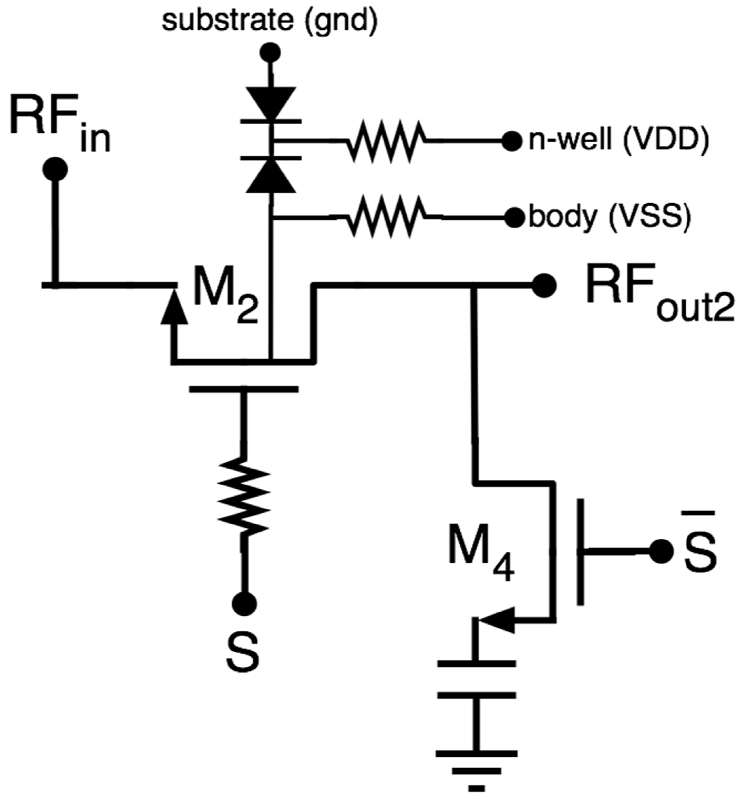


Figure 24. Schematic of single-pole single-throw (SPST) switch using triple-well n-MOSFET as series device.

The optimization of switches for a particular application (in this case, X-band) involves appropriate selection of device geometry. The geometry selection provides a balance in trade-offs between the on-state device resistance (R_{on}) and the off-state parasitic device capacitances (C_{off}). R_{on}*C_{off} product is a common benchmark for FET switch designs where the multiplier for 1 mm of gate width is often used to compare the quality of the FET used in the switch. For example, a transistor with a larger width will

provide a small Ron, but will also increase overlap and source/drain to body capacitances, thus increasing the overall switch performance metric product. The switches in the present work were realized to achieve optimum linearity and insertion loss at 9.5 GHz. Linearity is dominated by the device parasitic capacitances which can be reduced by optimally sizing the device, but at the cost of higher Ron. The optimal gate widths for the series and shunt devices were chosen as 200 µm and 100 µm, respectively. It is worth mentioning that the optimal width for switch design is technology dependent [30]. Series or shunt devices are stacked to distribute the large signal swing across multiple transistors, thus preventing high potential across the gate of a single device. The following three switch configurations were built to analyze the performance trade-off associated with stacking the series or shunt devices in series:

1. Series-Shunt: Single series device and single shunt device.
2. Series Stack-Shunt: Two similar devices stacked in series arm and a single shunt device.
3. Series-Shunt Stack: Single series device and two stacked devices in the shunt leg.

The two-port S-parameter characterization for switches was performed using an Agilent E8363 PNA. Switch 1 dB compression point (P1dB) measurements were performed using a novel high power test setup which allows us to apply +33 dBm RF power at the DUT input. The setup is described in detail in Sec 1.3.5. IIP3 of the switches was calculated using a conventional two-tone measurement setup.

As shown in Figure 25, the switch shows an insertion loss of < 1.5 dB across the X-band while maintain an isolation of about 14 dB (Figure 26). As one would expect, an additional series device degrades the switch insertion loss while improving the isolation

at the same time. However, the shunt stacked switch degrades the isolation by reducing the total resistance offered by the shunt leg to the ground.

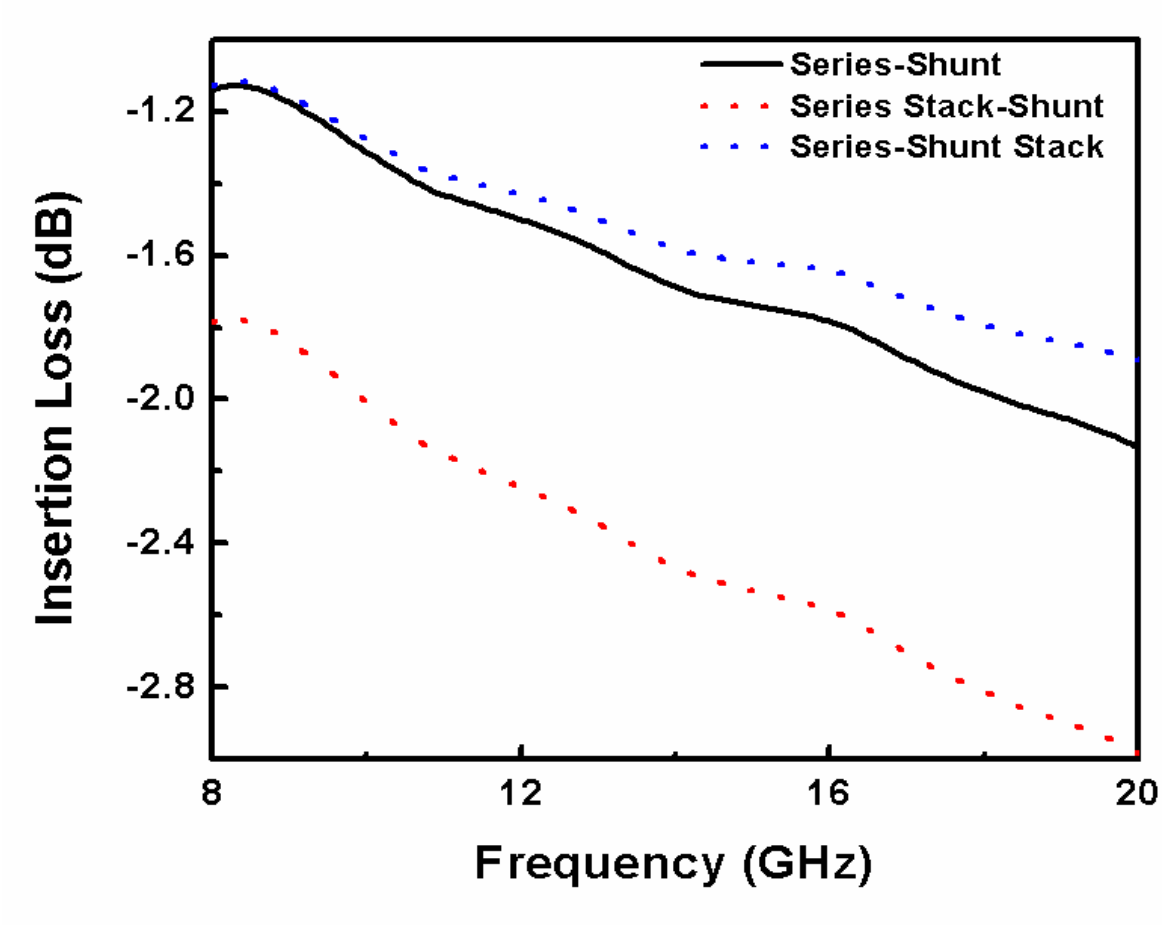


Figure 25. On-state S_{21} of series-shunt Single-Pole Single-Throw (SPST) RF switches optimized for X-band operation.

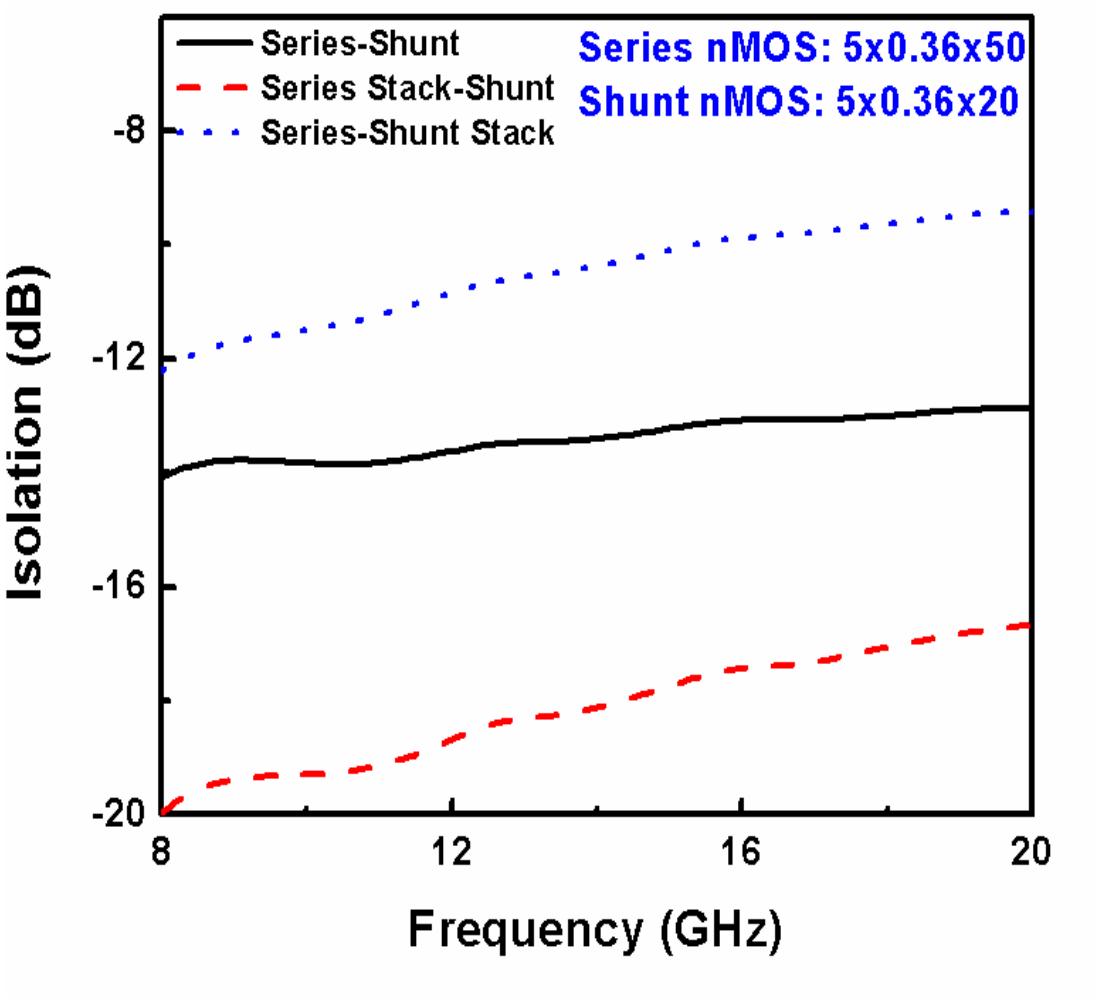


Figure 26. Off-state S_{21} of series-shunt Single-Pole Single-Throw (SPST) RF switches optimized for X-band operation.

The power sweep curve of the series-shunt switch gives a P1dB compression point of 22 dBm, as shown in Figure 27. This compression point is the record performance for any CMOS based switch at X-band. For the series-shunt stack switch, two-tone measurements in Figure 28 showed IIP3 performance of 25 dBm at 9.5 GHz.

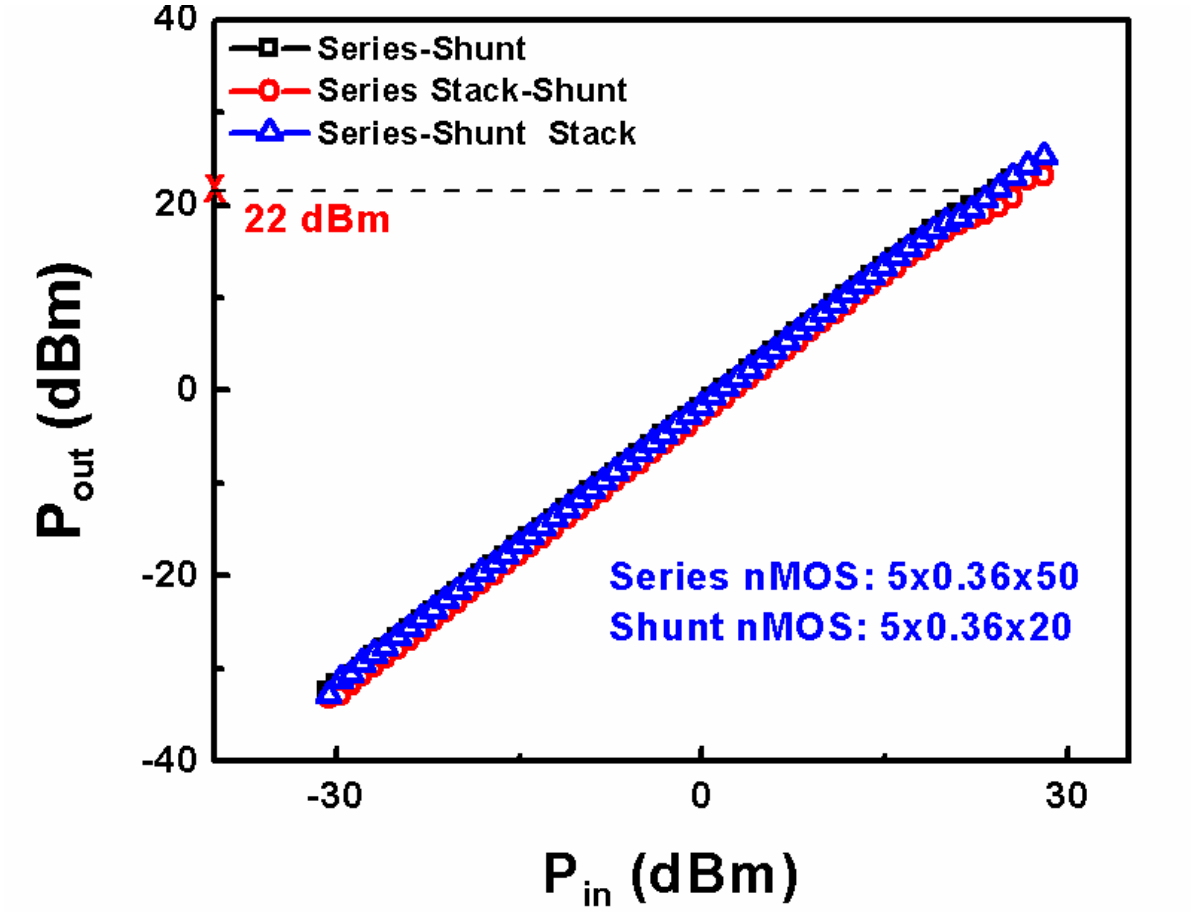


Figure 27. Record P1dB compression point of a CMOS based SPST switch at 9.5 GHz

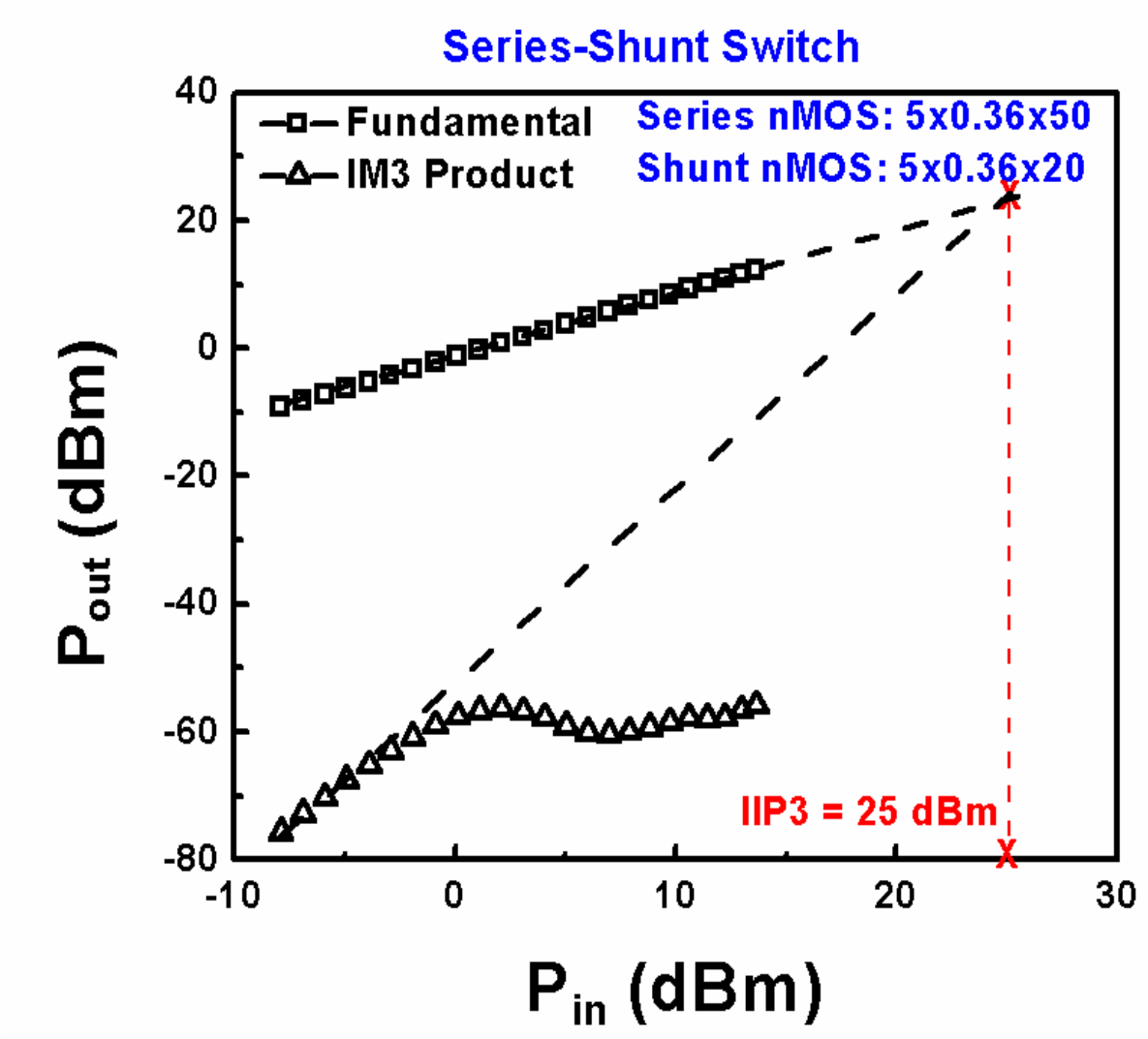


Figure 28. IIP3 of 25 dBm is measured for a series-shunt stack type SPST at 9.5 GHz.

4.2 SiGe HBT Switch Design

Highly-integrated, low-cost circuits have fueled the growth of BiCMOS technology for radio-frequency (RF) applications. Aggressive technology scaling and the integration of bandgap-engineered Silicon-Germanium (SiGe) technologies have resulted in dramatic performance improvements of silicon-based RF integrated circuits, thus providing cost

advantages over III-V technologies [31]. RF switches are crucial for operation of any radar or wireless transceiver. In addition to transmit/receive functionality, RF switches can be used for digital gain control and phase state selection in a typical RF front-end. Technology scaling and layout optimization has resulted in low insertion loss CMOS RF switches [32]. However, shorter channel length and thinner oxide limit the dynamic range and high power handling capability of the CMOS switches.

Near one watt X-band power amplifiers (PA) in SiGe BiCMOS technology have been demonstrated, thus highlighting the need for high power handling silicon RF switches [33]. Since solutions are already available for integrating the balun and high power PA on a single chip, a high power and high linearity T/R switch becomes the last external component (excluding the crystal oscillator) that needs to be integrated on chip to provide the most cost-efficient system-level solution. With SiGe HBT device performance constantly improving (with f_T now routinely above 200 GHz and even now approaching 500 GHz), it is possible to design a robust switch based on a diode-connected SiGe HBT [34]. In the present work, we focus on building low insertion loss and high-linearity RF switches, using SiGe HBTs, to enable integration with power amplifiers designed in the same technology platform.

The single-pole, single-throw (SPST) RF switches were designed using SiGe HBTs from a commercially available, 0.35 μm SiGe BiCMOS technology. Thru-Silicon Via (TSV) technology is used in this platform to provide a low ground plane inductance, which is highly desirable for power-amplifier applications [35]. The SiGe HBT acts as the series switching element, while a pFET is used to pull-up the circuit in the OFF state, as shown in Figure 29. When the switch is ON, the switching junction (B-E in forward

mode, B-C in inverse-mode) is forward-biased and the current flows from the collector (emitter) into the emitter (collector), in forward-mode (inverse-mode) operation. The schematic in Fig. 1 highlights the operation of the SiGe BiCMOS RF switch in inverse mode, in which the base-collector junction is used as the switching diode, instead of the conventional base-emitter junction.

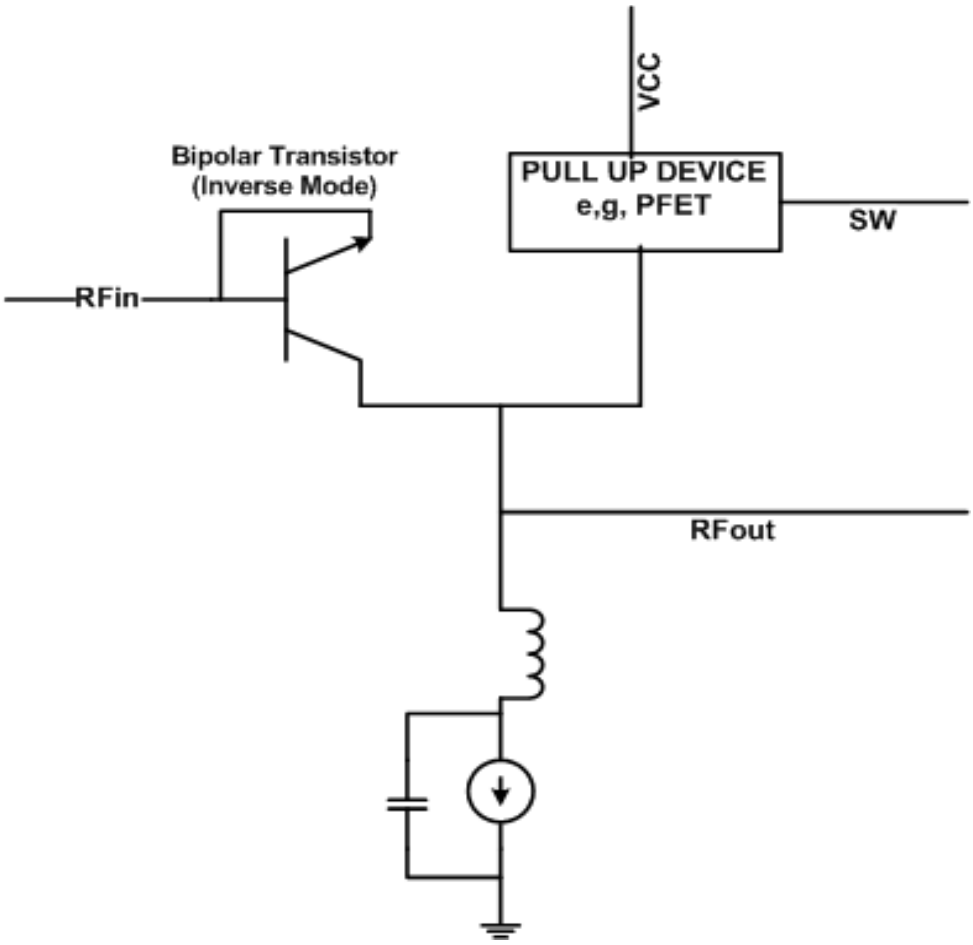


Figure 29. Schematic of the inverse-mode bipolar transistor as an RF switch.

When the switch is turned OFF, the pFET pulls the collector voltage of the SiGe HBT to the V_{CC} rail and eliminates any *dc* current flow through the device. Compared to CMOS RF switches, higher *dc* power is dissipated in SiGe HBT switches due to the bias

current flowing through the bipolar transistor in the ON state. The dimensions of the SiGe HBT chosen were $0.8x20\mu m^2$ with three emitter stripes, with a peak f_T of 33 GHz. The *npn* SiGe HBTs in the technology support only up to three-stripe emitter geometries. This is because at high current densities allowed in the technology (for PA applications) center fingers of a multi-finger device would be at a higher temperature than the outer fingers, causing potential reliability concerns. However, the RF switch current density is low enough to ignore this effect. The switches were optimized for operation in the X-band. For the three-stripe device, a *c-b-e-b-e-b-e-b-c* three-stripe layout is used.

4.2.1 Results and Discussions

A. Switch Performance

Figure 30 shows the measured insertion loss of both forward- and inverse-mode SiGe BiCMOS switches, and the SPST die picture (inset). The insertion loss of the inverse-mode switch is slightly higher than the forward-mode switch. Identical pFETs were used as shunt devices in both of the designs. The high intrinsic collector resistance is likely responsible for higher insertion loss in the inverse-mode switch, compared to the low emitter resistance in the forward-mode operation.

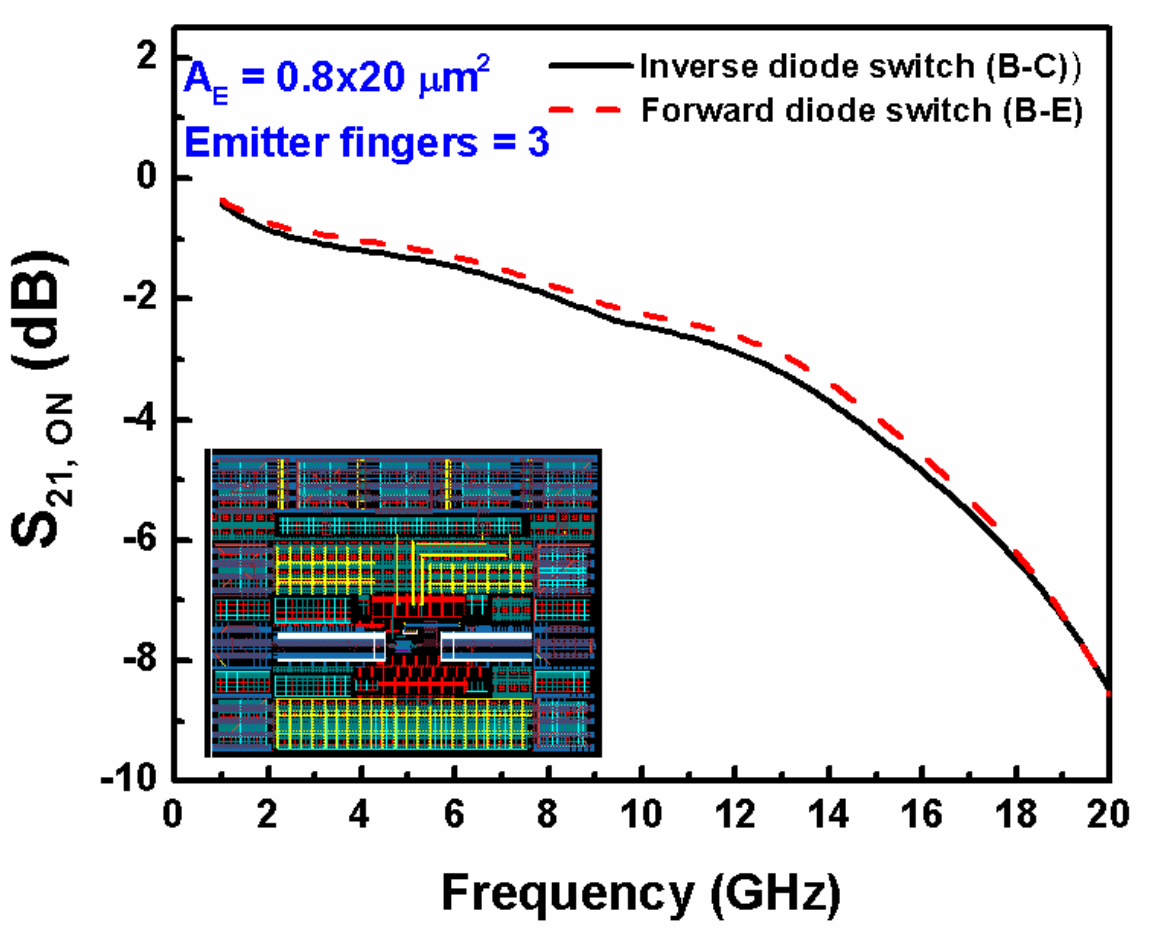


Figure 30. Insertion Loss of the SiGe BiCMOS RF switches in both forward- and inverse-mode orientation.

As seen in Figure 31, the isolation of the switch improves considerably when the base-collector junction is used as the switching diode. This improvement is observed across the whole frequency spectrum, with about 8 dB improvement at 2 GHz, and a 6 dB improvement around the center of X-band (9.5 GHz), respectively. When the switch is turned OFF, negligible leakage current flows through the diode and the junction is reverse-biased. The base-collector junction has a longer depletion region and thus,

smaller depletion capacitance than the base-emitter junction. Hence, this smaller capacitance allows for better isolation in inverse-mode switch.

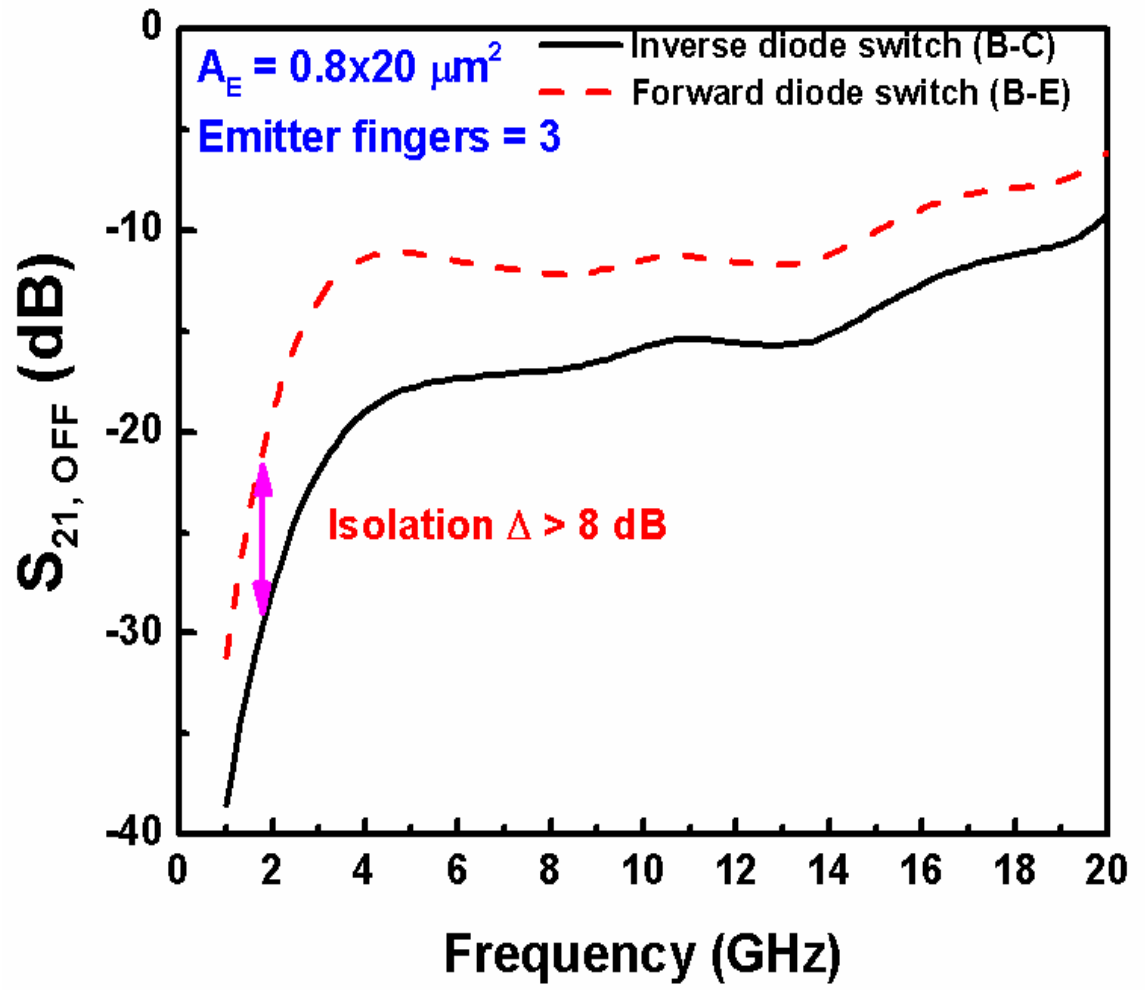


Figure 31. Improved isolation in the inverse-mode switch compared to the forward-mode switch across a wide frequency range.

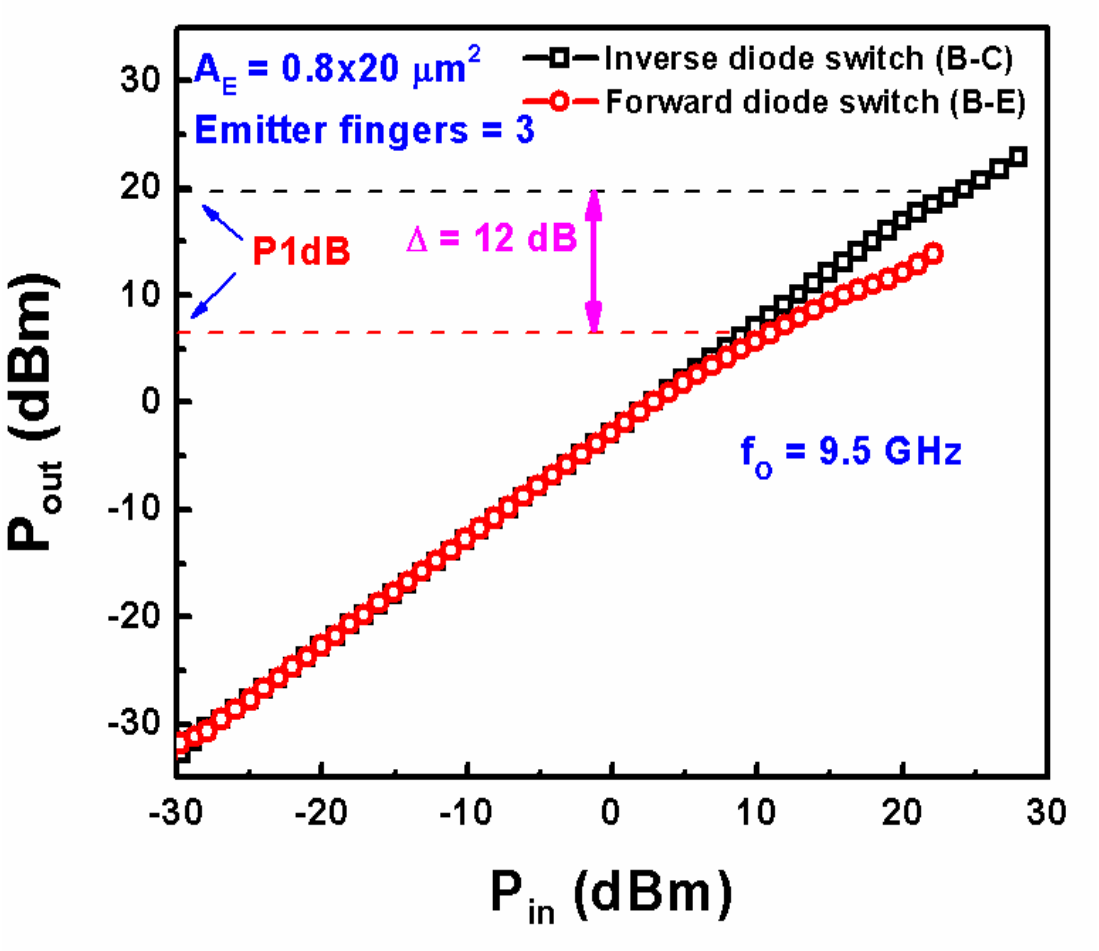


Figure 32. A 12 dB improvement in P1dB compression point of the switch through inverse-mode operation is obtained.

To evaluate the large-signal potential of SiGe BiCMOS switches, 1 dB compression point measurements were performed at 9.5 GHz on both forward-mode and inverse-mode switches. As shown in Figure 32, the inverse-mode switch gives a P1dB compression point of about 20 dBm, which is a 12 dB improvement over the forward-mode switch. This is a significant result. The improvement in power handling capability of the inverse-mode switch is due to the longer depletion width of the base-collector junction, thus allowing for a larger swing before the switch goes into compression. The transistors were

biased at 9 mA, which is well below the peak f_T current of the forward-mode device. This is done to ensure that the device is biased below peak f_T in the inverse-mode operation as well, to avoid other non-linear contributions from high-injection.

Two-tone measurements are used to calculate the input third-order intercept (IIP3) of the RF switches. The center frequency was kept at 9.5 GHz with a tone spacing of 1 MHz. Figure 33 shows the extrapolated IIP3 of the forward-mode switch. The linearity of inverse-mode switch was also 12 dB higher than the forward-mode switch, as shown in Figure 34. To the best of author's knowledge, an IIP3 of 35 dBm represents record linearity performance for a SiGe BiCMOS switch at X-band [36].

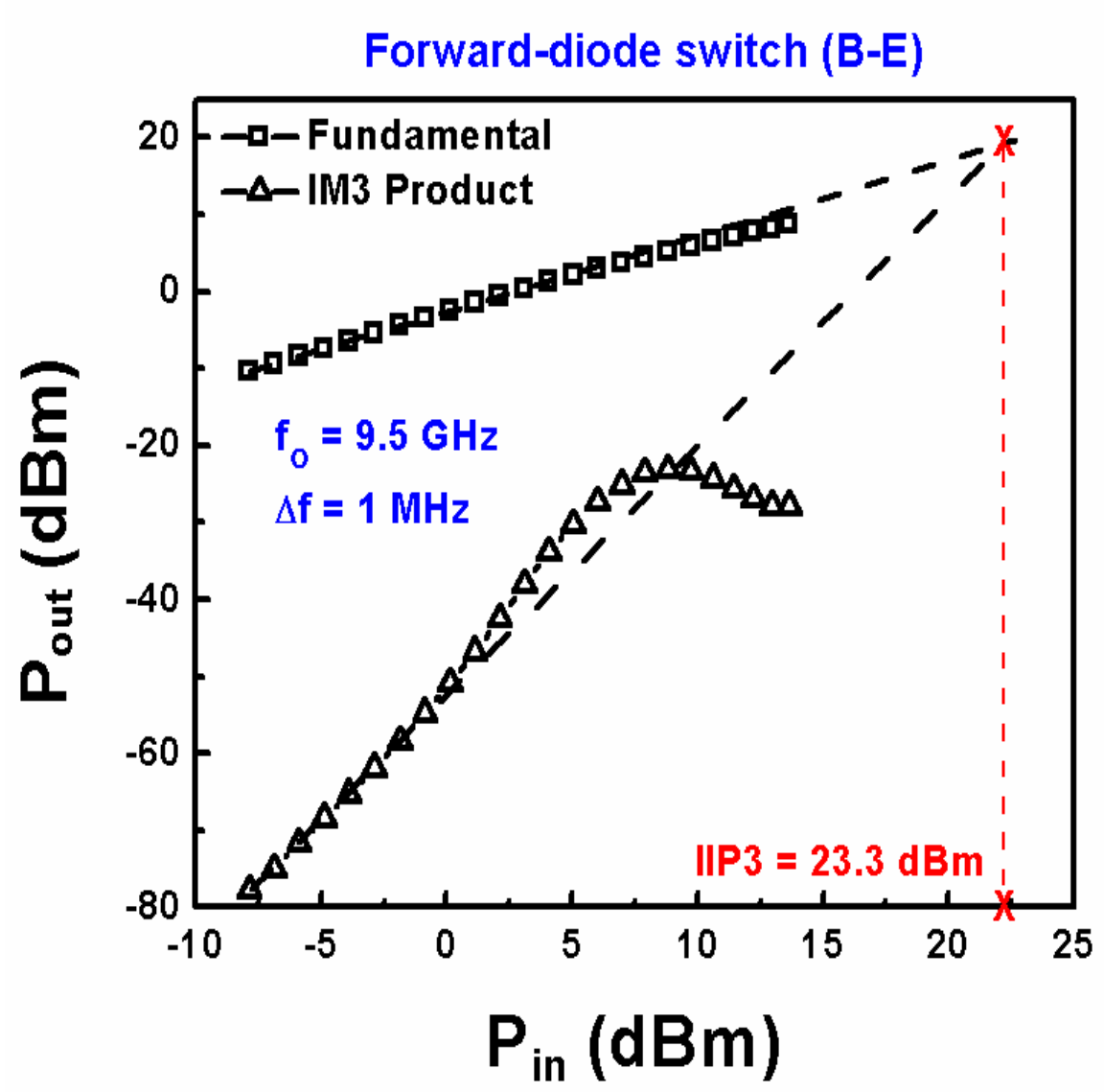


Figure 33. Extrapolated IIP3 using two-tone characterization of the forward-mode RF switch.

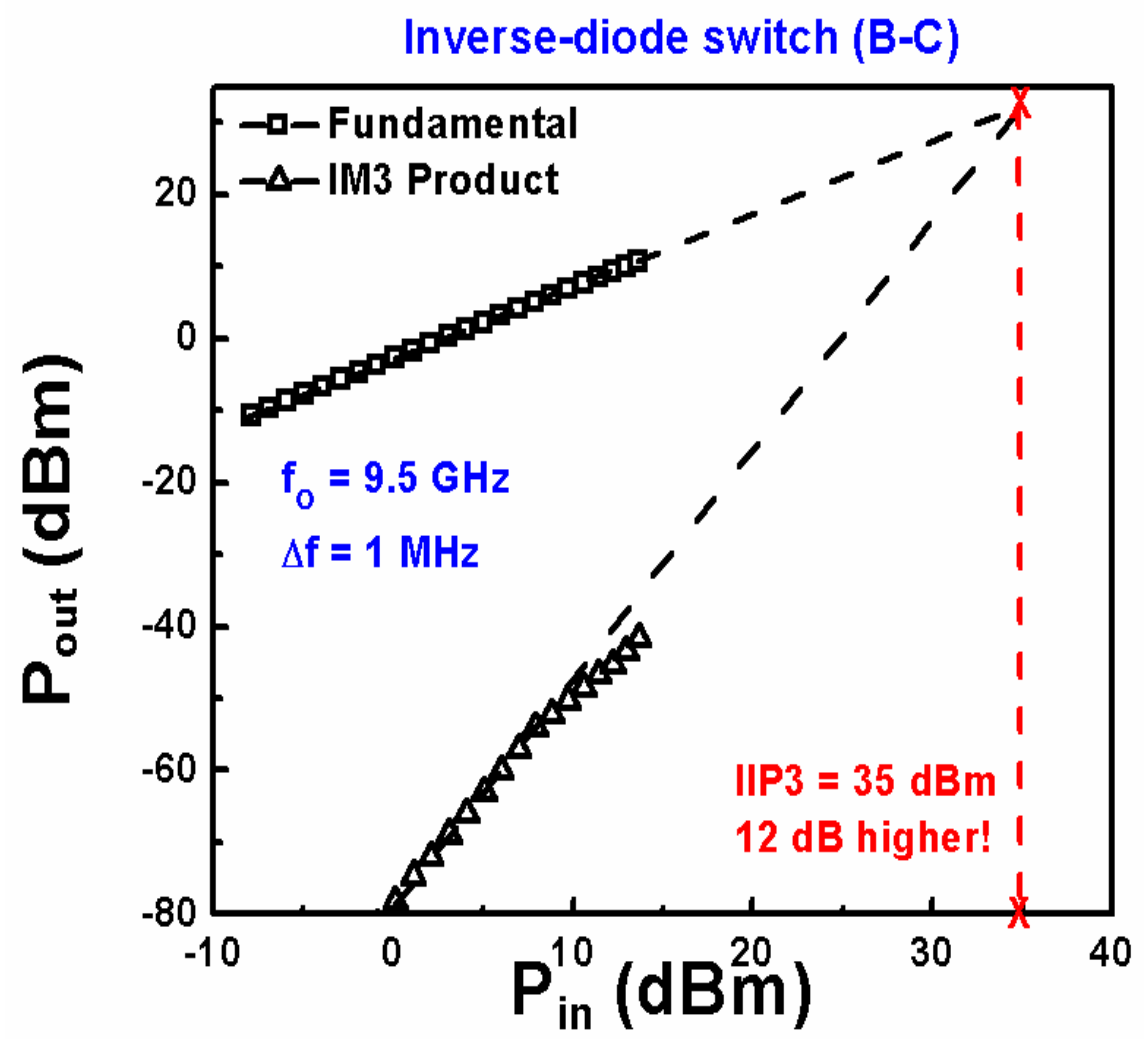


Figure 34. Using the inverse-mode switch topology, 12 dB improvement in IIP3 is measured over standard switch.

4.2.2 Summary

The inverse-mode RF switch operation of the SiGe HBTs is investigated for high-linearity and high-power handling capability. We find that the inverse-mode switch gives superior linearity performance, while maintaining reasonable insertion loss. High power and high dynamic range switches on silicon necessitate careful reliability analysis to

correlate device failure with circuit reliability. We find that high RF input power induces junction damage in SiGe HBTs, leading to degradation or failure of the RF switches. Insertion loss and isolation of forward-mode switch begin degrading at 30 dBm RF input power, while the inverse-mode switches can withstand 30 dBm of RF power.

CHAPTER 5

RF SWITCH RELIABILITY

5.1 CMOS RF Switch Reliability

The use of conventional MOS transistors for front-end building blocks of RF transceivers raises issues related to MOSFET reliability, particularly under RF and mixed-signal stress conditions. RF single-pole, double-throw (SPDT) n-MOSFET switch designs are explored for their power handling capability and robustness under RF stress. The series-shunt SPDT switches were designed using n-MOSFETs from 180 nm and 130 nm SiGe BiCMOS technology nodes [37]. A series-shunt topology, highlighted in Figure 35, was chosen for all of the switches.

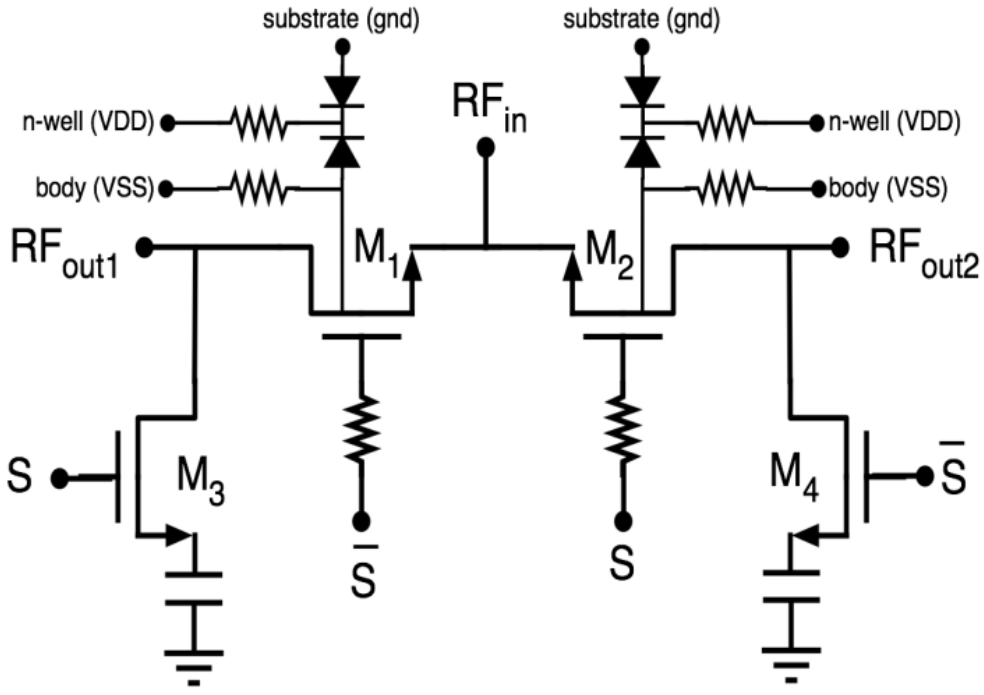


Figure 35. Single-Pole Double-Throw (SPDT) RF switch design topology used for reliability analysis.

An isolated triple-well n-MOSFET device was used as the series switch to improve insertion loss. The standard n-MOSFET device is used in the shunt leg to improve the isolation. The shunt devices M3 and M4 (Figure 35) cause a minimal degradation in insertion loss of the switch. The switching control is provided by a digital signal, S. When S is high, M2 is on and M4 is off, allowing the RF signal to pass from RF_{in} to RF_{out2}. Similarly, the signal flows from RF_{in} to RF_{out1} when S is low. Separate test structures with only the series transistor, M1 or M2 as a switch, were also tested to better understand the exact failure mechanisms of the RF switches under high RF drive.

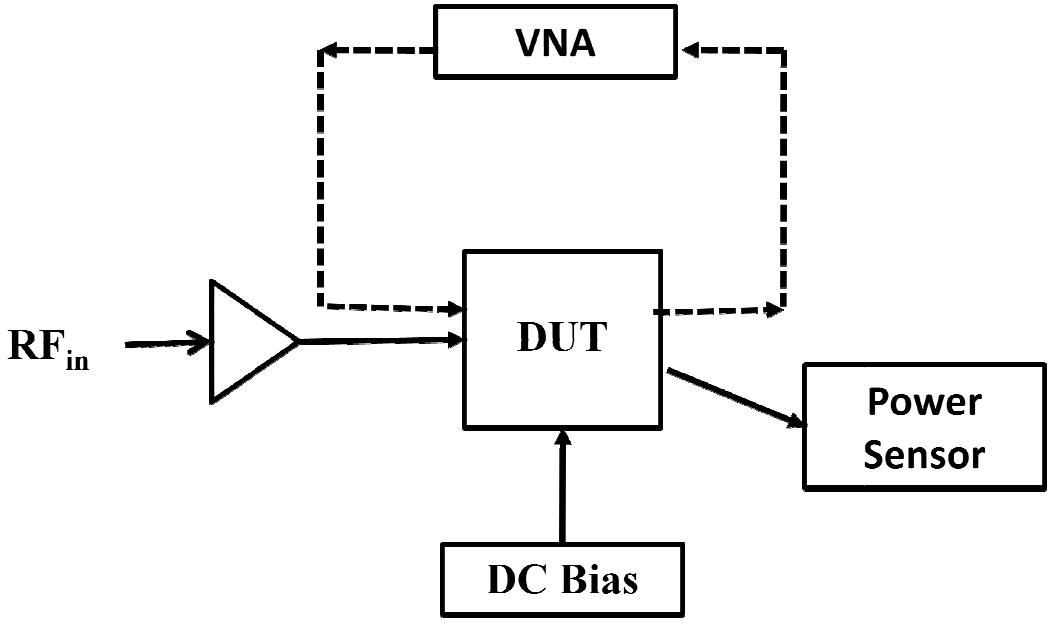


Figure 36. Block diagram of the setup used for applying RF stress and measuring S-parameters.

Figure 36 shows the test setup for high power RF reliability analysis of the switches. RF stress is applied at 9.5 GHz (in the middle of X-band) for 300 seconds when the switch is 'ON' by using a RF source and a traveling wave tube (TWT) amplifier with maximum gain of 40 dB at 9.5 GHz. For stressing at high input power, a separate RF

source becomes necessary to avoid reflected power at the network analyzer input. All losses were calibrated using a power sensor to de-embed the RF power applied to the DUT. S-parameters were measured while sweeping frequency from 1 GHz to 40 GHz with an applied input power of -17 dBm. Five different switches and device test structures were stressed at input power levels between 24 and 36 dBm, in 3 dBm steps. No DC biasing was used to accelerate oxide degradation.

Figure 33 shows the insertion loss degradation of the series transistor structure. No degradation was observed up to RF input power of 30 dBm. However, the insertion loss degraded at 33 dBm RF stress (inset) before the series transistor failed catastrophically during stressing at 36 dBm input power.

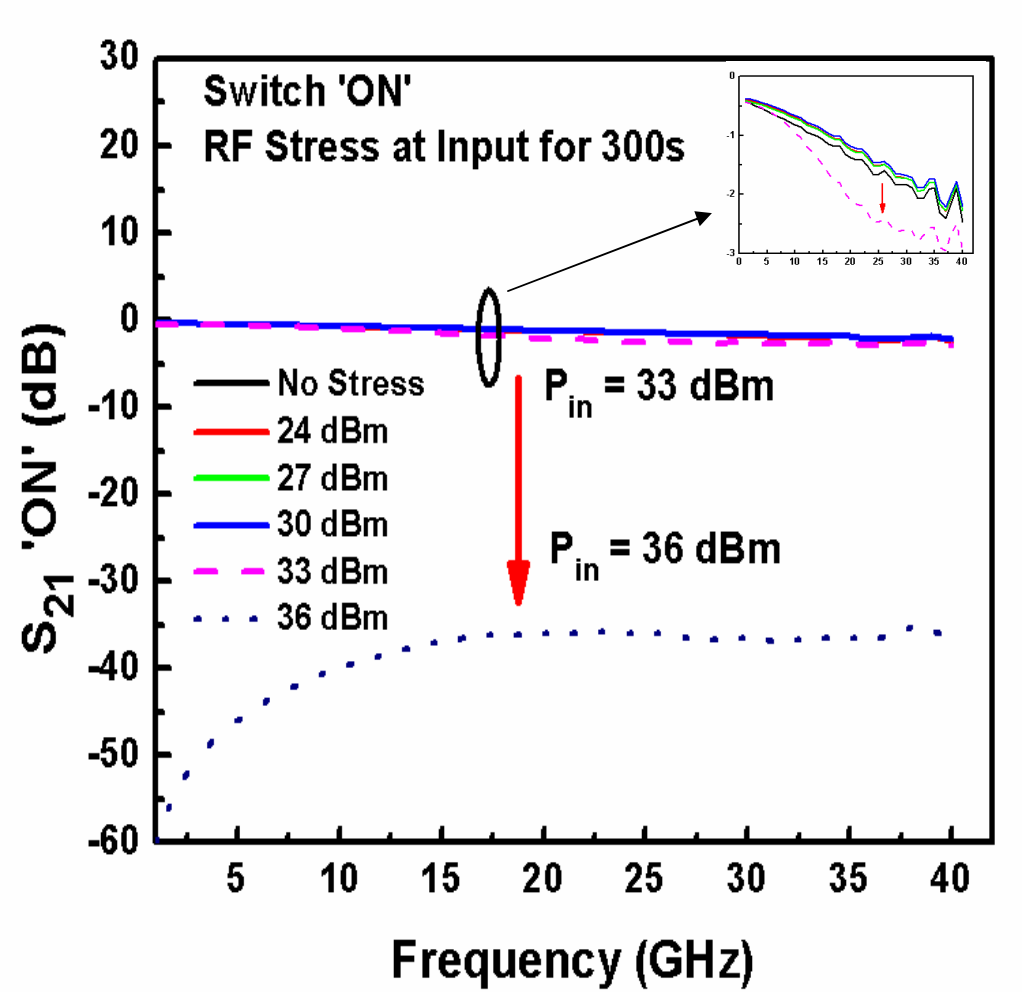


Figure 37. Insertion Loss of standalone DUT after RF-Stress. Degradation is observed at 33 dBm (inset) before device fails.

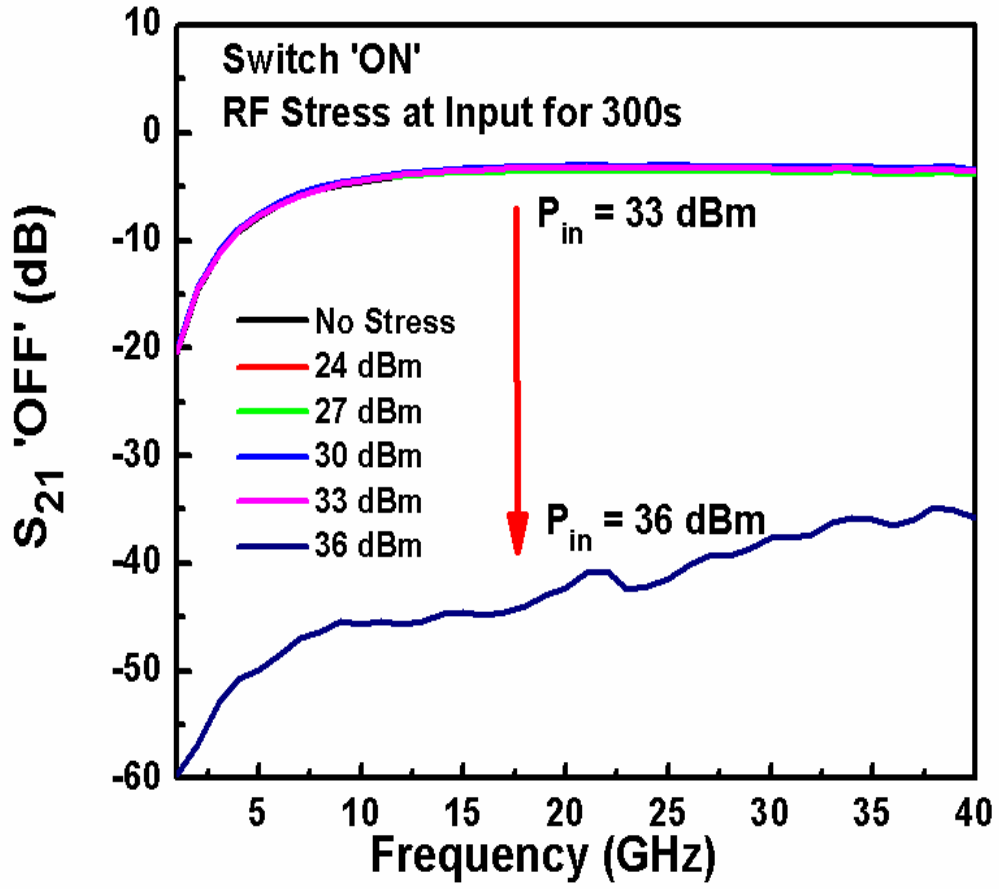


Figure 38. Isolation of the Series Transistor (M2) increases after RF stressing up to 36 dBm input power.

As shown in Figure 38, similar behavior was observed for transistor isolation or S_{21} when the switch was turned 'OFF'. Figure 39 shows the impact of RF stress on S_{11} of the device in the 'ON' state. The input matching conditions for the device change with RF stress and the device starts behaving as an electrical "open" after being subjected to 36 dBm input RF power. Similar behavior of S_{22} in Figure 40 implies that both ports (source, drain) behave as "open's" for small-signal power. The shunt transistor was not analyzed in detail, but we expect the device to show similar degradation when the switch is operated in the transmit state. Stacking of shunt devices at the transmit leg and series

devices at the receiving leg of the switch can help in improving breakdown voltage by distributing the large signal swing [38].

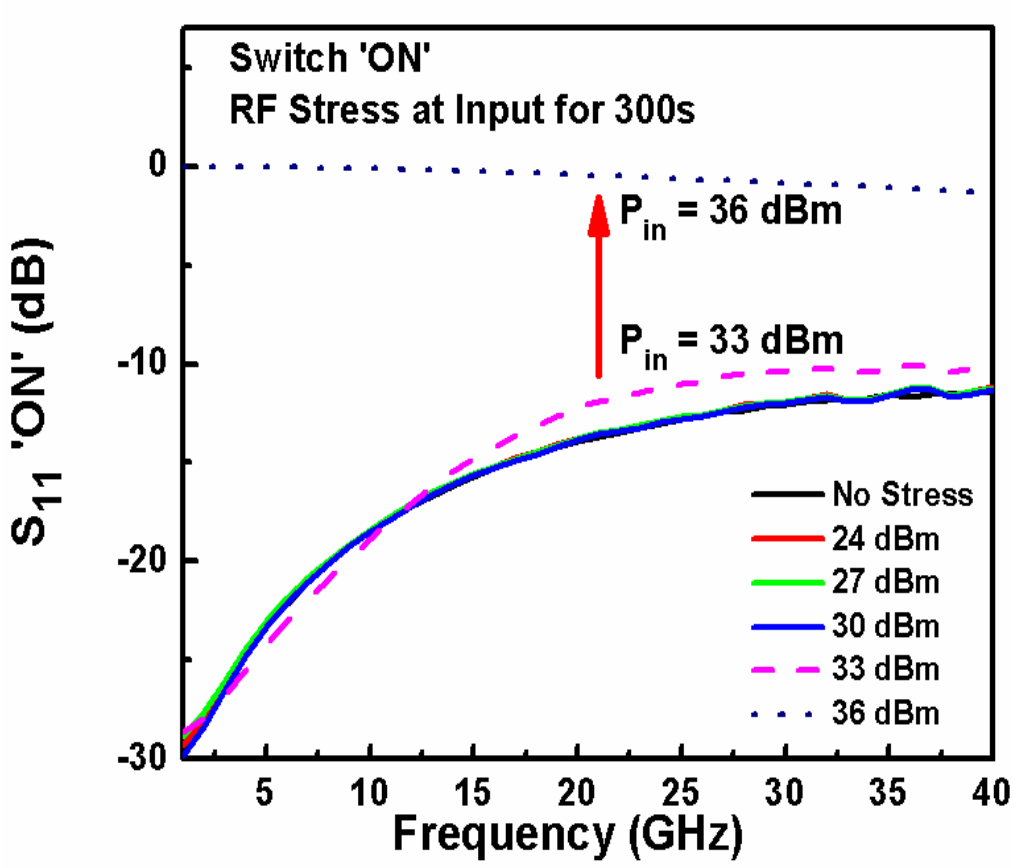


Figure 39. Input matching of the series transistor (M2) changes until the transistor behaves as an electrical "open" terminal after 36 dBm of RF stressing is applied.

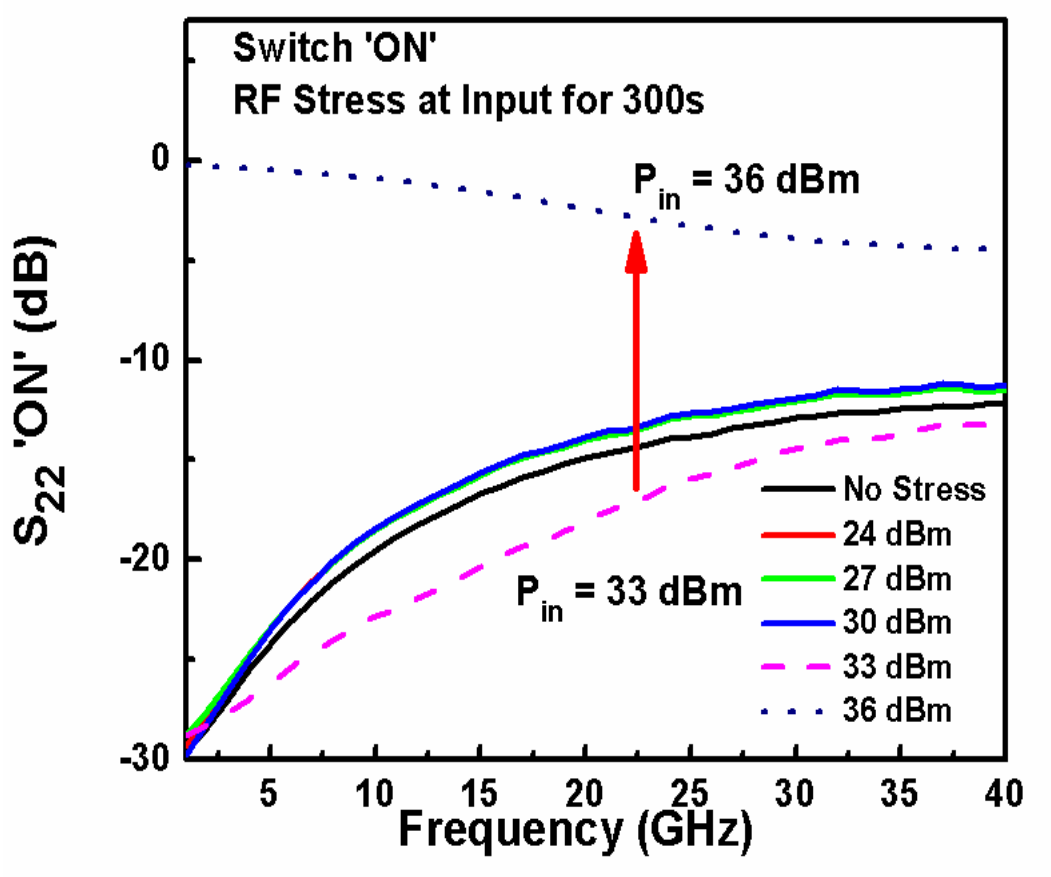


Figure 40. Output Matching of the DUT changes with RF stress.

To understand the failure mechanisms in the transistor, we performed DC sweeps on the transistor after RF stressing. Device failure was observed in the transfer characteristics of the device, which can be attributed to gate-oxide breakdown. As shown in Figure 41, the gate current of the device degrades considerably after 33 dBm of RF stress (and above). The devices exhibit typical breakdown current characteristics with very high current levels at low field. Similar gate current behavior has been observed for high voltage 0.28 µm CMOS devices used in power amplifiers [39]. No difference in gate current was observed when the source and drain terminals were swapped after gate breakdown. This observation may be attributed to the fact that no DC drain bias is

applied to the device during its operation as an RF switch (hence, no localized field). Instead, the transistor acts as a pass-gate switch without any DC bias on the drain and source terminals. Thus, hot carrier effects are negligible. The current flowing to the reverse biased n-well did not change after RF stressing (~175 pA). This observation eliminates the possibility of breakdown of the reverse-biased p-n junction between the body and n-well of triple-well process.

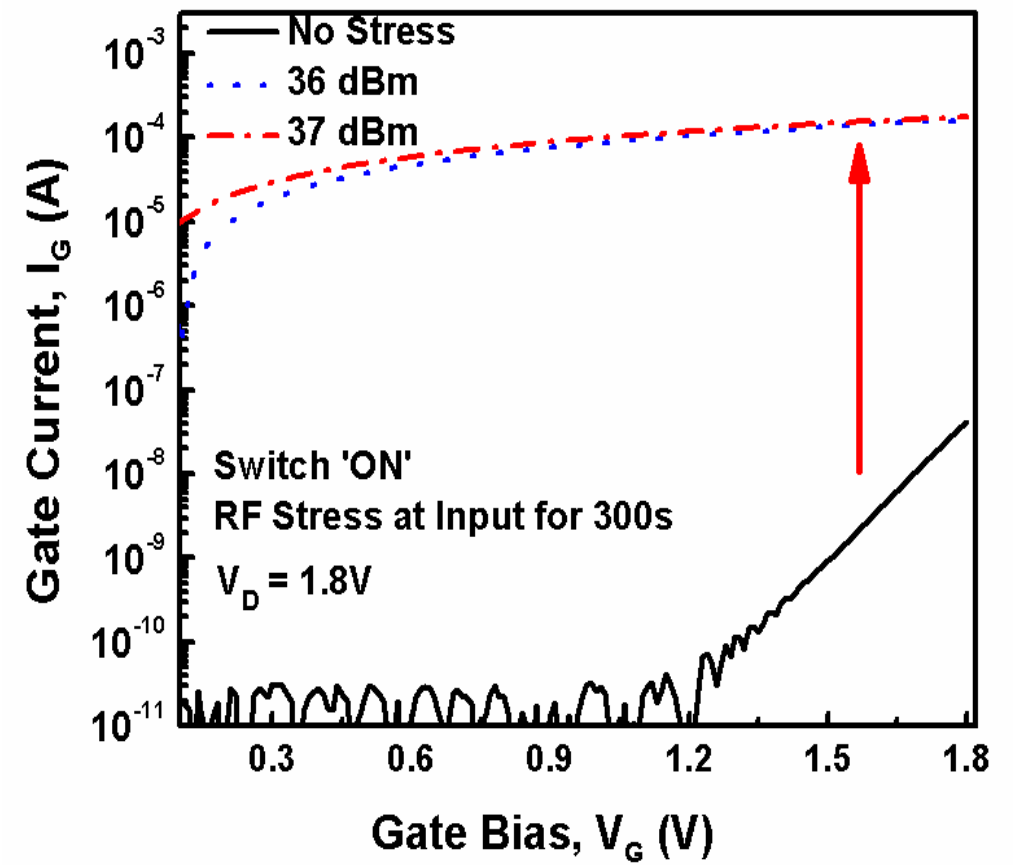


Figure 41. Gate-Breakdown induced by high RF power at the drain of the device produces failure of the transistor as an RF switch.

Reliability measurements were performed on RF switches designed in two different CMOS technology generations to assess the impact of node scaling. All switches were series-shunt SPDT switches with similar sized series and shunt transistors. Figure 42 shows that an RF switch designed in 130 nm CMOS shows degradation in isolation after stressing at 33 dBm input power, before it fails completely after 36 dBm stress. This degradation is presumably due to the damage in smaller sized shunt transistor, M4 (Figure 35) which reduces isolation of the switch since the shunt transistor is connected to AC ground. Notice that the effect of the shunt device can only be observed during the full operation of the switch. However, independent treatment of shunt device reliability needs attention.

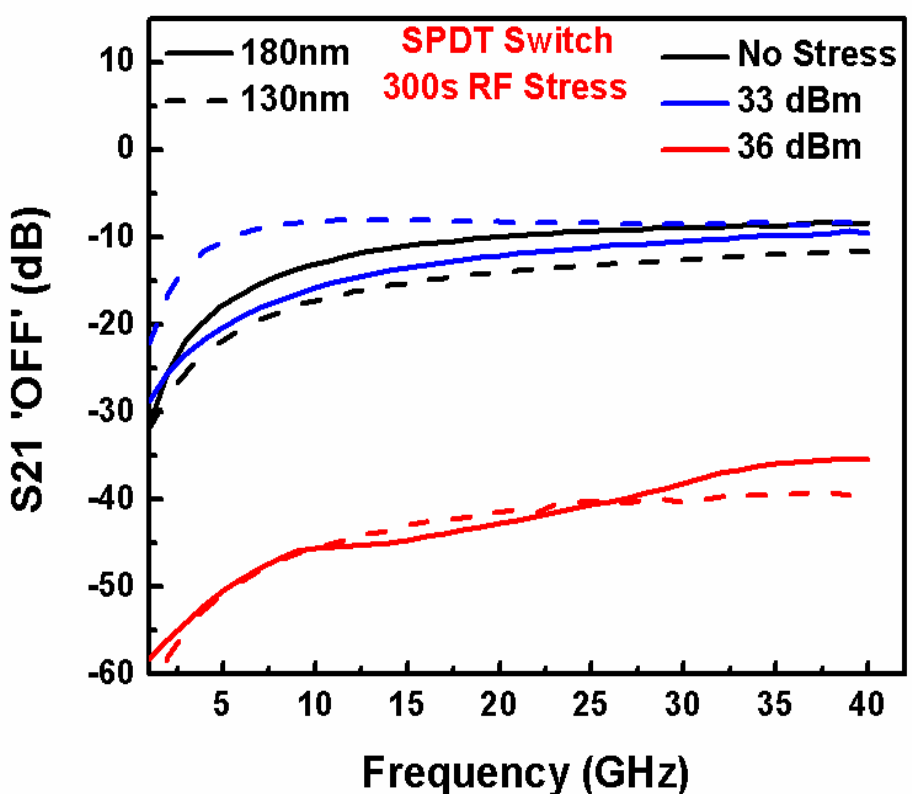


Figure 42. Impact of RF stress on isolation of SPDT switch in 180nm and 130nm CMOS technologies.

When the power is increased beyond 33 dBm, series transistor M2 breaks down, leading to failure of both 180 nm and 130 nm switches. Figure 43 shows that the effects of RF stress on insertion loss of the full switch are minimal before failure.

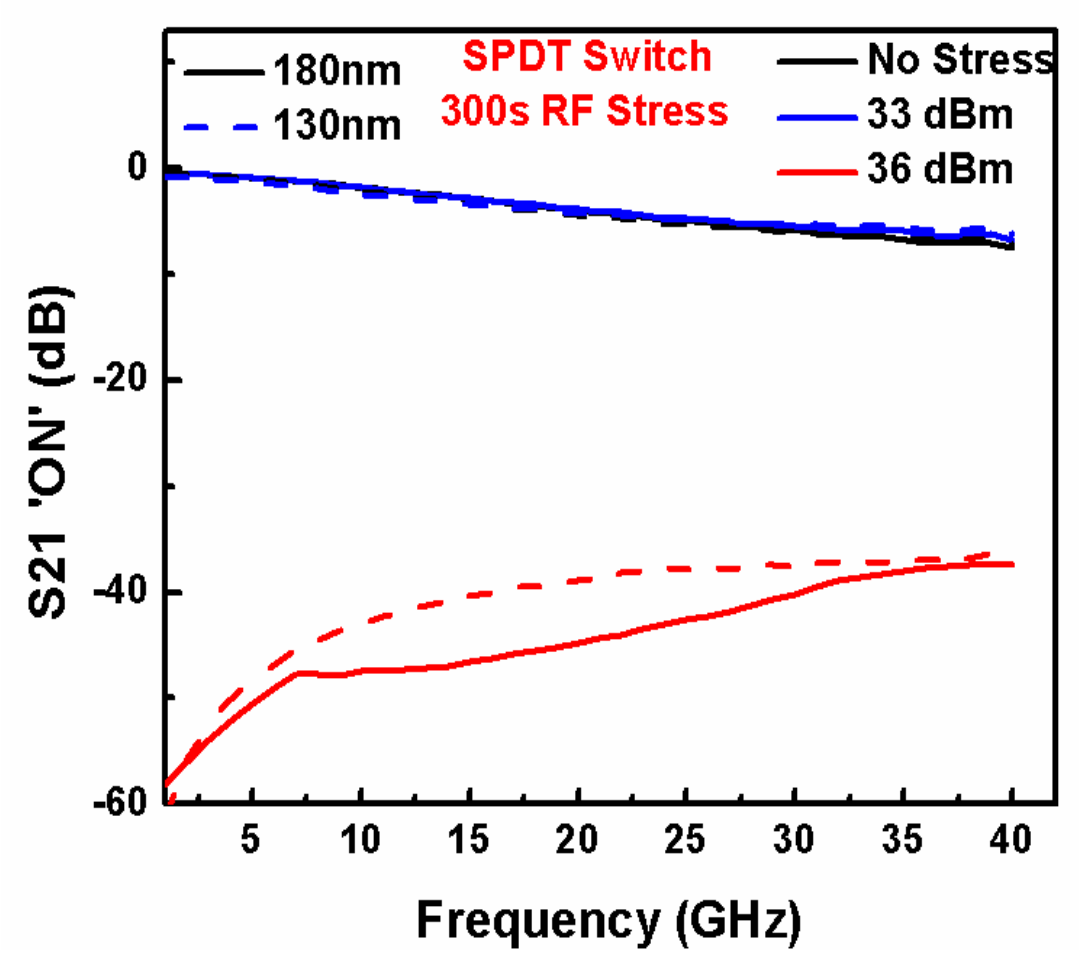


Figure 43. RF stress degrades the insertion loss of the SPDT switch in 180nm and 130nm CMOS technologies.

These results are extremely encouraging and address potential concern for reliable operation of CMOS switches under high RF power. The other area of potential concern includes reliability of LNA which is the next block in a typical receiver chain, which will be addressed as part of the dissertation.

5.2 SiGe BiCMOS Switch Reliability

We observed that the SiGe BiCMOS RF switches can handle high power (20 dBm) at 9.5 GHz, and potentially higher power at lower frequencies, while maintaining sub 1-dB insertion loss and isolation >25 dB up to 2.5 GHz. However, the reliability of SiGe BiCMOS switches at high power levels has to date not been investigated. RF stress is applied at 9.5 GHz (in the middle of X-band) for 300 seconds when the switch is 'ON' by using an RF source and an external amplifier with a gain of 37 dB. All losses were calibrated using a power sensor to de-embed the RF power applied to the switch. S-parameters were measured while sweeping frequency from 1 GHz to 20 GHz. The switches were stressed at input power levels between 24 dBm and 33 dBm, in 3 dB steps. The measurement setup is described in detail in Section 5.1.

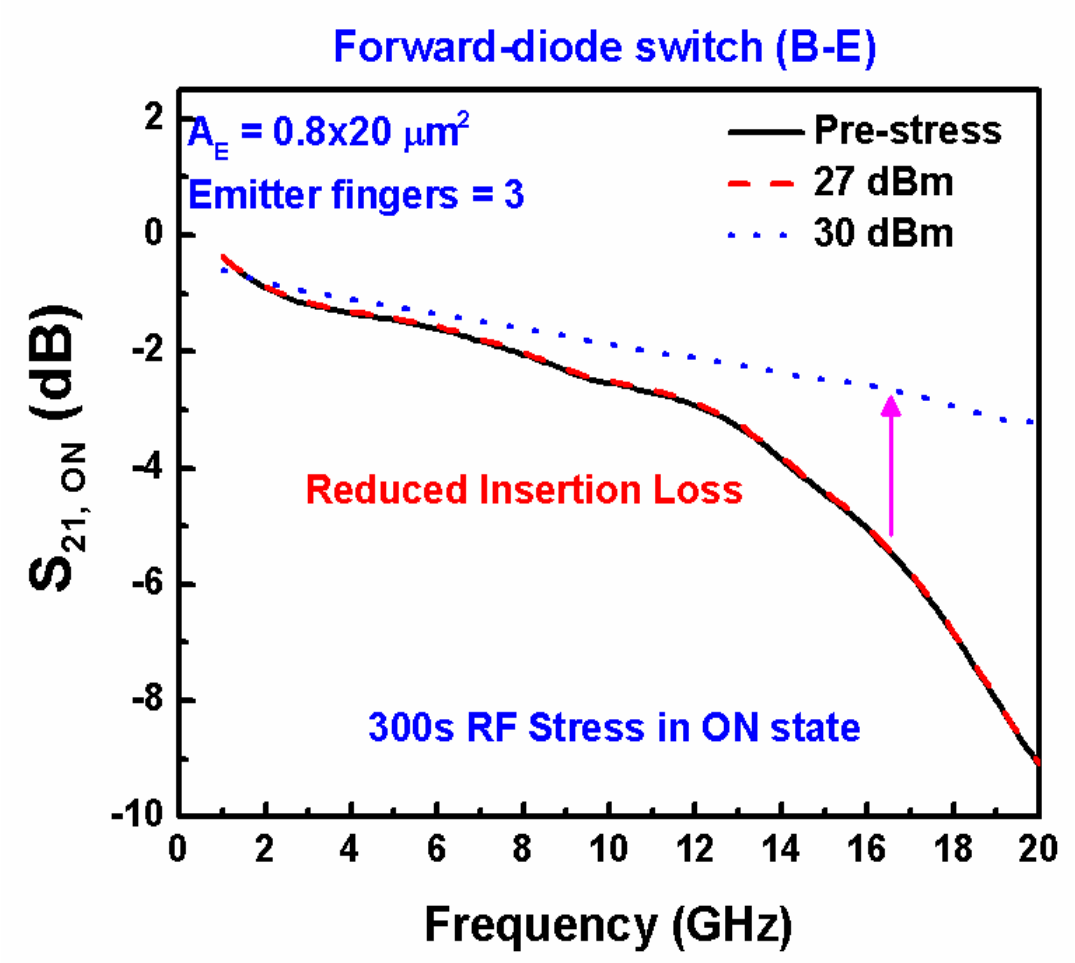


Figure 44. The insertion-loss of forward-mode switch improves after stressing at 30 dBm RF power for 300 seconds.

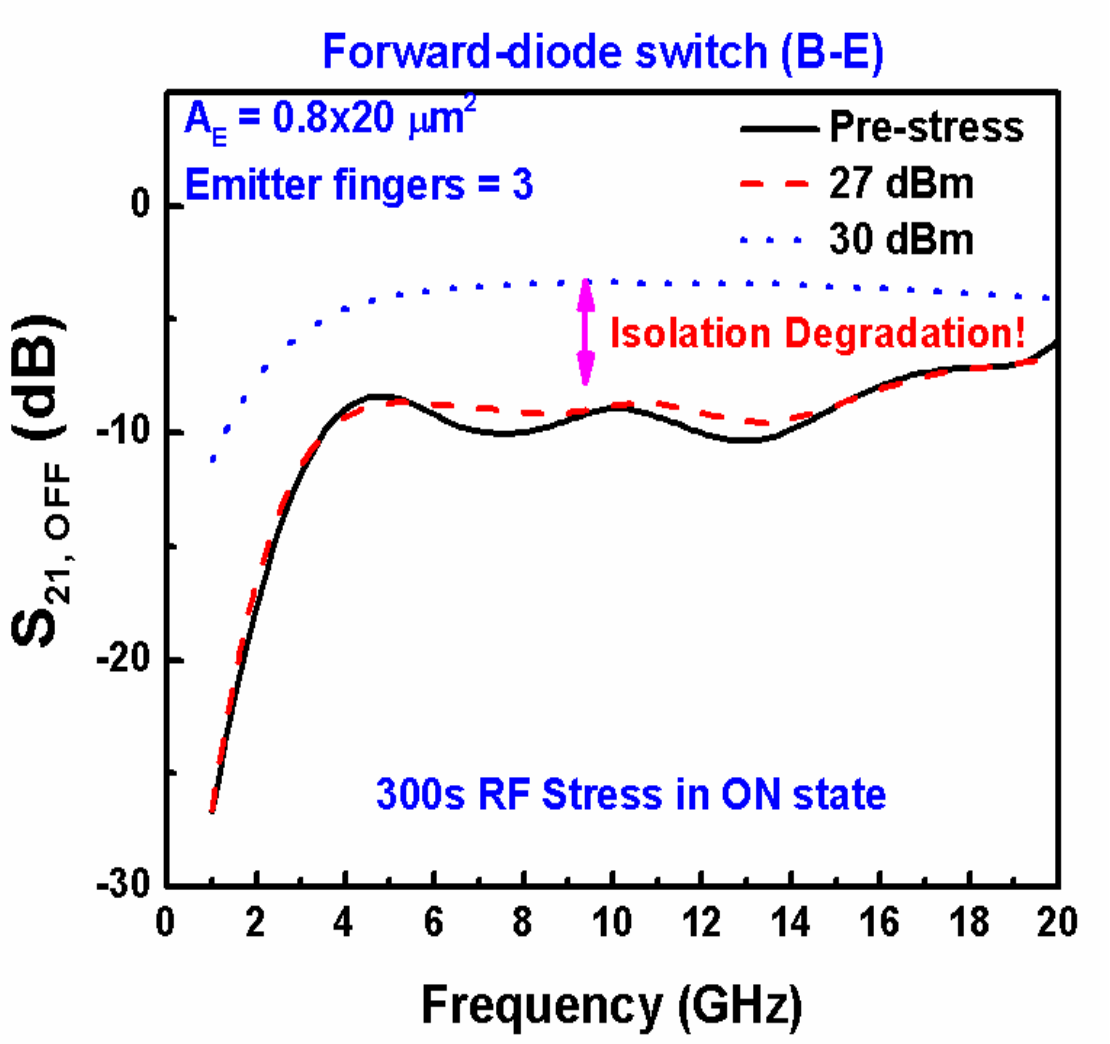


Figure 45. The isolation of the switch is considerably degraded after stressing at 30 dBm RF power due to the junction damage at the base-emitter interface.

Figure 44 shows the impact of RF stress on the insertion loss of the forward-mode switch. There was no change in performance after the switch was stressed at 24 dBm and 27 dBm for 300 seconds. Interestingly, after stressing at 30 dBm RF power, the switch showed an improvement in insertion loss. Figure 45 shows the isolation degradation observed in the switch at 30 dBm, leading to a near-failure condition (~5 dB drop in isolation).

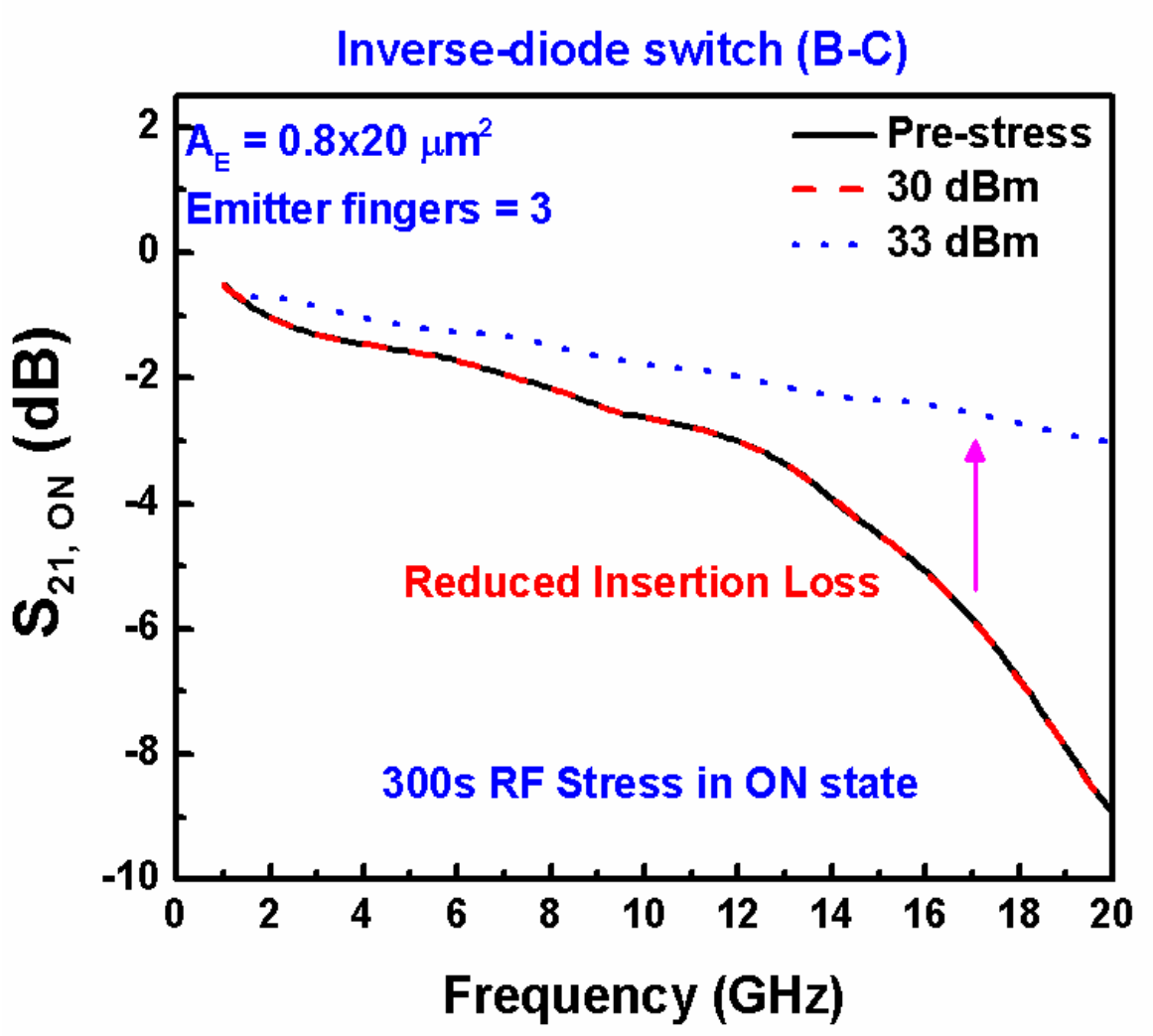


Figure 46. Insertion loss of inverse-mode switch improves, but after stressing at 33 dBm RF power for 300 seconds. There is no change after stressing at 30 dBm RF power.

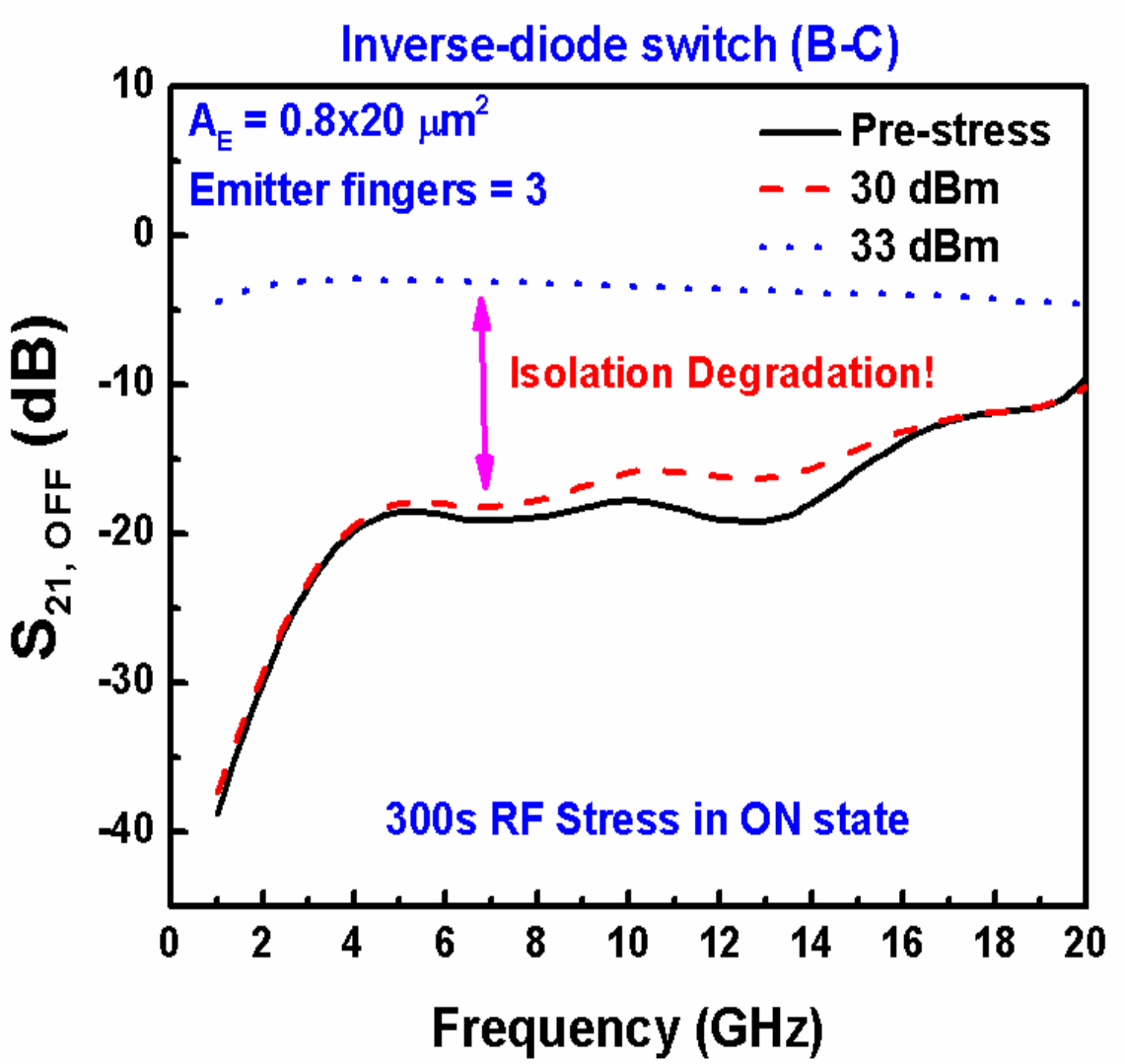


Figure 47. Isolation degradation similar to forward-mode switch is observed, indicating failure of the switch at 33 dBm RF input power.

This is contrary to known behavior for CMOS switches, where insertion loss degrades after RF stress due to gate oxide degradation [Section 5.1]. The improvement in insertion loss and degradation in isolation in the SiGe BiCMOS switches is highly suggestive of the junction damage in the base-emitter junction. Due to the damaged junction, the switch stayed nearly ON, even when the pFET was pulled up. If the shunt

pFET was damaged due to high RF power, then one would expect degradation in the insertion loss. Similar degradation was observed in insertion loss and isolation of inverse-mode switches, as shown in Figure 46 and 47, respectively. However, in the inverse-mode switch, the damage was observed after stressing the switch at 33 dBm for 300 seconds in ON state. The higher power handling capability of the inverse-mode switch is due to the higher value of BV_{CBO} compared to BV_{EBO} in the SiGe HBT.

CHAPTER 6

HIGH DYNAMIC RANGE SOI CMOS LNA

6.1 Introduction

High data rate wireless local area networks (LAN) have fueled the rapid growth of portable electronics. To keep the overall solution cost of portable devices low, the wireless transceiver should be highly integrated with the baseband as a System-on-Chip (SoC) solution, preferably using a low-complexity CMOS process [40]. Due to the scaling-induced reduction in supply voltage it has become increasingly difficult to integrate the RF front-end on the same chip with the digital baseband circuits, while also obtaining the required RF performance. As a result, "front-end modules" are typically used, which incorporate performance-critical blocks such as the RF switch and the low-noise amplifier (LNA) on the receive side, and the power amplifier (PA) on the transmit side [41]. In a typical radio receiver front-end, the LNA is one of the key components since it dominates the radio sensitivity. The LNA design involves tradeoffs between noise-figure (NF), gain, power dissipation, input matching, and linearity in the output signal. Adding in progressively lower power dissipation constraints inherent to battery-powered portable applications, a primary challenge in LNA design is achieving simultaneous noise and input matching at any given amount of power dissipation. Moreover, the amplifier's compression point requirement also imposes a limitation on the LNA transistor size, making the simultaneous noise and input match even more difficult to achieve in practice.

An integrated 5-GHz LNA implemented in floating body SOI CMOS technology is described in this letter. The 0.18 μm SOI CMOS technology, originally intended for RF switch applications [42], allows one to achieve sub-1.0 dB NF for the 5-GHz LNA. The role of the body-contacted SOI MOSFET in LNA design is also investigated. To the best of our knowledge, this work reports state-of-the-art noise performance, linearity and improved LNA figures-of-merit for silicon-based 5-GHz LNAs targeting WLAN applications.

6.2 Design of the CMOS LNA

The schematic diagram of the proposed LNA is shown in Figure 48. The LNA employs a cascode topology to realize the required gain and provide isolation between the receive port and the antenna. All of the matching elements are on-chip, and all capacitors are implemented as integrated MIM capacitors. The isolated SOI substrate enables high-Q inductors to minimize the loss through matching network. In addition, bond-wire inductance is absorbed in the matching network. The inductively-degenerated LNA can simultaneously achieve minimum NF, input impedance matching, and maximum transconductance gain. The input impedance of the inductively degenerated LNA can be expressed as:

$$Z_{in} = \frac{1}{j\omega C_{gs}} + j\omega(L_g + L_s) + \frac{g_m L_s}{j\omega C_{gs}} \qquad .. (1)$$

where g_m is the device transconductance and C_{gs} is the intrinsic gate-to-source capacitance of transistor M1. To match the input impedance to 50 Ω, the imaginary part of the impedance can be eliminated by resonating C_{gs} and (L_g + L_s) at an operating frequency of 5 GHz. The real part of the input impedance is shown as:

$$Z_{in} = \frac{g_m L_s}{j\omega C_{gs}} \quad \text{.. (2)}$$

The inductors used are 0.4 nH for L_s, 3.7 nH for L_g, and 2.2 nH for load inductor; the simulated quality factors, based on electro-magnetic simulations at 5 GHz are 7.8, 22.7 and 20.2, respectively.

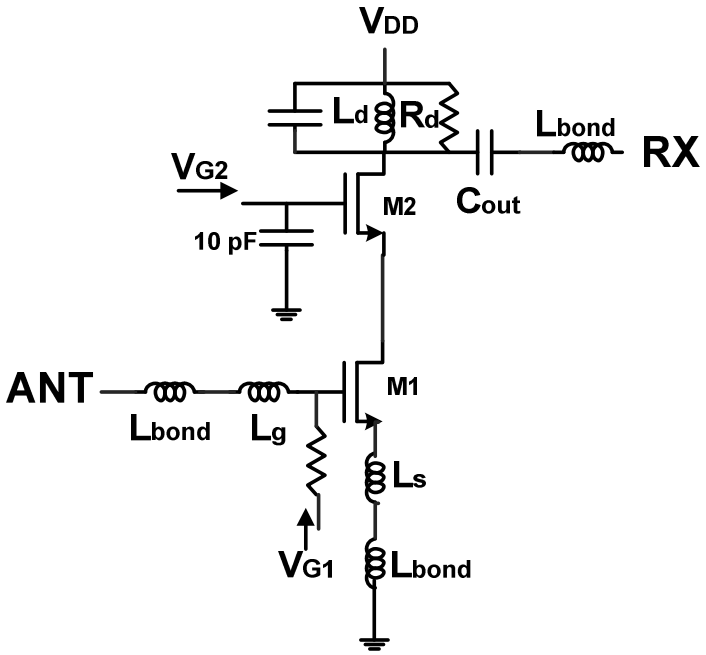


Figure 48. Circuit schematic of the inductively-degenerated cascode LNA.

6.3 Experimental Results

To validate the design and probe the impact of various technology options, the LNA has been fabricated in a 0.18 µm SOI CMOS process, with both floating-body and body-contacted FETs. The die photograph of the proposed LNA is shown in Figure 49. The active die area of the fully integrated LNA is 450 µm x 650 µm (excluding the pads). On-chip MIM capacitors serve to decouple *dc* supply. All measurements were performed on a FR-4 board after mounting the die directly on the board.

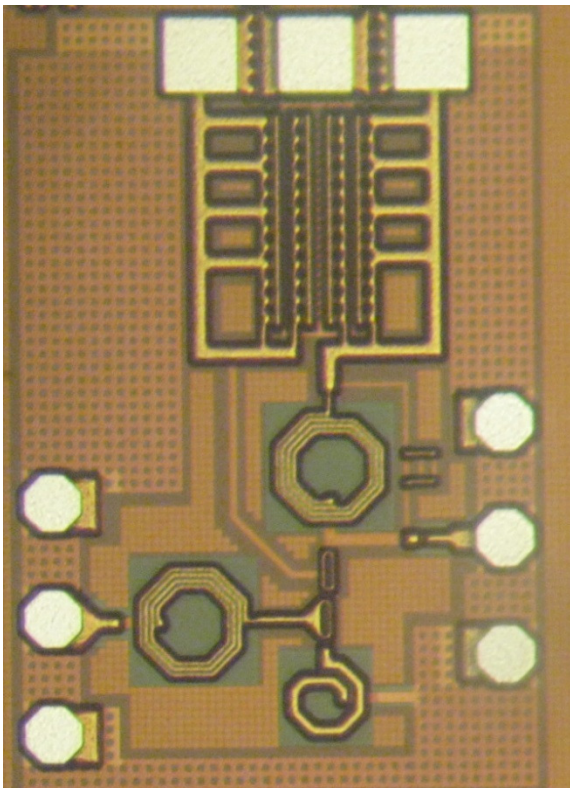


Figure 49. Die photograph of the fabricated LNA.

The measured S-parameters of the floating-body LNA are plotted in Figure 50. Due to the combination of the on-chip matching network and the bond-wire inductance, the input return loss is 33 dB at 5 GHz, while the output return loss is 13 dB at 5 GHz. A small-signal gain of 11 dB at 5 GHz is obtained with a supply voltage of 1.5 V and total current of 8 mA. Due to additional input capacitance (C_{gb}) associated with the body-contacted FET, a slightly different inductor value (L_g) at the input gives an input return loss of 22 dB, as shown in Figure 50. The gain of the body-contacted LNA biased at the same current is reduced to 9.3 dB, primarily because of lower transconductance (g_m) of the body-contacted device as compared to the floating body device.

A 0.95 dB NF with an error of +/- 0.05 dB is measured across five samples at

room-temperature for the floating-body LNA at 5 GHz, as shown in Figure 51. When the body terminal of the FETs is tied to its source terminal in the body-contacted LNA, the increased gate resistance due to the polysilicon abutting the body-contact degrades the NF to 1.9 dB at 5 GHz.

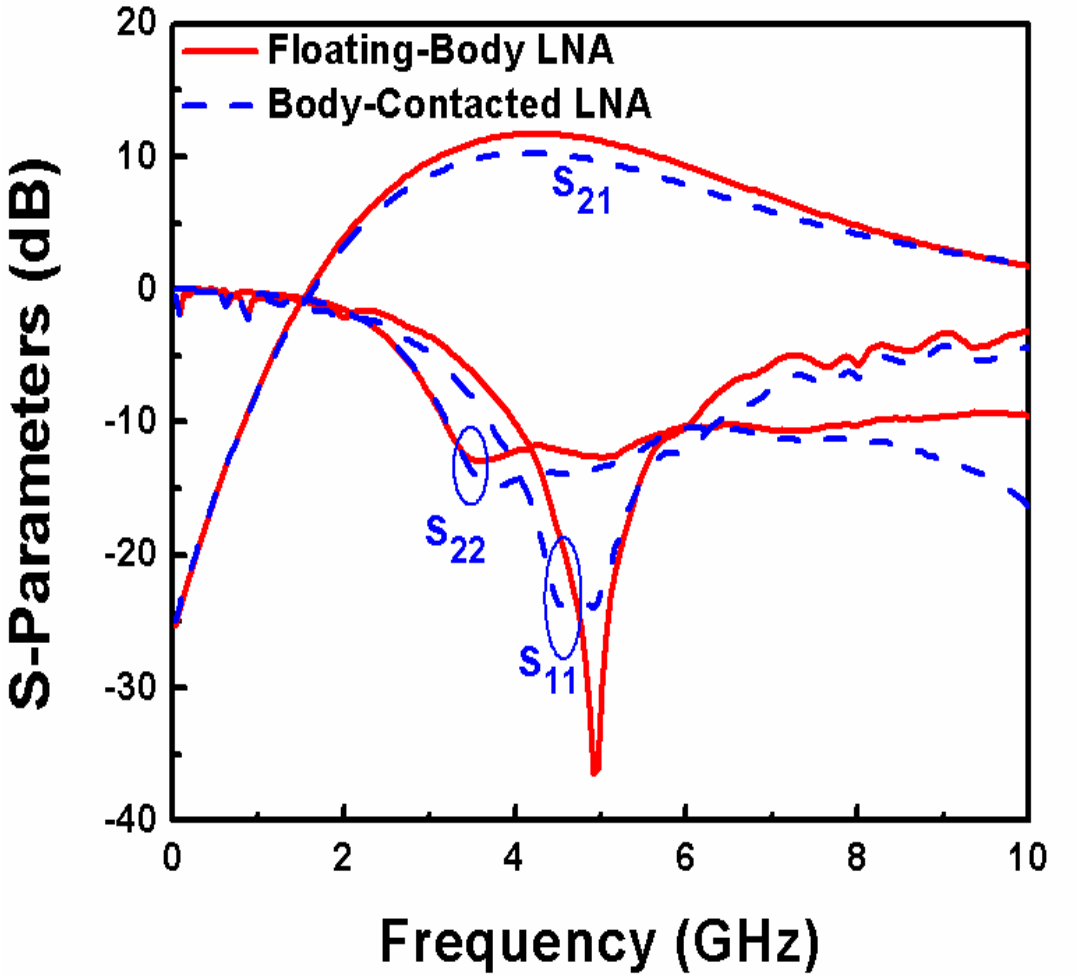


Figure 50. S-parameters of floating-body and body-contacted LNA with integrated input and output matched to 50 Ω.

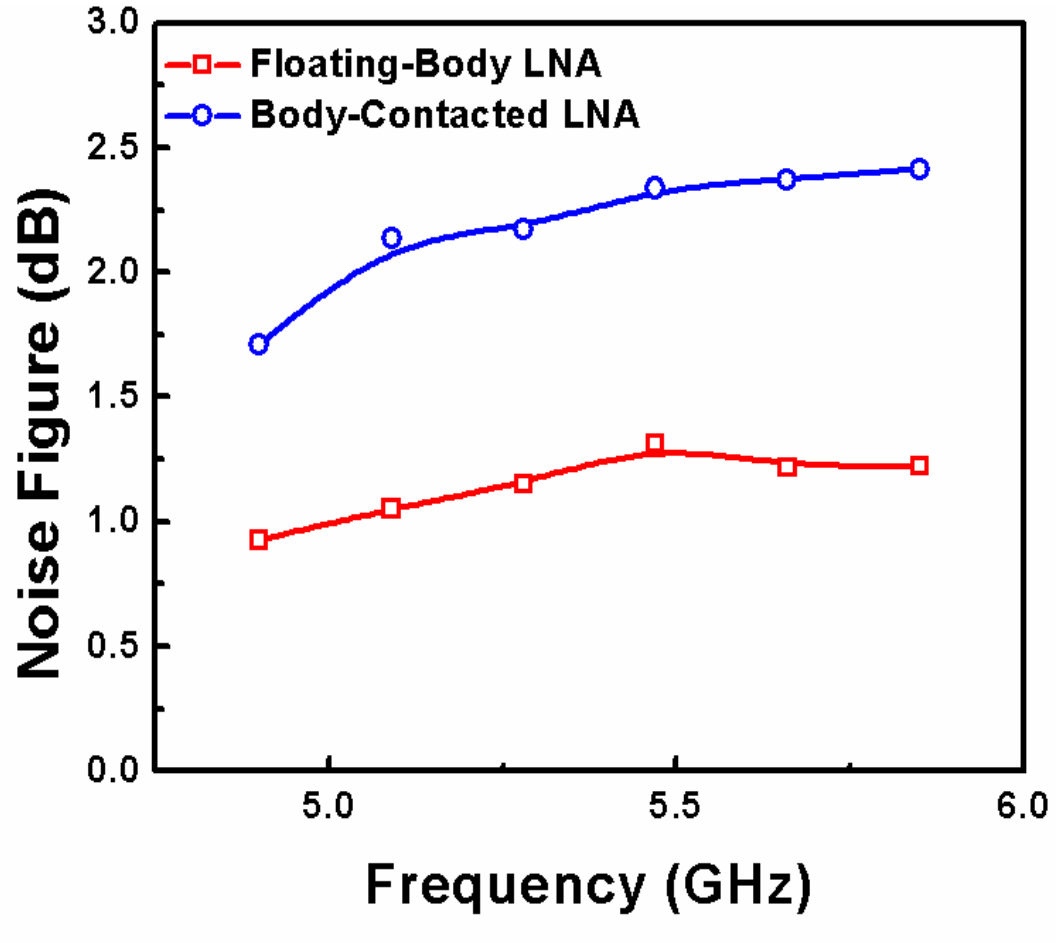


Figure 51. Measured NF of the LNA after de-embedding the input board loss.

Power handling capability of the LNA is critical for WLAN applications in order to avoid LNA compression and preserve the modulated signal received at the front-end. The input 1-dB compression point ($P_{1\text{-dB}}$) for the LNAs was measured to be -7 dBm, as shown in Figure 52(a). A two-tone test with equal power levels at 5.000 GHz and 5.001 GHz was performed to measure the input third-order intercept point (IIP3), as shown in Figure 52(b). The floating-body LNA has an IIP3 of 5 dBm while the body-contacted LNA has an IIP3 of 6.5 dBm.

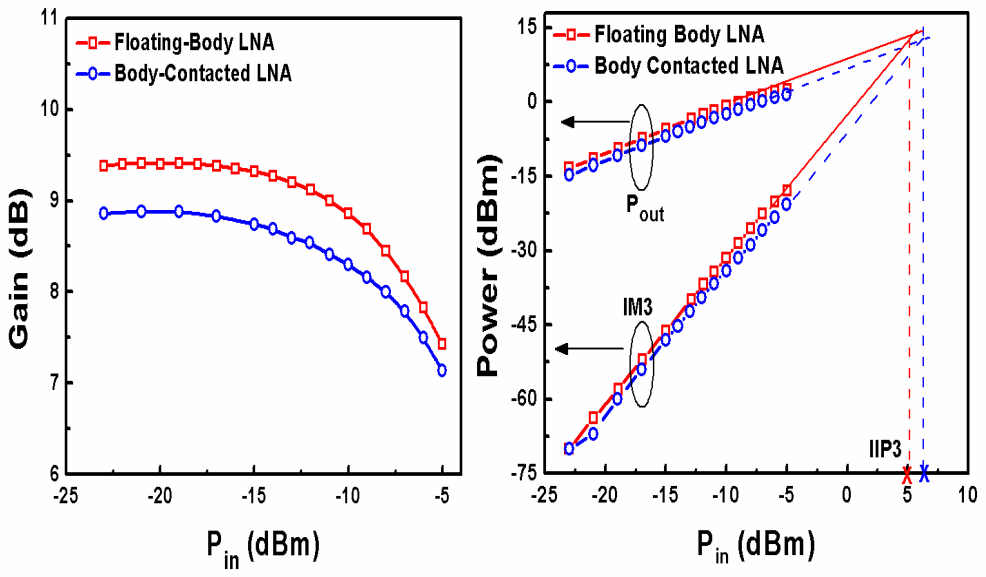


Figure 52. (a) Measured input $P_{1\text{-dB}}$ compression point of LNAs, and (b) comparison of measured harmonics and IIP3 of the floating-body and body-contacted, single-stage, inductively degenerated, cascode LNA.

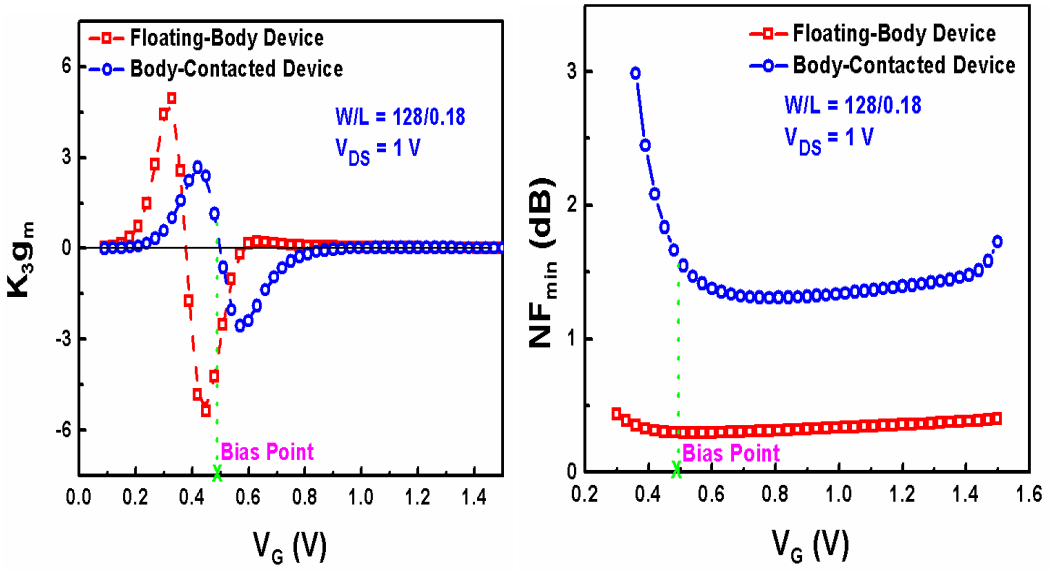


Figure 53. (a) Simulated K_3g_m, and (b) NF_{min} comparison of the floating-body and body-contacted input device of the LNA.

In Figure 53(a), simulated results show that the body-contacted device is biased closed to the minima of third-order derivative of drain current with respect to gate voltage (K_3g_m). Since IIP3 is directly proportional to K_3g_m, body-contacted device has a higher measured IIP3, as shown in Figure 52(b). Minimum-achievable noise-figure (NF_{min}) for a body-contacted device is 1-dB higher than the floating-body device, as illustrated in Fig. 53(b). This result is in harmony with measured NF difference for the two LNAs in Figure 51.

To evaluate the performance of the LNAs, different figures- of-merit (FOM) are often used. One figure-of-merit (FOM_1) is the ratio of the gain (in dB) to the dc power consumption (in mW), which is more commonly used for comparing low-power LNAs. Furthermore, it can be expanded to include the NF, IIP3, and operating frequency (f_c) as follows [43]. A larger FOM is better in all cases.

$$FOM_2 = \frac{Gain[abs]}{(NF-1)[abs].P_{DC}[mW]}$$

$$FOM_3 = \frac{Gain[abs].IIP3[mW].fc[GHz]}{(NF-1)[abs].P_{DC}[mW]}$$

A comparison between the present LNAs and other recently published LNAs is presented in Table I. It should be noted that all of the LNAs shown are fully integrated without off-chip components. By achieving a 0.95 dB NF while consuming 12 mW, this LNA exhibits the lowest NF and highest FOM_3. Furthermore, the proposed LNA also meets the stringent wireless LAN standards demanding high linearity and power-handling capability for the 802.11a/n standard.

TABLE I

PERFORMANCE COMPARISON BETWEEN RECENTLY PUBLISHED LNAS

	This work		[43]	[44]	[45]	[46]	[47]
	FB	**BC**					
Tech [µm]	0.18 SOI	0.18 SOI	0.13	0.13 SOI	0.18	0.18	0.09
Freq [GHz]	5.0	5.0	5.5	5.0	5.0	5.2	5.5
NF [dB]	0.95	1.9	2.6	1.4	4.1	1.1	2.9
V_{DD} [V]	1.5	1.5	1.2	1.2	0.6	1.8	1.2
P_{DC} [mW]	12	12	6.6	10	0.8	12.4	9.72
Gain [dB]	11.0	9.3	14.8	14	10.2	16.5	13.3
S_{11} [dB]	-33	-22	-	-12	-17.9	-	-14.4
S_{12} [dB]	-28	-28	-	-	-	-	-28
$P_{in\text{-}1dB}$ [dBm]	-7	-7	-	-	-23.8	-	-11.5
IIP3 [dBm]	5	6.5	-9	-	-15	-7.2	-3
FOM_1 [dB/mW]	0.92	0.78	2.24	1.4	12.8	2.76	1.37
FOM_2 [mW^{-1}]	1.21	0.44	1.01	1.31	2.57	1.87	0.5
FOM_3 [MHz]	19.11	9.83	0.7	-	0.41	1.85	1.38

6.4 Summary

We have presented a fully-integrated 5 GHz LNA for 802.11a/n WLAN applications. This state-of-the-art LNA features a NF below 1.0 dB and 11 dB power gain, while consuming 12 mW of power and maintaining an input return loss of 33 dB. The measured input 1-dB compression point at 5 GHz is -7 dBm, while IIP3 is 5 dBm. The body-contacted FET LNA performance is compared with the floating-body LNA. Due to the extra gate resistance and better control of body potential relative to source, the body-contacted FET based LNA is seen to have higher NF, but marginally better intermodulation performance.

CHAPTER 7

SWITCH AND LNA INTEGRATION FOR FEICS

7.1 Introduction

Wireless local area network (WLAN) systems switch between transmit and receive functionality using a single-pole double-throw (SPDT) RF switch at the front-end. However, most of the modern WLAN module architectures have settled on the use of a SP3T switch in order to also incorporate bluetooth (BT) functionality [48, 49]. This allows the common blocks such as crystal oscillator, bandgap reference, and power management units to be shared between WLAN and bluetooth, thus saving die size, I/O count, and cost. To keep the overall solution cost down, the transceiver should be highly integrated with the baseband PHY and MAC as a System-on-Chip (SoC) solution, preferably in a low-complexity pure CMOS process [50 – 53]. Due to extensive CMOS scaling (sub-100 nm) and integration of the WLAN transceiver with baseband, it has become extremely difficult to integrate the RF front-end on the same chip to obtain the desired performance. Thus, a standalone front-end module is typically used, which includes performance critical blocks such as the RF switch, the low-noise amplifier on the receive side, and the power amplifier on the transmit side [54, 55]. Lately, standalone WLAN power amplifiers, and a power amplifier integrated with the WLAN transceiver have been demonstrated in highly-scaled 65 nm CMOS technology [56, 57]. This approach necessitates RF front-end modules with only switch and LNA functionality for use with WLAN chipsets with integrated PAs.

Therefore, integrated SP3T and LNA as flip-chip die using GaAs pHEMT processes

have been reported [58, 59]. WLAN switches have been historically dominated by GaAs platforms because of their superior high power handling capability and semi-insulating substrate. Owing to low mobility, high substrate conductivity, low breakdown voltage, and various parasitic parameters of CMOS processes, it is very challenging to design CMOS switches and LNA to simultaneously achieve low-insertion loss, high isolation, wide bandwidth, high power handling and low-noise comparable to their GaAs counterparts [60]. However, in the present work, the first implementation of a single-chip fully-integrated SP3T and LNA front-end on 0.18 μm CMOS is reported for 802.11b/g WLAN applications at 2.5 GHz. The integrated solution includes on-chip *dc* blocking, bypass-mode, matching network and ESD protection and drives the die-size (0.64 mm^2) towards a low-cost, fully-integrated solution.

One of the key constraints for a WLAN (or any portable) system is power dissipation. The most efficient technological approach for reducing power consumption is power-supply voltage reduction. However, front-end power supply voltage (V_{DD}) is usually constrained by transceiver architecture and system requirements. In a typical radio receiver front-end, the low-noise amplifier (LNA) is one of the key components since it dominates the radio sensitivity. The LNA design involves tradeoffs between noise figure (NF), gain, power dissipation, input matching and linearity. With the added power dissipation constraint inherent in portable applications, the primary goal for LNA design is to achieve simultaneous noise and input matching at any given amount of power dissipation. The amplifier's compression point requirement also imposes a limitation on the LNA device size, thus making the simultaneous noise and input match harder to achieve. When the mobile device is close to a base station, the input signal can be high

enough to overdrive the amplifier and thereby cause distortion [61]. A bypass mode is incorporated into the receive functionality which allows the amplifier to be switched into a low gain mode when the device is close to a base station [62]. Usually the switching and LNA functions are achieved using two separate dies. This work presents a fully-integrated single-chip RF front-end solution for WLAN chipsets with integrated power amplifier. The power-handling techniques, as described in Section IV, allow one to achieve record power handling performance while maintaining competitive insertion loss with state-of-the-art CMOS T/R switches at 2.4 GHz without bluetooth functionality.

7.2 180 nm CMOS Technology

.The Front-End Integrated-Circuit (FEIC) has been fabricated in IBM's 180-nm bulk CMOS process. IBM's 7RF starting wafer is lightly doped p-type Si with a resistivity of 11 – 16 Ω-cm [63]. A low resistivity substrate can be detrimental for RF applications since it provides an extra capacitive component to the substrate. To verify the nature of the substrate in an RF context, an inductor's S-parameters were measured and substrate resistivity was used as a back-fit parameter in EM simulations, as shown in Figure 54(a). The substrate resistivity was verified to be 13 Ω-cm.

The technology utilizes a twin-well CMOS process with shallow-trench isolation to provide isolation between FETs and other devices. Both thin and thick gate-oxide FETs are available in the technology, with an operating voltage of 1.8 V and 3.3 V, respectively. Triple-well isolation is provided for both types of FETs for improved substrate isolation. MIM caps, spiral inductors and transmission lines for RF interconnects are also provided as back-end passives. Finally, this technology uses copper

wiring at the first metal level and aluminum wiring at the subsequent metal levels, as shown in Figure 54(b). A three-layer metal stack is used for the present design.

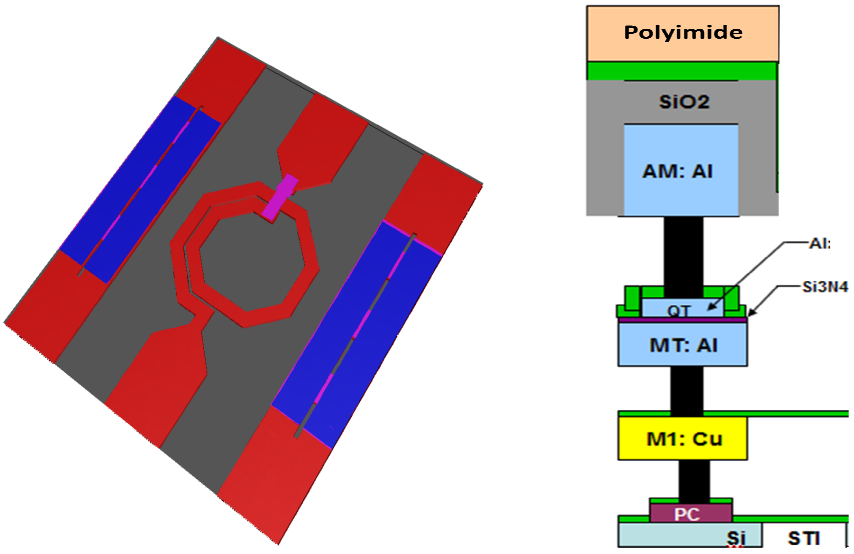


Figure 54(a). 3-D EM view of the inductor, and (b) back-end-of-line metal layers used in the three metal layer process.

7.3 RF Front-end IC Architecture

The front-end IC (FEIC) is a single-chip solution with a bluetooth port to complement WLAN chipsets with integrated power amplifier. The FEIC integrates a SP3T switch and a low-noise amplifier with bypass mode. It is capable of switching between WLAN receive, WLAN transmit and bluetooth, as illustrated in Figure 55.

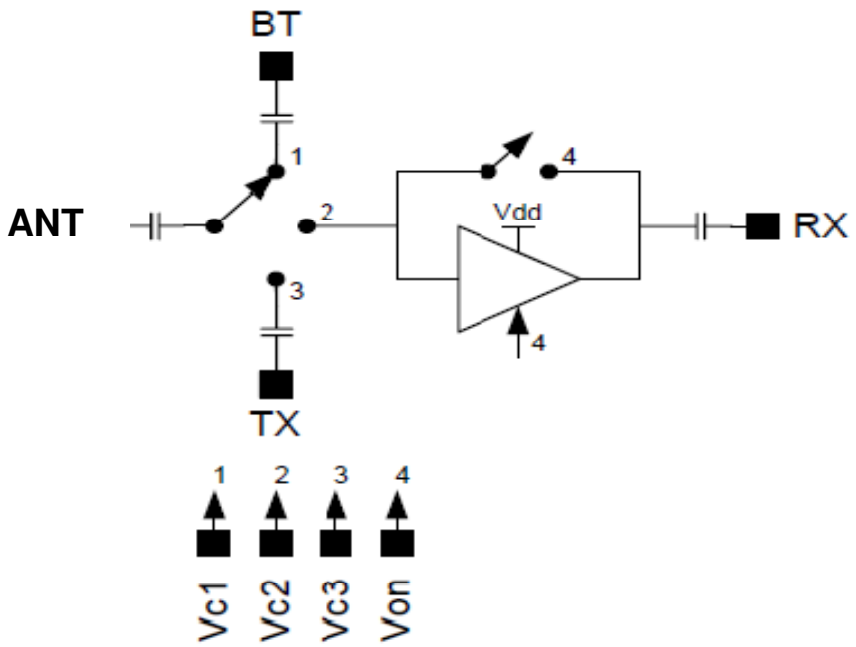


Figure 55. Architecture of a switch-LNA WLAN front-end with integrated bluetooth functionality.

When the transmit mode is ON, the signal from the PA is fed into the TX pin and the transmit throw of the switch is turned on. This allows the signal to be switched and propagated through to the antenna (ANT). In view of this architecture, one of the most critical specifications for the transmit and bluetooth switch is insertion loss. The maximum transmitted power of the system is reduced by the insertion loss of the transmit switch. Similarly, on the receive side, the insertion loss of the switch adds directly to the noise figure of the receiver. To avoid any interference from the WLAN transmit signal in the BT chain, adequate isolation is required between TX/RX and BT port of the SP3T. Hence, the number of shunt devices (for the on-throw) and series devices (for two off-throws) are critical to meet this isolation specification. Moreover, the Federal

Communications Commission (FCC) imposes strict regulations for out-of-band RF emission, thus limiting the maximum modulated harmonics from the switch.

TABLE II

CONTROLLER LOGIC FOR FEIC OPERATION

Mode#	Description	Vc1	Vc2	Vc3	Von
0	All Off	0	0	0	0
1	TX	0	0	1	0
2	BT	1	0	0	0
3	RX – high gain	0	1	0	1
4	RX – bypass	0	1	0	0

The FEIC is controlled by a logic decoder with four inputs and five modes, as shown in Table II. When the RX mode is enabled, Vc2 is set to high and the LNA is cascaded with the switch to improve the sensitivity of the receiver. The LNA shares a 3.3 V supply voltage with the switches and is turned on when both Vc2 and Von are high. To avoid overdriving the LNA and causing distortion from a strong RF input signal, a bypass mode is provided in the LNA. The bypass mode is turned on when Vc2 is high and Von is low. The LNA is matched on-chip and all necessary paths are *dc* blocked with MIM caps. The sizes of series *dc* blocking MIM caps are chosen to provide optimum match at the frequency of interest.

7.4 Design Methodology

Key figures-of-merit of a RF switch include insertion loss, isolation, and power-handling capability, as measured by the power 1-dB compression point (P_{1dB}). CMOS switches usually have a lower power-handling capability compared to III-V pHEMT switches due to their lower breakdown voltage and the parasitic diodes between source/drain and the body. To improve the power handling capability and linearity of the

switches, the following methods are used, as shown in Figure 56:

(i) the bulk and n-well terminals of triple-well nMOS are kept floating (from a RF standpoint) to avoid forward biasing of parasitic diodes under large input signal [64],

(ii) the series and shunt transistors are stacked to sustain higher voltage swings and therefore improve the power handling of the switch [65 – 67], and

(iii) a cross-biasing arrangement is used in a series-shunt switch topology to *dc* bias the source and drain terminals for maximum swing across each transistor. The source and drain are kept at the same *dc* potential by means of a polysilicon resistor tied between the two terminals.

Isolated triple-well nMOS devices use deep n-well to isolate the p-well and divide the voltage swing in a stack of devices. The deep n-well separates the bulk of the nMOS transistors from the p-substrate. The p-well and deep n-well are left floating, thus reducing the parasitic loss by increasing the effective impedance in the body of the device, as shown in Figure 56. The p-well is biased at 0 V, and the deep n-well is biased at 3.3 V through 20 kΩ polysilicon resistors to reverse bias the p-n junctions, reducing the parasitic capacitance associated with the diodes.

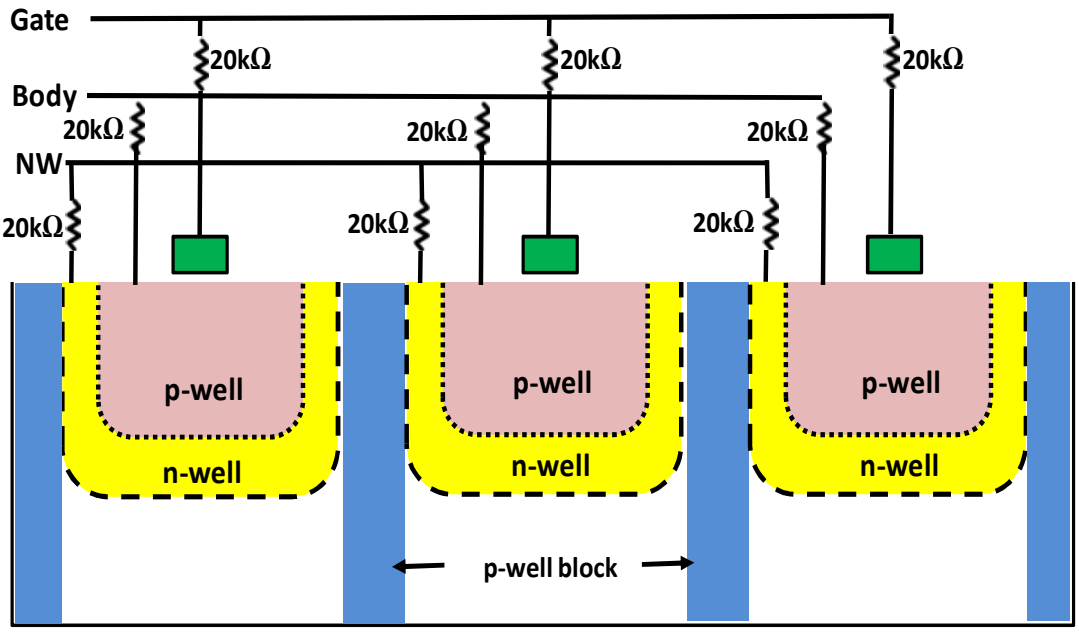


Figure 56. A stack of three series transistors with isolated gate, p-well and n-well using 20 kΩ polysilicon resistors.

At high frequency, the power handling of switch FETs is limited by voltage swing in the 'off' state (capacitive state) and current saturation in the 'on' state (resistive state). The series and shunt stacks are composed of two to three FETs each, so that the voltage across the stack is evenly divided among these FETs. Even though a three FET switch stack multiplies the voltage handling capability ideally by 3x, it also increases the insertion loss by adding the on-resistance of the three transistors in series. Thus, the increased power handling typically comes at the cost of higher insertion loss.

7.4.1 TX Switch Topology

A series-shunt topology was chosen for the TX switch, as shown in Figure 57. The transmit mode needs to handle more than one-watt (30 dBm) of RF power while

maintaining minimal insertion loss. When the transmit switch is on, the shunt (off) devices limit the maximum voltage swing before the parasitic diodes in the shunt transistors turn on and the switch starts to operate in compression. To minimize insertion loss of the transmit path, an asymmetrical switch design is used [61, 66]. An asymmetrical topology uses different switch stack designs for each switch throw, whereas a symmetrical topology adopts the same configuration in all throws with the most commonly used series-shunt configuration.

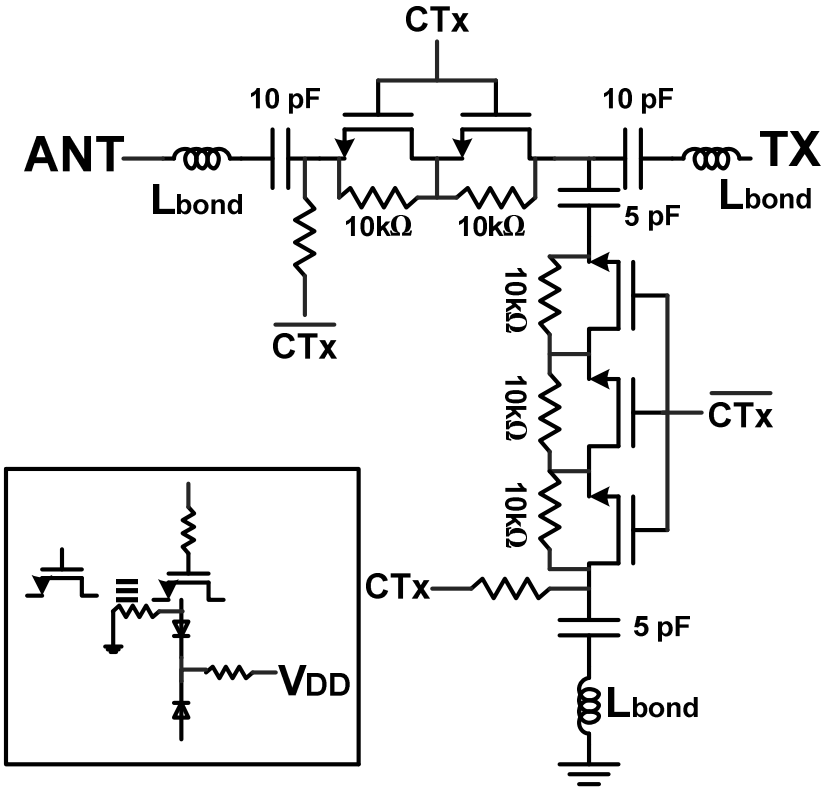


Figure 57. Series-shunt stacked FET switch topology with cross-biasing for the transmit switch.

The correct balance between the on-resistance, parasitic capacitance and harmonics requirement must be established to size the devices correctly. While a bigger device

allows lower on-resistance (and thus smaller insertion loss), it also has higher capacitance in off-state, leading to a higher insertion loss for other 'on' switch paths (bluetooth and receive) in the SP3T. In this case, the width of the series transistors was chosen to be 1000 μm, while the width of the shunt transistors was chosen to be 400 μm. This geometry optimizes the performance of the RF switches at 2.5 GHz. Since cross biasing is used to bias the series-arm and shunt-leg, on-chip *dc* blocking MIM capacitors are required, as shown in Figure 58. In the final analysis, the *dc* power dissipated by the switch FET is only due to the leakage current in the device.

7.4.2 BT Switch Topology

The voltage swings 20 V peak-to-peak when a signal of 30 dBm is transmitted into 50 Ω on the transmit throw. Thus, the BT switch in "off" state should be able to tolerate this voltage swing without any of the series FETs turning "on". A stack of three series FETs is used in the bluetooth throw to withstand the high transmit voltage swing, as shown in Figure 58. Additionally, it should not dissipate significant signal power and should maintain good isolation between transmit and bluetooth ports. The transmit throw also needs to have a good isolation in the BT mode so as not to draw power from the antenna (ANT), which would increase insertion loss.

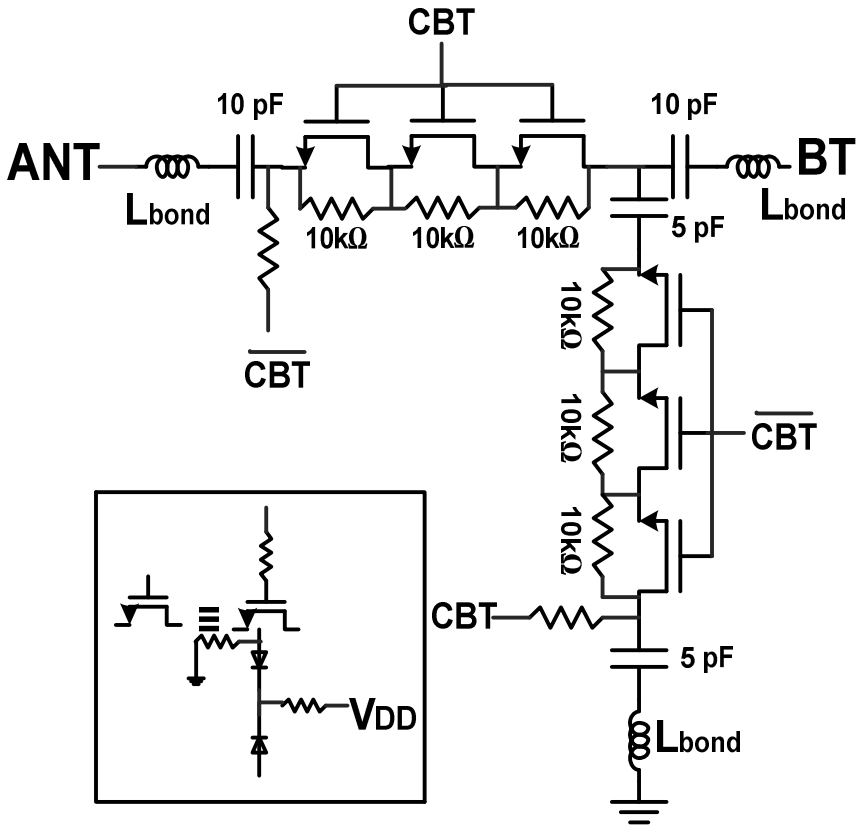


Figure 58. Series-shunt stack topology of the bluetooth switch with 3-series and 3-shunt stack of FETs.

7.4.3 RX Design

The switching part of the receive path uses a three-stack of series FETs. The shunt transistors are eliminated by adding a switch S1, which protects the LNA input from turning on due to the large voltage swing at the transmit output. Thus, S1 is turned on only during normal operation of the high-gain receive mode. The logic state CRX is set to high when either high-gain or bypass mode are enabled. The CLNA or CBYP are set to high when the high-gain or the bypass modes are enabled, respectively. The bypass switch uses a stack of four series transistors to maintain the required gain (-3 dB), as well

as to provide sufficient isolation between the input and the output of the LNA. To minimize feedback and maintain stable operation of the LNA, the bypass path is tapped after the first series transistor, as shown in Figure 59 below.

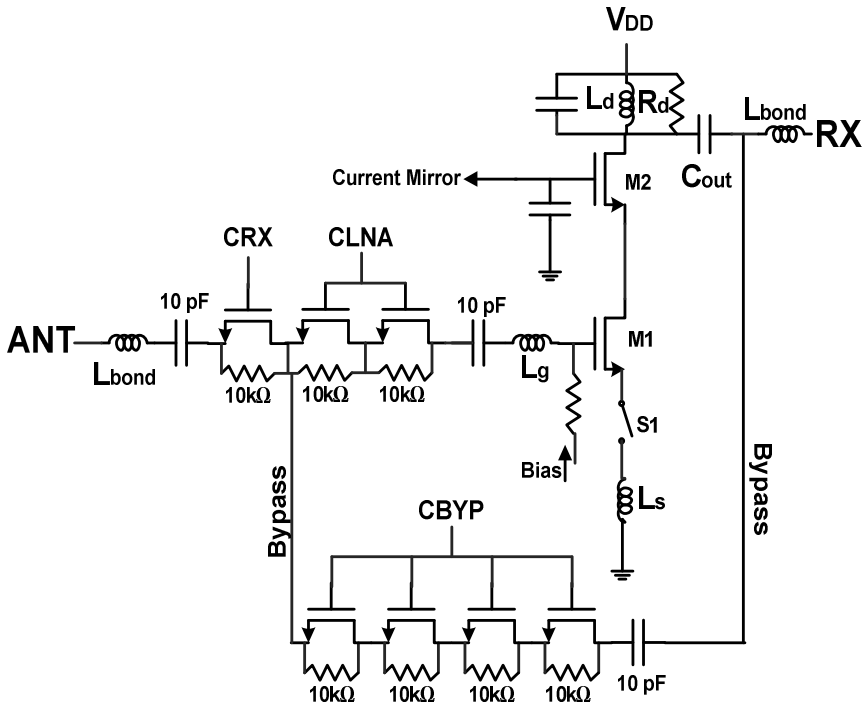


Figure 59. Schematic of the receive path with high-gain mode (switch + LNA) and bypass mode.

The LNA employs a cascode topology to realize high-gain and provide good isolation between the receive port and antenna. The 3.3 V thick-oxide cascode device (M2) enables direct operation with a 3.3 V rail, while the thin-oxide input device (M1) helps to minimize noise figure with a minimum channel length of 0.18µm. All of the matching elements are on-chip, and all the capacitors are implemented as MIM capacitors. The spiral inductor L_g utilizes a patterned ground shield structure, while the spiral inductor L_d is implemented without a ground shield to reduce the number of bond pads and hence the

die area. The Q-factor of the output inductor L_d is less significant because of the resistance $R_{d,}$ added to de-Q the output match for stable operation of the amplifier. The source degeneration inductance is implemented as a double bond-wire with an inductance of about 200 pH.

Once the drain current is fixed to 7 mA, the device width is scaled in order to move the real part of noise matching impedance close to 50 Ω. The gate widths of the FETs, M1 and M2, are both 300 μm. It is noteworthy that the devices cannot be sized too small due to the input P_{1dB} constraint. Hence, there is a three-fold tradeoff between *dc* power consumption, minimal noise figure and power handling requirements. The next step is to match the input impedance to 50 Ω, which is accomplished by the addition of bond wire degeneration inductor. The value for this inductor, L_s is given by:

$$Ls = \frac{50}{2\pi f_T} \qquad \ldots. (1)$$

where f_T is the cut-off frequency of the device at its operating point. Once the source degeneration inductance has been selected, the remaining portion of the input matching network, L_g, serves to resonate out the C_{GS} capacitance and conjugate match the reactive portion of the noise impedance. The following equation can be used to determine the value of L_g:

$$L_g = 1/(\omega^2 C_{GS}) - L_e \qquad \ldots. (2)$$

Typically, this type of matching network is very narrow band, and therefore is suitable for 802.11 b/g WLAN applications with less than 100 MHz bandwidth.

7.4.4 Controller Design

A simplified schematic of the logic controller is shown in Figure 60. Vc1 and Vc3 are buffered using NAND gates to provide enable signals for bluetooth and transmit throws, respectively. As shown in Table I, when Vc2 is high, either high-gain or bypass mode are enabled on the receive throw. Thus, the receive enable signal (CRx) is buffered from Vc2. Additional NAND logic is designed to enable the LNA in the high-gain mode, when both Vc2 and Von are high.

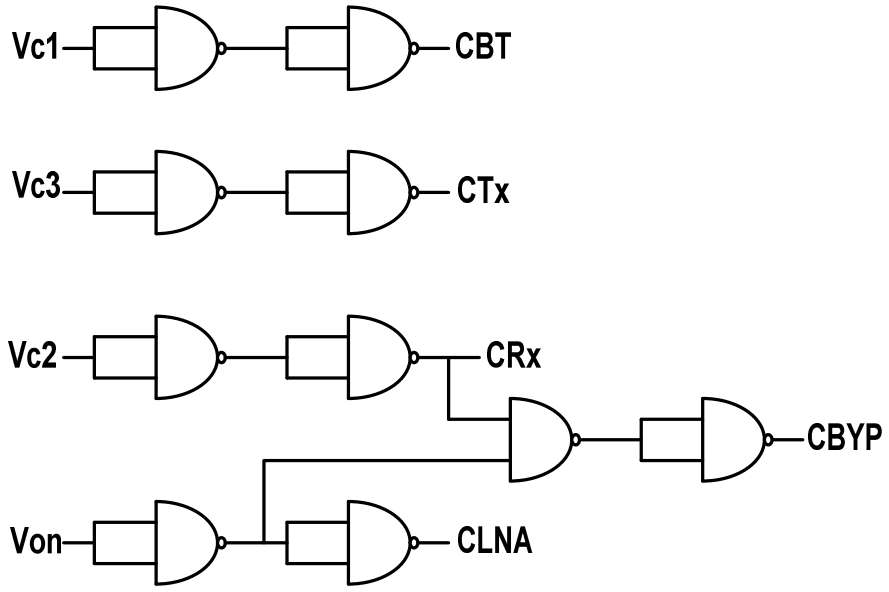


Figure 60. NAND gate based logic-decoder for switching between FEIC states.

7.5 Circuit Implementation

The IC was fabricated on 180-nm CMOS technology provided by IBM using a standard resistivity ($\rho \sim 13\ \Omega$-cm) substrate. The active devices used in the design are 1.8 V and 3.3 V nMOS transistors with triple-well isolation. The geometry of the active devices was chosen to minimize the contribution from substrate coupling, which cannot

be ignored in a low-resistivity bulk CMOS process. The values of the on-chip spiral inductors, L_g and L_d, have been optimized to 7.1 nH and 3 nH, respectively, as explained in Section IV.

A micrograph of the fabricated die is shown in Figure 61. The chip dimensions are 0.8 mm x 0.8 mm including on-chip *dc* blocking and decoupling MIM capacitors. The LNA draws 7 mA current from a 3.3 V supply.

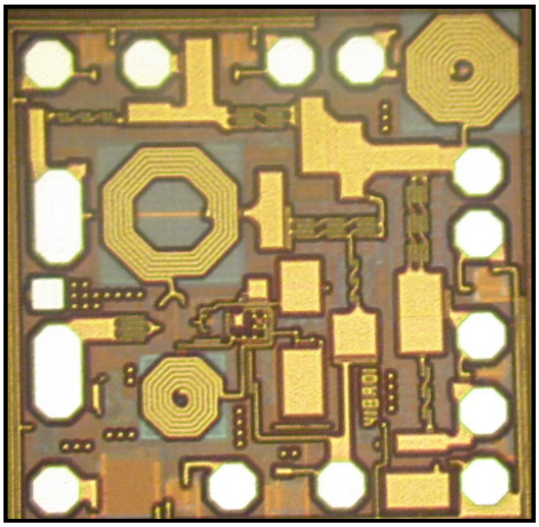


Figure 61. Die micrograph of the FEIC.

7.6 Results and Discussion

For all measurements, die were mounted directly on a FR-4 evaluation board and wire-bonded onto the respective traces. The reference plane for measurements is at the edge of the RF traces on the board.

7.6.1 Small-signal

The measured S-parameters of transmit and bluetooth switches are shown in Figure 62

and Figure 63, respectively. The 10 pF on-chip series MIM capacitor not only serves as a *dc* blocking capacitor, but it also helps improve return loss (and, in turn, insertion loss) of the switch. The measured insertion loss between the transmit port and antenna is 1.3 dB at 2.4 GHz, while between the antenna port and bluetooth port is 1.45 dB. The return loss is about 20 dB in both the cases. Thus, the higher insertion loss for the bluetooth throw can be attributed to the extra series transistor in the bluetooth path. It is noteworthy that the S-parameters are measured after terminating the remaining ports with 50 Ω load. The isolation between bluetooth and transmit throws is shown in Figure 64. The measured in-band isolation between transmit and bluetooth port is better than 28 dB. This prevents the transmit signal from leaking into the bluetooth path, and vice versa.

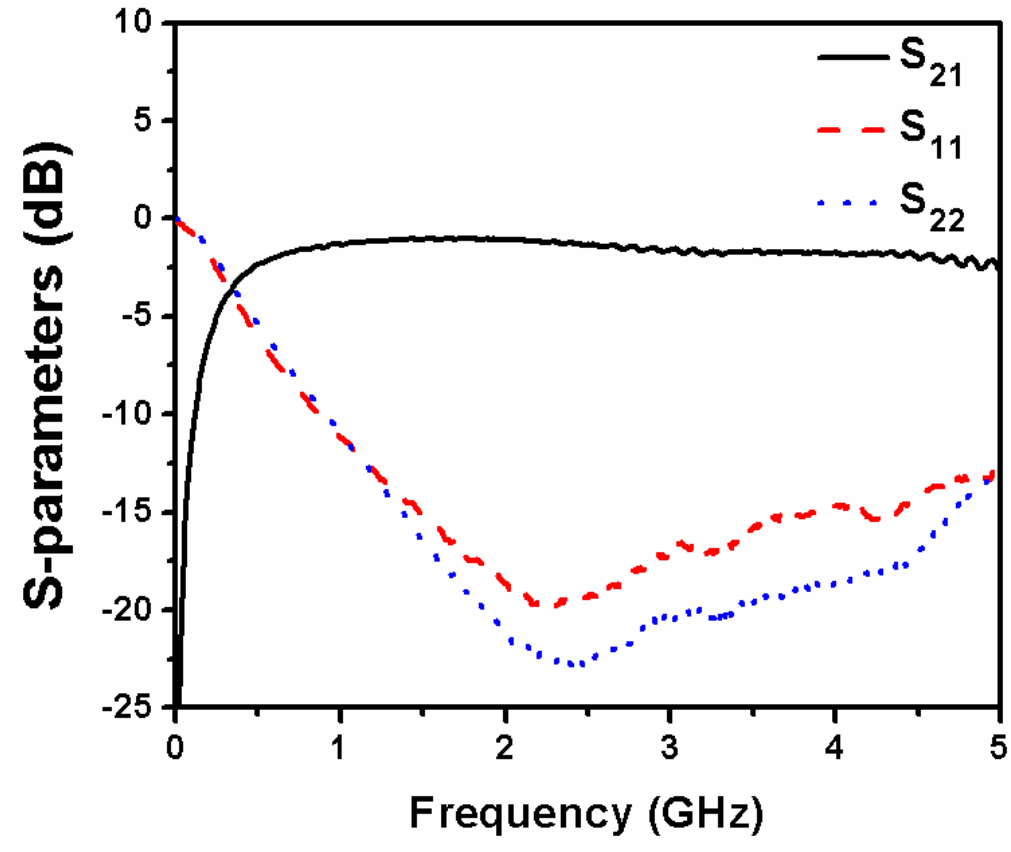


Figure 62. S-parameters of the transmit switch

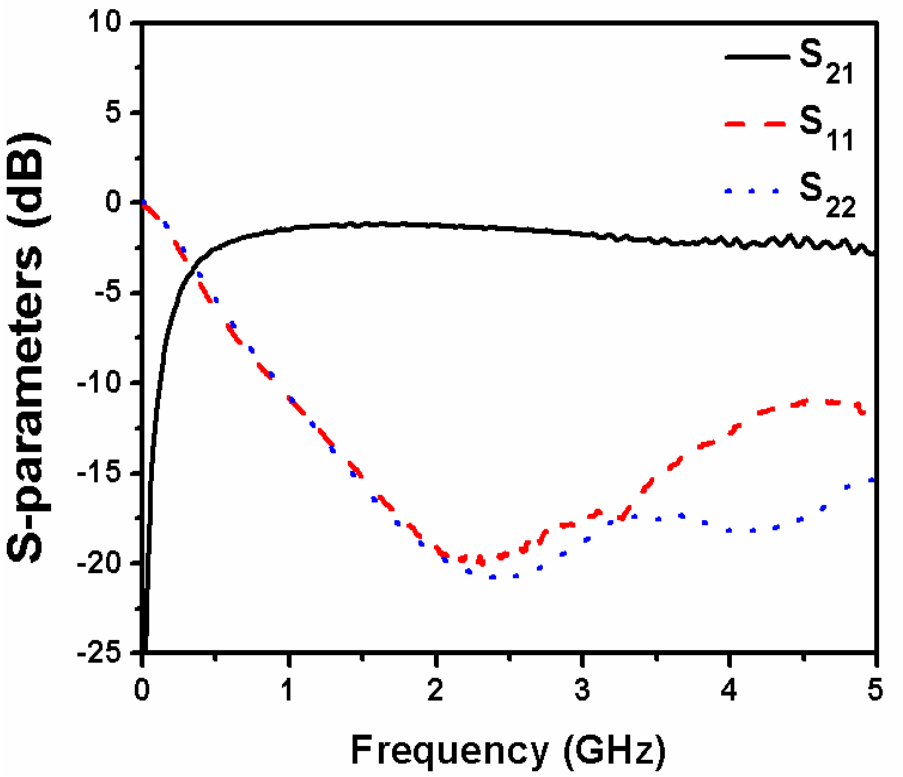


Figure 63. S-parameters of the bluetooth switch

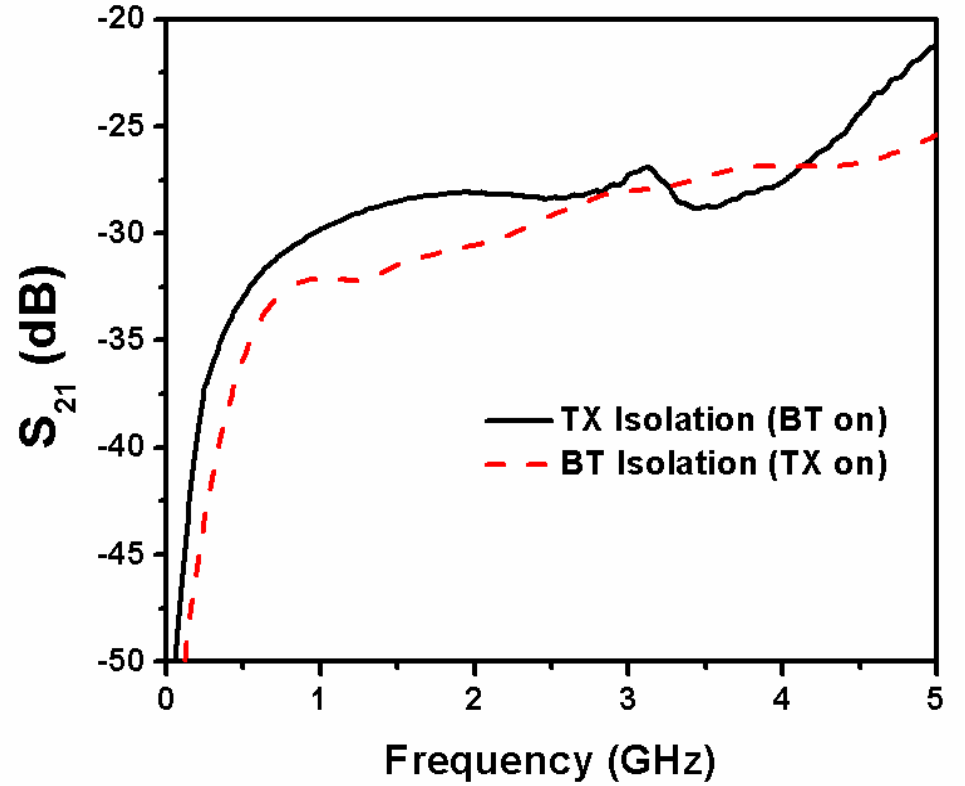


Figure 64. Isolation between transmit and bluetooth throws.

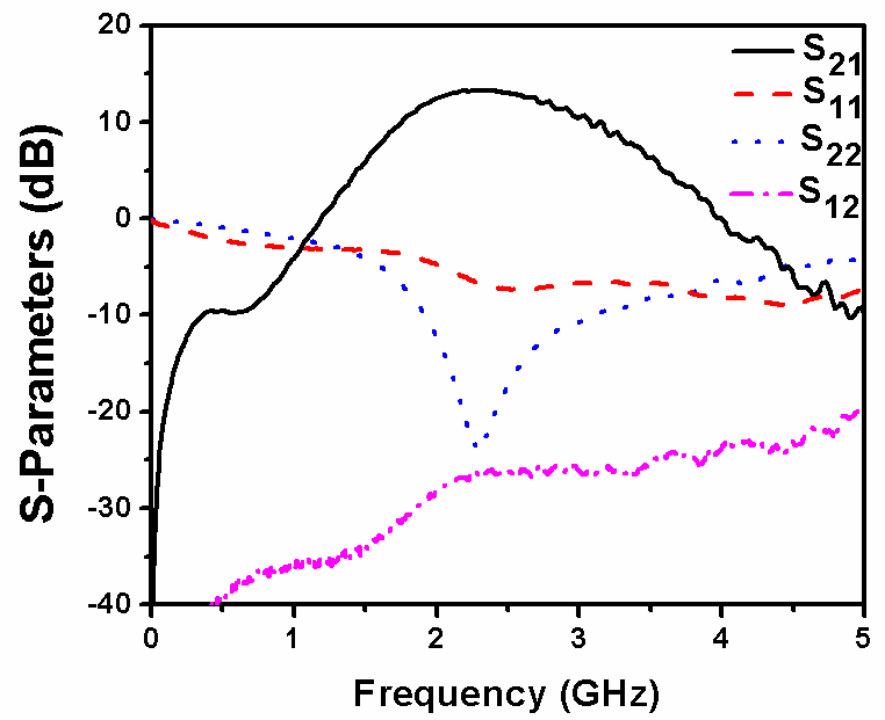


Figure 65. Measured small-signal parameters of the receive path in high gain mode.

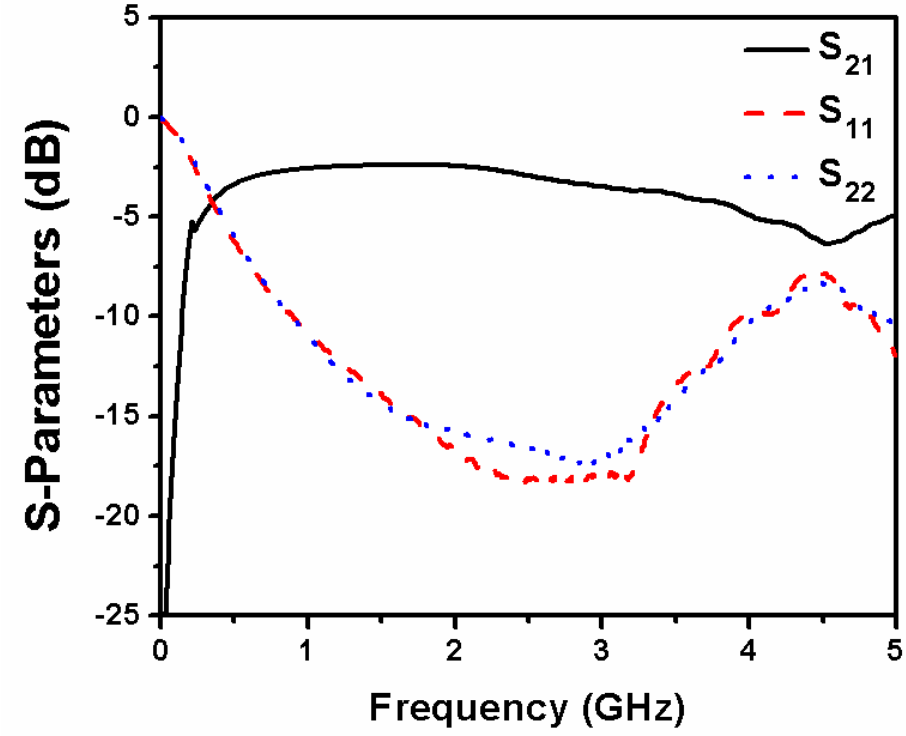


Figure 66. Measured small-signal parameters of the receive path in bypass or low-gain mode.

The measured S-parameters of the LNA are shown in Figure 65. In the high-gain mode, the LNA has a power gain of 13 dB at 2.4 GHz and a good output matching (S_{22} ~ -20 dB). The LNA draws 7.5 mA current from a 3.3 V supply. In the low-gain mode, the measured LNA gain is -2.7 dB (Figure 66), which meets the desired specification. The measured noise figure is plotted vs. frequency in Figure 67. The in-band receive noise figure is 3 dB, which includes the switch loss and the LNA noise figure. The noise figure is also plotted after de-embedding the noise added by the switch FETs. The inductively degenerated cascode LNA has a noise figure of about 1.5 dB between 2.4 GHz and 2.5 GHz.

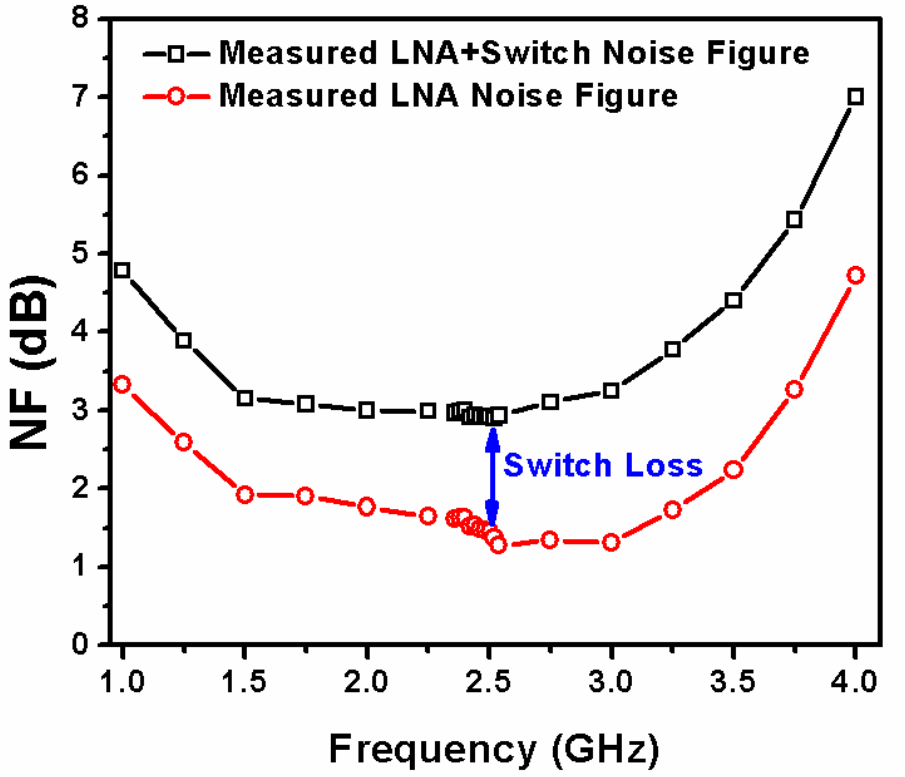


Figure 67. Noise Figure of the full receive path and the LNA. The LNA NF is 1.5 dB at 2.4 GHz.

7.6.2 Large-signal and Harmonics

Figure 68 shows the measured 1-dB compression point of the transmit switch. From the measured data, 33 dBm of linear input power can be transmitted to the antenna through the transmit path. Thus, input power handling greater than 2 W in a standard 0.18 µm CMOS switch has been reported with 1.3 dB insertion loss.

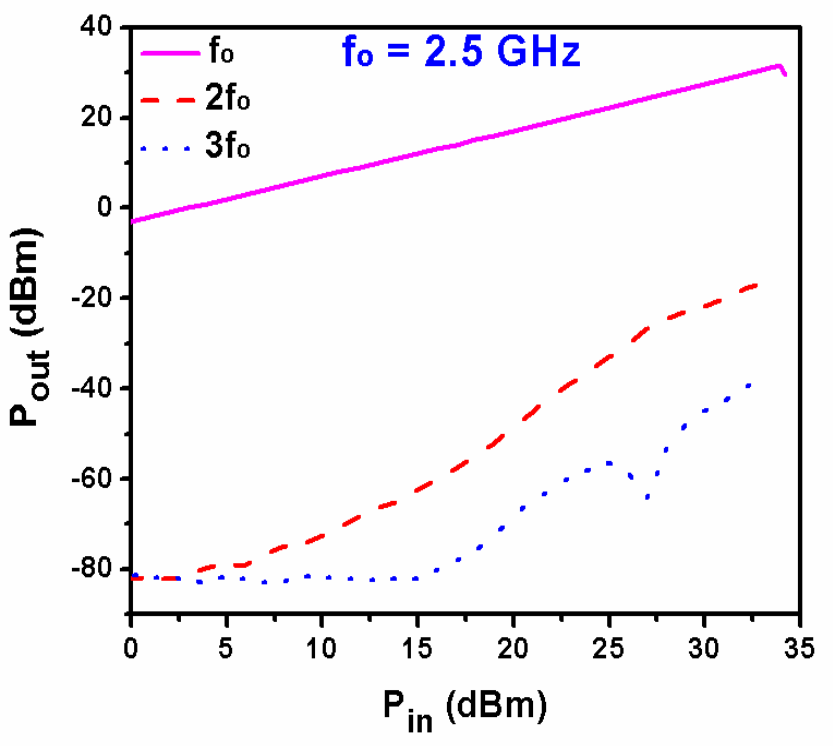


Figure 68. Measured 1-dB compression point and harmonics of the transmit switch

The less stringent requirements of the bluetooth throw allow for 30 dBm (1 W) linear power from the antenna to the bluetooth port, as shown in Figure 69. Second harmonics dominate the harmonic response of both the transmit and bluetooth switches. Figure 70 shows the two-tone measurement on the receive side with a tone-spacing of 1 MHz at a center frequency of 2.5 GHz. At 2.5 GHz, the IIP3 is measured to be 7 dBm. Therefore, the output IP3 of the LNA is 20 dBm. The input 1-dB compression point of the LNA is

measured to be -6 dBm after de-embedding the board loss.

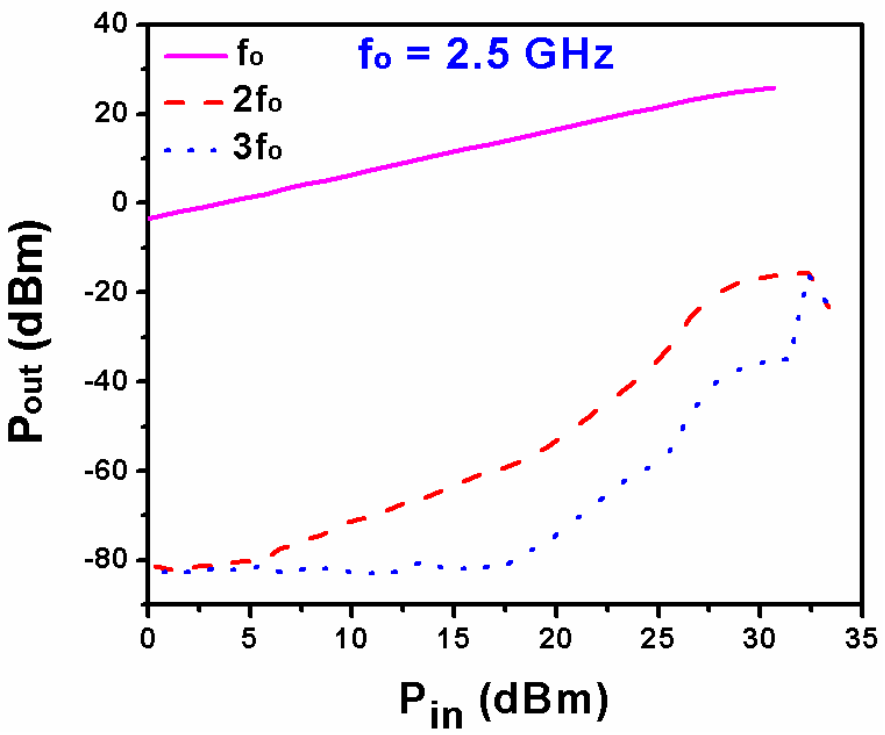


Figure 69. Measured 1-dB compression point and harmonics of the bluetooth switch

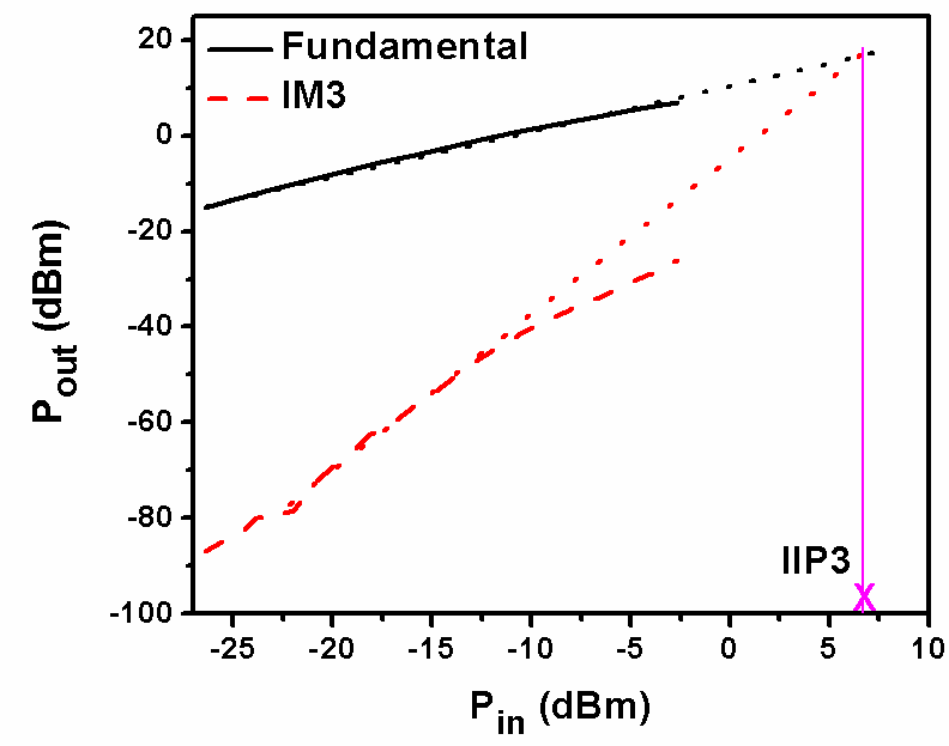
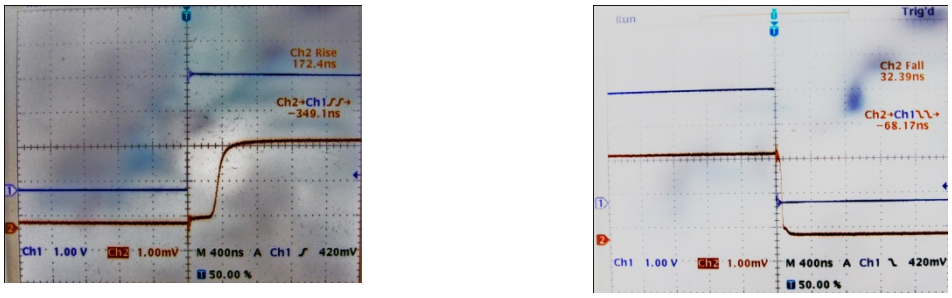


Figure 70. Measured 1-dB compression point and harmonics of the receive switch

7.6.3 Switching Time

The switching times for both transmit and bluetooth throws were measured at 2.5 GHz with an input power of +5 dBm, as shown in Figure 71. The enable pin for the corresponding switch is triggered and the output of the switch is monitored on the scope. The turn-on time includes the delay and rise-times, while the turn-off time includes the delay and fall-times. The turn-on and turn-off times of the switch are dominated by the R-C time constant of the circuit, which is determined by the dc blocking capacitor, gate-isolation resistor and the cross-biasing resistor. The turn-on time is measured to be 350 ns while the turn-off time is about 70 ns.



(a) (b)

Figure 71. (a) Turn-on, and (b) turn-off time measurements for the switch paths at 2.5 GHz with an input power of +5 dBm.

Table III compares the results of this work with state-of-the-art CMOS switches. It is noteworthy that a SP3T switch is expected to have higher insertion loss compared to SPDT, due to the off-state capacitance from the extra throw. The insertion loss of the SP3T switch presented in this work is better or comparable to most of SPDT designs at a

similar technology node. The highest power handling and lowest NF is obtained due to the cross-biasing approach, the body isolation, the transistor stacking, and carefully optimized cascode topology for LNA, respectively. The reported NF for [68, 69] includes mixer and balun loss in the receive chain as well.

TABLE III

SUMMARY OF 2.4 GHZ CMOS SWITCHES

Freq	Switch	Tx IL (dB)	Iso (dB)	Linearity (dBm)	NF (dB)	Switching Time (ns)	Tech (µm)	Ref
2.4 GHz	SP3T	1.3	28	33	3	350	0.18	This work
2.4 GHz	SPDT	1.5	32	28.5	-	-	0.18	[64]
2.4 GHz	SPDT	1.5	24	11	4.5	-	0.18	[69]
2.4 GHz	SPDT	1.1	20.6	20.6	-	-	0.18	[70]
2.4 GHz	SPDT	1.8	15	-	6	-	0.18	[71]
2.4 GHz	SPDT	0.4	30	30	5.5	150	0.09	[68]

7.7 Summary

We have a presented a systematic approach for designing fully-integrated, switch-LNA based front-end ICs for wireless applications in bulk CMOS technology. A detailed analysis of the switch and LNA design and topology tradeoffs has been presented. A cross-biasing approach is combined with the benefits of body isolation technique and transistor stacking to achieve transmit P_{1dB} greater than 33 dBm, while maintaining 1.3 dB insertion loss. The receive switch is cascaded with the LNA architecture which degrades the noise figure by 1.5 dB. The integrated switch-LNA achieves a total noise

figure of 3 dB with moderate quality on-chip matching inductors and *dc* blocking. The fully-integrated 802.11b/g/n solution includes on chip *dc* blocking capacitors, bypass-mode, matching network and hence, does not require any external components. The switch exhibits better than 28 dB isolation between transmit and bluetooth ports.

FUTURE WORK

Fully-integrated RF Front-End Integrated Circuits demand power-amplifier integration on the same module. However, due to decreasing form factor, package dimensions and reduced cost, it is becoming harder to integrate two to three die solutions on the same package. A useful extension of this work would be the integration of CMOS power amplifier along with the switch and LNA on the same chip. This would allow fully-integrated RF front-end solution for WLAN applications.

DC reliability studies on CMOS devices are used to predict the reliability of RF switches. However, during RF switching, CMOS devices are operated under a high voltage swing instead of a constant DC bias. The generation-recombination of the carriers is dependent on the frequency of operation and thus hot carrier lifetime may be a complex function of the frequency of operation. This work presents the first study on reliability of RF switches under RF stress and the mechanism involved. However, a more comprehensive understanding of switch breakdown under RF swing is needed to accurately predict the reliability of RF switches under large-signal.

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He is currently a Senior Design Engineer at Skyworks Solutions, where he is developing high linearity RF front-ends using CMOS technology. From 2010 to 2011, he developed front-end solutions for WLAN applications at SiGe Semiconductor. He was the recipient of IEEE Electron Devices Society Masters Fellowship in 2007. He has also received two Best Student Paper awards at the IEEE Bipolar Circuits and Technology Meeting (BCTM) held in Austin, TX in 2010, and the IEEE International SiGe Technology and Devices Meeting (ISTDM) held in Hsinchu, Taiwan in 2008.