FINAL REPORT

THERMAL MODEL FOR MICROELECTRONIC CHIPS AND PACKAGES

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August 1986

Summary

The Heat Transfer Laboratory in the School of Mechanical Engineering at Georgia Institute of Technology has been actively studying heat transfer from microelectronic components for the past three years. A large portion of that research effort has focused on the problem of measuring the temperature distribution over the surface of an energized microelectronic chip. The work has emphasized an experimental technique consisting of a computer software package coupled with a personal computer, an infrared imaging camera, digitizing equipment, image processing equipment and graphics display hardware. The system has evolved to such a degree that the technique can automatically adjust and accomodate for variations in surface emissivity of the chip, and the hardware/software package ultimately provides the true surface temperature of the chip. It is anticipated that surface temperatures can be measured to within 1°C at an average temperature of 100°C for a spot size of approximately 0.025mm.

The technique of measuring the surface temperature of a chip is a relatively simple one. The complex nature of the problem has been greatly simplified by the software which performs the detailed calculation and the process of surface emissivity mapping. After the surface of the chip has been scanned at a known reference temperature and the digitized signal has been compared to a reference blackbody, the emissivity map of the chip's surface is stored for future reference. Then the chip is energized in its operating environment and the output from the infrared camera is once again digitized. Each pixel of data is then automatically corrected for local emissivity values and the local

spot temperature calculated. The end result is therefore the spatial variation in temperature for the entire chip surface.

This experimental technique should prove to be a valuable tool for the designer of microelectronic circuitry. Local hot-spots can easily be identified and the maximum temperatures can be quantified. If the maximum temperature is considered to adversely affect the performance of the chip, corrective action can be taken. This technique can also be used to assess the changes in thermal performance of the chip as a result of changes in environmental conditions and changes in load on the chip. Areas within the chip that operate above their limiting temperatures can easily be identified. Areas of concentrated or excessive heat dissipation can be identified, and the influence on the local temperature can be assessed. By taking corrective measures, the chip design can be revised to produce one which is less likely to fail during operation.

Introduction

The objective of this proposed study is to model heat transfer from microelectronic devices. The drive towards higher functional density in microelectronic devices has already resulted in printed features on Very Large Scale Integration (VLSI) devices that are shrinking toward submicron dimensions. Further increase in microelectronic device density is currently constrained by the ability of the component to dissipate heat to the surroundings. As a result, the subject of heat transfer from microelectronic devices is vigorously being studied and analyzed by the thermal packaging community in the electronic industry.

The continuous increase in chip density (integration size) and reduction in chip separation distance can inevitably pose a thermal failure of the chip microcomponents if proper thermal analysis and design is not incorporated into the design of the chip and its packaging. The energy dissipated in a semiconductor device is associated with the passage of electrons through the transistor or diode emitter-base junction. From a thermodynamic point of view, transistor switching is an irreversible process, and the energy driving the switching action is eventually dissipated as heat. The energy dissipation generally occurs within 0.04 mm (1.6 mil) of the top surface of the chip. The resultant heat sources are highly localized, and the exact distribution is determined by the internal circuit layout of the chip [1-9].

For reliable operation of electronic systems, the heat dissipation must be accomplished effectively to maintain the junction temperatures below the maximum allowable component temperature of the chip. To obtain

the commonly accepted failure rates of 0.5 to 2.0 percent per thousand hours of operation, the semiconductor elements are generally operated at junction temperatures below 110 - 125°C [1,10]. For electronics systems that are required to operate with especially long operating life or with low maintenance and replacement-cost constraints, it is often desirable to have an average junction temperature as low as 60°C [1]. Usually a minor temperature increase above the maximum allowable component temperatures will result in a sharp decrease in reliability; however a large temperature excursion can produce a "thermal runaway" condition which may lead to thermal failure of the device [1,4,6]. When a semiconductor device is operated at or near its maximum power dissipation limits, the heat generated cannot be effectively dissipated by the accompanying heat sink hardware. As a result, an increase in the junction temperature above the maximum allowable temperature is imminent, and this will cause more current to flow through the junction, even though the voltage and other circuit values are kept constant. This behavior in turn causes the junction temperature to increase even further, producing a corresponding increase in current flow. If this cascading process, referred to as thermal runaway, is not stopped, then the temperature will continue to rise and the device will eventually fail [4,6]. The prevention of catastrophic thermal failure constitutes the primary motivation for the thermal control of semiconductor components. While present heat fluxes from microelectronic chips fall in the range of 2 to 3 W/cm^2, increasingly higher density chip designs of the future will have projected heat flux requirements on the order of 100 W/cm^2[11]. These trends suggest that advanced thermal analysis/design and thermal

control techniques have to be applied to future chip designs in order to provide safe thermal operating limits.

The heat dissipation capability of semiconductor devices to a suitable heat sink (usually atmospheric air) is dependent on the total thermal resistance of the heat flow path. For microelectronic semiconductor systems, the thermal resistance from the component junction to the environment can be classified into three levels: i) the component level, ii) the package level, and iii) the system level [7]. The component level thermal resistance constitutes the resistance of the microelectronic entity that exists between the junctions and the outside surface of the case. The package level resistance consists of the resistance to heat flux from the surface of the case to a suitable reference point (e.g. temperature of air surrounding the component) in the entire system. The system level resistance refers to the heat transfer and fluid flow resistances that exist between the microelectronic packages and the ultimate heat sink which is the environment [7]. This proposed study will mainly be concentrated on the heat transfer from microelectronic chips at the component level.

Background to Proposed Research

The subject of heat transfer from microelectronic chips has been studied since the introduction of the first integrated circuit and numerous papers have been published on the subject. These papers have analyzed the thermal problem from either the component, package or system level. The majority of these papers can be classified into either theoretical or experimental studies, with the exception of a few major

studies which consider a combined theoretical and experimental analysis.

Theoretical:

Bar-Cohen et al. [10], Preston [12], Blodgett [13] and Oktay et al. [14] have summarized the problems associated with the continual miniaturization of microelectronic features, packaging, cooling techniques and other problems involved in the design of microelectronic devices. Bauer [15], Stafford [16] and Katronge and Northover [17] have discussed the application of very high packaging density chip carriers which improve the electrical and thermal performance of microelectronic devices. The advantages of using a chip carrier include its capability for achieving high pin counts for complex circuits and its closely coupled circuits which minimize signal propagation delays.

Adamain [18] and Emerald and Dewey [11] have provided relations to determine the allowable power dissipation levels at a given coolant temperature for simple package geometries. Procedures for determining thermal resistance and selection of heat sink hardwares were given.

For a more detailed analysis of the temperature distribution in microelectronic devices, either an analytical or a numerical approach is necessary. Hein [19] has analyzed the three dimensional, steady-state problem for heat inputs from multiple sources on a substrate. He has considered heat transfer by convection and conduction from the chip.

Gray and Hamilton [20] and Gray [21] have presented a method for analayzing the transient temperature distributions in a silicon substrate using lumped or distributed heaters and sensors as the integrated chip. They have solved the two dimensional, transient conduction equation to provide the temperature distribution on the surface of a chip and they

have neglected heat losses from the chip due to convection and radiation.

Linsted and Surly [22] have solved the three dimensional, steady-state conduction problem for a chip with a constant heat flux source of finite area located at the center of the chip. The bottom surface of the chip was assumed to be isothermal and all the four chip edges and remainder of the nondissipating chip surface were assumed to be adiabatic.

Ellison [23,24] has provided three dimensional, steady-state solutions for chips mounted on composite substrates. He has considered problems with chips mounted on composite media with up to four layers of unequal thickness and different thermal conductivity.

Kokkas [25] has investigated the complete three dimensional, transient problem of heat flow in multilayer structures. He has assumed heat losses due to radiation and convection are negligible. Also, heat losses through wires bonded to the semiconductor chip were neglected.

David [26] has obtained the three dimensional, steady-state temperature distribution for hybrid circuits based on the solution of Laplace's Equation using Fourier techniques. He has assumed conduction to be the dominant heat transfer mechanism, and therefore neglected radiation and convection. Power generation in the hybrid device were assumed to be dissipated uniformly at the surface of a single chip.

Castello and Antognetti [27] and Antognetti [28] have presented the three dimensional, steady-state and transient solutions of a power integrated circuit mounted on a copper substrate. In order to permit the analytical solution of the heat-flow problem, they have simplified the structure of the component by assuming that most of the heat flows

through the portion of the substrate directly below the silicon chip. The heat spreading effects of the high conductivity copper was neglected.

Kadambi and Abuaf [29] have approached the problem by using two dimensional or axisymmetric approximations in their steady-state and transient analysis. They assumed a uniform heat flux over the chip area and convection from the bottom of the copper substrate. Heat spreading effects in the copper substrate were included in their analysis.

Since the interface between the chip and the substrate base is difficult to deal with analytically, many researchers have employed numerical methods in their thermal models. Thermal analyzer software that use finite difference or finite element techniques were utilized by Thompson and Blum [30], Wenthen [31], Boucher [32], Baxter [33], Baxter and Anslow [34], Cook et al. [35], Murtuza [36] and Pound [37] to model the thermal characteristics of semiconductor devices.

Blodgett and Barbour [38], Chu et al. [39] and Oktay and Kammerer [40] have reported an innovative conduction-cooling assembly called the Thermal Conduction Module. The TCM which uses Helium gas encapsulation contains 118 LSI devices mounted on a multilayer ceramic substrate. The thermal characteristics of the TCM at the chip and module levels were analyzed using numerical simulations.

Experimental:

McLaughlin and Fitzroy [41] summarized the various techniques for experimental measurements of temperature in integrated circuits. Because of the small dimension of microelectronic devices, noncontacting measurement methods must be used to avoid distorting the temperature field. In the defense industry, the testing procedures for the

determination of thermal characteristics of microelectronic devices in military equipment are in accordance with the guidelines given in MIL-STD-883C Method 1012.1 [42].

Goel and Gray [43] and Choudhury [44] reported on the use of liquid crystals for measuring temperatures of microelectronic devices. Liquid crystals react to changes in temperature by changing color, which provides a visual method for non-destructive testing and evaluation.

Sanders [45], Maher [46], Boulton and Siegal [47] and Boulton [48] have summarized the role of thermography in the design, development, production and in-use evaluation of microelectronic devices and assemblies. Infrared imaging systems are used to detect, isolate and quantify extreme temperature differences which usually indicate a defect in the component.

Martin [49], Weight [50], Egan [51] and Boulton [52] have reported the use of thermal imaging to detect temperature anomalies on PC Boards. Kallis et al. [53], and Boulton [54] have discussed the application of thermography for testing hybrid circuits. At the single component level, Yu [55] and Lidback [56] have presented temperature measurements of the surface of a chip using an infrared imaging technique. They have eliminated the difficulty of compensating for emissivities by coating the chip surface with a black velvet coating which has an emissivity close to unity.

Wickersheim [57] has presented a new thermometry technique for measuring component temperature of microelectronic devices. Flouroptic thermometry utilized a small contact sensor constructed from insulating material which provides complete electrical isolation and minimal thermal

perturbation. Temperature measurements using Flouroptic thermometry is based on the isolation and measurement of the relative intensities of two flourescent emission lines which originated from an europium activated phosphor when illuminated by UV radiation.

In a combined theoretical and experimental analysis, Coats [58] numerically modeled the microelectronic device using a thermal analyzer program. Experimentally, he measured the substrate temperature using diode chips eutectically bonded to the surface of the substrate.

Sergent and Schuyler [59] described a numerical solution technique to predict the approximate temperature rise in hybrid microcircuits. Temperature measurements were made using an infrared microscope. They included emissivity corrections but primarily compare only temperatures of areas with equal emissivities.

A major study involving theoretical and experimental analysis was reported by Baxter [60,62], Baxter and Brouillette [61] and Anslow et al. [63]. These reports described the thermal characteristics and measurement techniques for microelectronic chips and packages. Computer simulations, infrared radiance measurements and electrical temperature sensitive parameters measurements were used to study the thermal characteristics of a thermal test chip. The problem of emissivity corrections for infrared radiation measurements and the use of various chip coatings to eliminate the chip translucence problem were discussed.

Proposed Research

The purpose of this research project is to develop a thermal model of a microelectronic semiconductor device at the component level. The

thermal model will be capable of predicting the transient, local temperatures over the entire surface of an energized chip. The proposed project can be broken into two distinct tasks:

1. Theoretical Model of the Heat Transfer from a Microelectronic Chip. The theoretical approach will result in a computer program capable of predicting the temperature distribution within a microelectronic package as a function of package design, power consumption of the chip, mounting techniques and materials used in the construction of the package.

2. Experimental Measurement of the Temperature Distribution Across the Surface of Microelectronic Chips. The bulk of the experimental measurement will be made with an infrared camera system used in conjunction with a digital video processor and a microcomputer for data acquisition and storage.

The experimentally measured temperature data will be used to verify the results of the computer-predicted temperature distribution.

Theoretical Model

Preliminary work on the thermal model has produced a conservative one-dimensional model of a microelectronic chip encased in a dual-in-line package (DIP). This transient one dimensional model was developed using an explicit finite difference formulation based on a typical DIP geometry configuration given in Figure 1.

The model assumes that the semiconductor chip is at a uniform temperature. The one dimensional assumption restricts the heat transfer

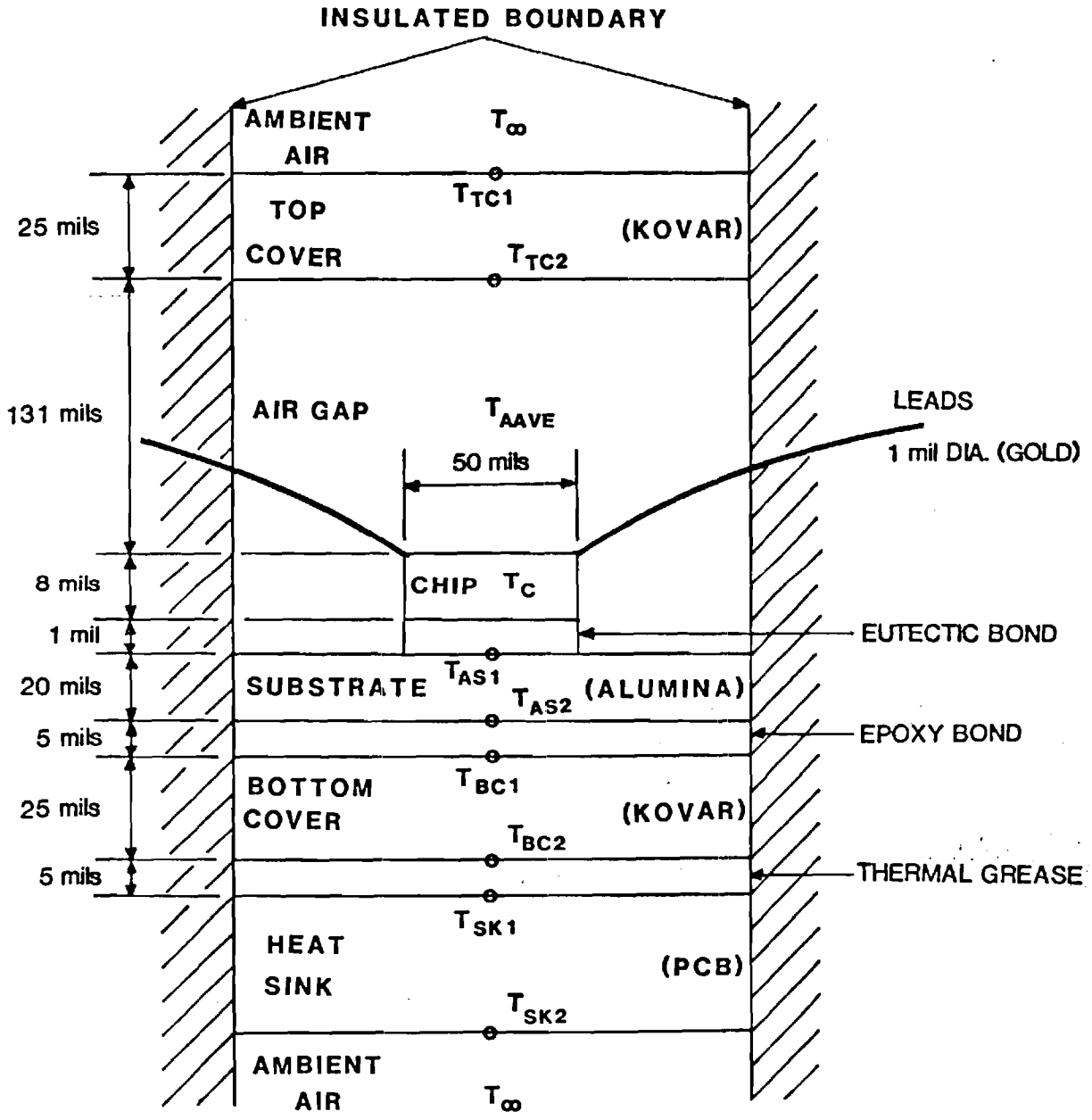


FIG. 1 ONE DIMENSIONAL DIP PROFILE

(NOT TO SCALE)

in the vertical direction only. The assumption of insulated sides will give a rather conservative preliminary approximation. Heat is assumed to be generated uniformly throughout the chip and it is dissipated through combinations of series-parallel thermal resistances to the outer surface of the package. A portion of the heat is conducted in series through the eutectic bond, ceramic substrate, epoxy bond and the cover material before reaching the outer surface of the bottom cover. Heat is also conducted from the chip through the lead wires. The remaining heat is dissipated by conduction (due to the small spacing of the air gap, convective cells cannot develop) and radiation in parallel through the air gap and then by conduction through the cover material to the outer surface of the top cover. At the outer surface of the top cover, heat is assumed to be transferred to the ambient surrounding by free convection and radiation. Heat removal from the outer surface of the bottom cover is more complicated, because it is dependent on the mounting configuration of the DIP onto the PCB and the heat sink configuration assumed in the model.

Preliminary results have been obtained using the 1-D transient model for various initial conditions, heat sink boundary conditions and dissipation rates. Figure 2 shows the temperature-time plot of the DIP for the following conditions: convective heat sink PCB [1,7,8], temperature dependent properties [64,65], adjustable time steps, initial temperature of 25°C, and a dissipation rate of 6.2 W/cm^2 in the chip.

The one dimensional thermal model is capable of providing a conservative approximation of the temperature distribution in a microelectronic package. However, preliminary infrared temperature

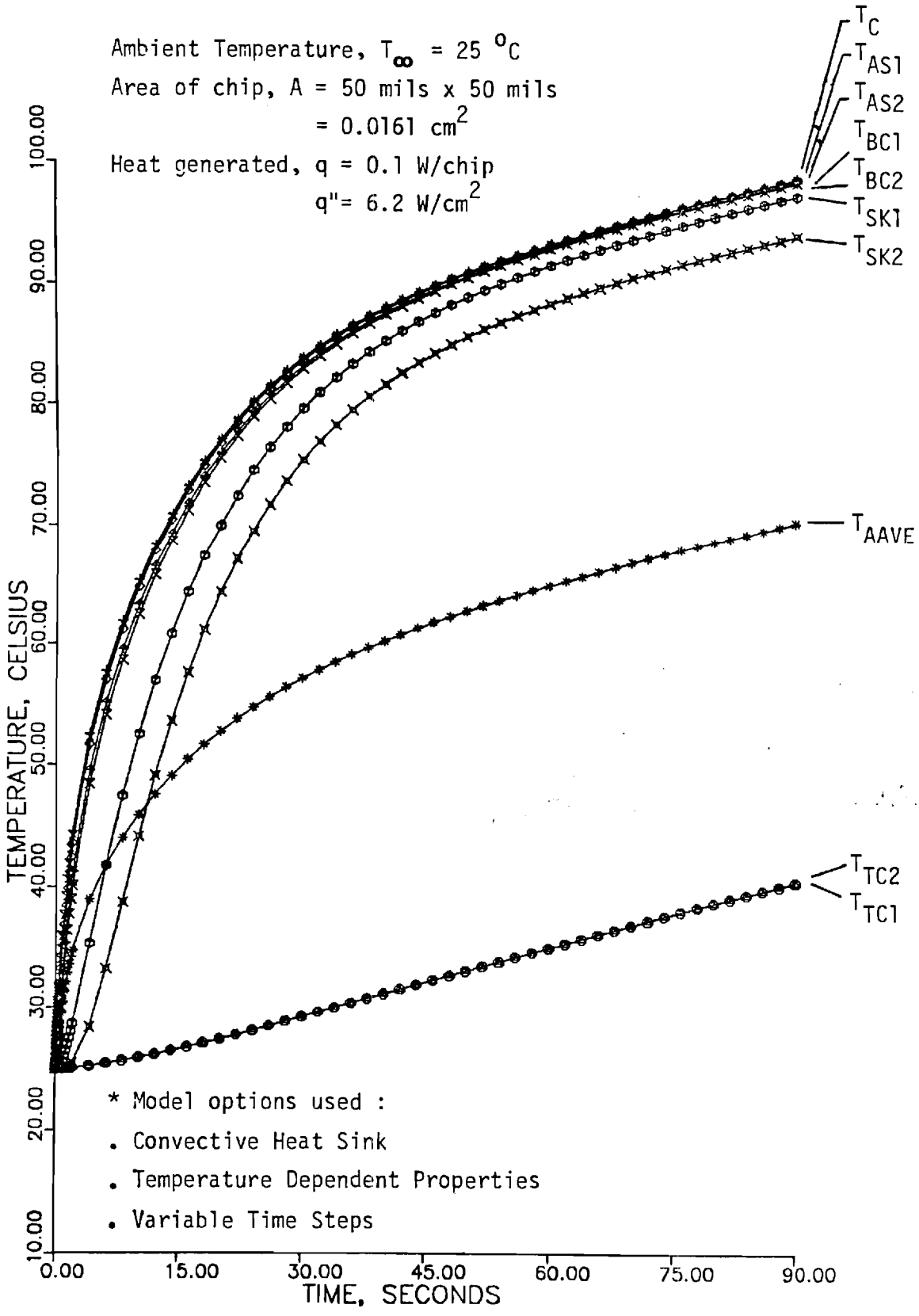


FIG. 2 TEMPERATURE DISTRIBUTIONS IN A DIP

measurements of a thermal test die provided by GTE indicates that local temperature variations exist across the surface of the chip. Thus, the assumption of uniform chip temperature in the one dimensional thermal model is inadequate for predicting localized hot spot temperatures. A three-dimensional model will be required to provide detailed information on the location and magnitude of hot spot temperatures on the surface of the chip. Instead of facing the substantial task of writing a general thermal model program, it was decided that time will be more efficiently utilized by adapting a commercially available software package for predicting the transient, three-dimensional temperature distribution in a microelectronic package. After a review of the available thermal model programs, MITAS-II [66] was selected for use in the theoretical modeling of the chip package. A portion of the proposed work will involve adapting MITAS-II to the task of predicting the transient, three dimensional temperature distribution in a microelectronic package.

MITAS-II has been used to solve several heat transfer problems with known analytical solutions. These initial applications serve to check the accuracy and applicability of MITAS-II. Initially, the temperature distribution for a steady-state classical fin with constant cross-sectional area was solved for the following cases: (i) convection from surface and end of fin; (ii) convection from surface of fin with insulated ends; and (iii) convection and radiation from surface of fin with insulated ends. The MITAS-II simulation results for all three cases agree identically with the analytical solutions (case (i) & (ii) [67], case (iii) [68]).

To further the understanding of MITAS-II's capability, the program

was applied to more complicated problems that resemble the heat transfer from a microelectronic chip and package. A one-dimensional model of a heater with internal generation (resembling heat dissipation in a chip) was selected and cases with increasing complexity were solved. The cases examined were as follows: (i) steady-state, constant properties (k=constant); (ii) steady-state, temperature dependent properties (k=k(T)); (iii) transient, constant properties (k=constant); and (iv) transient, temperature dependent properties (k=k(T)). The MITAS-II simulation results for cases (i), (ii), and (iii) agree identically with the analytical solutions [69] for the temperature distribution in the heater. For case (iv), a closed-form analytical solution is not available for comparison, however, transient simulation results for large time periods agree exactly with the steady-state analytical results of case (ii). A comparison of the MITAS-II simulation results with the analytical solution for case (iii) is shown in Figure 3.

Currently, a search is being conducted on the availability of a suitable thermal test chip that can duplicate the heat dissipation in a chip with a realistic design. Once the thermal test chip is obtained, MITAS-II will be adapted to model the heat transfer from the chip.

Experimental Measurements

The proposed experimental research involves measuring the temperature distribution on the surface of microelectronic chips. The equipment required for data collection centers around an infrared imaging radiometer that produces a thermograph video output, a digital video processor that digitizes the video output, and a microcomputer that controls the data acquisition process and provides data storage. A

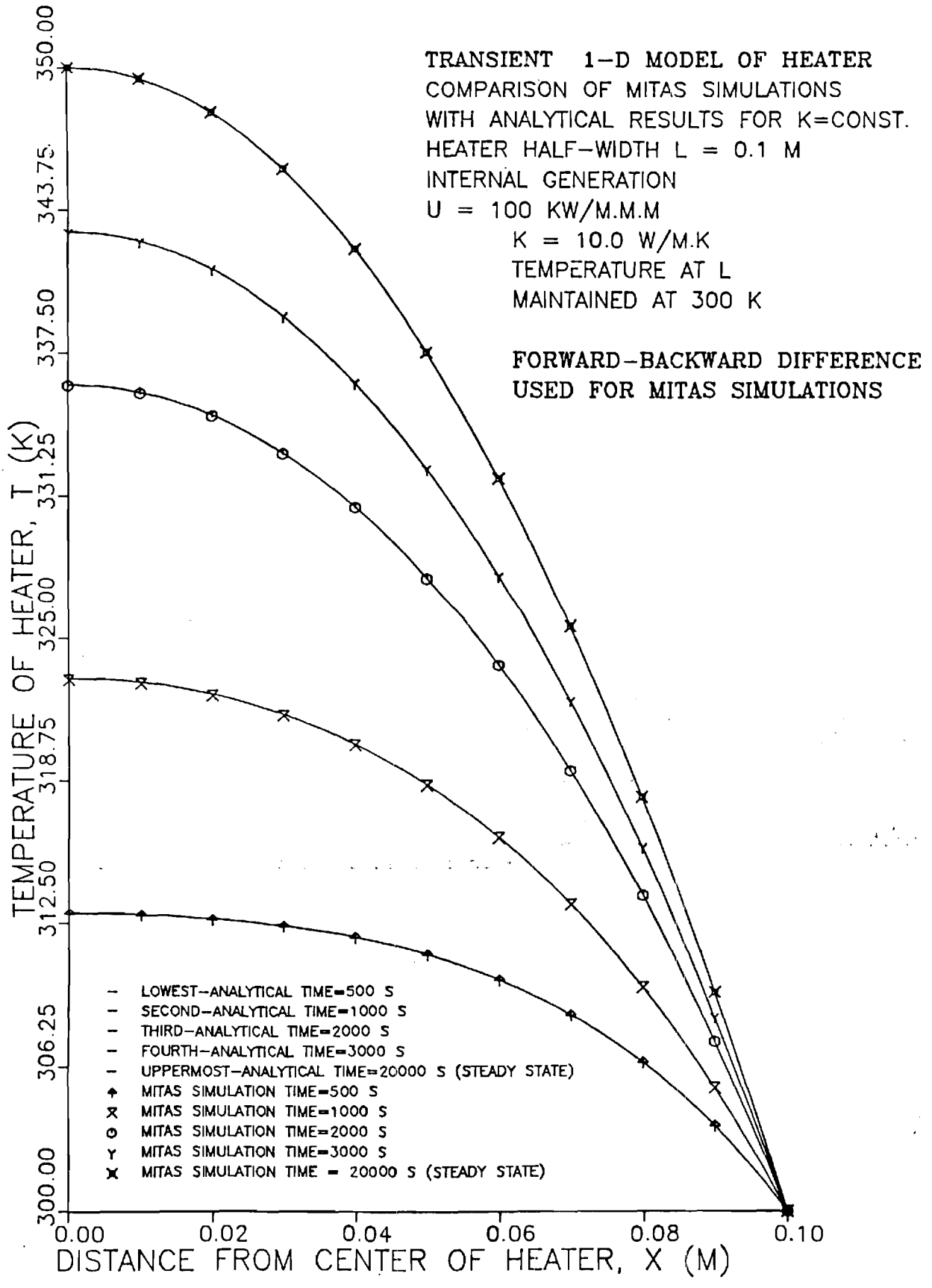


Figure 3. MITAS(FWDBCK)/ANALYTICAL RESULTS FOR K=CONST.

microcomputer specifically equipped for image processing is used to transform the test data to spatially match the master frame emissivity map. Either a main-frame computer or a microcomputer equipped with a Math Coprocessor can be used to process the spatially aligned data into a temperature distribution for the surface of the chip, which can then be displayed using Enhanced Graphics hardware.

Infrared Measurements

The infrared camera system, manufactured by Inframetrics, [70] produces a TV compatible video output signal of the thermal patterns radiated by a target. The scanner senses the infrared radiation emitted by the target using a liquid Nitrogen cooled Mercury-Cadmium-Telluride detector. The signal from the scanner is processed by the Control/Electronics unit into a video output which is proportional to the local radiant energy of the target. The black-and-white video output that is displayed on a TV monitor permits qualitative and quantitative data analysis by interpretation of gray tones or isotherm scale readings. In addition, a pseudo-color presentation of the video output can be generated by processing the output signal from the Control/Electronics unit with an Iso/Line Scan Colorizer. The resultant quantized color image representing different temperature ranges is obtained by superimposing eight discrete colors onto the black-and-white imagery.

The infrared camera is ideal for qualitative temperature detections. "Hot spots" within the target area can readily be detected. However, in order to determine a numerical temperature value for a region of interest, an involved manipulation and calibration of the equipment is required. The quantitative analysis is complicated by the non-blackbody

characteristics of the surfaces of microelectronic chips. The complexity of the temperature determination is compounded by the unknown emissivities of the materials which are distributed in micro proportions depending on the internal circuit layout of the chip.

The emissivity of a surface can be obtained using the following relation:

$$e_t = (\Delta I_{tr} - I_{ba}) / (I_t - I_{ba})$$

where

I_t = Absolute Isotherm Units of the target at T_e;

ΔI_{tr} = Difference in Isotherm Units between target and reference at T_e;

I_{ba} = Absolute Isotherm Units of the background;

e_t = emissivity of the target;

T_e = temperature of target
(target heated to a known temperature for emissivity mapping).

Once emissivity is known, the following relation is used to correct for emissivity and account for reflection from the background in an actual test.

$$I_t = (\Delta I_{tr} / e_t) + (1 - 1 / e_t) I_{ba}$$

After correction for emissivity, the Absolute Isotherm Units can be used to obtain temperature from the calibration curves (graphical method) or by substituting into polynomial functions expressing temperature as a function of Isotherm Units:

$$T = C31 + C32\ I + C33\ I^2 + C34\ I^3 + C35\ I^4$$

where

C3n's = calibration constant for infrared camera.

Preliminary measurements using the infrared camera system have been carried out for two types of chip packages. The first is an actual production chip consisting of a Motorola 6801 chip mounted in a 40-pin dual-in-line package (DIP). The other type of package examined consists of a Motorola Thermal Test die mounted in a leadless ceramic chip carrier (C^3) package. These 16-lead Thermal Test chip packages, provided by GTE Packaging Technology Center, consist of two heater implants that duplicate the heat dissipation in an actual chip. Prior to measuring the chip temperature with the infrared equipment, temperature-resistance measurements of the chip were made for both type of packages. The temperature-resistance calibrations will provide an approximate check of the results obtained from the infrared radiation measurements.

Only the outer surface of the Motorola 6801 chip package can be analyzed using the infrared camera because the chip itself is encapsulated within the DIP. Since the outer surface of the package consists of a single material, the temperature distribution can readily be evaluated once the emissivity of the surface is known. The Thermal Test die, on the other hand, is sealed within the chip carrier package with a glass window. Since glass is opaque to infrared radiation, the video output obtained from the infrared camera when focused on the leadless chip carrier package was due to radiation emitted from the heated glass. After the glass window was removed to expose the chip, slight variations in temperature were observed when the chip area was scanned with the normal lens. However, when the chip was scanned with a 3X telescope coupled to a microscopic objective, the magnified image

revealed an "apparent" temperature variation on the surface of the chip. The terminology of an "apparent" temperature is used to denote results that have not been corrected for emissivity. Variations in the apparent temperature can be attributed to either actual temperature differences on the surface or they can arise from emissivity differences due to the different materials on the surface. The metallized regions are observed to produce lower apparent temperatures on the chip due to their high reflective properties (low emissivity). Figure 4 is a magnified video output showing the variation in surface apparent temperatures that exist on the Thermal Test die. The actual temperature distribution can be evaluated once the emissivities of the microstructures on the chip surface are known.

Digitizing and Graphics Display

The Isotherm Units calibration curve of the infrared camera can be used to determine the emissivity and ultimately the temperature. However, since the video image produced by the infrared camera indicates complex thermal patterns across the surface of the chip, the temperature at every pixel of the video image must be determined. Since the number of pixels for each frame of video image is very large, a computer is ideal for carrying out the necessary computations. Thus, the video output from the infrared equipment must be stored and made accessible to a computer which will perform the computations and provide the temperature results. The video output signal from the infrared camera can be read to and stored in the memory of the digital video processor at 512x512 addressable pixels per frame of video. The analog signal at each pixel location is digitized and assigned an integer number ranging from 0

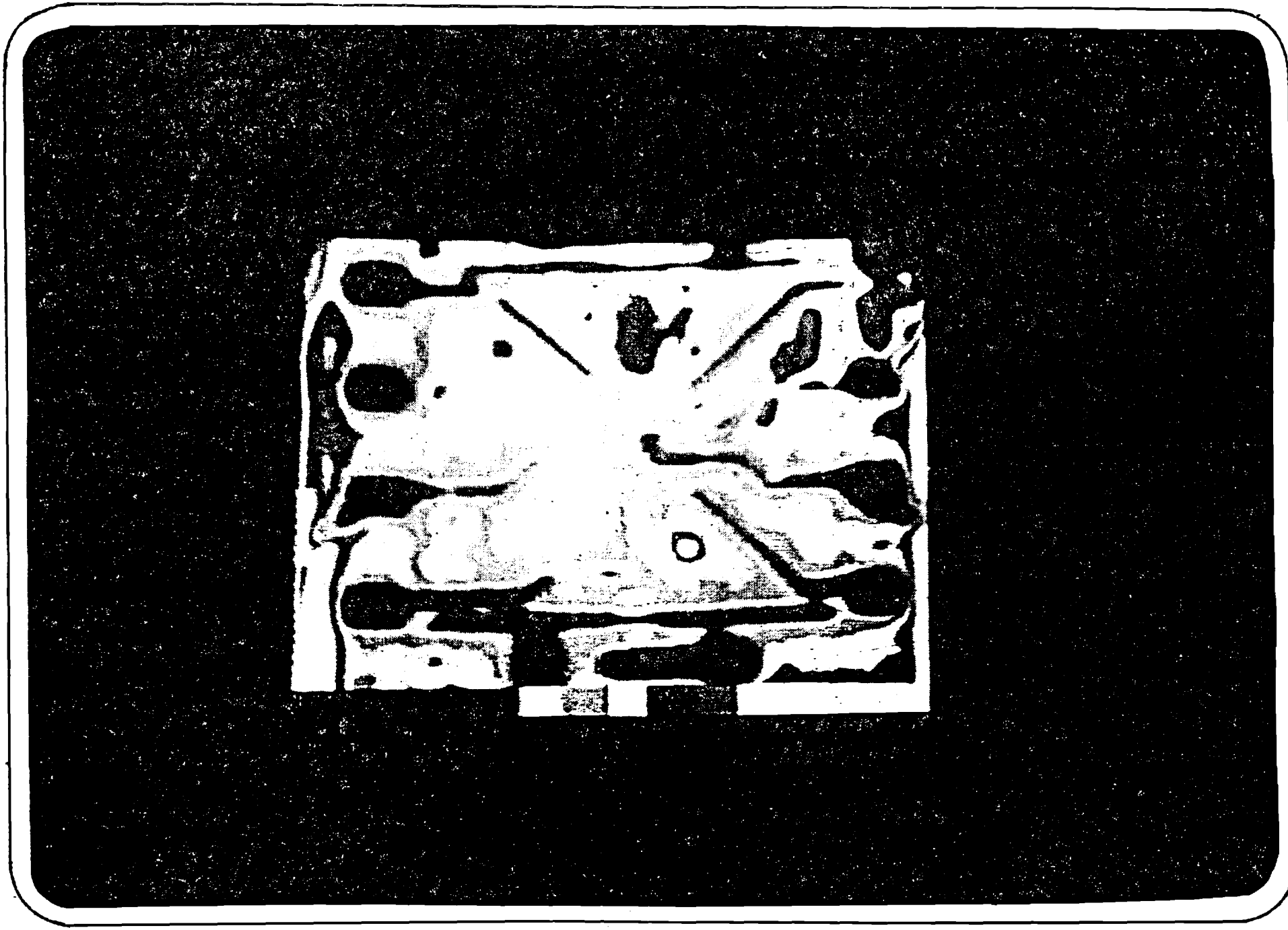


Figure 4. Video Output from the Infrared Camera showing the Apparent Temperature Distribution Across the Surface of a Thermal Test Chip.

to 255, depending on the intensity level (0-black, 255-white).

The digitized signal can then be transferred from the digital video processor's memory to a PC and ultimately stored on floppy diskettes. Since the PC has limited memory capacity and low computational speed, the large number of digital video data can be more efficiently processed using a mainframe computer. A communication software package has been used to transfer files between the PC and the host computer. Figure 5 is a three dimensional plot of the infrared radiation intensity distribution on the surface of a Thermal Test chip. The original 512x512 digital video data have been reduced and averaged to produce the 100x100 "reduced" data used to generate the plot in Figure 5.

Using a personal computer equipped with the Enhanced Graphics Adapter and Monitor, the "processed" data can be displayed in high resolution graphics (640x350 pixels) using 16-color isotherm bands as shown in Figure 6 for the thermal test die. This capability permits the reconstruction of the "processed" data into a video image for comparison with the video output of the infrared camera. A reconstructed video image displayed using the same 8-color output by the infrared camera system is shown in Figure 7 for the thermal test die. Figure 8 and 9 are pictures of an actual chip used in the thermography experiment. A computer reconstructed video image of the energized chip is shown in Figure 10.

Emissivity Corrections

Due to the complex distribution of materials on the chip surface and the large number of pixels per video image, it would be impractical to identify the material, determine its emissivity and then input

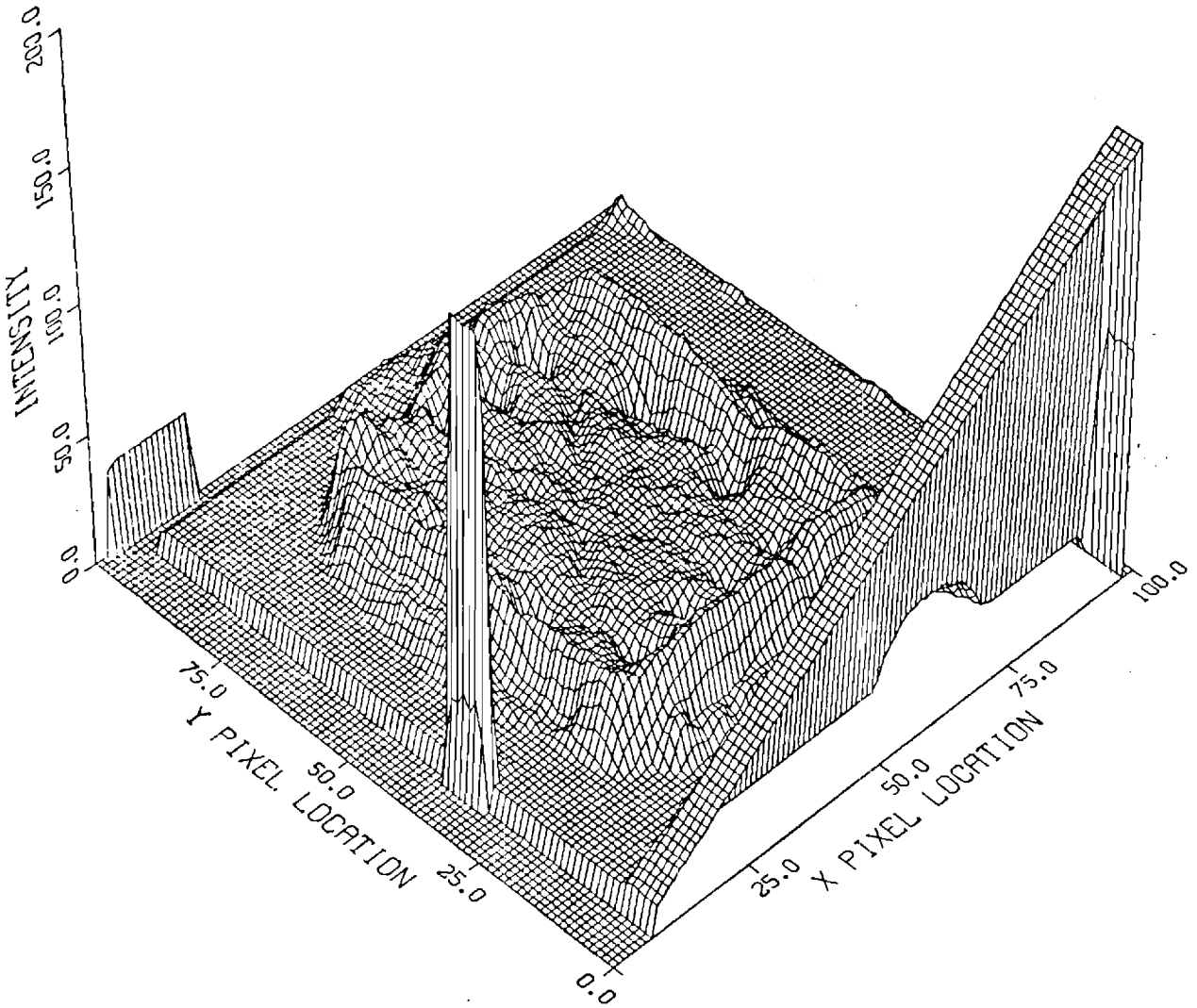


Figure 5. Infrared Intensity Level of a Thermal Test Chip.

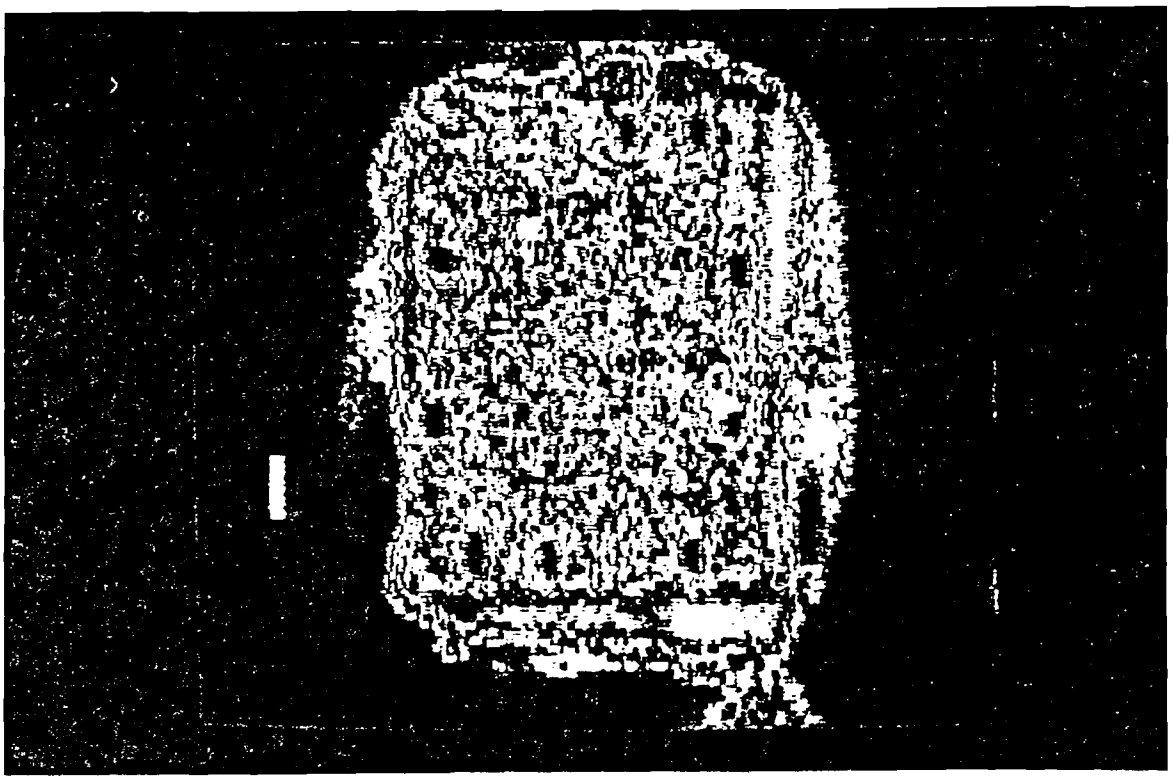


Figure 6. Computer Constructed Thermograph of a Thermal Test Chip in High Resolution (640 x 350 pixels) in 16 Colors Contour.

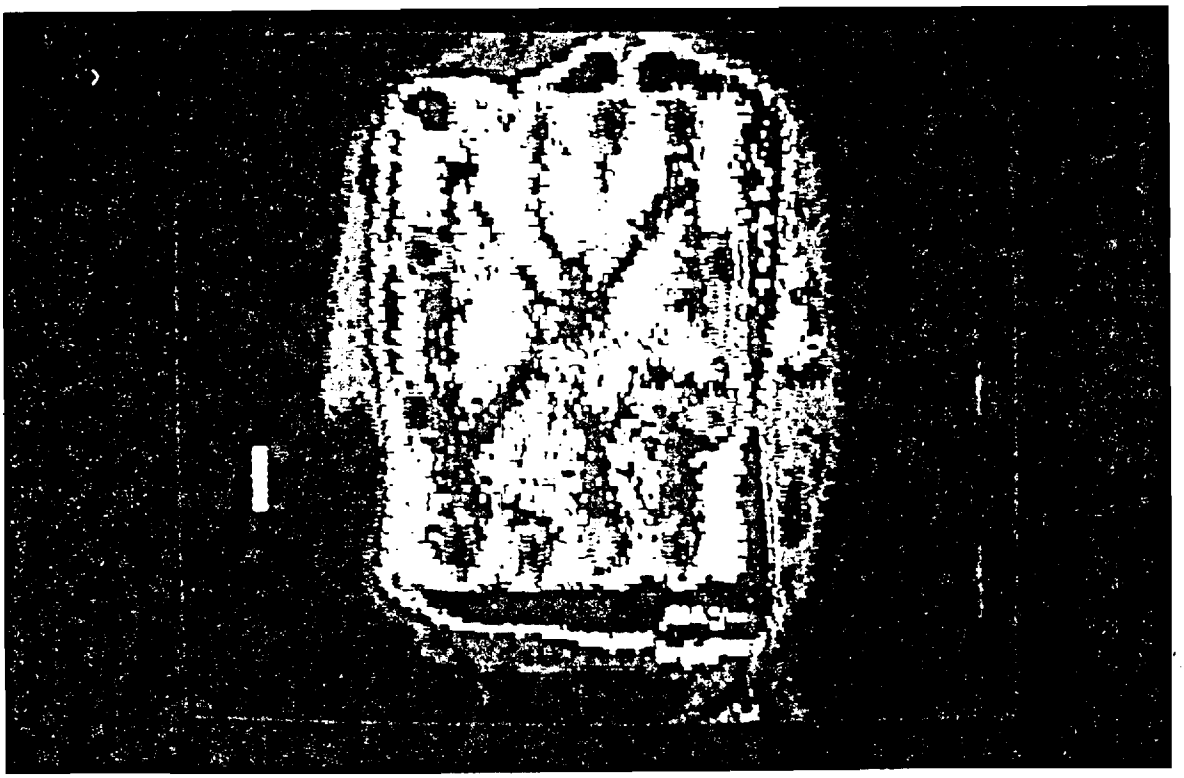


Figure 7. Computer Constructed Video Image of a Thermal Test Chip Displayed Using High Resolution Enhanced Graphics, with 8 Colors Contour (Duplicate IR Camera Output).

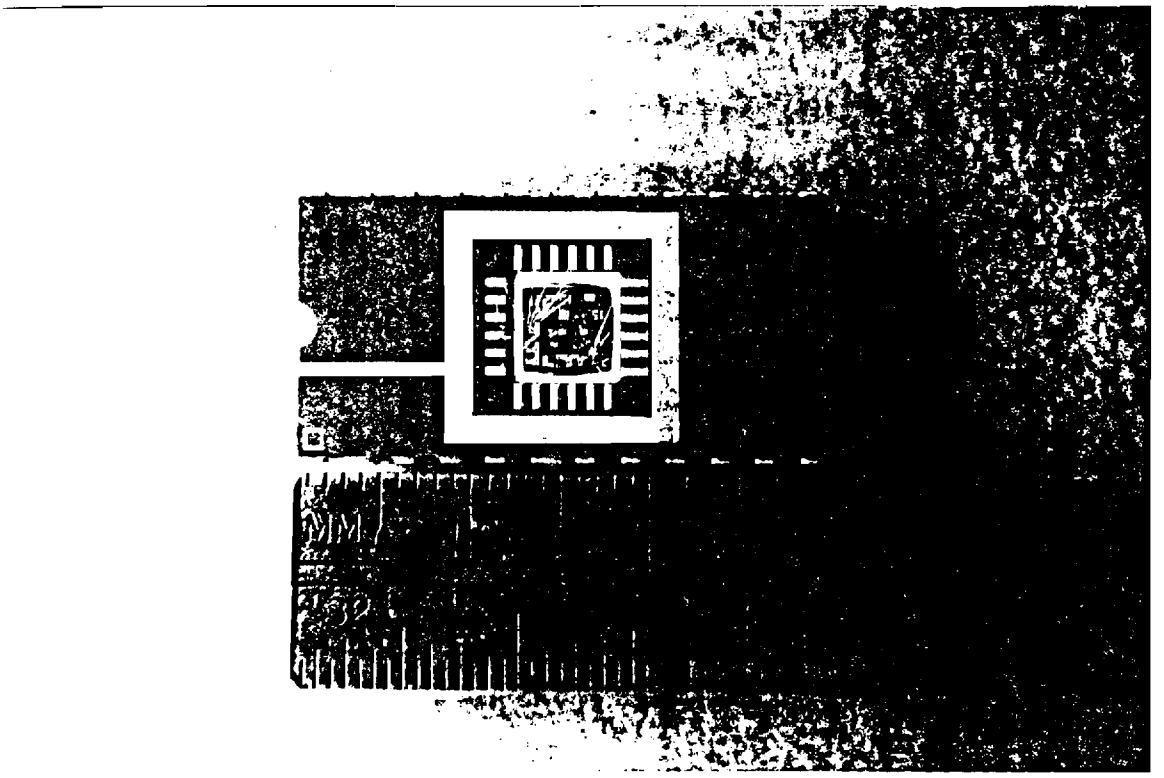
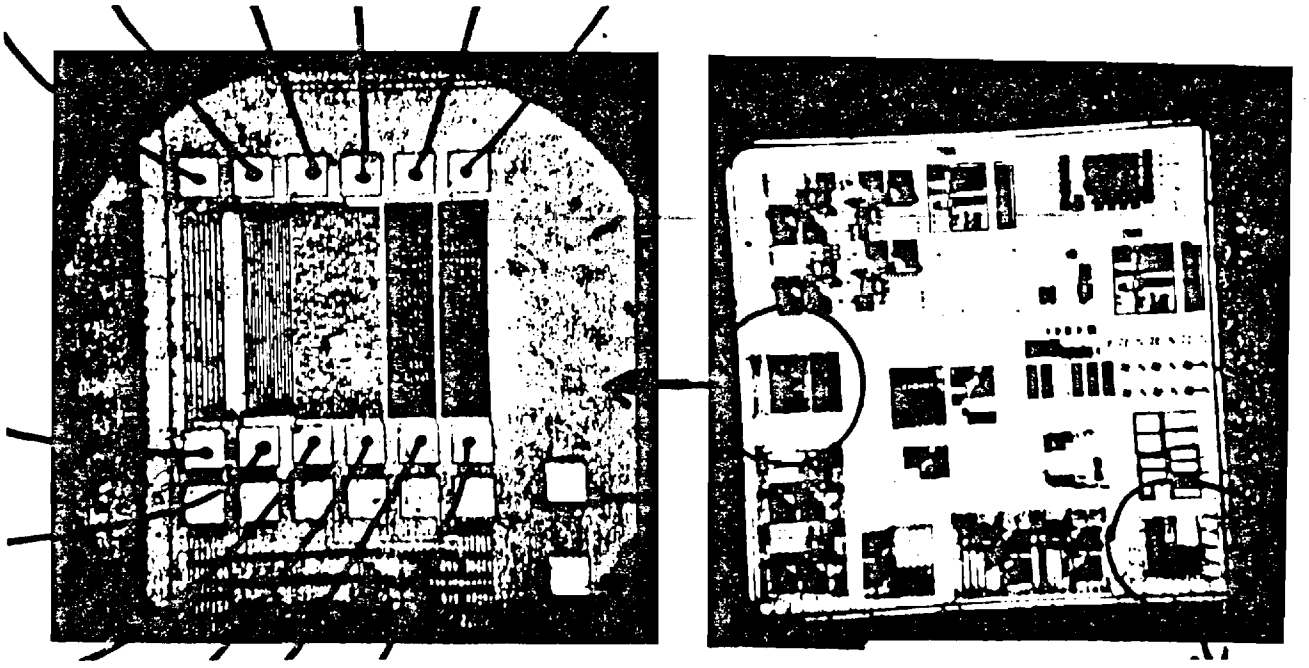


Figure 8. An Actual Chip Used in the Thermography Experiment.



(a) (b)

Figure 9. Detail of Microcomponents on the Actual Chip (4.8 mm x 4.8 mm).
(a) Enlarged Portion of the Actual Chip that was Energized;
(b) Entire Chip.

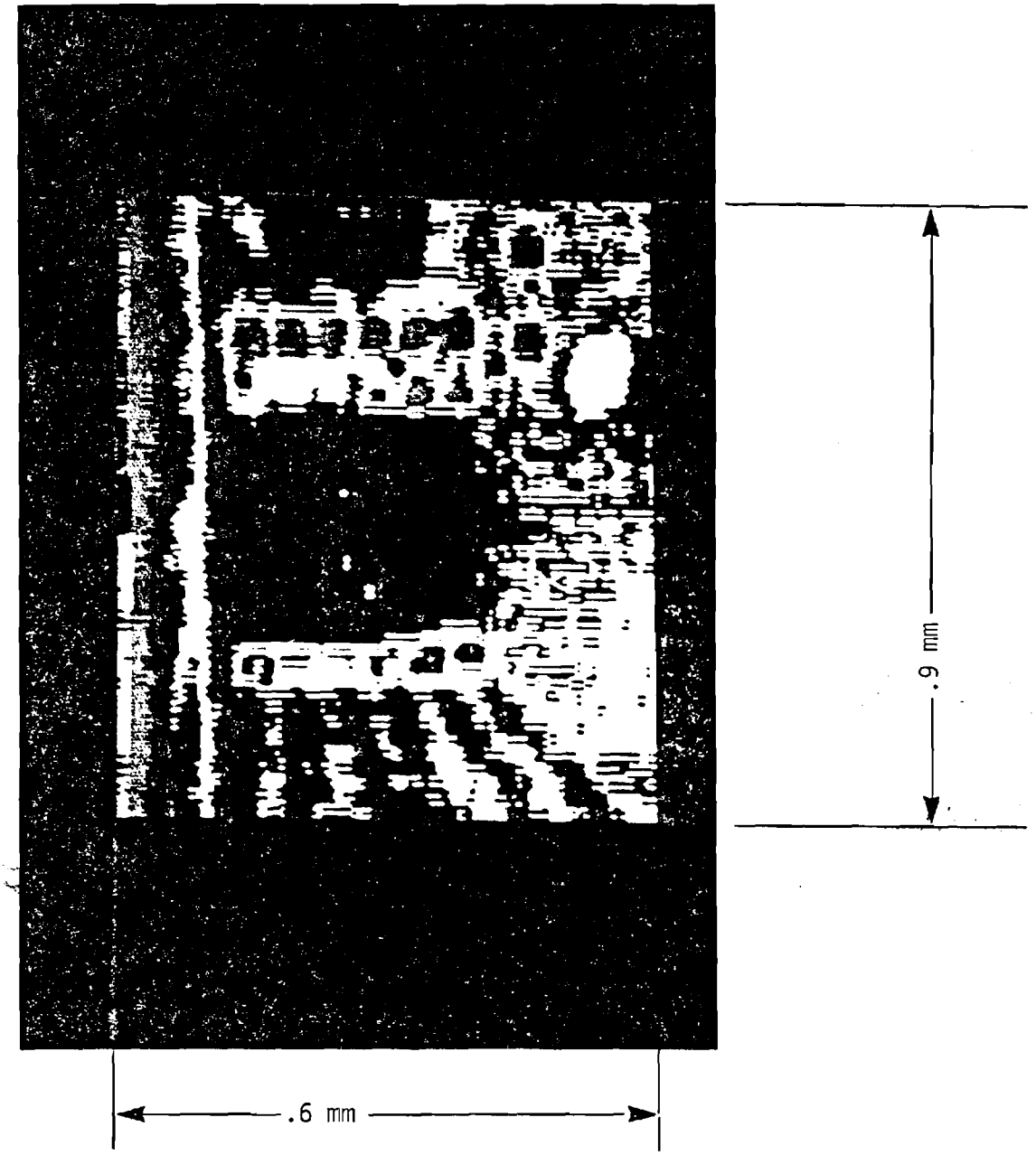


Figure 10. Computer Constructed Thermograph of the Enlarged Portion of the Actual Chip (Figure 6a). The Magenta Rectangular Area Represents the Energized Resistor on the Chip.

emissivity values for temperature calculations at all the pixel locations. An emissivity "mapping" process is proposed for the determination of emissivities at every pixel location of the video image. An isothermal cavity will be used to heat the chip to a constant known temperature. The radiation intensity of the chip surface will be compared to the radiation intensity of a blackbody source set at the same temperature of the chip. This information will be digitized and made accessible to a computer for the emissivity computation at every pixel location of the video image. Thus an emissivity map can be created for any chip and the respective pixel emissivity value can be retrived to evaluate temperature in subsequent actual power-up testing of the same chip. However, due to the small spatial dimensions of microelectronic devices, it is impractical to align physically the image of a test frame with that of a previously stored emissivity master frame. Image processing hardware and software by Earth Resources Data Analysis System (ERDAS) will be used to geometrically transform the spatial locations of the test frame and align it with that of the master frame prior to temperature computation.

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GEORGIA TECH 1885-1985

DESIGNING TOMORROW TODAY

THE GEORGE W. WOODRUFF SCHOOL OF
MECHANICAL ENGINEERING

August 8, 1986

Dr. John C. Gustafson
Department Manager
Physical Electronics Tech Center
GTE Laboratories, Inc.
40 Sylvan Road
Waltham, MASS 02254

Dear Dr. Gustafson:

Geow Heng has made excellent progress on his thesis since the beginning of the year. He has advanced to the stage where he can now scan the surface of the chip or chip package with the infrared camera and process the data through a digitizer and PC to map the local surface temperature. He has also developed a technique that allows him to locally correct for the variations in the emissivity of the chip or package. The emissivity correction scheme utilizes an image processing software package that was originally developed for enhancing earth satellite photographs. The entire technnique is a unique one which will permit local temperature measurements on a spot size as small as 0.025 mm to within 1 °C.

I have enclosed a summary report of Geow's accomplishments to date. This document will serve as a final report of work that GTE sponsored in the School of Mechanical Engineering through December 1985.

We would like to thank you for your financial support of the micro-electronic packaging project. We would not have been able to make any of this progress without your help. We will mail you a copy of Mr. Heng's Ph.D thesis when he completes it sometime next year.

If you have any comments or questions about the enclosed report, please feel free to call me.

Sincerely,

William Z. Black

WZB:rh
Enclosure

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