High-Speed SiGe HBT BiCMOS Circuits for Communication and Radar Transceivers

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High-Speed SiGe HBT BiCMOS Circuits for Communication and Radar Transceivers

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To my family,

friends,

and loved ones.

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SUMMARY

This dissertation explores high-speed silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) bipolar complementary metal oxide semiconductor (BiCMOS) circuits for next-generation ground- and space-based millimeter-wave (MMW $\geq$ 30 GHz) communication front-ends and X-band (8 to 12 GHz) radar (*ra*dio *d*etection *a*nd *r*anging) modules. The requirements of next-generation transceivers, for both radar and communication applications, are low power, small size, light weight, low cost, high performance, and high reliability. For this purpose, the high-speed circuits that satisfy the demanding specifications of next-generation transceivers are implemented in SiGe HBT BiCMOS technology, and the device-circuit interactions of SiGe HBTs to transceiver building blocks for performance optimization and radiation tolerance are investigated.

For X-band radar module components, the dissertation covers:

1. The design of an ultra-low-noise X-band SiGe HBT low-noise-amplifier (LNA) (Chapter II, also published in [1]).

2. The design of low-loss shunt and series/shunt X-band Si CMOS single-pole double-throw (SPDT) switches (Chapter III, also published in [2]).

3. The design of a low-power X-band SiGe HBT LNA for near-space radar applications (Chapter IV, also published in [3]).

For MMW communication front-end circuits, the dissertation covers:

4. The design of an inductorless SiGe HBT ring oscillator for MMW operation (Chapter V, also published in [4]).

5. The study of emitter scaling and device biasing on MMW SiGe HBT voltage-controlled oscillator (VCO) performance (Chapter VI, also published in [5]).

6. The study of proton radiation on MMW SiGe HBT transceiver building blocks (Chapter VII, also published in [6]).

CHAPTER I

INTRODUCTION

1.1 Millimeter-Wave Wireless Communication Transceiver Front-Ends

The global telecommunications market is predicted to reach over $3.1 trillion by 2008 [7], [8]. The double-digit compound annual growth rate (CAGR) of the global wireless market is estimated at $678.5 billion in 2008 [7], [9]. In the United States, wireless telephony has become less expensive than landline with the introduction of one-rate pricing plans, spurring an increase in wireless subscriberships and thus handset revenues [9], [10]. Moreover, high-speed wireless access and wireless local area network (WLAN) systems are also driving the wireless market as users demand more broadband connectivity for multimedia applications [11]. Clearly, the wireless market is a key driver for the communications industry.

To satisfy the need for more bandwidth, next-generation wireless access will operate in the 60 GHz industrial, scientific, and medical (ISM) band, in which a 5 GHz (59 to 64 GHz) spectrum has been set aside by the Federal Communications Commission (FCC) for general unlicensed short-range (< 1 km), broadband (> 1 Gb/s), point-to-point or point-to-multipoint applications as part of the fourth-generation (4G) system [12]. The envisioned connectivity of a 60 GHz wireless network is shown in Figure 1.

The allocation of the 60 GHz band creates new challenges and opportunities for millimeter-wave (MMW $\geq$ 30 GHz) transceiver front-end design. Figure 2 shows a block diagram of a 60 GHz MMW transceiver. The front-end combines a heterodyne transmitter (Tx) with a direct-conversion receiver (Rx) [13]. It includes a power amplifier

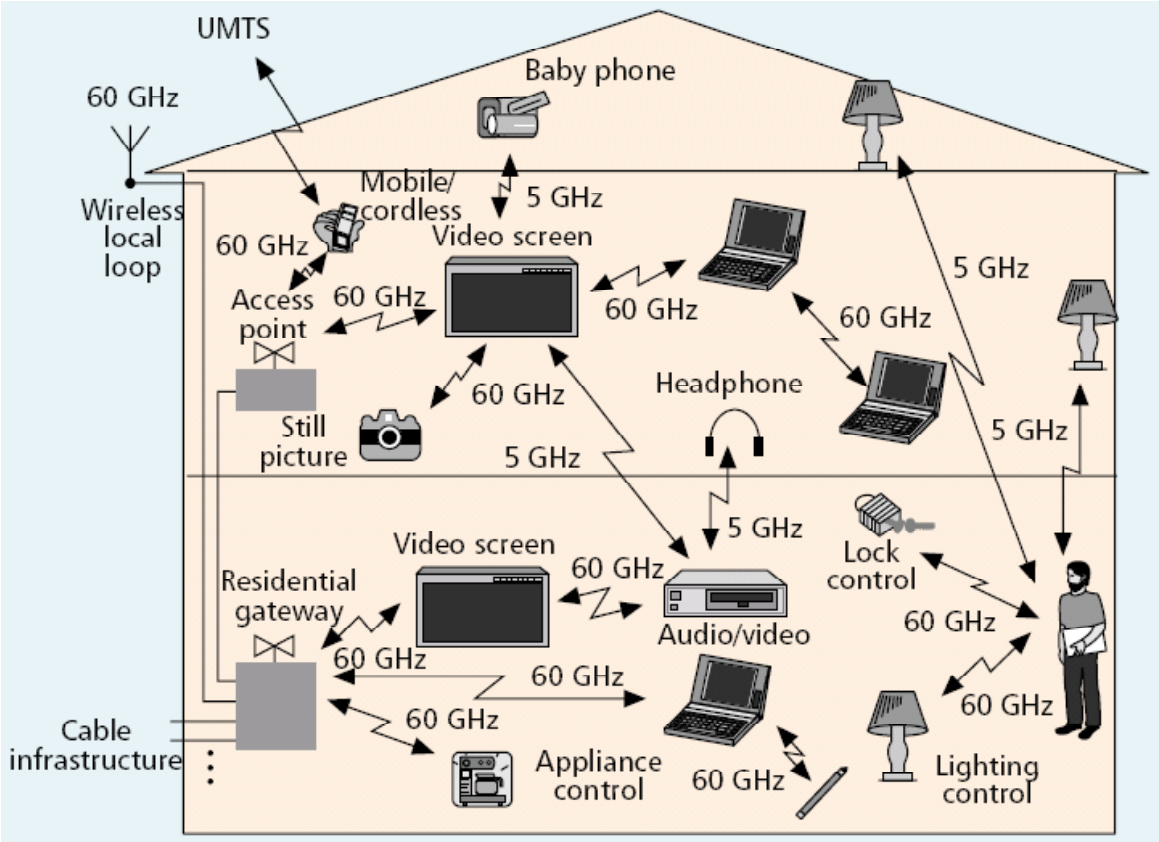


Figure 1: Connectivity of a 60 GHz wireless network (after [12]).

(PA), band-pass filters (BPFs), up-conversion mixers, frequency multipliers, an intermediate frequency (IF) amplifier, quadrature phase generators, frequency dividers, low-pass filters (LPFs), voltage-controlled oscillators (VCOs), a low-noise amplifier (LNA), down-conversion mixers, and variable-gain amplifiers (VGAs).

Current front-ends operating at 60 GHz are typically hybrid assemblies composed of individual monolithic microwave integrated circuits (MMICs) implemented in III-V compound semiconductor technologies such as gallium-arsenide (GaAs) and/or indium-phosphide (InP) [14]-[21]. The separate MMICs are then assembled in multi-chip modules (MCMs) to realize the complete transceiver front-end. Figure 3 shows the MCMs of a 60 GHz MMW transceiver.

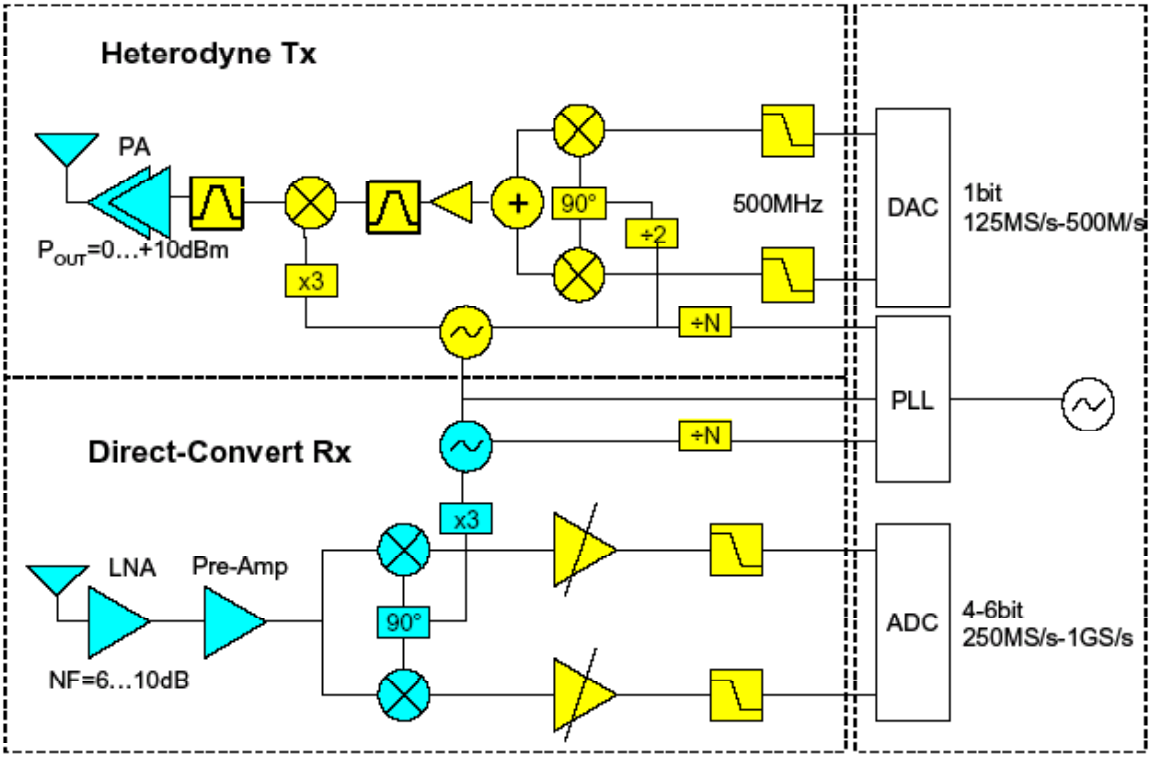


Figure 2: Block diagram of a 60 GHz MMW transceiver (after [13]).

III-V compound semiconductors offer significant performance advantages over traditional silicon (Si) technologies. Considering that a 6" GaAs starting wafer costs more than $5000, whereas an 8" Si starting wafer costs less than $100 [22], it is clear that III-V technologies cost much more. Furthermore, the assembled MCM front-ends are bulky and heavy. Considerable cost savings can be achieved if the front-end MMICs can all be implemented in a Si-based technology, enabling the integration of the complete front-end, along with analog and digital circuitries on a single chip, thereby also foregoing the cost, weight, and size penalty associated with MCMs.

1.2 X-Band Active Phased Array Radar Transmit/Receive Modules

A phased array radar contains a number of antenna elements in which the amplitude and phase of the signal feeding to each element can be varied such that the effective radiation

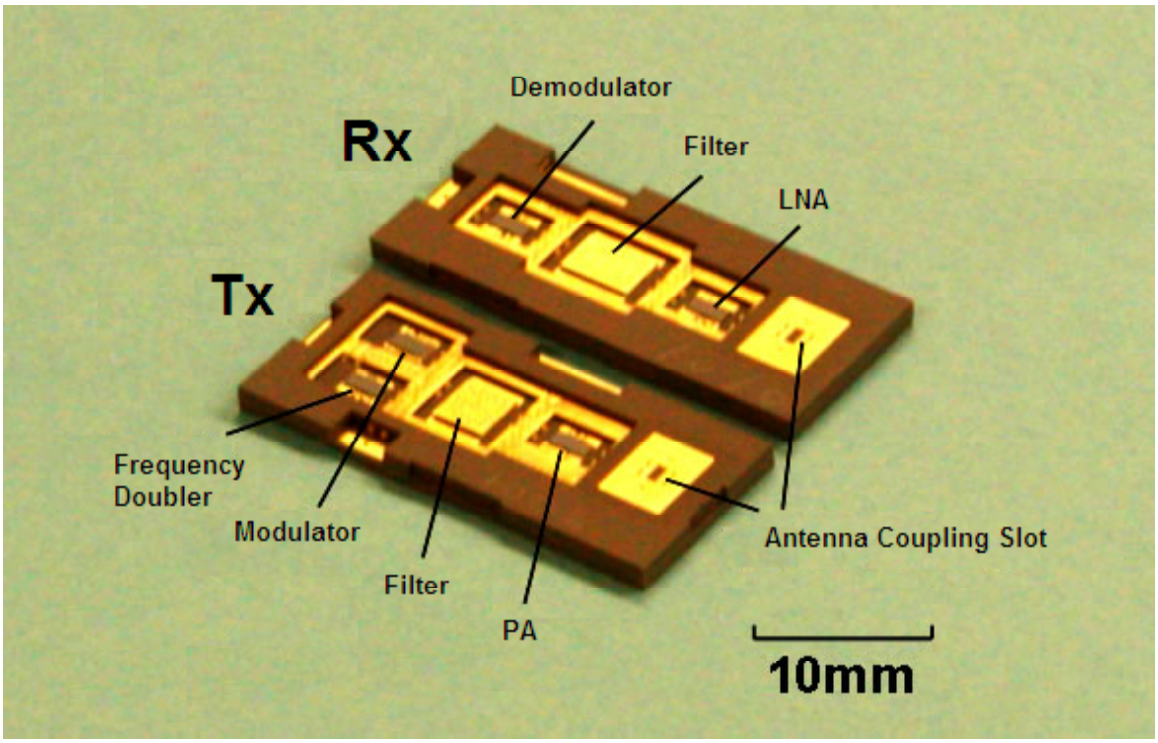
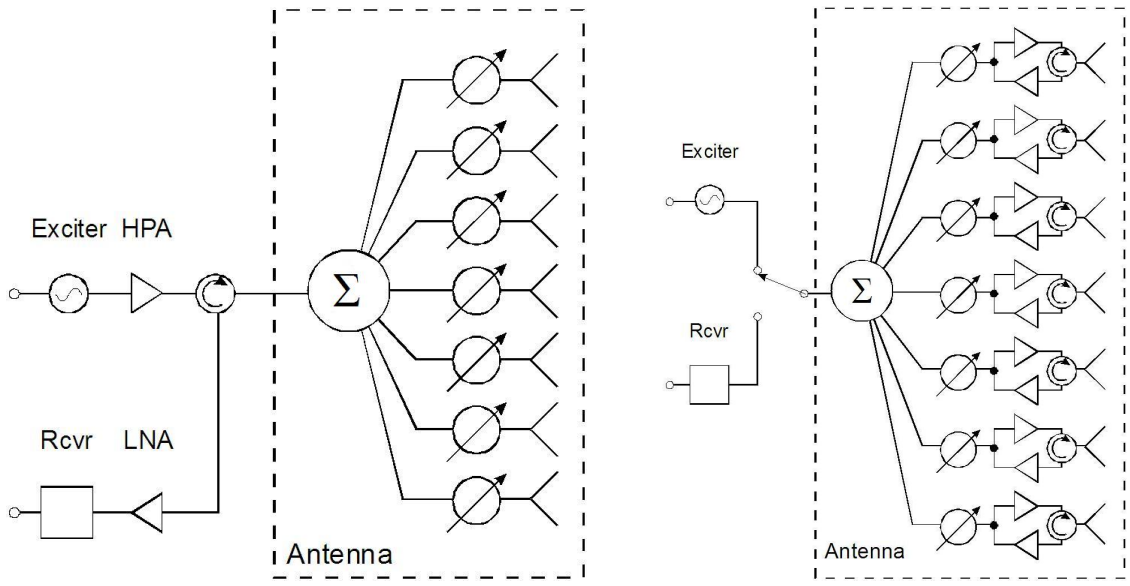


Figure 3: Photograph of the MCMs of a 60 GHz MMW transceiver (after [21]).

pattern is reinforced in the desired direction and suppressed in others, thereby improving the signal-to-noise ratio (SNR) and the overall efficiency of the system [23]. Passive phased array radars typically use a high-power vacuum tube transmitter to drive a subarray of antennas, as shown in Figure 4(a), where as active phased array radars use a solid-state transmit/receive (T/R) module to drive each antenna element [24]-[26], as shown in Figure 4(b). Figure 5(a) and 5(b) shows a photograph of a passive and an active phased array radar, respectively.

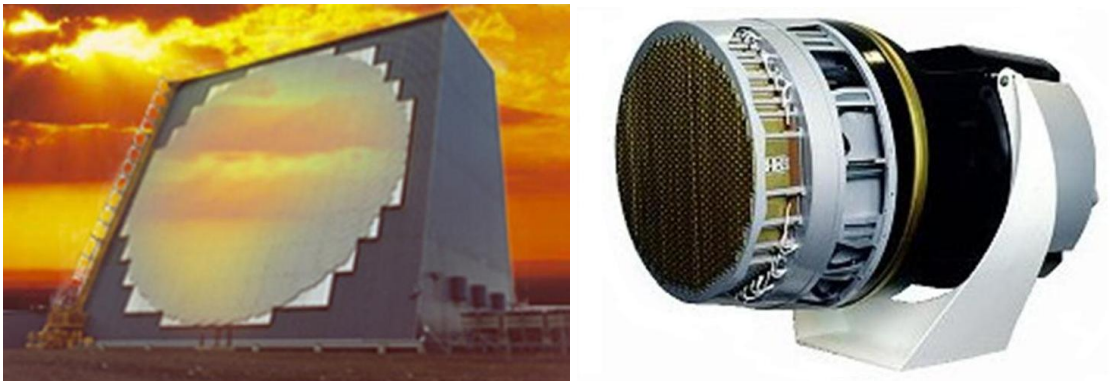
An active phased array radar is often favored because the loss on transmit is reduced and the SNR on receive is improved as a result of the close proximity of the PA and LNA, respectively, to the radiating element. Figure 6 shows the block diagram of a T/R module in an X-band (8 to 12 GHz) active phased array radar. It consists of a PA, a limiter, an LNA, a single-pole double-throw (SPDT) switch, a phase shifter (PS), and a circulator [27].

Similar to the MMW transceiver front-ends operating at 60 GHz, the X-band active



(a) (b)

Figure 4: Block diagram of (a) a passive and (b) an active phased array radar (after [25]).



(a) (b)

Figure 5: Photograph of (a) a passive and (b) an active phased array radar (after [26]).

phased array radar T/R modules are MCMs assembled with separate III-V MMICs [28]-[32], with each MCM costing up to $1000 [33]. Moreover, current active phased array radar employs a high power density (HPD) approach, where high supply current and large prime power are used to operate the array (i.e., a 1 MW diesel generator is required to run 25,000 HPD MCMs, as shown in Figure 7), resulting in large waste heat load [33]. Hence, current-generation of X-band active phased array radars is very expensive to deploy and

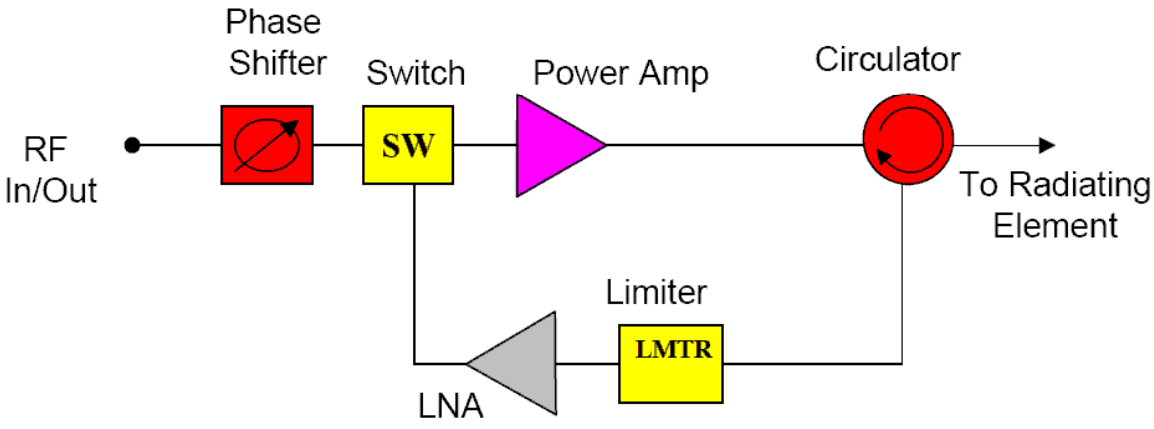


Figure 6: Block diagram of an X-band active phased array radar T/R module (after [27]).

operate.

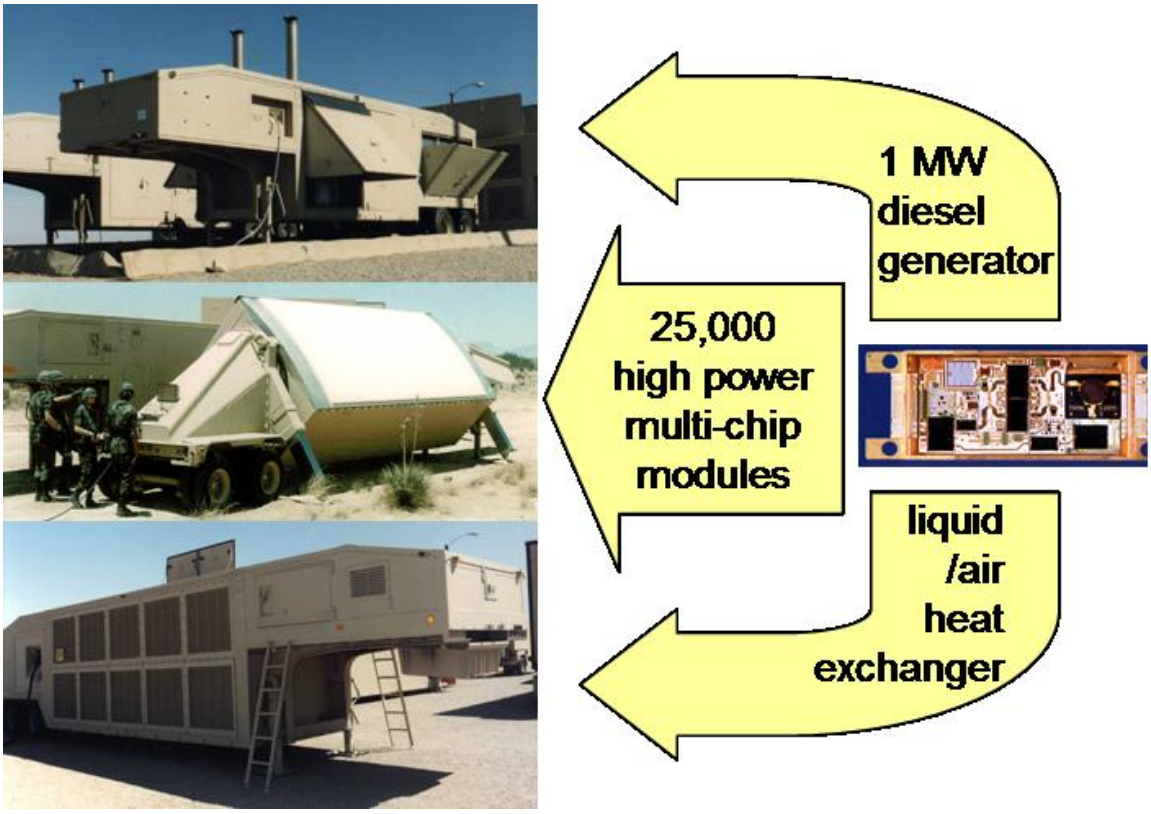


Figure 7: Current active phased array radar using a HPD approach (after [33]).

The performance of a radar system can be evaluated based on several figure-of-merits (*FOM*s). The track *FOM* is the power-aperture-gain product, defined as [25]

$$FOM_{track} = PAG, \tag{1}$$

where P, A, and G are the average transmit power, aperture area, and gain of the array, respectively. In an active phased array radar, power, aperture, and gain are given as [25]

$$P = P_e N, \tag{2}$$

$$A = A_e N, \tag{3}$$

and

$$G = G_e N \approx \frac{4\pi A_e}{\lambda^2} N \tag{4}$$

where P_e, A_e, G_e are the average transmit power, aperture area, and gain of a single antenna element, respectively, and λ and N are the wavelength of operation and number of antenna elements in the array. The track *FOM* for an active phased array radar is then

$$FOM_{track,active} = PAG = P_e A_e^2 \frac{4\pi}{\lambda^2} N^3. \tag{5}$$

Thus, for a fixed $FOM_{track,active}$, the P_e can be drastically reduced by increasing N, thereby reducing the total prime power required and waste heat load generated.

Based on this concept, an innovative panel-based X-band active phased array radar called SPEAR, which stands for *S*calable *P*anels for *E*fficient *A*ffordable *R*adar, aims to reduce both deployment and operation cost by using a low power density (LPD) approach [25], [33], in which tens of thousands of single-chip T/R modules (costing < $10 each) operate on reduced prime power, as shown in Figure 8. A key challenge of SPEAR is the development of a suitable low-cost, highly efficient, single-chip, X-band T/R module [27], [34]. Perhaps these low-cost modules can be implemented in a Si-based technology, where analog and digital circuitries can be integrated as well.

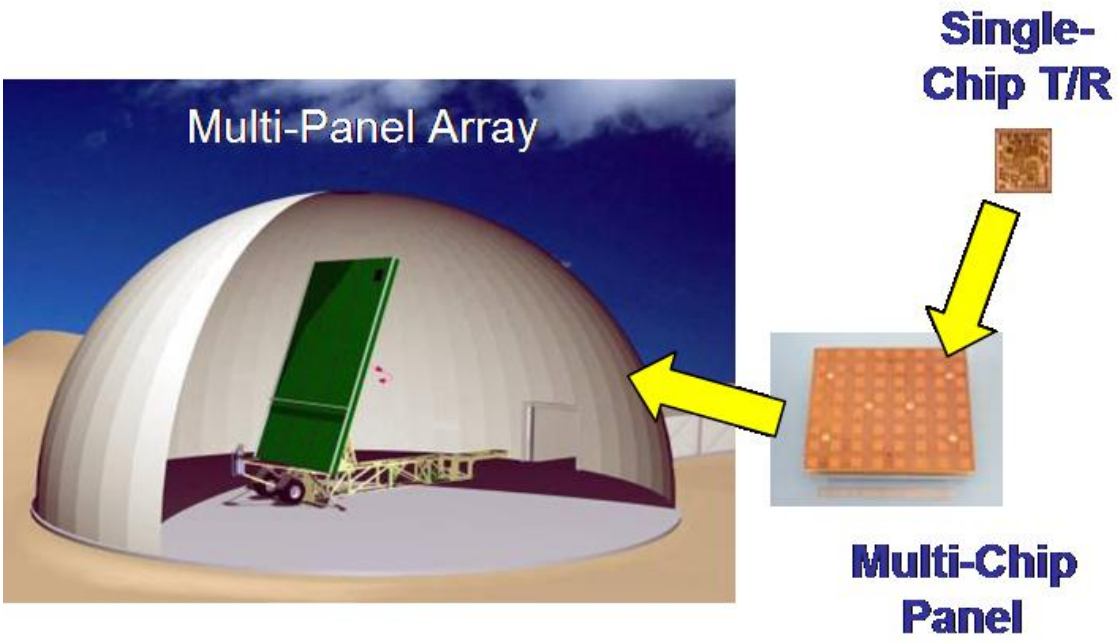


Figure 8: Future active phased array radar using an LPD approach (after [33]).

1.3 SiGe HBT BiCMOS Technology

In addition to maintaining high performance and high reliability, it is clear that achieving low power, small size, light weight, and low cost are essential requirements for next-generation communication front-ends and radar modules. Recently, an alternative integrated circuit (IC) technology based on silicon-germanium (SiGe) alloys has shown the potential to fulfill these requirements [35].

SiGe heterojunction bipolar transistor (HBT) technology utilizes bandgap engineering to dramatically improve Si bipolar junction transistor (BJT) performance while maintaining strict compatibility with conventional Si complementary metal oxide semiconductor (CMOS) manufacturing, thus offering a bipolar complementary metal oxide semiconductor (BiCMOS) technology. The incorporation of germanium (Ge), which has a smaller energy bandgap than that of Si (0.66 eV versus 1.12 eV), into the neutral Si base creates a SiGe alloy with a bandgap reduction of approximately 75 meV from Si for each 10% of Ge introduced [35]. The resulting SiGe HBTs have many advantages over traditional Si

BJTs. The improvements are best illustrated with an overlay of the forward-active mode energy band diagrams for a Si BJT and a graded-base SiGe HBT, both with constant emitter, base, and collector doping, as shown in Figure 9. For the SiGe HBT, the Ge content is linearly graded from 0% near the metallurgical emitter-base (EB) junction to a maximum value of Ge content near the metallurgical collector-base (CB) junction, and then quickly ramped back down to 0%. The Ge induced reduction in base bandgap occurs from the EB edge of the quasi-neutral base , $\triangle E_{g,Ge}(x = 0)$, to the CB edge of the quasi-neutral base, $\triangle E_{g,Ge}(x = W_b)$.

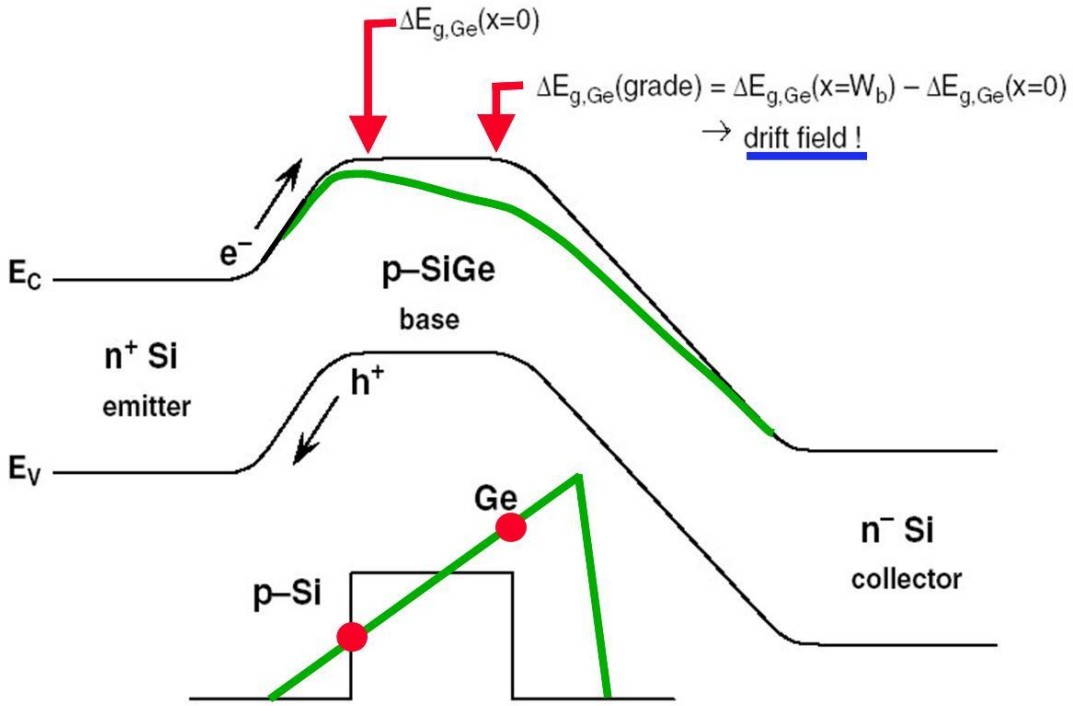


Figure 9: Energy band diagram for a Si BJT and a graded-base SiGe HBT (after [35]).

The introduction of Ge at the EB edge of the quasi-neutral base lowers the potential barrier for injecting electrons into the base from the emitter, translating into exponentially more electron injection for the same applied base-emitter voltage (V_{BE}), resulting in a higher collector current (I_C), and hence an increase in current gain (β). The enhancement

in β of a SiGe HBT over an identically constructed Si BJT is [35]

$$\frac{\beta_{SiGe}}{\beta_{Si}} \propto \frac{\triangle E_{g,Ge}(grade)/kTe^{\triangle E_{g,Ge}(0)/kT}}{1-e^{-\triangle E_{g,Ge}(grade)/kT}}, \tag{6}$$

where $\triangle E_{g,Ge}(grade) = \triangle E_{g,Ge}(x = W_b) - \triangle E_{g,Ge}(x = 0)$. As expected, the improvement is exponentially dependent on the EB boundary value of the Ge induced band offset. Figure 10 confirms the enhancement in β with measured Gummel characteristics.

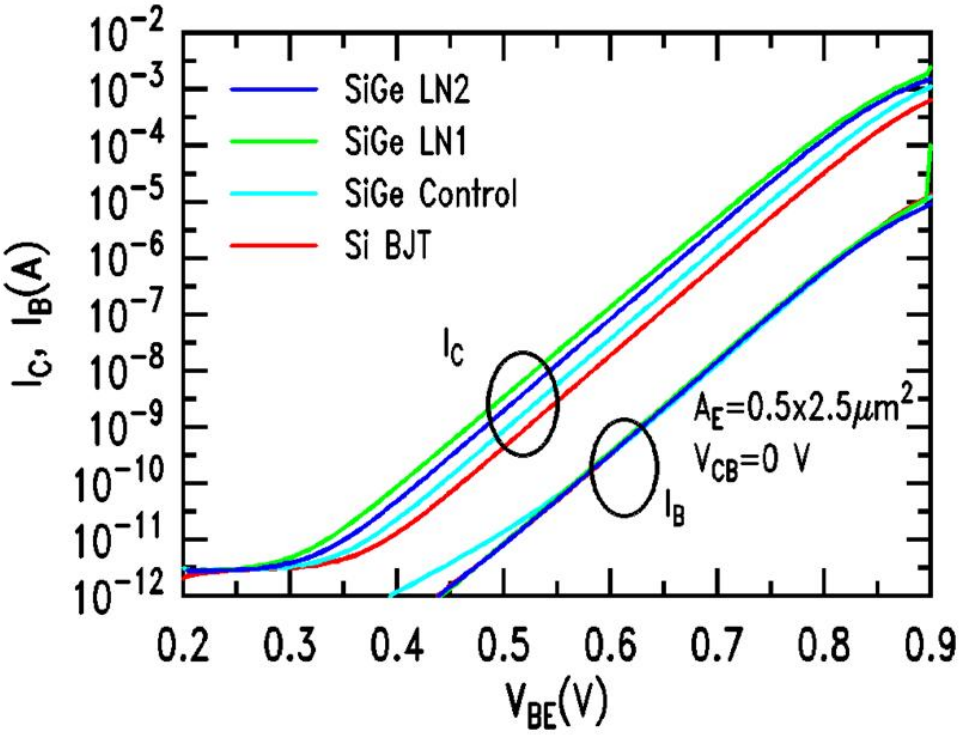


Figure 10: Comparison of measured Gummel characteristics of comparably constructed Si BJT and SiGe HBTs with different Ge profiles (after [35]).

The grading of Ge across the neutral base in SiGe HBTs, with a higher Ge content at the EB edge of the quasi-neutral base, changes the energy band in such a way that a built-in drift field aiding minority electron transport across the neutral base is induced, thereby reducing the base transit time (τ_b), which dominates the total transit time in Si BJTs, and hence increases the unity current gain cutoff frequency (f_T). The intensity of

the Ge gradient induced drift field across the neutral base is determined by the amount of Ge grading. The resulting reduction in τ_b of a SiGe HBT over an identically constructed Si BJT is [35]

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} \propto \frac{kT}{\triangle E_{g,Ge}(grade)} \cdot \left\{ 1 - \frac{kT}{\triangle E_{g,Ge}(grade)} \left[1 - e^{-\triangle E_{g,Ge}(grade)/kT} \right] \right\}. \tag{7}$$

As expected, the improvement is reciprocally dependent on the Ge induced bandgap grading factor. Figure 11 confirms this reduction in τ_b with measured f_T. Other advantages, such as increases in Early voltage (V_A) and maximum oscillation frequency (f_{max}), reductions in low-frequency ($1/f$) and high-frequency (broadband) noise, and improved low-temperature performance of SiGe HBTs over traditional Si BJTs are described in [35].

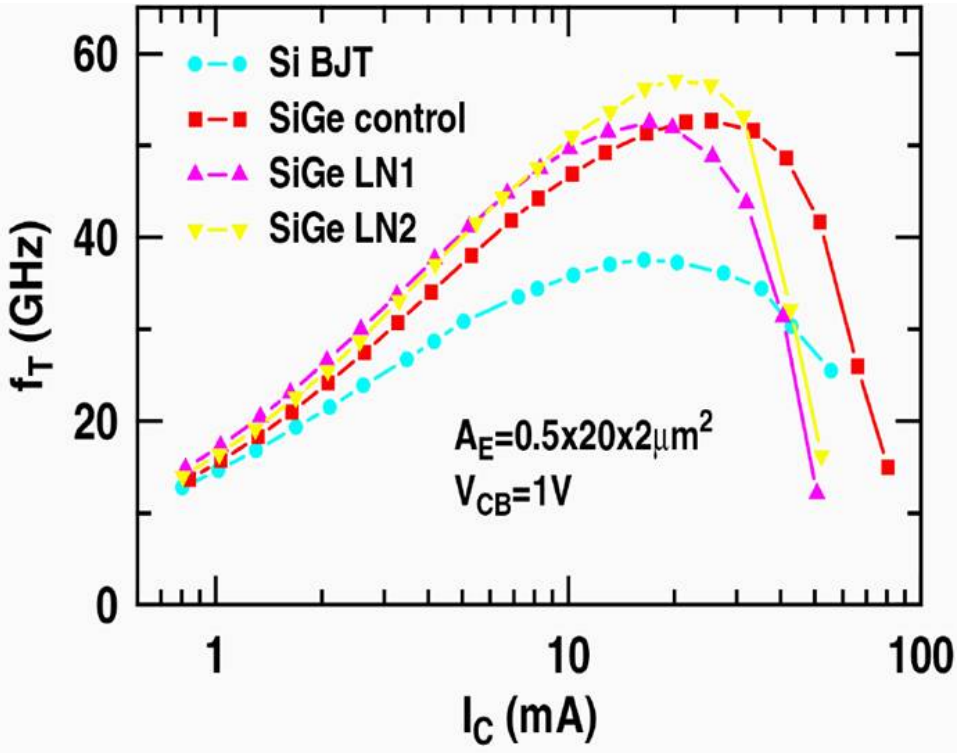


Figure 11: Comparison of measured cutoff frequencies of comparably constructed Si BJT and SiGe HBTs with different Ge profiles (after [35]).

SiGe HBT BiCMOS technology is relatively new, even though the concept of HBTs

was pioneered by Dr. H. Kroemer back in 1957 [36]. Limited by SiGe film growth problems, the first functional SiGe HBT was not demonstrated until 1987 [37]. The first demonstration of performance advantage over Si BJT came in 1990, with a peak f_T roughly twice as high at 75 GHz [38]. The first SiGe HBT technology entered commercial production in 1994 [39]. Figure 12 shows the schematic cross section of a first-generation SiGe HBT. Soon after, the first successful integration of SiGe HBT and CMOS technology into SiGe HBT BiCMOS technology was demonstrated in 1995 [40]. Since then, SiGe HBT BiCMOS technology has evolved very rapidly, reaching a point where it is of comparable performance with the best-of-breed III-V compound semiconductor technologies. Table 1 shows the key specifications of commercial SiGe HBT BiCMOS technologies offered by IBM Microelectronics [41]-[43].

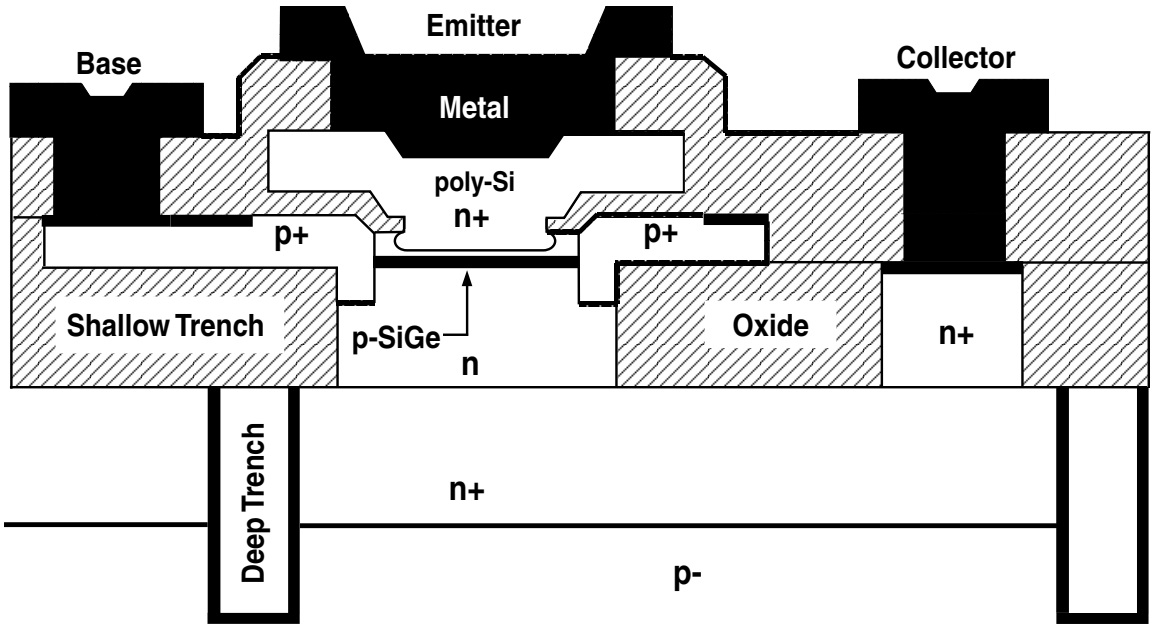


Figure 12: Cross section of a first/second-generation (*npn*) SiGe HBT (after [35]).

With the recent announcement of third-generation SiGe technology incorporating *pnp* SiGe HBTs with f_T/f_{max} of 80/120 GHz [44], as well as fourth-generation SiGe HBTs achieving f_T/f_{max} of 375/210 GHz [45] and 300/300 GHz [46], the application space for

SiGe HBT BiCMOS technology has broadened from a variety of analog and radio frequency (RF) applications to include microwave and MMW applications. SiGe HBT BiCMOS technology thus combines III-V like device performance with high integration, high yield, and hence low cost of Si, thereby enabling a fully integrated digital, analog, RF, and MMW system-on-a-chip (SOC) design solution. Furthermore, SiGe HBTs have also been shown to be robust with respect to proton radiation without any costly radiation hardening [35]. With these attributes, SiGe HBT BiCMOS technology may provide the high performance, high reliability, small size, light weight, and low cost transceivers needed for next-generation ground- and space-based communication and radar systems.

Table 1: Key specifications of commercial SiGe HBT BiCMOS technologies offered by IBM Microelectronics.

IBM Technology	5HP/6HP [41]	7HP [42]	8HP [43]
SiGe HBT Generation	First	Second	Third
f_T [GHz]	47	120	200
f_{max} [GHz]	65	100	280
BV_{CEO} [V]	3.3	1.8	1.7
$W_{E,eff}$ [μm]	0.42	0.18	0.13
CMOS L_{eff} [μm]	0.35	0.14	0.092
CMOS Supply [V]	3.3	1.8	1.5

1.4 Motivation for Dissertation

The unique properties of SiGe HBTs make them suitable for a variety of applications. Comparing to Si RF CMOS devices, SiGe HBTs have better frequency response, in fact on-par or even better than state-of-the-art III-V devices, making them suitable for many RF and MMW applications. Being a bipolar transistor, the transconductance of a SiGe HBT is higher than that of a Si CMOS device, an attractive feature for analog applications. Even though the performance of the Si RF CMOS devices improves as technology scales, current-generation of SiGe HBTs still out performs current-generation of Si RF CMOS

devices. The ability of SiGe HBTs to integrate seamlessly with conventional Si CMOS into a SiGe HBT BiCMOS technology offers a level of integration and cost advantage over III-V technologies. However, since III-V devices have larger bandgaps, and hence higher breakdown voltages, they will continue to dominate the market for power devices, as well as optoelectronic devices because of their direct-gap nature. Figure 13 shows the application spectrum of various device technologies envisioned by the International Technology Roadmap for Semiconductors (ITRS) in 2005 [47]. SiGe HBT BiCMOS technology is well positioned for applications where the performance required are beyond the reach of Si RF CMOS and where the cost requirements are prohibitive for implementation in III-V technologies.

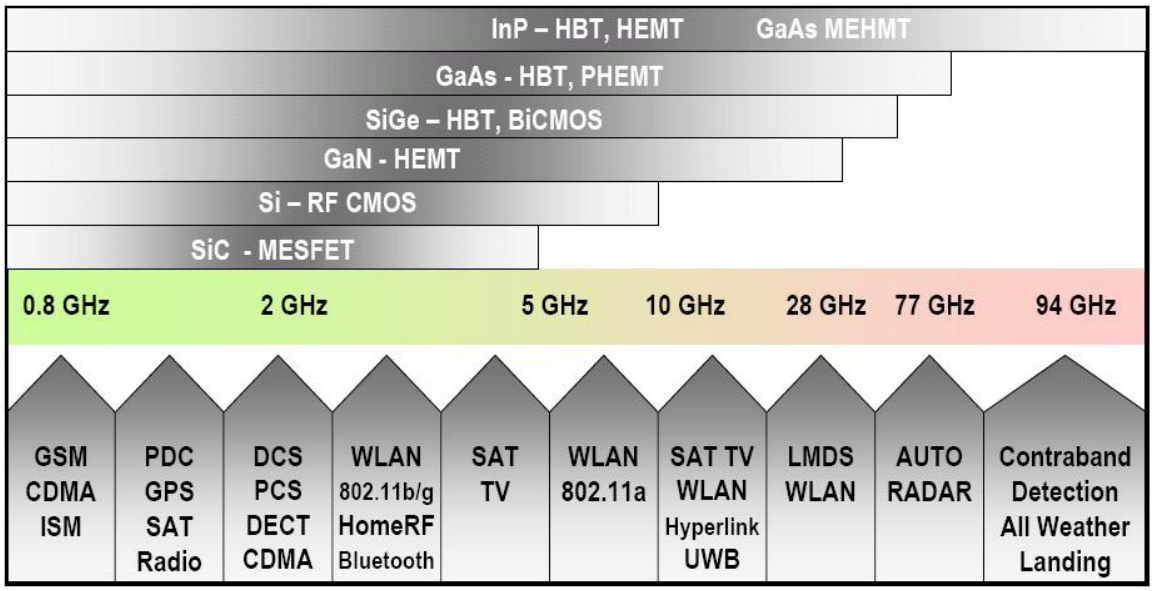


Figure 13: Application spectrum of various device technologies (after [47]).

The objective of the research in this dissertation is to explore high-speed SiGe HBT BiCMOS circuits for next-generation ground- and space-based X-band radar modules and MMW communication front-ends. The requirements of next-generation transceivers, for both radar and communication applications, are low power, small size, light weight, low cost, high performance, and high reliability. For this purpose, the high-speed circuits

that satisfy the demanding specifications of next-generation transceivers are implemented in SiGe HBT BiCMOS technology, and the device-circuit interactions of SiGe HBTs to transceiver building blocks for performance optimization and radiation tolerance are investigated.

1.5 Organization of Dissertation

Chapter II (also published in [1]) presents the design of an ultra-low-noise X-band SiGe HBT LNA for a monolithically integrated active phased array T/R radar module. Implemented in a 0.13 μm, 200 GHz SiGe HBT BiCMOS technology, the LNA occupies 730×720 μm^2 with bondpads, and dissipates 15 mW from a 2.5 V power supply. The circuit exhibits a gain (G) greater than 19 dB from 8.5 to 10.5 GHz, and a mean noise figure (NF) of 1.36 dB across X-band. At 10 GHz, the input 1-dB compression point (IP_{1-dB}) and the input third-order intercept point (IIP_3) are -10.0 dBm and 0.8 dBm, respectively.

Chapter III (also published in [2]) presents the design of low-loss shunt and series/shunt X-band Si CMOS SPDT switches for a monolithically integrated active phased array T/R radar module in a 0.13 μm, 200 GHz SiGe HBT BiCMOS technology. From 8.5 to 10.5 GHz, the worst case return loss (RL), insertion loss IL, and isolation are 14.5, 1.89, and 20.5 dB, respectively, for the reflective shunt switch, and 22.2, 2.33, and 22.5 dB, respectively, for the absorptive series/shunt switch. Both switches exhibit an IIP_3 of about 28 dBm and dissipate no dc power.

Chapter IV (also published in [3]) presents the design of a low-power X-band SiGe HBT LNA for near-space radar applications. Implemented with 180 GHz SiGe HBTs, the circuit occupies 780 × 660 μm^2. The LNA exhibits a G of 11.0 dB at 9.5 GHz, a mean NF of 2.78 dB across X-band, and an IIP_3 of -9.1 dBm near 9.5 GHz, while dissipating only 2.5 mW.

Chapter V (also published in [4]) presents the design of an inductorless MMW SiGe HBT ring oscillator. Implemented in a 0.18 μm, 120 GHz SiGe HBT BiCMOS technology,

the circuit occupies an extremely compact active area of only 60 × 180 μm^2 due to lack of inductors. The frequency is tunable from 28.36 to 31.96 GHz, and the measured phase noise is -85.33 dBc/Hz at 1 MHz offset from 31.96 GHz. Operating on a -3.0 V supply, the total power consumption is 87 mW. The resulting oscillator *FOM* is -156 dBc/Hz.

Chapter VI (also published in [5]) presents the study of emitter scaling and device biasing on MMW SiGe HBT VCO performance. A comprehensive experimental investigation is carried out, for the first time, to explore the device-circuit interactions of 200 GHz SiGe HBTs to a variety of VCO specifications. Design insights and tradeoffs for optimizing VCO performance, including oscillation frequency (f_{osc}) and phase noise, are given.

Chapter VII (also published in [6]) presents the first experimental results on the study of 63.3 MeV proton radiation on MMW space data link transceiver building blocks implemented with 200 GHz SiGe HBTs. A 60 GHz SiGe HBT LNA and VCO were each irradiated to proton fluences of 5.0×10^{13} p/cm^2. The device- and circuit-level performance degradation associated with these extreme proton fluences are examined.

Chapter VIII concludes the dissertation with a discussion on possible future work.

CHAPTER II

THE DESIGN OF ULTRA-LOW-NOISE X-BAND SIGE HBT LNA FOR RADAR APPLICATIONS

2.1 Introduction

For next-generation X-band active phased array radars, a major challenge is the development of a suitable low-cost (< $10 each), highly efficient, single-chip T/R module [48]-[50]. With the high cost and integration difficulties associated with III-V technologies, SiGe HBT BiCMOS technology is a logical alternative if a single-chip SiGe HBT BiCMOS T/R module can be successfully demonstrated. Figure 14 shows the block diagram of the envisioned monolithically integrated T/R module.

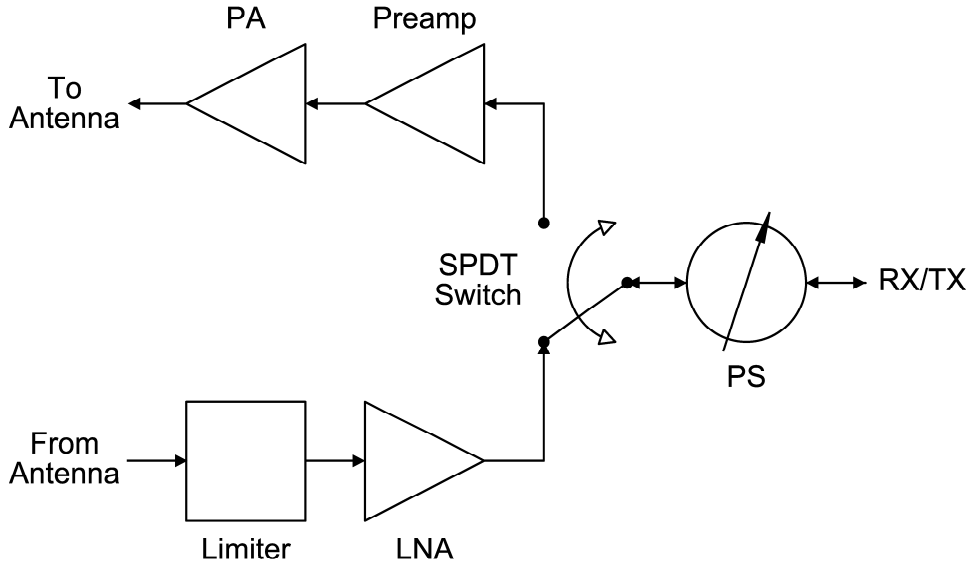


Figure 14: Block diagram of the envisioned monolithically integrated T/R module.

This chapter presents the design and implementation of a circuit block essential to the envisioned monolithic X-band T/R module: the ultra-low-noise SiGe HBT LNA. The radar

system specifications require the LNA to operate from 8.5 to 10.5 GHz, have a *NF* less than 2.0 dB, a *G* greater than 15 dB, and an IIP_3 great than -10.0 dBm [34], clearly a challenging set of performance targets in Si-based technology. The SiGe HBT BiCMOS technology used to fabricate the LNA is discussed in Section 2.2. Section 2.3 describes the details of the LNA design. Measurement results are presented in Section 2.4. Section 2.5 compares the ultra-low-noise LNA to other state-of-the-art SiGe HBT LNAs operating in X-band.

2.2 SiGe HBT BiCMOS Technology

A commercially available 0.13 μm, 200 GHz SiGe HBT BiCMOS technology is used to implement the LNA [43]. It features state-of-the-art SiGe HBTs with peak f_T/f_{max} of 200/280 GHz, 0.13 μm ASIC compatible 1.2 V Si CMOS devices, and a full suite of passive elements, including metal-insulator-metal (MIM) capacitors and thin-film resistors. Five levels of copper interconnects are available, along with two thick top layers of aluminum metallization to enable high-quality factor (Q) inductor and transmission line designs.

The advancement in SiGe HBT performance is achieved by employing: (1) a "raised extrinsic base" structure which eliminates any out-diffusion of the extrinsic base, thereby significantly lowering base-collector capacitance (C_{BC}); (2) an unconditionally stable, 25% peak germanium, carbon-doped, graded epitaxial SiGe base; (3) an *in-situ* doped polysilicon emitter; and (4) a laterally scaled emitter width which minimizes base resistance and thus improves frequency response and noise characteristics. A schematic cross section of the 200 GHz SiGe HBTs is shown in Figure 15.

2.3 Low-Noise Amplifier Design

An LNA presents considerable design challenges because of simultaneous need for: (1) low *NF*, (2) high *G*, (3) high linearity (IP_{1-dB} and IIP_3), (4) high input and output *RL* (minimum S_{11} and S_{22}), (5) unconditional stability, and (6) low power dissipation (P_{diss}). The above requirements are interdependent on one another, and can rarely be concurrently

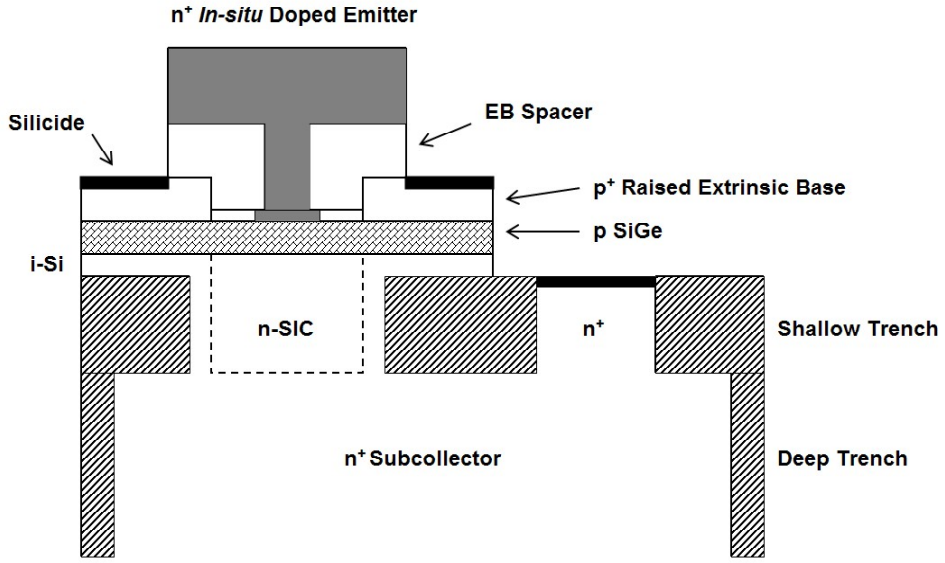


Figure 15: Schematic cross section of the 200 GHz SiGe HBTs.

met. Hence, tradeoffs are inevitable. The schematic of the ultra-low-noise SiGe HBT LNA is shown in Figure 16, and employs a cascode topology. The input transistor Q_1 acts as a transconductor and the common base transistor Q_2 acts as a unity current gain buffer. The addition of transistor Q_2 minimizes the Miller effect of C_{BC} of Q_1 and simplifies the LNA design from a bilateral to a unilateral design. However, the LNA now requires a higher supply voltage (V_{CC}).

The LNA design was accomplished as follows using commercial circuit simulators with fully calibrated device models:

1. An optimum collector current density ($J_{C,opt}$) at minimum NF_{min} was determined with equally sized Q_1 and Q_2 as a basic unit cell, as opposed to using only Q_1, because the cascode structure has a different $J_{C,opt}$ than a common emitter stage [51]. However, a J_C of 1.5 × $J_{C,opt}$ was chosen to improve G and IIP_3 without significantly degrading NF_{min} because of the broad nature of minimum NF_{min} versus J_C in SiGe HBTs [52]-[54]. Hence NF and P_{diss} are effectively traded for G and IIP_3.

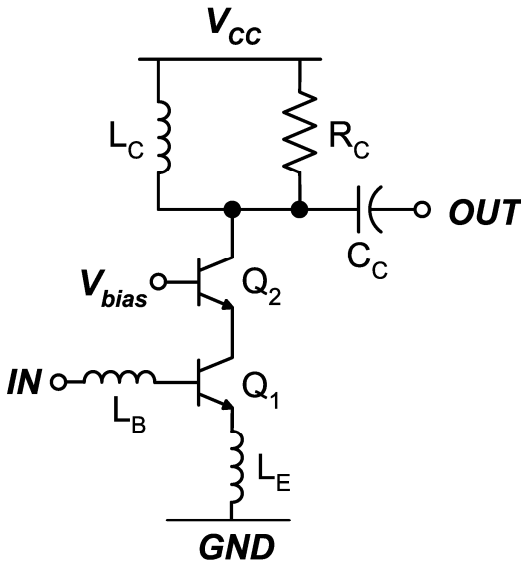


Figure 16: Simplified schematic of the ultra-low-noise SiGe HBT LNA.

2. The emitter lengths of Q_1 and Q_2 were scaled so that the optimum source resistance ($R_{S,opt}$) is equivalent to 50 Ω while maintaining the same J_C. The scaling of emitter length has little effect on minimum NF_{min} at a given J_C [52]. The resistive part of the noise impedance is now matched. Hence P_{diss} is effectively traded for noise matching.

3. The emitter degeneration inductor (L_E) serves to match the real part of the input impedance, as well as improve linearity by creating a series-series negative feedback, at a cost of reducing *G*, and a slight increase in *NF*. The L_E is given by [55]

$$L_E = \frac{50}{2\pi f_T}, \tag{8}$$

where f_T is the cutoff frequency of the scaled cascode structure biased at J_C. Since an L_E of less than 100 pH is required (smaller than the smallest spiral inductor provided by the foundry), a transmission line is used instead. The resistive part of the input impedance is now matched. Hence *G* and *NF* are effectively traded for input matching and IIP_3.

4. The series base inductor (L_B) serves to cancel out the input reactance of the base-emitter capacitance (C_{BE}) of Q_1, as well as to transform the optimum noise reactance to 0 Ω [55]. The L_B is given by [55]

$$L_B = \frac{1}{\omega^2 C_{BE}} - L_E, \tag{9}$$

where ω is the operating frequency. The L_B required was about 1 nH. An inductor with a peak Q of 20 at 11 GHz was used. Both noise matching and input matching are now simultaneously achieved.

5. The collector resistor (R_C) was added to ease output impedance matching, as well as to improve stability, at a cost of reducing G and IIP_3. Hence G and IIP_3 are effectively traded for output matching and stability.

6. The output impedance matching was achieved by using an L-network with a shunt inductor (L_C) and a series capacitor (C_C), which also act as a *dc* feed and a *dc* block, respectively. Once the LNA is output matched, the design would be complete.

2.4 Measurement Results

The LNA was measured on-wafer in an electromagnetic interference (EMI) shielded room using ground-signal-ground (GSG) coplanar microwave probes. Probe level calibration was performed and cable loss was accounted for during testing. Operating from a V_{CC} of 2.5 V, the LNA draws an I_C of 6 mA, and thus dissipates 15 mW. Figure 17 shows the LNA chip micrograph. The total die area is 730 × 720 μm^2, including bondpads.

The scattering (S) parameters were measured using an Agilent 8510C vector network analyzer (VNA). Figure 18 shows the measured S_{11} and S_{22} (input and output *RL*). The S_{11} is less than -15 dB at 8.5 GHz, decreases to less than -16 dB at 9 GHz, and then increases to less than -11 dB at 10.5 GHz. The S_{22} is less than -9 dB at 8.5 GHz, decreases to less than -21 dB at 9.6 GHz, and then increases to less than -10 dB at 10.5 GHz. Figure 19 shows

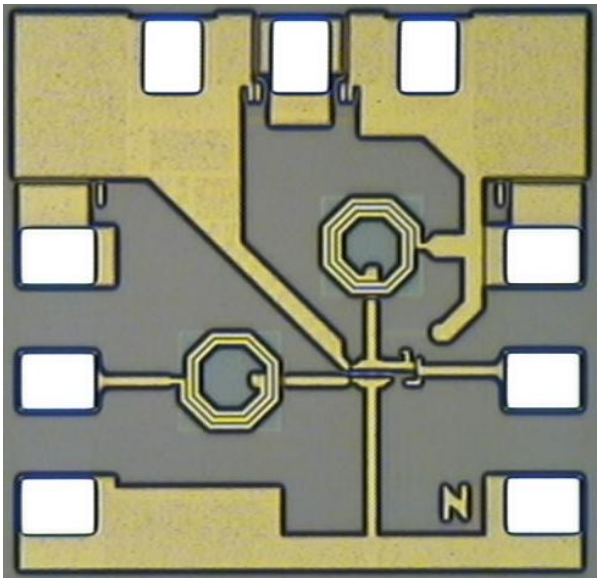


Figure 17: Chip micrograph of the ultra-low-noise SiGe HBT LNA.

the measured S_{21} and S_{12} (G and isolation). The S_{21} is greater than 20 dB at 8.5 GHz and decreases to greater than 19 dB at 10.5 GHz. The S_{12} is always less than -35 dB.

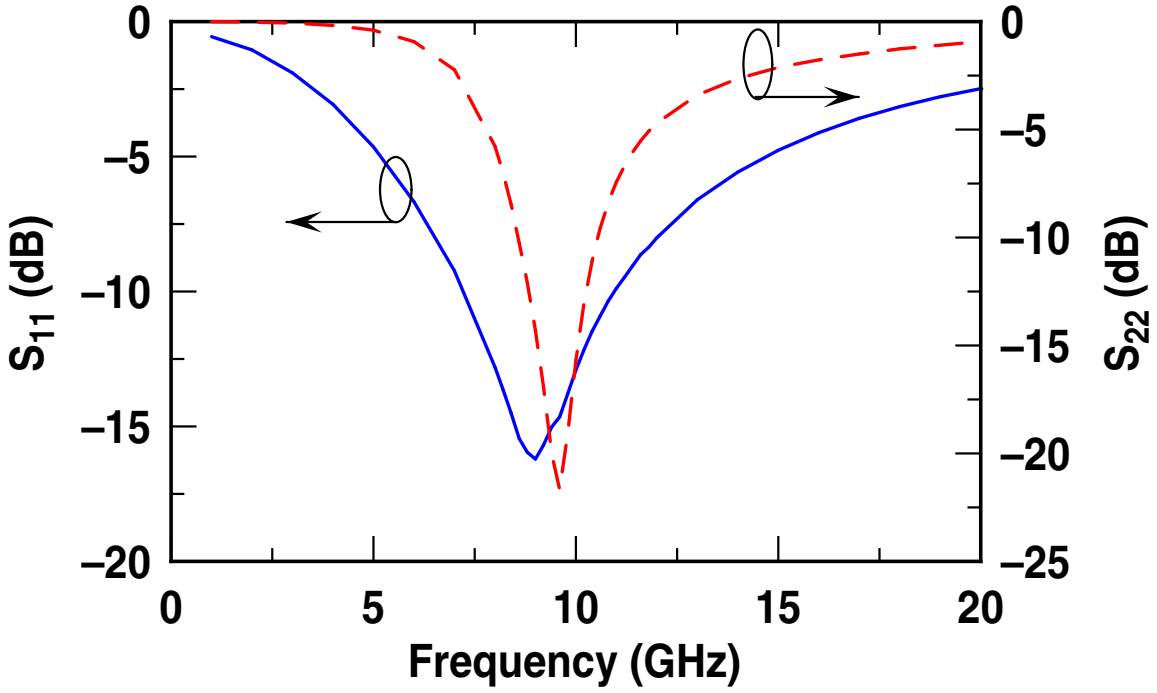


Figure 18: Measured S_{11} and S_{22} (input and output RL) of the ultra-low-noise SiGe HBT LNA.

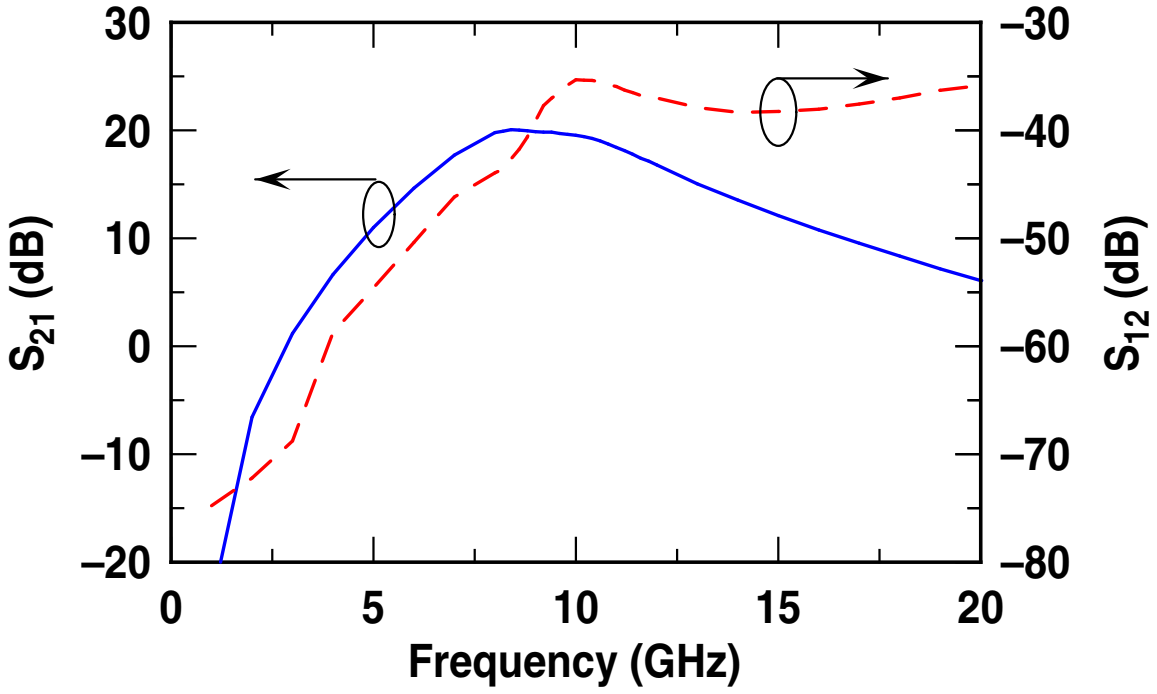


Figure 19: Measured S_{21} and S_{12} (G and isolation) of the ultra-low-noise SiGe HBT LNA.

The LNA noise was measured using an ATN NP5B controller with an Agilent 8970B *NF* meter and 8971C down-converter. Figure 20 shows the measured *NF* and G (S_{21}). The *NF* varies from 1.15 to 1.50 dB across X-band, with a mean *NF* of 1.36 dB.

To evaluate the linearity of the LNA, both 1-dB compression point (P_{1-dB}) and third-order intercept point (IP_3) were measured. Figure 21 shows the LNA power transfer characteristics for a single-tone at 10 GHz. The measured input and output P_{1-dB} (IP_{1-dB} and OP_{1-dB}) were -10.0 and 8.5 dBm, respectively. Figure 22 shows the measured third-order intermodulation (IM_3) product at 9.99 GHz with the fundamental at 10.00 GHz for a two-tone input at 10.00 and 10.01 GHz. The extrapolated input and output IP_3 (IIP_3 and OIP_3) were 0.8 and 20.2 dBm, respectively.

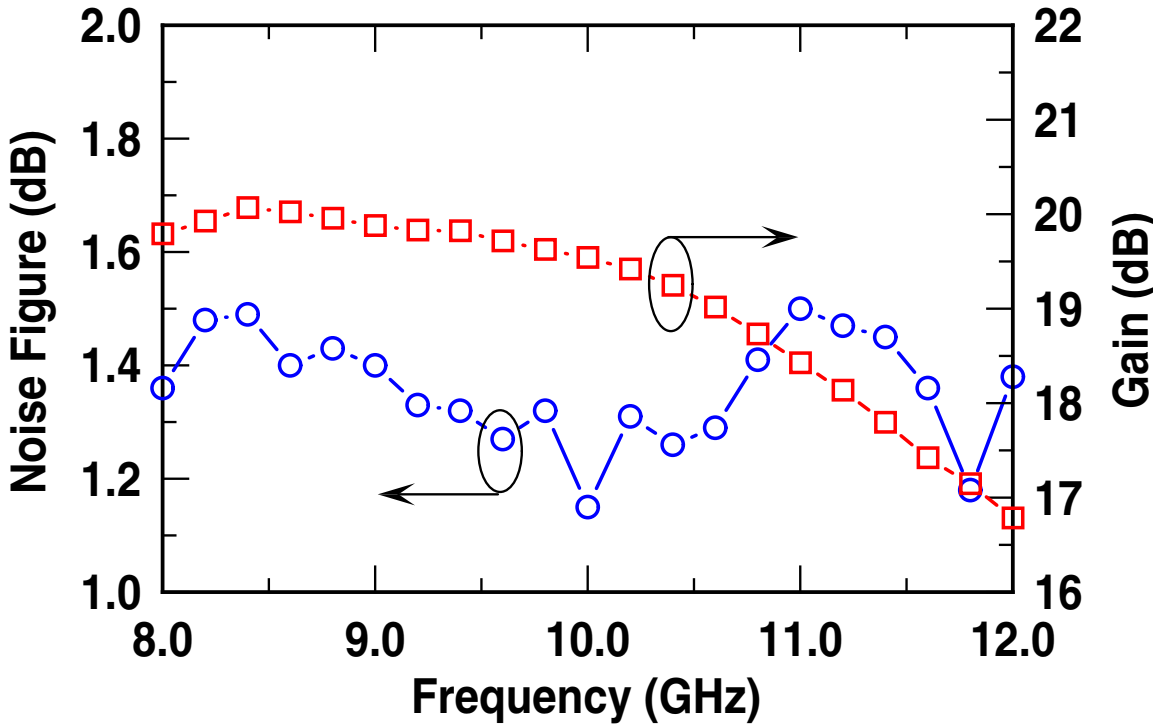


Figure 20: Measured *NF* and *G* of the ultra-low-noise SiGe HBT LNA across X-band.

2.5 Performance Comparison

Numerous LNAs have been published in literature. Comparison of the present LNA to other state-of-the-art SiGe HBT LNAs operating in X-band [56]-[59] is summarized in Table 2. To the best of the author's knowledge, the present LNA achieves the lowest *NF* of any Si-based LNA operating in X-band. The improvement in *NF* is attributed predominantly to the lateral width scaling of the SiGe HBTs.

2.6 Summary

A SiGe HBT LNA with 1.36 dB mean noise figure across X-band has been designed and fabricated in a 0.13 μm, 200 GHz SiGe HBT BiCMOS technology. It exhibits more than 19 dB of *G* from 8.5 to 10.5 GHz, with an IIP_3 of 0.8 dBm at 10 GHz. To the best of the author's knowledge, this LNA achieves a lower *NF* than any other implemented in Si-based technology operating in X-band.

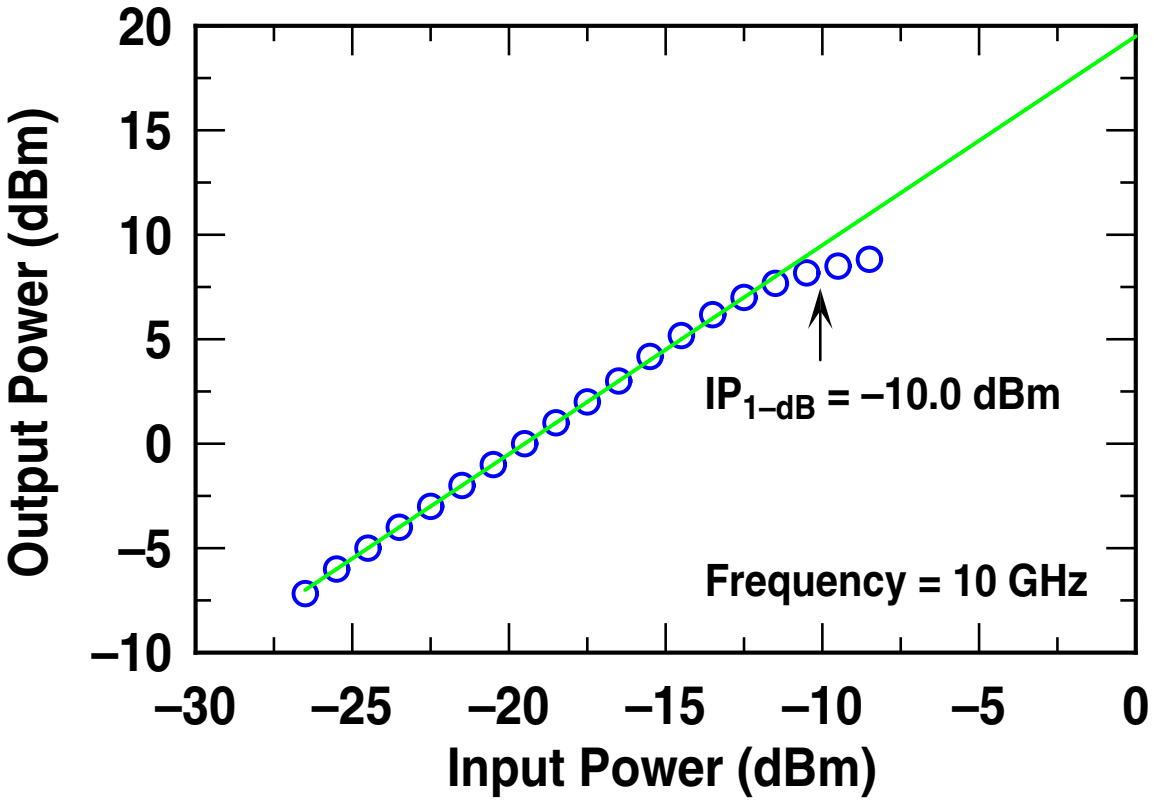


Figure 21: Measured P_{1-dB} (single-tone) of the ultra-low-noise SiGe HBT LNA.

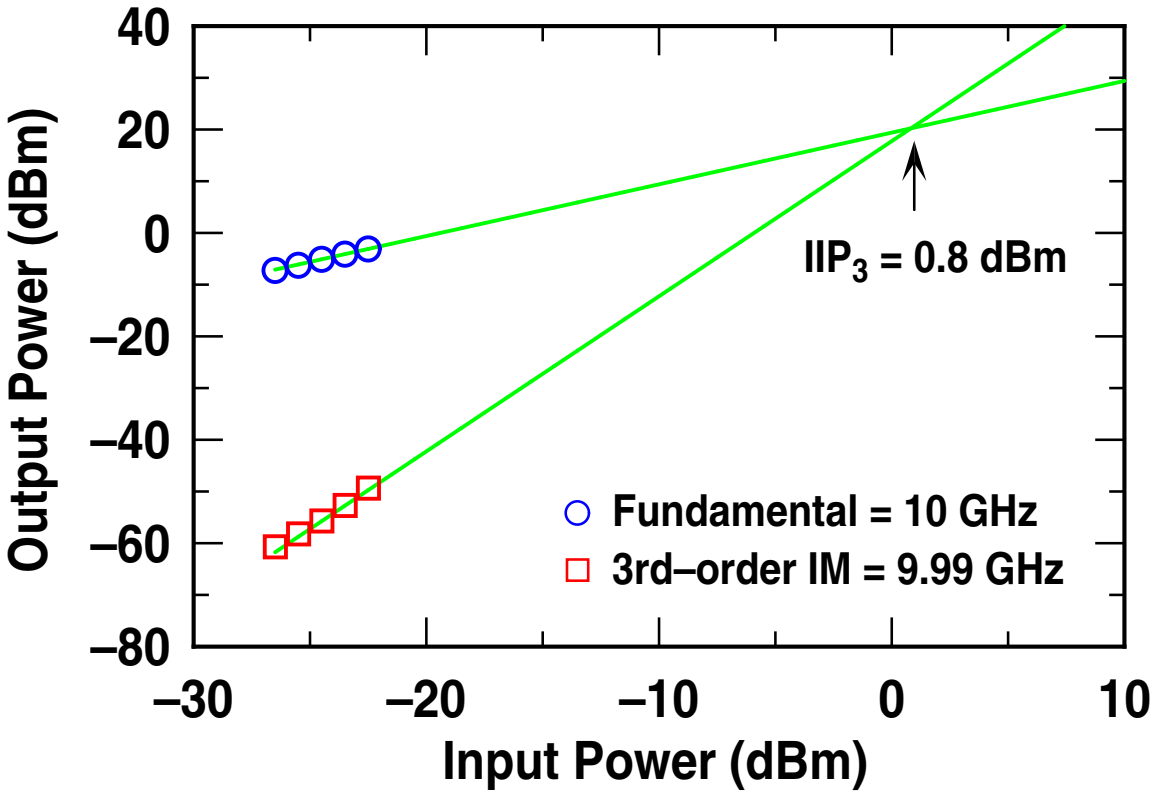


Figure 22: Measured IP_3 (two-tone) of the ultra-low-noise SiGe HBT LNA.

Table 2: Comparison of state-of-the-art SiGe HBT LNAs operating in X-band.

Reference	Frequency [GHz]	NF [dB]	S_{21} [dB]	P_{diss} [mW]	IP_{1-dB} [dBm]	IIP_3 [dBm]	SiGe HBT peak f_T [GHz]
This work	10.0	1.36 mean	19.5	15.0	-10.0	0.8	200
[56]	10.0	1.68	24.2	33.6	-0	-6.7	120
[57]	8.2	1.6	22.0	14.4	-17.7	-	70
[58]	10.5	2.0	26.3	26.6	-	-	80
[59]	10.0	3.3	15.0	43.2	-19.0	-6.8	50

CHAPTER III

THE DESIGN OF LOW-LOSS SHUNT AND SERIES/SHUNT X-BAND SI CMOS SPDT SWITCHES FOR RADAR APPLICATIONS

3.1 Introduction

Next-generation X-band active phased array radar systems aims to reduce both deployment and operational expenses by employing scalable, LPD arrays assembled using low-cost, monolithically integrated T/R modules [25]. A significant challenge for implementing such radar systems is the development of highly efficient T/R modules in an affordable process technology [48]-[50]. SiGe HBT BiCMOS technology is chosen here because it combines III-V like device performance with low-cost Si manufacturing. A key to the successful development of such T/R modules are low-loss microwave power switches, which are clearly challenging to implement on lossy Si substrates.

The initial development of the X-band SiGe HBT LNA was presented in Chapter II and that of the X-band SiGe HBT PS in [60]. Here, another circuit block essential to the envisioned monolithic X-band T/R module is presented: the low-loss SPDT switch. The connections of the SPDT switch ("switch" for short) to other T/R module components are shown in Figure 23. It has a "common port" connected to the PS. The "through port" is connected to the LNA while the "isolated port" is connected to the preamp during receive (RX), and vice versa during transmit (TX). The system specifications require the switch to operate from 8.5 to 10.5 GHz, have an *RL* greater than 12 dB (on connected ports), minimum *IL*, an isolation greater than 20 dB, minimum P_{diss}, and handle the output power of the LNA, which translates to an IP_{1-dB} greater than 8.5 dBm and an IIP_3 greater than

20.2 dBm.

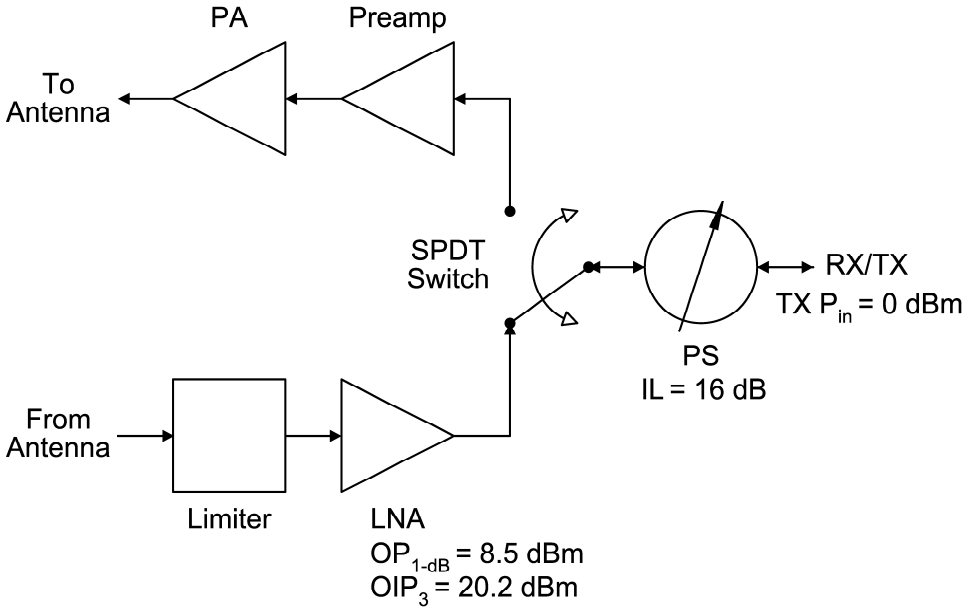


Figure 23: Connection of the SPDT switch to other T/R module components.

In this chapter, two different symmetrical switch topologies with no *dc* power dissipation are designed, implemented, and compared: one is a shunt CMOS switch with $\lambda/4$ sections ("shunt switch" for short), the other is a series/shunt CMOS switch with matching networks ("series/shunt switch" for short). Section 3.2 describes the details of the switch design, and measurement results are presented in Section 3.3. Section 3.4 compares the low-loss switches to other state-of-the-art Si CMOS SPDT switches operating from 5.0 to 15.0 GHz.

3.2 Single-Pole Double-Throw Switch Design

3.2.1 Shunt Switch

A simplified schematic of the shunt switch is shown in Figure 24. The switch operates as follows: When M_1 is "off" and M_2 is "on", the short at P_3 is seen as an open from P_1 through the $\lambda/4$ section at resonance. Thus signal flows from P_1 to P_2, and P_3 is isolated. Only minimum gate length *n*FETs are used because of the lower on-resistance (R_{on}). The

width of the *n*FETs determines the tradeoff between *IL* and isolation. A larger width reduces R_{on} and thus improves isolation, but also increases the off-capacitance (C_{off}), mainly C_{DB}, thus increasing *IL*. Since the "isolated port" is shorted, this switch is of a reflective type.

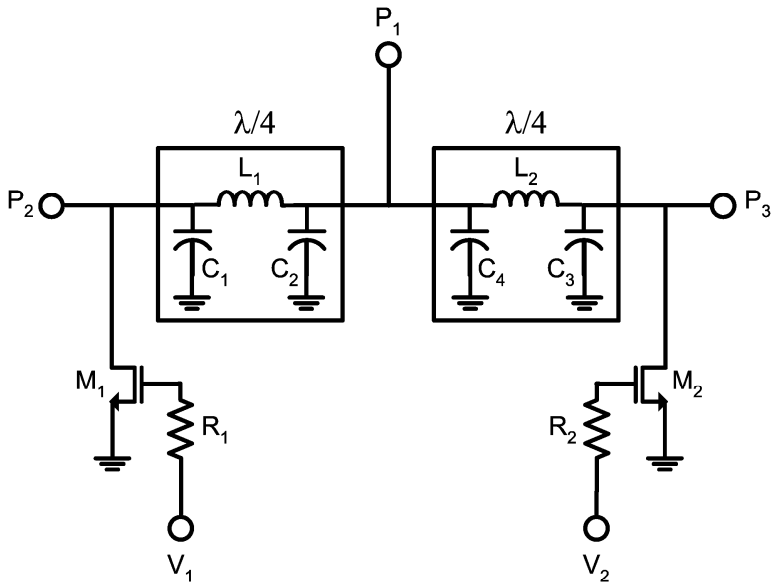


Figure 24: Simplified schematic of the low-loss shunt Si CMOS SPDT switch with $\lambda/4$ sections.

The $\lambda/4$ sections are a *C-L-C* π-network. The values of L and C are easily solved for as

$$L = \frac{Z_o}{2\pi f_o} \tag{10}$$

and

$$C = \frac{1}{2\pi f_o Z_o}, \tag{11}$$

where Z_o is the characteristic impedance and f_o is the center frequency. The pad capacitance and C_{DB} can be absorbed into the capacitors of the π-network.

The gate resistors are added to float the gate of the "off" *n*FET at RF, and hence the gate voltage is determined by the capacitive voltage divider of C_{GD} and C_{GS}. During negative

signal cycles, only a portion of the negative signal appears at the gate, thus increasing the signal level on when the *n*FET turns "on", and hence improves linearity [61]. However, the parasitic drain-body *pn*-junction diode can still turn "on" to distort the signal [62].

3.2.2 Series/Shunt Switch

A simplified schematic of the series/shunt switch is shown in Figure 25. The switch operates as follows: When M_1 and M_4 are "off", and M_2 and M_3 are "on", the signal flows from P_1 to P_2, and P_3 is isolated. The series *n*FETs provide the switching function, and their geometries impact *IL*. A small width results in high R_{on} whereas a large width results in high parasitic capacitance (mainly C_{DB} and C_{SB}), both increasing *IL* [62]. Thus, a width for minimum *IL* exists for the series *n*FETs.

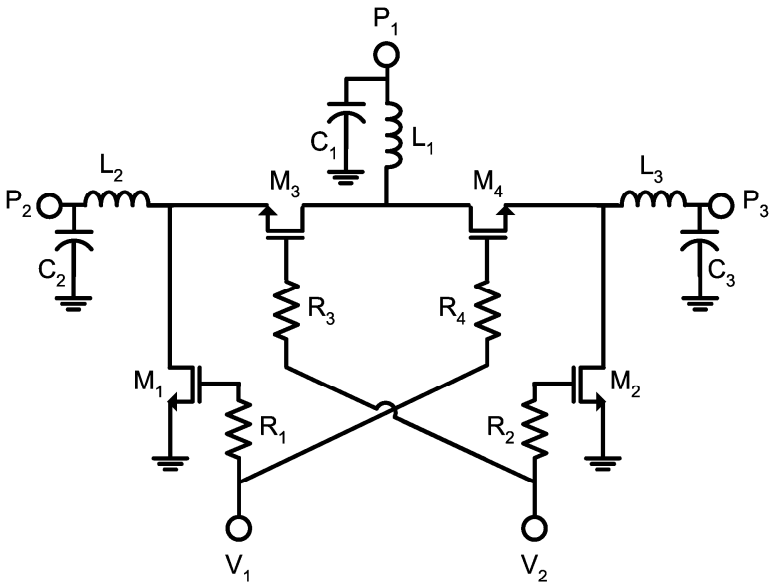


Figure 25: Simplified schematic of the low-loss series/shunt Si CMOS SPDT switch with matching networks.

The shunt *n*FETs improve isolation by shorting the "isolated port." The width of the shunt *n*FETs can be scaled to improve isolation with little increase in *IL*, as well as to provide a match for the "isolated port," resulting in an absorptive type switch.

The matching networks are of series-*L* and shunt-*C* L-network used to improve *RL* at

RF [63]. The pad capacitance can be absorbed into the capacitor of the L-network.

Gate resistors are also added to float the gate of the "on" series *n*FET at RF. The gate voltage, bootstrapped by C_{GD} and C_{GS}, minimizes the gate to channel voltage swing during signal cycles, thus keeping R_{on} nearly constant, and hence improves linearity [61], [62], [64]. However, the parasitic drain/source-body *pn*-junction diode can still turn "on" to distort the signal [62], as in the shunt switch.

3.3 Measurement Results

The switches were designed and fabricated in a commercially available SiGe HBT BiCMOS technology featuring 200 GHz SiGe HBTs, 0.13 μm ASIC compatible 1.2 V CMOS devices, and a full suite of RF passives [43], the very same one used for the ultra-low-noise X-band SiGe HBT LNA described in Chapter II. Even though only *n*FETs were used in the switch designs, the SiGe HBT BiCMOS technology was chosen for the eventual integration with the LNA, PS, preamp, PA, and limiter which utilize the high-performance SiGe HBTs. The core of the shunt switch occupies 520 × 340 μm^2 (1210 × 560 μm^2 including bondpads), as shown in Figure 26. The core of the series/shunt switch occupies 460 × 420 μm^2 (910 × 640 μm^2 including bondpads), as shown in Figure 27.

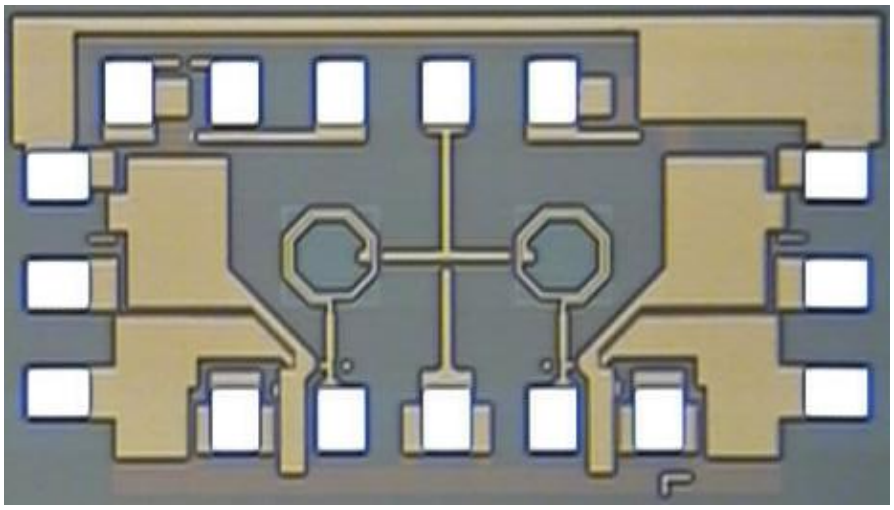


Figure 26: Chip micrograph of the low-loss shunt Si CMOS SPDT switch with λ/4 sections.

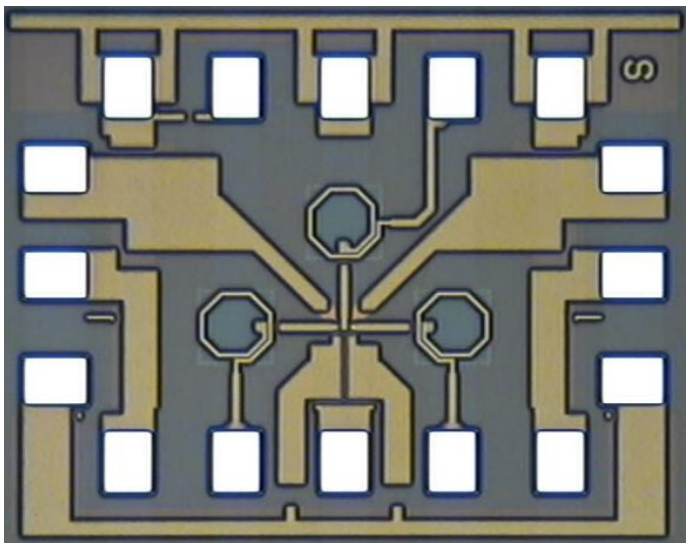


Figure 27: Chip micrograph of the low-loss series/shunt Si CMOS SPDT switch with matching networks.

The switches were measured on-wafer with V_1 set to 0 V and V_2 set to 1.2 V, thus making P_2 the "through port" and P_3 the "isolated port". Figure 28, 29, and 30 compare the measured S_{11}, S_{22} and S_{33}, respectively. The S_{11} (*RL* of P_1) for the shunt switch is less than -12 dB from 7.5 to 12.0 GHz, whereas the S_{11} for the series/shunt switch is less than -13 dB to 20.0 GHz. The S_{22} (*RL* of P_2) for the shunt switch is less than -12 dB from 5.5 to 12.5 GHz, whereas the S_{22} for the series/shunt switch is less than -15 dB to 20.0 GHz. The S_{33} (*RL* of P_3) for the shunt switch is greater than -4 dB to 20.0 GHz, thus indicating a reflective type switch, whereas the S_{33} for the series/shunt switch is less than -15 dB to 20.0 GHz, thus indicating an absorptive type switch.

As shown in Figure 31, the S_{21} (*IL*) for the shunt switch is greater than -2.0 dB from 7.9 to 11.0 GHz with a maximum of -1.78 dB at 9.5 GHz, whereas the S_{21} for the series/shunt switch decreases almost linearly with -0.15 dB/GHz from -1.95 dB at 8.0 GHz to -2.55 dB at 12.0 GHz. As shown in Figure 32, the S_{31} (isolation) for the shunt switch is less than -20 dB above 8.3 GHz, whereas the S_{31} for the series/shunt switch is less than -20 dB to 13.5 GHz.

The measured IP_{1-dB} and IIP_3 were 10.1 and 28.1 dBm, respectively, for the shunt

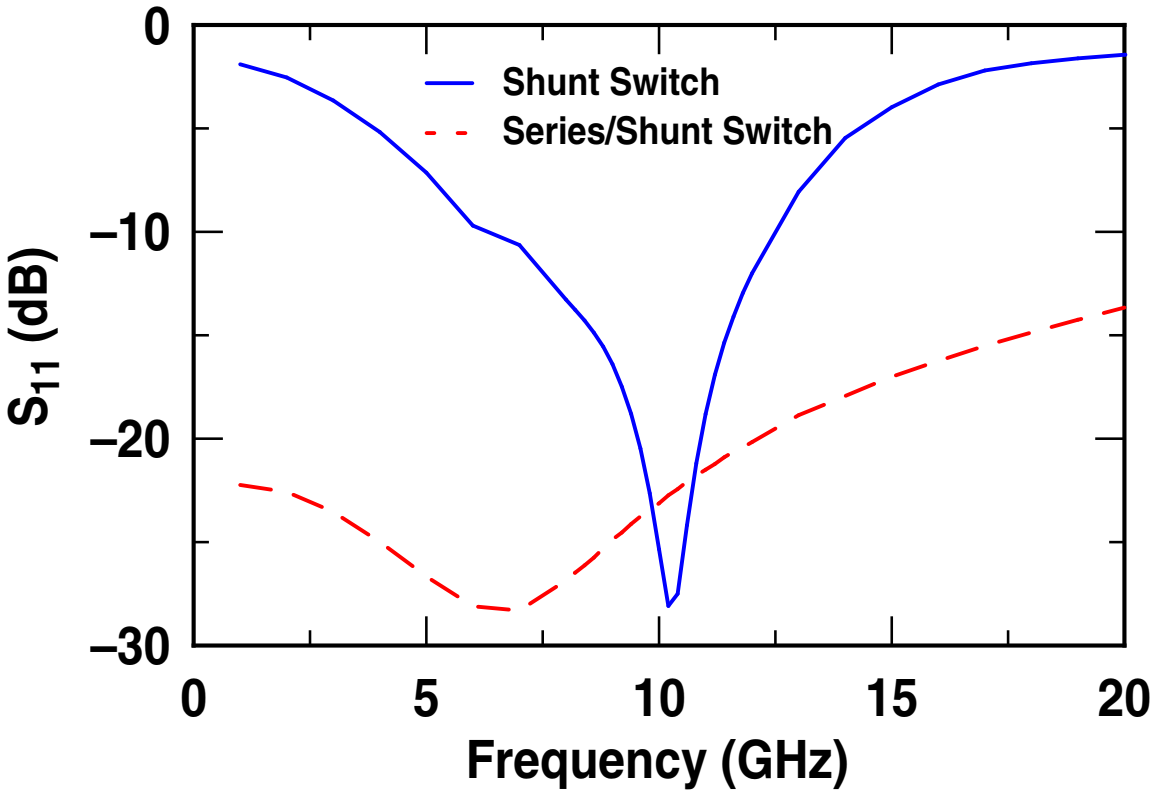


Figure 28: Measured S_{11} (P_1 *RL*) of the low-loss shunt and series/shunt Si CMOS SPDT switches.

switch, as shown in Figure 33, and 11.1 and 27.9 dBm, respectively, for the series/shunt switch, as shown in Figure 34. Both switches exhibit similar linearity characteristics, limited by the turning "on" of "off" *n*FETs and parasitic drain/source-body *pn*-junction diodes.

From Figure 28 to 32, it is clear that the shunt switch has a narrower band of operation. This is caused by the $\lambda/4$ sections of the shunt switch operating at frequencies other than f_o creating mismatch, and hence degrading *RL* and *IL*. Even though the series/shunt switch has a wider band of operation, the isolation and *IL* still degrades with increasing frequency. This is caused by the feed-through of RF signals via the parasitic capacitances of the "off" *n*FETs, as well as capacitive loss to the body as frequency increases. The performance of the present switches are summarized in Table 3. Both switches met all the target requirements.

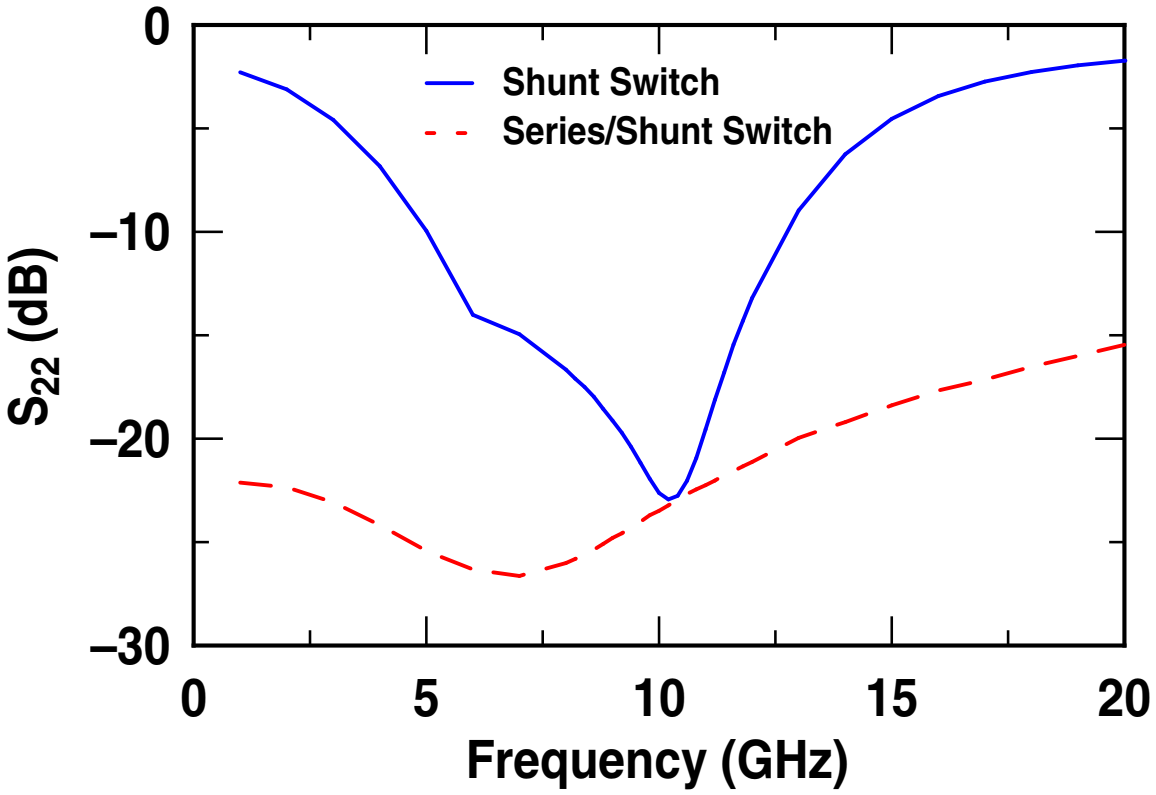


Figure 29: Measured S_{22} (P_2 *RL*) of the low-loss shunt and series/shunt Si CMOS SPDT switches.

3.4 Performance Comparison

Benchmarking of the present switches to other state-of-the-art 5.0 to 15.0 GHz Si CMOS SPDT switches is summarized in Table 4. The performance of the designed switches are comparable to other Si CMOS SPDT switches found in triple well technologies [65], on non-standard substrates [61], using special device structures [66], using extra *dc* biases [63], [67], or using asymmetrical designs [64] to improve performance.

3.5 Summary

Low-loss shunt and series/shunt Si CMOS SPDT switches were implemented in a 0.13 μm, 200 GHz SiGe HBT BiCMOS technology for next-generation X-band phased array radar T/R modules using only standard *n*FETs. Both switches met the target design requirements. The switches performed as well as other published Si CMOS SPDT switches

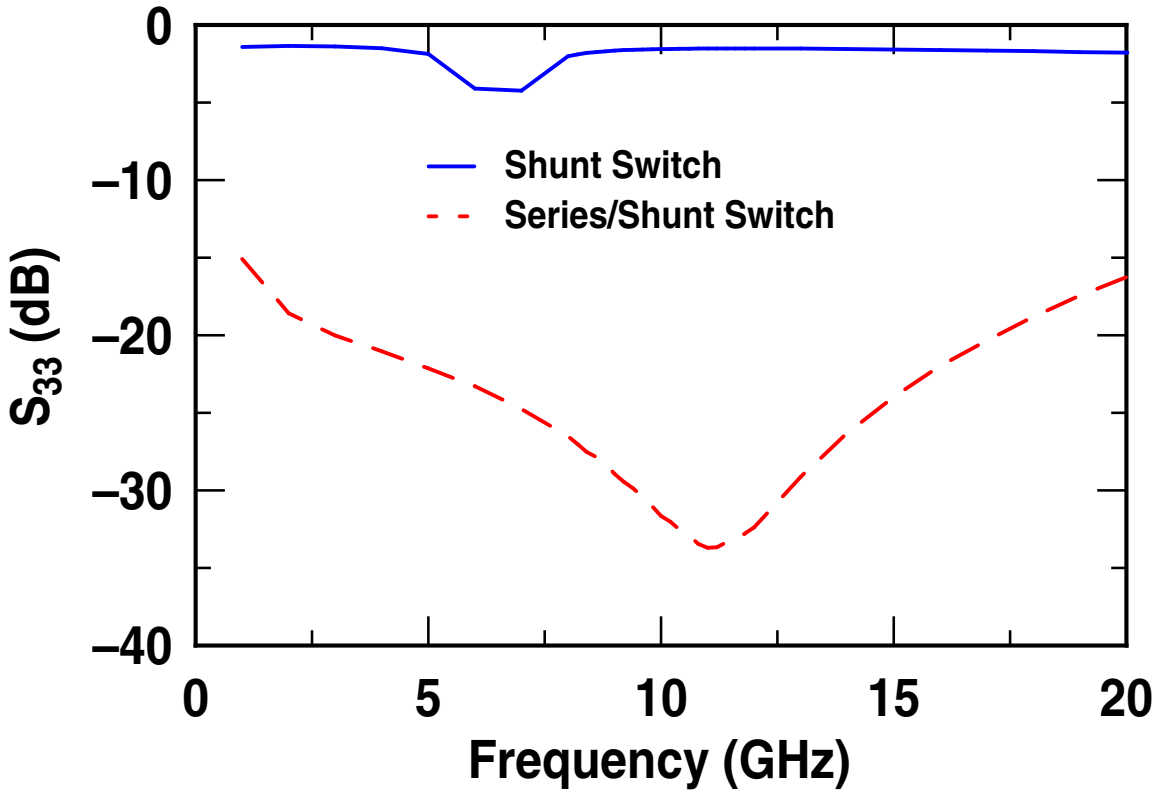


Figure 30: Measured S_{33} (P_3 RL) of the low-loss shunt and series/shunt Si CMOS SPDT switches.

using more complicated designs or non-standard processes.

Table 3: Performance summary of the low-loss shunt and series/shunt Si CMOS SPDT switches.

	Target	Shunt	Series/Shunt
Freq. [GHz]	8.5-10.5	8.5-10.5	8.5-10.5
Type	-	Reflective	Absorptive
RL [dB]	> 12	> 14.5	> 22.2 (all ports)
IL [dB]	Minimum	< 1.89	< 2.33
Isolation [dB]	> 20	> 20.5	> 22.5
IP_{1-dB} [dBm]	> 8.5	10.1 (at 10 GHz)	11.1 (at 10 GHz)
IIP_3 [dBm]	> 20.2	28.1 (at 10 GHz)	27.9 (at 10 GHz)
P_{diss} [mW]	Minimum	0	0

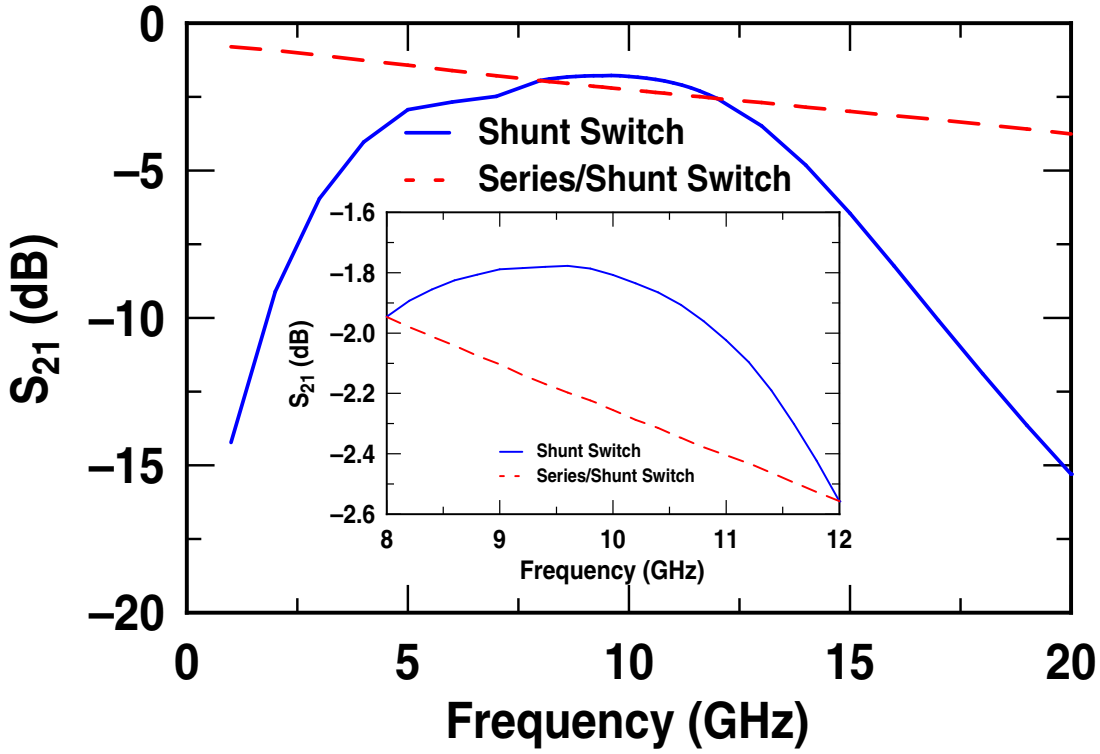


Figure 31: Measured S_{21} (IL) of the low-loss shunt and series/shunt Si CMOS SPDT switches.

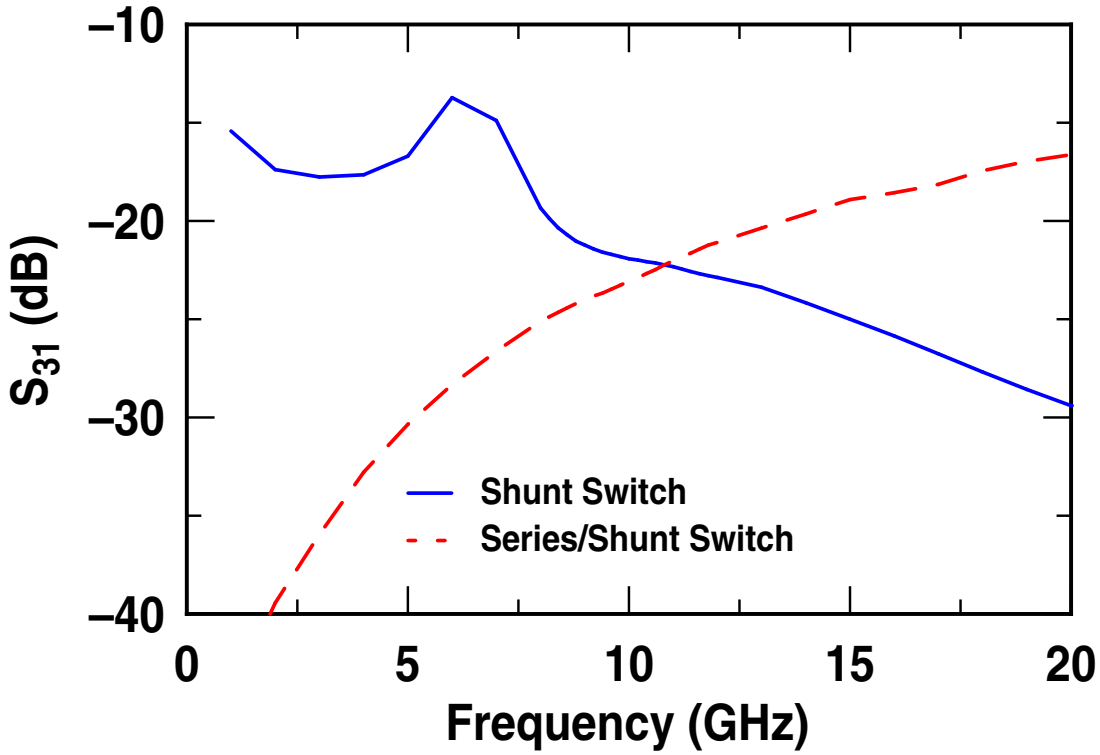


Figure 32: Measured S_{31} (isolation) of the low-loss shunt and series/shunt Si CMOS SPDT switches.

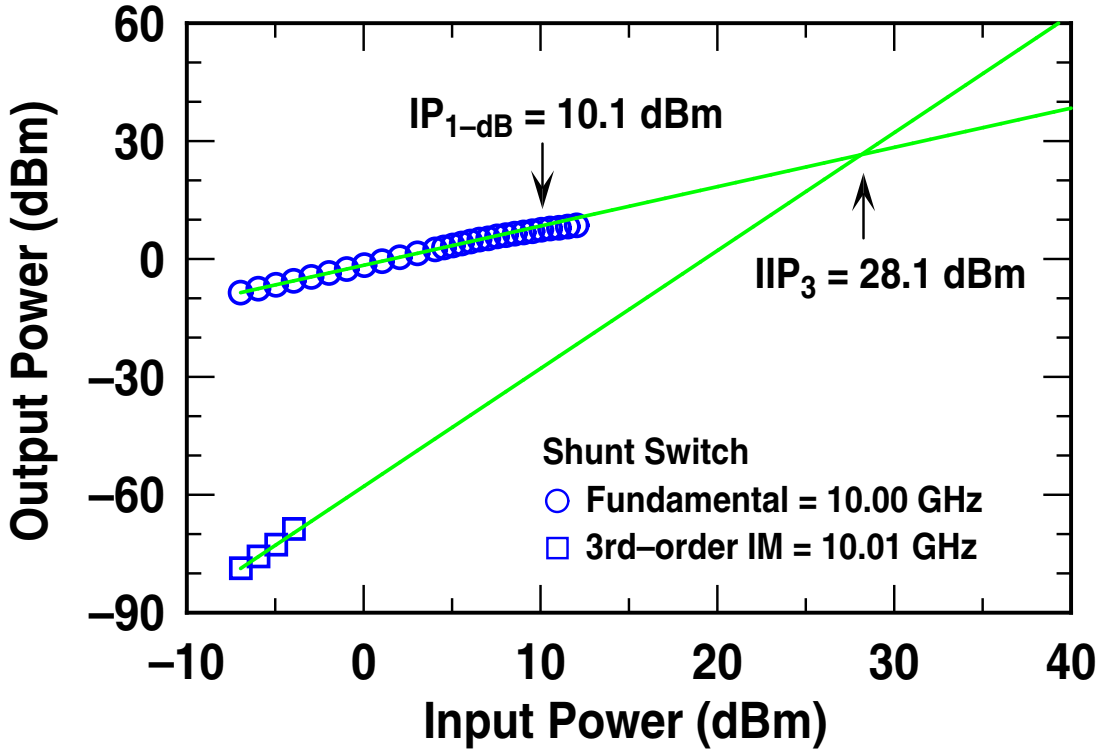


Figure 33: Measured linearity (P_{1-dB} and IP_3) of the low-loss shunt Si CMOS SPDT switch.

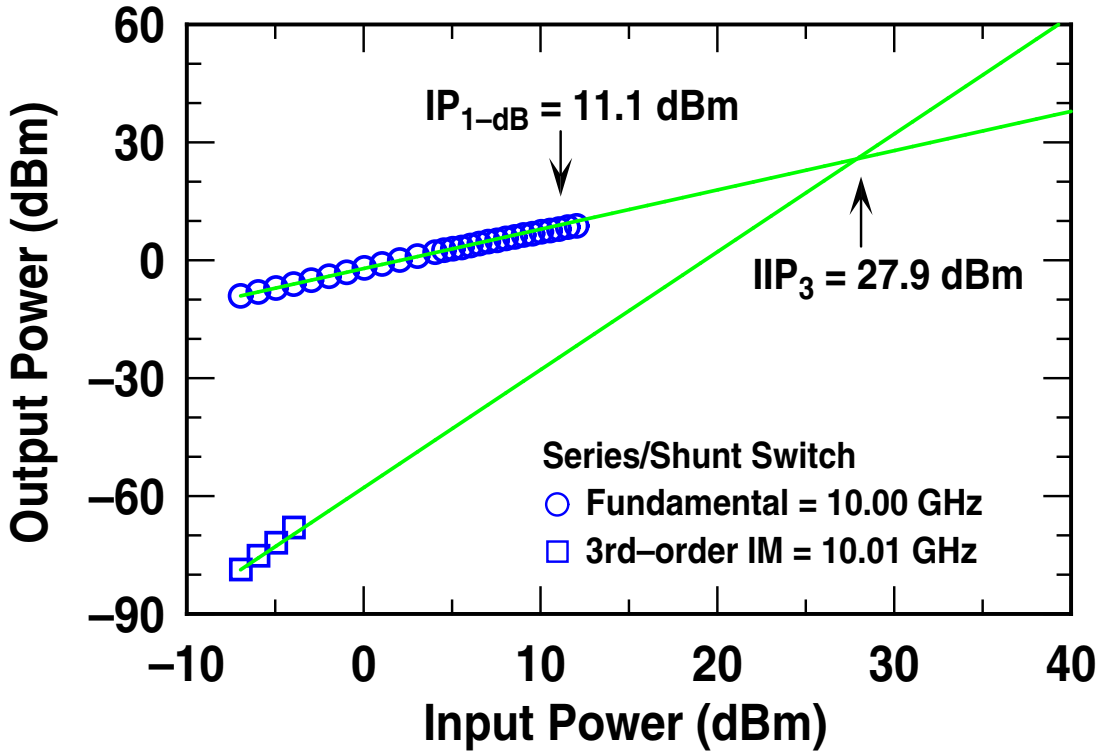


Figure 34: Measured linearity (P_{1-dB} and IP_3) of the low-loss series/shunt Si CMOS SPDT switch.

Table 4: Comparison of state-of-the-art 5.0 to 15.0 GHz Si CMOS SPDT switches.

Reference	Freq. [GHz]	*RL*: $P_1/P_2/P_3$ [dB]	*IL* [dB]	Isolation [dB]	IP_{1-dB} [dBm]	IIP_3 [dBm]	P_{diss} [mW]	V_{dc} [V]	Process Technology
Shunt	10.0	25.3/22.6/1.5	1.81	21.9	10.1	28.1	0	1.2	0.13 μm BiCMOS*
Series/Shunt	10.0	23.1/23.4/31.6	2.25	23.1	11.1	27.9	0	1.2	0.13 μm BiCMOS*
[63]	15.0	24/12.5/-	1.8	17.8	21.5	34.5	0	1.2/1.8/3.0	0.13 μm CMOS
[67]	5.825	-/-/-	0.8	29	17	33	0	1.3/1.8/3.6	0.18 μm CMOS
[65]	5.8	13.2/13.4/-	1.1	27	20	25.5	0	-1.8/1.8	0.18 μm Triple Well CMOS
[64]	5.2	TX: 30/-/33	1.52	30	28.0	-	< 1	1.8	0.18 μm CMOS
		RX: 11/25/-	1.42	15	11.5	-	0		
[66]	5.0	TX: -/-/21.0	0.95	26.3	22.7	-	0	1.0/2.8	0.18 μm CMOS with DETs
		RX: -/17.1/-	1.44	22.2	18.4	-	0		
[61]	5.0	-/-/-	1.56	33	12	-	0	2.5	0.25 μm CMOS SOI

* Only standard *n*FETs were used. The 0.13 μm, 200 GHz SiGe HBT BiCMOS technology was chosen for eventual integration with LNA, PS, and preamp.

CHAPTER IV

THE DESIGN OF LOW-POWER X-BAND SIGE HBT LNA FOR NEAR-SPACE RADAR APPLICATIONS

4.1 Introduction

The need for persistent global tactical surveillance and intelligence reconnaissance is driving the demand for near-space (e.g., airship) radar development [68]-[70]. Airship-based radar systems operate at near-space altitudes (e.g., 70,000 feet), and can provide continuous ground and airborne moving target indication for a year or more without refueling [68]-[70]. Due to limited prime power, LPD phased array radar designs are favored over high-power ones, where large numbers of antenna elements are used to improve search-and-track capabilities instead of increasing the output power of each transmitter [69], [70]. Each radar element must also be highly power-efficient, extremely light-weight, and relatively low-cost, since many thousands of these elements are assembled together, deployed in near-space, and operated continuously [69], [70]. These demands place very stringent requirements on the T/R modules of airship-based radar. A key challenge of such radars is, once again, the development of highly integrated, highly efficient, T/R modules in an affordable IC technology platform.

Given the unique properties of SiGe HBT BiCMOS technology, it may in fact be an ideal choice for implementing airship-based radar modules, given its low-cost and high-level of maturity compared to antimonide-based compound semiconductor (ABCS) technologies currently being developed for such applications.

This chapter presents the design and implementation of an essential component in such an airship-based radar T/R module: a low-power X-band SiGe HBT LNA. The SiGe HBT

BiCMOS technology used to fabricate the LNA is discussed in Section 4.2. Section 4.3 describes the details of the low-power LNA design. Measurement results are presented in Section 4.4. Section 4.5 compares the low-power LNA to other state-of-the-art SiGe HBT LNAs operating in X-band.

4.2 SiGe HBT BiCMOS Technology

A state-of-the-art complementary SiGe HBT BiCMOS technology, featuring both *npn* and *pnp* SiGe HBTs with f_T/f_{max} of 180/185 GHz and 80/120 GHz, respectively, is used to implement the low-power LNA [44]. It provides four levels of aluminum interconnects with the top layer being a thick metal, a full suite of RF passive elements including MIM capacitors and spiral inductors, and a complete set of 0.25 μm digital CMOS devices.

A key feature of the complementary SiGe HBT BiCMOS technology is the formation of the whole *npn*/*pnp* SiGe HBT structure in one active area without shallow trench isolation between the active emitter and the collector contact region. This provides low-capacitance isolation from the substrate, and low collector resistances for both types of transistors. The performance gain of the *pnp* SiGe HBTs is mainly due to a highly tuned vertical doping profile taking full advantage of the reduced phosphorus diffusion in the carbon-doped base. Schematic cross section of the *npn* and *pnp* SiGe HBTs are shown in Figure 35.

4.3 Low-Power LNA Design

The primary goal of this work is to minimize P_{diss} (< 3 mW) of a SiGe HBT LNA operating from a 2.5 V system, while simultaneously maintaining sufficiently low *NF* (< 3 dB) at 10 GHz. A cascode LNA topology, shown in Figure 36, is again chosen for reasons discussed in Chapter II. The design of minimum *NF* cascode LNAs has been examined extensively [51]-[55]. This design methodology is modified here for low-power performance.

After $J_{C,opt}$ at minimum NF_{min} is determined for the cascode Q_1 and Q_2 transistors (using emitter geometries of 0.21 × 0.84 × 8 μm^2 as a unit cell), the number of unit cells

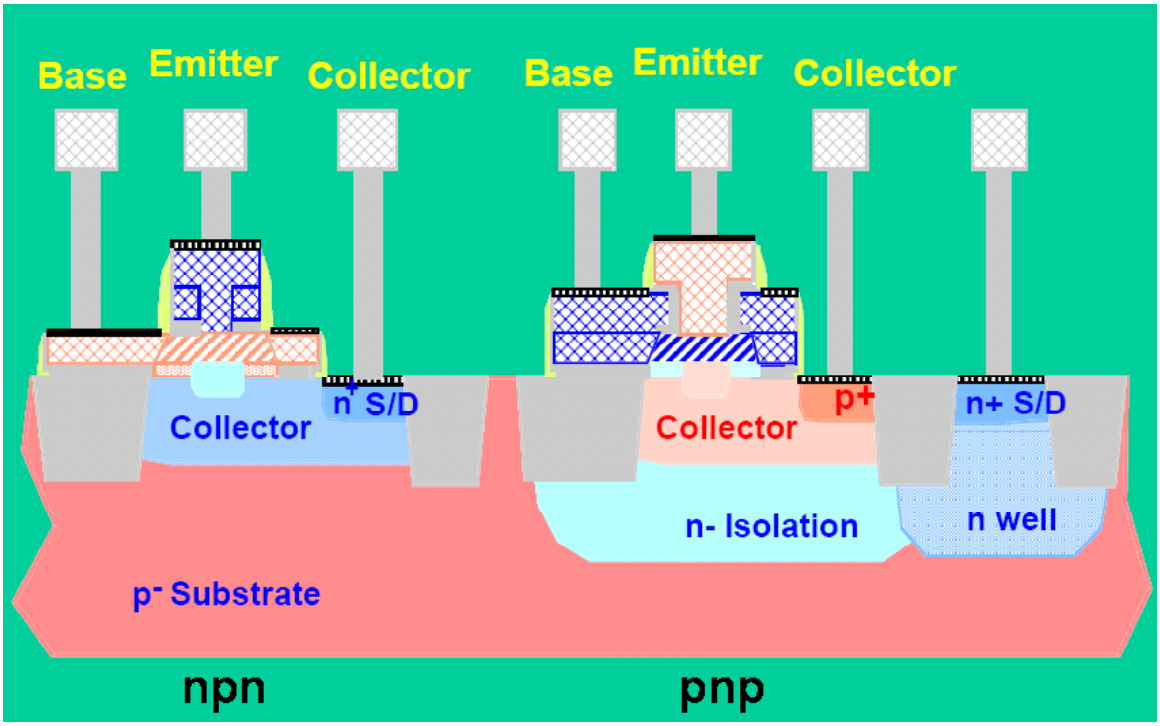


Figure 35: Schematic cross section of the complementary *npn* and *pnp* SiGe HBTs.

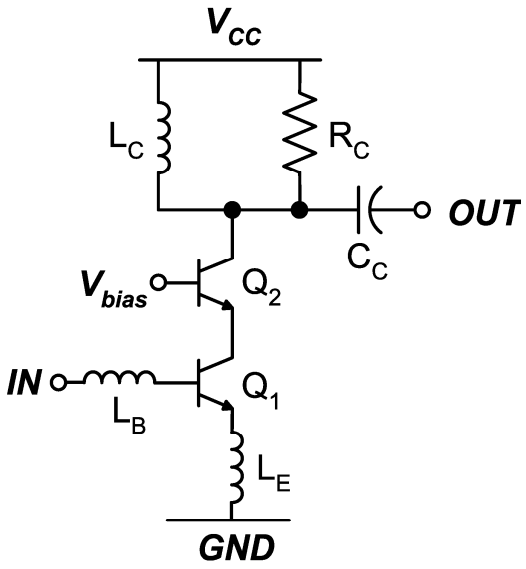


Figure 36: Simplified schematic of the low-power SiGe HBT LNA.

(M) used in parallel is set to the largest integer multiple of the unit cell emitter length (l_e = 0.84 × 8 μm) that is smaller than the overall l_e with an optimum source resistance ($R_{S,opt}$)

of 50 Ω, while still maintaining $J_{C,opt}$, as shown in Figure 37. $R_{S,opt}$ is given as [51]

$$R_{S,opt} \cong \frac{R_n f_T}{f} \frac{1}{\sqrt{\frac{I_C}{2V_T}(r_e + r_b)\left(1 + \frac{f_T^2}{\beta f^2}\right) + \frac{f_T^2}{4\beta f^2}}} \tag{12}$$

where

$$R_n \cong \frac{V_T}{2I_C} + (r_e + r_b) \sim \frac{1}{l_e} \tag{13}$$

is the noise resistance, f is the operation frequency, I_C is the collector current, V_T is the thermal voltage, r_e is the emitter resistance, r_b is the base resistance, and β is the current gain. This design approach differs from a minimum *NF* design methodology, where $R_{S,opt}$ is set to or near 50 Ω for noise match, thus, effectively determining l_e and I_C. Given the inverse relation of $R_{S,opt}$ to l_e at $J_{C,opt}$, a decrease in l_e from 25.54 μm (at an $R_{S,opt}$ of 50 Ω) to 20.16 μm (with an M of 3) results in an increase of $R_{S,opt}$ to 63 Ω with a corresponding decrease in I_C from 5.17 to 4.08 mA.

However, it is important to have an $R_{S,opt}$ of 50 Ω for the LNA, since the system impedance of a T/R module is typically 50 Ω. At a fixed l_e, $R_{S,opt}$ is directly related to I_C for small I_C, and inversely related to I_C for large I_C, as indicated by Equation 12 and 13. The maximum $R_{S,opt}$ occurs when I_C is equal to the $I_{C,opt}$ at minimum NF_{min}. The $R_{S,opt}$ and NF_{min} for an l_e of 20.16 μm as a function of I_C are shown in Figure 38, with the maximum $R_{S,opt}$ of 63 Ω occurring at an I_C of 4.08 mA, which is also the $I_{C,opt}$ for the given l_e. Thus, there are two options for matching $R_{S,opt}$ to 50 Ω: one with an I_C larger than $I_{C,opt}$, the other with an I_C smaller than $I_{C,opt}$. For low-power applications, choosing the latter helps reduce power dissipation. This choice results in a reduction of I_C from 4.08 to 1.00 mA, with a corresponding increase in NF_{min} from 1.09 to 1.60 dB. In effect, NF_{min} is traded for P_{diss}. Here, a 76% reduction in P_{diss} is achieved with a 0.51 dB increase in NF_{min}. The procedure for minimum *NF*, cascode LNA design [51]-[55] can now be used for input and output impedance matching.

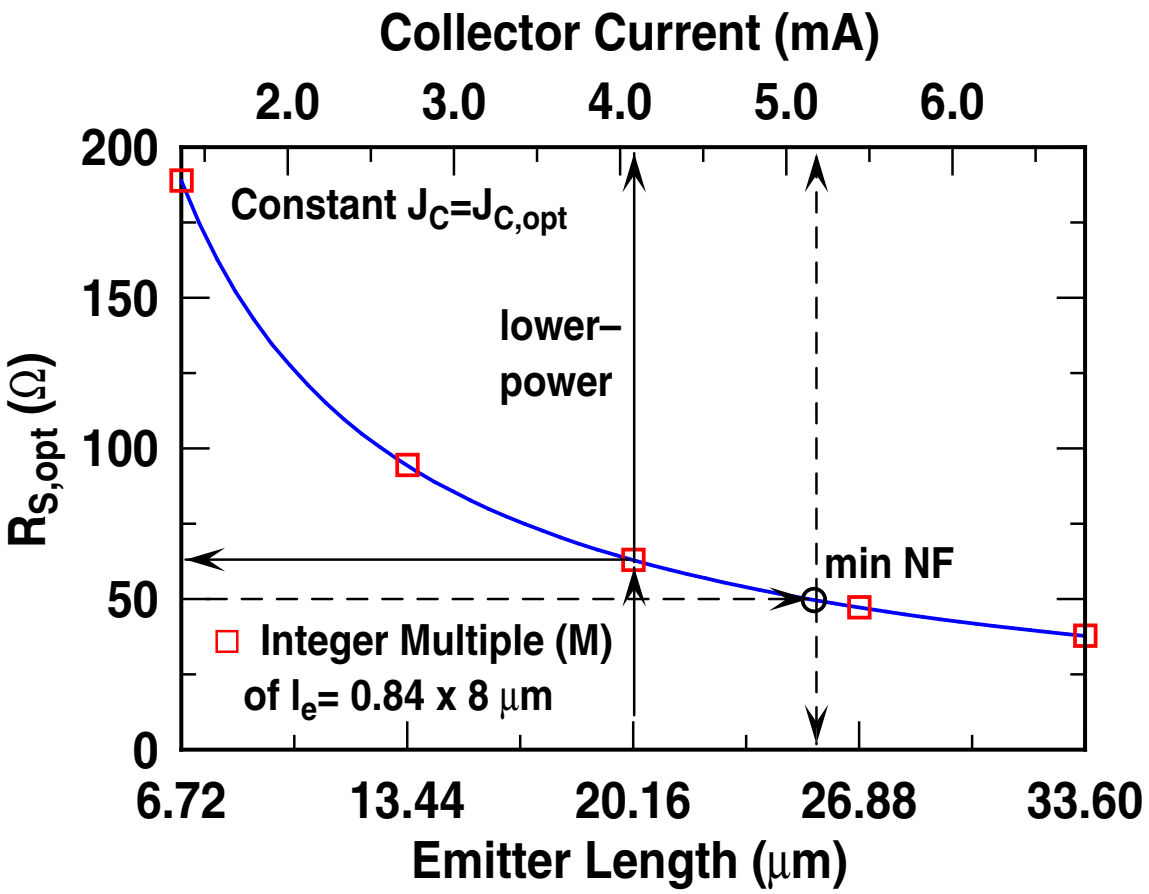


Figure 37: Simulated $R_{S,opt}$ versus l_e of cascode Q_1 and Q_2 biased at $J_{C,opt}$.

4.4 Measurement Results

Even though a complementary SiGe HBT BiCMOS technology was used to fabricate the LNA, only 180 GHz *npn* SiGe HBTs were utilized in the low-power LNA. Custom spiral inductors and transmission lines were designed for the LNA using Agilent Momentum. Figure 39 shows the chip micrograph of the low-power SiGe HBT LNA. The total die area is 780 × 660 μm^2, including bondpads.

Measured on-wafer with a 2.5 V supply, the LNA draws 1.0 mA, and thus dissipates 2.5 mW. Figure 40 shows the measured *S* parameters and *NF*. The measured S_{11} (input *RL*) is less than -10 dB from 9.4 to 11.6 GHz, the S_{22} (output *RL*) is less than -10 dB from 8.8 to 9.8 GHz, and the S_{21} (*G*) is greater than 10 dB from 8.6 to 10.2 GHz. The S_{12} (isolation),

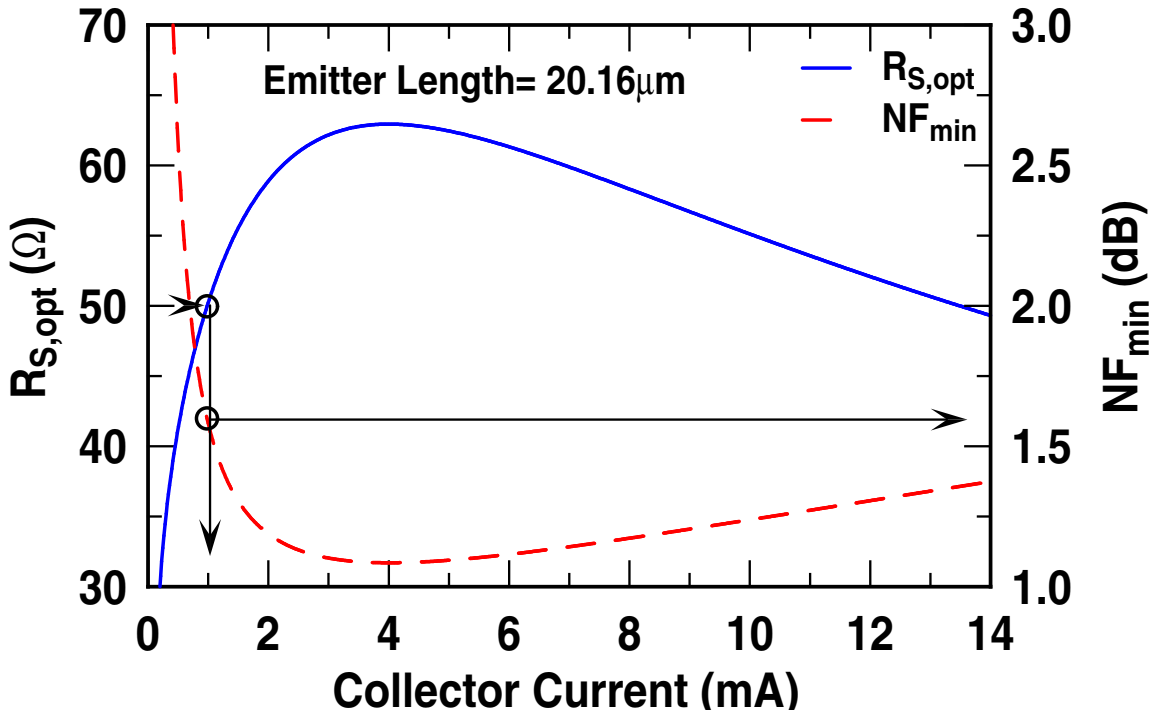


Figure 38: Simulated $R_{S,opt}$ and NF_{min} versus I_C of cascode Q_1 and Q_2 with an l_e of 20.16 μm.

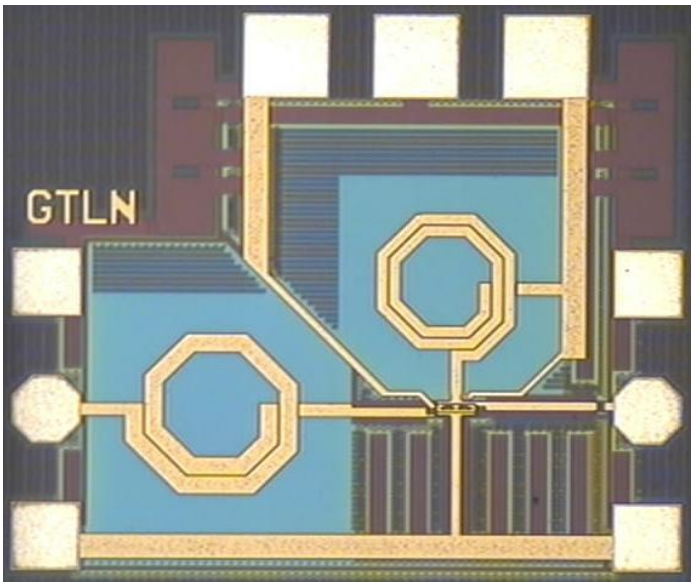


Figure 39: Chip micrograph of the low-power SiGe HBT LNA.

not shown, is always less than -32 dB. The *NF* varies from 2.48 to 3.20 dB across X-band, with a mean of 2.78 dB. The measured IIP_3, shown in Figure 41, is -9.1 dBm for a two-tone

input at 9.50 and 9.51 GHz.

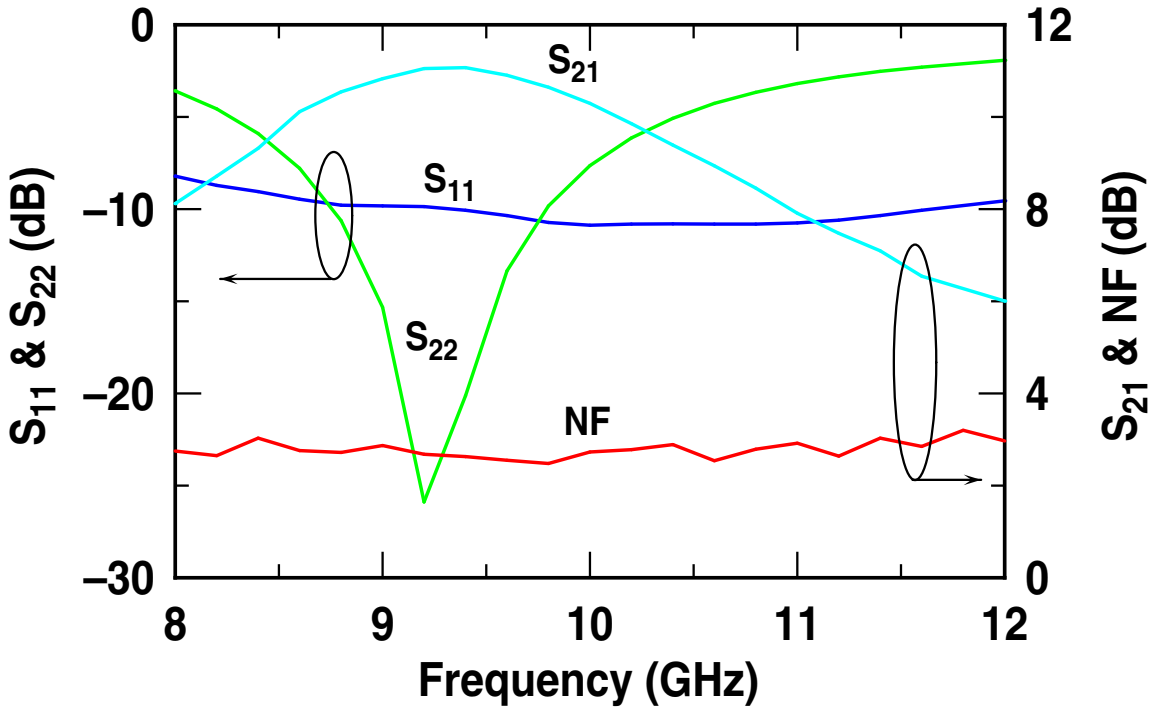


Figure 40: Measured S_{11}, S_{22}, S_{21}, and *NF* of the low-power SiGe HBT LNA.

Figure 42 shows the measured S_{21}, *NF*, and IIP_3 as I_C is increased. Biased for minimum *NF*, the LNA exhibits an S_{21} of 19.7 dB at 9.5 GHz, a mean *NF* of 2.10 dB across X-band, and an IIP_3 of -7.0 dBm near 9.5 GHz while drawing 4.35 mA from a 2.5 V supply. A 77% reduction in P_{diss} with a 0.68 dB increase in *NF* is in close agreement to that predicted in the Section 4.3 when the LNA is biased for normal, low-power operation at 1.0 mA.

4.5 Performance Comparison

To compare the present LNA to other state-of-the-art SiGe HBT LNAs operating in X-band, LNA *FOM*s were determined according to

$$FOM_1 = \frac{S_{21}[dB]}{P_{diss}\,[mW]} \tag{14}$$

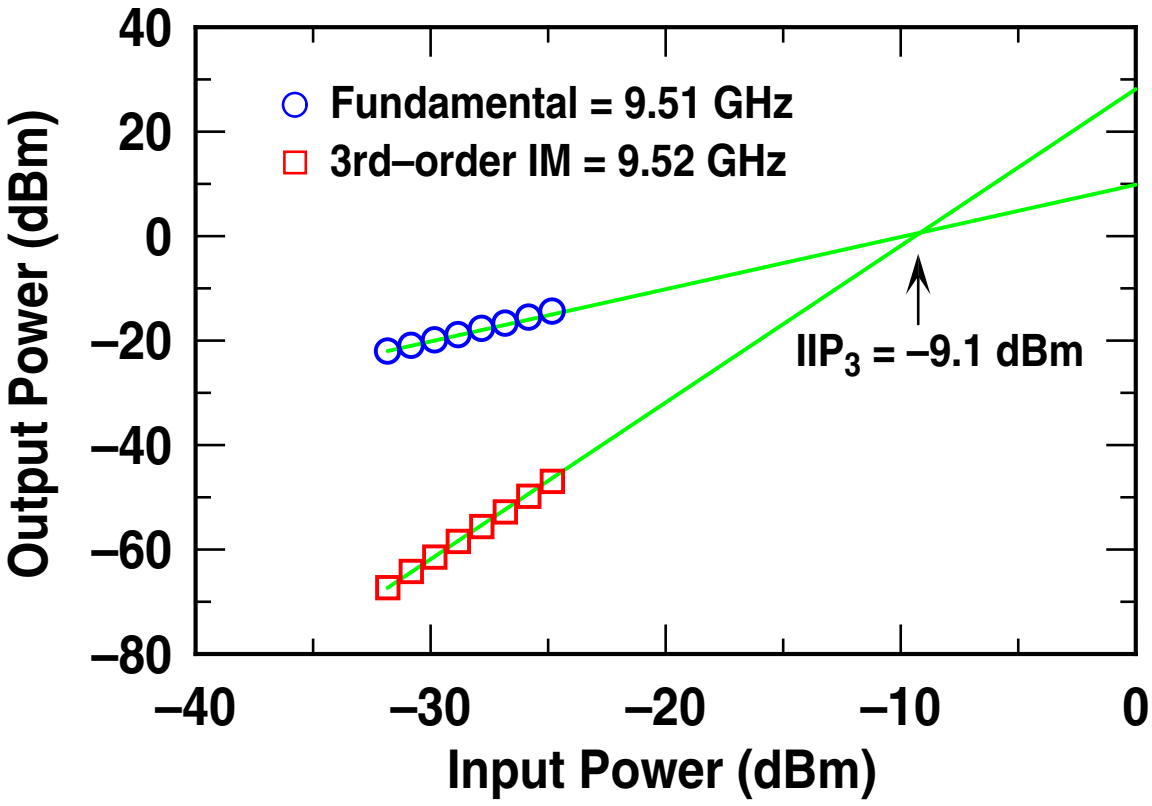


Figure 41: Measured IP_3 of the low-power SiGe HBT LNA.

and

$$FOM_2 = \frac{S_{21}\,[abs]}{(NF\,[abs] - 1) \cdot P_{diss}\,[mW]}. \tag{15}$$

The comparisons are summarized in Table 5, with a higher *FOM* being better in both cases. The present LNA achieves the highest FOM_1 and the third highest in FOM_2 while dissipating only 2.5 mW.

Given that total ionizing dose radiation is a key system-level reliability concern for near-space radar applications, it is also important to note that SiGe HBTs have a proven multi-Mrad built-in (i.e., free) radiation tolerance, giving it a potentially attractive advantage over other technology platforms [71].

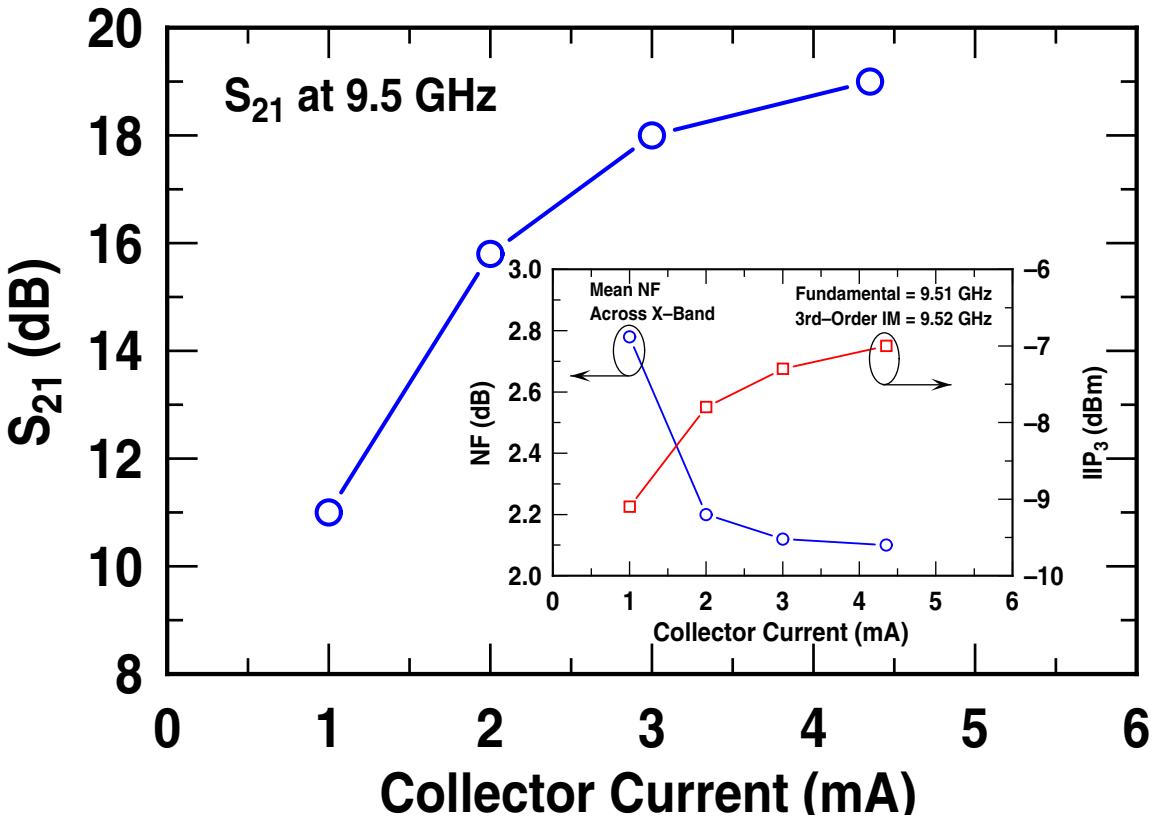


Figure 42: Measured S_{21}, NF, and IIP_3 of the low-power SiGe HBT LNA as a function of I_C.

4.6 Summary

A 2.5 mW X-band SiGe HBT LNA has been demonstrated. The LNA exhibits an S_{21} of 11.0 dB at 9.5 GHz, a mean NF of 2.78 dB across X-band, and an IIP_3 of -9.1 dBm near 9.5 GHz. The performance of the LNA, together with its natural total-dose radiation immunity, demonstrates the potential of SiGe HBT BiCMOS technology for near-space radar applications.

Table 5: Comparison of state-of-the-art SiGe HBT LNAs operating in X-band.

Reference	Frequency	NF	S_{21}	P_{diss}	IIP_3	SiGe HBT peak f_T	FOM_1	FOM_2
	[GHz]	[dB]	[dB]	[mW]	[dBm]	[GHz]	[dB/mW]	[1/mW]
This work	9.5	2.78 mean	11.0	2.5	-9.1	180	4.40	1.58
[1]	10.0	1.36 mean	19.5	15.0	0.8	200	1.30	1.71
[56]	10.0	1.68	24.2	33.6	-6.7	120	0.72	1.02
[57]	8.2	1.6	22.0	14.4	-	70	1.53	1.96
[58]	10.5	2.0	26.3	26.6	-	80	0.99	1.33
[59]	10.0	3.3	15.0	43.2	-6.8	50	0.35	0.11

CHAPTER V

THE DESIGN OF INDUCTORLESS SIGE HBT RING OSCILLATORS FOR MMW OPERATION

5.1 Introduction

Due to their design simplicity, inherent multi-phase output, wide frequency tuning capability, compact size, and ease of integration, ring oscillators are now essential building blocks in high-speed digital and optical communication systems. In spite of this, ring oscillators have yet to find many applications in the MMW range because of the high frequency and stringent phase noise requirements. Hence, oscillators for MMW applications have traditionally been implemented as harmonic oscillators using an *LC* tank with a high-Q as the resonator. However, with the large area required for inductors, the limited frequency tuning range of *LC* oscillators, and the trend towards very large scale integration (VLSI), inductorless ring oscillators remain logical alternatives. Research into high-performance devices and novel circuit topologies to overcome the limitations of inductorless ring oscillators has yielded several designs with high operating frequency [72]-[75]. Still, the proposed oscillators [72]-[75] are limited only to K-band (18 to 26 GHz) operation.

This chapter presents the design and implementation of an inductorless SiGe HBT ring oscillator capable of MMW operation. The 0.18 μm, 120 GHz SiGe HBT BiCMOS technology used to fabricate the oscillator is discussed in Section 5.2. Section 5.3 reviews the operating principles of ring oscillators, while Section 5.4 describes the details of the inductorless SiGe HBT ring oscillator design for MMW operation. Measurement results of the ring oscillator are presented in Section 5.5. Section 5.6 compares the present oscillator to other state-of-the-art inductorless ring oscillators operating in a similar frequency range.

The oscillator, optimized for high-frequency operation, low-power consumption, and ultra-compact size, demonstrates the potential of inductorless SiGe HBT ring oscillators for MMW applications.

5.2 SiGe HBT BiCMOS Technology

A commercially available 0.18 μm, 120 GHz SiGe HBT BiCMOS technology is used to implement the inductorless SiGe HBT ring oscillator [42]. It features high-performance SiGe HBTs with a peak f_T/f_{max} of 120/100 GHz, ASIC compatible 1.8 V Si CMOS devices, and a full suite of passive elements, including MIM capacitors and thin-film resistors. Three levels of copper interconnects are available, along with two thick top layers of aluminum metallization to enable high-Q inductor and transmission line designs. A schematic cross section of the 120 GHz SiGe HBTs is shown in Figure 12 of Section 1.3.

5.3 Ring Oscillator Operating Principle

A ring oscillator is realized by connecting an odd number of single-ended inverting amplifiers in a feedback loop, thus forming a ring structure. Figure 43 shows a block diagram of an N odd stage single-ended ring oscillator.

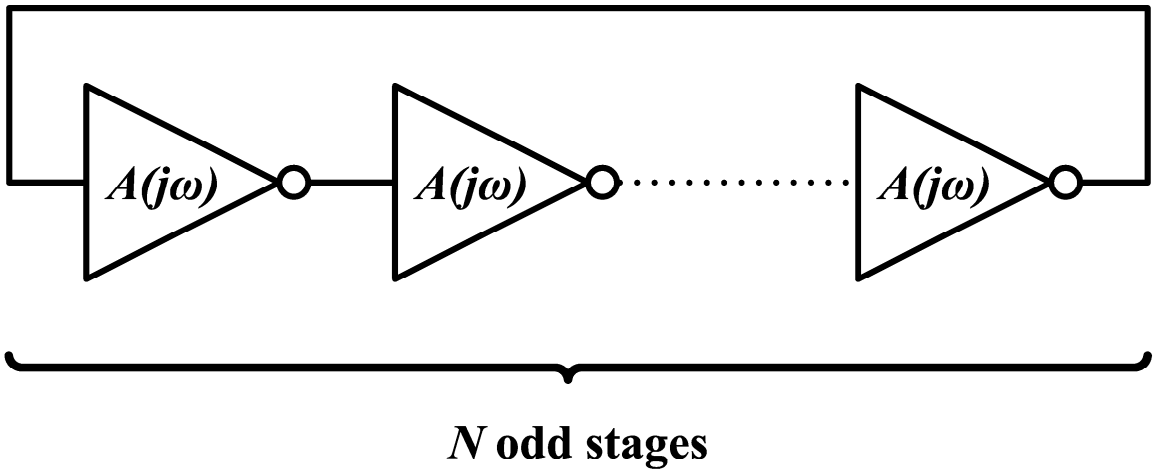


Figure 43: Block diagram of an N odd stage single-ended ring oscillator.

The operation of any oscillator can be divided into two distinct phases. One is the startup phase, and the other is the steady-state phase. Even though linear models are often used to analyze the steady-state behavior of oscillators, oscillators are fundamentally nonlinear and care must be taken when using linear approximations [76], [77]. On the other hand, linear models are perfectly valid for oscillator startup analysis because the oscillation amplitude is small. Hence, linear models can determine the startup condition for oscillation, and loosely estimate the steady-state frequency [77].

The small-signal open-loop transfer function of a ring oscillator is given as

$$H(j\omega) = [A(j\omega)]^N, \tag{16}$$

where $A(j\omega)$ is the transfer function of an inverting amplifier and N is the number of amplifier stages. For a ring oscillator to begin oscillation, the open-loop gain must be greater than unity when the total phase shift around the loop is in multiples of 2π radians. Each inverting amplifier contributes a static *dc* phase shift of π radians, resulting in net π radians for odd stages. Hence, the inverting amplifiers themselves must then contribute the other π radians of frequency-dependent *ac* phase shift required. These conditions, known as the Barkhausen criteria, are

$$|H(j\omega)| > 1 \tag{17}$$

and

$$arg[H(j\omega)] = \pi. \tag{18}$$

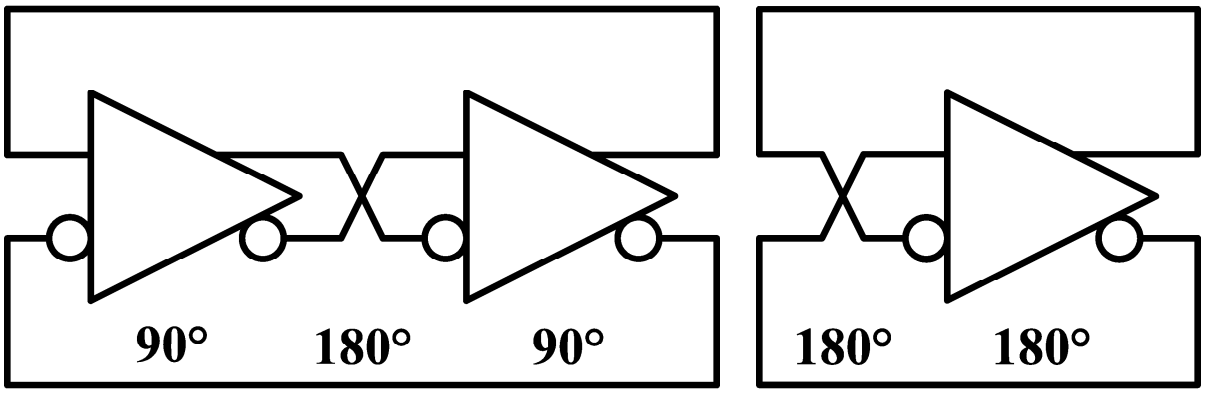
With differential inverting amplifiers, an even number of stages can be used. The static *dc* phase shift required can be achieved by simply interchanging the outputs of one inverting amplifier to the inputs of the next stage.

In time domain, the oscillation frequency of a ring oscillator is determined by the delay associated with the charging and discharging of parasitic capacitors. Thus, the oscillation

frequency is given by

$$f_{osc} = \frac{1}{2NT}, \tag{19}$$

where N is the number of amplifier stages, and T is the delay through each stage. The extra factor of two in the denominator is because the signal must propagate twice around the loop to obtain one full period. According to (19), the f_{osc} of a ring oscillator can be increased by reducing N. If N is reduced by a factor of two, the oscillator can potentially operate at twice the frequency, in addition to dissipating only half the power. Phase noise also decreases as N is reduced in a differential ring oscillator [78]. In contrast, the frequency-dependent *ac* phase shift contributed by each stage is now doubled. As N is further reduced, it becomes increasingly more difficult to maintain sufficient frequency-dependent *ac* phase shift before the open-loop gain drops to less than unity. Figure 44 shows the phase shift contributions required for oscillation startup in a two-stage and a single-stage differential ring oscillator. For the limiting case where $N = 1$, that single-stage must provide the whole π radians of frequency-dependent *ac* phase shift while still maintaining an open-loop gain of greater than unity. If the open-loop gain drops to less than unity when π radians of frequency-dependent *ac* phase shift is reached, the Barkhausen criteria is not satisfied and the ring oscillator will not startup.



(a) (b)

Figure 44: Phase shift contributions required for oscillation startup in (a) a two-stage and (b) a single-stage differential ring oscillator.

5.4 Inductorless MMW Ring Oscillator Design

It is clear from the above discussion that a single-stage ring oscillator provides the highest f_{osc} possible. Thus, the inductorless MMW SiGe HBT ring oscillator is based on the single-stage feedback topology. The goal is to obtain sufficient frequency-dependent *ac* phase shift and small-signal open-loop gain within that single-stage by relying on its internal poles. Consider a single-stage inductorless SiGe HBT ring oscillator core composed of a simple differential inverting amplifier with its outputs fed back to its inputs of the opposite polarity, as shown in Figure 45. The open-loop simulation, shown in Figure 46, indicates that the frequency-dependent *ac* phase shift is still less than π radians when the open-loop gain drops to less than unity. Thus, the single-stage ring oscillator based on this simple differential inverting amplifier core will not oscillate since the Barkhausen criteria are not satisfied. Several improvements to the simple inverting amplifier core have been proposed to improve the phase condition of the inverting amplifier, by adding poles to increase the delay around the loop [73], [75], [79]. The differential inverting amplifier core used in the present oscillator design is shown in Figure 47. It is a modified version of that found in [79]. A cross-coupled pair (Q_5-Q_6) added on top of the differential pair (Q_1-Q_2) provides positive feedback to increase phase shifting [79], [80]. Open-loop simulation, shown in Figure 48, indicates π radians of frequency-dependent *ac* phase shift occur at about 35 GHz, while the small-signal gain is 4.5 dB. Hence, the Barkhausen criteria are satisfied, enabling oscillations to build up. Transient simulations are in agreement and show the oscillator stabilizing to about 32 GHz.

The advantages of using only one cross-coupled pair, in the present work, as opposed to the two proposed in [79], are as follows. One cross-coupled pair suffices in improving the phase conditions for oscillation with these SiGe HBTs. The use of the second cross-coupled pair would result in extra delay and reduce the maximum achievable f_{osc}. In addition, an increase of one $V_{BE(on)}$ in the supply is needed to accommodate the addition of the second cross-coupled pair, resulting in extra, unwanted power dissipation.

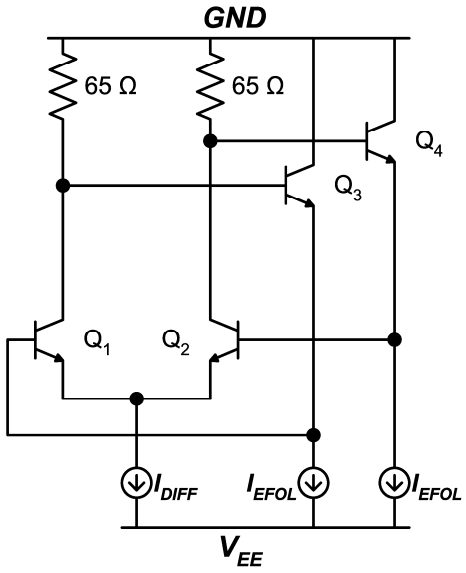


Figure 45: Simplified schematic of a simple differential inverting amplifier core that fails to oscillate.

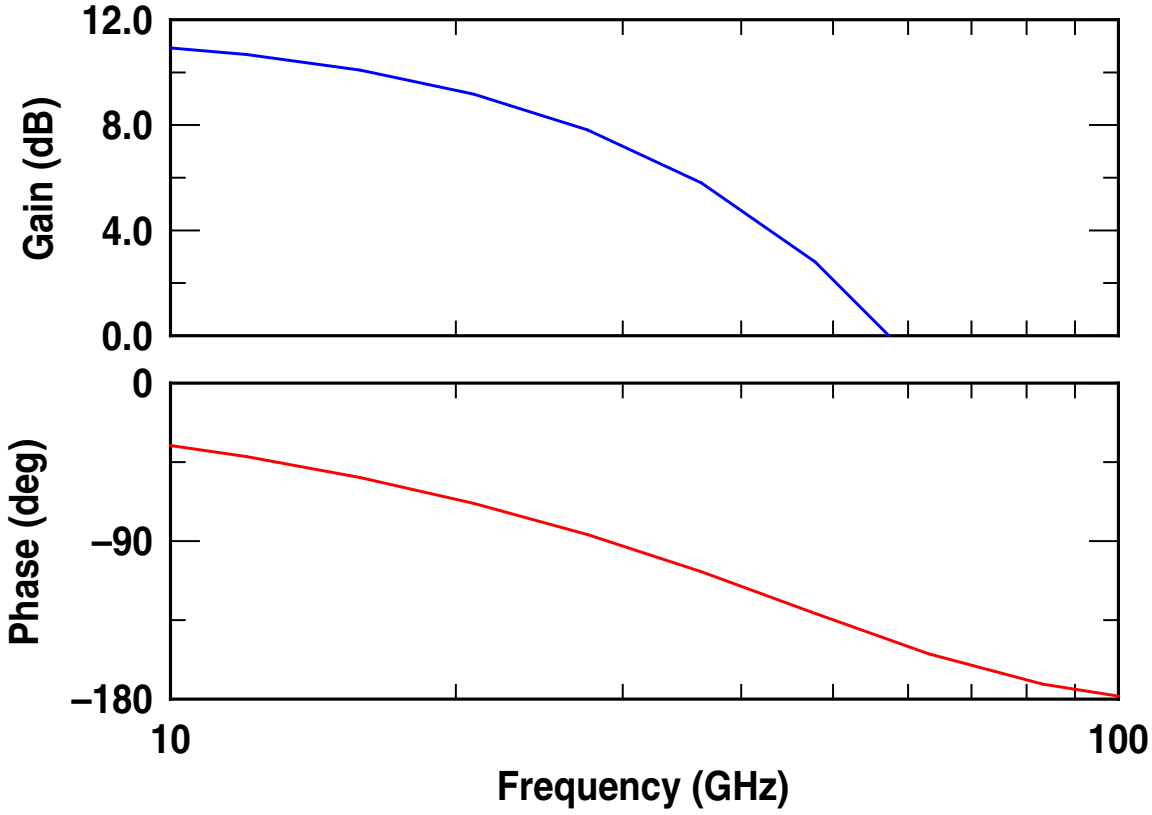


Figure 46: Open-loop simulation of the simple inverting amplifier.

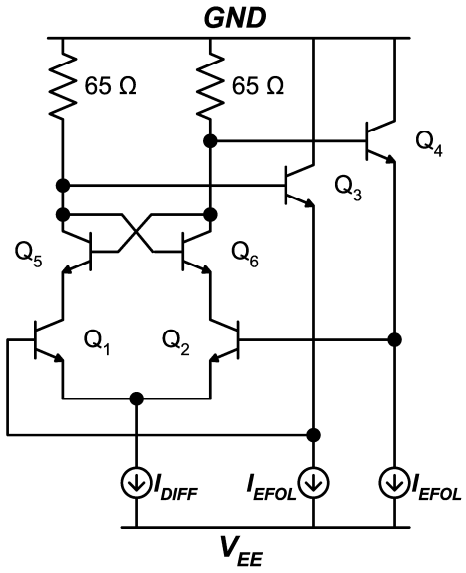


Figure 47: Simplified schematic of a modified differential inverting amplifier core that oscillates.

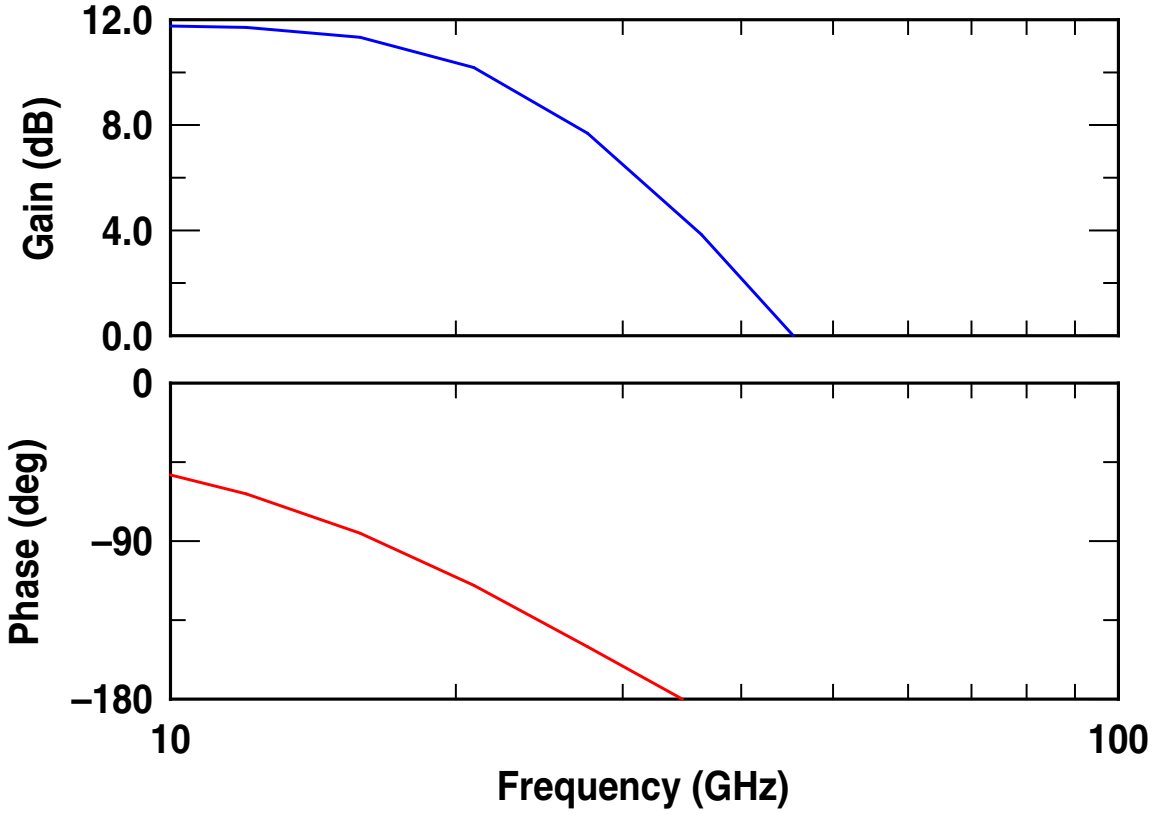


Figure 48: Open-loop simulation of the modified inverting amplifier.

5.5 *Measurement Results*

The layout of the inductorless MMW SiGe HBT ring oscillator is done in a symmetrical fashion to minimize the effect of common-mode noise. The circuit occupies an extremely compact active area of less than 60 × 180 μm^2. The total chip size, including bondpads, is only 380 × 730 μm^2, as shown in Figure 49.

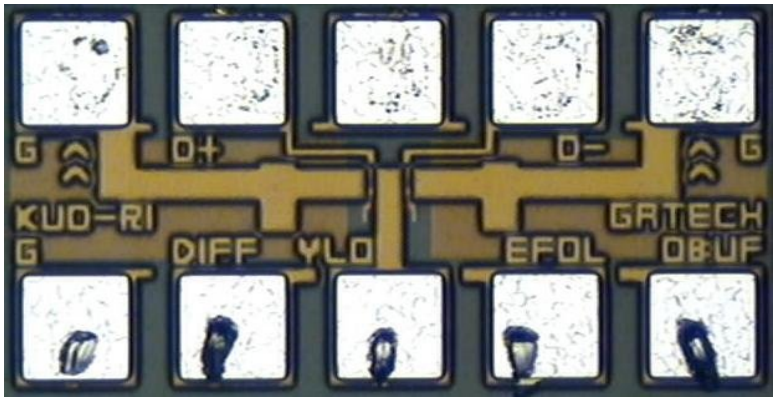


Figure 49: Chip micrograph of the inductorless MMW SiGe HBT ring oscillator.

The oscillator is tested on-wafer in an RF shield room using 40 GHz probes and cables. Custom-built filters are placed on the *dc* supplies to reduce the impact of supply noise. The oscillator is characterized with one output connected to a spectrum analyzer, while the other output is terminated with 50 Ω through an equal length cable for symmetry. The measured loss of the connection from the spectrum analyzer to the oscillator of 6.0 dB is used to calibrate the measured signal power. The oscillator operates on a single supply of -3.0 V and consumes, including output buffers, only 87 mW. The output spectrum of the oscillator operating at 31.96 GHz with a measured signal power of -18.67 dBm is shown in Figure 50. The measured f_{osc} agrees well with the f_{osc} from the steady-state transient simulation. At that frequency, the measured phase noise is -85.33 dBc/Hz at 1 MHz offset, as shown in Figure 51. The f_{osc} is tuned through the base bias current of the emitter-follower pair. A decrease in the emitter-follower tail current decreases f_T and the charge current of the parasitic capacitances, hence decreasing the f_{osc} [75]. The measured f_{osc} as a function of

base bias current, as shown in Figure 52, ranges from 28.36 to 31.96 GHz, resulting in a 12% tuning range around the mid-band frequency. Adjusting the base bias current of the emitter-followers also affects the output signal power. The calibrated (measured + loss) output power as a function of base bias current, as shown again in Figure 52, ranges from -13.50 to -12.67 dBm. Less than 1 dB of output power variation is achieved when the frequency is tuned.

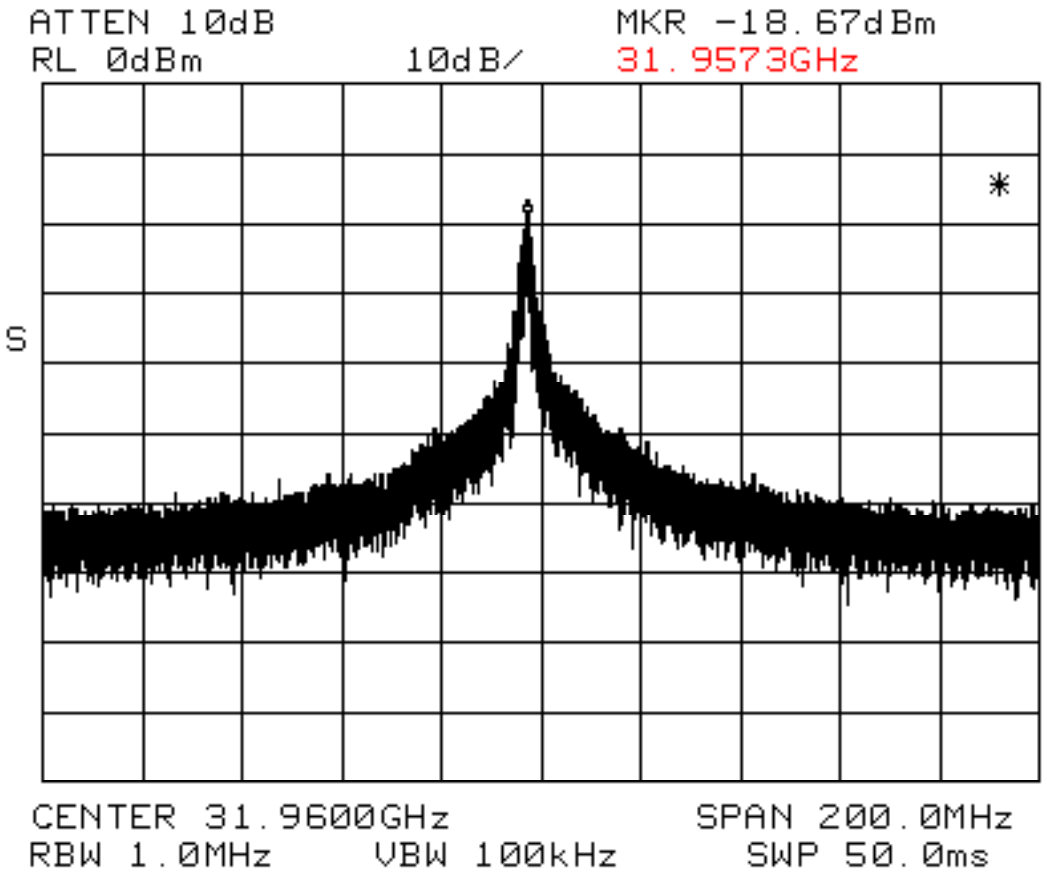


Figure 50: Measured output power spectrum of the inductorless MMW SiGe HBT ring oscillator operating at 31.96 GHz.

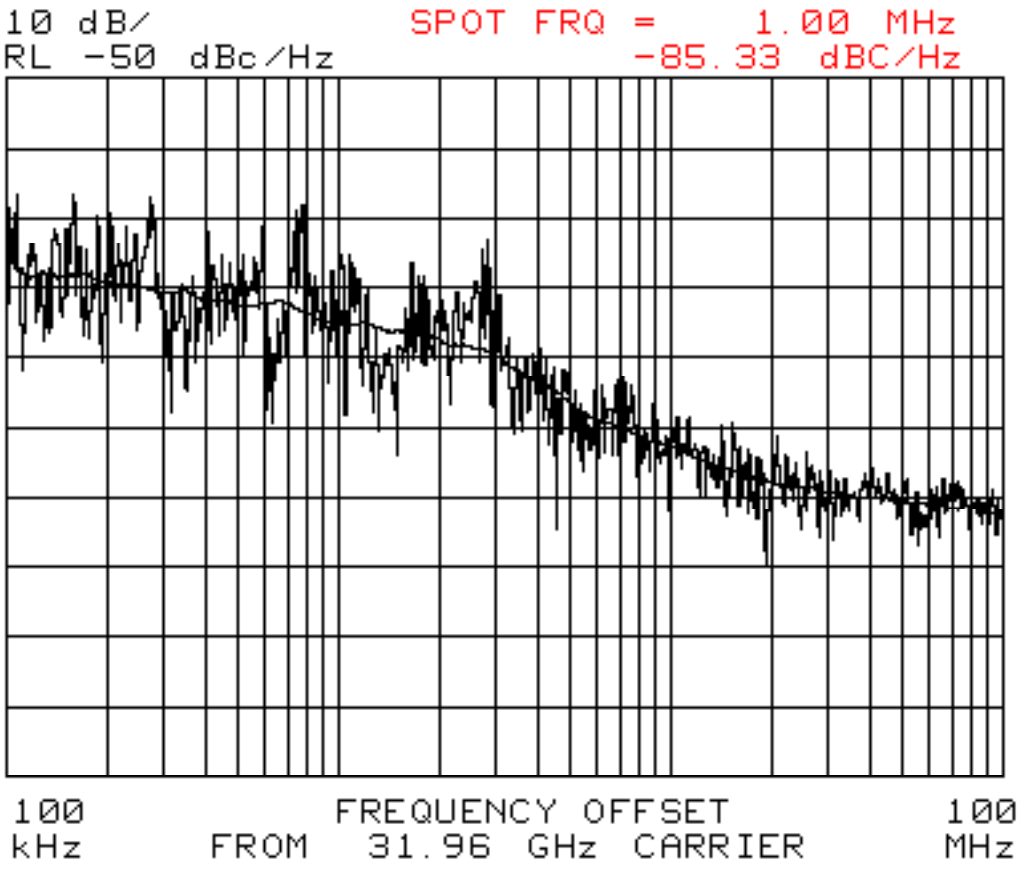


Figure 51: Measured phase noise of the inductorless MMW SiGe HBT ring oscillator operating at 31.96 GHz.

5.6 Performance Comparison

Numerous ring oscillators have been published. To compare the performance of the present oscillator to other state-of-the-art inductorless ring oscillators operating over a similar frequency range [72]-[75], the oscillator *FOM* is used to normalize the phase noise with respect to oscillation frequency, offset frequency, and dissipated power according to

$$FOM = L(f_m) - 20\log\frac{f_{osc}}{f_m} + 10\log\frac{P_{diss}}{1\text{ mW}}, \tag{20}$$

where L is the phase noise, f_m is the offset frequency, and P_{diss} is the dissipated power. The comparison is given in Table 6. In addition to occupying the smallest active area, the present oscillator achieves an *FOM* of -156 dBc/Hz, which is the best to date, because of

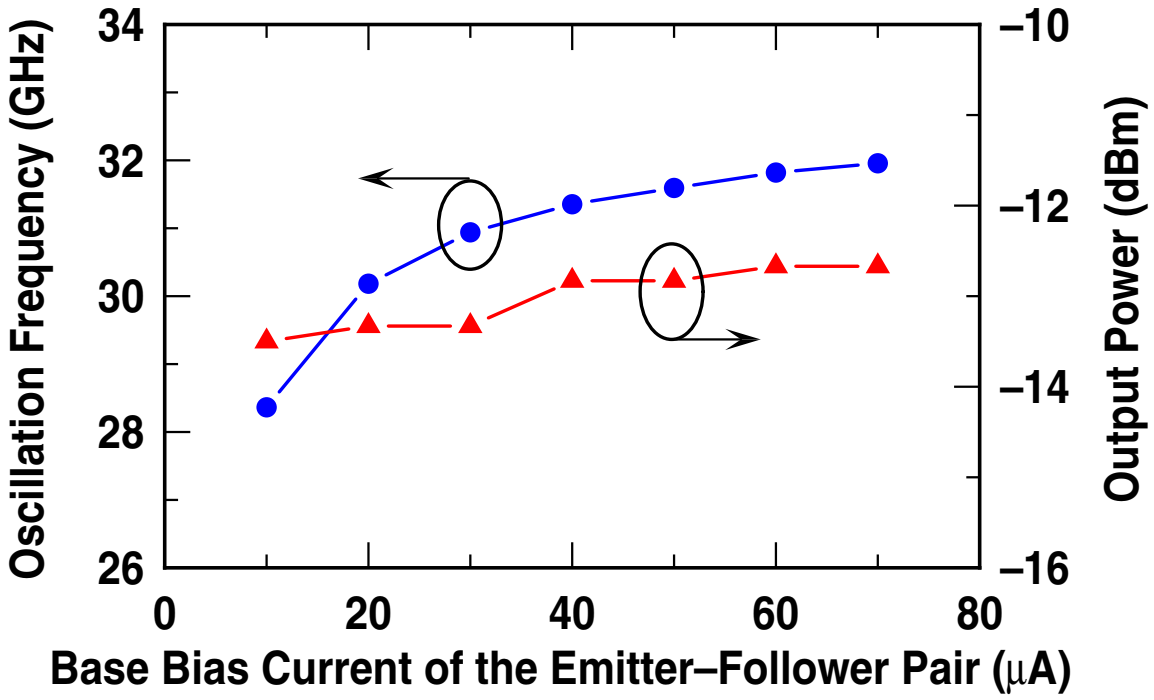


Figure 52: Measured oscillation frequency and calibrated output power versus the base bias current of the emitter-follower pair in the inductorless MMW SiGe HBT ring oscillator.

an increase in f_{osc} and a reduction in P_{diss}.

5.7 Summary

An inductorless SiGe HBT ring oscillator optimized for MMW operation, low-power consumption, and ultra-compact size has been realized with an addition of a cross-coupled pair to the simple differential inverting amplifier. Comparing to other state-of-the-art inductorless ring oscillators operating in a similar frequency range, the present oscillator achieves the best *FOM*. The circuit demonstrates the potential of inductorless SiGe HBT ring oscillators for MMW applications.

Table 6: Comparison of state-of-the-art inductorless ring oscillators operating over a similar frequency range.

Reference	L [dBc/Hz]	f_m [MHz]	f_{osc} [GHz]	P_{diss} [mW]	FOM [-/GHz]	Process/f_T [dBc/Hz]	Active Area [mm^2]
This work	-85.33	1	31.96	87	-156.03	SiGe/120	0.0108
[72]	-85.00	1	26.60	250	-149.52	InP/53	-
[73]	-87.67	1	25.18	240	-151.89	SiGe/45	0.0225
[74]	-83.33	1	21.18	152	-148.03	SiGe/120	0.0180
[75]	-90.00	1	18.69	130	-154.29	InP/100	0.1972

CHAPTER VI

THE STUDY OF EMITTER SCALING AND DEVICE BIASING ON MMW SIGE HBT VCO PERFORMANCE

6.1 Introduction

MMW VCOs are essential building blocks in both wireless and wired communication systems. VCOs are used to generate local oscillators (LOs) for short-range broadband wireless transceivers operating at 60 GHz, as well as clocks for data retiming in optical networks operating at 40 Gb/s. Many metrics are used to characterize the performance of such VCOs, including f_{osc}, frequency tuning range, output power (P_{out}), and P_{diss}. Perhaps the most important specification of any VCO is phase noise or jitter, which primarily determines the channel spacing in RF systems or timing margin in digital systems. Models developed to understand, estimate, and minimize the up-conversion of both $1/f$ and white noise to phase noise in a variety of oscillator topologies can be found in literature [81], [82].

Traditionally, MMW VCOs have been implemented in III-V technologies [83]. However, through aggressive vertical profile scaling, SiGe HBT BiCMOS technology has become a formidable contender in recent years [84]. While the implications of geometrical scaling, both vertical and horizontal, of SiGe HBTs on the performance of VCOs have been explored [85]-[87], these studies on device-circuit interactions are limited to VCOs operating at less than 10 GHz with SiGe HBTs having peak f_T of at most 120 GHz. The design tradeoffs for MMW SiGe HBT VCOs associated with emitter scaling in state-of-the-art SiGe HBTs with peak $f_T \geq 200$ GHz have yet to be experimentally examined in detail, and are addressed here for the first time.

In this chapter, the fundamental questions of what emitter length (l_e) and what bias condition of advanced SiGe HBTs best optimize a given MMW SiGe HBT VCO performance metric are investigated. The 200 GHz SiGe HBTs and the MMW SiGe HBT VCOs used in this experiment are described in Section 6.2. Section 6.3 discusses and explains the measured results. Design implications are presented in Section 6.4.

6.2 Experiment

The experiment is based on a low-power (2.64 mW minimum), low-phase noise (-99 dBc/Hz at 1 MHz offset) 33 GHz Colpitts VCO [88], which employs line inductors instead of spiral ones, implemented with 200 GHz SiGe HBTs [89]. The schematic of the MMW SiGe HBT VCO is shown in Figure 53. Transistors Q_1-Q_2 are the common base Colpitts transistors and Q_3-Q_4 are the cross-coupled time switch transistors [90]. By fixing the VCO circuit and layout design, and using different l_e of 2.5, 5.0, and 10.0 μm for transistors Q_1-Q_4, while keeping the emitter width (w_e) constant at 0.12 μm, the impact of emitter geometry scaling, along with device *dc* biasing, are investigated. Since the *LC* tank resonator and the tail current biasing transistors are not altered among the three MMW SiGe HBT VCOs, resonator noise and tail current noise are not investigated in this work. The MMW SiGe HBT VCOs were fabricated side-by-side on a single chip, shown in Figure 54, to minimize process variation, along with *dc* and *ac* test structures for correlating changes in circuit performance back to device parameters. The measured forward mode Gummel characteristics and the extrapolated f_T versus I_C curves are shown in Figure 55 and 56, respectively.

6.3 Results and Discussion

The MMW SiGe HBT VCOs were measured on-wafer in an RF shield room using 50 GHz probes and cables, with one output connected to a spectrum analyzer while the other output was terminated with 50 Ω through an equal length cable for symmetry. The

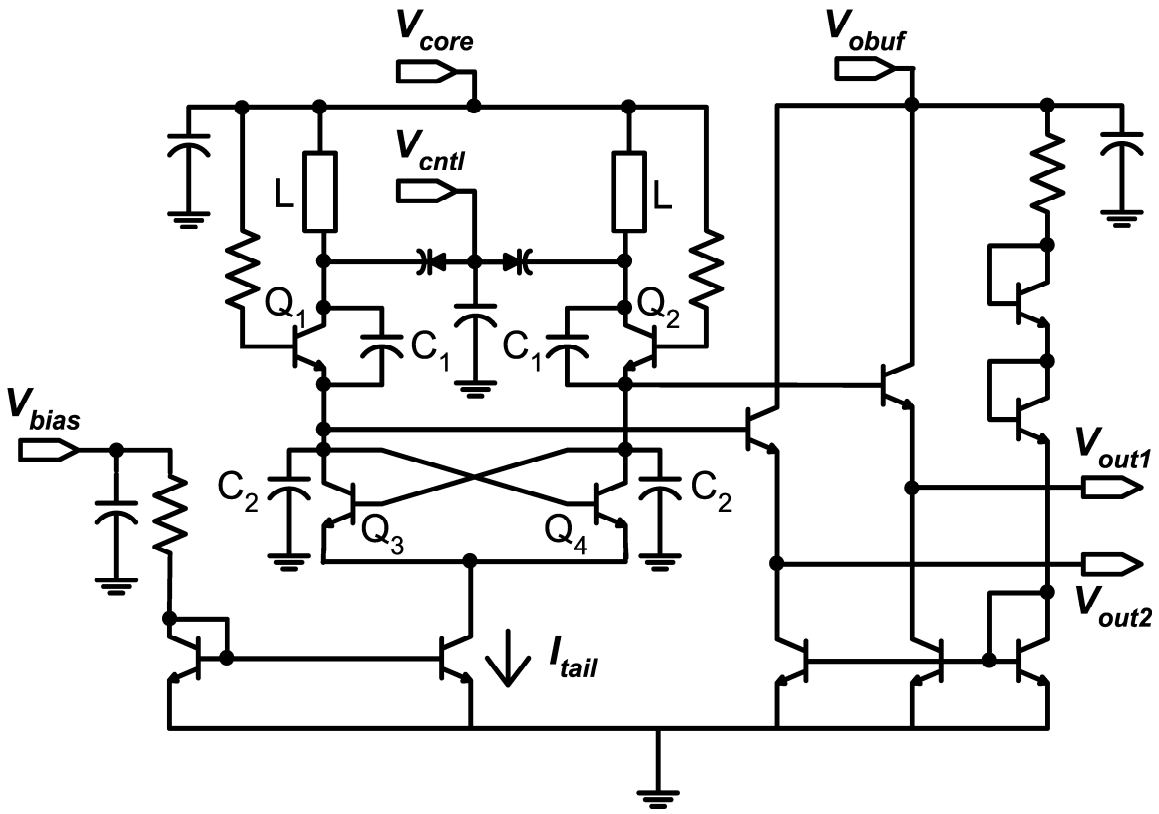


Figure 53: Simplified schematic of the MMW SiGe HBT VCO (after [88]).

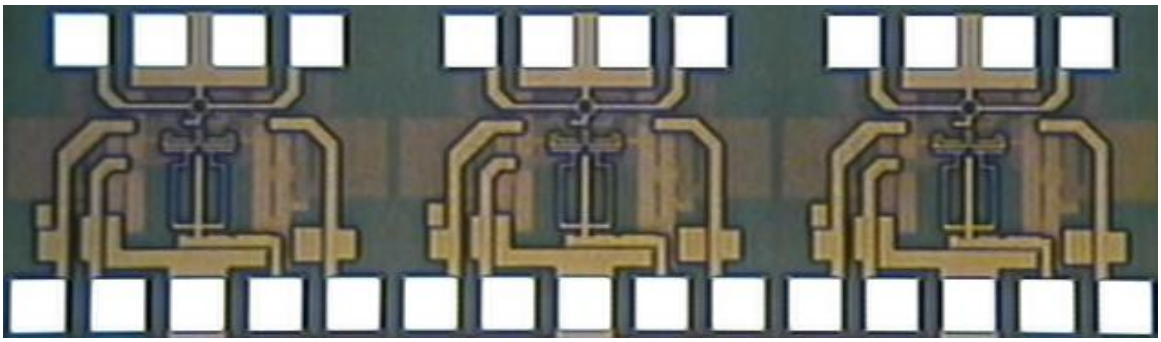


Figure 54: Chip micrograph of the MMW SiGe HBT VCOs fabricated side-by-side, with emitter area (A_e) of Q_1-Q_4 = 0.12 x 10.0, 0.12 x 5.0, and 0.12 x 2.5 μm^2 from left to right, respectively.

measured loss of the connection from the spectrum analyzer to the VCO of 6.1 dB was used to calibrate the measured signal power. A typical output power spectrum is shown in Figure 57. The phase noise of the MMW SiGe HBT VCOs was measured with the

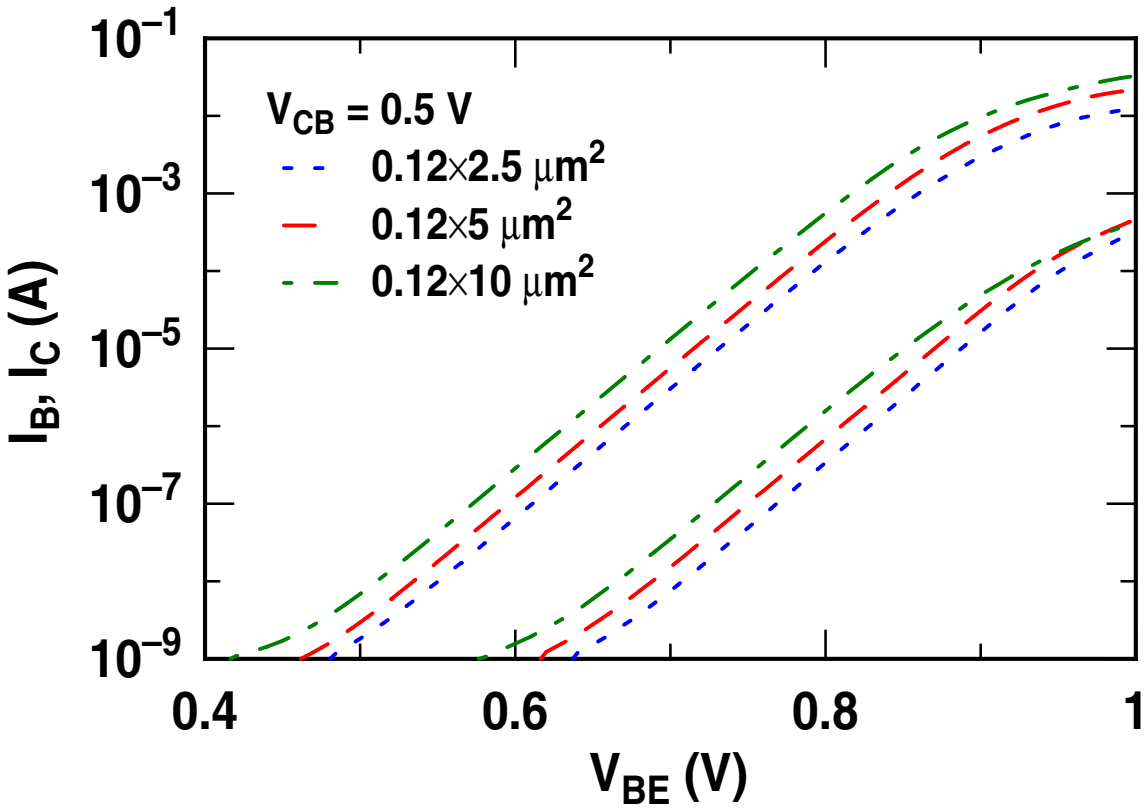


Figure 55: Measured forward mode Gummel characteristics of the 200 GHz SiGe HBTs.

firmware utility of the spectrum analyzer. Since the VCOs were free running, some center frequency drifting caused problematic close-in phase noise (offset < 10 kHz, up-converted from $1/f$ noise) measurement. However, the far-from-carrier phase noise at 1 MHz offset (up-converted from white noise) was robust and repeatable, and thus is used in this study. Figure 58 shows a typical phase noise plot.

6.3.1 Oscillation Frequency Versus Tail Current

The tail current (I_{tail}) of the MMW SiGe HBT VCOs can be adjusted by changing the bias voltage (V_{bias}) of the current mirror. The measured f_{osc} as a function of I_{tail} is shown in Figure 59. The f_{osc} of the MMW SiGe HBT VCOs increases (ranging from 3.75% at an I_{tail} of 4.5 mA to 5.85% at an I_{tail} of 1.5 mA) as l_e scales down because of a reduction in device capacitances. This demonstrates the significant impact of device parasitics, however

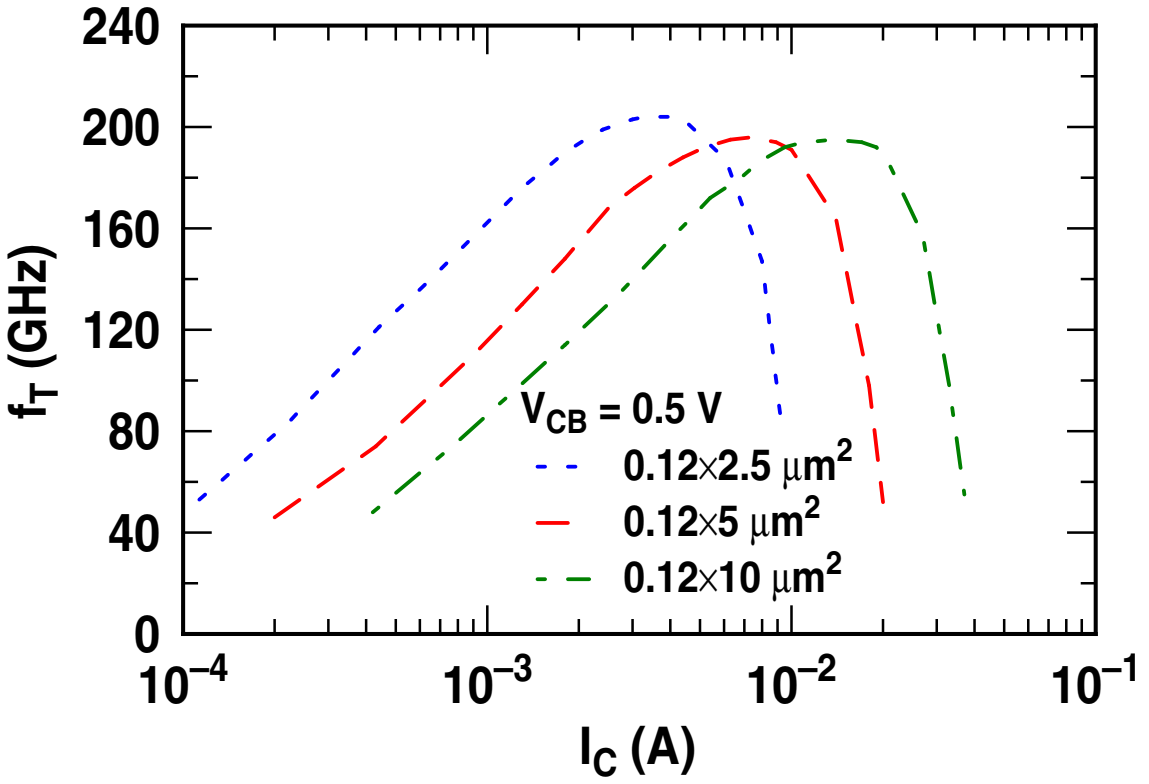


Figure 56: Extrapolated cutoff frequency versus collector current of the 200 GHz SiGe HBTs.

small, on circuit operation in the MMW range. The f_{osc} also has a negative dependence on I_{tail}, and this dependence increases as l_e is reduced. This can be explained as follows. For transistors with smaller l_e to sink the same I_C as the larger devices, the base-emitter voltage (V_{BE}) needs to be correspondingly higher, as seen from Figure 55. However, the diffusion capacitance (C_D) of the forward biased base-emitter junction has an exponential dependence on V_{BE}. As I_{tail} is increased, the C_D of the devices with smaller l_e increases faster because its V_{BE} is larger, and thus contributes more capacitance, causing f_{osc} to decrease more rapidly.

6.3.2 Output Power Versus Tail Current

The P_{out} of the MMW SiGe HBT VCOs is proportional to the tank voltage (V_{tank}) through a capacitive voltage divider formed by C_1 and C_2, as shown in Figure 53. At low

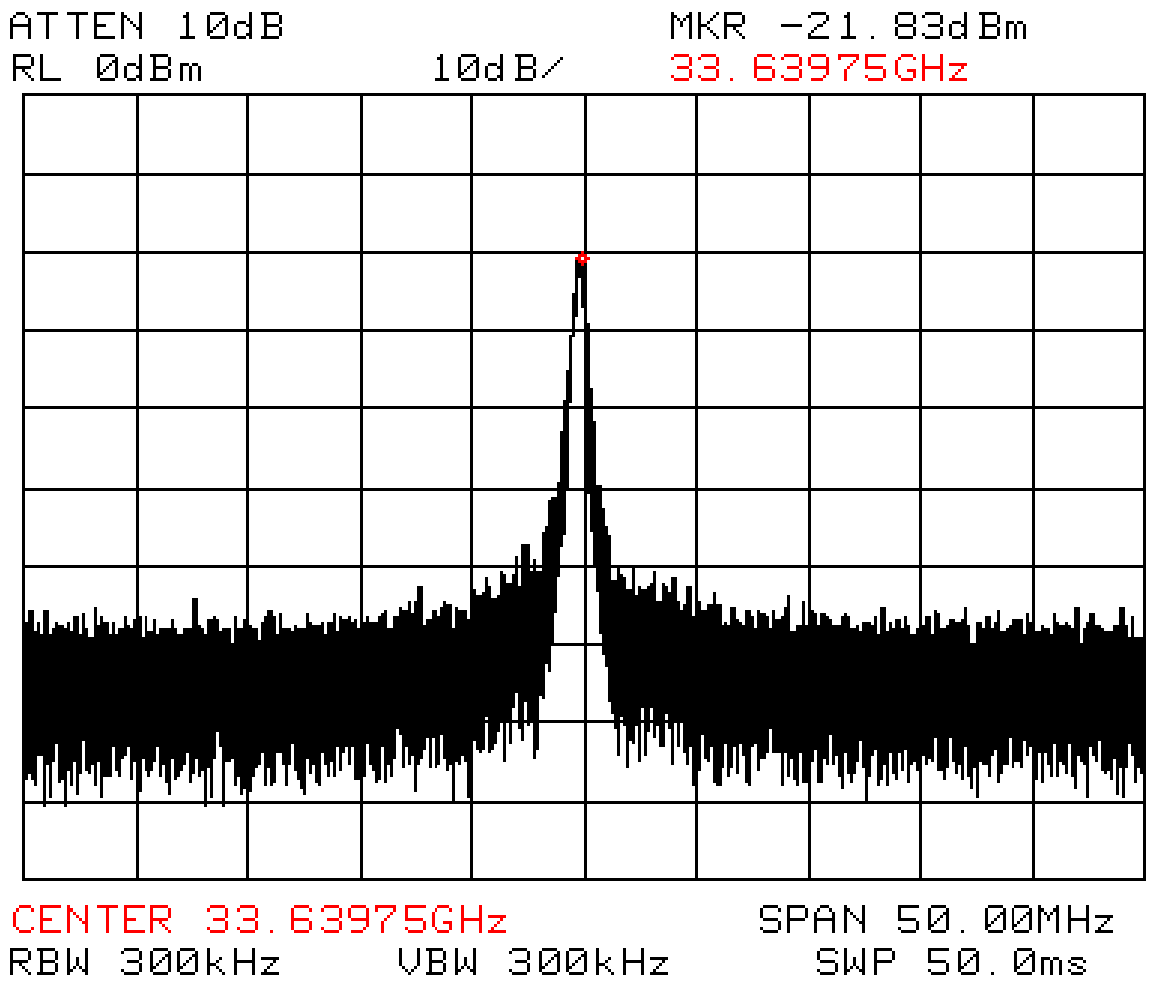


Figure 57: Measured output power spectrum of the MMW SiGe HBT VCO (A_e = 0.12 x 5.0 μm^2, I_{tail} = 2.5 mA, V_{core} = 2.5 V, and V_{cntl} = 0 V).

I_{tail} bias, P_{out} increases proportionally as I_{tail} is increased. This region of operation is current limited since V_{tank} is solely determined by I_{tail} and the LC tank resonator's equivalent resistance [91]. At high I_{tail} bias, P_{out} remains roughly constant as I_{tail} is increased since it is voltage limited by the available voltage headroom of the V_{tank} swing [91]. Thus, P_{out} should be relatively independent of l_e. The calibrated P_{out} (measured + loss) as a function of I_{tail} is shown in Figure 60. The P_{out} of the VCOs, even though increasing for the most part as l_e is scaled down, are within 2 dB of one another. It can be seen from Figure 60 that the operation of P_{out} crosses over from being current limited to being voltage limited at around 3.5 to 4.5 mA.

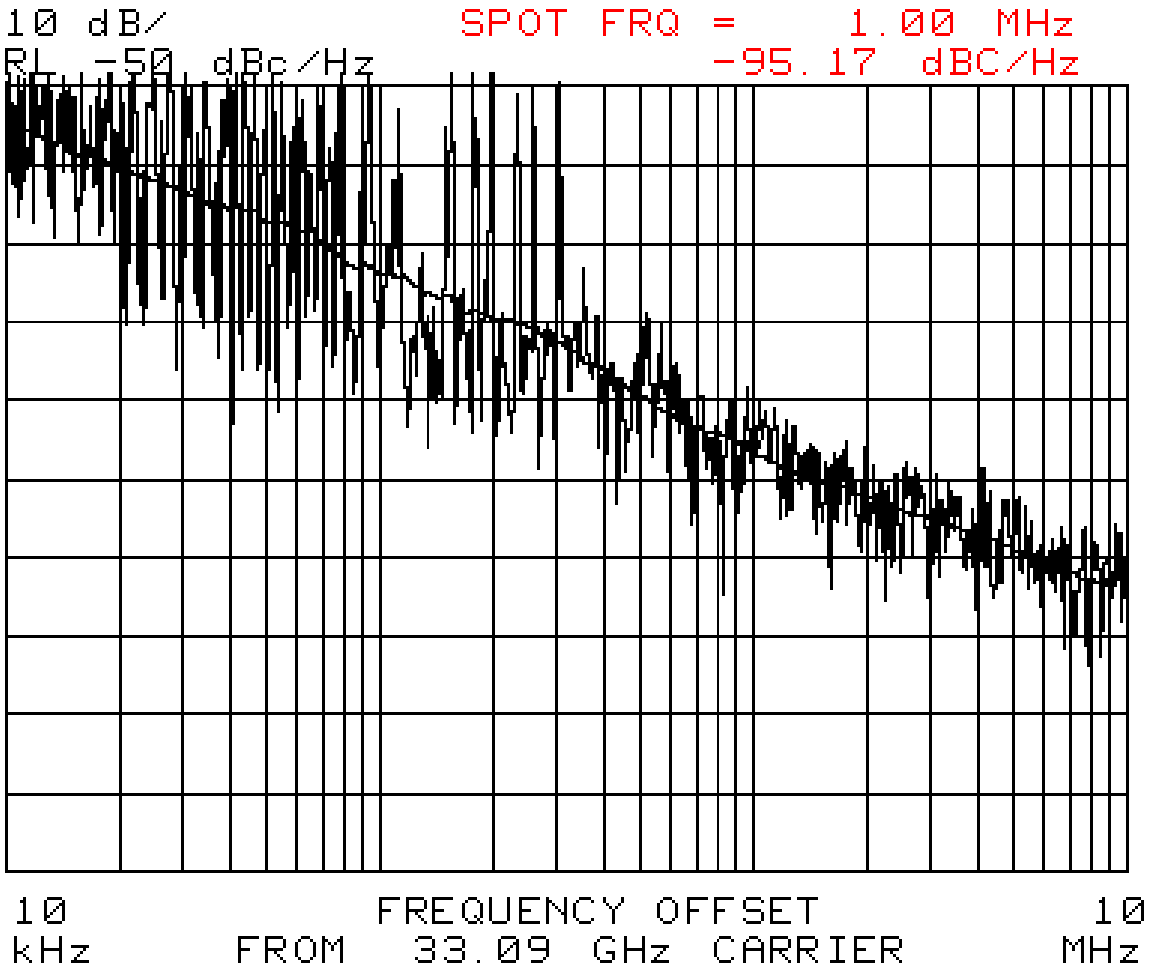


Figure 58: Measured phase noise of the MMW SiGe HBT VCO (A_e = 0.12 x 10.0 μm^2, I_{tail} = 2.6 mA, V_{core} = 2.5 V, and V_{cntl} = 0 V).

6.3.3 Phase Noise Versus Tail Current

The phase noise of the MMW SiGe HBT VCOs at 1 MHz offset was measured for different values of I_{tail}. As shown in Figure 58, the phase noise plot exhibits an ideal $1/f^2$ (-20 dB/dec) slope in the frequency offset range of 10 kHz to 10 MHz, which is a clear indication of up-conversion of white noise [81], [82]. The white noise sources in a SiGe HBT are: (1) base shot noise, (2) collector shot noise, and (3) base resistance thermal noise.

Figure 61 shows the measured phase noise of the MMW SiGe HBT VCOs. Initially,

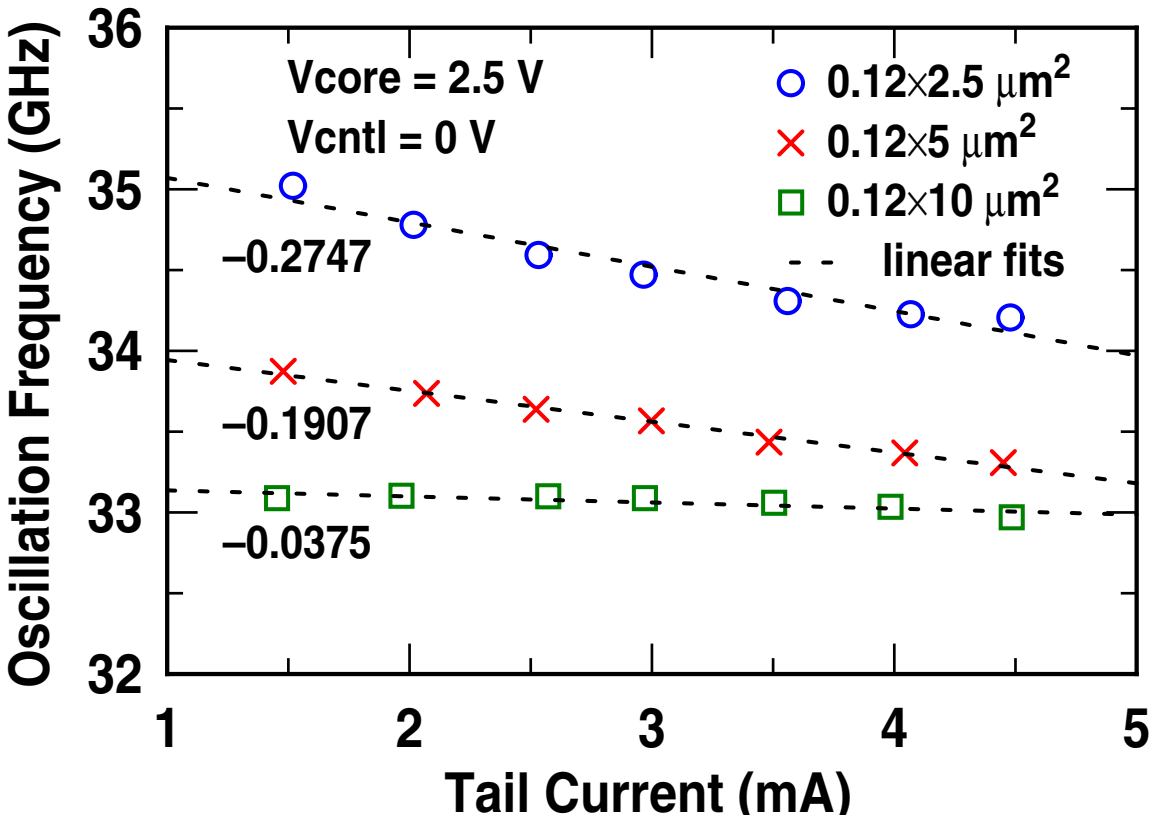


Figure 59: Oscillation frequency of the MMW SiGe HBT VCOs versus tail current.

phase noise reduces with the increase in I_{tail}. As I_{tail} is raised further, the phase noise increases. The minimum phase noise is observed for an I_{tail} of around 3.5 to 4 mA. This corresponds closely to the point where P_{out} crosses over from being current limited to being voltage limited. The observation can be explained as follows. In current limited operation, the increase in I_{tail} increases the V_{tank} oscillation amplitude, resulting in a raise in signal power, and thus improving phase noise [91], [92]. Once P_{out} becomes voltage limited, further increase in I_{tail} results in an increase in collector and base shot noise, and thus degrading phase noise [92].

When the VCOs are biased at the same I_{tail}, the collector shot noise contributions are similar across the VCOs, as well as the base shot noise contributions (to the first order, assuming similar β-I_C rolloffs for each device). Thus, the difference in phase noise is mainly caused by the difference in base resistance (r_b) as l_e is scaled. The measured phase

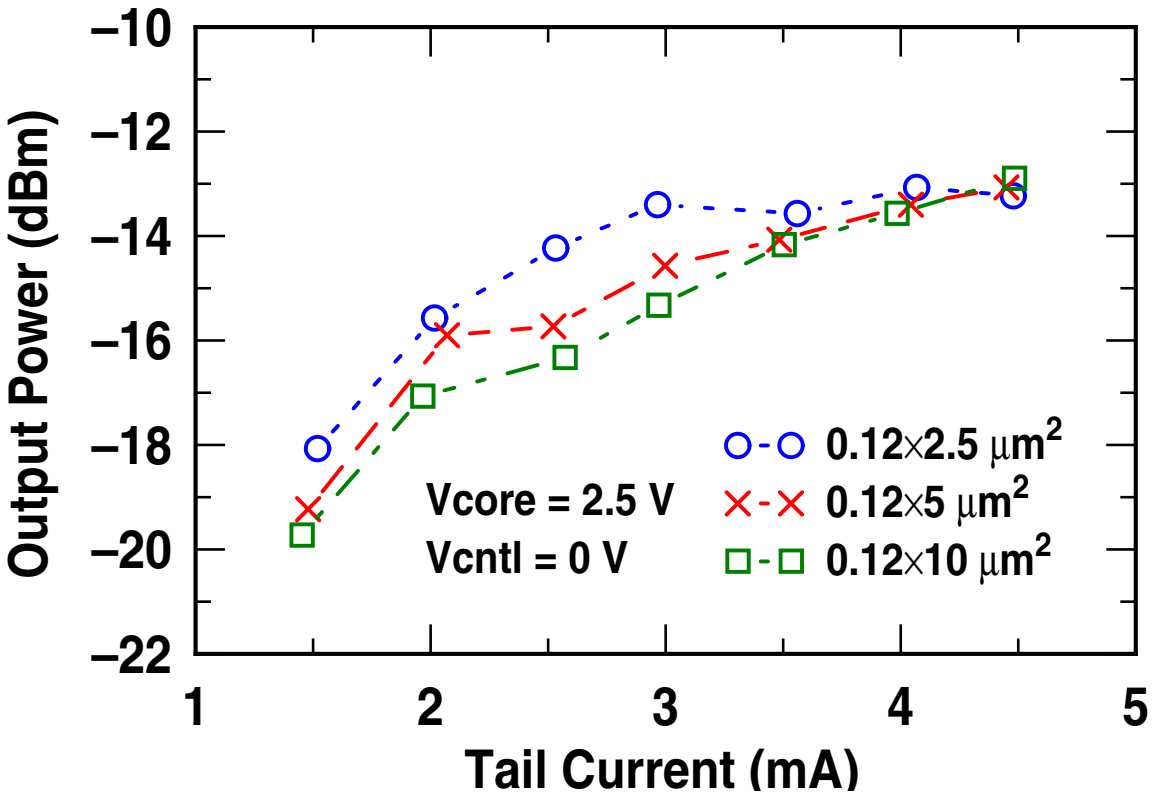


Figure 60: Output power of the MMW SiGe HBT VCOs versus tail current.

noise improves as l_e is increased. This is as expected, since a device with the longer l_e has a smaller r_b [93].

6.3.4 Oscillation Frequency Versus VCO Core Voltage

The variation in the f_{osc} of a VCO as a function of its supply voltage is known as "frequency pushing." As the VCO core voltage (V_{core}) is reduced, the operating voltage headroom of the transistors decreases, resulting in a decrease in I_{tail}, as well as a reduction of the reversed biased base-collector voltage (V_{BC}), thus increasing the depletion capacitance (C_J) at the base-collector junction. Figure 62 shows the frequency pushing characteristics of these MMW SiGe HBT VCOs. The measured f_{osc} decreases as V_{core} is reduced, as expected. The VCOs have a linear frequency pushing dependence on V_{core}, regardless of l_e, with similar pushing sensitivities, ranging from 475 to 525 MHz/V (only 50 MHz/V variation).

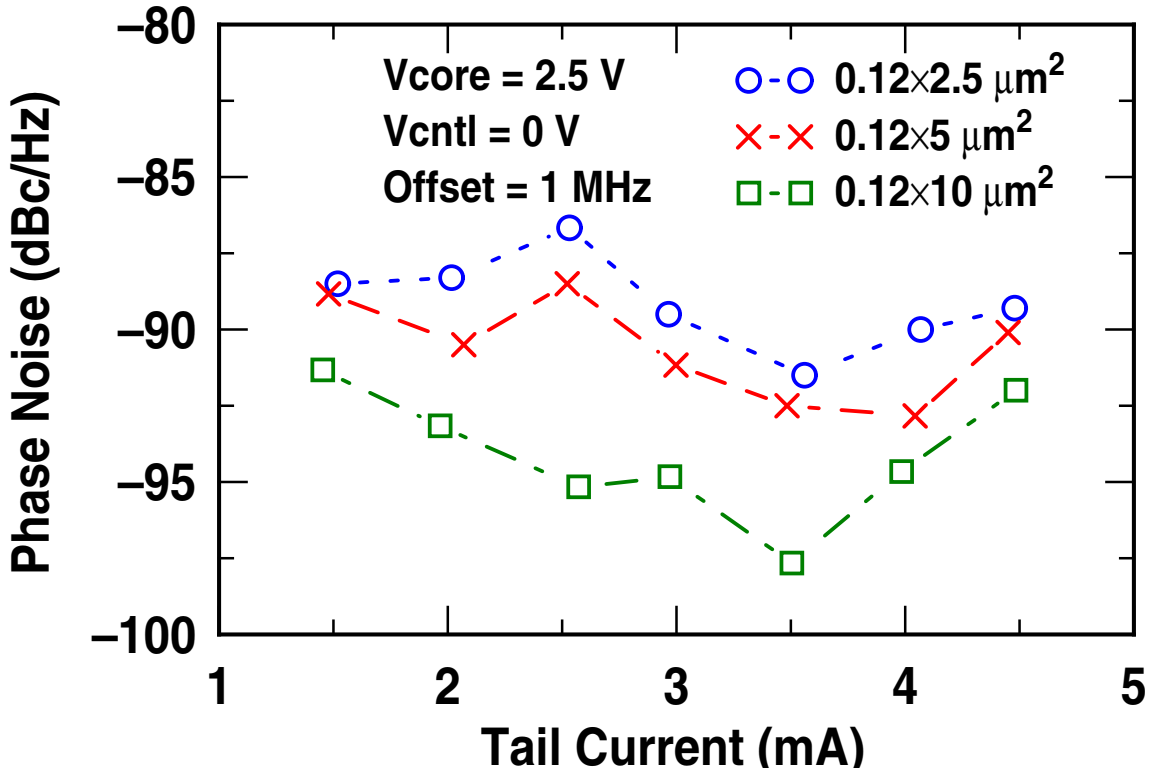


Figure 61: Phase noise of the MMW SiGe HBT VCOs at 1 MHz offset versus tail current.

6.3.5 Oscillation Frequency Versus Varactor Control Voltage

The f_{osc} of the MMW SiGe HBT VCOs is tuned through the control voltage (V_{cntl}) applied to the reverse biased varactor diodes. The tuning sensitivity and linearity are shown in Figure 63. The f_{osc} decreases monotonically as the reverse bias voltage on the varactor diodes is reduced by increasing V_{cntl} from 0 to 2.5 V, since the varactor diode capacitance increases monotonically with decreasing reverse bias. All VCOs exhibit a linear tuning sensitivity when V_{cntl} is varied from 0 to 1.5 V. This is expected since the varactor diodes were not changed among the VCOs. The tuning constants, however, are not identical, having a sharper slope as l_e scales down, from -600.4 to -632.6 MHz/V. This can be explained as follows. Transistor with smaller l_e contributes less parasitics, resulting in a higher f_{osc}. Thus, the same incremental increase in the varactor diode capacitance has a comparatively larger effect on the overall equivalent capacitance of the *LC* tank resonator.

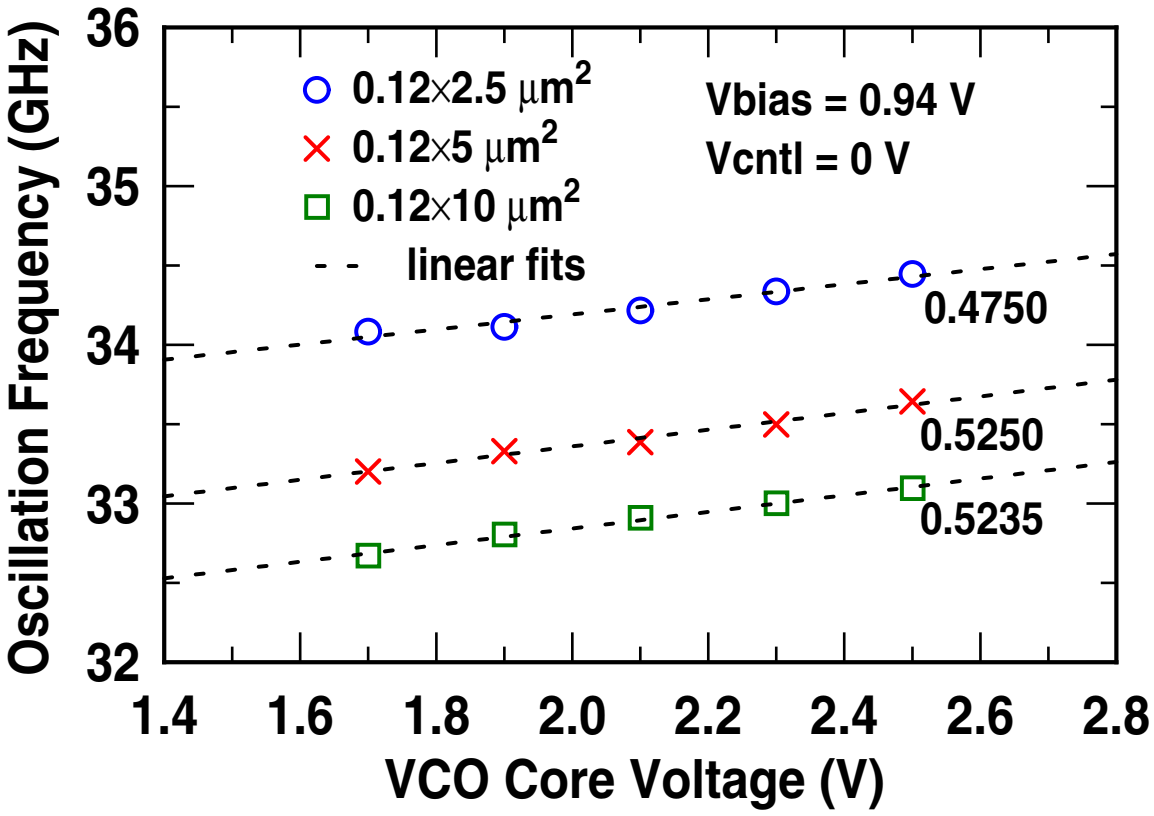


Figure 62: Oscillation frequency of the MMW SiGe HBT VCOs versus VCO core voltage.

6.4 Design Implications

The results of Section 6.3 are used to gain insight into the design tradeoffs associated with emitter scaling and device biasing of 200 GHz SiGe HBTs for various MMW SiGe HBT VCO performance metrics. Lower sensitivity of f_{osc} to I_{tail} is achieved when l_e is increased, as shown in Figure 59. However, to achieve a higher f_{osc} under the same bias condition (i.e., at the same I_{tail}, and thus the same P_{diss}), a smaller l_e is desired. The P_{out} of a VCO is relatively independent of l_e, as shown in Figure 60. To achieve the best phase noise performance, a VCO should be biased with just enough I_{tail} to reach maximum P_{out} (i.e., on the verge of being voltage limited) [92], as can be seen by comparing Figure 60 and 61. Under the same bias condition, VCOs using transistors with larger l_e also produce lower phase noise. One might be tempted to use devices with increasingly larger l_e to reduce the phase noise up-converted from white noise sources. This design approach,

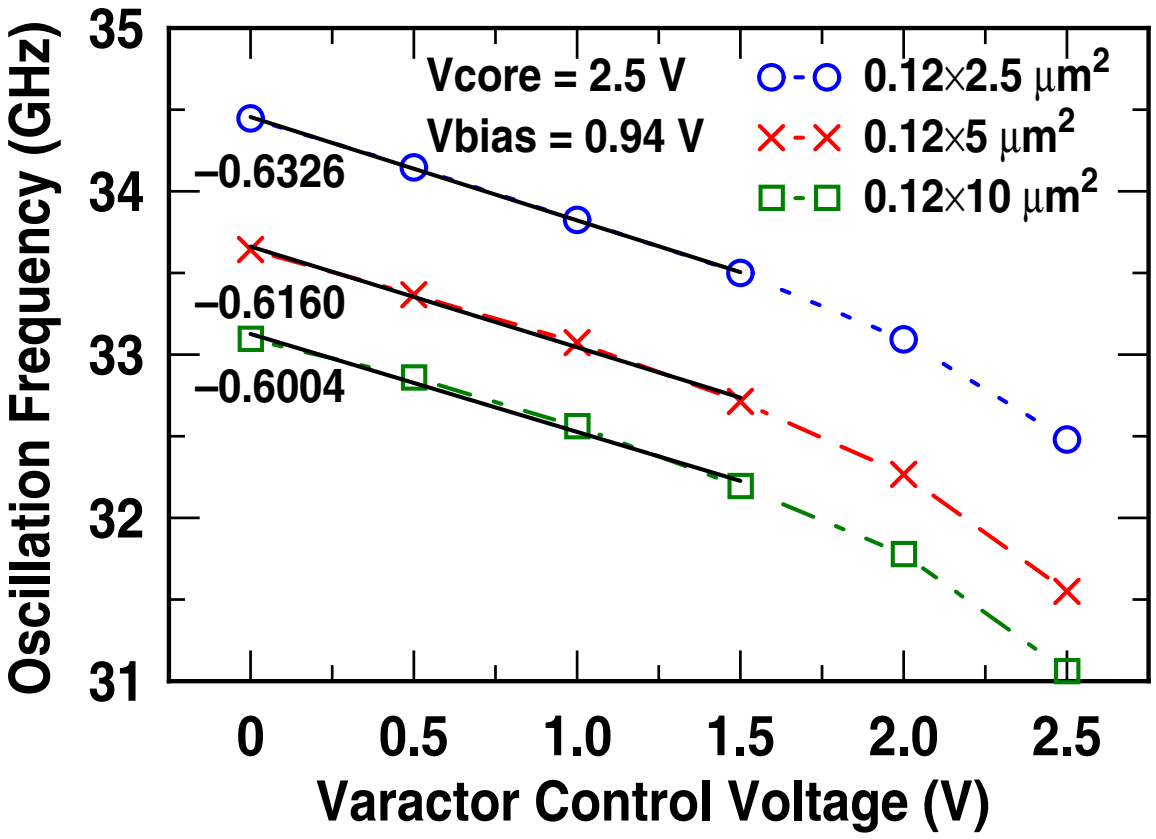


Figure 63: Oscillation frequency of the MMW SiGe HBT VCOs versus varactor control voltage.

however, may cause issues with oscillation startup, due to the fact that f_T decreases as l_e scales up at a fixed I_C below peak f_T, as shown in Figure 56 (i.e., f_T-I_C curve shifts to the right) [86]. In addition, overly aggressive l_e up-scaling may not further reduce phase noise, since r_b is already at a point in the technology where the base resistance thermal noise is overshadowed by the shot noise contributions, which then set the lowest phase noise attainable [86]. The frequency pushing characteristics are independent of l_e and V_{core} (i.e., similar linear sensitivity), as shown in Figure 62. The linear frequency tuning range is also independent of l_e, as shown in Figure 63. However, a higher linear tuning constant can be obtained as l_e scales down.

6.5 Summary

In this chapter, the impact of emitter scaling and device biasing on various MMW SiGe HBT VCO performance metrics were experimentally explored using fully integrated Colpitts oscillators implemented with 200 GHz SiGe HBTs. The observed VCO performance trends are explained through transistor measurements. This device-circuit interactions study yielded design insights for optimizing MMW SiGe HBT VCO performance.

CHAPTER VII

THE STUDY OF PROTON RADIATION ON MMW SIGE HBT TRANSCEIVER BUILDING BLOCKS

7.1 Introduction

A monolithically integrated MMW SiGe HBT transceiver operating in the 60 GHz ISM band is being developed with 200 GHz SiGe HBTs [94], [95]. In addition to short-range terrestrial wireless broadband applications, such a transceiver can also find application in inter-satellite communication links. This chapter presents, for the first time, experimental results on the effects of proton radiation on critical building blocks for such a MMW SiGe HBT transceiver.

7.2 Experiment

The goal of this work is to carefully assess the impact of radiation exposure on 60 GHz SiGe HBT transceiver building blocks implemented with 200 GHz SiGe HBTs [89], and use an additional transistor-level radiation experiment to better understand the observed circuit response. Two key building blocks are chosen for this study: one is the LNA, which is used to amplify the received signals while adding minimal noise, and the other is the VCO, which is used to generate LO signals for up- and down-conversion mixers. Each SiGe HBT circuit was designed, laid out, fabricated, and characterized before and after being irradiated, along with SiGe HBT *dc* and *ac* test structures needed for correlating changes in circuit performances back to device parameters.

Since extremely few samples of the 60 GHz SiGe HBT LNA and VCO were available, only one sample of each circuit was irradiated, along with two samples of *dc* test structures

and two samples of *ac* test structures, with each sample containing multiple devices. The samples were irradiated with 63.3 MeV protons at the Crocker Nuclear Laboratory at the University of California at Davis. The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup. Tantalum (Ta) scattering foils located several meters upstream of the target establish a beam spatial uniformity of 15% over a 2.0 cm radius circular area. Beam currents from about 20 nA to 100 nA allow testing with proton fluxes from 1.0×10^9 to 1.0×10^{12} proton/cm^{2}sec. The dosimetry system has been previously described [96], [97], and is accurate to about 10%. At proton fluences of 1.0×10^{12} and 5.0×10^{13} p/cm^2, the measured equivalent gamma dose was approximately 135 and 6,759 krad(Si), respectively. The SiGe HBT *dc* test structures, *ac* test structures, and circuits were irradiated with all terminals floating. Previous studies have shown that this has minimal effect on the transistor-level radiation response [98]. All samples were irradiated to a proton fluence of 5.0×10^{13} p/cm^2, while the *ac* test structures were re-irradiated with another proton fluence of 5.0×10^{13} p/cm^2 resulting in a net fluence of 1.0×10^{14} p/cm^2. Since proton radiation causes both ionization damage and displacement damage, the two cannot be easily separated without further neutron and gamma ray experiments.

7.3 Transistor-Level Response

Measurements of the SiGe HBT *dc* and *ac* test structures were made to quantify the transistor-level radiation response. Only the results of the device with standard emitter area of 0.12×2.5 μm^2 are presented, as similar trends were observed in devices with other emitter areas.

7.3.1 SiGe HBT *dc* Response

Proton tolerance of pre-production 200 GHz SiGe HBTs has previously been reported in [99]. The SiGe HBTs used in this investigation represent an improved version to the one examined in [99], this time with an optimized ideal base current, reduced base resistance,

and improved noise performance. The measured forward and inverse mode Gummel characteristics of the 200 GHz SiGe HBTs, shown in Figures 64 and 65, respectively, reveals a remarkably minor degradation of the base current at a few Mrad(Si). As has been previously discussed in [100], the base current degradation in the forward mode is caused by the proton-induced G/R centers located at the emitter-base (EB) spacer edge, where as the base current degradation in the inverse mode is caused by the proton-induced G/R centers located at the shallow trench isolation (STI) edge. Figure 66 shows the schematic cross section of the 200 GHz SiGe HBTs, highlighting the two oxide regions that are damaged during exposure to ionizing radiation.

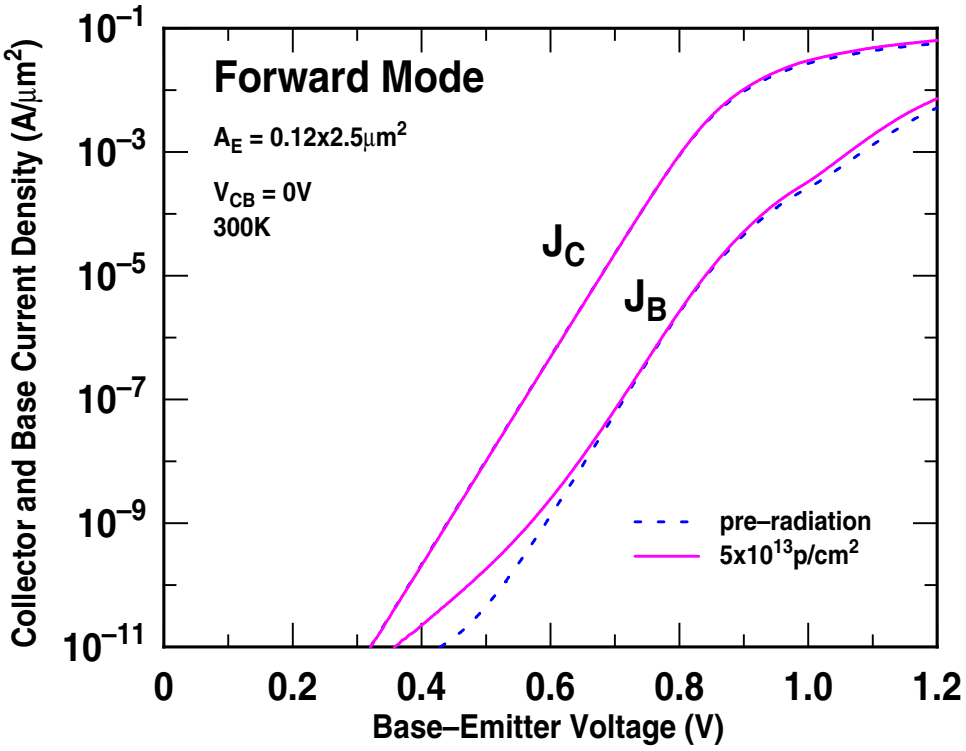


Figure 64: Measured pre- and post-irradiated forward mode Gummel characteristics of the 200 GHz SiGe HBTs.

7.3.2 SiGe HBT *ac* Response

The transistor S parameters were measured from 1 to 45 GHz at each bias point and subsequently deembedded using an "open-short" method. The current gain (h_{21}), Mason's

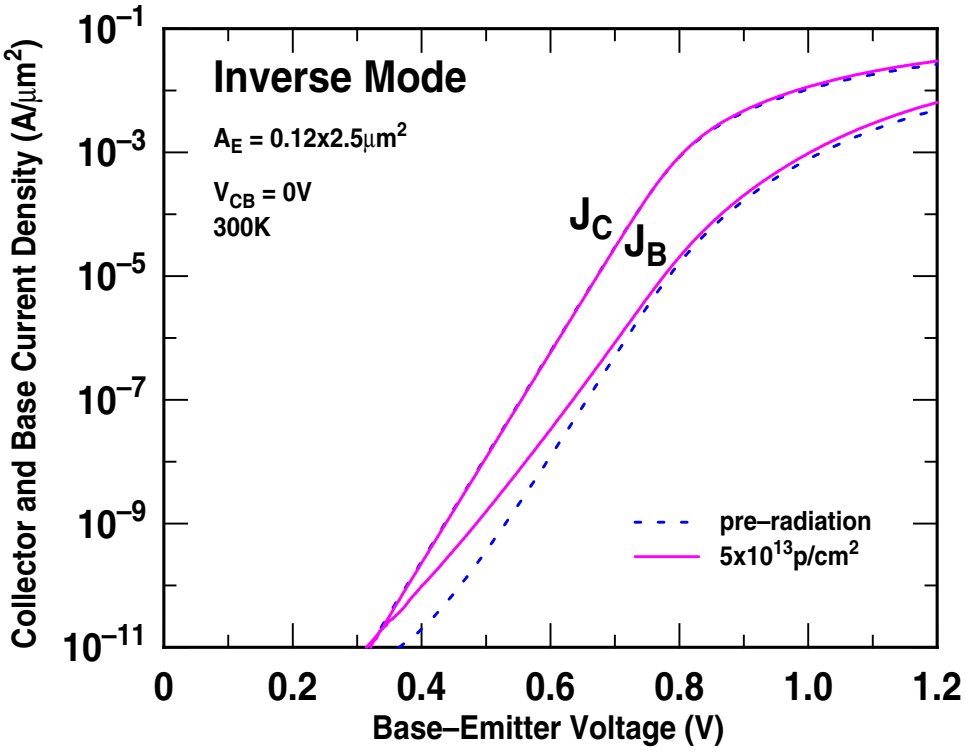


Figure 65: Measured pre- and post-irradiated inverse mode Gummel characteristics of the 200 GHz SiGe HBTs.

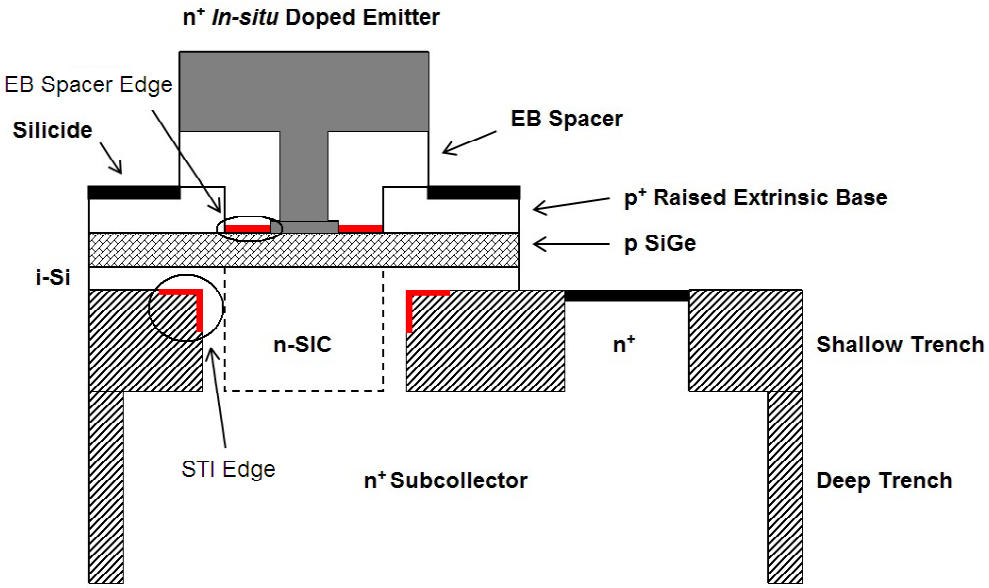


Figure 66: Schematic cross section of the 200 GHz SiGe HBTs showing the two damage regions during exposure to ionizing radiation.

unilateral gain (U), and r_b were then calculated from the deembedded S parameters. The f_T and f_{max} were extrapolated from h_{21} and Mason's U with a -20 dB/decade slope line to 0 dB. Typical pre- and post-radiation deembedded S parameters biased at peak f_T are shown in Figure 67, the associated h_{21} and Mason's U are shown in Figure 68, and the extracted r_b is shown in Figure 69. The extrapolated f_T and f_{max} up to 1.0×10^{14} p/cm^2 proton fluences are shown in Figure 70. Only slight variations were observed between the pre- and post-irradiated results. The most apparent proton-induced device degradation lies in the increase of r_b in Figure 69, presumably caused by displacement effects in the neutral base region and the deactivation of boron dopants. Clearly, these 200 GHz SiGe HBTs are remarkably hard to proton radiation at the transistor-level without any intentional hardening.

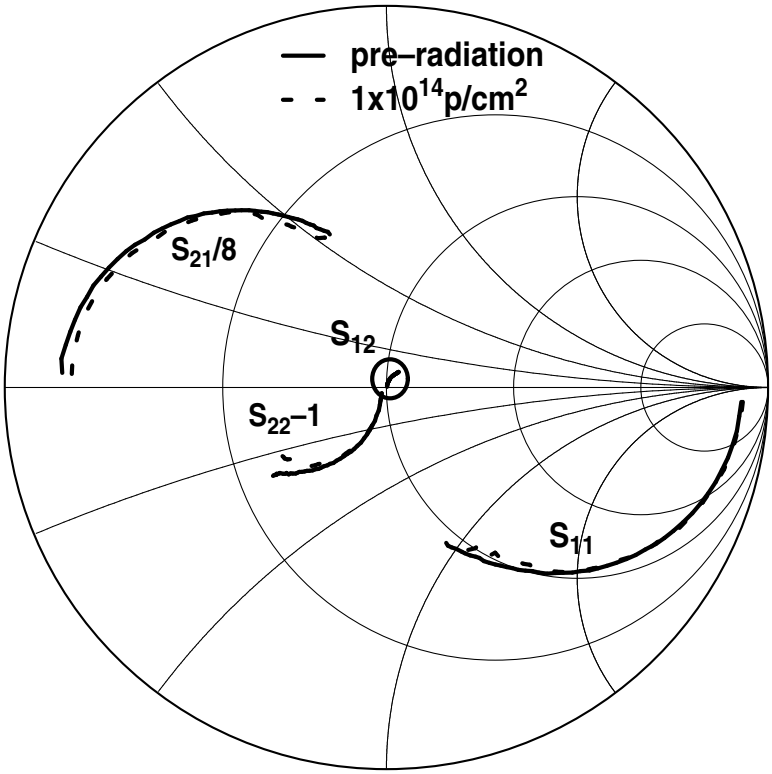


Figure 67: Deembedded pre- and post-irradiated S parameters of the 200 GHz SiGe HBTs biased at peak f_T.

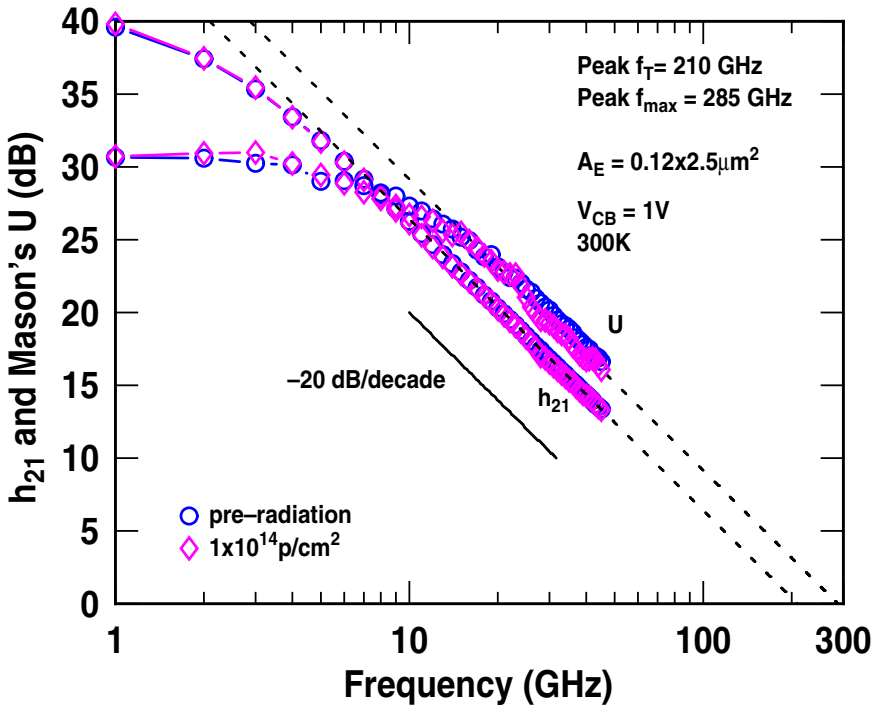


Figure 68: Measured pre- and post-irradiated h_{21} and Mason's U versus frequency of the 200 GHz SiGe HBTs biased at peak f_T.

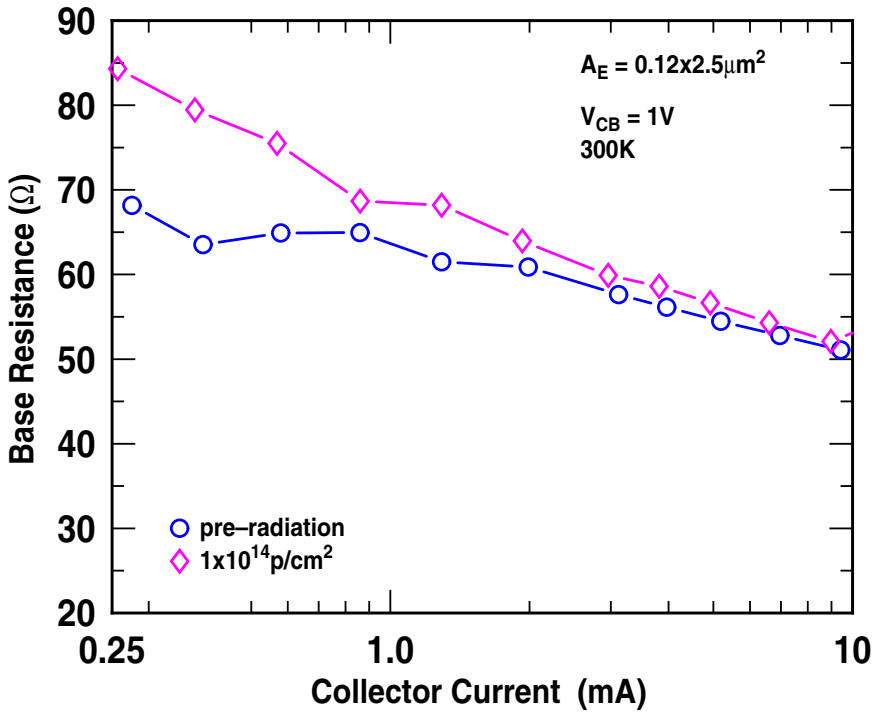


Figure 69: Extracted pre- and post-irradiated r_b versus collector current of the 200 GHz SiGe HBTs.

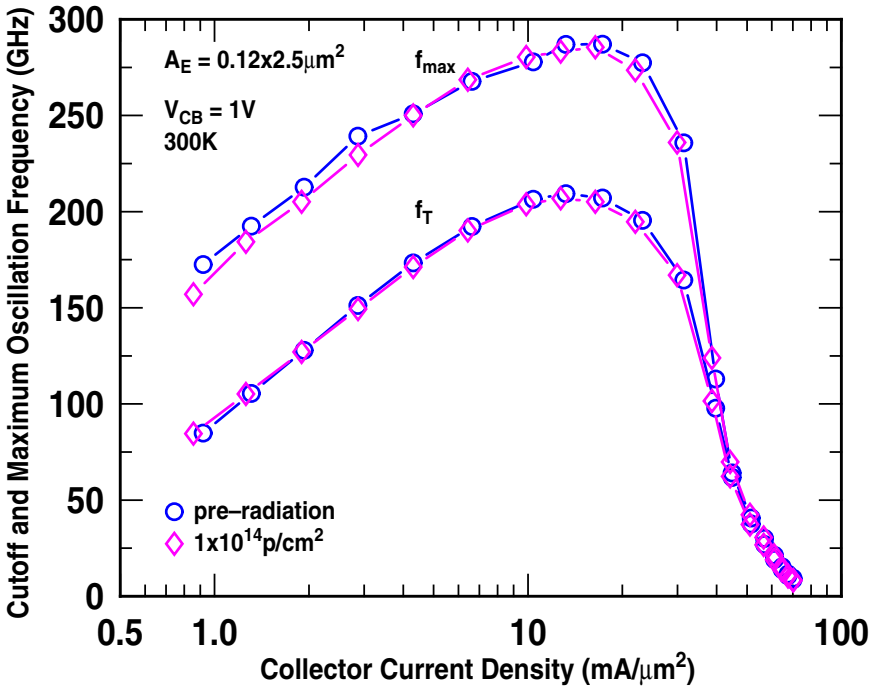


Figure 70: Extrapolated pre- and post-irradiated f_T and f_{max} versus collector current density of the 200 GHz SiGe HBTs.

7.4 Circuit-Level Response

7.4.1 SiGe HBT LNA Response

The 60 GHz SiGe HBT LNA, whose schematic is shown in Figure 71, employs a two-stage architecture using microstrips [95]. The LNA gain is adjustable by changing the second-stage bias current. The fabricated 60 GHz SiGe HBT LNA, shown in Figure 72, occupies 0.92 × 0.57 mm^2. The pre- and post-irradiated gain and *NF* of the 60 GHz SiGe HBT LNA are shown in Figure 73 and 74, respectively. The ripple in *NF* (Figure 74) is attributed to the measurement setup rather than to the LNA itself. The LNA gain decreased by 0.5 dB, *NF* increased by 0.4 dB, S_{11} remained unchanged, and S_{22} increased by 1.5 dB. Detailed results are summarized in Table 7.

The proton-induced changes in the 60 GHz SiGe HBT LNA performance are minor, proving that it is robust from a proton radiation perspective for space applications. The increase in S_{22} may be attributed to the effects of proton radiation on the microstrips and

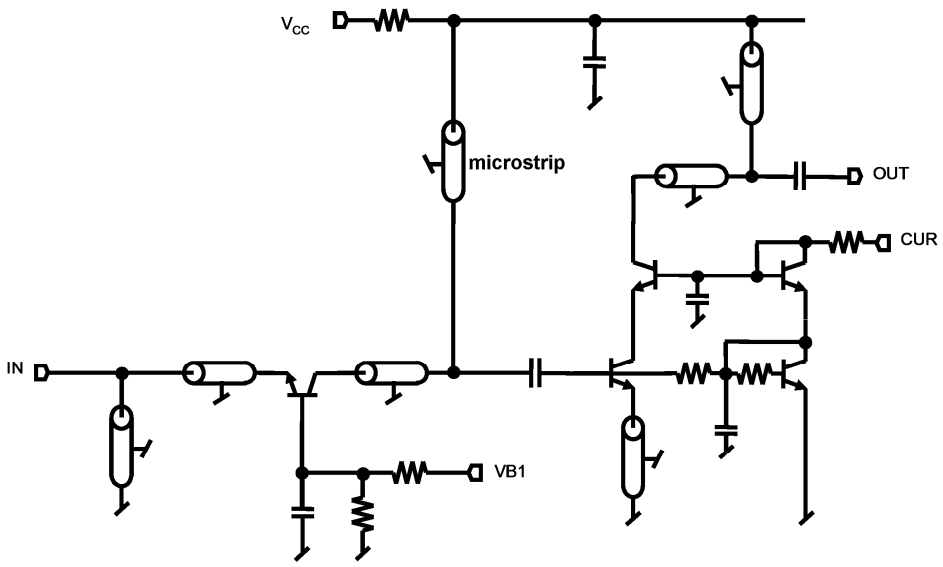


Figure 71: Simplified schematic of the 60 GHz SiGe HBT LNA.

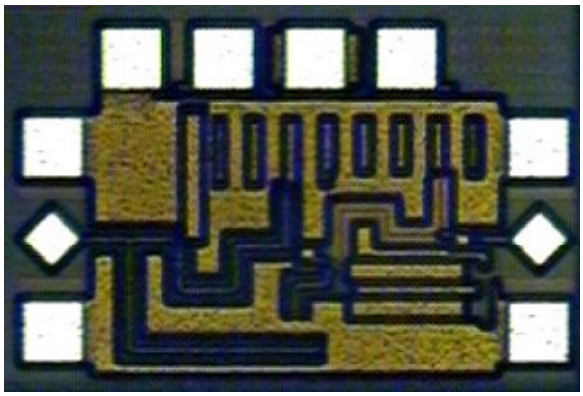


Figure 72: Chip micrograph of the 60 GHz SiGe HBT LNA.

the SiGe HBTs, yet the LNA remains well-matched to 50 Ω. The degradation in gain may be attributed to the slight decrease in S_{21} (Figure 67) of the 200 GHz SiGe HBTs after radiation. The increase in *NF* may be attributed to the increase in r_b (Figure 69) of the 200 GHz SiGe HBTs, which adds directly to the *NF* of the LNA.

7.4.2 SiGe HBT VCO Response

The 60 GHz SiGe HBT VCO, whose schematic is shown in Figure 75, employs a differential Colpitts architecture with microstrips and base-collector junction varactors [95].

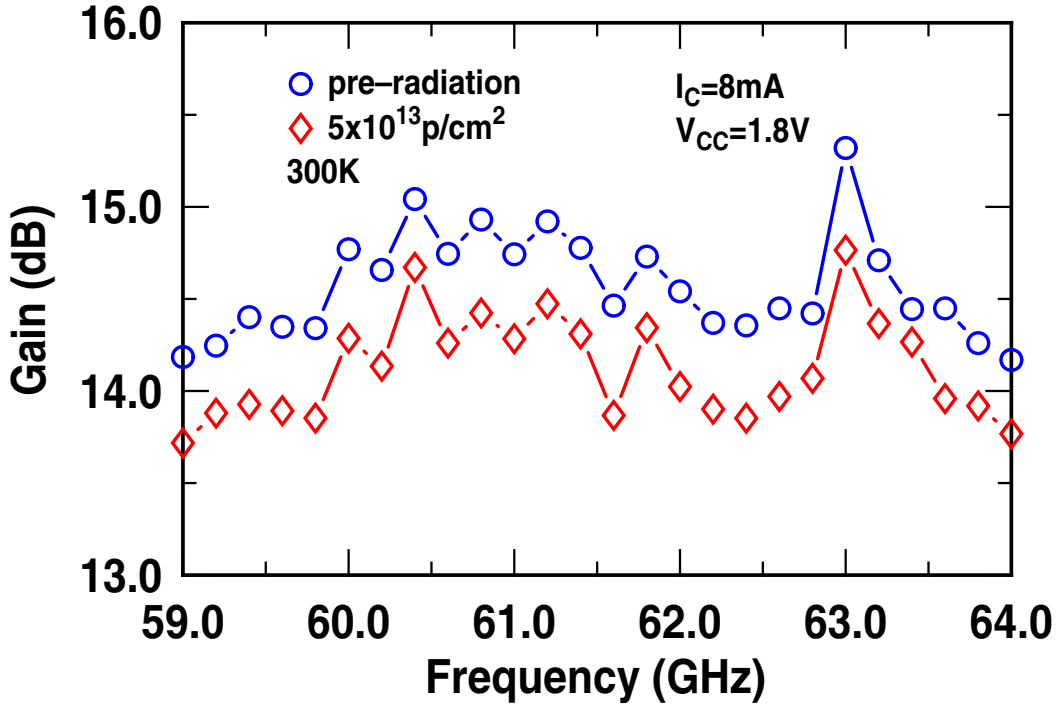


Figure 73: Measured pre- and post-irradiated gain of the 60 GHz SiGe HBT LNA.

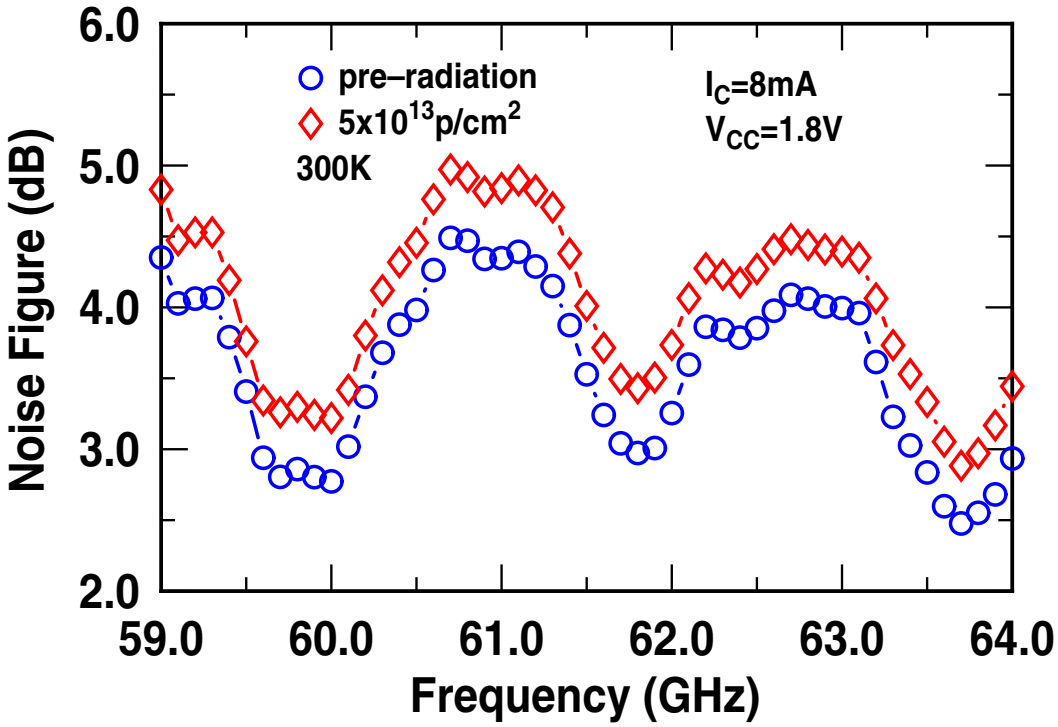


Figure 74: Measured pre- and post-irradiated *NF* of the 60 GHz SiGe HBT LNA.

Table 7: Performance summary of the pre- and post-irradiated 60 GHz SiGe HBT LNA.

Parameters	Pre-Radiation	Post-Radiation	Units
Frequency	61.5	61.5	GHz
Gain	14.5	14.0	dB
Mean *NF*	3.6	4.0	dB
S_{11}	-6.0	-6.0	dB
S_{22}	-18.0	-16.5	dB
V_{CC}	1.8	1.8	V
I_C	8	8	mA

The fabricated 60 GHz SiGe HBT VCO, shown in Figure 76, occupies 0.9×0.6 mm^2. The pre- and post-irradiated output power spectrum of the 60 GHz SiGe HBT VCO are shown in Figures 77 and 78, respectively. The VCO operating frequency shifted 0.3 GHz while the phase noise (L) degraded 2 to 5 dB at 1 MHz offset. Detailed results are summarized in Table 8.

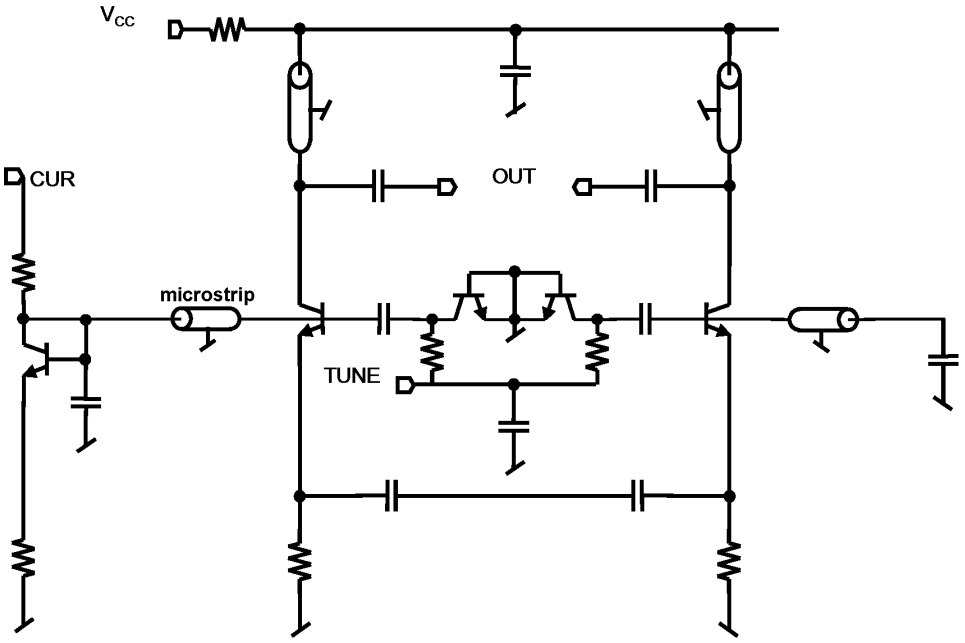


Figure 75: Simplified schematic of the 60 GHz SiGe HBT VCO.

The proton-induced changes in the 60 GHz SiGe HBT VCO performance are minor,

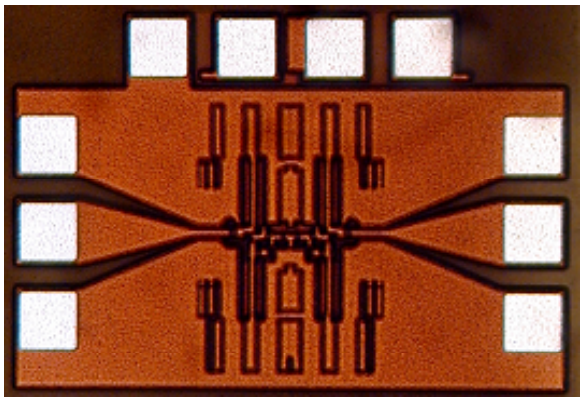


Figure 76: Chip micrograph of the 60 GHz SiGe HBT VCO.

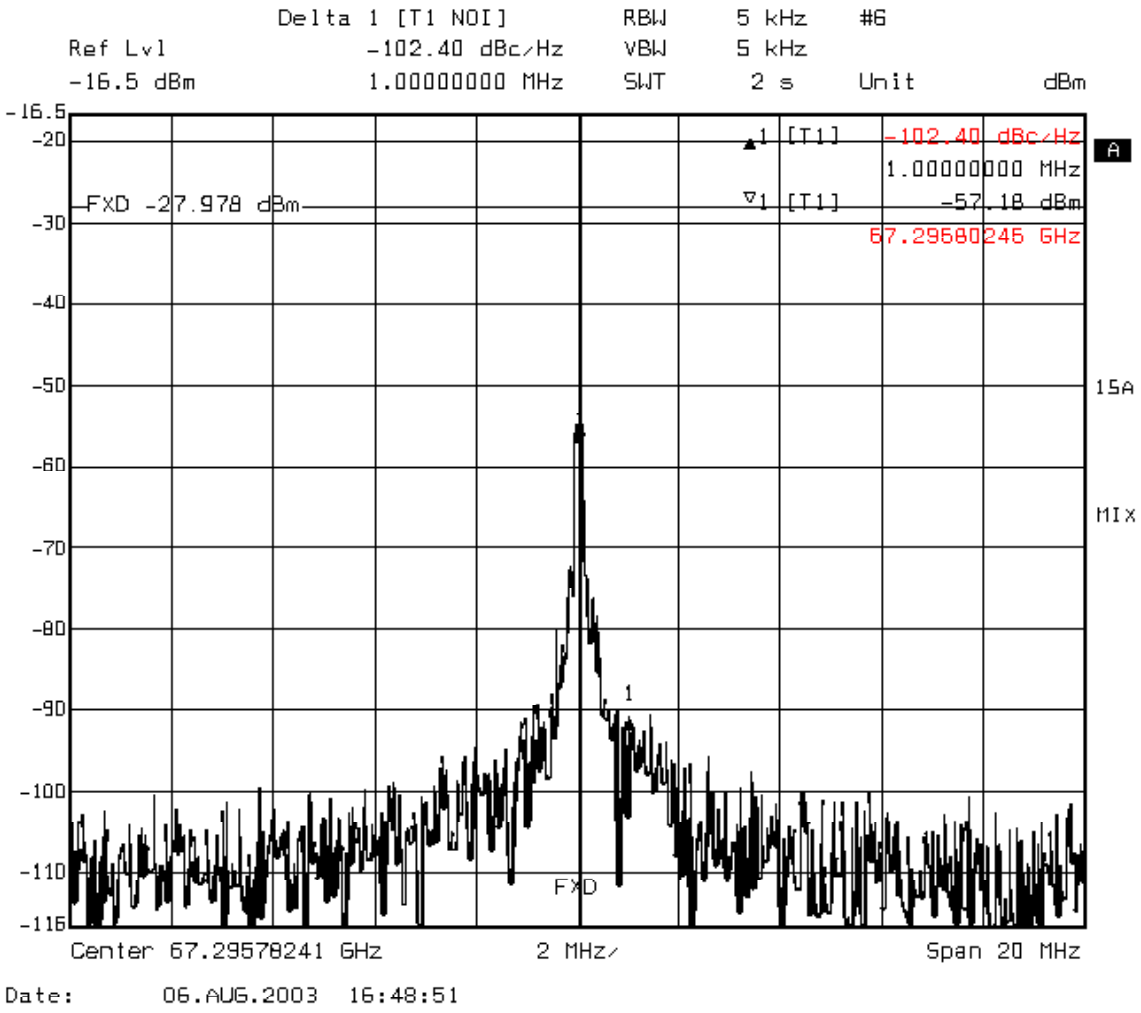


Figure 77: Measured output power spectrum of the pre-irradiated 60 GHz SiGe HBT VCO.

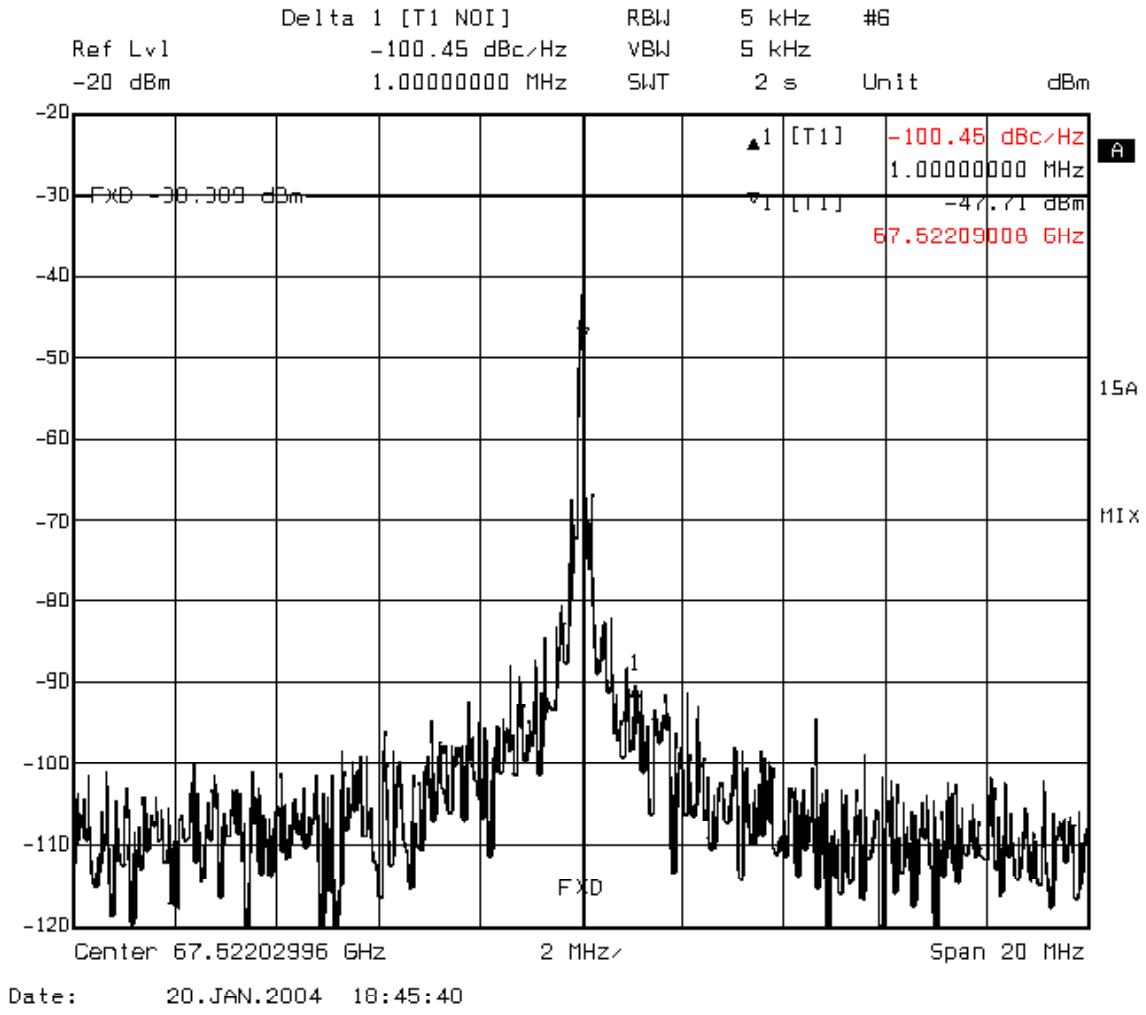


Figure 78: Measured output power spectrum of the post-irradiated 60 GHz SiGe HBT VCO.

Table 8: Performance summary of the pre- and post-irradiated 60 GHz SiGe HBT VCO.

Parameters	Pre-Radiation	Post-Radiation	Units
Frequency	65.8 to 67.9	65.5 to 67.6	GHz
P_{out}	-11	-11	dBm
L(1 MHz)	-98 to -102	-93 to -100	dBc/Hz
V_{CC}	3	3	V
I_C	8	8	mA

proving that it is robust from a proton radiation perspective for space applications. The shift in operating frequency may be attributed to the effects of proton radiation on the microstrips

and the base-collector junction varactors that form the tank of the VCO, as well as on the 200 GHz SiGe HBTs. The degradation in phase noise may be attributed to an increase in the SiGe HBT low-frequency noise [101] that is up-converted into phase noise. Similar observations were made in [98], but in that case on a 5 GHz VCO using a first-generation SiGe HBT technology.

7.5 Summary

The effects of 63.3 MeV proton radiation on 60 GHz SiGe HBT transceiver building blocks implemented with 200 GHz SiGe HBTs have been investigated here for the first time. A 60 GHz SiGe HBT LNA and VCO were irradiated to proton fluences of 5.0×10^{13} p/cm^2. The degradation associated with these extreme proton fluences is found to be minor, suggesting that the MMW SiGe HBT transceivers should be robust to proton radiation for space applications.

CHAPTER VIII

CONCLUSION AND FUTURE WORK

The contributions of this research are:

1. Implemented a 1.36 dB mean *NF* X-band SiGe HBT LNA for radar applications. To the best of the author's knowledge, this LNA achieves the lowest *NF* of any LNA in Si-based technology at X-band (Chapter II, also published in [1]).

2. Implemented sub-2.5 dB *IL* shunt and series/shunt X-band Si CMOS SPDT switches. The switches performed as well as other CMOS switches using more complicated designs or non-standard processes (Chapter III, also published in [2]).

3. Implemented a 2.5 mW X-band SiGe HBT LNA. The low-power performance of this LNA, together with its natural total-dose radiation immunity, demonstrates the potential of SiGe HBT BiCMOS technology for near-space radar applications (Chapter IV, also published in [3]).

4. Implemented a 32 GHz inductorless SiGe HBT ring oscillator. The high-frequency operation demonstrates the potential of inductorless ring oscillators for MMW applications (Chapter V, also published in [4]).

5. Studied the effects of emitter scaling and device biasing on MMW SiGe HBT VCO performance. The design tradeoffs associated with device-circuit interaction are experimentally examined in detail (Chapter VI, also published in [5]).

6. Studied the effects of proton radiation on MMW SiGe HBT transceiver building blocks. The performance degradations are found to be minimal, suggesting that such SiGe HBT transceivers should be robust from a proton tolerance perspective

for space applications, without intentional hardening at either the device- or circuit-level (Chapter VII, also published in [6]).

In the future, this work can be extended by:

1. Investigating the input power handling capabilities of the ultra-low-noise X-band SiGe HBT LNA presented in Chapter II to determine whether a limiter is necessary to protect it from high-power inputs.
2. Investigating the cryogenic noise performance of the ultra-low-noise X-band SiGe HBT LNA presented in Chapter II for possible radio astronomy applications.
3. Investigating methods to further reduce *IL* of the low-loss Si CMOS SPDT switches presented in Chapter III.
4. Investigating substrate coupling issues associated with the integration of various SiGe HBT BiCMOS T/R module circuit blocks onto a single chip.
5. Investigating SiGe HBT BiCMOS LNA topologies to further minimize power consumption for near-space and space radar applications.
6. Investigating methods of improving phase noise in inductorless SiGe HBT ring oscillators.
7. Investigating the device-circuit performance interactions of various MMW SiGe HBT transceiver building blocks.
8. Investigating the impact of proton, neutron, and gamma ray radiation exposure on various MMW SiGe HBT transceiver building blocks.

REFERENCES

[1] W.-M.L. Kuo, Q. Liang, J.D. Cressler, and M.A. Mitchell, "An X-band SiGe LNA with 1.36 dB mean noise figure for monolithic phased array transmit/receive radar modules," in *IEEE Radio Frequency Integrated Circuits Symposium Dig.*, 2006, pp. 549-552.

[2] W.-M.L. Kuo, J.P. Comeau, J.M. Andrews, J.D. Cressler, and M.A. Mitchell, "A comparison of shunt and series/shunt *n*MOSFET single-pole double-throw switches for X-band phased array radar T/R modules," accepted at the Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2007.

[3] W.-M.L. Kuo, R. Krithivasan, X. Li, Y. Lu, J.D. Cressler, H. Gustat, and B. Heinemann, "A low-power, X-band SiGe HBT low-noise amplifier for near-space radar applications," *IEEE Microwave Wireless Compon. Lett.*, vol. 16, pp. 520-522, Sep. 2006.

[4] W.-M.L. Kuo, J.D. Cressler, Y.-J.E. Chen, and A.J. Joseph, "An inductorless Ka-band SiGe HBT ring oscillator," *IEEE Microwave Wireless Compon. Lett.*, vol. 15, pp. 682-684, Oct. 2005.

[5] W.-M.L. Kuo, Y.-J.E. Chen, J.D. Cressler, and G. Freeman, "Effects of emitter scaling and device biasing on millimeter-wave VCO performance in 200 GHz SiGe HBT technology," in *Proc. Asia-Pacific Microwave Conference*, 2005, pp. 852-855.

[6] W.-M.L. Kuo, Y. Lu, B.A. Floyd, B.M. Haugerud, A.K. Sutton, R. Krithivasan, J.D. Cressler, B.P. Gaucher, P.W. Marshall, R.A. Reed, and G. Freeman, "Proton radiation response of monolithic millimeter-wave transceiver building blocks implemented in 200 GHz SiGe technology," *IEEE Trans. Nucl. Sci.*, vol. 51, pp. 3781-3787, Dec. 2004.

[7] Telecommunications Industry Association Press Release, "International telecommunications market expected to continue double digit growth rates reaching over $2 trillion in 2008," Jul. 13, 2005. [Online]. Available: http://www.tiaonline.org/media/press_releases/index.cfm?parelease=05-42. [Accessed Sep. 21, 2005].

[8] Telecommunications Industry Association Press Release, "Spending in U.S. telecom industry rises 7.9% to $784.5 billion in 2004," Feb. 1, 2005. [Online]. Available: http://www.tiaonline.org/media/press_releases/index.cfm?parelease=05-03. [Accessed Sep. 21, 2005].

[9] Telecommunications Industry Association Press Release, "U.S. wireless market to reach $212.5 billion by 2008," Feb. 10, 2005. [Online]. Available:

http://www.tiaonline.org/media/press_releases/index.cfm?parelease=05-05. [Accessed Sep. 21, 2005].

[10] Telecommunications Industry Association Press Release, "U.S. wireless handset revenue on the rise," Mar. 17, 2005. [Online]. Available: http://www.tiaonline.org/media/press_releases/index.cfm?parelease=05-14. [Accessed Sep. 21, 2005].

[11] Telecommunications Industry Association Press Release, "Wi-Fi and WiMAX key drivers of wireless equipment spending, with market reaching $29.3 billion by 2008," Apr. 21, 2005. [Online]. Available: http://www.tiaonline.org/media/press_releases/index.cfm?parelease=05-24. [Accessed Sep. 21, 2005].

[12] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: prospects and future directions," *IEEE Commun. Mag.*, vol. 40, pp. 140-147, Jan. 2002.

[13] B. Gaucher, T. Beukema, S. Reynolds, B. Floyd, T. Zwick, U. Pfeiffer, D. Liu, J. Cressler, "MM-wave transceivers using SiGe HBT technology," in *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems Dig. Papers*, 2004, pp. 81-84.

[14] A.K. Oki, D.C. Streit, R. Lai, A. Gutierrez-Aitken, Y.C. Chen, R. Grundbacher, P.C. Grossman, T. Block, P. Chin, M. Barsky, D. Sawdai, M. Wojtowicz, E. Kaneshiro, and H.C. Yen, "InP HBT and HEMT technology and applications," in *Proc. International Conference on Indium Phosphide and Related Materials*, 2000, pp. 7-8.

[15] M. Kärkkäinen, M. Varonen, J. Riska, P. Kangaslahti, and V. Porra, "A set of integrated circuits for 60 GHz radio front-end," in *IEEE MTT-S International Microwave Symposium Dig.*, 2002, pp. 1273-1276.

[16] Y. Mimino, K. Nakamura, Y. Hasegawa, Y. Aoki, S. Kuroda, and T. Tokumitsu, "A 60 GHz millimeter-wave MMIC chipset for broadband wireless access system front-end," in *IEEE MTT-S International Microwave Symposium Dig.*, 2002, pp. 1721-1724.

[17] K. Fujii, M. Adamski, P. Bianco, D. Gunyan, J. Hall, R. Kishimura, C. Lesko, M. Schefer, S. Hessel, H. Morkner, and A. Niedzwiecki, "A 60 GHz MMIC chipset for 1-Gbit/s wireless links," in *IEEE MTT-S International Microwave Symposium Dig.*, 2002, pp. 1725-1728.

[18] O. Vaudescal, B. Lefebvre, V. Lehoué, and P. Quentin, "A highly integrated MMIC chipset for 60 GHz broadband wireless applications," in *IEEE MTT-S International Microwave Symposium Dig.*, 2002, pp. 1729-1732.

[19] D. Yamauchi, R. Quon, Y.-H. Chung, M. Nishimoto, C. Romo, J. Swift, R. Grundbacher, D. Lee, and L. Liu, "A compact transceiver for wide bandwidth and high power K-, Ka-, and V-band applications," in *IEEE MTT-S International Microwave Symposium Dig.*, 2003, pp. 2015-2018.

[20] A. Yamada, E. Suematsu, K. Sato, M. Yamamoto, and H. Sato, "60GHz ultra compact transmitter/receiver with a low phase noise PLL-oscillator," in *IEEE MTT-S International Microwave Symposium Dig.*, 2003, pp. 2035-2038.

[21] K. Ohata, K. Maruhashi, M. Ito, S. Kishimoto, K. Ikuina, T. Hashiguchi, K. Ikeda, and N. Takahashi, "1.25Gbps wireless gigabit ethernet link at 60GHz-band," in *IEEE Radio Frequency Integrated Circuits Symposium Dig.*, 2003, pp. 509-512.

[22] "Transmit/receive modules," class notes for *Phased Array Antennas for Radar and Communications*, Continuing Education, Georgia Institute of Technology, Mar. 11-14, 2003.

[23] N. Fourikis, *Advanced Array Systems, Applications and RF Technologies*. London, UK: Academic Press, 2000.

[24] R. Tang and R.W. Burns, "Array technology," *Proc. IEEE*, vol. 80, pp. 173-182, Jan. 1992.

[25] M. Mitchell and T. Wallace, "Low power density arrays," presented at 50th Annual Tri-Service Radar Symposium, Albuquerque, NM, 2004.

[26] M.A. Mitchell, T. Wallace, M. Harris, J.D. Cressler, J. Comeau, J. Andrews, L. Kuo, M. Morton, J. Papapolymerou, B. Parks, and G. Wilson, "Feasibility of T/R module functionality in a single SiGe IC," presented at Radio Frequency Module Manufacturing Workshop, Huntsville, AL, 2005.

[27] T. Wallace, "T/R module design for a low power density array," Air and Missile Defense Division, Georgia Tech Research Institute, Memorandum TAT030509, 2004.

[28] B.A. Kopp, "X-band transmit/receive module overview," in *IEEE MTT-S International Microwave Symposium Dig.*, 2000, pp. 705-708.

[29] Y.-B. Jung, S.-Y. Eom, S.-I. Jeon, J.-I. Choi, and H.-K. Park, "The design of T/R module for X-band APAA system used in satellite communications," in *IEEE MTT-S International Microwave Symposium Dig.*, 2002, pp. 1337-1340.

[30] B.A. Kopp, M. Borkowski, and G. Jerinic, "Transmit/receive modules," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 827-834, Mar. 2002.

[31] M. Gloanec, M. Camiade, V. Serru, Z Ouarch, and K. Beilenhoff, "Advanced MMICs for remote sensing and radar applications," in *Proc. 33rd European Microwave Conference*, 2003, pp. 871-874.

[32] U. Hackenberg, M. Adolph, H. Dreher, H. Ott, R. Reber, R. Rieger, and B. Schweizer, "Polarisation agile, highly accurate T/R-module for synthetic aperture radar," in *Proc. 33rd European Microwave Conference*, 2003, pp. 875-878.

[33] M. Mitchell, M. Harris, and J.D. Cressler, "Single chip T/R module," Internal Research and Development, Georgia Tech Research Institute, 2004.

[34] M. Mitchell, "SiGe T/R chip preliminary requirements," Air and Missile Defense Division, Georgia Tech Research Institute, Memorandum STRC050302, 2004.

[35] J.D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Norwood, MA: Artech House, 2003.

[36] H. Kroemer, "Theory of a wide-gap emitter for transistors," *Proc. IRE*, vol. 45, pp. 1535-1537, Nov. 1957.

[37] S.S. Iyer, G.L. Patton, S.S. Delage, S. Tiwari, and J.M.C. Stork, "Silicon-germanium base heterojunction bipolar transistors by molecular beam epitaxy," in *International Electron Devices Meeting Tech. Dig.*, 1987, pp. 874-876.

[38] G.L. Patton, J.H. Comfort, B.S. Meyerson, E.F. Crabbé, G.J. Scilla, E. DeFrésart, J.M.C. Stork, J.Y.-C. Sun, D.L. Harame, and J.N. Burghartz, "75-GHz f_T SiGe-base heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 11, pp. 171-173, Apr. 1990.

[39] D.L. Harame, K. Schonenberg, M. Gilbert, D. Nguyen-Ngoc, J. Malinowski, S.-J. Jeng, B. Meyerson, J.D. Cressler, R. Groves, G. Berg, K. Tallman, K. Stein, G. Hueckel, C. Kermarrec, T. Tice, G. Fitzgibbons, K. Walter, D. Colavito, T. Houghton, N. Greco, T. Kebede, B. Cunningham, S. Subbanna, J.H. Comfort, and E.F. Crabbé, "A 200 mm SiGe-HBT technology for wireless and mixed-signal applications," in *International Electron Devices Meeting Tech. Dig.*, 1994, pp. 437-440.

[40] D. Nguyen-Ngoc, D.L. Harame, J.C. Malinowski, S.J. Jeng, K.T. Schonenberg, M.M. Gilbert, G.D. Berg, S. Wu, M. Soyuer, K.A. Tallman, K.J. Stein, R.A. Groves, S. Subbanna, D.B. Colavito, D.A. Sunderland, and B.S. Meyerson, "A 200 mm SiGe-HBT BiCMOS technology for mixed signal applications," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 1995, pp. 89-92.

[41] D.C. Ahlgren, G. Freeman, S. Subbanna, R. Groves, D. Greenberg, J. Malinowski, D. Nguyen-Ngoc, S.J. Jeng, K. Stein, K. Schonenberg, D. Kiesling, B. Martin, S. Wu, D.L. Harame, and B. Meyerson, "A SiGe HBT BiCMOS technology for mixed-signal RF applications," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 1997, pp. 195-197.

[42] A. Joseph, D. Coolbaugh, M. Zierak, R. Wuthrich, P. Geiss, Z. He, X. Liu, B. Orner, J. Johnson, G. Freeman, D. Ahlgren, B. Jagannathan, L. Lanzerotti, V. Ramachandran, J. Malinowski, H. Chen, J. Chu, P. Gray, R. Johnson, J. Dunn, S. Subbanna, K. Schonenberg, D. Harame, R. Groves, K. Watson, D. Jadus, M. Meghelli, and A. Rylyakov, "A 0.18 μm BiCMOS technology featuring 120/100 GHz (f_T/f_{max}) HBT and ASIC-compatible CMOS using copper interconnect," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2001, pp. 143-146.

[43] B.A. Orner, Q.Z. Liu, B. Rainey, A. Stricker, P. Geiss, P. Gray, M. Zierak, M. Gordon, D. Collins, V. Ramachandran, W. Hodge, C. Willets, A. Joseph, J. Dunn, J.-S. Rieh,

S.-J. Jeng, E. Eld, G. Freeman, and D. Ahlgren, "A 0.13 μm BiCMOS technology featuring a 200/280 GHz f_T/f_{max} SiGe HBT," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2003, pp. 203-206.

[44] B. Heinemann, R. Barth, D. Bolze, J. Drews, P. Formanek, O. Fursenko, M. Glante, K. Glowatzki, A. Gregor, U. Haak, W. Höppner, D. Knoll, R. Kurps, S. Marschmeyer, S. Orlowski, H. Rücker, P. Schley, D. Schmidt, R. Scholz, W. Winkler, and Y. Yamamoto, "A complementary BiCMOS technology with high speed npn and pnp SiGe:C HBTs," in *IEEE International Electron Devices Meeting Tech. Dig.*, 2003, pp. 117-120.

[45] J.-S. Rieh, B. Jagannathan, H. Chen, K. Schonenberg, S.-J. Jeng, M. Khater, D. Ahlgren, G. Freeman, and S. Subbanna, "Performance and design considerations for high speed SiGe HBTs of f_T/f_{max}=375GHz/210GHz," in *Proc. International Conference on Indium Phosphide and Related Materials*, 2003, pp. 374-377.

[46] J.-S. Rieh, D. Greenberg, M. Khater, K.T. Schonenberg, S.-J. Jeng. F. Pagette, T. Adam, A. Chinthakindi, J. Florkey, B. Jagannathan, J. Johnson, R. Krishnasamy, D. Sanderson, C. Schnabel, P. Smith, A. Stricker, S. Sweeney, K. Vaed, T. Yanagisawa, D. Ahlgren, K. Stein, and G. Freeman, "SiGe HBTs for millimeter-wave applications with simultaneously optimized f_T and f_{max} of 300 GHz," in *IEEE Radio Frequency Integrated Circuits Symposium Dig.*, 2004, pp. 395-398.

[47] *International Technology Roadmap for Semiconductors 2005 Edition* (2005). [Online]. Available: http://www.itrs.net/Links/2005ITRS/Home2005.htm. [Accessed Jul. 21, 2006].

[48] J.D. Cressler, "Proposal for SiGe T/R chip," School of Electrical and Computer Engineering, Georgia Institute of Technology, 2004.

[49] J.D. Cressler, "Statement of work for SiGe T/R chip," School of Electrical and Computer Engineering, Georgia Institute of Technology, 2004.

[50] J.D. Cressler, J. Papapolymerou, J. Comeau, L. Kuo, J. Andrews, and M. Morton, "Overview of GEDC SiGe radar designs," presented at SiGe Radar Preliminary Design Review, Atlanta, GA, 2005.

[51] M. Gordon and S.P. Voinigescu, "An inductor-based 52-GHz 0.18 μm SiGe HBT cascode LNA with 22 dB gain," in *Proc. 30th European Solid-State Circuits Conference*, 2004, pp. 287-290.

[52] J.R. Long, "A low-voltage 5.1-5.8-GHz image-reject downconverter RF IC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1320-1328, Sep. 2000.

[53] G. Niu, Q. Liang, J.D. Cressler, C.S. Webster, and D.L. Harame, "RF linearity characteristics of SiGe HBTs," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1558-1565, Sep. 2001.

[54] O. Shana'a, I. Linscott, and L. Tyler, "Frequency-scalable SiGe bipolar RF front-end design," *IEEE J. Solid-State Circuits*, vol. 36, pp. 888-895, Jun. 2001.

[55] S.P. Voinigescu, M.C. Maliepaard, J.L. Showell, G.E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D.L. Harame, "A scalable high-frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1430-1439, Sep. 1997.

[56] V.J. Patel, H.S. Axtell, C.L. Cerny, G.L. Creech, R.G. Drangmeister, M.A. Gouker, T.L. James, A.G. Mattamana, I.O. Mbuko, R.A. Neidhard, E.B. Nykiel, P.L. Orlando, D.L. Selke, J.M. Wiedemann, and T.K. Quach, "X-band low noise amplifier using SiGe BiCMOS technology," in *IEEE Compound Semiconductor Integrated Circuit Symposium Tech. Dig.*, 2005, p. 49-52.

[57] G. Gramegna, A. Magliarisi, and M. Paparo, "An 8.2-GHz, 14.4mW, 1.6dB NF SiGe bipolar LNA with DC current reuse," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2003, pp. 49-52.

[58] D. Zöschg, W. Wilhelm, H. Knapp, M. Wurzer, T.F. Meister, J. Böck, H.-D. Wohlmuth, K. Aufinger, and L. Treitinger, "Monolithic integrated LNAs in silicon-based bipolar technologies," in *Proc. IEEE/AFCEA EUROCOMM 2000. Information Systems for Enhanced Public Safety and Security*, 2000, pp. 400-403.

[59] U. Erben, H. Schumacher, A. Schüppen, H. Dietrich, and J. Arndt, "Application of a production ready SiGe HBT process to 1.9, 5.7 and 10 GHz low noise MMIC's," in *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems Dig. Papers*, 1998, pp. 100-104.

[60] J.P. Comeau, M.A. Morton, J.D. Cressler, J. Papapolymerou, and M. Mitchell, "A high-linearity 5-bit, X-band SiGe HBT phase shifter," in *IEEE MTT-S International Microwave Symposium Dig.*, 2006, pp. 1668-1671.

[61] C. Tinella, J.M. Fournier, D. Belot, and V. Knopik, "A high-performance CMOS-SOI antenna switch for the 2.5-5-GHz band," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1279-1283, Jul. 2003.

[62] F.-J. Huang and K. O, "A 0.5-μm CMOS T/R switch for 900-MHz wireless applications," *IEEE J. Solid-State Circuits*, vol. 36, pp. 486-492, Mar. 2001.

[63] Z. Li and K.K. O, "15-GHz fully integrated nMOS switches in a 0.13-μm CMOS process," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2323-2328, Nov. 2005.

[64] N.A. Talwalkar, C.P. Yue, H. Gan, and S.S. Wong, "Integrated CMOS transmit-receive switch using *LC*-tuned substrate bias for 2.4-GHz and 5.2-GHz applications," *IEEE J. Solid-State Circuits*, vol. 39, pp. 863-870, Jun. 2004.

[65] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin, Y.-T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to

improve power performance," *IEEE Trans. Microwave Theory Tech.*, vol. 54, pp. 31-39, Jan. 2006

[66] T. Ohnakado, S. Yamakawa, T. Murakami, A. Furukawa, E. Taniguchi, H. Ueda, N. Suematsu, and T. Oomori, "21.5-dBm power-handling 5-GHz transmit/receive CMOS switch realized by voltage division effect of stacked transistor configuration with depletion-layer-extended transistors (DETs)," *IEEE J. Solid-State Circuits*, vol. 39, pp. 577-584, Apr. 2004.

[67] Z. Li, H. Yoon, F.-J. Huang, and K.K. O, "5.8-GHz CMOS T/R switches with high and low substrate resistance in a 0.18-μm CMOS process," *IEEE Microwave Wireless Comp. Lett.*, vol. 13, pp. 1-3, Jan. 2003.

[68] A.E. Alving, "SPO overview," presented at 23rd DARPA Systems and Technology Symposium, Anaheim, CA, 2004.

[69] L. Corey, "Tailored tactical surveillance," presented at 23rd DARPA Systems and Technology Symposium, Anaheim, CA, 2004.

[70] P. Chisholm, "Super antennas," Military Information Technology Online Edition, vol. 9, no. 10, Dec. 2005. [Online]. Available: http://www.military-information-technology.com/article.cfm?DocID=1282. [Accessed Feb. 20, 2006].

[71] J.D. Cressler, "On the potential of SiGe HBTs for extreme environment applications," *Proc. IEEE*, vol. 93, pp. 1559-1582, Sep. 2005.

[72] R.K. Montgomery, D.A. Humphrey, R. Hamm, F. Ren, R.J. Malik, R.F. Kopf, A. Tate, P.R. Smith, R.W. Ryan, J. Lin, and Y.K. Chen, "10 and 26 GHz differential VCOs using InP HBTs," in *IEEE MTT-S International Microwave Symposium Dig.*, 1996, pp. 1507-1510.

[73] N. Saniei, H. Djahanshahi, and C.A.T. Salama, "25 GHz inductorless VCO in a 45 GHz SiGe technology," in *IEEE Radio Frequency Integrated Circuits Symposium Dig.*, 2003, pp. 269-272.

[74] W.-M.L. Kuo, J.D. Cressler, Y.-J.E. Chen, and A.J. Joseph, "A compact 21 GHz inductorless differential quadrature ring oscillator implemented in SiGe HBT technology," *Materials Science in Semiconductor Processing*, vol. 8, pp. 445-449, Feb.-Jun. 2005.

[75] H. Djahanshahi, N. Saniei, S.P. Voinigescu, M.C. Maliepaard, and C.A.T. Salama, "A 20-GHz InP-HBT voltage-controlled oscillator with wide frequency tuning range," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1566-1572, Sep. 2001.

[76] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331-343, Mar. 1996.

[77] E.E. Hegazi, J. Rael, and A.A. Abidi, *The Designer's Guide to High-Purity Oscillators*. New York, NY: Kluwer Academic Publishers, 2005.

[78] A. Hajimiri, S. Limotyrakis, and T.H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 790-804, Jun. 1999.

[79] B. Razavi, "A 2-GHz 1.6-mW phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 32, pp. 730-735, May 1997.

[80] B. Razavi, "A 2.5-Gb/s 15-mW clock recovery circuit," *IEEE J. Solid-State Circuits*, vol. 31, pp. 472-480, Apr. 1996.

[81] D.B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, pp. 329-330, Feb. 1966.

[82] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, pp. 179-194, Feb. 1998.

[83] H. Wang, K.-W. Chang, D.C.-W. Lo, L.T. Tran, J.C. Cowles, T.R. Block, G.S. Dow, A. Oki, D.C. Streit, and B.R. Allen, "A 62-GHz monolithic InP-based HBT VCO," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 388-390, Nov. 1995.

[84] H. Li, H.-M. Rein, R.-E. Makon, and M. Schwerd, "Wide-band VCOs in SiGe production technology operating up to about 70 GHz," *IEEE Microwave Wireless Compon. Lett.*, vol. 13, pp. 425-427, Oct. 2003.

[85] B. Van Haaren, M. Regis, O. Llopis, L. Escotte, A. Gruhle, C. Mähner, R. Plana, and J. Graffeuil, "Low-frequency noise properties of SiGe HBT's and application to ultra-low phase-noise oscillators," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 647-652, May 1998.

[86] G. Niu, J. Tang, Z. Feng, A.J. Joseph, and D.L. Harame, "Scaling and technological limitations of $1/f$ noise and oscillator phase noise in SiGe HBTs," *IEEE Trans. Microwave Theory Tech.*, vol. 53, pp. 506-514, Feb. 2005.

[87] Z. Jin, M. Erturk, J.D. Cressler, and A.J. Joseph, "The impact of low-frequency noise variations on the modeling and operation of SiGe circuits," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2005, pp. 192-195.

[88] Y.-J.E. Chen, W.-M.L. Kuo, Z. Jin, J. Lee, Y.V. Tretiakov, J.D. Cressler, J. Laskar, and G. Freeman, "A low-power Ka-band voltage-controlled oscillator implemented in 200-GHz SiGe HBT technology," *IEEE Trans. Microwave Theory Tech.*, vol. 53, pp. 1672-1681, May 2005.

[89] B. Jagannathan, M. Khater, F. Pagette, J.-S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D.R. Greenberg, R. Groves, S.J. Jeng, J. Johnson, E. Mengistu, K.T. Schonenberg, C.M. Schnabel, P. Smith, A. Stricker, D. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, "Self-aligned site NPN transistors with 285 GHz f_{MAX} and 207 GHz f_T in a manufacturable technology," *IEEE Electron Device Lett.*, vol. 23, pp. 258-260, May 2002.

[90] R. Aparicio and A. Hajimiri, "A noise-shifting differential Colpitts VCO," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1728-1736, Dec. 2000.

[91] A. Hajimiri and T.H. Lee, *The Design of Low Noise Oscillators*. Norwell, MA: Kluwer Academic Publishers, 1999.

[92] J.J. Rael and A.A. Abidi, "Physical processes of phase noise in differential LC oscillators," in *Proc. IEEE Custom Integrated Circuits Conference*, 2000, pp. 569-572.

[93] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice Hall PTR, 1998.

[94] B. Gaucher, T. Beukema, S. Reynolds, B. Floyd, T. Zwick, U. Pfeiffer, D. Liu, and J. Cressler, "Silicon monolithic broadband millimeter wave radio technology", in *Proc. International Conference on Space Mission Challenges for Information Technology* , 2003, pp. 113-120.

[95] S. Reynolds, B. Floyd, U. Pfeiffer, and T. Zwick, "60 GHz Transceiver Circuits in SiGe Bipolar Technology," in *IEEE International Solid-State Circuits Conference Dig. Tech. Papers*, 2004, pp. 442-443.

[96] K.M. Murray, W.J. Stapor, and C. Castenada, "Calibrated charged particle radiation system with precision dosimetric measurement and control," *Nuclear Instruments and Methods in Physics Research*, vol. A281, pp. 616-621, Sep. 1989.

[97] P.W. Marshall, C.J. Dale, M.A. Carts, and K.A. LaBel, "Particle-induced bit errors in high performance fiber optic data links for satellite data management," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1958-1965, Dec. 1994.

[98] J.D. Cressler, M.C. Hamilton, R. Krithivasan, H. Ainspan, R. Groves, G. Niu, S. Zhang, Z. Jin, C.J. Marshall, P.W. Marshall, H.S. Kim, R.A. Reed, M.J. Palmer, A.J. Joseph, and D.L Harame, "Proton radiation response of SiGe HBT analog and RF circuits and passives," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 2238-2243, Dec. 2001.

[99] Y. Lu, J.D. Cressler, R. Krithivasan, Y. Li, R.A. Reed, P.W. Marshall, C. Polar, G. Freeman, and D. Ahlgren, "Proton tolerance of third-generation, 0.12 μm 185 GHz SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 1811-1815, Dec. 2003.

[100] J.D. Cressler, R. Krithivasan, G. Zhang, G. Niu, P.W. Marshall, H.S. Kim, R.A. Reed, M.J. Palmer and A.J. Joseph, "An investigation of the origins of the variable proton tolerance in multiple SiGe HBT BiCMOS technology generations," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3203-3207, Dec. 2002.

[101] Z. Jin, G. Niu, J.D. Cressler, C.J Marshall, P.W. Marshall, H.S. Kim, R.A. Reed, and D.L. Harame, "$1/f$ noise in proton-irradiated SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 2244-2249, Dec. 2001.

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