A Fully-Integrated All-Digital Outphasing Transmitter

for Wireless Communications

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2009

A Fully-Integrated All-Digital Outphasing Transmitter

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ACKNOWLEDGEMENTS

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of the proposed research is to present a new all-digital outphasing transmitter IC, a comprehensive explanation of its operation, and its performance characterization. The all-digital transmitter chip leverages flexible digital phase modulators (DPMs) to adaptively compensate for amplifier mismatches. As the DPM uses a digital input to directly modulate the RF phase of each path, the phase control becomes very simple and accurate for power amplifier (PA) gain/phase mismatch compensation. Furthermore, this digital phase modulation scheme also facilitates minimizing the distortion of an RF combiner. It is newly proposed that two distinct digital predistortion algorithms are required for perfect compensation for both PAs and a combiner. All phase calibration values can be adaptively calculated as a function of outphase angle and saved in digital look-up tables to predistort the phase inputs of two DPMs.

Various types of PAs and combiners are investigated to further enhance the performance of the outphasing transmitter. These features are implemented in a chip fabricated in a 0.18-μm CMOS process and evaluated with IEEE 802.16e baseband symbols.

CHAPTER I

INTRODUCTION

The demand for higher data throughput in wireless communications has been increasing at a tremendous rate over the past decade. Figure 1.1 shows the evolution of wireless communication trends with various coverage ranges.
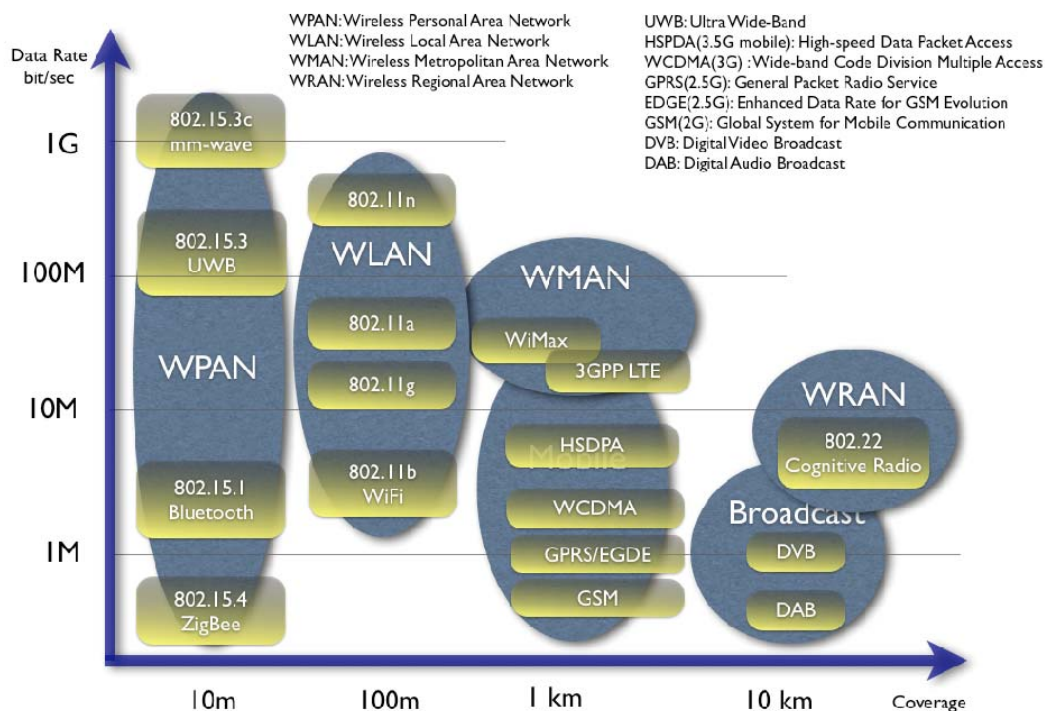
Figure 1.1. Evolution of wireless communications.

As shown in the figure, every new emerging wireless standard requires a higher data rate with more stringent user connectivity. To deal with these requirements, both

spectral and power efficiencies are important factors in modern wireless communication for high-speed data connection and long battery life, respectively.

However, an intrinsic trade-off exists between these two PA design metrics. To increase the spectral efficiency, baseband signals should have complex I/Q symbols, which require both amplitude and phase modulation. Since most amplitude modulated signals have high peak-to-average-power ratio (PAPR), a substantial back-off is generally needed to ensure adequate amplifier linearity; thus the average power efficiency is significantly degraded. For example, orthogonal frequency division multiplexing (OFDM) is very spectrally efficient and mitigates multi-path fading due to its long symbol duration, but one of the major drawbacks of the OFDM system is its sensitivity to nonlinear distortion due to its wide variation in signal envelope and low average power efficiency. Figure 1.2 shows the time-domain waveform of an IEEE802.11g OFDM-Wireless local area network (LAN) signal and its probability density function (PDF) of output power [1].

(a)   (b)
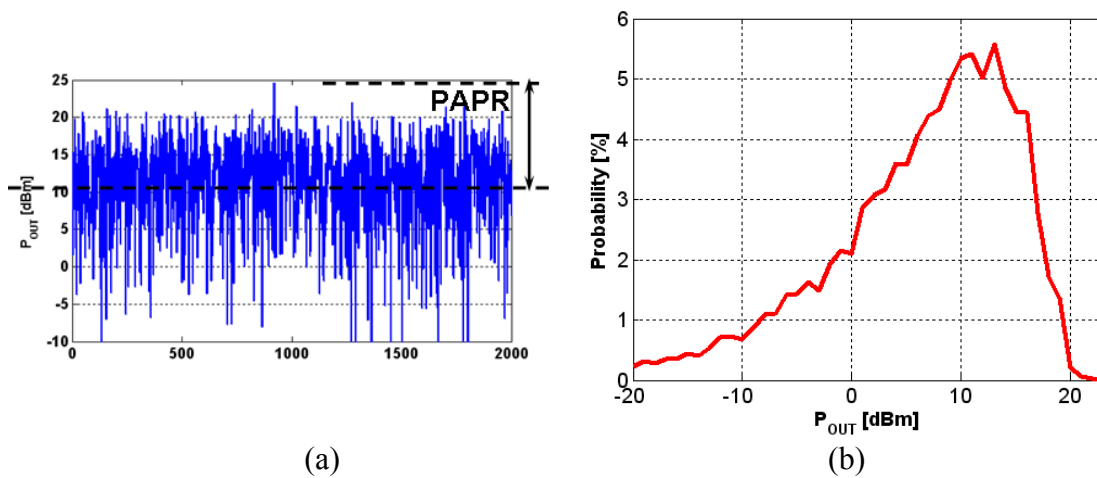
Figure 1.2. Signal profile of OFDM-Wireless LAN. (a) Time-domain signal waveform, (b) PDF of output power.

As shown in the figure, the output power of the OFDM signal is much less than the peak output power at most times. However, PAs, which consumes the largest amount of power in a typical wireless transmitter, tend to be most efficient only when delivering peak output power, while the efficiency degrades with reduced output power. Figure 1.3 shows typical linear PA efficiency graphs.
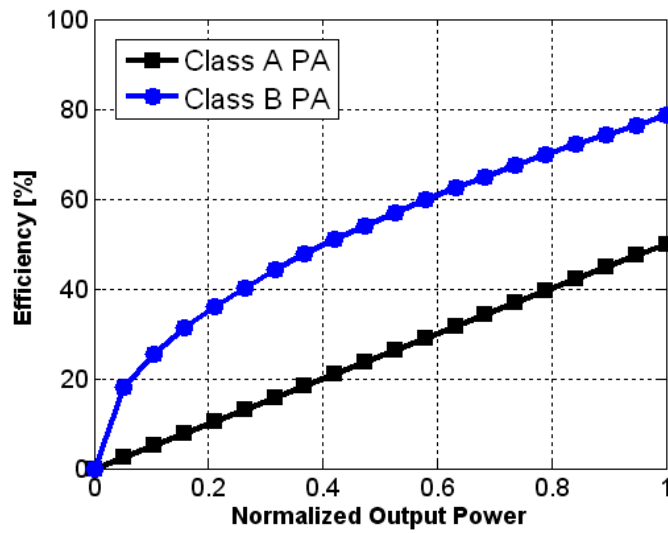
Figure 1.3. Maximum efficiency of ideal Class A and Class B PAs.

Therefore, to support the large PAPR in the OFDM systems, the PAs unfortunately have to spend most of their time in back-off where the efficiency is poor. The average power efficiency of an OFDM system using linear PAs can be calculated by multiplying the PDF of output power by the efficiency profile of linear PA and it is typically much less than 15% in most CMOS PAs; thus most of the system power is dissipated in PA to meet the linearity requirements of an OFDM signal [2].

To resolve efficiency degradation problems in linear PAs, various efficiency enhancement technologies have been proposed. Figure 1.4 compares three major linear amplification techniques. A polar transmitter, also called envelope elimination and restoration (EER), is one of the most promising techniques for improving efficiency. Compared to a Class A PA, the polar transmitter demonstrates a much higher power efficiency. The polar transmitter basically operates by converting complex I/Q symbols into envelope and constant envelope phase signals. The constant envelope signal is amplified through a highly efficient nonlinear PA with a separate envelope control path. However, despite the efficiency improvement, the separate amplitude modulation through a low dropout (LDO) regulator, DC/DC converter, $\Sigma\Delta$ modulator, or PWM has significant bandwidth limitation and efficiency degradation problems in commercial wideband systems [3]-[11].
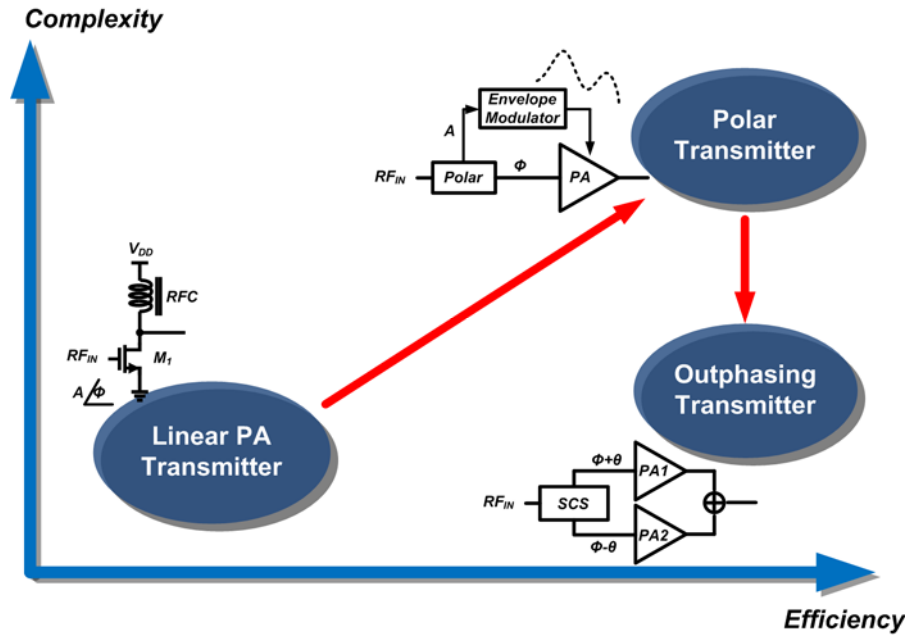
Figure 1.4. Comparison of linear amplification techniques.

The outphasing power amplification, also called linear amplification using nonlinear components (LINC), was proposed as another solution that may offer high efficiency with good linearity [12]. LINC eliminates the high linearity demands on a single PA by summing the outputs of two nonlinear PAs via a power combiner to amplify non-constant envelope signals. This technique produces an amplifier with the linearity of a moderate back-off linear PA at an efficiency approaching that of a switching amplifier. Also, the outphasing transmitter, which uses two simple wideband switching PAs, can be a good solution for highly power efficient and wideband operation. Figure 1.5 shows the efficiency comparison of different linear amplification techniques.
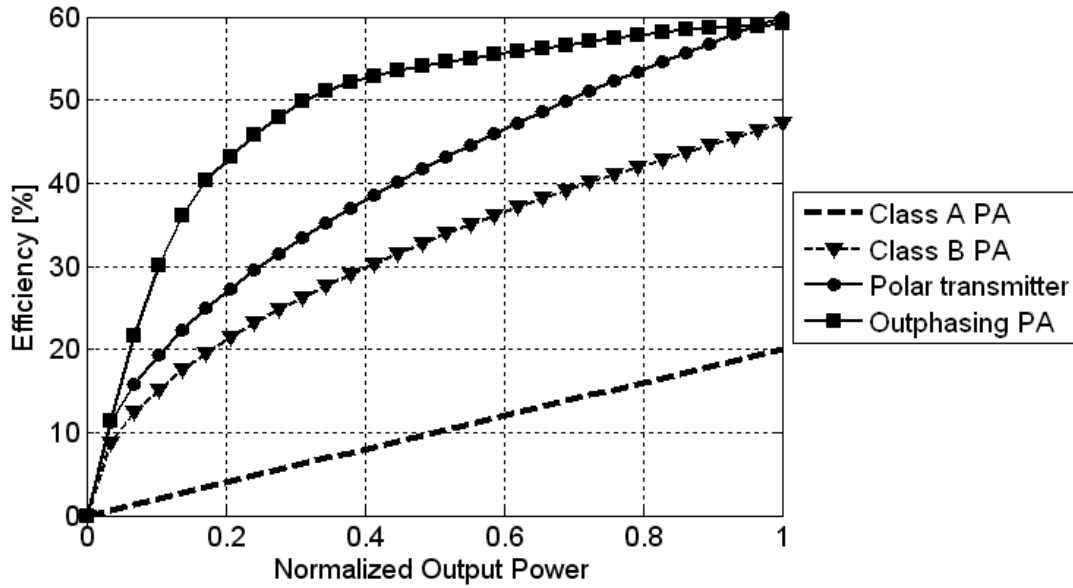
Figure 1.5. Comparison of efficiency with different linear amplification techniques.

The power efficiency of a Class A amplifier decreases with output power P_{out} (relative to its peak value $P_{out,max}$) proportional to $P_{out}/P_{out,max}$. Similarly, for a Class B amplifier, the efficiency varies as $(P_{out}/P_{out,max})^{0.5}$. Class AB amplifiers have output power

variation intermediate between these values. Thus, there is customarily an inherent trade-off between linearity and efficiency in a typical amplifier design [2]. The peak efficiency of a polar transmitter is much higher than that of linear PAs and overall efficiency is mainly determined by the efficiency of the envelope modulator, such as a LDO and DC/DC converter. Also, the outphasing transmitter can provide comparable efficiency with the polar transmitter through PA and combiner optimization. The efficiency curve of the outphasing transmitter will be analyzed in detail.

The goal of this research is to enhance the efficiency at back-off and thus reduce the average power consumption of such systems operating with large PAPR through the outphasing amplification techniques. In this dissertation, a new architecture for an all-digital outphasing transmitter is presented. The transmitter employs a novel DPM, which enables all transmitter blocks other than the switching PAs to operate via digital signals. By modulating the outphase signals digitally, mismatches caused by PAs and the combiner are detected and stored in digital look-up tables for each frequency channel. Furthermore, by modulating phase directly, the proposed outphasing transmitter needs only two kinds of test algorithms for complete mismatch compensation, which is very simple compared to an outphasing transmitter based on a quadrature modulator as used in prior work.

The original contributions and main focus of this dissertation include:

1.   Development of a new all-digital outphasing transmitter architecture with detailed system requirements and error compensation algorithms.

2.   First all-digital outphasing modulator with a 0.18-μm CMOS technology for OFDM signals.

3.   First to introduce a fully-integrated all-digital outphasing transmitter IC with thorough PA and combiner analysis.

This dissertation is organized as follows:

Chapter 1 is an introduction of this dissertation and demonstrates the necessity of highly efficient linear power amplifiers in wireless communications. Following that, the organization of the dissertation is described. In chapter 2, a brief historical background and origin of the problems of an outphasing amplification technique is introduced. In chapter 3, a behavioral model for a new all-digital outphasing transmitter, consisting of dual DPMs and switching power amplifiers, is described in detail. This transmitter architecture not only provides linear amplification of OFDM modulation, but also permits fine phase control for error calibration. The effects of phase quantization on digital modulation error performance are studied. The study confirms the feasibility of an all-digital amplifier approach and demonstrates that modulation specifications can be met using quite modest digital work lengths.

Chapter 4 focuses on real circuit implementation of the all-digital outphasing modulator with a 0.18-μm CMOS technology. Each building block is described with its detailed operating principles. Also, the overall modulator IC performances, such as total power consumption, phase noise results of a frequency synthesizer, and modulation errors, are demonstrated. Chapter 5 describes and analyzes the effects of switching power amplifiers on overall outphasing transmitter efficiency. The average system efficiency mainly depends on the characteristics of power amplifiers; thus various nonlinear

switching PAs are analyzed numerically in an outphasing transmitter. In addition, a fully-integrated all-digital outphasing transmitter IC is presented to verify the PA analysis. Two types of PAs, Class D and Class E, are implemented and integrated with the outphasing modulator presented in chapter 4.

Finally, chapter 6 summarizes the dissertation and provides guidance towards future research possibilities.

CHAPTER II

OUTPHASING AMPLIFICATION

2.1   Principle of Outphasing Amplification

The outphasing amplification technique basically operates by representing an amplitude and phase modulated signal, $S_{IN}(t)$, as the difference of two constant amplitude, phase modulated signals, $S_1(t)$ and $S_2(t)$ [13]. These two signals can then be amplified separately through high efficiency nonlinear switching PAs and recombined to produce the amplified original signal, as shown in Figure 2.1.
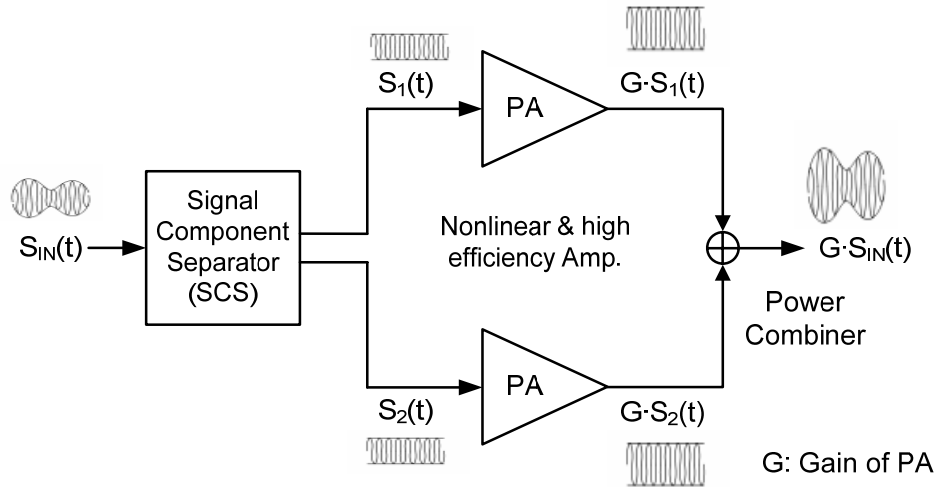
Figure 2.1. Outphasing signal decomposition.

A complex polar representation of the original signal can be written as

$$S_{IN}(t) = \left[S_I(t) + j \cdot S_Q(t) \right] \cdot e^{j\omega_c t} = \left| S_{IN}(t) \right| \cdot e^{j\left[\omega_c \cdot t + \phi(t) \right]}, \tag{2.1}$$

where

$$\left| S_{IN}(t) \right| = \sqrt{S_I^2(t) + S_Q^2(t)} \tag{2.2}$$

$$\phi(t) = tan^{-1}\left(\frac{S_Q(t)}{S_I(t)} \right). \tag{2.3}$$

The original signal can also be expressed by a sum of two phase modulated signals as

$$S_{IN}(t) = S_1(t) + S_2(t) \tag{2.4}$$

$$S_1(t) = A_{max} \cdot e^{j\left[\omega_c \cdot t + \phi(t) + \theta(t) \right]} \tag{2.5}$$

$$S_2(t) = A_{max} \cdot e^{j\left[\omega_c \cdot t + \phi(t) - \theta(t) \right]} \tag{2.6}$$

$$S_{OUT}(t) = G \cdot S_{IN}(t) = G \cdot \left[S_1(t) + S_2(t) \right], \tag{2.7}$$

where G is the gain of each PA and $\theta(t)$ is the outphase angle given by

$$\theta(t) = \cos^{-1}\left(\frac{\left| S_{IN}(t) \right|}{2 \cdot A_{max}} \right) \tag{2.8}$$

and $(2 \cdot A_{max})$ is the peak of the $S_{IN}(t)$ envelope.

From (2.5) and (2.6), both $S_1(t)$ and $S_2(t)$ have only phase information, $\varphi(t)$ and $\theta(t)$. $\varphi(t)$ is the phase of the original baseband symbol and $\theta(t)$ is the additional phase modulated angle related to the outphasing amplification. The block, which calculates this

outphase angle calculation, is called a signal component separator (SCS). The outphasing decomposition and reconstruction can easily be represented by a vector diagram, as shown in Figure 2.2.
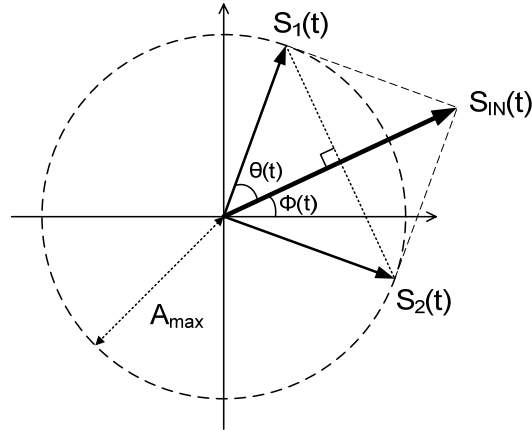
Figure 2.2. Vector representation of outphasing signal decomposition.

For an ideal outphasing amplifier, the two PAs should have identical gain and phase response for linear amplification and operate at saturation, yielding maximum amplifier efficiency. Simultaneously, the power combiner, which is used to combine the output of both PAs, should operate linearly over all the frequency bands of interest with perfect isolation between both inputs. However, both the non-identical responses of PAs and the power combiner's imperfect isolation distort the output signal of the outphasing transmitter. Thus, compensation algorithms for minimizing such distortion are necessary for a useful practical implementation. In this research, simple digital calibration methods using look-up tables are presented, which replace the conventional quadrature modulator with a handy DPM.

2.2   Challenges

Despite the efficiency enhancement, the outphasing topology has not been widely used in commercial amplifiers due to its strict matching requirements both in the phase and amplitude of each path [14][15] and non-isolation distortion and efficiency degradation caused by the RF power combiner [16][17].

2.2.1   Matching Requirements and Mismatch Error Compensation

For an ideal outphasing amplifier, the two PAs should have identical gain and phase response for linear amplification and operate at saturation, yielding maximum amplifier efficiency. Simultaneously, the power combiner, which is used to combine the output of two PAs, should operate linearly over all the frequency bands of interest with perfect isolation between both inputs. However, both the non-identical responses of PAs and the non-isolation properties of a power combiner distort the output signal of the outphasing transmitter. The mathematical analysis to evaluate the effects of the imbalances and the non-isolation distortion on the performance of the outphasing transmitter shows that only a gain imbalance of 0.3~0.4 dB or the phase imbalance of 2~3° can be tolerated [18]. Thus, extremely precise compensation algorithms for minimizing such errors are necessary for a useful practical implementation.

2.2.2   Efficiency Enhancement vs. Linearity

The key advantage of an outphasing system is the ability to maintain a high efficiency and the efficiency mainly depends on the configuration of a power combiner,

which adds the outputs of two nonlinear PAs. There are two kinds of combiner architectures, isolated and non-isolated, as shown in Figure 2.3. An isolated combiner, such as a Wilkinson combiner, provides good linearity, but the out-of-phase components of the combined signals are directed to the isolated resistor load and dissipated when the output power decreases. On the contrary, a non-isolated combiner, such as a Chireix combiner, is a lossless combining structure, which provides much higher combining efficiency than the isolated combiner at the cost of linearity due to the lack of isolation. Thus, to take advantage of the high efficiency, an outphasing system requires the use of a non-isolated combiner with the improved linearity through appropriate calibration algorithms.

(a) Isolated combiner   **(b) Non-isolated combiner**
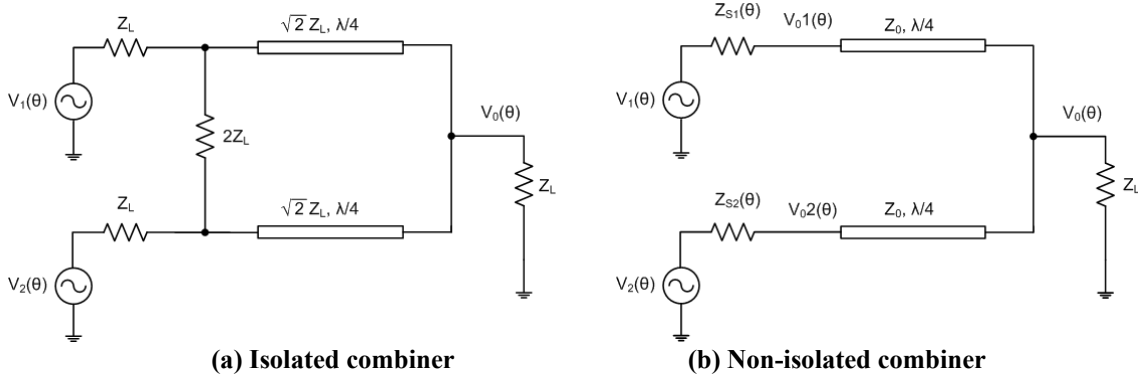
Figure 2.3. Combiner architecture: isolated and non-isolated combiner.

2.3   Prior Art

2.3.1   *Quadrature Modulator based Outphasing Transmitter with Mismatch Calibration*

Figure 2.4 shows a conventional analog outphasing transmitter based on I/Q quadrature modulators [19]. In the transmitter, the two outphasing signals, $S_1(t)$ and $S_2(t)$,

are modulated separately by I/Q quadrature modulators. Also, a digital error detection block measures any gain and phase mismatches between the two paths and combiner through a demodulation feedback path, and calibrates the errors by the predistortion of digital baseband symbols. The conventional outphasing transmitter consists of many analog blocks, such as baseband filters, I/Q generation blocks, mixers, driver amplifiers, and so on. Those analog blocks make the system bulky and more susceptible to process and temperature variations than digital blocks in integrated circuits.
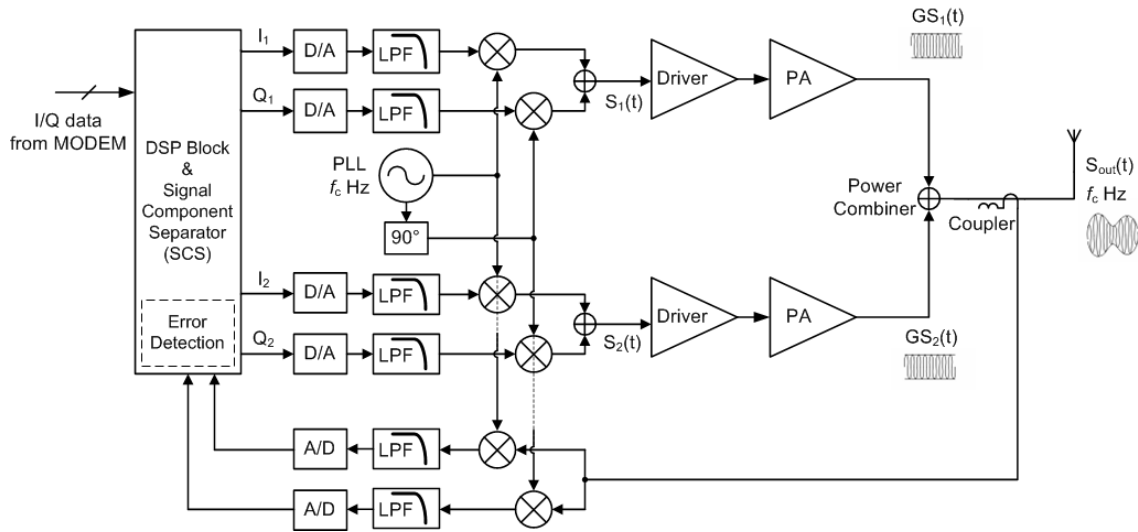
Figure 2.4. Conventional analog outphasing transmitter with I/Q quadrature modulators.

Several mismatch calibration schemes have been proposed in [20] and [21], but the method of predistorting baseband symbols requires extremely complex calculations in conjunction with a digital-to-analog converter (DAC) and analog quadrature modulator, which may not be suitable for commercial products.

2.3.2 Analog Phase Shifter based Outphasing Transmitter

An outphasing transmitter using two analog phase shifters is presented in Figure 2.5 [14]. In the transmitter, the essence of the outphasing modulation techniques lies in the analog phase shifters that vary the phases of the incoming clock with respect to baseband outphase angles. In the baseband DSP block of the transmitter, the input data are coded and mapped according to the in-phase and the quadrature-phase components, and the data are converted into analog signals with baseband filters. Then, the baseband phase control voltage generator of the transmitter generates the output signals, $V_p(t)$ and $V_m(t)$, proportional to the outphase angle, $\varphi(t)+\theta(t)$, $\varphi(t)-\theta(t)$ in (2.5) and (2.6), respectively.
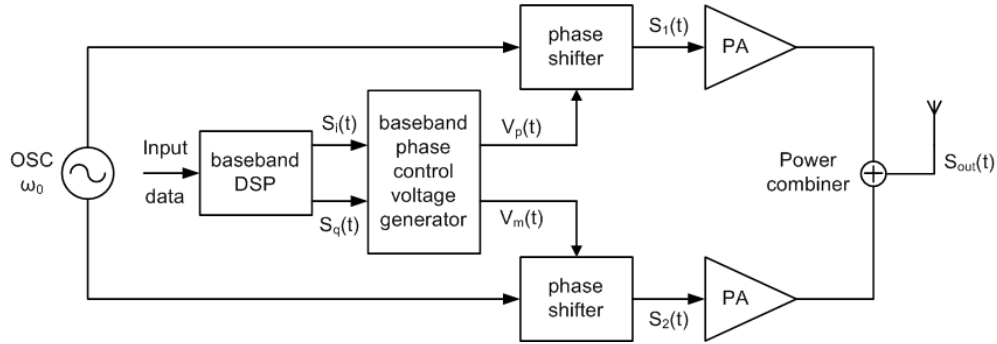
Figure 2.5. Analog phase shifter-based outphasing transmitter.

There are no mixers to upconvert baseband signals to RF or downconvert the RF signals to the baseband for reference feedback signals compared to the quadrature modulator-based outphasing transmitter. Elimination of the analog blocks and the feedback path in the phase-shifter-based outphasing transmitter results in high-speed, wideband operation, as well as no I/Q mismatches. The simple architecture of the

transmitter facilitates the phase modulation of the outphasing system and makes it more robust on circuit variations than the previous quadrature modulator-based transmitter. However, the analog control of the phase shifter degrades the accuracy of output phases, and the open loop structure is also not adequate for the flexible calibration of path mismatches and combiner errors.

2.3.3 Chireix Power Combiner for Efficiency Enhancement

A Chireix power combiner, made of $\lambda/4$ transmission-line sections with shunt reactances, is a lossless combining structure that offers substantially higher combining efficiencies [22]. In Figure 2.6, the input impedances of the Chireix combiner, Z_{in1} and Z_{in2}, can be represented as

$$Re[Z_{in1}] = \frac{2\left(\frac{Z_L}{Z_0^2}\right)cos^2(\theta)}{4\left(\frac{Z_L^2}{Z_0^4}\right)cos^2(\theta) + \frac{1}{\omega^2 L^2} - \frac{\left(4Z_L cos(\theta) sin(\theta)\right)}{Z_0^2 \omega L}} \qquad (2.9)$$

$$Im[Z_{in1}] = \frac{\frac{1}{\omega L} - \left(\frac{2Z_L}{Z_0^2}\right)sin(\theta)cos(\theta)}{4\left(\frac{Z_L^2}{Z_0^4}\right)cos^2(\theta) + \frac{1}{\omega^2 L^2} - \frac{\left(4Z_L cos(\theta) sin(\theta)\right)}{Z_0^2 \omega L}} \qquad (2.10)$$

$$Re[Z_{in2}] = \frac{2\left(\frac{Z_L}{Z_0^2}\right)cos^2(\theta)}{4\left(\frac{Z_L^2}{Z_0^4}\right)cos^2(\theta) + \omega^2 C^2 - \frac{\left(4Z_L cos(\theta) sin(\theta)\right)\omega C}{Z_0^2}} \qquad (2.11)$$

$$Im\left[Z_{in2}\right] = \frac{-\omega C - \left(\dfrac{2Z_L}{Z_0^{\,2}}\right)\sin(\theta)\cos(\theta)}{4\left(\dfrac{Z_L^{\,2}}{Z_0^{\,4}}\right)\cos^2(\theta) + \omega^2 C^2 - \dfrac{\left(4Z_L\cos(\theta)\sin(\theta)\right)\omega C}{Z_0^{\,2}}}. \qquad (2.12)$$
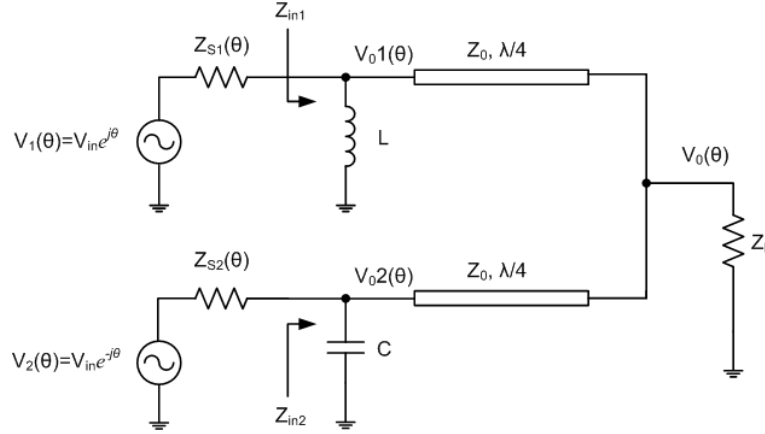
Figure 2.6. Chireix power combiner.

The basic idea of the Chireix combiner is to add parallel reactive elements to cancel the reactive parts of the loads, *Im[Z_in1]* and *Im[Z_in2]*, at a certain predefined phase offset value, thereby allowing maximum efficiency to also be achieved at a phase difference value other than $\theta=0$ [23]. However, those reactives are optimized at one outphase angle and not adaptive for all outphase angles. Also, both efficiency and linearity are degraded at other phase angles because each PA does not operate as an ideal voltage source. Therefore, the Chireix combiner requires an adaptive compensation scheme for the variable input impedance of each port to improve linearity over all outphase angles.

CHAPTER III

ALL-DIGITAL OUTPHASING TRANSMITTER SYSTEM

Recent advances in digital processing capabilities and VLSI technology scaling, fueled by Moore's law, have widened the gap between digital and analog circuits in terms of their performance/complexity/cost trade-offs. This trend is projected to become even more significant in the future. The proposed all-digital outphasing transmitter extends the outphasing concept from its analog origins to a digital form based on a baseband DPM, which operates solely via digital signals. Compared to the previous analog approaches, the digital modulation scheme can accommodate many signal types and provide fine phase control for error calibration.

3.1 Main Architecture

A block diagram of the proposed all-digital outphasing transmitter is shown in Figure 3.1. The transmitter consists of a DSP block, phase locked loop (PLL), two DPMs, two nonlinear switching PAs, an RF power combiner, and an amplitude/phase detection block for mismatch compensation loops. First, the oversampling part of the DSP block oversamples I/Q data from the MODEM with interpolation for image suppression. Since the transmitter operates with digital baseband inputs, the baseband images, which appear

at multiples of the sampling rate, can violate the spectral mask if not properly oversampled [24]. The SCS converts the oversampled I/Q data into two phase-only data by (2.5) and (2.6). Then, the digital pattern generator block creates bit streams, $PH\_DATA_1[n]$ and $PH\_DATA_2[n]$, to control the DPMs according to the phase information from the SCS. The pattern generator can also take calibration values into account for baseband predistortion. The DPMs use the clock signals from the PLL and the digital phase data, $PH\_DATA_i[n]$, to generate two phase modulated signals, $S_1(t)$ and $S_2(t)$. Both phase modulated signals from the DPMs are then amplified by driver amplifiers (DAs) and nonlinear switching PAs, respectively, and finally combined to create the amplified version of the original signal, $S_{OUT}(t)$.
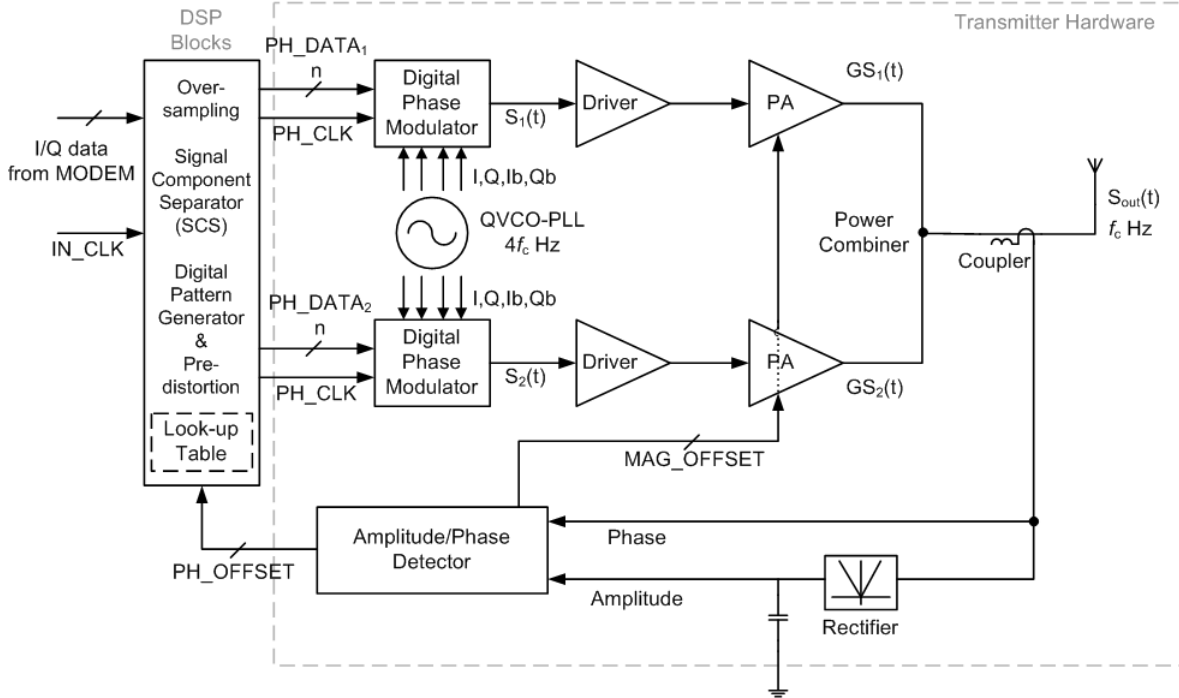
Figure 3.1. Block diagram of proposed all-digital outphasing transmitter.

19

Additionally, the amplitude/phase detection block measures and calculates path mismatches and distortion caused by both PAs and the combiner. Simple single-tone RF test signals synthesized by the DPM can reveal these artifacts via the detector; thus the amplitude/phase detector is enough for the measurements. This topology is much simpler than using a demodulator and analog-to-digital converters (ADCs) proposed in [25] in the feedback path for error detection.

The most noticeable difference from a conventional outphasing system is that conventional DACs, baseband filters, and I/Q modulators are replaced by DPMs. In general, a conventional I/Q modulator consists of two mixers and an RF sumer. The mixer uses baseband analog inputs, I and Q, from the DAC with reconstruction filters; thus the precise phase control for predistortion requires intricate complex number calculations. However, in the proposed digital outphasing transmitter, as the DPM operates with digital baseband inputs, the complex calculation for the phase calibration is substituted by simple bit additions or subtractions because the calibration values can be stored in look-up tables for each frequency channel. Thus, the predistortion block can be easily implemented by simple DSP blocks integrated with the SCS.

The actual implementation of the DPM, the digital pattern generator, and the detailed operation algorithms for the mismatch detection and calibration are presented as follows.

3.2 System Requirements

Some digital modulation schemes, such as quadrature phase shift keying (QPSK) and quadrature amplitude modulation (QAM), have discrete phase values in modulated RF signals. However, modulators that can generate continuous phase values at RF are often required for oversampled baseband symbols or more complex modulation schemes. For example, in OFDM systems, as frequency-domain baseband data have been converted to time-domain data by an inverse fast Fourier transform (IFFT), the phases of baseband symbols can be any values between -180° and +180°. To support such modulation schemes, the phase modulator must produce continuous phase values. Moreover, the outphasing transmitter also requires fine phase tuning for mismatch compensation.

In the digital transmitter, each DPM modulates the clock signal according to a digital phase input, thus it has a finite resolution in phase. Phase quantization may degrade modulation accuracy, as measured by error vector magnitude (EVM) because the finite resolution generates quantization noise at each phase angle of the outphasing amplifier. Therefore, it is necessary to determine the minimum number of bits required for a given modulation scheme, which will ensure compliance with the appropriate specification. The relation between signal to noise ratio (SNR_q) and the word length of signal quantization has been well discussed in many textbooks and papers [26][27]. The SNR_q after a b_s-bit quantization is given by

$$SNR_q = 6.02 \cdot b_s + 1.76 - 20 \cdot \log_{10} k \text{ [dB]}, \tag{3.1}$$

where b_s denotes the number of bits and k denotes the peak factor, the ratio of the peak amplitude to the mean amplitude of the signal.

Every additional bit in signal quantization increases SNR_q by 6.02 dB and its absolute value depends on the PAPR of the original signal. To avoid signal quality degradation due to quantization, the SNR_q should be larger than the SNR of the original signal. Therefore, the number of bits of a DPM, b_{DPM}, should be

$$b_{DPM} \geq \frac{SNR - 1.76 + PAPR}{6.02},$$
(3.2)

where both SNR and PAPR are from the original signal in dB before the phase quantization.

To evaluate the quantization effects on OFDM signals, the EVM values of IEEE 802.16e signals were tested with different phase resolution [1]. Figure 3.2 shows the simulation results.
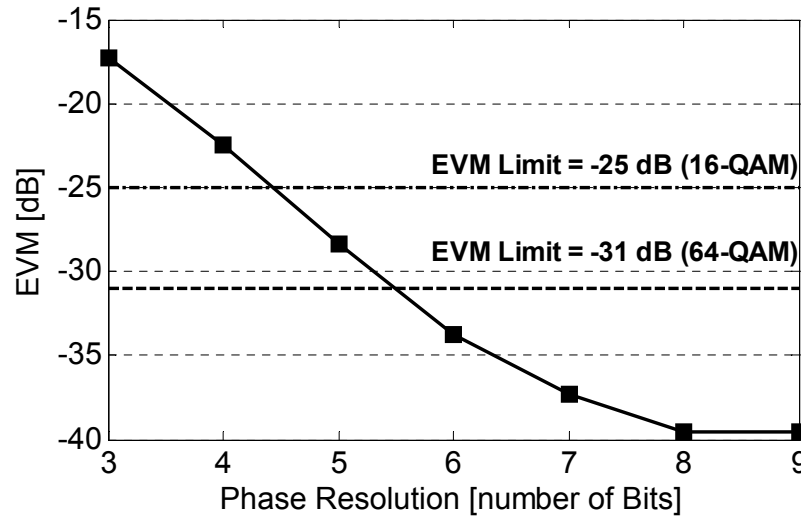
Figure 3.2. Effects of number of bits in DPM on IEEE 802.16e modulation.

The original signal has the SNR of 40 dB before phase quantization. From the graph, it is seen that the EVM decreases by 6 dB with an each additional bit until it reaches the original EVM value. Therefore, the DPM of the system must provide at least 5 and 6-bit phase resolution to meet required EVM limit of 16-QAM and 64-QAM, respectively, and 8-bits to avoid significant SNR degradation.

3.3   Key Building Blocks

3.3.1 Digital Phase Modulator

In general, most DPMs have 3 or 4 bits of resolution within a small phase range [28][29]. To implement a DPM with high phase resolution and a wide phase control range (-π ~ +π) for the outphasing modulator, a special DPM architecture adopting frequency dividers with quadrature phase clock is preferred, as has been suggested in prior work [30]. A clock frequency four times higher than the RF, provides two phase control bits through the frequency dividers and two additional control bits are obtained by selecting one of the quadrature signals of the clock. Finer phase control can be accomplished by a phase interpolator. An exemplary DPM design is shown in Figure 3.3.

It consists of a quadrature voltage-controlled oscillator (VCO) with four times higher frequency than RF, an input register, a 4:2 multiplexer (MUX), frequency dividers, a fine digital phase interpolator, and a XOR gate. Once loaded into the input register, the phase data, $PHASE_i[n]$, controls each building block for phase modulation: 2-bit for the 4:2 MUX, 1-bit for the pulse generator, 1-bit for the XOR gate, and the remaining (n-4)-bit for the digital PI for fine phase control.

23
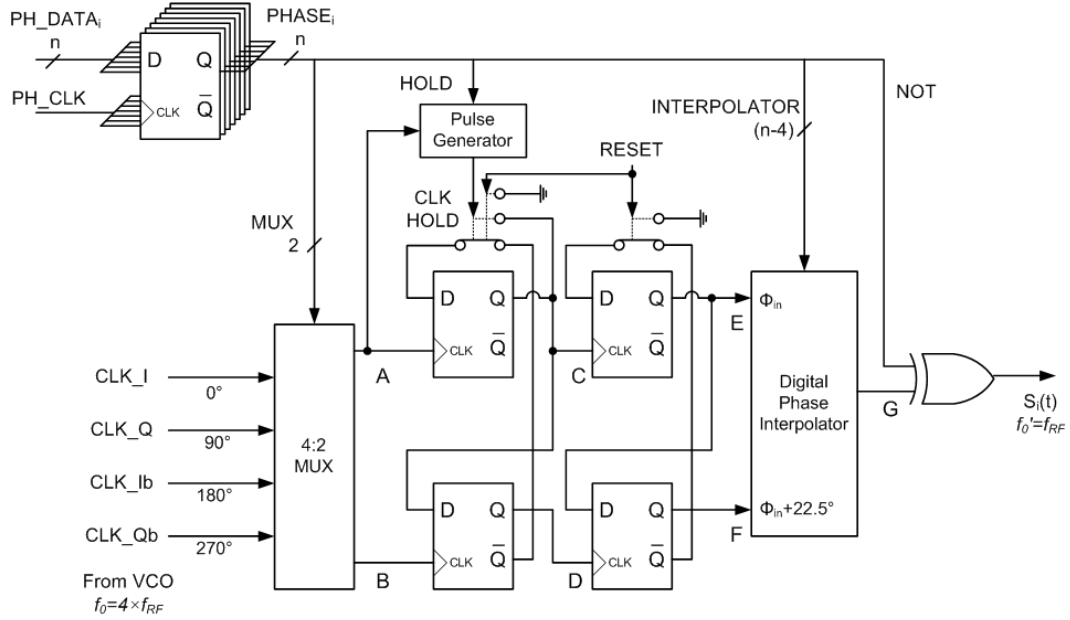
Figure 3.3. Block diagram of n-bit digital phase modulator.

The 4:2 MUX selects one pair of clock signals from four phase I/Q clock signals so that A leads B by $\pi/2$, i.e., $(A, B) \in \{ (CLK\_I, CLK\_Q), (CLK\_Q, CLK\_Ib), (CLK\_Ib, CLK\_Qb), (CLK\_Qb, CLK\_I) \}$. Since the frequency of the LC quadrature VCO is four times that of the phase modulated signal, $S_i(t)$, the 4:2 MUX rotates phase with the step size of $\pi/8$ from 0 to $\pi/2$. The following two D-flipflops (DFFs) divide the clock signals, A and B, by two and delay phase by holding the upper DFF from toggling for one period of the clock signal, if needed. The pulse signal, *HOLD*, is turned on for one period of the clock signal when it is high. The next two DFFs just divide the clock signals, C and D, by two. Thus, the four DFFs divide the clock signals by four and rotate phase by 0 or $\pi/2$ with the resolution of $\pi/8$. The digital PI interpolates between the two clock signals, E and F, with (n-4) bit resolution and outputs the phase modulated signal to the XOR gate. The input signals of the interpolator, E and F, always have a phase difference of $\pi/8$.

24

Therefore, the output signal, $S_i(t)$, has a phase value between the two signals corresponding to its control input. Lastly, the XOR gate can invert the clock signal, G, which is equivalent to the phase of -π, and output signal is fed into PA driver amplifier. As a result, the n-bit DPM modulates phase from -π to π with the minimum step size of $(2\pi)/2^n$.

The timing diagram describing the phase shift mechanism with 8-bit resolution is shown in Figure 3.4 as an example. As seen in the figure, each bit should be carefully calculated to generate a desirable phase output. When $S_i[k]$ is k-th baseband symbol including calibration of a certain path, the 8-bit quantized phase of the symbol can be represented as

$$PH_i[k] = \left\lfloor \angle(S_i[k]) \times \frac{2^8 - 1}{2\pi} + 0.5 \right\rfloor, \text{ where } -\pi < \angle(S_i[k]) \leq \pi. \tag{3.3}$$

The bits, *MUX[1:0]*, *HD (HOLD)* and *NOT*, are from the relative phase difference between a previous symbol and a current symbol. The four most significant bits (4 MSB) of the relative phase difference between the symbols are calculated as

$$\Delta PH_i[k]\big|_{4MSB} = \left\{ \left(\left\lfloor \frac{PH_i[k]}{2^4} \right\rfloor - \left\lfloor \frac{PH_i[k-1]}{2^4} \right\rfloor + 8 \right) \mod 16 \right\} - 8. \tag{3.4}$$
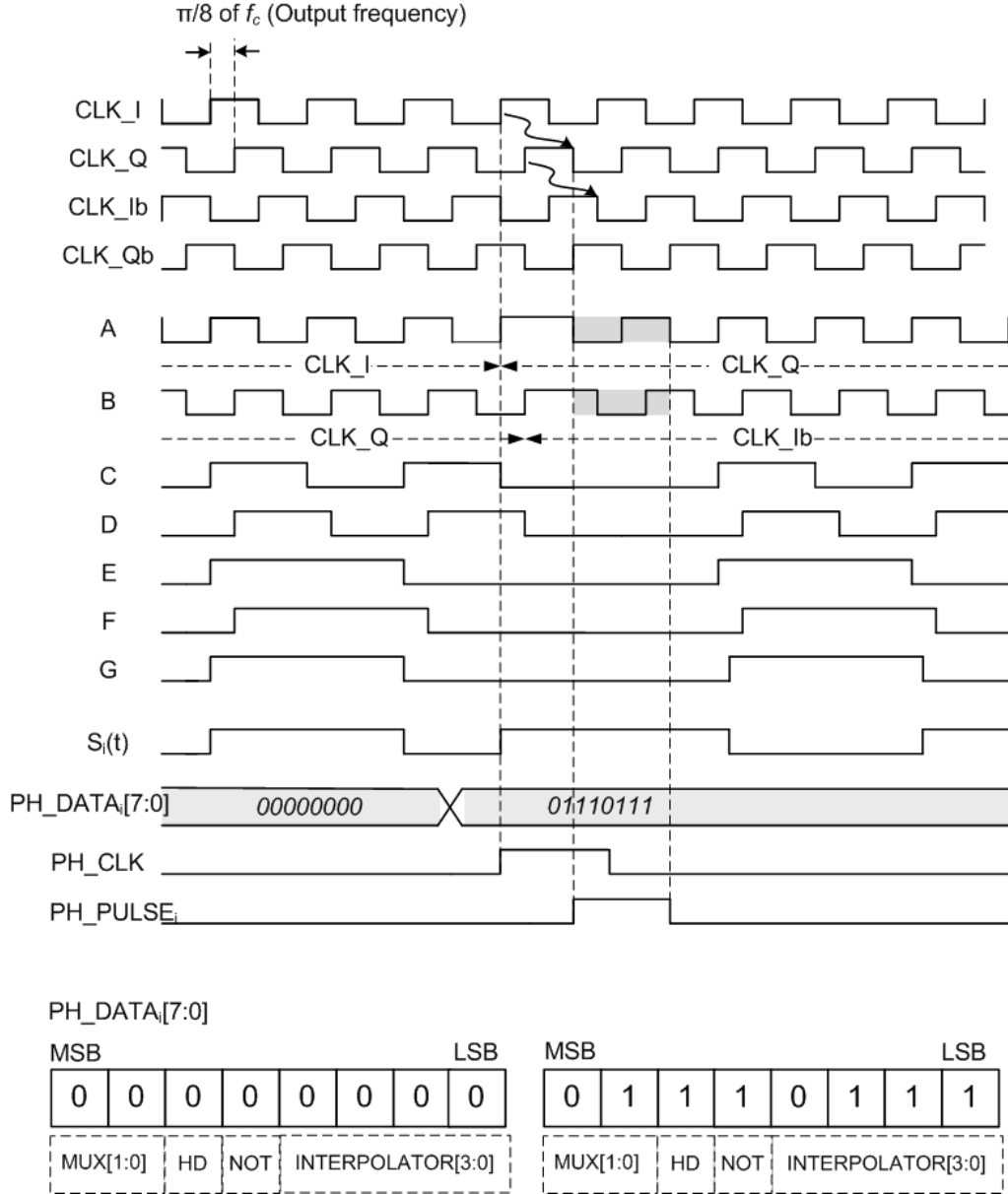
Figure 3.4. Timing diagram of 8-bit digital phase modulator.

$\Delta PH_i[k]\big|_{4MSB}$ is an integer value between -8 and +7 showing the phase shift

between (k-1)-th and k-th symbol with the resolution of $\pi/8$. The DPM phase control bits

at k-th symbol, $\Delta MUX[1:0]$, HD and NOT, can be determined by the $\Delta PH_i[k]\big|_{4MSB}$ where Δ

$MUX[1:0]$ is the incremental difference of $MUX[1:0]$ between a previous and a current

symbol. Figure 3.5 shows the relative phase shifting diagram, and each bit value is summarized according to the relative phase differences, $\Delta PH_i|_{4MSB}$.
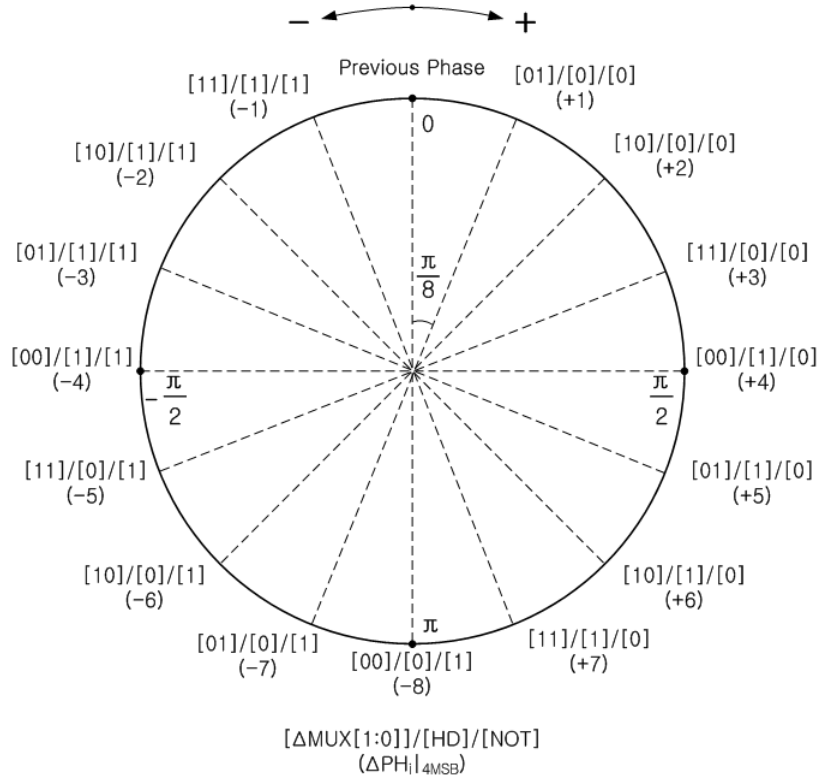
Figure 3.5. Relative phase shift corresponding to input signals.

In addition, the input bits of the phase interpolator, *INTERPOLATOR[3:0]*, at the *k*-th symbol are from the four least significant bits (4 LSB) of the current phase value as shown in (3.5).

$$INTERPOLATOR[3:0] = \left\{ \left(PH_i[k] + 2^7 \right) \mod 16 \right\} \tag{3.5}$$

27

Another possible DPM design is using a simple delay locked loop (DLL) block, as shown in Figure 3.6. The n-bit DPM modulates the phase of incoming clock by two steps, coarse and fine steps. It is composed of a delay locked loop (DLL) with 2^k delay stages and a 2^k-by-2 multiplexer for the coarse phase step ($k \leq n$) and a digital phase interpolator (DPI) for the fine step. Up to achievable minimum delay for a given device process, we can obtain 2^k different phases with the resolution of $(2\pi)/2^k$ from the delay stages of the DLL. The two signal paths, S_1 and S_2, in outphasing modulation can share the delay stages. Finer phase control is accomplished by the DPI, which generates intermediate phases between the two inputs with a phase difference of $(2\pi)/2^k$.
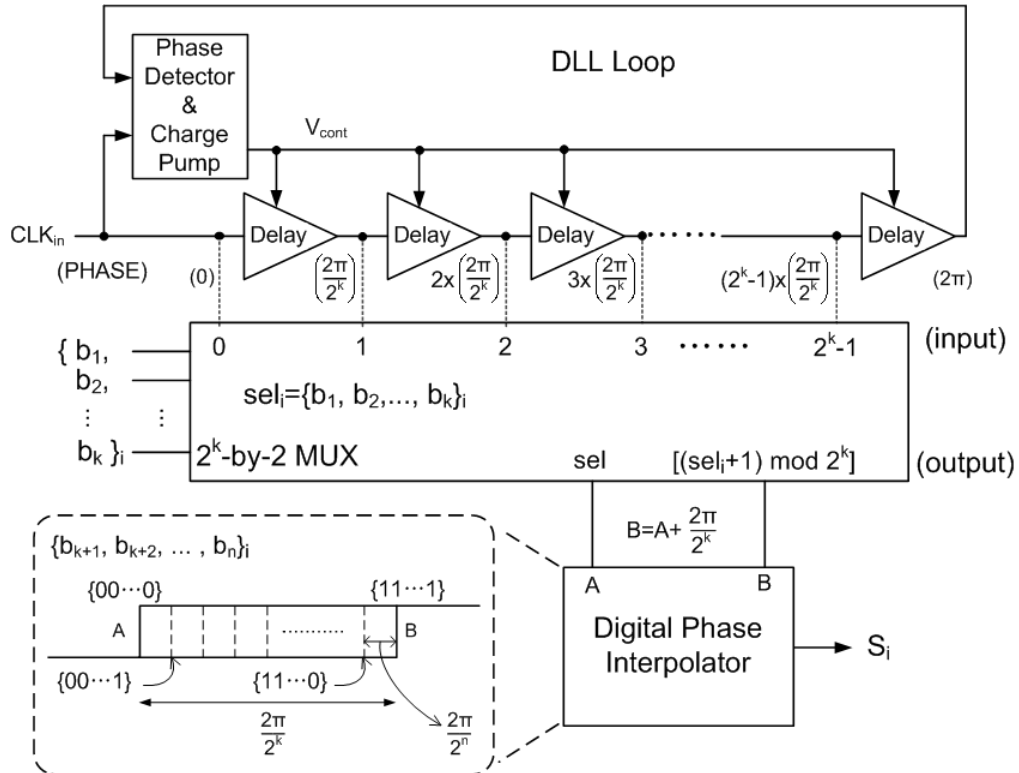
Figure 3.6. DLL-based digital phase modulator.

The phase control bits, $PH\_DATA_{1,2}[n]=\{b_1, b_2, \cdots, b_n\}_{1,2}$, at time, t, are made in the digital pattern generator and used to control the phase of each signal for phase modulation. The b_1 is the most significant bit (MSB), and b_n is the least significant bit (LSB) on phase control. Then, the bits are given by

$$\{b_1, b_2, ..., b_k\}_i = \left\lfloor \frac{PH_i(t)}{2^{n-k}} \right\rfloor \qquad (k \leq n) \tag{3.6}$$

$$\{b_{k+1}, b_{k+2}, ..., b_n\}_i = \left(PH_i(t) \mod 2^{n-k} \right), \tag{3.7}$$

$$\text{where } PH_i(t) = \left\lfloor \angle\left(S_i(t)\right) \cdot \frac{(2^n - 1)}{2\pi} + 0.5 \right\rfloor \tag{3.8}$$

and $0 \leq \angle\left(S_i(t)\right) < 2\pi$.

The simple phase control of the DPM facilitates the phase calibration for various mismatch and error correction algorithms. Moreover, the proposed digital transmitter, implemented without conventional analog mixers and filters, is suitable for a wide variety of modulation schemes and signal bandwidths.

3.3.2 Power Amplifier

The load-sensitive properties of the PA can influence the performance of the outphasing transmitter. In [31] and [32], various types of switching PAs, such as Class D,

E, F, were evaluated to find the optimum candidates for an outphasing transmitter. In [32], each input impedance of a combiner varies due to the non-isolation effects of a combiner, and can be represented by a function of the outphase angle, θ. Likewise, PAs were substituted by ideal voltage or current sources with output impedance, Z_0. The results showed that voltage-mode Class D (VMCD) and Class F PAs are good choices for an outphasing transmitter because they have an output current – a voltage relationship that is similar to the ideal voltage source, but the sensitive characteristics in load impedance of Class E PA render it a poor candidate for an outphasing transmitter [33]. To demonstrate this sensitivity of a Class E PA, the basic topology of the PA is shown in Figure 3.7 [34]. The circuits include a transistor, shunt capacitor C_1, RF chock L_1, and series tuned output circuit L_0, C_0. Ideally, the tuned output circuit does not impact the output impedance of the PA, but there exists a residual series reactance due to the circuit because the series resonant circuit is usually not perfectly tuned at the operating frequency. This feature makes the Class E PA highly reactive and load impedance-sensitive.
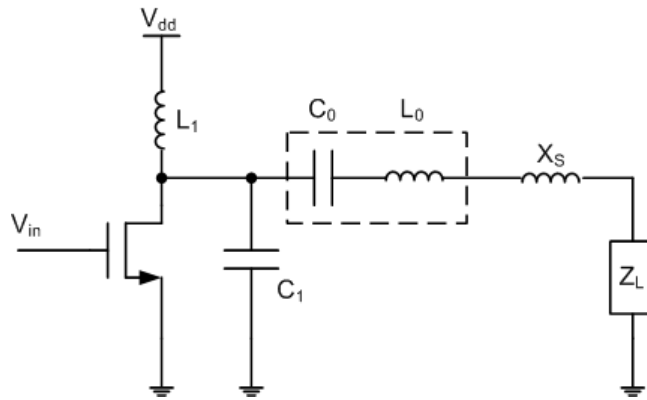
Figure 3.7. Basic topology of Class E amplifier.

However, every PA operates as a non-ideal voltage or current source, and therefore they are all influenced by load impedance to some degree. Thus, precise compensation for the time-varying load impedance is required to optimize the performance of the outphasing transmitter. Proper calibration can even improve the linearity of the outphasing transmitter using a Class E PA. The output impedance of each PA, $Z_0(\theta)$, consists of both amplitude and phase elements. Therefore, the phase error in the impedance can be cancelled by shifting the phase of an input signal in the opposite direction, and the amplitude error can be compensated by adjusting the supply voltage of the PA.

3.3.3 Power Combiner

In the outphasing technique, there are two kinds of power combiners: isolated and non-isolated combiners. The isolated combiner, such as a Wilkinson combiner, has all matched input and output ports independent of the amplitude and phase of input signals. This feature has the advantage of low distortion, but most of the energy can be dissipated in the combiner when the outphase angle, θ, is close to 180°, which corresponds to significant efficiency degradation. On the contrary, in a non-isolated combiner, the equivalent input impedance of each input port varies depending on the amplitude and phase of the input. A Chireix combiner is one of the non-isolated combiners using the load modulation technique [33]. A Chireix combiner is a lossless combining structure that provides much higher combining efficiency than that of the isolated combiner at the cost of linearity due to non-isolation characteristics.

In a general Chireix combiner, two reactive shunt elements are inserted to mitigate the reactive input impedances of the combiner, thus improving overall efficiency [23], but those susceptances are optimized at one outphase angle and are not adaptive for all outphase angles. Thus, both efficiency and linearity are degraded at other phase angles. Therefore, adaptive compensation of the input impedance of each input can improve both combining efficiency and linearity over all outphase angles. To track the input impedances of a combiner with respect to all outphase angles, the detailed power combiner architecture needs to be analyzed. Figure 3.8 shows a general non-isolated combiner topology. $Z_{S1}(\theta)$ and $Z_{S2}(\theta)$ are the output impedances of PA, and $Z_{in1}(\theta)$ and $Z_{in2}(\theta)$ are input impedances of the combiner at port 1 and port 2, respectively. Each impedance value is represented by a function of the outphase angle, θ, to take non-isolation effects into account.

Figure 3.8. Architecture of general non-isolated combiner.

From (2.5) and (2.6), the input voltages of the power combiner, $V_1(\theta)$ and $V_2(\theta)$, are defined as follows.

32

$$V_1(\theta) = 0.5 r_{max} e^{j\theta} \tag{3.9}$$

$$V_2(\theta) = 0.5 r_{max} e^{-j\theta} \tag{3.10}$$

The original signal angle, $\varphi(t)$, and dependence of θ on time are suppressed since it does not affect the mismatch analysis [20]. If one assumes that the output impedances of two PAs remain constant as Z_S overall the outphase angle such as an ideal voltage source, then the reflection coefficient, $\Gamma(\theta)$, between the PA output and the combiner input will be

$$\Gamma(\pm\theta) = \frac{Z_{in}(\pm\theta) - Z_s}{Z_{in}(\pm\theta) + Z_s} \tag{3.11}$$

where

$$Z_{in}(\pm\theta) = \frac{1}{\dfrac{Z_L}{Z_0^2}\left[2\cos^2\theta \mp j\sin(2\theta)\right]}. \tag{3.12}$$

$\Gamma(\theta)$ takes into account the lack of isolation between both branches, as each branch is seen as a dynamic load to the other. With equation (3.9) and (3.10), the following output voltage expression is obtained as derived in [35].

$$V_0 1(\theta) = GV_1(\theta)[1+\Gamma] = |V_0 1| e^{j\theta'} \tag{3.13}$$

$$V_0 2(\theta) = GV_2(-\theta)[1+\Gamma] = |V_0 2| e^{-j\theta'} \tag{3.14}$$

$$V_0(\theta) = 2G\left(\frac{Z_L}{Z_0}\right)\left(\frac{r_{max}}{2}\right)|1+\Gamma(\theta')|\cos(\theta') \tag{3.15}$$

where $\theta = \theta' - \angle(1+\Gamma(\theta'))$ and G is the gain of each PA.

It is seen that despite the non-isolation effects in a combiner, only the output signal amplitude is distorted if the PA output impedance remains constant. However, because the PA does not behave as an ideal voltage source, there exists one more circuit parameter that causes distortions in the combiner. The output impedances of PAs, $Z_{in1}(\theta)$ and $Z_{in2}(\theta)$, are also a function of the outphase angle, and they are not identical, which means that the phase of the output signal can also be distorted. The only way to estimate the effects on the output signal is to measure it in actual circuits. In [33], a load-pull analysis method was proposed to measure output signal phase distortion on a Class E PA, but this method is not adequate for commercial products. Thus, the method of applying test vectors and measuring their responses was adopted for calibration in this preliminary research. Fortunately, because the DPM in the proposed transmitter has a finite number of test vectors, calibration is much easier than with the methods using conventional predistortion for both measurement and compensation.

3.4   Digital Mismatch Compensation Algorithms

As long as the two signal paths of the transmitter are perfectly symmetrical and isolated, the output of the outphasing amplifier is linear, as shown in (2.7). However,

process, voltage and temperature (PVT) variations in real circuits can generate path mismatches, and thereby degrade signal path linearity. Figure 3.9 shows a general power combiner topology of the outphasing transmitter. In the previous mismatch analysis methods in [36]-[39], the gain of each PA is always regarded as a constant. Thus, they could not compensate for imperfect isolation in the combiner. Here, the gain of each path is represented as a function of outphase angle, $\theta(t)$, as shown in (2.5) and (2.6) to include the effects of imperfect combiner isolation. The distortion due to the combiner is determined by the relative angle differences between the two input vectors. Thus, the original signal angle, $\varphi(t)$, and dependence of S_1, S_2, S_{OUT} and θ on time are suppressed since it does not affect the mismatch analysis.
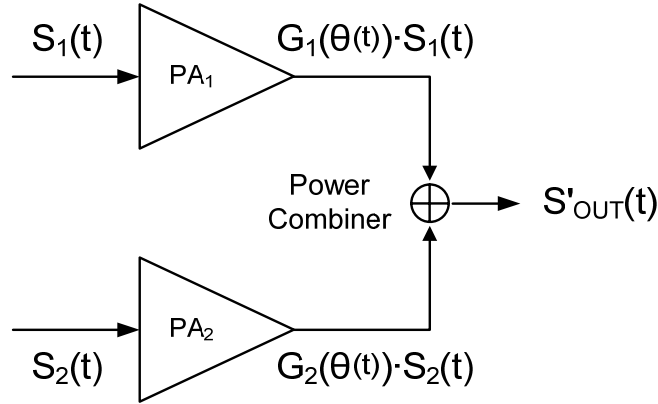
Figure 3.9. Errors of outphasing amplification.

The most significant advantage of the proposed DPM-based transmitter is that the calibration is much easier and simpler than the methods using the conventional calculation-based predistortion presented in [20] and [39]. Any mismatches caused by circuits can be detected and stored in digital look-up tables for each frequency channel

because the DPM has a finite number of vectors to represent all available output amplitudes.

3.4.1 *Foreground Mismatch Compensation Algorithms*

Foreground mismatch compensation algorithm detects and calibrates any gain and phase mismatches between the two branches and the distortion due to the combiner during initialization. For the calibration, the two DPMs generate and inject various test vectors into PAs, and then the combiner output is measured when power is turned on. The calibration results will be stored in digital look-up tables as a function of outphase angle, θ. The algorithm consists of static mismatch compensation and dynamic mismatch compensation.

A. Static Mismatch Compensation

The static mismatch compensation method is used to compensate for unbalanced PAs and any path or load mismatches between the two signal paths when they are out-of-phase or $\theta=90°$. Figure 3.10 demonstrates the steps in the gain/phase mismatch compensation algorithm. Gain/phase mismatches are detected by simply letting two test vectors, S_1 and S_2, have equal amplitude and opposite phases, and then monitoring the amplitudes of S_{OUT}. As shown in the figure, if gain/phase mismatches exist, S'_{OUT} is not zero and has an amplitude as shown in (3.16).
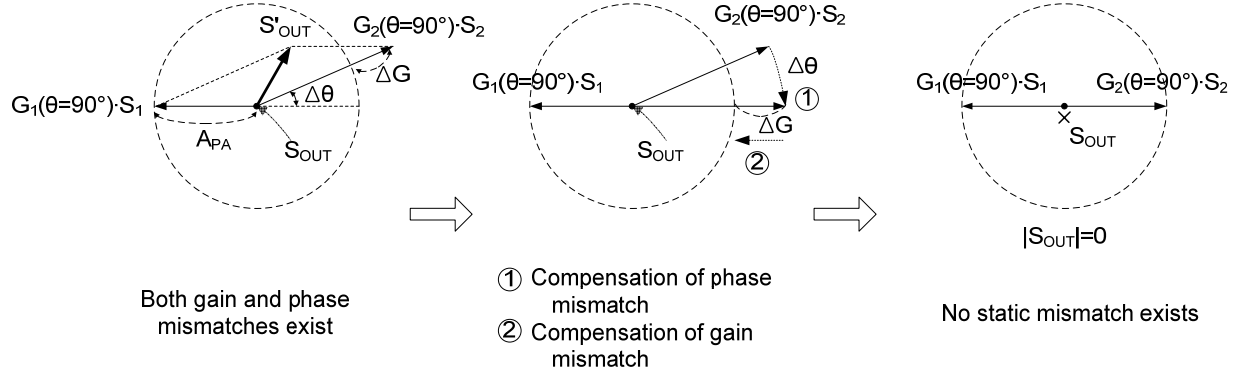
Δθ, ΔG : Gain and phase mismatches when two input signals are out-of-phase (θ=90°)
S'_{OUT} : Output signal with gain and phase mismatches
S_{OUT} : Ideal output signal

Figure 3.10. Sequence of steps for static mismatch compensation.

$$
\begin{aligned}
\left|S'_{OUT}\right| &= \left\{\left[\left(A_{PA}+\Delta G\right)\cdot\cos\left(\Delta\theta\right)-A_{PA}\right]^2 \right. \\
&\quad \left. +\left[\left(A_{PA}+\Delta G\right)\cdot\sin\left(\Delta\theta\right)\right]^2\right\}^{\frac{1}{2}} \\
&= \sqrt{\Delta G^2 + 2\cdot A_{PA}\cdot\left(A_{PA}+\Delta G\right)\cdot\left[1-\cos\left(\Delta\theta\right)\right]}
\end{aligned}
\tag{3.16}
$$

where

$$
\Delta\theta = \angle\left(G_1\left(\theta=90°\right)\cdot S_1\right)+\angle\left(G_2\left(\theta=-90°\right)\cdot S_2\right),
\tag{3.17}
$$

$$
\Delta G = \left|\left|G_1\left(\theta=90°\right)\cdot S_1\right|-\left|G_2\left(\theta=-90°\right)\cdot S_2\right|\right|
\tag{3.18}
$$

and A_{PA} is the output amplitude of the PA$_1$.

The gain mismatch is corrected after first compensating for phase difference in the two branches.

Phase mismatch, $\Delta\theta$, is first compensated by initializing the amplitude offset to be zero and by selecting the phase offset that minimizes $|S'_{OUT}|$ or ΔG. Amplitude mismatch,

37

ΔG, is then compensated by setting *PH_OFFSET* to the selected value and by finding the *MAG_OFFSET* that makes $|S_{OUT}|$ as small as possible. The selected offset values, *PH_OFFSET* and *MAG_OFFSET*, are provided to the SCS and nonlinear PAs, respectively, for gain/phase adjustment, as shown in Figure 3.1. *PH_OFFSET* is added or subtracted from DPM control bits at the digital pattern generator for constant phase mismatch cancellation and *MAG_OFFSET* is used to control the bias of each nonlinear PA to produce the same gain in each branch.

B. Dynamic Mismatch Compensation

Dynamic mismatch compensation method is used for the compensation of combining errors and losses in the outphasing transmitter. To compensate for those errors and losses, the two test vectors that have the opposite outphase angles, $\pm\theta$ ($0 \leq \theta < 90°$), are used, as shown in Figure 3.11(a). If there are no path mismatches and no combiner errors, the net combiner output impedance is purely real with an amplitude corresponding to the outphase angles, $\pm\theta$, due to their symmetries on the real axis. However, the combining errors can cause imperfect phase cancellation in the combiner, which generates phase and amplitude errors in the combiner output. Figure 3.11(a) shows the exemplary combiner response to the conjugate phase test signals. Suppose that at some outphase angle, θ, the output vector is no longer on the horizontal axis but rather its angle is negative. Then, both input signals should be calibrated in the same direction, $+\alpha(\theta)$, to cancel the phase offset of the output. This is called common phase compensation.

Simultaneously, the amplitude of the combined output signal is also diminished due to the losses in passive components. This is also shown in Figure 3.11(a). To remove

the effects of losses, both input signals should be calibrated in the opposite direction, $\pm\beta(\theta)$, to reduce the angle between the two vectors corresponding to the outphase angle, θ. This is called differential phase compensation.

Dynamic mismatch compensation consists of: first, common phase compensation; then, differential phase compensation. These steps are summarized in Figure 3.11(a).

Again, the original baseband symbol angle, φ, in (2.3) does not affect the compensation of mismatch, since the phase and amplitude distortion is only a function of the outphase angle, θ ($0 \leq \theta < 90°$). The total number of test vectors for the dynamic mismatch compensation is $2^n/4 = 2^{(n-2)}$, which is the number of possible phases in the first quadrant of an n-bit DPM in Figure 3.11(a). Also, the static mismatch compensation can be performed before the dynamic mismatch compensation is performed because the static compensation only measures a minimum output amplitude, which is independent of the dynamic compensation. Both compensation angles, $\alpha(\theta)$ and $\beta(\theta)$, can be saved in digital look-up tables for each channel and calibrate the input bit streams of DPMs with simple digital addition or subtraction operations.

Finally, after the completion of the look-up tables, the calibrated baseband symbols, S_{CAL1} and S_{CAL2} shown in Figure 3.11(b), including the static and dynamic mismatch compensation can be represented as

$$S_{CAL1} = S_1 \cdot e^{j\left[\alpha(\theta)-\beta(\theta)\right]} \tag{3.19}$$

$$S_{CAL2} = S_2 \cdot e^{j\left[\alpha(\theta)+\beta(\theta)-\Delta\theta\right]}. \tag{3.20}$$

Output with test vector 1. Common phase compensation 2. Differential phase compensation
                                                +α(θ)   ±β(θ)
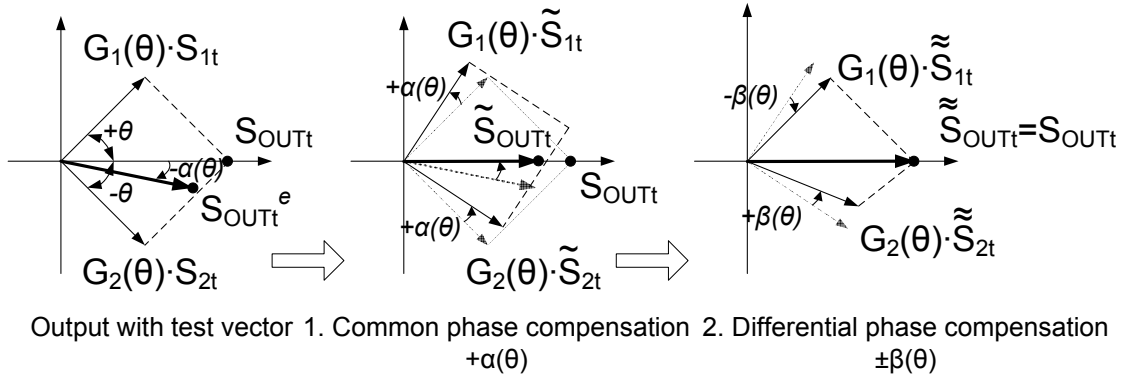
S_{1t}, S_{2t} : Test signals for dynamic mismatch compensation
S_{OUTt} : Ideal output signal from test signals
S_{OUTt}^{e} : Distorted output signal due to gain and phase errors at combiner

+α(θ) : Common phase compensation
±β(θ) : Differential phase compensation as a function of out-phase angle, θ

(a)

Original input vector   1. Common phase compensation 2. Differential phase compensation
                                                +α(θ)   ±β(θ)
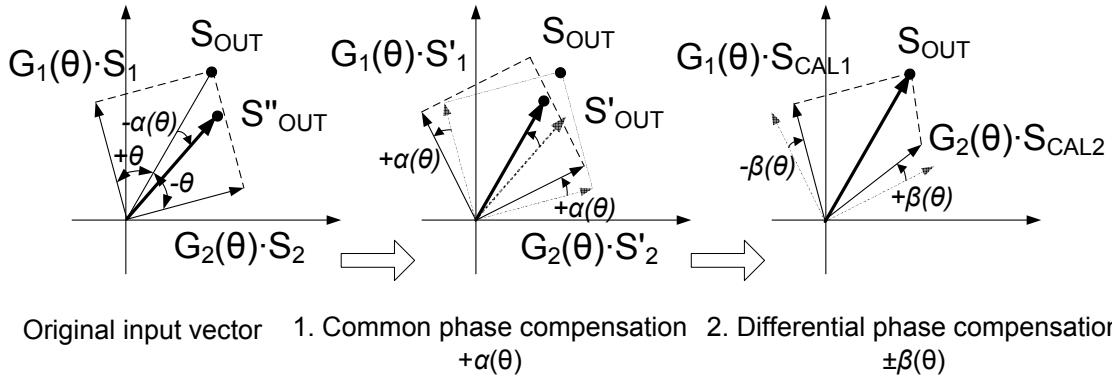
$S"_{OUT}$: Output signal with gain and phase errors at combiner
S'_{OUT} : Output signal after phase error calibration
S_{OUT} : Output signal after gain and phase calibration

(b)

Figure 3.11. Sequence of steps for dynamic mismatch compensation. (a) Dynamic error measurement with test vectors, (b) Dynamic mismatch compensation with look-up tables.

3.4.2 Background Mismatch Compensation Algorithms

The foreground mismatch compensation is the initial characterization of the outphasing system before communication. Thus, it requires a series of test vectors and an empty time slot. However, the mismatches and variations change over time. Also, the calibration and data transmission cannot operate simultaneously. Therefore, the only way to calibrate the time-varying effects is to measure the errors from data signals and compensate them continuously.

In the foreground compensation, the digital look-up tables summarize the calibration values as a function of the outphase angle, θ. As each data symbol has an outphase angle value as in (2.5) and (2.6), it is possible to update the calibration information by monitoring and comparing the relationship between the outphase angle of the data and its combiner output signal at the amplitude/phase detector with the same manners of the foreground compensation. Thus, the background mismatch compensation is also available during data transmission.

3.4.3 Simulation Results

To validate the proposed compensation algorithms above, two sets of simulation setups have been designed using the ADS simulator [40] with various WiMax modulation schemes. The first setup was developed to measure the mismatch effects caused by both PAs and a combiner to test vectors, and the second setup is an entire 5.8 GHz WiMax transmitter testbed system to demonstrate the performance of the compensation algorithms. The testbed consists of a digital baseband generation part with 8-bit DPMs, an error calibration block, an outphasing amplifier block, and a measurement block. The outphasing amplifier is composed of two Class E PAs and a non-isolation combiner using

41

circuit co-simulation environments. The measurement block is used for calculating an EVM, system efficiency, and output signal spectrum. In the setup, Class E PAs with a non-isolation combiner are selected to maximize the effects of the non-isolation distortions.

For the Class E PA, a 0.18-μm standard CMOS process library is used for circuit design. The PA consists of a driver stage and a power stage, and its tuned output circuits are designed to operate at 5.8 GHz for WiMax applications. The maximum available output power of the PA is 22 dBm with an efficiency of 73%. The architecture of the non-isolation combiner is the same as that of a general Chireix without shunt elements, and the characteristic impedance of the quarter-wave transformer is 40 Ω to transform the output impedance of the PA, 16 Ω, to 100 Ω. In practice, it may be difficult to design a DPM that operates at 5.8 GHz because its internal frequency must be four times higher than the carrier frequency. In this simulation setup, the operating frequency of 5.8 GHz is chosen to verify the calibration performance in the WiMax-OFDM modulation scheme. Also, the proposed transmitter architecture is applicable to other wireless standards, which use different frequency bands.

Figure 3.12 shows the EVM and the output signal spectrum for an 8-bit all-digital outphasing transmitter without error compensation. The gain and phase mismatches were 5% and $6°$, respectively. As expected, the output signals cannot meet the EVM requirements of the transmitter due to the distortions from PAs and a combiner.

(a) Constellation (64-QAM, EVM = -22.24 [dB])   **(b) Output spectrum**
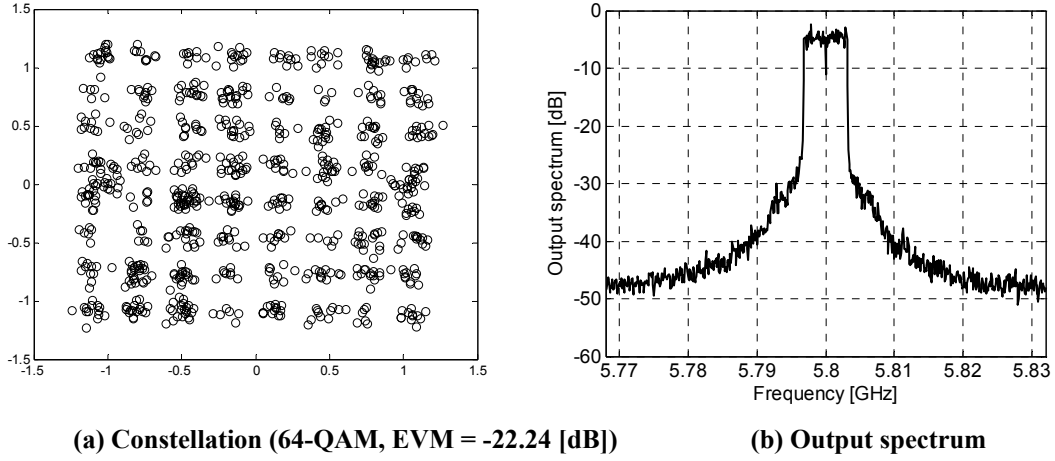
Figure 3.12. EVM and spectrum of output signal before mismatch calibration.

To reduce the distortion through calibration, the static and dynamic compensation values are generated with the responses of the test vector, as demonstrated in Figure 3.10 and Figure 3.11. The gain/phase mismatches between the two PAs are detected through the static mismatch measurement. In addition, the test vectors for the dynamic mismatch compensation create 64-by-2 calibration look-up tables for the 8-bit DPMs. Each row has two compensation parameters, α and β, and they are recorded according to the outphase angle, θ, with a resolution of $\pi/2^7$ from 0 to π/2. The calibration tables are summarized in Figure 3.13.

Finally, Figure 3.14 shows the EVM and the signal spectrum of the output signal after calibration. The EVM value and the shape of the output spectrum are similar to the results from the quantization effects in Figure 3.2, as the compensation mechanisms can improve the performance up to the resolution of DPMs.

1. Static mismatch compensation

$\Delta\theta_1=0$, $\Delta r_1=1$ $\qquad\qquad$ $\Delta\theta_2=6°$, $\Delta r_2=0.95$

2. Dynamic mismatch compensation
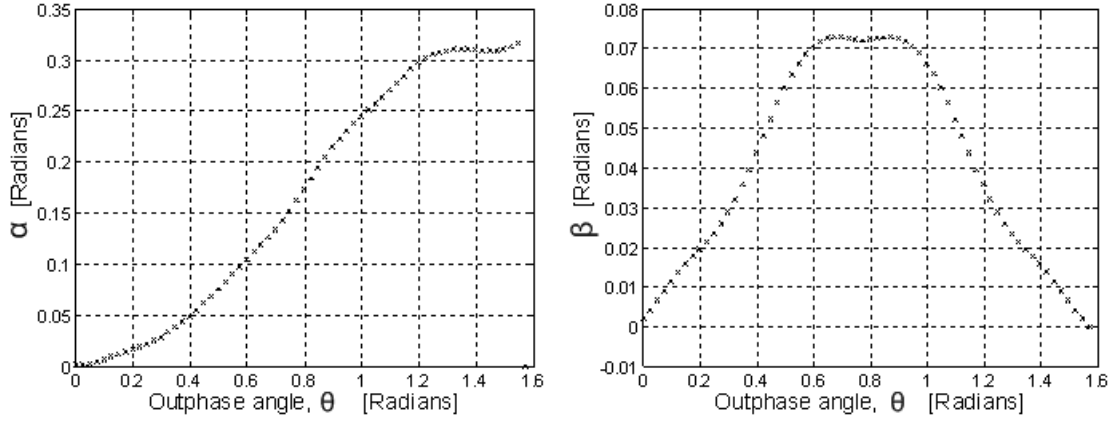
Figure 3.13. Summary of look-up tables.

(a) Constellation (64-QAM, EVM = -33.48 [dB]) $\qquad$ **(b) Output spectrum**
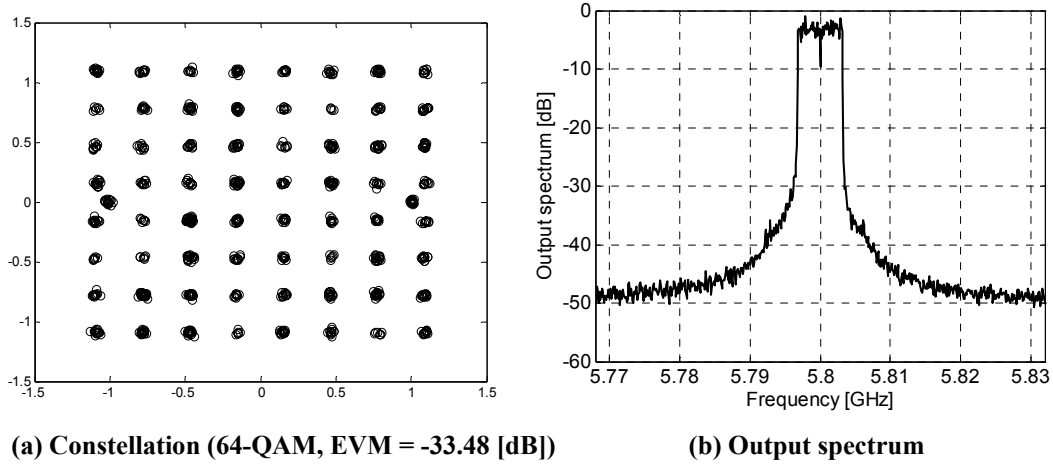
Figure 3.14. EVM and spectrum of output signal after mismatch calibration.

In this chapter, a new all-digital outphasing transmitter architecture was presented. As the DPM modulates each outphase angle directly in the digital domain, any phase mismatch caused by PAs or an RF combiner can be easily compensated within the resolution of the DPM. For complete error compensation, two distinct mismatch

compensation algorithms are used. One is static mismatch compensation for unbalanced paths, and the other one is for dynamic mismatch compensation. The dynamic error compensation is composed of common and differential phase calibration for error caused by the non-ideal behavior of both PAs and an RF combiner. The compensation can also be easily accomplished by using digital look-up tables. The simulation results show that the methods can improve the linearity.

CHAPTER IV

ALL-DIGITAL OUTPHASING MODULATOR IC

IMPLEMENTATION

4.1. IC Implementation

The architecture of the proposed all-digital outphasing transmitter was discussed in the previous chapter with system requirements and digital mismatch compensation algorithms. To verify the functionality of the all-digital outphasing transmitter technique and the mismatch compensation algorithms in real circuit implementation, a test chip of the digital modulator is designed and fabricated.

Figure 4.1 shows a block diagram of an all-digital outphasing transmitter. The chip consists of an on-chip PLL with a quadrature LC VCO, an I^2C block, two DPMs, and two driver amplifiers. The frequency range of the VCO is from 2.6 to 3.0 GHz, and it is controlled by 4-bit capacitor banks. Thus, the corresponding output frequency of DPM is from 650 to 750 MHz. The I^2C block sets various digital registers, such as the division number of PLL, capacitor tanks for the VCO, debugging ports, and so on. The target application of the modulator IC is a UHF band white space cognitive radio system, which is an emerging wireless communication standard based on the concept of opportunistic spectrum sharing [41].
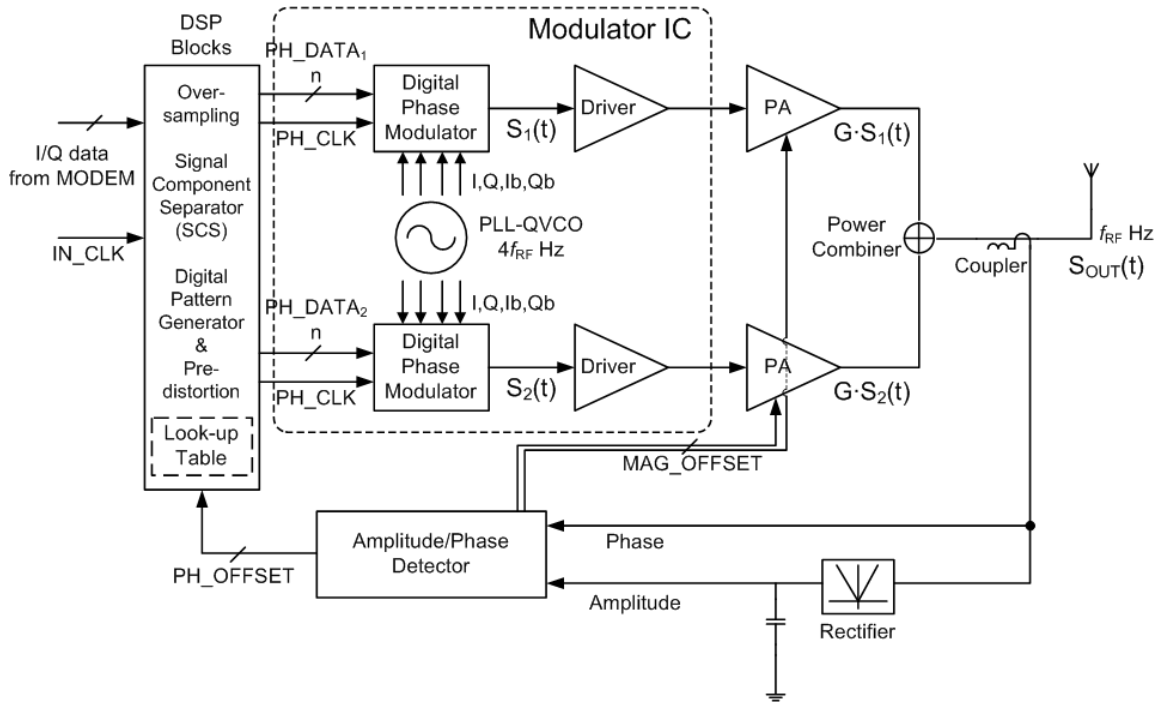
Figure 4.1. Block diagram of all-digital outphasing transmitter.

4.2. Building Blocks

4.2.1. Digital Phase Modulator

A clock frequency four times higher than the RF, provides two phase control bits for the two frequency dividers and two additional control bits are obtained by selecting one of the two quadrature signals of the clock. Finer phase control can be accomplished by a digital phase interpolator (PI).

Figure 4.2 shows a block diagram of the proposed DPM. The 9-bit phase data, *PH_DATA$_i$[8:0]*, control each building block for phase modulation: 2-bit for the 4:2 multiplexer (MUX), 1-bit for the 90°-pulse generator HOLD line, 1-bit for the XOR gate, and the remaining 5-bit for the digital PI.

PH_DATA$_i$ PHASE$_i$
9 9
PH_CLK
D Q
CLK Q̄

HOLD NOT
Pulse Generator PI 5
HOLD$_P$ RESET Binary to Thermometric Converter
MUX 2 PI$_T$ 32

CLK_I 0°
CLK_Q 90°
CLK_Ib 180°
CLK_Qb 270°
From PLL $f_0=4×f_{RF}$

4:2 MUX

A D Q CLK Q̄ FF1 C D Q CLK Q̄ FF3
B D Q CLK Q̄ FF2 D D Q CLK Q̄ FF4

E Φ$_{in}$
F Φ$_{in}$+22.5°

Digital Phase Interpolator

G S$_i$(t) $f_0'=f_{RF}$

MUX [1]	MUX [0]	HOLD	NOT	PI [4]	PI [3]	PI [2]	PI [1]	PI [0]

PH_DATA$_i$[8:0]

0
-180° ←→ +180°
Previous Phase

[00]/[0]/[0]
[11]/[1]/[1] [01]/[0]/[0]
[10]/[1]/[1] [10]/[0]/[0]
[01]/[1]/[1] [11]/[0]/[0]
[00]/[1]/[1] 22.5° [00]/[1]/[0]
[11]/[0]/[1] [01]/[1]/[0]
[10]/[0]/[1] [10]/[1]/[0]
[01]/[0]/[1] [11]/[1]/[0]
[00]/[0]/[1]

[ΔMUX[1:0]]/[HOLD]/[NOT]
4-bit coarse phase control by frequency divider

PI[4:0]/32 = α
E F
22.5°

G = αE + (1-α)F

5-bit fine phase control by phase interpolator

Figure 4.2. Block diagram of proposed 9-bit digital phase modulator.

The 4:2 MUX selects one pair of clock signals among four phase I/Q clock signals so that A leads B by 90°, i.e., (A, B) ∈ { (CLK_I, CLK_Q), (CLK_Q, CLK_Ib), (CLK_Ib, CLK_Qb), (CLK_Qb, CLK_I) }. Since the frequency of the quadrature VCO is four times that of the phase modulated signal, $S_i(t)$, the 4:2 MUX rotates phase with a step size of 22.5° from 0 to 90°. The following two D-flipflops (DFFs), FF1 and FF2, divide the clock signals, A and B, by two and delay the phase of 90° by holding the FF1 from toggling for one period of the clock signal when HOLD is high. The next two DFFs, FF3 and FF4, just divide the clock signals, C and D, by two. Thus, the four DFFs divide the clock signals by four and rotate the phase from 0 to 180° with a resolution of 22.5°. Then, the digital PI interpolates between the two clock signals, E and F, with 5-bit resolution. The digital PI, shown in Figure 4.3, consists of 32 unit gain cells in both paths

48

and the weighting of each path is controlled by the digital inputs of the PI, *PI[4:0]*, through a binary to thermometric converter. The XOR gate inverts the output of the digital PI, G, if NOT is high, which is equivalent to the additional phase of 180°. As a result, the DPM modulates phase from -180° to 180° a the step size of 360°/(2^9) or 0.703°.
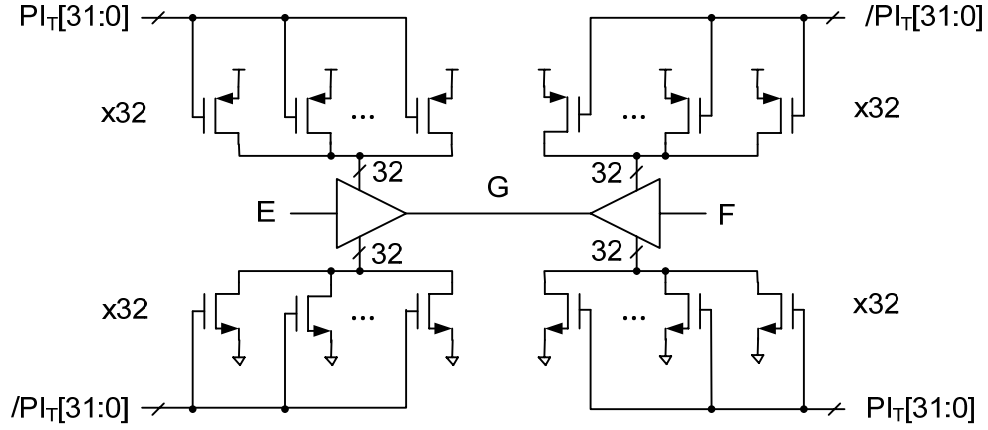

Figure 4.3. Circuit implementation of 5-bit digital phase interpolator.

The 5-bit PI may not have linear responses with respect to its input bits due to its open-loop structure. Figure 4.4 shows the delay measurement of the 5-bit PI. To get a better linearity, the input of the PI is calibrated by 4-bit input remapping and the PI has a 4-bit effective resolution after the remapping. As the 5-bit PI is designed to have an effective 4-bit resolution, the DPM has an 8-bit resolution and modulates the phase from -π to π with the minimum step size of π/2^8 or 1.41°.
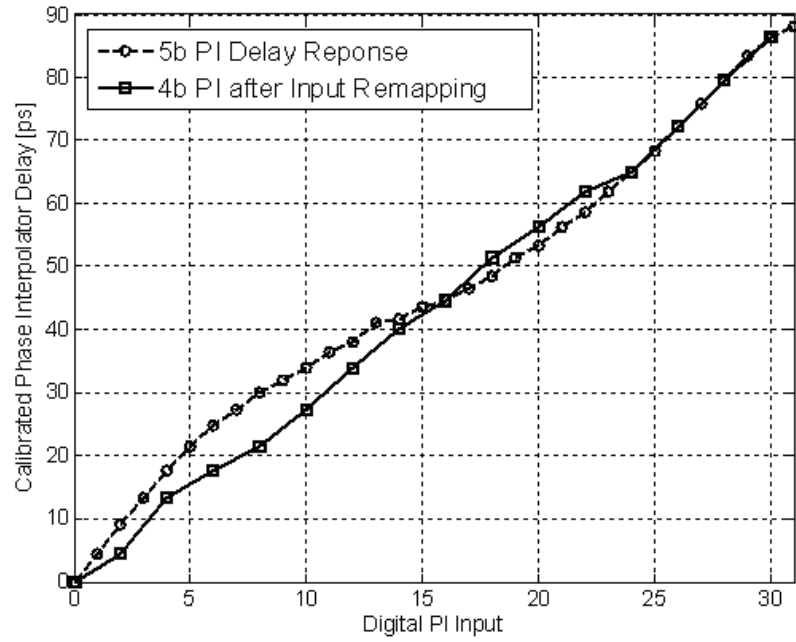
Figure 4.4. Measurement results and calibration of digital phase interpolator.

An exemplary timing diagram of the 9-bit DPM is shown in Figure 4.5.

Figure 4.5. Timing diagram of 9-bit digital phase modulator.

The simple DPM phase control facilitates phase calibration for various mismatch and error correction algorithms. Moreover, the proposed digital transmitter, implemented without conventional analog mixers and filters, is suitable for a wide variety of modulation schemes and signal bandwidths.

4.2.2. Voltage-Controlled Oscillator

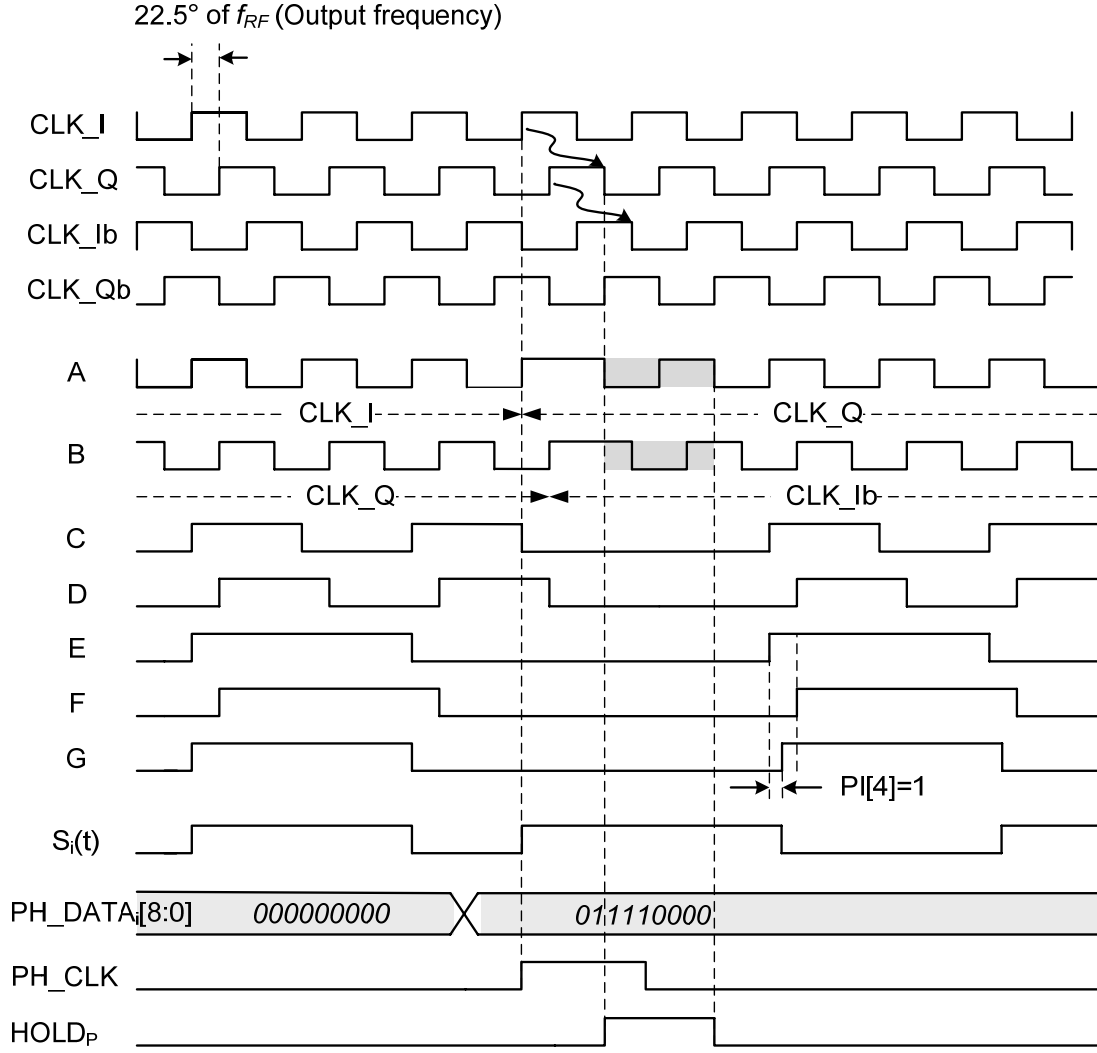Figure 4.6 shows the schematic of the quadrature VCO used in the modulator. The on-chip 2.2~2.8 GHz LC quadrature VCO generates differential I/Q clock signals for the proposed DPM. The LC-type VCO is used for low phase noise at clock outputs. By using large coupling transistors between two LC oscillators, the phase error between I/Q clock signals is kept low to not degrade the phase resolution of the DPM even if mismatch exists. The frequency band of the VCO is selected by a 4-bit control word, $C_{bank}[3:0]$, for both low VCO gain and wide frequency range.
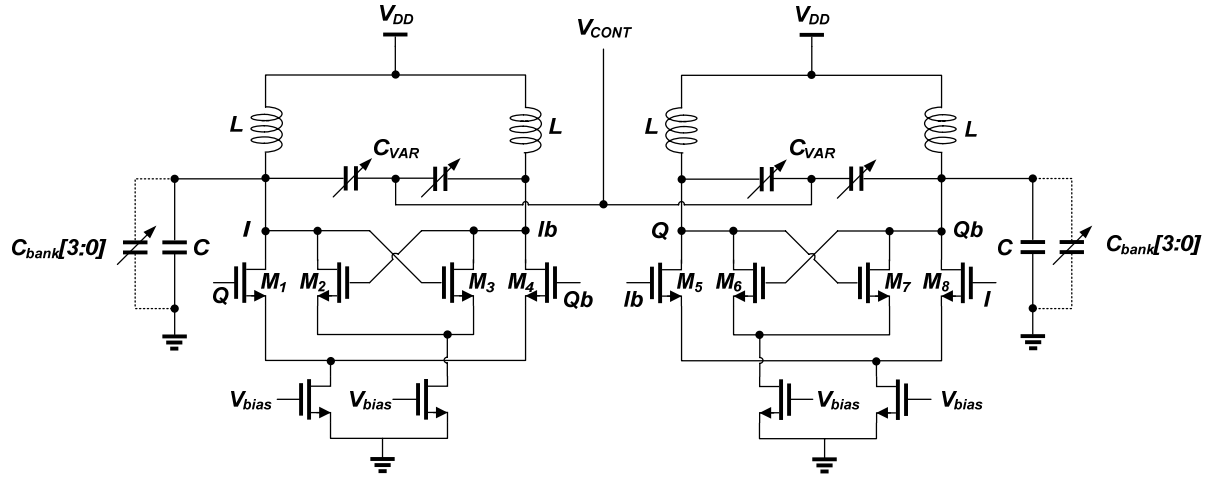
Figure 4.6. Schematic of on-chip quadrature VCO.

4.2.3. Frequency Synthesizer

The integrated PLL is a basic type-II, 3rd order integer-N PLL, as shown in Figure 4.7. It consists of a phase frequency detector (PFD), a charge pump (CP), a 2nd order loop filter, a quadrature LC VCO, and a dual modulus frequency divider. The frequency of the reference signal, f_{ref}, is 6 MHz and VCO frequency ranges from 2.2 to 2.8 GHz. The 2nd order loop filter consists of series R_1 and C_1 in parallel with C_2. C_2 is added to suppress

52

the ripples in the V_{cont} signal and is only about one-tenth of C_1 to not change the frequency response of the filter [42].

Figure 4.7. Block diagram of integrated frequency synthesizer.
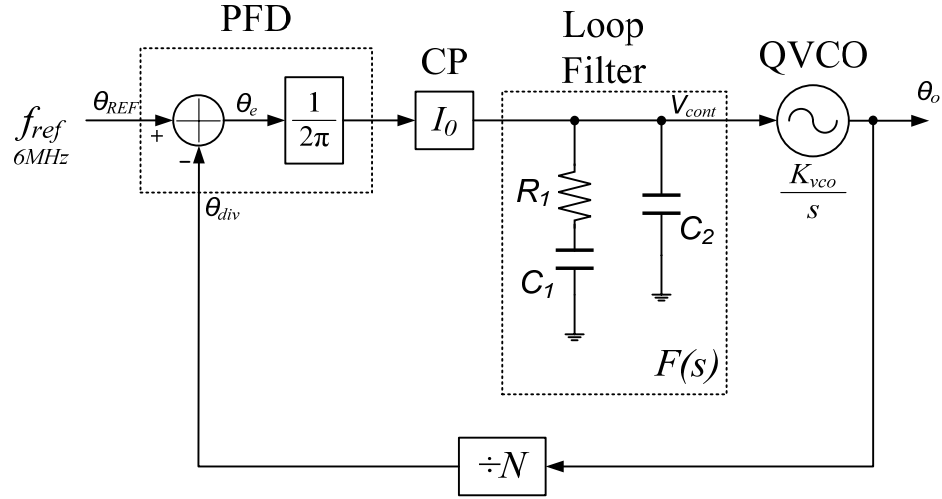
The transfer function of the loop filter in the PLL is

$$F(s) = \frac{1}{s \cdot (C_1 + C_2)} \cdot \frac{1 + s \cdot R_1 \cdot C_1}{1 + s \cdot R_1 \cdot C_k} \qquad (4.1)$$

where

$$C_k = \frac{C_1 \cdot C_2}{C_1 + C_2} .$$

Then, the open-loop transfer function of the synthesizer is given by

$$GH(s) = \frac{K_{VCO}}{2\pi} \cdot \frac{I_0}{N} \cdot \frac{F(s)}{s}$$

$$= \frac{K_\phi \cdot K_{VCO}}{N \cdot (C_1 + C_2) \cdot s^2} \cdot \frac{\dfrac{s}{\omega_z} + 1}{1 + \dfrac{s}{\omega_P}} \tag{4.2}$$

where

$$\omega_z = \frac{1}{R_1 \cdot C_1}, \quad \omega_p = \frac{C_1 + C_2}{R_1 \cdot C_1 \cdot C_2} = \frac{1}{R_1 \cdot C_k}, \text{ and } K_\phi = \frac{I_0}{2\pi}.$$

The magnitude of the transfer function and phase margin (PM) are then given by

$$\left| GH(\omega) \right| = \frac{K_\phi \cdot K_{VCO}}{N \cdot (C_1 + C_2) \cdot \omega^2} \sqrt{\frac{\left(\dfrac{\omega}{\omega_z}\right)^2 + 1}{1 + \dfrac{1}{\left(\dfrac{\omega_p}{\omega}\right)^2}}} \tag{4.3}$$

and

$$PM = tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - tan^{-1}\left(\left(\frac{\omega_p}{\omega_c}\right)^{-1}\right), \tag{4.4}$$

respectively, where the unit gain frequency is denoted as ω_c.

In this PLL design, the pole-zero location ratio, A ($A = \omega_c/\omega_z = \omega_p/\omega_c$), is determined as 3.16 for the PM of 55°. From the design parameters, the values of the loop filter are as follows.

$$R_1 = \frac{\omega_c \cdot N \cdot A^2}{K_\phi \cdot K_{VCO} \cdot (A^2 - 1)} \quad\quad\quad (4.5)$$

$$C_1 = \frac{K_\phi \cdot K_{VCO} \cdot (A^2 - 1)}{\omega_c^2 \cdot N \cdot A} \quad\quad\quad (4.6)$$

$$C_2 = \frac{K_\phi \cdot K_{VCO}}{\omega_c^2 \cdot N \cdot A} \quad\quad\quad (4.7)$$

With I_0=100 µA and K_{VCO}=80 MHz/V of designed circuit parameters, the values of the loop filter components are calculated as R_1=157.1 kΩ, C_1=7.114 pF, and C_2=791.7 fF, respectively.

4.3.   Measurement Results

The fully-integrated all-digital outphasing modulator IC was fabricated in a 0.18-µm CMOS technology. Figure 4.8 shows the die photograph of the chip. The die size is 4.48 mm^2 including ESDs and pads. The chip consists of an on-chip PLL with LC quadrature VCO, an I^{2}C block, two DPMs, and two DAs. The digital serial interface, I^{2}C, controls the chip through a PC via an Ethernet connection. The fabricated IC is mounted on an FR-4 PCB as a chip-on-board and a 6 MHz TCXO generates a reference clock for the PLL.
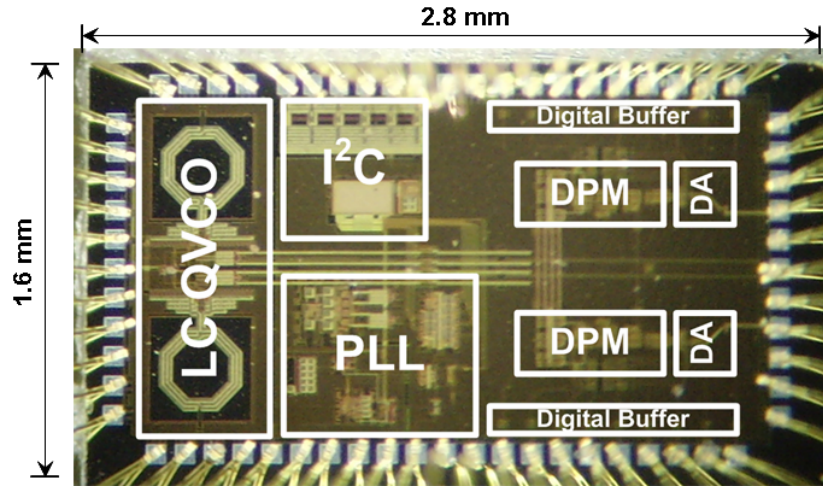
Figure 4.8. Chip microphotograph.

The current consumption of the frequency synthesizer including the quadrature VCO is 30 mA. Each DPM and DA consumes 35 mA and 4 mA, respectively. The total current consumption of the modulator IC is 120 mA from a 1.8 V supply including buffers and peripheral digital blocks.

Figure 4.9 shows the output spectrum and phase noise measurement results of the integrated PLL after DPM output. From the measurement, the reference spur level of the PLL is -64.22 dBc at 6 MHz offset. The measured phase noise is -120 dBc/Hz at 1 MHz offset when the output frequency of the quadrature VCO is 2.52 GHz.
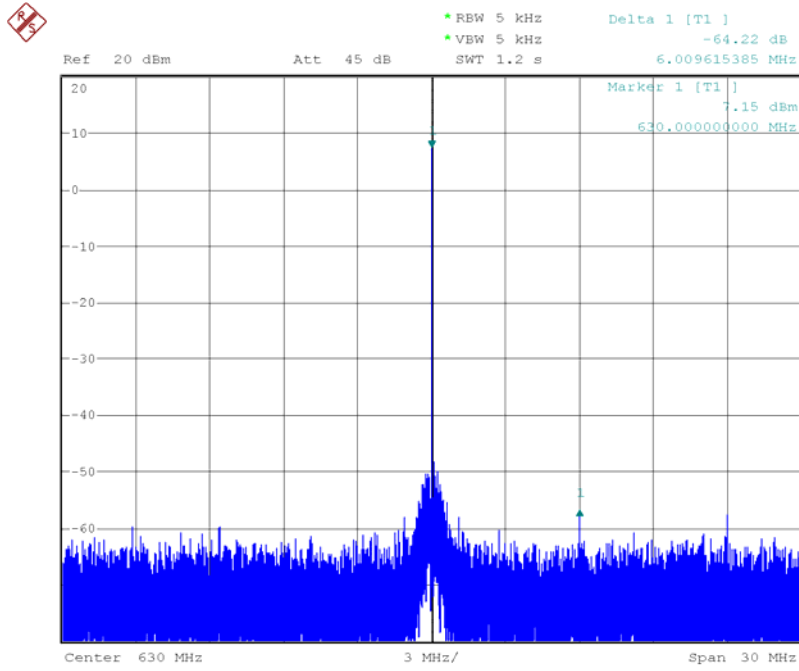
(a)
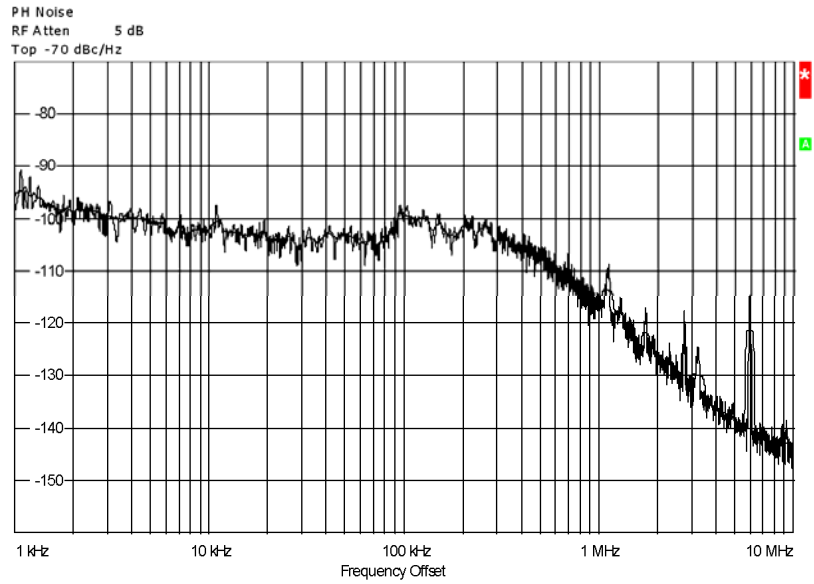
(b)

Figure 4.9. PLL measurement results. (a) Output spectrum, (b) Phase noise.

Figure 4.10 shows the measurement setup of the outphasing modulator chip. An 18-bit digital data generator provides phase information, *PH_DATA$_{1,2}$[8:0]*, into two

DPMs and two external saturated Class AB PAs with a wideband RF combiner are connected through SMA cables. The channel power is 21 dBm with external 20 dB PAs. For measurement, a -29 dB attenuator is used. A vector signal analyzer measured and recorded the output signal performance from the chip. The baseband phase data were generated by a MATLAB program and loaded into the digital data generator through a GPIB interface.
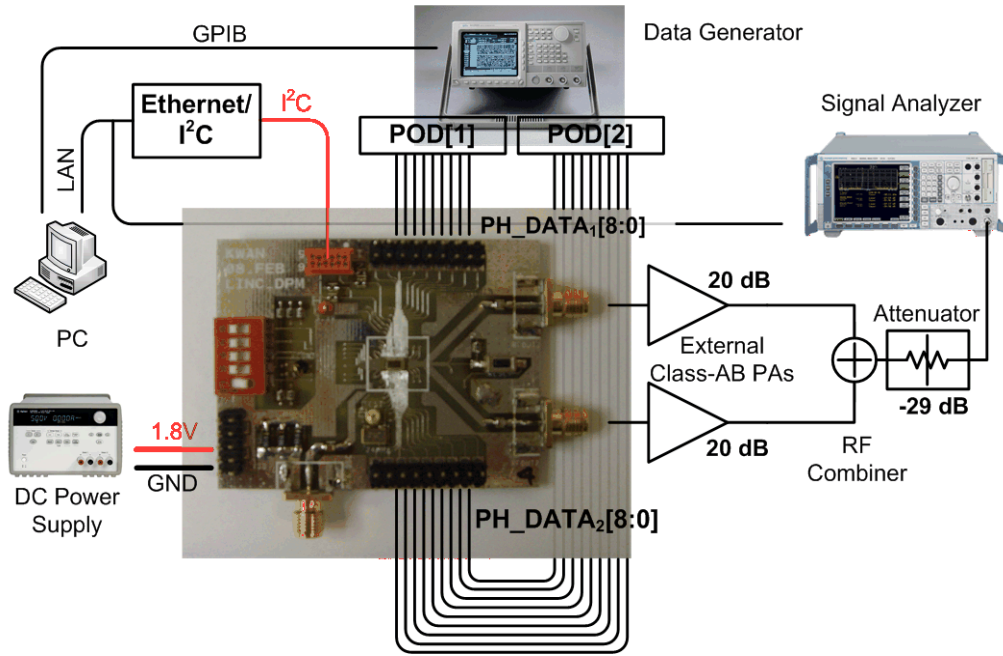

Figure 4.10. Measurement setup.

In Figure 4.11, the waveforms of *HOLD$_1$*, *PH_CLK*, *S$_1$(t)*, and *S$_2$(t)* show the operation of the DPM. In the example, two signals, *S$_1$(t)* and *S$_2$(t)*, have the same phase output at the beginning. After *PH_CLK* samples *HOLD$_1$* signal as 1, the phase of *S$_1$(t)* is delayed by $\pi/2$.

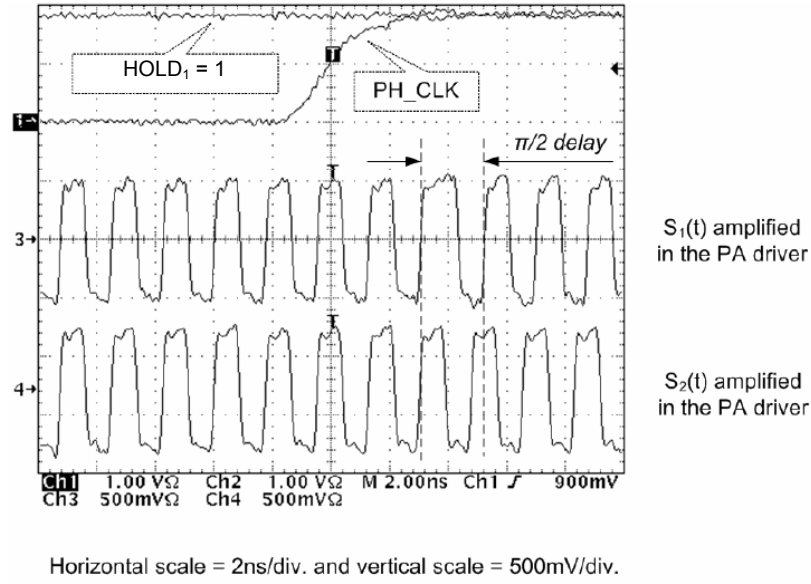Horizontal scale = 2ns/div. and vertical scale = 500mV/div.

Figure 4.11. Phase modulated $S_1(t)$ with $HOLD_1$ and PH_CLK.

To verify the feasibility of the modulator chip on OFDM signals, 7 MHz bandwidth 16-QAM IEEE 802.16e baseband symbols are used to generate the phase data, $PH\_DATA_{1,2}[8:0]$. The original baseband symbols have the symbol rate of f_B=8 MHz and oversampled to 48 MHz for digital image suppression.

Figure 4.12(a) shows the measured output signal spectrum before applying the mismatch compensation algorithms. Branch mismatches were due to the two external PAs and cables. The phase mismatch of 19.7° and gain mismatch were detected through the static mismatch measurement. Also, the test vectors for the dynamic mismatch compensation create 128-by-2 calibration look-up tables for the 9-bit DPMs. Each row has two compensation parameters, $\alpha(\theta)$ and $\beta(\theta)$, and they are recorded and applied according to the outphase angle, θ, with the resolution of 0.703° from 0° to 90°. In the figure, digital baseband images are apparent at the multiples of the baseband symbol rate, f_B=48 MHz.

59

Figure 4.12(b) shows the output signal spectrum after mismatch compensation. The adjacent channel power ratio (ACPR) of the signal spectrum is improved from -23 to -35 dBc at 10 MHz offset through the mismatch compensation algorithms. In addition, the baseband symbols are oversampled to f_B=80 MHz. By moving the images away from the operating frequency range of external PAs, the baseband images are effectively suppressed.

Before applying the mismatch compensation algorithms, no meaningful EVM value was measured due to the path mismatches. Figure 4.13 shows EVM results after the mismatch compensation. The digital mismatch compensation algorithms achieved an EVM of -25.38 dB, which satisfies the EVM limit for the 16-QAM modulation scheme.
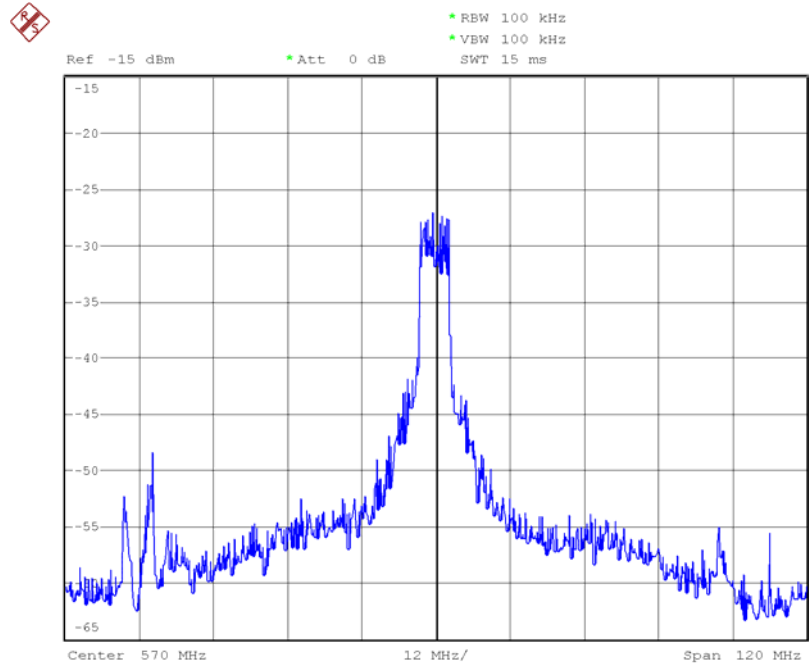
(a)
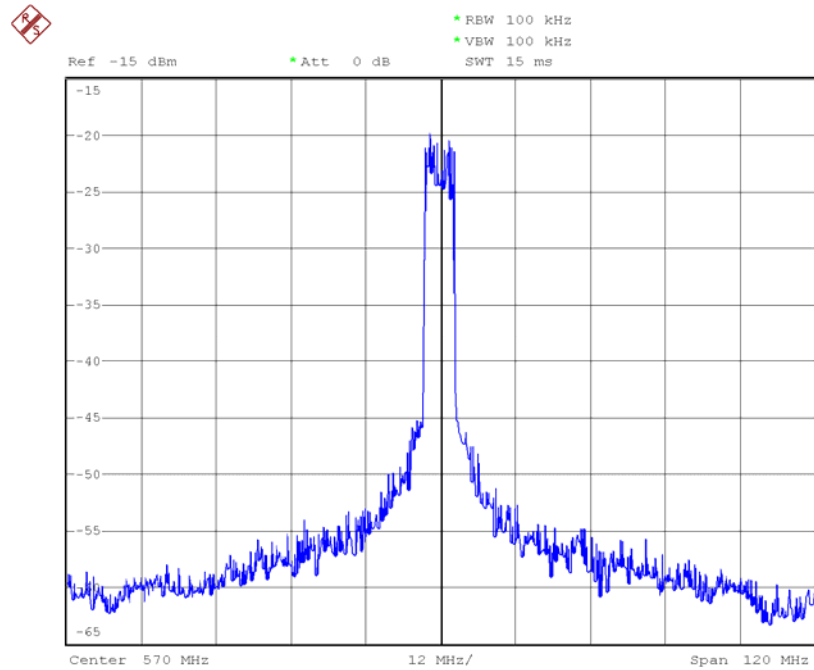
(b)

Figure 4.12. Spectrum of output signal before and after mismatch compensation. (a) Before mismatch compensation with f_B=48 MHz, (b) After mismatch compensation with f_B =80 MHz.

EVM = -25.38 dB
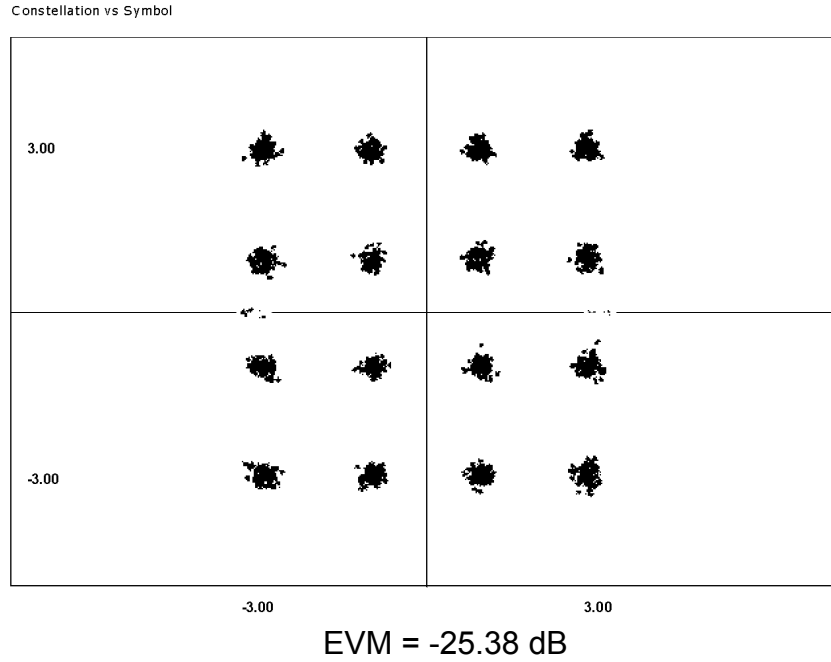
Figure 4.13. EVM measurement after mismatch compensation with f_B =80 MHz.

Table 4.1. Performance summary of outphasing modulator.

RF frequency [MHz]	Measured @ 570 Range: 450~800
Reference spur [dBc]	-64.22
Phase noise at 1MHz offset [dBc/Hz]	-120
Power consumption [mW]	216
Phase resolution [°]	0.703
Modulation scheme	IEEE 802.16e WiMax 16-QAM
ACPR [dBc]	-35
EVM [dB]	-25.38

The presented architecture demonstrates the possibility of an all-digital transmitter, which is highly reconfigurable for many communication standards and adaptive for various error calibrations. Also, as the development of CMOS processes reduces device size into the deep sub-micron region, the more digital circuits are

preferred. Therefore, the presented all-digital outphasing transmitter, implemented without analog mixer and filters, can be a good model for future digital RF transceivers.

CHAPTER V

A FULLY-INTEGRATED ALL-DIGITAL OUTPHASING

TRANSMITTER

The objective of this chapter is to evaluate various types of PAs in an outphasing amplification system and to implement a fully-integrated all-digital outphasing transmitter, which demonstrates a high performance in both efficiency and linearity with CMOS PAs.

In outphasing amplification, choosing the right type of power combiner is the key to maximize its efficiency performance. An isolated matched combiner, such as a Wilkinson combiner, has constant input and output impedances. Thus, it provides good isolation between two combined paths, which corresponds to good signal linearity but low average efficiency because the unused signal power is dissipated in a passive load when an output signal power is small [23]. This requires the use of a non-isolated combiner and the key advantage of the non-isolated combiner is the ability to maintain a high efficiency at the small output power by reducing DC currents.

Figure 5.1 shows a basic structure of a Wilkinson combiner. In a Wilkinson combiner, the input impedance of each port is always constant regardless of both input and output signals. Thus, input voltage and current have the same phase. To combine the

two input signals, V_1 and V_2, the quadrature components of the two inputs are dissipated in the isolation resister, $2 \cdot R_L$, which degrades combining efficiency.
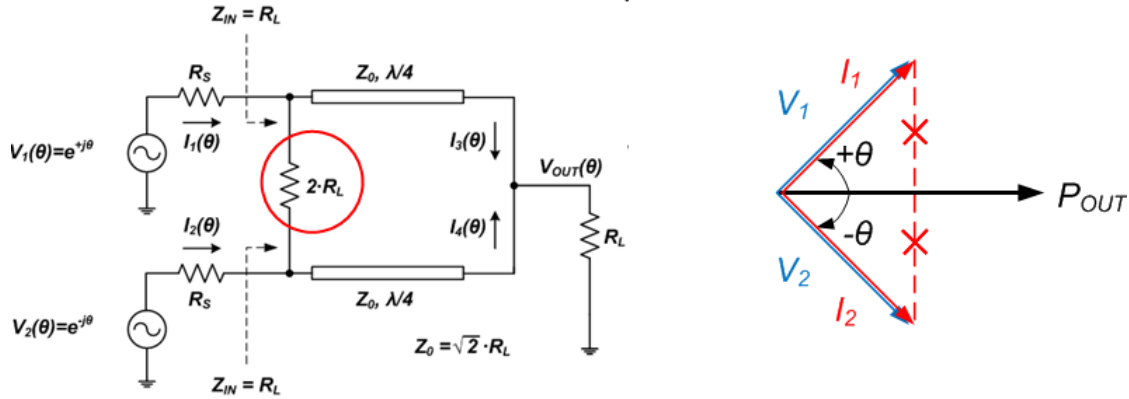

Figure 5.1. Wilkinson power combiner.

However, in a non-isolated combiner, there is no passive isolation component, as shown in Figure 5.2. Therefore, the achievable maximum combining efficiency can be 100 %, but each source should be carefully designed to not degrade combining linearity due to the non-isolation effects.
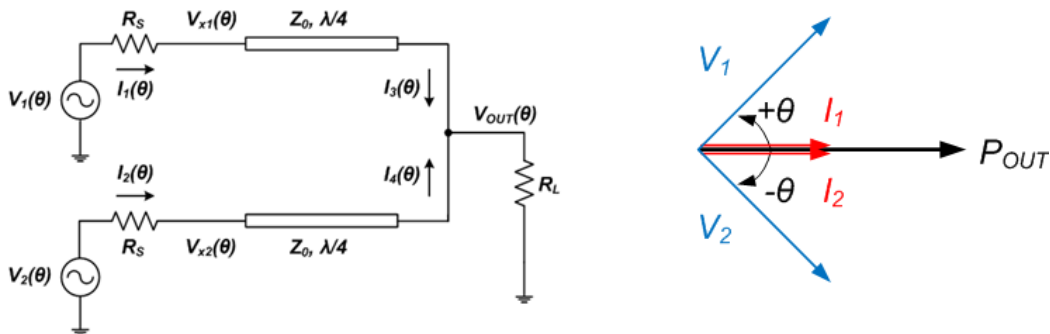
Figure 5.2. Non-isolated power combiner.

In Figure 5.3, the ideally achievable efficiency of the outphasing transmitter is computed with respect to output power levels. As shown in the figure, a Wilkinson combiner, one of the isolated combiners, provides good linearity, but the combining efficiency is degraded linearly when output signal decreases. On the contrary, a non-isolated combiner has a lossless combining structure and provides much higher combining efficiency than that of an isolated combiner.

Figure 5.3. Comparison of power efficiency with different combiner and PA structure.

Thus, to take the advantage of high efficiency, the proposed research will focus on the analysis of an optimum PA selection in a non-isolated combining architecture and on applying it to the design of a fully-integrated all-digital outphasing transmitter.

5.1. Power Combiner

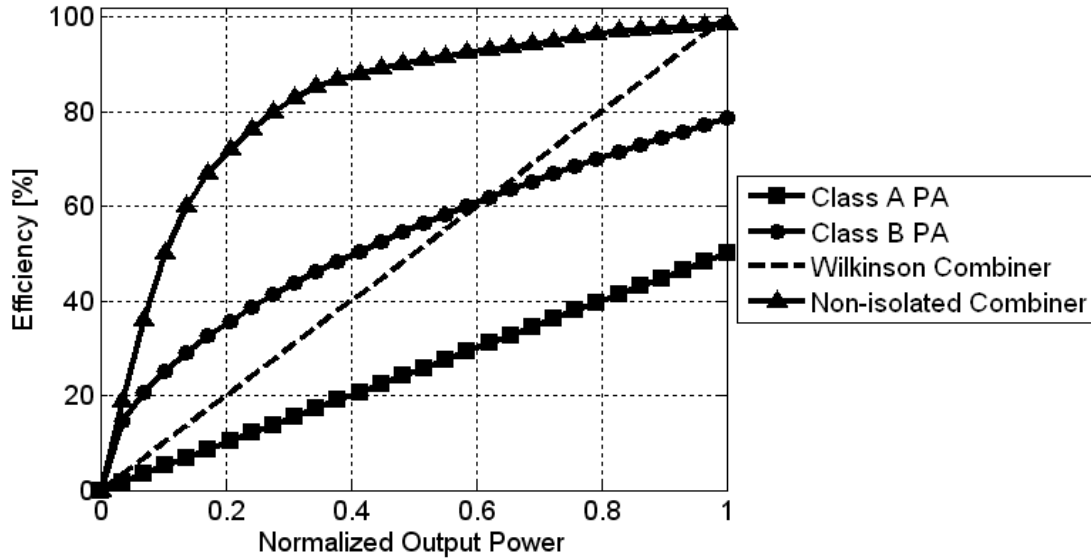Figure 5.4 shows a general three-port non-isolated combiner topology. Each switching PA is modeled as a voltage source. R_S is the output impedance of the PA and two quarter-wave transformers invert the impedance between the PA and load. Each voltage and current value of a node is represented by a function of the outphase angle, θ, to take non-isolation effects into account. In the non-isolated combiner, the equivalent input impedance of each port varies depending on the phase of input, which makes load modulation possible.
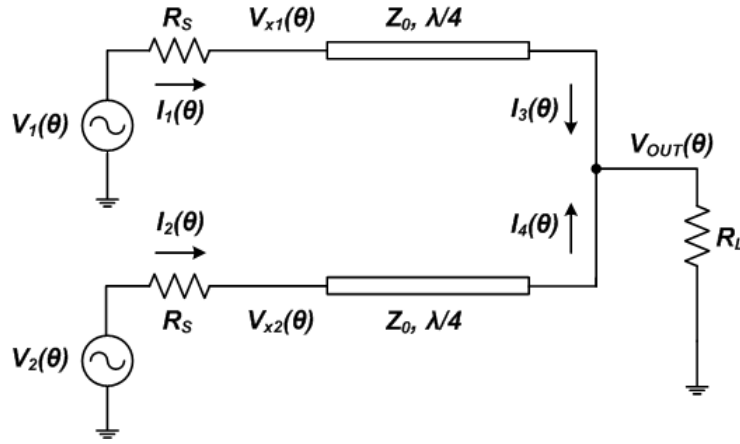
Figure 5.4. Non-isolated combiner with transmission lines.

From (2.5) and (2.6), the input voltages of the power combiner, $V_1(\theta)$ and $V_2(\theta)$, are defined as follows.

$$V_1(\theta) = A_{max} \cdot e^{j\theta} \tag{5.1}$$

$$V_2(\theta) = A_{max} \cdot e^{-j\theta} \tag{5.2}$$

The original signal angle, $\varphi(t)$, and dependence of θ on time are suppressed since it does not affect the mismatch analysis. It is assumed that the output impedances of two

PAs remain constant as R_S over all the outphase angles. To analyze the relationship between the two input signals and the output signal through the combiner, the properties of the quarter-wave transformer are used. Through the quarter-wave transformers, voltage is converted into current and vice versa [43].

$$V_{x1}(\theta) = j \cdot Z_0 \cdot I_3(\theta) \tag{5.3}$$

$$V_{x2}(\theta) = j \cdot Z_0 \cdot I_4(\theta) \tag{5.4}$$

$$I_1(\theta) = j \cdot \frac{1}{Z_0} \cdot V_{OUT}(\theta) \tag{5.5}$$

$$I_2(\theta) = j \cdot \frac{1}{Z_0} \cdot V_{OUT}(\theta) \tag{5.6}$$

From (5.5) and (5.6), $I_1(\theta)=I_2(\theta)$ and the output signal voltage and power of the combiner can be expressed as

$$
\begin{aligned}
V_{OUT}(\theta) &= -j \cdot \frac{A_{max} \cdot \cos\theta}{\left(\dfrac{R_S}{Z_0} + \dfrac{Z_0}{2 \cdot R_L}\right)} \\
&= -j \cdot \left(\frac{Z_0 \cdot R_L}{Z_0^{\,2} + 2 \cdot R_L \cdot R_S}\right) \cdot \left[V_1(\theta) + V_2(\theta)\right]
\end{aligned}
\tag{5.7}
$$

$$
\begin{aligned}
P_{OUT}(\theta) &= \frac{1}{2} \cdot \frac{\left|V_{OUT}(\theta)\right|^2}{R_L} \\
&= 2 \cdot R_L \cdot \left|\frac{Z_0 \cdot A_{max}}{Z_0^{\,2} + 2 \cdot R_L \cdot R_S}\right|^2 \cdot \cos^2(\theta)
\end{aligned}
\tag{5.8}
$$

respectively.

Therefore, the characteristic impedance of the quart-wave transformer, Z_0, should be selected to generate the desired output power at the load. Finally, the efficiency of the outphasing transmitter adopting the non-isolated combiner, η, can be summarized as

$$\eta(\theta) = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} = \frac{P_{OUT}}{P_{OUT} + \frac{1}{2} \cdot R_S \cdot \left(|I_1|^2 + |I_2|^2 \right)}$$
$$= \left| \frac{Z_0^2}{Z_0^2 + 2 \cdot R_L \cdot R_S} \right| \tag{5.9}$$

The load modulation effects in the non-isolated combiner forces the output currents of two PAs, $I_1(\theta)$ and $I_2(\theta)$, to be the same and the output signal is not distorted if each PA operates as an ideal voltage source. The combining efficiency is constant regardless of the outphase angle, θ, and always 100 % if R_S is zero. Therefore, to enhance the overall performance of the outphasing transmitter, the output impedance of PA, R_S, should be kept as small as possible.

It is shown that ideal voltage sources are required for the outphasing amplifier for both no signal distortion and maximum combining efficiency. However, the load-sensitive properties of actual PAs may influence the performance of the outphasing transmitter. In [32], various types of switching PAs, such as Class D, E, and F, were evaluated to find the optimum candidates for the outphasing transmitter by showing the voltage and current waveforms of the PAs without mathematical circuit analysis. The results argued that voltage-mode (VM) Class D, which is shown in Figure 5.5, is a good choice because it has an output current – a voltage relationship that is similar to the ideal voltage source, but the sensitive characteristics in load impedance of Class E, which is shown in Figure 5.6, render it a poor candidate for an outphasing transmitter. For proper

Class E operation, each passive element, such as C_{P1}, C_0, L_0, and R_{load}, should have a fixed value [44]. A Class F PA, which operates based on harmonic tuning and trap, has better voltage source characteristics than Class E, but bulky tuning circuits may not be suitable for an outphasing combine structure.
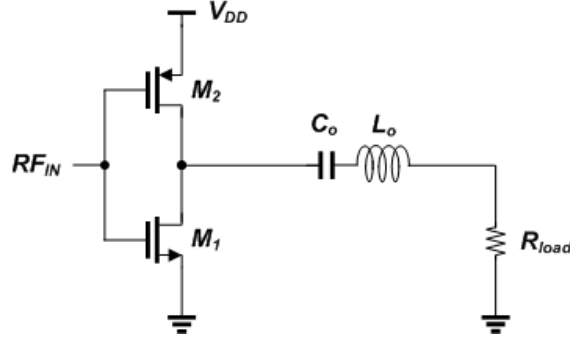
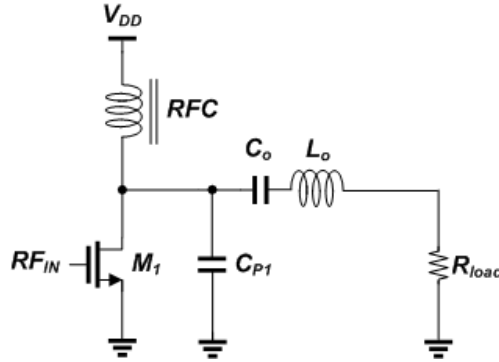Figure 5.5. Simple schematic of VM Class D PA.
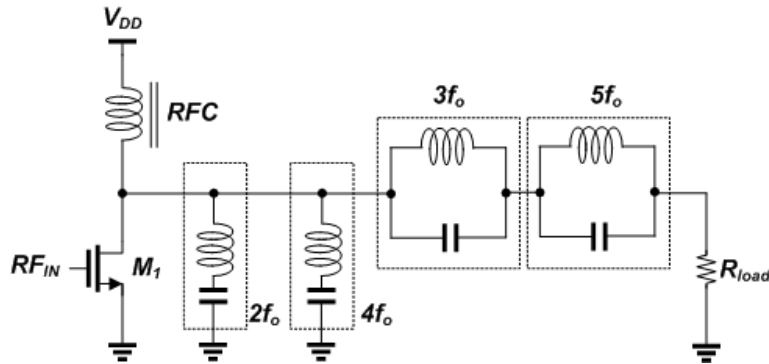
Figure 5.6. Simple schematic of Class E PA.

Figure 5.7. Simple schematic of Class F PA.

70

For more quantitative comparison, the combining efficiency and signal linearity is simulated as a function of the outphase angle, θ. Figure 5.8 and Figure 5.9 show the simulation results using the non-isolated combiner and the Wilkinson combiner with VM Class D and Class E. All transistors in the PAs are modeled as switches with R_{ON} of 0.5 Ω and designed to generate the same output power for fair comparison. From the results, the efficiency of the non-isolated combiner adopting VM Class D is almost 100 % over the entire outphase angles with perfect linearity, but the results of the non-isolated combiner using Class E show less efficiency improvement than the Wilkinson combiner with worse linearity.
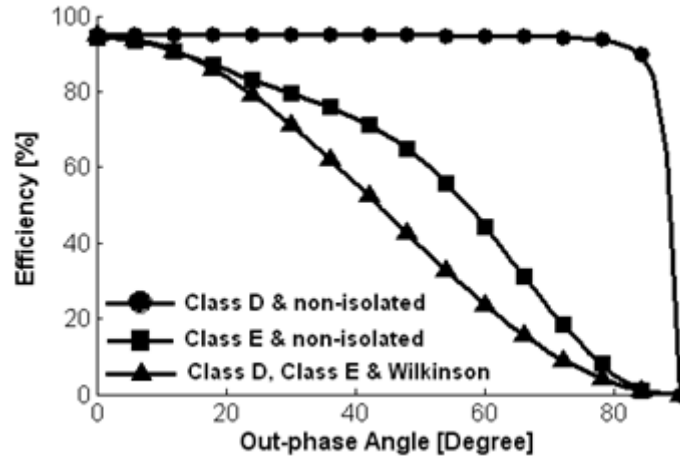

Figure 5.8. Efficiency comparison between isolated and non-isolated combiner.

Modern CMOS device scaling enables Class D PA to operate up to 2.5 GHz [45]. Therefore, further analysis will focus on the design using VM Class D. For the applications using much higher frequency above 2.5 GHz, Class F PA can be used with the non-isolated combiner as demonstrated in [46].
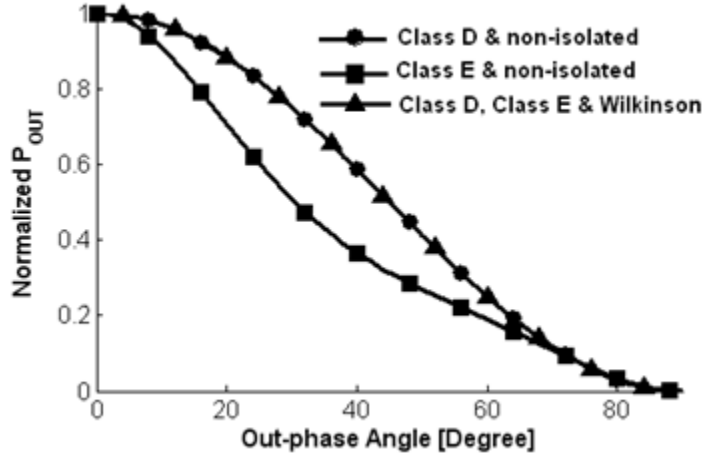
Figure 5.9. Linearity comparison between isolated and non-isolated combiner.

5.2. Design Considerations

Based on the analysis of a non-isolated combiner and PAs, it may be possible to achieve almost 100 % power efficiency over the entire output power range without degrading signal linearity. However, it may be impossible to implement it with real circuits. The non-ideal effects of actual circuits may degrade both the efficiency and linearity of the outphasing architecture.

5.2.1. Efficiency

In the efficiency simulation shown in Figure 5.8, Each PA is modeled as switch. When the switch is on, it has almost zero impedance, R_{ON}=0.5. When the switch is off, it is perfectly open, R_{OFF}=∞. However, the transistors in real PAs have bigger R_{ON} and finite R_{OFF}. In VM Class D, the R_{ON} of the two transistors can be regarded as r_{DS}. As r_{DS}

increases, the maximum achievable efficiency decreases due to power losses in the transistors as in (5.9). Thus, to achieve maximum efficiency, the gate-width of the transistor should be large enough to reduce r_{DS}. Also, it is desirable that the transistors turn on and off as abruptly as possible to have a constant r_{DS} value.

The parasitic capacitance, C_P, in the transistors should also be taken into account. The large gate-width transistors are necessary for maximum efficiency, but the large size transistors increase the parasitic capacitance. The parasitic capacitance can degrade efficiency by decreasing slew rate in Class D operation. The parasitic capacitance canceling technique inserting a parallel inductor, L_P, at the drain of the transistors may be used to compensate the efficiency degradation [47].

Figure 5.10 shows the complete model of a non-isolated combiner with VM Class D PAs. Quarter-wave transformers are implemented by π-networks for smaller circuit areas and the values of C_π and L_π are given by

$$C_\pi = \frac{1}{\omega \cdot Z_0} \tag{5.10}$$

$$L_\pi = \frac{Z_0}{\omega} \tag{5.11}$$

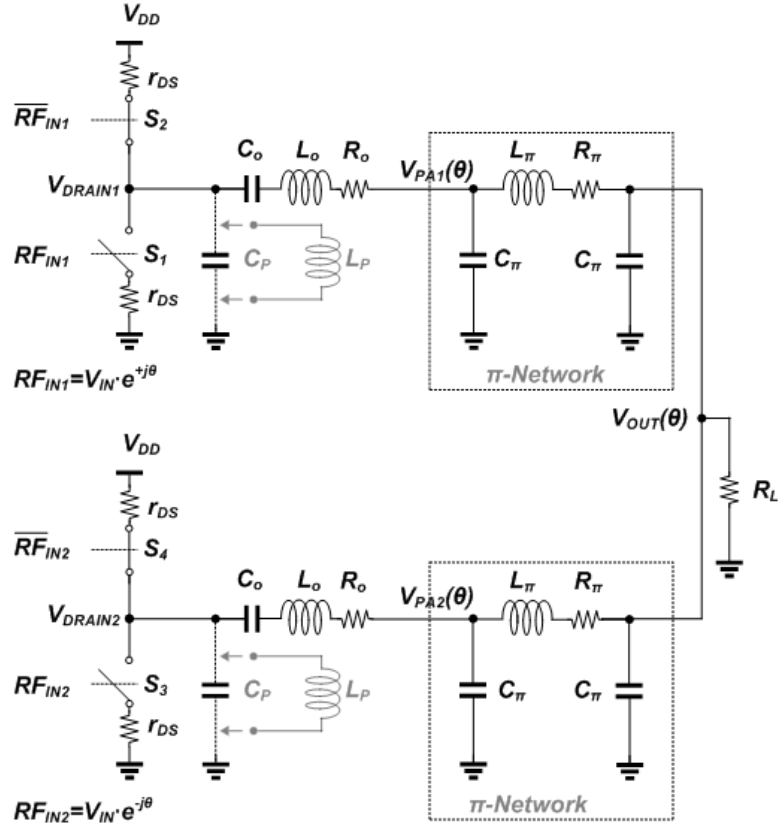where $\omega = 2 \cdot \pi \cdot f_{RF}$ and f_{RF} is the frequency of RF signals.

Figure 5.10. Schematic of VM Class D model with non-isolated combiner.

The series resonant circuit, C_0 and L_0, can be regarded as a short line at the carrier frequency, f_{RF}. Therefore, a simplified circuit diagram using ABCD matrices can be represented as Figure 5.11.
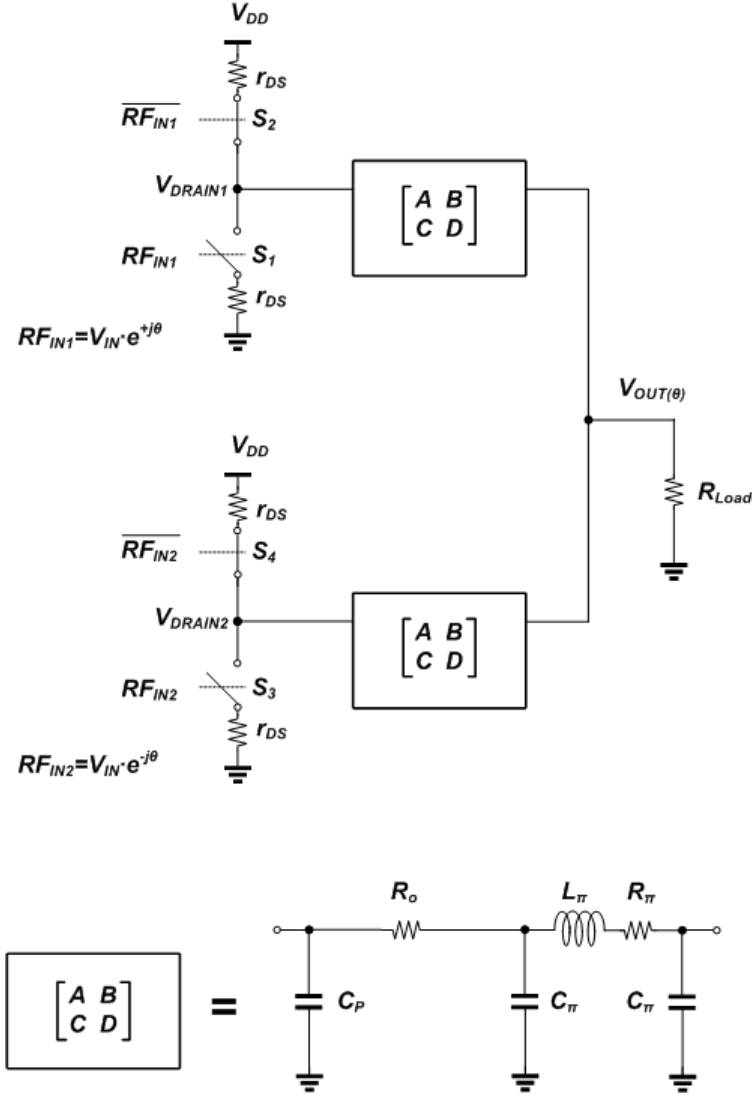
Figure 5.11. Simplified schematic of VM Class D model with non-isolated combiner.

The values of the ABCD matrix can be calculated as follows [43].

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}
$$

$$
= \begin{bmatrix} 1 & R_0 \\ j \cdot \omega \cdot C_P & 1 + j \cdot \omega \cdot C_P \cdot R_0 \end{bmatrix} \begin{bmatrix} j \cdot \omega \cdot C_\pi \cdot R_\pi & R_\pi + j \cdot \omega \cdot L_\pi \\ -\omega^2 \cdot C_\pi^2 \cdot R_\pi + j \cdot \omega \cdot C_\pi & j \cdot \omega \cdot R_\pi \cdot C_\pi \end{bmatrix} \tag{5.12}
$$

and

$$
A = -\omega^2 \cdot R_\pi \cdot R_0 \cdot C_\pi^2 + j \cdot \omega \cdot C_\pi \cdot \left(R_\pi + R_0 \right) \tag{5.13}
$$

$$B = R_\pi + j \cdot \omega \cdot (R_\pi \cdot R_0 \cdot C_\pi + L_\pi) \tag{5.14}$$

$$\begin{aligned} C = -\omega^2 \cdot C_\pi \cdot (R_\pi \cdot C_P + R_\pi \cdot C_\pi + R_0 \cdot C_P) \\ + j \cdot \omega \cdot C_\pi \cdot (1 - \omega^2 \cdot R_0 \cdot R_\pi \cdot C_P \cdot C_\pi) \end{aligned} \tag{5.15}$$

$$D = -\omega^2 \cdot C_P \cdot (L_\pi + R_0 \cdot R_\pi \cdot C_\pi) + j \cdot \omega \cdot R_\pi \cdot (C_P + C_\pi) \tag{5.16}$$

If the VM Class D PAs are modeled as ideal voltage sources, then the final schematic of the outphasing transmitter can be simplified, as shown in Figure 5.12.
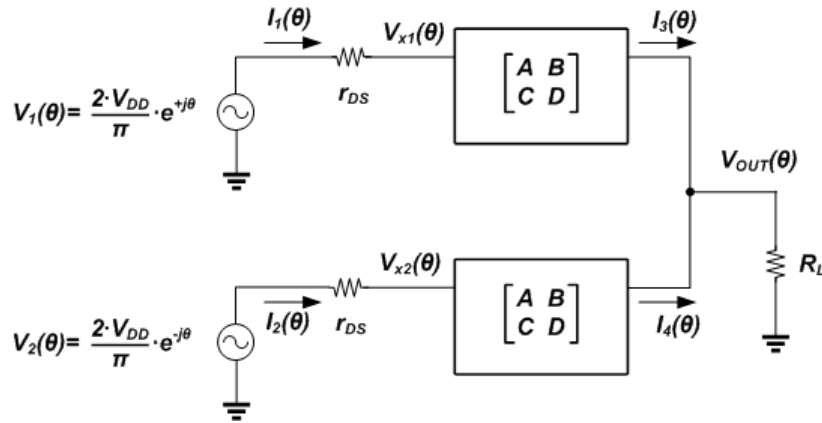
Figure 5.12. Equivalent schematic of VM Class D model with non-isolated combiner.

Based on the properties of an ABCD matrix, the final equivalent schematic can be analyzed as follows.

$$\begin{bmatrix} V_{X1}(\theta) \\ I_1(\theta) \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} V_{OUT}(\theta) \\ I_3(\theta) \end{bmatrix} \tag{5.17}$$

$$\begin{bmatrix} V_{X2}(\theta) \\ I_2(\theta) \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} V_{OUT}(\theta) \\ I_4(\theta) \end{bmatrix} \tag{5.18}$$

and

$$V_1(\theta) - V_{X1}(\theta) = r_{DS} \cdot I_1(\theta) \qquad (5.19)$$

$$V_2(\theta) - V_{X2}(\theta) = r_{DS} \cdot I_2(\theta) \qquad (5.20)$$

$$V_{OUT}(\theta) = R_L \cdot \left[I_3(\theta) + I_4(\theta) \right] \qquad (5.21)$$

Thus,

$$V_{X1}(\theta) + V_{X2}(\theta) = \left(2 \cdot A + \frac{B}{R_L} \right) \cdot V_{OUT}(\theta) \qquad (5.22)$$

$$I_1(\theta) + I_2(\theta) = \left(2 \cdot C + \frac{D}{R_L} \right) \cdot V_{OUT}(\theta) \qquad (5.23)$$

$$\frac{V_1(\theta) + V_2(\theta) - \left[V_{X1}(\theta) + V_{X2}(\theta) \right]}{r_{DS}} = I_1(\theta) + I_2(\theta) \qquad (5.24)$$

$$\left[r_{DC} \cdot \left(2 \cdot C + \frac{D}{R_L} \right) + 2 \cdot A + \frac{B}{R_L} \right] \cdot V_{OUT}(\theta) = V_1(\theta) + V_2(\theta). \qquad (5.25)$$

Finally, both the output voltage and the overall efficiency of the outphasing transmitter are calculated including all passive elements and parasitic effects. The output voltage is

$$V_{OUT}(\theta) = \frac{\dfrac{4}{\pi} \cdot V_{DD} \cdot \cos\theta}{r_{DS} \cdot \left(2 \cdot C + \dfrac{D}{R_L} \right) + 2 \cdot A + \dfrac{B}{R_L}} \qquad (5.26)$$

and the overall power efficiency is

$$\eta(\theta) = \cfrac{\cfrac{|V_{OUT}(\theta)|^2}{R_L}}{V_1(\theta) \cdot I_1^*(\theta) + V_2(\theta) \cdot I_2^*(\theta)}$$

$$= \cfrac{\cfrac{|V_{OUT}(\theta)|^2}{R_L}}{V_1(\theta) \cdot \left[C \cdot V_{OUT}(\theta) + D \cdot I_3(\theta)\right]^* + V_2(\theta) \cdot \left[C \cdot V_{OUT}(\theta) + D \cdot I_4(\theta)\right]^*} \qquad (5.27)$$

$$= \cfrac{\cfrac{\pi}{2} \cdot \cfrac{|V_{OUT}(\theta)|^2}{V_{DD} \cdot R_L}}{\left| \left(2 \cdot C + \cfrac{D}{R_L}\right)^* \cdot V_{OUT}^*(\theta) \cdot \cos\theta + \cfrac{\left(\cfrac{4}{\pi} \cdot V_{DD}\right) \cdot \sin^2\theta}{\left| r_{DS} + \cfrac{B}{D} \right|} \right|}$$

The four main factors that can degrade the overall efficiency of the outphasing transmitter using VM Class D PAs are C_P, r_{DS}, R_0, and R_π. The calculation results of their effects on the efficiency are summarized in Figure 5.13, Figure 5.14, Figure 5.15, and Figure 5.16.
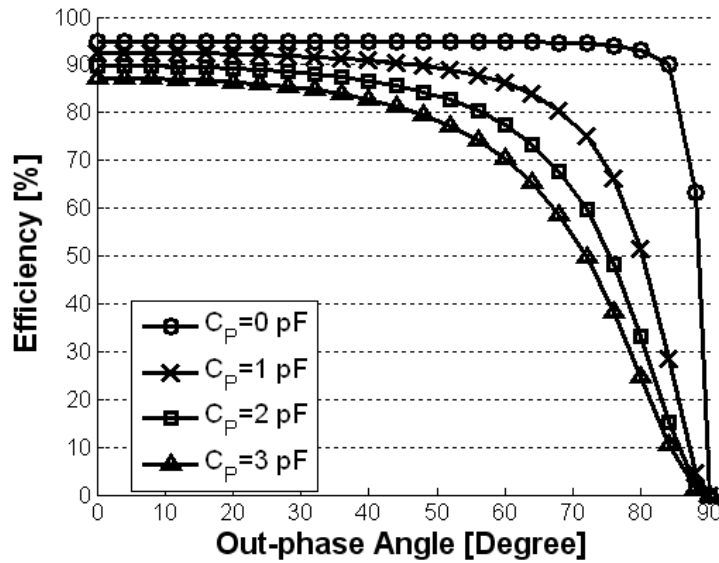

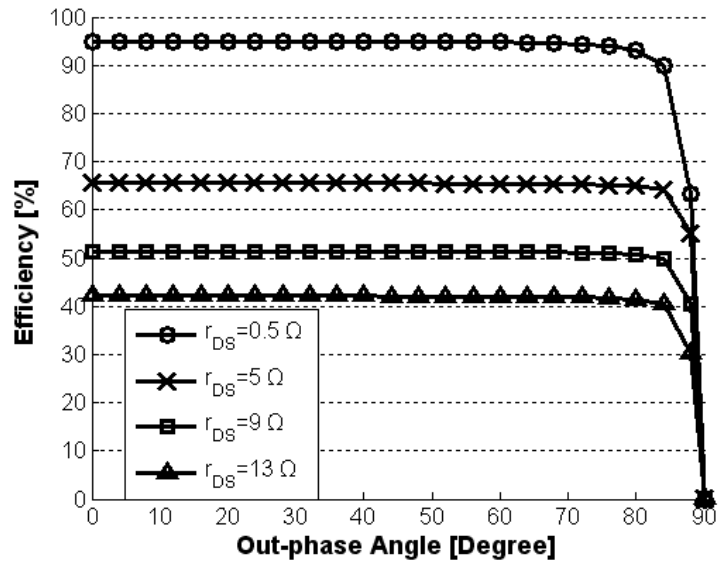Figure 5.13. Efficiency results with different C_P values.

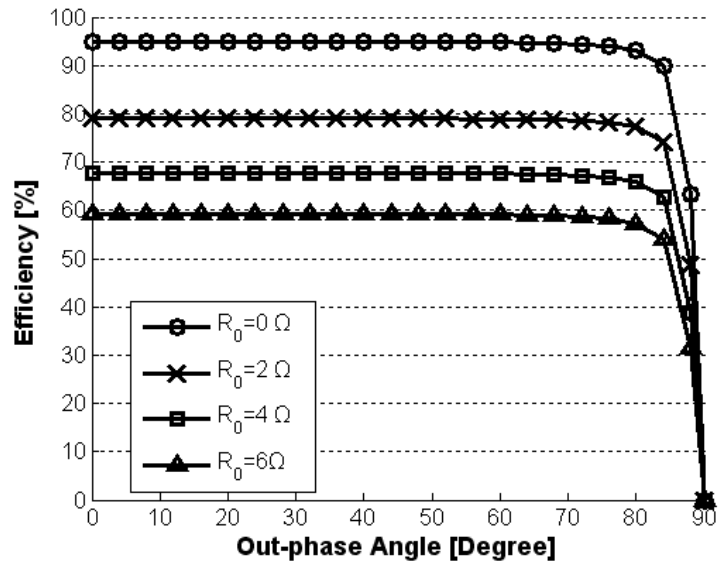Figure 5.14. Efficiency results with different r_{DS} values.

Figure 5.15. Efficiency results with different R_0 values.
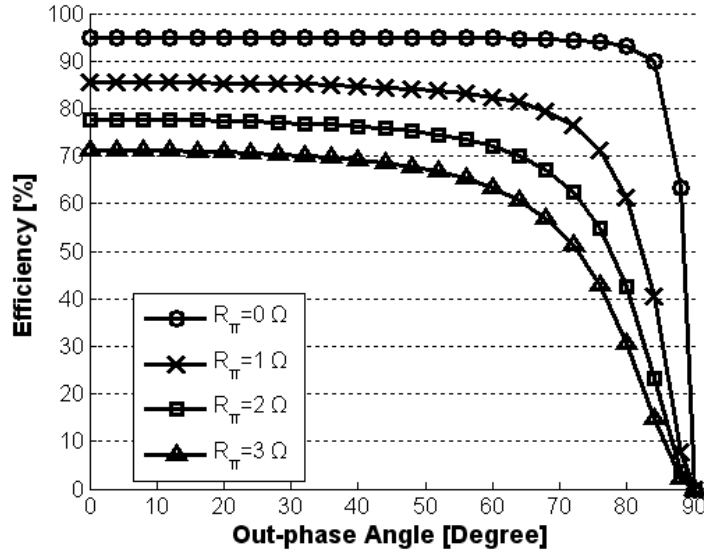
Figure 5.16. Efficiency results with different R_π values.

5.2.2. Linearity

As long as the two signal paths of the transmitter are symmetrical, the output of the outphasing amplifier is perfectly linear as shown in (5.26). However, process, voltage and temperature (PVT) variations of real circuits can generate path mismatches; thus they degrade the overall signal linearity. Moreover, the mismatches and variations change as time goes. Therefore, the only way to calibrate the mismatch effects is to measure them in actual circuits and compensate them continuously. The most significant advantage of the proposed DPM-based transmitter is that the calibration is much easier and simpler than the methods using the conventional calculation-based predistortion presented in [15] and [20]. As shown in chapter 4, any mismatches caused by circuits can be detected and stored in digital look-up tables for each frequency channel because the DPM has a finite number of output vectors.

5.3. Circuit Implementation

To verify the efficiency analysis of the all-digital outphasing transmitter with a different PA structure in real circuit implementation, two test chips of the fully-integrated all-digital outphasing transmitter are designed and fabricated. The fully-integrated all-digital outphasing transmitter IC was fabricated in a 0.18-μm CMOS technology. Figure 5.17 shows a block diagram of an all-digital outphasing transmitter. Each chip consists of an all-digital outphasing modulator, which is demonstrated in chapter 4, and integrated CMOS Class D and Class E PAs. However, quadrature clock signals are generated from differential divider with an external clock signal for a simple architecture and die area saving in the transmitter with class D PAs.
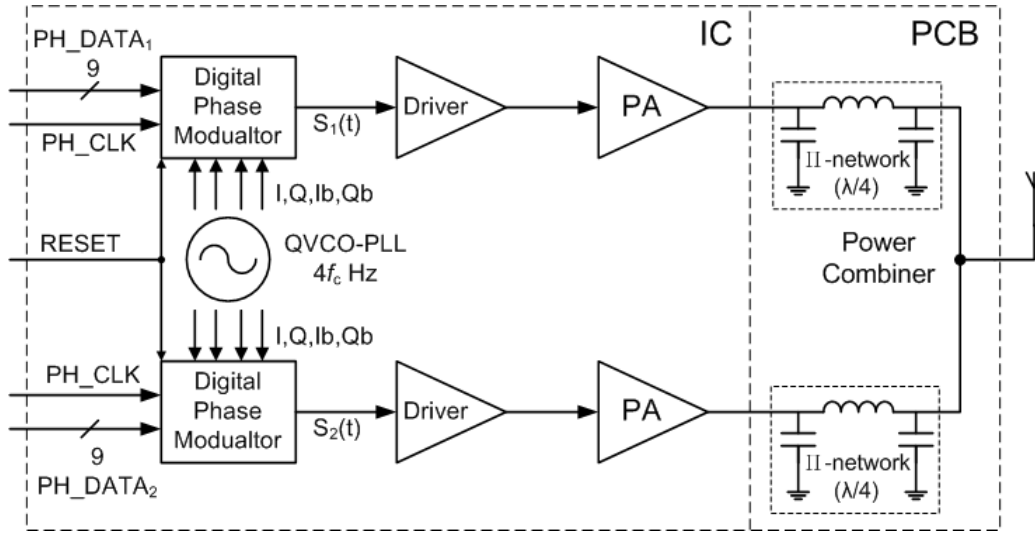
Figure 5.17. Block diagram of fully-integrated all-digital outphasing transmitter.

Figure 5.18 and Figure 5.19 show the die photograph of the chips.

81
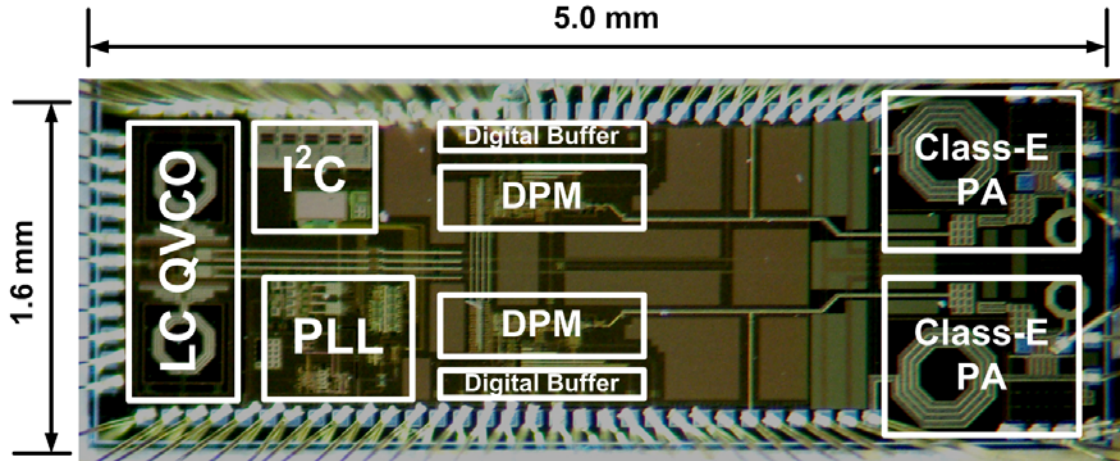
Figure 5.18. Chip micrograph (Fully-integrated all-digital outphasing transmitter with Class E PAs).
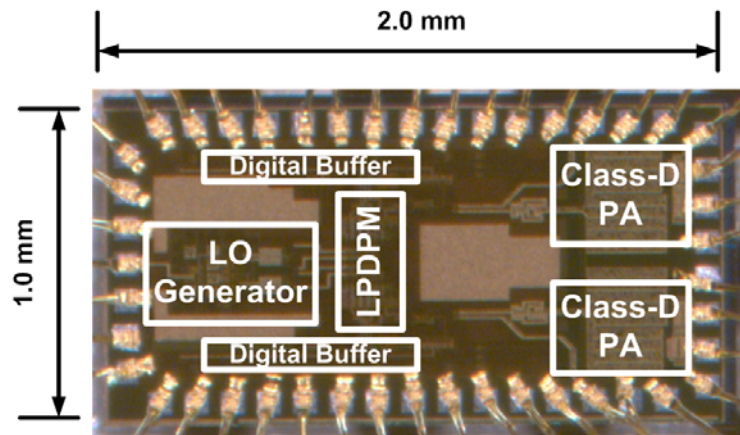
Figure 5.19. Chip micrograph (All-digital outphasing transmitter with LPDPM and Class D PAs).

The outphasing transmitter IC, which is implemented with Class E PAs, uses isolated Wilkinson combiner due to the load-sensitive characteristics of a Class E amplifier. For Class E switching operations, a strict load condition should be met, otherwise both efficiency and linearity of Class E PA are significantly degraded [49]. With the isolated combiner, the transmitter has an advantage in overall linearity performance with expense of combing efficiency.

The outphasing transmitter using Class D PAs is designed for the operations with highly power-efficiency non-isolated combiner. As demonstrated in this chapter, Class D PA has the similar characteristics of ideal voltage source; thus it may show better combing efficiency compared to the transmitter using isolated combiner. Any linearity degradation caused by non-ideal effects of real circuits can be calibrated with the compensation algorithms presented in chapter 3.

5.4. Key building Blocks

The outphasing transmitter integrated with Class E PAs has the same building blocks with the all-digital outphasing modulator presented in chapter 4 except for the integrated PAs. However, the outphasing transmitter that uses Class D PAs has a different DPM structure for low power operations.

5.4.1. Low Power Digital Phase Modulator

Figure 5.20 shows a block diagram of the proposed low power DPM (LPDPM). The 9-bit phase data, $PH\_DATA_i[8:0]$, control each building block for phase modulation: 3-bit for the 9:2 multiplexer (MUX), 1-bit for the XOR gate, and the remaining 5-bit for the digital PI.

Figure 5.20. Block diagram of proposed low power digital phase modulator.

Compared to the DPM design proposed in the outphasing modulator in chapter 4, the new LPDPM generates all possible nine phases (A though H and /A) from quadrature clock signals. Therefore, desirable output phases can be easily selected from the multiple phases by the simple 9:2 MUX. Moreover, the two signal paths, S_1 and S_2, of the outphasing transmitter can share the LPDPM phase generation core. An exemplary timing diagram of the 9-bit LPDPM is shown in Figure 5.21.

Figure 5.21. Block diagram of proposed low power digital phase modulator.

For the circuit implementation of the proposed LPDPM, true single phase clocking (TSPC) D-flipflops are used for high-speed operations [48]. The schematic of the TSPC flipflop and the operating principles of the digital PI are shown in Figure 5.22.

(a)   (b)

Figure 5.22. Building blocks for LPDPM. (a) Schematic of TSPC D-flipflop, (b) Digital PI.

5.4.2. Class E Power Amplifier with Isolated Combiner

Figure 5.23 shows the schematic of Class E PAs and Wilkinson power combiner. The Class E PA consists of driver and power stages. Input signals, S_1 and S_2, are fed from DPMs of the digital outphasing modulator. A target operating frequency ranges from 400 to 800 MHz.
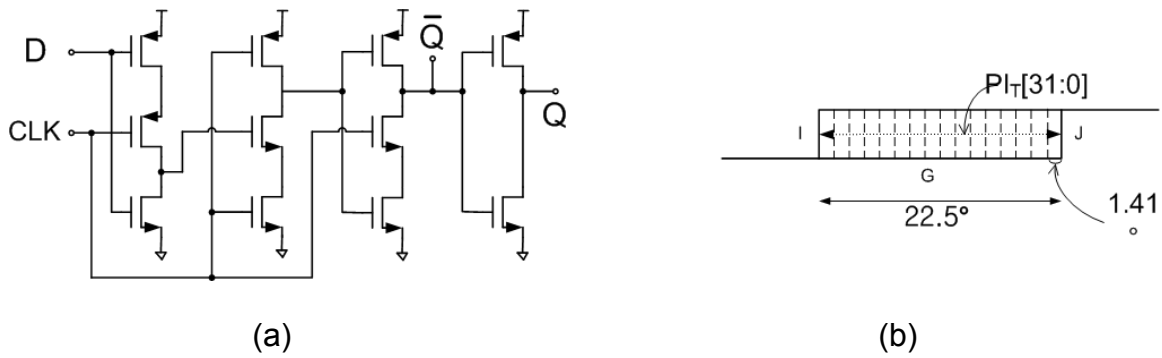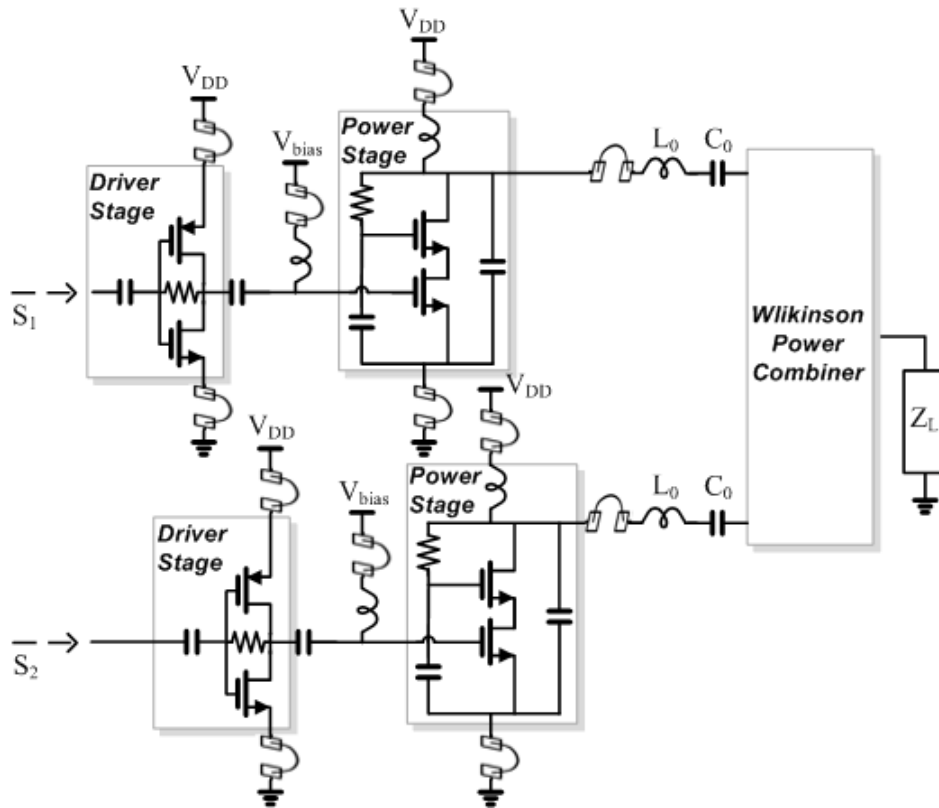

Figure 5.23. Schematic of implemented Class E PAs and combiner.

5.4.3. Class D Power Amplifier with Non-isolated Combiner

The schematic for Class D PAs and non-isolated combiner is already shown in Figure 5.10. For a Class D PA design, the well-known Class D architecture, shown in Figure 5.5, is used. The target output power of each PA is 20 dBm; thus the maximum

output power of the outphasing transmitter will be around 23 dBm. The operating frequency band is the same as that of Class E PA.

5.5. Measurement Results

5.5.1. Measurement Setup

The measurement setup for each outphasing transmitter is shown in Figure 5.24 and Figure 5.25, respectively. The fabricated ICs are mounted on an FR-4 PCB as a chip-on-board. Digital control bit streams are generated in digital pattern generator and the modulation performance of each transmitter is measured through a vector signal analyzer.
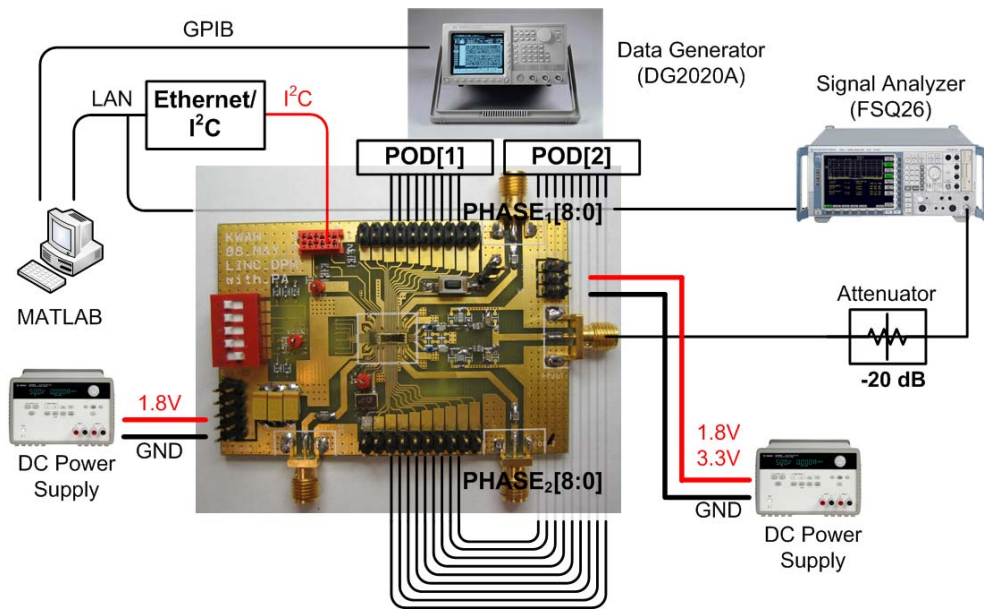

Figure 5.24. IC measurement setup for fully-integrated all-digital outphasing transmitter with Class E PAs.
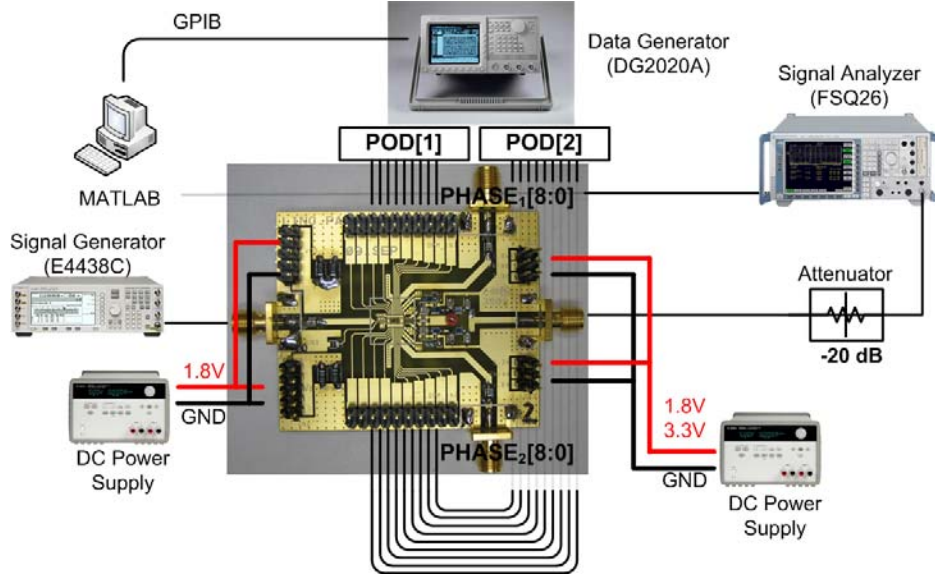
Figure 5.25. IC measurement setup for all-digital outphasing transmitter with Class D PAs.

Both efficiency and linearity of each digital outphasing transmitter are measured and compared. To save die area, the outphasing transmitter using Class D PAs uses high-speed differential frequency divider circuits instead of an integrated PLL for quadrature clock generation.

5.5.2. Measurement Results

Figure 5.26 shows the measurement results of the outphasing transmitter using Class E PAs and an isolated Wilkinson combiner. As the transmitter IC uses an isolated combiner, it demonstrates good linearity. However, the combining efficiency is degraded linearly as the output power decreases because each Class E PA consumes constant DC power regardless of the combined output power.
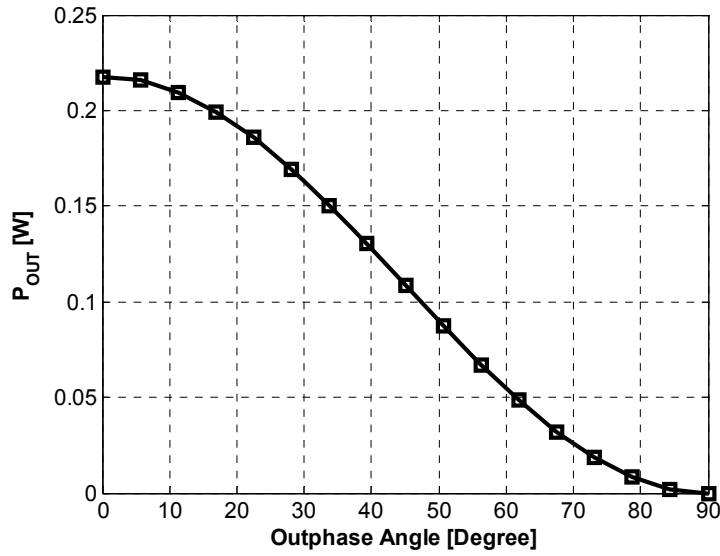
(a)
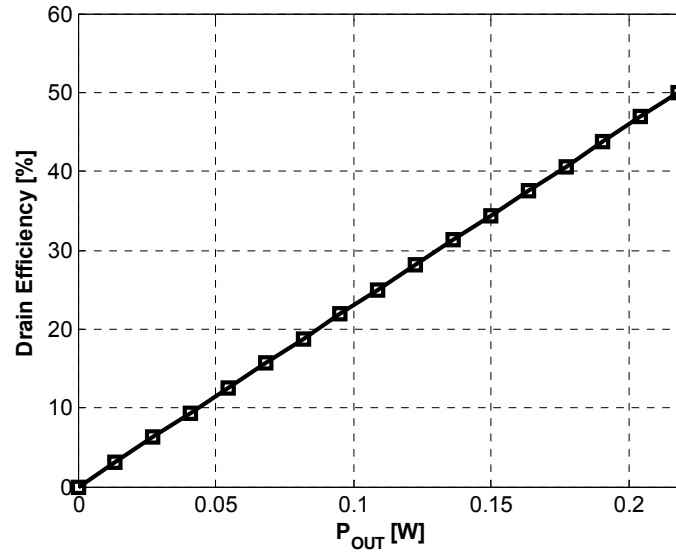
(b)

Figure 5.26. Output power and efficiency measured with different outphase angle in outphasing transmitter with Class E PAs. (a) Output power, (b) Drain efficiency.

Figure 5.27 shows the measurement results of the outphasing transmitter using Class D PAs and a non-isolated combiner. As the transmitter uses a non-isolated combiner, it shows linearity degradation compared to the transmitter using Class E PAs

with an ideal combiner. However, it demonstrates a better combining efficiency performance due to the load modulation effects presented in (5.27).
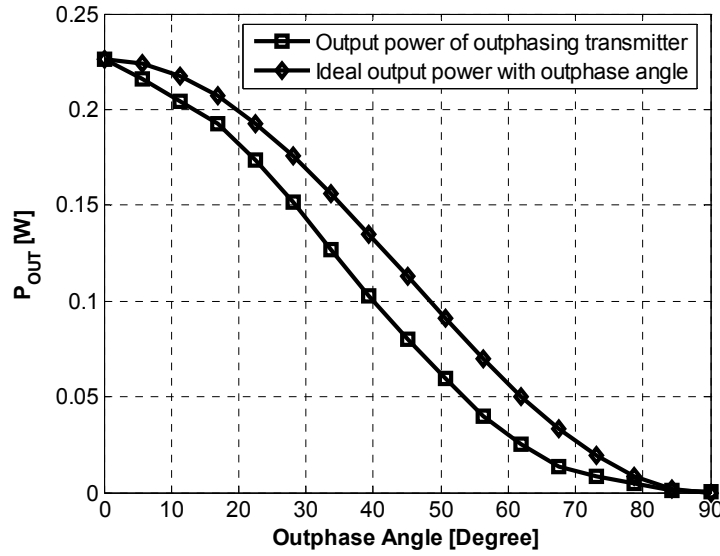
(a)
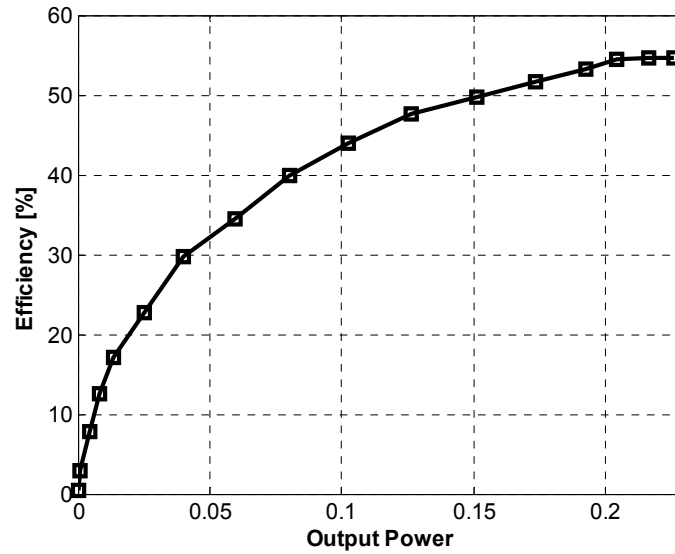
(b)

Figure 5.27. Output power and efficiency measured with different outphase angle in outphasing transmitter with Class D PAs. (a) Output power, (b) Drain efficiency.

Finally, Figure 5.28 and Figure 5.29 show the output spectrum and constellation results of the outphasing transmitter using Class E and Class D PAs, respectively.
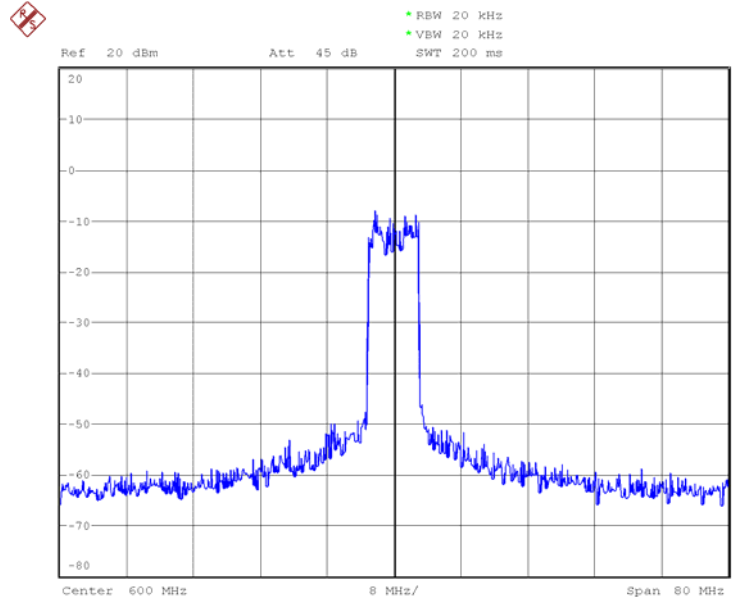
(a)
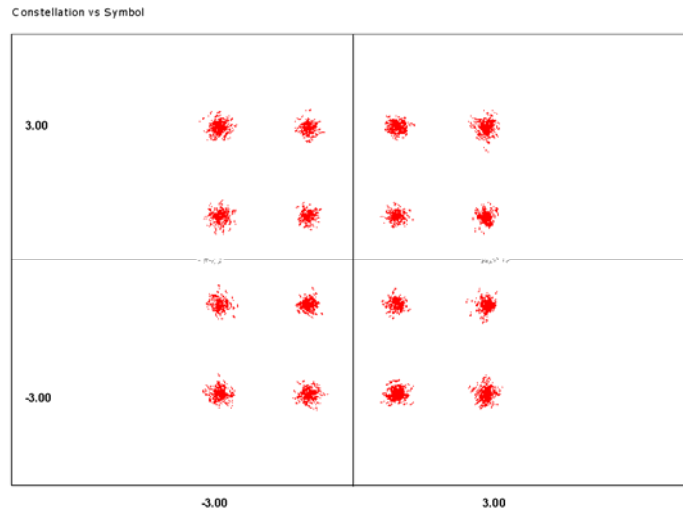
(b)

Figure 5.28. Output spectrum and EVM measured in outphasing transmitter with Class E PAs. (a) Output spectrum, (b) Constellation (EVM=-26.7 dB).

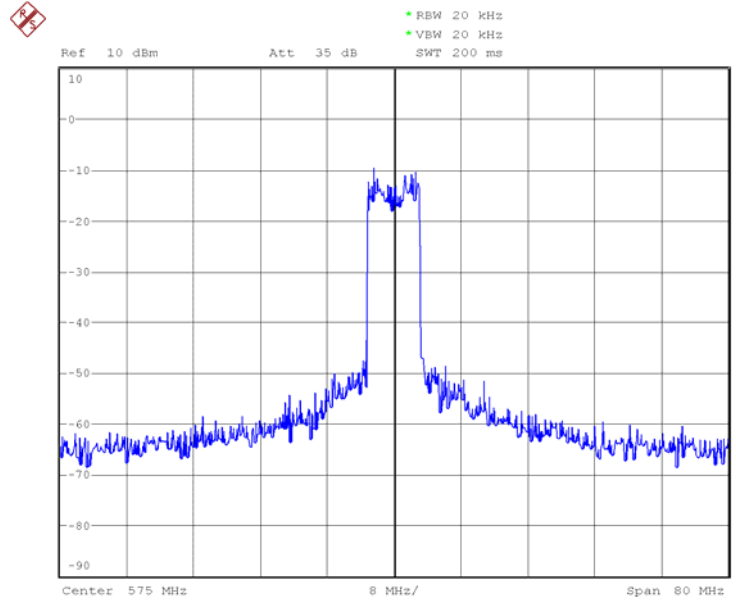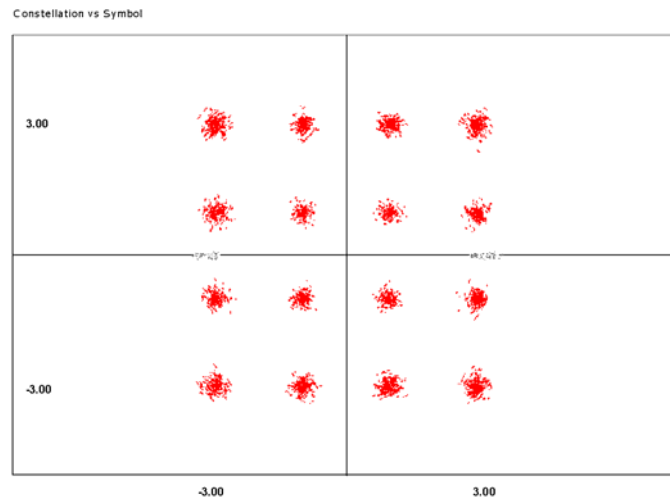Figure 5.29. Output spectrum and EVM measured in outphasing transmitter with Class D PAs. (a) Output spectrum, (b) Constellation (EVM=-25.5 dB).

Any linearity degradation caused by the non-isolation effects of a combiner were calibrated at digital baseband bit streams by the compensation algorithms presented in chapter 3. The measurement results show that a LPDPM consumes 42 mA at a 1.8 V supply.

92

CHAPTER VI

CONCLUSION

In this research, a new all-digital outphasing transmitter architecture was presented, along with a comprehensive circuit and system description. As the DPM modulates each outphase angle directly in the digital domain, any phase mismatch caused by PAs or the RF combiner can be easily compensated within the resolution of the DPM. For complete error compensation, two distinct mismatch compensation algorithms are used. One provides static mismatch compensation for unbalanced paths, and the other one is for dynamic mismatch compensation. The dynamic error compensation is composed of common and differential phase calibration for error caused by the non-ideal behavior of both PAs and the RF combiner. The compensation is easily accomplished by incorporating calibration results into digital look-up tables. The measurement results show that the modulator chip implementing these compensation methods can effectively amplify an OFDM signal and improve the amplifier linearity.

The proposed architecture demonstrates the possibility of an all-digital transmitter, which is highly reconfigurable for many communication standards and adaptive for various error calibrations. Also, as the development of CMOS processes reduces device size into the deep sub-micron region, the more digital circuits are preferred. Therefore,

the proposed all-digital outphasing transmitter, implemented without analog mixer and

filters, can be a good model for future digital RF transceivers.

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