EORGIA INSTITUTE OF TECHNOLOGY — OFFICE OF CONTRACT ADMINISTRATION

PROJECT ADMINISTRATION DATA SHEET

[X] ORIGINAL
[ ] REVISION NO. ____

roject No. A-2917 — DATE: 4/13/81

roject Director: Dr. N. W. Cox, Jr. — ~~School~~/Lab EML/PSD

ponsor: Hughes Aircraft Company, Space and Communications Group;
El Segundo, California 90245

ype Agreement: Purchase Order No. 28-712179-LV3

ward Period: From 3/11/81 To ~~6/15/81~~ 9/15/81 (Performance) ---- (Reports)

ponsor Amount: $13,000 (Firm Fixed Price) — Contracted through:

ost Sharing: None — (GTRI)/~~GIT~~

itle: Analysis of Four (4) GaAs FET's

DMINISTRATIVE DATA — OCA CONTACT Duane Hutchison x 4820

) Sponsor Technical Contact:

) Sponsor Admin./Contractual Contact: Mr. R. W. Nastri, Buyer; Bldg. S12, Mail Station W323; Hughes Aircraft Company; P. O. Box 92919 - Airport Station; Los Angeles, California 90009 (213) 648-8693

eports: See Deliverable Schedule — Security Classification: None

efense Priority Rating: None

ESTRICTIONS

ee Attached N/A Supplemental Information Sheet for Additional Requirements.

ravel: Foreign travel must have prior approval - Contact OCA in each case. Domestic travel requires sponsor approval where total will exceed greater of $500 or 125% of approved proposal budget category.

quipment: Title vests with Sponsor; however, none authorized/proposed.

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GEORGIA INSTITUTE OF TECHNOLOGY OFFICE OF CONTRACT ADMINISTRATION

SPONSORED PROJECT TERMINATION SHEET

Date 9/28/81

Project Title: Analysis of Four (4) GaAs FET's

Project No: A-2917

Project Director: Dr. N. W. Cox, Jr.

Sponsor: Hughes Aircraft Co., Space & Communications Group

Effective Termination Date: 9/15/81

Clearance of Accounting Charges: 9/15/81

Grant/Contract Closeout Actions Remaining:

- [x] Final Invoice ~~and Closing Documents~~
- [ ] Final Fiscal Report
- [ ] Final Report of Inventions
- [ ] Govt. Property Inventory & Related Certificate
- [ ] Classified Material Certificate
- [ ] Other _____

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A - 2917

ANALYSIS OF MICROWAVE FIELD EFFECT TRANSISTORS

Prepared for:

Space and Communications Group
Hughes Aircraft Company
Los Angeles, California

Requisition Number 599775

Prepared by:

J. W. Amoss
N. W. Cox
G. N. Hill

Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

15 September 1981

INTRODUCTION

The work described in this report was performed for the Space and Communications Group, Hughes Aircraft Company, under Requisition Number 599775 dated January 26, 1981. The job description stated that the Georgia Tech Research Institute was to:

> "Analyze four GaAs FETs labeled 'A', 'B', 'C', 'D' that will be sent under separate cover. Information desired is a complete description of both horizontal and vertical geometries. Materials and material properties associated with these geometries. Semiconductor doping profiles, buffer layer quality and thickness, contact resistance, crystallogographic orientation of gate, presence of N^+ contacts, gate recess (if any), drift mobility, and current voltage curves. Caution: these FETs are subject to damage from static electricity, equipment voltage spikes and self oscillation if not terminated with resistive loads. It is expected that these FETs will be destroyed during the course of analysis and need not be returned."

Upon receipt of order, the following tasks were defined:

1) Mount chip and examine optically. Take photograph. Identify gate, source, and drain pads. Obtain overall and large-scale dimensions from photograph.

2) Obtain current-voltage curves.

3) Obtain SEM photos and estimate area of gate.

4) Take C-V measurements between gate and source-drain.

5) Slice sample and SEM. Use energy dispersive X-ray analysis capability of SEM to identify materials. Use voltage contrast capability to determine thickness (and possible doping profile) of active region.

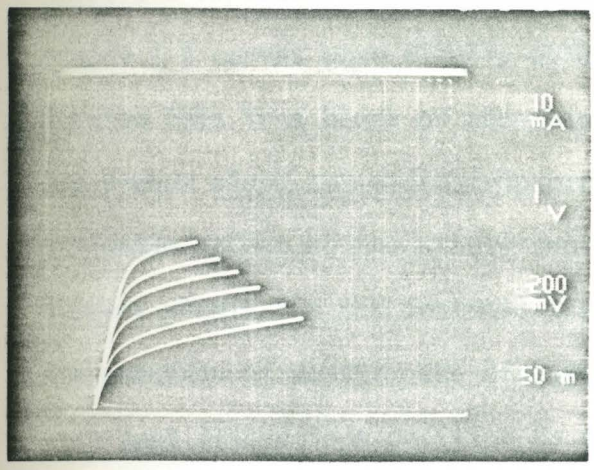
6) Determine crystallographic orientation of gate by X-ray diffraction techniques.

During these investigations, Georgia Tech received three separate shipments of FETs. In each case they were labeled with the manufacturers name rather than with the letters A, B, C, D as specified in the work description.

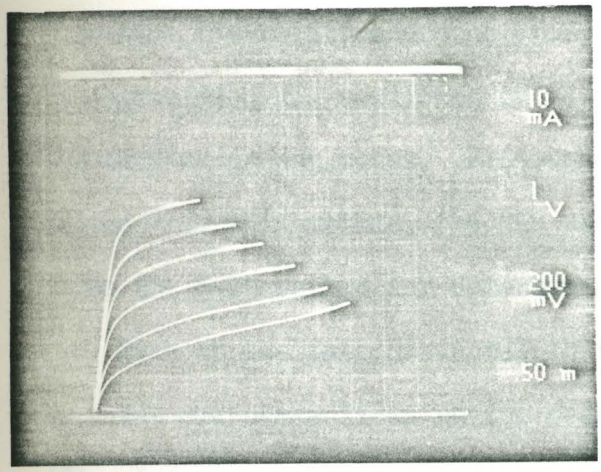
The initial shipment consisted of one chip each from NEC, Mitsubishi, and Avantek and a number of chips from Hughes, Malibu. One of the Malibu chips was received mounted in a microstrip circuit which facilitated probing and handling. In addition, the mounted chip appeared to be stable electrically whereas the unmounted chips showed signs of instability. Preliminary investigations on the mounted chip indicated that some of the basic FET parameters could be calculated from measured d.c. characteristics. This required the chip to be completely stable under a broad range of biasing conditions.

A second shipment of Malibu chips, each mounted in a microstrip circuit were sent for further testing. Each chip appeared to be stable and to be similar electrically to that of the initial Malibu chip. The current voltage characteristics of the chips from the second shipment are shown in Figure 1. A third shipment consisting of two chips from each manufacturer, each mounted in an actual circuit,was subsequently received. Unfortunately, the chips from three manufacturers (including those from Malibu) proved to be unstable. Typical current voltage characteristics showing these instabilities for selected devices are shown in Figure 2.

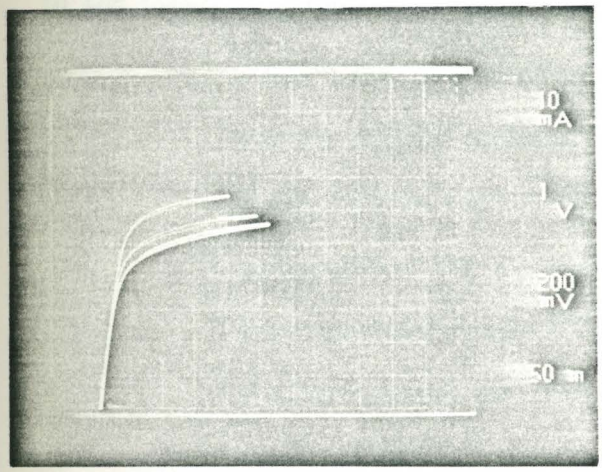
An inordinate amount of time was spent in obtaining the I-V characteristics of each device. These data were considered important since, in addition to being one of the primary tasks, it was to be used in calculating effective values for the doping density and the thickness of the active layer. It was



a. Malibu A-1

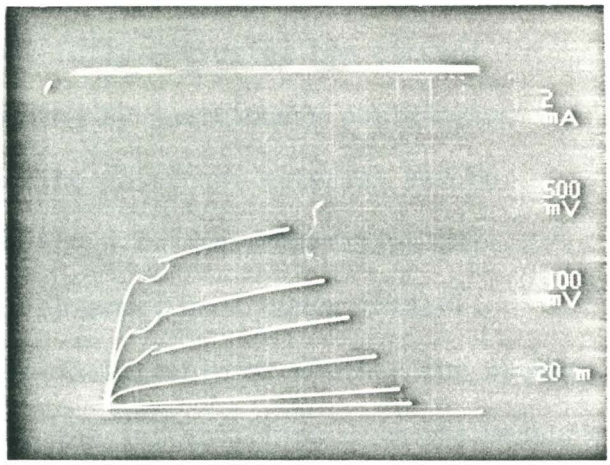


b. Malibu A-2

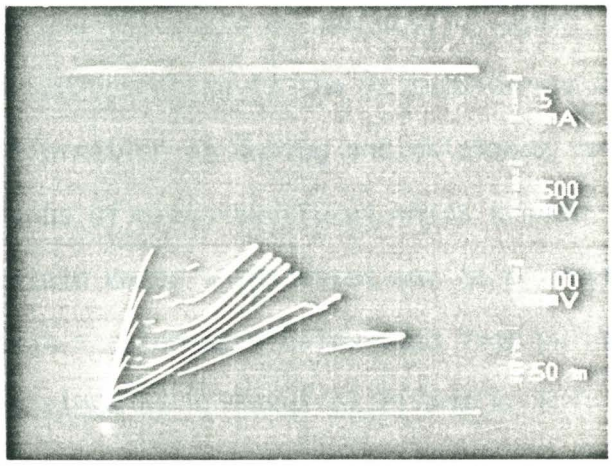


c. Malibu A-3

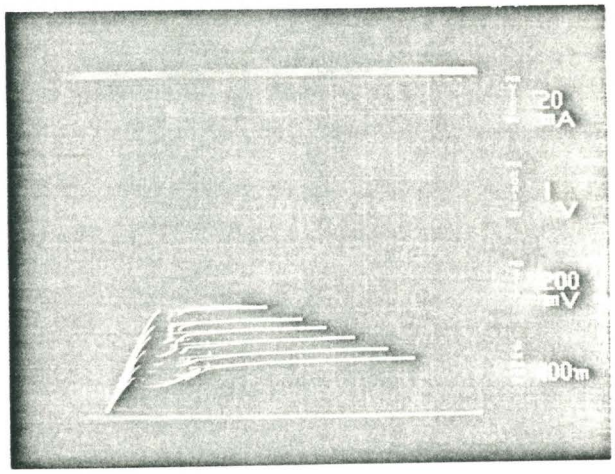
Figure 1. Malibu Chips,
Second Shipment



a. Malibu B-2



b. NEC-2



c. Avantek -2

Figure 2. Selected Chips,
Third Shipment

therefore imperative that stable characteristics be measured. Relatively stable I-V curves were finally obtained by fully enclosing the circuit mounted FETs in a block of absorbant foam and by judiciously positioning the probes along the microstrip circuit. The absorbant material had no noticable effect on the stable regions of the d.c. characteristics but largely eliminated the instabilities when observed on a curve tracer. The question of whether the circuit was in fact stable or whether the probes were just placed in a position to decouple the instabilities from the measuring equipment was not fully resolved.

Another task which received considerable attention was an attempt to determine the relative doping profile and the thickness of the active layer by observing cross-sectioned chips on an SEM operating in the voltage-contrast and sample-current modes. Although no information on doping and thickness resulted from this method, the SEM photographs of cross-sectioned chips proved to be the best method for determining certain metal thicknesses and gate lengths.

Much of the data presented in the next section were calculated from point-by-point measurements using the model described by H. Fukui [1,2] and R. Fair [3]. The equations used to calculate the various parameters are indicated in the comment column of Table II by (equation) [reference].

NOTATION

I_s	open-channel saturation current
I_d	drain current
I_m	maximum channel current
I_o	zero-gate-bias channel current
I_{dss}	zero-gate-bias drain current
I_f	maximum forward-gate-bias drain current
I_{pf}	drain current at $V_{ds} = V_{kf}$ and $V_{gs} = -V_p$
I_{do}	zero-gate-bias drain current at $V_{ds} = V_{ko}$
I_{po}	drain current at $V_{ds} = V_{ko}$ and $V_{gs} = -V_p$
V_{kf}	knee voltage for $V_{gs} = V_f$
V_{ko}	knee voltage for $V_{gs} = 0$
V_{ds}	drain-source bias voltage
V_{gs}	gate-source bias voltage
V_f	maximum forward gate bias voltage
V_p	extermal gate pinch-off voltage
V_b	gate built-in voltage
W_p	total gate pinch-off voltage
R_s	source series resistance
R_d	drain series resistance
R_{gs}	gate-source series resistance
N	free carrier concentration
a	active channel thickness
L_g	gate length

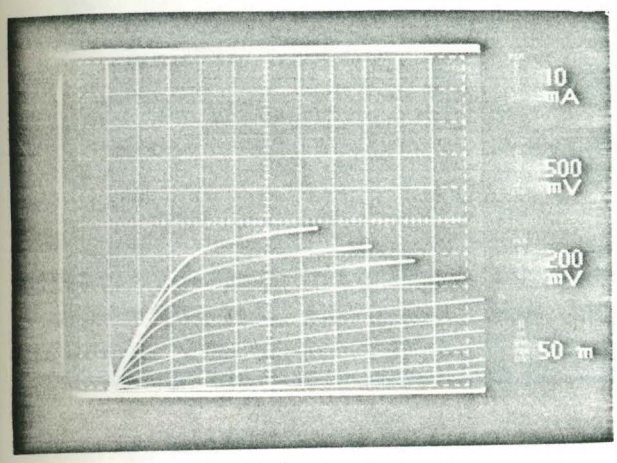
L_S	source-gate center length
L_D	drain-gate center length
Z	total device width
σ	normalized effective zero-gate-bias parameter
δ	normalized source parasitic parameter
β	maximum channel opening factor
γ	zero-gate-bias channel opening factor
η	ideality factor
μ_o	low-field mobility
g_m'	inherent small-signal transconductance
g_m	measured small-signal transconductance

Summary of Results

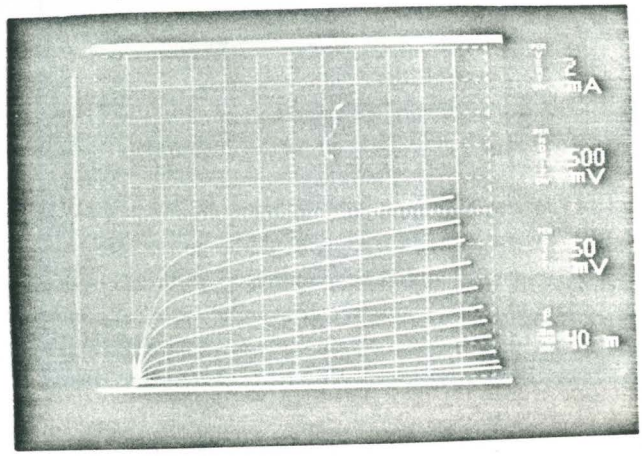
Photographs of the I-V characteristics of the various chips after stabilization are shown in Figure 3. The first two photographs illustrate the electrical differences between the Malibu chips of the first two shipments (similar) and those of the third shipment. Note that the saturated drain current differs by a factor of about 5. Since other significant differences were noted during these investigations, chips from the second and third shipments (designated Malibu-A and Malibu-B, respectively) were included in the analysis.

Most of the measured and calculated parameters for the five devices are listed in Tables I and II. Various physical parameters such as source-gate center length, drain-gate center length, gate length, and gate width were obtained from the optical and SEM photographs of Appendix A. Some of the electrical data were taken from the curve tracer photographs of Figures 3 and 4. Many of the calculated parameters were obtained by plotting and analyzing several sets of d.c. data following the technique of Fukui [1]. Most of this data were taken point-by-point using digital meters in conjunction with the curve tracer.

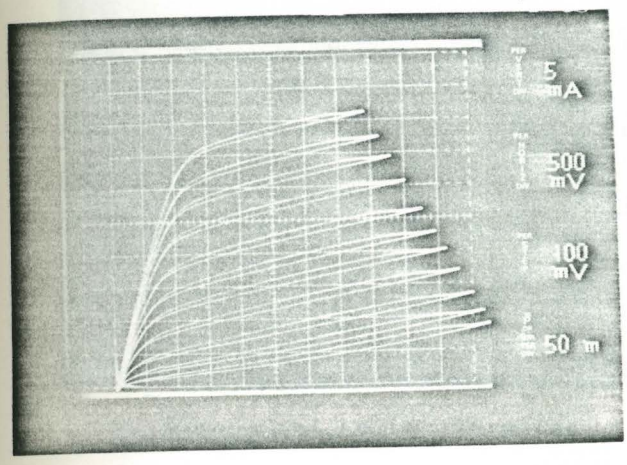
The ideality factor, built-in voltage, and R_{gs} were calculated from the forward I-V characteristics of the gate. The source-drain series resistance and the external gate pinch-off voltage were determined by plotting drain current vs gate voltage at a fixed drain bias of 50 mV. Doping density and active layer thickness were determined by assuming an effective gate length equal to the measured gate length. Intolerable errors occur when calculating an effective gate length for devices with short gate lengths and low pinch-off voltages from measured data. As stated previously, an inordinate amount



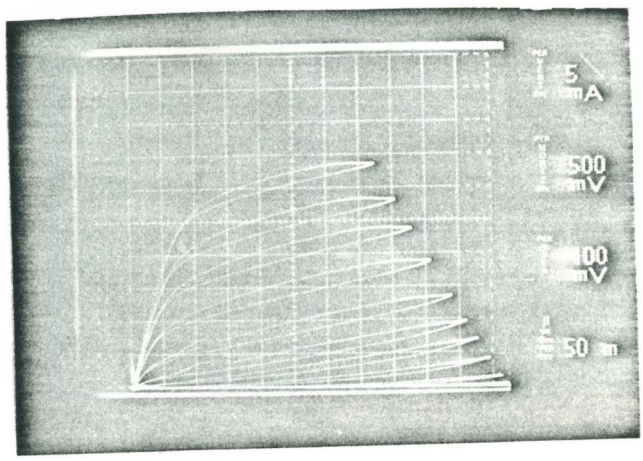
a. Malibu -A



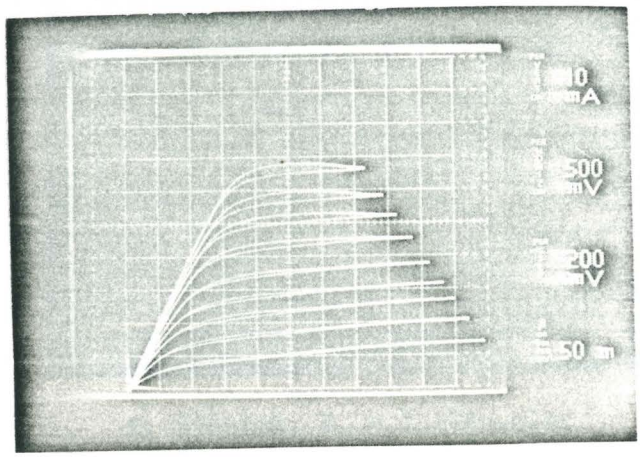
b. Malibu -B



c. Mitsubishi

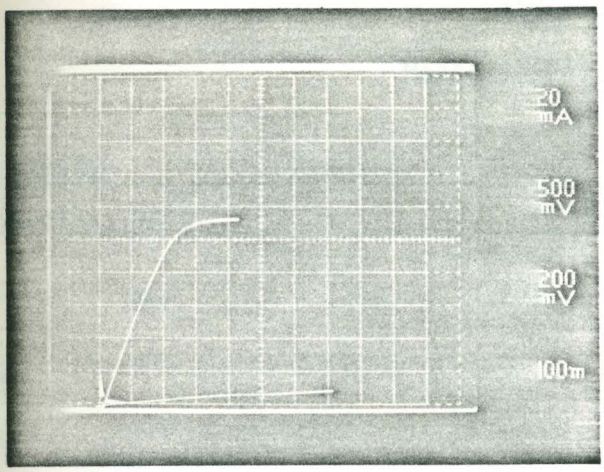


d. NEC

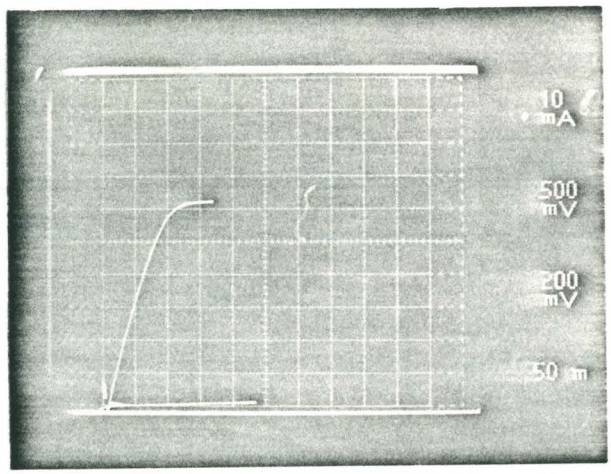


e. Avantek

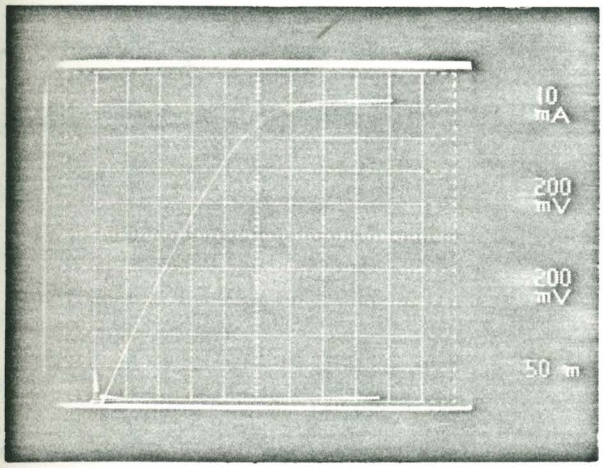
Figure 3. I-V Characteristics with zero offset.



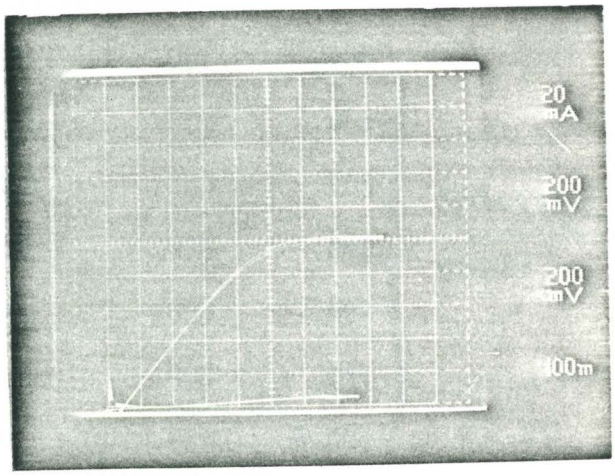
a. Malibu -A, V_f - 1.14 volta



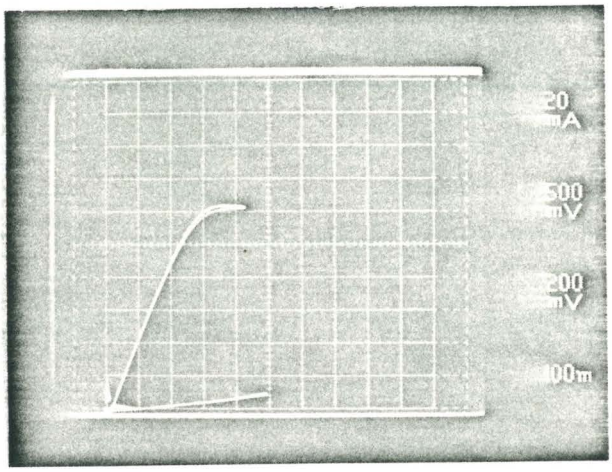
b. Malibu -B, V_f = .99



c. Mitsubishi, V_f = .99 volts



d. NEC, V_f = 1.111



e. Avantek, V_f = 1.114 volts

Figure 4. I-V Characteristics with positive offset.

TABLE I

Measured Parameters

Parameter Symbol	Unit	Avantek	NEC	Mitsub.	MAL-B	MAL-A	Comments
		Measured Parameters					
Z	mm	.250	.275	.300	.300	.300	From optical & SEM photographs
L_g	μ	.5	.5	.7	.6	.5	
L_s	μ	1.6	2.2	1.6	1.7	1.7	
L_d	μ	1.6	.8	3.2	1.5	1.5	
V_f	V	1.14	1.11	.99	.99	1.14	
I_f	A	.122	.101	.091	.061	.108	From Curve Tracer Photographs
I_{pf}	A	.002	.001	.001	.001	.003	
I_m	A	.120	.100	.090	.060	.105	
I_{do}	A	.062	.025	.035	.008	.043	
I_{po}	A	.001	.000	.000	.000	.002	
I_o	A	.061	.025	.035	.008	.041	
V_{kf}	V	1.00	.70	.75	.65	1.00	
$g_{m,sat}$	℧	.042	.066	.043	.029	.038	Point-by-point at V_{ds} = 3V
I_{dss}	A	.064	.033	.039	.009	.049	

TABLE II

Calculated Parameters

Parameter Symbol	Unit	Avantek	NEC	Mitsub.	MAL-B	MAL-A	Comments
		Calculated Parameters					
η	-	1.21	1.34	1.18	1.19	1.14	(30)[1]
V_b	V	.642	.648	.718	.681	.693	(27)[1]
V_p	V	1.968	.475	1.041	.312	1.290	Obtained by plotting data
R_s+R_D	Ω	6.2	5.6	6.2	7.7	8.0	
R_s	Ω	3.1	3.6	2.0	4.0	4.1	
R_D	Ω	3.1	2.0	4.2	3.7	3.9	
R_{gs}	Ω	6.	6.	5.	8.	8.	
β	-	.775	.667	.684	.619	.744	(8,11)[2]
I_s	A	.155	.150	.132	.097	.140	(5)[1]
N	$10^{17}cm^{-3}$	2.1	3.8	1.6	1.5	1.6	(19)[1]
a	μ	.130	.064	.124	.095	.130	(20)[1]
δ	-	.291	.681	.498	.826	.408	(10)[1]
σ	-	.092	.274	.079	.196	.150	(11)[1]
γ	-	.396	.165	.265	.075	.250	(12)[1]
I_o	A	.061	.025	.035	.007	.041	(8)[1]
V_{kf}	V	.996	.690	.739	.613	.994	(14)[1]
V_f	V	1.08	1.09	.97	1.01	1.19	(9)[2]
g_m', sat	$\mho$	.049	.079	.049	.033	.051	(14)[3]
g_m, sat	$\mho$	.042	.063	.043	.029	.042	(33)[1]
g_m,(.030)	$\mho$	.033	.065	.044	.055	.038	(35,33)[1]
g_m,(.040)	$\mho$	.036	.069	.047	.063	.041	(35,33)[1]
g_m,(I_{dss})	$\mho$	.044	.066	.047	-	.044	(35,33)[1]

* These values were calculated assuming $E_c = .29 \times 10^4$ v/cm, $v_s = 1.4 \times 10^7$ cm/sec, and $V_c = 0$.

of time was spent in interpreting data and in correlating it with FET models. The best agreement between measured values and calculated values using Fukui's model was obtained with the set of parameters listed in Table II. In this sense, the parameters listed are considered the most probable values.

An attempt was made to determine the doping profile of the active layer from C-V data by the conventional technique. This technique requires that the effective gate area be accurately known and that the capacitance data be corrected for fringing and other parasitic effects. Unfortunately, these effects are more important and become more difficult to determine for short gate devices. Figure 5 shows the results of reducing the C-V data to a doping density and depletion width using an effective area of 3.76×10^{-6} cm^{-2}. This is more than twice the nominal LZ product. Even if correction factors were applied, the conventional technique would not provide profile information within the zero-bias depletion region. For short-gate and low pinch-off devices, this region occupies a significant portion of the active region. When correlated with other measurements, however, the technique would provide relative doping information in the region close to the buffer layer.

Another difference between the two types of Malibu FETs had to do with the source and drain contacts. Figure 2A of the Appendix shows this difference. Note that the material under the source and drain pads for the Malibu-B and NEC FETs has a highly granular appearance while the material for the Malibu-A, Mitsubishi, and Avantek FETs has a more uniform appearance. The granular or spongy appearance suggests a bi-element alloy contact, probably Ge-Au, where one element has alloyed into the GaAs. Energy dispersive analysis, however, could not detect the primary alloying element. The differences in appearances could, therefore, be due to different alloy time, temperature, or even material. One exception was the Mitsubishi FET where a high concentration Si was detected in the vicinity of the contacts. This FET may have

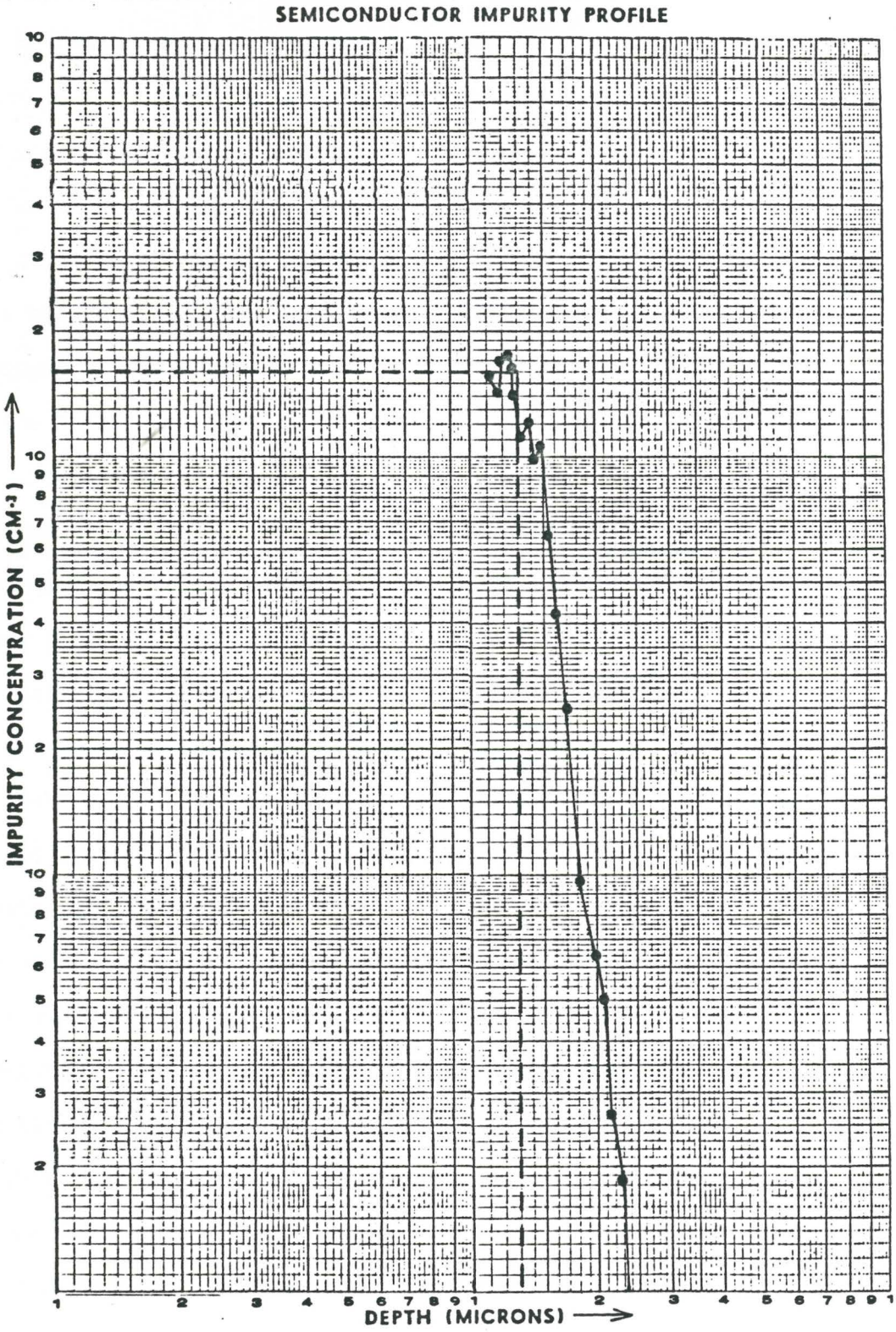


Figure 5. Doping density profile of Malibu-A FET derived from C-V data.

a silicon doped N^+ layer grown over the active layer. Both layers appear to have been etched away outside a parameter surrounding the source and drain. In the region between the source and drain a channel was etched into the active layer where an aluminum channel was deposited.

Cross sectional sketches of each FET showing certain dimensions which effect operation are depected in Figure 6. In each case, the gates are recessed a significant amount into relatively thick active layers. Although no accurate method of determining the total thickness of the active layer could be found, it was estimated from the depth of recess (measured from SEMs) and the fully open channel thickness (calculated) to be between .4 - .5 microns except for the Avantek FET.

The gates of the Malibu and Avantek chips were approximately centered between the gate and source contacts. The gates (4) for the Mitsubishi FET was considerable closer to the source contact. This was probably not due to miss alignment problems which, because of the geometry, would have resulted in some of the gates being closer to the sources and others being closer to the drains. The gate for the NEC FET, however, practically lay alongside the drain contact which perhaps was due to miss alignment.

The metal thicknesses shown in the sketches are only approximate. There were some discrepancy between different SEM photographs taken on the same device in essentially the same region. The thicknesses of the Ni, Ti, W, Pt layers could not be determined accurately and were, therefore, not assigned a value.

The calculated values of active layer doping for the Avantek, Mitsubishi and Malibu devices were in the 1.5×10^{17} cm^{-3} to 2.1×10^{17} cm^{-3} range with active layer thicknesses varying from .096 microns to .130 microns. In

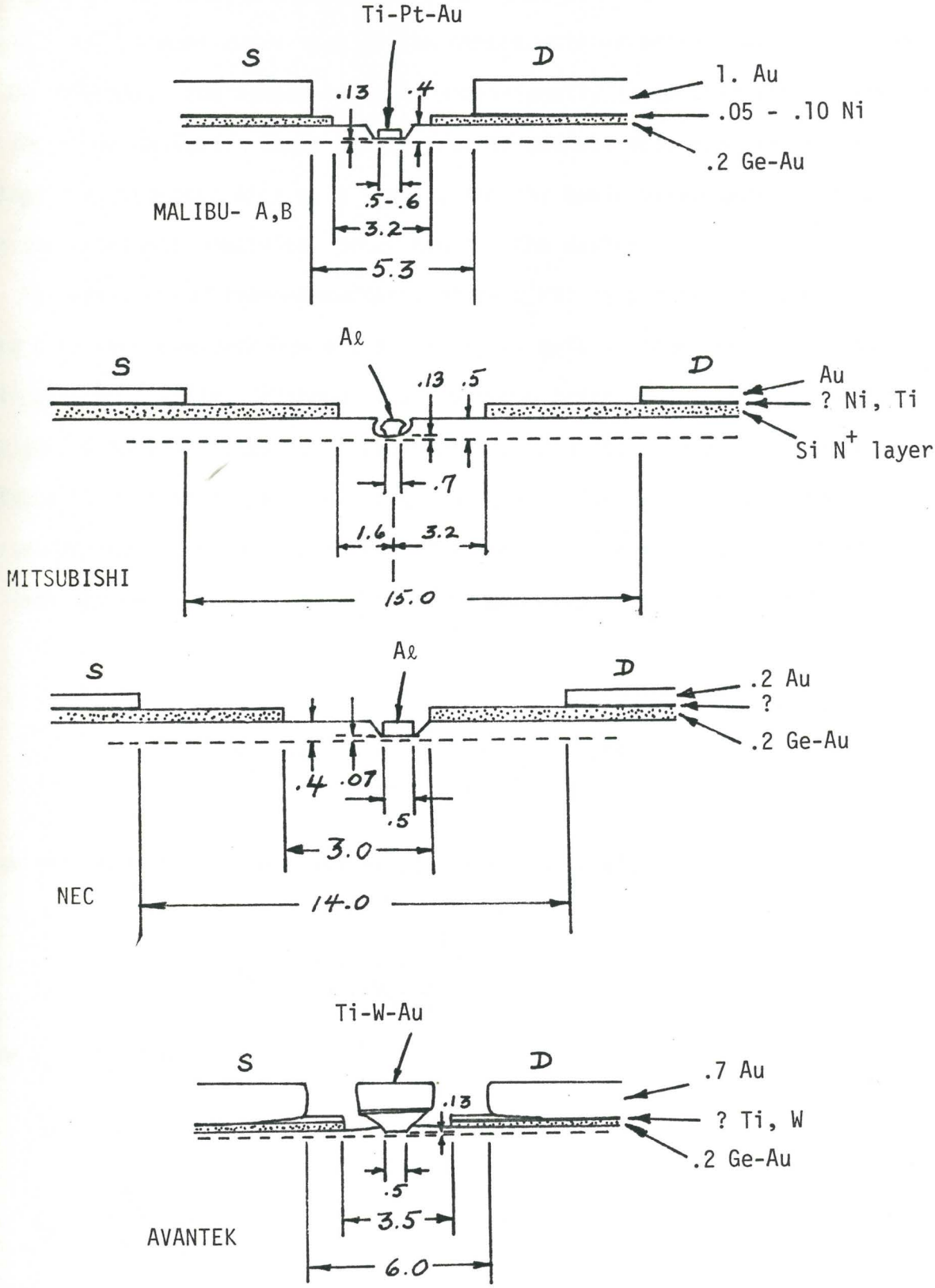


Figure 6. Cross Sectional View of FETs.

contrast, the calculated active layer doping of the NEC device was close to 4×10^{17} cm^{-3}, almost twice that of the others, with an active layer thickness of .064 microns. The latter value is significantly lower than the thicknesses for the other devices. These parameters, of course, determine the pinch-off voltage and, together with gate length, are the basic parameters which determine the intrinsic electrical properties of the device.

The small-signal transconductance of each FET is plotted in Figure 7. These data were measured from drain current vs gate voltage for the constant drain bias of 3 volts. Although the I-V curve tracer photographs showed no signs of instabilities for a drain bias of 3 volts, there is evidence of instabilities in the data plotted, especially for the Malibu-A and Avantek devices. Calculated values of transconductance are also plotted for each device. The values indicated by ●——● were calculated from

$$g_m', (I_d) = \frac{I_s}{2W_p \left(1 - \frac{I_d}{I_s}\right)} \quad \text{and}$$

those indicated by the darkened symbols were calculated by

$$g_m', \text{sat} = \frac{I_{dss}}{2W_p \, \eta_s^{1/2}(1 - \eta_s^{1/2})}$$

where $W_p = V_p + V_b$,

$\eta_s = V_b/W_p$, and

$$g_m = \frac{g_m'}{1 + R_s g_m'} .$$

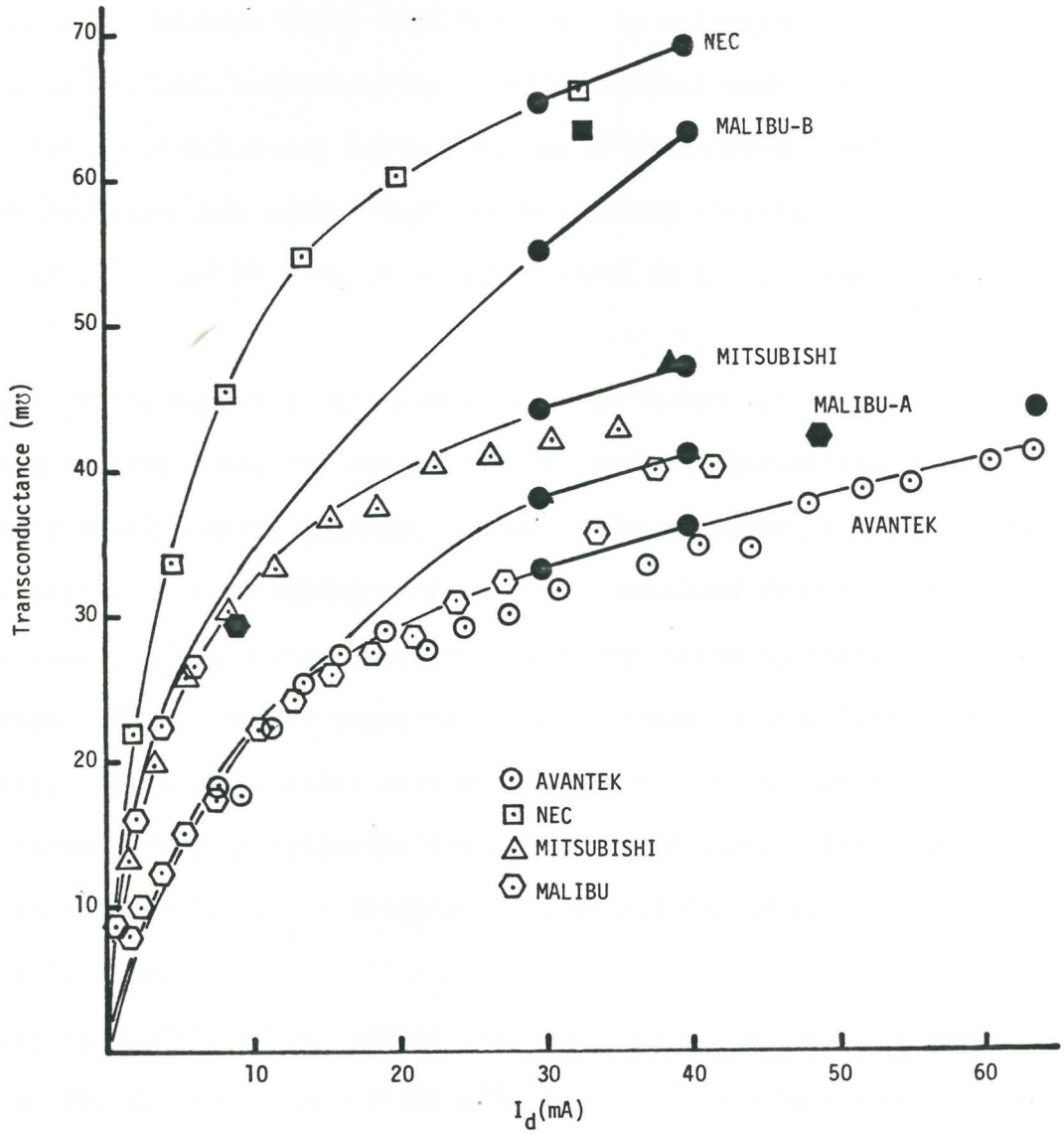


Figure 7. Measured and Calculated small-signal transconductance at V_{ds} = 3 Volts. Darkened symbols are calculated values.

CONCLUSIONS AND RECOMMENDATIONS

The analysis of processed state-of-the-art microwave FETs proved to be an interesting but formidable task. These devices are more likely to oscillate than lower frequency, less sophisticated FETs and special efforts had to be made to suppress these oscillations. In retrospect, it is felt that more accurate data would have resulted if contact pads placed on non-conductive (at d.c.) but lossy (absorbant at RF frequencies) material such as Eccosorb had been used rather than the microstrip circuit. Using the conductors of an actual RF circuit probably added to the problems of instability.

Because of the numerous parameters involved in FET operation, both physical and material, and the intractability of these parameters from non-uniformly doped models, it seems unlikely that accurate, detailed structural information such as doping profile can be resolved from d.c. measurements unless many of the other parameters are determined beforehand by other methods. This prompted the efforts to determine active layer thickness by using the sample-current contrast capability of the SEM with only limited results. Profile determination by the conventional technique, also, proved inaccurate due to fringing effects and the uncertainty in effective gate area.

The doping profile in the active layer, of course, effects the linearity of the device. Some of the efforts on this analysis suggest that the actual doping profile of a FET can be determined more accurately during device development. This will allow large area test gates to be formed at selected spots on the wafer during FET processing for profile evaluation.

It is always satisfying to obtain good correlation between measured device parameters and measured performance. Gain and noise figure data accompanied the third shipment of FETs consisting of two chips, #1 and #2, from each manufacturer mounted in a microwave circuit. Attempts to correlate that data with theoretical expectations based on the parameters of this analysis met with mixed results.

The data analyzed in this report were taken on chip #2 of each manufacturer. The measured noise figure for the circuits containing these chips were all essentially 3.4 db except for the one containing the NEC chip which was 2.17 db. The measured basic FET parameters of this chip were significantly different from the others, i.e., the doping density and thickness of the active layer for this device were about 4.0×10^{17} cm^{-3} and .06 microns, respectively, while those for the other FETs were between $1.5 - 2.0 \times 10^{17}$ cm^{-3} and .10 - .13 microns. The FET also had a significantly larger small-signal transconductance value at its saturation current than the others. On the other hand, both circuits containing the Mitsubishi chip gave noise figures below the average of the sample yet SEM photographs indicated it had the longest gate length.

These attempts to correlate parameters to performance, however, are based on a small sample and, therefore, subject to unknown errors. The noise figure data supplied show little statistical differences among the devices. The circuit containing NEC #1 and NEC #2, for example, gave noise figures of 2.62 dB and 2.17 dB, respectively. The noise figures of all other circuits except that containing Avantek #1 (2.73 db) fell within the range. This raises several questions. Are these noise figure differences due to differences in test conditions or are they due to actual differences in device parameters? If the latter, how uniform are the chips of a particular

manufacturer. Since only one chip from each manufacturer was analyzed, are the parameters obtained typical of that type device?

REFERENCES

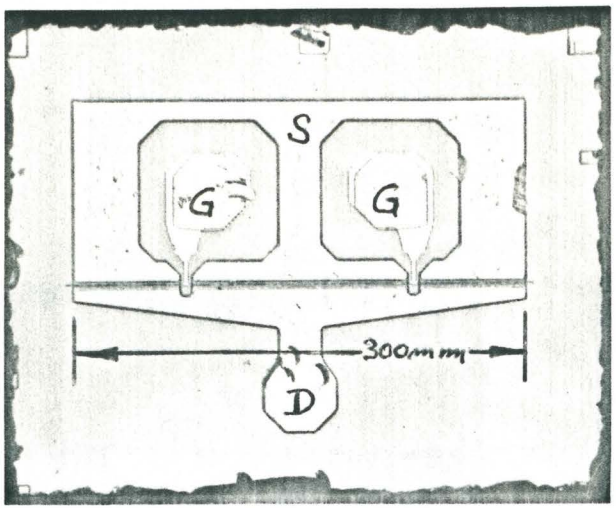
1. H. Fukui, "Determination of the Basic Device Parameters of a GaAs MESFET," The Bell System Technical Journal, Vol. 58, No. 3, pp. 771-797, March 1979.

2. H. Fukui, "Channel Current Limitations in GaAs MESFETs," Solid State Electronics, Vol. 22, pp. 507-515, 1979.

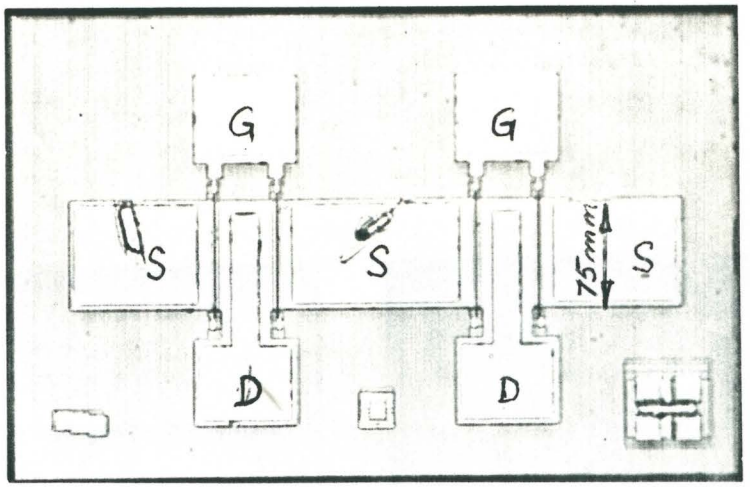
3. R. B. Fair, "Graphical Design and Iterative Analysis of the D.C. Parameters of GaAs FET's," IEEE Transactions on Electron Devices, Vol. ED-21, No. 6, pp. 357-362, June 1974.

APPENDIX A

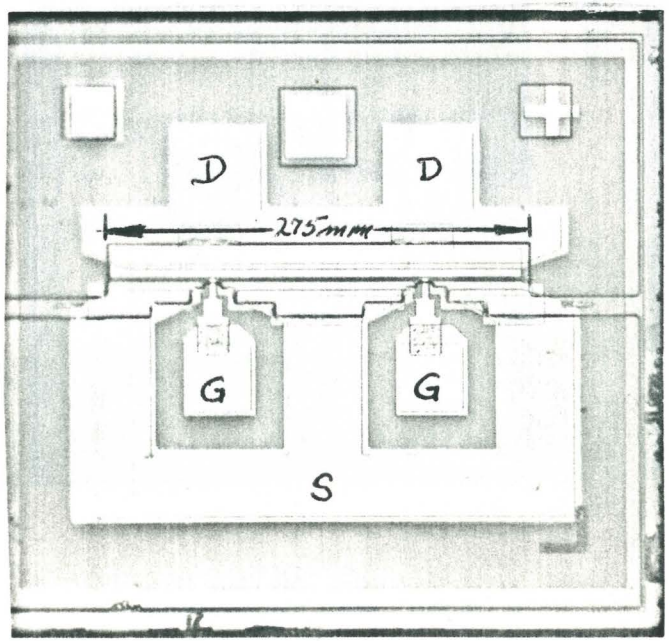
Optical And SEM Photographs And Energy Dispersive X-Ray Data



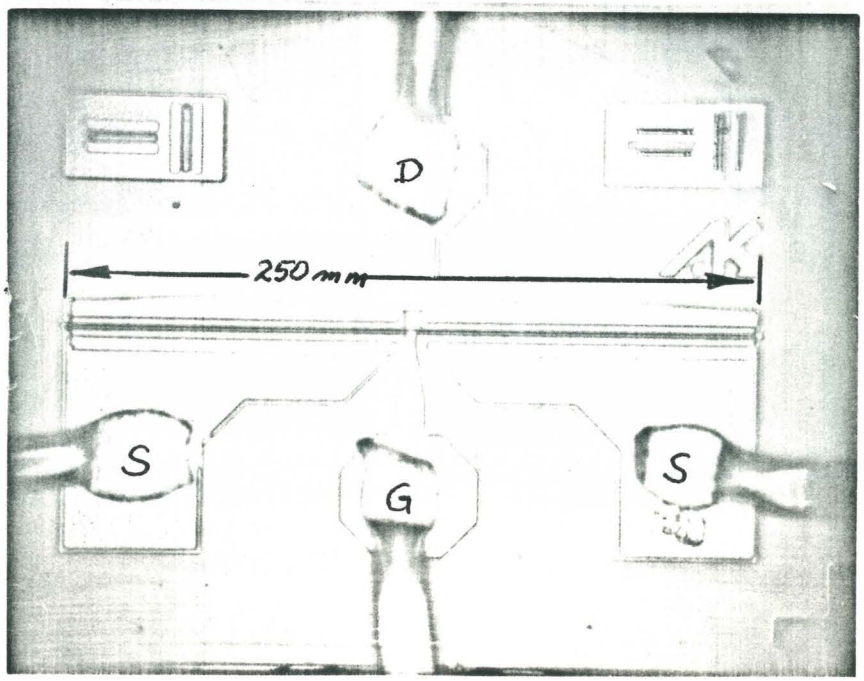
a. Malibu - A,B



b. Mitsubishi

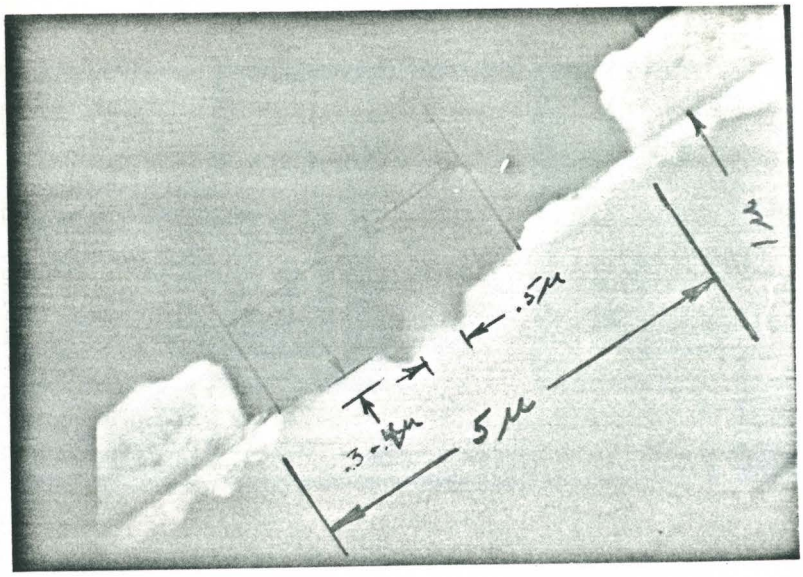


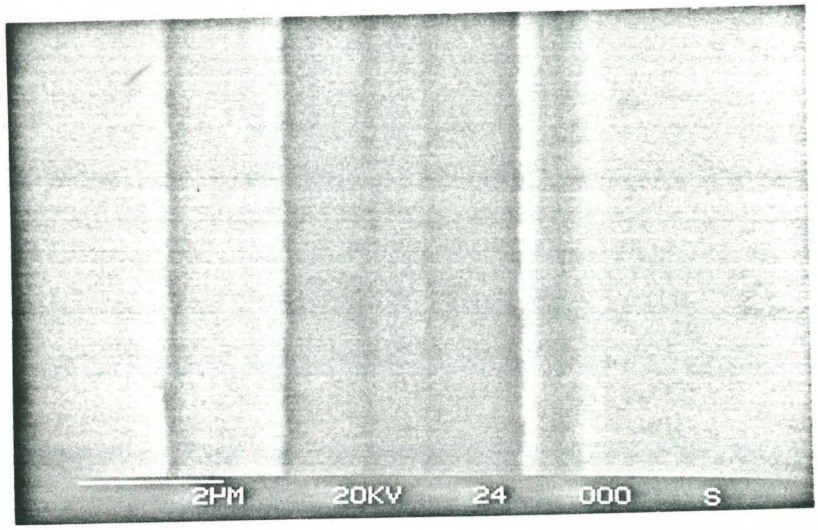
c. NEC



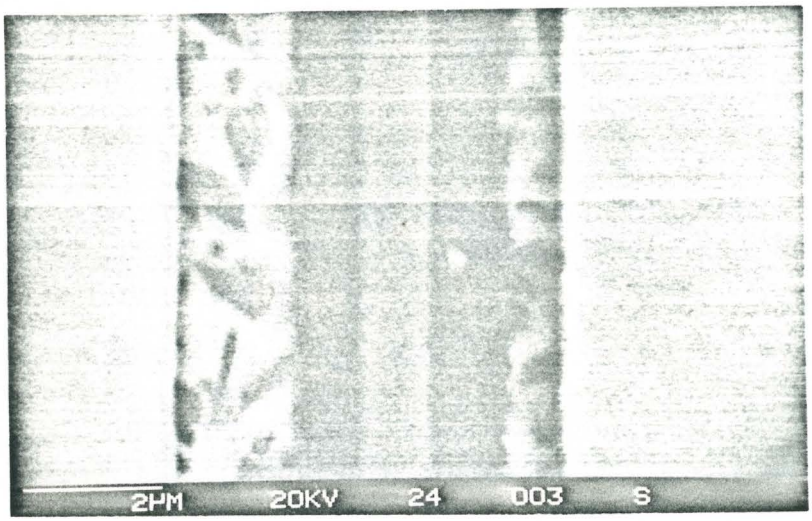
d. Avantek

Figure 1A. Microphotographs of Chips.





Malibu-A



Malibu-B

Figure 2A. SEM Photographs of Malibu Chips.

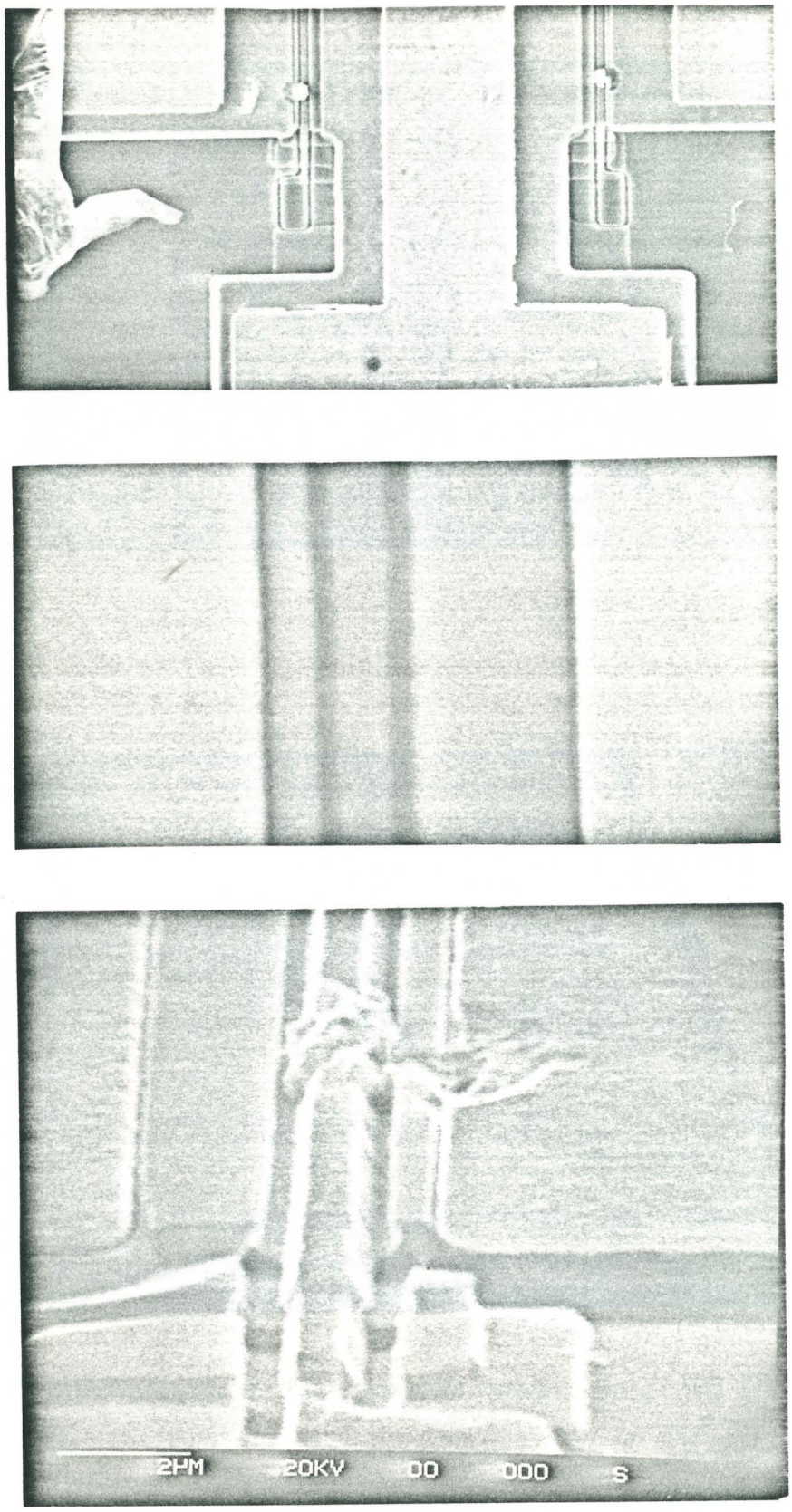
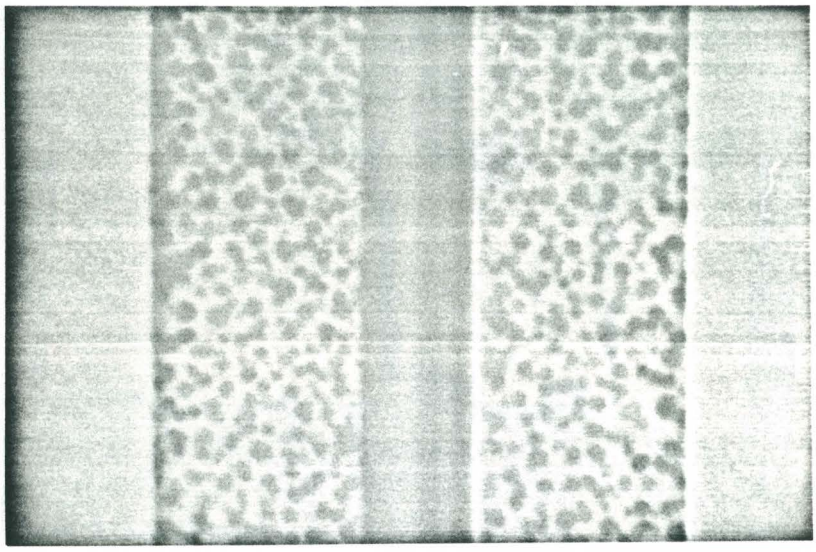


Figure 3A. SEM Photographs of Mitsubishi Chips.



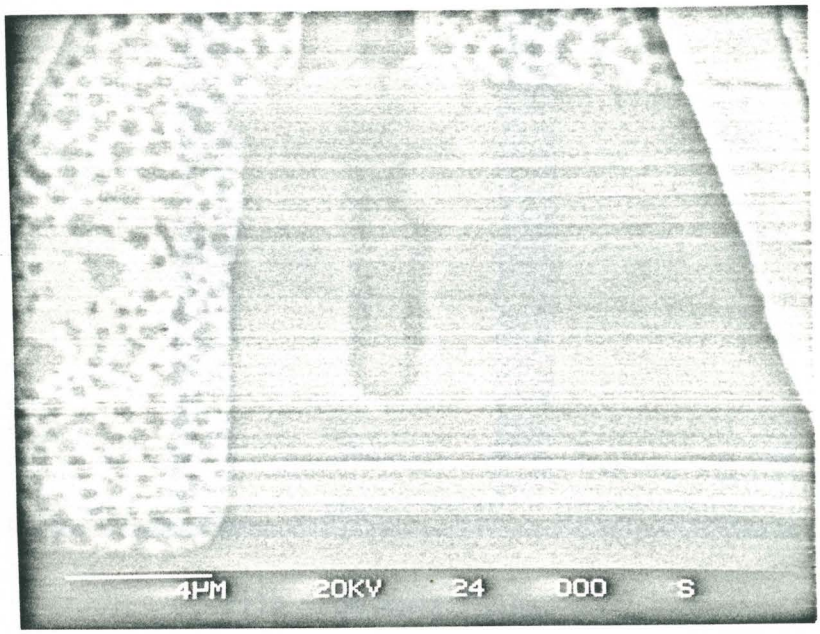
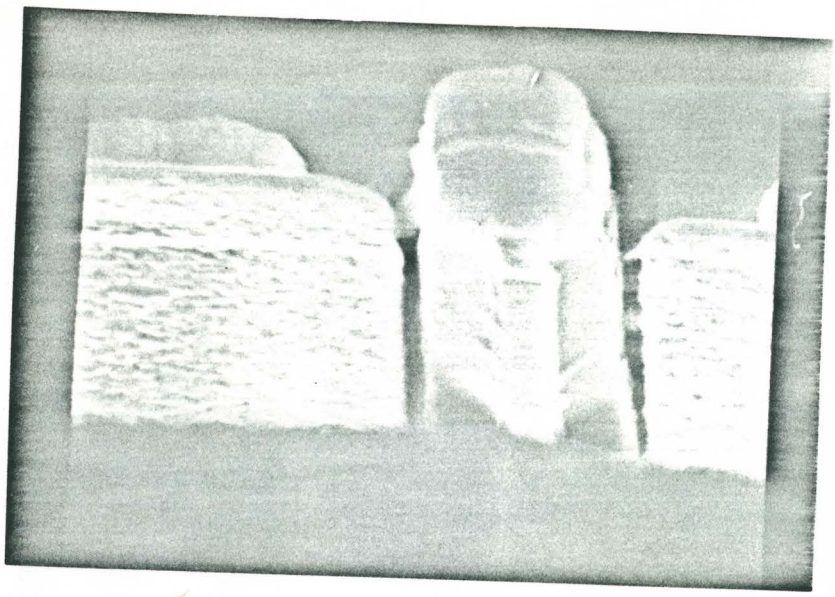
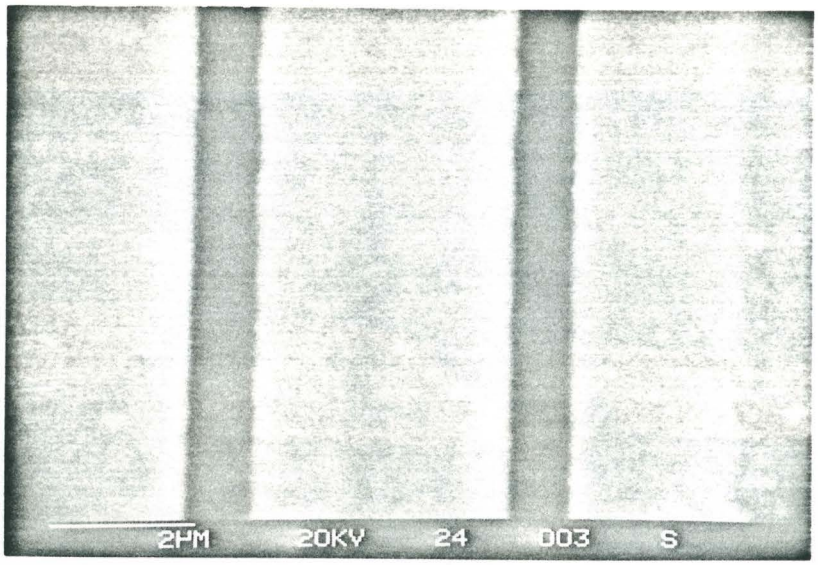


Figure 4A. SEM Photographs of NEC Chip.

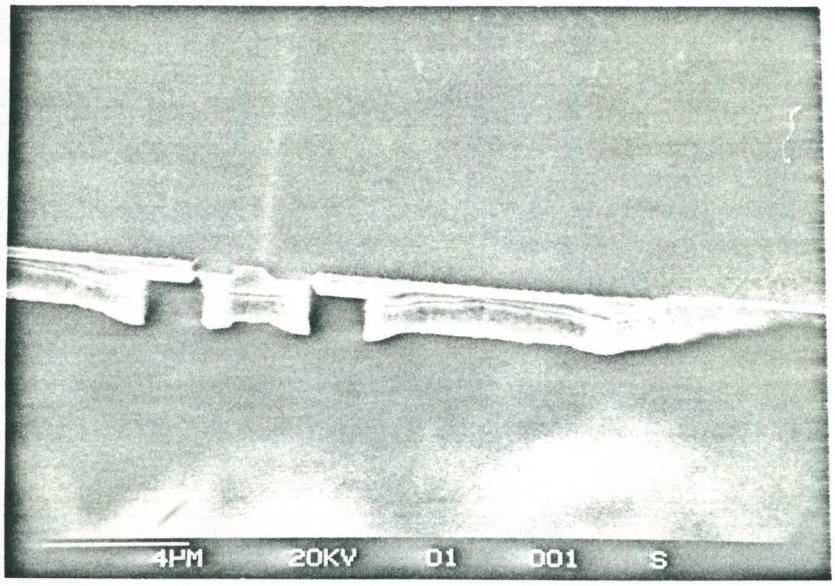


Etched chip, 45° tilt from
semiconductor side.



0° tilt from metal side.

Figure 5A. SEM Photograph of Avantek Chip.



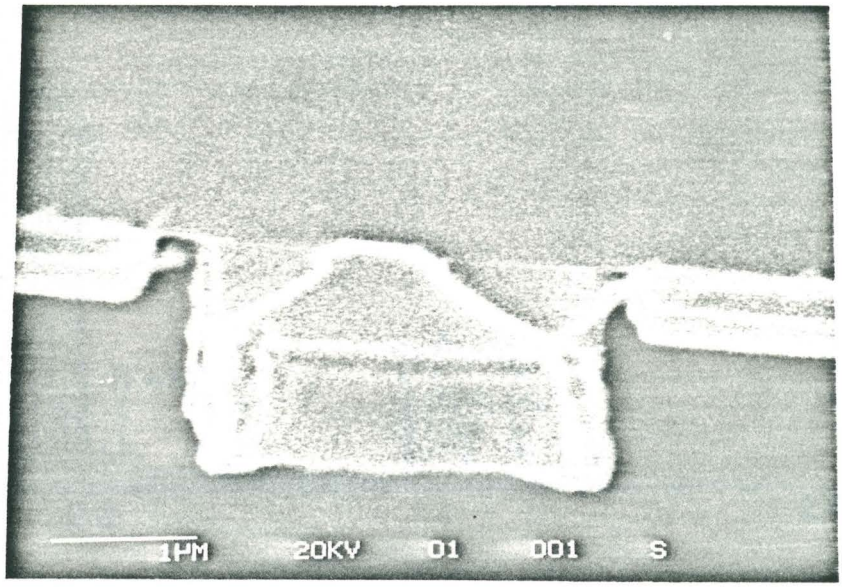
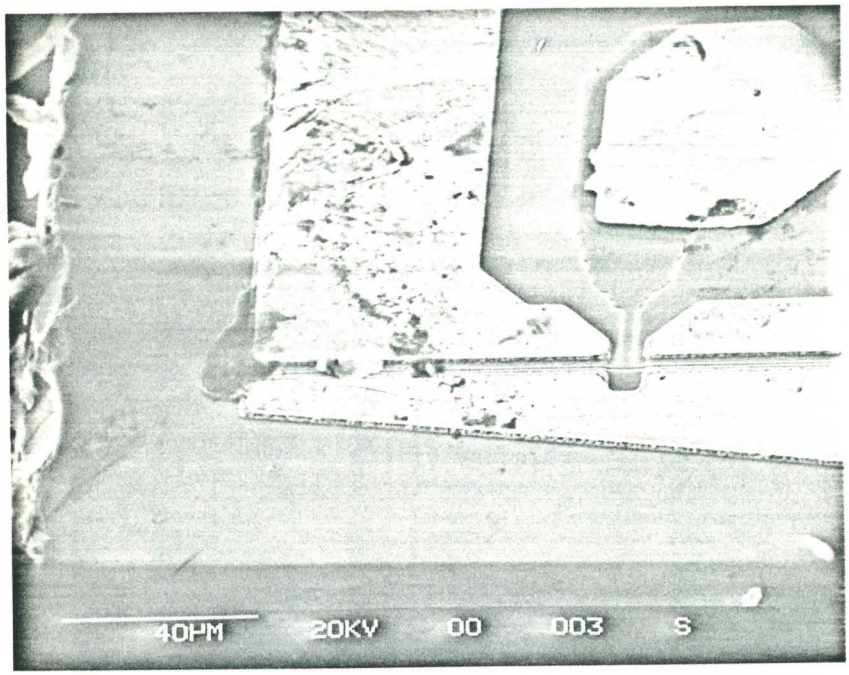


Figure 6A. Cross-section (90° tilt) of Avantek Chip.



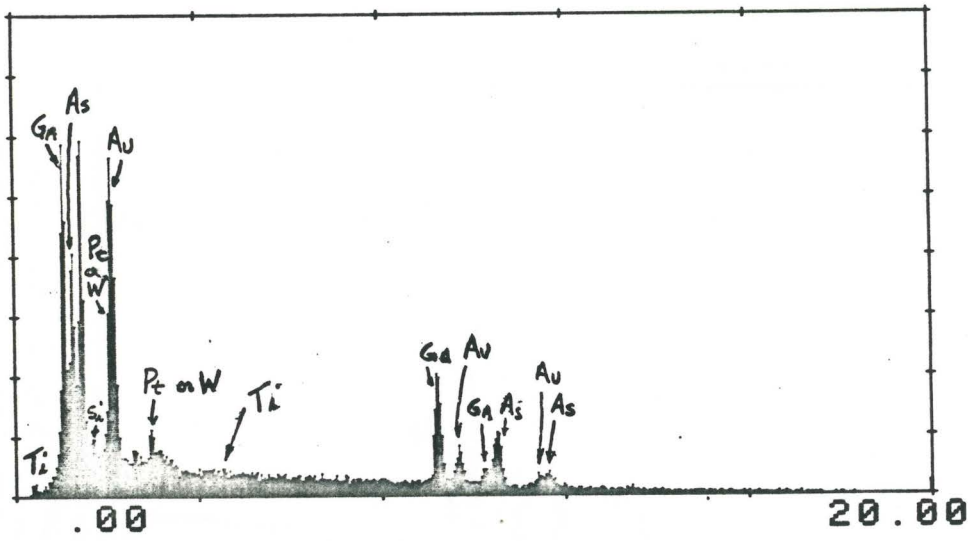
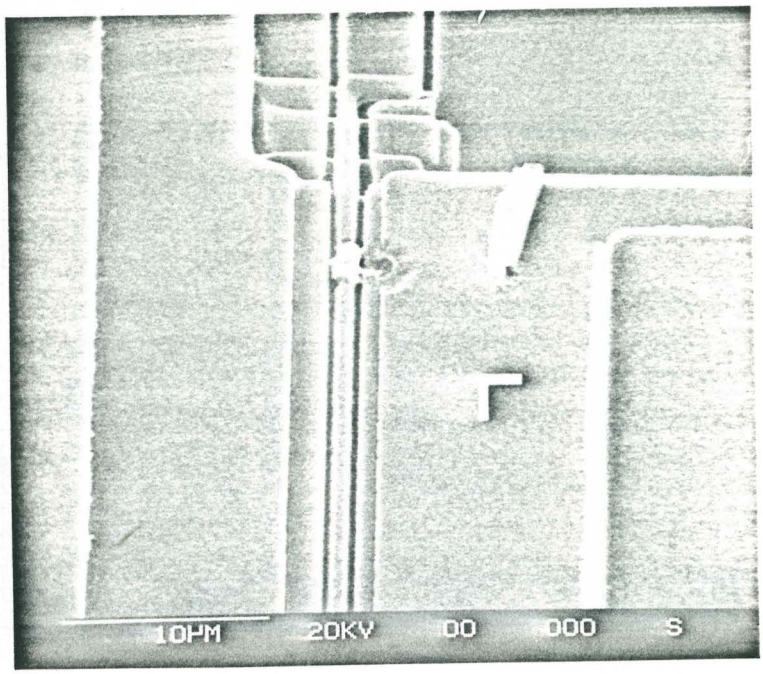


Figure 7A. Energy Dispersive Analysis of Malibu FET in the Vacinity of Gate Region.



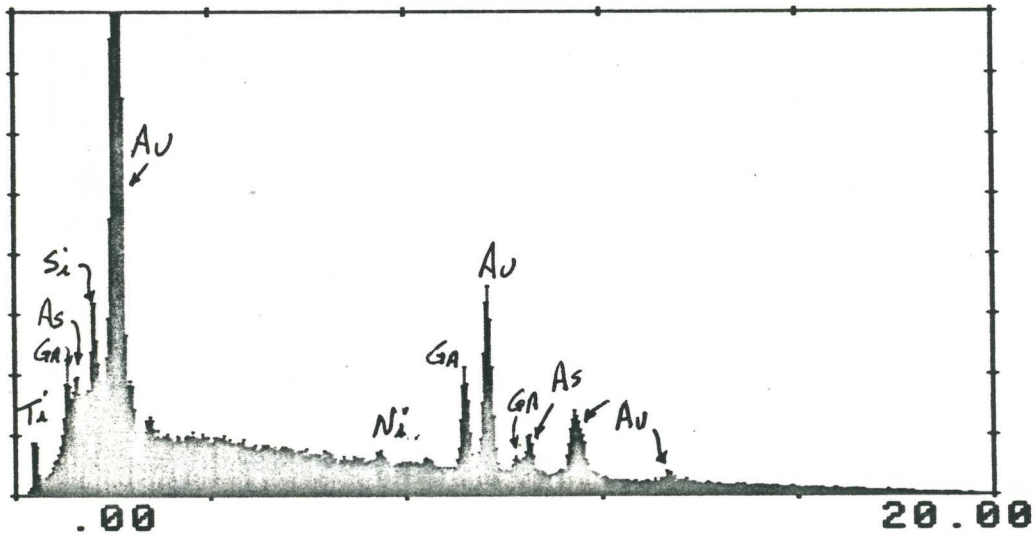
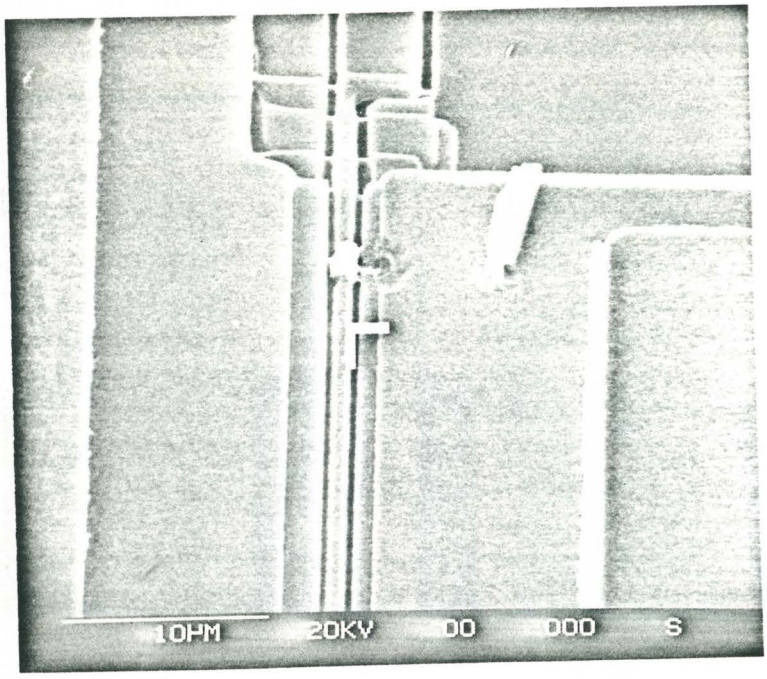


Figure 8A. Energy Dispersive Analysis of Mitsubishi FET at Region Indicated.



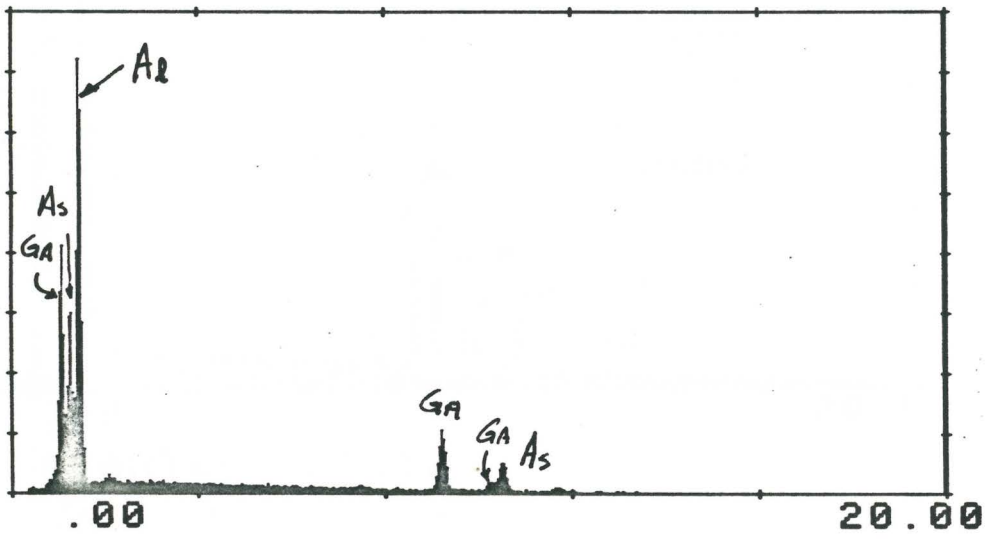
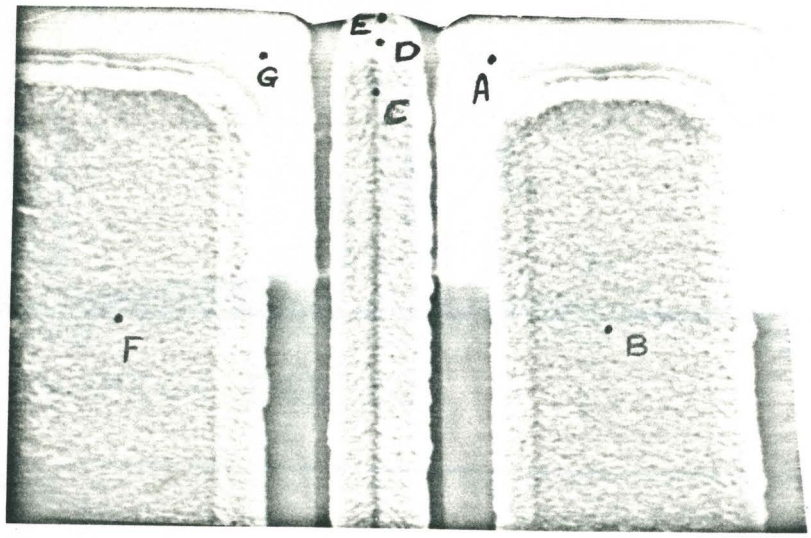


Figure 8A. Continued



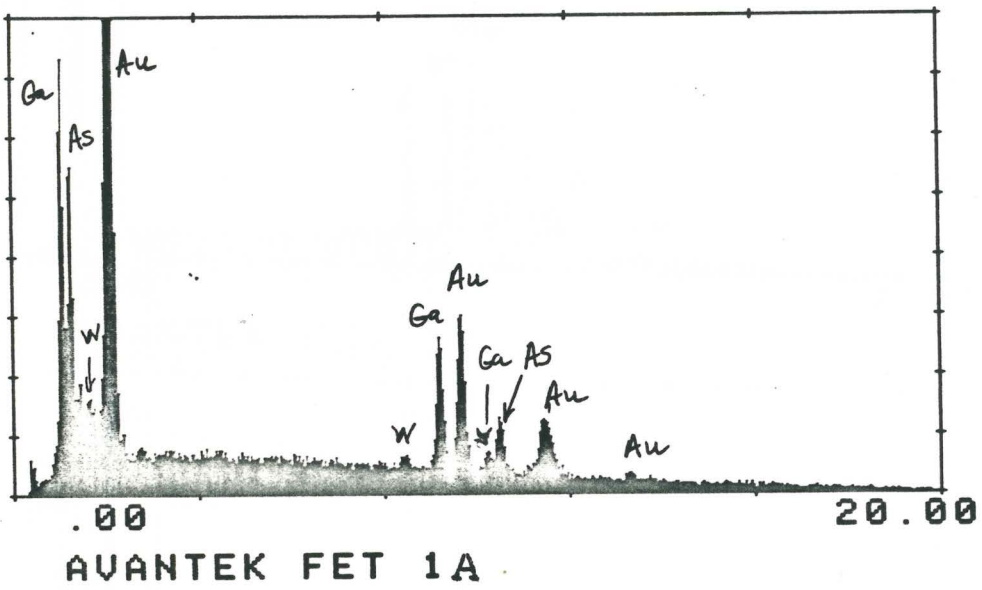
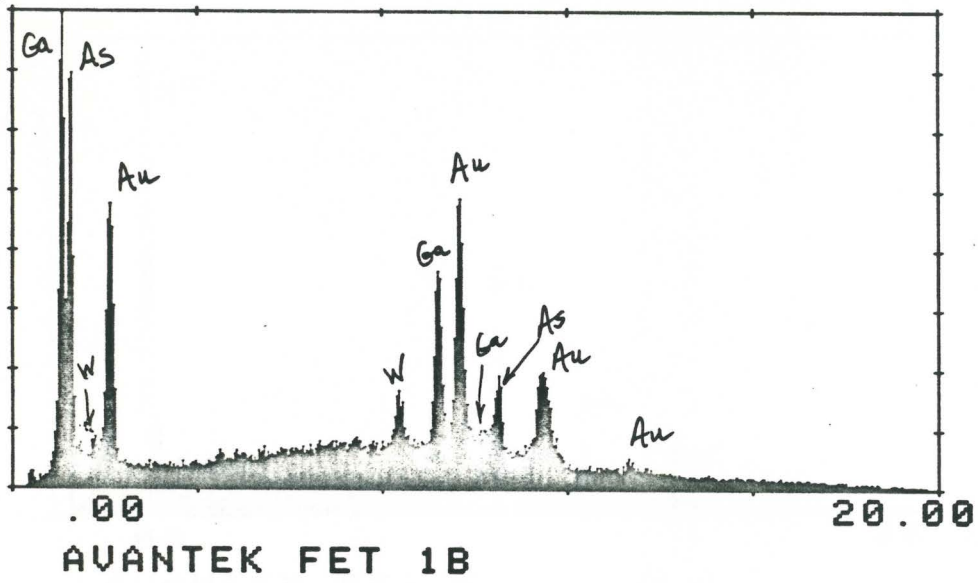
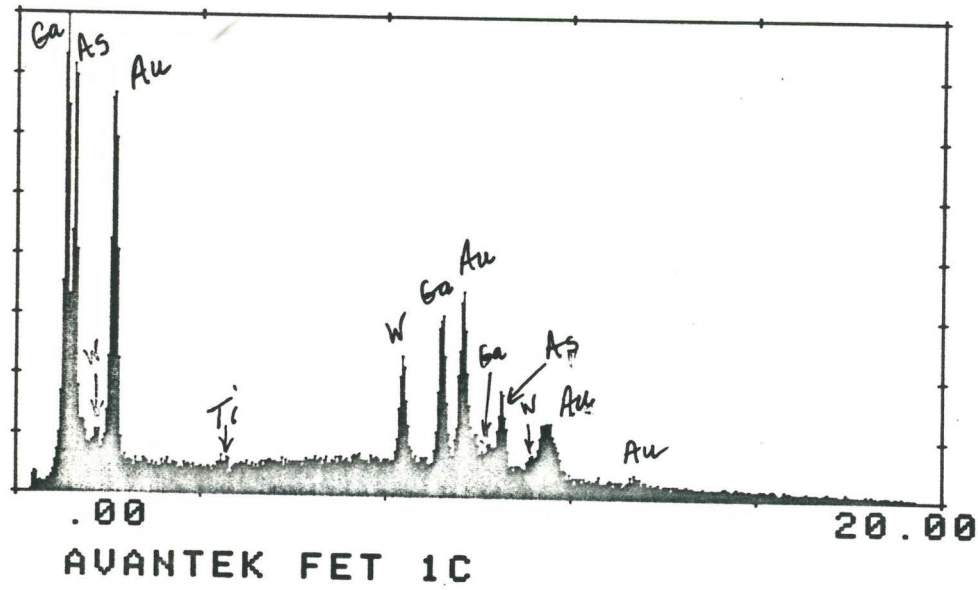


Figure 9A. Energy Dispersive Analysis of Avantek FET at Regions Indicated.





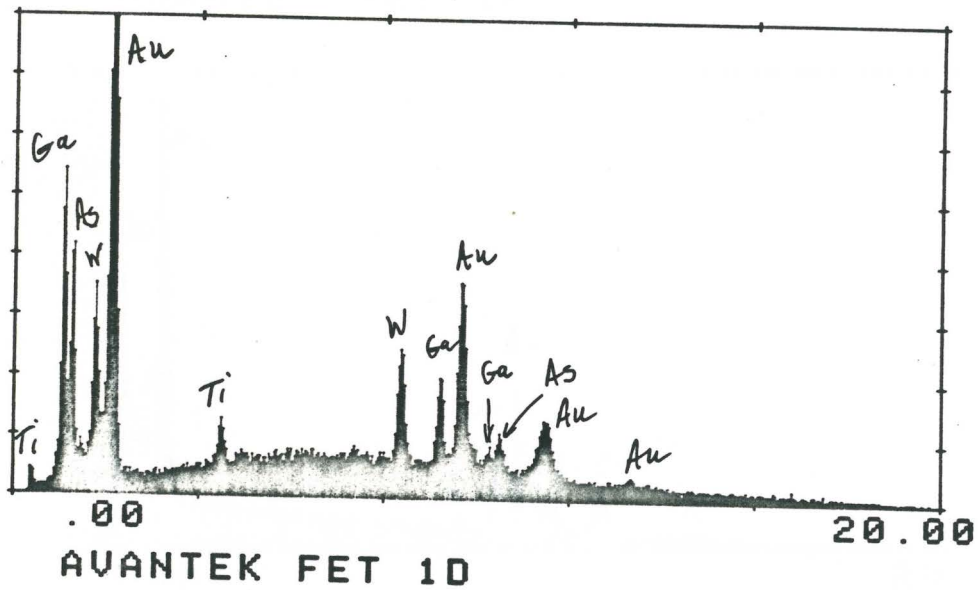
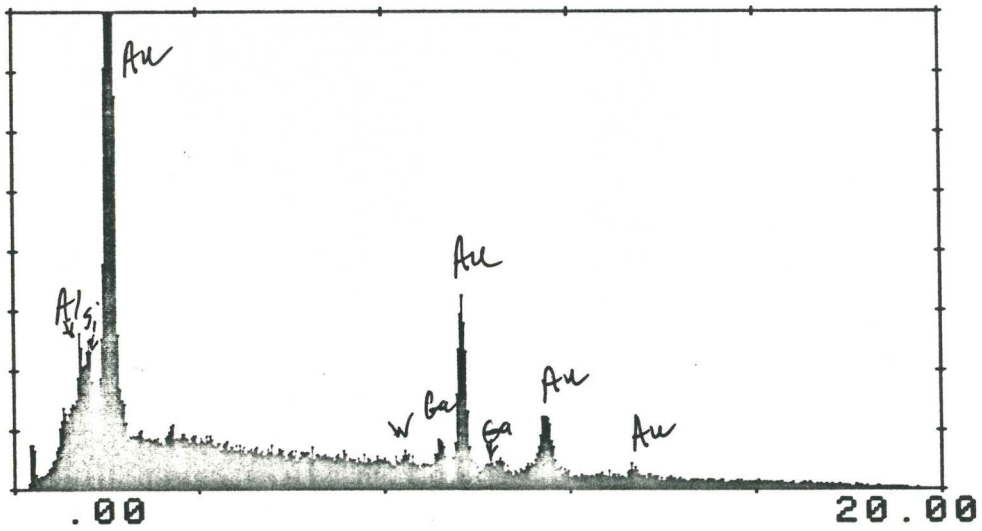
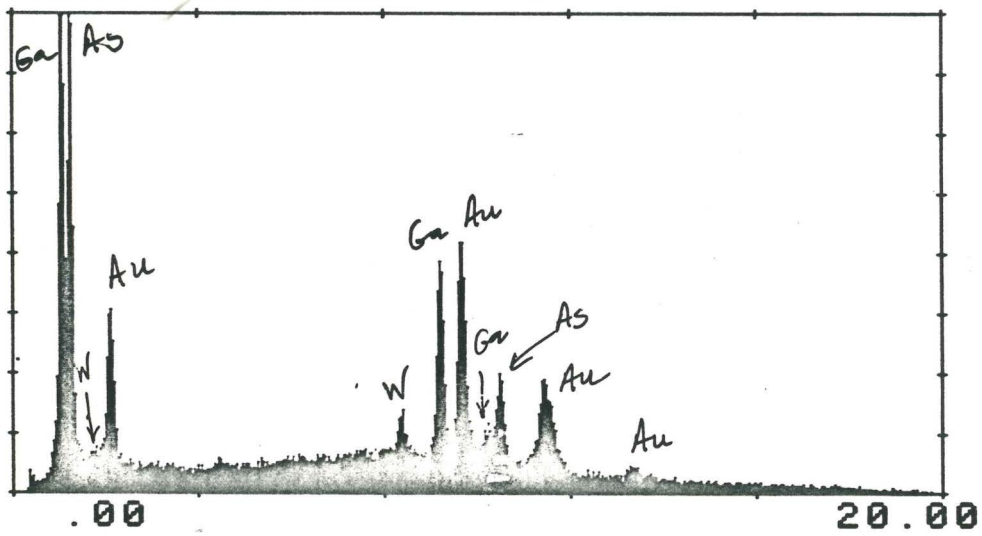


Figure 9A. Continued.





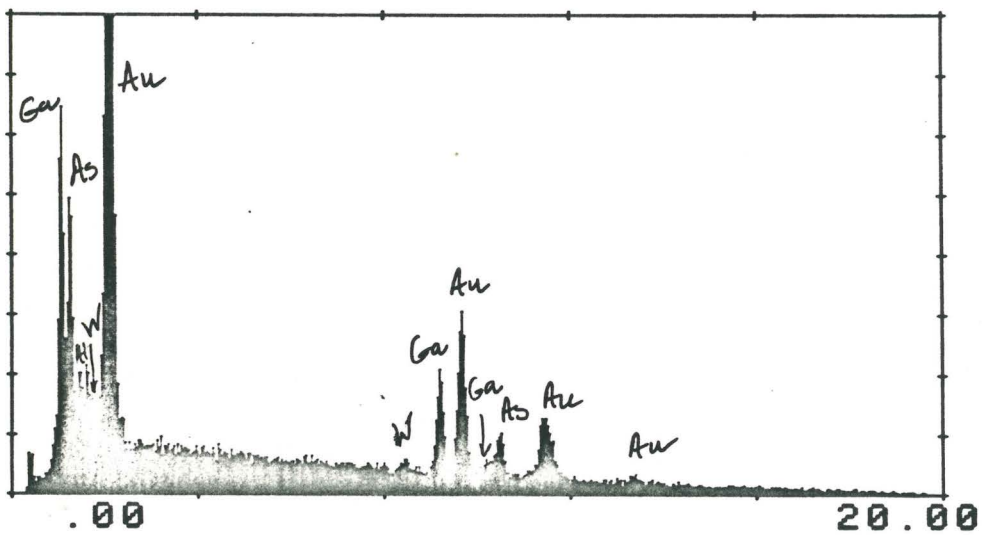


Figure 9A. Continued.