Design of Process and Environment Adaptive Ultra-Low Power Wireless Circuits and Systems

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Design of Process and Environment Adaptive Ultra-Low Power Wireless Circuits and Systems

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To my loving parents Mrs. Suprity Sen and Mr. Dilip Kumar Sen…

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SUMMARY

The explosive growth of portable battery operated devices has mandated design of low power circuits and systems to prolong battery life. These devices fabricated in modern nanoscale CMOS technologies suffer from severe process variation due to the reduced controllability of the fabrication process, causing yield loss. This calls for integrated low power and process tolerant design techniques, or design of systems that can adapt to its process and environment to maintain its performance while minimizing power consumption.

Currently, most of the wireless circuits are designed to meet minimum quality-of-service requirements under worst-case wireless link conditions (interference, noise, multi-path effects), leading to high power consumption when the channel is better than worst-case. In this research, we develop a multi-dimensional adaptation approach for wireless transmitters and receivers that optimally trades-off power vs. performance across temporally changing operating conditions by concurrently tuning control parameters in the RF front end to lower power consumption. Tunable circuits (e.g. LNA) with built-in tuning knobs providing independent controllability of important specifications allow optimal adaptation. Process sensing using intelligent test and calibration facilitates yield improvement and the design of process tolerant environment adaptive systems.

Chapter 1. INTRODUCTION

The objective of the proposed research is to investigate the design of Self-Aware Radio Frequency Circuits and Wireless Communication Systems that can adapt to environmental and process variations to always operate at minimum power levels possible, extending battery life.

The explosive growth of portable battery operated devices has mandated design of low power circuits and systems to prolong battery life. These devices are designed in modern nanoscale CMOS technologies to allow integration of mega functionalities per chip. The reduced controllability of the fabrication process at these nano dimensions requires the design of process variation tolerant components and systems. This calls for integrated low power and process tolerant design techniques, or design of systems that can adapt to its process and environment to maintain its performance while minimizing power consumption.

Currently, wireless circuits are designed to meet minimum quality-of-service requirements under worst-case wireless link conditions (interference, noise, multi-path effects), leading to high power consumption when the channel is better than worst-case. In the proposed research work, we develop a multi-dimensional adaptive power management approach that optimally trades-off power vs. performance across temporally changing operating conditions by concurrently tuning control parameters in the RF and digital baseband components of the wireless transmitter and receiver. This adaptation is performed in real-time for low power operation.

Low cost testing methodologies are developed for identification of the *health* of the wireless circuit/system. These are used in conjunction with tuning algorithms that tune a

wireless system under process variation to meet performance specifications and recover yield loss. This testing and adaptation is performed once during the post manufacture test/tune phase to compensate for manufacturing variations. This can also be applied periodically during in field operation of a device to account for performance degradation due to ageing. Finally, *process tolerant environment adaptive* systems are designed.

1.1. Origin and History of the Problem

The number of transistors in an Integrated Circuit (IC) has been doubling every 18 months following Moore's Law for last few decades. This has allowed the sustained growth of the IC industry by increasing the functionality per chip in every generation. However, increasing functionality per unit area has increased the power consumption per unit area (power density) significantly. According to data published by Intel in early 2000's [1] the power density of the microprocessors would reach that of a nuclear reactor if low power techniques are not employed. Hence a significant amount of research in VLSI in the first decade of 21st century has been targeted towards low power IC designs.

The doubling of transistor per unit area has been achieved by technology scaling, i.e. reducing the dimensions of the transistors. Scaling reduces the area as well as the capacitance associated with each node making the circuits faster. However, with continued scaling the IC industry is past the sub-micron dimensions and has reached the nanometer regime. The controllability of the fabrication process has reduced significantly due to these nanoscale dimensions of the transistors. This causes variability in fabrication resulting in undesired variation in the circuit and system performance. The traditional static circuits fail to meet the demand of the stringent system requirements due to the underlying variation of the transistors. This calls for a new paradigm of variability aware

circuit and system design, where the circuits/systems are intelligent enough to understand the underlying variation and able to heal itself by compensating appropriately (self-healing circuits/systems).

Low Power and Variation tolerant Analog/Mixed Signal/RF circuits' require a new/different set of design techniques that adapt the wireless transceiver systems and underlying circuits to simultaneously meet low power and high performance requirements with minimum power.

1.2. Conventional Wireless Systems

Conventional wireless circuits/systems are designed for the worst case channel, environment and process corner. Each of the variations is dealt by incorporating significant built in design margin which results in high power consumption. The sub blocks are designed for their respective specifications with enough design margins such that they work by themselves over channel, environment and process variations. The system and underlying circuits are not aware (for the most part) of their health and surroundings, i.e. they are so called *static* circuits.

1.3. Need for Environment and Process Adaptive Wireless Systems

1.3.1. Low Power Requirements in Wireless/Portable Systems

With the projected explosion in the number of multimedia wireless applications in the consumer electronics market, power consumption will be a critical metric in future designs of multi-mode multi-standard wireless devices, as most of these devices are portable (battery operated) and battery lifetime is a key demand among consumers. At the physical layer level, low-power design methodologies for digital systems have been

studied extensively but relatively fewer techniques have been proposed for Mixed Signal (MS) and Radio Frequency (RF) systems. However a lot of the Mixed Signal/ RF circuits (e.g. an Analog to Digital Converter (ADC), a Power Amplifier (PA)) are power hungry and are generally have to be overdesigned to work across different operating environments, process and temperature. Due to the sensitive nature of analog circuits and variety of specifications that needs to be satisfied simultaneously, low power techniques for analog/RF systems are required that adapts the system to always operate at the minimum power level possible.

1.3.2. Process Variation in Mixed Signal Circuits and Yield Loss

With aggressive scaling of CMOS the controllability of the fabrication process is decreasing with each technology node. In the nanometer design regime, high performance Analog/RF circuits are expected to be increasingly susceptible to process variations. It is becoming increasingly impossible to keep the 3σ variations of the process parameters within 10% bound [2][3]. The variability in the nanometer regime is making circuits less reliable and resulting in significant yield (% of non-faulty chips) loss.

Modern Wireless circuits are designed to be extremely high performance as demanded by the consumer. This requires designing the circuits at the "edge", making the circuits very sensitive to any process variation. In the nanometer regime, the increased variation in the process causes these high performance systems to vary al lot from its desired specifications, resulting in throwing away of the device. This causes yield loss and results in reduced profit for the IC design company. With static design techniques, if we try to address this issue by leaving an increased guard band, the power consumption goes up. Hence there is a pressing need for variation tolerant circuits which are also low

power. Significant research work has been done in recent years in variability aware design of digital circuits. Important techniques include adaptive body biasing [4], dynamic supply voltage scaling [5][6] and variable size keepers [7]. Radio Frequency (RF) circuits are very sensitive to the increasing process variation. To make RF design successful in the nanometer regime with acceptable yield there is an increasing demand for variability tolerant RF circuit design techniques, similar to their digital counterpart.

One way to address this issue is to have intelligent circuits and systems that can understand the process corner it is in and tune itself to meet the required specifications, while minimizing power consumption. This requires built in tunability in Analog/Mixed Signal/ RF circuits which is traditionally not that common due to the sensitive nature of these circuits.

1.4. Prior work in Adaptive Wireless Systems

In this section we summarize the prior efforts in adaptive wireless circuits as well as system design for low power and process variation tolerance.

1.4.1. Adaptivity in Low Noise Amplifiers (LNA)

There have been few efforts on designing an adaptive LNA for process variation tolerance. These are summarized as follows. Tuning of the input match frequency can be achieved using several-tap tunable inductors [8]. Another way to control only the non-linearity of the LNA is to add an extra current stealing path (Inter-Modulation Distortion or IMD sinker) to a traditional LNA design [9]. The gain of an LNA can be stabilized using damped LC loads [10]. Though this takes care of gain variation to some extent it is not able to compensate for noise figure (NF) and input reflection co-efficient (S11). Also

this technique is specific to tuned amplifiers. The input and output matching is a critical requirement to ensure proper transfer of signal in RF Amplifier. These matching networks can be made process variation insensitive by breaking then from one step to two step and choosing the components values such that the sensitivity to process variation is minimized [11]. A process and temperature variation tolerant Bluetooth RFIC was designed in [12] by using bandgap references, current compensation circuit and active loads.

1.4.2. Adaptivity in Power Amplifiers (PA)

A PA is the last block in a wireless transmitter that drives the signal to be transmitted to the antenna. Due to high transmission power requirements the PA tends to be the most power hungry block in the transceiver. It needs to provide gain to the signal while delivering high output power, i.e. process signals with extreme large swing (typical swing is close to 1.7 to 2 times the supply voltage). The key specifications include Gain, Non-linearity (IIP3), input and output matching, Adjacent Channel Power Ratio (ACPR), bandwidth (BW) and efficiency. Since the signal levels in a PA are very high the tunability achieved by gate and drain bias control are minimal. Voltage based tuning can be aided by dynamically companding in the digital to reshape the signal to reduce its peak to average ratio [13]. Output of the PA has to conform to stringent spectrum requirements set by the Federal Communications Commission (FCC). This requires highly linear operation of the PA, which reduces its efficiency or makes it power hungry. A pre-distortion function, i.e. the inverse of the PA nonlinearity is used in the baseband DSP to increase the overall linearity of the system even with low power consumption.

In the system level, to reduce interference and increase efficiency, output power of the Mobile Station (MS) is varied depending on the channel condition and distance from the Base Station (BS). Using power control information (based on received signal strength) sent by the BS to MS through the BCH (Broadcast channel) [14][15], the PA average output power is varied. If the DC power consumption is kept fixed (i.e. static PA) the efficiency of the PA is very low for the time that it is not transmitting at the maximum average output power level. An approach to increase the operational efficiency of RF transmitters has been to use a tunable PA (such as Agilent ACPM-7891[16]) in the front-end. A MS power controller (such as National Semiconductor LMV243[17]) uses the information from BS to control the output power of the PA by applying proper control voltages and sometimes using a control loop[15][18]. Output power is varied in a wide range as described in [19]. For example, output power could be varied from 5 -39 dBm for GSM 900MHz band. This recovers some of the efficiency loss due to variable distance between the BS and MS.

To increase the efficiency of PAs using circuit level techniques, the supply voltage of the PA is changed according to the envelope of the signal. These PAs can be broadly divided into 3 categories [20], namely slow tracking, envelope tracking and polar modulation PAs. A slow tracking PA [21] supplies the PA with a voltage slightly greater than the largest peaks of the envelope. Hence it can only recover the efficiency loss due to power-control back-off. An envelope following or envelope tracking PA [22]-[24] have been developed in which the supply voltage is dynamically modulated by the estimated or tracked envelope to keep drain efficiency high. Hence it allows recovery of lost efficiency due to both modulation and power-control back-off. In these methods, the

envelope amplitude information has to be extracted from the signal and incurs extra complexity and increased hardware overhead. In polar modulated PAs [25], [26] the supply modulator applies the required envelope signal directly onto the carrier through a saturating PA. Though the use of saturated PAs increase efficiency, the bandwidth requirements of the AM path is significantly high and the noise requirements of the supply modulator makes this implementation impractical. A power management block presented in [27] provides good efficiency while providing variable output voltages. This on-chip block can generate drain and gate bias for a PA using inputs from DSP making adaptation of PAs easier. This work also shows adaptation of a PA with varying average output power to maintain high efficiency, using the above mentioned PMU.

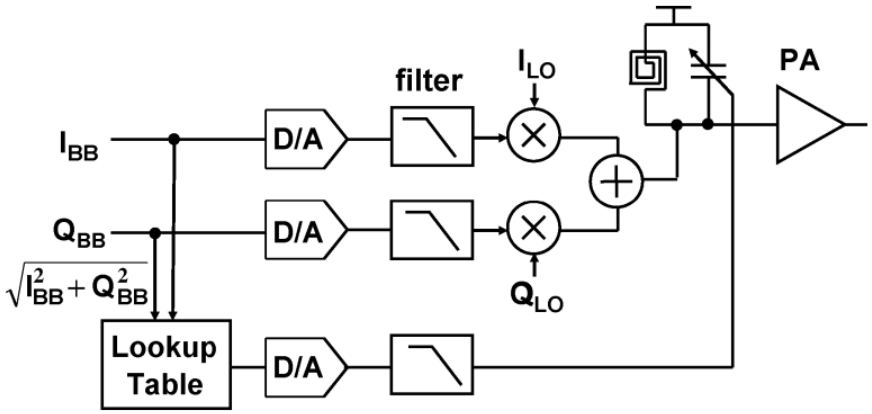


Figure 1: Feed-forward AM-PM correction using varactor tuning [28]

Another significant effect in the PA is input power dependent gain compression and phase distortion. AM-PM distortion can be corrected by introducing an opposite phase shift to cancel the signal power dependent phase shift of the PA. Figure 1 shows a schematic that achieves this goal. A varactor is placed across one of the inductors in the mixer or the PA. By changing the control voltage of the varactors [28], the resonance frequency of the tank can be changed, thus modifying the phase shift incurred by the signal. The control voltage changes according to the amplitude of the input signal in such

a way as to cancel the AM-PM distortion of the PA. This shows a real-time technique to correct for AM-PM. Under process shift, the AM-PM curve changes for a PA. This can also be compensated for using this technique just by changing the way control voltages are applied.

1.4.3. Adaptivity in Analog to Digital Converters (ADC)

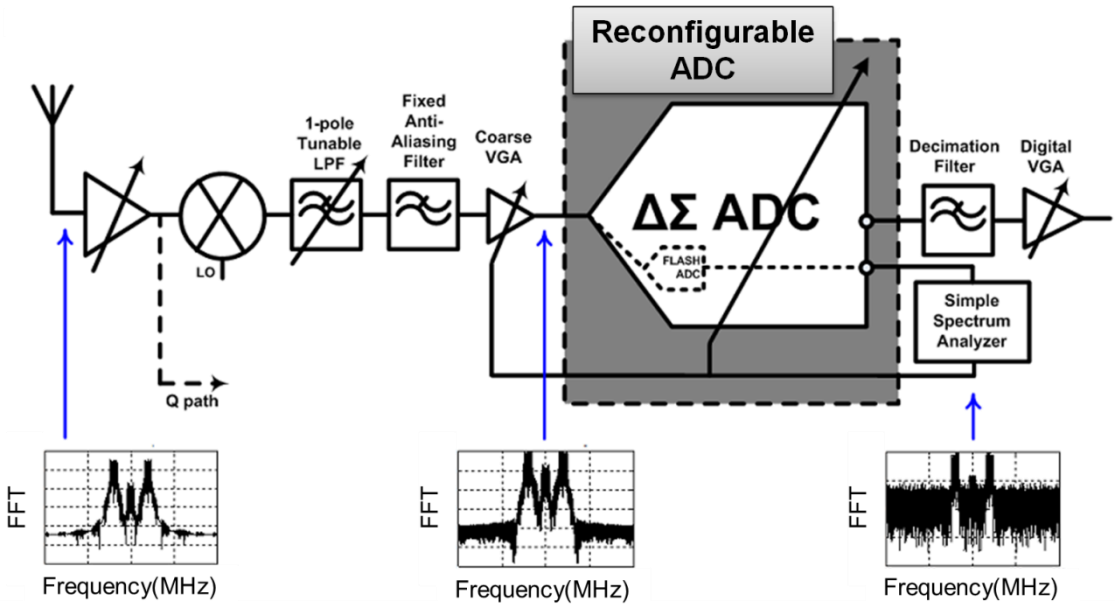


Figure 2: Reconfigurable ADC as a part of a wireless receiver that reduces its power consumption when interference is not high [29].

ADCs or Analog to Digital Converter is an important sub block in a wireless receiver. It converts the analog signal to digital domain for further processing by the DSP. There has been some effort to make ADCs low power by using them in an environment adaptive manner. To reduce power consumption the order of the loop filter can be reduced dynamically depending on the interference environment in a sigma delta ADC [29]. This could be achieved as shown in Figure 2. The reconfigurable ADC consists of several modes allowing power versus performance tradeoff. As the

interference to signal ratio goes down the requirement of the ADC dynamic range is relaxed and hence a lower power mode can be used. A low resolution flash ADC is used for spectrum sensing. A simple spectrum Analyzer is used for spectrum sensing from the flash ADC output and the mode of the ADC is set based on the sensed spectrum. This allows power savings by choosing lesser performance when interference in the received signal is low.

1.4.4. System Level Adaptivity in Transceivers

Several techniques for low power operation of wireless circuits have been proposed in the literature. At the physical layer, low-power design methodologies for digital systems [30][31] and analog/RF systems [32][33] have been studied extensively. The issue with these approaches though is that circuit designs incorporate margins to account for *worst-case* estimates of process variability, and thermal effects in the RF front-end, and channel conditions corresponding to different modes (data rates) of transmission. However, for most of the time a wireless device is powered up for operation, it *is not in a worst case environment* and hence, consumes more power than necessary under the majority of operating conditions. The need for dynamically adapting RF front-end, baseband and digital circuits to save power and enable multi-mode operability in future wireless devices was discussed in [34][35][36]. There exist media access control (MAC) and network-level dynamic power management schemes [37] that conserve power by adapting the data rate (modulation and coding rates) based on certain channel quality metrics derived from the analysis of training symbols. Present-day wireless devices also feature high-power, low-power, and shut-down modes, that are activated on the basis of prevailing channel conditions. Though these approaches are effective in reducing the

power consumption levels, they do so in a few discrete steps, and hence do not fully exploit the design margins through fine-grained system-level adaptation. In a recently published work [38], an energy scalable RF transmitter was proposed, where the front-end is dynamically tuned (supply, bias, resistances) for each data rate modulation set by the higher-level link layer protocol. The tuning is driven by channel quality as determined by channel estimation metrics and relies on simulation of a large number of channel and RF front-end settings. In [40], the authors show a reconfigurable LNA based on DSP assisted testing and self-tuning.

Chapter 2. DESIGN FOR PROCESS VARIATION TOLERANCE

2.1. Problems with Process Variation: Yield Loss

The continued scaling following Moore's law has resulted in feature sizes in the nanometer regime. The reduced controllability of sub-wavelength lithography has resulted in severe manufacturing variations. This in turn results in parametric variation in the specifications of the circuits, resulting in more and more devices failing the required performance threshold. This results in significant yield loss which directly affects the profit margin. Hence, design techniques that are robust to manufacturing variations are required. In the prosed research, we tackle this issue in two ways. First circuit level process tolerance is demonstrated using an LNA as a test vehicle. These circuits inherently show robustness to process variation. A second approach is to tackle process variation using system level control. These *self-healing* systems would consist of a way to sense the process corner or health of the system. Using this information and built in tuning knobs a system level algorithm tunes the device back until it comes back within its acceptable specification bound. The next two sections describe such circuit level and system level process tolerance, respectively.

2.2. Circuit Level Approach: A Self-healing LNA example

Design of a *self-compensating process variation tolerant RF Low Noise Amplifier (LNA)* is described here [40]. A novel non–intrusive mixing technique is described which enables minimal intrusion negative feedback in RF circuits making them process variation tolerant. The following design technique provides 18% yield improvement over comparable conventional LNA under severe process variation.

A well-known and widely used method for process variation tolerance in analog circuits is negative feedback. This can also provide a formal methodology in designing process variation tolerant RF circuits. But this technique is not very common in RF circuits, as any type of conventional sensing and mixing in highly sensitive RF nodes changes the RF circuit performance significantly. So, loss due to performance degradation becomes greater than the gain achieved by stabilization using negative feedback. The techniques described here address this problem by developing a non-intrusive mixing technique as well as minimizing the intrusion of the sensing circuit. This enables use of negative feedback in RF circuits and helps in designing process variation tolerant RF front ends. Figure 3a shows a conventional cascoded LNA typically used in RF receiver front ends. Next, the minimal intrusion sensing and non-intrusive mixing technique is described.

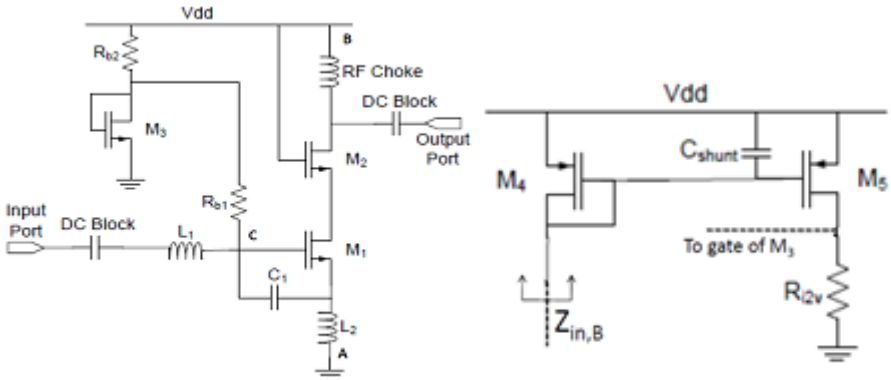


Figure 3: a) Conventional cascoded LNA b) Minimal intrusion sensing circuit

2.2.1. Minimal Intrusion Sensing

In the LNA of Figure 3a the most important single parameter that could give the information about effect of process variation on it, is the bias current flowing through the main branch (containing M1 and M2, L2 and RF choke) (Id). For ensuring proper RF

operation, the LNA needs to be biased up "properly" under any process condition. So emphasis is placed on sensing Id to acquire information about the process. To acquire true information of Id it has to be sensed directly from the main branch. The problem now, is to minimize the intrusion, i.e. to minimize the effect of the sensing circuitry on the RF performance of the LNA. The two likely sensing points are A and B (Figure 3a). In [41] sensing from A has been proposed by inserting a small resistance (7Ω) in between L2 and ground. But this increases noise figure (NF) of the LNA severely. Another approach is shown in [42] where the RF voltage across L2 is sensed and is processed in baseband using a 'three tonal' approach to find out information about the LNA. However, it can only be used for testing the LNA with known test input signal. Figure 3b shows the sensing circuit which is to be inserted at point B. This is essentially a PMOS current mirror with an additional C_{shunt}. The resistance looking into the transistor M_4 without C_{shunt} is $1/g_{m,M4}$. This impedance should be minimized to minimize the loading on the LNA. Hence $(W/L)_{M4}$ is made as large as possible to minimize the resistance looking into the diode connected transistor. Also C_{shunt} is added in parallel with $C_{gs,M4}$ and $C_{gs,M5}$. This capacitance is big enough to short at RF frequencies, almost shorting the impedance looking into sensing network ($Z_{in,B}$). At RF frequencies it could be written as follows:

$$Z_{in,B} = \frac{1}{Y_{in,B}} = \frac{1}{g_{m,M4} + j\omega_{RF}(C_{shunt} + C_{gs,M4} + C_{gs,M5})} \quad (1)$$

$(W/L)_{M4}$ and C_{shunt} are maximized to maximize the denominator in (1) and hence make $Z_{in,B} \rightarrow 0$ at RF frequencies. This minimizes the amount of loading on the LNA due to the sensing circuitry. Also $(W/L)_{M4}/(W/L)_{M5}$ is designed to be 100 to make I_{M5} very low compared to I_d. This ensures *insignificant additional power consumption* compared to the

original LNA. R_{i2v} converts this sensed current into a voltage which would be used for mixing.

2.2.2. Non-Intrusive Mixing

Traditional analog mixing techniques (shunt and series mixing) fail in RF frequencies as the feedback network is directly connected to the gate or source of M_1. Connection to the gate (point C in Figure 3a) changes the input impedance significantly, whereas connecting to the source increases NF and also degrades input matching.

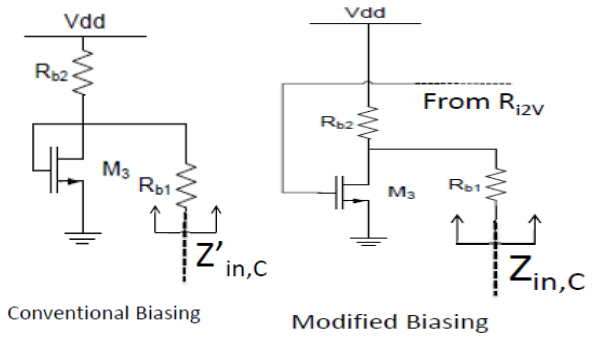


Figure 4: Non-intrusive mixing using modified biasing technique

Figure 4 shows a novel mixing arrangement by modifying the biasing transistor. Instead of biasing M1 from a diode connected M3 (conventional biasing), it is biased from the drain voltage of M3, where M3 is biased by the voltage generated across Ri2v (modified biasing). This doesn't load node C at all and still provides the required mixing capability. The impedance looking into Rb1 (Zin,C) should be as high as possible, such as the biasing arrangement has no effect on RF performance. This impedance could be written as follows:

$$Z'_{in,C} = R_{b1} + R_{b2} \| \frac{1}{g_{m,M_3}} \tag{2}$$

$$Z_{in,C} = R_{b1} + R_{b2} \,||\, r_{o,M3} \tag{3}$$

Where, $g_{m,M3}$ and $r_{o,M3}$ are the transconductance and output resistance of the biasing transistor M_3 respectively. $Z'_{in,C}$ is the impedance looking into conventional biasing circuit whereas $Z_{in,C}$ is the impedance looking into the modified biasing/mixing circuit. Since

$$r_{o,M3} >> \frac{1}{g_{m,M3}} \Rightarrow Z_{in,C} > Z'_{in,C} \tag{4}$$

Hence, the modified biasing circuit improves the RF performance and hence it's completely non-intrusive.

2.2.3. Process Variation Tolerant LNA

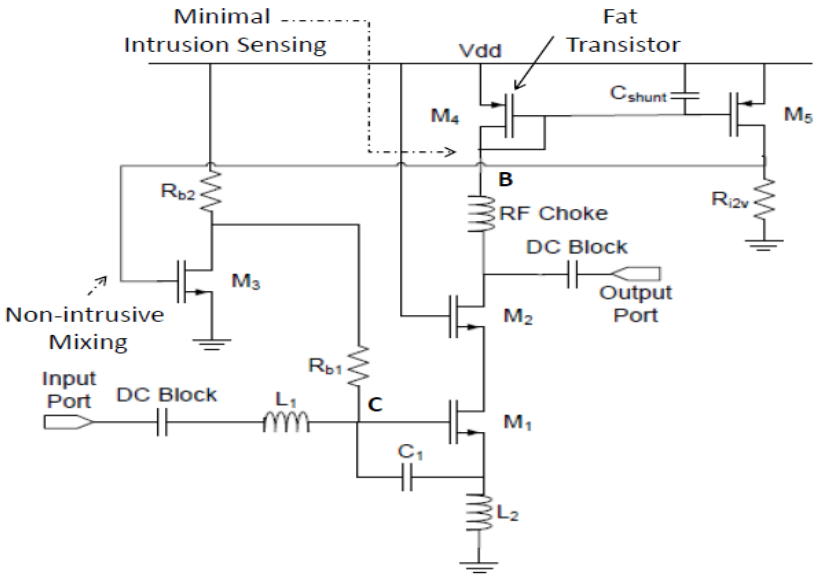


Figure 5: Complete circuit diagram of process variation tolerant LNA

The concepts described in the previous sections are used to build a process variation tolerant Low Noise Amplifier as shown in Figure 5. The analysis of the circuit could be understood by following the feedback loop. Due to process variation, say I_d has

increased from its nominal designed value. This results in similar increase in the mirrored current I_{M5} and hence increases the voltage across R_{i2v}. This acts as the gate to source voltage of M_3 ($V_{G,M3}$). As $V_{G,M3}$ goes up drain voltage of M_3 goes down reducing the biasing voltage (point C) of the transconductance stage, in turn reducing I_d. Thus through this negative feedback loop this circuit keeps the I_d constant (as close as possible to the nominal designed value of I_d) or in other words keeps the LNA biased "properly" even under severe process variation. Under RF operation since $Z_{in,B} \rightarrow 0$ it doesn't have much effect on the circuit and keeps the RF performance of the circuit intact.

(5) and (6) shows the dependence of $V_{G,M1}$ on I_d. As I_d increases $V_{G,M1}$ decreases and vice versa showing the validity of the negative feedback. The parameters in these equations are used in their traditional sense and they are optimized in the design to maximize the sensitivity of the feedback loop.

$$V_{G,M_3} = I_d \times \frac{(W/L)_{M_5}}{(W/L)_{M_4}} \times R_{i2v} \tag{5}$$

$$V_{G,M_1} = V_{dd} - \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{M_3}(V_{G,M_3} - V_{tn})^2 \times R_{b2} \tag{6}$$

2.2.4. Yield recovery through process variation tolerant LNA

The results of the design are presented in this section. For comparison purposes a conventional LNA and a process variation tolerant LNA has been designed in TSMC 0.25μ technology, working at 1.8 GHz with similar gain, noise figure (NF) and input return loss (S11) (Refer Table 2). Simulations have been performed using Agilent ADS design tools. Severe process variations have been introduced to important process parameters as shown in Table 1. The parameters considered are minimum channel length (L_{eff}), oxide thickness (T_{ox}), threshold voltage (V_t), capacitances (C) and inductances (L).

Table 1 Variation of parameters considered

Process Parameter	L_{eff}	T_{ox}	V_t	C	L
3σ variations (%)	60	30	30	30	30

Table 2 Comparison of Both LNA

Design	Nominal Gain(dB)	Nominal NF(dB)	Nominal S11(dB)	**Yield (%)**
LNA (conventional)	15.072	1.131	-22.85	**64**
LNA (process-tolerant)	15.019	1.136	-23.05	**82**

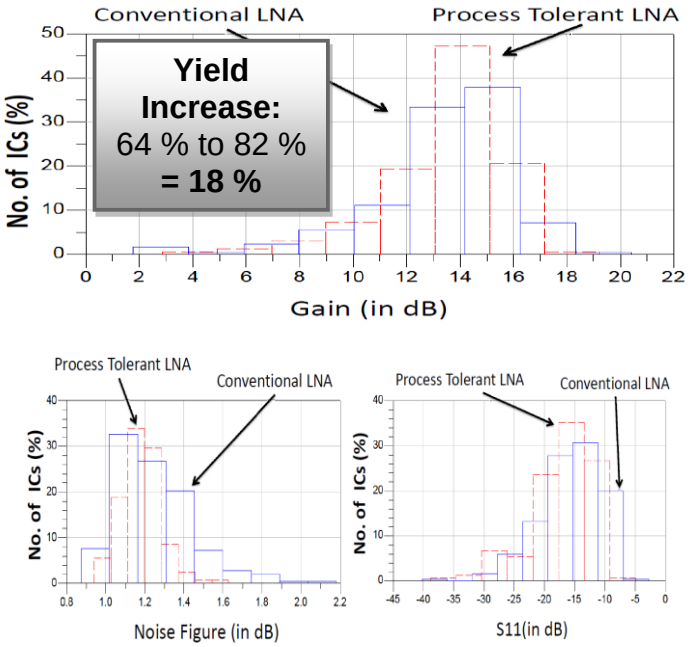


Figure 6 Variation of Gain, NF and S11 of the process variation tolerant LNA and conventional LNA

Yield analysis has been performed with the following performance constraint: 11dB<Gain<17dB, S11<-10dB and NF<1.35dB. The yield of the variation-tolerant circuit is found to be a significant 18% higher than its conventional counterpart. Fig. 6 shows the distribution of % of ICs based on gain, NF and S11 obtained from yield analysis. It can be seen that for all the specs process-tolerant LNA performs better than the conventional one (less variation around its nominal spec). Hence the above described techniques lets us design a process variation tolerant LNA which self-compensates under variation. This technique can very easily be extended to other RF components opening up the paradigm of variability aware RF front end design.

2.3. System Level Approach

2.3.1. Effect of Process Variation and Built in Tunability

As described in previous sections the reduced controllability of the fabrication process in the nanometer regime reflects as significant variation of the important specifications from chip to chip. The yield of a system design gets affected severely as variation in the subsystems directly affects the system specifications. We have discussed circuit level techniques to address this issue. In this section we investigate requirements and possibility of system level healing. The general methodology of '*healing'* a process skewed system is to have *built in tunability* in the system and intelligently tune the system under variation such the system specifications come back within acceptable bounds[43][44][45][46].

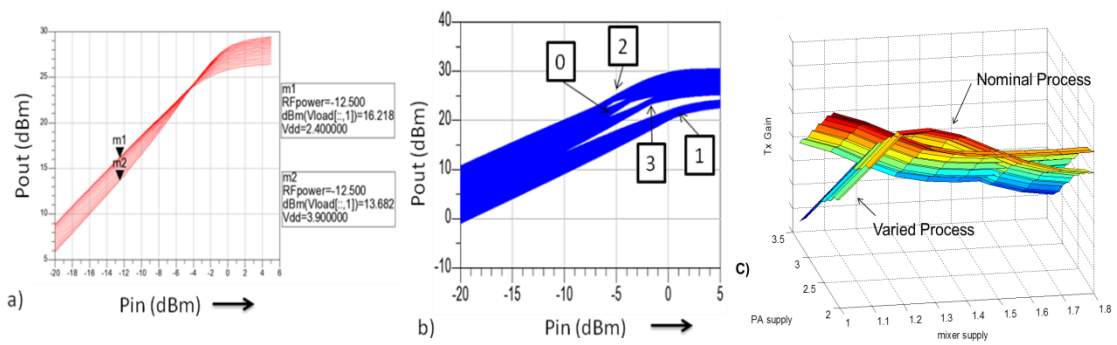


Figure 7: a) P_{out} vs P_{in} for a PA over V_{dd} variation. b) P_{out} vs. P_{in} over all combination of tuning knobs (supply and bias) for 4 process instances c) Gain of a transmitter over all tuning knob combinations for 2 process instances. [46]

This calls for identifying proper tuning knobs in a design such that the tunable range obtained of the specifications concerned is close to or more than the variations of the same for a 3 sigma variation of the process parameters. This fact is illustrated for a PA in Figure 7. Figure 7a shows the P_{out} vs. P_{in} for a PA with V_{dd} (supply voltage) varying within its tuning range. It can be seen that for higher supply voltages gain is lower (due to g_m being lower at high values of I_d), P_{1dB} is higher and vice versa. So gain vs. P_{1dB} tradeoff can be achieved by using supply as a tuning knob. Similarly even more tuning capability is achieved by using supply and bias of the PA as two tuning knobs simultaneously. Figure 7b plots the Pout vs. Pin for the PA over all combinations of supply and bias knob settings for 4 process instances, 0 being the nominal instance. It is to be noted that some of them (namely 2 & 3) exhibit 'small parameter variation' [46] and can be tuned back completely by choosing the right tuning knob values. On the other hand there are instances (like 1) which exhibit 'large parameter variation' and can only be tuned for its Gain and not P1dB. To understand how a specification changes with process and how it can be tuned back the Gain of an illustrative Transmitter (with tunable PA and

Mixer) is shown in Figure 7c for the nominal process and a varied process instance. For the nominal case the transmitter is to be biased at maximum gain. However, under variation this setting is not optimum for gain. So the job of the *healing algorithm* is to find out a new tuning knob setting such that the gain is closest to its nominal value for the varied process instance. Now there could be several such knob settings that provide the same gain. A *power conscious* self-healing system would choose the setting with minimum hit in power consumption. A *system level* power conscious self-healing framework would find a new setting that optimizes all the specifications for the system simultaneously while minimizing power.

2.3.2. System Level Healing Framework

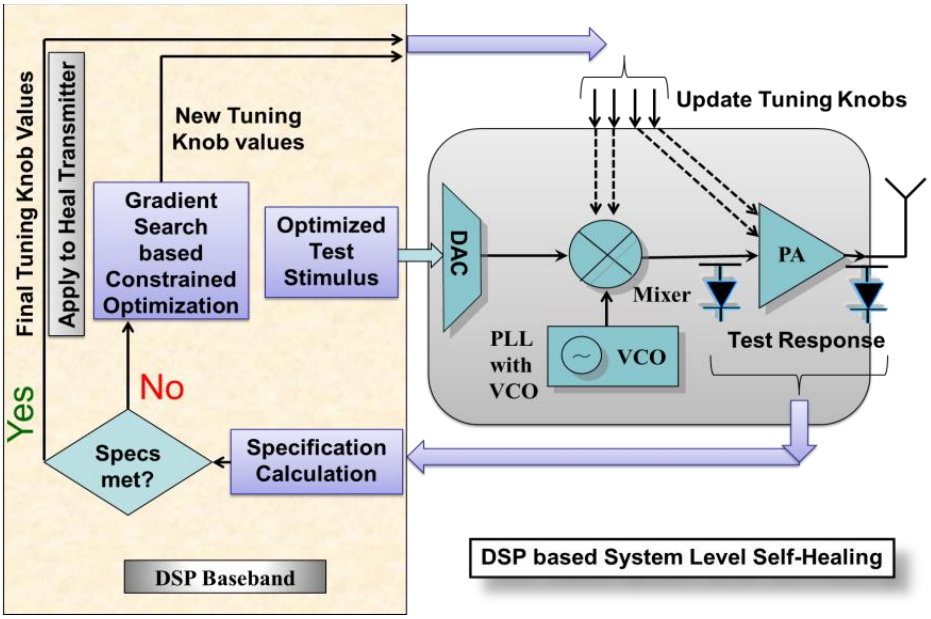


Figure 8: System Level Power Conscious Self-Healing Framework

The framework for power conscious system level self-healing is described below and is shown in Figure 8. The methodology consists of the following key steps:

- The system is made up of tunable components with built in tuning knobs.

- During production test/characterization/tune phase any instance with non-nominal specifications are tuned to be as close as possible to the nominal one.
- An optimized test stimulus is applied to the system with nominal tuning knob settings. Important specifications are calculated from the test response using standard methods or alternate test methods [47] using built in sensors (as shown in Figure 8) for faster response time.
- If the specifications are within the preset bounds the device passes and the current knobs settings are to be applied while operation.
- If not, the device would have failed in static sense and should now be healed to try to pass it, so that the yield increases.
- A power conscious constraint optimization algorithm updates the knobs settings and repeats this procedure until the best knob setting for the given process is achieved.
- The final setting found from the optimizations is applied to the system during runtime operation.
- At the end of the optimization a significant number of instances are expected to meet all of the specifications (as 2 & 3 in Figure 7b), however there would be some that would still not meet all the specifications (as 4 in Figure 7b).

The detailed of this system level self-healing methodology is to be found in a co-authored work titled "Self-Healing RF SoCs: Low Cost Built-In Test and Control Driven Simultaneous Tuning of Multiple Performance Metrics" [50].

2.3.3. Need for Process Identification through testing

One aspect of achieving complete self-healing systems is to be able to test for the health of the RF system. Identifying the process corner of the manufactured device

requires low cost fast test techniques targeted towards key specifications. To make tuning/self-healing realistic or implementable in real production test phase it is important to tune the system within the time it takes to test the system using present techniques. This calls for orders of magnitude improvement in test times compared to standard testing methodologies. The process information gathered from the testing phase is then used by an algorithm to tune the system back to recover yield loss.

There have been significant efforts for developing fast and accurate test techniques. The most important being Alternate Test [47] that uses regression based techniques to map the response of a device to carefully crafted test stimulus to its specifications. This technique, though very useful in fast and accurate prediction of most of the specifications, does not perform well for some key specifications like amplitude to phase distortion (AM-PM) etc. Hence low cost test techniques targeted towards such key specifications are required. In this work we address this by developing a low cost rapid test methodology for AM-PM and IQ mismatch testing. The next chapter will first highlight the Alternate Test and then describe the development of new test techniques.

Chapter 3. LOW COST TESTING FOR IDENTIFICATION OF PROCESS-VARIATION abcdeffwwgre

3.1. Previous Work

3.1.1. Alternate Testing

Conventional test strategies for mixed-signal, analog and RF circuits are based upon specification based testing techniques where the DUT specifications are measured and compared against pre-defined specification bounds to make pass/fail decisions for each specification. This requires a different test set-up for each specification resulting in an increase in test time and test cost. Alternate test [51]-[52] & [53], (as shown in Figure 9) on the other hand makes use of a single test configuration and predicts *all of the specifications of interest with a single input stimulus*, thereby, reducing the overall test time and test cost.

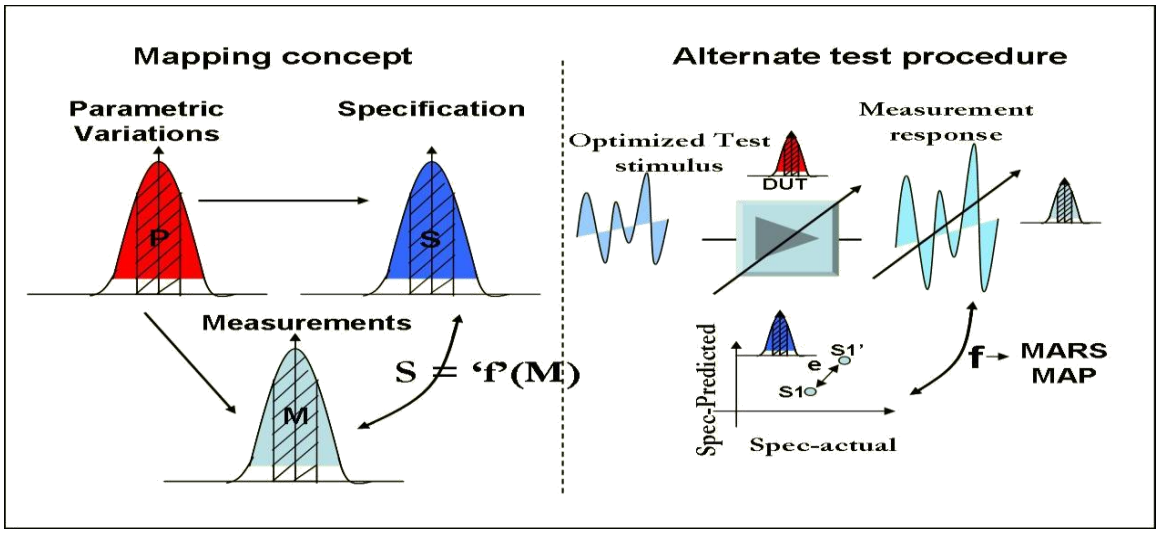


Figure 9: Alternate test framework

The fundamentals of alternate test framework are briefly described in this chapter. Consider variations in the process parameter space **P** of Figure 9 that affect the specifications of the DUT. For low cost diagnosis, an *alternate set of measurements* is determined such that the *test measurements are strongly correlated with variations in the test specification values* of the device under test (DUT) under process variations. This set of measurements defines the *measurement space* **M** of Figure 9. For RF devices, the set of **M** measurements is made on the output of a sensor (e.g. envelope detector) connected to the RF device. Any deviation in the observed measurements from the expected implies a corresponding deviation of the measured RF specifications of the DUT from the expected in the *specification space* **S,** due to perturbations in the process space **P** (see perturbations indicated in Figure 9). A nonlinear regression mapping model using MARS (*M*ulti-Variate *A*daptive *R*egression *S*plines) [54] is then developed using measurements on a "training set" of devices. This model is then used to predict the RF test specifications **S** of the DUT from the observed alternate test measurements **M** as shown in Figure 9. The process of applying the alternate test and predicting the DUT specifications S from the alternate test measurements is performed by algorithms running on the baseband DSP. The failure coverage of the alternate testing technique depends on the choice of the input test stimulus. The input test stimulus is carefully optimized to result in an output response that is *highly correlated with the specification values of interest*. The optimization of the test stimulus depends on the type of DUT being tested and the performance parameters being evaluated. For a given DUT there are several test generation algorithms [55] available for optimizing the input test stimulus. The optimized test stimulus is applied to each of these DUTs and their resulting responses are sampled

and stored. Simultaneously, the output specifications of these devices are measured using the conventional specification test set-ups. The sampled transient measurements are mapped onto the specifications of the device using non-linear regression functions. During production test, this non-linear regression function is used to predict the specifications of a DUT from its response to the same optimized test stimulus. The production test implementation of alternate test technology is shown in Figure 10.

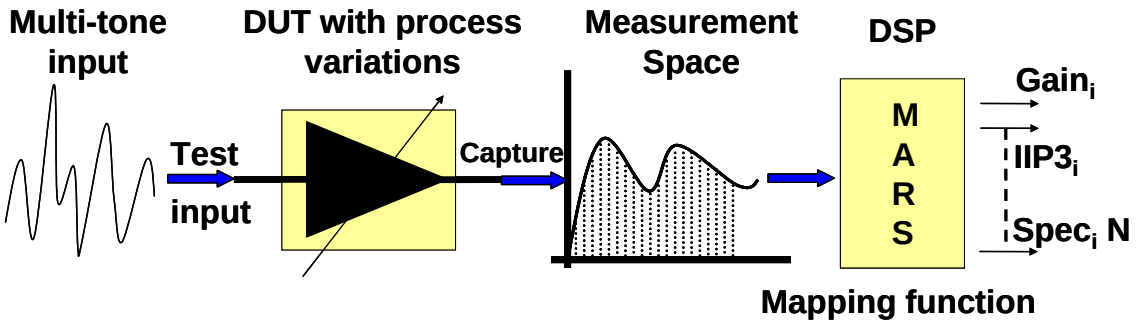


Figure 10: Production test implementation of alternate tests

Though the above described Alternate test is very fast and accurate at predicting specifications like Gain, IIP3 (a linearity metric) etc. it is not so good at measuring phase distortions.

3.1.2. Need for Phase Distortion Testing

Modern wireless communication systems exhibit an increased demand for spectrally efficient modulation techniques. This, in conjunction with strict FCC regulations on out of band interference of a transmitter necessitates the use of high linearity RF (Radio Frequency) front ends. In this context, the linearity of RF transmitters is dominated by the linearity of the RF Power Amplifier (RF PA). The crucial non-linear distortion effects at high powers in a PA are amplitude and phase distortions or AM-AM (Amplitude Modulation to Amplitude Modulation) and AM-PM

(Amplitude Modulation to Phase Modulation). Hence, measurement and calibration of AM-AM and AM-PM distortion is critical for robust operation of wireless communications devices. It has been shown [56] that by just calibrating for the AM-PM effects of a PA its efficiency can be increased ~3× (2.4% to 6.7%). As MS/RF SOCs are increasingly going to be in the "critical path" of future multimedia systems based on VLSI systems in scaled technologies, the testing of MS/RF components [57], [58], [59], [60], [61], [62], [63] is a critical problem in the manufacturing of reliable VLSI systems.

There have been a number of techniques listed in prior literature which deal with modeling and compensation of AM-AM and AM-PM effects. These range from simple polynomial based models to complex models based on volterra filters [64][65] to model memory effects in PAs. In [66] the authors present a detailed comparative study of behavioral modeling techniques for PAs. In [67], an equation based nonlinearity model for power amplifiers is developed. The authors argue that digital pre-distortion is the best way to deal with PA non-linearity. AM-AM distortion manifests itself in RF devices as compressed gain at high input power levels and hence are considerably less challenging to measure. It can be measured by placing a power detector at the PA output and measuring the output power level while sweeping the power of the input sine test signal. However, accurate measurement of AM-PM effects requires high precision instrumentation and is expensive and time consuming. The most common form of AM-PM distortion measurement is through use of a Vector Network Analyzer (VNA). The measured phase of the S21 parameter in the swept-power S parameter measurement provides AM-PM distortion information for the amplifier. Besides cost and time (setup time and calibration time) considerations in this particular setup, the measurement is

highly sensitive to proper calibration. Hence, low cost test method for measuring AM-AM and AM-PM is desired for production testing solutions. Analog Devices AD8302 [68] could be used to measure gain and phase measurements between two signals. This requires several stages of log amplifiers, phase detectors, subtractors, etc. and a complete feedback loop for stability. Apart from using significant amount of hardware the biggest drawback of this design is that it cannot distinguish between positive or negative phase shifts. In [70], authors develop an AM-AM and AM-PM method using unequal two tones. Another interesting test technique to measure AM-AM and AM-PM simultaneously could be found in [71] using active load pull. However, this technique and most of the other techniques found in literature do not provide a low-cost measurement solution. In this paper w*e concentrate on developing a truly low cost AM-AM and AM-PM measurement technique using only sine waves as test signals.*

3.1.3. AM-AM & AM-PM and its Effect on Communication Systems

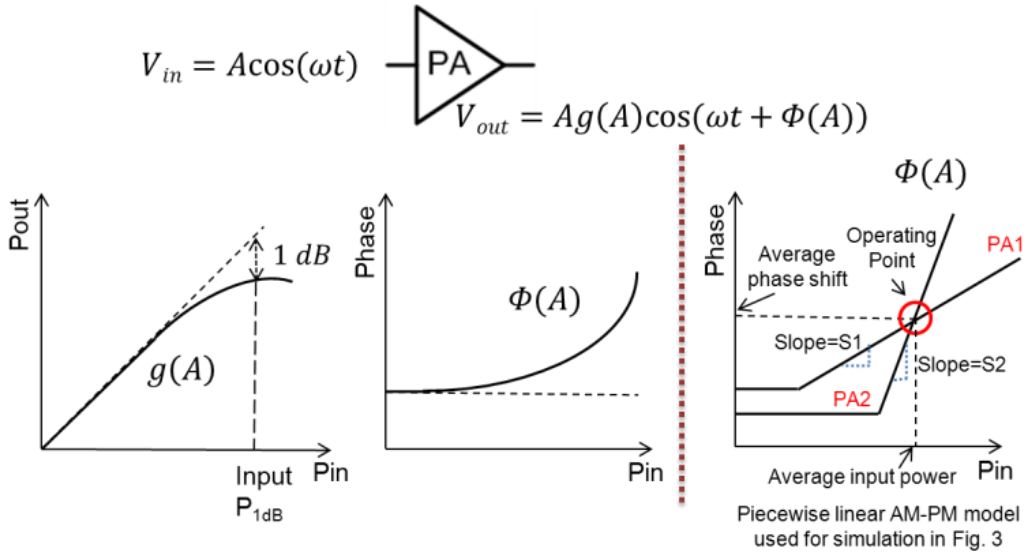


Figure 11: Gain Compression and Phase deviation [73]

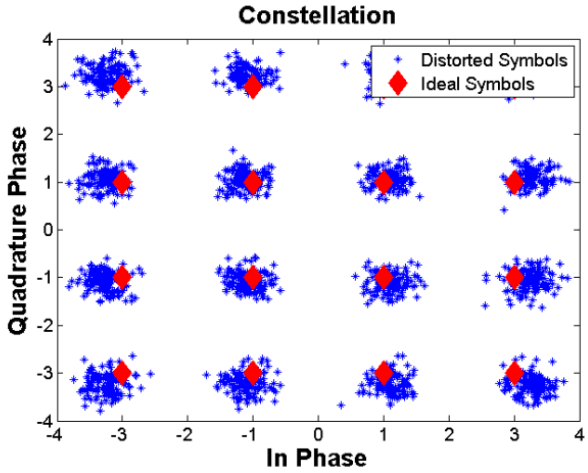


Figure 12: Effect of AM-AM on 16 QAM OFDM: it spreads the received constellation depending on the gain compression

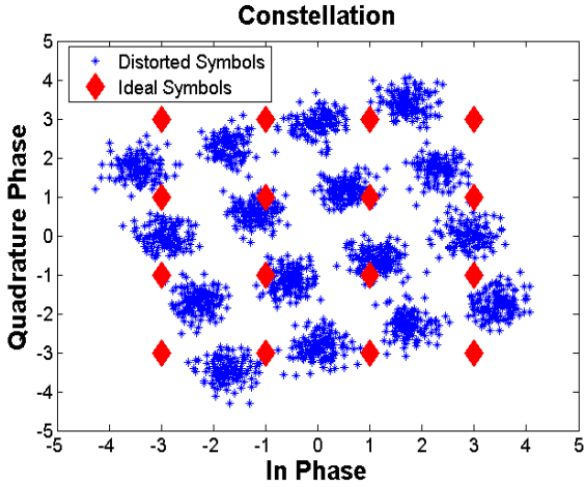


Figure 13: Effect of frequency independent AM-PM on 16 QAM OFDM: it rotates and spreads the received constellation; the rotation depends on the average power (refer Figure 11) whereas the spread depends on the slope of phase deviation curve at the operating point (S1 vs. S2 in Figure 11)

An RF Power Amplifier is the most power hungry block in a wireless transceiver. The important parameters that define the performance of an RF Power Amplifier (RF PA) are gain, phase deviation, 1-dB compression point, amplitude-to-amplitude distortion

(AM-AM distortion) and amplitude-to-phase distortion (AM-to-PM distortion) as defined in [74][75]. RF power amplifiers (PAs) are large signal devices that exhibit non-linear effects with increasing input power. The reduction of gain with increasing input power is known as *gain compression* and the change in phase is known as phase distortion.

AM-AM distortion is defined as the change in gain per dB increase of input power and characterized by dB/dB. Similarly AM-PM is defined as the phase change per dB increase of input power and is expressed in degrees/dB. With an input of $Acos(\omega t)$ the output of a PA can be written as $V_{out} = Ag(A)\cos\big(\omega t + \emptyset(A)\big)$ [73] where $g(A)$ represents gain compression and $\emptyset(A)$ represents the phase deviation with increasing input power (refer Figure 11).

The effect of AM-AM on a 16 QAM OFDM signal is shown in Figure 12 with the PA exited into 3dB of saturation. The results are obtained using a transceiver system simulation with the only non-ideality being gain compression of the PA. The effect of AM-AM is to spread the constellation leading to higher probability of a received symbol being misclassified as a wrong one, increasing the bit error rate (BER). From a frequency domain perspective, AM-AM distortion causes intermodulation distortion (IMD) resulting in the folding of the out of band signal onto the desired signal spectrum, thereby resulting in higher bit error rate.

AM-PM distortion or phase distortion causes unequal amplitude dependent rotation in the received constellation causing difficulties in signal detection. The effect of only frequency independent AM-PM non-ideality on a 16 QAM OFDM signal is shown in Figure 13. A piecewise linear simulation model is used for the AM-PM distortion as shown in Figure 11. The distortion is comprised of two parts: rotations of the centers of

masses of the received symbols and spread around the centers of masses. The *rotation* depends on the difference between the average power of the signal and the input power at which AM-PM effect first kicks in (refer Figure 11), for the given amplifier. It is to be noted that this rotation depends on the average power of the signal and hence is harder to compensate for if the average output power of the PA keeps on changing due to transmit power control requirements. The *spread* depends around the rotated centers of masses depends on the slope of the phase deviation curve (AM-PM) at the average operating point (S1 or S2 in Figure 11). For the same phase shift at the given input average power the average rotation for PA1 and PA2 would be same, whereas use of PA2 would result in higher spread as it has a higher slope (S2>S1) around the average operating point. Both the rotation and spread could cause the received symbol to be decoded improperly, increasing BER. Apart from increasing BER AM-AM and AM-PM effects also cause out of band emissions in the transmitted signal leading to violation of the defined FCC transmit spectral mask.

3.2. Low Cost Testing for Phase Distortion

In this section the methodology for low cost AM-PM distortion testing in Power Amplifiers are described.

3.2.1. Phase to Amplitude Transformation: Basics

Key Observation: *The difference of two sine waves with identical amplitude and frequency but different phase is another sine wave with the same frequency whose amplitude is proportional to the phase difference of the two sine waves.*

Let us consider two sine waves of frequency ω, amplitude A and ϕ phase difference. V_{diff} is the difference between the two waveforms. Assuming both of them as *cosine* waves we get (as in [76])

$$V_{diff} = A\cos(\omega t) - A\cos(\omega t + \phi) = 2A\sin(\phi/2) \times \sin(\omega t + \phi/2) \quad (7)$$

Similarly for *sine* waves it can be shown that

$$V_{diff} = A\sin(\omega t) - A\sin(\omega t + \phi) = -2A\sin(\phi/2) \times \cos(\omega t + \phi/2) \quad (8)$$

In both the cases, it is found that

$$|V_{diff}| = 2A\sin(\phi/2) \quad (9)$$

i.e. the amplitude of the difference of the two waves is dependent on the phase difference of the original waveforms, more accurately, is proportional to the *sin( )* of half of the phase difference between them. Figure 14 shows this observation in graphical form. Figure 14a shows a sine wave with zero phase and four other sine waves with increasing phase shift (ϕ=-10, -30,-60 and -90). Figure 14b shows the difference between the zero phase signal and the four signals with different phase values. As derived in Equation (8), the difference between the waveforms is a cosine wave with same frequency, $\phi/2$ phase delay (evident from the delayed zero crossing) and an amplitude given by $-2A\sin(\phi/2)$ (since ϕ is negative, this term is positive).

This fact can be used to simplify phase measurements by converting any phase distortion to proportional amplitude change and measuring it. This allows low cost implementations of phase measurements as amplitude measurements tend to be much cheaper than phase measurements. This work describes how this *Phase to Amplitude*

Conversion (PAC) can be used to facilitate low cost measurement of AM-AM and AM-PM distortions in RF Power Amplifiers.

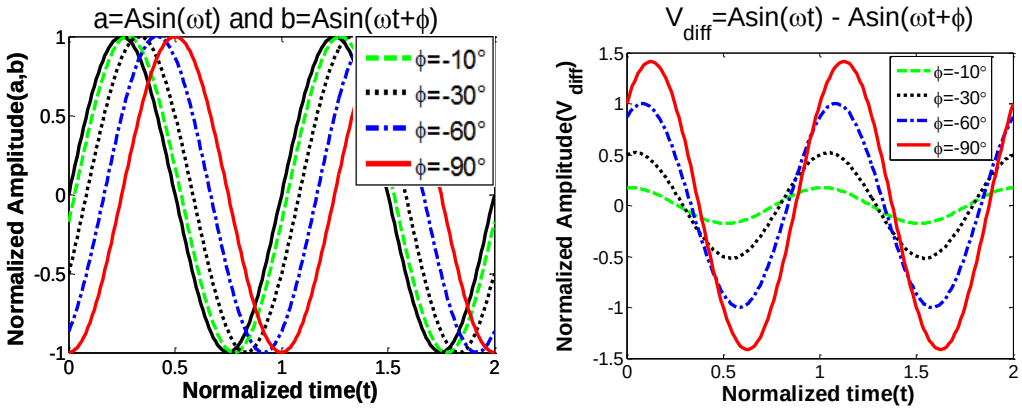


Figure 14: a) $A\sin(\omega t)$ and $A\sin(\omega t+\phi)$ for different ϕ. b) Difference wave showing amplitude proportional to the phase difference of the two waves in a).

3.2.2. AM-AM & AM-PM Measurement Using Phase to Amplitude Conversion

Traditional RF power amplifiers have a power detector (PD) at the output of the amplifier. Using this PD, low-cost measurement of gain compression is fairly straightforward. However, AM-PM distortion effects with increasing output power levels are difficult to measure accurately without a VNA. This section addresses this problem by developing a low cost phase distortion measurement technique using phase to amplitude conversion (PAC). *The key innovation is to first calibrate the AM-AM distortion effect "out" of the AM-PM distortion measurement procedure, then map the AM-PM distortion into amplitude variations of a "difference" signal and measure the amplitude using peak detection*. Once the peak value of the "difference" signal is determined, the underlying AM-PM distortion of the RF PA device under test can be easily calculated. This technique comprises only of peak detection and difference

generation operations making it amenable to very lost implementation. This work is targeted towards *one shot* low cost measurement of continuous wave (CW) AM-AM and AM-PM effects in RF PA, as found in commercial PA datasheets, without the use of costly VNA.

Traditional Measurement Techniques

AM-AM and AM-PM can be determined from gain and phase deviation measurements obtained by sweeping the PA input power across a range of values and observing the PA output. The most common form of this measurement is performed using a vector network analyzer (VNA) using a swept Scattering Parameter measurement, where the magnitude and phase component of S21 (forward transmission co-efficient) provides gain compression and phase deviation information with input power. AM-AM and AM-PM is calculated from this data by taking the difference between successive data points. This measurement includes the following steps:

1) Calibration of the VNA for the measurement setup.
2) Measurement of gain vs. input power.
3) Measurement of phase deviation vs. input power.

The VNA provides an integrated method of obtaining the amplitude and phase distortion information but uses very sophisticated hardware inside it and hence tend to be very costly.

Measurement using Phase to Amplitude Conversion

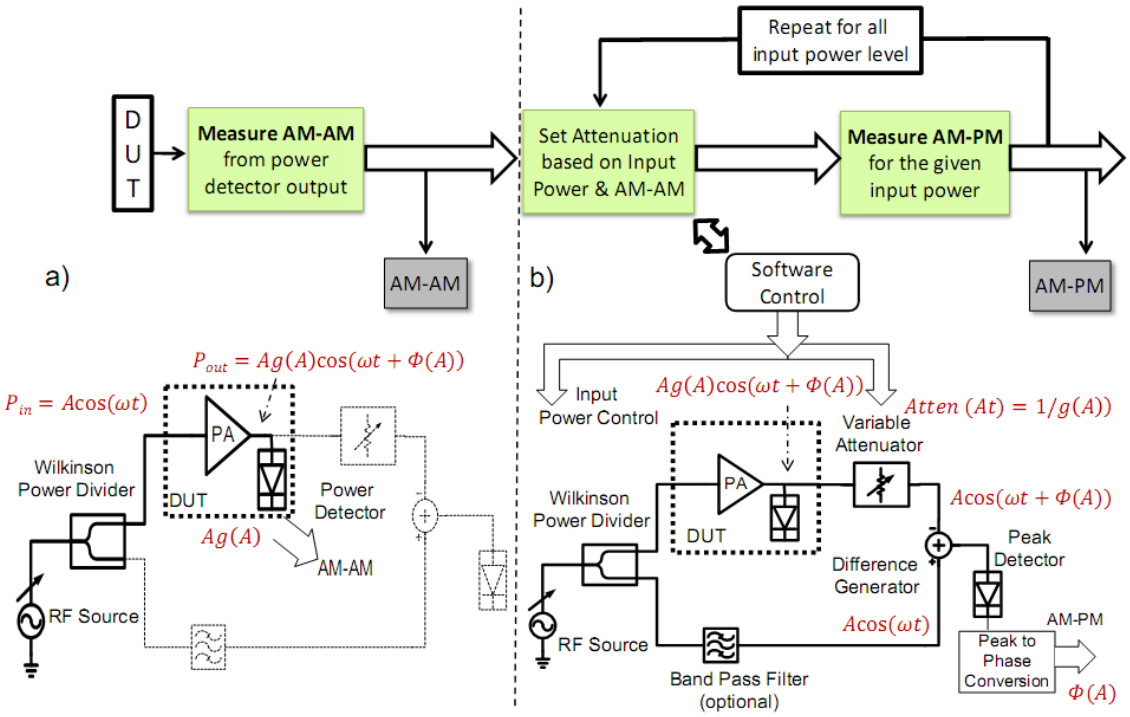


Figure 15: Block diagram two step measurement technique utilizing PAC and using RF difference generator

Figure 15 shows the test setup for the low cost test technique. Figure 15a and b show the setup for AM-AM and AM-PM distortion measurement, respectively. There are two steps in the test procedure. Step 1 measures the Gain and AM-AM distortion effects of the PA. Step 2 uses data from Step 1 to measure the AM-PM distortion of the PA. These are described below.

Step 1: A controllable output power RF signal source is used to generate the RF sinusoidal input signal (Figure 15a). A Wilkinson Power Divider (WPD) splits this signal into two signals with equal output power, i.e. $A\cos(\omega t)$. One signal is used to drive the

RF PA input and the other signal is used as a reference for distortion measurement. Commercial PAs (e.g. MAX 2242 [77]) generally have a power detector at the output. This can be used to measure the PA output power across different input power levels. The difference between the output and input power (with the drop due to WPD accounted for) provides $g(A)$, i.e. gain at lower power levels and gain compression (hence AM-AM) at higher power levels.

Step 2: Figure 15b shows the AM-PM distortion measurement setup. The reference signal derived from the power divider output should be as "clean" as possible. If the *reverse isolation* of the power divider is not very high the reference signal contains unwanted noise and therefore careful attention should be paid to the reverse isolation spec of the power divider. An optional band pass filter (BPF) at the RF test frequency can be used for generating a clean reference as shown in Figure 15. A variable attenuator is used at the output of the PA to equalize the power of the reference and the attenuated output. For each input power value a software actuated control mechanism sets this attenuation value (*At*) as per the gain and AM-AM distortion values measured in Step 1, i.e. as per equation 4:

$$At = 1/g(A) \tag{10}$$

In case a BPF is used, its input-to-output power loss is used to modify the attenuation values of the attenuator so that the correct "difference" signal is produced at the output of the test setup. The variable attenuator ensures that the power of both the attenuated PA output and the reference is the same for all input power levels, thereby removing the AM-AM distortion effects. These two signals are then passed through a difference generator circuit (described later) which produces the difference signal

$V_{diff} = A\cos(\omega t) - A\cos(\omega t + \phi)$ as per Equation (7). Finally, a peak detector measures $|V_{diff}|$ from which the phase shift ϕ using Equation (11) derived from Equation (9), for each power level concerned is obtained.

$$\phi = \sin^{-1}(|V_{diff}|/2A) \tag{11}$$

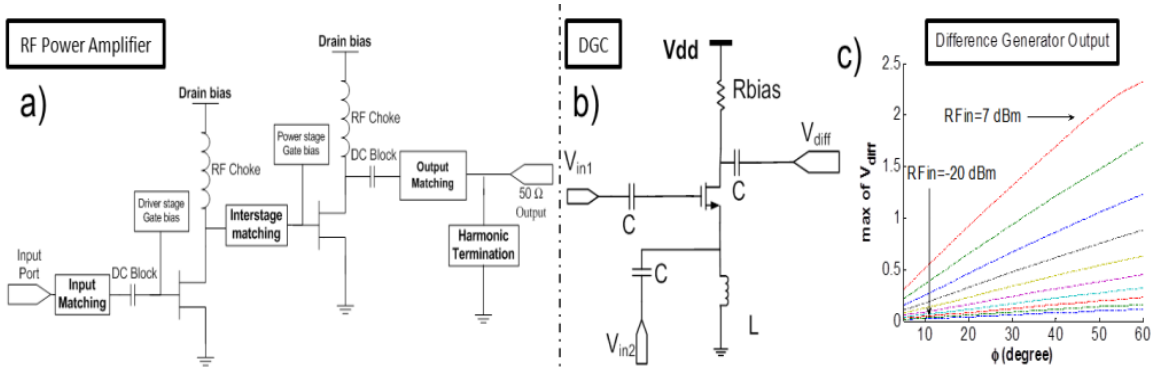


Figure 16: a) Schematic of Power Amplifier used for this work b) Schematic of RF difference generator circuit c) DGC output increases with increasing ϕ

The variable attenuation and the difference generator circuits are the key modules used. As described earlier, for $|V_{diff}|$ to be truly due to the phase shift introduced by AM-PM distortion, it is important that both the signals that are compared have the same amplitude. If this is not the case, $|V_{diff}|$ will be a function of the amplitude mismatch between the two signals and hence phase distortion prediction will be inaccurate. However, since the actual attenuation required is given by the gain specification at different input power levels (obtained in Step 1), the same can be controlled accurately by software. The difference generator circuit needs to be linear across the range of input signal power concerned. Any nonlinearity in this circuit can be characterized and the test procedure can be calibrated to achieve correct phase distortion measurement.

RF Power Amplifier

A two stage RF PA has been designed using CMOS 0.35u technology for simulation purposes. The simplified schematic for this PA is shown in Figure 16a. An input matching is provided before the driver stage so that maximum power could be transferred from the signal source. The driver stage was designed to provide a gain of around 13 dB whereas the power stage was designed to deliver a gain of around 9 dB at 2.4GHz. The driver stage and the power stage were connected through an inter-stage matching network of band pass type. Output matching is provided to match the output to 50 ohm. A harmonic termination network at the output provides good suppression at harmonic frequencies. The complete PA is designed from a 3.3V supply to have a gain of 19.6 dB, output 1 dB compression point (P1dB) of 25.5 dBm and Power Added Efficiency (PAE) greater than 40%. The input P1dB of the PA is around 6 dBm (25.5-19.6=5.9).

Difference Generator Circuit (DGC)

The most critical non-standard block in this method is a difference generator circuit that generates the difference between two input RF signals of identical frequency. Hence the challenge is to design a difference amplifier with the following properties:

1) The output is proportional to the difference of the two input signals.
2) The difference generator should have wide bandwidth as both inputs and outputs are of RF frequency.
3) It should be as linear as possible for the input range concerned.

A simplified schematic of the implementation of such a difference generator circuit is shown in Figure 16b. A resistive loaded common source amplifier is used for this

purpose. DC biasing is provided through inductors (L) at both gate and source, whereas the RF input signals are AC coupled through capacitors(C). R_{bias} sets the current through the device as well as the gain. The AC coupled output is equal to V_{diff} as per Equation (8) if the inputs are given by $V_{in1} = A\sin(\omega t)$ and $V_{in2} = A\sin(\omega t + \phi)$. The gain (G) of the circuit would add a scaling factor to V_{diff} which is accounted for by modifying (9) as:

$$\phi = \sin^{-1}(|V_{diff}|/2AG) \tag{12}$$

The RF input port (V_{in1}) is matched to 50 ohm to match the PA output impedance. The other input port (V_{in2}) is a high impedance input which samples the signal from a 50 ohm termination on the reference signal path. The output voltage is proportional to the phase difference between the two inputs as can be seen from Figure 16c. It shows $|V_{diff}|$ with ϕ for several values of the input power concerned. It also shows that the design behaves very linearly from RF power levels from -20 dBm to 7 dBm for phase shifts up to even 60 degrees. For smaller phase shift values it is linear even at higher input power levels.

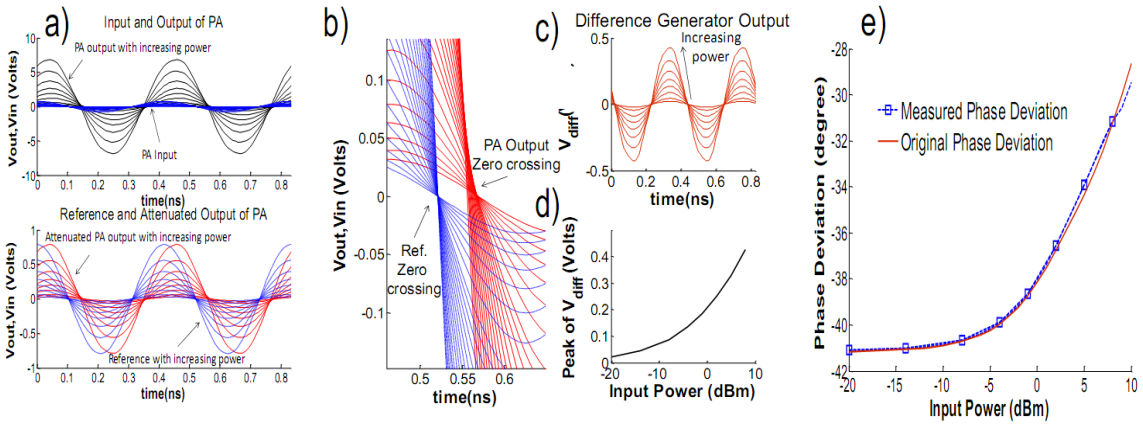


Figure 17: a) Original PA output and Reference, normalized PA out and reference b) Zoomed in version of fig a, showing phase distortion in RF out c) difference waveform d) peak detector output e) Original and measured phase deviation.

Simulation Results

Figure 17a (top) shows the reference (equal to the PA input) and PA output for different input power levels. The difference in the power levels is due to the gain of PA. It also shows (bottom) the attenuated PA output and the reference for several input power levels. It can be seen that the AM-AM effects have been removed accurately and the attenuated output and the reference have same amplitude for all the input power levels. If a constant attenuation (equal to the linear gain of the PA) were used then the PA output would have been lesser in amplitude than the reference for higher input power due to gain compression.

Zoomed in version of Figure 17a at zero crossing is shown in Figure 17b. Zero crossing of the reference remains same for all input powers as expected. The difference in zero crossing is equivalent to the phase difference between the two waves. It is interesting to note that the changing zero crossing of the attenuated PA output reflects the actual phase distortion occurring in the PA as amplitude increases. This shows that the phase distortion is present before difference generation and hence we expect this to reflect in V_{diff}. Figure 17c and d show V_{diff} (difference generator output) and $|V_{diff}|$ (peak detector output) for increasing input power levels. In Figure 17a, the original two signals are $\cos(\omega t)$ and $\cos(\omega t + \phi)$ with ϕ negative. The difference signal in Figure 17c is $\sin(\omega t + \phi/2)$ supporting Equation (7). The amplitude of this difference signal is given by Equation (9). Hence using Equation (11), we get the phase deviation plot of Figure 17e. The actual phase deviation obtained from circuit level simulation in Agilent ADS is plotted for comparison purposes. The measurement has an rms error of only ***0.18%*** over the total input power range.

The AM-AM distortion measured and the AM-PM distortion derived from phase measurements are plotted in Figure 18. The AM-PM measurement shows rms error of only ***5.8 %***.

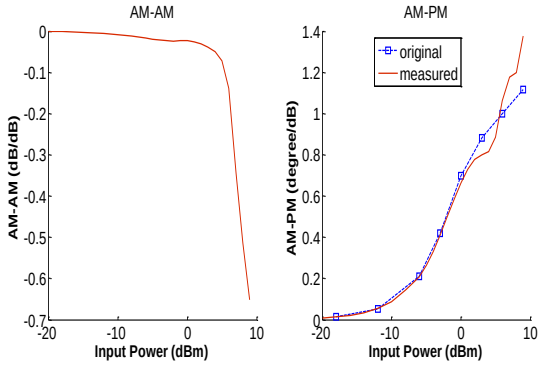


Figure 18: a) Measured AM-AM and Measured and actual AM-PM

3.2.3. Single Setup AM-AM & AM-PM Measurement

We have seen how phase distortion can be converted to amplitude for easy low cost measurement purposes and how a simple measurement setup allows accurate AM-AM and AM-PM measurements. Here we extend this concept to a ***single setup*** low cost AM-AM and AM-PM measurement using some more hardware than required by the previous technique. However, it doesn't require a high frequency difference generator, a variable attenuator or a power detector making it less prone to the non-linearity effects of the above. Using down conversion and sampling of the high frequency signals this implementation performs the amplitude equalization and difference generation in software.

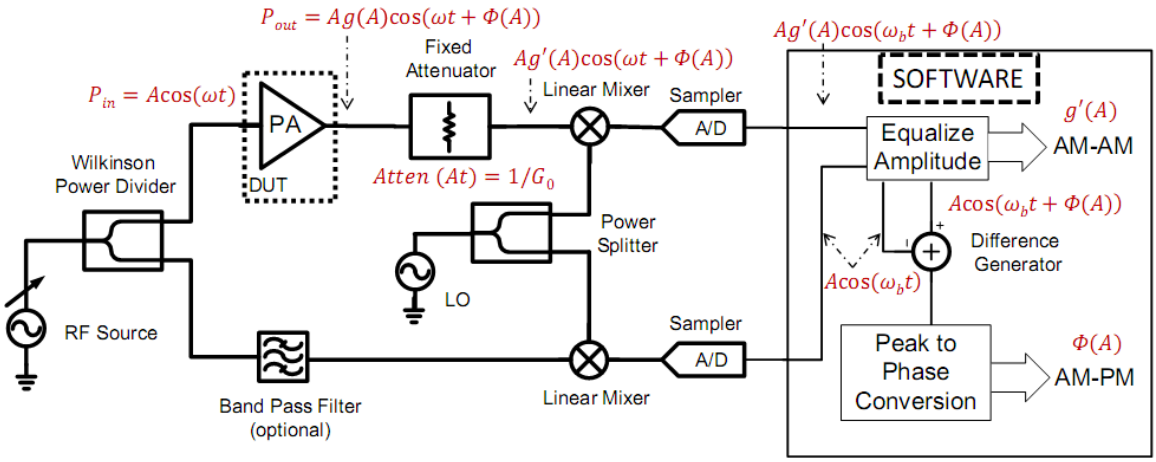


Figure 19: Block diagram of one shot AM-AM and AM-PM measurement setup using down conversion and sampling

Measurement Setup and Methodology

Figure 19 shows the block diagram of the measurement setup. A variable output power RF source is used to generate the input signal. It is then divided into two equal parts using a Wilkinson power divider, one of which is used as the PA input whereas the other is used as reference signal. The reference signal derived from the power divider output should be as "clean" as possible. If the *reverse isolation* of the power divider is not very high the reference signal contains distortion. An optional band pass filter (BPF) at the RF test frequency can be used for generating a clean reference.

A *fixed attenuator* with attenuation equal to the nominal linear gain of the PA is used. This allows both the attenuated PA output and reference to be at similar power levels, allowing the following mixers to operate with similar linearity requirements, but does not remove AM-AM distortion effect from the attenuated output. Two matched linear down conversion mixers are used to down convert both the attenuated PA output and the reference to low frequency signals (50 MHz in our case). A single RF source is used as the Local Oscillator (LO) signal of both the mixers by dividing it using a power splitter

(WPD). Two matched analog-to-digital converters (ADCs) are used to sample these signals. The method requires only one capture in the two ADCs for a given input power. The captured signals are processed as described below.

The sampled signals have the same frequency but their amplitude and phase differ at higher power levels due to gain compression and phase deviation. The amplitude equalizer block performs the following operations:

1. Equalize the amplitude of the down converted PA output and reference for the lowest input power level. Since at lower input power, the PA does not exhibit gain compression and the attenuator attenuates by the same amount (linear gain of a nominal PA) ideally there should not be any amplitude difference between the two signals being compared. Any amplitude mismatch at this input power level reflects the amplitude mismatch in both the signal paths (path of reference signal, path of signal through DUT) arising from the presence of a non-nominal PA (G_{offset}), non-exact attenuation, non-matched mixers and ADCs ($G_{mismatch}$) . This mismatch is constant across all power levels and hence, if any mismatch exists, down converted PA outputs for all input power levels are equalized for the respective amount of power gain or loss (G_{offset} + $G_{mismatch}$). This removes any amplitude mismatch arising from all effects except gain compression. After this step, the downconverted signals corresponding to lower input power levels for which the PA does not exhibit gain compression have equal amplitudes with the corresponding reference signal.

2. There is still residual amplitude differences present between the two signals being compared for higher input power levels *due to AM-AM distortion effects*. In this step these are equalized digitally and as a by-product, the amount of the equalization at each

power level corresponds to the gain compression at that input power value. Hence, the outputs of the 'Equalize Amplitude' block are two signals with no amplitude difference (phase difference still preserved) and the gain compression information of the PA over all power levels. The gain of the PA can be written as:

$$\textbf{\textit{Gain of PA}} = G_0 + G_{offset} + G_{compression} \quad (13)$$

Where,

$At = 1/\,g(A)\big|_{linear\_region} = 1/G_0$ = Attenuation of fixed attenuator, G_0= linear gain of nominal PA.

G_{offset} = Power equalization amount in step 1, if there is no mismatch (in dB, gain difference due to non-nominal PA, constant for all power levels). In presence of mismatches in the two paths, $G_{mismatch}$ can be found using *one-time calibration* for the setup that need not be repeated for every device. The calibration is only needed if the absolute value of gain is desired for each power level in presence of mismatch. If only the gain compression is desired, no calibration is needed as step 1 compensates for both G_{offset} and $G_{mismatch}$.

$G_{compression}$ = Power equalization amount in step 2 (in dB, different for different power levels in the compression region).

The mathematical description of the system is shown below (also refer Figure 19). The attenuator has attenuation (*At*) equal to the inverse of the nominal gain of the *nominal PA*. The output of the attenuator has a signal whose amplitude is only dependent on the AM-AM. This formula assumes that the mixers and ADCs are properly matched or mismatch is calibrated out. The effect of mismatch is studied later. The two sampled signals can be represented by Equation (14) and (15). Gain compression is found by taking the ratio of

the peaks of these signals as shown in Equation (16).

$$g'(A) = g(A) / G_0$$

$$V_{BB\_PAout} = Ag'(A)\cos(\omega_b t + \Phi(A)) \quad (14)$$

$$V_{BB\_ref} = A\cos(\omega_b t) \quad (15)$$

$$G_{compression} = |V_{BB\_PAout}| / |V_{BB\_ref}| \quad (16)$$

Next, two amplitude equalized outputs from the 'Equalize Amplitude' block are passed through a difference generator that produces the difference signal V_{diff}. It is important that both the signals that are compared have the same amplitude to ensure $|V_{diff}|$ is only due to the phase shift introduced by AM-PM distortion.

$$V_{diff} = A\cos(\omega_b t + \emptyset(A)) - A\cos(\omega_b t) \quad (17)$$

$$Phase\ Deviation = \emptyset = \sin^{-1}|V_{diff}/2A| \quad (18)$$

The peak of the difference signal $|V_{diff}|$ is proportional to the sine of the phase difference of the two input signals as described in sub-ection 3.2.1. Application of Equation (18) in the 'Peak to Phase Conversion' block, provides the phase deviation and hence AM-PM between the signals being compared at all any given input power level.

The method used here utilizes the fact [79][80][81] that phase deviation is preserved by frequency translation and provides accurate phase information as long as the mixers are operating in the linear range of input power concerned. Another issue is the amount of attenuation to be programmed in the "fixed" attenuator. We suggest it should be set to be the same as the linear expected gain of the PA DUT (in dBs). In case the attenuation is not exact, Step 1 of the procedure outlined earlier for operation of the 'Equalize Amplitude' block compensates for any subsequent amplitude mismatch effects. The main

purpose of this attenuator is to ensure that both the signals being compared are in the same power range so that the dynamic range requirements of components of devices in both the reference signal and DUT signal paths are the same and hence, matched mixers and ADCs can be used.

Results

This subsection describes the simulation results. A 2.4 GHz simple sine wave is used as the test stimulus along with a 2.45 GHz LO. The down converted signals are of 50 MHz as can be observed from Figure 20. This plot shows the signals after step 1 in the 'Equalize Amplitude' block in Figure 19.

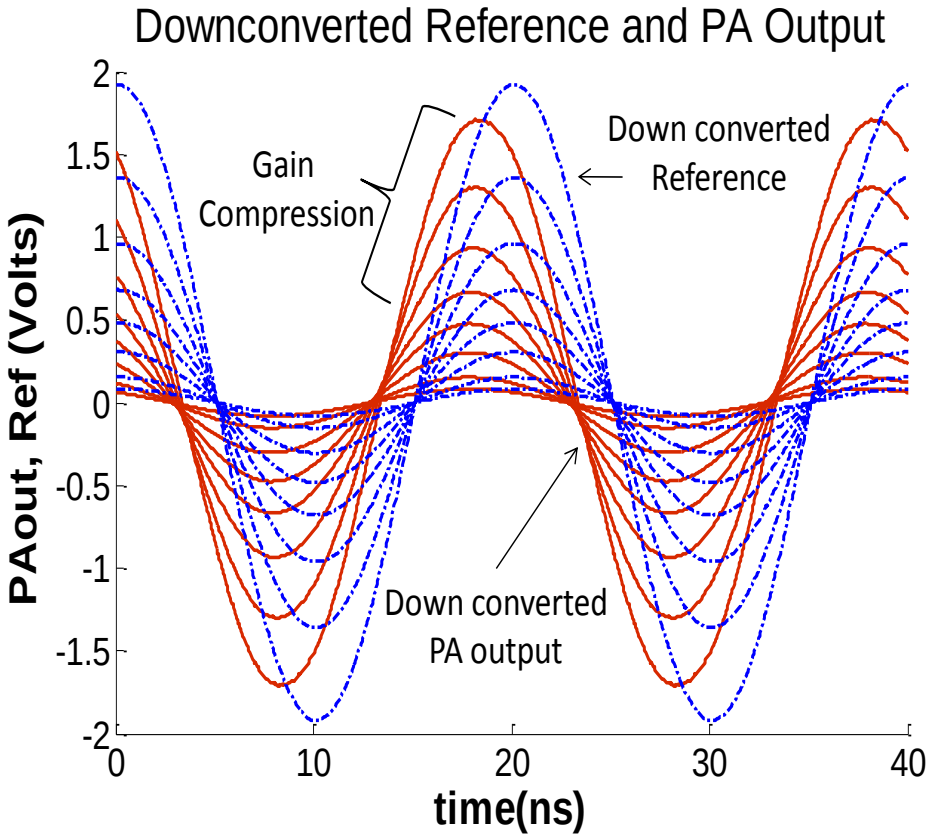


Figure 20: Down converted PA output and reference

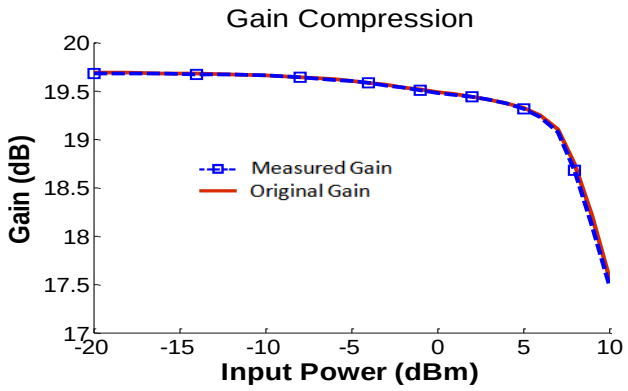


Figure 21: Gain compression: original and measured

The output has same amplitude as the reference for lower power levels, whereas, for higher powers it exhibits gain compression as pointed out in the figure above. This lets us measure AM-AM in step 2 as described earlier. In Figure 21, the measured gain values using Equation (7) are plotted along with the original gain values obtained from circuit level simulation in Agilent ADS over the input power range concerned. The gain measurement turns out be very accurate with only 0.03% rms error over all power levels.

Zoomed in version of the Figure 20 is shown in Figure 22a. Zero crossing of the reference remains same for all input powers as expected. The difference in zero crossing is equivalent to the phase difference between the two waves. It is important to note that the changing zero crossing of the attenuated PA output reflects the actual phase distortion occurring in the PA as amplitude increases. This shows that the phase distortion is present before difference generation and hence we should expect the phase distortion to reflect in V_{diff}. Figure 22b and c show V_{diff} (difference generator output) and $|V_{diff}|$ (peak detector output), respectively, for increasing input power levels. The amplitude of this difference signal is given by Equation (8). Hence using Equation (9), we get the measured phase deviation as shown in of Figure 23 along with the actual phase deviation. The measurement has an rms error of only 0.22% over the total input power range.

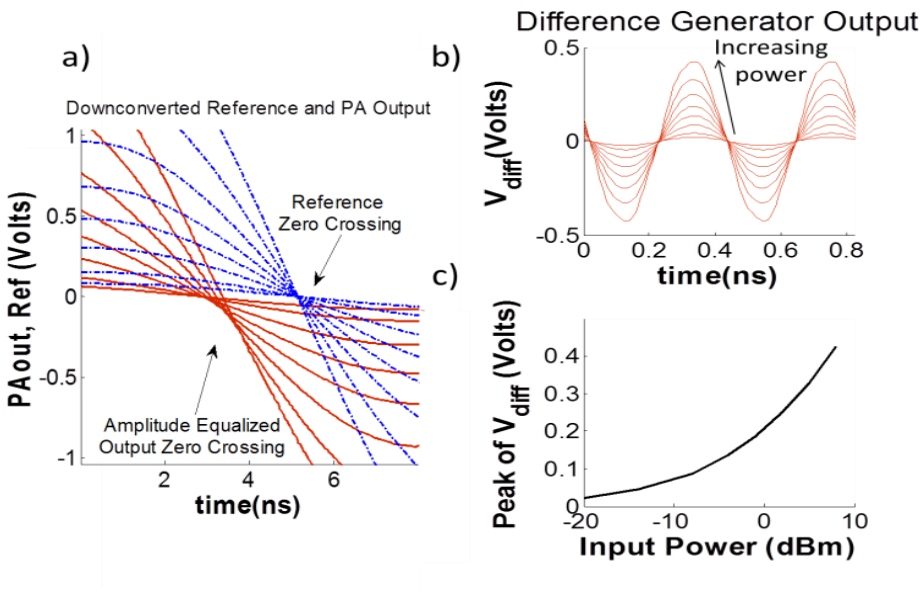


Figure 22: a) Zoomed in version signal and reference, showing the effect of phase distortion in RF out zero crossings b) difference waveform c) peak detector output.

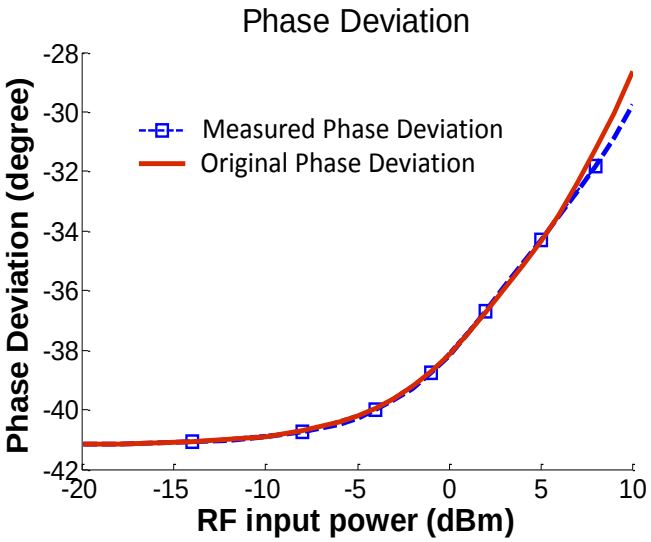


Figure 23: Phase deviation: Original and measured

A gilbert cell mixer with source degeneration and single to differential end conversion was used as the down conversion mixer for simulation purposes. This mixer had an input 1 dB compression point of 5dBm, i.e. the mixer was not linear enough. The slight deviation of the measured phase from actual at higher power levels is due to the

compression of the mixer at these power levels. With a more linear mixer (which is readily available as off the shelf component) measurement accuracy would further increase. Another point to note is the output leads the reference in phase in Figure 24. This is caused as both the down conversion mixers are inverting. But this does not affect measurement accuracy.

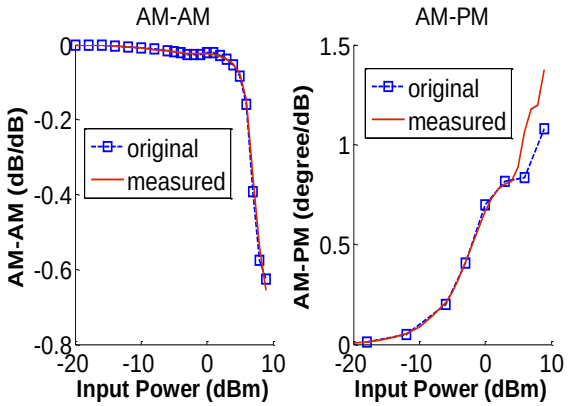


Figure 24: a) Measured AM-AM b) Measured and actual AM-PM

The AM-AM and AM-PM derived from the measurements above are plotted in Figure 24 along with their actual values. They exhibit an rms measurement error of 1% and 4.74% respectively.

Considerations

Since the method relies on subtraction of two signals coming from two matched paths, the effects of gain/phase mismatch should be studied carefully. Any phase mismatch directly affects the phase measurement and hence needs to be calibrated as in a VNA. Since the low-cost method measures phase by converting it to amplitude, it is interesting to analyze the effects of any gain mismatch in both paths on phase measurement. Any gain mismatch would directly affect the gain value for that instant.

However, if the mismatch remains constant with increasing power it's taken out and doesn't affect the AM-AM measurement. In case there is unequal amplitude equalization for gain mismatch the input of the difference generator is then given as follows:

$$\left|V_{in-}\right| = \left|A\cos(\omega t)\right| \neq \left|At \times Ag\left(A\right)\cos(\omega t + \Phi(A))\right| = \left|V_{in+}\right| \quad (19)$$

which introduces some error in phase measurement performed using Equation (9) as both the inputs differ in amplitude. Figure 25a shows how phase measurement gets affected with -10% to +10% gain mismatch. The ***rms error*** in phase measurement with gain mismatch is shown in Figure 25b. Figure 25c shows the ***maximum*** measurement error in phase with gain error in dB form the nominal value. 10% of gain mismatch introduces around 6% error in worst case. For a gain mismatch of 1 dB the maximum phase error is within 3.1 degrees from a nominal of 41.1 degrees. For realistic gain mismatches (<0.4 dB) the *maximum* phase error is within 1 degrees and *rms error* is within 2.3%. This mismatch is the amount of gain mismatch equalization error and not the absolute gain mismatch in the paths, as the absolute mismatch is taken out in step 1. Also, it is important to note that the minimum error does not occur at zero mismatch, as the deviation due to mixer non-linearity (as shown in Figure 25) results in higher overall rms error compared to -1% gain mismatch. This can be calibrated out by input power dependent non-linear calibration or use of a highly linear mixer (done in the experimental validation section) as a part of the setup.

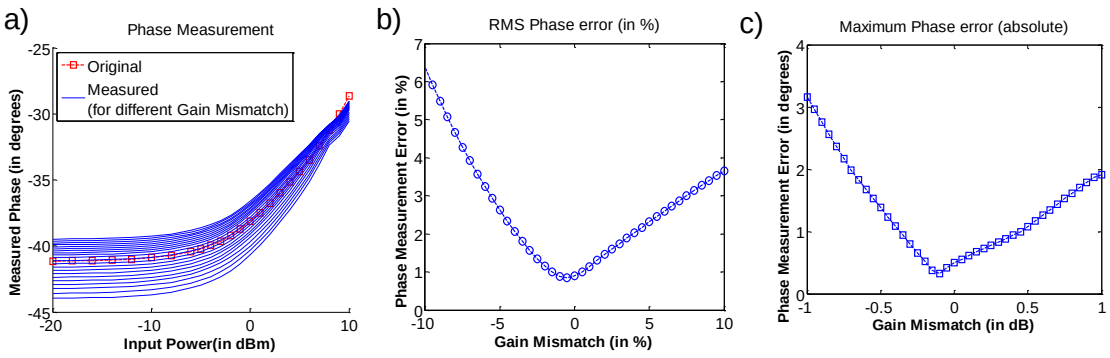


Figure 25: a) Actual and measured Phase deviation with different amount of errors in compensation for gain mismatch b) RMS Phase error with Gain mismatch in % c) Absolute Maximum Phase measurement error (in degree) with Gain Mismatch in dB.

Characterization of the technique under Different Process

Since we use fixed attenuator whose attenuation is equal to the gain of the nominal PA (G_0) the down converted PA output and down converted reference would be different in amplitude for any non-nominal PA whose gain in the linear region is not equal to G_0. The gain difference due to process could be found out by comparing the difference in signal amplitudes in the linear region. This is done as follows:

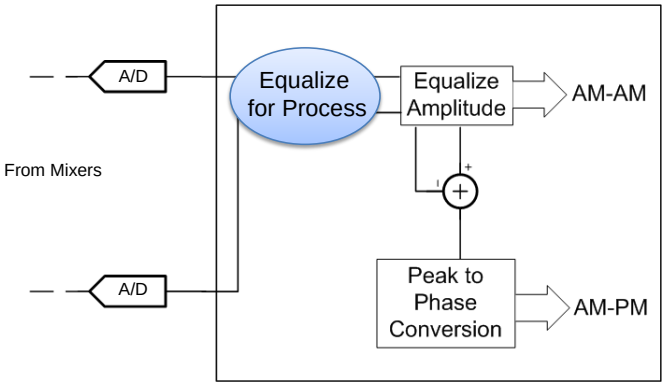


Figure 26: Gain adjustment for Process variation

1. In the calibration phase, a golden PA with nominal gain is used and the setup is calibrated for any gain mismatches in the two paths, arising from non-matched test

circuitry. This is one-time measurement for the test setup.

2. During testing, first the mismatches in amplitude in both paths are logged for lowest values of input power. This provides the gain deviation due to the non-nominal PA.
3. This value from step is equalized for all the other measurements in different power levels for the same PA in the "*Equalize for Process*" block (Figure 26).

Monte Carlo simulation in Agilent Advanced Design System is performed on the designed PA with Gaussian variation on threshold voltage (V_t), oxide thickness (t_{ox}), drain inductors, matching inductors (L) and capacitors (C). The gain compression and phase deviation is noted for 6 instances.

The low-cost measurement technique is also applied to each instance to find out the AM-AM and AM-PM. The gain compression and phase deviation using the low-cost method and the original (from Agilent ADS) is plotted in Figure 27a and b respectively, for 6 (PID 0 to PID 5) instances showing the accuracy of the method under process variation. The corresponding AM-AM and AM-PM variations for these 6 instances are shown in Figure 28. Comparative results show that the method holds over several process instances.

Until now, a low cost AM-PM test methodology has been developed that uses phase to amplitude conversion to perform low cost testing, using simple *off-the-shelve* hardware and a simple signal processor. While this is not the main subject of the paper, an overview of how this scheme might be implemented without the use of a signal processor, is described in the appendix for the sake of completeness.

This technique also uses variable output power sine wave stimulus generator to measure AM-PM at different input power values. In the next section, we extend this

technique by using the core ideas developed in this section while generating the power sweep using a single amplitude modulated (AM) modulated stimulus.

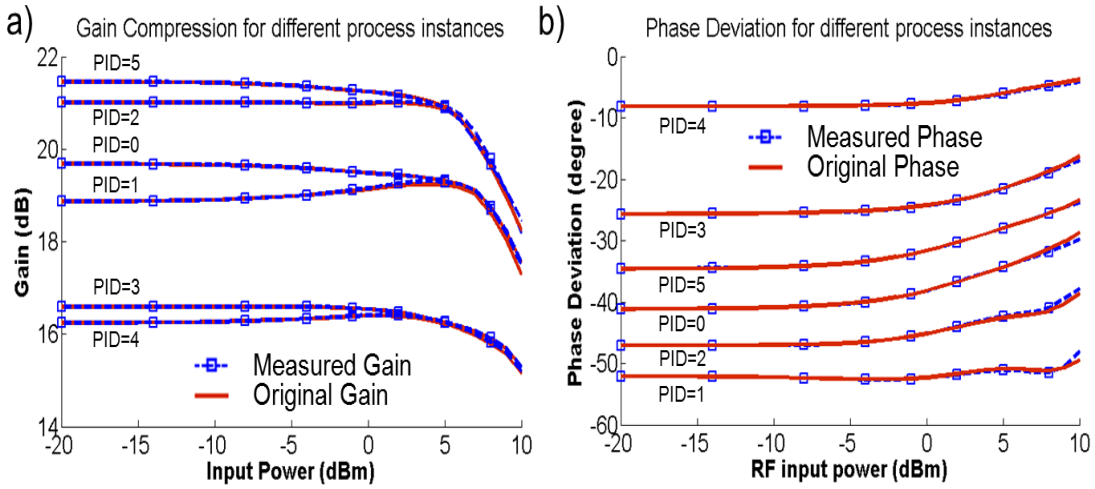


Figure 27: a) Gain Compression b) Phase deviation for different process instances

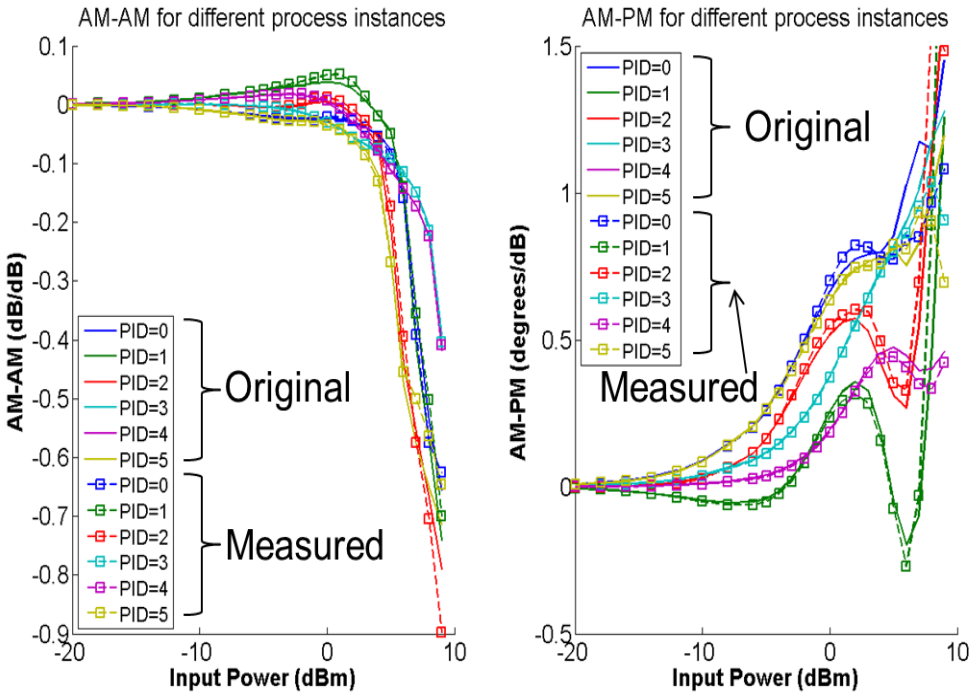


Figure 28: AM-AM and AM-PM measured and original over 6 process instances

3.2.4. Experimental Validation

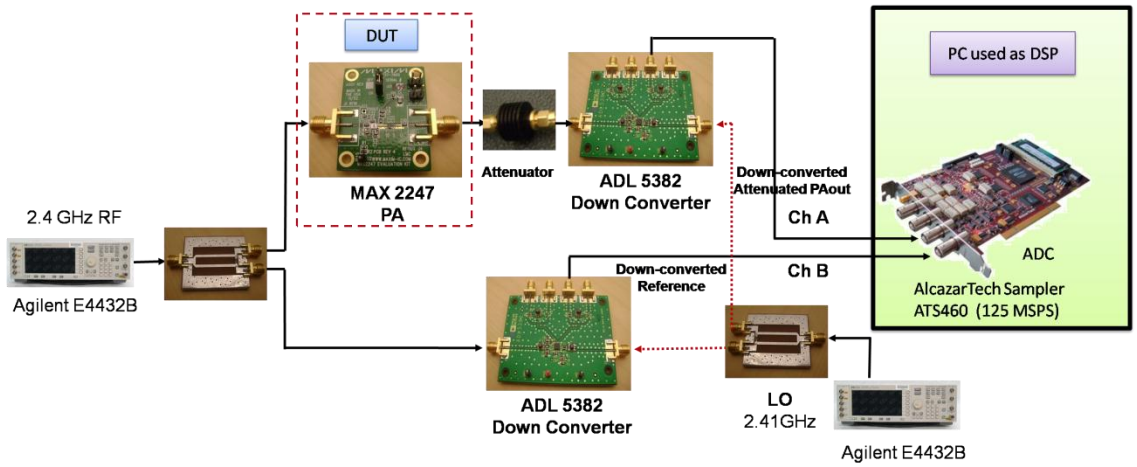


Figure 29: Single setup measurement setup of AM-AM and AM-PM on MAX 2247 WLAN High Power Amplifier (HPA)

This section describes hardware implementation of the low cost AM-AM and AM-PM measurement methodology using Phase to Amplitude Conversion by applying it on two DUTs, namely a high power WLAN PA MAX2247 and an amplifier RF2411. The technique has also been verified over process variation (mimicked by varying the supply voltage). Results for measurement using AM stimulus is also shown.

The test setup is shown in Figure 29. The device under test (DUT) is a 2.4 GHz WLAN SiGe Linear Power Amplifier from MAXIM. It has 29 dB power gain operating from a 3.3 V supply voltage. The variable power RF input from Agilent E4432B (signal generator) is divided in two equal parts using a custom designed WPD. One output is passed through the DUT and attenuated (fixed attenuation) before feeding to one of the two matched mixers. The other WPD output goes directly to the other mixer and acts as a reference. Analog Devices ADL 5382 is used to downconvert both attenuated PA output and the reference signal to 10 MHz baseband signals for low cost sampling purposes. Both the LOs are derived from the same RF signal generator using a Wilkinson power

divider. This allows the sampled signals to be synchronized. Two channels (Ch. A and Ch. B in Figure 29) of an ATS460 sampler is used to sample the downconverted signals at 125Msps (lower sampling speeds also work fine as long as the peaks of the sine waves are captured properly).

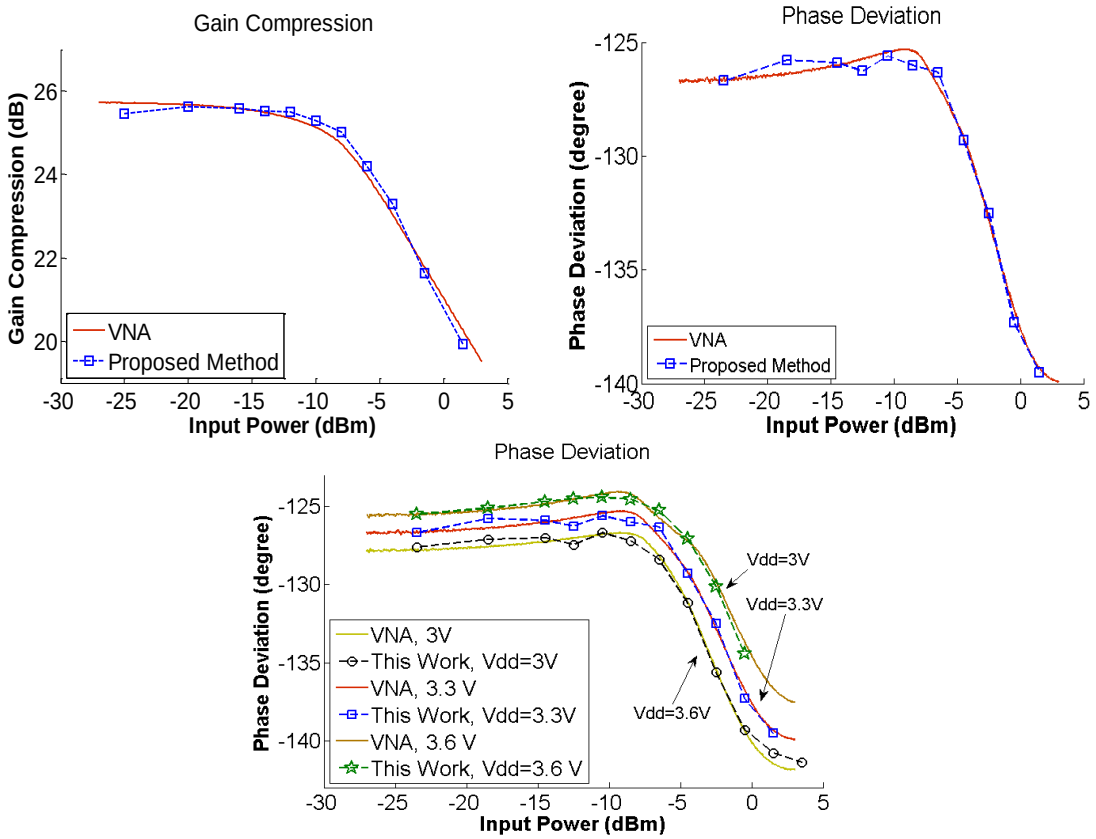


Figure 30: Measurement using low cost method and VNA a) Gain Compression and b) Phase deviation measurement for MAX 2247 HPA for nominal instance c) Phase deviation for 3 supply voltages of the PA

The sampled signals are first amplitude equalized to find AM-AM and then subtracted to convert the phase difference to amplitude and is measured to find AM-PM. The nominal results are shown in Figure 30a and b with the actual gain and phase distortion measurements from a VNA. Figure 30c shows that the variations in phase deviation are tracked closely using the low-cost methodology over supply voltage

variations of the PA. Figure 31a and b shows the performance of the low-cost method for two process instances of the PA, both at nominal supply. The gain compression and phase deviation measurements on a low power amplifier DUT RF2411 is shown in Figure 31c and d. All the measurements exhibit rms error less than 3% proving the applicability of the low cost test technique over different devices, variations and also using AM test stimulus.

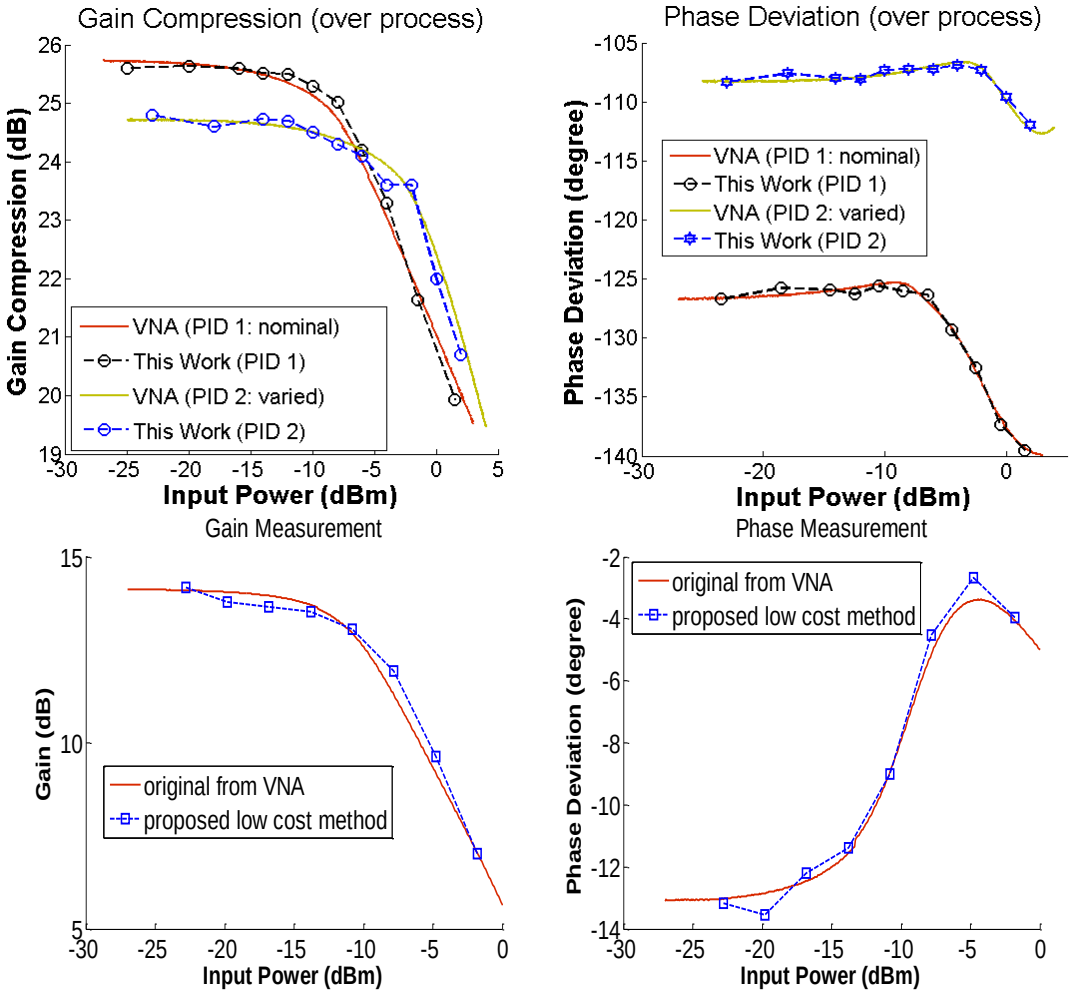


Figure 31: Measurement using low cost method and VNA for a) Gain Compression and b) Phase deviation for 2 process instances (nominal and varied) of MAX 2247 PA and c) Gain Compression and d) Phase deviation for RF2411 Amplifier

3.3. Amplitude and Phase Distortion from Single Data Acquisition

In this section the concept presented in the previous section is extended to perform AM-PM testing from single amplitude modulated (AM) stimulus.

3.3.1. AM-AM and AM-PM from AM Stimulus

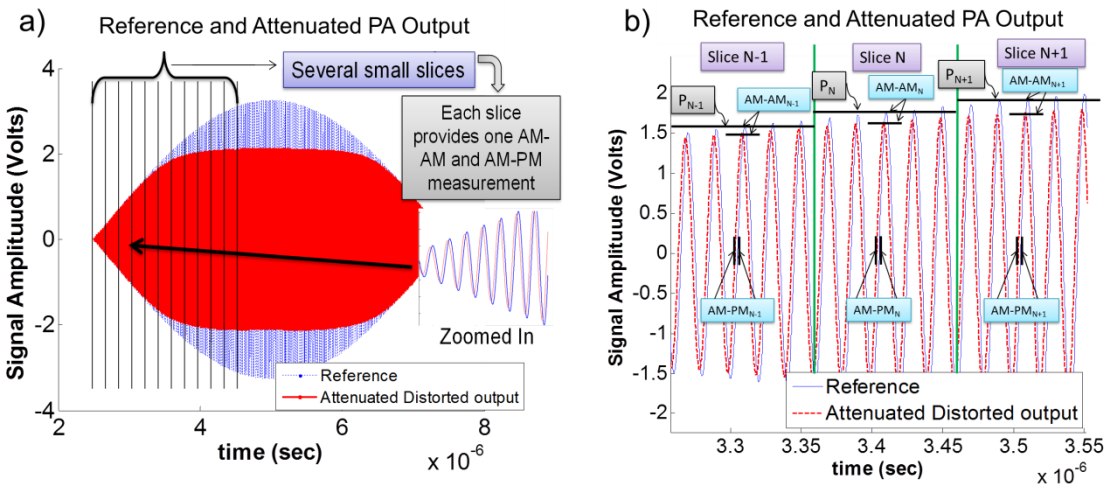


Figure 32: a) One Cycle of down converted PA_{out} and Reference b) Expanded view of a) showing 3 slices having 5 cycles each. The average power of each cycle is taken as the power of that slice. The AM-AM and AM-PM provides a data point on the complete distortion curve at the average power level.

In this section we propose using a modulated test stimulus for determining the complete gain compression and phase distortion information for different input power levels from a *single test without the requirement of any power sweep*. If the modulated sine wave has enough amplitude to drive the PA into the non-linear region as shown in Figure 32a, the PA goes through both small and large signal RF input levels during the complete envelope. Figure 32a and b show the down-converted envelope of the input (reference) and the attenuated PA output (the reason for attenuation w described in next

section). The RF input and PA outputs are down-converted to an intermediate frequency (IF) so that it can be sampled by a low cost ADC and processed in a DSP. The method developed in this section uses the fact that *phase deviation and hence phase distortion is preserved by frequency translation* [79][80].

At the start of the low frequency envelope since the amplitudes of the RF cycles are small the PA does not exhibit significant gain compression and phase distortion. With increasing amplitude of the envelope these effects start to become prominent. It is evident that for higher amplitude of the envelope the PA exhibits significant AM-AM and AM-PM distortion. Hence the complete information about gain compression and phase deviation for each power level is present in these two waveforms. We propose dividing these waveforms into several small slices as shown in Figure 32a. Each slice contains several RF cycles (at least one). The ratio of the average amplitude of the output to the average amplitude of the reference within each slice is the gain compression at the average input power of the slice. Similarly the phase difference within that slice is found by subtracting these two signals and applying Equation (9) on a slice by slice basis. Repeating this over "rising" half of the envelope provides the gain compression and phase deviation values for different input power levels, the number of data points being equal to number of slices used. Such a procedure avoids the use of multiple phase distortion measurements at different input power levels as in [56].

This methodology is described in details in Figure 32b, which shows the expanded view of Figure 32a. Let us consider three slices namely, the N^{th} slice and two slice on each side ($N-1^{th}$ slice and $N+1^{th}$ slice). For the case shown each slice contains 5 cycles of the downconverted waveform. Since,

$$f_{mod} \ll f_{BB} \tag{20}$$

i.e.,f_{mod} the modulating frequency is much slower than f_{BB}, the down converted baseband frequency. Hence the change in envelope within a slice is very small, allowing us to approximate the power of the slice as the average power. So the powers of these 3 slices are P_{N-1}, P_N and P_{N+1} respectively. The AM-AM distortion at power P_N is given by the difference in amplitude of the reference waveform and the attenuated distorted output. Similarly, the phase distortion at P_N the phase deviation among the two above mentioned waveforms within slice N. As P_N increases more and more distortion is observed. This is as shown below:

$$\mathrm{AM} - \mathrm{AM}_N = \frac{|Attenuated\ Distorted\ output|}{|Reference|}\Bigg|_{Slice_N} \tag{21}$$

$$V_{diff} = Reference - \frac{Attenuated\ Distorted\ output}{\mathrm{AM} - \mathrm{AM}_N} \tag{22}$$

$$\mathrm{AM} - \mathrm{PM}_N = \emptyset_N = \sin^{-1}\frac{|V_{diff}|}{2|Reference|} \tag{23}$$

Equation (21) provides AM-AM values at power P_N. The difference waveform V_{diff} is obtained by equalizing for the AM-AM values for that power level in the DSP (Equation (22)). The amplitude of V_{diff} is proportional to the sin of the phase deviation. Hence Equation (23) provides the AM-PM at power P_N. Repeating this over all slices in the rising half of the envelope provides the complete amplitude and phase distortion characteristic for the Device Under Test (DUT) over all power levels. The specification of the device is calculated as follows:

$$Gain = AM - AM|_{N=1} + Attenuation \tag{24}$$

$$Gain\ Compression = AM - AM + Attenuation \tag{25}$$

$$IIP3 = \sqrt{\left|\frac{4}{3}\frac{\alpha_1}{\alpha_3}\right|} \tag{26}$$

Where α_1 and α_3 are the non-linearity coefficients of the Gain Compression curve. In this work we focus on showing how AM-AM and AM-PM is obtained from a single-tone AM stimulus. Other specifications of the device can be calculated as above.

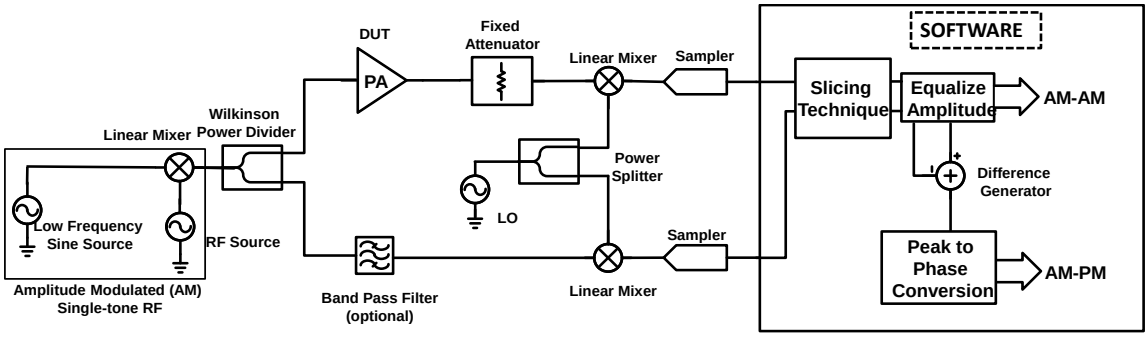


Figure 33: Amplitude and Phase Distortion measurement setup

3.3.2. Implementation

The test setup is shown in Figure 33. A low frequency sine wave source is used to generate the envelope signal which is upconverted to the required RF frequency using an upconversion mixer. The modulated signal is then divided into two equal parts using a Wilkinson power divider (WPD), one of which is used as the PA input whereas the other is used as a reference signal. A fixed attenuator with attenuation equal to the nominal linear gain of the PA is used, which allows both the attenuated PA output and reference to be at similar power levels, but does not remove AM-AM distortion effect from the attenuated output. Two matched linear down conversion mixers are used to down-convert both the attenuated PA output and the reference to intermediate frequency signals (50 MHz). A single RF source is used as the Local Oscillator (LO) signal of both the mixers by dividing it using the power divider. Two matched analog-to-digital converters (ADCs)

are used to sample these signals. The sampled signals have both gain compression and phase distortion information over the full cycle of the low frequency envelope. The following steps are performed to extract this information.

(1) The captured signals are divided into several time-slices as described above each containing at least one cycle of the IF frequency.

(2) The amplitude difference of the reference and attenuated output for the first slice are equalized using a fixed attenuator. Since the signal levels used in this calibration step are low, the PA is in the linear region and any difference is due to the specific gain characteristics of the PA device being tested. This factor provides the linear gain of the DUT using the difference measured and the known attenuation. All the slices are equalized with this constant factor.

Next, for each slice:

(3) The difference between the reference and attenuated PA output provides the gain compression.

(4) Gain compression is equalized out and the signals are subtracted. Using Equation (16), we get the phase deviation for each cycle.

The choice of number of slices is governed by the following equations:

$$Tot\_cycles = f_{BB}/f_{mod} \tag{27}$$

$$N_{slices} = Tot\_cycles/Cyc\_per\_slice \tag{28}$$

Tot_cycles is defined by the modulating frequency and the down converted baseband frequency. N_{slices} provides the total number of data points on the AM-AM and AM-PM curve and can be increased by reducing Cyc_per_sclice. In the following results

we have used Cyc_per_slice.as 5. The only requirement of the input single-tone AM stimulus is that its amplitude should be high enough so that the PA exhibits compression within the envelope.

Simulation Results

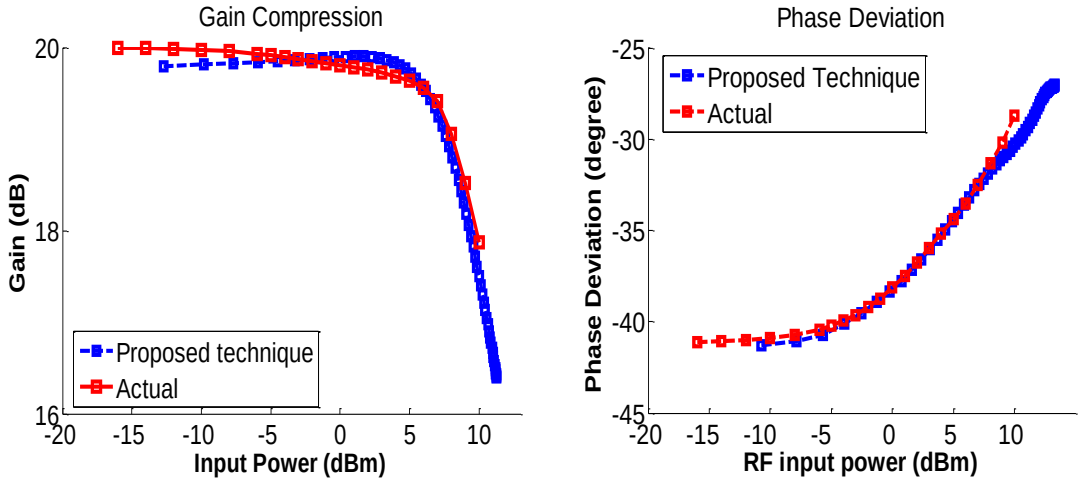


Figure 34: Gain Compression and Phase Deviation measurement

The measured gain compression and phase deviation using this low cost technique are plotted in Figure 34, along with the corresponding values, measured using a Vector Network Analyzer (VNA). Comparison of the results proves the validity of the low-cost test methodology. From this information, AM-AM and AM-PM distortion can be easily calculated by taking the difference of two consecutive values of gain and phase. Also the specifications of the PA can be calculated using the Equations (20)-(22).

3.3.3. Experimental Setup and Results

The hardware experiments performed to validate the low cost AM-AM and AM-PM testing using the baseband single-tone test i.e. amplitude modulated RF) and single data acquisition.

Experimental Setup

The setup shown in Figure 3 has been recreated in hardware as shown in Figure 35. The RF DUT is a Maxim 2.4 GHz Power Amplifier (MAX 2247). Instead of using an up-conversion mixer, an amplitude modulated two tone RF signal is sent as the RF input from an Agilent E4432B (signal generator). Due to the limitation of the E4432B module we used, only a 50 KHz modulation on top of a 2.4 GHz RF carrier was possible. This is equivalent to sending a 50 KHz sine wave, up converting it to RF using an up-conversion mixer. Tis single tone AM test input is divided in two equal parts using a Wilkinson Power Divider (not shown for simplicity). One input goes through the PA and the other is used as a reference. Two matched Analog devices Down-conversion mixer (ADL 5382) were used to down-convert the signal to baseband. The input signal power was kept high enough so that the DUT goes into compression. We use a constant 30 dB attenuator at the output of the PA to make sure the down-converter operates in the linear region. The modulated RF signals were down-converted to a 10 MHz baseband signal with 50 KHz modulation riding on it. Hence, f_{BB}=10 MHz, f_{mod}*=50KHz, Tot_cycles=200 and Cyc_per_slice* was used as 5. This was subsequently sampled by a two channel AlazarTech (ATS460) sampler ADC (sampling speed: 125 MSps). A computer (PC) was used as the software to perform the slicing algorithm. Applying Equation (17)-(19) on the sampled and sliced data on both channels the AM-AM and AM-PM is measured. This is compared with the amplitude and phase distortion measured using an Agilent E8363 PNA and the results are shown to have good agreement in the next subsection, providing validity of the *low cost AM stimulus* based distortion testing.

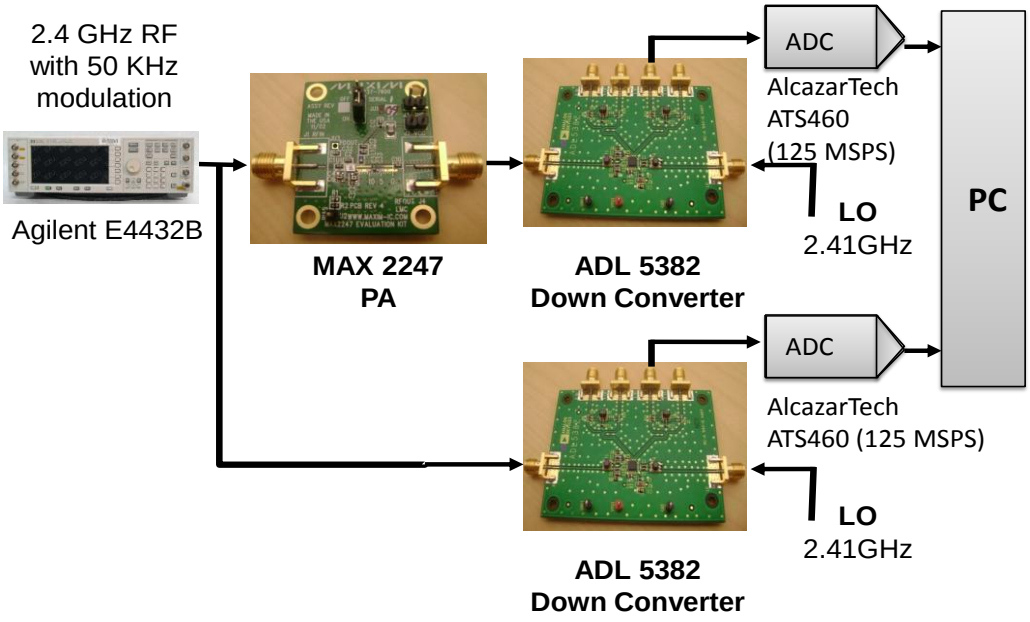


Figure 35: Experimental setup

Experimental Results

Figure 36a shows the Gain Compression obtained using AM stimulus based methodology and a standard VNA overlaid on top of each other for the Max 2247 DUT. Figure 36b shows the phase deviation over several power levels. VNA uses power sweep whereas the AM stimulus based technique does not use power sweep. It relies on the fact that an AM signal with sufficient amplitude sweeps the complete input power range of the DUT. The results show an absolute average error of 0.26 dB in Gain Compression and 0.42 degrees in Phase Deviation. This translates to an **RMS error of 1.4% and 0.43%** in Gain Compression and Phase Deviation, respectively.

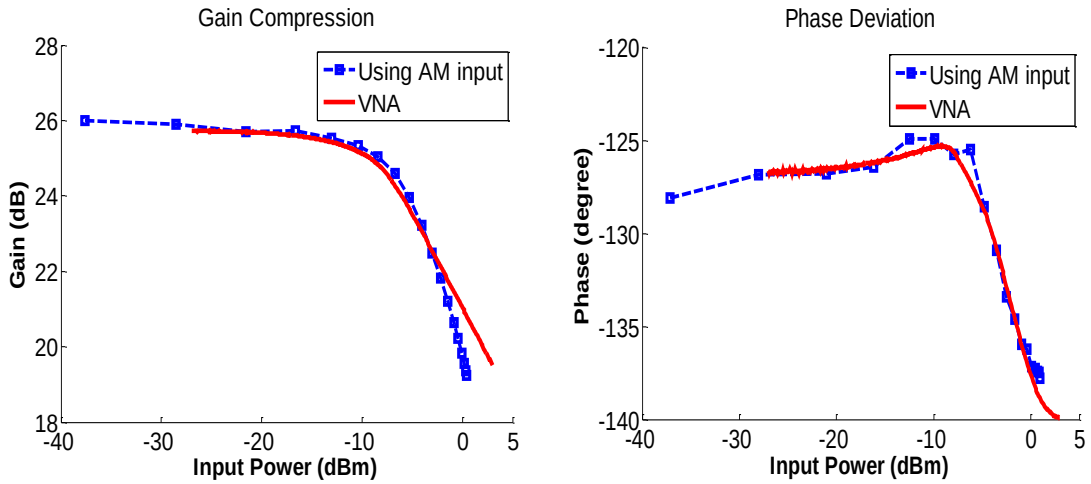


Figure 36: Comparison of a) Gain b) Phase deviation measured using single-tone AM stimulus without any power sweep and a standard VNA.

In summary, this work develops a rapid low cost test technique to compute multiple RF specifications as Gain, IIP3, AM-AM and AM-PM through single output capture *using a simple amplitude modulated single-tone test stimulus without any power sweep*. Compared to traditional RF tests it provides significant advantage of test time, cost and simplicity. It is for the first time that the test setup with same low complexity as an alternate test is used to test for the above mentioned specs without the need for *trainings* that is usually associated with a typical alternate test. Simulation and hardware results show accurate computation of the specifications.

3.3.4. Discussions about Low-Cost Phase Distortion Testing

The previous section and this section (Section 3.2 and 3.3) propose phase to amplitude conversion based methodology for low cost AM-AM and AM-PM measurement, which is traditionally done by costly VNAs. It uses 2 WPD, 2 mixers, 2 ADCs, and 2 RF sources. It uses one extra mixer and a low frequency source in case AM stimulus is used,

with the advantage of no power sweep and hence low test time. The benefits of the technique are as follows:

Test cost: Traditionally, AM-AM measurement is straight forward (using a power detector). However AM-PM measurement requires the use of a VNA, which typically costs anywhere between $40,000 to $100,000 or more. The test setup described above can be implemented with off the shelf components within about $1000 (assuming the signal generator is replaced with a PLL) and can be tested using simple RF signal generator, providing a significant test cost improvement using an *in house* test solution than using a VNA.

Test time: For measurement at each power point, at least 1 cycle of the low frequency waveform (10 MHz in hardware setup) is required. We used 5 cycles for robustness purposes. This means 5×0.1µs =0.5µs. This is multiplied by the number of power points we require per curve plus the sampling delay etc. Overall, it is as fast as a VNA can measure by sweeping its input power if automated power sweeping input is arranged. Using the AM stimulus based measurement it's can even be faster than the VNA as it uses an one shot method (only one output capture) and doesn't require any power sweep, as opposed to a VNA which sweeps the power and uses several output capture to measure the specifications.

Calibration: As in a VNA, this method also requires calibration. Due to the nature of the measurement technique specifically targeted towards AM-AM and AM-PM measurement it needs to only calibrate for gain and phase, instead of short circuit, open circuit and matched calibrations in case of a VNA. In this work, calibration is performed for each setup and part once, at one power level to characterize for the gain and phase

mismatches contributed by the setup. The DUT is replaced with a golden (known) PA and input is provided such that it is in the linear region. Both the down-converted channels are captured. Any gain and phase mismatch between the two captured signals provide the required calibration in both attenuation and phase shift (as the PA characteristics is known). These calibration coefficients are used for all other measurements including measurement for different process instances and for different supply voltages.

The reported results are obtained without calibration for *input power dependent non-linearity* of test circuitry, as the mixers and the following circuitry are operated in the linear region by attenuating the output of the PA, minimizing their error contributions. However, if *even higher accuracy is desired* this calibration can easily be integrated into the framework as the setup uses digital backend computation on analog measurement. A golden PA, with known nonlinearity characteristics, can be used in place of DUT. The input power is varied and the downconverted signals in both the paths are captured. Knowing the PA nonlinearity, it can be de-embedded from the captured amplitude and phase nonlinearity of each path. Finally, the de-embedded results are stored in the DSP in a look up table (LUT). During actual testing, the right correction function can be applied from the LUT based on the input power applied to the PA.

LO, Signal Source and DSP requirements: This AM-PM testing method can be incorporated easily with minimal changes in tester DSP. It has to perform the "equalize amplitude", "difference generation", "peak to phase conversion" operations along with the calibration. All of this consists of simple peak detection, multiplication and subtraction operations. The final $\sin^{-1}$ can be implemented as a function or a LUT. The

local oscillator's (LO) frequency should match that of the RF input frequency correctly. The signal generator should be capable to sweeping its output power for the same frequency. If frequency dependent AM-AM and AM-PM effects are to be studied the signal generator and LO frequency should be varied concurrently.

CW vs. modulated signal: It is to be noted that this test technique is targeted towards measurement of continuous wave (CW) AM-AM and AM-PM performance of an RF PA as found is commercially available PA datasheets, without using a VNA. The performance of the PA might slightly deviate under complex modulated (e.g., 16 QAM OFDM) signals. Though the correlation between the CW performance and complex stimulus performance is high, it varies depending on the signal characteristics and is still an active area of research. Further analysis of this phenomenon is beyond the scope of this paper.

Finally, the maximum phase measurement errors while using the two low-cost techniques are listed in Table 3 for different measurement cases. All the measurements exhibit rms error less than 3% proving the applicability of the low cost test technique over different devices, variations and also using AM test stimulus.

Table 3 Maximum error in phase deviation measurement over different experiments (in degrees)

<table>
<tr><td colspan="4">MAX 2247</td><td>RF2411</td></tr>
<tr><td colspan="2">With Supply</td><td colspan="2">With Process</td><td>Using AM stimulus</td><td>Power Sweep</td></tr>
<tr><td>Vdd</td><td>Phase Error</td><td>PID</td><td>Phase Error</td><td>Phase Error</td><td>Phase Error</td></tr>
<tr><td>3.6</td><td>0.5</td><td rowspan="2">1</td><td rowspan="2">0.6</td><td rowspan="3">1.9</td><td rowspan="3">0.7</td></tr>
<tr><td>3.3</td><td>0.6</td></tr>
<tr><td>3.0</td><td>0.8</td><td>2</td><td>0.7</td></tr>
</table>

3.4. IQ Mismatch Measurement and Compensation

In this section the idea presented in the previous sections is extended for low cost IQ mismatch measurement and compensation. The key contribution presented in this paper is a gain and phase imbalance measurement and compensation methodology using simple sine wave test stimuli and just a built in power detector.

In IQ transmitters by virtue of the quadrature up-conversion any phase mismatch in the carriers translates to the amplitude. This fact is exploited to measure both gain and phase mismatch in IQ transmitters using simple amplitude measurements through power detectors. The low-cost technique reduces the built in hardware requirement to a minimal power detector for DSP driven built in measurement and compensation of IQ imbalance. Any phase imbalance in the RF domain also holds in the baseband domain after down-conversion. Using this fact the IQ imbalance in RF receiver could be easily measured in the baseband just by using a high frequency one tone RF signal as the receiver input. The amplitude and phase difference of down converted and sampled I and Q signals provide a measure of the gain and phase imbalance in the receiver. This one tone signal is generated from the transmitter itself, eliminating the requirement of any extra hardware.

3.4.1. Transmitter IQ Imbalance Measurement

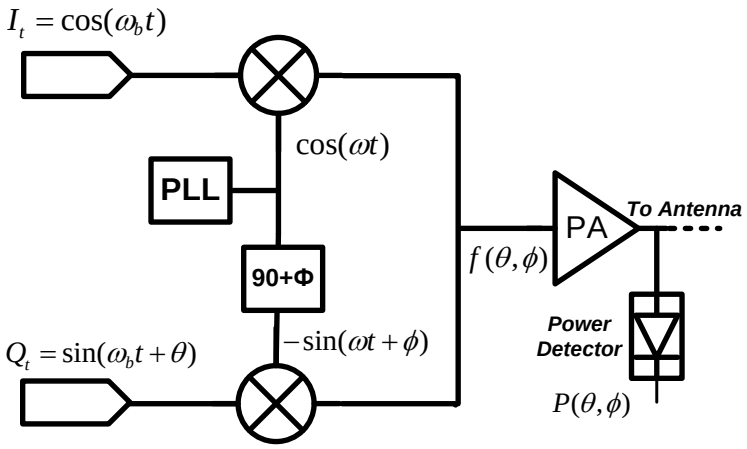


Figure 37: IQ transmitter system with envelope detector

The gain and phase mismatch in an IQ transmitter can be measured using the following two step procedure [82].

Step 1:

1a) Apply $I_t = Acos(\omega_b t)$ and $Q_t = 0$. $P = P_I$ 1b) Apply $I_t = 0$ and $Q_t = Acos(\omega_b t)$. $P = P_Q$

Gain Mismatch $G_{\_m} = \sqrt{P_I / P_Q}$

Step 2:

Apply $I_t = Acos(\omega_b t)$ and $Q_t = -G_{\_m} Acos(\omega_b t)$

and find phase difference could be found from the transmitter output as:

$$\phi = 2\left[\arcsin\left(\frac{|Tx\_out|}{|M|}\right) - 45\right] \quad (29)$$

The details of the derivation can be found in [82]. Figure 38 shows the measured and actual gain and phase mismatch, highlighting the accuracy of the low-cost method.

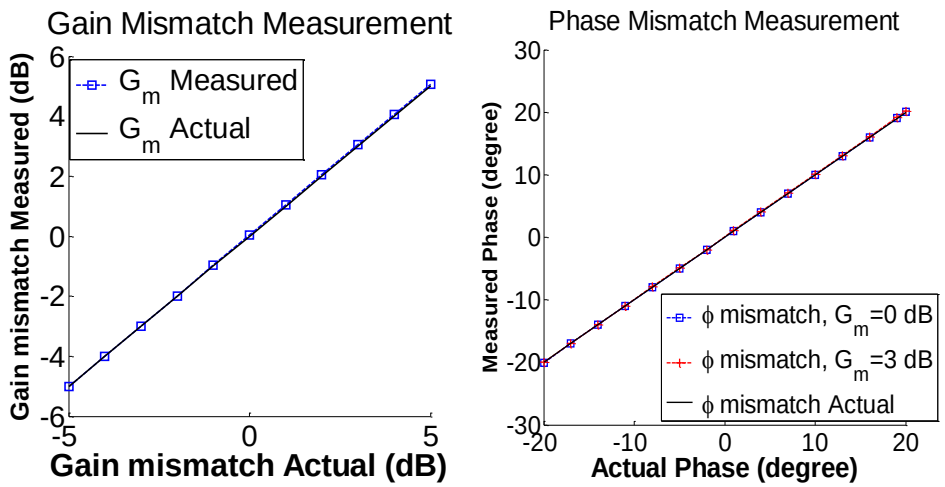


Figure 38: IQ transmitter a) Gain mismatch measurement b) Phase mismatch for two gain mismatches

3.4.2. Receiver IQ Imbalance Measurement

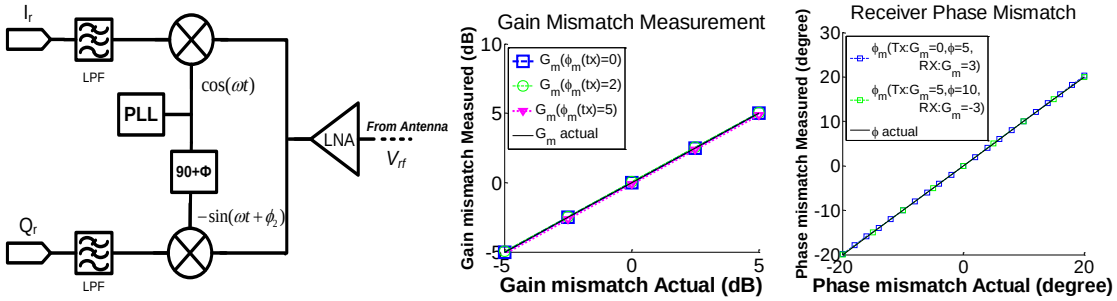


Figure 39: a) Receiver IQ imbalance b) Gain mismatch measurement for compensated and uncompensated transmitter c) Phase mismatch for two sets of compensated transmitter and receiver parameter

The IQ mismatch parameters of a receiver can also be found using a similar technique as that of the transmitter. They key idea here is to apply the baseband stimulus in the transmitter in a quadrature manner such that the transmitter output is a single tone. Applying this single tone in loopback mode, the received I and Q signal should have same amplitude and no phase difference if there is no mismatch present. Any gain

mismatch affects the relative amplitude and any phase mismatch affects the relative phase. This is used to measure the gain and phase imbalance using phase to amplitude conversion using methods described during phase distortion testing [82]. The results are shown in Figure 39.

3.4.3. DSP Assisted IQ Mismatch Compensation

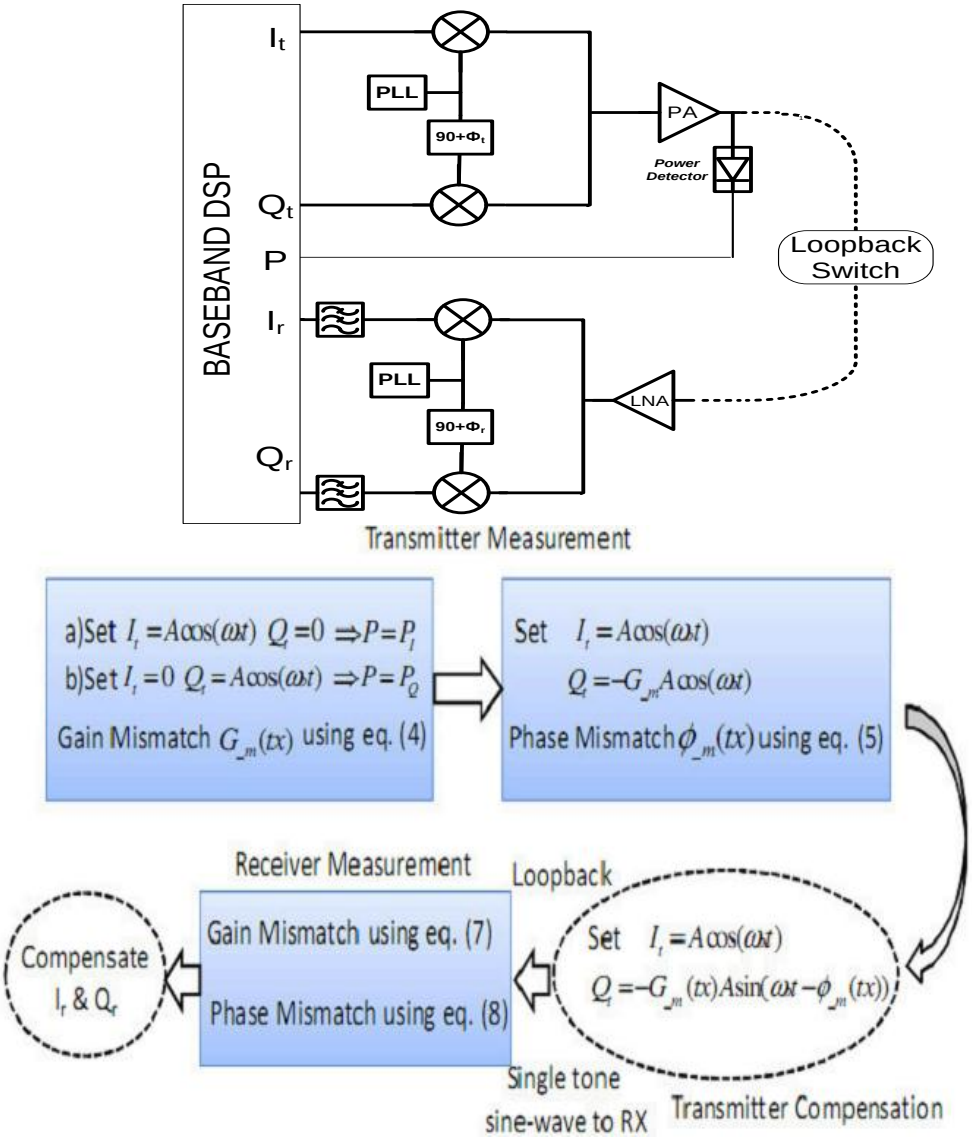
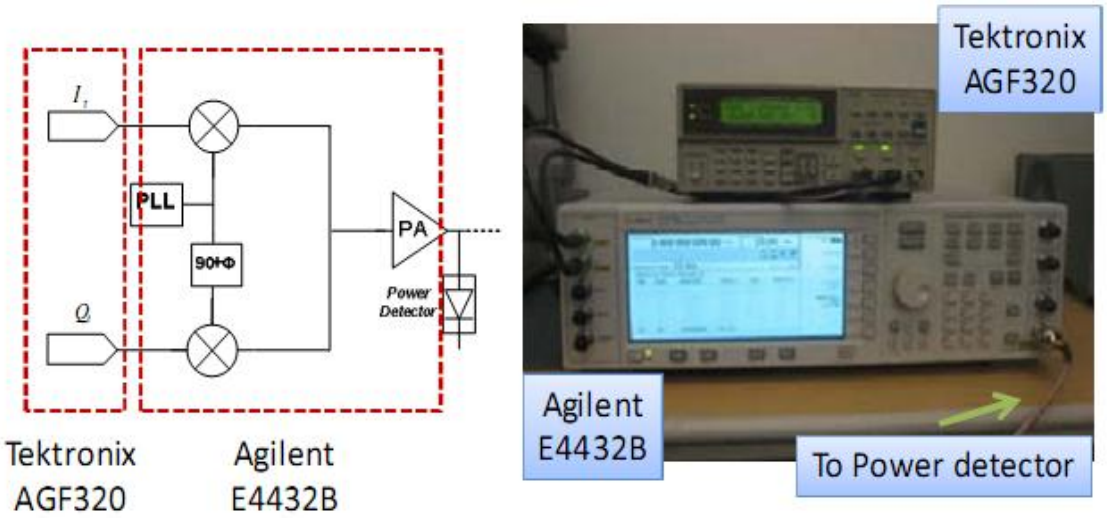


Figure 40: a) System block diagram with both Transmitter and Receiver with built in power detector b) Measurement and Compensation methodology

The system diagram for IQ mismatch measurement and compensation using loopback test and a built in power detector is shown in Figure 40a. The compensation methodology is shown in Figure 40b.

3.4.4. Experimental Validation

The setup for hardware validation of the low-cost technique for transmitter is shown in Figure 41a. Tektronix function generator AGF320 is used to generate It and Qt. RF signal generator Agilent 4432B has a built in quadrature up converter with controllable IQ gain and phase mismatch. This has been used as the IQ modulator for this experiment. Using I_t and Q_t as 1 MHz sine waves with amplitude of 0.3V and phase of 90^0 and 270^0 respectively. The IQ modulator uses a RF carrier of 2.4 GHz. The gain and phase mismatch measurement shown in Figure 41b and c show an error of only 0.5% and 4.5%, respectively. This shows that the low-cost technique can be used for IQ imbalance measurement and compensation.



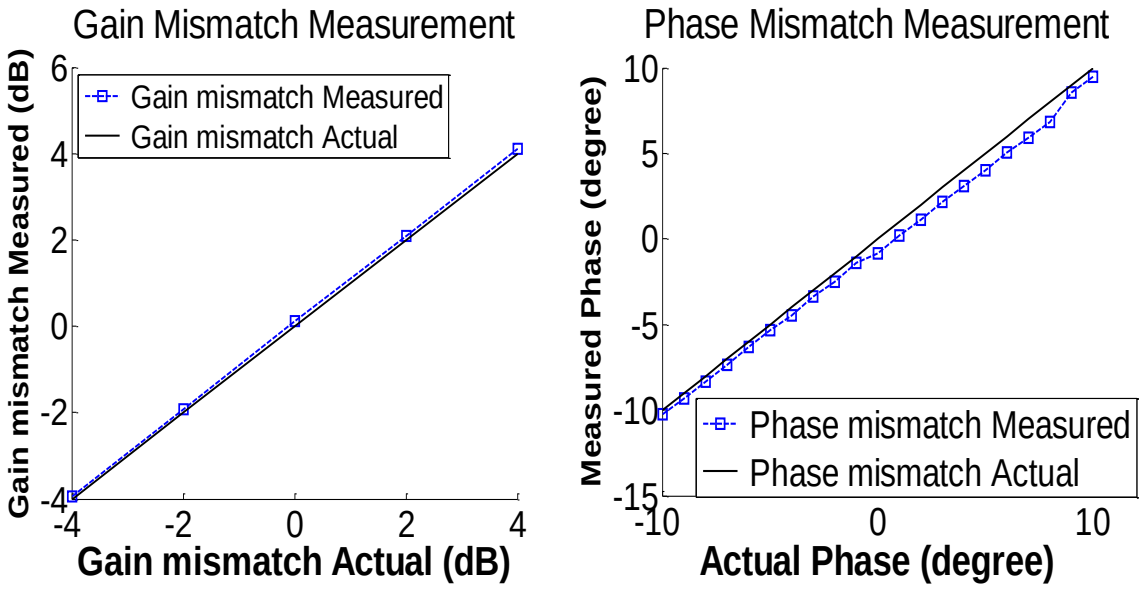


Figure 41: a) Experimental Setup Measured and Actual b) Gain mismatch c) Phase mismatch

3.5. BIST/Digital Compatible Distortion Model Extraction Driven Testing of RF Devices

Testing of Radio Frequency (RF) circuits for nonlinearity specifications generally requires the use of multiple test measurements contributing to increased test cost. Prior RF test methods have suffered from significant test calibration effort (training for supervised learners) when using compact tests or from increased test time due to direct specification measurement. On the other hand, due to aggressive technology scaling, there are a plenty of digital transistors available that can be used to simplify testing of Analog/ Mixed Signal (AMS) and RF devices. In this section, a simple RF test methodology is developed that: (a) allows RF devices to be tested for several distortion specifications in test time comparable to what can be achieved using supervised learning techniques while retaining the accuracy of direct specification measurement, (b) allows

multiple RF specifications to be determined concurrently from a single data acquisition and (c) does not require any training for accurate test specification computation. Next, this method has been extended to be digital compatible for testing of RF devices using digital testers or on-chip built in self-test (BIST) compatible testing. The low-cost method based on distortion model extraction is shown to give excellent results across common RF performance metrics while providing ~10× improvements in test time compared to previous methods.

The motivation of this work is to develop low cost RF tests approach that:

(a) Allows RF devices to be tested with the least test time possible.

(b) Allows multiple RF specifications to be determined concurrently from a single data acquisition.

(c) Does not require any training of supervised learners for accurate test specification computation.

(d) Does not require any power sweep as a part of the tests reducing total test time and hence test cost.

(e) Minimizes the use of high frequency test instrumentation allowing low cost operation.

(f) Utilizes digital logic to generate RF test pattern that can efficiently test RF devices further lowering test cost.

A key observation enabling the above goals is that a single tone baseband upconverted to RF or an amplitude modulated RF test stimulus sweeps the whole input power range of the DUT during the envelope. Hence all the gain and non-linearity

specifications can be measured from a consolidated amplitude modulated RF stimulus through single data acquisition without requiring any power sweep.

To validate the test technique developed, the golden response for a given test is mapped to the distorted response obtained from ADS characterization data (see Figure 42) to compute the N-model (polynomial) that defines the AM-AM characteristics of the device. The degree of the polynomial model affects the accuracy of the DUT characterization. In this work, a polynomial of up to '6th' degree is computed from the captured response for accurate characterization of the RF DUT.

3.5.1. Distortion Model based Testing using Modulated RF Stimulus

This sub-section describes how gain and nonlinearity can be tested accurately using an RF stimulus that is amplitude-modulated with a single-tone baseband signal. First, we develop the test theory and then provide simulation results.

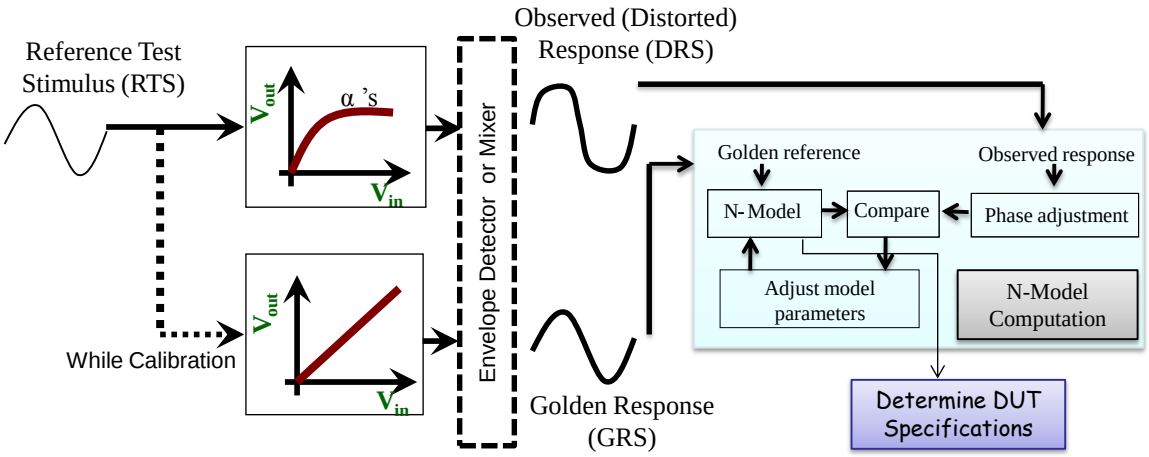


Figure 42: Conceptual block diagram

A. Approach

The low-cost approach builds on the following ideas and is illustrated in Figure 42:

(a) A amplitude-modulated RF test stimulus is computed in such a way that the response of the RF DUT to the stimulus exhibits strong statistical correlation with its test specification values under multi-parameter DUT perturbations (This is similar to the manner in which the test stimulus is constructed for the alternate test approach [83], [84], [85], [86] and results in an optimal choice for the baseband tone frequency and the RF carrier frequency. Note that the choice of the RF carrier frequency is an issue only for wideband RF devices). The resulting stimulus is called the *Reference Test Stimulus (RTS).*

(b) The DUT is excited by the reference test stimulus and its response is down-converted to baseband using either an *envelope detector or a mixer*. The down-converted signal is digitized for analysis. Note that the observed response is distorted by the DUT gain and phase transfer non-idealities. Hence, this response is also called the *Distorted Response Signal (DRS).*

(c) The DUT is removed and the input signal (RTS) is directly down-converted by the same mixer or envelope detector and digitized by a data converter. This is the ideal or *Golden Reference Signal (GRS*, see calibration in Figure 43*).*

(d) For comparison of the golden signal and the observed test responses, the phases of the same are adjusted digitally (by aligning the response peaks with low amplitude, as for low amplitude there is only phase deviation and no phase distortion) to compensate for the small-signal phase delay introduced into the RF signal by the RF DUT. This removes any phase delay caused by the DUT, but the amplitude dependent phase distortion (relatively much smaller than the small-signal phase delay) still remains.

(e) In the presence on non-linear components following the DUT, the non-linearity of the envelope detector or mixer is found out from the GRS and its inverse is applied to the DRS to correct for this nonlinearity. For example, in presence of detector nonlinearity the GRS and can be written as:

$$GRS = e(\mathrm{x}) \tag{30}$$

$$DRS = e(f(x)) \tag{31}$$

where, *f*() is the DUT transfer function to be measured and *e*() is the detector nonlinearity and x is the test input. e^{-1}() is found from (30) and applied to (31) to correct for detector nonlinearity. When the detector is linear enough, this transformation is not needed and directly DRS and GRS can be used for distortion model computation.

(f) We assume a finite order *Nonideality Behavioral Model* (*N-Model* in Figure 42) for the RF DUT including AM-AM and AM-PM distortion effects, with initial parameter values corresponding to an ideal DUT with no signal distortion. The purpose of the model is to map any DUT input stimulus to its output response captured. In general, such a behavioral model may include memory effects. Starting with the initial model parameter values as described earlier, the actual model parameter values are then computed using an iterative procedure (illustrated by the feedback loop through the "adjust model parameters" block in Figure 42) in such a way that the output of the model is the observed distorted reference signal (DRS) when the input to the model is the golden reference signal (GRS). In this technique the N-Model is the distortion model concerned.

(g) It is shown later that the N-model that maps the golden reference signal (GRS) to the observed distorted (down-converted) reference signal (DRS) directly yields the RF DUT AM-AM (amplitude) distortion characteristics. The relevant Gain, IIP3, IIP2 and P1dB specifications of the DUT are directly computed from the model parameters so extracted.

B. RF DUT Parameter Extraction Framework

In this sub-section, we are primarily interested in measuring memory-less AM-AM distortion effects in the presence of amplitude distortion as well as phase distortion in the RF power amplifier (PA). However, the response of the RF device is down-converted by an envelope detector that filters out phase distortion effects as long as the envelope signal is slow enough compared to the RF signal making the effects of the phase distortions introduced in the RF cycles negligible on the envelope. Hence, for measurement of AM-AM distortion effects alone, the N-model is assumed to be of polynomial form defined by

$$y = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3 + ... + \alpha_N x^N \qquad (32)$$

where, N is the order of the polynomial used. For an ideal device, α1 = gain, α2 = 0 and α3 = 0, etc. For a specific DUT, the objective is to find the values of α1, α2, α3 etc. such that when x is the golden reference signal (*GRS*) in the polynomial above, y is the distorted response signal (*DRS*).

To validate the low-cost approach, the golden response for a given test is mapped to the distorted response obtained from ADS characterization data (see Figure 42) to compute the N-model (polynomial) that defines the AM-AM characteristics of the device. The degree of the polynomial model affects the accuracy of the DUT characterization. In

this work, a polynomial of up to '6th' degree is computed from the captured response for accurate characterization of the RF DUT.

Once the polynomial y=*f*(x) for a specific RF DUT is known, the specifications that define the AM-AM distortion characteristics such as Gain, IIP2, IIP3 and P1dB (input) can be computed from the computed N- model parameters. Coefficients α1, α2 and α3 (from a 6th degree fit) are used to calculate specs based on the following equations [94].

$$\text{Gain} = 20*\log(\alpha 1) \quad \text{(dB)} \tag{33}$$

$$\text{IIP2} = \left\| \frac{\alpha 1}{\alpha 2} \right\| \quad \text{(volts)} \tag{34}$$

$$\text{IIP3} = \sqrt{\frac{4}{3}\left\| \frac{\alpha 1}{\alpha 3} \right\|} \quad \text{(volts)} \tag{35}$$

$$\text{P1dB (input)} = \sqrt{0.145.\frac{\alpha 1}{\alpha 3}} \quad \text{(volts)} \tag{36}$$

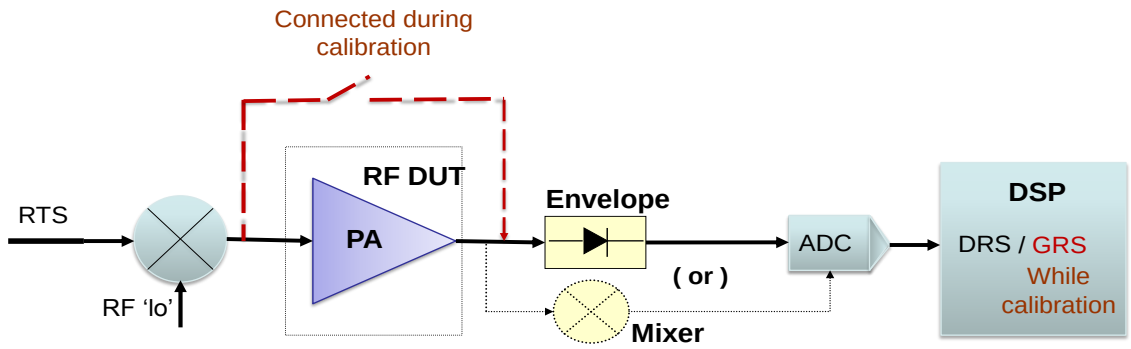


Figure 43: Rapid Gain and Nonlinearity Test System

C. N-model Parameter Computation

Using the test setup of Figure 43, the golden response signal (GRS) and the distorted response signal (DRS) of the RF DUT are first captured. The polynomial that characterizes the distortion can then be computed by constructing the "Vandermonde"

matrix 'V' (discussed below). As explained earlier, GRS is assigned to be *x* and DRS is assigned to be *y* in the polynomial $y = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3$. The objective is to determine the polynomial coefficients that map x to y. In general, we assume that the polynomial y = *f*(x) is of degree *n*. For a given 'x' and a degree 'n' the Vandermonde matrix can be constructed as follows:

$$v_{i,j} = x_{i,n-j} \tag{37}$$

where $v_{i,j}$ is an element of the Vandermonde matrix V with row index 'i' and column index 'j'. From the Vandermonde matrix, the polynomial coefficients are obtained by solving the following equation in the 'least squares' sense.

$$V.p \approx y \tag{38}$$

Equation (38) is solved by using standard QR factorization techniques ($V^{-1} * y$) to calculate p in a computationally efficient manner.

Note 1: The sine waves at the output of the RF devices (GRS and DRS) are shown only for explanation purposes. In practice the developed theory of signal transformation makes no assumption regarding the wave-shape (sine, cosine, envelope etc) of the GRS and DRS.

Note 2: In a practical test setup, the DRS undergoes transformations from the measurement setup artifacts in addition to the distortion characteristics of the RF device. However since the GRS is captured into the digital signal processor via the same measurement setup/path, the artifacts introduced by the measurement setup can be calibrated out of the measurement as described in step (e) in Section 3.1. Further, any mismatch between the measurement setup paths can be de-embedded based on prior characterization.

The key advantage of the low-cost technique is the ability to capture the distortion characteristics (Gain, IIP2, IIP3, P1dB) of the test system without the need for training of a supervised learner and is accomplished using a single output capture to a simple amplitude modulated RF test stimulus.

D. Feasibility of Nonlinearity Estimation from Envelope Signal

The output signal of the local oscillator (LO) fed to the up-conversion frequency mixer is given by:

$$c(t) = A_c \sin(\omega_c t + \Delta\phi_c(t)) \tag{39}$$

where A_c, ω_c and $\Delta\varphi_c(t)$ denote the amplitude, angular frequency and phase noise of the LO output signal, respectively. The modulation (base-band) signal is given by

$$m(t) = A_m \sin(\omega_m t + \Delta\phi_m(t)) \tag{40}$$

where A_m, ω_m and $\Delta\varphi_m(t)$ denote the amplitude, angular frequency and phase noise of the modulation signal, respectively. The signal at the output of the mixer can then be expressed as

$$x(t) = A_m \sin(\omega_m t + \Delta\phi_m(t)) \times A_c \sin(\omega_c t + \Delta\phi_c(t)) \tag{41}$$

whose envelope is defined as

$$e_x(t) = \left| A_c A_m \sin(\omega_m t + \Delta\phi_m(t)) \right| \tag{42}$$

Note that ideal frequency mixing is assumed for simplifying the relevant formulae. When x(t) is fed to a nonlinear power amplifier, the output signal distortion is proportional to the instantaneous power of the input signal [95]. In other words, the nonlinear distortion is a function of $e_x(t)$. Thus, considering AM/AM and AM/PM distortions, the nonlinear power amplifier output is derived as:

$$y(t) = f_{AM/AM}\left[e_x(t)\right] \cdot \sin\left(\omega_c t + \Delta\phi_c(t) + f_{AM/PM}\left[e_x(t)\right]\right) \quad (43)$$

The power amplifier is followed by an envelope detector which extracts the envelope of its input signal. The envelope of y(t) is shown as

$$e_y(t) = f_{AM/AM}\left[e_x(t + f_{AM/PM}\left[e_x(t)\right]/\omega_c)\right] \quad (44)$$

Hence, the envelope detector output signal contains information needed to estimate the nonlinear distortion effect of the power amplifier.

It is also seen that the use of an envelope detector effectively "masks" AM-PM distortion effects and is therefore reliable for determining the AM-AM distortion characteristics of the DUT as long as AM-PM distortion is less than 10 degrees (this is usually the case). This is because phase deviations in the RF carrier are effectively "filtered out" by the low pass filter of the envelope detector as shown in Equation (44).

E. Simulation Results

Here the simulation results obtained for a two stage RF power amplifier (PA) designed in 0.18u CMOS using Agilent Advanced Design Systems (ADS) is presented. The nominal AM-AM and AM-PM characteristics obtained from ADS simulation are shown in Figure 44. Monte-Carlo simulations are then performed in ADS to generate process variations to obtain multiple AM-AM and AM-PM distortion curves. Using these process varied models the test strategy is implemented in MATLAB to validate the effectiveness of the concept developed.

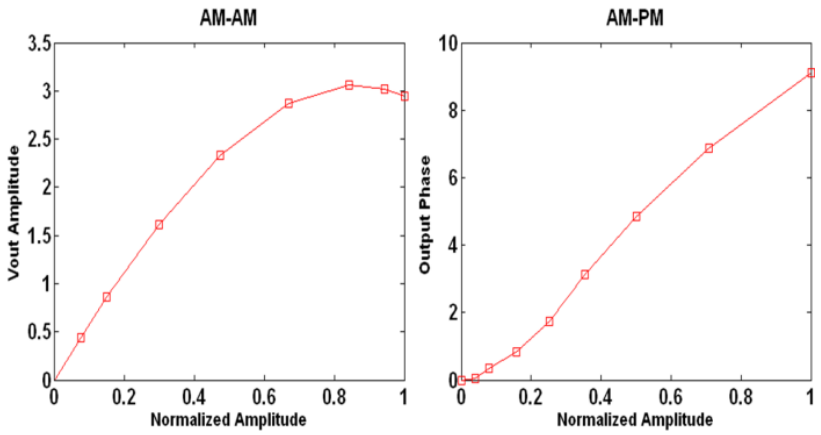


Figure 44: AM-AM and AM-PM characteristics of the PA DUT from Agilent-ADS simulations

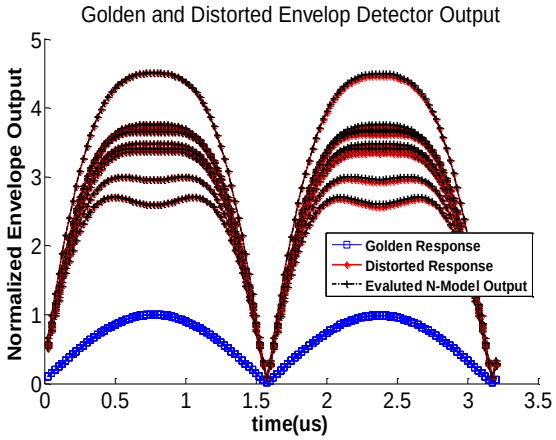


Figure 45: DRS for several instances and GRS

A single tone baseband signal (312 KHz) is upconverted to 2.4 GHz and sent to the DUT input. This amplitude modulated signal should have enough amplitude to exercise the nonlinearities of the PA. The DUT output is through an envelope detector as shown in Figure 43 and this provides the DRS. GRS is calculated by shorting the PA. One cycle of the GRS and the DRS for several different PA instances are shown in Figure 45. Equations (4) to (7) are then used to compute the specifications such as Gain, IIP2, IIP3 and P1dB for the GRS and DRS for a given PA instance. However, the AM-AM distortion model extraction theory discussed earlier assumes that the RF carrier frequency

is significantly larger (> 100×) than the frequency of the baseband signal with which it is modulated (which is the same as the bandwidth of the envelope detector). If this is not the case, AM-PM distortion of the RF carrier signal can distort the envelope detector output and introduce errors (small) into the AM-AM distortion model extracted from the measurement. Accordingly, the error in the resulting gain/IIP3 measurements introduced by this phase distortion is computed for one "golden" device and factored into the specifications calculated for all the devices. The quality of the low-cost test is evaluated by comparing the computed specifications against specifications obtained from ADS simulations as shown in Figure 46a for 500 PA instances generated using Monte-Carlo simulations. The 'x' axis for the plots refers to specs from ADS and the 'y' axis refers to specs obtained from the low cost test technique. Results are shown for envelope sensor. The RMS error in each specification is calculated for all the instances and plotted in Figure 46b for each specification. The maximum error over all specs and instances being less than 1.5% proves the validity of the approach.

For reference Figure 46c shows the same graphs of Figure 46a when corrections for the effects of AM-PM distortion on the observed envelope are not factored into account. The error histograms are shown in Figure 46d and indicate about 5% maximum error.

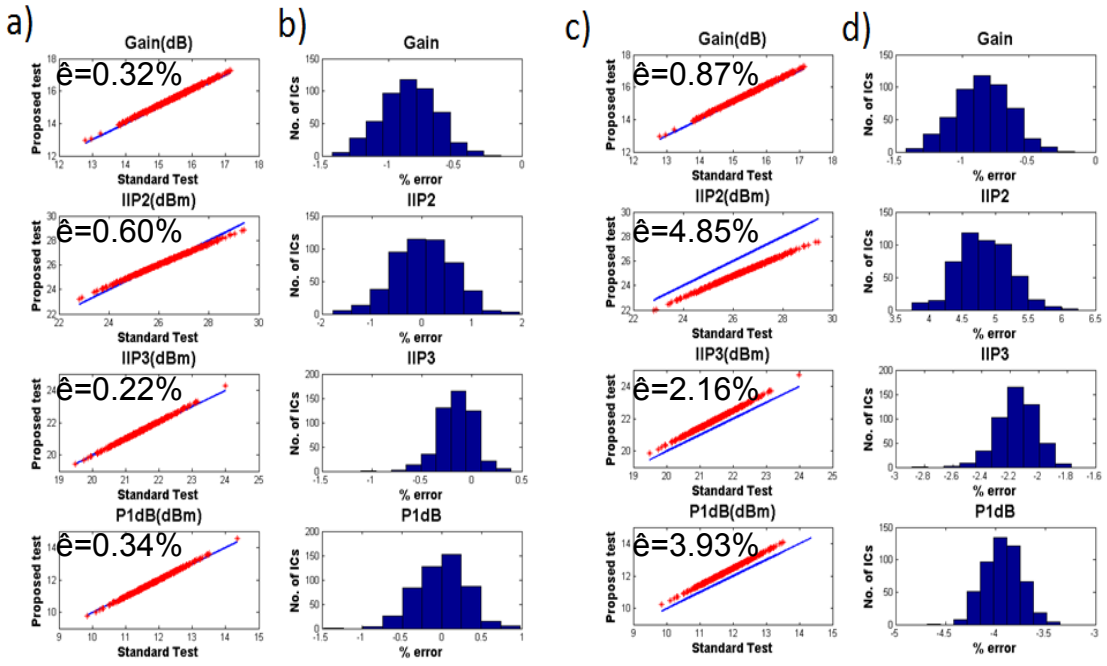


Figure 46: Comparison of low-cost test with actual test for 500 instances a) absolute specs (Gain, IIP2, IIP3 and P1dB), b) RMS error histogram for a, c) absolute specs without correction for AM-PM, d) RMS error histogram for c (ê = RMS Error in %).

3.5.2. Digital/BIST Compatible Distortion Model based Testing using Digital Pulse Sequences[1]

In this sub-section, we extend the ideas of distortion model based testing to develop a digital-compatible testing approach for RF circuits using optimized pulse sequences that can be driven by a digital test system interfaced to the RF tester load board. Digital compatible pulse based testing is developed to:

(a) Use of a Finite State Machine or a modified Linear Feedback Shift Register (LFSR) along with simple digital circuitry for generating test stimulus for RF devices. This

[1] The work presented in this sub-section is done in conjunction with Aritra Banerjee [97]

allows the testing to be compatible with digital testers as well as it is amenable for BIST implementation.

(b) Determination of multiple RF DUT specifications from a single data acquisition of the digital input stimulus without requiring the use of supervised learning methods for pass/fail determination.

Down conversion of the RF test response is performed by a simple envelope detector placed on the tester load board. A low-speed (relative to RF frequencies) A/D converter on the load board is used to digitize the down-converted response of the RF device under test (DUT). It is shown that the low-cost approach allows the critical gain and nonlinearity specifications of the RF DUT to be determined accurately using a single data acquisition. The above technique eliminates multiple-level power measurements or the use of expensive high frequency test instrumentation.

A. Pulse Generation Methodology

The pulse generation technique employs low cost digital circuitry consisting of a Linear Feedback Shift Register (LFSR) and basic logic gates. The pulses are constrained by the finite pulse width and rise and fall times. The bit stream of the LSFR, running at a relatively slow clock speed, is passed through an inverter and a logical AND / OR operation is performed on the original bit stream and the (delayed) inverter output. This creates sharp pulses whose width is determined by the delay of the inverter. The high frequency components of these pulses are utilized to test the RF device. For the AND gate structure, pulses are generated at each positive edge of the bit sequence and for the OR gate, pulses are produced at every negative edge as shown in Figure 47 and Figure 48 respectively.

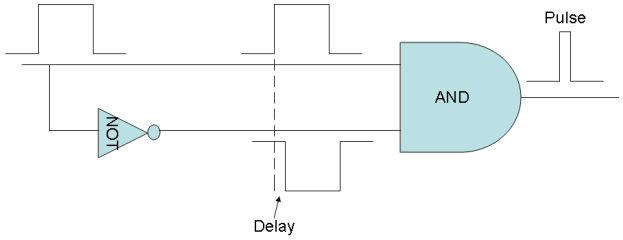


Figure 47: Pulse generation using AND gate and inverter

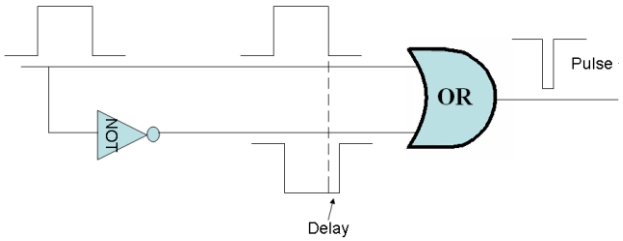


Figure 48: Pulse generation using OR gate and inverter

In the frequency domain, a pulse is represented by a sinc function of the form $\tau \sin c\left(\frac{\omega\tau}{2}\right)$ where τ is the width of the pulse. A pulse sequence comprises of several pulses which are time shifted version of a pulse at t=0. The Fourier transform of a signal g(t) which is shifted in the time domain can be expressed as :

$$g(t-t_0) \Leftrightarrow G(\omega)e^{-j\omega t_0} \tag{45}$$

where g(t) is the original signal in the time domain and $G(\omega)$ is its Fourier transform. When the signal is time shifted by t_0 its phase spectrum changes by $-\omega t_0$ [96]. An optimization process is used [97] to find the right time shifted sequence of pulses so that using the frequency components of the pulse sequence in the frequency band of interest, the coefficients of the nonlinear polynomial model can be estimated accurately.

A limitation in pulse generation comes from the fact that a pulse cannot be made infinitely narrow. The delay of the inverter gate of Figure 47 and Figure 48 defines the minimum achievable pulse width. As the pulse width increases, the main lobe of the sinc function narrows down in the frequency domain while its magnitude at low frequency increases as shown in Figure 49. It should be ensured that at 2.4 GHz the signal component has enough amplitude so that it can excite the nonlinearity of the RF DUT.

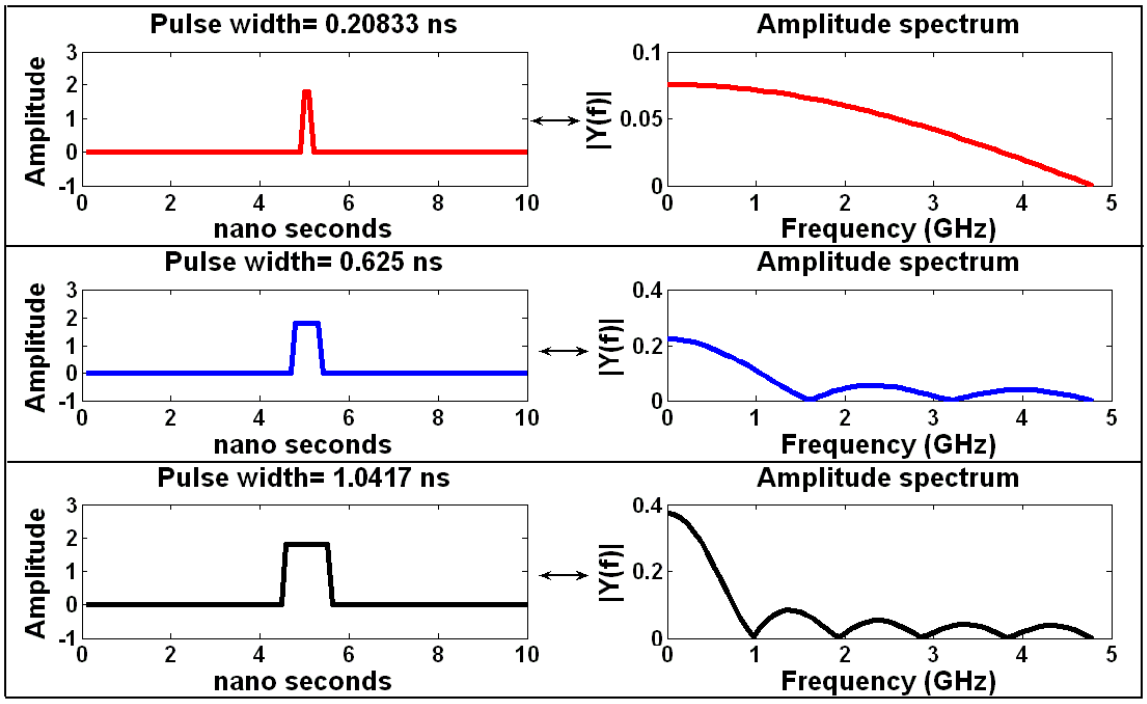


Figure 49. Variation in frequency spectrum with change in pulse width

Another limiting factor is the finite rise and fall time of the pulses which is approximately 10% of the clock time period. As the rise and fall time increases, the high frequency component of the signal reduces as shown in Figure 50.

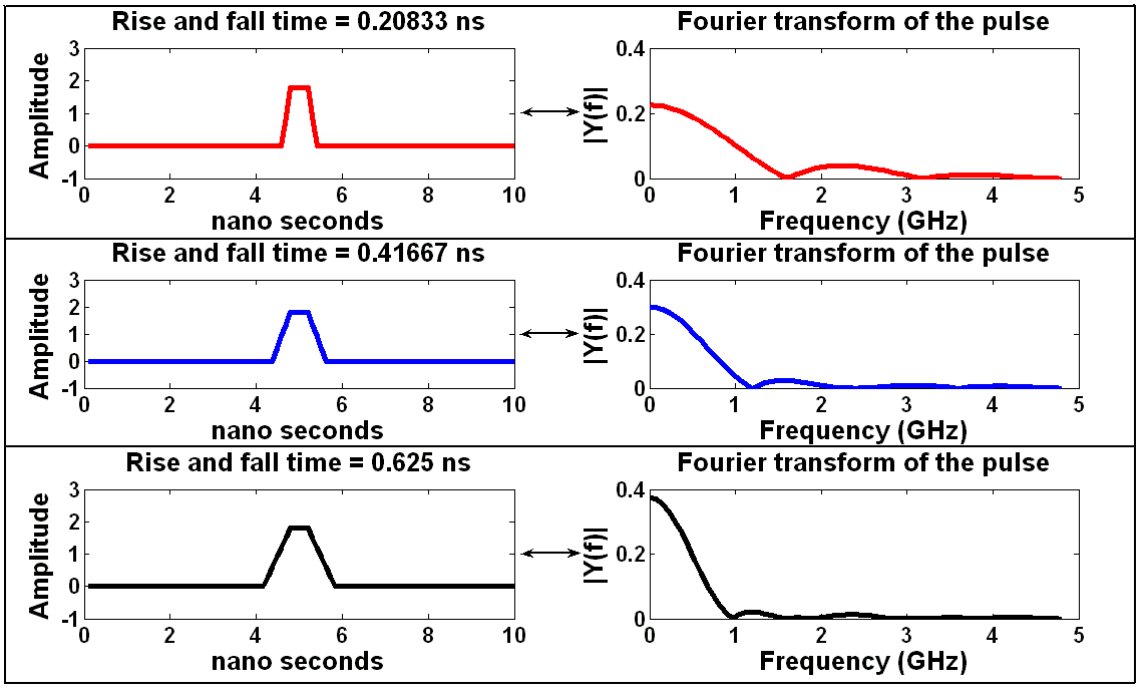


Figure 50. Change in frequency component distribution with different rise and fall time of the pulse

B. Setup for Test of RF Devices with Digital Pulse

A WLAN OFDM power amplifier operating at 2.4 GHz is used for validating our digital pulse based testing approach. Figure 51 illustrates the test setup. The test stimulus (bit stream) is generated from a Finite State Machine (FSM) or a modified linear feedback shift register (LFSR) [98] running at relatively low frequency (200 MHz). Using the AND / OR gate and inverter configurations of Figure 47 and Figure 48, sharp pulses are generated at each positive / negative transition of the original bit signal. Note that the minimum spacing between two closest pulses is limited by the period of the original LFSR bit signal. The derived pulse stream is passed through a band pass filter whose center frequency is 2.4 GHz. In this way RF test signal is directly generated from the digital *circuit without any up-conversion and without extra hardware*. The response of the DUT to this test stimulus is captured, down-converted using an envelope detector

and digitized. The golden response signal (GRS) (during calibration) and the distorted response signals (DRS) are captured. Based on the captured signals, the values of the model parameters ($\alpha_1, \alpha_2, \alpha_3$ etc. depending on the model used) of the RF DUT are calculated in the digital signal processor by mapping the golden reference to the distorted response through the DUT model. Finally the specifications of the RF DUT are calculated using the extracted parameter values from (4) to (7).

C. Simulation Results

PA Model and Optimized Stimulus

For simulation purposes the same PA described in Section 3 is used. Monte Carlo simulation is used to generate 50 device instances, by varying the important process parameters. The digital pulse based test methodology is applied to the process varied devices and the test results are presented in this section.

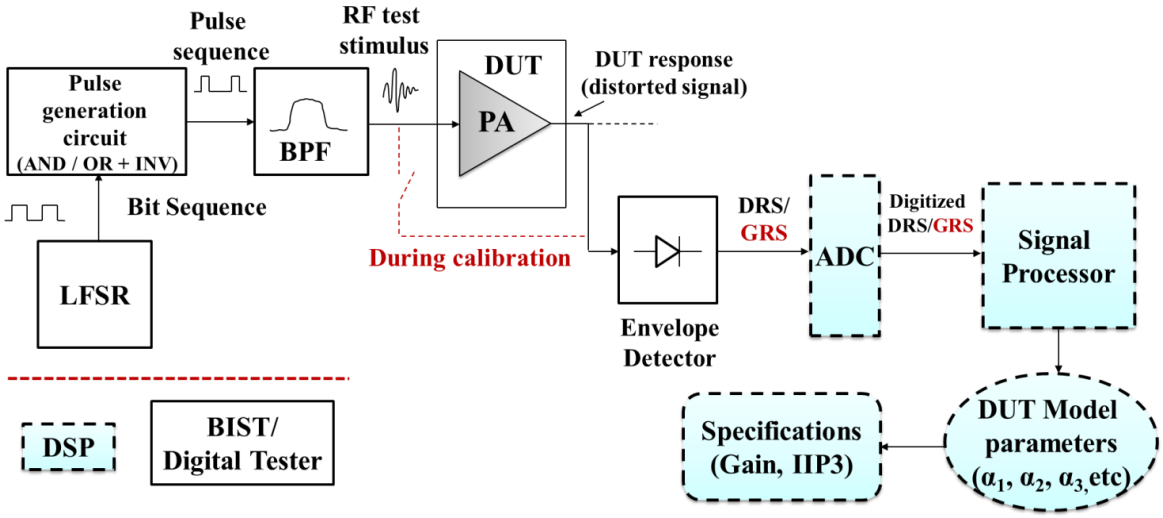


Figure 51. Digital/BIST Compatible Test Setup

The accuracy of the test can be improved by finding the right stimulus that minimizes prediction errors. An optimized pulse sequence is used to perform the PA

testing. The optimized pulse sequence is found using elitism based Genetic Algorithm that converges around 250 generations [97]. After convergence of the genetic algorithm, the value of the fitness function for the best candidate solution is found to be 0.0498 which implies that the prediction error is very small for this optimized test input. The optimized pulse sequence of consists of several frequency components extending from DC to 4.8 GHz. The frequency components of the optimized pulse sequence are shown in Figure 52a.

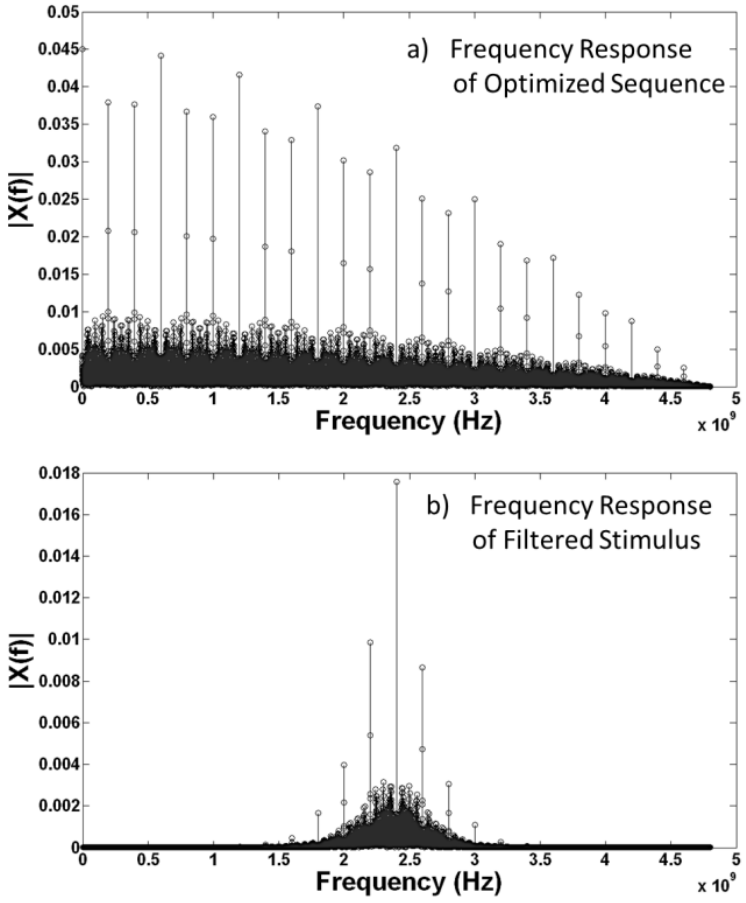


Figure 52. a) Frequency domain representation (FFT) of the optimized pulse sequence b) Band pass filtered test stimulus in freq. domain

The multi-frequency characteristic of the optimized pulse sequence is utilized to produce a multitone test signal at 2.4 GHz which is used to test the RF DUT. The multitone test stimulus is obtained from the digital pulse sequence by band pass filtering it at 2.4 GHz. The frequency domain characteristic of the filtered high frequency test stimulus is shown in Figure 52b. This multi-tone test signal is directly applied as a test input to the RF DUT. From the down-converted and digitized response of the DUT, the model parameters and the gain and IIP3 specifications of the RF PA are computed as described above. The predicted specifications of the device show excellent correlation to its original specifications as shown in next subsection.

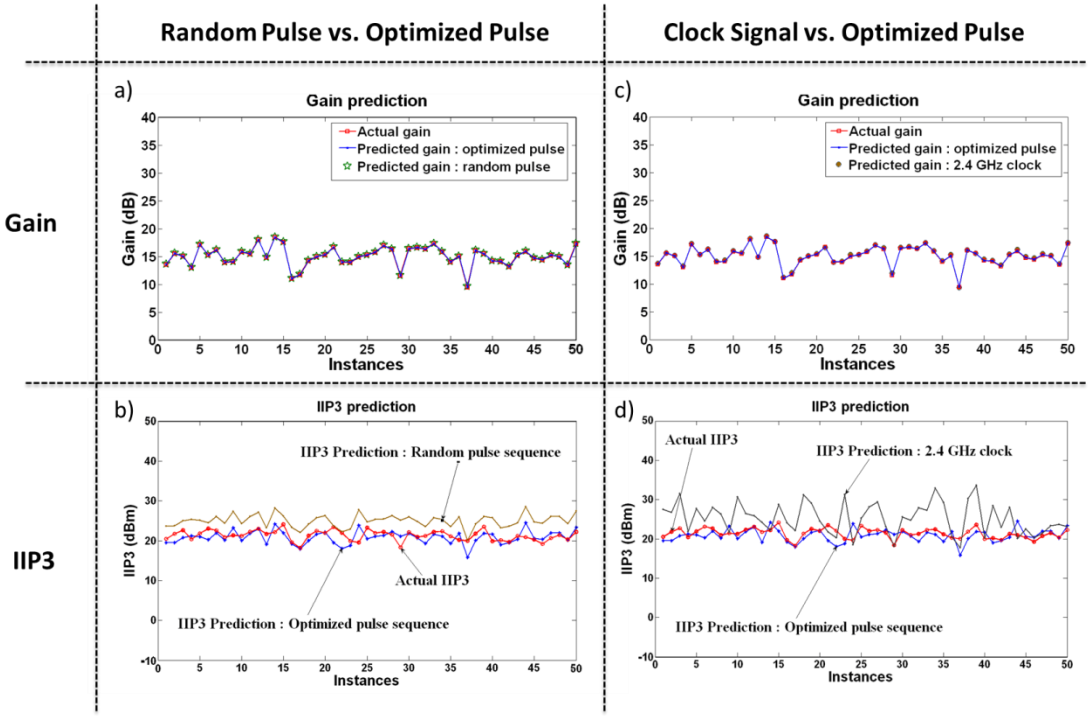


Figure 53: Simulation results using digital stimulus for distortion model based testing a) Gain b) IIP3 for random pulse vs. optimized pulse c) Gain d) IIP3 for clock signal vs. optimized pulse

Test Accuracy

The test results for the PA using optimized digital pulse sequences are shown in Figure 53. Two important specifications Gain and IIP3 are shown for this case. These results are plotted along with the actual specification values. The results are also compared with test accuracy achieved if the digital compatible testing is performed using only random pulse sequences or just clock signal.

The Gain and IIP3 obtained using the optimized pulse sequence is compared with the ones obtained using a random pulse sequence for is plotted in Figure 53a and b respectively. In both of the cases, gain prediction is very accurate. However, IIP3 computation with the optimized pulse sequence is superior to that computed using the random pulse pattern and is shown in Figure 53.

We also compare our ability to compute the gain and IIP3 specifications using a clock signal running at 2.4 GHz vs. the optimized pulse based test approach. As before, the gain computation perfectly matches with the original gain values as shown in Figure 53c. However, the IIP3 computation plot of Figure 53d clearly demonstrates that the optimized pulse sequence is far better than the clock signal for determining IIP3 values.

Table 4 Error value for different input test stimulus

Input	Optimized pulse sequence	Random pulse sequence	Clock @ 2.4 GHz
Error (in predicted alpha values)	0.0498	0.2211	1.7835

Table 4 shows the rms error value in the prediction of the PA model parameters for three different cases – optimized pulse sequence, a random pulse sequence and a clock running at 2.4 GHz, showing the effectiveness of using optimized digital pulses.

Extension of the optimized pulsed based test methodology to Embedded Testing

The test generation technique discussed in this paper can easily be extended to Built-in-Self-Test. The digital circuitry of the RF chip itself can be utilized to generate the RF test stimulus. This technique would be very effective when a receiver is subjected to testing since in transmitter the RF signal is inherently generated by the mixer which is not the case for the receiver. Also this low cost RF test stimulus generation technique can be used to test the individual components of the transmitter when it is not known if the mixer is in good or bad condition. For the embedded testing approach it is assumed that the digital signal processor of the chip is capable of mapping the golden reference to the distorted response and finding the parameter values of the DUT.

3.5.3. Hardware Validation

We present, in this sub-section, the hardware experiments performed to validate the distortion model driven low cost gain and nonlinearity testing using the amplitude modulated RF (i.e. single baseband tone) test stimulus and single data acquisition.

A. Experimental Setup

The setup shown in Figure 43 has been recreated in hardware as shown in Figure 54. The RF DUT is a Maxim 2.4 GHz Power Amplifier (MAX 2247). Instead of using a up-conversion mixer as in Figure 43, an amplitude modulated two tone RF signal is sent as the RF input from a Agilent E4432B (signal generator). Due to the limitation of the E4432B module we used, only a 50 KHz modulation on top of a 2.4 GHz RF carrier was

possible. This is equivalent to sending a 50 KHz sine wave, up converting it to RF using an up-conversion mixer. An Analog devices Down-conversion mixer (ADL 5382) was used to down-convert the signal to baseband. The Distorted Response Signal (DRS) is obtained by providing a high enough input signal power so that the DUT goes into compression. We use a constant 30 dB attenuator at the output of the PA to make sure the down-converter operates in the linear region. Due to the inability of the down converter to process a 50 KHz (close to DC) signal, we used two step down-conversion. First, the signal was down-converted to a 1 MHz signal with 50 KHz riding on it. This was subsequently sampled by an AlazarTech (ATS460) sampler ADC (sampling speed: 125 MSps). In the DSP, a low pass filter was used to obtain the 50 KHz DRS. The sampled DRS is shown in Figure 55. The Golden Response (GRS) was obtained by shorting the DUT input to the DUT output without the RF PA and attenuator.

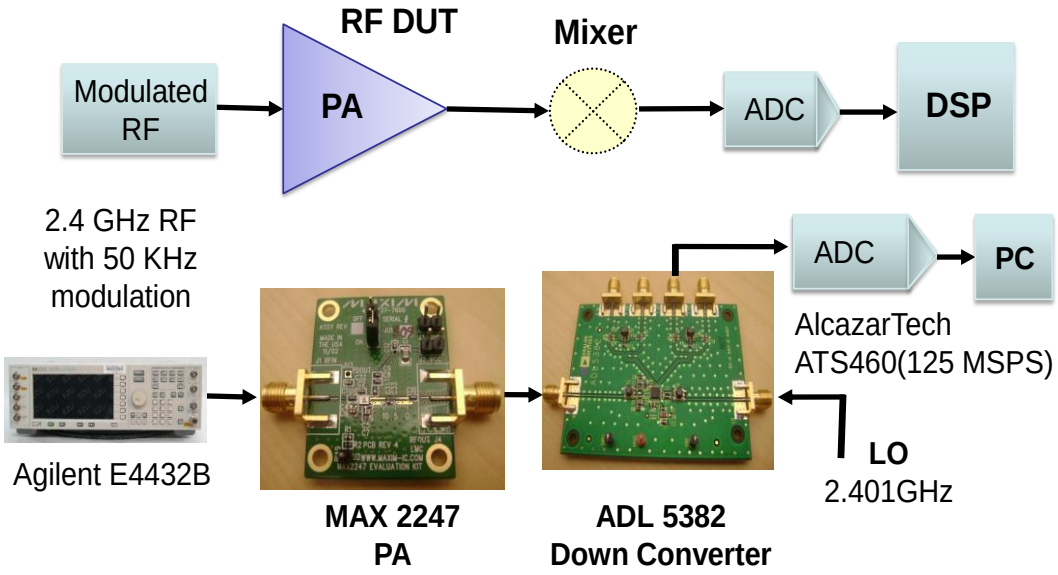


Figure 54: Experimental setup

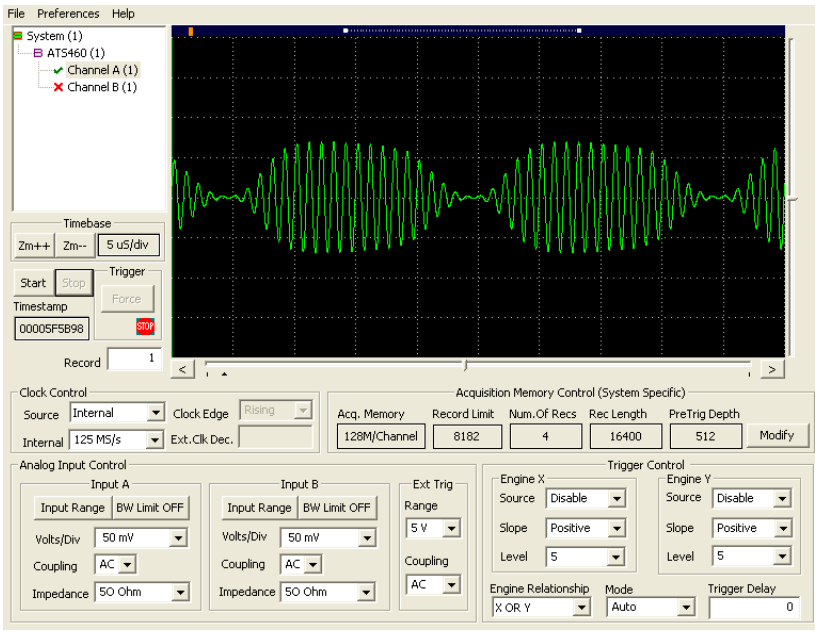


Figure 55: Captured down converted distorted response signal using AlazarTech Sampler

B. ***Experimental Results***

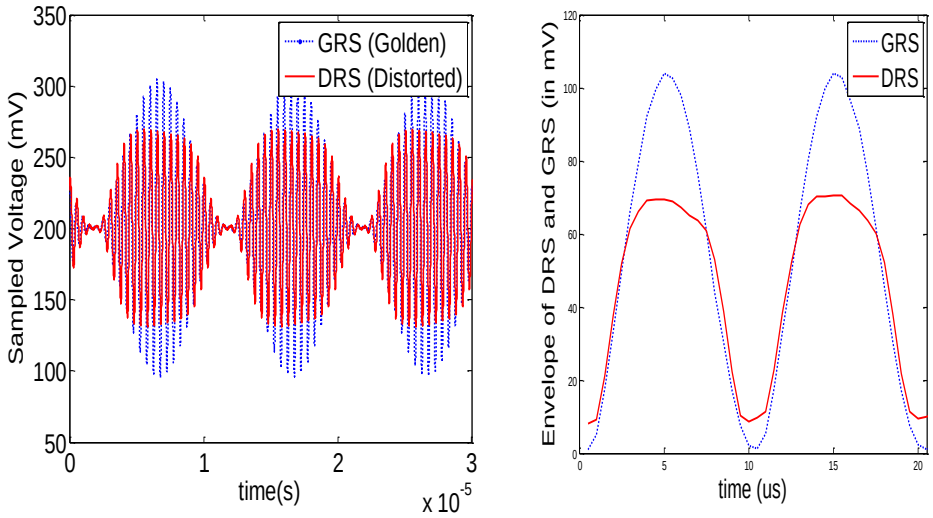


Figure 56: a) Measured GRS and DRS b) Envelope of both

This section presents the measurement results derived from the experimental setup described in the previous section using formulae in Section 3. Figure 56a shows the GRS and DRS overlaid on top of each other. The filtered version of this signal is shown

in Figure 56b and is used for N-model computation. The gain and P1dB and IIP3 original valued are obtained from the Max 2247 datasheet [99] and are also verified by standard tests. Table 5 shows the comparison between the original values and the measured specifications using the distortion model driven test technique.

Table 5 Hardware measurement results

Specification	Gain (dB)	Input referred P1dB (dBm)	IIP3 (dBm)
Original	29.3	-7	2.8
Measured	29.13	-6.37	3.2

3.5.4. Discussions

A. Key Accomplishments

The key accomplishments of the paper are as follows:

Test Cost: The technique developed is a *low-cost test solution* as the signals are sourced and measured at low frequencies.

Single Data Acquisition: Results show that accurate computation of multiple specifications such as Gain, IIP2, IIP3 and P1dB and phase distortion is possible from a *single data acquisition*!

Test Simplicity: The test is simply a low frequency sine wave upconverted to RF i.e. an amplitude modulated RF signal. This test is accurate for multiple specs using a single data capture without the need for training of a supervised learner.

Digital/BIST Compatible Testing: The distortion model based testing of RF devices is compatible with digital compatible pulse sequence based testing. Hence the RF devices

can be tested using digital tester and minimal load-board circuitry. This methodology is also readily extendable to BIST.

Test Time: The test time for the methods developed is equal to the single output capture time (test length is in tens of μs) plus the times for computation in DSP. This *test time is significantly lower than standard RF tests and is comparable to some of the fastest available test techniques such as Alternate test.*

B. Comparison with Alternate Test

This technique can provide fast and low cost measurement of RF specifications and imperfections. Alternate test methods proposed in [83], [84], [85], [86] is also able to do so, but at the cost of significant learning process involved upfront. Under process and temperature variations, the alternate test creates the models (mapping functions) dynamically using supervised learning, whereas the developed method uses predefined static models (as shown is section 3.2). Hence we get rapid low cost testing without overhead of supervised learning by trading of some adaptability of the underlying models.

C. IIP3 Measurements for High Power Devices

The models proposed in [94] and used in Section 3 for RF specification prediction holds good for most of the amplifiers where the gain compression is the dominating factor for causing the P1dB of the device. This method assumes an inherent relation between P1dB and IIP3 (close to 10 dB apart) as described in [94]. But there exists some high power devices for which nonlinearity at low input powers (IIP3 calculation) is much lower compared to the compression effects exhibited at large signals (P1dB calculation) due to various large signals effects like clipping etc. This result in an IIP3 of the device

which is more than 10 dB higher than it input P1dB. For testing such devices a multi-tone baseband signal should be applied such as shown in Figure 57 and the N-Model created between the high power lobes of DRS and GRS should be used to calculate P1dB whereas the N-Model created from the low power lobes should be used to calculate IIP3. We propose this extension of the method presented in this section as a future work.

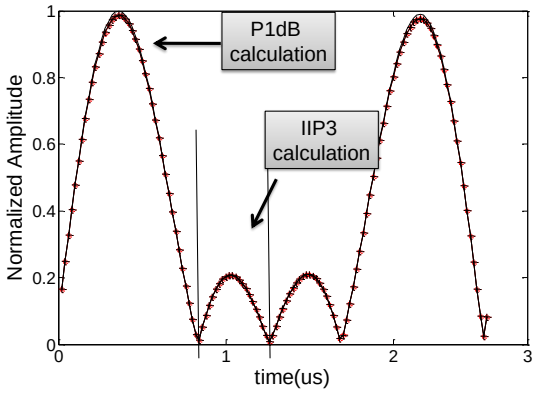


Figure 57: Proposed test for P1dB and IIP3 calculation for high power devices

Finally, in this section a rapid low cost test technique is developed to compute multiple RF specifications as Gain, IIP2, IIP3, P1dB through single output capture using a simple amplitude modulated test stimulus. Compared to traditional RF tests it provides significant advantage of test time, cost and simplicity. The test methodology is compatible to both analog single-tone test stimulus and optimized digital pulse sequences. Hence it allows digital compatible testing and can be easily extended to BIST implementations. It is for the first time that the test setup with same low complexity as an alternate test is used to test for the above mentioned specifications without the need for *trainings* that is usually associated with a typical alternate test. Simulation and hardware results show accurate computation of the specifications for a 2.4 GHz PA using both analog and digital test stimulus.

Chapter 4. ENVIRONMENT-ADAPTIVE ZERO MARGIN LOW-POWER WIRELESS TRANSMITTERS

This chapter deals with design of environment (channel) adaptive wireless transmitter systems for low power operation. Design of power-efficient OFDM transmitters suffer from a major bottleneck due to the high peak-to-average ratio (PAR) of OFDM signals as the efficiency of a linear RF power amplifier reduces drastically due to backoff requirements. In this paper we propose a system level approach for dynamic power reduction in OFDM transmitters with varying channels. The methodology developed uses adaptive baseband companding/ expanding of the OFDM signal along with concurrent PA re-biasing to save power. Using channel information from standard channel estimation techniques for dynamic PAR adaptation, the adaptation approach achieves a PAR reduction as high as 7.25dB. Under favorable channels this translates to a power savings of 5.5× compared to static Power Amplifiers (PA) and 3.6× compared to adaptive PAs with only output power adaptation.

4.1. Previous Work

4.1.1. Background

The explosive advancement in wireless communication technologies in recent years has necessitated the development of spectrally efficient modulation techniques. Orthogonal Frequency Division Multiplexing (OFDM) based signal modulation has evolved as a popular choice for wireless communication standards such as WLAN, UWB, MIMO, DVB-T and more recently WiMaX. OFDM uses a number of closely spaced orthogonal subcarriers (N) increasing robustness to multipath fading, interference

etc. The WLAN standard uses 64 carriers, while WiMAX uses 256, 1024 or 2048 carriers. A key issue with the use of OFDM based modulation is the high peak-to-average (PAR) ratio of the transmitted OFDM signal. The PAR increases with number of orthogonal carriers (N). As shown in Figure 58, PAR increases linearly with N for small values of N. For higher values (i.e. N> 64) the PAR hovers around an average value of 12 dB, since full coherent addition of the different carriers occurs with very low probability [100]. Following this, in practice the PAR for a 256-carrier OFDM-modulated signal (WiMAX) is also observed to be around 12 dB [101].

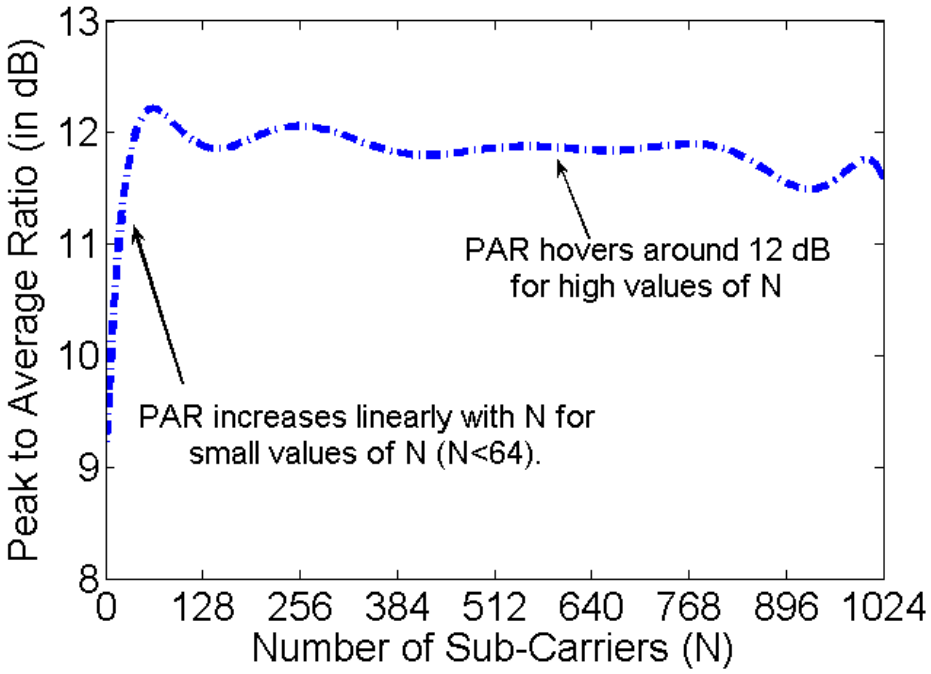


Figure 58: PAR of OFDM Signal with no. of Subcarriers [102]

The RF Power Amplifier (RF PA) tends to be one of the most power hungry blocks in typical mobile transmitters. Figure 59 shows the breakdown of power consumption for a commercial wireless transmitter (Intel Prism- II). Note that only 8% of the total power is the transmitted power, whereas a significant amount of the total power

(41%) is wasted in the Power Amplifier [103]. This efficiency of the PAs are going down with the increasing popularity of spectrally efficient high PAR OFDM signals which require high linearity PAs for transmitting such signals with acceptable distortion (as opposed to saturated PAs that work with constant envelope signals but exhibit high efficiency). One way for the PA to operate in the linear region is to back off the operating point by at least the PAR of the signal. This is a major bottleneck in the implementation of power efficient transmitters since the efficiency (η) of a linear PA reduces by a factor of two for every 3dB power back-off. η is unacceptably low (~5%) for class A PAs with realistic back-off.

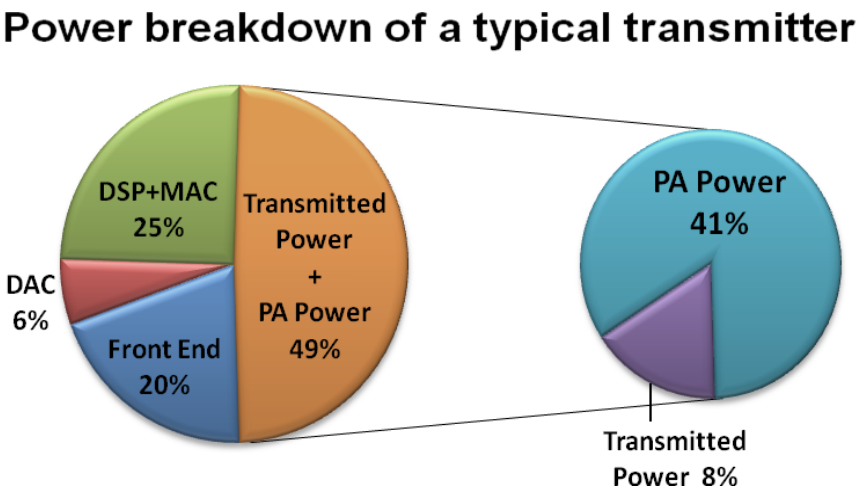


Figure 59: Typical transmitter power consumption breakdown

To circumvent this problem, several circuit and system level solutions are employed /proposed to increase efficiency. In the system level, to reduce interference and increase efficiency, *average output power* of the Mobile Station (MS) is varied depending on the channel condition and distance from the Base Station (BS). The PA average output power adaptation is performed using power control information (based on received signal strength) sent by the BS to MS through the BCH (Broadcast channel)

[104], [105]. If the DC power consumption is kept fixed (i.e. static PA) the efficiency of the PA is very low for the time that it is not transmitting at the maximum average output power level. An approach to increase the operational efficiency of RF transmitters has been to use a tunable PA (such as Agilent ACPM-7891 [106]) in the front-end. A MS power controller (such as National Semiconductor LMV243 [107]) uses the information from BS to control the output power of the PA by applying proper control voltages and sometimes using a control loop [105], [108]. Output power is varied in a wide range as described in [109]. For example, output power could be varied from 5 -39 dBm for GSM 900MHz band. This recovers some of the efficiency loss due to variable distance between the BS and MS. This adaptation is as shown in Figure 60 from biasing point B1 to B2, through average output power reduction. *However, it should be noted that this adaptation is performed only to cope for the* ***variable attenuation*** *in the channel and do not have any information about either the high PAR of the OFDM signal or other distortion effects like interference and multi-path fading.*

To increase the efficiency of PAs using circuit level techniques, the supply voltage of the PA is changed according to the envelope of the signal. These PAs can be broadly divided into 3 categories [110], namely *slow tracking*, *envelope tracking* and *polar modulation* PAs. A *slow tracking* PA [111] supplies the PA with a voltage slightly greater than the largest peaks of the envelope. Hence it can only recover the efficiency loss due to power-control back-off. An *envelope following* or *envelope tracking* PA [112], [113], [114] have been developed in which the supply voltage is dynamically modulated by the estimated or tracked envelope to keep drain efficiency high. Hence it allows recovery of lost efficiency due to both modulation and power-control back-off. In

these methods, the envelope amplitude information has to be extracted from the signal and incurs extra complexity and increased hardware overhead. In *polar modulated* PAs [115], [116] the supply modulator applies the required envelope signal directly onto the carrier through a saturating PA. Though the use of saturated PAs increase efficiency, the bandwidth requirements of the AM path is significantly high and the noise requirements of the supply modulator makes this implementation impractical. A power management block has been proposed in [117] which provide good efficiency while providing variable output voltages. This on-chip block can generate drain and gate bias for a PA using inputs from DSP making adaptation of PAs easier. This work also shows adaptation of a PA with varying average output power to maintain high efficiency, using the proposed PMU. Though all of the above methods increase efficiency they have been targeted towards fixed PAR OFDM signals.

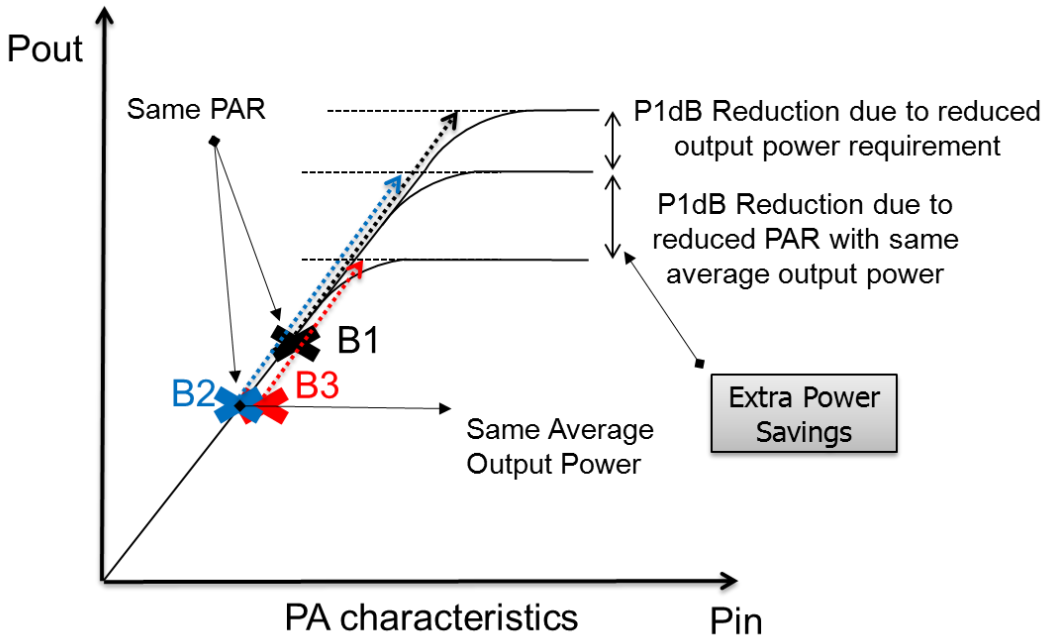


Figure 60: Extra Power savings through dynamic PAR reduction

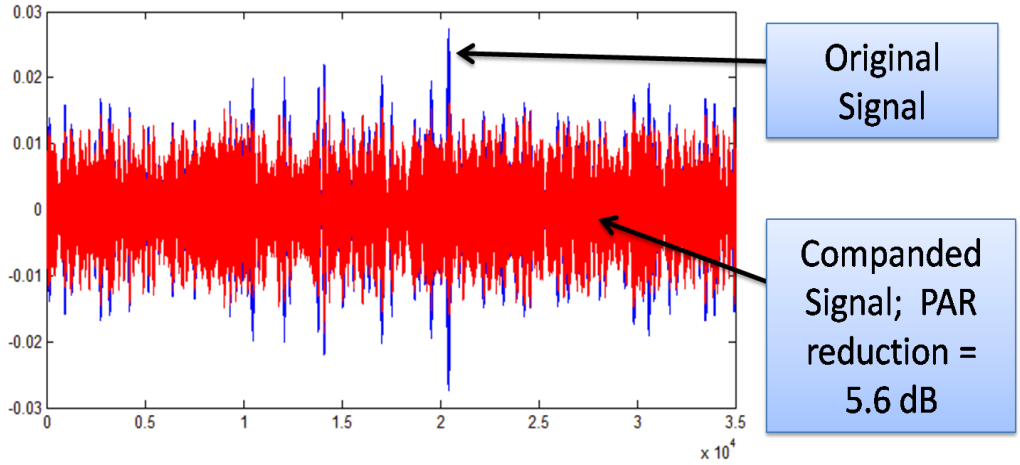


Figure 61: Original and Companded OFDM signal

The problem of low efficiency can also be alleviated by companding the high PAR OFDM signals. *Companding* is a signal processing technique in which the OFDM-modulated waveform is passed through a non-linear transfer function to reduce its PAR. This non-linear transfer function attenuates the OFDM signal as a function of its instantaneous amplitude, with higher amplitude values experiencing larger attenuation. In the receiver, the signal is passed through the "inverse" of this non-linear transfer function to recover the original signal for demodulation. Figure 61 shows an original OFDM signal and the signal after companding to reduce its PAR by 5.6 dB. It can be clearly seen that the companded signal has significantly lower peaks compared to the original one, relaxing the linearity requirement of the transmit PA. The PA linearity relaxation and hence power savings is directly proportional to the amount of companding applied to the OFDM signal. Significant research on PAR reduction of OFDM signals has been done and several static techniques have been presented in the published literature. But almost all of them are either very computation intensive or introduce significant noise into the signal. Since these techniques introduce noise, the maximum achievable reduction in PAR is limited by the worst case environment of the transceiver system. Here, the term

"environment" refers primarily to the quality of the wireless channel (not only attenuation, but the sum quality including all distortions effects like interference and multi-path fading etc.). *However, most of the time a wireless device is powered up for operation, it is not in its worst case operating environment*. Hence, when the wireless channel quality is good, the PAR value can be traded off for decreased quality (later quantified by Error Vector Magnitude or EVM) of the RF signal generated by the transmitter, saving considerable power in the same without impacting the specified bit error rate of the received signal. Under this operating paradigm, amount of PAR reduction can be traded off for power consumption under the majority of operating conditions.

In this work, we present a system level power control strategy for an adaptive transmitter which not only modulates varying average output power based on channel attenuation (i.e. from B1 to B2 in Figure 60) but also ***performs dynamic reduction of PAR under favorable channel conditions in conjunction with adaptive biasing of the PA, providing an extra degree of power savings in the PA*** (from B1 to B3 in Figure 60, i.e. extra power savings by dynamically going from B2 to B3).

4.2. Adaptation Framework

This section describes the adaptation framework. Figure 62 shows the transceiver system with detailed baseband architecture. WiMAX OFDM (with N=256) is used as modulation of choice in the baseband for this work. However, this technique will hold for any OFDM system with high PAR signals. The companding (in transmitter) and expanding (in receiver) blocks are made adaptive for realization of the adaptive system.

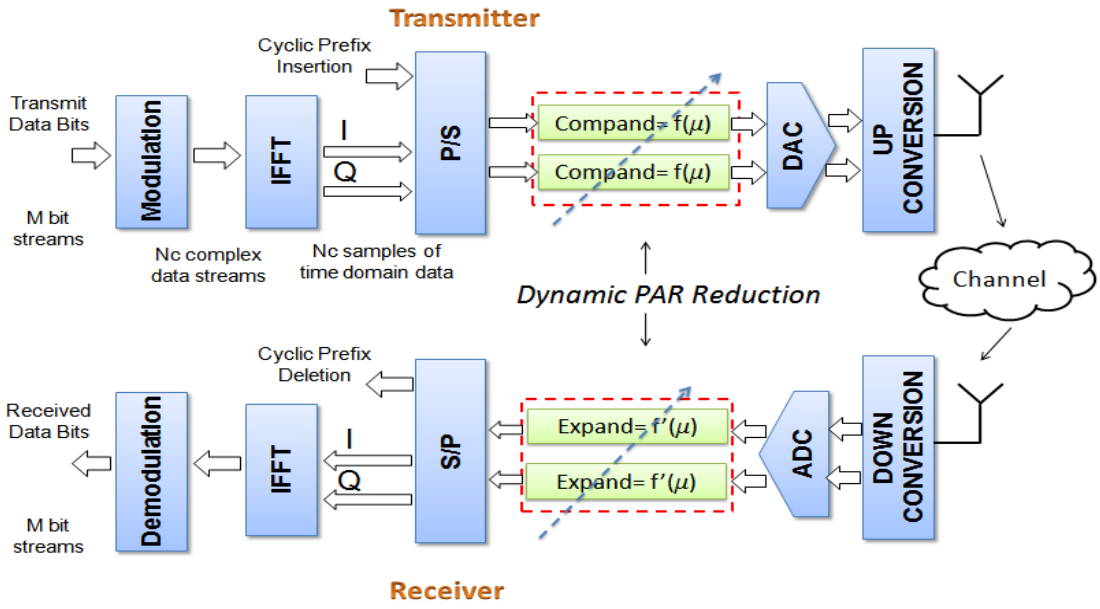


Figure 62: An OFDM transceiver and dynamic companding in baseband for PAR adaptation

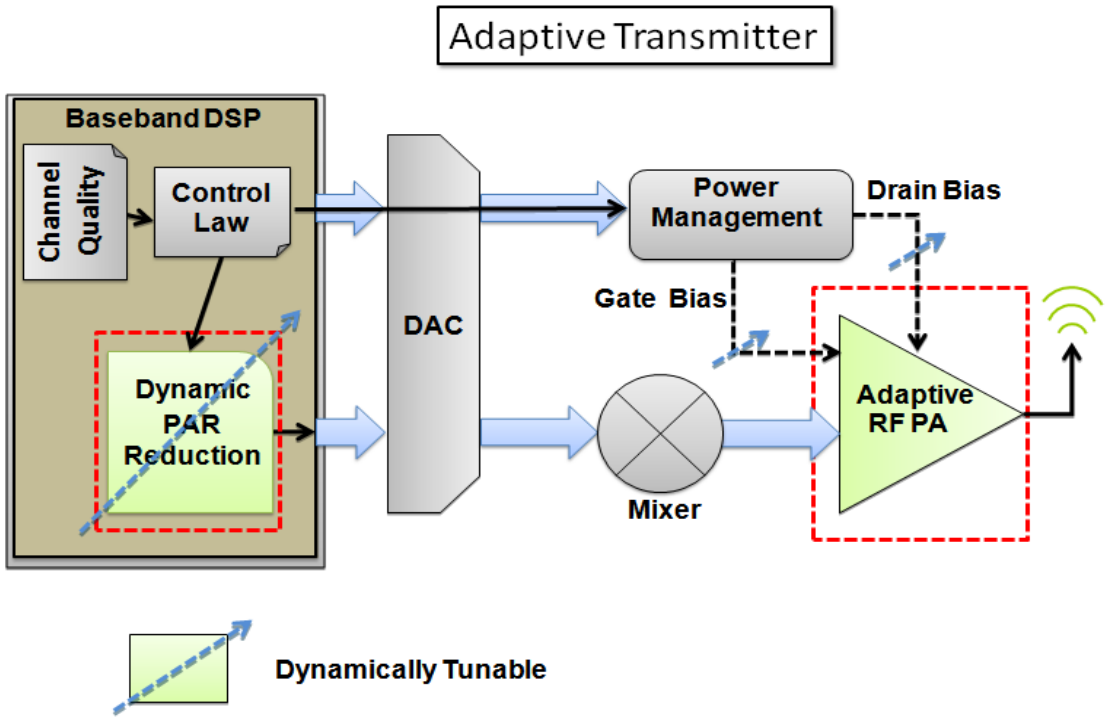


Figure 63: Low-power adaptation of mobile transmitter through concurrent dynamic companding and adaptation of RF PA (Concurrent PAR and PA adaptation)

Figure 63 shows the details of the mixed signal and RF portion of the transmitter. PA adaptation is performed by controlling its drain and gate bias to trade off power for linearity. The implementation of the power management block used can be found in [117]. The key components that enable the adaptive operation of the transmitter are briefly outlined below:

- The radio-link quality is estimated dynamically in the receiver using traditional channel estimation algorithms and fed back to the transmitter using Broadcast channel for adaptation purposes.
- For good channels the dynamic PAR reduction block in the transmitter DSP reduces the PAR of the transmitted OFDM signal, reducing the P1dB requirements of the PA for a given PA output power level. The control law controls both PAR reduction and P1dB reduction (through Power Management block) concurrently depending on the channel quality.
- The PA is adaptively re-biased (Figure 63) to save power (lower P1dB) by applying gate and drain bias through the power management block. An adaptive RF PA is designed that maintains its class of operation across different operating points to enable this adaptively by trading of linearity (P1dB) for power.

The above described framework is used to *concurrently control* the amount of companding (PAR reduction) and PA biasing to exploit built-in design margins in the transmitter system under favorable channel conditions to yield significant power savings.

4.3. Channel Quality Estimation and Feedback

To perform closed loop feedback, we need a received signal quality metric which

can be calculated in real-time and captures the sum effect of the channel (noise, fading components, interference etc.) and the noise and non-linearity introduced by the transmitter and the receiver. Traditionally Bit Error Rate (BER) is used for estimating this. Since real-time BER computation is impractical (due to the large number (~10^5 or more) of symbols that need to be transmitted for reliable BER estimation), we propose using Error Vector Magnitude or EVM for this purpose. EVM, which can be calculated over few symbols, is defined as follows:

$$EVM = \sqrt{\frac{1}{N}\frac{\sum_{1}^{N}\|y_i - x_i\|^2}{\|y_{\max}\|^2}} \tag{46}$$

where,

y_i = Received complex data (I+jQ),

x_i = Transmitted complex data (I+jQ),

y_{max} = Outermost data point in the constellation diagram,

N = Number of complex data points used for computation,

where N is sufficiently large.

Traditionally, radio-links are built to meet a certain BER threshold (say 10^{-3}, i.e. 1 bit error per 1000 bits). Through repeated system simulations under different channel conditions and transmitter biasing conditions it is found [118], [119] that *around and above* BER threshold, EVM and BER shows good correlation as shown in Figure 64 (for both QPSK and 16 QAM modulation). Hence, EVM thresholds are found corresponding to a given BER threshold for each modulation scheme (BPSK, QPSK, 16- QAM, 64-QAM etc.). If the EVM of the received signal is more than the EVM threshold concerned the quality of the received signal is not acceptable.

1-bit information of the received signal quality (which captures sum effect of channel quality and transceiver quality) is fed back by encoding it in the header sequence to the MS transmitter from the BS receiver to aid the adaptation of the PA. The value of this bit is defined as follows:

Bit value = 0 ; if $EVM_{\text{received signal}} > EVM_{\text{threshold}}$

= 1 ; if $EVM_{\text{received signal}} < EVM_{\text{threshold}}$

This *channel quality* feedback information controls the adaptation as shown in Figure 63. Increasing the companding factor introduces more noise and hence increases EVM (lower PAR → lower linearity requirement → lower power). Hence a 1 means the value of companding should be increased and vice versa.

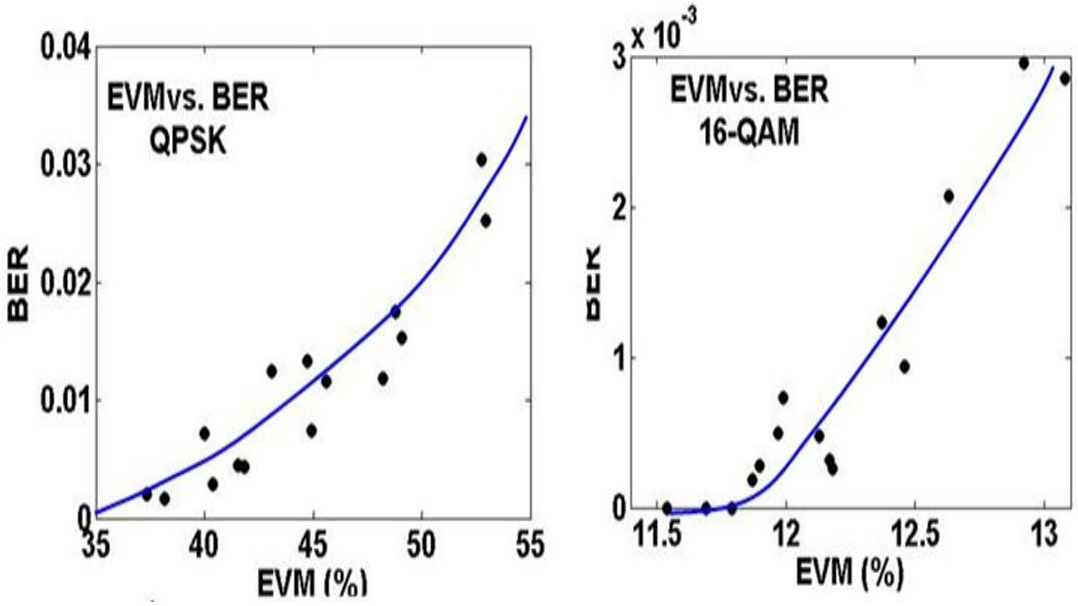


Figure 64: Correlation between EVM and BER

4.4. Environment Dependent PAR reduction

This section provides a brief overview of the traditional static PAR reduction techniques and then proposes a dynamic (i.e. environment dependent) PAR reduction

technique.

4.4.1. Traditional Static PAR reduction techniques

In the past, there has been significant research on PAR reduction of OFDM signals [120], [121]. The available techniques can broadly be classified into four categories. The first relies on the use of a partial transmit sequence (PTS) [122], [123] in which sub-blocks of data are adjusted by a phase factor to reduce the PAR of the complete data block. This approach though quite effective, is complex and requires significant signal processing. The second, called tone reservation [124] adds power to free carriers to reduce the PAR. The shortcoming of this technique is that it reduces the data rate, and wastes transmitted power.

Among the simpler and more practical techniques, clipping and companding are employed. In clipping, the OFDM signal is clipped at a certain predefined PAR level. This introduces in-band noise (increased bit error rate (BER)) as well as out of band noise (increased adjacent channel interference (ACI)). Due to its simplicity, the technique is attractive. However, the in-band noise and out-of-band emissions due to clipping must be contained within specified FCC limits. An improved technique suggested by Armstrong [26] clips and filters the signal several times while removing out of band spectral components after each clipping and filtering iteration. An improvement over [125] is proposed in [126] where the in-band and out-of-band components are simultaneously processed after clipping. The amount of clipping noise that can be tolerated without significantly affecting BER depends upon the amount of noise in the wireless communication channel.

In companding, instead of clipping the signal, it is companded intelligently i.e. the

smaller values of the signal are enhanced whereas the bigger values are suppressed, reducing PAR. At the receiver the signal is expanded using the reverse formula. As opposed to clipping, this doesn't add any noise to the signal if the channel is very good. The basic of them all is μ-law companding first proposed in [127]. Since then several companding techniques like A law companding, exponential companding etc. have been presented in [128], [129], [130], [131], [132], [133], [134], [135]. In [102] it has been shown μ-law performs better than A law regarding BER.

4.4.2. Adaptive PAR reduction

Traditional clipping/companding techniques for OFDM signals introduce in-band noise and/or reduce the signal-to-noise ratio (SNR) of the received signal rendering them susceptible to bit errors under noisy channel conditions. To avoid this, the clipping/companding level is set to a fixed value that accounts for the worst-case channel conditions for all allowable data transmission rates. Here, more aggressive PAR reduction techniques can be used adaptively, using available channel estimation techniques to drive the PAR adaptation. Among the above mentioned techniques companding is the most suitable for dynamically reducing the PAR depending on the environment, since it's simple and the amount of PAR reduction could be directly set by changing one parameter value. In this work we have used μ-law companding.

The dynamic PAR reduction block (Figure 63) compands the OFDM signal digitally in an adaptive manner (increasing the degree of compression as channel quality improves and vice versa) and use signal expanding (Figure 62) at the receiver to recover the original signal (as opposed to clipping in which signal information is lost) without violating received bit error rate (BER) threshold. The companding formula is given by:

$$x_{nc} = K \frac{sign(x) \times \ln\left[1 + \mu \left|\frac{x_n}{A}\right|\right]}{\ln[1+\mu]} \text{ where, } 0 \le \left|\frac{x_n}{A}\right| \le 1 \quad (47)$$

Where, x_n is the original signal, x_{nc} is the companded signal and A is a constant.

K is adjusted such that the RMS power of x_{nc} and x_n remains same. Receiver uses equation 2 for expanding the signal. All the barred quantities are for the receiver and have similar meaning as those for the corresponding quantities in the transmitter.

$$\tilde{x}_n = \tilde{K} \frac{\exp\left[\frac{\tilde{x}_{nc}}{\tilde{A} \times sign(x)} \ln[1+\mu]\right] - 1}{sign(x) \times \mu} \quad (48)$$

The amount of PAR reduction that can be achieved is dependent on the companding factor μ which in turn depends on the channel quality. The amount is also dependent on the modulation used. Figure 65 plots the PAR reduction achieved on a 256 WiMAX OFDM signal with varying μ for QPSK and 16 QAM modulations. It is to be noted that for very low values of μ (0.01) there is no companding at all and the amount of PAR reduction increases with increasing μ (e.g. 7.25 dB for μ=90 for QPSK).

4.4.3. Radio Link Quality

From (47) and (48), $\tilde{x}_n = x_n$ for an ideal RF stage and ideal channel. In other words, the signal can be companded by any factor and retrieved under ideal conditions. This relationship does not hold in the presence of circuit and radio link (channel) noise. The received signal becomes distorted when other real world factors such as multi-path, interference, and circuit non-linearities etc. are considered. To ascertain this relationship,

simulation studies are performed for varying channel conditions with different amount of noise, attenuation, fading and interference. The factors considered in channel modeling are explained below.

- The wireless channel attenuates the radio waves traveling through it and adds noise resulting in signal to noise ratio (SNR) degradation. This SNR degradation is modeled through attenuation and noise addition to the received signal.
- The radio signal experiences frequency selective fading in multi-path environment. This effect is modeled using an FIR filter. The length of the FIR filter determines the maximum delay spread in the channel.
- The modeling of adjacent channel and microwave interferers are performed with frequency drift, power drift and AM-PM modulation functionalities [136].

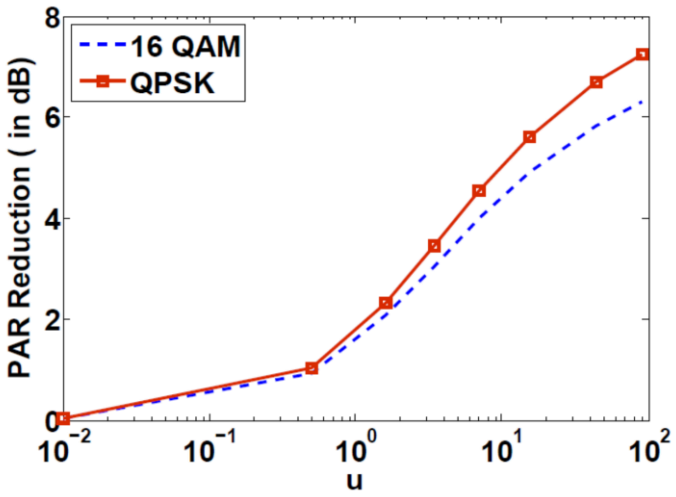


Figure 65: PAR reduction as a function of μ

4.4.4. Maximum Achievable PAR reduction under different environmental conditions adaaaaaaaaaaaaaaaaaaaaaa

A set of 12 channels (ranging from best to worst) was modeled by simultaneously perturbing SNR degradation, fading and interference parameters. As described in section

III, the degradation of the received signal due to these effects are accurately captured in Error Vector magnitude (EVM), which is computed in traditional wireless receivers.

For the absolute best channel the transceiver system operates at the highest modulation, i.e. 64 QAM for WiMAX MS (if supported). To maintain a BER less than 10^{-3}, which is acceptable for many wireless systems, it has been found that EVM <5% (for 64 QAM) is required. As the channel degrades the EVM increases and using built in data rate switching algorithms the transmitter reduces its modulation to 16 QAM to maintain a BER < 10^{-3}(BER threshold). As the channel continues to degrade, EVM further increases and the transmitter switches to QPSK and BPSK for EVM > 14 % and EVM > 35% respectively. It has been found from several repeated simulations of the complete transceiver system under different wireless channels that the full set of channels under which an adaptive data rate switching wireless system operates, can be divided into few subsets of channels each corresponding to one of the data rates/modulation. Each such subset contains variety of channels ranging from best to worst (defined by the EVM) for that particular data rate. Table 6 highlights this fact showing the channels used for this work. All EVM values are calculated without applying companding/expanding.

In this paper, the effect of OFDM-QPSK and OFDM-16 QAM has been studied, since these two are the mandatory modulation for a MS in WiMAX whereas 64 QAM is optional [104]. Also 64 QAM requires a very good radio link making the benefit due to linearity-power tradeoff minimal. Figure 66 shows PAR reduction and BER as a function of companding factor (μ) and EVM increase as a function of PAR reduction for good and moderate channels. Results have been shown for both QPSK (Figure 66 a, b) and 16 QAM (Figure 66 c, d) modulations.

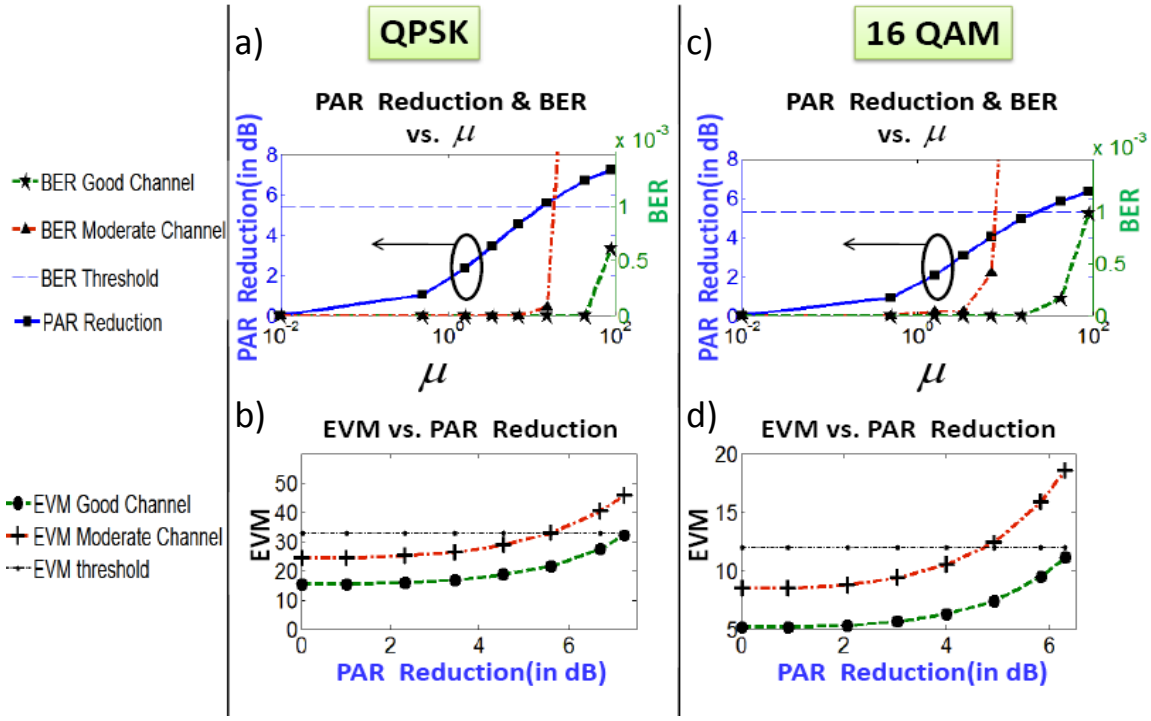


Figure 66: Maximum achievable PAR reductions under different channel conditions for QPSK and 16 QAM modulations

Figure 66a shows BER for good and moderate channels in dotted brown and green respectively. The blue horizontal line represents the BER threshold of the system. It also shows the PAR reduction with companding (blue solid line). Figure 66b shows corresponding EVM (brown and green) for both the channels along with $EVM_{threshold}$ (black dotted). Here $EVM_{threshold}$ is the EVM value corresponding to the BER threshold and is used as the threshold metric for system performance compliance. It can be seen that starting from the initial EVM value (defined by the channel) EVM increases as increased companding is applied to reduce PAR. BER does not increase up to certain inflection point and then increases rapidly (refer Figure 66a). The reason for no significant increase in BER initially is: though there is distortion present in the system due to companding, channel effects and HPA non-linearity, it is small compared to the

constellation boundaries resulting in most of the symbols being decoded properly. As EVM starts to come close to the EVM threshold (shown in Figure 66b) significant number of symbols start to be decoded improperly, resulting in sharp increase in BER.

Table 6: Channel Definition

Modulation	64 QAM	16 QAM (5% ≤ EVM ≤ 14%)			QPSK (14% ≤ EVM ≤ 35%)			BPSK
Channel	EVM <5%	Best	Moderate	Worst	Best	Moderate	Worst	EVM > 35%
EVM		5.15	8.5	12	15.5	24.4	32	

Hence, for each channel, companding can be increased until the point BER threshold is violated, i.e. EVM < $EVM_{threshold}$, as described in Section III. For a moderate channel in QPSK (dotted brown line in Figure 66a, b, also note Table 7) the BER threshold and hence $EVM_{threshold}$ is reached for a companding of 5.6 dB for μ=15.5 (blue solid line in Figure 66a). Hence for the moderate channel for QPSK, 5.6 dB of *PAR reduction can be achieved without any loss of received signal quality*. This adaptation is performed by increasing companding in a pre-defined increment as long as the EVM feedback "Bit value = 1" (Section III). Once this bit value becomes 0 the companding stops there indicating EVM = $EVM_{threshold}$. Thereafter the system hovers around that companding until the channel condition varies. From the graphs, it is observed that under favorable channel conditions, a PAR reduction of **7.25 dB** (QPSK) and **6.3 dB** (16 QAM) can be achieved without violating the BER threshold of 10^{-3}. Figure 66 also shows the BER for a moderate channel for which maximum achievable PAR reduction is found to

be 5.6 dB (QPSK) and 4 dB (16QAM). For worst case channel, where the initial EVM (i.e. EVM without companding/expanding) is close to the EVM threshold, minimum PAR reduction (μ=0.01) is used to maintain acceptable performance. Table 7 summarizes PAR reduction achievable for different channels along with the dynamic μ values used. It is clear that adaptive PAR reduction performs better than static techniques [125], [126] under most environmental conditions.

Table 7: Comparison of this work with traditional methods

PAR REDUCTION (dB)	THIS WORK						[125]	[126]
	QPSK			16 QAM			QPSK	
	Best	Moderate	Worst	Best	Moderate	Worst	Best	Best
	7.25	5.6	0.025	**6.3**	4	0.023	4.2	5
μ	90	15.5	0.01	90	7	0.01		

4.4.5. PAR Reduction: A closer look

The previous section reported how significant PAR reduction can be achieved when the system is adapted according to the surrounding environment within the modulation boundaries. This section takes a closer look at what enables the power savings. Figure 67a shows the SNR boundaries for adaptive data rate modulation in a typical WiMAX wireless system. These SNR boundaries translate to EVM boundaries as shown in Figure 67b. Depending on the radio link, the SNR and hence the corresponding EVM values determine the quality of the received signal at any point of time. Traditional systems employ data rate switching to increase the data rate if the channel is good (i.e. good channel implies lower EVM and vice versa). For example, modulation is changed adaptively (from 64-QAM to BPSK) in WiMAX (Figure 67a) as the channel quality degrades [137]. But *this discrete adaptation is still sub optimal as each data rate*

accommodates a range of channel conditions across which power cannot be modulated with fine granularity. For example, say for a given channel EVM is 15.5% (refer to Figure 67b). This system operates with QPSK signal modulation. However the QPSK operating regime extends from an EVM value of 15.5% to 33%, within which the system is static. The technique provides continuous adaptation for power and reduces the PAR of the OFDM signal until the system reaches the EVM threshold (33% for QPSK) Note that for a traditional system the transmitter would have stayed at 15.5% EVM and would not adapt within the QPSK range. As shown by arrows in Figure 67, in this case a 7.25 dB of PAR reduction in possible. Similarly, in the case of moderate channel for QPSK (initial EVM = 24.4%) 5.6 dB of PAR reduction is possible. *In essence, irrespective of the environment, the adaptive transmitter makes sure that the system is operating at the 'edge' of acceptable EVM value and hence maximum PAR reduction is achieved across a range of channel conditions, leading to significant power savings*.

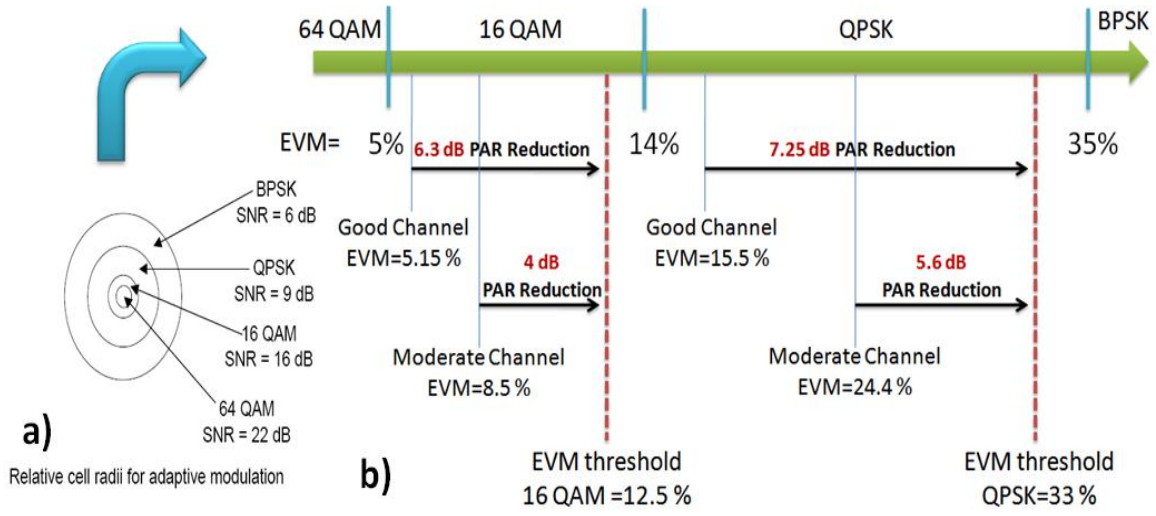


Figure 67: A closer look at the adaptation process

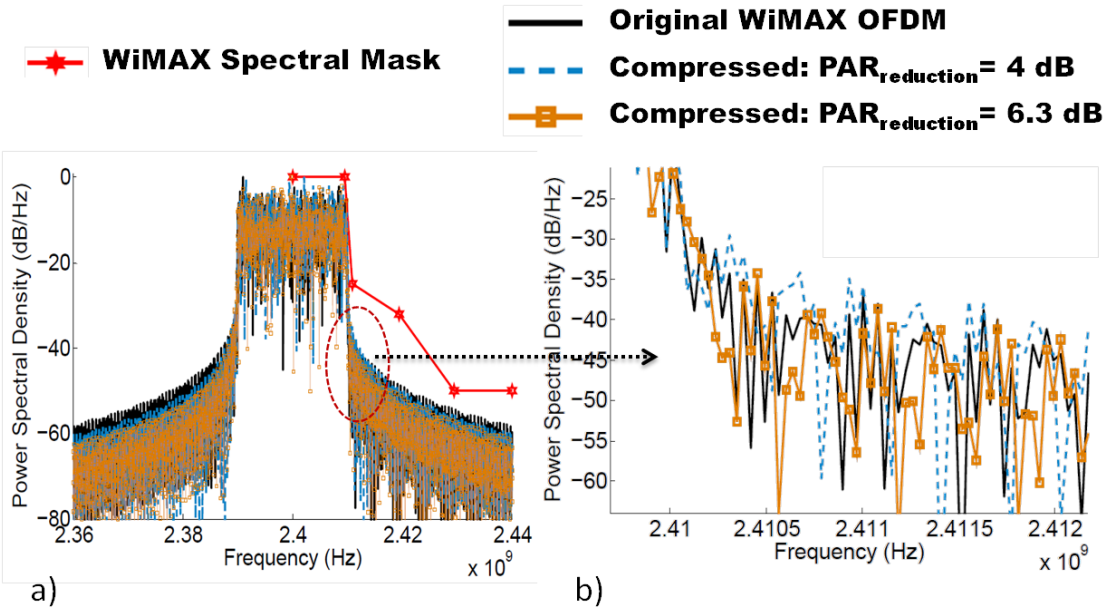


Figure 68: a) Out of band emission characterization b) Zoomed In

4.4.6. Out of band emission characterization

Companding of the transmitted OFDM signal may produce out-of-band components. The effect of the dynamic companding was studied to ensure that the FCC spectral mask conditions are met for all levels of companding. Figure 68 [13] shows the spectrum of a 16-QAM WiMAX (N=256) OFDM signal for the original as well as companded signal with two levels of companding (μ=7 and μ=90). It is observed that the out-of-band components though present, were under the limits imposed by the spectral mask conditions[104]. The out-of- band emission performance of the dynamic companding approach is better than that of the clipping technique in [125] which violates the spectral mask at specific frequency points [126].

4.5. Adaptive Power Amplifier

4.5.1. Adaptivity of Power Amplifiers

The gate and drain bias of the PA are tuned dynamically to trade off its 1 dB compression point (P1dB, a linearity metric) with DC power consumption. Practical implementation of such a dynamic biasing depends on sensitivity of the load impedance to these bias point changes. Power amplifiers can be adapted through modulation of their gate and drain bias (without using adaptive matching network) if and only if, for all the biasing conditions concerned, the matching requirements are relatively similar. A study of the required optimum load impedance for varying supply and bias is performed here. To validate the generality of the claims the study is repeated for two process technologies, namely a CMOS process and a GsAs HFET process. Table 8 shows the variation of the optimum load impedance (Z_{Lopt}) for MOS and GaAs HFET devices. The results for the MOS and GaAs HFET have been found by iterative load-pull and source-pull simulations in Agilent Advanced Design System on TSMC 0.25u CMOS process, and using measurements from load-pull experiment on *Sirenza Microdevices SHF-0289* (GaAs HFET), respectively.

Table 8: Optimum load impedance with adaptive biasing

	MOSFET			GAS HFET	
Vdd; Id	1.8 V; 24 mA	1.4 V; 18 mA	1.0V; 12mA	3V; 200mA	3V; 100mA
Z_{Lopt} (Ω)	*21.6+j23.2*	*21.1+j20.3*	*21.4+j18.3*	*15.2+j2.7*	*16.2+j2. 3*

The Z_{Lopt} for both the cases are also shown in the smith chart in Figure 69. The variations of Z_{Lopt} for different bias conditions are observed to be within ± 10% of its original value, which is within the limits of component tolerances for the matching

network, thus proving the feasibility of the approach. This observation means that even without load impedance modulation while adapting the PA, the mismatches would not be significant, allowing power savings.

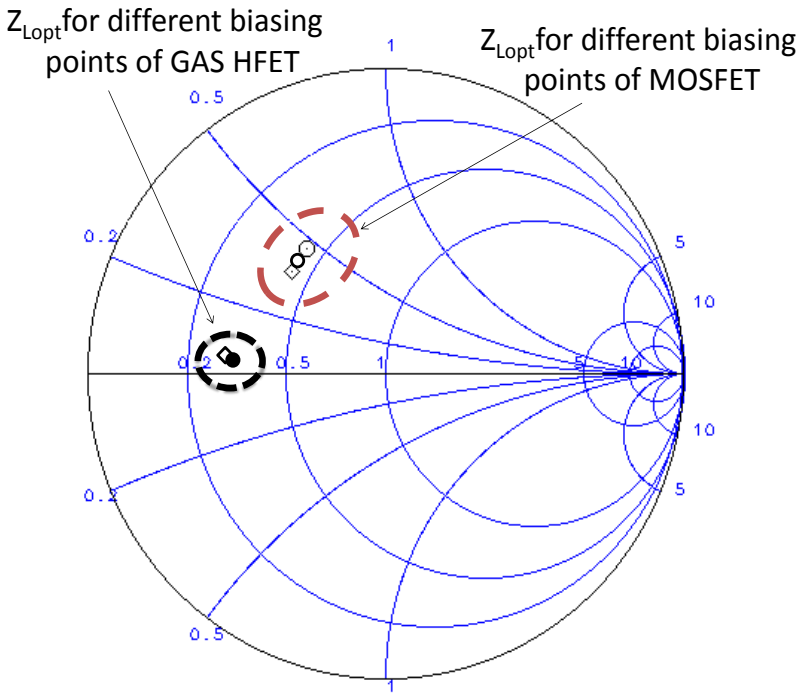


Figure 69: Z_{Lopt} for different bias conditions

4.5.2. Adaptive CMOS PA Design

An adaptive PA (2.4GHz, 16 dB gain) has been designed in TSMC 0.25µ CMOS process for class A operation. It is a simple one stage implementation as shown in Figure 70. The operating point trajectory for changing gate and drain bias voltages is shown in Figure 71. Lower values of biasing points reduce the signal swing, in turn reducing P1dB. But this reduction in P1dB allows reduced DC power consumption in the PA. Hence, depending on the channel conditions and companding of the baseband signal, when high P1dB is not required, the PA is operated at lower power consumption levels without compromising linearity. Higher power version of this PA can also be designed using

GaAs devices and can be adapted similarly.

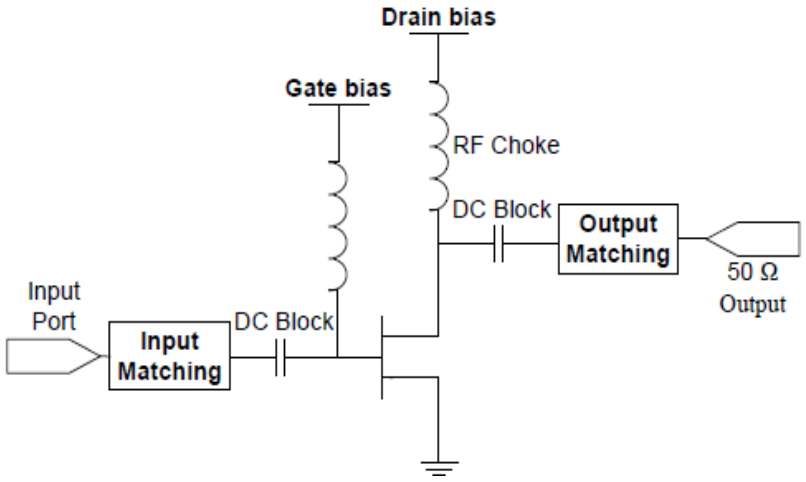


Figure 70: Simplified schematic of 1-stage PA

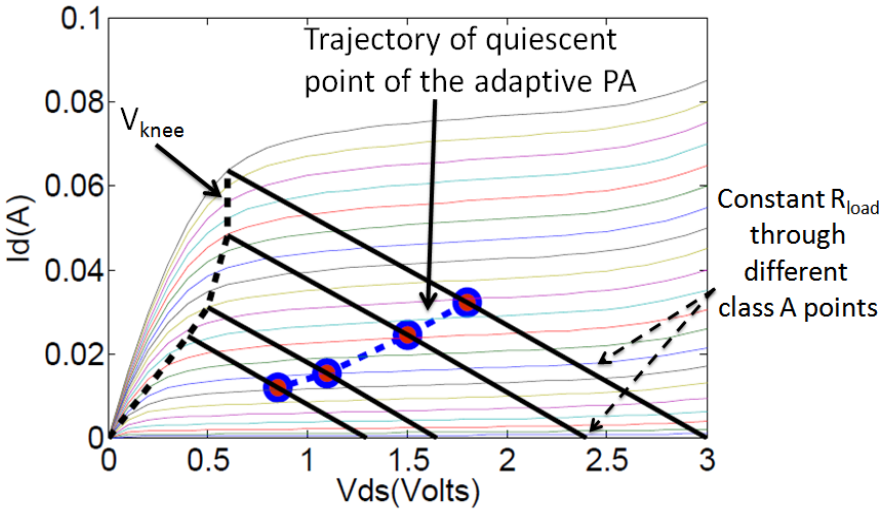


Figure 71: Trajectory of bias points of adaptive PA

4.5.3. Power savings

Figure 72 shows the Gain and Power Added Efficiency (PAE) curves with input power for the 4 states (S1 to S4) of the PA, highlighted in Figure 71 (increasing state relates to lower power operation of the PA). It is to be noted that for power levels below P1dB of a

static PA (state 1) the PAE increases with adaptation as we go to low power states (state 2, 3 and 4 respectively).

The P1dB and DC power consumption of the adaptive PA and comparable static PA across the different bias points has been shown in Figure 73. The average output power of the MS PA changes depending upon its distance from base station and the quality of the radio-link. P_{avg}_r signifies this *reduction of average output power* compared to its maximum value. *PAR_r* signify the maximum possible *reduction in PAR of OFDM signal* for any given channel through dynamic companding (section IV D). The reduction in average output power and PAR both relax the P1dB requirement of the PA (Equation 3). *P1dB_r* signifies *the total relaxation in P1dB* of the adaptive PA. The drain (V_d) and gate (V_g) voltage is dynamically set depending upon required P1dB reduction through a Look up Table (LUT), which define the locus for reduction of supply and gate bias such that the class of the PA is maintained (refer Figure 71). In real-time, the system follows this locus using the receiver EVM feedback information with predefined increment to save power. For a P1dB reduction of 9 dB, the DC power consumption reduces from 58mW to 11mW is observed providing 82.75 % (or 5.27×) power savings.

$$P1dB\_r = P_{avg}\_r + PAR\_r \tag{49}$$

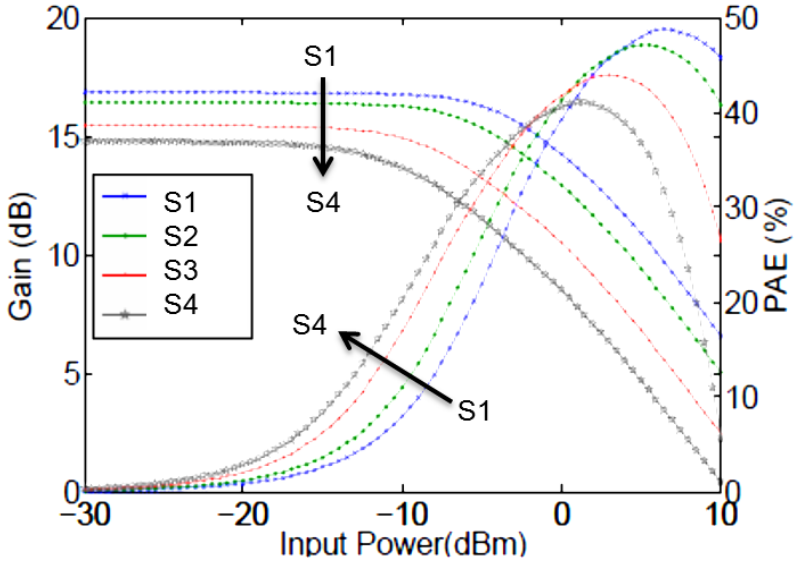


Figure 72: Gain and PAE in different states of the adaptive PA

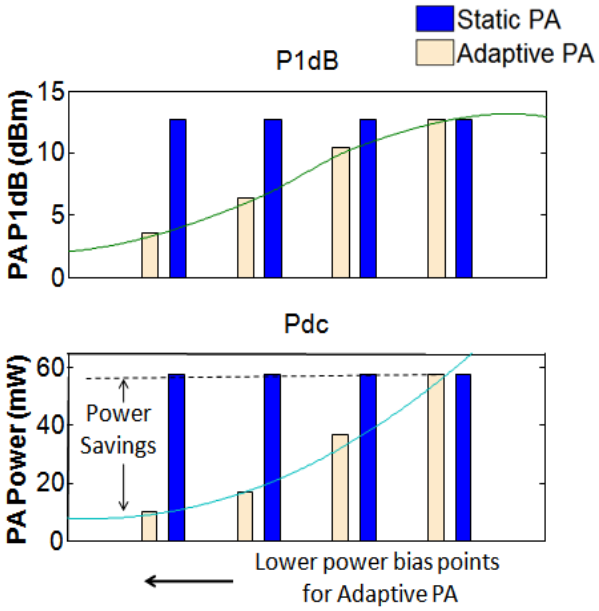


Figure 73: Power savings through PA adaptation

The LUT described above is design specific and is derived from the data taken during alignment/characterization phase. Hence the voltage values are for nominal conditions. A feedback control loop could be used as in [105] to maintain correct biasing and hence output power under non-nominal conditions.

4.6. HARDWARE VALIDATION

4.6.1. Experimental Setup

Figure 74a and b shows the setup for experimental validation of this approach and the simplified schematic of the *Adaptive PA*, respectively. Matlab environment in a computer is used as the baseband. Random data bits are QPSK OFDM modulated and sent out using National Instruments Data Acquisition Card (NI DAQ). An off the shelf up converting mixer (RFMD 2638) up converts the signal to 2.4GHz, which is passed through a custom designed *Adaptive PA*. The receiver consists of a Low Noise Amplifier (LNA) and a passive down conversion mixer (Mini Circuits Z X05-5). A RF signal source is used to produce the LO signal for both up and down converting mixer. The down converted data is sampled using NI DAQ and demodulated in Matlab. EVM is calculated in the baseband. The PAR of the transmitted signal is also controlled through Matlab. The transmitter output is attenuated, added with noise generated by a noise source (using a Wilkinson power combiner) and fed back to the receiver input. This simulates the attenuation and noise added by channel during actual operation. The two stage *Adaptive PA* is designed with Sirenza Microdevices SHF 0289 GaAs HFET device and discrete components. It has an operating frequency range from 2.3 to 2.7 GHz, gain of 10 dB, P1dB > 23dBm, efficiency of 30 %. It features separate gate and drain control voltages for adaptation purposes. The PA can maintain its class of operation while its power consumption is reduced if proper biasing is applied.

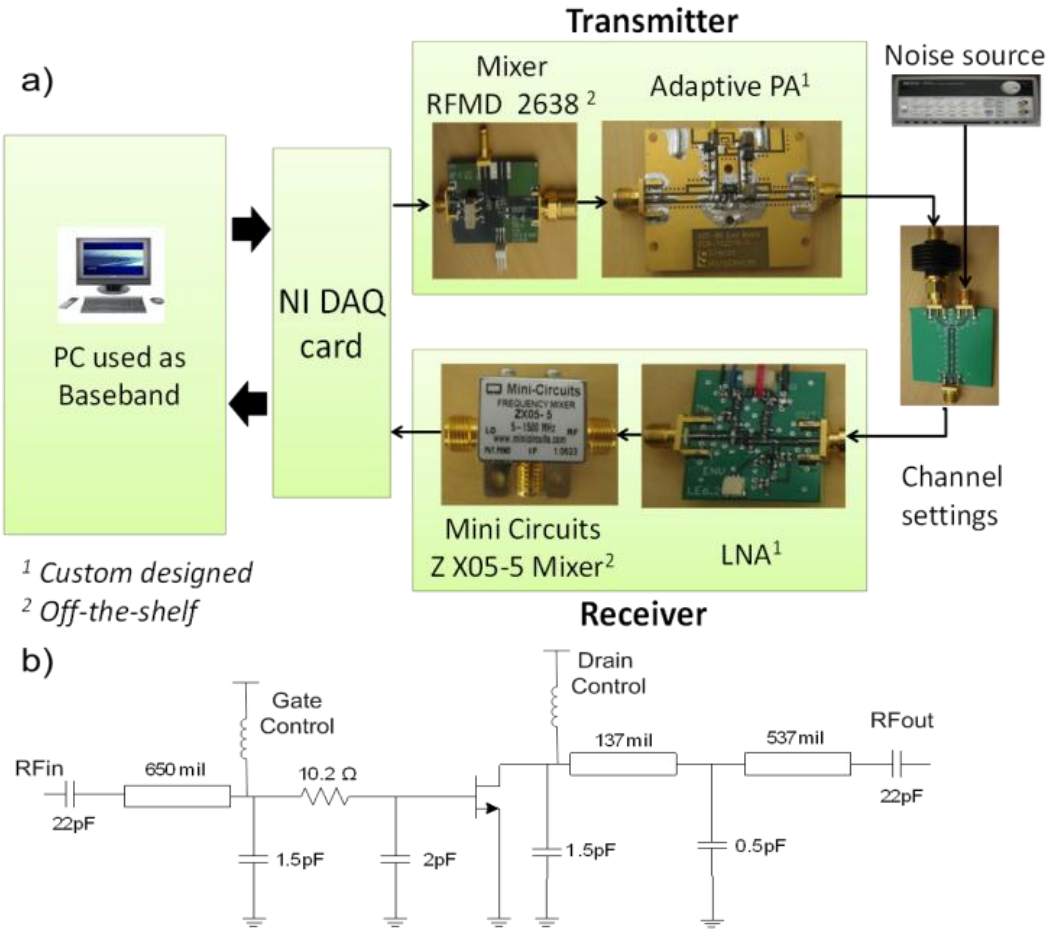


Figure 74: a) Experimental setup b) Simplified schematic of Adaptive PA

4.6.2. Results

The system is operated with QPSK OFDM modulation. According to section IV the system could support EVM from 14% to 35% with acceptable BER. First, the system is operated without any PAR reduction. EVM is found to increase with worsening channel as expected. Now for a fixed channel (constant attenuation and noise addition), PAR reduction is gradually increased. Figure 75a shows such a case for a *good channel*. Without PAR reduction EVM was 17 %. As we increase PAR reduction EVM starts increasing first gradually, then in a rather steep manner. It can be seen that for a EVM threshold of 33% more than 7 dB of PAR reduction is possible.

The custom designed *Adaptive PA* was characterized for its 1dB compression point (P1dB) at different biasing points ie. different DC power consumptions (Pdc). Figure 75b plots this P1dB vs. Pdc curve. It shows more than 9 dB adaptability in P1dB (23.5 dBm to 14 dBm) as power disspitation goes down from 912 mW to 150 mW.

Generally, there is a VGA in the receiver which equalize for the variable input power of the received signal as long as it's within the operating power range of the receiver (more than its sensitivity and less than its blocking power). Traditional PA's which adapt for its output power tries to make sure that the received power is within this range. But it does not pay any attention to *received signal quality*. Bit errors are caused not only because of the low received signal strength; it can also happen at higher signal strength due to noise, interference multi-path effects etc. This work monitors the complete quality of the received signal by monitoring EVM and exploits it to reduce PA output power even further than traditional PAs when received signal quality is good (as shown in Figure 76).

For example, let us consider a scenario where due to reduced attenuation in the channel the output power of the traditional PA could be reduced by 2dB (the channel is good). The post reduction EVM at the receiver is 17.2 % as shown in Figure 75a. Using the adaptation technique developed here, we can achieve another 7 dB of PAR reduction as EVM goes from 17.2% to 33%. Compared to a 1.5X savings (23.5 dBm → 21.5 dBm => 912 mW →590 mW) in traditional adaptive output power PA, the concurrent adaptation technique allows a savings of ***5.5*×** ((23.5 dBm → 14.5 dBm => 912 mW → 165 mW). Hence, ***dynamic PAR reduction and PA re-biasing*** allows an extra savings of **3.6×** (590 mW → 165 mW), as shown in Figure 76. The savings reported above is best

case savings. In worst case, i.e. when channel is very bad, PA would switch back to highest power to have maximum linearity (no power savings) as in case of traditional adaptive output power PA.

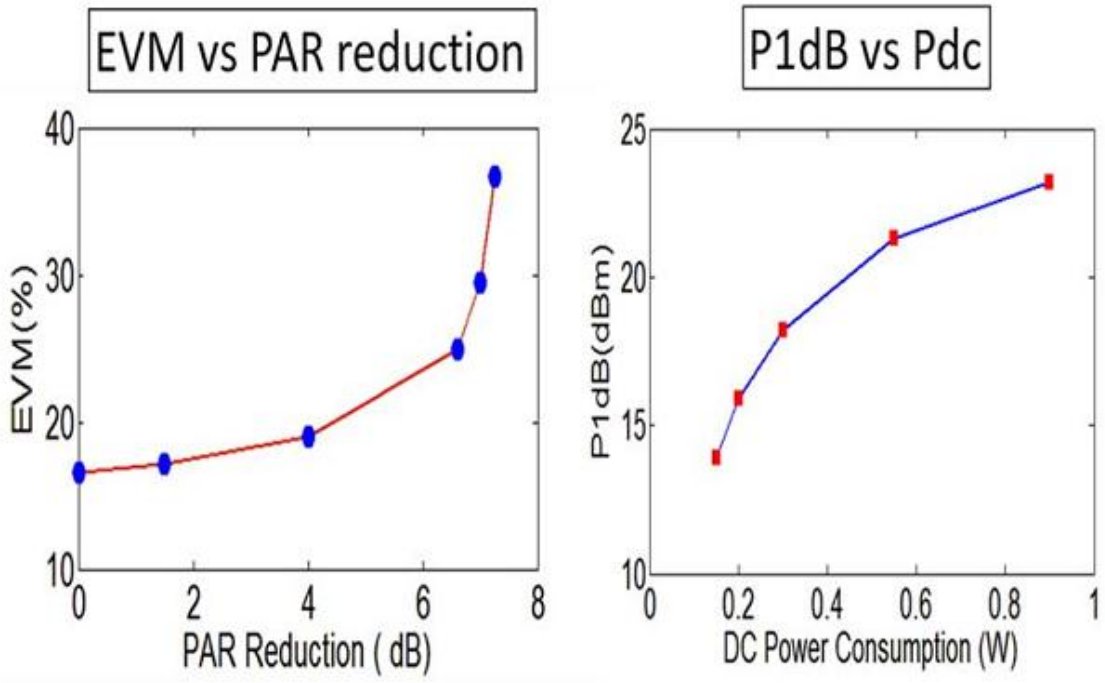


Figure 75: Experimental results: a) EVM vs. PAR b) P1dB vs. Pdc

Table 9: Extra Power Savings under different channel

	QPSK			16-QAM		
Channel Quality	Good	Moderate	Worst	Good	Moderate	Worst
PAR Reduction (dB)	7	5.6	0	6.3	4	0
P1dB required (dBm)	23.5-(2+7)= 14.5	23.5-(2+5.6)= 15.9	23.5	23.5-(2+6.3)= 15.2	23.5-(2+5.6)= 17.5	23.5
Pdc (mW)	165	180	912	200	260	912
Extra Power Savings*	3.6×	3.27×	0	2.95×	2.27×	0

*(*Assuming output power reduction of 2dB for illustrative purposes)*

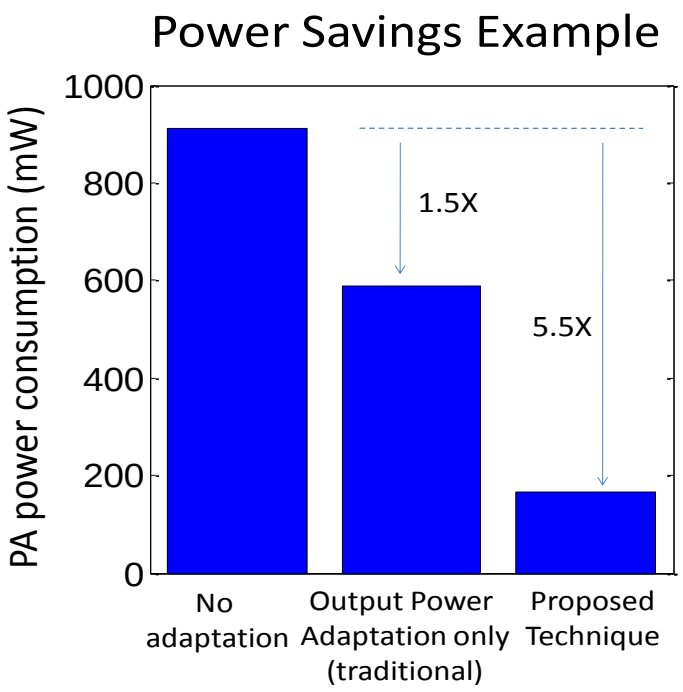


Figure 76: Comparison of power savings

The power savings possible for the designed adaptive PA for different channel conditions are summarized in Table 9.

4.6.3. Discussions and Summary

Implementation of the *dynamic PAR reduction and PA re-biasing* technique involves two kinds of overhead: a dynamic PAR reduction block and an adaptive PA. Adaptive PAs also require a power management unit that can adapt its output voltage according to some input control bits from the baseband. Traditional systems already employ variable output power PAs as described in section VI. So no significant extra hardware or power is required to use these PA. In traditional system we do have a PAR reduction block, but it is static. We assume varying the μ of such PAR reduction block dynamically would introduce insignificant power overhead compared to the amount of

power saved in the PA. (as the PA power consumption is much more compared to the power required for implementing a simple digital function in the baseband (Figure 62).

The experimental results assumed a 2 dB average output power reduction for illustrative purposes. In reality, the average output power variation is also channel-dependent and can vary between a wide range [109], depending upon standard and implementation. Under an increased output power control range the percentage of total power savings from average output power control would increase. However the extra power savings achieved by the dynamic PAR reduction technique remains the same.

In summary, a system level approach for environmental adaptation of power conscious OFDM transmitters is developed. It employs channel dependent dynamic digital PAR reduction in conjunction with adaptive re-biasing of the Power Amplifier. The adaptation approach aggressively exploits the built-in design margins in RF transmitters to achieve significant power savings across varying channel conditions. Hardware experiments show a 5.5× savings compared to 1.5× savings in traditional methods with only average output power control. Simulation and hardware results demonstrate the feasibility of the proposed framework making a strong case for implementation in future multi-mode multi-standard radios.

Chapter 5. ENVIRONMENT ADAPTIVE VIRTUALLY ZERO MARGIN LOW POWER RF (VIZOR) RECEIVER SYSTEMS

This chapter deals with design of environment (channel) adaptive wireless systems for low power operation. An adaptive receiver, its associated algorithms, tunable circuits and system level algorithms controlling real-time adaptation is shown. A jammer detector design for adaptation to jammer/blockers in the channel is also presented. Finally application of such an environment adaptive systems to MIMO receivers is described.

A. Need for Environment Adaptive Wireless Systems

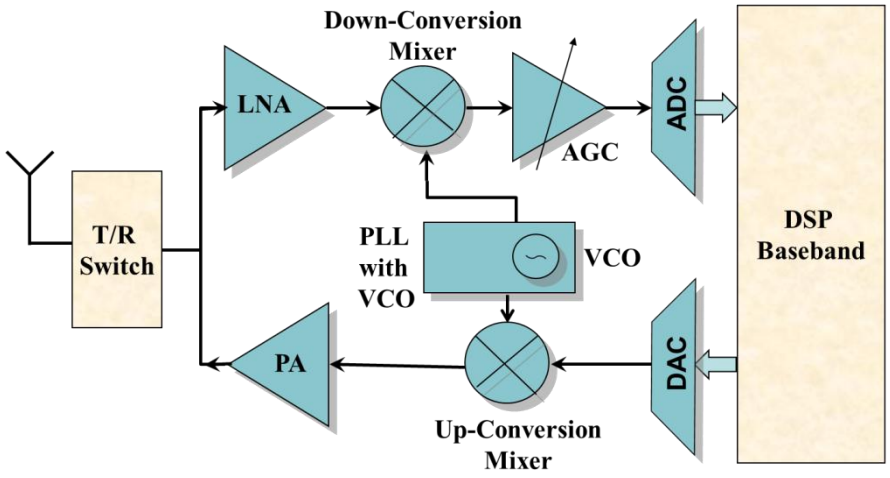


Figure 77: Mobile Radio Transmitter and Receiver

Most of the modern portable systems include a radio for wireless communication. The key difference between non-wireless portable systems and portable wireless systems is that wireless these systems have to transmit and receive through a channel, which keeps on varying. Hence these systems need to operate at highest performance when the environment is at its worst. Static systems would waste a lot of power as they would over perform when the environment (channel) is better than its worsts case condition. One way

to increase battery life of these systems is to design low power circuits and efficient algorithms. But static low power systems are still non optimum in terms of efficiency. Power efficient wireless systems can be designed by adapting the system and the underlying circuits as the environment changes, to deliver just the required amount of power.

Figure 77 shows a simplified block diagram of a wireless radio transceiver system. A digital baseband DSP sends data to be transmitted through the Digital to Analog Converter (DAC) to the Analog/RF portion of the transmitter. An upconversion mixer up converts the low frequency data to Radio Frequencies (RF) signal for transmission. A Power Amplifier (PA) boosts up the RF signal power and transmits is through the antenna. The Transmit Receive Switch (T/R Switch) selects signals to be transmitted from the transmitter or to be received and sent to the receiver. In receive mode the weak received signal is amplified by the Low Noise Amplifier (LNA) and then down converted to lower frequency by the down conversion mixer. It is then sampled by the Analog to Digital Converter (ADC) and sent to baseband for further processing. A Phase Locked Loop (PLL) including a Voltage Controlled Oscillator (VCO) provides the mixers with required Local Oscillator signals.

The above described architecture is called Direct Conversion Receiver as the low frequency data is directly upconverted to RF frequencies without any intermediate stage. It is very commonly used in wireless radios and would be used in several occasions throughout this chapter.

The trend in low power Analog/RF systems is twofold. One is to design circuits with inherent low power consumption. The second is to adapt those circuits over process,

temperature, environment, workload etc. This leads us to complete system level adaptation of wireless front ends using end to end metrics for ensuring performance. These systems are called Virtually Zero Margin RF (VIZOR) as they thrive to take out the built in design margins that is a must in static circuits and systems. The rest of this chapter is dedicated towards describing VIZOR systems, receiver and transmitter implementation.

B. Dynamic Supply Voltage Scaling for RF receiver: Concept

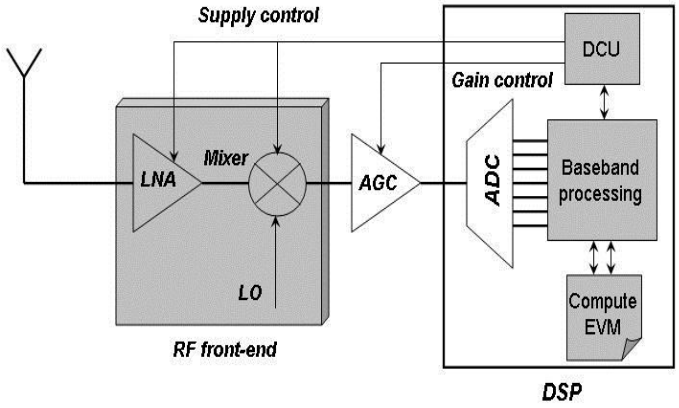


Figure 78:.Adaptation approach: Dynamic Supply Voltage Control (DSVC)

The conceptual diagram for the adaptive system using Dynamic Supply Voltage Control (DSVC) is shown in Figure 78. The details of the adaptation methodology are shown in the next section. The supply voltage is continuously scaled down to reduce power consumption of the device. With the scaling down of the supply voltage, the system-level adaptation metric (for example EVM, detailed in next section) is expected to worsen as shown in Figure 79. This is allowed to continue as long as the metric is within certain pre-defined threshold value. After this, the power supply is increased in steps until the system-level metric is satisfied. By allowing the system to dynamically adapt this

way, the V_{supply} of the system hovers around the lowest possible value for which received signal quality meets the required specifications. Thus, this scheme achieves significant power savings by operating the system at the optimum supply voltage. The design margin is reduced through the above mentioned dynamic control loop between the RF front-end and the baseband processor. For a given channel, the adaptation approach strives to operate the device with the lowest supply voltage while maintaining the system specification.

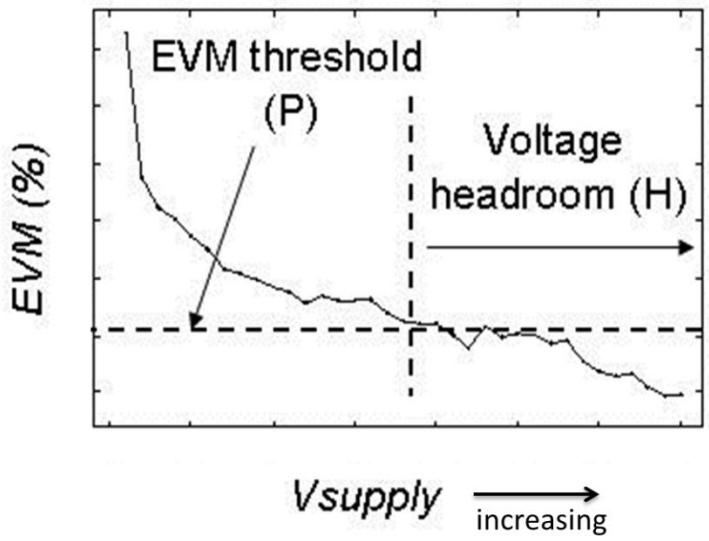


Figure 79:.EVM vs. supply voltage variation.

Figure 79 shows the variation of EVM with supply voltage for a typical RF receiver. It is observed that the EVM varies significantly with the supply voltage. As expected, the EVM degrades as the supply voltage is reduced from its nominal. The degradation is slow at first, but degrades faster as the supply voltage continues to be reduced. If the threshold value of EVM is set to a particular value *P*, the supply voltage headroom is given by *H*. Thus, implementing a dynamic control loop would allow the optimal operation of the system such that the EVM metric is below *P*. The adaptation

approach implements DSVC to achieve minimum power operation of the device using the above mentioned concept.

5.1. VIZOR Receiver

5.1.1. Low Power Adaptation Framework

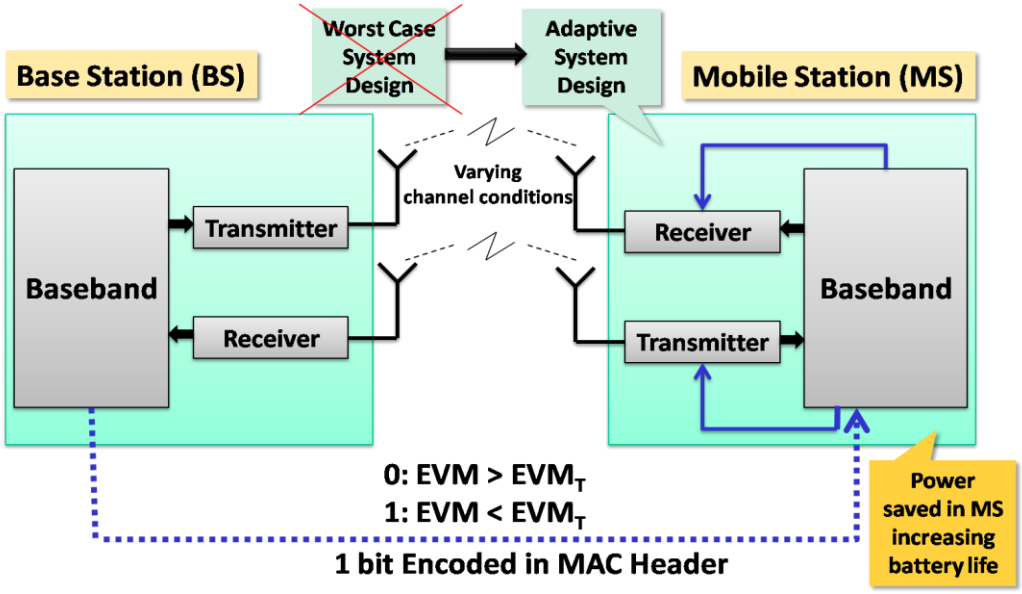


Figure 80: System Level Adaptation Framework

The overall framework for transceiver adaptation is shown in Figure 80. The mobile station (MS) is the point of interest where power consumption is minimized to increase battery lifetime using adaptation in both the transmitter and receiver. A real-time system-level adaptation approach for a tunable wireless transceiver, driven by closed-loop feedback control based on an adaptation metric is presented here. This *metric* (in this case illustrated via Error Vector Magnitude (EVM) of the received symbols) exhibits strong statistical correlation with Bit Error Rate (BER), i.e. usually used for characterizing the performance of a wireless link. The feedback control of the wireless device is designed so that this EVM value is always close to a specified upper limit

irrespective of channel (environment) conditions. The EVM is calculated in the MS receiver baseband, and this information is used to govern the tuning of the receiver. Performance of the receiver is increased if calculated EVM is greater than the threshold EVM (E_T) (corresponding to the maximum BER), and vice versa. The EVM always hovers around its threshold value, providing just enough power to the system to maintain desired performance. In contrast the MS transmitter performance is tracked by computing the EVM in the baseband of the BS, as described in details in the previous chapter. To facilitate power versus performance tradeoff of the MS transmitter, this EVM information has to be delivered to the MS from the BS. This is achieved by encoding the information into the MAC header of the next data packet transmitted from BS to MS. The assumption here is the environment changes slowly compared to the duration of the packets, which is valid for a majority of the time that the device is in operation. To keep the transmitted MAC bit overhead minimum only 1 bit reporting scheme is adopted. The BS sends back 0 or 1 depending on EVM is greater or lesser than EVM_T respectively. Using this information the MS baseband controls the tuning of the MS transmitter. Both the transmitter and receiver adaptation is performed in a standard compliant manner from data rate perspective, meaning the adaptation algorithm works in conjunction with higher level data rate switching protocol and strives to operate at minimum power by operating the system close EVM_T (different for different modulation) for any given data rate. A comprehensive system-level framework is presented that tunes multiple system control 'knobs' that include RF and digital blocks. A control law running on the baseband processor tunes these knobs while simultaneously performing baseband compensation on the received data to save power across all operating conditions without compromising the

BER specification. Thus, by dynamically trading off performance (when not required) such an *Adaptive System* [139][140][141][142] shows significant power savings compared to *Worst Case Systems*.

5.1.2. A Suitable Adaptation Metric: EVM

The key issues to be considered in developing a dynamic feedback-driven power control for wireless systems include defining a suitable adaptation metric and the acceptance bounds on this metric for satisfactory operation. This metric should provide the best indication of the system performance under all possible environmental conditions and should be estimated in run-time. Bit Error Rate (BER), i.e. the number of received erroneous bits, is traditionally used to characterize the received signal performance. However, BER of a typical wireless transceiver is about 10^{-4} to 10^{-6}, i.e. 1 bit error in 10^{6} bits. It leads to the requirement of transmitting hundreds of millions of bits to ascertain the BER of the system, making BER a non-real-time metric and cannot be used for adaptation receiver adaptation for our purpose where channel changes in the order of seconds or lesser.

A different metric is needed that has good correlation with BER and can be calculated in real-time. Error Vector Magnitude (EVM) fits the requirements. EVM quantifies the difference (error vector) between the transmitted and received symbols at the baseband as shown in Figure 81.

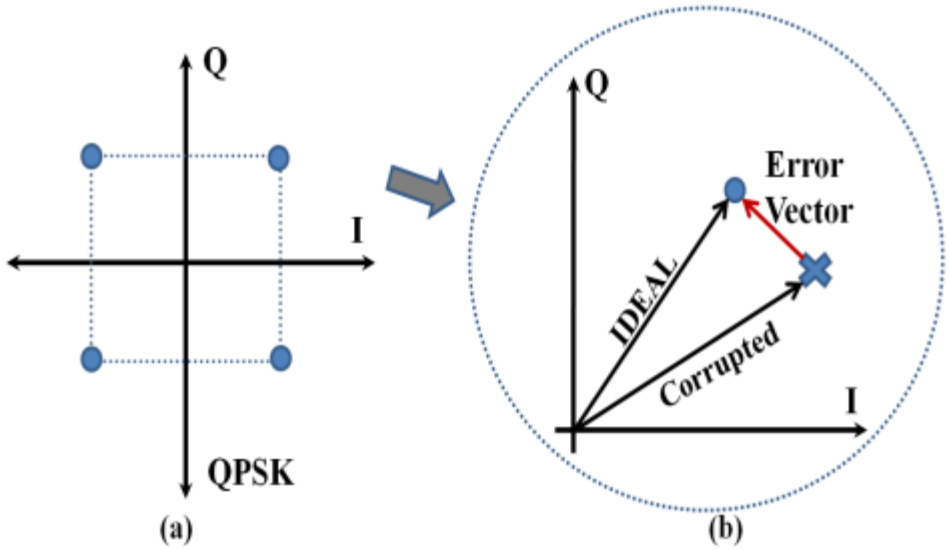


Figure 81: (a) Constellation plot for QPSK, (b) Error vector for a transmitted and received symbol in the 1st quadrant, the rms of the error vectors over several symbols provides EVM

The above definition of EVM is general and is applicable to both single and multiple-carrier systems. It provides a simple and useful metric for measuring the quality of digitally modulated signals. It is integrated into several existing and upcoming communication standards. It can be defined by the following equation (also presented in Chapter 4).

$$EVM = \sqrt{\frac{1}{N}\frac{\sum_{1}^{N}\|y_i - x_i\|^2}{\|y_{\max}\|^2}} \tag{50}$$

where,

y_i = Received complex data (I+jQ),

x_i = Transmitted complex data (I+jQ),

y_{max} = Outermost data point in the constellation diagram,

N = Number of complex data points used for computation,

where N is sufficiently large.

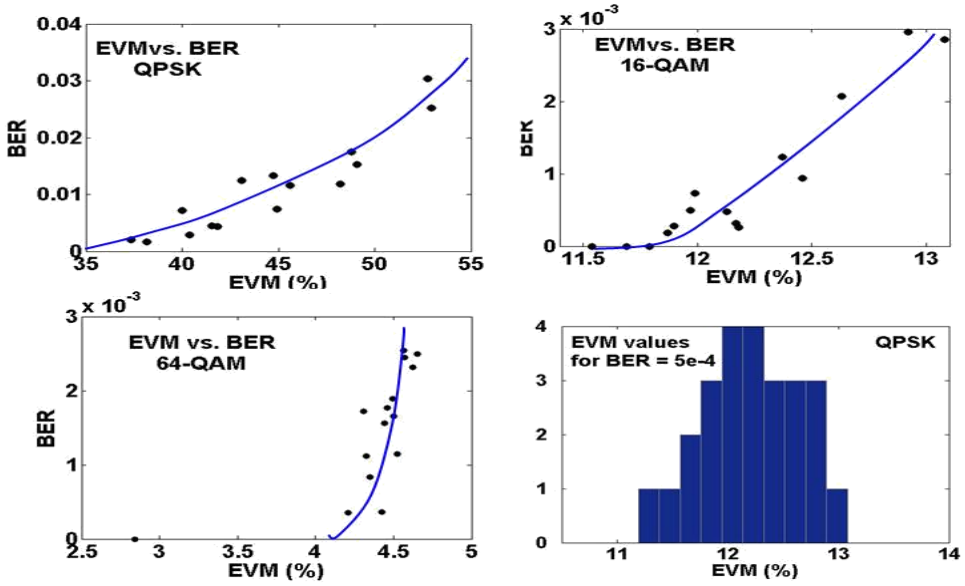


Figure 82: EVM vs. BER relations for QPSK, 16-QAM, 64-QAM and EVM threshold estimation for QPSK

The received signal passes through all the receiver components before it is demodulated and decoded in the baseband processor. The EVM specification therefore captures the *cumulative effect* of the environment such as attenuation, interference, multipath fading etc. as well as all the circuit-level specifications such as gain, non-linearity, noise figure, input/output match, ADC resolution etc. EVM computation is a byproduct of the normal baseband processing and represents minimal hardware/power overhead. Figure 82 shows the relation between EVM and BER for three modulation scheme, namely QPSK, 16-QAM and 64-QAM. It also shows the variance in this metric for guard band estimation purposes. A good correlation between these metrics and a low variance allows using EVM as the adaptation metric. For example, if BER bound is set at

1e-3, the corresponding mean EVM bound for the QPSK and 16-QAM cases can be approximated to about 35% and 12.5%, respectively.

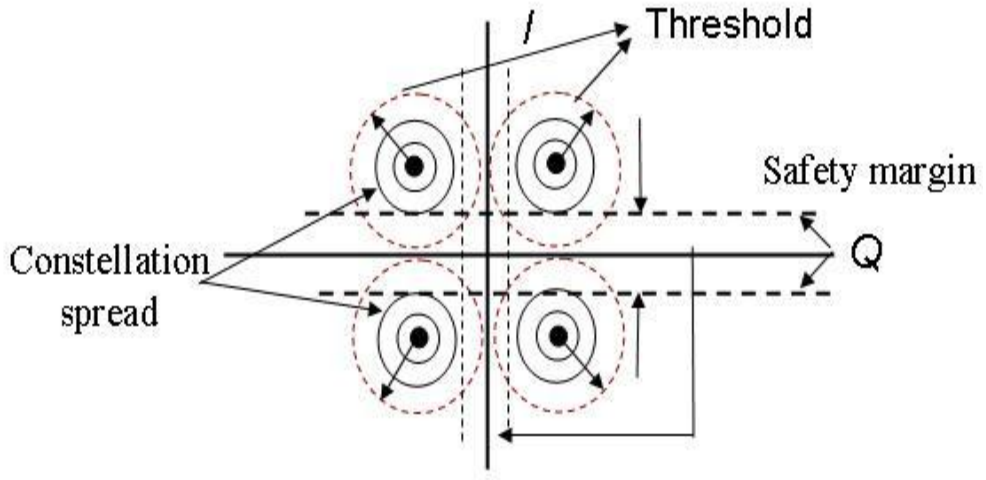


Figure 83: Feedback control: QPSK constellation viewpoint

Figure 2a shows the constellation diagram for QPSK encoded symbols. As the channel conditions and receiver performance is degraded to save power, the constellation points for each symbol lie inside circles of increasing size, corresponding to increasing EVM. When the circles cross the horizontal and vertical constellation boundaries, the received symbols are decoded incorrectly and bit errors occur. Theoretically, one could leave a safety margin and operate within the largest circle determined by the safety margin without causing bit errors. However, even for conservative designs, periodic bit errors do occur in practice. Hence, the safety margin is determined by the maximum specified bit error rate (BER). Under feedback control, the receiver will operate within the boundary of the largest circle not crossing the specified safety margin for the constellation diagram. . Figure 82 shows the EVM vs. BER curve for the system. This has been used to set the EVM limit (33%) for a specified BER (5×10^{-4}). The guard band

can be estimated by repeated system simulation to find the uncertainty window in EVM calculation and can be <2% in this case as shown in Figure 82.

5.1.3. Adaptive Receiver Design Framework

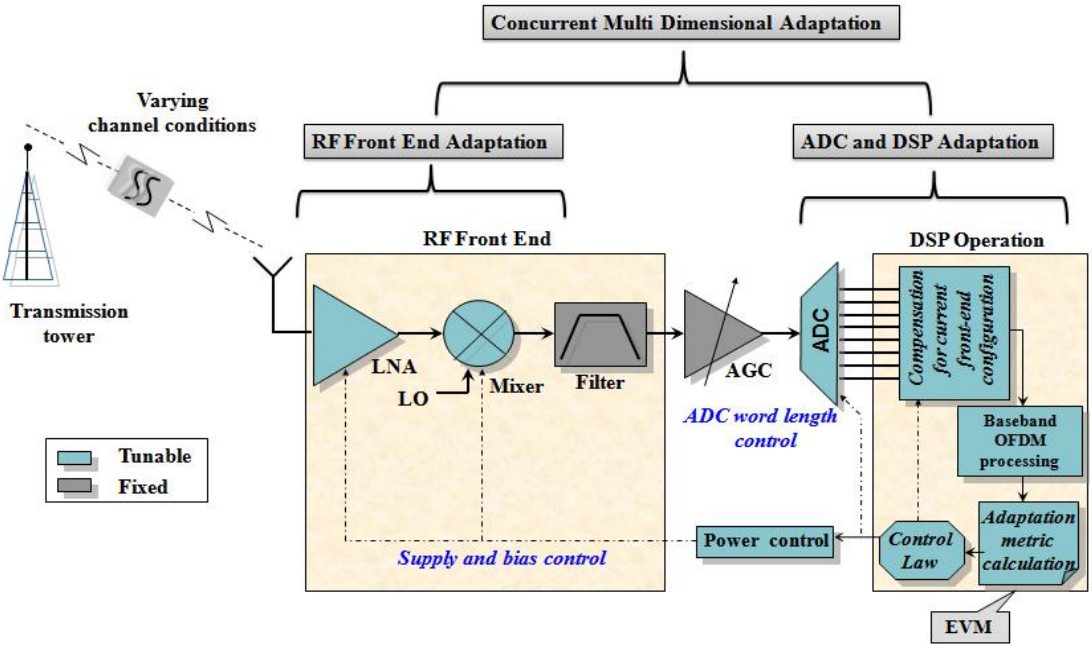


Figure 84: Adaptive Receiver Framework

Figure 84 shows the components of the Adaptive Receiver. It consists of both tunable RF components (LNA, mixer) as well as a tunable mixed signal block (ADC). The tunable supply/bias voltages for LNA and mixer, along with the tunable analog-to-digital converter (ADC) word length serve as control 'knobs' for EVM-based feedback control. These tuning knobs provide a way to reduce performance for reduced power operation of the above mentioned blocks. The transmitted signal from the tower goes through a varying channel and passes through the receiver and gets sampled by the ADC. In the DSP, the sampled signal is compensated for known (pre-characterized) non-ideality of the current front end configuration and passed though baseband OFDM processor, which calculates EVM as a byproduct. If the EVM is less than the EVM

threshold for the current modulation the power control block reduces the tuning knobs of the tunable components following a predefined *control law* to save power. This control law defines how all the 'knobs' change in relation to each other when the receiver performance is being turned down. This calls for a multi-dimensional tuning algorithm that optimizes how the knobs should change (i.e. the *control law*) in design phase and applies it to the adaptive receiver in run time to guarantee optimum performance of a nominal adaptive receiver.

5.1.4. Design Phase Optimization

During the design phase, a multi-dimensional optimization algorithm is used to determine a *Minimum Power and Maximum EVM locus* (that defines how to turn down the 'knobs' with respect to each other). A set of channel conditions ranging from good to bad are modeled for use in the optimization procedure. The channel parameters (interference, multipath, attenuation) are perturbed to obtain channels ranging from good (low EVM) to bad (high EVM). For each of these channel conditions, the optimal settings for control 'knobs' are computed through a multi-dimensional optimization procedure as described below. Each optimized point refers to a set of knob values that provides the optimum power for the given channel and is a point on the locus (refer Figure 85). The set of all points for all the channels define the optimum *control law*.

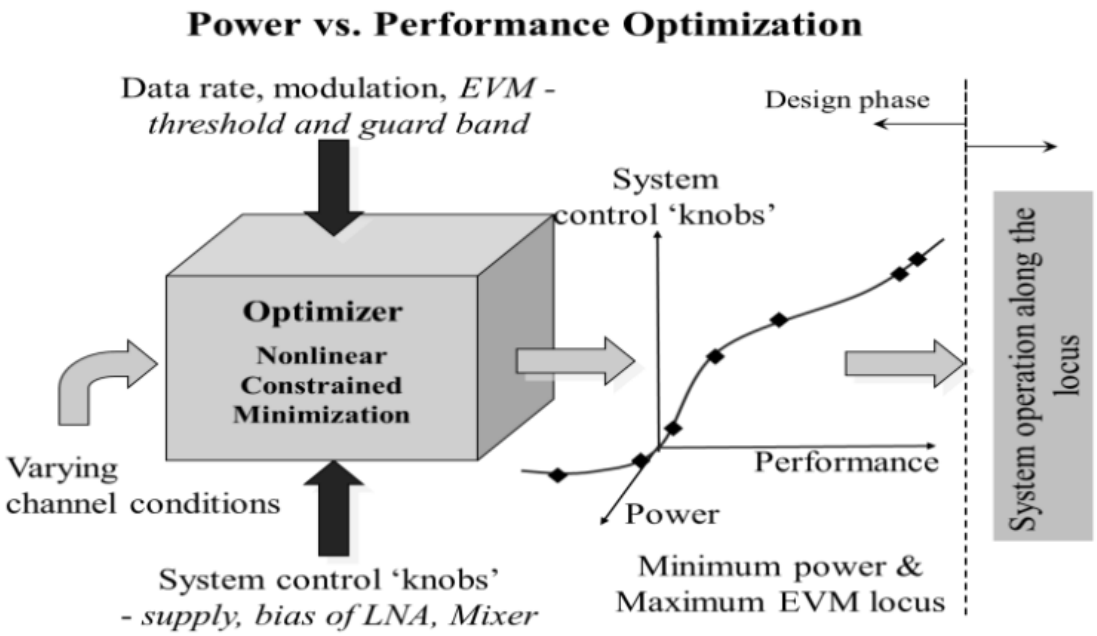


Figure 85: Receiver Power Optimization

Development Optimal Control Law

The goal of the optimization algorithm is to find the control knob settings for each channel that would allow EVM $<E_T$ with minimum power consumption. This can be achieved by using a *constrained optimization (minimization)*, with EVM $<E_T$ being the *constraint* and power being the objective function. The development of the optimal power control law (*locus*) is summarized below:

Input: Maximum allowed EVM (E_T) for each signal modulation (QPSK, QAM-16,-64).

Constraint: $EVM \leq E_T - guard\ band$

Objective Function: *Power Consumption to be minimized*

Goal: For each signal modulation and channel, find V_{dd}, V_b, = *f(channel quality)* such that power is minimized and EVM constraint is satisfied.

A constrained minimization algorithm *(MATLAB: fmincon)* is used to obtain the optimal locus. It is done as follows:

1. For a given channel, the optimal set of control knobs (V_{dd}, V_{bias} or W) is found from the optimizer that satisfies the EVM constraint with minimum power.
2. A table of these voltage values obtained across a range of channel conditions defines an *optimal locus* of points in an N-dimensional space for N available tuning knobs. This forms the locus that is programmed in the device and used in run time.

During run time, the control law forces continuous adaptation of the device to minimize power while meeting the BER constraint at all data rates and channel conditions. This is done by operating the system along the optimal locus of the control knob settings obtained from the optimization procedure. The threshold and guard band for EVM (feedback) is set based on the estimated channel quality and current data rate. In our approach, the voltage scaling is performed independently for each modulation in a standard-compliant manner such that the received signal quality meets the required bit error rate specification for each modulation.

5.1.5. Run Time Operation of the Device

During run time, the control law forces continuous adaptation of the device to minimize power while meeting the BER constraint at all data rates and channel conditions. This is done by operating the system along the optimal locus of the control knob settings obtained from the optimization procedure. The threshold and guard band for EVM is set based on the estimated channel quality and current data rate. The voltage scaling is performed independently for each modulation in a standard-compliant manner such that the received signal quality meets the required bit error rate specification for each modulation. The run time operation is shown in Figure 86. EVM keeps on increasing (a) as the VIZOR controller throttles the receiver power lower and lower (b)

until EVM threshold is reached. The design of the power control circuitry is crucial in the adaptation approach, as it determines the power savings. Low-power operability would be limited by the response and settling time of the feedback control circuitry. Careful optimization of the control loop parameters is necessary to ensure stability, especially under fast varying channel conditions. Response times of the order of a few micro seconds for power management blocks have been presented in literature [27], whereas the channel variation is much slower compared to this. In case the channel changes abruptly the VIZOR controller takes the system to full power operation to avoid significant data loss.

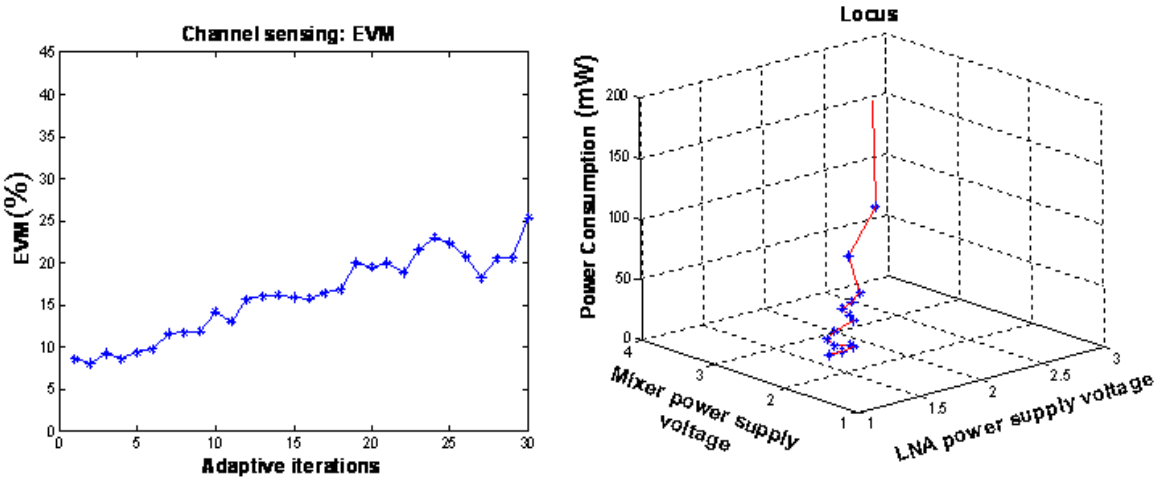


Figure 86: a) EVM variation with time b) Operation along the locus showing power savings compared to the static case (highest point on the locus).

5.1.6. Power Savings through Receiver Adaptation

The power-EVM optimizer is used to obtain the locus of optimal control knobs settings for a set of 12 different channels (locus points) ranging from good to bad. Three popular modulation schemes – QPSK, 16-QAM and 64-QAM are studied. The optimal RF front-end power consumptions across these channel conditions are plotted for the

three different modulations in Figure 87a. It is observed that for a majority of the channel conditions, the optimal RF power consumption is lower than nominal value of 48mW. It is also observed that the optimal control knob settings and the associated power consumption is lowest for QPSK modulation. This is due to the tighter requirements on the SNR for 16-QAM and 64-QAM (higher data rates). The optimal *W* required along the locus points is shown in Figure 87b. As observed, simulations indicate that sufficient margin exists for pruning *W* (maximum of 8 bits) under favorable channel conditions. Up to 2 bits of resolution can be sacrificed for QPSK modulation under majority of the channel conditions. Though the margin is lower in the case of 16-QAM and 64-QAM modulation, the system budget allows for a bit drop under good channel conditions.

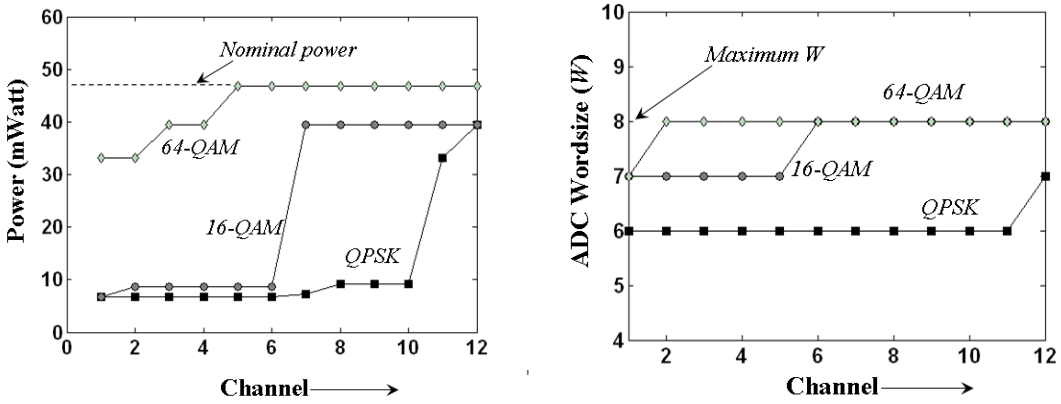


Figure 87: a) Power consumption for different modulations b) Optimal ADC wordsize (*W*) along the locus for different modulations

In wireless standards such as WLAN, the higher-level MAC protocol dynamically changes the data rate (modulation and coding) based on the channel conditions. The control law operates within the framework of the protocol by operating the device near the threshold for each data rate. From simulations, the computed upper bounds of EVM specification for QPSK, 16-QAM, and 64-QAM modulations are 35%, 12%, and 4.3%,

respectively, for a BER compliance of 5e-4. While the data rate and modulations are changed by the higher-level protocol, the above described adaptive operation minimizes power consumption in the receiver by exploiting the EVM margins. The available margins for each modulation are a strong function of the individual circuit components of the receiver. Therefore, careful designs of tunable components in the receiver that exhibit power vs. performance tradeoff maximize the power savings in a VIZOR receiver. The adaptive receiver shows significant power savings across different channel conditions with *a maximum savings going up to 4X (QPSK),* excluding the efficiency loss in the PMU.

Even more power can be saved by using multidimensional adaption along with post-distortion for correcting some of the non-linearities introduced by the low power front end [139].

5.1.7. Extra Power Savings through Adaptive Biasing for DSVC

As the supply voltage is scaled down the performance of the circuits degrade steeply as shown by dashed lines in Figure 88 and Figure 89a for Gain, NF and OIP3 of the LNA respectively. This limits the lowering of supply voltage. If the rate of degradation of LNA specifications with supply is can be lowered (through dynamic compensation), i.e. gradual degradation in the specifications can be achieved, the supply voltage can be reduced to lower levels than in the uncompensated case. This has direct implications for increasing the power savings that can be obtained from the adaptation approach.

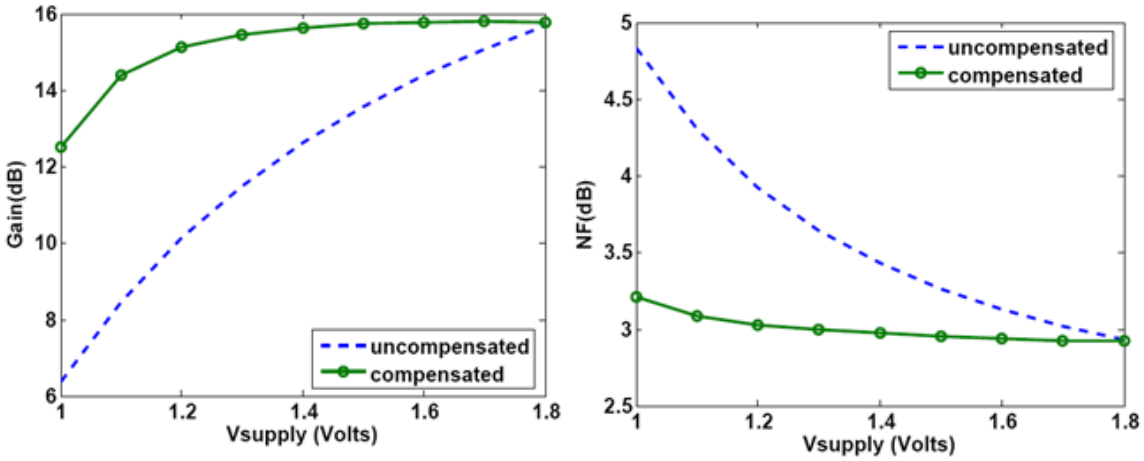


Figure 88: Gain and NF change as supply voltage is scaled down.

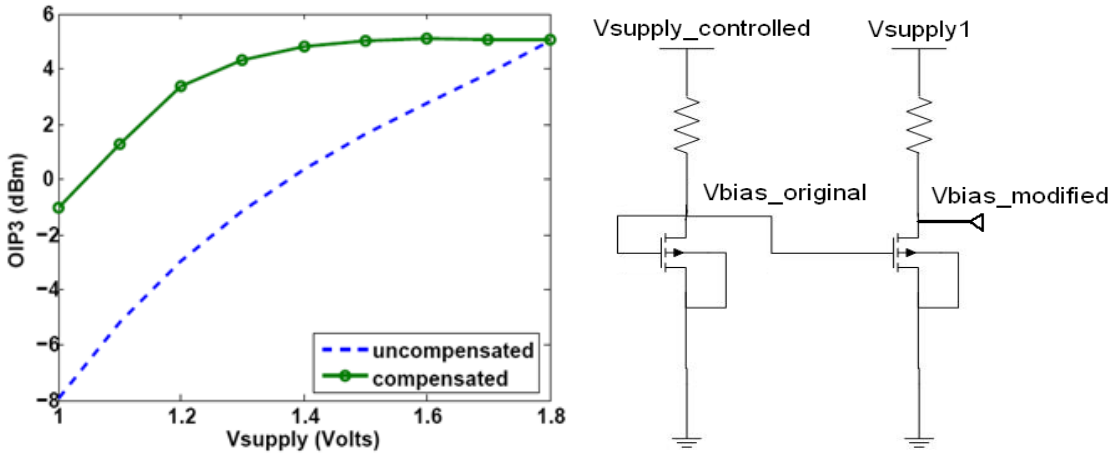


Figure 89: a) OIP3 degradation with supply voltage scaling b) Adaptive biasing circuit.

To reduce this steep degradation of the circuit performance with supply voltage reduction an adaptive biasing technique is adopted. The degradation of the LNA specifications arises due to two main factors with decreasing *Vsupply*– the decrease in current through the branches, and secondly due to the reduction of the bias voltages (dashed line of Figure 90) of each stage. If the bias voltages of the stages can be dynamically adapted to counteract the effect of supply voltage reduction, the variation of current through the stages can be minimized. This is achieved with the novel biasing circuit shown in Figure 89b. The change in *Vbias_modified*, which is used to bias the CS

stage of the LNA, as function of supply voltage is given by the following equation and shown in Figure 90 (solid line). It should be noted as *Vsupply_controlled* goes down *Vbias_original* goes down and hence *Vbias_modified* goes up as required for compensation. The tuning required to obtain a desired bias voltage variation is done by careful selection of the device aspect ratios (W/L), resistances and *Vsupply1*.

$$V_{bias\_modified} = V_{supply1} - K'(\frac{W}{L})(V_{bias\_original} - V_t)^2 \times R \qquad (51)$$

The biasing circuit is forced to operate in the sub-threshold such that the power consumption is not significant. This is possible because these transistors are not in the RF path and only the voltage output is important for biasing. Using compensation, the current is kept constant, and the degradation of LNA specifications are minimized for supply voltage reduction. This can be clearly seen in the plots Figure 88 and Figure 89a (solid line). It is evident that this adds another dimension of power savings that can be achieved with the proposed approach.

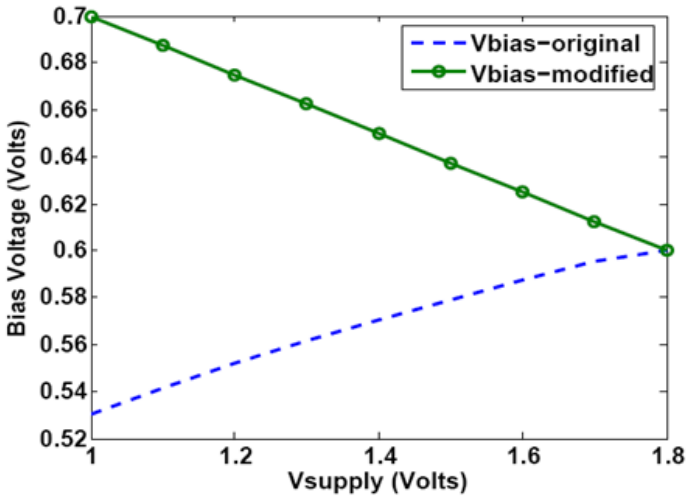


Figure 90: Biasing voltages for uncompensated and compensated case

Simulation Results with Adaptive biasing

The baseband portion of an MB-OFDM receiver chain is implemented in MATLAB for the purpose of a complete study. Randomly generated binary data is QPSK modulated and fed to a 256-point IFFT module that generates a complex time domain waveform which is up-converted and transmitted. The above mentioned sequence of steps is the OFDM modulation that is performed in communication systems. In an actual MBOFDM system, several modulation schemes such as QPSK, 16-QAM, 64- QAM are used with varying data rates. The bandwidth of the baseband data that is transmitted is set at 256MHz which is the MB-OFDM standard. Random Gaussian noise is added to the transmitted data to mimic the effect of the channel. At the receiver, the received RF signal is down-converted by the RF front-end to baseband frequency. The RF front-end of the receiver chain comprises the LNA and mixer. Hence this system-level simulation study enables the study of receiver operation in the presence of a dynamically tuned LNA.

At the receiver baseband, the down-converted data is fed to an FFT block which generates a sequence of received complex data points. The received symbols are compared with the known transmitted symbols to compute the EVM value. It is noted that the computed EVM values quantifies the sum total of the transmission-reception link that includes the performance of the circuits, channel etc. In this simulation, all the elements in the transmit-receive chain are kept constant except for the LNA. The computed EVM is used as the adaptation metric for DSVC of the LNA as explained earlier. Figure 91 plots the dynamic supply voltage variation of the system for the uncompensated and compensated (adaptive bias) cases. It is observed that by

compensating the LNA with adaptive bias circuitry, the system can be operated at a lower supply voltage. As can be seen from Figure 91a, the LNA supply voltage is dynamically tuned to minimize the power consumption while simultaneously satisfying the adaptation metric threshold (EVM threshold < 33%). Figure 91b shows the variation of power consumption with *Vsupply*. Figure 92 shows the effect of compensation on the adaptation metric. The constellation plots of received OFDM QPSK symbols are plotted for a particular value of the supply voltage (Vsupply = 1.5V). As observed from the figure, adaptive bias compensation provides a higher level of system performance, as evident from the reduced scatter of the constellation plot.

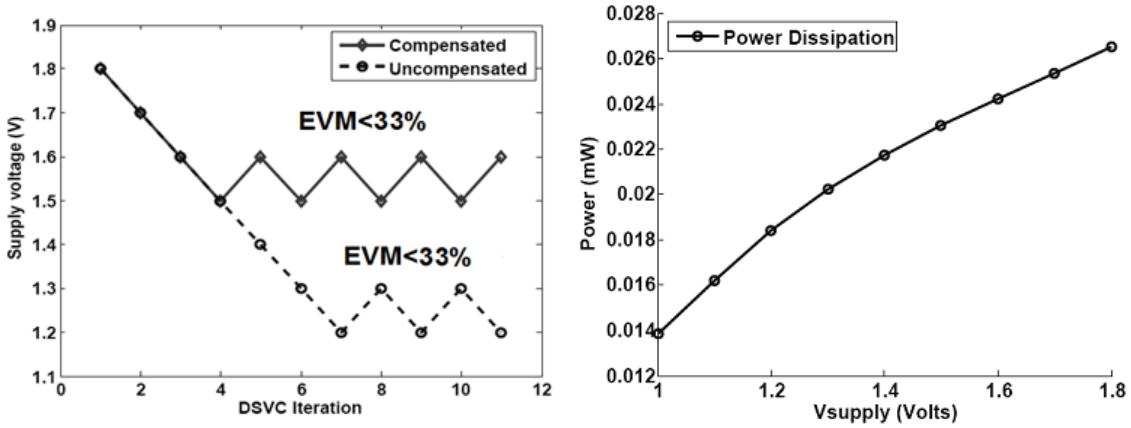


Figure 91: a) DSVC of the LNA for the compensated and uncompensated case b) Power dissipation with supply voltage

Finally, the DSVC operation of the system is studied through the above described simulation framework. Figure 93 illustrates the DSVC operation of the device over time. Initially, the supply voltage is at 1.8V (nominal) and starts decreasing based on the control law. The threshold of the adaptation metric (EVM) is set to 33%. The baseband processor, therefore, drives the supply voltage down until the received EVM crosses this threshold. Once this occurs at Vsupply = 1.2V(EVM = 36%) as observed in Figure 93,

the supply voltage starts increasing until the EVM passes the threshold, following which it starts decreasing again. The supply voltage variation therefore follows a *saw-tooth-like pattern* at equilibrium. This equilibrium represents the *optimal supply voltage level* for the system. In the event of an interferer or noise affecting the receiver, the correct operation of the system is affected, resulting in a higher value of EVM. The supply voltage therefore increases from the optimum level to counteract this effect. In Figure 93, the supply voltage increases to about 1.7V in the presence of a narrow-band interferer. This value of the supply voltage represents the new value of optimal supply voltage in the presence of an interferer. As the interferer disappears, the system reverts back to its original stage. Thus, the adaptation approach enables the dynamic adaptation of the system to strive for minimizing power (supply) consumption At optimum *Vsupply* (1.2V) a power savings of 31% is achieved compared to nominal power consumption (Figure 91b). To control *Vsupply* a power management block as shown in [27] could be used.

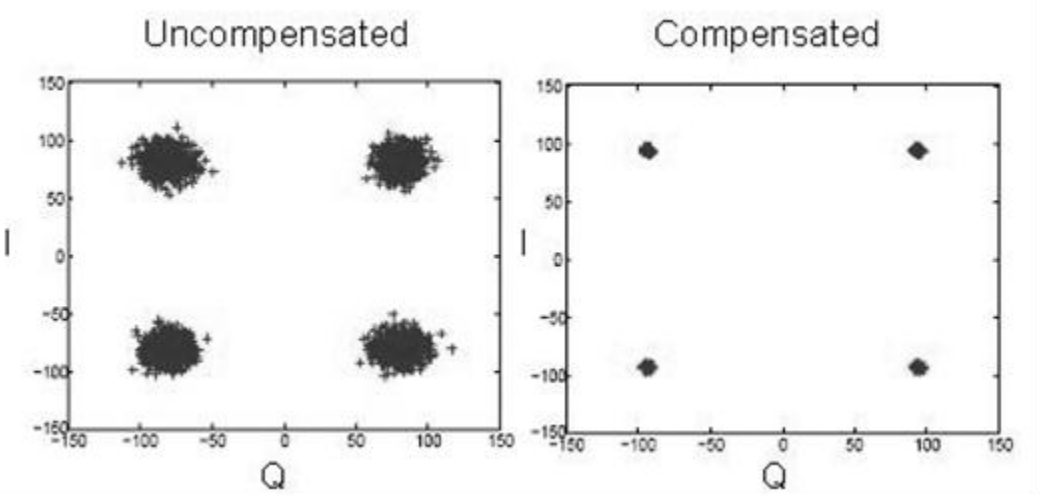


Figure 92: Received constellation plots (uncompensated and compensated)

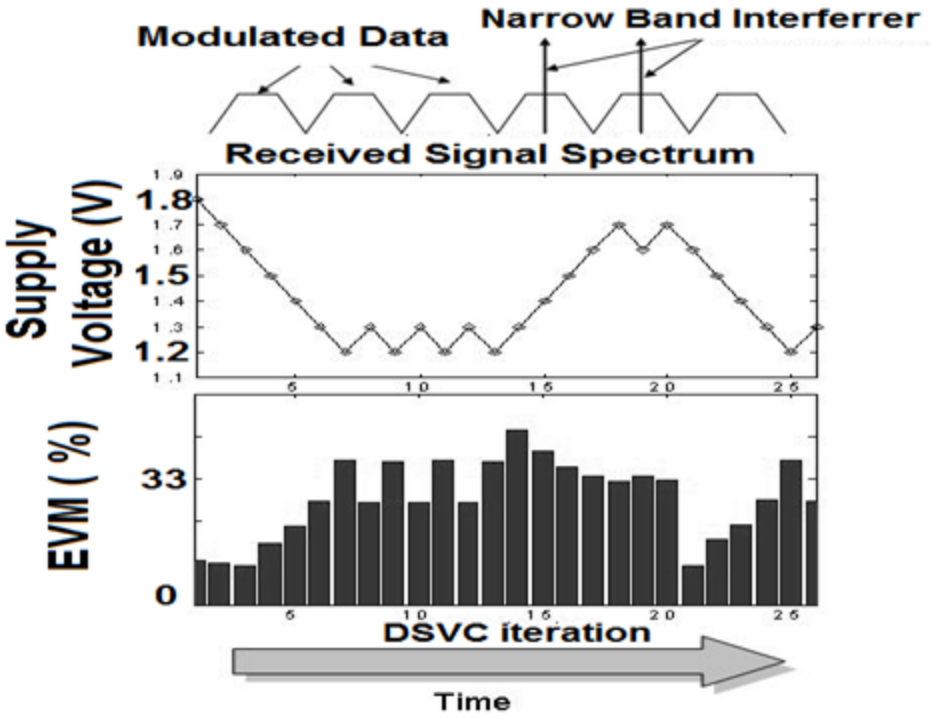


Figure 93: Simulation study of the DSVC operation of the system under narrow-band interference

5.1.8. Live Demonstration: VIZOR Receiver

A live demonstration was designed to demonstrate the real-time closed loop adaptation of RF receivers for low power operation. The setup is shown in Figure 94. The transmitter was designed using off-the shelve upconversion mixer and PA. The receiver consisted of custom designed adaptive LNA and down-conversion mixer, whose performance could be traded off for power using built-in tuning knobs. Matlab in a PC was used as the baseband for the OFDM transceiver as well as for implementing the control loop using several digitally controllable Keithley power supplies.

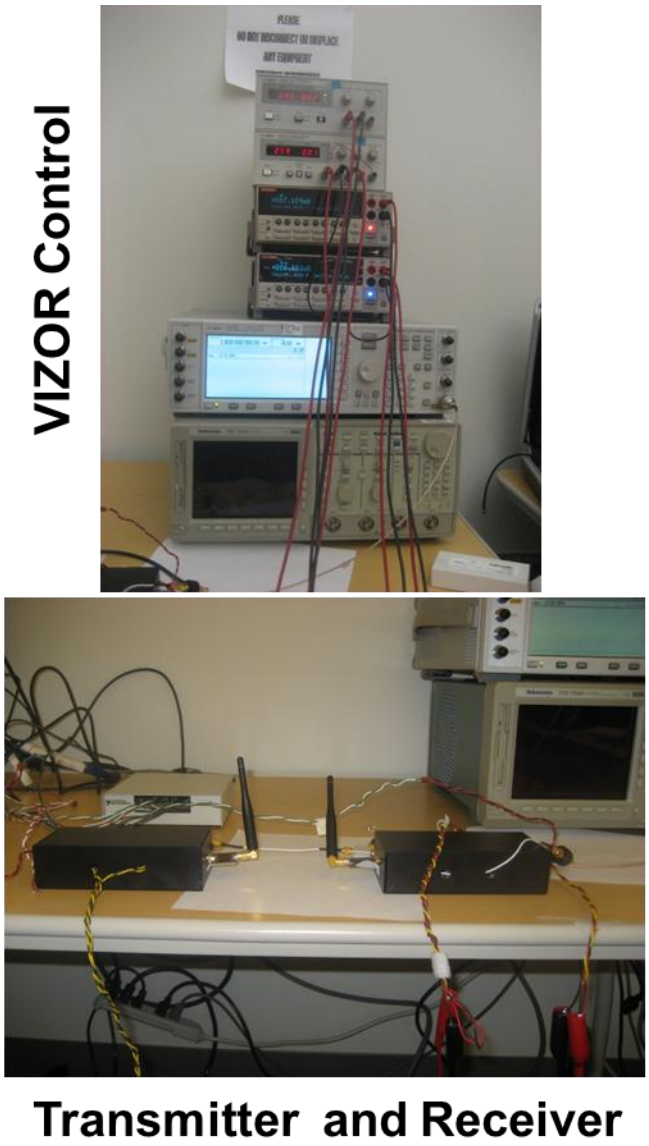


Figure 94: Setup for live demonstration of a VIZOR receiver

The VIZOR demonstration system in operation is shown in Figure 95. The user interface allows choosing between nominal operation or VIZOR mode. When VIZOR mode is enabled, the system strives to adapt to lower power points (EVM increases, constellation spreads) until EVM threshold or minimum power point is reached, after which it keeps on hovering around that value minimizing power consumption for te given channel.

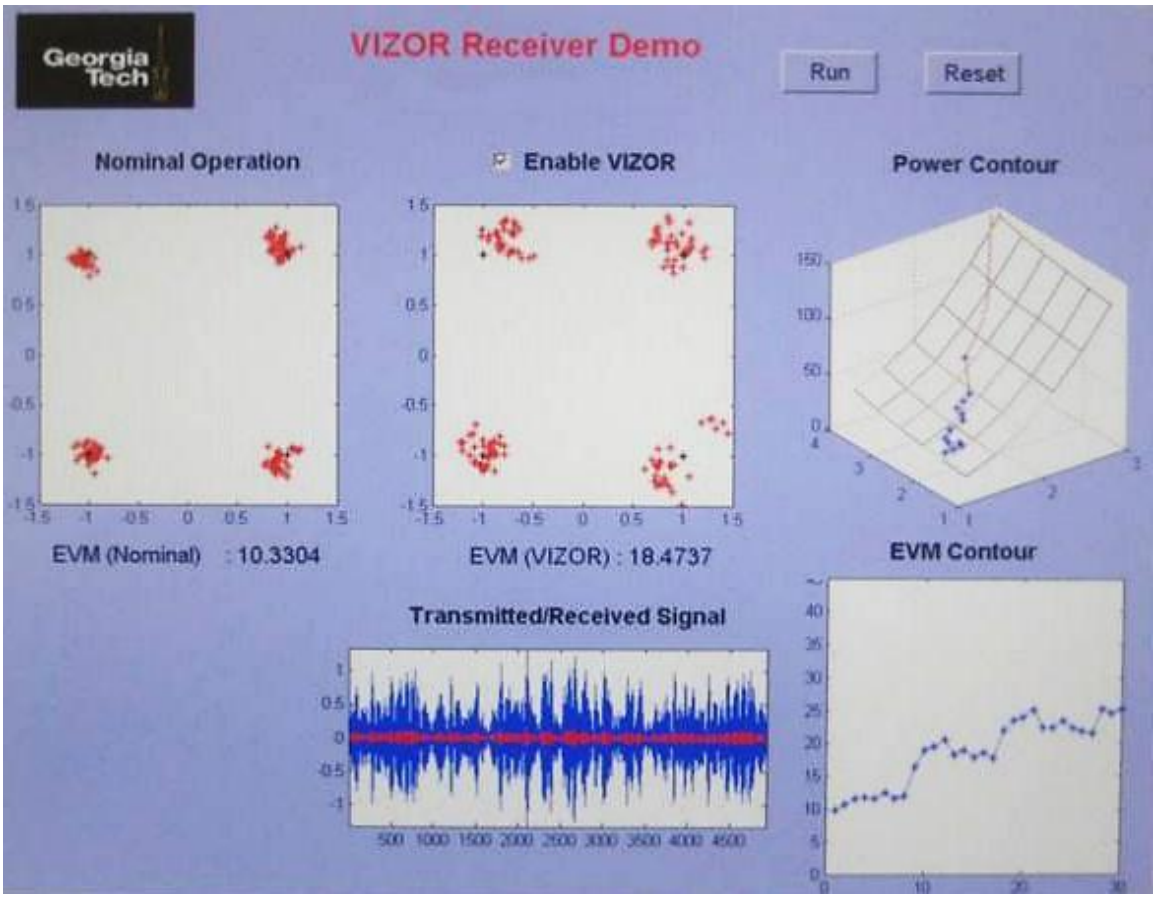


Figure 95: VIZOR receiver user interface

5.2. Built-in *Orthogonal Tunability* for Optimal Adaptation[2]

Modern wireless systems are increasingly incorporating adaptability to operate at low power under varying channel conditions and to increase yield under severe process variation as shown in previous sections and in Chapter 2. Effective adaptation requires built in tuning knobs in the RF front end circuits. Due to the sensitive nature of RF circuits traditional tuning knobs affect more than one specification simultaneously. To ensure optimal adaptation it is beneficial to have carefully designed tuning knobs that allows independent control of important specifications. In this section the design of an

[2] Please refer to the journal version for an updated version of the work presented in this section.

inductorless RF LNA is discussed whose specifications can be traded off independently/ orthogonally of each other for reduced power consumption. Two built in tuning knobs are introduced for orthogonal adaptation of Gain and linearity. The orthogonally tunable LNA, designed in 0.18µ CMOS achieves a 14 dB Gain and 30 dB OIP3 control range as its power consumption goes down by 20×.

5.2.1. Need for Orthogonal/Independent Tunability in RF Circuits

The continuously growing popularity of battery operated portable systems with wireless connectivity has mandated the design of low power RF/analog systems. The implementation of these increasingly complex systems in nanometer CMOS technologies with increased variability results in low yield of the RF systems. The requirement of low power and high yield cannot be simultaneously solved by traditional static design techniques. Hence there is a thrust toward adaptive or reconfigurable wireless systems that use underlying tunable RF/Analog and Mixed Signal blocks. These systems meet the stringent goal of both power and performance by intelligently tuning the sub blocks depending on its environment, process corner and application requirements at any given time. This adaptability is enabled by built in tunability in the RF circuits allowing trade off of power vs. performance as well as tradeoff between specifications. However, most of the traditional RF designs exhibit highly interdependent nature of the specifications. Also traditional designs lack enough built-in tuning knobs to achieve independent control of specifications. This work highlights the benefits of carefully designed built in tuning knobs and proves the concept by using an RF LNA with two dedicated built-in tuning knobs that enable independent (orthogonal) control of two specifications namely gain and linearity without any extra power overhead in the LNA core.

Traditional wireless circuits/systems are overdesigned to operate under varying channel conditions. Recently, RF systems are being designed [142], [146], [147], [148] to adapt to environment (channel) by trading off the quality of the receiver front end circuits to save power when the channel quality is better than worst case. For example, when the received signal strength is moderate and there is no blocker present the linearity of the LNA can be compromised for lower power consumption. These environment adaptive systems require built in tunability in the RF front end circuits to achieve power savings through adaptation.

In the nanometer regime increased process variation leads to loss of yield as more and more components fail one or more of the required specifications. This problem is even more severe in RF systems as they exhibit lower yield than digital systems due to the interdependent and complex nature of several specifications. In [149], [150], authors present Self-Healing Systems that can understand the process corner of the manufactured devices using sophisticated tests and then tunes the failing devices in post manufacture tuning phase to bring then within predefined specification bound and hence increase yield. For example, due to manufacturing variation, the gain of a device is low but the linearity is acceptable. It is desirable to have a tuning knob that can only tune for gain without affecting linearity with minimum power overhead. Hence, these process adaptive systems also require built in orthogonal tunability in the RF front end circuits to recover yield loss.

Most of the traditional RF circuits are static or minimally tunable using some digital controllability. For example, high power, low power and shut down modes are available in some commercially available transceivers. If available, the tuning knobs

affect different specifications in an interdependent manner. This is not enough for optimal operation of complete self-aware self-adaptive systems. Also future radios will integrate more and more functionalities in a single chip. Hence integration of the RF components with digital circuits is of utmost importance. In this section we demonstrate the design and benefits of orthogonal tuning knobs using an inductorless LNA as a test vehicle, which will facilitate easy integration.

5.2.2. Inductorless LNA

A. Design Criteria

In this work we concentrate on inductorless designs for easy integration with digital and increased scalability. Future multi-mode and multi-standard SDRs require the LNAs to work over a several frequency bands. To achieve this by tuned LNAs several LC tuned loads and input matches are required leading to high area. It also requires switching between these tuned circuits for different modes. Inductorless LNAs [151], [152], [153], [154], [155] exhibit the benefit of being wideband, very compact and only one circuit can cover all the required bands. Also trade-off of power vs. performance is better in inductorless designs as the specifications are controlled more by the transistors than lumped elements.

Traditional LNA designs with inductors exhibit high gain and selectivity by using LC tuned gain peaking in a certain narrow band. It is harder to achieve similar gain without an inductor at the same frequency over a wide bandwidth in inductorless LNAs. Also traditionally inductorless LNAs exhibit very high noise figure. In this work, we demonstrate a two stage inductorless design that achieves sufficient gain, good input matching, noise figures comparable to tuned designs and exhibits extended power vs.

performance trade-off. The designed LNA covers the DVB-H band, the TV white space and GSM band.

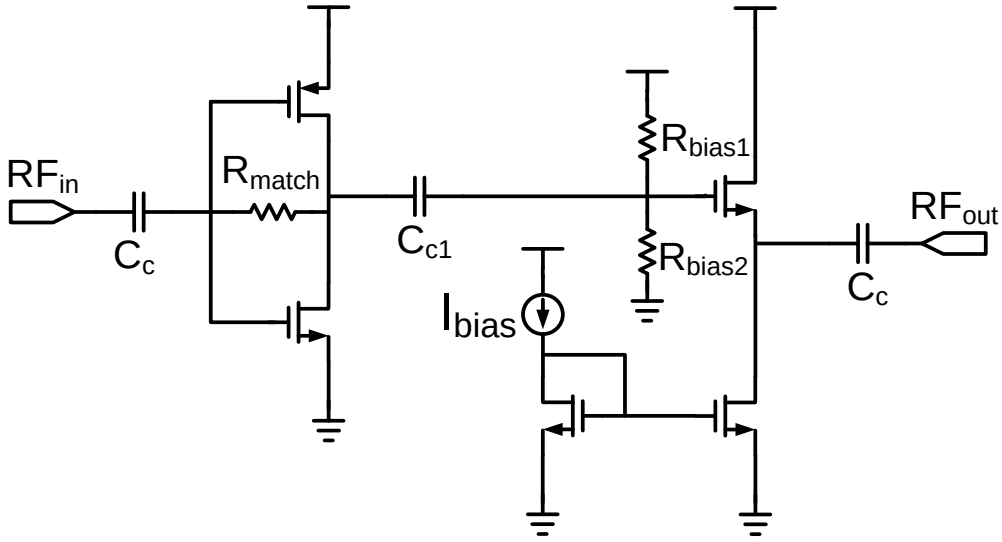


Figure 96: Inductorless two stage LNA

B. <u>Two Stage Design</u>

The simplified schematic of the inductorless LNA is shown in Figure 96. The input stage provides input matching to 50Ω and high voltage gain. The 2nd stage or output stage provides high current drive capability into low load impedance (50Ω). This stage can be optimized differently if the LNA is driving a mixer with higher input impedance.

The input stage is built using one PMOS and one NMOS gm transistors with the drains connected together. It provides high voltage gain while driving high impedance of the 2nd stage. It also provides a broadband 50Ω input match using negative feedback through Rmatch. The value of Rmatch is optimized to maximize gain (S21), minimize Noise Figure (NF) and reduce input return loss (S11). This stage is self–biased though the NMOS, PMOS and Rmatch. The high voltage gain provided by the input stage is converted to power gain by the source follower output stage. The common drain NMOS

is biased using two high biasing resistances Rbias1 and Rbias2 and is AC coupled with the input stage using coupling cap Cc1. The output stage, biased using NMOS current mirror, is optimized for Output 3rd order Intercept Point (OIP3) with minimum power possible.

In [151], the authors present a two stage noise cancelling LNA. In [154], the authors increase the gain of the LNA over a wide frequency range by introducing an extra stage than that of [151]. In this work we concentrate on minimizing the number of transistors in the LNA to reduce NF. The first stage is designed to have very high voltage gain to reduce the overall NF, allowing better NF than comparable designs as shown in the next subsection.

C. Simulation Results for Two-stage LNA

The LNA shown in Figure 96 is designed using National Semiconductor 0.18µ process (CMOS9T5V) with 1.8V of supply voltage. The S-parameters and the NF of the designed LNA is shown in Figure 97 from 10MHz to 10GHz range. The 3dB bandwidth extends from 70 MHz to 1.5 GHz. At 1 GHz the LNA provides 15.3 dB power gain, -12.8 dB S11 with a very low NF of 1.88 dB. It consumes 12.6mA current, among which 9mA is consumed in the input stage as it provides simultaneously wideband 50Ω input match and high voltage gain to reduce NF. The current consumption includes the buffer (2nd stage). The performance of this LNA is compared with state of the art LNAs found in literature in Table 10, showing it is comparable in terms of OIP3, and performs better in terms of gain and NF. Now this static LNA design would be extended to work as an orthogonally tunable LNA in the next section. These results show that the base LNA design is comparable to the state of the art inductorless LNA designs.

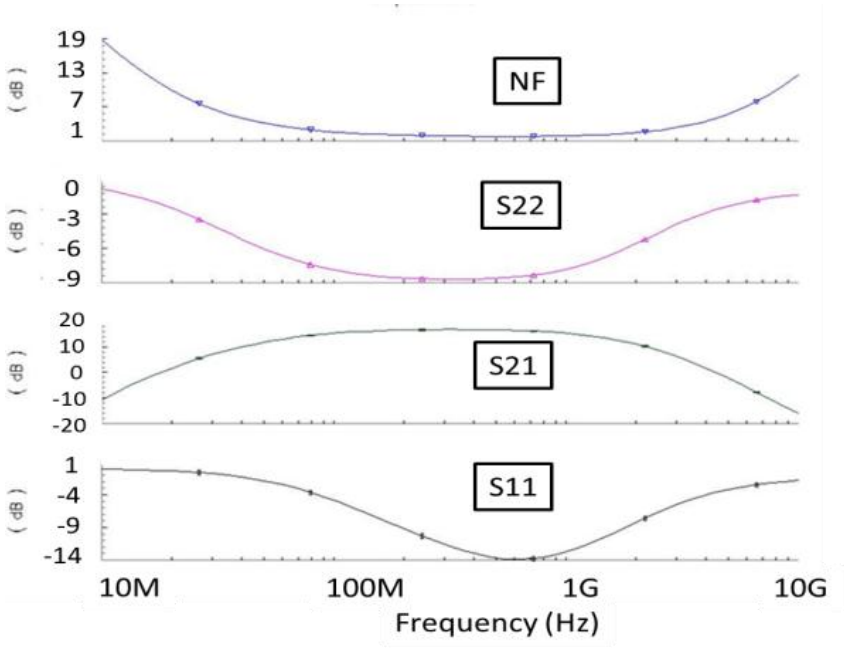


Figure 97: Noise Figure and S-parameters of the designed LNA

Table 10 Comparison with existing inductorless LNA

	This work	[151]	[154]	[155]
Technology	**0.18µ**	0.25µ	0.13µ	0.18µ
S21 (dB)	**15.3**	13.7	11	9.8
NF (dB)	**1.88**	2	3.6	2.3
S11(dB)	**-12.8**	-12	-5.3	-9
S22 (dB)	**-7.84**	-12	-	-
Id/Vdd (mA/V)	**12.6/1.8**	14/2.5	19/1.5	7/1.8 (w/o buffer)
OIP3 (dBm)	**-1**	13.7	3.8	-7
BW (Hz)	**70M-1.5G**	2M-1.6G	2G-9.6G	2-4.6G

5.2.3. Design of Orthogonal Tuning Knobs

A. Specifications to be orthogonally tuned

The most important specifications for a LNA are power Gain (S21), NF, Output 3rd Order intercept Point (OIP3) and Input Match (S11). When input signal strength is moderate with strong interferers present, a highly linear receiver (high OIP3) is required; however gain and NF can be relaxed. High gain and low NF is needed for a weak input signal to provide high sensitivity. When the input signal strength is high low gain and higher NF would suffice. Hence it is to be noted that Gain and NF requirements go together and does not exhibit any contradiction. In this work, we concentrate on an orthogonal tunability between OIP3 vs. Gain and NF, while having acceptable S11.

First we develop tunability of OIP3 and then Gain in the following subsections. The specifications reported are at 1GHz.

B. OIP3 Tuning

The LNA of Figure 96 is to be modified for OIP3 tunability. One option to tradeoff OIP3 for power would be to reduce supply voltage. However, supply voltage reduction is not recommended as the efficiency of the power management unit reduces with reduced output voltage, making the power savings minimal. This also results in S21 degradation making the adaptation non-orthogonal. In the design of Figure 96, the OIP3 is dominated by the output source follower buffer stage as the signal levels are low enough in the 1st stage not to get compressed and affect linearity of the composite LNA, i.e. the power required in the 1st stage for reasonable gain and NF already provides high enough OIP3 for this stage. Hence the most effective OIP3 tunability can be achieved by controlling the tail current of the source follower 2^{nd} stage. This is done by applying a

controllable bias VIIP3. The result of linearity tunability is shown in Figure 98a in terms of OIP3. It exhibits tunability from 5 dBm to -25 dBm as current consumption in that stage reduces from close to 9mA to 0.7mA. The gain stays relatively flat with VIIP3, as shown in Figure 102d for most of the tuning range (VIIP3>0.55 V).

C. Gain and NF Tuning

Most of the Gain and NF is controlled by the input stage. The 1st stage does not affect the OIP3 until the current is very small. Hence tuning of Gain and NF is performed using a current source control in the input stage. However, the original design being self-biased, there is no controllability. In this subsection we evaluate the possible gain control options. The LNA is maintained in super threshold while adaptation to enable high frequency gain. Also supply voltage control is ruled out due to reasons described earlier.

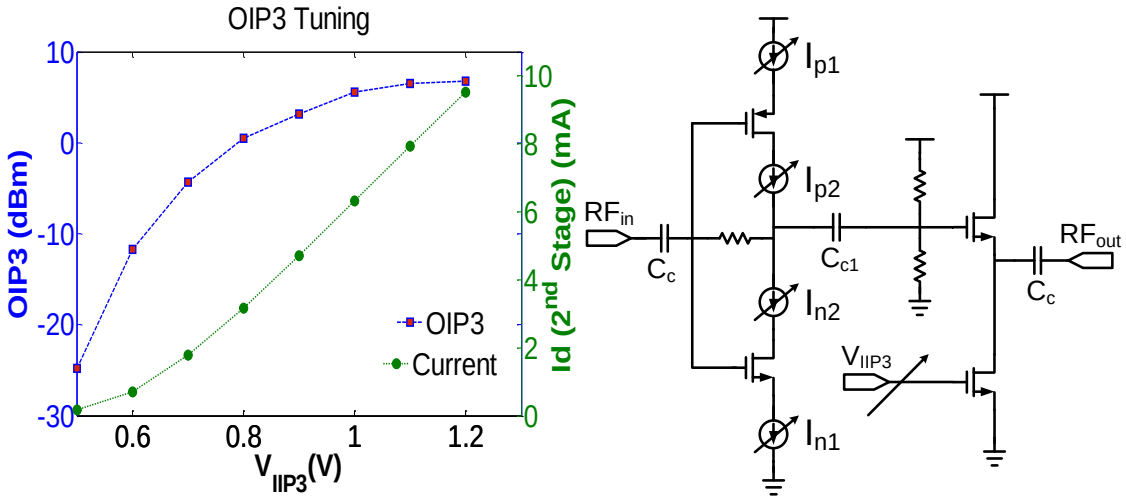


Figure 98: a) OIP3 tuning b)Possible Gain and NF tuning knob choices

Possible Tuning Options:

There are four possible places to insert a current controller in the input stage as shown in Figure 98b. Ip1 and In1 represent a PMOS and NMOS tail current source respectively. Similarly, Ip2 and In2 are cascoded PMOS and NMOS current sources. The

effect of inserting current control knob at these places are evaluated by looking at the NF, Gain, S11 and current consumption for each current source control. A tunable voltage (VGain) is applied to control the current of these current sources. For PMOS control the voltage varies between 0 V and 1.3 V, whereas for NMOS control this voltage varies from 0.5 V to 1.8V. It should be noted that the PMOS and NMOS sources exhibits maximum current for 0 and 1.8 V respectively.

The performance with the tuning knobs in four possible positions namely PMOS tail (Ip1), PMOS cascode (Ip2), NMOS tail (In1) and NMOS cascode (In2) are shown in Figure 99. The tail sources (both NMOS and PMOS) degenerate the gm transistors resulting in a reduced gain in the high current region. It also exhibits a lower dynamic range for power vs. performance tradeoff. The cascode sources provide better S11 and NF at high current regime making it a better choice over tail current sources. Among NMOS and PMOS, the PMOS cascode source exhibits less NF for same current values (see VGain=0.8). Hence we choose the PMOS cascode current source as the tuning knob for gain tuning.

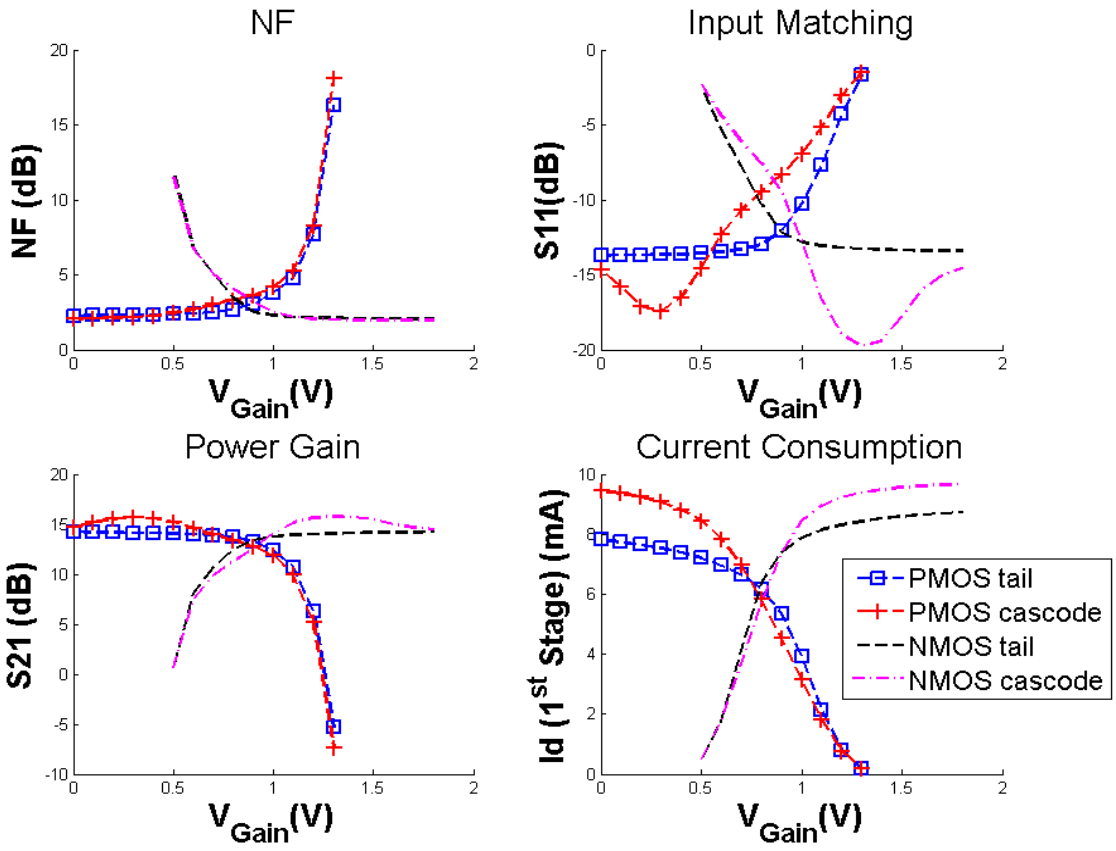


Figure 99: Performance comparsison for different gain control knobs

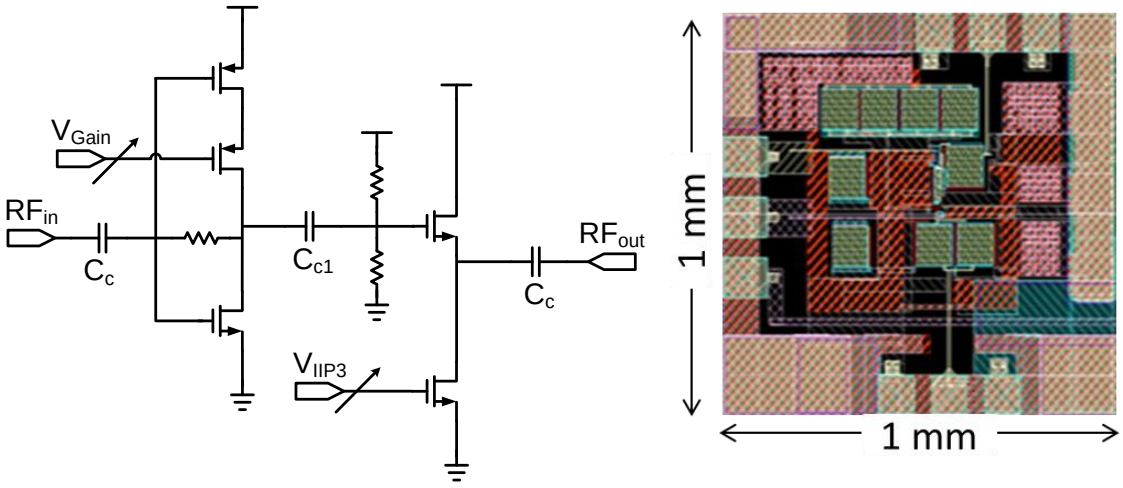


Figure 100: a) Schematic b) Layout of orthogonally tunable LNA

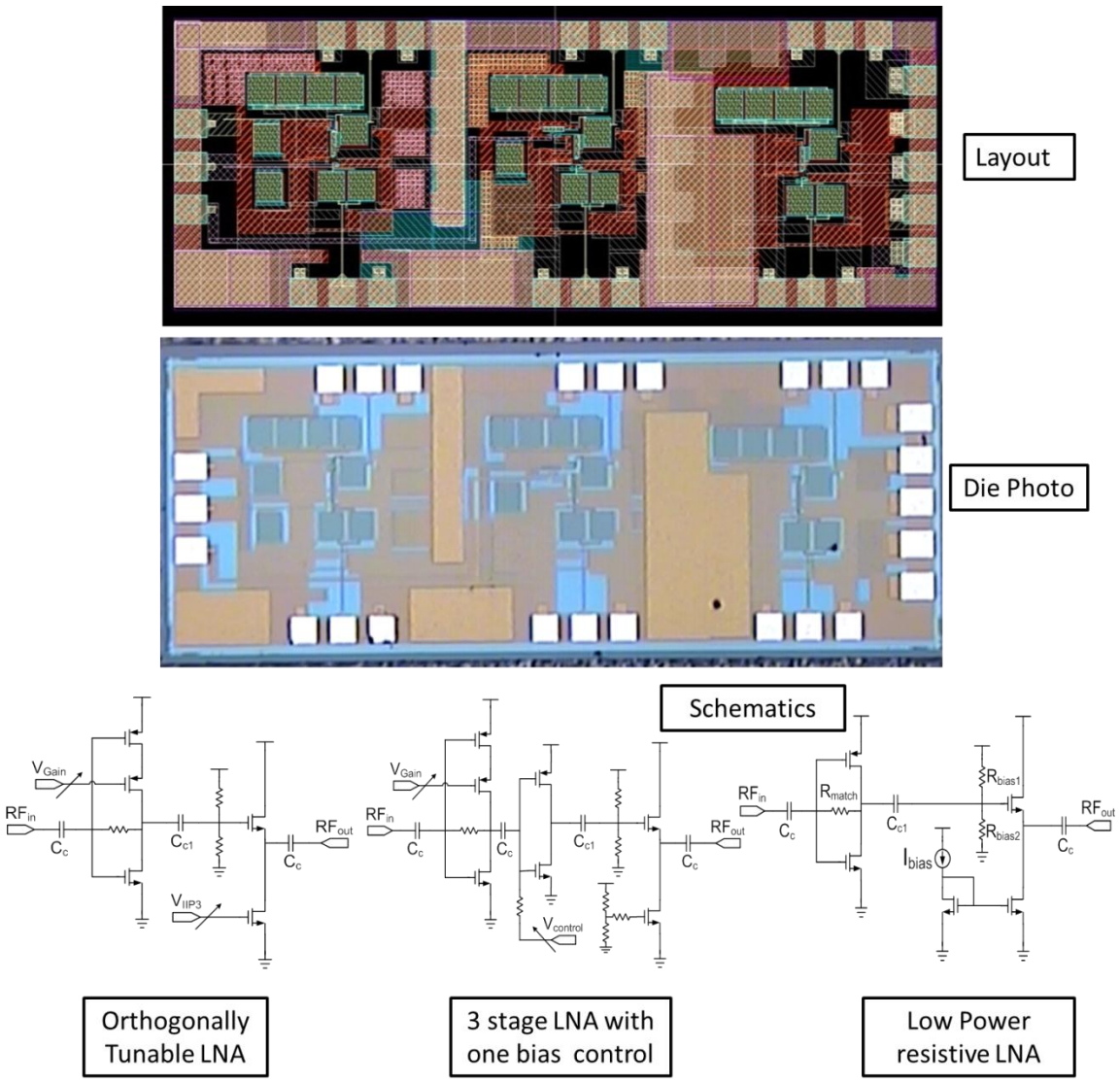


Figure 101: Layout and Die Micrograph and schematics of the orthogonally tunable LNA and two other LNA for comparison purposes

5.2.4. Results: Orthogonally Tunable RF LNA

The schematic and layout of orthogonally tunable LNA with gain and linearity tuning knobs are shown in Figure 100a and Figure 100b, respectively. The design has been implemented in 0.18µ CMOS9t5v process and fabricated. The die photo is shown in Figure 101 (the measured results follow the simulated ones presented with expected

variations). V_{Gain} and V_{IIP3} provide independent control of Gain and OIP3 with power. In a full chip implementation incorporating this tunable LNA the voltage controls could be replaced with digitally controlled current DACs, but the concept remains the same. In this Section we present the results of the designed LNA.

A. Orthogonal Tunability

Figure 102b shows the total current consumption with both the tuning knobs. It can be seen that total current can be traded off from 18.5mA to 0.76mA in a very gradual manner. Figure 102c shows the NF tunability. It changes by 6-8 dB with V_{Gain} whereas remains relatively constant with V_{IIP3}. Figure 102a shows how S11 changes over the tuning range. It remains within an acceptable range (<-5db) for most of the tuning range (VGain<1V).

Figure 102d shows the gain controllability with two tuning knobs. Gain exhibits a gradual degradation of 14 dB (17.7 dB to 3.6 dB @ VIIP3=1.2) with V_{Gain}. Gain does not change much with V_{IIP3} for V_{IIP3}>0.55. For lower values the source follower exhibits a high loss resulting in reduction of S21. But for V_{IIP3}>0.55 the LNA can be tuned orthogonally as desired. Figure 102e shows the OIP3 tunability. The OIP3 is relatively constant with V_{Gain} while exhibiting a gradual degradation of 30 dB (5 dBm to -25 dBm) with V_{IIP3}.

Hence the designed LNA can be orthogonally tuned for a 14 dB gain control range and 30 dB linearity control range. This tunability allows this LNA to deliver just the required amount of performance under any channel or process variation and save power. The measurement setup is shown in Figure 103 and the measured results for a working LNA die are shown in Figure 104 for 22mA bias current.

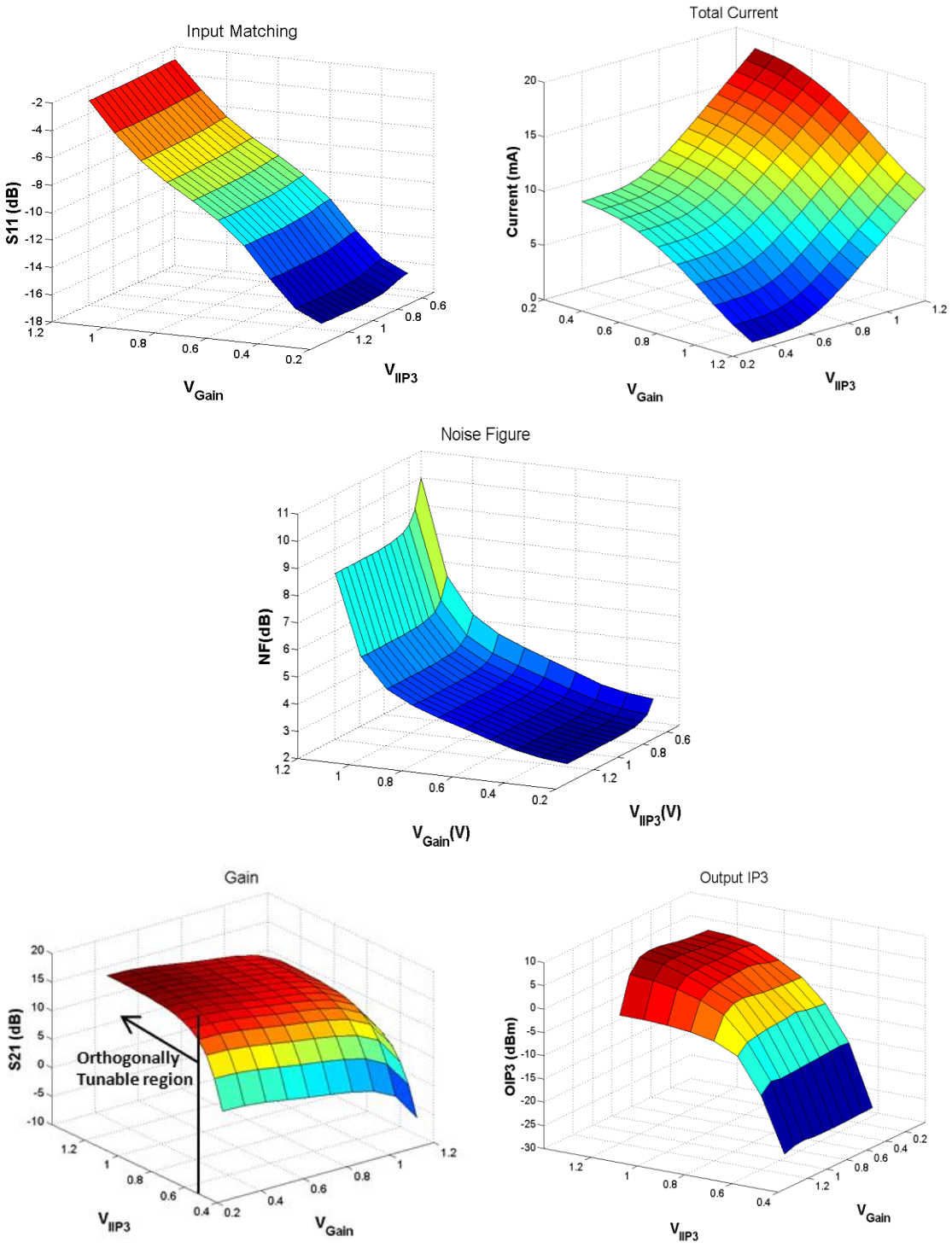


Figure 102: a) Variation of S11 with tuning knobs, Orthogonal Tunability in b) Total current c) NF d) S21(gain) e) OIP3(linearity)

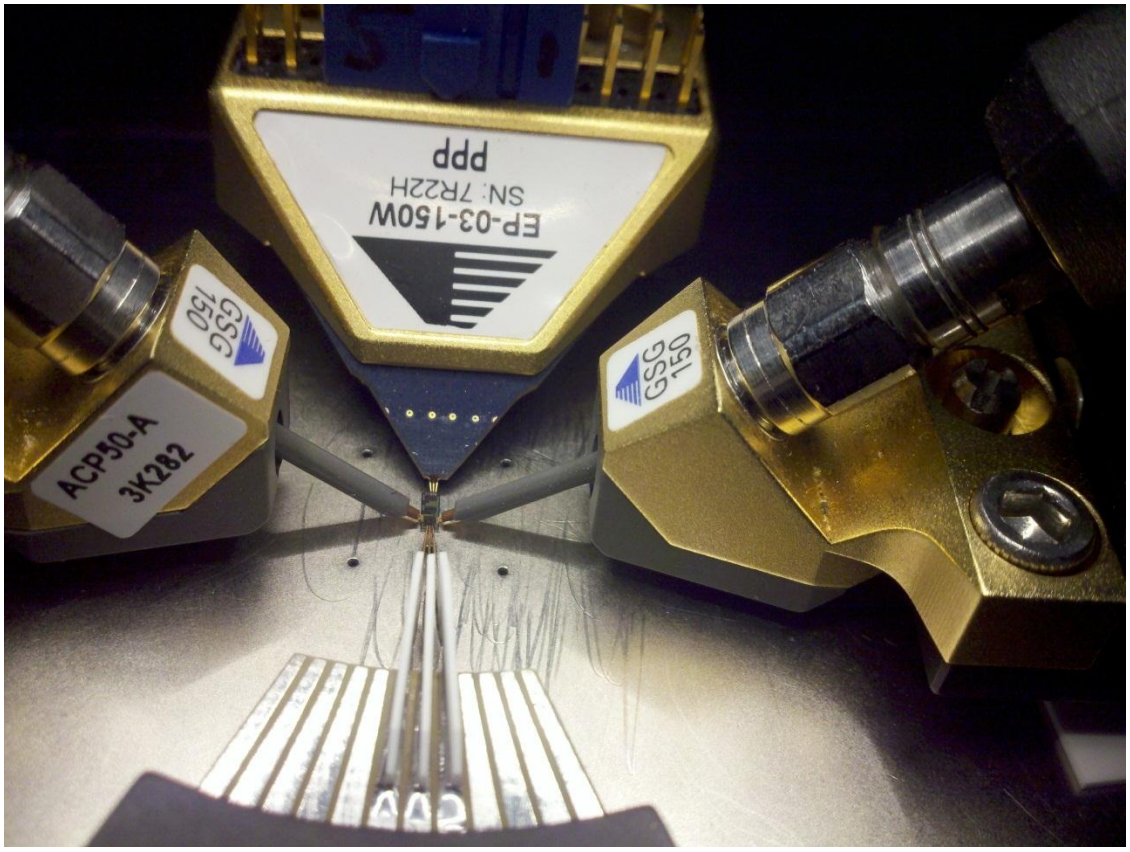


Figure 103: Measurement setup

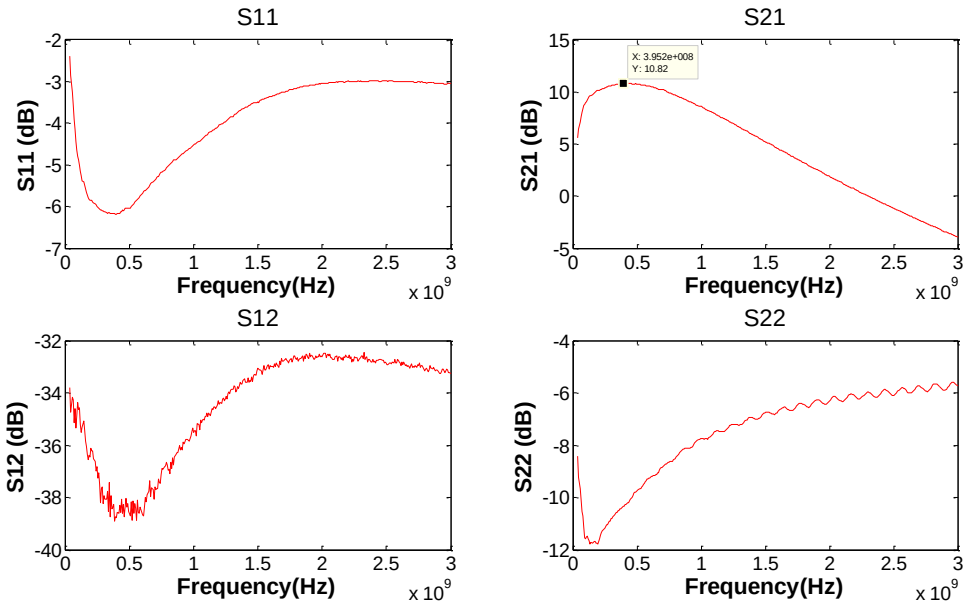


Figure 104: Measured result for orthogonally tunable LNA at 22mA bias current

B. Benefits of Orthogonal Tunability

Gain and OIP3 tunability can also be achieved in traditional designs using supply voltage control. Figure 105 plots the Gain and OIP3 of a simple LNA vs. its total current consumption as its supply voltage is reduced. It also shows the gain and OIP3 of the designed orthogonally tunable LNA (controlled using VGain) for similar current consumption. Let us consider the following situation: there is high interferes/blockers present in the channel along with a moderate received signal strength. This requires a low gain but high OIP3 in the receiver. If the static LNA is used it provides high gain, high OIP3 resulting in more power consumption than required. If the simple LNA (Figure 96) is used to reduce the gain to save power OIP3 also reduces, resulting in very low power savings. However, with the orthogonally tunable LNA the OIP3 remains constant as gain is reduced to save power (12mA→5mA). Similar savings are achieved while self-healing if a process skewed device has high gain but low OIP3 and it needs to be self-healed for linearity without affecting gain, with minimum power overhead. Healing using a simple LNA would mean increasing both gain and OIP3 leading to sub-optimal power consumption.

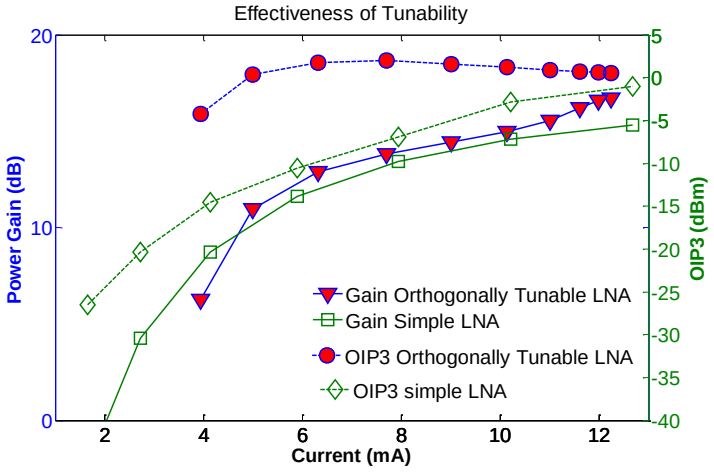


Figure 105: Effectiveness of Orthogonal Tunability

C. Summary and Future Work

In summary, this work discusses the design of an LNA whose specifications can be traded off for power independently of each other. An inductorless LNA, comparable to the state of the art is designed and orthogonal tuning knobs are introduced for independent adaptation for gain and linearity. The orthogonally tunable LNA, designed in 0.18µ CMOS achieves a 14 dB Gain and 30 dB OIP3 tuning range as its power consumption goes down by 20×. In future, this LNA and similar RF front end components will be used in adaptive receivers that can adapt to channel conditions as well as manufacturing process variations to ensure power optimal tuning. This work presents the requirement and benefits of orthogonally tunable circuits and uses an inductorless LNA as a vehicle to demonstrate the concept. The tuning knobs will vary from circuit to circuit, but the concept presented here remains the same. In future, similar built in tuning knobs will be implemented in mixer, VGA, ADC etc. that allow independent tuning of their respective important specifications for power.

In the next subsection the use of this orthogonally tunable LNA shows significant extra power savings in an adaptive receiver, making the adaptation optimal.

5.2.5. Adaptive Receiver with Orthogonally Tunable LNA[3]

Here we look into an adaptive receiver using the orthogonally tunable LNA and compare its performance with a traditional receiver using such a traditional adaptive LNA, i.e. a Non-orthogonally tunable LNA.

[3] This part of the work is done is conjunction with Debashis Bannerjee

A. Non-orthogonally tunable LNA

In order to demonstrate the benefit of having a system with orthogonally tunable knobs we compare it with a system where all the knobs are not orthogonally tunable. In order to do so we decide to take away 1 degree of freedom by tying the Gain and IIP3 tuning knobs of the orthogonal LNA together so that they scale simultaneously. However in order to make a fair comparison the 2 LNAs must have similar specifications. So we ensure that both the Gain and IIP3 variation of the new LNA spans the entire range of Gain and IIP3 of the original LNA. In this fashion we now have an LNA with non-orthogonally tunable knobs but with figures which are directly comparable with the original LNA. Such a LNA has been described in literature in [156] by using VDD as a tuning knob. The Power versus Gain and IIP3 of the 2 LNAs in our case are shown in Figure 106.

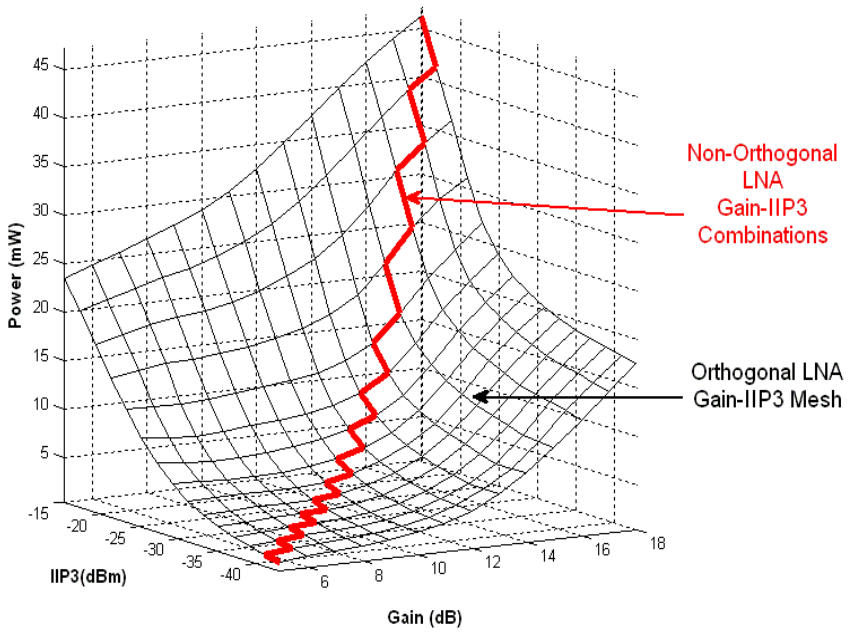


Figure 106: Power profile for orthogonal and non-orthogonal LNA

B. Channel Conditions

The signal passes through the channel between the transmitter and the receiver. The channel corrupts the signal by adding AWGN, through the presence of interferers and due to multipath effect. Also the channel causes the signal to attenuate due to path loss between the transmitter and the receiver. The effect of a channel is characterized at the receiver through the SNR at the input of the LNA and the attenuation of the signal through the channel. Here, 4 cases are considered:

(i) High SNR, Low attenuation.

(ii) High SNR, High attenuation.

(iii) Low SNR, Low attenuation.

(iv) Low SNR, High attenuation.

To demonstrate how an orthogonally tunable system may give an advantage in terms of power savings compared to a non-orthogonal one we focus on cases (i), (ii) and (iii).

In case (ii) the signal is relatively small and hence the EVM will be dominated by the addition of noise by the LNA. Hence the gain of the LNA should be large enough to keep the output SNR of the LNA high enough. Since the strength of the signal is low the IIP3 of the LNA can be tuned to a low value if possible to save power. In case (i) and (iii) the signal strength is relatively higher and the EVM is dominated by the effect of the signal hitting the non-linearity of the LNA. Hence the IIP3 of the LNA should be kept high enough while the gain of the system can be tuned to a low value to save power.

C. Optimization algorithm

The system is characterized for a number of known channels and a set of optimum tuning knob combinations is found where the system operates with minimum power but acceptable bit error rates (BER). It has been shown in Section 5.1 that for QPSK a BER of 5x10-4 translates to an EVM of 33% (after keeping a safety margin). Thus our optimization algorithm should find the point in the performance space at which the system operates with minimum power but with an EVM<33%. For this we use the algorithm as shown in Figure 107. Tsave is the final optimized tuning knob setting.

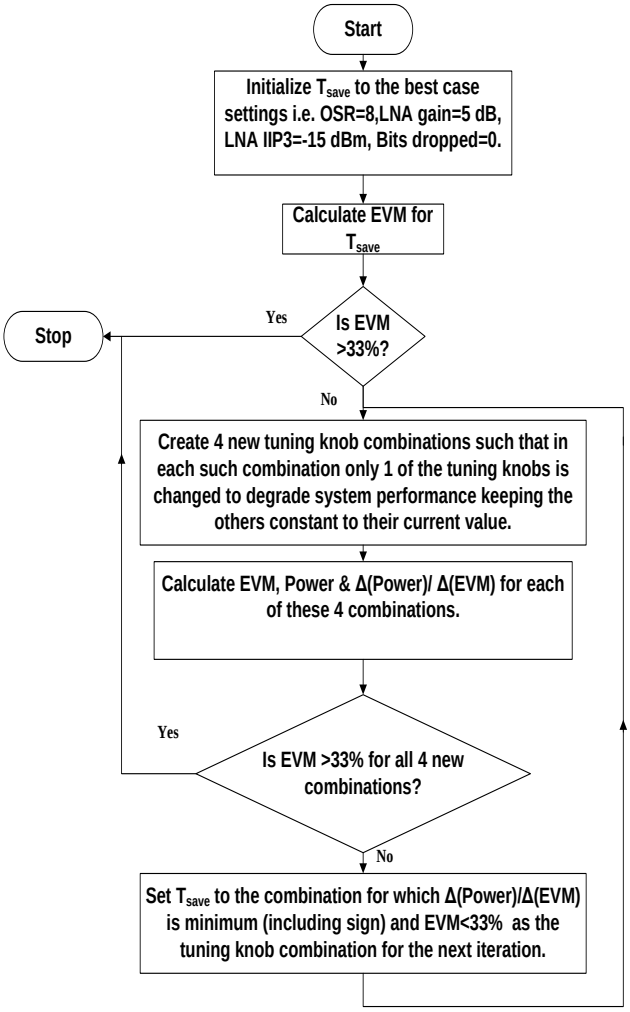


Figure 107: Flowchart of optimization algorithm used

D. ***Results***

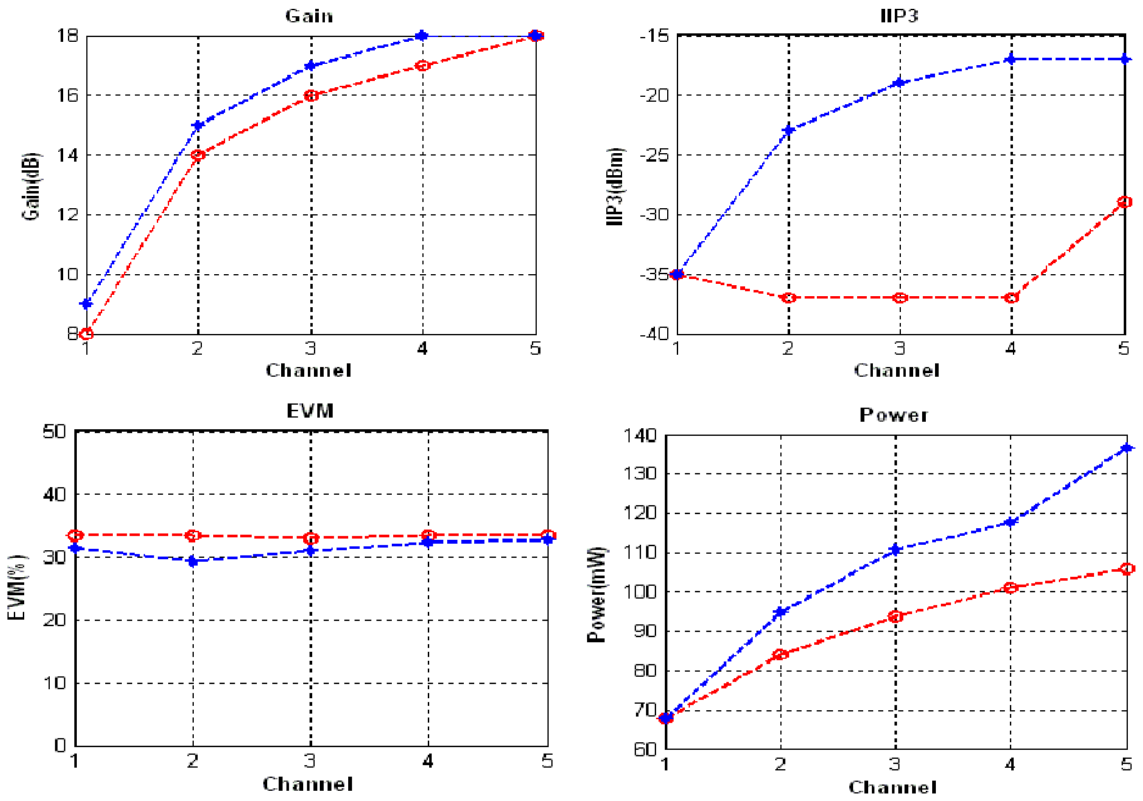


Figure 108: Gain settings, IIP3 settings, EVM and Power for channels with progressively increasing path loss (attenuation) but constant high output SNR

In this section we present the simulation data for the comparison of orthogonal and non-orthogonal receivers. We perform the simulation for 2 cases:

(a) Constant high SNR at LNA input, varying attenuation (path loss) of channel.

(b) Varying SNR at LNA input, constant low attenuation (path loss) of channel.

For each of these 2 cases we construct several channels and run the optimization algorithm on the receiver chain to find the optimum tuning knob setting.

Constant high SNR, varying attenuation(path loss)

We construct a series of channels with constant SNR but attenuation progressively increasing with channel index. As the attenuation increases the signal

strength becomes smaller and the noise added by the LNA becomes more and more significant. Thus using Friis formula for noise we can say that we require a higher gain from the LNA. However as the signal strength is small a low IIP3 is sufficient. For orthogonally tunable LNA the gain can be tuned independent of the IIP3 and hence the gain is scaled up while IIP3 remains low. However for the non-orthogonal tuning case IIP3 also scales up with gain. Thus in the first case we have increasing gain with almost constant low IIP3. In the second case we have increasing gain and IIP3. This leads to a higher power in the second case. Thus orthogonal tuning knobs lead to power savings. The LNA gain, IIP3 and power consumption across the channels is shown in Figure 108. The difference in power savings for the 2 cases for the maximum attenuation is found to be 22.35%.

Varying SNR, constant low attenuation(path loss)

In this case a number of channels having the same relatively low attenuation, but with SNR (at LNA input) progressively reducing with channel index, is constructed. As the attenuation is low, the signal strength is high and the contribution of the NF to the total noise is small. Instead the major contribution to EVM comes from the signal hitting the non-linearity. Thus to reduce the contribution of non-linearity to the EVM, the IIP3 has to be scaled up as the SNR degrades across the channels. Gain on the other hand can be kept relatively small. However as in previous case this is not possible in the non-orthogonally tunable LNA as the gain scales linearly with IIP3. Thus here again the orthogonal system leads to a larger power savings. The simulation results are shown in Figure 109. We see that the gain for the orthogonal case remains much smaller than the

non-orthogonal LNA. The system with orthogonal tuning knobs provides a maximum power savings of 13.5% over the non-orthogonal case.

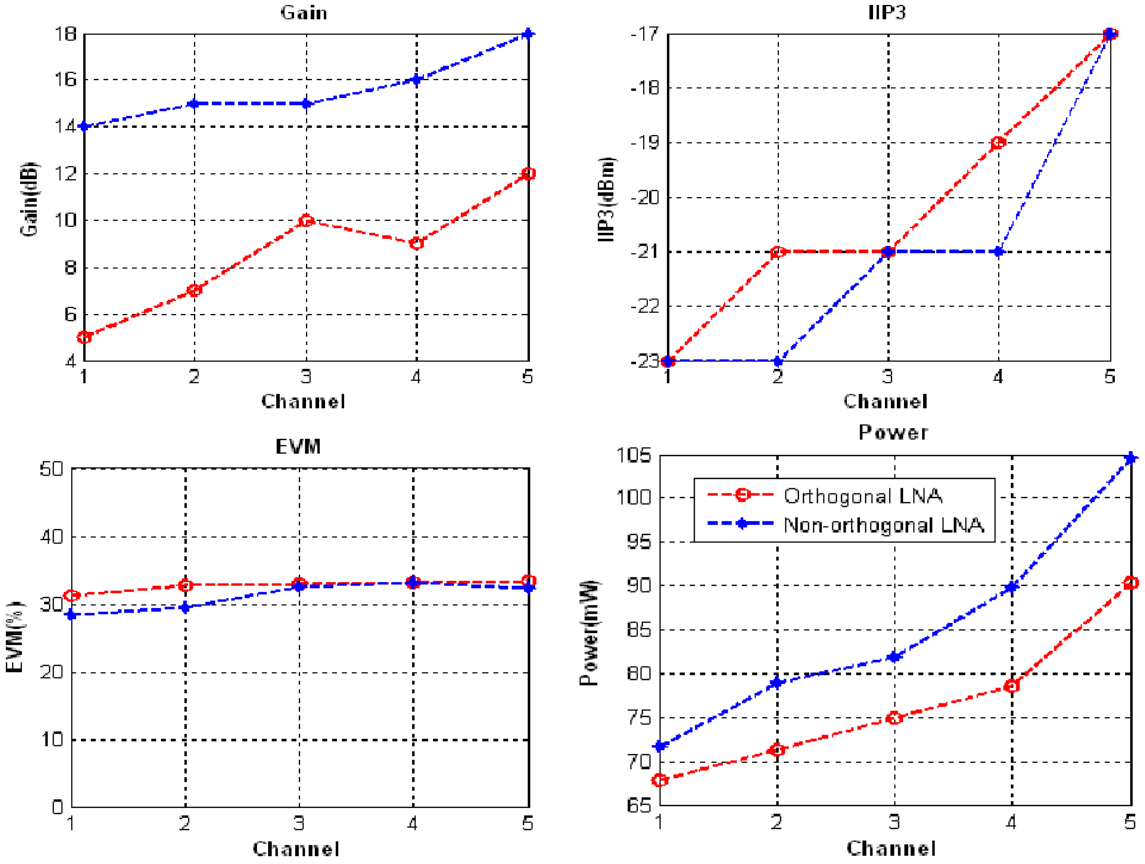


Figure 109: Gain settings, IIP3 settings, EVM and Power for constant path loss (attenuation) and progressively noisier channels

E. Summary

This work demonstrates the benefits of using orthogonal tuning knobs in a RF receiver and also compares the results with a RF receiver where all the knobs are not orthogonal. It is shown through simulation that the use of orthogonal tuning knobs leads to significant savings in power. In other words with the use of orthogonal tuning knobs a greater region of the performance space becomes available to the optimization algorithm. This enables it to choose a point which has greater power savings in many cases. The orthogonal tuning knobs led to an additional power savings of 22.35%. This savings is

over and above the significant savings already made in the power adaptive system. However, it should be noted that the actual power savings would vary with system architecture, nature of tuning knobs and the associated power laws. Thus, although the total power savings would vary from case to case, having orthogonal tuning knobs reduces the chances of the optimized tuning knob solutions being sub-optimal.

5.3. Low-Power Jammer Detector for Adaptation to Channel Blockers[4]

In the previous sections, we have shown how adaptive receivers can save power by adapting to different channel conditions. We've also shown how built-in special (orthogonal) tuning capabilities can make this adaptation optimal. However, the adaptation discussed henceforth assumed there are no jammer/interferer present in the channel. In this section we discuss the effect of jammers and how they can be detected using an ultra-low power jammer detector. Once the strength of jammer is detected the receiver can be configured accordingly to adjust its linearity to process the jammer by adapting tunable building blocks (LNA, mixer, filters) such as the orthogonally tunable LNA.

5.3.1. Need for Receiver Adaptation to Jammer

Jammers/interferers/blockers are undesired signal close in frequency to the desired received signal. They can be generated by a close by transmitter on a different wireless device or even from the same wireless device. For example, in case of a mobile

[4] Please refer to the journal version for an updated version of the work presented in this section.

phone having GSM (voice), DVB-H (mobile TV) and Wi-Fi (internet) the GSM and WiFi transmitted signals act as jammers for the DVB-H receiver. Since the jammers have significantly higher amplitude than that of the weak received signal, even after filtering it has significant effect on distorting the received signal. The strong jammer takes the LNA or the following receiver components into saturation reducing the capability of these blocks of processing the weak desired signal. One solution is to build a highly linear receiver to handle jammers but it results in unacceptably high power consumption. Hence the jammer strength should be detected properly and the receiver should be adapted accordingly: high linearity (high power) when jammer is present and low power when it's absent. Figure 110 shows the possible important cases of the channel with different SNR and jammer strength and highlights the receiver/LNA requirements for each channel. It also shows the power consumption that should be expected for each case if the receiver can be adapted.

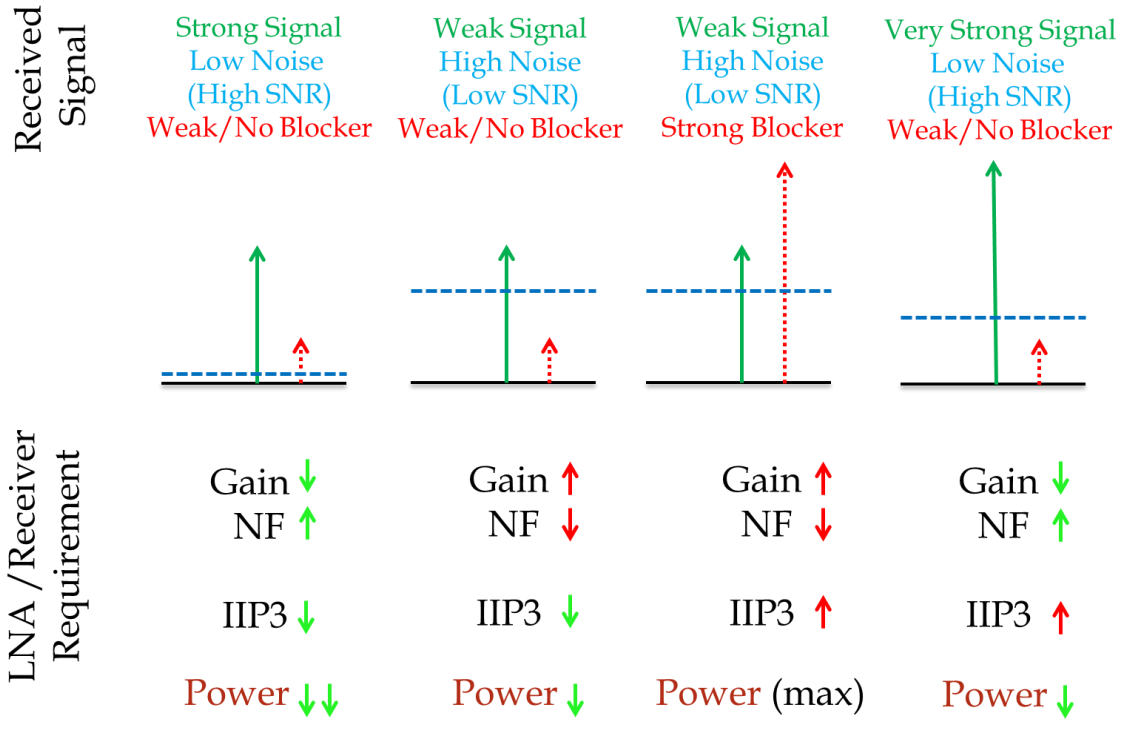


Figure 110: Possible important cases of the channel receiver/LNA requirements for each channel along with the power consumption that should be expected for each case if the receiver is adapted.

5.3.2. Background and Overview of Jammer Detector

To simultaneously meet the stringent power budget and high performance requirements modern portable radio receivers employ adaptive circuit/system techniques. Adaptive receivers [157], [158] opportunistically reduce its power consumption when operating environment is better than its worst case. The highest power requirement in wireless receiver design comes from the widely varying signal and blocker/jammer scenarios that a receiver has to deal with. Handling high blocker requires high linearity whereas low signal strength calls for very low noise figure and high gain. One way to save power in a receiver is to operate in a low linearity mode when there are no jammers present in the radio channel. To enable this, adaptive receivers' monitor the signal and jammer strength by employing an extra built in low power circuit called jammer detector (JD) that can detect the presence of jammers in the operating environment.

Traditional jammer detectors used in commercial receivers are narrow band (NB JD) [158], i.e. they can only look for jammers in the close vicinity of the signal. They are generally implemented by tapping the intermediate/low frequency output of the down-conversion mixer. Similar implementation of an NBJD can be found in [159], that uses 4 power detectors (2 in IF frequency and 2 in digital) to measure the power in different points along the receiver chain to estimate jammer and signal powers.

However, only NBJD does not provide the true jammer scenario as it cannot give an estimation of far-out jammers (caused by own transmitter in concurrent operation

mode or from other transmitters) which also cause problems when the signal to be sensed is very low and the jammers are very high power. For example a DVB-H receiver suffers from such far out jammers at GSM (900 MHz), WLAN (2.4GHz) and jammers at odd harmonics of the local oscillator frequency. The only circuits that are capable of measuring these jammers are on-chip spectrum analyzer [160] or multi-resolution spectrum sensing [161] developed for cognitive radios, both of which are significantly high power, consuming almost same power as the receiver itself.

To address the issue of far-out jammer detection this work proposes the design of an ultra-low power miniature wideband (1GHz @ 2.2 mW, 2.4 GHz @ 3.6 mW) jammer detector (WBJD) as part of an adaptive DVB-H receiver. This design includes a high gain low power RF amplifier to increase JD sensitivity, a low power peak detector and digital conditioning circuit that allows a programmable attack time, all within 2.2 mW.

5.3.3. Motivation & Working Principle

The motivation of this work to develop a state-of-the art lowest power, low area wide band jammer detector (WBJD), capable of measuring far-out jammers and work in conjunction with NBJD for optimal adaptation of the adaptive receiver system. We also target to provide a programmable attack time for the WBJD ranging from µs to ms, i.e., the WBJD can scan at the environment for programmable timing window allowing the receiver to adapt to an instantaneous or average jammer conditions, depending on the system requirements, reducing unnecessary fast switching of the receivers. In summary, the key ideas of this work are:

- To develop the lowest power wideband jammer detector (using ultra low power RF/Analog circuit design techniques).

- To provide programmable attack time for the WBJD (using digital jammer decision circuit (JDC) following the RF)

The WBJD works in conjunction with NBJD to provide an estimate of the far out and close in jammers present. The estimated strength of the received signal, once the jammers are attenuated by the filters in the digital baseband, is used along with WBJD and NBJD output by a system level control algorithm [162] to adapt the receiver for low power. This is done by using adaptive jammer thresholds based on the received signal strength range and the present gain mode (G0, G1 etc).

5.3.4. WBJD Architecture & Circuit Design

This section provides the details of the WBJD architecture, details of each circuit block and simulation results.

A. Receiver Overview

The multi-band DVB-H receiver covers the VHF, UHF and L-band for mobile TV applications. Adaptivity through jammer detection is enabled in the VHF and UHF bands. The signal path containing the LNA, Mixer and Base Band Filters (BBF) has programmable gain modes (G0, G1 etc.) by adapting the LNA and the BBFs. G0 has the highest gain (best sensitivity), lowest linearity(-20 dBm) and power (66.3 mW@ 1.3 V). G1 has little less gain to handle strong jammers with higher linearity (-5 dBm) consuming 1.92× more power (127.4mW). The highest power savings comes from G0 to G1 through use of two different LNA topologies. Traditional JDs are narrow band (NB). Along with a NBJD this chip uses a low power WBJD to detect the GSM/DCS/WLAN transmitters going active in concurrent mode and far out DVB jammers. System level algorithm for adaptation using NB and WB JD is described in [162].

B. WBJD Architecture

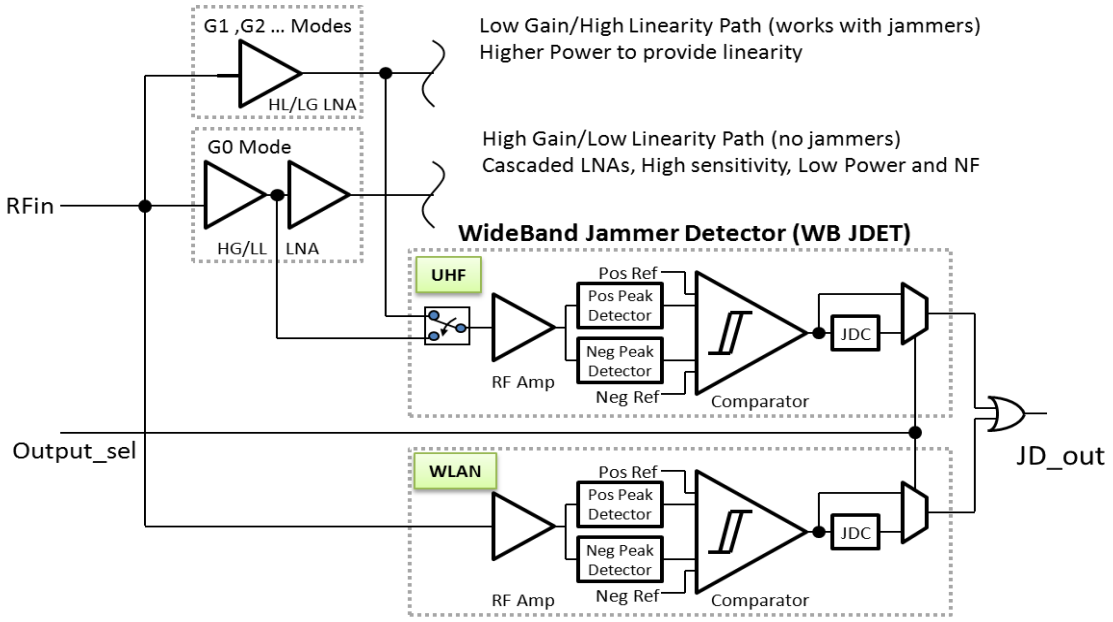


Figure 111: Wide Band Jammer detector(WBJD) architecture within the DVB-H receiver

Figure 111 shows the architecture, consisting of two WBJDs, for UHF and DCS/WLAN band. The UHF JD detects DVB & GSM jammers in G0/G1 gain states. The input is sampled from the LG LNA output in G1 and HG LNA 1st stage output in G0, instead of the RF input to achieve a low -50 dBm sensitivity by having significant gain from the signal path. The WLAN JD directly samples the RF input as the sensitivity requirements are relaxed. Compared to the UHF JD the WLAN JD consumes more current to provide wider bandwidth up to 2.4 GHz. The outputs are ORed to find the final JD output. Either one or both the detectors can be turned on as required. Each JD consists of a RF amplifier that amplifies the weak jammer signal to be detected simultaneously by positive and negative peak detectors, to increase sensitivity. An analog comparator compares the detected value with a pre-defined programmable threshold to provide a high

or low output. A JD decision circuit (JDC) provides a programmable attack time by counting the no. of jammers present within a time window and asserting a high JDC out if the jammer has existed long enough. Either the comparator output or the JDC output can be sampled out using a MUX.

C. Ultra Low-Power RF Amplifier

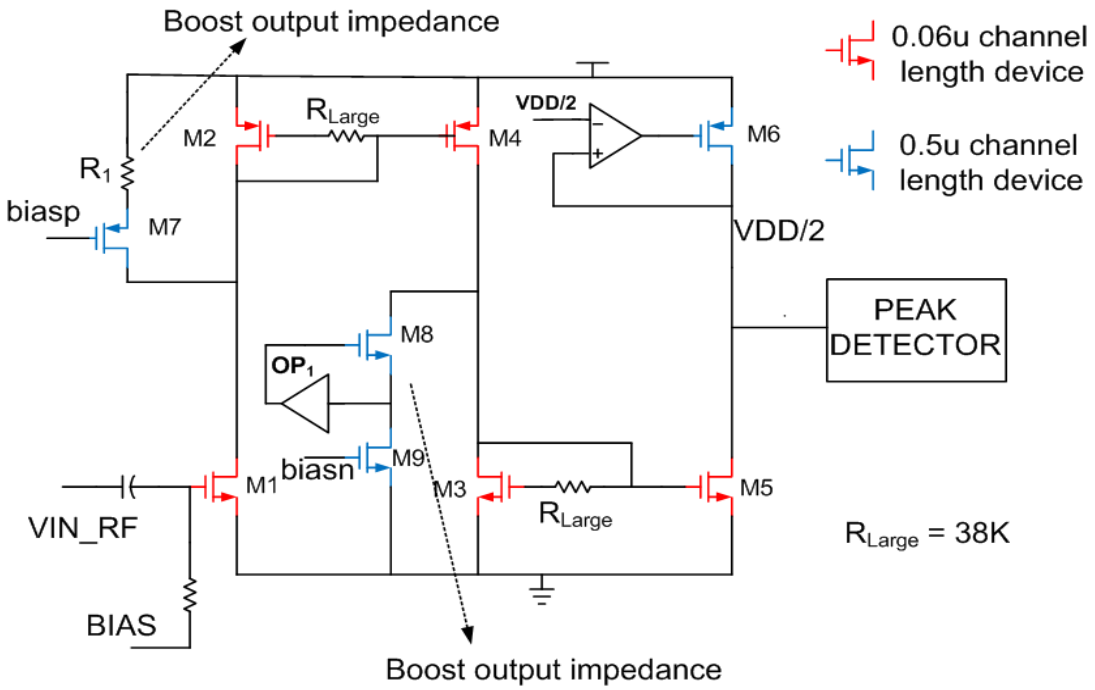


Figure 112: Peaking Current Mirror based low power RF amplifier

The RF Amp provides high gain at very low power the using wideband current mirror based amplification. To boost the f_t of as standard current mirror bias current has to be increased. With the peaking current mirror [163] a large resistor R introduces a zero that extends the BW with a low bias current. Figure 112 shows the schematic of the 3 stage RF Amp using peaking current mirror based amplification. M1 converts the RF signal into current mode, M2-M4 and M3-M5 peaking current mirrors amplify it twice and high impedance active load M6 converts it back to voltage mode. M1 is kept small reduce loading. To provide enough gm the DC current in M1 has to be significant, which

when multiplied by the gain of the current mirrors result in high DC current in the following branches. A DC current stealing approach is used to keep the 2nd and 3rd stage current low while providing the same AC gain. Transistors M1 to M5 that carry the RF signal are minimum channel length to maximize BW. M6 to M8 are long channel to provide high impedance. At 65nm even the rds of the long channel devices are not high enough. To reduce loading of the current stealing branches, R1 degenerates M7 to increase output impedance and M8, M9 along with OP1 provides high impedance using active cascode. Active biasing of M6 allows high output impedance and maintains output node at half Vdd. The BW of RFAmp varies between 1GHz to 2.4GHz based on the bias current. The bias currents are derived from a bandgap circuit and the biasp & biasn voltages are derived from a replica amplifier circuit for stable gain. The RFAmp has 30dB gain with ±1 dB over temperature and process. It consumes only 720 µA@1.3V for 1 GHz BW.

D. Peak detector and Comparator

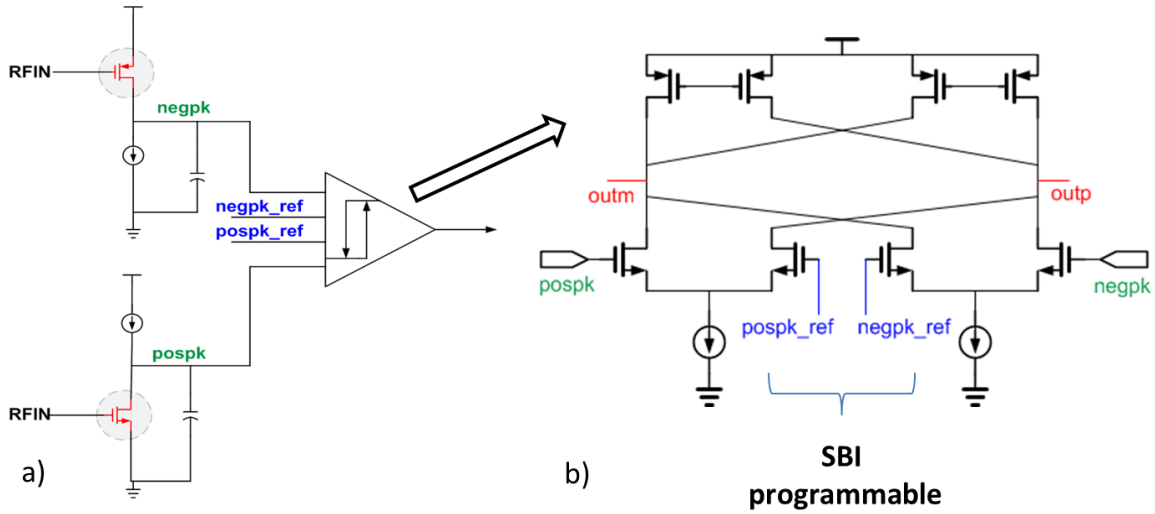


Figure 113: a) Peak detector and b) Analog Comparator

Two peak detectors detect the positive and negative peak of the RF signal. In contrast to traditional source follower based peak detectors common source devices, biased in weak inversion are used, that turn on when the input swings beyond a certain threshold causing a half wave rectified current to flow through the capacitor. The capacitors hold the peak of the waveform. A hysteresis comparator compares the peak detector outputs with references, programmable through SBI. The wide BW peak detectors provide 7dB gain to increase sensitivity.

E. JD Conditioning Circuit : Programmable Attack Time

Figure 114a shows the JDC decision scheme. As soon as a jammer is present the analog comparator turns high within 2 to 3ns. However the system requires a programmable attack time ranging in us to ms. This is achieved by a 10-bit master counter and an 8-bit slave counter. Once the jammer arrives for the 1st time an analog timer (relaxation oscillator with variable time period from 2.4 to 6.1 μs) starts to run and drives both the master and slave counter. The master counter keeps on counting up to its timeout value and provides a JD timing window ranging from 5μs to 6.3ms. The slave counter counts iff the comparator output is high (Figure 114a and Figure 115b). At the end of the time period a timeout signal is asserted that resets all the JDC circuits. The slave counter provides an average value of how long jammer was present within the JD timing window. If this value is greater than a predefined threshold the JDC asserts a JD_out meaning jammer is present long enough in the environment.

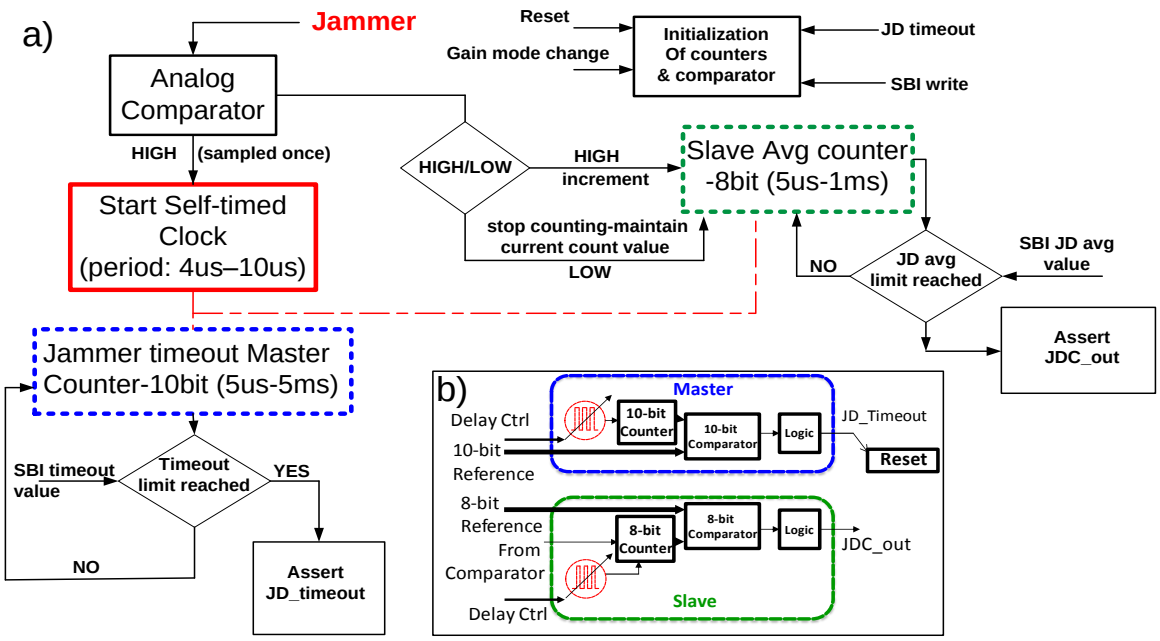


Figure 114: a) Jammer detect decision scheme b) Master counter maintains timeout whereas slave counter finds out the average jammer value and asserts JDC_out

F. Simulation Result: WBJD system in operation

Figure 115a and b show the conceptual diagram of jammer detection and timeout. Figure 115c shows simulation result of the complete system including LNA and WBJD under the presence of a continuous jammer. With jammer present, the comparator output is high and both the master and slave clocks are running. Both the counters keep on counting until the slave counter reaches a pre-programmed threshold (=5 in this simulation). This means jammer is presents long enough and JDC_out goes high resulting in a gain mode change from G0 to G1 and all the JDC states are reset.

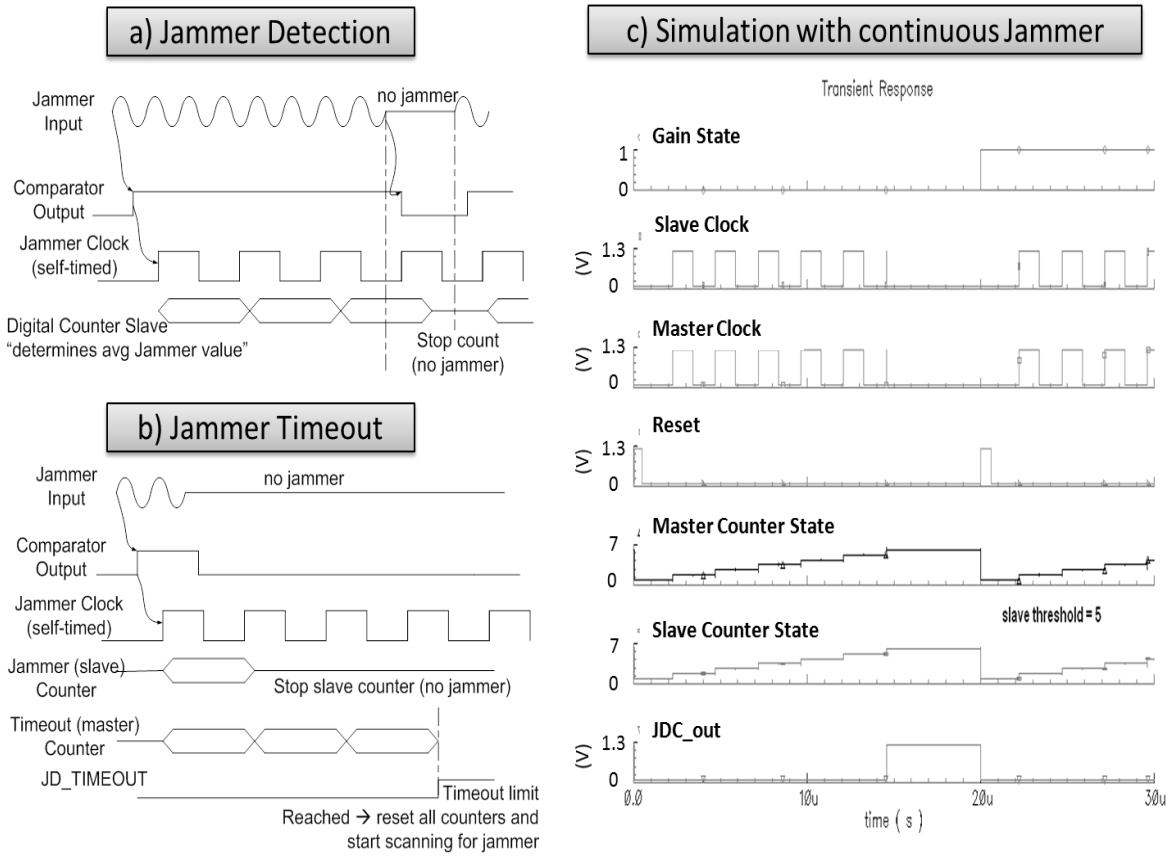


Figure 115: a) Slave counter provides average value of jammer b) Master Counter determines time window within which jammers are counted once the first jammer comes. At the end of this window it provides a timeout which resets all JDC states. c) Simulation result and timing diagram with continuous jammer present (JDC_out goes high, gain mode changes and resets all JDC states)

5.3.5. Fabricated Chip and Measurement Results

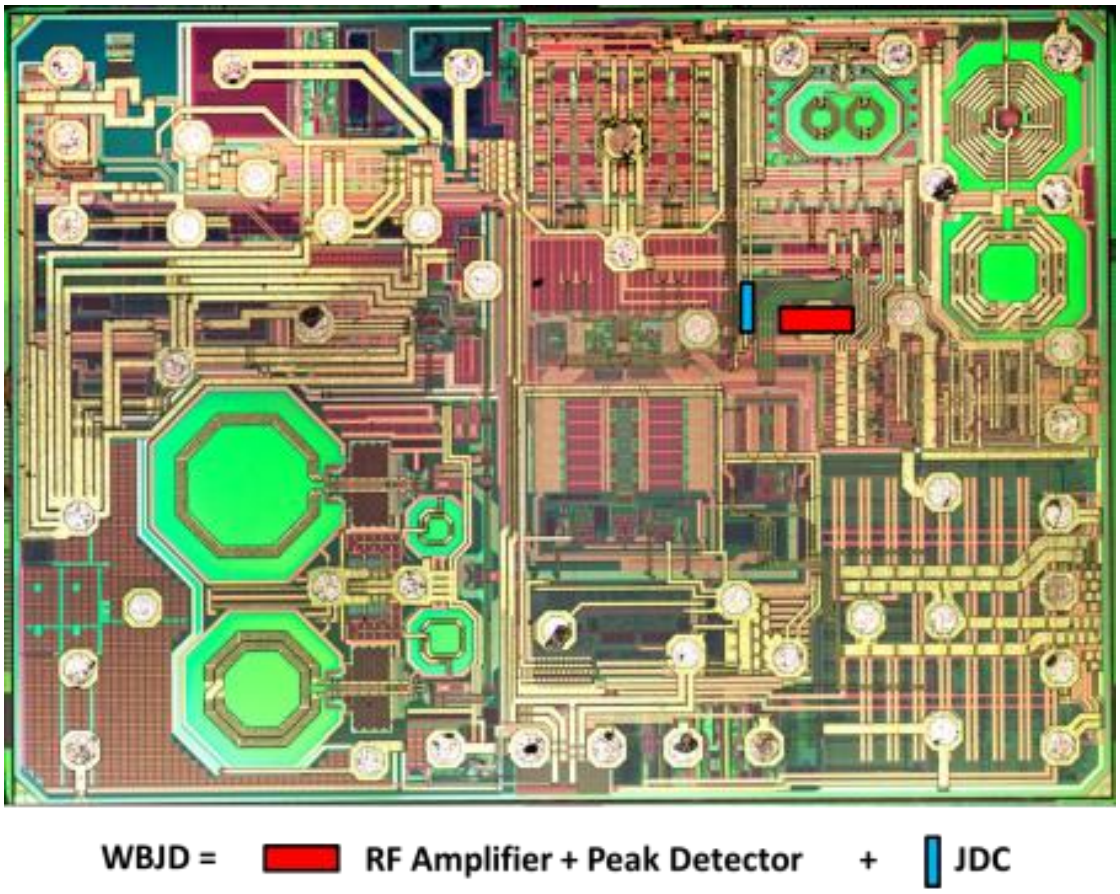


Figure 116: Die photo of complete multi-band adaptive DVB-H receiver including the Wide Band Jammer Detector (WBJD: QUALCOMM Confidential, used with permission)

Figure 116 shows the chip micrograph of the DVB-H receiver. The WBJD is only 0.45% of the total chip area. The UHF JD designed in 65 nm CMOS consumes a total of 1.713mA (RFAmp 720µA, Peak det & Comparator 392 µA, JDC 305 nA, Current DAC 98 µA and Replica bias 503µA) from 1.3V supply. With 2.2mW total power and 0.015 mm2 total area this WBJD could easily be incorporated in any adaptive receiver without significant power or area penalty. This design hence provides the lowest power reported wideband jammer detector and is compared with its contemporaries in Table 11.

Figure 117 shows measurement data from the DVB-H receiver for UHF WBJD trip points in both G0 and G1 mode for different jammer frequencies (signal at 671 MHz) ranging from 150 MHz to 900 MHz (GSM). The worst case WBJD trip point is -49 dBm and most of the trip points achieve the targeted sensitivity -50 dBm. The variation with frequency is expected by design and is taken care of by the algorithms of the control system [162] in the adaptive receiver. Measured WBJD trip points over frequency for 20 devices in Figure 118a for G0 mode and measured WBJD trip point histogram with GSM jammer in G1 mode is presented in Figure 118b. The adaptation switch-points for different gain modes of the adaptive receiver is shown in Figure 119 with and without the presence of jammer.

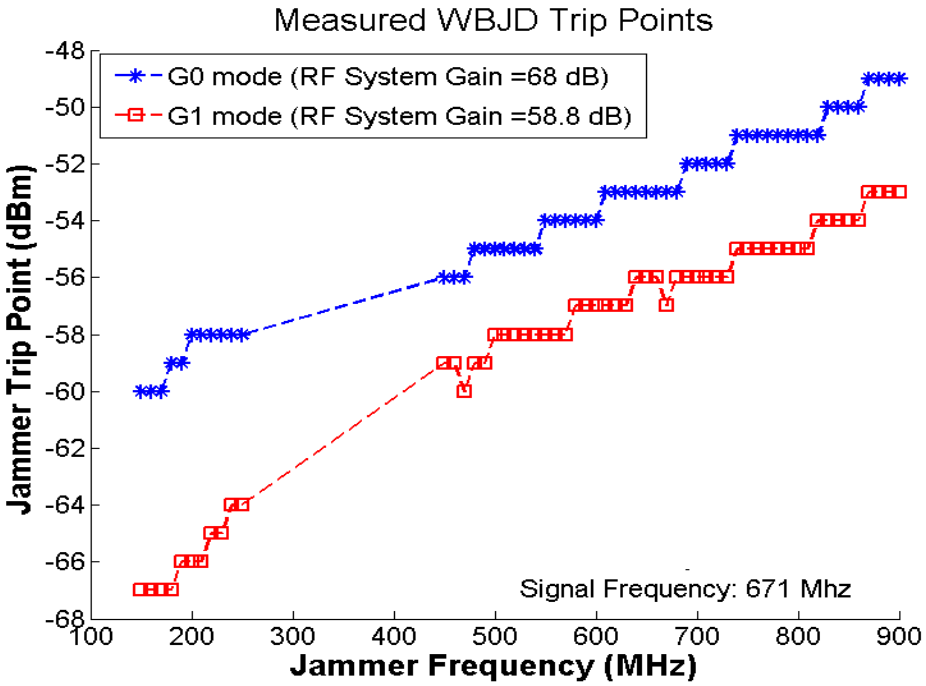


Figure 117: a) Measured WBJD trip points over frequency in G0 mode and G1 mode (with DVB-H signal at 671 MHz)

In summary, the design of an ultra-low power wideband jammer detector for sensing far out jammers is presented. It combines ultra-low power RF circuit design

techniques with a programmable digital decision circuit to provide 1GHz wide jammer detection capability at only 2.2mW power with a programmable attack time ranging from 5µs to 6.3ms. Such a low power WBJD enables adaptive operation of wireless receivers making the receiver system significantly low power.

Table 11 Comparison with other Jammer detectors

Technology	Power	Area	BW	Tech Node	Comment
WBJD (this work)	**2.2 mW**	**0.015 mm^2**	**1 GHz**	65 nm	Power detection based, low power, low area, wide BW
NBJD [2]	~6 mW	~0.1 mm^2	80 MHz	65 nm	Power detection based, low power moderate area, BUT narrow BW
Spectrum Analyzer [s1]	49.2 mW	0.88 mm^2	7 GHz	0.13µm	Provides frequency information with coarse resolution, significantly high power
MRSS [s2]	122 mW	9.2 mm^2 (with pads)	UHF Band	0.18µm	Provides frequency information with both coarse and fine resolution, extremely high power

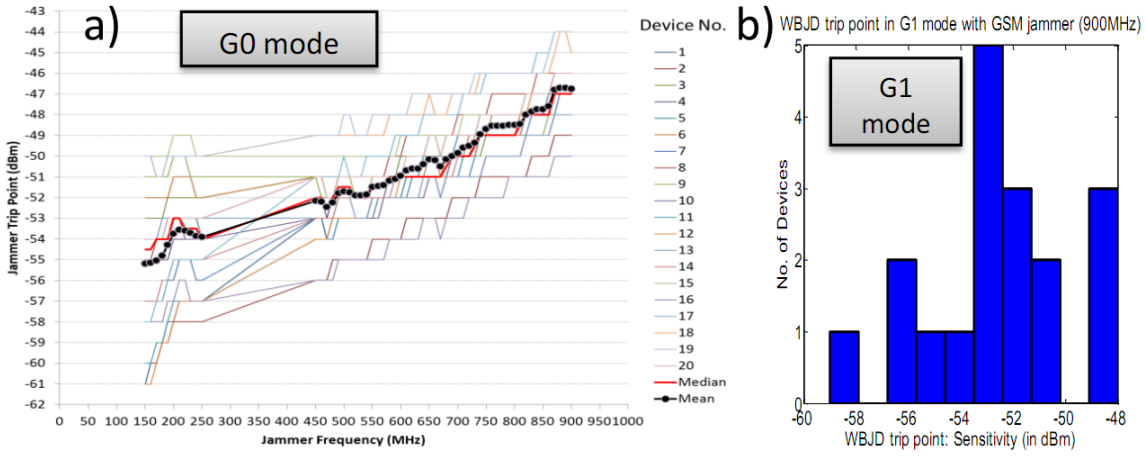


Figure 118: a) Measured WBJD trip points over frequency for 20 devices in G0 mode b) Measured WBJD trip point histogram with GSM jammer in G1 mode (both in presence of desired DVB-H signal at 671 MHz)

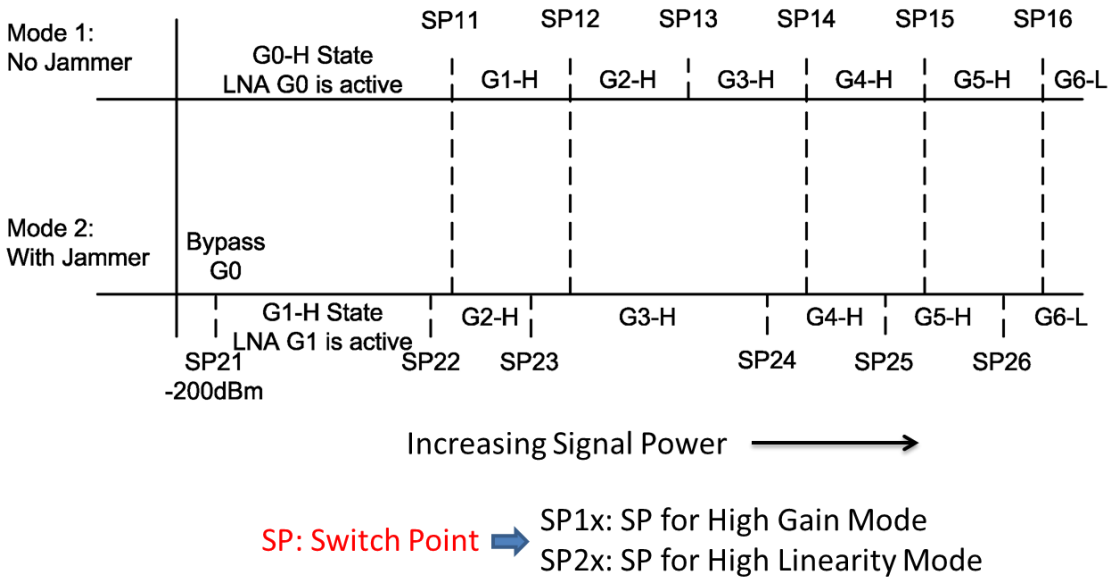


Figure 119: Operation of the adaptive receiver with and without jammer [162]

5.4. VIZOR Receivers for Multiple Input Multiple Output (MIMO) Systems

In this section we investigate the applicability of VIZOR or real-time low power adaptation of RF front end systems to Multiple Input Multiple Output (MIMO) systems that are increasingly becoming popular for high data rate robust wireless communication.

5.4.1. MIMO: Basics

MIMO systems are becoming increasingly popular in wireless communication as with duplicated receiver paths it can provide either significant SNR gain (diversity mode) or increased data rate (multiplexing mode) or both depending on the mode chosen. MIMO systems are robust under severe channel conditions and can multiply the data rates very fast using more than one transmitter and receiver.

MIMO systems can be categorized into the following 3 kinds:

a) **1xN system**: 1 transmitter and N receivers are used. Received data from several receivers are combined after channel estimation and inverse to provide diversity gain, or SNR advantage, which can be used for increasing throughput or operating under worse channels. Among the many techniques used for combination of the signals, Maximal Ratio Combining (MRC) is on of the most popular one and would be used in this work.

b) **Mx1 system**: This was first proposed by Alamouti and is called Transmit Diversity MIMO system. This includes M transmitters and only one receiver. The received data can only be decoded if the transmitted data from several transmitters are designed properly using Alamouti scheme and extensions of that.

c) **MxN system**: In general, today's MIMO transceivers can use both transmit and receive diversity to maximize gains. In this case there exist M transmitters along with N receivers.

Simulation framework: A simulation framework for MIMO systems have been developed that can support 2×1, 1×N and 1×1 for comparison purposes. In this work we concentrate on 1xN systems in diversity mode and look at the benefits that can be achieved by applying VIZOR in such a system.

Figure 120 shows a typical 1×2 MIMO system receiver, where data from both the paths are combined after channel estimation and inversion is done. This adds the received signal (as they are correlated) whereas averages the channel noise (as they are uncorrelated) increasing the SNR of the received signal.

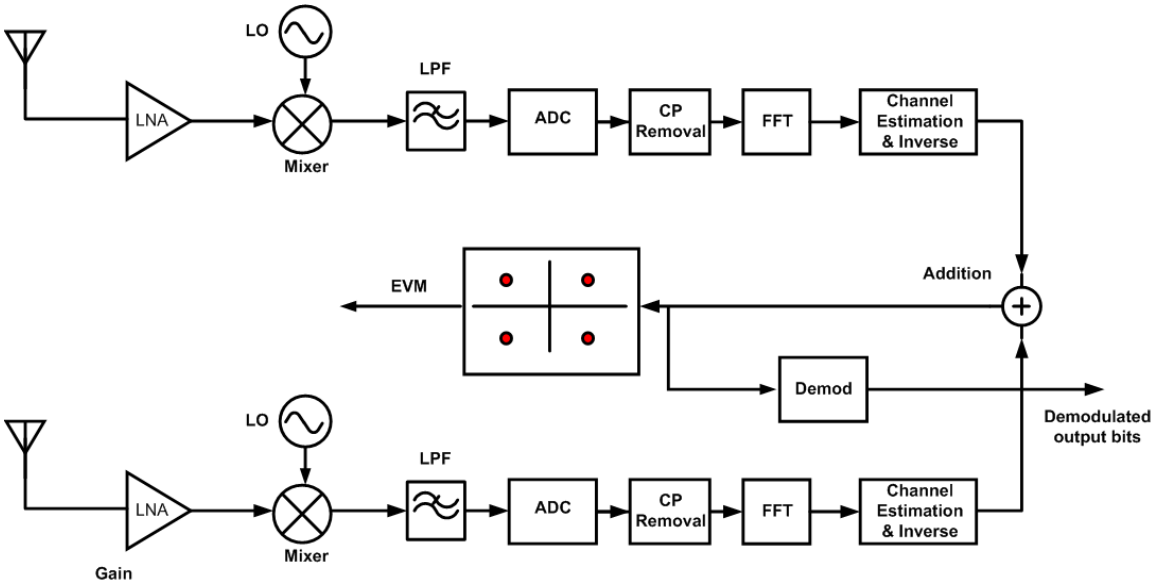


Figure 120: Basic MIMO 1×2 receiver system

5.4.2. MIMO VIZOR

Opportunities: Intuitively, why one should be interested in applying VIZOR to MIMO systems? The key idea is that MIMO systems increase performance of the receiver by using duplicate receiver paths. The VIZOR system saves power by providing only the required amount performance to the receiver. In such an adaptive power constrained system, any performance boost (coming from MIMO mode) may lead to significant extra power savings. In this work we investigate the feasibility of such an approach.

MIMO VIZOR Framework: A simulation framework for MIMO systems including VIZOR mode have been developed to support 2×1, 1×N and 1×1 for comparison purposes. The feasibility study is performed using comparing a 1×1 and 1×2 diversity system. The 1×2 MIMO VIZOR system is shown in Figure 121, where the Gain and IIP3 of both the LNA's are controllable using VIZOR control loop driven by closed loop feedback control. The effect of VIZOR operation is studies in next sub-section.

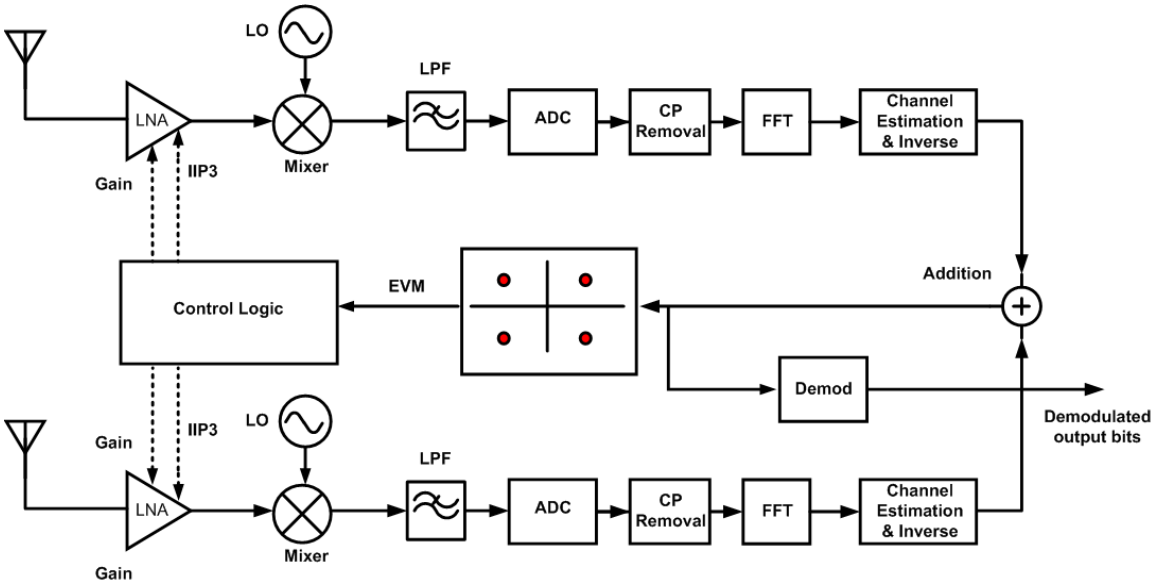


Figure 121: MIMO VIZOR 1×2 receiver system

5.4.3. Extra Power Saving using MIMO VIZOR Mode

In the receiver in Figure 121 power performance tradeoff in the receiver can be achieved by either controlling the Gain or the IIP3 of the LNAs. For clearer understanding, we change one at a time and study the benefits achievable. In this work we have assumed symmetric change of the receiver LNA's. If more power savings can be achieved by changing the LNAs differently from each other should be studied later.

Effect of IIP3 Scaling: For a given received signal strength, the IIP3 of both the LNA's in the two receive paths are changed simultaneously. The results are compared with a 1×1 system by varying IIP3 of the single LAN similarly. Figure 122 shows that 1×2 systems have a constant advantage over 1×1 systems. This is coming from benefits due to averaging of the constant channel noise. However, this benefit is dependent on the channel noise and does not increase with LNA performance degradation. Hence, it can be claimed that if power performance degradation is achieved by IIP3 scaling, MIMO systems do not have significant advantage over SISO systems for application of

adaptation (VIZOR mode). This is intuitive as the degradation in IIP3 distorts the signal in a deterministic way, leading to no extra improvement in SNR by combining two similarly distorted signals.

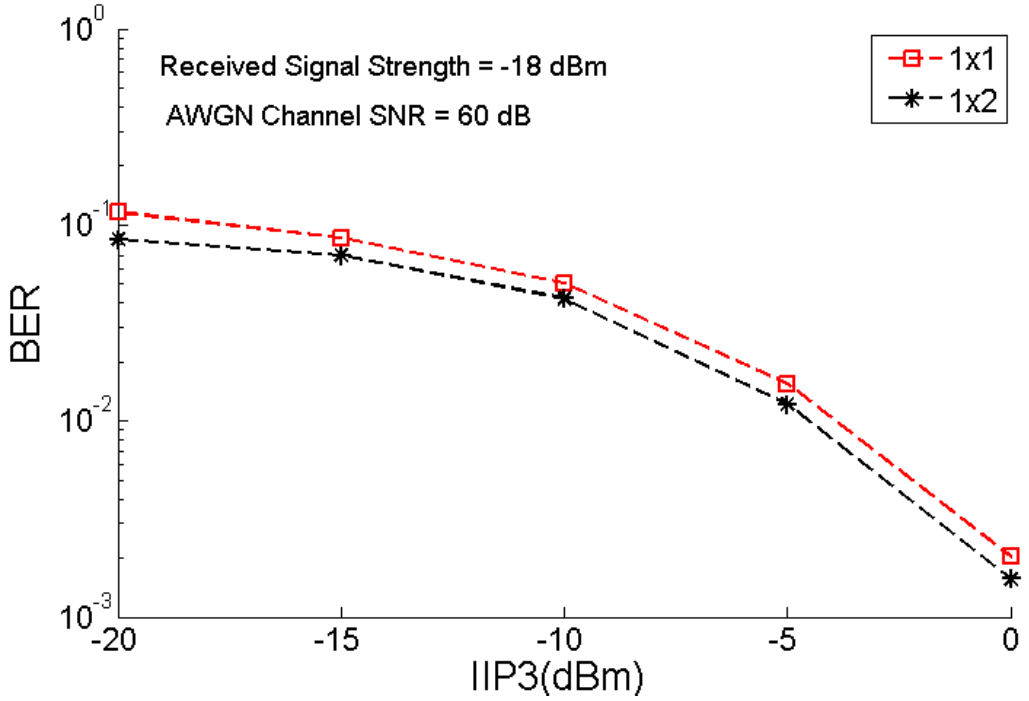


Figure 122: BER for 1×1 and 1×2 systems with different LNA IIP3

Effect of Gain/NF Scaling: On the other hand, if the Gain of the LNA is scaled down (along with increase in LNA NF); the sum effect is to increase the receiver noise figure (NF) as the receiver power is reduced. The system performance for 1×1 and 1×2 is plotted in Figure 123 as the receiver NF is increased. We see a significant improvement from 1×1 to 1×2 systems. This happens as the noise introduced by both the receivers are uncorrelated and hence by MIMO system this noise can be averaged out, leading to cleaner signal under the performance degradation mode using Gain/NF control.

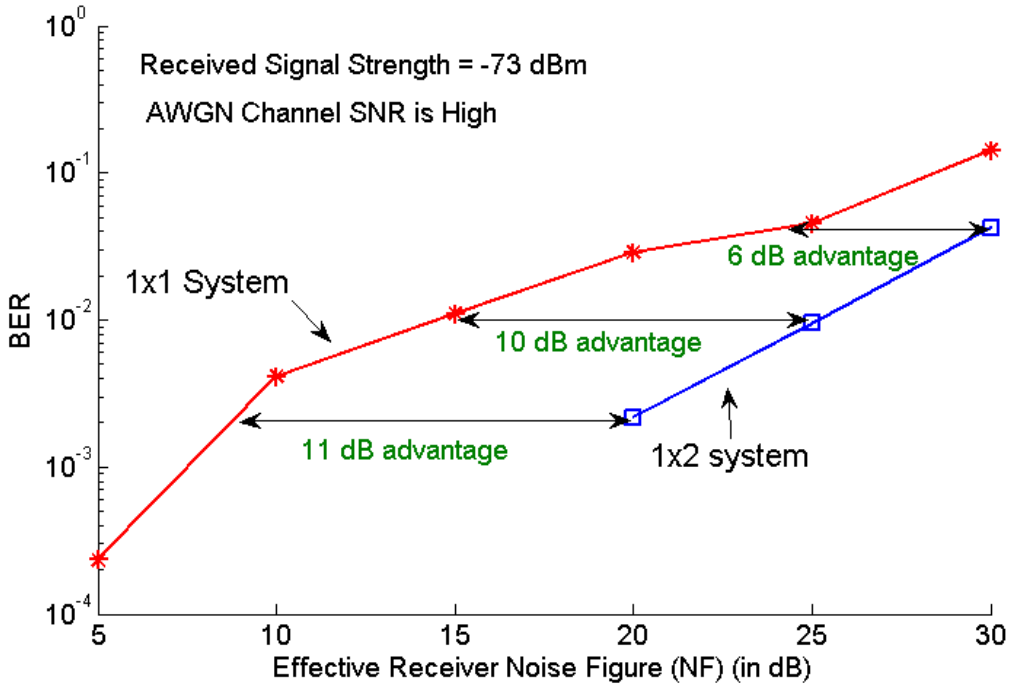


Figure 123: BER for 1×1 and 1×2 systems with different receiver Noise Figure (NF)

Power Savings: As can be seen from Figure 123, the benefits in SNR (NF that can be tolerated for the same BER) varies from 6 dB to 11 dB, i.e. about 8 dB on an average. It implies that if a 1×2 MIMO system is used instead of a 1×1 system the receiver in the MIMO system can have about 8 dB extra NF. As the power consumption of an amplifier doubles for reducing the NF by 3 dB, a 8dB relaxation in NF means each amplifier would consume $2^{-8/3}$ P, i.e. 0.16P power, where P is the power consumption of a comparable amplifier with 8 dB higher NF (that is used in a 1×1). However, MIMO systems would require 2 paths, leading to total power consumption of 0.32P plus extra power for buffers to route LO signal. This implies, using a MIMO VIZOR system in 1×2 mode, the total RF front end power could be reduced to about ***half*** of what is required in 1×1 VIZOR systems.

Chapter 6. Pro-VIZOR: Process Variation Tolerant VIZOR

With continued scaling the of device geometry in the nanometer regime the controllability of the fabrication process has reduced significantly, resulting in severe process variation. The effect of process variation in Analog/RF circuits shows up as failing of one or more specifications, resulting in classification of the device as faulty. This in turn reduces the yield of the system. To increase yield under process variation more built in design margin is required for static designs, increasing power consumption. Hence low power adaptive design methodologies become even more significant under sever process variation.

The previous section described the environment-adaptive VIZOR operations of the transmitter and receiver modules of MS for changing channel conditions. In both the cases, the device operation follows a pre-defined control law ('locus') that is obtained during the design/characterization phase. It should be noted that the optimal control law that is obtained is specific for a device and may not work well for another device in the manufacturing lot due to process variations. To address this issue, a test and process tuning (calibration) procedure must be performed during the production test phase to ensure that all the device operate at minimum power level while satisfying the system EVM/BER. The main components of such a *process variation tolerant environment adaptive transceiver* are discussed below.

6.1. Components of Process tolerant VIZOR (Pro-VIZOR)[5]

The enabling technology that operates the wireless device at minimum power consumption levels across all environmental (channel) conditions and process variation consists of:

- **Channel Sensing:** The wireless device should be able to accurately estimate the current operating environment so that it can adapt accordingly. Here environment refers to the transmission channel between the wireless access point (AP) or base station (BS) and the mobile station (MS).
- **Process Sensing:** To ensure optimum adaptation to varying channel conditions, the device should be able to self-test and ascertain the performance sensitivity of the individual circuit components to adaptation. Due to the process spread in manufactured devices, the adaptation in each device should be *calibrated* to enable minimum power operation. Unlike channel sensing (which is continuous), process sensing is a one-time procedure performed during production test.
- **Process and Environment Adaptability:** For this purpose, process estimation of the device is performed using simple tests during the production test/tuning phase, and process tuned. During run time operation, the process-tuned device uses a set of tunable 'knobs' that can be used to adaptively tune the system to continuously varying channel conditions. Given any operating channel, the system should consume only the minimum amount of power required to maintain desired performance. This requires that the components (RF circuits, ADC, baseband

[5] Please refer to the journal version for an updated version of the work presented in this section.

processing) of the wireless device to be dynamically adapted using an optimal control law.

- **Control Algorithm for Environmental adaptation:** A system-level multi-dimensional control algorithm that actuates environment sensing and adapts the process-tuned device using closed-loop feedback is required. The tuning of system components is based on an optimal control law ('locus') that is obtained during pre-production device characterization and later calibrated (process tuned) during production test.

The channel sensing and environmental adaptation was described in last section. Here we discuss how process sensing and tuning for process variation.

6.2. Process Sensing using Test

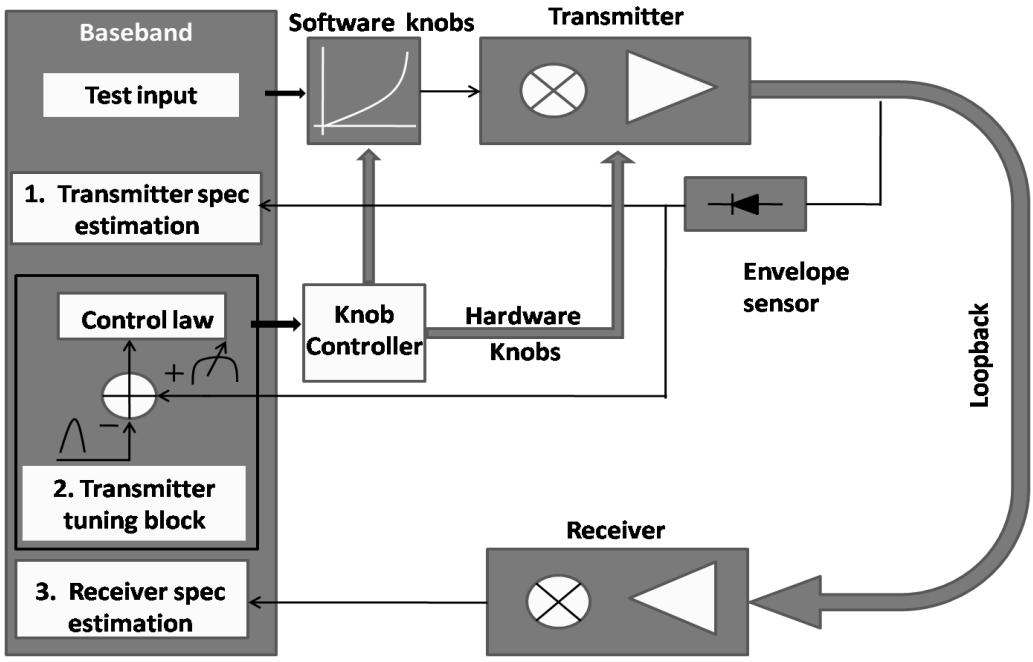


Figure 124: ACT based loopback testing approach

Process sensing and tuning is performed using simple tests during the production testing phase of the product development cycle. Alternate testing methodology [47] has been proposed to devise simple and fast tests to estimate complex specification through simple test measurements using supervised learning techniques. Loopback based alternate testing of RF transceivers has been proposed earlier as a low-cost production test technique where the performance-parameters (specifications) of a complex transceiver are estimated using a simple test approach. In loopback based alternate testing the output of the transmitter is looped back to the receiver to estimate the receiver parameters. But loopback test suffers from accuracy issues because the looped back signal from the transmitter usually does not have high fidelity due to process variations in the transmitter itself. An adaptive testing technique such as shown in Figure 124 enables process sensing using loopback test highly accurate.

Adaptive calibration test (ACT): the adaptive test methodology adopts a two- step procedure to ensure high accuracy of estimation.

- Test the transmitter for its specifications.
- Tune the transmitter for process variations by changing the available hardware and software knobs to ensure a near ideal operation of the transmitter
- Estimate the receiver specifications using loopback from the transmitter.

The tuning performed in this phase of product development cycle is to facilitate low-cost process test. Once the specifications are estimated accurately the tuning knobs can be reverted back to nominal operating conditions.

Tuning technique: In ACT based tuning technique we make use of an envelope detector to obtain information about the transmitter characteristics. A golden envelope response pertaining to an ideal transmitter instance is obtained before-hand.

Circuit tuning: A simple gradient based adaptive algorithm is used to dynamically control the circuit tuning parameters. The algorithm tunes the bias and supply values continually till the observed envelope of the system is within a certain tolerance limit in comparison to the golden envelope.

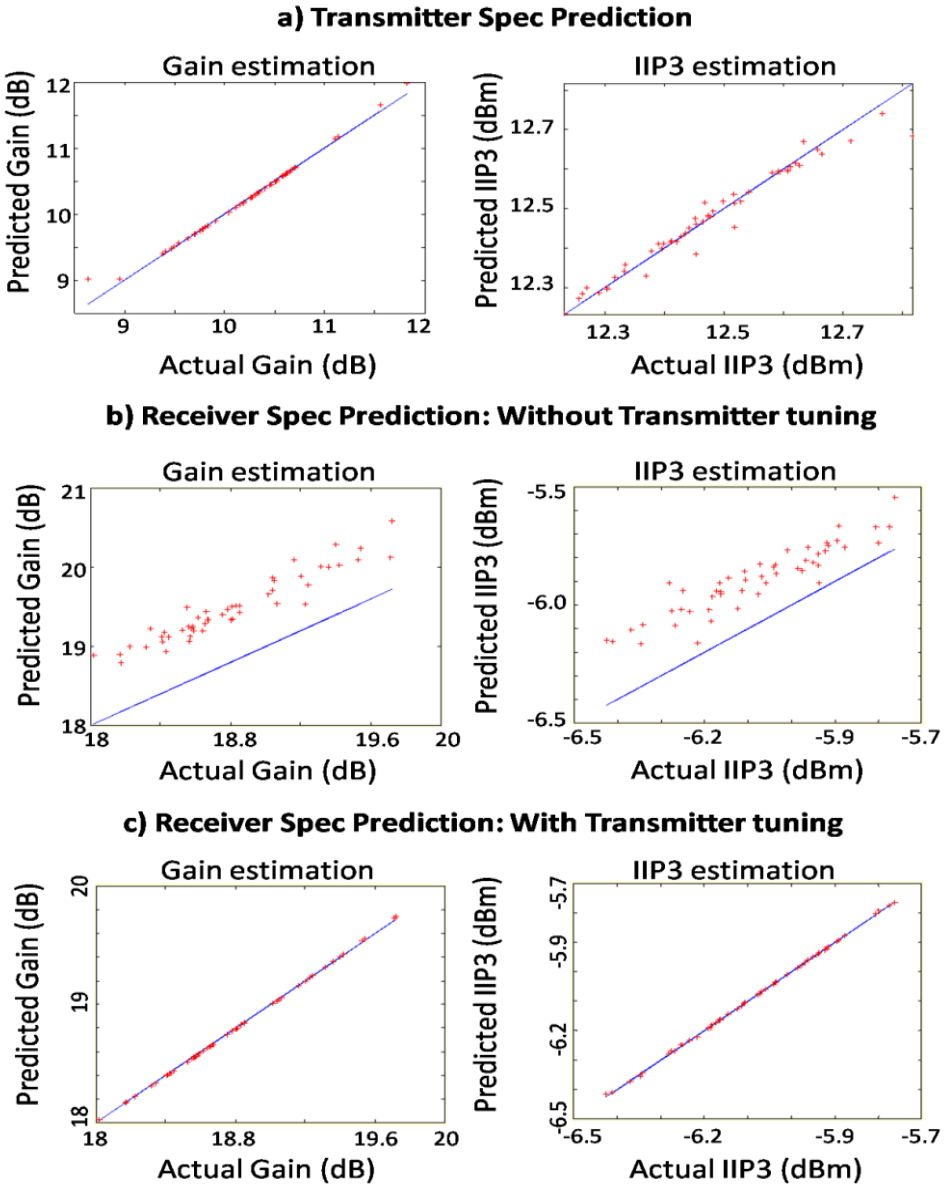


Figure 125: Estimation plots for system specifications

The distortion information obtained by comparing the observed envelope with the golden envelope is then used, to compute the coefficients of the correction polynomials, to correct the input of the system in such a way that the output of the system is in correspondence to near ideal operation (i.e. after tuning the observed envelope is as close as possible to the golden envelope). The results showcased later in this section are used to demonstrate the validity of the idea of tuning a transmitter by just observing its envelope output. The experiment for the validation of ACT enabled loopback approach was performed on a set of 200 instances of the transceivers. Among them, a set of 150 instances were used to develop the regression model between the specifications and the measurement responses. 50 instances were then used for validation purposes. Figure 125a. shows the prediction of the transmitter gain and IIP3 for 50 instances of the DUT. Figure 125b. shows the estimation of receiver specifications without tuning the transmitter (conventional loopback approach). Figure 125c. shows the receiver spec prediction for ACT based loopback approach. The process parameter sensed in step a) and c) would now be used for performing process tolerant VIZOR operation.

6.3. Low Power Adaptation under Process Variation

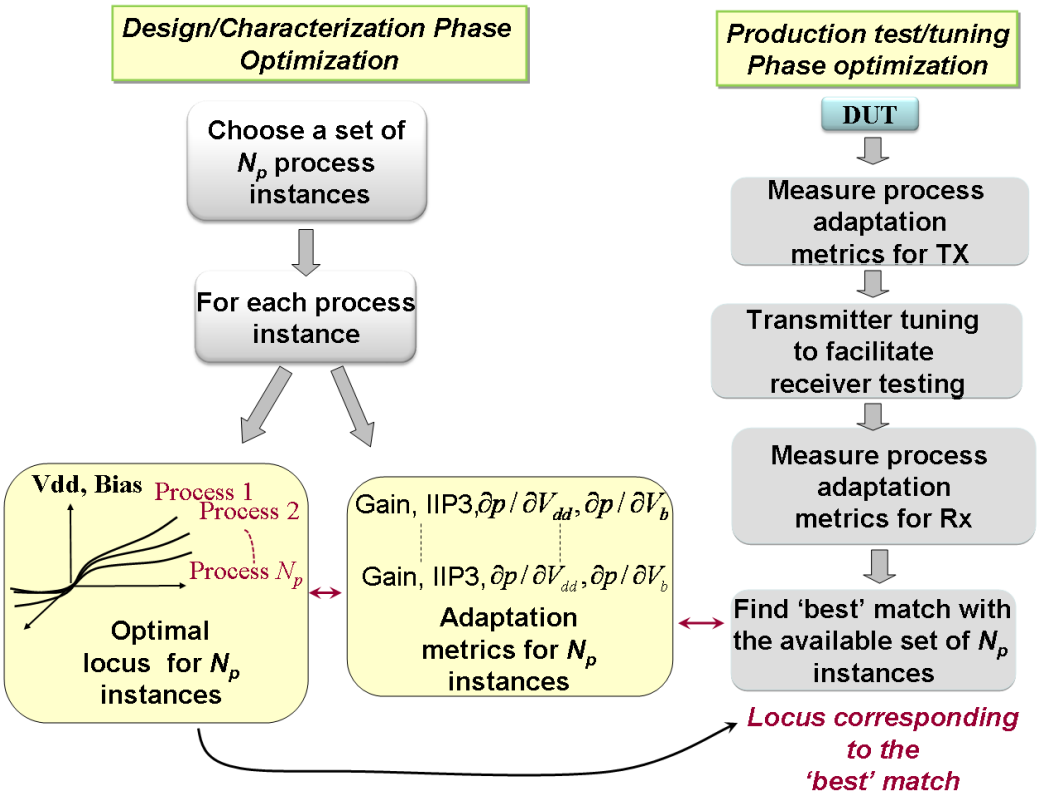


Figure 126: Process sensing and estimation of optimal locus for minimum power operation of the DUT under process variation

An illustration of process tuning procedure is given in Figure 126. Process estimation using alternate test and tuning is performed during the production test phase. Figure 126 shows the process estimation and tuning flow was for a transceiver. The power optimal operation of a VIZOR transmitter or receiver depends on a pre-characterized locus as discussed before. Due to process variations in manufactured devices, the optimal locus is different for every device. Therefore, the purpose of process tuning is to identify the 'right' locus for the DUT. The following steps are performed to ensure this. A set of Np process perturbed (nominal distribution) instances that adequately span the entire process space is generated during the design/characterization

phase. For each of these instances, the optimal locus is obtained using the earlier described optimization. Key circuit-level specification values such as gain, IIP3 (third order intercept), phase noise etc., and power sensitivities are measured and stored. Here, the power sensitivity refers to the power gradients w.r.t. changing tuning knob values - $\partial p / \partial V_{dd}, \partial p / \partial V_b$. The above mentioned device characteristics, referred to as the process-adaptation metrics along with the optimal locus constitute completely characterize a device. Moreover, the process-adaptation metrics of each device exhibit a strong correlation with the optimal locus for that device. If the process-adaptation metrics can be accurately measured for a device, the corresponding optimal locus can be estimated using a simple correlation-based mapping function. Here, a simple look-up table (LUT) based approach is used. A LUT consisting of the adaptation metrics along with optimal locus for the Np instances is stored for future reference (product test/tuning phase). During the production test/tuning phase, the process-adaptation metrics are first measured for the transmitter module in the DUT. Once the transmitter metrics are measured, the corresponding 'best' fit locus is obtained by referring to the LUT and comparing the adaptation metrics of the DUT with the available set. Next, the transmitter is tuned to facilitate receiver testing as described earlier. Once this is done, the receiver adaptation metrics are estimated, which are in turn used to estimate the optimal locus for DUT. Thus, the 'best' fit locus can be obtained for each device facilitating minimum power operation during run time.

6.4. Low Power Adaptation under Process Variation

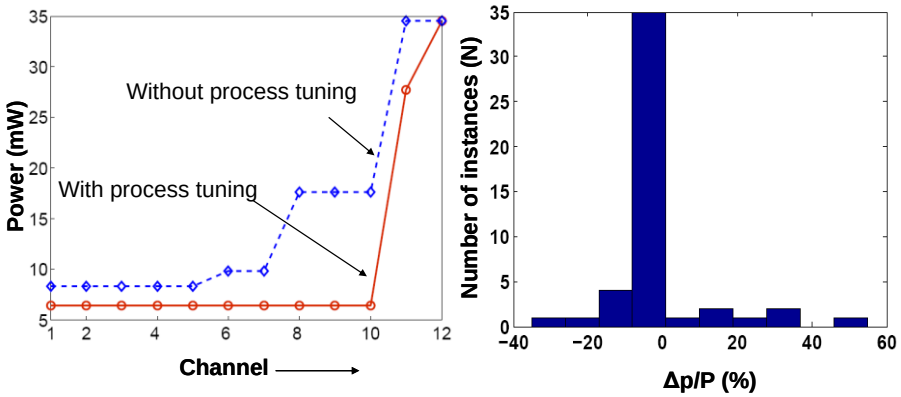


Figure 127: a) Power Savings obtained with process tuning b) Optimality of locus selection: Histogram of *Δp/P in %.*

Figure 127a plots the DC power consumed by a process perturbed instance before and after process tuning. Run time operation of the device was first simulated. For this purpose, the device was adapted for changing channel conditions using a locus obtained for a nominal device. Later the device was tested and the optimal locus is obtained after estimation of process-adaptation metrics. The run time operation was then simulated using the obtained optimal locus. As observed from Figure 127a, when process tuned, the device consumes lesser power for all the 12 different simulated channel conditions. The difference in device DC power consumption (Δp), while operating along the actual and estimated loci are calculated and plotted as an histogram for all the 50 instances in Figure 127b. The Δp's for most of the instances being close to be zero shows the accuracy of process sensing and tuning approach.

6.5. Experimental Validation

6.5.1. System Implementation of Adaptive Receiver

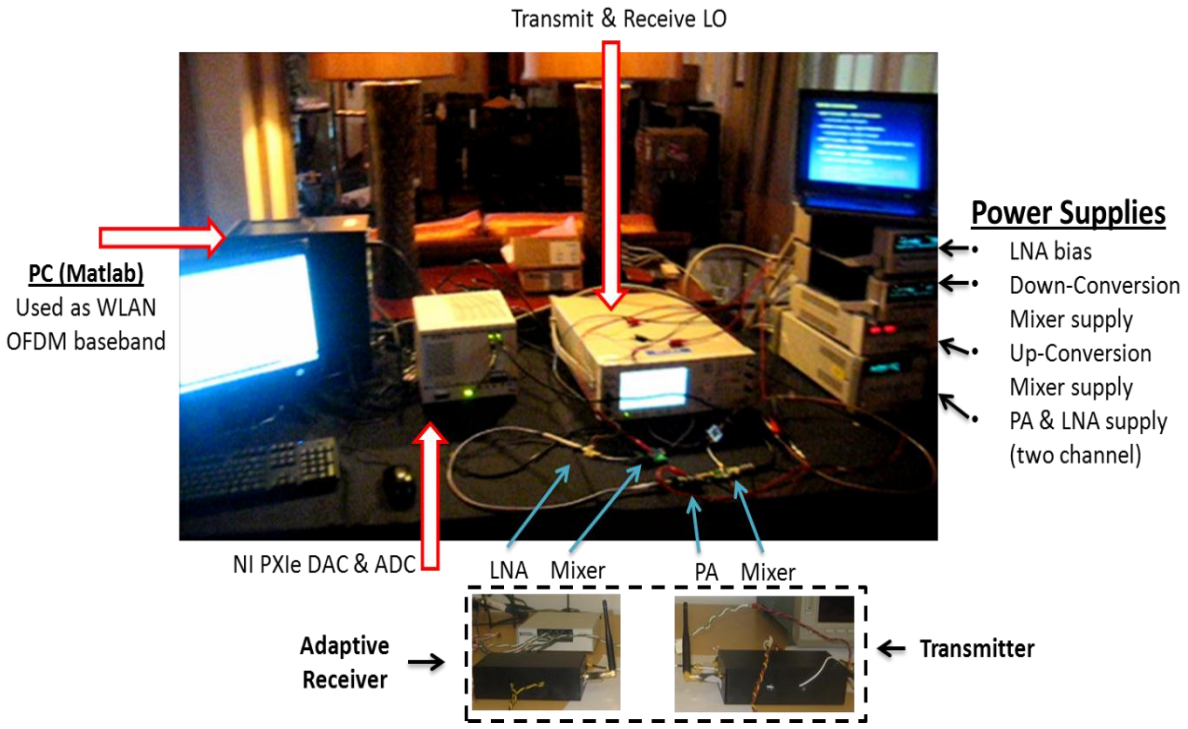


Figure 128: Real-time demonstration hardware setup

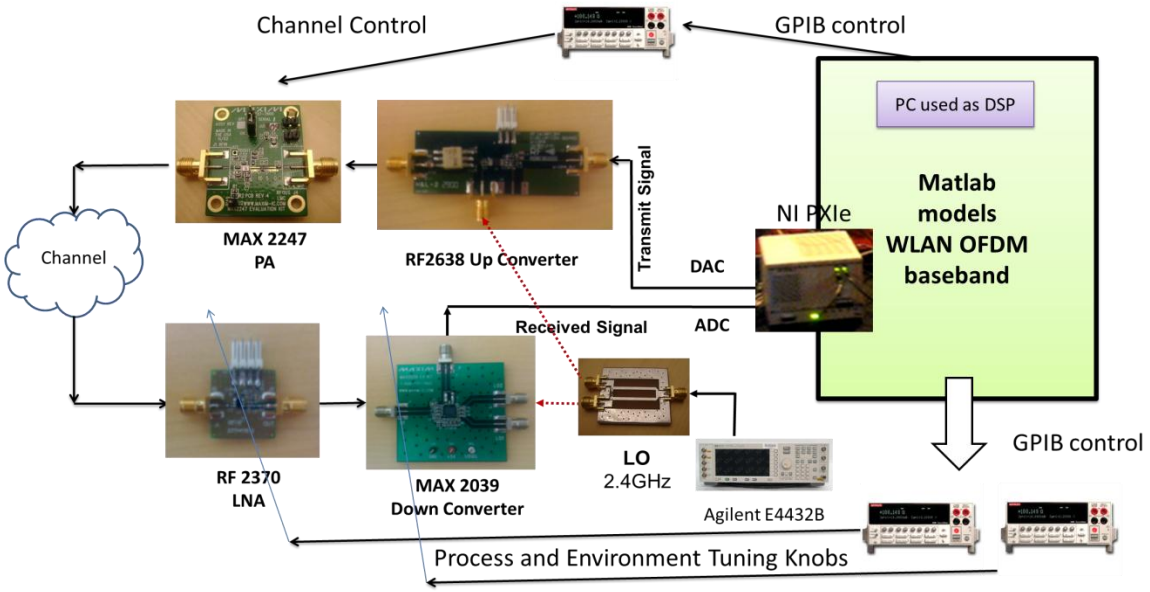


Figure 129: Block diagram of the adaptive receiver within OFDM transceiver

The system implementation for real-time demonstration is described here. The transceiver has the capability to transmit and receive with wireless channels using antennas as shown in the inset of Figure 128. However for creating repeatable channels a set of 4 channels is modeled using attenuation in the PA and noise addition in the baseband. Figure 128 shows the demonstration setup and Figure 129 shows the block diagram of the demonstration of the variation-tolerant low-power adaptive WLAN OFDM transceiver.

The baseband is implemented in the software (MATLAB) in a PC and the DAC and ADC in a National Instruments (NI) PXIe chaise are used for data conversion. The DAQ consists to high speed NI 14 bit Arbitrary Waveform Generator (AWG) NI PXI 5412 operating at 100 MS/s. The ADC is implemented using an 8 bit NI PXI 5114 high speed digitizer operating at 100 MS/s.

The transmitter is implemented using a WLAN upconversion mixer RF2638 operating at 3V and a Power Amplifier (MAX 2247), which is a three stage design for WLAN application providing a Gain of 29 dB. The nominal supply voltage of the power amplifier is 3.3V. For the sake of demonstration of the various channels the supply voltage of the power amplifier is configured to various values. 4 distinct channels were implemented by stepping the supply voltage from 3.3 to 1.8 V. The noise associated with the channels is modeled as an AWGN source in the software (MATLAB). The output of the Power Amplifier is attenuated by 15 dB and fed to a WLAN LNA RF2370. The LNA has an external configurable supply and bias control and is operated in the high gain mode. The nominal values of the supply voltage and bias are 3.0 V respectively. The LNA has a gain of 13 dB and an IIP3 of 7 dBm. The bias voltage of 3 V is used as a

tuning knob for dynamic power savings and is varied in steps of 0.5 V ranging from 3 to 1.1 V. The supply voltage of the LNA is configured to depict process perturbations and is varied in from 3.0 V to 0.6 V.

Table 12 Summary of Process and Environment Adaptive Low Power Receiver Experimental Setup

Parameters	Values/Descriptions
Baseband	WLAN OFDM (Matlab, PC) 20 MHz
Transmitter (freq.)	Mixer, PA (2.4GHz)
Receiver (freq.)	LNA, Mixer (2.4GHz), ADC (NI)
Channel Control Knobs	PA Supply (attenuation) + Noise addition (in baseband)
Process Control Knobs	LNA supply
Tuning knobs for real-time adaptation	LNA bias, Mixer supply
Power (total receiver)	64mW(nominal), 5mW(min)
Power savings	~13x (best case), operates at highest power for worst case channel
Testing	Self-testing and self-tuning system

For the sake of demonstration 2 process perturbations (nominal and varied) with voltages set at either corners is utilized. The down-conversion mixer used is a MAX2309. The mixer is a high linearity passive design with a nominal supply of 5V. The mixer has a gain of -8 dB and an IIP3 of 33 dBm for a LO power of 0 dBm. The supply voltage of

the mixer is used as a tuning knob and is varied from 5 V to 2.6 V. LO signal generator feeds the transmitter and the receiver through a Wilkinson power divider. The 2.4 Ghz 0 dBm LO signal is generated using Agilent E4432B signal generator. The details of the implementation are summarized below in Table 12.

6.5.2. Results: Pro-VIZOR Live Demonstration

A real-time demonstration has been developed as shown in Figure 128. This uses controlled channel conditions and controllable process variation. For any given channel and process, the system always thrives to operate at the minimum power level possible. Figure 130a shows the interface for the real-time adaptive wireless receiver demonstration. The received constellation (QPSK, for this example) is plotted on top left. This shows the current quality of the received signal. The designed adaptive wireless system trades off the received signal quality to save power, i.e., for a good channel the constellation plot starts with a very low spread and keeps on spreading more and more as the system adapts until the point where EVM is close to ET (33% for QPSK). The bottom left figure shows receiver power with possible tuning knobs (LNA bias, mixer supply). It also shows the optimized locus for the given process instance (red line). The system always operates on this locus, going up (increasing power) if channel conditions degrade and vice versa. The figures in the middle plot the current EVM and power consumption with each iteration as the system adapts to lower power points. The adaptation options are shown in top right. The demonstration supports just adaptation for environment (channel adaptation), built-in testing for process variation (process detect) and variation-tolerant environmental adaptation by choosing an optimal locus once the process variation has been detected (process adaptation). The possible controls are shown at the bottom. This

experiment uses 4 controlled channels generated by introducing attenuation (through the transmit PA) and noise addition in the baseband. The receiver process can be varied by controlling the LNA supply. The channel and process can be controlled using the slider menu located at the bottom of the demonstration interface. Finally, the bottom right figure shows the pre calculated response of the receiver (signature) to an optimized test stimulus for both process instances. During process detection, the received response to this test stimulus is matched with either of the stored responses using a LMS algorithm to choose the right process instance. This shows a simplified version of process detection and adaptation described earlier. In real operation any number of process instances can be detected based on an even more complicated test stimulus and intelligent test techniques.

Figure 130, as presented shows the system in operation. The complete curves in middle of Figure 130a (of EVM and power) are obtained for the best channel. For the best channel EVM starts with a low value (power is high) and the system adapts until EVM reaches close to EVM threshold and power consumption is minimized. Power consumption goes from 64mW to 5mW, allowing a 13× savings. The figure also shows the operation of the system for a worse channel (channel id =2) for which the starting EVM itself is pretty high (27%) and hence the power savings possible is lower (it is going down only upto 25 mW).

Figure 130b and c shows the real-time EVM and power for the following conditions, describing how the system behaves under different channel and process. For best good channel and nominal process the system settles at a power of 5mW. For a bad channel nominal process it hovers around a power of 25mW. Now for the same good channel if process is varied (bad) the starting EVM is high (as the received signal quality

is not that good. Without process tuning (blue curve) the system settles at a power of 15mW. If process detection and tuning is applied (i.e. the right locus is selected for the given process) the system settles around 10mW (better than 15mW without variation tolerance). The environment adaptation allows the system to operate at a very low power (compared to 64mW) and the process adaptation makes the environmental adaptation optimal under process variation (15mW to 10mW).

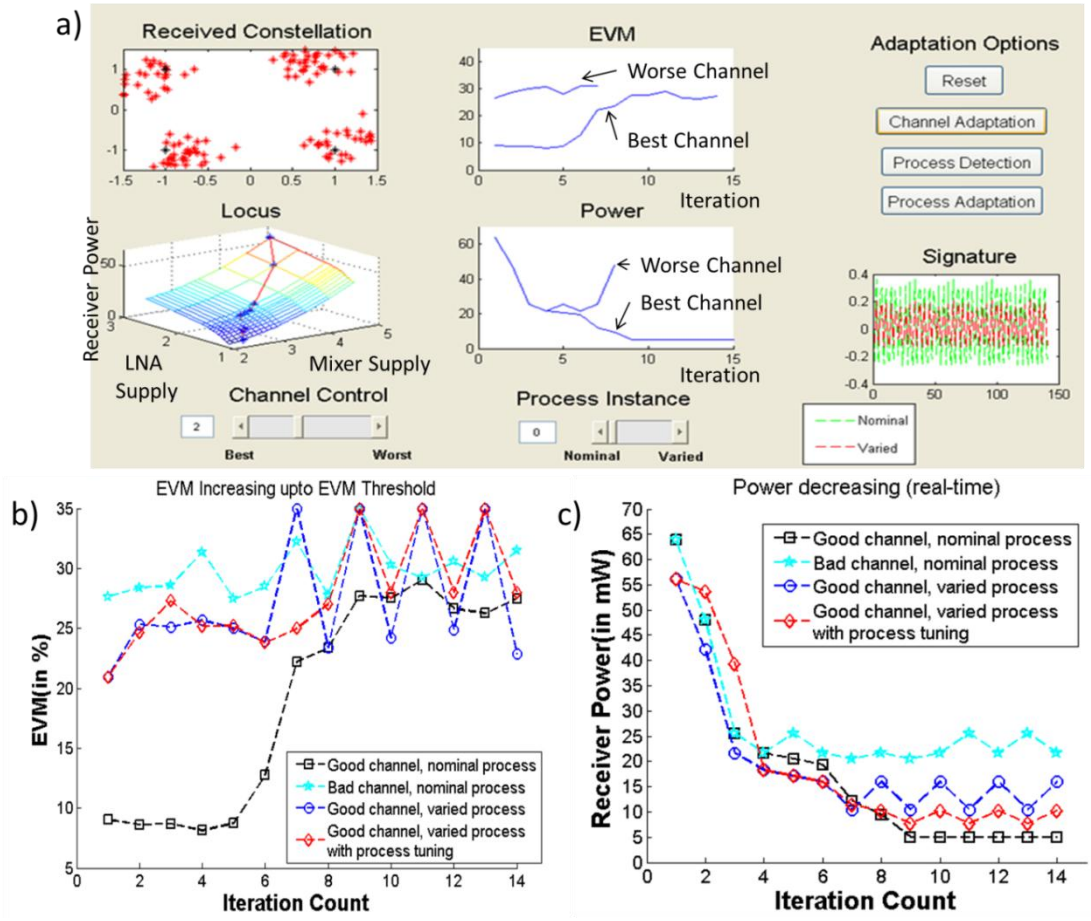


Figure 130: a) demonstration interface b) real-time EVM c) real-time power

In summary, a multi-dimensional adaptation framework for environment and process adaptation of wireless receivers for voltage over-scaled low power operation is demonstrated. An environment adaptation approach operates the receiver of a wireless

device at minimum possible power consumption levels without violating system-level performance metrics: EVM and BER. The adaptation approach aggressively exploits the built-in margins in transmitter and receiver to enable minimum power operation. The variation-tolerant environment adaptation allows about 13x savings in power under best case conditions. In future, this can serve as a key technique for adaptive low power software defined radios/digital assisted radios.

Chapter 7. Conclusions and Future Work

The objective of this research is to investigate the design of Self-Aware Radio Frequency Circuits and Wireless communication Systems that can adapt to environmental and process variations to always operate at minimum power levels possible, extending battery life.

Currently, wireless circuits are designed to meet minimum quality-of-service requirements under worst-case wireless link conditions (interference, noise, multi-path effects), leading to high power consumption when the channel is better than worst-case. In the proposed research work, we develop a multi-dimensional adaptive power management approach that optimally trades-off power vs. performance across temporally changing operating conditions by concurrently tuning control parameters in the RF and digital baseband components of the wireless transmitter and receiver. This adaptation is performed in real-time for low power operation.

Low cost testing methodologies are developed for identification of the health of the wireless circuit/system. These are used in conjunction with tuning algorithms that tune a wireless system under process variation to meet performance specifications and recover yield loss. This testing and adaptation is performed once during the post manufacture test/tune phase to compensate for manufacturing variations. This can also be applied periodically during in field operation of a device to account for performance degradation due to ageing.

Finally, process tolerant environment adaptive systems are designed which includes the following key aspects:

- Design of environment adaptive transmitters and receivers for low power operation by always operating with zero built in design margin.
- Low cost testing and diagnosis of key specifications of wireless transceivers.
- Adaptation to process variation for traditional wireless systems as well as environment (channel) adaptive wireless systems.

The research presented in this thesis on design of process variation tolerant environment adaptive RF systems consists of the following key contributions:

1. A circuit level technique for variation tolerance of RF circuits is demonstrated using an example of a self-healing LNA. The concept of system-level self-healing is introduced and key components are described in Chapter 2.
2. To compensate for process variation, the variation needs to be characterized using low-cost test techniques. Alternate test can provide such a low cost testing for multiple specifications from one measurement. However, its performance is limited with respect to phase distortion measurements. In chapter 3, we develop low-cost phase distortion measurement techniques for high Power Amplifiers using phase distortion to amplitude conversion. We then extend this technique for low-cost IQ gain and phase mismatch measurement in wireless transceivers. Finally, a digital/BIST compatible distortion model extraction driven testing of RF devices is developed.
3. The highest power consuming block in a RF transmitter is a Power Amplifier. A zero margin low power environment adaptation transmitter system is developed in Chapter 4 using concurrent dynamic companding and PA rebiasing, leading to 3x savings in the PA.

4. In a wireless receiver, a multi-dimensional closed loop adaptive power management approach is developed in Chapter 5 for environment adaptive low power zero margin operation. Built-in orthogonal (or independent) tunability of the important specifications allow optimal adaptation. This is demonstrated by designing an orthogonally tunable LNA and using it within a VIZOR receiver. A low power jammer/blocker/interference detector is designed that allows detection of environmental blockers and enables low power/high gain mode of the receiver whenever the operating environment is blocker-free. Finally, a feasibility study of application of VIZOR receivers in MIMO systems shows significant power savings can be achieved when performance is traded off in MIMO VIZOR systems using gain/NF control of the amplifiers.
5. The optimality of the environment adaptation technique described in Chapter 4 and 5 depends on the process corner of the manufactured device. Chapter 6 develops a process sensing and calibration technique that allows process-variation-tolerant virtually zero margin operation (Pro-VIZOR) of the environment adaptive systems.

The goal of the techniques developed in this research is to operate a wireless transceiver in low power and increase process variation tolerance using adaptive circuit/system design techniques. In future, an adaptive digital-assisted radio could possibly incorporate the techniques developed in this research along with other low power and variation tolerance techniques. An example of such an adaptive radio is shown below. Figure 131 uses a wireless video monitoring system as a vehicle to demonstrate different adaptive low power techniques applicable to a wireless transceiver system

developed in this work as well as in conjunction with this work [164]. A camera provides video surveillance whenever required. Adaptive video encoding reduces the data rate by intelligently encoding more information for the region where there is object/activity and encoding significantly less data otherwise. Probabilistic symbol remapping arranges the important symbols in such a way (e.g., in inner constellation points in case of 16-QAM) that the important data suffers from minimum distortions due to the front-end nonlinearity (which increases with the application of the low power modes). Dynamic companding and PA rebiasing saves power in the PA. Pre- and post-distortion techniques increase the power savings range under good channels.

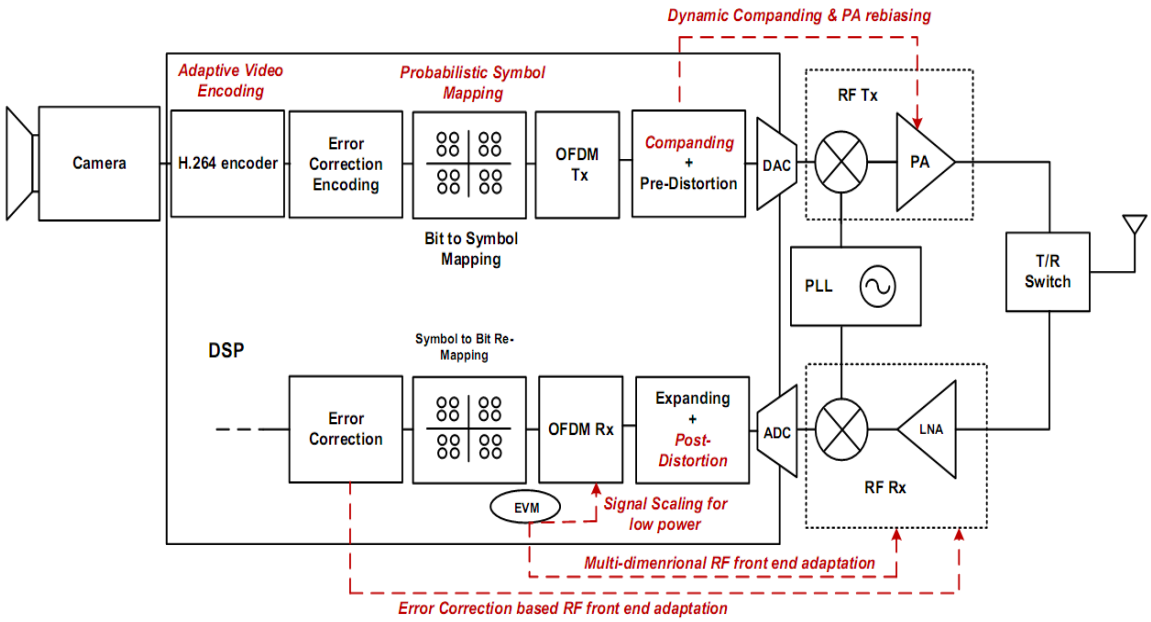


Figure 131: Adaptation of wireless transceiver to workload and variability with the key adaptation mechanisms highlighted [164]

In the wireless receiver, adaptation is performed in different levels to save power. EVM based feedback control is used for the digital OFDM receiver as well as the RF front end. Error correction based adaptation could also provide greater savings in the

receiver. In future adaptive systems, all these techniques are envisioned to be used simultaneously to allow true *zero-margin* operation.

In summary, a process variation tolerant environment adaptive system design framework has been developed. Techniques for process-tolerance are discussed in circuit and system level. New lost cost methodologies for amplitude and phase distortion testing in RF systems are highlighted. Environment adaptive low power transmitter and receiver topologies and the design of tunable circuits that can help such adaptability have been developed as a part of this research. Finally, using the intelligent low cost test information process tolerant environment adaptive systems are designed.

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