SILICON-BASED RF/MM-WAVE POWER AMPLIFIERS AND TRANSMITTERS FOR FUTURE ENERGY-EFFICIENT AND BROADBAND COMMUNICATION SYSTEMS

A Dissertation
Presented to
The Academic Faculty

by

Song Hu

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2017

SILICON-BASED RF/MM-WAVE POWER AMPLIFIERS AND TRANSMITTERS FOR FUTURE ENERGY-EFFICIENT AND BROADBAND COMMUNICATION SYSTEMS

Approved by:

Dr. Hua Wang, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Gee-Kung Chang
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. John D. Cressler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Haomin Zhou
School of Mathematics
Georgia Institute of Technology

Dr. Maysam Ghovanloo
School Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: March 30, 2017

To my family and friends

To the loving memory of my maternal grandfather

ACKNOWLEDGEMENTS

Time flies. It has been fifty-six months since I came to the United States and started the journey of my doctoral study. These fifty-six months turn out to be an important part of my life, which blend the memorable moments of excitement, accomplishments, and anxieties. As Mencius said, what a person can achieve is highly determined by the surrounding people. I could never reach this far without the insightful guidance and generous help from many people during this journey.

First, I'd like to express my sincerest gratitude to my doctoral advisor, Professor Hua Wang. Being a knowledgeable and wise person, Hua not only taught me technical skills and knowledge but also helped me establish and develop passionate, independent, creative yet principled minds in tackling challenges throughout my life. Hua's wisdom, vision, and enthusiasm will have a lifelong and profound influence on my future career. I cannot feel more proud to be your first doctoral student.

I am also very grateful to Professor John D. Cressler, Professor Maysam Ghovanloo, Professor Gee-Kung Chang, and Professor Haomin Zhou for being on my dissertation committee. I appreciate all your valuable feedback, which helped me improve this dissertation.

I feel very fortunate to have worked with world-renowned experts from industry in my field. I appreciate the inspiring technical discussions and meetings with Dr. Shouhei Kousai and Dr. Kohei Onizuka at Toshiba Corporation. I also would like to extend my appreciation to Toshiba for the generous support of silicon chip fabrication.

I feel honored to be a member of Georgia Tech Electronics and Micro-System (GEMS) Lab. From every GEMS member and visiting scholar that I interacted with, including Jong Seok Park, Taiyun Chi, Tso-Wei Li, Fei Wang, Min-Yu Huang, Doohwan Jung, Moez Karim Aziz, Sensen Li, Edgar Garay, Huy Thong Nguyen, Bert Zhu, Choongsoon Kim, Michael Kroger, Juan Pablo Caram, Manoj Aripirala, Stefan Lepkowski, Chi-Hsien Chiu, Mohan Yang, Dr. Jun Luo, and Dr. Venkatesh Ramalingam, I learned a lot, including skills from BBQ to swimming and knowledge from English language to global cultures.

I'd like to thank all the other friends, especially Ming Yi, Yue Zhang, Chao Weng, Kehuang Li, Lingchen Zhu, Jason Chen, and Jialing Tong at Georgia Tech, who helped me during my early time in the United States.

In addition, I'd like to thank Professor Zhiliang Hong at Fudan University, who led me to the world of circuits and always supports me.

I owe my deepest gratitude to my family. My parents give me unconditional love and support at any time. No words in any languages can express my love to you. My dear maternal grandfather, I miss you from the bottom of my heart. I wish I could have been around you when you left us in 2015. I am sure you will be proud of my accomplishments.

Song Hu

Atlanta, GA

Mar. 25, 2017

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

5G	Fifth-generation
ACLR	Adjacent channel leakage ratio
AM	Amplitude modulation
AFG	Arbitrary function generator
AWG	Arbitrary waveform generator
CE	Collector efficiency
CMOS	Complementary metal-oxide semiconductor
CW	Continuous-wave
DCS	Default code set
DPD	Digital predistortion
DAC	Digital to analog converter
DE	Drain efficiency
DLTM	Dynamic load trajectory manipulation
EOC	Efficiency optimum code
EOCS	Efficiency optimum code set
EM	Electromagnetic
EER	Envelope elimination and restoration
ET	Envelope tracking
EVM	Error vector magnitude
FET	Field-effect transistor
FPGA	Field-programmable gate array
ITR	Impedance tuning range

P_{in}	Input power
LOC	Linearity optimum code
LM	Load-modulation
LTE	Long term evolution
LUT	Look-up table
mm-wave	Millimeter-wave
OOB	Out-of-band
OFDM	Orthogonal frequency division multiplexing
PCT	Parallel combining transformer
PE	Passive efficiency
PM	Phase modulation
PAPR	Peak-to-average power ratio
P_{out}	Output power
PA	Power amplifier
PBO	Power back-off
PDF	Probability density function
PVT	Process, voltage, temperature
QoS	Quality of service
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
RF	Radio frequency
P_{sat}	Saturated output power
SCT	Series combining transformer
SoC	System-on-chip
TDDB	Time-dependent dielectric breakdown

WLAN	Wireless local area network
ZVS	Zero voltage switching

SUMMARY

Next-generation wireless networks pose unmet challenges for conventional communication circuits and systems. To satisfy the voracious demand for higher data rates using scarce spectrum resources, modern wireless networks often employ sophisticated modulations such as high-order quadrature amplitude modulation (QAM). They routinely require high-quality communication links. Consequently, energy efficiency is often compromised in conventional solutions. Current solutions also entail extraordinary challenges when extended to future civilian and defense electronics featuring wide bandwidth. My approaches to addressing these challenges fuse state-of-the-art mixed-signal techniques with large-signal radio frequency (RF)/millimeter-wave (mm-wave) and holistically design active circuits with on-chip electromagnetic (EM) structures. My research introduces new circuit topologies and system architectures that eliminate the tradeoffs and the limits of conventional solutions. In addition, my approaches are conducive to system-on-chip (SoC) integration in silicon.

A digital polar Doherty power amplifier (PA) fully integrated in a 65 nm bulk CMOS process is first introduced. The digital Doherty PA architecture optimizes the cooperation of the main and auxiliary amplifiers and achieves superior back-off efficiency enhancement. This digital intensive architecture also allows in-field PA reconfigurability which both provides robust PA operation against antenna mismatches and allows flexible trade-off optimization on PA efficiency and linearity. The active Doherty load modulation and power combining at the PA output are achieved by two transformers in a parallel

configuration, which ensure an ultra-compact PA design and broad bandwidth. Both continuous-wave (CW) and modulation measurement results are demonstrated.

A comprehensive theoretical study on Doherty PAs under antenna impedance mismatch is performed. It is demonstrated for the first time that by varying the relative gain and phase of the main and auxiliary amplifiers, the PA performance degradation caused by the antenna impedance mismatch can be largely compensated. Such compensation effect is studied extensively for different antenna impedance conditions. Four types of Doherty PAs, i.e., three digital Doherty PAs with different degrees of flexibility and the classical analog Doherty PA, are covered in the complete theoretical analysis. To intuitively show the introduced concept, numerical simulation results based on the theoretical analysis are shown. In addition, measurement results on a fully integrated digital Doherty PA in 65nm bulk CMOS are demonstrated to verify the theoretical study.

In order to enhance the PA efficiency enhancement up to the deep power back-off (PBO) region, a broadband mixed-signal CMOS PA with a hybrid Class-G Doherty architecture is introduced. In addition, a mixed-signal linearization technique is introduced to ensure the PA's AM-AM linearity by digital PA operation and suppresses the PA's AM-PM nonlinearity by real-time analog phase compensation. A Doherty PA carrier bandwidth extension technique is also introduced. A proof-of-concept PA fully integrated in a standard 65 nm bulk CMOS process is demonstrated. Its measured CW and modulation performance advances the state-of-the-art CMOS PA PBO efficiency with superior broadband operation.

To further explore the potential of hybrid PAs, a mixed-signal PA architecture with the real-time hybrid operation of Class-G and dynamic load trajectory manipulation (DLTM) is introduced. This hybrid technique brings the following advantages. First, the Class-G operation substantially relaxes the required impedance tuning range of the load-modulation (LM) network, allowing for a compact and low-loss transformer-based LM network that occupies only a single-transformer footprint. Secondly, DLTM enables PA efficiency enhancement in both Class-G supply modes. Furthermore, a new DLTM operation achieves PA efficiency peaking during PBO as well as PA carrier bandwidth extension. Mixed-signal digitally intensive PA operations ensure the PA output accuracy, including both amplitude and phase. A prototype PA is fully integrated in a standard 65nm bulk CMOS process and its CW and modulation measurement results are demonstrated.

In order to address the challenges in mm-wave 5G applications, a 28/37/39GHz multiband linear Doherty power amplifier is demonstrated. A broadband and low-loss transformer-based Doherty output network is introduced to enhance the Doherty PA efficiency and carrier bandwidth. The Doherty operation is further enhanced by a power-dependent Doherty PA uneven-feeding scheme based on a "driver-PA co-design" method. The PA fully integrated in 130nm SiGe delivers output power and linearity performance that meet the requirements of mm-wave 5G massive MIMO systems. Substantial efficiency enhancement is achieved in all three 5G bands, which advances the state of the art.

CHAPTER 1. INTRODUCTION

1.1 Background

The last decade has witnessed an enormous surge of wireless devices. The mobile devices have earnt explosive popularity in human's daily life. Ubiquitous access to the internet with fast data streaming is desired in many existing applications. Moreover, applications supported by the mobile devices is ever increasing. These demand wireless systems with larger communication capacities and higher data rates. However, radio spectrum resources are limited for wireless communications. Radio frequency (RF) bands have already been densely allocated for different commercial and military applications. Therefore, spectrally efficient modulation methods are often deployed in modern wireless communication standards. For example, high-order quadrature amplitude modulation (QAM) and orthogonal frequency division multiplexing (OFDM) are utilized in Long Term Evolution (LTE) and Wireless Local Area Network (WLAN). Meanwhile, sophisticated power control schemes are often leveraged in modern wireless networks to maximize the system capacity. For example, base stations in modern wireless networks often set transmission power levels for the connected handsets. Different users with different wireless path conditions and requested data rates are required to transmit different power so that the overall system capacity is optimized. As a result, the transmitted signals of mobile devices often show large variations in the amplitude of the envelope (Figure 1a). In

other words, they have large peak-to-average power ratios (PAPRs) (Figure 1b). This presents design challenges for power amplifiers (PAs) in mobile devices.

PA is often the most power-hungry building block in a wireless transceiver. Achieving high PA energy efficiency is critical to extend the battery life of a mobile device and ease the thermal management. However, conventional PAs suffer significant efficiency drop in power back-off (PBO) [1], [2]. Classic PA efficiency enhancement techniques often offer very limited efficiency improvement in deep PBO. The average energy efficiency for a conventional PA when amplifying a high-PAPR signal is hence very low (Figure 1b).

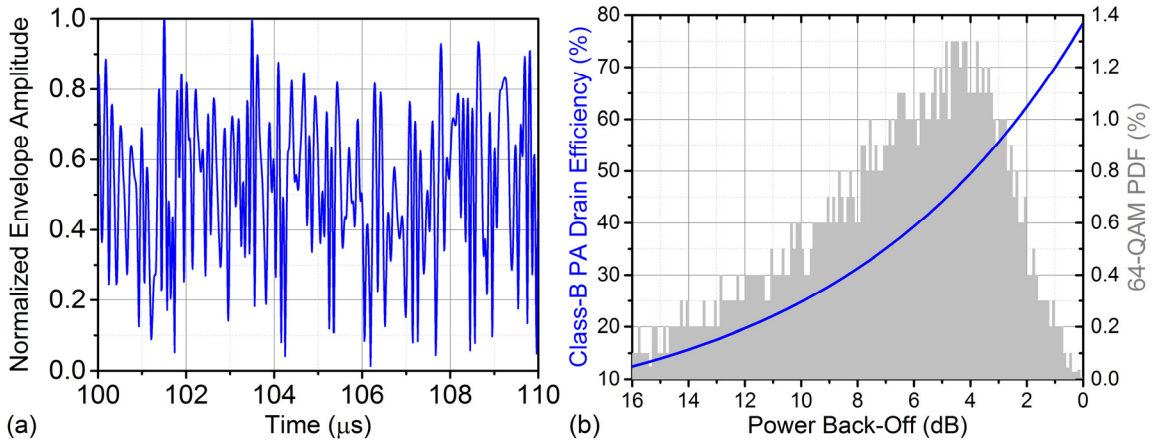


Figure 1 – (a) Normalized envelope amplitude and (b) power probability density function (PDF) for a 10MSym/s 64-QAM signal with PAPR = 5.8dB. The efficiency curve of an ideal Class-B PA is also plotted in (b).

In parallel, it is essential for a PA to amplify the signal with high fidelity to ensure the quality of service (QoS) of a wireless link [1], [2]. This poses stringent requirements when the PA need to amplify a high-PAPR signal, in which case the PA nonlinearity need to be minimized across a wide power range. Both PA amplitude and phase responses,

namely PA amplitude modulation to amplitude modulation (AM-AM) and AM to phase modulation (AM-PM), are often of concern in modern wireless systems.

The object of the introduced research is to achieve high-efficiency high-linearity PA in complementary metal-oxide semiconductor (CMOS) for modern wireless communications. New mixed-signal PA architectures and circuit techniques are introduced to address the design challenges posed by high-PAPR signals. Moreover, the introduced solutions should potentially benefit from the CMOS technology downscaling and be conducive to system-on-chip (SoC) integration.

1.2 Efficiency Enhancement Techniques for CMOS RF PAs

To improve the PA PBO efficiency, multiple PA architectures and circuit techniques have been presented in literatures. They can be grouped into three categories which essentially adjust the dc current, the supply voltage, or the PA load impedance during PBO (Figure 2). The advantages and limitations of each PA PBO efficiency enhancement technique will be discussed in details in this section.

The adaptive-biasing analog PA [3]-[5] and basic digital PA using RF power digital to analog converter (DAC) [6]-[11] reduce the PA dc current during PBO. However, they typically offer limited PBO efficiency improvement. For example, the basic digital PA only achieves Class-B-like PBO efficiency behavior.

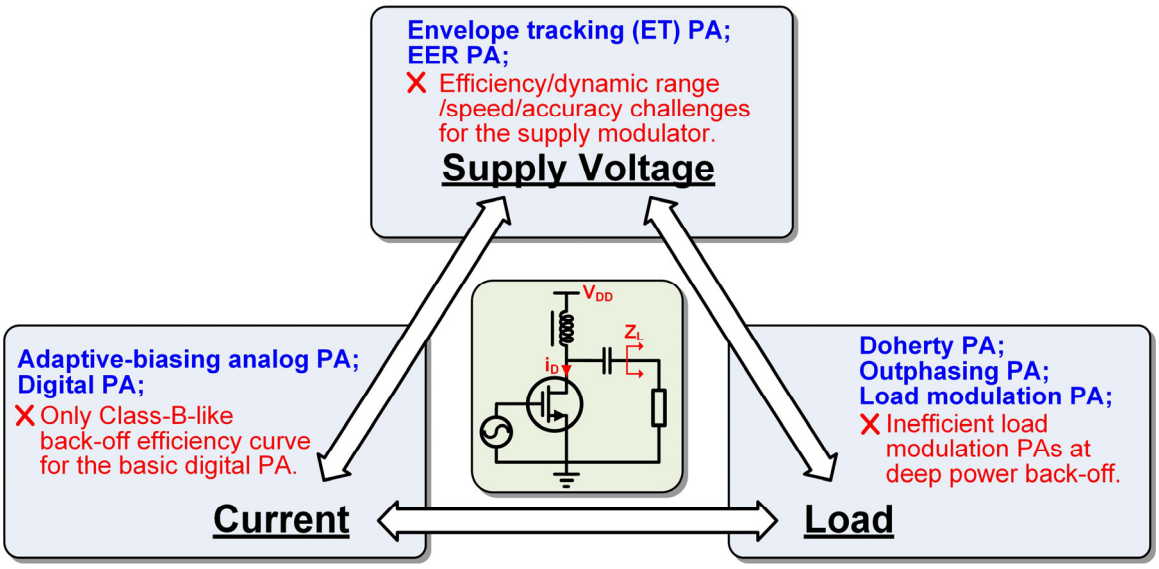


Figure 2 – Summary and categorization of existing PA PBO efficiency enhancement techniques.

Envelope elimination and restoration (EER)/envelope tracking (ET) PAs [3], [12]-[20] save the PA dc power consumption in PBO by dynamic power supply [21]. However, the analog supply modulator often presents stringent design trade-offs among its efficiency, dynamic range, and speed [22]-[24]. This becomes particularly challenging for signals with large PAPRs and high modulation rates. As a compromised solution, the Class-G supply modulation [25] has recently become popular in PA implementations [26]-[28]. Different from analog supply modulators, Class-G supply modulators output discrete supply levels (Figure 3). This alleviates the supply modulator design trade-off and potentially allows high modulation rates. However, the existing Class-G PAs do not offer efficiency improvement within each supply mode (Figure 3). Moreover, significant design overhead is required to address the gain and phase discontinuities during mode switching in the analog Class-G PA [28].

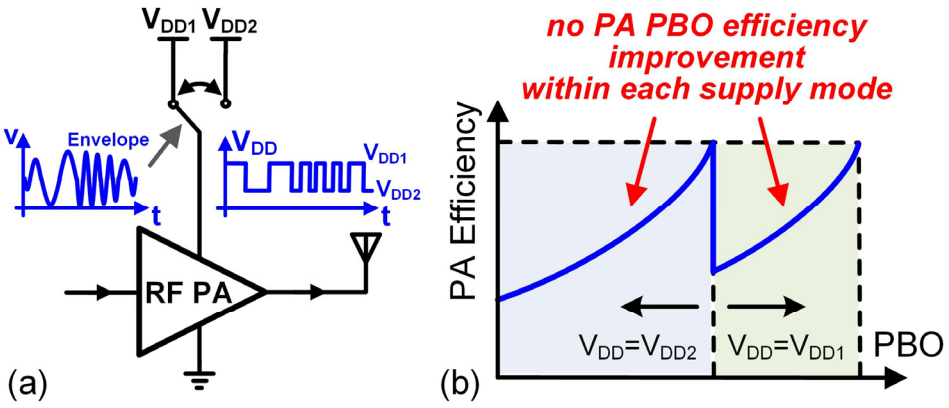


Figure 3 – (a) Schematic of a Class-G PA with a 2-level (1-bit) supply modulator. (b) Theoretical PA efficiency behavior of a 2-level Class-G PA.

Outphasing [29]-[33], Doherty [34]-[53], and load modulation (LM) [54]-[64] PA architectures improve the PA PBO efficiency by modulating the effective PA load impedances in PBO. However, conventional silicon-based outphasing, Doherty, and load-modulation PAs often achieve compromised performance in practice and they offer very limited efficiency enhancement in deep PBO.

An outphasing PA need to generate two constant amplitude signals from the composite signal, which encode the amplitude modulation information as a differential phase shift. This process demands additional computation power in the digital baseband. Moreover, the efficiency of outphasing power combiners often degrades significantly in deep PBO. For an isolating outphasing combiner, e.g., a Wilkinson combiner, power is wasted in the isolation resistor in PBO. A non-isolating outphasing combiner, e.g., a Chireix combiner, is only effective for a small range of the outphasing angle, i.e., a limited PBO range.

The Doherty PA configuration achieve enhanced PBO efficiency by leveraging the active load-pull effect (Figure 4). Compared with EER/ET and outphasing PAs, it potentially supports large modulation bandwidth without costly computation for the input signals. Doherty PAs have been widely employed in base stations. However, several key challenges exist for the CMOS integration of Doherty PAs [39]-[46]. Non-ideal cooperation between the main and auxiliary PA paths, together with large and lossy passive networks, often leads to compromised performance for the conventional analog Doherty CMOS PAs in practice.

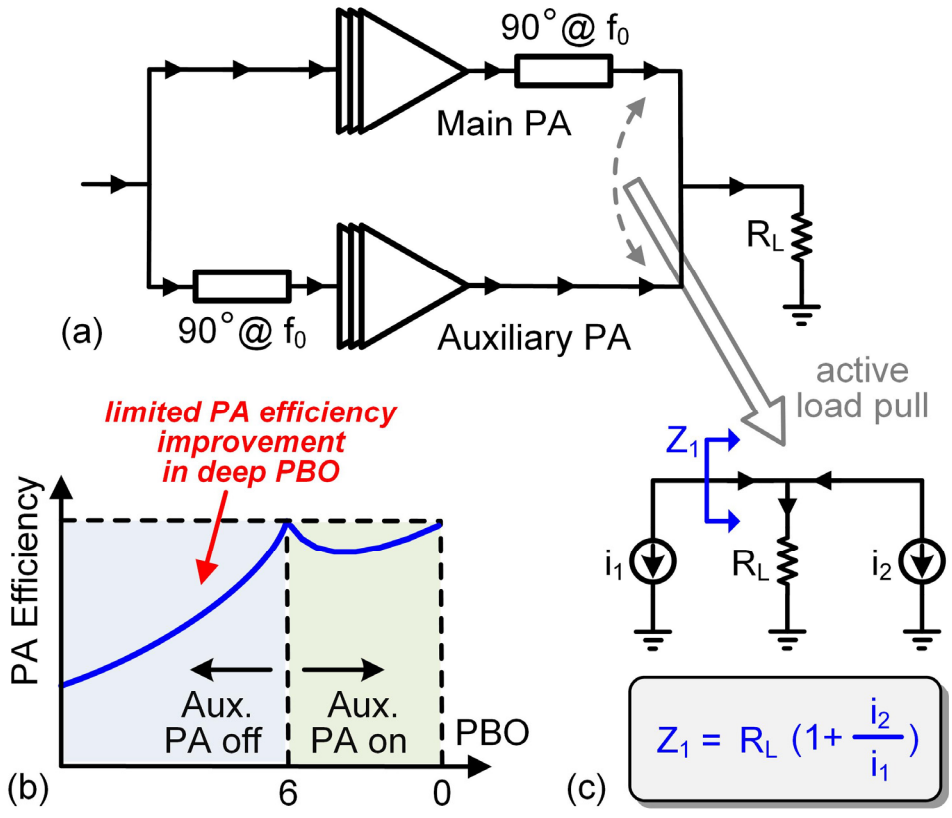


Figure 4 – (a) Schematic of a classic 2-way Doherty PA. (b) Theoretical PA efficiency behavior of a classic symmetric 2-way Doherty PA. (c) Concept of the active LM effect.

The desired Doherty PA operation highly relies on the cooperation between the two PA paths, especially the turning-on point of the auxiliary PA and the relative gain relationship of the two PAs (Figure 4). However, it is challenging to satisfy these in analog Doherty PAs. Conventionally, to mimic Doherty operation, the auxiliary PA is often biased with a smaller conduction angle compared with the main PA. Additional analog techniques, including dynamic biasing [42] and asymmetrical main and auxiliary amplifiers [43] have been reported to enhance the analog Doherty PA performance. However, most techniques rely on dedicated tuning and lack the flexibility for in-field adjustment. Achieving desired cooperation between the two amplification paths remains elusive in practice.

Moreover, a $\lambda/4$ impedance inverter is needed in a Doherty PA to combine the main and the auxiliary PA outputs (Figure 4). Its compact and low-loss realization presents another major challenge for CMOS Doherty PAs. Conventionally, this impedance inverter is often approximated as a C-L-C low-pass π-network. The series inductor can be either a slab [39], [41], [42] or a spiral [40] inductor, which often requires a large area particularly in differential configurations. A series combining transformer (SCT) network has been employed in Doherty PA designs [43]. However, the efficiency of the SCT network intrinsically suffers from the non-zero output impedance of the auxiliary PA when it is turned-off in the low power region. Although switch controlled capacitors [44] or LC tuning networks [45] can be added at the auxiliary PA output to address this issue, these techniques requires additional complexity and chip area and may also degrade the

reliability and passive loss. In addition, a variable balun transformer has been reported in a CMOS Doherty PA [46]. It also requires switch controlled capacitors at the PA output, and only discontinuous LM can be realized.

Furthermore, classic Doherty PAs offer limited efficiency enhancement in deep PBO. For example, marginal efficiency enhancement is achieved for a classic symmetric 2-way Doherty PA when PBO is larger than 6dB (Figure 4). Modified Doherty PA techniques have thus been presented in literatures, including asymmetric [35], [47], [48], multiway [49]-[51], and multistage Doherty PAs [35], [52], [53]. However, these techniques complicate cooperation among the multiple PA paths, require more complex and lossy passive networks, and often lead to extra PA efficiency penalty in practice.

In LM PAs, the PA load is adjusted by a reconfigurable passive network during the PBO to enhance the PA PBO efficiency. Conventional LM PAs face stringent design trade-offs among the passive network complexity/area/loss and effective PBO range [54], especially when efficiency enhancement in deep PBO is required. For example, the L-network (Figure 5a) has a limited impedance tuning range. With one more tuning component, the π-network (Figure 5b) extends the tuning range. However, it has significant loss in practice for large impedance tuning ratios, since it travels through high-Q impedance regions at the intermediate stages of the impedance transformation. This problem is alleviated in the two-stage ladder network (Figure 5c) but at the expense of additional loss and larger footprint. Although the transformer-based schemes (Figure 5d)

could be a compact solution, it also experiences strong trade-off between tuning range and loss. Moreover, dramatic phase variations may present during impedance tuning for these networks, resulting in significant PA AM-PM distortions [63].

In summary, employing an individual PA efficiency enhancement technique often results in limited PA efficiency enhancements when deep PBO is needed.

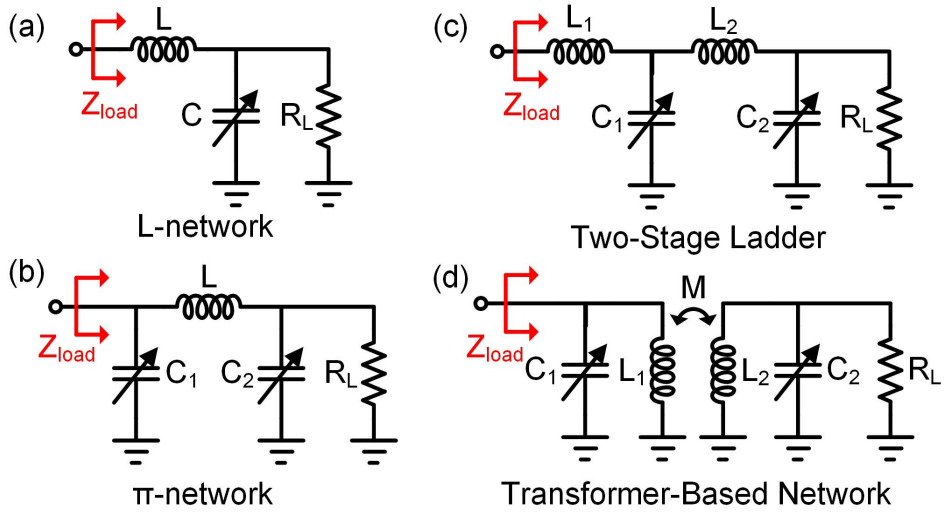


Figure 5 – Existing PA load tuning networks.

Multiple PA efficiency enhancement techniques can be combined in one PA design to achieve hybrid operation. For example, the supplies of the outphasing and Doherty PAs are controlled by the analog supply modulators in [65]-[67]. The dc current or supply voltage is reduced in discrete steps for the outphasing PAs in [68] and [69]. Switch-based PA LM is combined with active load-pull based Doherty operation in [70]. However, these techniques increase the complexity but still demonstrate limited efficiency improvement in deep PBO.

1.3 Linearization Techniques for CMOS RF PAs

Intensive research has been performed in the field of PA linearization [1], [2]. Techniques both in the system architecture and transistor levels have been presented. In general, the existing PA linearization techniques can be grouped into two types, i.e., linearizing the PA by making corrections at the PA input or output.

Both predistortion and feedback techniques linearize the PA by making suitable adjustment to the amplitude and phase of the PA input signal. Predistortion can be realized in the analog domain [71] or digital domain [72]. Digital domain predistortion often rely on look-up tables (LUTs). Feedback techniques often use analog loops to compute the input correction in real time. Both Cartesian and polar analog feedback loops have been demonstrated for PA linearization [1], [2].

Feedforward techniques linearize the PA by applying corrective signals at the PA output. For example, an auxiliary signal amplification path with a differently biased transistor can be combined with the main amplification path to cancel distortions [5].

In most cases, digital predistortion can be combined with other linearization techniques to achieve further improvement. Next, major concerns for feedback and feedforward techniques will be discussed.

Feedback techniques are robust to process, voltage, temperature (PVT) and PA load variations. However, most feedback techniques need to generate down-converted

derivatives. Therefore, feedback techniques are generally not considered as favorable solutions in wideband applications. A PA-closed loop technique is introduced recently to overcome the bandwidth issue of conventional feedback linearization techniques [73]. The amplitudes and phases of the PA output and the PA driver input are directly detected at RF and compared to control the gain and phase shift of the PA, respectively. Separate amplitude and phase feedback also helps with the PA stability. However, the effectiveness of the PA-closed loop technique in [73] is limited by the nonlinearity of the linearization circuits in the feedback loop.

Compared with feedback techniques, signal processing for linearization purposes is performed on the RF signal in feedforward techniques. Therefore, feedforward techniques fundamentally can support higher modulation rates. In practice, feedforward techniques require the accurate timing of various paths for optimum linearization. The LUTs also need to be updated when the PVT and PA load conditions change. It should be noted that the time-domain resolution of digital signals gets superior to the voltage resolution of analog signals in deep-submicron CMOS processes [6]. This offers the opportunity to facilitate the signal timing of the feedforward signals. In addition, the overhead for LUT update could be marginal for a SoC in a deep-submicron CMOS process.

CHAPTER 2. A TRANSFORMER-BASED RECONFIGURABLE DIGITAL POLAR DOHERTY PA FULLY INTEGRATED IN BULK CMOS

This chapter presents a digital polar Doherty PA with transformer-based input and output passive networks [74], [75]. The main and auxiliary PAs are implemented as two digitally controlled RF power DACs with switching PAs comprising the unit cells. This architecture enables the reconfiguration of the two PA paths to achieve superior PA PBO efficiency enhancement, robust Doherty operation against load variations, and flexible efficiency and linearity optimization. Ultra-compact form-factor and broadband operation are ensured by the transformer input and output networks. Section 2.1 presents the introduced digital polar Doherty PA. The passive network designs are shown in Section 2.2. The measurement results are demonstrated in Section 2.3.

2.1 Digital Polar Doherty PA Architecture

2.1.1 Digital Polar Doherty Architecture

The introduced digital polar Doherty PA is conceptually shown in Figure 6b. Unlike analog Doherty PAs (Figure 6a), both main and auxiliary PAs are implemented as digitally controlled RF power DACs. As a result, the auxiliary PA turning-on point and the two PAs' gain relationship can be precisely controlled using the digital settings. This leads to a

fundamentally improved Doherty operation and hence enhanced PBO efficiency compared with analog Doherty PAs.

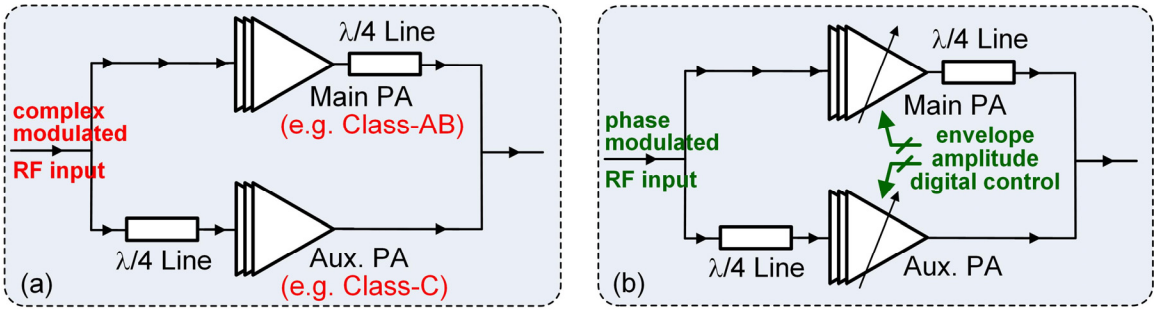


Figure 6 – (a) Conventional analog Doherty PA. (b) Introduced digital polar Doherty PA architecture.

Moreover, the polar operation is embedded in the introduced architecture, which allows the use of switch-mode PAs for high peak efficiency (Figure 6b). The PM RF input is first split into two signals with 90° phase difference. These two RF signals are then separately amplified by the main and auxiliary RF power DACs. The desired AM is first digitized and then mapped to the main and auxiliary RF power DAC control codes.

Therefore, the introduced digital polar Doherty architecture can potentially achieve both high peak efficiency and enhanced PBO efficiency. Furthermore, it is demonstrated in Chapter 3 that the introduced architecture enables reconfigurable Doherty active LM, which can compensate the antenna mismatches and achieve robust Doherty operation resilient to load variations. In addition, measurement results show that such flexibility enabled by the digital control also provides a unique degree of freedom to optimize the PA efficiency with its linearity.

2.1.2 PA Core and Driver Design

The main and auxiliary RF power DACs are each implemented as 5-bit binary-weighted power cells for the proof of concept. All the DAC bits share the same unit power cell for minimum mismatches. 5-bit DACs, which have moderate implementation and measurement overhead, are chosen for quadrature phase shift keying (QPSK) and 16-QAM modulation schemes. The digital Doherty PA architecture can accommodate RF DACs with a larger number of bits and binary/thermometer coding methods.

We adopt the differential inverse Class-D (Class-D^{-1}) PA as the unit power cell for the two RF power DACs (Figure 7), which is compatible with transformer output networks for efficient and broadband power combining [10], [11], [79]. With a parallel LC resonant load, the Class-D^{-1} PA differential output voltage is sinusoidal and satisfies the zero voltage switching (ZVS) condition. The Class-D^{-1} PA core is a pseudo differential cascode amplifier (Figure 7) with thick oxide cascoded devices for enhanced power handling. An optimum device size is determined by the trade-off between the switching PA on-resistance and its output capacitance. Small on-resistance is desired for high PA efficiency, but requires large devices and driving power. Section 2.2 shows that small device output capacitance is preferred to improve the passive efficiency (PE) of the introduced Doherty output network. In addition, larger device output capacitors provide leakage paths for the even order harmonics, which deviates the current waveform from the desired Class-D^{-1} operation, increases the voltage/current waveform overlaps, and thus degrades efficiency.

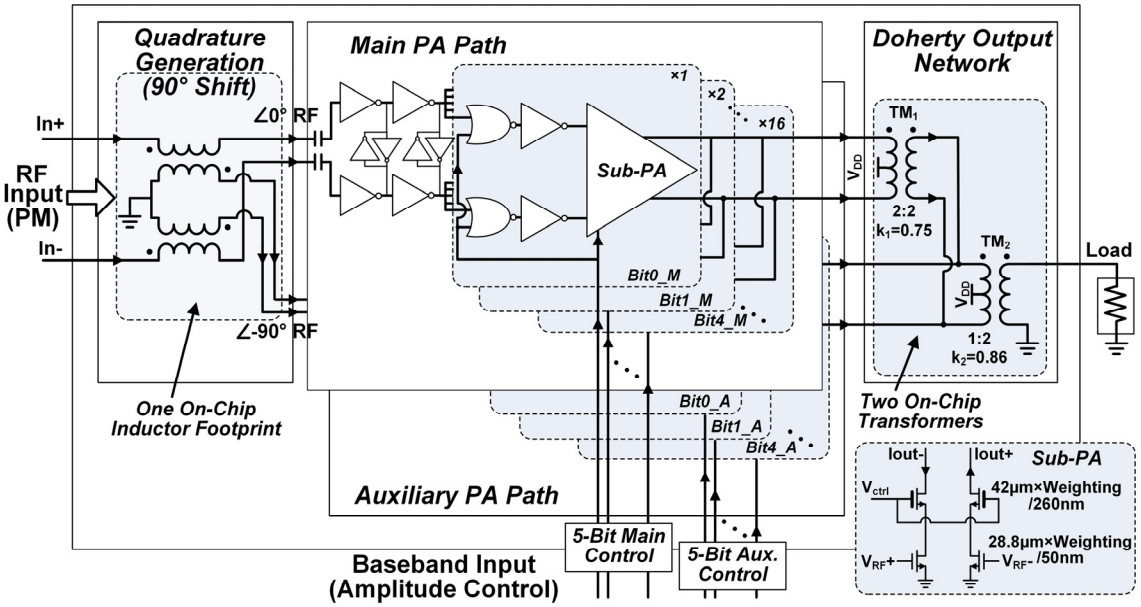


Figure 7 – Schematic of a digital polar Doherty PA.

The PA cores are driven by four-stage digital drivers. Both the PA core and the last two-stage drivers are 5-bit binary weighted (Figure 7). If a sub-PA is off, its last two-stage drivers are also turned off to minimize their impact on the PBO efficiency. Cross-coupled inverters are placed in the driver chain to balance the differential signals and suppress common-mode oscillation [9].

2.2 Passive Network Designs in A Fully Integrated Doherty PA

2.2.1 Doherty Input Passive Network Design

The Doherty input passive network generates two outputs from the RF input with 90° apart and feeds the two PA paths. To perform such quadrature generation, the RC-CR network and its extensions, the polyphase filters, are conventionally used but pose

significant RF loss [40]. Couplers based on coupled slab [39] or spiral inductors can be used instead. However, a large footprint is needed in differential configurations [39], and the required low coupling (k=0.707) raises the loss and narrows the bandwidth [80].

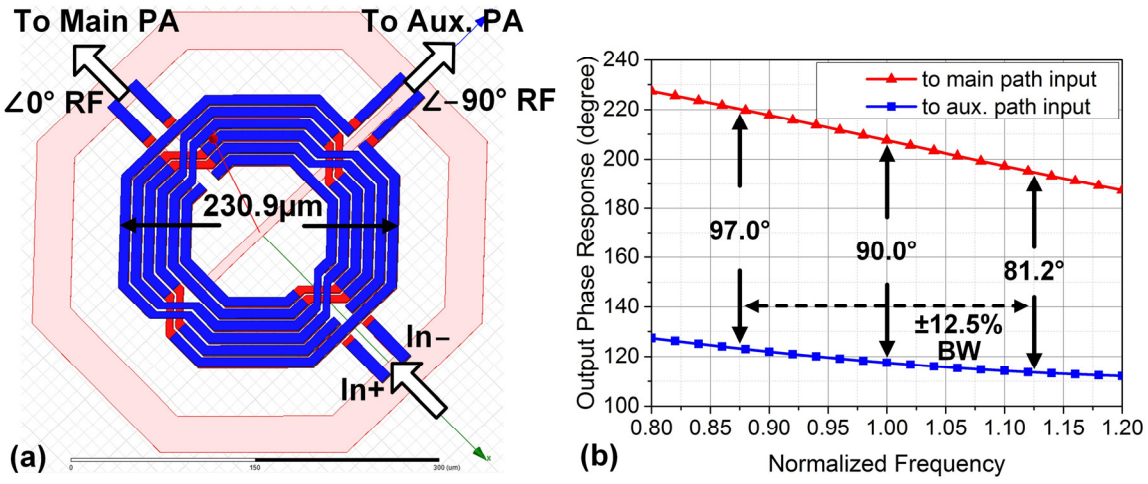


Figure 8 – (a) Six-port folded-transformer-based differential quadrature generation structure. (b) EM simulation results showing the wideband differential quadrature generation.

We adopt a 6-port folded transformer-based differential quadrature generation structure as the input network (Figure 8). It folds two transformers with constructive magnetic coupling to achieve a 6-port fully differential network within only one inductor footprint for significant area reduction (Figure 8a). Unlike conventional transformer couplers, the introduced design favors a larger coupling coefficient, leading to less loss and wider bandwidth. Its 3D EM simulations show 0.7 dB loss at the centre frequency and a maximum 8.8° phase error over 25% bandwidth for the differential quadrature outputs (Figure 8b), ensuring the broadband Doherty PA operation.

2.2.2 Doherty Output Passive Network Design

This section introduces a parallel combining transformer (PCT) based Doherty output passive network (Figure 9). Note that parallel power combining naturally fits the classic Doherty PA operation, which combines the currents from the two PA paths (Figure 6). The design process is explained as follows. As the starting point (Figure 9a), the two PAs are connected through a *C-L-C* π-network as the $\lambda/4$ impedance inverter and their output parasitic capacitors (C_{Dev1} and C_{Dev2}) are tuned out with shunt inductors (L_1 and L_2). The components can be reorganized as in Figure 9b. Next, series inductor L_{Inv} in the π-network and the main PA shunt inductor L_1 are absorbed into a 2:2 transformer TM_1 (Figure 9c). The coupling coefficient of TM_1 is designed to allow its leakage and magnetizing inductors to absorb L_{Inv} and L_1, respectively. Meanwhile, the load R_{Load} is replaced by the 50Ω load and a 1:2 transformer TM_2 for impedance down-scaling (Figure 9c). TM_2 also absorbs the auxiliary PA tuning inductor L_2.

This design thus achieves a fully differential Doherty output network by two transformers (Figure 9d). It provides Doherty active LM, power combining, impedance down-scaling, and differential to single-ended conversion. The transformer TM_1 isolates the dc of the two amplifiers. The TM_1 and TM_2 center taps supply the main and auxiliary PAs, respectively.

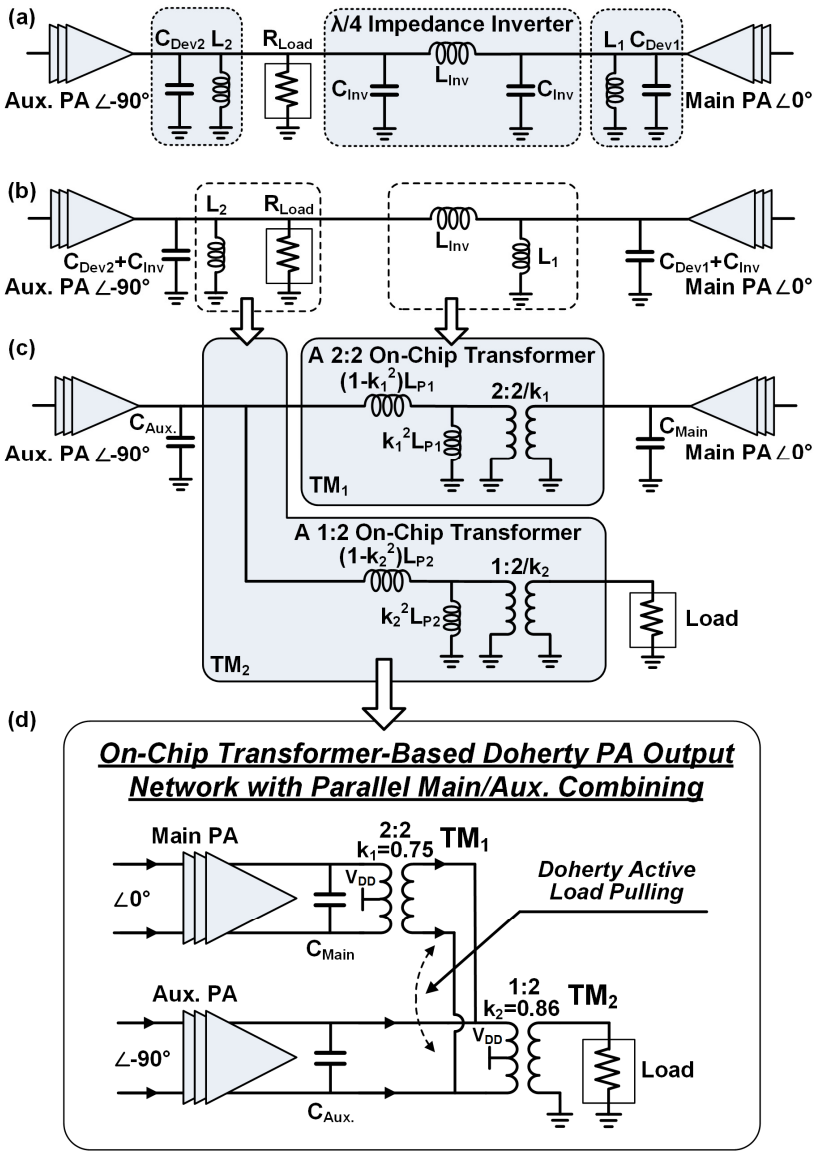


Figure 9 – Introduced parallel-combining-transformer-based Doherty output passive network.

A systematic design and optimization methodology for the PCT based Doherty output network is presented as follows. The main and auxiliary PAs are assumed to be identical. Given the desired output power (P_{out}) and supply voltage, the PA core and the optimum load impedance Z_{opt} can be first-order determined by the large-signal load-pull simulation. The device output capacitance C_{Dev} can thus be estimated, which generally

presents a smaller value in a more advanced process. The optimum PA load R_{opt} at the frequency ω can be calculated by $Z_{opt}(\omega)=R_{opt} // (j/\omega/C_{Dev})$.

In Figure 10, n_1 (n_2), k_1 (k_2), L_{L1} (L_{L2}), and L_{M1} (L_{M2}) are the turn ratio, coupling coefficient, the leakage inductance and magnetizing inductance of the transformer TM_1 (TM_2). TM_2 and the tuning capacitor C_{T2} comprise the impedance down-scaling network. Assume the impedance looking into this network from the primary side of TM_2 is Z_4 (Figure 10). The antenna load R_L should be transformed to $Z_4=R_{opt}/2$ by TM_2 and C_{T2} to meet the required impedance for the desired Doherty operation.

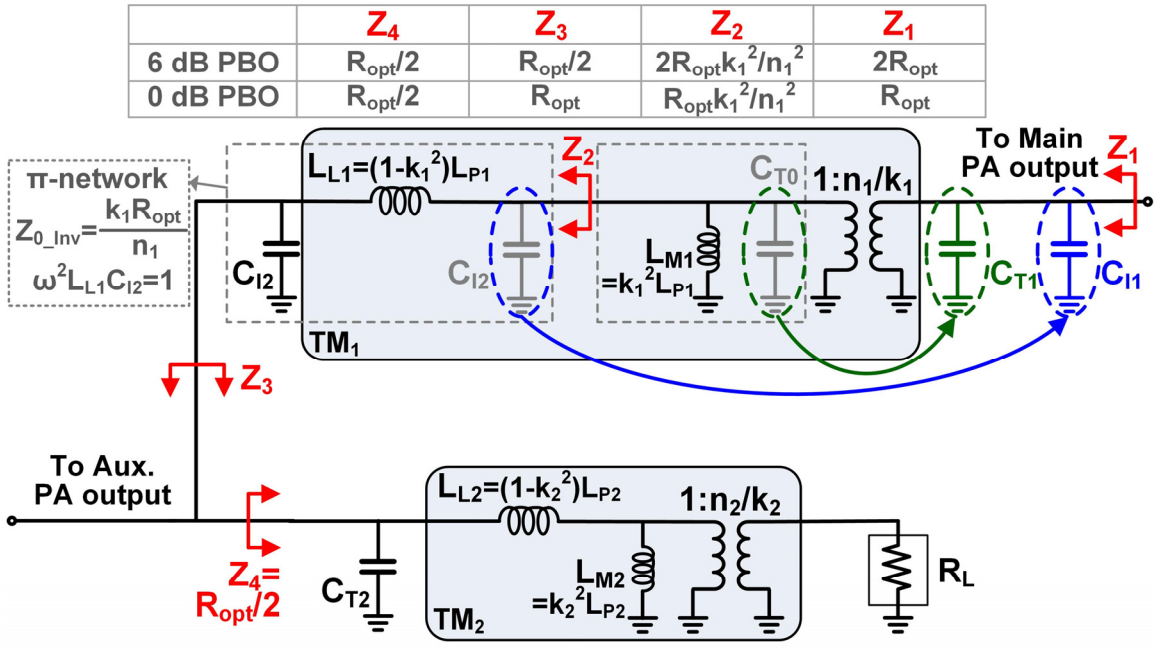


Figure 10 – Design methodology for the introduced PCT-based Doherty output network.

To achieve the desired Doherty operation, the antenna load R_L should be transformed to $R_{opt}/2$. In Figure 10, this is realized by a $1:n_2$ transformer with coupling

coefficient k_2 and a tuning capacitor C_{T2}. The design of this impedance transformation network is discussed first, which can also serve as a general guideline to scale between two real loads by a non-ideal transformer.

Assume the magnetizing and leakage inductance of TM_2 are $k_2^2 L_{P2}$ and $(1-k_2^2)L_{P2}$ and the impedance looking into this impedance down-scaling network from the primary side of TM_2 is Z_4. C_{T2} is designed to null the imaginary part of Z_4 at ω and its capacitance can be calculated as

$$C_{T2} = \frac{R_L^2 + \omega^2 n_2^4 (1-k_2^2) {L_{P2}}^2}{\omega^2 L_{P2} (R_L^2 + \omega^2 n_2^4 (1-k_2^2)^2 {L_{P2}}^2)}. \quad (1)$$

Then, Z_4 in Figure 10 will be a purely real impedance and

$$Z_4 = \frac{\omega^2 n_2^2 (1-k_2^2)^2 {L_{P2}}^2 + R_L^2 / n_2^2}{k_2^2 R_L}. \quad (2)$$

By equating Z_4 with $R_{opt}/2$, one can solve the primary inductance of TM_2 as

$$L_{P2} = \frac{\sqrt{k_2^2 R_L R_{opt} / 2 - R_L^2 / n_2^2}}{\omega n_2 (1-k_2^2)}. \quad (3)$$

Note $C_{T2} > 1/\omega L_{P2}$ and $Z_4 > R_L/(n_2 k_2)^2 > R_L/(n_2/k_2)^2$ are always true for $k_2 \in (0, 1)$ in (1) and (2). The latter result can also be easily observed in the Smith chart interpretation (Figure 11). Therefore, the non-ideal coupling between the two coils in the impedance downscaling transformer not only degrades the efficiency and bandwidth, but also limits

the smallest real impedance which can be presented to the PA. This matches with common design intuitions.

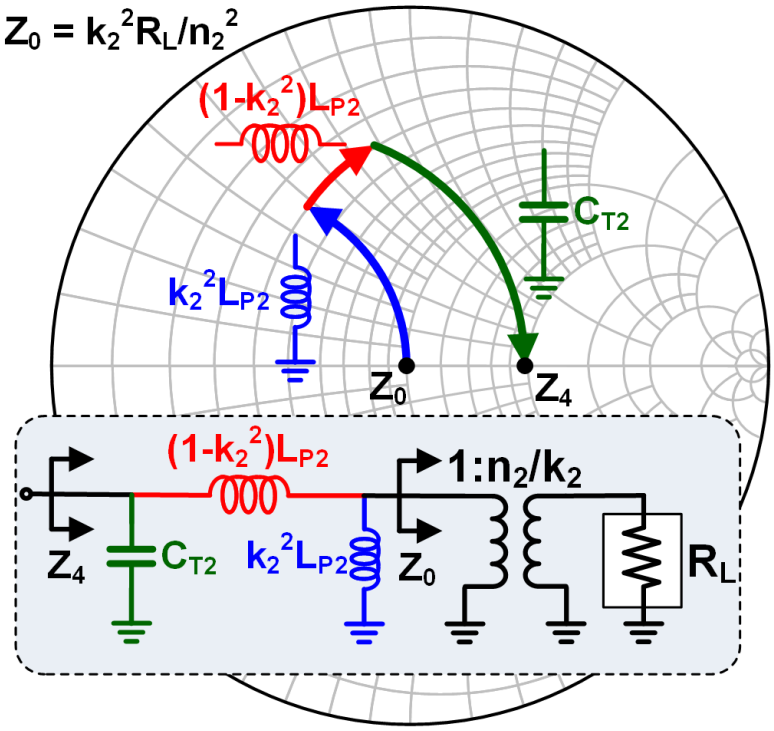


Figure 11 – Explanation on the Smith chart for the effects of the non-ideal magnetic coupling in the impedance down-scaling transformer.

Besides, an impedance down-scaling transformer is more sensitive to the loss of the coil where the down-scaled impedance is presented. It can be shown that in a transformer with a moderate or low loss and a >1 loaded quality factor, the loss at the primary side (with fewer turns) dominates. This also aligns with common design practices.

Therefore, the topology and geometry for the impedance down-scaling transformer need to be properly designed considering the trade-off among the coupling coefficient, quality factors, and parasitic capacitance. In this digital Doherty PA design, the impedance

down-scaling transformer is implemented as a 1:2 transformer with two parallel primary coils sandwiched with the two-turn secondary coil. This topology enhances both the quality factor of the primary coil and the coupling coefficient between the coils.

The transformer TM_1 absorbs the series inductor in the $\lambda/4$ impedance inverter (Figure 10), and its design process is explained here. The TM_1's leakage inductor L_{L1} and the two C_{I2} form the *C-L-C* $\lambda/4$ impedance inverter. Its magnetizing inductor L_{M1} is resonated out by a shunt capacitor C_{T0} at the operating frequency ω. This is then followed by an ideal 1:(n_1/k_1) transformer based on the transformer modeling. Assume Z_1 is the impedance presented to the main PA; Z_2 is the impedance looking into the impedance inverter from its right side; Z_3 is the impedance seen by the impedance inverter from its left side (Figure 10). First, this *C-L-C* $\lambda/4$ impedance inverter together with the 1:(n_1/k_1) transformer should transform $Z_3=R_{opt}$ to $Z_1=R_{opt}$ at 0 dB PBO and $Z_3=R_{opt}/2$ to $Z_1=2R_{opt}$ at 6 dB PBO for the desired Doherty operation. Therefore, the characteristic impedance of this impedance inverter, Z_{0_Inv}, should satisfy

$$Z_{0\_Inv} = \sqrt{L_{L1} / C_{I2}} = \sqrt{(1-k_1^2)L_{P1} / C_{I2}} = k_1 R_{opt} / n_1. \tag{4}$$

At the same time, the $\lambda/4$ impedance inverter requires that

$$\omega^2 L_{L1} C_{I2} = \omega^2 (1-k_1^2) L_{P1} C_{I2} = 1. \tag{5}$$

C_{I2} and L_{P1} can be solved as:

$$C_{I2} = n_1 / (\omega k_1 R_{opt}) \tag{6}$$

and

$$L_{P1} = \frac{R_{opt}}{\omega n_1 (1/k_1 - k_1)}. \tag{7}$$

C_{T0} in Figure 10 is used to tune out the magnetizing inductor of TM_1 at ω, therefore

$$C_{T0} = 1/(\omega^2 k_1^2 L_{P1}). \tag{8}$$

Note that C_{I2} (on the right side of L_{L1}) and C_{T0} should be transformed to the secondary side of TM_1 to absorb the secondary parasitic capacitor of TM_1, C_{TM1_S}, and the main PA's output parasitic capacitor, C_{Dev}, which become C_{I1} and C_{T1} (Figure 10) with the values as:

$$C_{I1} = k_1^2 C_{I2} / n_1^2 = k_1 / (\omega n_1 R_{opt}) \tag{9}$$

and

$$C_{T1} = k_1^2 C_{T0} / n_1^2 = (1 - k_1^2) / (\omega n_1 k_1 R_{opt}). \tag{10}$$

At the main PA output, one may add an extra C_{E1} to complete the capacitance absorption as

$$C_{Dev} + C_{TM1\_S} + C_{E1} = C_{I1} + C_{T1}. \tag{11}$$

Substituting (9) and (10) into (11), one can obtain

$$C_{Dev} + C_{TM1\_S} + C_{E1} = 1/(\omega n_1 k_1 R_{opt}). \quad (12)$$

This is named as the capacitance budget equation at the main PA output. Similarly, at the auxiliary PA output, the capacitance budget equation is written as:

$$C_{Dev} + C_{TM1\_P} + C_{TM2\_P} + C_{E2} = C_{I2} + C_{T2}, \quad (13)$$

where C_{TM1_P} and C_{TM2_P} are the parasitic capacitors of TM_1 and TM_2 at their primary sides, respectively. C_{E2} is the extra tuning capacitor at the auxiliary PA output if needed.

Transformer efficiency η is derived in [85] as:

$$\eta = \frac{R_{TF\_L}/n^2}{\left(\frac{\omega L_P/Q_S + R_{TF\_L}/n^2}{\omega k L_P}\right)\frac{\omega L_P}{Q_P} + \frac{\omega L_P}{Q_S} + \frac{R_{TF\_L}}{n^2}}, \quad (14)$$

where R_{TF_L} is the load impedance for the transformer, which can be either the antenna impedance R_L for TM_2 or the actively modulated impedance Z_3 in parallel with C_{I2} for TM_1; k is the coupling coefficient; Q_P and Q_S are the quality factors for the primary and secondary coils with *1:n* as the primary/secondary turn ratio. From (14), a larger coupling coefficient k improves the transformer efficiency. A larger k is also desired for wide bandwidth operation.

For given R_{opt} and C_{Dev}, a larger k ($0<k<1$) leads to a larger L_{P1} based on (7). Meanwhile, the right side of (12) decreases when k increases. It manifests several design insights. First, to provide a large capacitance budget at the main PA output, the turn ratio

of TM_1 should be small. Hence, TM_1 is designed as a 2:2 transformer (n_1=1). Secondly, to absorb a larger parasitic capacitance by the device and the transformer TM_1, the extra tuning capacitor C_{E1} should be avoided. Thirdly, (12) suggests that a better passive performance can be achieved in a more advanced process. This is because a smaller C_{Dev} relaxes the required capacitance budget and allows a higher coupling coefficient k, which improves the transformer PE.

In addition, (14) reveals another important design aspect that the transformer PE relies on the load impedance. In the desired Doherty operation, due to the active LM, the impedance loading of the transformer TM_1 can vary from $R_{opt}//(1/j/\omega/C_{I2})$ to $(2R_{opt})//(1/j/\omega/C_{I2})$, depending on the power level. This means the PE of TM_1 and thus the overall PE will change with respect to the PA P_{out}. The SCT network also presents a similar characteristic. Note that this is different from single-branch transformer-based PAs, where the PE remains the same for different PA P_{out} levels due to the constant load impedance.

The 3D EM structure of the output network and the simulated effective load impedance for the main and auxiliary PAs are shown in Figure 12 and Figure 13, respectively. The two PA loads both present decreasing real parts in the high-power region, demonstrating the true Doherty active load pulling behavior. Moreover, the imaginary parts in the PCT network are tuned out over the whole power range without any switch controlled capacitor. The efficiency of this network versus the P_{out} is plotted in Figure 14. The power dependent PE is due to two reasons. First, the main PA output experiences more loss than

the auxiliary PA output; therefore, the overall PE increases at a higher P_{out} when the auxiliary PA contributes more power via a passive path with a higher efficiency. Secondly, as previously discussed, TM_1 efficiency inherently varies when the P_{out} backs off and its effective load impedance varies. Simulation shows 70.4% peak PE at 0 dB PBO.

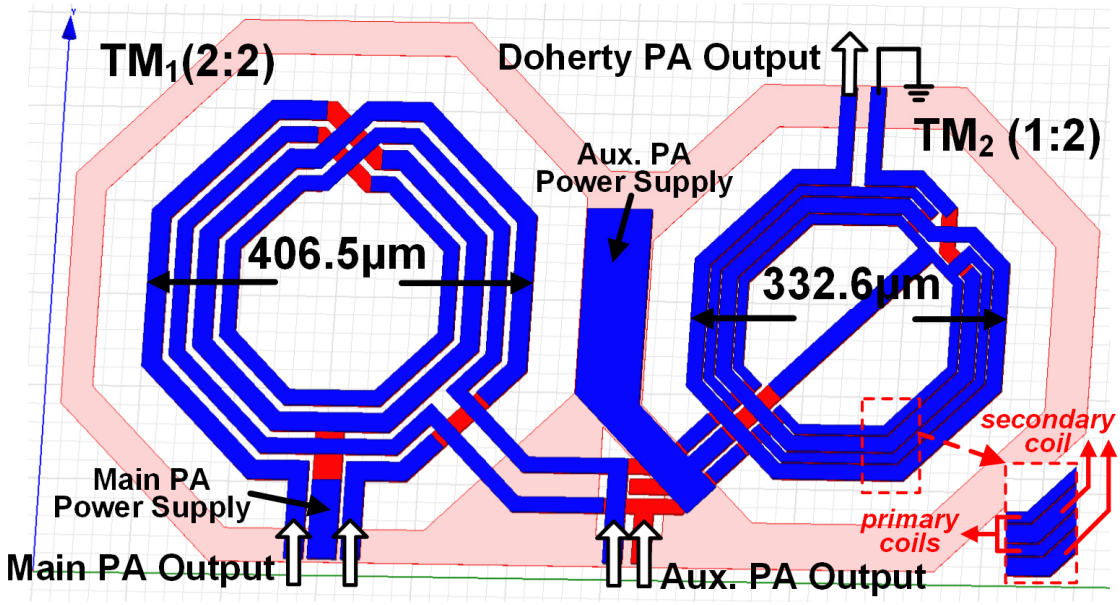


Figure 12 – Implementation of the introduced Doherty output passive network.

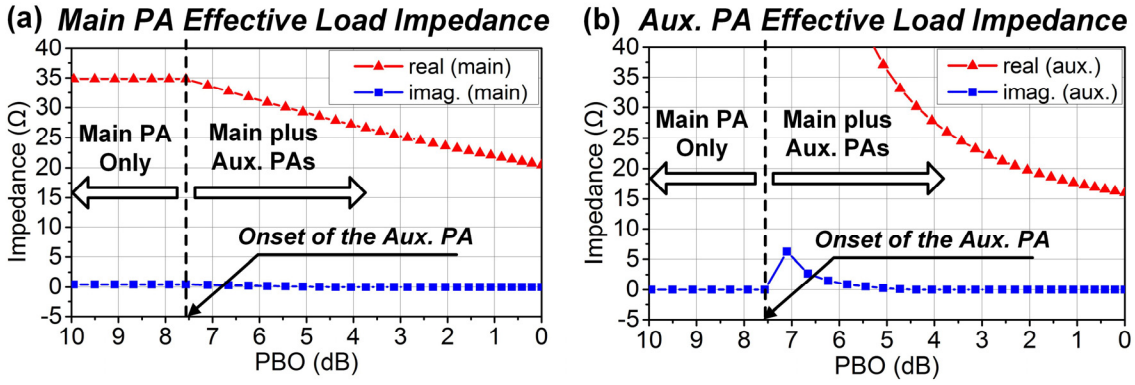


Figure 13 – Effective load impedance for the main and auxiliary PAs based on the EM-simulated Doherty output passive network. Device output parasitic capacitors and constant tuning capacitors are included. The two PA RF currents are assumed to follow ideal Doherty operation.

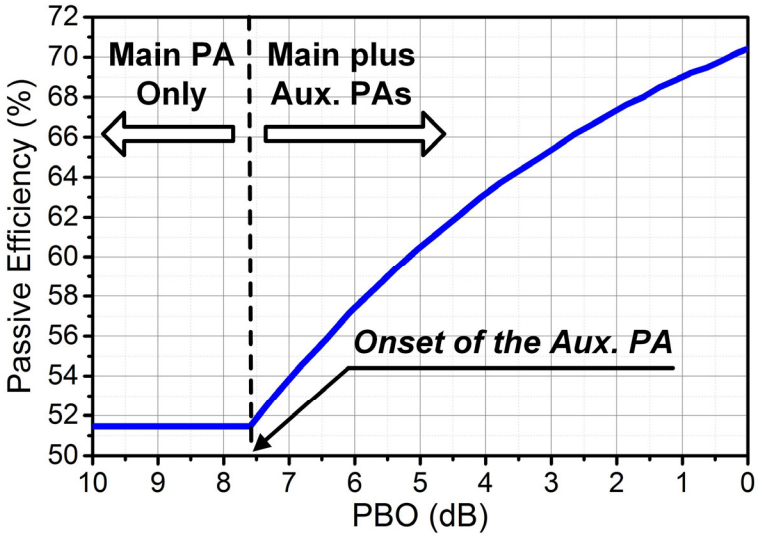


Figure 14 – Simulation results of the PE with the EM-simulated Doherty output passive network.

2.3 Experimental Results

The PA is implemented in a standard 65 nm bulk CMOS process with 1.41×1.48 mm^2 area (Figure 15a). The supply bypass chip capacitors are placed close to the chip in a staircase fashion to reduce the wire-bond inductance and resistance and improve the PA stability and efficiency (Figure 15b). The supplies for the PA cores and the digital drivers are 3 V and 1.2 V, respectively.

2.3.1 Continuous-Wave (CW) Measurement

The PA is first characterized using CW signals with a 50Ω standard load. The peak PA P_{out} and efficiency are shown in Figure 16. The PA achieves its peak power of +27.3 dBm at 3.82 GHz with 16.8 dB power gain. The peak PA DE and PAE are 32.5% and 28.6% at 3.60 GHz, respectively. The −1 dB bandwidth of the PA is 3.10−3.98 GHz. This

24.9% wide bandwidth is mainly due to the broadband input and output passive networks. At 3.82 GHz, the suppressions of second and third harmonics are 38.1 dBc and 54.7 dBc at the peak PA P_{out}.

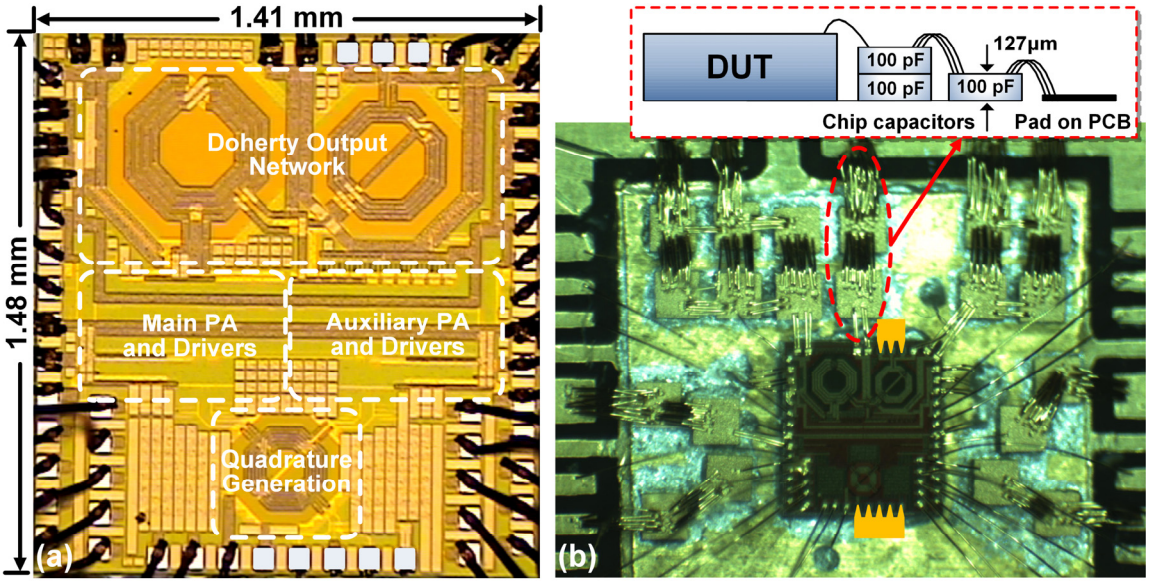


Figure 15 – (a) Chip microphotograph. (b) Chip assembly.

The main/auxiliary PA code combinations are then swept with the 50Ω load, and Figure 17 shows the PA DE versus the PBO level at 3.82 GHz. Different points represent different AM control codes. Code (X, Y) means that there are X and Y unit power cells turned on in the main and auxiliary PAs. For a given PBO level, the optimum code can be chosen to achieve the best efficiency, which is called the efficiency optimum code (EOC). Note that this is a unique reconfigurability advantage of the digital Doherty PA compared with the analog counterparts, since the latter cannot arbitrarily set the gains of the two PAs. The maximum absolute and relative efficiency improvement compared with a Class-B PA

is 7.0% at 5.4 dB PBO (from 16.2% DE to 23.2% DE) and 47.9% at 8.1 dB PBO (from 11.9% DE to 17.6% DE), respectively.

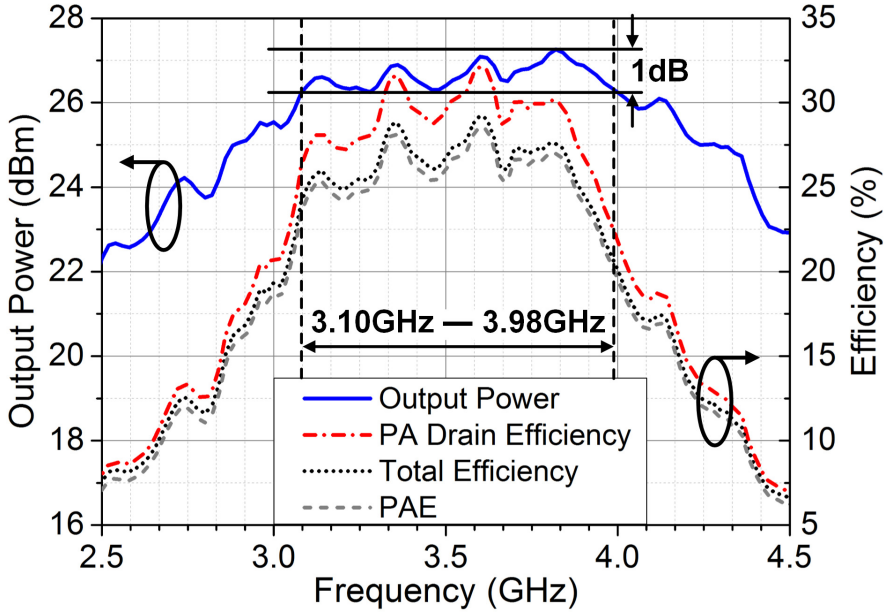


Figure 16 – Measured PA P_{out} and efficiencies.

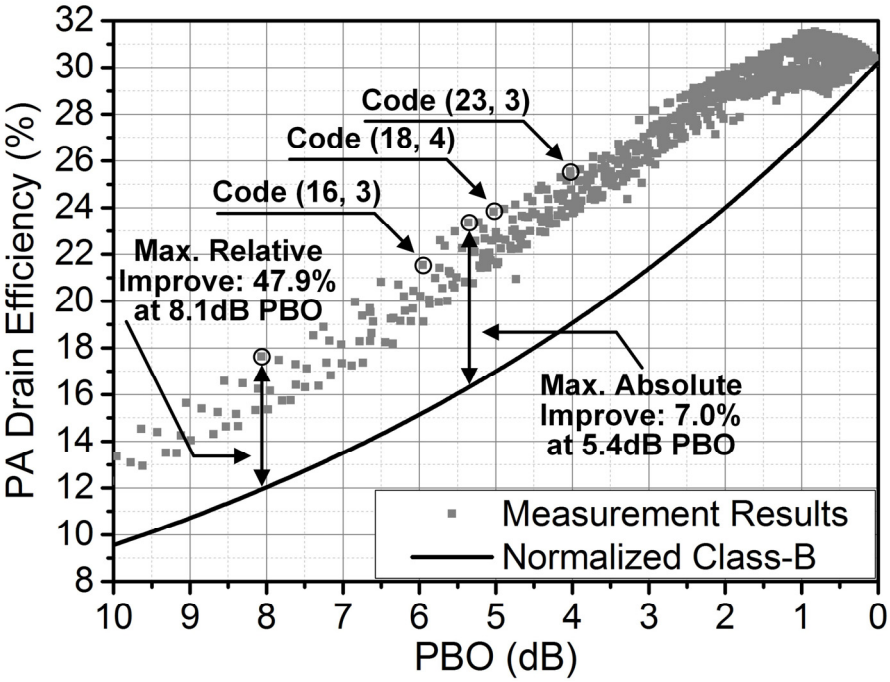


Figure 17 – Measured PA drain efficiency (DE) with the 50Ω standard load.

2.3.2 Modulated Signal Measurement

The PA is then characterized with modulated signals. An RF vector signal generator synthesizes the PM RF input signal, and the AM signals are realized as the 10-bit control signals by an field-programmable gate array (FPGA) board. The AM control codes determine the PA P_{out}, so the appropriate codes can be set dynamically to synthesize the modulated envelope. The full power range is always utilized, and no AM or PM predistortion is applied in the following modulation tests.

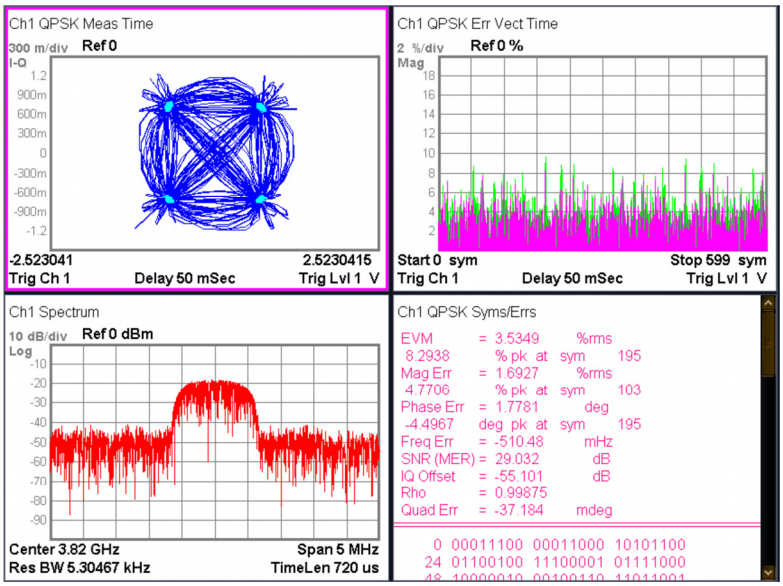


Figure 18 – Modulation test with 1MSym/s QPSK at +23.5dBm average P_{out} and 26.8% PA DE.

Using the EOCs obtained in the static measurement, the PA achieves 3.5% rms error vector magnitude (EVM) (Figure 18) with +23.5 dBm average power and 26.8% PA DE at 3.82 GHz for the QPSK signal (1 MSym/s, 3.7 dB PAPR) with a ×10 oversampling ratio. Compared with a Class-B PA, there is 37.4% relative DE improvement by the

Doherty operation. The suppression of the sampling aliases is consistent with a zero-order hold system. The sampling rate is limited by the test setup.

In the tests with the 16-QAM signal (500 kSym/s, 10 MHz sampling rate, 5.4 dB PAPR), if using the EOCs, the PA achieves 5.6% rms EVM (Figure 19a) with +21.8 dBm average power and 22.1% PA DE at 3.82 GHz. This is 37.8% better than the Class-B operation.

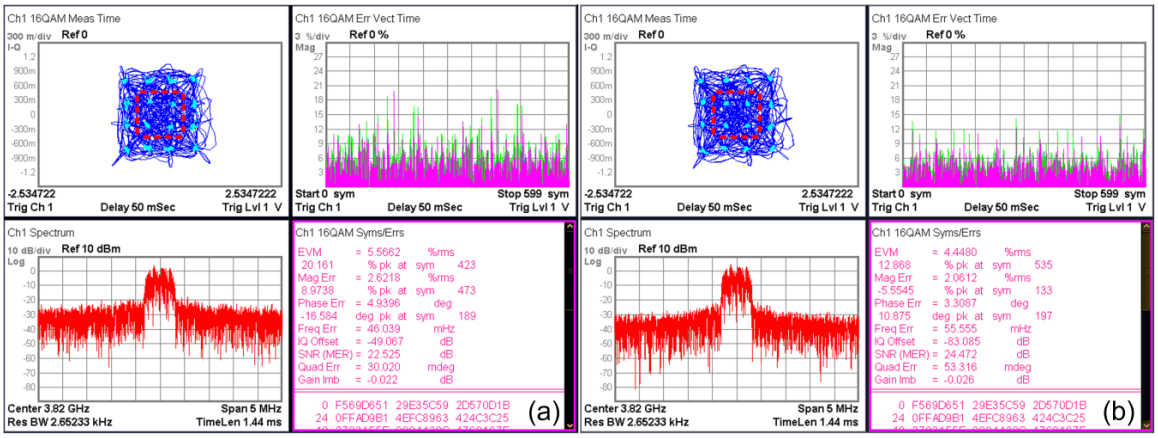


Figure 19 – Modulation tests with 500kSym/s 16QAM when applying (a) efficiency optimum codes, and (b) linearity optimum codes for all the power levels.

However, when using the EOCs for the 16-QAM testing, the undesired rotation of the inner four constellation points is observed (Figure 19a). This is the AM-PM distortion which dominates the EVM degradation, since at each power level, the codes with the highest efficiency (EOCs) may not guarantee the minimum phase distortions (Figure 20a). For a given PA P_{out}, the control code with the least phase distortion measured in the static test is selected (Figure 20a). It is defined as the linearity optimum code (LOC). Using the

LOCs for the whole power range, AM-PM distortion effects are significantly reduced in the measured constellation and the EVM is improved (Figure 19b). The PA achieves 4.4% rms EVM with +22.2dBm average power and 20.2% PA DE. Note that the code selection strategy, i.e., choosing the EOCs or LOCs, offers a new degree of freedom to trade-off between the PA linearity and efficiency (Figure 20). This again manifests the reconfigurability advantage of the digital Doherty PA over the conventional analog counterparts. The achieved average DE by LOCs is 20.3% better than the Class-B operation. In addition, the LOCs improve not only the in-band linearity, evaluated by EVM, but also the out-of-band (OOB) linearity, which is justified by adjacent channel leakage ratio (ACLR) (Figure 21). This is due to the better matched symbol trajectory by the reduced phase distortion.

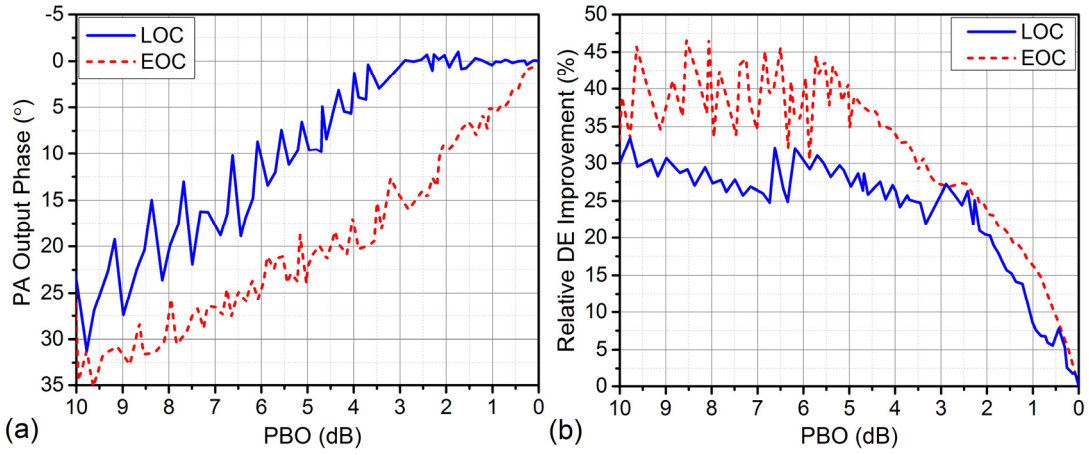


Figure 20 – (a) Measured large signal phase response referred to the value at the peak P_{out} and (b) relative PA DE improvement over Class-B for LOCs and EOCs.

Moreover, leveraging the digital control, one can adopt a hybrid code setting using the EOCs and LOCs for different power levels. Table 1 lists the 16-QAM measurement

results for five cases. The power levels using the LOCs are in column 2. The rest power levels adopt EOCs. The measured spectrum for the case No. 4 is shown in Figure 21. The flexible and reconfigurable digital control offers a unique degree of freedom to optimize linearity together with efficiency. For different applications with different constellations and specifications on in-band/OOB linearity, the digital Doherty PA can be reconfigured to optimize the efficiency. Additional digital predistortions can further improve the PA linearity, but the introduced PA's built-in reconfigurability naturally augments such predistortions and potentially reduces their complexities.

Table 1 – Measurement results with different control code optimization methods

Case No.	PBO levels using LOCs (dB)	Average P_{out} (dBm)	PA DE (%)	EVM (% rms)	ACLR (dB)
1	no	21.8	22.1	5.6	21.8
2	-2~-3 and -9~-10	21.7	21.7	5.7	22.1
3	-1~-4 and -8~-11	21.9	21.1	5.4	23.0
4	0~-5 and -7~-12	22.0	20.6	4.5	25.1
5	all	22.2	20.2	4.4	28.3

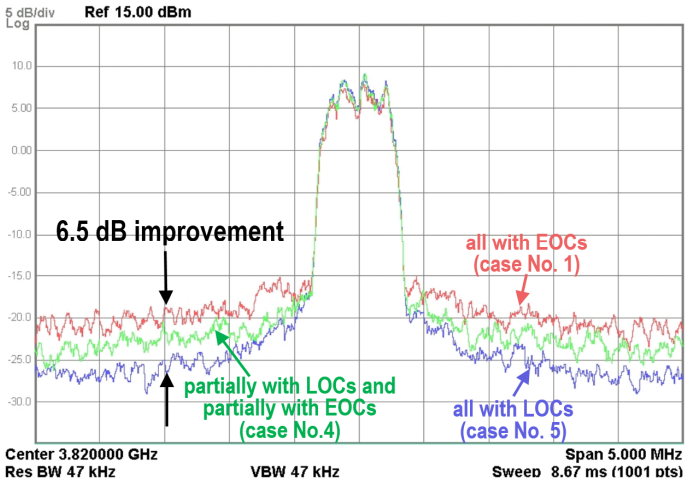


Figure 21 – OOB linearity comparison when applying different code selection strategies. See Table 1 for the configurations in different cases.

Table 2 summaries the measured PA performance. There is no degradation observed over tests with more than 30 hours. Comparisons with other CMOS Doherty PAs and CMOS PAs using other back-off efficiency enhancement techniques are shown in Table 2 and Table 3, respectively.

Table 2 – Performance summary and comparison with other CMOS Doherty PAs

	Freq. (GHz)	Peak P_{out} (dBm)	Peak η (%)	Relative η improvement at 6/5/4dB PBO †† (%)	EVM (%)	Robustness against antenna mismatches †††	Area (mm^2)	Tech. (nm)	Architecture	
This work	3.10-3.98	27.3	32.5 (DE)	42/41/34 (DE)	3.5 (QPSK) 4.4 (16QAM)	Yes	2.1	65	Digital	Transformer-based parallel power combining
W. M. Gaber ESSCIRC '12	2.0	24.8	26 (DE)	100*/37†/28† (DE)	N.A.	N.A.	3.5	90	Digital	Transformer-based series power combining with switched tuning capacitors
M. Elmala JSSC June '06	3.65	28.9	39 (PAE)	-37/-9†/7† (PAE)	4.9 (64QAM)	N.A.	2.7	90	Analog	Slab-inductor-based network
N. Wongkomet JSSC Dec. '06	1.7	31.5	36** (PAE)	33†/28†/19† (PAE)	3.8 (8PSK)	N.A.	9.0	130	Analog	Spiral-inductor-based network with off-chip balun
K. Onizuka VLSIC '12	2.4	30.5	34 (PAE)	33†/29†/24† (PAE)	10 (WLAN)	N.A.	N.A.	65	Analog	Transformer + slab inductor
K. Onizuka ASSCC '12	2.4	30.4	33 (PAE)	36†/32†/29† (PAE)	N.A.	N.A.	3.3	65	Analog	Transformer + slab inductor
E. Kaymaksut JSSC July '12	2.17†-2.75†	26.3	33 (PAE)	52/48†/41† (PAE)	5.6 (WLAN)	N.A.	1.9	90	Analog	Transformer-based series power combining

* achieved by switched tuning capacitors at the aux. PA output. ** excluding the loss of the off-chip balun.

† calculated based on the reported figures. †† compared with Class-B operation.

††† robust PBO efficiency enhancement against antenna mismatches.

Table 3 – Modulation performance comparison with CMOS PAs using other back-off efficiency enhancement techniques

	Technique	Freq. (GHz)	Peak P_{out} (dBm)	Peak η (%)	Average P_{out} (dBm)	Average η (%)	EVM (%)	Relative η improvement †† (%)	Robustness against antenna mismatches †††	Area (mm^2)	PA Supply (V)	Technology (nm)
This work	Doherty	3.82	27.3	30.2 (DE)	21.8 16QAM	22.1 (DE) 16QAM	5.6 16QAM	37.8	Yes	2.1	3	65
K. Oishi JSSC Dec. '12	EER	1.95	N.A.	N.A.	25.6 16QAM	35.3 (PAE) 16QAM	<7 16QAM	N.A.	N.A.	14	3.7	90
D. Kang T-MTT Oct. '13*	ET	1.85	30.2	48 (PAE)	26 16QAM	34.1 (PAE) 16QAM	2.8 16QAM	15.2	N.A.	2.4	4.5	180
H. Xu JSSC May '11	Outphasing	2.4	25.3	35 (PAE)	19.6 64QAM	21.8 (PAE) 64QAM	5.6 64QAM	20.1	N.A.	1.3	2	32
L. Ding JSSC May '15*	Outphasing	0.9	24.4	55† (PAE)	18.4 OFDM	32† (PAE) OFDM	N.A.	16.4	N.A.	1.2	1.7	45

* using an off-chip PA output matching network.

† excluding the loss of the off-chip PA output matching network. †† compared with Class-B operation.

††† robust PBO efficiency enhancement against antenna mismatches.

2.4 Summary

A +27.3 dBm digital polar Doherty PA fully integrated in 65nm bulk CMOS is presented. Digitally intensive architecture results in superior, robust, and flexible Doherty operation. It is suitable for system-on-chip applications, where the digital control can be readily derived from the digital baseband. Broadband and ultra-compact transformer-based passive structures are also presented for fully-integrated Doherty PAs.

CHAPTER 3. ANTENNA IMPEDANCE VARIATION COMPENSATION BY EXPLOITING A DIGITAL DOHERTY PA ARCHITECTURE

This chapter presents a complete theoretical analysis for the digital Doherty PAs under antenna impedance variations [76]. The analysis demonstrates for the first time that by varying the relative gain and phase of the main/auxiliary amplifiers, the PA performance degradation by antenna impedance mismatch can be largely compensated. The theoretical analysis results also offer unique design insights compared with purely numerical simulations. In addition, experimental results on a CMOS digital Doherty PA are presented for verification. Note that the conventional analog Doherty PA is covered by the introduced theoretical model as a case with a fixed gain relationship of the main/auxiliary amplifiers and no phase tuning flexibility.

The chapter is organized as follows. In Section 3.1, the theoretical model of a Doherty PA with both amplitude/phase controls is presented with basic analysis results. The behavior of a Doherty PA under antenna impedance variations is thoroughly discussed in Section 3.2 for different Doherty PA types and antenna impedance conditions. The limitation of the introduced technique is also presented together with design methods as potential solutions. Section 3.3 shows the simulation results. The measurement results of a fully integrated digital Doherty PA in bulk CMOS are demonstrated in Section 3.4. The

measurement results verify the introduced method of using a digital Doherty PA to compensate antenna mismatch.

3.1 Theoretical Modeling and Analysis of Digital Doherty PAs

The conceptual schematic of a general digital Doherty PA is shown in Figure 6b. The RF input signal is split into two signals with 90° phase difference by the input passive network, which are then separately amplified by the main and auxiliary amplifiers. The amplified signals are combined through the output passive network for constructive power combining and Doherty active LM. The amplifier gain tunability can be realized by implementing each amplifier as an RF power DAC, e.g., an array of digitally controlled power cells connected in parallel. The phase tunability of the two amplifier paths can be realized by tunable delays, e.g., varactor loads, in the two amplifier paths.

3.1.1 A Behavioural Model for Doherty PAs

A behavioral model (Figure 22) is introduced to describe the general Doherty PA in Figure 6b. First, two RF current sources are used to represent the RF outputs from the main and auxiliary amplifiers. Phasor representations are used in Figure 22. The RF currents from the two amplifiers are independently weighted by quantities x and y. The main amplifier output leads the auxiliary amplifier by 90° at the operating frequency f_0 due to the phase shift by the Doherty input network. I_0 is the scaling factor for the RF currents. In a symmetric Doherty PA, x and y both range from 0 to 1 during the Doherty operation.

For an asymmetric Doherty PA with a stronger auxiliary amplifier, it has $x \in [0,1]$ and $y \in [0, I_{aux}(\max)/I_0]$ with $I_{aux}(\max)/I_0 \geq 1$. The independent phase tuning of the two amplifier paths is represented by phases α and β in the main and auxiliary amplifier paths respectively (Figure 22). For simplicity, the output parasitic capacitors of the amplifiers are assumed to be tuned out.

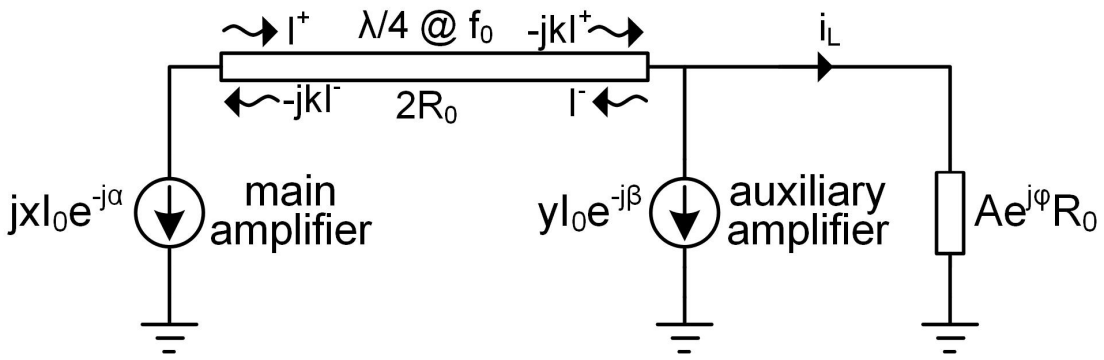


Figure 22 – Introduced Doherty PA model.

The antenna impedance is modeled as $Ae^{j\varphi}R_0$ with $A \in (0, +\infty)$ and $\varphi \in [-90°, +90°]$ to represent any passive non-zero load. The standard load R_0 with $A=1$ and $\varphi=0°$ means no antenna mismatch. The load reflection coefficient Γ is $(Ae^{j\varphi}-1)/(Ae^{j\varphi}+1)$. When the load VSWR, $(1+|\Gamma|)/(1-|\Gamma|)$, varies from 1 to 3, the corresponding values of the load magnitude A and phase φ are plotted with respect to Γ in Figure 23 and Figure 24.

The Doherty output network is modeled as a λ/4 transmission line (characteristic impedance=$2R_0$) to provide the required impedance inversion. Its loss is modeled as a loss factor k for the RF currents ($0<k\leq 1$), with $k=1$ for the lossless case. The following discussions will focus on the PA operation at the operating frequency f_0. The output

harmonics of both amplifiers are assumed to be terminated as "shorted", so the two amplifiers have sinusoidal voltage waveforms at their outputs.

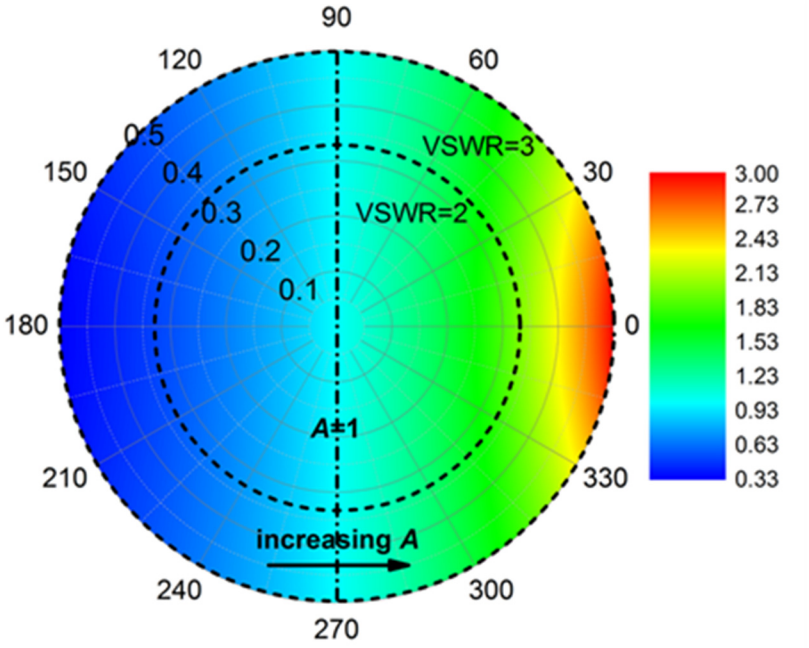


Figure 23 – Values of *A* for the impedance within the VSWR=3:1 circle.

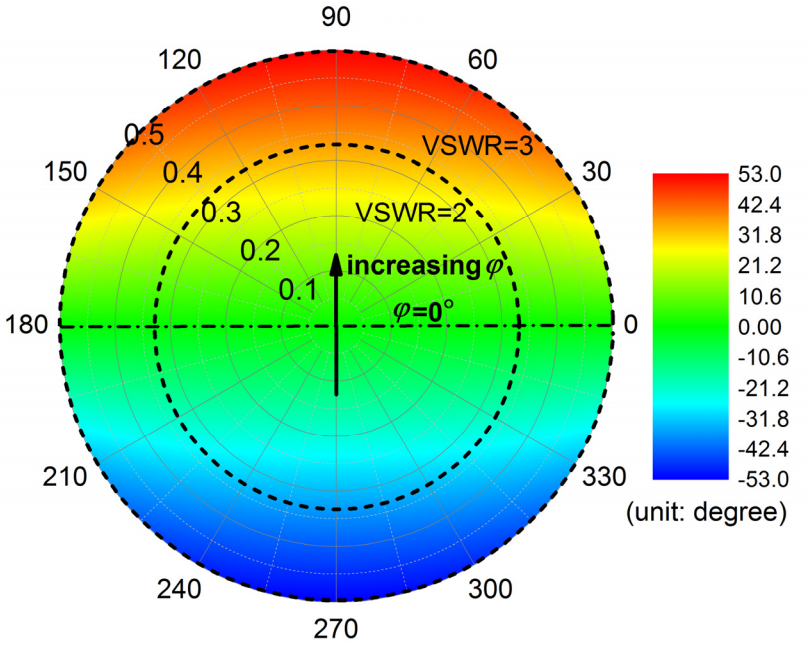


Figure 24 – Values of φ for the impedance within the VSWR=3:1 circle.

Assume a lossless output network (k=1), a symmetric Doherty PA and a matched load (A=1 and φ=0°), at the peak PA P_{out} (x=y=1), the loads observed by both amplifiers are $2R_0$. Assume that this is the optimum load-pull impedance and the two amplifiers have zero knee voltages, the quantities R_0, I_0, and the supply voltage V_{DD} follow

$$V_{DD} = 2I_0R_0, \tag{15}$$

and the maximum RF voltage amplitude at the two amplifier outputs are both V_{DD}. This is true if all the output harmonics are terminated as "shorted". To obtain the dc power and the PA efficiency, the main and auxiliary amplifiers are assumed to work in the Class-B mode without the loss of generality. This matches most RF DACs' operation, as their dc currents are linearly proportional to the RF output currents, determined by the numbers of digital power cells enabled. Thus, the total dc power consumption is

$$P_{dc} = \frac{4}{\pi}(x+y){I_0}^2R_0. \tag{16}$$

Next, the behavior of the digital Doherty PA with a lossy output network, mismatched antenna impedance and arbitrary main/auxiliary amplifier setting is analyzed.

3.1.2 The Doherty PA Model with a Lossy Output Network

At the main amplifier output, the RF currents satisfy

$$-jkI^- - I^+ = jxI_0e^{-j\alpha}, \tag{17}$$

while the RF voltage at the auxiliary amplifier output has

$$(-jkI^{+}+I^{-})2R_0=(-jkI^{+}-I^{-}-yI_0e^{-j\beta})Ae^{j\varphi}R_0. \tag{18}$$

Therefore, I^{+} and I^{-} can be solved based on (17) and (18). And the current flowing through the load can be derived as:

$$i_L=-jkI^{+}-I^{-}-yI_0e^{-j\beta}=-2\frac{2kxe^{-j\alpha}+y(1-k^2)e^{-j\beta}}{2(1-k^2)+A(1+k^2)e^{j\varphi}}I_0. \tag{19}$$

The total RF power delivered to the antenna load is given as:

$$P_{out}=\frac{1}{2}\left|i_L\right|^2\,\mathrm{Re}(Ae^{j\varphi}R_0)=\frac{1}{2}\left|i_L\right|^2\,AR_0\cos\varphi. \tag{20}$$

The total DE of the Doherty PA is

$$\eta=P_{out}/P_{dc}, \tag{21}$$

where P_{out} and P_{dc} are obtained from (20) and (16), respectively. Besides, the RF voltage at the main amplifier output is

$$v_{main}=(I^{+}-jkI^{-})2R_0=\frac{-2j(1+k^2)xe^{-j\alpha}-j(1-k^2)Axe^{j(\varphi-\alpha)}+2jkAye^{j(\varphi-\beta)}}{2(1-k^2)+Ae^{j\varphi}(1+k^2)}V_{DD}, \tag{22}$$

and the output RF voltage at the auxiliary amplifier is given by

$$v_{aux}=i_LAe^{j\varphi}R_0=\frac{-2kxe^{-j\alpha}-y(1-k^2)e^{-j\beta}}{2(1-k^2)+A(1+k^2)e^{j\varphi}}Ae^{j\varphi}V_{DD}. \tag{23}$$

The effective load impedances observed by the main/auxiliary amplifiers thus can be calculated as:

$$Z_{main} = \frac{v_{main}}{-jxI_0 e^{-j\alpha}} \tag{24}$$

and

$$Z_{aux} = \frac{v_{aux}}{-yI_0 e^{-j\beta}}, \tag{25}$$

which account for the active LM between the main/auxiliary amplifiers during the Doherty PA operation.

The equations (19)-(25) provide the close-form expressions for the general Doherty PA with a lossy output network, mismatched antenna load, and arbitrary main/auxiliary amplifier RF current setting (amplitude and phase). The special case of a lossless output network is presented below.

3.1.3 The Doherty PA Model with a Lossless Output Network

The condition of a lossless output network (k=1) simplifies the equations (19)-(25) and offers evident design insights. First, the RF current through the load is

$$i_L = -2\frac{x}{A}e^{-j(\alpha+\varphi)}I_0, \tag{26}$$

while the PA P_{out} and the DE are

$$P_{out} = \frac{1}{2}\left|i_L\right|^2 AR_0 \cos\varphi = 2\frac{x^2}{A} I_0{}^2 R_0 \cos\varphi \tag{27}$$

and

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\pi}{2}\frac{x^2}{A}\frac{\cos\varphi}{x+y}. \tag{28}$$

In parallel, the RF output voltages of the two amplifiers are

$$v_{main} = -j(\frac{2x}{A}e^{-j(\alpha+\varphi)} - ye^{-j\beta})V_{DD} \tag{29}$$

and

$$v_{aux} = -xe^{-j\alpha}V_{DD}. \tag{30}$$

The effective impedance values observed by the main and auxiliary amplifiers are then given as:

$$Z_{main} = \frac{v_{main}}{-jxI_0e^{-j\alpha}} = \frac{2R_0}{x}(\frac{2x}{A}e^{-j\varphi} - ye^{-j(\beta-\alpha)}) \tag{31}$$

and

$$Z_{aux} = \frac{v_{aux}}{-yI_0e^{-j\beta}} = \frac{2xR_0}{y}e^{-j(\alpha-\beta)}. \tag{32}$$

From (27), the maximum PA P_{out} is

$$P_{max} = P_{out}(x=1) = 2{I_0}^2 R_0 \frac{\cos\varphi}{A}. \tag{33}$$

Based on (27) and (33), the PBO can be derived as:

$$10\log_{10}(P_{out}/P_{max}) = 20\log_{10} x. \tag{34}$$

The equations (27)-(34) capture the behavior of both the digital Doherty PA and the conventional analog Doherty PA.

For a symmetric Doherty PA with a matched load, i.e., $x, y \in [0,1]$, $\alpha=\beta=0°$, and $A=1$, $\varphi=0°$, equation (27)-(32) can be further simplified as

$$P_{out} = 2x^2 {I_0}^2 R_0, \tag{35}$$

$$\eta = \frac{\pi}{2}\frac{x^2}{x+y}, \tag{36}$$

$$v_{main} = -j(2x-y)V_{DD}, \tag{37}$$

$$v_{aux} = -xV_{DD}, \tag{38}$$

$$Z_{main} = \frac{2R_0}{x}(2x-y), \tag{39}$$

and

$$Z_{aux} = \frac{2x}{y}R_0. \tag{40}$$

In a classic Doherty PA, the mechanism to achieve improved back-off efficiency is to maintain the main amplifier output RF voltage swing at its maximum value within the

desired PBO range. This requires the main amplifier load to effectively decrease at a higher PA P_{out}, which is achieved by operating the auxiliary amplifier with a deliberate output RF current, called Doherty active LM. Based on (37), this constant output voltage swing constraint at the main amplifier output means that the desired main/auxiliary RF output current relationship should follow

$$y = \begin{cases} 2x-1, & 1/2 < x \le 1 \\ 0, & 0 \le x \le 1/2 \end{cases}. \tag{41}$$

This relationship indicates that when both amplifiers are on, it should have $1/2<x\le 1$. Based on (34), this means that the efficiency peaking due to the Doherty operation happens at 6 dB (x=0.5) PBO for a symmetrical Doherty PA. Moreover, when both amplifiers are on (0 dB≤PBO<6 dB), based on (36), (37), (39), and (41), one can obtain the total PA efficiency as well as the main amplifier output RF voltage and load as:

$$\eta = \frac{\pi}{2}\frac{x^2}{3x-1}, \tag{42}$$

$$v_{main} = -jV_{DD}, \tag{43}$$

and

$$Z_{main} = \frac{2R_0}{x}. \tag{44}$$

Note that the equations (41)-(44) agree well with the known design guidelines of an analog symmetric Doherty PA. In a conventional analog Doherty PA design, the

auxiliary amplifier is often biased in the mode with a smaller conduction angle than the main amplifier to approximate the gain relationship in (41). However, such analog techniques cannot precisely define the turning-on point of the auxiliary amplifier and the gain relationship between the two amplifiers, which often compromises the Doherty performance in practice.

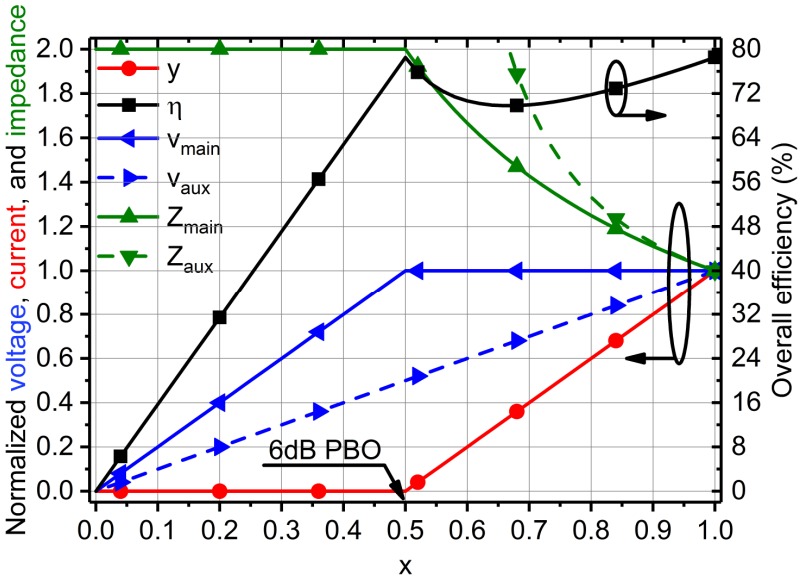


Figure 25 – Simulated performance for a conventional symmetric analog Doherty PA based on the introduced model. The antenna impedance is assumed to have no mismatch.

Based on the introduced model, the simulated operation details of the two amplifiers are plotted with respect to the normalized main amplifier RF output current $x \in [0,1]$ in Figure 25. The plot includes the output RF voltage swings normalized to V_{DD}, effective load impedances normalized to $2R_0$, and the total PA DE. The normalized auxiliary amplifier RF current y is also plotted. These results all agree well with the classic Doherty PA operations, validating the introduced theoretical model.

Based on the results for a Doherty PA with a lossless output network, i.e., the equations (27)-(34), the following two key design insights can be obtained, which however have not been explicitly discussed in previous literature.

1. *The Doherty PA P_{out} quantitatively only depends on the RF current from the main amplifier and the load condition and is independent of the auxiliary amplifier output.* This result is valid only for a lossless output network, and it can be explained intuitively as follows. If the RF current from the auxiliary amplifier increases, it actively modulates the antenna impedance, resulting in an increasing antenna load observed by the main amplifier path. After the impedance inversion by the λ/4 line, the main amplifier actually sees a decreasing load $|Z_{main}|$ and thus delivers a reduced output RF power based on (37) and (39). At the same time, the P_{out} of the auxiliary amplifier increases and it exactly compensates the main amplifier power decrease based on (38) and (40). Therefore, the total PA P_{out} quantitatively only depends on the main amplifier output and the antenna impedance, and is independent of the auxiliary amplifier output.

Note that this result is valid for an arbitrary main/auxiliary amplifier output relationship, which includes but is not limited to the classic analog Doherty PA. It is also valid regardless of whether the Doherty PA is symmetric or not. But it does not hold for a lossy output matching network which attenuates the main amplifier RF output current.

2. *The auxiliary amplifier RF output voltage swing does not exceed the swing at the maximum P_{out} for any antenna impedance and arbitrary main/auxiliary amplifier setting*. Based on (30), this output RF voltage swing is linearly proportional to the main amplifier output RF current for a lossless output network. This holds for any antenna impedance condition as well as any main/auxiliary amplifier RF output current ratio and phase difference.

3.2 Antenna Impedance Variation Compensation and PA Performance Enhancement by Exploiting the Digital Doherty PA Architecture

Antenna impedance variations can perturb the desired PA operation and degrade its P_{out}, efficiency, linearity, and reliability. In this section, the methodology of utilizing the active LM of the Doherty PA to compensate the antenna impedance variations and achieve PA performance enhancement under certain antenna impedance mismatches is investigated. The analysis is based on the theoretical Doherty PA model in Section 3.1. For the theoretical analysis in this section, a lossless output network is assumed for simplicity. The effects of the passive loss in the output network will be covered in the simulation studies in Section 3.3.

As shown in (30), the RF voltage amplitude at the auxiliary amplifier output is always smaller than the swing at the maximum P_{out}, i.e., $|v_{aux}| \leq V_{DD}$ for Class-B PA operation, in any PA operation condition of main/auxiliary amplifier path settings and

antenna impedance. However, this does not hold for $|v_{main}|$ under antenna impedance variations, potentially leading to the undesired waveform clipping and spectrum corruption. At a large antenna load VSWR, this may also lead to rapid degradation due to the effects like time-dependent dielectric breakdown (TDDB) and even device breakdown. In the following discussions, it is assumed that the main amplifier output RF voltage amplitude should stay below V_{DD} to avoid such device stress. This poses limits on the antenna load impedance regions in Figure 23 and Figure 24.

3.2.1 PA Performance Enhancement Examples

Before the comprehensive theoretical analysis, two representative examples which demonstrate the feasibility of using the digital Doherty PA to compensate and enhance the PA performance under antenna impedance mismatch are shown.

Example 1: Assume the antenna impedance as $Z_{antenna}=2R_0$, i.e., $A=2$ and $\varphi=0°$ in the load expression $Ae^{j\varphi}R_0$. Thus, $Z_{antenna}$ is located on the 2:1 VSWR circle with phase(Γ)=0° (Figure 23 and Figure 24). For a conventional symmetric analog Doherty PA with such a mismatched load, when both the main and auxiliary amplifiers are fully on ($x=y=1$), one can find that $v_{main}=0$ and $\eta=39.27\%$ based on (29) and (28). In fact, when the two amplifiers output their maximum currents, the Doherty active LM nulls the RF output from the main amplifier by presenting zero load impedance at its output (31), causing a significant degradation of the overall PA efficiency.

On the other hand, in a digital Doherty PA which can independently configure the main/auxiliary amplifier outputs, the auxiliary amplifier can be turned off (x=1 and y=0). This thus restores the main amplifier RF voltage amplitude (29), i.e., $|v_{main}|=V_{DD}$, and the overall DE is recovered to 78.54% based on equation (28).

Note that the total PA P_{out} are the same for both cases, i.e., a half of the maximum PA P_{out} with a standard load $Z_{antenna}=R_0$. Essentially, the PA DE is recovered by turning off the auxiliary amplifier, which is feasible in the digital Doherty PA configuration.

Example 2: Assume the antenna impedance as $Z_{antenna}=R_0/2$, i.e., A=0.5 and φ=0° in $Ae^{j\varphi}R_0$. Thus, $Z_{antenna}$ is located on the 2:1 VSWR circle with phase(Γ)=180° (Figure 23 and Figure 24). For a conventional symmetric analog Doherty PA with such antenna impedance, if the PA operates at its 6 dB PBO (x=0.5 and y=0), one can find that $|v_{main}|=2V_{DD}$. Thus, the main amplifier is overdriven and faces distortion and reliability issues in practice. However, if one keeps the main amplifier output and increases the auxiliary amplifier output, e.g., x=0.5 and y=1, $|v_{main}|$ is then reduced to V_{DD}, relieving the overdriven issue. Note that in both cases, the total PA P_{out} stays the same, since it only depends on x (Design Insight 1 in Section 3.1.3). Therefore, the Doherty active LM enhances the linearity and reliability of the PA in this example.

In both examples, the digital Doherty PA architecture recovers the PA performance under the antenna impedance variation. *Specifically, the desired PA performance*

enhancement here is defined as delivering the target RF power to a given mismatched load while providing the maximum PA efficiency with no device stress.

Given a complex antenna impedance $Ae^{j\varphi}R_0$, the target P_{out} or PBO level defines the value of x, i.e., the normalized output RF current of the main amplifier, based on equations (27) and (34). At this P_{out} and fixed x, based on equation (28), maximizing the PA efficiency means minimizing y. At the same time, the main amplifier needs to operate without voltage clipping. Therefore, the optimum performance enhancement can be summarized as: given $Ae^{j\varphi}R_0$ and x, find y, α and β to satisfy $|v_{main}| \leq V_{DD}$ while minimizing y. This methodology thus seeks to find the digital Doherty PA operation, which delivers the target RF power to a given mismatched antenna load, avoids main amplifier voltage clipping, and maximizes the total PA efficiency.

3.2.2 Antenna Mismatch Compensation and PA Performance Enhancement by Utilizing the Digital Doherty PA Architecture

Based on equation (29), the normalized RF voltage amplitude at the main amplifier output is given as:

$$\left(\frac{|v_{main}|}{V_{dd}}\right)^2 = [y\cos(\alpha-\beta+\varphi)-\frac{2x}{A}]^2+[y\sin(\alpha-\beta+\varphi)]^2. \quad (45)$$

This equation indicates that only the phase difference, i.e., $(\alpha-\beta)$, matters, which aligns with basic design intuitions.

To facilitate the following discussions, four types of Doherty PAs are defined, which have different degrees of freedom in tuning the main/auxiliary paths.

Type-I: Both the RF currents (x, y) and the extra phase difference ($\alpha-\beta$) of the main/auxiliary amplifiers can be independently and arbitrarily configured.

Type-II: The RF currents (x, y) can be arbitrarily set for the two paths, but there is no extra phase tuning, i.e., ($\alpha-\beta$)=0.

Type-III: The RF current phase difference ($\alpha-\beta$) between the two paths can be arbitrarily set, but their currents (x, y) follow the fixed relationship in the conventional analog Doherty PA, i.e., equation (41).

Type-IV: There is no flexibility of configuring the RF current weightings (x, y) or the phase difference ($\alpha-\beta$) of the two paths. The RF current weightings follow the fixed relationship in (41). This is the case for the conventional analog Doherty PA, and it is used as the baseline for performance comparison.

The following discussions are intended to address several key questions. (1) Is it possible to enhance PA performance at any target P_{out} level under arbitrary antenna impedance mismatch by the digital Doherty PA architecture? If not, what are the constraints on the antenna impedance and the target RF P_{out}? (2) If the antenna impedance mismatch can be compensated to deliver the desired RF power, what is the digital Doherty PA operation setting (x, y, α, and β) to achieve the maximum efficiency without device

stress? Evidently, since the four Doherty PA types offer different degrees of freedom for configuration, they result in different conclusions for the above questions. All the four Doherty PA types are covered in the following discussions.

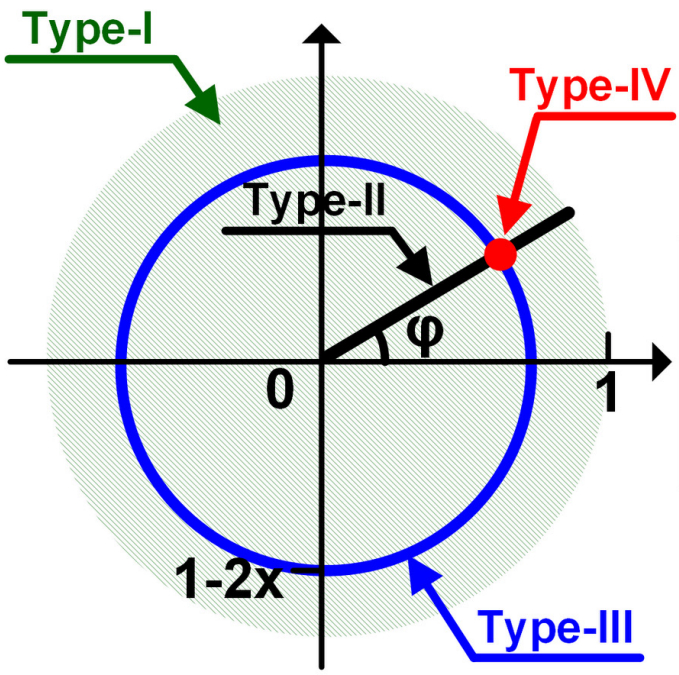
In order to provide design insights, the analysis is pursued using a graphical method. Numerical simulation results will be presented in Section 3.3 to intuitively visualize and summarize the graphical analysis results.

Equation (45) can be interpreted as the normalized main amplifier RF output voltage equals the Euclidean distance between the two points, i.e., ($y\cos(\alpha-\beta+\varphi)$, $y\sin(\alpha-\beta+\varphi)$) and ($2x/A$, 0), in a 2D Cartesian space. Note that the given antenna impedance determines the quantities A and φ, and the required PA P_{out} fixes the quantity x based on (27). Thus, the point ($2x/A$, 0) is completely determined in the 2D Cartesian space for a given PA operation case. Therefore, one needs to find y (the normalized RF output current of the auxiliary amplifier) and ($\alpha-\beta$) (the extra phase difference between the two amplifier paths), so that the target distance is less than 1 to ensure no clipping while y should be minimized to ensure the maximum PA DE (28). Further, ($\alpha-\beta+\varphi$) and $2x/A$ are respectively denoted as θ and c, and the equation (45) can be rewritten as:

$$(|v_{main}|/V_{dd})^2 = (y\cos\theta - c)^2 + (y\sin\theta)^2. \quad (46)$$

Note that ($y\cos\theta$, $y\sin\theta$) represents a point on a circle of radius y centered at the origin of the 2D Cartesian space. For a given P_{out} or equivalently for a given x, the valid

PA operation points ($y\cos\theta$, $y\sin\theta$) depend on the Doherty PA type. Assume a symmetric Doherty PA, any point within the unity circle centered at the origin is available for Type-I Doherty PA. For Type-II Doherty PA, only the points on the line segment with the origin and ($\cos\theta$, $\sin\theta$) as two terminal points are valid. For Type-III Doherty PA, only the points on the circle of radius $y=2x-1$ centered at the origin are achievable. Since there is no flexibility for Type-IV Doherty PA, only the point ($y\cos\theta$, $y\sin\theta$), where $y=2x-1$ is valid. Figure 26 illustrates the valid PA operation points for the four Doherty PA types.



Doherty PA Type	Amplitude Tunability	Phase Tunability
Type-I	√	√
Type-II	√	×
Type-III	×	√
Type-IV	×	×

Figure 26 – Valid PA operation regions for the four Doherty PA types. (The main and auxiliary amplifiers are assumed to be symmetric in this plot.)

Therefore, the goal of the graphical analysis is to find the point on the 2D Cartesian space, which simultaneously satisfies three constraints:

(1) *Being within the valid PA operation region depending on the Doherty PA type;*

(2) *Being within a unity circle centered at (2x/A, 0) for no clipping at the main amplifier output;*

(3) *Being the closest towards the origin (0, 0) to achieve the minimum y and maximum efficiency.*

If the constraints (1) and (2) cannot be satisfied at the same time, the desired PA operation thus does not exist. In other words, the digital Doherty PA cannot deliver the target RF power to such a mismatched antenna impedance without causing voltage clipping at main amplifier output. Techniques to address this limitation will be presented in the next section. The analysis in this section focuses on the Doherty PAs with symmetric main and auxiliary amplifiers (x, $y \in [0,1]$). Asymmetric Doherty PAs will be discussed in the next section.

3.2.2.1 Unconditional Clipping Scenario

For Type-I and II Doherty PAs, if $c>2$ ($A<x$), the two unity circles shown in Figure 27 do not intersect. In such case, $|v_{main}|/V_{DD} \leq 1$ cannot be satisfied and undesired voltage clipping at the main amplifier output always happens.

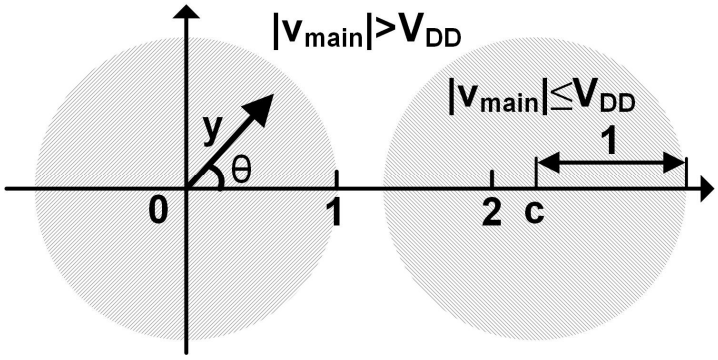


Figure 27 – Unconditional clipping scenario for Type-I and II Doherty PAs.

For Type-III and IV Doherty PAs, when the auxiliary amplifier is on and follows the main/auxiliary amplifier relationship of $y=(2x-1)\in(0,1]$. If $(2x-1)+1<c$ ($A<1$), the two circles, one with radius $(2x-1)$ at the origin and one with unity radius centered at $(c, 0)$ do not intersect (Figure 28), and undesired voltage clipping again occurs at the main amplifier output.

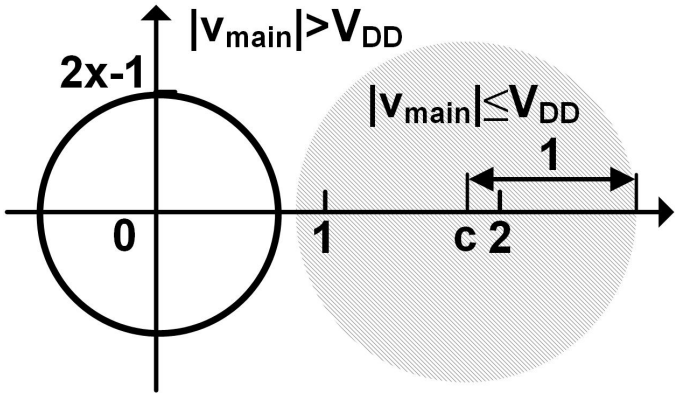


Figure 28 – Unconditional clipping scenario for Type-III and IV Doherty PAs.

We call these PA operation cases "*Unconditional Clipping Scenario*". In this scenario, for any load phase φ, the Doherty PA cannot deliver the target power to such antenna impedance without causing voltage clipping at the main amplifier output.

3.2.2.2 Unconditional Non-Clipping Scenario

For the PA operation cases when the three constraints (Section 3.2.2) can always be met for any load phase φ, they are named "*Unconditional Non-Clipping Scenario*". Different Doherty PA types have different unconditional non-clipping PA operation cases, which are presented below.

For Type-I Doherty PA, if $0 \le c \le 2$ ($A \ge x$), clipping can be avoided for any load phase φ. As a subset, when $0 \le c \le 1$ ($A \ge 2x$), the origin is always enclosed by the unity circle centered at (c, *0*) (Figure 29). The origin (y=0) satisfies all the constraints, meaning that the auxiliary amplifier should be turned off. The best achievable total PA efficiency is

$$\eta = \frac{\pi}{2}\frac{x}{A}\cos\varphi, \tag{47}$$

which is the efficiency of the main amplifier operating alone.

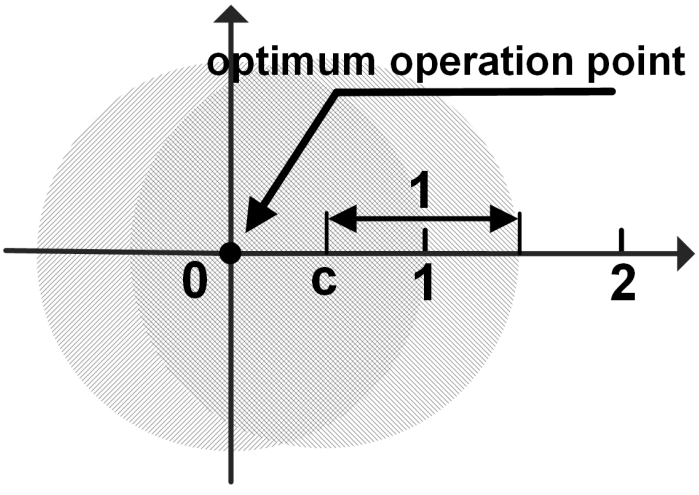


Figure 29 – Unconditional non-clipping scenario for Type-I and II Doherty PAs ($0 \le c \le 1$).

If $1<c\leq 2$ ($A\leq x\leq 2A$), the two unity circles always intersect (Figure 30). For Type-I Doherty PA, the non-clipping constraint is always achievable. The optimum PA configuration can be graphically found as

$$y = c - 1 = \frac{2x}{A} - 1 \tag{48}$$

and θ=0° (Figure 30). The latter phase condition (θ=0°) leads to

$$\alpha - \beta = -\varphi, \tag{49}$$

which means the extra phase difference between the two amplifier paths should exactly cancel the phase angle of the antenna impedance.

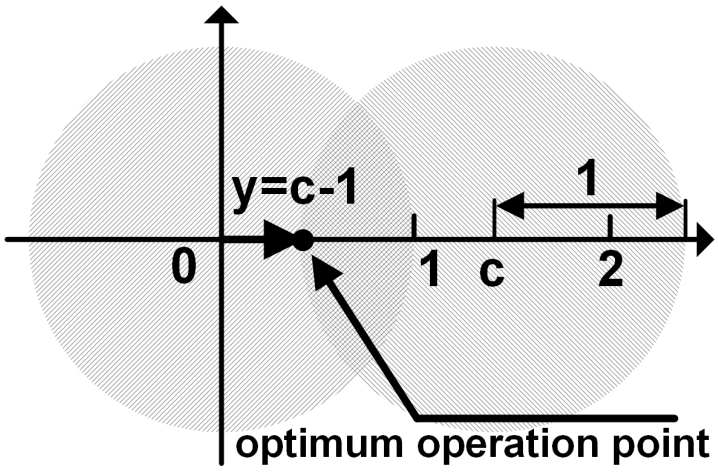


Figure 30 – Unconditional non-clipping scenario for Type-I Doherty PA ($1<c\leq 2$).

Based on (28) and (48), the total PA efficiency is

$$\eta = \frac{\pi}{2}\frac{x^2}{A}\frac{\cos\varphi}{x+(2x/A-1)} = \frac{\pi}{2}\frac{x^2\cos\varphi}{(A+2)x-A}. \tag{50}$$

Type-II Doherty PA behaves similar to Type-I Doherty PA when $0 \le c \le 1$ ($A \ge 2x$, Figure 29). But it behaves differently when $1 < c \le 2$, which will be discussed in next section.

For Type-III Doherty PA, when the auxiliary amplifier is on, it follows the relationship of $y=(2x-1)$. If $(2x-1)+1 \ge c$ ($A \ge 1$), the two circles intersect. For a given phase angle φ of the load, by varying θ through adjusting $(\alpha-\beta)$, the non-clipping constraint $|v_{main}| \le V_{DD}$ can be satisfied (Figure 31). The required minimum phase tuning is solved as:

$$(\alpha-\beta)=\begin{cases}0, & if\ |\varphi| \le \tilde{\varphi} \\ -\varphi+\tilde{\varphi}, & if\ |\varphi| > \tilde{\varphi}\ and\ \varphi > 0 \\ -\varphi-\tilde{\varphi}, & if\ |\varphi| > \tilde{\varphi}\ and\ \varphi < 0\end{cases}, \tag{51}$$

where

$$\tilde{\varphi}=\arccos\left(\frac{(A^2+1)x-A^2}{A(2x-1)}\right). \tag{52}$$

The achieved best PA efficiency in this case is

$$\eta=\frac{\pi}{2}\frac{x^2}{3x-1}\frac{\cos\varphi}{A}. \tag{53}$$

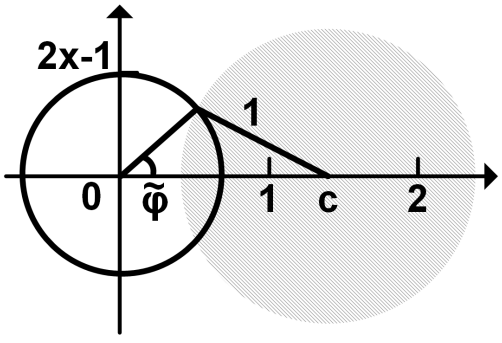


Figure 31 – Unconditional non-clipping scenario for Type-III Doherty PA.

For Type-IV Doherty PA, i.e., the analog Doherty PA without any amplitude/phase tuning flexibility, because $\varphi \in [-90°, +90°]$, if the right half of the circle with radius $(2x-1)$ centered at the origin is completely enclosed in the unity circle centered at $(c, 0)$ (Figure 32), i.e., $A \geq \sqrt{x/(1-x)}$, there is no voltage clipping at the main PA output for any load phase φ. Under the load conditions without voltage clipping, the total PA DE is the same as (53).

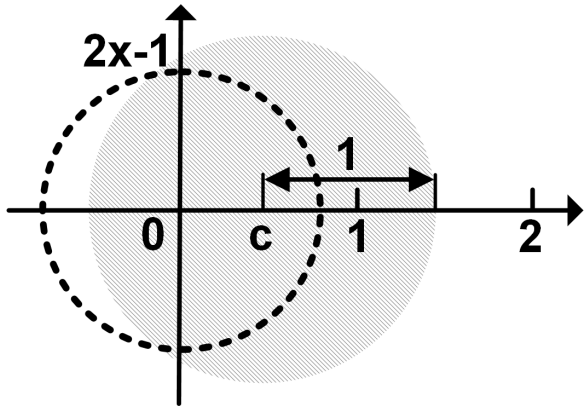


Figure 32 – Unconditional non-clipping scenario for Type-IV Doherty PA.

3.2.2.3 Conditional Non-Clipping Scenario

For the PA operation case when the PA efficiency can be restored without causing voltage clipping at the main amplifier output only for certain antenna impedance phases, it is defined as the "*Conditional Non-Clipping Scenario*".

For Type-II Doherty PA, to assess the antenna impedance conditions which do not cause clipping in this scenario, A is further divided into two regions, $x \leq A < \sqrt{2}x$ and $\sqrt{2}x \leq A < 2x$. Note that in Type-II Doherty PA, $\theta = \varphi$, as there is no phase tuning. Figure 33a

and Figure 33b show the boundary cases in these two situations. For $x \le A < \sqrt{2}x$, the complex antenna impedance phase φ should satisfy

$$|\varphi| \le \tilde{\varphi} = \arccos(\frac{x}{A}), \tag{54}$$

while for $\sqrt{2}x \le A < 2x$, φ should be constrained within

$$|\varphi| \le \tilde{\varphi} = \arcsin(\frac{A}{2x}). \tag{55}$$

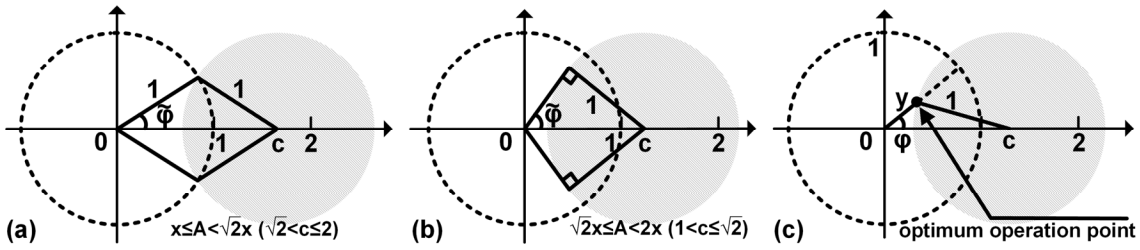


Figure 33 – Conditional non-clipping scenario for Type-II Doherty PA.

Considering the preconditions between the quantities x and A, equation (54) means $0° \le \tilde{\varphi} < 45°$, and equation (55) means $45° \le \tilde{\varphi} < 90°$. In both antenna impedance phase constraints, for a given x, $\tilde{\varphi}$ monotonously increases when A increases; for a given A, $\tilde{\varphi}$ monotonously decreases when x increases.

When the antenna impedance phase is within the constraints, the y value for the enhanced PA performance can be calculated as (Figure 33c):

$$y = \frac{2x}{A}\cos\varphi - \sqrt{1 - (\frac{2x}{A}\sin\varphi)^2}. \tag{56}$$

The corresponding PA DE is thus given as:

$$\eta = \frac{\pi}{2} \frac{x^2 \cos\varphi}{Ax + 2x\cos\varphi - \sqrt{A^2 - 4x^2 \sin^2\varphi}}. \tag{57}$$

For Type-IV Doherty PA, the unconditional clipping scenario means $A<1$ and the unconditional non-clipping scenario means $A \geq \sqrt{x/(1-x)}$ based on the previous analysis. When $1 \leq A < \sqrt{x/(1-x)}$ (Figure 34), in order to have no voltage clipping, the antenna impedance phase should satisfy

$$|\varphi| \leq \tilde{\varphi} = \arccos\left(\frac{(A^2+1)x - A^2}{A(2x-1)}\right). \tag{58}$$

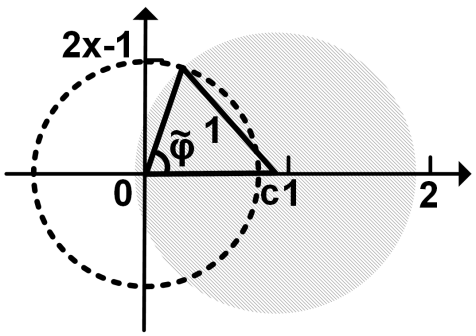


Figure 34 – Conditional non-clipping scenario for Type-IV Doherty PA.

The dependence of $\tilde{\varphi}$ on A and x is examined by

$$\frac{\partial(\cos\tilde{\varphi})}{\partial A} = \frac{x - 1 - x/A^2}{2x-1} \tag{59}$$

and

$$\frac{\partial(\cos\tilde{\varphi})}{\partial x} = \frac{A - 1/A}{(2x-1)^2}. \tag{60}$$

The discussion here is limited to Type-IV Doherty PA when the auxiliary amplifier is on, i.e., $(2x-1)>0$. Given $A\geq 1$, (59) is then negative whereas (60) is always positive. This means that decreasing A or increasing x shrinks the non-clipping area, making it more difficult to find the valid PA operation configuration for such antenna impedance and P_{out}.

Table 4 – Summary of the analytical results on antenna impedance variation compensation and PA performance enhancement by exploiting the digital Doherty PA architecture

	Type-I			Type-II			
	Unconditional Clipping	Unconditional Non-Clipping		Unconditional Clipping	Conditional Non-Clipping		Unconditional Non-Clipping
Condition	$A<x$	$x\leq A<2x$	$A\geq 2x$	$A<x$	$x\leq A<\sqrt{2}x$	$\sqrt{2}x\leq A<2x$	$A\geq 2x$
Tolerable φ for conditional non-clipping	-	-	-	-	$\lvert\varphi\rvert\leq \arccos(\frac{x}{A})$	$\lvert\varphi\rvert\leq \arcsin(\frac{A}{2x})$	-
Optimum y	-	$2x/A-1$	0	-	$\frac{2x}{A}\cos\varphi-\sqrt{1-(\frac{2x}{A}\sin\varphi)^2}$		0
Optimum $(\alpha-\beta)$	-	$-\varphi$	0	-	-	-	0
Restored efficiency	-	$\frac{\pi}{2}\frac{x^2\cos\varphi}{(A+2)x-A}$	$\frac{\pi}{2}\frac{x}{A}\cos\varphi$	-	$\frac{\pi}{2}\frac{x^2\cos\varphi}{Ax+2x\cos\varphi-\sqrt{A^2-4x^2\sin^2\varphi}}$		$\frac{\pi}{2}\frac{x}{A}\cos\varphi$

	Type-III		Type-IV (Classic Analog Doherty PA)		
	Unconditional Clipping	Unconditional Non-Clipping	Unconditional Clipping	Conditional Non-Clipping	Unconditional Non-Clipping
Condition	$A<1$	$A\geq 1$	$A<1$	$1\leq A<\sqrt{x/(1-x)}$	$A\geq\sqrt{x/(1-x)}$
Tolerable φ for conditional non-clipping	-	-	-	$\lvert\varphi\rvert\leq\arccos(\frac{(A^2+1)x-A^2}{A(2x-1)})$	-
Optimum y	-	-	-	-	-
Optimum $(\alpha-\beta)$	-	$\begin{cases}0, & if\ \lvert\varphi\rvert\leq\tilde{\varphi}\\ -\varphi+\tilde{\varphi}, & if\ \lvert\varphi\rvert>\tilde{\varphi}\ and\ \varphi>0\\ -\varphi-\tilde{\varphi}, & if\ \lvert\varphi\rvert>\tilde{\varphi}\ and\ \varphi<0\end{cases}$ $\tilde{\varphi}=\arccos(\frac{(A^2+1)x-A^2}{A(2x-1)})$	-	-	-
Restored efficiency	-	$\frac{\pi}{2}\frac{\cos\varphi}{A}\frac{x^2}{3x-1}$	-	$\frac{\pi}{2}\frac{\cos\varphi}{A}\frac{x^2}{3x-1}$	

For Type-IV Doherty PA, under the load conditions without clipping, its total PA DE is the same as (53).

In addition, it can be seen that the conditional clipping scenarios in Type-II/-IV Doherty PAs are due to their lack of phase tunability.

The above analysis results for the three scenarios and four Doherty PA types are summarized in Table 4, and further interpretations will be presented in Section 3.3.

3.2.3 Extending the Non-Clipping Antenna Impedance Region

As demonstrated above, the digital Doherty PAs can recover the PA performance for certain mismatched antenna impedances. To extend the non-clipping antenna impedance region, three design techniques are presented in this section.

3.2.3.1 Asymmetric Doherty PA Design

Asymmetric analog Doherty PA designs with stronger auxiliary amplifiers ($x \in [0,1]$, $y \in [0, y_{max}]$, and $y_{max}>1$) have been reported to enhance efficiency over a wider PBO range. The analysis indicates that when this asymmetric design technique is applied to the digital Doherty PAs with flexibility on the RF current weightings from the two amplifier paths (Type-I and II), it can extend the antenna impedance region where the PA performance can be enhanced without main amplifier voltage clipping. In the graphical analysis, a stronger auxiliary amplifier expands the size of the circle centered at the origin, which directly

increases the accessible region. This results in a decreased unconditional clipping area for Type-I/-II (Figure 27), an increased unconditional non-clipping area for Type-I (Figure 30), and an increased conditional non-clipping area for Type-II (Figure 33a).

Intuitively, a larger auxiliary amplifier current decreases the effective load impedance seen by the main amplifier after the impedance inversion, leading to a smaller RF voltage swing and making the main amplifier less likely to clip.

3.2.3.2 Additional Tunable Matching Network

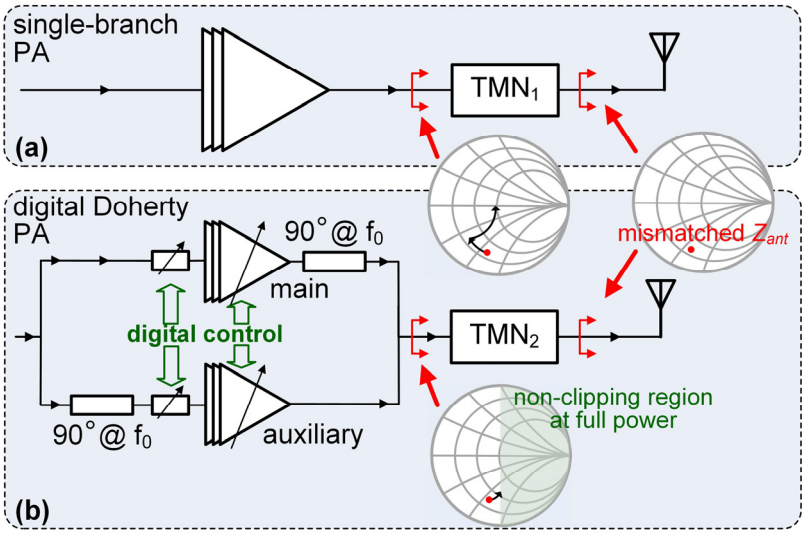


Figure 35 – Comparison of the required TMN in single-branch PA and digital Doherty PA.

TMN has been conventionally used to adjust load impedance (Figure 35a). TMN can be jointly implemented with digital Doherty PAs. In this case, TMN only needs to tune the load into the impedance region where the digital Doherty PA can compensate the remaining mismatch (Figure 35b). This significantly reduces the impedance tuning range

requirement for the TMN (Figure 35), since part of the antenna impedance compensation and PA performance enhancement is achieved through the digital Doherty PA operation. In practice, this eases the TMN design tradeoff between its tunability and loss.

3.2.3.3 Backing-Off the Peak P_{out}

Backing-off the peak P_{out} can also address load variations for PA designs. Despite its degradation on maximum PA power and efficiency, it offers simplicity in implementation.

Peak PBO can also be used in digital Doherty PAs to address the voltage clipping issue for those load conditions outside the non-clipping load region. As shown in Table 4, once non-clipping is achieved at this reduced peak P_{out}, there is no clipping for lower power levels. A minimum back-off in peak power is desired. The graphical analysis method can again be used to calculate the minimally required peak PBO. Backing off the peak P_{out} is to move the unity circle centered at $(2x/A, 0)$ towards the left in the 2D Cartesian space. If denoting $\tilde{x}$ for the maximum x after having back-off in peak power, the results of $\tilde{x}$ for four types of symmetric Doherty PAs under an antenna load of $Ae^{j\varphi}R_0$ are summarized in Table 5. The results will be further interpreted in the following section.

Table 5 – Minimally required peak PBO for the clipping load condition

Doherty PA Type	Type-I	Type-II	Type-III	Type-IV
$\tilde{x}$	A	$\begin{cases} A\cos\varphi, & if\ 0^\circ \le \lvert\varphi\rvert < 45^\circ \\ A/(2\sin\varphi), & if\ 45^\circ \le \lvert\varphi\rvert \le 90^\circ \end{cases}$	$A/2$	$\begin{cases} A/2, & if\ A<1 \\ A(A-\cos\varphi)/(A^2-2A\cos\varphi+1), & if\ A\ge 1 \end{cases}$

3.3 Simulation Results

Numerical simulations are performed to visualize and summarize the analysis results in Section 3.2. In the simulation, for Type-I/-II Doherty PAs, the main and auxiliary amplifier are each assumed to be a 5-bit binary weighted RF DAC. Therefore, in a symmetric Doherty PA, x and y can both vary independently from 0 to 1 with a step of 1/31, resulting in 1024 combinations of (x, y). For Type-I/-III Doherty PAs, the extra phase difference between the two paths, ($\alpha-\beta$), is assumed to be tunable from −180° to 180° with a step of 1°.

3.3.1 Effects of the Output Network Loss

Figure 36 and Figure 37 show the simulated PA efficiency with respect to the PBO level for a symmetric Type-II Doherty PA under a standard load (A=1, φ=0°). The output network is assumed to be lossless (k=1) in Figure 36 and lossy (k=0.8) in Figure 37. Each point in the two figures represents one RF current combination (x, y). All the 1024 combinations are computed and the efficiency results are plotted.

In Figure 36, the points in each vertical line have the same PBO but different efficiency values. The (x, y) combinations on the same PBO line have the same x but different y. This agrees with Section 3.1.3 that the Doherty PA P_{out} quantitatively only depends on the RF current from the main amplifier when the output network is lossless.

However, for a lossy output network, the points with equal x values lie in curved lines (Figure 37), showing that the passive loss makes the PBO depend on both x and y.

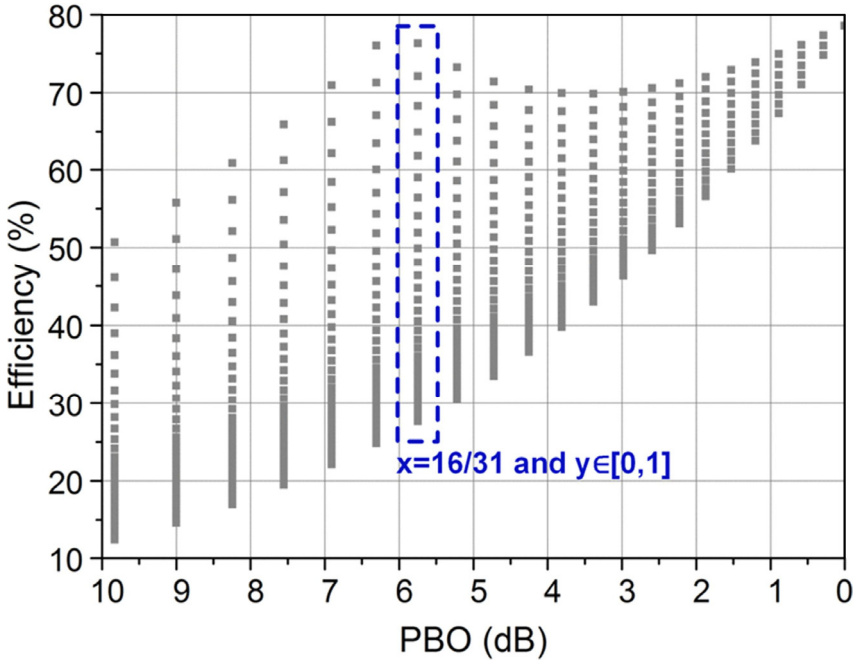


Figure 36 – Simulated efficiency with a lossless output network (k=1 in Figure 22).

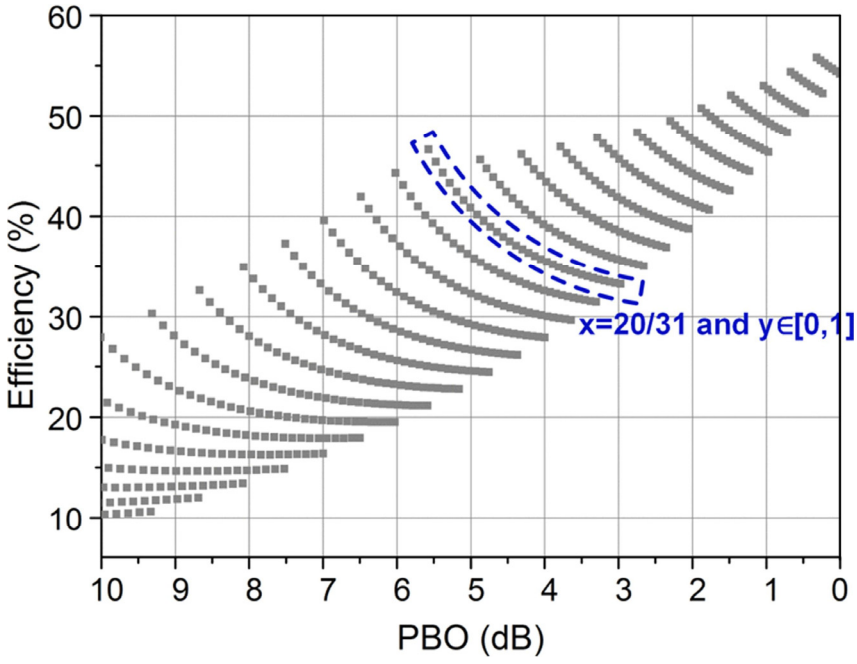


Figure 37 – Simulated efficiency with a lossy output network (k=0.8 in Figure 22).

In Figure 36, the 6 dB PBO efficiency peak is the same as the efficiency at the peak power (0 dB PBO), showing the ideal Doherty PBO efficiency behavior. However, in Figure 37, both efficiency values are reduced compared with the lossless case due to the output network loss. The 6 dB PBO efficiency is also lower than the 0 dB PBO efficiency. This is because the main amplifier power dominates at the 6 dB PBO, which experiences the loss of the output network. On the other hand, the auxiliary amplifier contributes significant power at the 0 dB PBO, which is not attenuated by the lossy output network.

3.3.2 PA Efficiency Enhancement and Optimum PA Configurations for the Symmetric Doherty PA Design

The key questions raised in Section 3.2.2 have been addressed through the graphical analysis. To demonstrate and summarize the analysis results, numerical simulations with exhaustive sweep and optimum search are conducted to find the best PA performance after enhancement and the corresponding settings. Here it is assumed that the output network is lossless.

Figure 38 and Figure 39 show the results at the peak power and 3 dB PBO, respectively. In each figure, sub-figures (a)-(d) are the PA efficiencies for Type-I to IV Doherty PAs with the same color scale bar. Sub-plot (d) represents the conventional analog Doherty PA with no tunability as the baseline reference. Sub-plots (e) and (f) are y and ($\alpha-\beta$) to achieve the recovered PA efficiency shown in (a) for Type-I Doherty PA. Sub-

plot (g) is the required y for Type-II Doherty PA. Sub-plot (h) is the required $(\alpha-\beta)$ for Type-III Doherty PA.

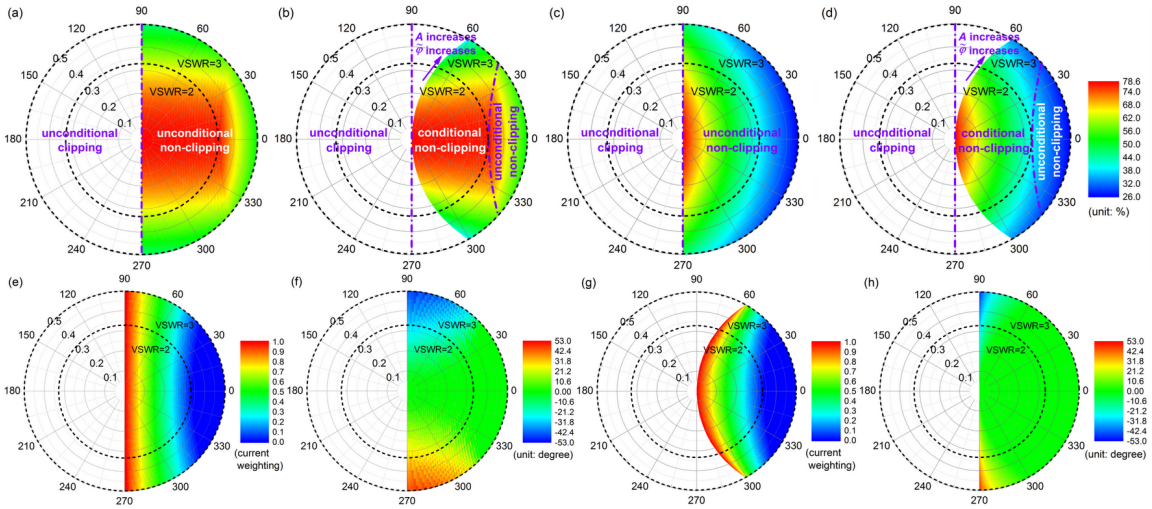


Figure 38 – Optimized PA efficiencies and the required PA tuning parameters at the peak PA P_{out} (x=1) for different load conditions. (a)-(d) show the PA drain efficiencies for Type-I to IV Doherty PAs. They share the same color bar shown in (d). Due to the Class-B operation assumption, the efficiency at the matched load is 78.5% for this peak PA P_{out} case. (e) and (f) are the required y and $(\alpha-\beta)$ for Type-I Doherty PA to achieve the optimum PA efficiency; (g) is the required y for Type-II Doherty PA; (h) is the required $(\alpha-\beta)$ for Type-III Doherty PA.

Antenna impedance regions which lead to voltage clipping are left blank in all the plots. Figure 38 and Figure 39 indicate that if the antenna load impedance falls to the left side of the Smith chart ($|Z_{antenna}|<R_0$), the Doherty PA may present voltage clipping at the main amplifier output and cause linearity and reliability issues. It should be noted that this is opposite to how a single-branch PA behaves, in which cases linearity and reliability issues rise when the load impedance is in the right side of the Smith chart ($|Z_{antenna}|>R_0$). This difference is due to the impedance inversion in the Doherty PA, which translates a

reduced antenna impedance to an increased impedance at the main amplifier output, causing potential voltage clipping.

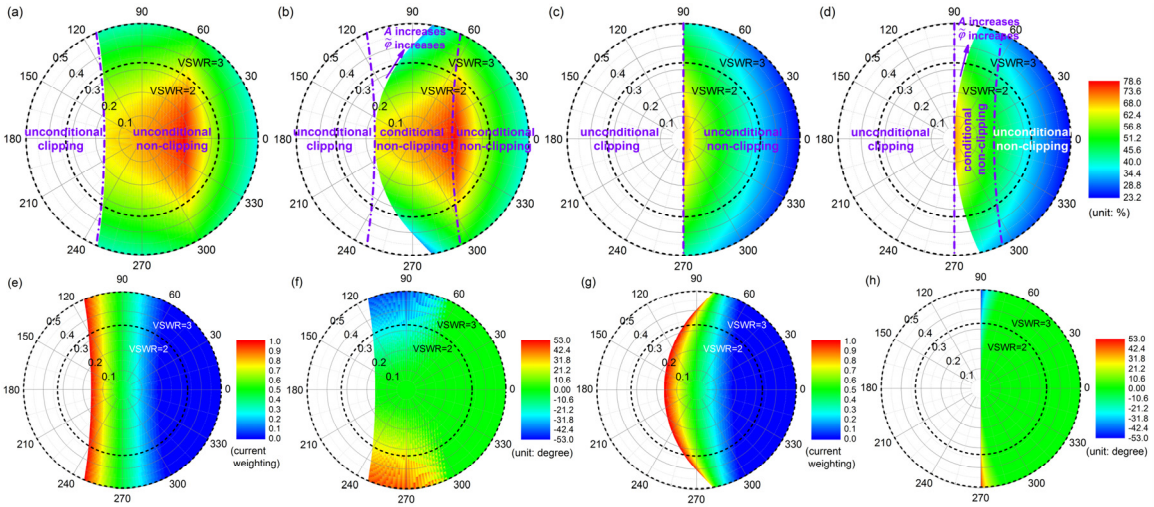


Figure 39 – Optimized PA efficiencies and the required PA tuning parameters at 3 dB PBO (x=22/31) for different load conditions. (a)-(d) are the PA drain efficiencies for Type-I to IV Doherty PAs. They share the same color bar shown in (d). Due to the Class-B operation assumption, the efficiency at the matched load is 70.2% for this 3 dB PBO case. (e) and (f) are the required y and ($\alpha-\beta$) for Type-I Doherty PA to achieve the optimum PA efficiency; (g) is the required y for Type-II Doherty PA; (h) is the required ($\alpha-\beta$) for Type-III Doherty PA.

The difference on the non-clipping load region shape between Type-I/-III and Type-II/-IV Doherty PAs is worth being pointed out. When the antenna load varies to the right side of the Smith chart, for Type-I/-III Doherty PAs, the non-clipping antenna impedance area covers all the φ for sufficiently large A. However, for Type-II/-IV Doherty PAs, there is an intermediate region where the tolerable φ gradually increases as A increases. This intermediate stage for Type-II/-IV Doherty PAs corresponds to the "conditional non-clipping scenario" in the graphical analysis. The simulation results also

verify the monotonicity of $\tilde{\varphi}(A)$ as derived in Section 3.2.2.3. This difference between Type-I/-III and Type-II/-IV Doherty PAs results from the lack of the phase tunability in the latter two types. This is also reflected in the load regions where the phase tuning capability is highly utilized in subplots (f) and (h) in Figure 38 and Figure 39. In other words, the flexibility on adjusting the phase difference between the two amplifier paths extends the non-clipping load area.

Comparing Figure 38 and Figure 39, during the PBO, the clipping antenna impedance region shrinks for Type-I/-II/-IV Doherty PAs, while it remains the same for Type-III Doherty PAs. There are two reasons causing the reduction of the clipping load area for those three types. On one hand, when x decreases for lower P_{out} during the back-off, the load area in the unconditional clipping scenario ($A<x$ for Type-I/-II in Table 4) becomes smaller and the load area in the unconditional non-clipping scenario ($A\geq x$ for Types-I, $A\geq 2x$ for Types-II, and $A \geq \sqrt{x/(1-x)}$ for Type-IV in Table 4) becomes larger. On the other hand, in the conditional clipping scenario for Type-II/-IV Doherty PAs, tolerable φ for the same A increases at PBO. This aligns with the result on the monotonicity of $\tilde{\varphi}(x)$ discussed in Section 3.2.2.3.

Regarding the PA efficiency at the peak P_{out}, for Type-IV Doherty PA, the classic analog Doherty PA, the efficiency is degraded to 26.2% for the load of VSWR=3:1 and phase(Γ)=0° as the worst case (Figure 38d). This value is recovered to 46.5% and 37.1% in Type-I/-II Doherty PA, respectively. More importantly, as shown in Figure 38a and

Figure 38b, the efficiencies can be recovered up to values larger than 60% for most of the antenna impedances without voltage clipping. Note that due to the Class-B operation assumption, the PA peak efficiency for the matched antenna load is 78.5%. In addition, during PBO, the best recovered efficiency at some mismatched loads can be even higher than that of the standard load. For example, at 3 dB PBO, the efficiency with the standard load is 70.2%. Whereas on the right side of the Smith chart, certain loads achieve 78.5% after efficiency enhancement, shown in Figure 39a and Figure 39b. Moreover, comparing the common non-clipping load regions for Type-I/-II Doherty PAs (Figure 38a/Figure 38b or Figure 39a/Figure 39b), they present similar recovered PA efficiencies. Besides, it should be noted that Type-III Doherty PA cannot recover the PA efficiency (Figure 38c), and it suffers the same efficiency degradation as the classic analog Doherty PA (Type-IV). These show that the flexibility on y, i.e., tuning the RF output current amplitude of the auxiliary amplifier, plays a critical role to compensate the antenna impedance variation effect and restore the efficiency of a Doherty PA.

It is also important to analyze the simulation results on the required PA tuning parameters which achieve the optimum PA efficiency. Regarding y, as shown in sub-plots Figure 38e/Figure 38g and Figure 39e/Figure 39g, when the load varies to the right side of the Smith chart, the auxiliary amplifier RF output current needs to be decreased. In fact, Example 1 studied in Section 3.2.1 also illustrates this result. On the other hand, at PBO, as shown in Figure 39e and Figure 39g, since the value of y with the standard load is smaller

than unity, when the load varies to the left side of the Smith chart, y can be increased until reaching its maximum. Intuitively, when the magnitude of the antenna load is larger than the normal value, due to the impedance inverter, the magnitude of the impedance seen by the main amplifier decreases. In order to recover the efficiency by restoring the voltage amplitude at the main amplifier output, the RF current from the auxiliary amplifier should be decreased to reduce the active LM effect. Similarly, when the amplitude of the load is smaller than the normal value, y should be increased.

Regarding the required phase tuning, for Type-I Doherty PA (Figure 38f and Figure 39f), when A is sufficiently large, no phase tuning is required. When A is smaller, phase tuning need to be leveraged and the distribution of the required tuning phase follows the distribution of the load phase angle φ (Figure 24) but with opposite signs. This matches with the graphical analysis results in Table 4. Figure 38f and Figure 39f show that the tunability on the phase difference between the two amplifier paths is particularly beneficial if the PA performance needs to be enhanced under load impedances with significant reactive parts. Moreover, the required maximum value of tuning phase in Figure 38f and Figure 39f is exactly the peak value of the load phase angle in concern (Figure 24). This result helps at the circuit design stage to define the required phase tuning range based on the given specification on the desired load region for PA performance enhancement. These results also apply for Type-III Doherty PA (Figure 38h and Figure 39h). In fact, for equation (52) obtained in the graphical analysis, $\tilde{\varphi}=0°$ for any x if substituting $A=1$ into it.

And the simulation results on the required maximum value of tuning phase for the Type-III case can be explained if replacing $\tilde{\varphi}$=0° into equation (51).

3.3.3 Asymmetric Digital Doherty Design

To verify the effects of the asymmetric design technique discussed in Section 3.2.3.1, simulations are performed on an asymmetric Type-II Doherty PA with the auxiliary amplifier having twice the current capacity as the main amplifier. In this case, x still varies from 0 to 1 with a step of 1/31, while y varies from 0 to 2 with a step of 2/31. Figure 40 summarizes the simulation results. Figure 40a and Figure 40b show the optimized PA efficiency and the desired y at the peak power; Figure 40c and Figure 40d are the results for the 3 dB PBO case. Comparing the non-clipping load area at the same P_{out} level in symmetric and asymmetric designs (e.g. Figure 38b/Figure 40a for the peak power, or Figure 39b/Figure 40c for 3 dB PBO), the non-clipping load area for the asymmetric design is increased significantly. First, the unconditional clipping load area is reduced. Second, the tolerable φ for the same A in the conditional non-clipping load region is increased. These agree with the explanations in Section 3.2.3.1 using the graphical analysis method. Figure 40b and Figure 40d show the corresponding y to achieve the recovered efficiencies. The extension of the non-clipping load region in the asymmetric design is due to the increased tuning range of the auxiliary amplifier output current.

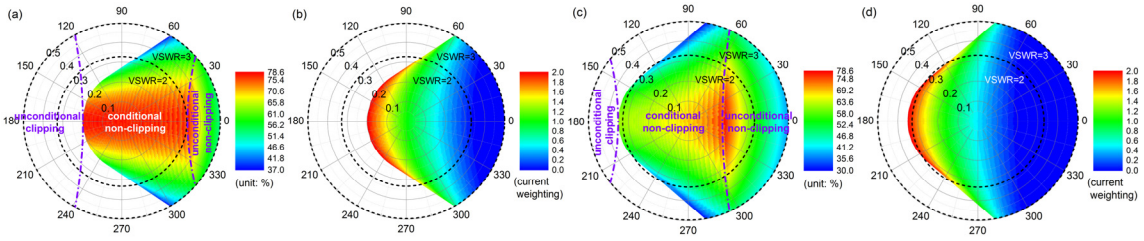


Figure 40 – Optimized PA efficiencies and the required PA tuning parameters for an asymmetrical (main/auxiliary = 1:2) Type-II Doherty PA at different load conditions. (a) and (b) show the PA efficiency and the required *y* at full power. (c) and (d) show the PA efficiency and the required *y* at 3 dB PBO.

3.3.4 Incorporating Peak PBO

As presented in Section 3.2.3.3, backing off the peak power is one of the solutions to extend the non-clipping load area for the digital Doherty PA architecture. The simulation results on the minimally required peak PBO for different types of symmetric Doherty PAs are shown in Figure 41. For those load regions where the load variation can be compensated solely by the digital Doherty PA architecture, the needed peak PBO is zero. The minimally required peak PBO for the worst case within the VSWR=3:1 circle is 7.8 dB for Type-III/-IV Doherty PAs. This value increases to 4.8 dB for Type-I/-II Doherty PAs. If further comparing Type-I and II Doherty PAs, larger peak PBO is required in less load conditions for Type-I Doherty PA. This demonstrates that less peak power needs to be sacrificed when the conventional peak PBO scheme is incorporated with the digital Doherty PA architecture. Besides, the more flexibility in the digital Doherty PA architecture, the more benefit gained by this hybrid technique.

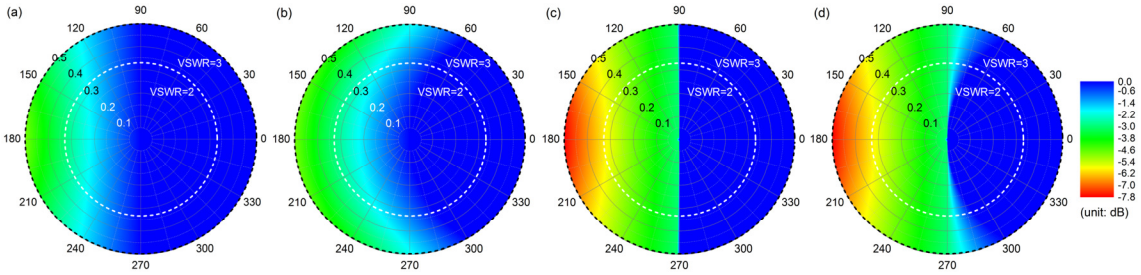


Figure 41 – The minimally required peak PBO. (a)-(d) are the results for Type-I to IV Doherty PAs, respectively.

3.4 Experimental Results

The fully integrated digital Doherty PA introduced in Chapter 2 is used here for the experimental validation. It is a Type-II digital Doherty PA, which offers sufficient antenna impedance mismatch compensation capability with moderate overhead. The measurement results are presented to verify the introduced concept.

3.4.1 CW Measurement

This digital Doherty PA is first characterized by CW signals with a 50Ω standard load. When both main and auxiliary amplifiers are fully on, the PA delivers +27.1 dBm peak P_{out} with 30.9% DE and 16.6 dB power gain at 3.60 GHz. The loss of the output network in this setting is 1.5 dB. The control words for both RF power DACs are then swept to capture the PA performance at the PBO. The measurement results are shown in Figure 42, where each point represents the result for one RF power DAC configuration. The code (M, A) means that there are M and A unit power cells turned on in the main and auxiliary amplifiers, respectively. For the same P_{out}, there exist several DAC configurations

which however offer different efficiencies. One can always choose the efficiency optimum control word. Figure 42 also shows the efficiency curve of an ideal Class-B PA as the comparison; the curve is normalized to the efficiency at the peak power. The Doherty PA achieves a maximum efficiency increase of 5.0% over a normalized Class-B PA at 5.7 dB PBO, which is 31% relative efficiency improvement.

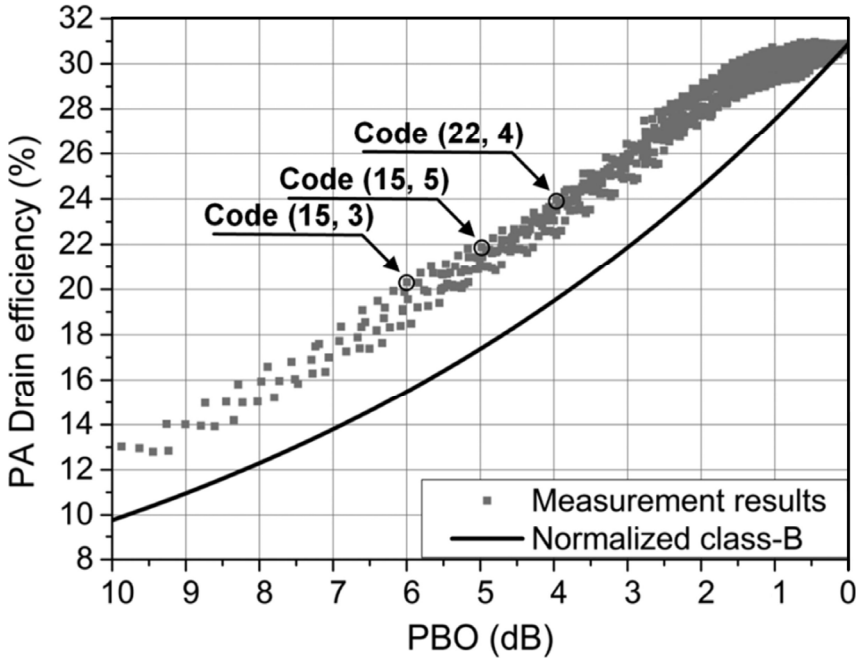


Figure 42 – Measured PA efficiency with the 50Ω standard load (3.6GHz, VSWR=1).

This digital Doherty PA is then characterized by CW signals with mismatched loads. To mimic the antenna impedance mismatch, an automated tuner by Maury Microwave is used to change the PA load impedance. The measurement results show that the back-off efficiency enhancement by Doherty operation is maintained when antenna impedance mismatch presents. Figure 43 illustrates the measurement results when the load is set at VSWR=2:1 with phase(Γ)=+60° (A=1.363, φ=+33°). The PA delivers +25.0 dBm

peak P_{out} with 21.9% DE and 14.5 dB power gain. The maximum efficiency improvement over a normalized Class-B PA is 4.6% at 5.2 dB PBO, which is 38% relative efficiency improvement. Note that the efficiency optimum code settings for mismatched loads are different from the ones for the 50Ω load. This demonstrates the efficacy of using the amplitude tunability in a digital Doherty PA to enhance the PA performance under mismatched antenna impedances.

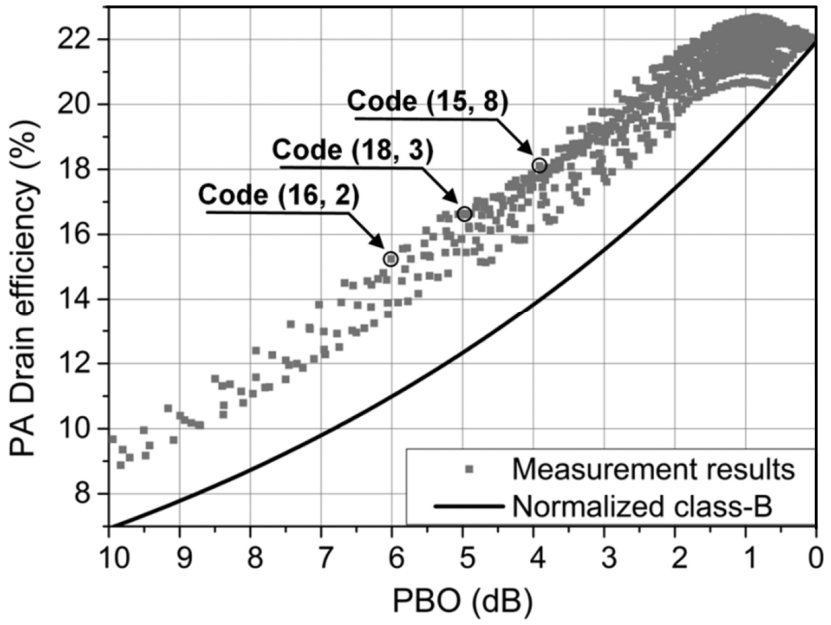


Figure 43 – Measured PA efficiency with the load at VSWR=2:1, phase(Γ)=+60° (3.6GHz).

To further investigate the Doherty operation with load variations, the efficiency optimum control words at several P_{out} levels with different loads are listed in Table 6. Results for load impedances having A<1 are not included in Table 6, since those impedances may result in severe voltage clipping at the main amplifier output for a Type-II Doherty PA (Section 3.2 and 3.3).

For a given load, it is shown in Table 6 that the power level depends on the current weightings from both amplifiers. Since the output network presents 1.5 dB loss at the peak power mainly due to the metal ohmic loss and the substrate loss, this dependence of the P_{out} on both amplifier current weightings confirms the theoretical results.

More importantly, for the same PBO level, Table 6 shows that the efficiency optimum control words for those three mismatched loads have one common property, i.e., a decreased auxiliary amplifier current weighting compared with the results for the 50Ω standard load. This result aligns with the analysis and simulations.

Table 6 – Measured efficiency optimum configurations in various load conditions

Load / PBO (dB)	LOAD I: standard load (A=1, φ=0°)	LOAD II: VSWR=2:1 phase(Γ)=0° (A=2, φ=0°)	LOAD III: VSWR=2:1 phase(Γ)=+60° (A=1.363, φ=+33°)	LOAD IV: VSWR=2:1 phase(Γ)=-60° (A=1.363, φ=-33°)
6.0	(15,3)	(15,1)	(16,2)	(15,0)
5.5	(15,4)	(14,2)	(18,2)	(15,1)
5.0	(15,5)	(14,3)	(18,3)	(17,0)
4.5	(19,4)	(18,1)	(19,4)	(20,0)
4.0	(22,4)	(14,5)	(15,8)	(23,0)

3.4.2 Modulated Signal Measurement

To assess the PA performance with modulated signals, this digital Doherty PA is measured with 1 MSym/s QPSK and 500 kSym/s 16-QAM signals, which present 3.7 dB and 5.4 dB PAPR, respectively. An RF vector signal generator synthesizes the phase modulated RF input signal, and the amplitude modulated signals are realized as the 10-bit

control signals by an FPGA board. No digital predistortion (DPD) is applied during the dynamic measurement.

Based on the data obtained in the CW measurement in Section 3.4.1, the envelope of the required AM transient waveform can be mapped to the efficiency optimum control words for the main/auxiliary amplifiers. It is called the efficiency optimum code set (EOCS) in the dynamic tests. Note that the EOCS is generally load dependent. In addition, the maximum P_{out} is mapped to the main/auxiliary amplifier setting of (31, 31) to utilize the full power range of the PA.

This Doherty PA is first measured with the 50Ω load using QPSK and 16-QAM modulation signals. At 3.6 GHz, it achieves 3.5/3.9% rms EVM with +23.3/+21.9 dBm average P_{out} and 22.9/18.2% PA DE for QPSK/16-QAM signals. Measured ACLR with 1.5/1 MHz offset for QPSK/16-QAM signals are −33.4/−35.3 dBc.

Measurement with modulation signals are then performed with mismatched loads in Table 6. When using the EOCS for each load condition, <5.6% (<−25 dB) rms EVM and <−30 dBc ACLR can be achieved for all the cases for both QPSK and 16-QAM signals. For example, with LOAD III in Table 6, this Doherty PA achieves 4.7/5.1% rms EVM and −33.5/−36.0 dBc ACLR with +21.1/+20.0 dBm average P_{out} for QPSK/16-QAM signals. The EVM and ACLR measurement results for the QPSK signal are shown in Figure 44. The average efficiency improvement over the normalized Class-B operation are 3.5% and

4.4% for QPSK and 16-QAM signals, respectively. Note that these are 25% and 36% relative efficiency enhancement over the normalized Class-B operation.

As a comparison, the PA is also measured under the mismatched load but using the EOCS for the 50Ω standard load, which is called the default code set (DCS). For example, with LOAD III in Table 6, if using the DCS, this Doherty PA achieves 4.5/3.7% rms EVM, −35.6/−36.2 dBc ACLR with +21.6/+20.8 dBm average P_{out}. The EVM and ACLR measurement results for the QPSK signal are shown in Figure 45. The average efficiency improvement over the normalized Class-B operation are 2.4/3.0% for QPSK/16-QAM signals, which are 16% and 22% relative efficiency improvement over the Class-B operation. Comparing these results with the efficiency enhancement by using the EOCS for LOAD III, the EOCS achieves a better efficiency enhancement. This verifies the introduced technique that utilizing the gain reconfigurability of the digital Doherty PA, one can achieve efficiency enhancement under antenna mismatch. On the other hand, the DCS results in marginally improved in-band and out-of-band linearity, i.e., EVM and ACLR (Figure 44 and Figure 45). However, the EOCS offers significantly enhanced PA efficiency over the DCS with marginal degradation on the linearity performance, demonstrating the benefits of the introduced concept.

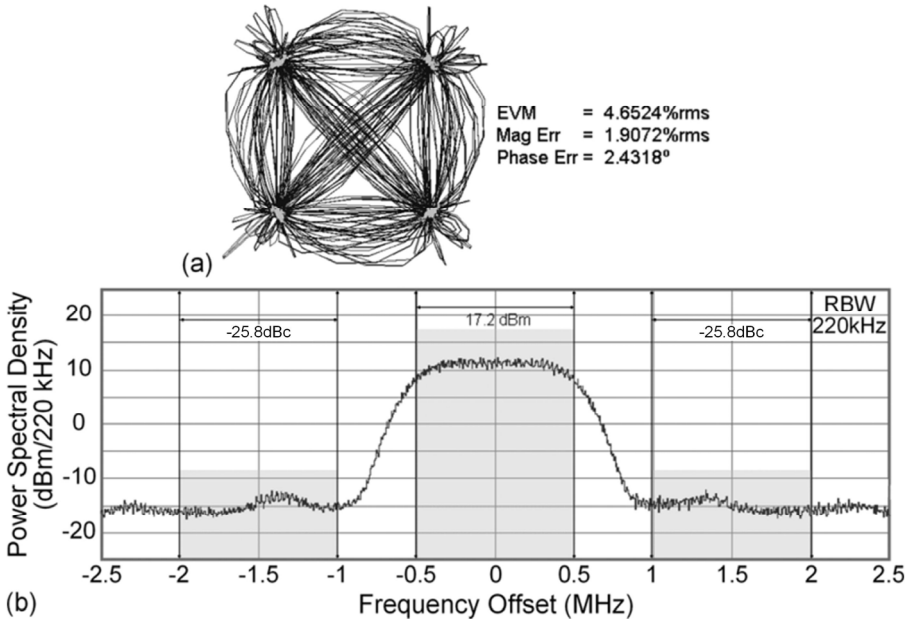


Figure 44 – Measured (a) EVM and (b) ACLR with the load at VSWR=2:1, phase(Γ)=+60° at 3.6 GHz using the EOCS.

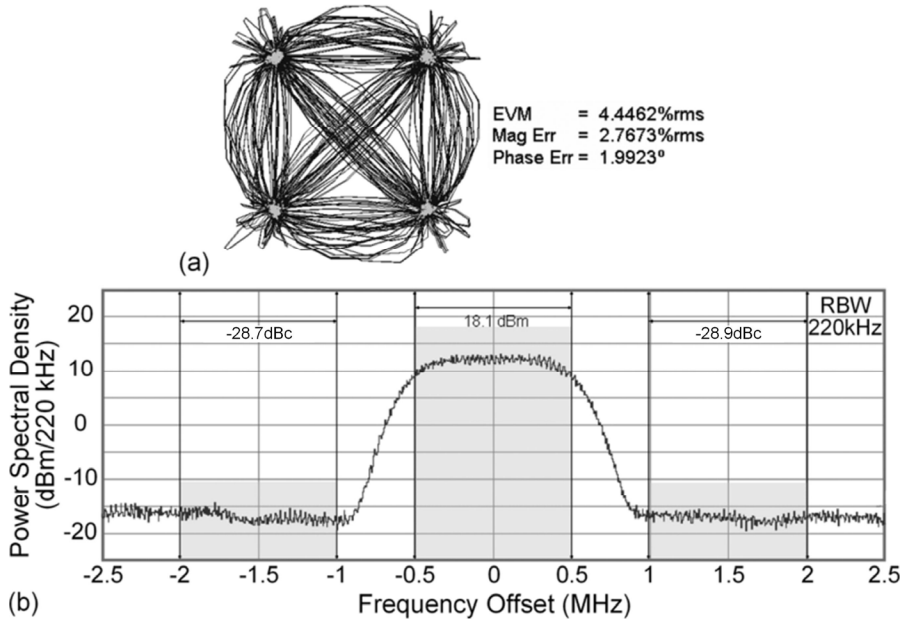


Figure 45 – Measured (a) EVM and (b) ACLR with the load at VSWR=2:1, phase(Γ)=+60° at 3.6 GHz using the DCS.

Table 7 and Table 8 summarize the measurement results for different mismatched antenna impedances, including the absolute and relative efficiency improvement over the

normalized Class-B operation, EVM, and ACLR, using both the EOCS and DCS. They also verify the introduced concept.

In summary, the measurement results of the implemented Type-II digital Doherty PA demonstrate the efficiency enhancement and performance recovery under antenna impedance mismatch by digitally reconfiguring its main/auxiliary amplifier RF current weightings.

Table 7 – Measured efficiency and linearity with mismatched loads using different code sets for the QPSK signal

Load and code set		Absolute η improve (%)	Relative η improve (%)	EVM (%)	ACLR (dBc)
VSWR=2:1 phase(Γ)=0°	EOCS	2.3	15	4.95	-25.1
	DCS	1.3	8	4.78	-27.9
VSWR=2:1 phase(Γ)=+60°	EOCS	3.5	25	4.65	-25.8
	DCS	2.4	16	4.45	-28.7
VSWR=2:1 phase(Γ)=-60°	EOCS	3.4	22	4.79	-24.4
	DCS	3.0	20	3.94	-25.9

Table 8 – Measured efficiency and linearity with mismatched loads using different code sets for the 16-QAM signal

Load and code set		Absolute η improve (%)	Relative η improve (%)	EVM (%)	ACLR (dBc)
VSWR=2:1 phase(Γ)=0°	EOCS	3.7	30	5.34	-25.9
	DCS	2.4	17	4.33	-26.8
VSWR=2:1 phase(Γ)=+60°	EOCS	4.4	36	5.09	-26.5
	DCS	3.0	22	3.68	-27.7
VSWR=2:1 phase(Γ)=-60°	EOCS	4.1	34	4.93	-26.0
	DCS	3.4	29	4.75	-26.8

Applying additional DPD to this digital Doherty PA may potentially further improve the linearity. Moreover, since the main and auxiliary amplifiers in the designed digital Doherty PA are implemented as power DACs, this directly offers digital control "knobs" for applying predistortion signals. Thus, this built-in flexibility of the digital intensive characteristic naturally facilitates such predistortions and potentially reduces their implementation complexities and overhead.

3.5 Summary

A comprehensive study on Doherty PAs under antenna impedance variations has been presented in this chapter. Complete theoretical analysis covering four types of Doherty PAs have been presented. It is demonstrated for the first time that, by reconfiguring the relative magnitudes and phases of the main/auxiliary amplifiers in the digital Doherty PA, the effect of antenna impedance mismatch can be largely compensated and the PA efficiency can be restored for certain antenna impedances. The measurement of a fully integrated digital Doherty PA implemented in 65nm CMOS are presented to validate this introduced concept. A PA resilient to load variations with closed-loop antenna impedance detection and compensation can be achieved by combining the introduced concept with the antenna impedance detection methods.

CHAPTER 4. A BROADBAND MIXED-SIGNAL CMOS PA WITH A HYBRID CLASS-G DOHERTY EFFICIENCY ENHANCEMENT TECHNIQUE

This chapter presents a CMOS PA with a hybrid Class-G Doherty architecture for PBO efficiency enhancement without any control switches at the PA output [77], [78]. Compared with the existing hybrid techniques [65]-[69], the introduced architecture achieves a substantial PA efficiency improvement in deep PBO with reduced design complexity and low PA output noise degradation. A mixed-signal real-time linearization technique is employed for the first time. In addition, a Doherty PA RF bandwidth extension technique is demonstrated. Section 4.1, 4.2, and 4.3 present the deep PBO efficiency enhancement, mixed-signal linearization, and RF bandwidth extension techniques together with the CW measurement results. The modulation tests are shown in Section 4.4.

4.1 Hybrid Class-G Doherty Efficiency Enhancement and CW Efficiency Measurement

4.1.1 Hybrid Class-G Doherty PA Architecture

This chapter presents a hybrid Class-G Doherty PA architecture for PA PBO efficiency enhancement (Figure 46). By combining the Class-G and Doherty operation, the deep PBO efficiency enhancement characteristic of a multi-stage Doherty PA is achieved without adding any extra complexity in the input or output RF passive networks. The

introduced hybrid Class-G Doherty operation is presented below. For simplicity, the main and auxiliary PAs are assumed to be symmetric. The PA knee voltage is assumed to be zero. All the harmonics are assumed to be shorted to ground.

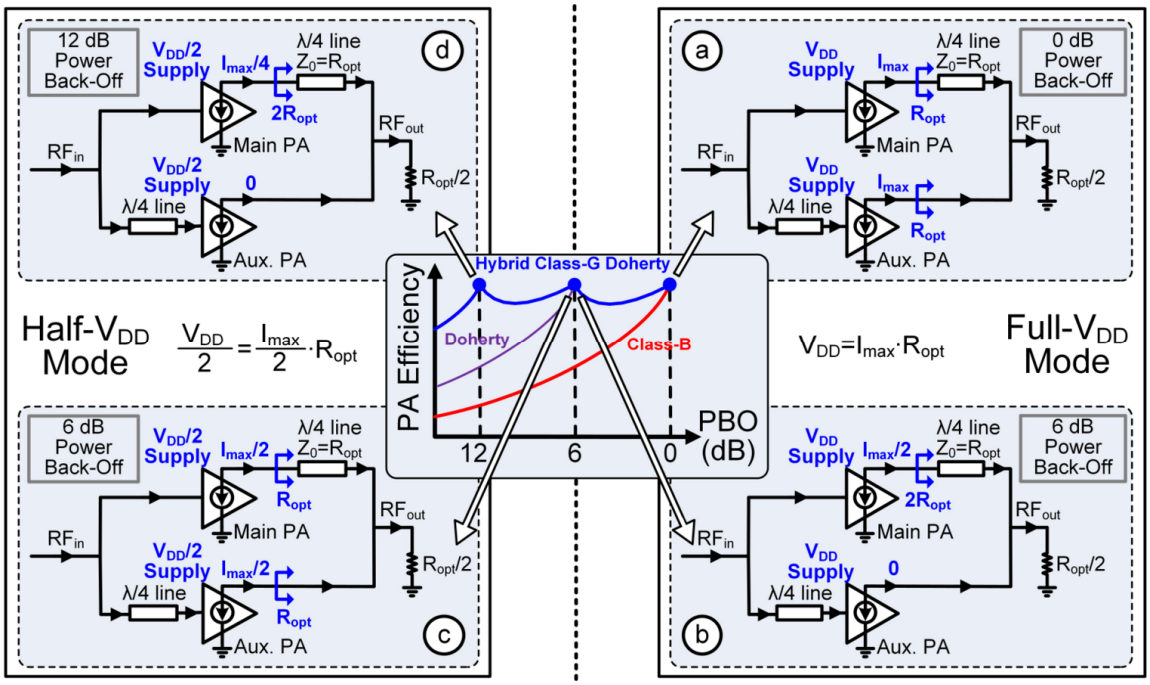


Figure 46 – Introduced hybrid Class-G Doherty operation and its theoretical PA efficiency behavior. The main and auxiliary PAs are assumed to be identical RF power DACs with zero knee voltages. All the harmonics are assumed to be terminated as short to ground.

From 0 dB to 6 dB PBO, the PA operates in the full-V_{DD} mode (Figure 46a and Figure 46b), and it performs the 2-way Doherty operation by digitally reconfiguring its main and auxiliary RF power DACs [75]. At the peak P_{out} (Figure 46a), i.e., 0 dB PBO, both the main and auxiliary PAs are fully on with their maximum RF output currents I_{max}[1]. Due to the Doherty active LM, both PAs have the same effective load of R_{opt}, which is the optimum load-pull impedance for the main and auxiliary RF power DACs. The RF voltage

amplitudes at both PA outputs are at their maximum values, i.e., the full supply voltages V_{DD}, and the maximum PA efficiency is achieved. At 6 dB PBO (Figure 46b), the auxiliary PA is turned off. The load of the main PA is $2R_{opt}$. The main PA is configured to output a half of its maximum RF current $I_{max}/2$. Thus, the maximum RF voltage amplitude, equal to the supply voltage V_{DD}, is again realized at the main PA output, and the maximum PA efficiency is again achieved. Between 0 and 6 dB PBO, digitally reconfiguring the main and auxiliary PAs ensures that this PA follows the 2-way Doherty PA operation with the supply voltages of V_{DD} and the maximum output currents of I_{max}.

A half-V_{DD} mode by changing both PA supplies to $V_{DD}/2$ using the Class-G operation (Figure 46c and Figure 46d) is introduced to extend the PA efficiency enhancement beyond 6 dB PBO as offered by a classic 2-way Doherty PA. At 6 dB PBO in half-V_{DD} mode, both PAs are programmed to output the half of their maximum RF currents $I_{max}/2$. Since the two PAs have identical RF output currents, the same as PA operation at 0 dB PBO in full-V_{DD} mode, both PAs again have the same effective load impedance of R_{opt}. The output RF voltages for both PAs are then maximized, equal to their supply voltages $V_{DD}/2$. As a result, the maximum PA efficiency is achieved at 6 dB PBO in the half-V_{DD} mode. Moreover, the PA maintains the same P_{out}, i.e., 6 dB PBO, ensuring continuous P_{out} during supply mode switching. Between 6 and 12 dB PBO, the PA operates as a 2-way Doherty PA with the supply voltages of $V_{DD}/2$ and the maximum RF currents of $I_{max}/2$. At 12 dB PBO, the auxiliary PA is turned off and the main PA outputs a quarter

of its maximum RF current (I_{max}/4). The load of the main PA is $2R_{opt}$ again, the same as 6 dB PBO in the full-V_{DD} mode. Therefore, the RF voltage amplitude at the main PA output reaches its maximum value as its supply V_{DD}/2, and maximum PA efficiency is again achieved at 12 dB PBO.

In summary, the introduced hybrid Class-G Doherty PA architecture extends the PA PBO efficiency enhancement of a symmetric 2-way Doherty PA from 6 dB to 12 dB using only one 2-level (1-bit) Class-G supply modulator. It achieves the PA PBO efficiency behavior of a 3-stage Doherty PA [36] but without any extra complexity in the input or output passives.

The Class-G Doherty hybrid operation can also be interpreted using load-line analysis (Figure 47). Since most single-branch RF power DACs exhibit Class-B-like PBO efficiency behavior, Class-B operation is assumed for the main and auxiliary PAs. In each supply mode, the effective load impedance seen by the main (auxiliary) PA is modulated from R_{opt} (R_{opt}) to $2R_{opt}$ (open) in the load-line plots due to the active load pull. The Class-G supply switching in the load-line plots is explained as follows. At 6 dB PBO (full-V_{DD} mode), the PA P_{out} equals the main PA P_{out}, proportional to the area sum of M1, M2, and M3, as $I_{max} \times V_{DD}$. On the other hand, at 6 dB PBO (half-V_{DD} mode), the PA P_{out} equals the sum of the main and auxiliary PA P_{out} values. The main PA P_{out} is proportional to the M1 and M2 area sum ($0.5 \times I_{max} \times V_{DD}$), while the auxiliary PA P_{out} is proportional to the A1 area ($0.5 \times I_{max} \times V_{DD}$). Thus, the PA P_{out} at 6 dB PBO (half-V_{DD} mode) is proportional to

$I_{max} \times V_{DD}$, equal to the PA P_{out} at 6 dB PBO (full-V_{DD} mode). This ensures no P_{out} discontinuity when switching between full-V_{DD} and the half-V_{DD} modes at 6 dB PBO. Moreover, the load-line analysis shows that the introduced Class-G Doherty PA can be extended to even deeper PBO levels, e.g., 18 dB or more, by adding more Class-G supply levels. This corresponds to adding more "zigzag" and "parallel" load lines for the main and auxiliary PAs, respectively (Figure 47). In practice, such extension is limited by the PA knee voltage, the supply modulator, and the power consumption of the overhead circuits at low P_{out} levels, etc.

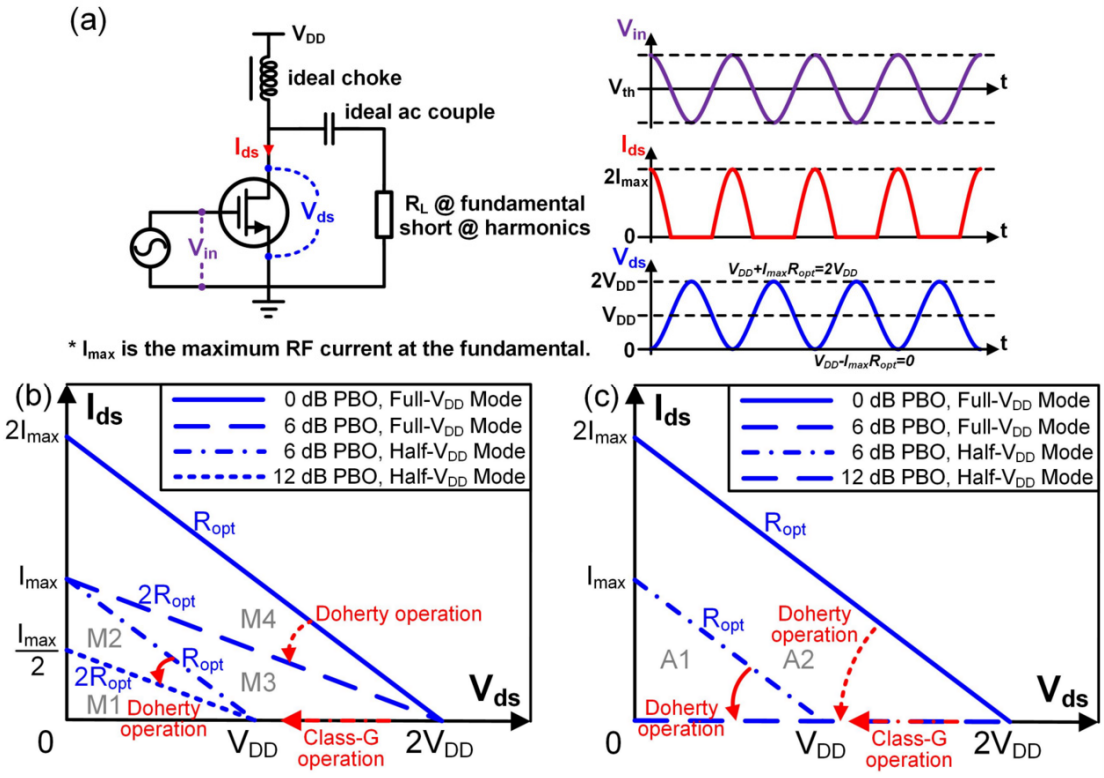


Figure 47 – The load-line analysis for the introduced hybrid Class-G Doherty PA operation. (a) The voltage and current definitions with their waveform illustrations at peak P_{out}. (b) The main PA's load-line behavior. (c) The auxiliary PA's load-line behavior. Class-B operation with zero knee voltage is assumed for both PAs. PA P_{out} can be calculated based on the area enclosed by the load lines and the I_{ds} and V_{ds} axes.

In summary, the introduced hybrid Class-G Doherty PA architecture fully exploits the advantages of both Class-G and Doherty PA techniques. PA efficiency for a given supply voltage is enhanced up to 6 dB PBO by the Doherty operation, while the 2-level Class-G supply switching extends the total efficiency-enhancement range from 6 dB to 12 dB PBO. Note that although a 3-stage Doherty PA also can enhance PA efficiency up to 12 dB PBO, it requires substantially more complicated Doherty input/output passive networks. In addition, by utilizing the Doherty PA operation, only two supply voltages are used to cover 12 dB PBO. In contrast, the multi-level outphasing PA requires four supply voltages for 12 dB PBO [69], resulting in significant overhead in its supply modulator and regulator designs.

4.1.2 Hybrid Class-G Doherty PA Implementation

As a proof of concept, a fully integrated hybrid Class-G Doherty PA is implemented in a standard 65 nm bulk CMOS process. The schematic details are shown in Figure 48.

4.1.2.1 Active Circuit Designs

The PA adopts the digital polar Doherty PA architecture [75]. The main and auxiliary PAs are implemented as RF power DACs each consisting of 5-bit binary-weighted thermometer-coded cascode Class-D^{-1} power cells. The PA is driven by the constant-envelope PM RF signal, and the AM is synthesized by dynamically activating the proper numbers of power cells using two 5-bit digital words. The digital Doherty PA

architecture offers the precise and flexible control of the two PAs' RF output currents for optimum Doherty operation in practice. The switching-mode PA cells provide high peak PA efficiency, and the PBO efficiency is enhanced up to the deep (12 dB) by the Class-G Doherty operation.

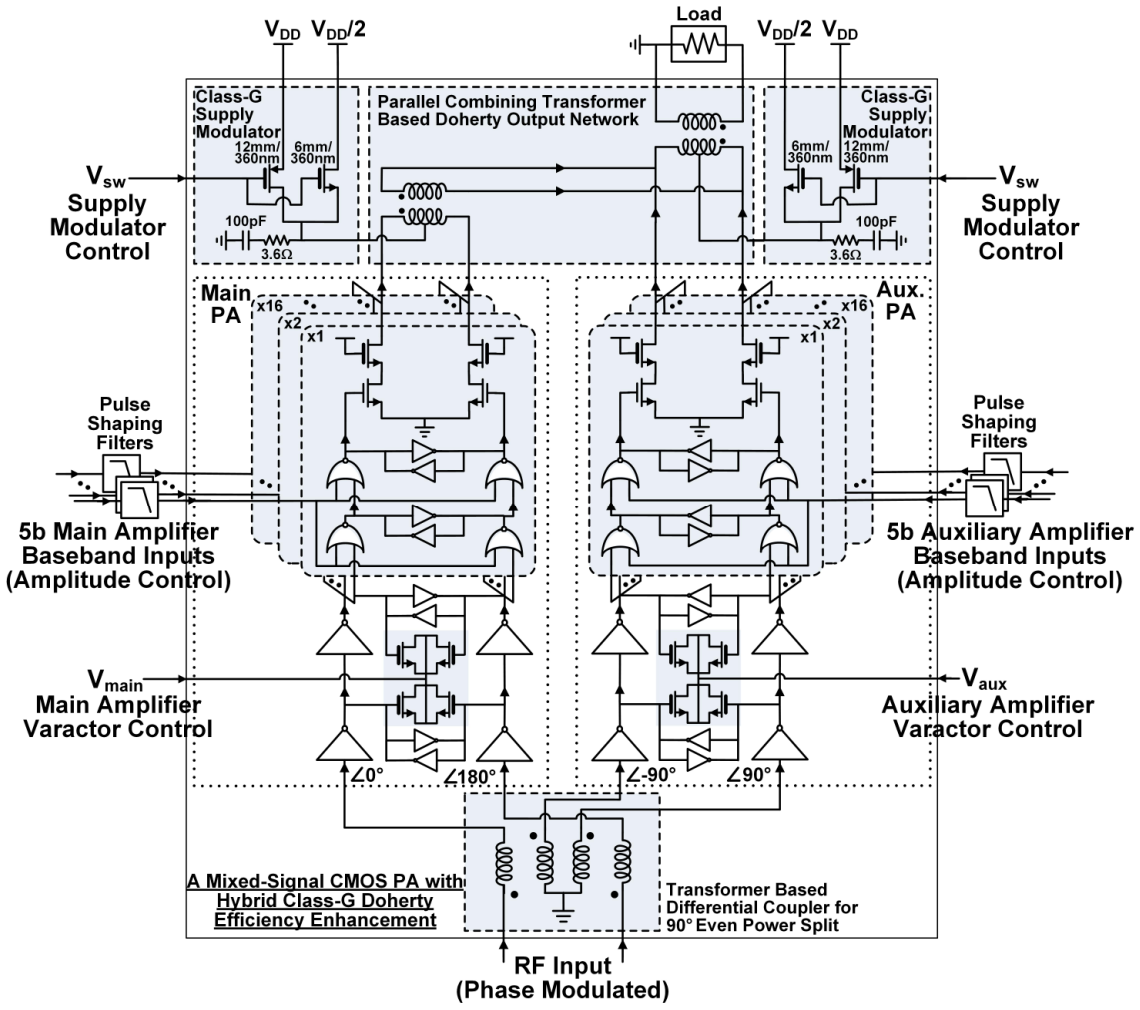


Figure 48 – Schematic of the proof-of-concept Class-G Doherty PA design fully integrated in a standard 65 nm bulk CMOS process.

The PA cores are driven by four-stage digital drivers. The last two stage drivers are 5-bit binary-weighted NOR gates (Figure 48). When certain PA cells are disabled during

PBO, their corresponding last two-stage drivers are turned off to save power. Cross-coupled inverters are placed in the driver chain to improve common-mode stability and differential-mode signaling. The supplies of the last two stages of cross-coupled inverters are fed from the internal nodes of the NOR gates to ensure proper operation while the branch is off (Figure 49). The digital baseband amplitude controls are filtered and pulse-shaped to suppress spurs and sampling images.

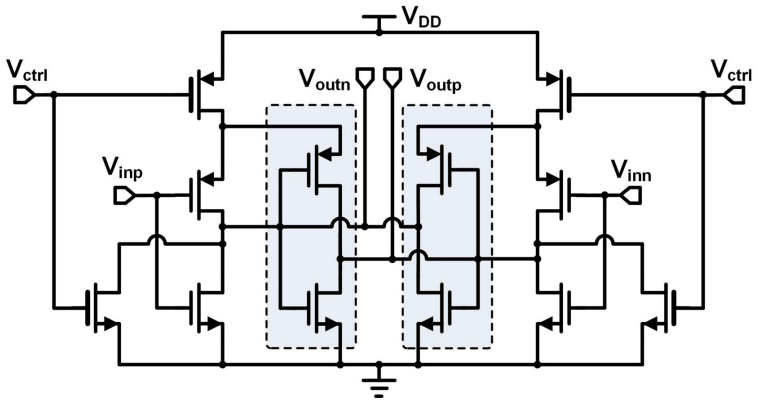


Figure 49 – Schematic of the NOR gate digital driver circuit, and similar circuits are used for the last two stage drivers. The cross-coupled inverters are highlighted in the dotted boxes.

The Class-G supply modulators use a 12 mm/360 nm PMOS switch in the full-V_{DD} (3V) path and a 6 mm/360 nm NMOS switch in the half-V_{DD} (1.65V) path (Figure 48). The simulated on-resistances for the PMOS and NMOS switches are 0.34Ω and 0.38Ω (Figure 50a), ensuring negligible PA efficiency degradation (Figure 50b). The two supply values obviate the need of complementary switches (Figure 50). This simplifies the supply modulator logic and ensures easy timing control and reduced dynamic power consumption. The supply modulator output is smoothed by series R-C damping legs (Figure 48) [69],

which are carefully designed by considering the supply waveform smoothing, modulation speed, chip area, and charging/discharging energy loss during supply switching. The damping leg can reduce the amplitude of the switching glitch at the Class-G supply modulator output, allowing higher modulation rates. However, it demands extra chip area and the charging/discharging power ($2\times(0.5\times CV_{DD1}^2-0.5\times CV_{DD2}^2)\times$switching rate). One should ensure that the charging/discharging power occupies only a small portion of the total PA dc power.

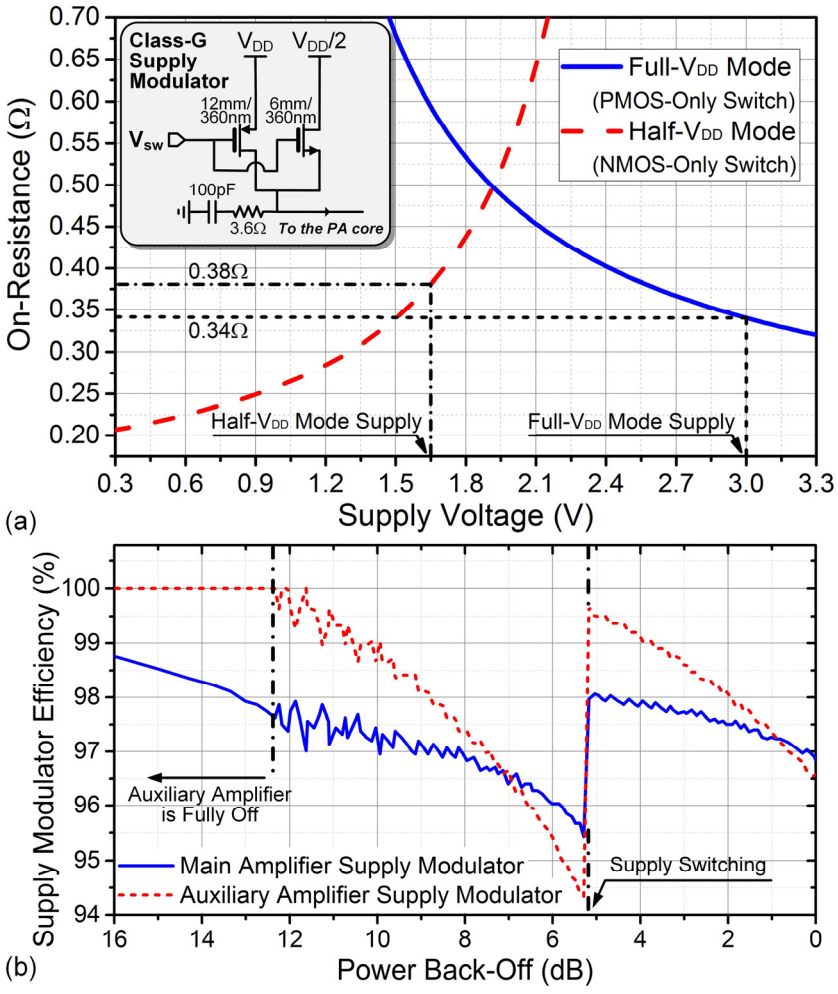


Figure 50 – (a) Simulated on-resistance for the Class-G supply modulator. (b) Simulated efficiency for the supply modulators of the main and auxiliary amplifiers.

4.1.2.2 Passive Network Designs

Transformer-based Doherty input and output passive networks are employed to provide low loss, wide bandwidth, and compact footprints (Figure 48). A 6-port folded-transformer differential 90° coupler is used as the Doherty input network. Within only one inductor footprint, it converts the differential RF input to two outputs with an equal power split and a 90° phase difference. The Doherty output network adopts a PCT structure. It achieves the Doherty LM, power combining, differential-to-single-ended conversion and impedance down-scaling within two inductor footprints. To accommodate the auxiliary PA's supply modulator, a 400-μm interconnect is required to connect the two transformers. Since the interconnect's parasitic inductance is undesired in the PCT Doherty output network [75], it is implemented with a twisted-wire configuration (Figure 51a). In addition, the ground ring is enhanced for the 1:2 output balun to minimize its return-path loss (Figure 51a).

Next the PE of the PCT Doherty output network in the context of the Class-G operation is analyzed. The analyses in [75] show that the PE of the PCT Doherty PA output network decreases during PBO until the auxiliary PA is fully turned off. This is first because the main PA output signal path has more loss than the auxiliary PA due to the output impedance inverter, and the main PA contributes more P_{out} than the auxiliary PA during PBO. Secondly, the output impedance inverter performs a larger impedance transformation during PBO and results in more passive loss. Since the main and auxiliary

PAs have equal RF output currents at 6 dB PBO in half-V_{DD} mode ($I_{main} = I_{aux} = I_{max}/2$) just like the 0 dB PBO case in full-V_{DD} mode ($I_{main} = I_{aux} = I_{max}$), these two PBO points have the same main/auxiliary RF output current ratio and thus the same Doherty active LM with the same PE. The simulation verifies that the output network PE is restored to its peak at 6 dB PBO in half-V_{DD} mode by the Class-G operation (Figure 51b). In contrast, a conventional Doherty PA does not have such PE enhancement after 6 dB PBO. This output network PE behavior and the hybrid Class-G Doherty active operation enhance the PA efficiency up to the deep PBO.

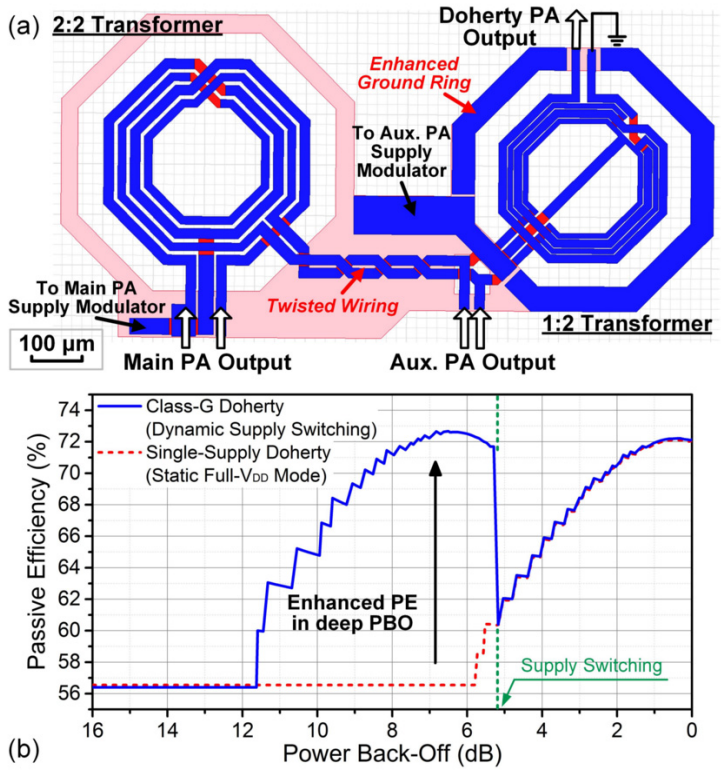


Figure 51 – (a) The Doherty output passive network implemented in hybrid Class-G Doherty PA. (b) Simulated PE of the PCT Doherty output network for the hybrid Class-G Doherty operation and the conventional Doherty operation. The passive structures are 3D EM-modelled, and the transistor-level PA cells program the PBO and provide the parasitic loadings.

4.1.3 CW Measurement Results

The PA is implemented in a standard 65 nm bulk CMOS process and occupies 1.47×2.15 mm^2 (Figure 52). The main and auxiliary Class-G supply modulators each occupy 0.05 mm^2. The supply of the PA core is 3 V for the full-V_{DD} mode and 1.65 V for the half-V_{DD} mode, and the driver supply is 1.2 V. The half-V_{DD} supply of 1.65V is to compensate the non-zero PA knee voltage.

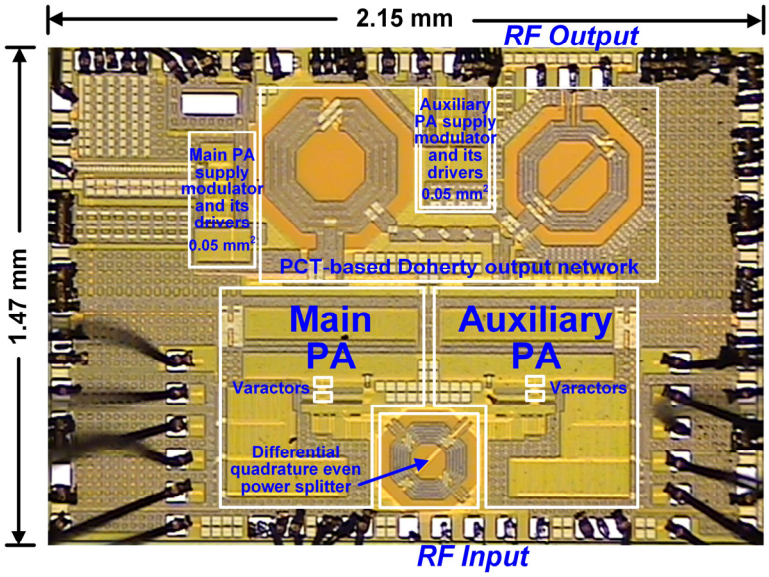


Figure 52 – Chip microphotograph.

The PA is first characterized in the CW measurements at 3.71 GHz. When all the power cells are on, the PA achieves +26.7 dBm peak P_{out} with 40.2% peak DE and 16 dB power gain. To measure the PA PBO performance, the amplitude digital control codes for main and auxiliary PAs are swept in both full-V_{DD} and half-V_{DD} modes (Figure 53). Each data point in Figure 53 represents one main/auxiliary PA digital control code setting in the

given supply voltage mode. At each P_{out} level, the code for the maximum efficiency can be selected as the EOCS for output amplitude interpolation. The measured DE at 6 and 12 dB PBO are 37% and 26.2%, which are 1.84× and 2.61× enhancement over Class-B PA operation. A maximum 2.66× efficiency enhancement is achieved at 11.5 dB PBO. These results demonstrate the superior performance of the introduced hybrid Class-G Doherty PA architecture for PA PBO efficiency enhancement.

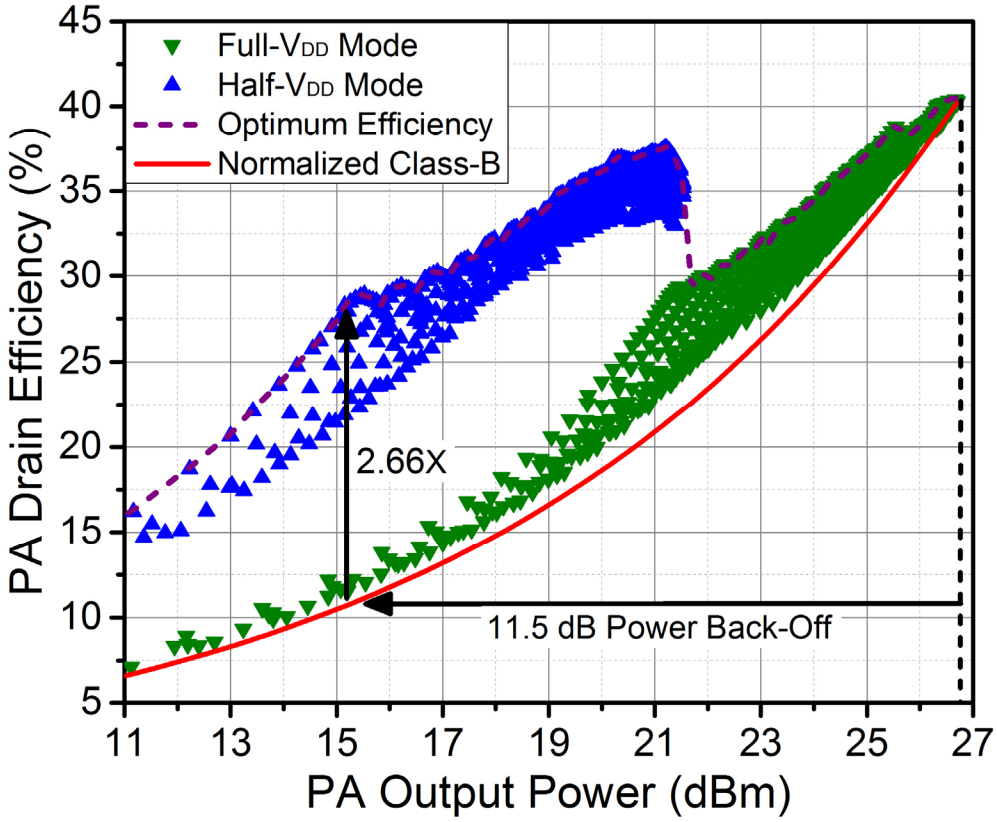


Figure 53 – Measured PA DE at 3.71 GHz versus PA P_{out} in CW measurement.

Note that there is a PA efficiency jump at the supply mode transition around 6 dB PBO (Figure 53). This is due to the increased output network PE when switching from full-V_{DD} to half-V_{DD} mode (Section 4.1.2.2). However, although the 6 dB PBO (half-V_{DD}

mode) exhibits the same high PE as the 0 dB PBO (full-V_{DD} mode), the measured PA efficiency at 6 dB PBO (half-V_{DD} mode) is slightly lower than that at 0 dB PBO (full-V_{DD} mode). This is mainly because of the lower PA active circuit efficiency due to the non-zero PA knee voltage and the suboptimal cascode PA operation in the half-V_{DD} mode.

4.2 Mixed-Signal Linearization and CW AM-PM Measurement

4.2.1 Amplitude Distortion Minimization in the Hybrid Class-G Doherty PA

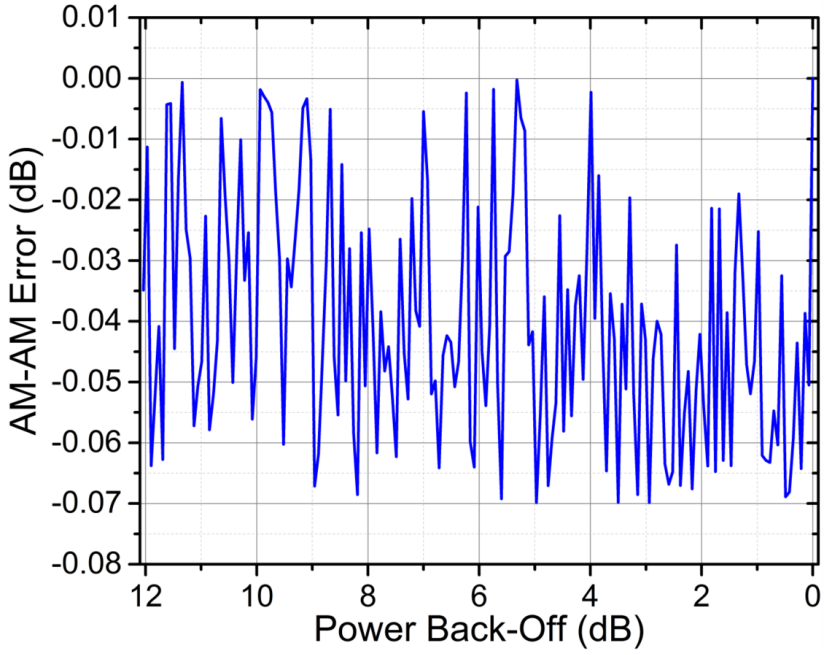


Figure 54 – Measured AM-AM error for the EOCs up to 12 dB PBO.

The EOCs are employed for the main and auxiliary power DACs in the hybrid Class-G Doherty PA. The desired output signal amplitude is interpolated with the maximum PA PBO efficiency, and the PA AM-AM distortions are minimized in the hybrid Class-G Doherty operation. Moreover, using 5-bit binary power DACs for the

main/auxiliary PAs provide a measured maximum P_{out} quantization error of less than 0.07 dB within 12 dB PBO (Figure 54), ensuring an accurate signal amplitude interpolation with a fine resolution. This error can be further reduced by increasing the bit numbers in the power DACs. In contrast, extra design complexities are needed to compensate for the gain discontinuity in the analog Class-G PA [28].

4.2.2 Phase Distortions in the Hybrid Class-G Doherty PA

Besides the AM-AM nonlinearity, the AM-PM nonlinearity is another critical design aspect. Typically, there are four sources for the AM-PM nonlinearity. 1) The AM-PM of the drivers. This is not significant in the hybrid Class-G Doherty PA (Figure 55), since the drivers process a constant-envelope PM signal in this polar PA. 2) The nonlinear gate capacitance C_{gs} of the common-source transistors in the PA core. This factor also contributes negligible phase distortions again due to the constant-envelope PM driving signal in the digital PA. 3) The RC parasitic pole at the source of the common-gate transistor in the PA core. For a digital PA, although certain power cells are turned off during PBO, the ratio between the activated common-source and the common-gate transistors remains constant. Therefore, this RC parasitic pole also contributes negligible PA AM-PM distortions. 4) The complex pole at the PA output. In silicon-based PAs, the PA load impedance is often designed to be inductive and to resonate with the parasitic capacitance at the PA drain output to optimize the PA performance. However, this nonlinear PA output

drain parasitic capacitance varies substantially during PBO operation. This shifts the frequency of the PA output complex pole and leads to PA phase distortions.

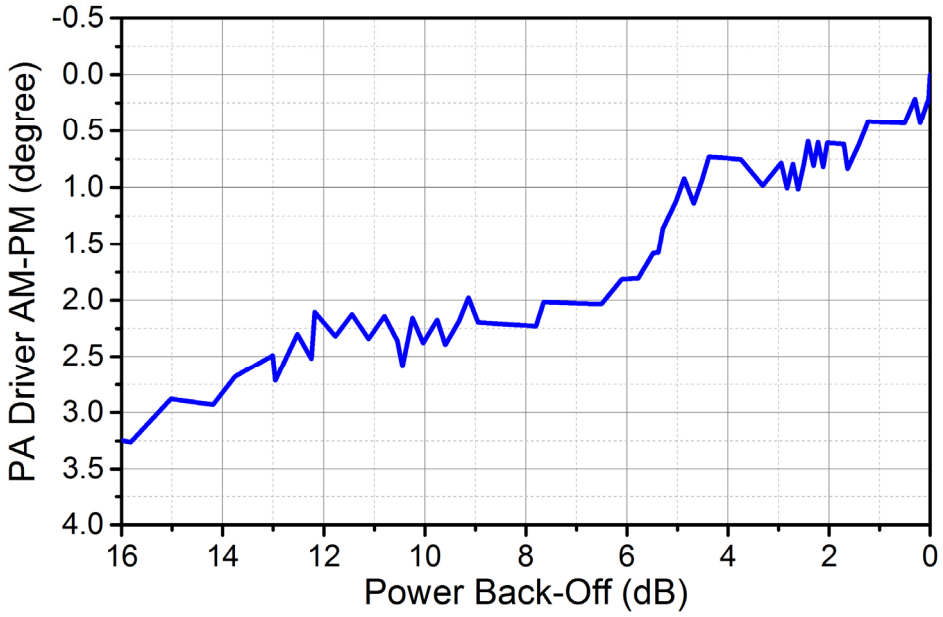


Figure 55 – Simulated AM-PM response of the PA digital driver chain (from Doherty PA input to Class-D^{-1} PA core input).

The nonlinear PA output drain parasitic capacitance includes both the gate-drain capacitance C_{gd} and the junction capacitance C_{bd} of the common-gate transistor M_1 (Figure 56). C_{gd} depends on M_1 operating condition, and a substantial C_{gd} increase happens when M_1 enters the triode region [86]. Therefore, the time-averaged C_{gd} during the PA large-signal operation can vary significantly for different PA output drain voltage swings. In general, a larger drain voltage swing leads to a larger effective C_{gd} due to the increased M_1 triode operation (Figure 56). Moreover, the PA supply voltage also affects the time-averaged C_{gd}. For a given voltage swing, a lower supply leads to a higher equivalent C_{gd} also due to the increased M_1 triode operation (Figure 56).

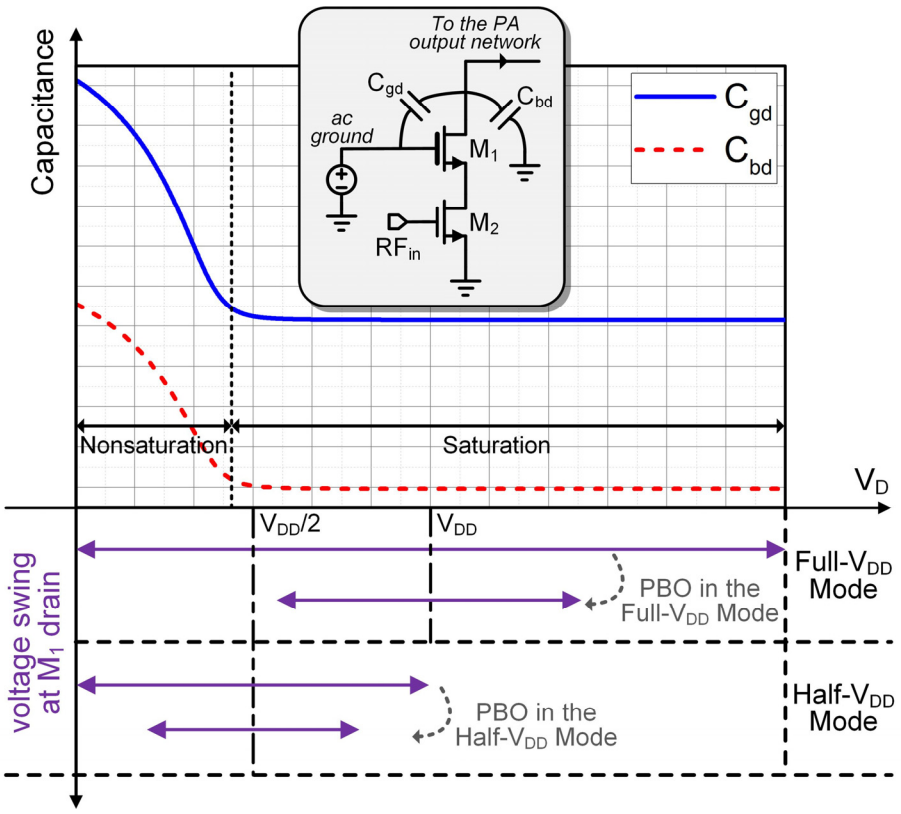


Figure 56 – Conceptual illustration for the drain output nonlinear capacitance of a cascode PA during PBO and Class-G supply switching operation. The knee voltage is assumed to be zero.

In parallel, the M_1 drain junction capacitance C_{bd} shows similar nonlinear behavior as C_{gd}, i.e., exhibiting a larger capacitance for a lower drain voltage (Figure 56). It shows a larger time-averaged capacitance for a larger drain voltage swing and/or a lower supply voltage.

The AM-PM behavior of the Class-G Doherty PA is explained as follows. From 0 dB to 6 dB PBO in the full-V_{DD} mode (or from 6 dB to 12 dB PBO in the half-V_{DD} mode), the RF voltage swing at the main PA output is kept approximately constant, while the auxiliary PA output swing decreases. Thus, the averaged nonlinear capacitance at the main

PA output remains almost the same, while it decreases at the auxiliary PA output, resulting in its phase leading behavior in PBO. After the power combining, the Doherty PA output thus shows an increased leading phase during the PBO in both supply modes. In addition, when the supply voltage is lowered, the main and auxiliary PA nonlinear output capacitances increase, the 6 dB PBO point (half-V_{DD} mode) thus shows a phase jump as a lagging phase. Note the 6 dB PBO (half-V_{DD} mode) has a lagging phase compared with the 0 dB PBO (full-V_{DD} mode), also due to the nonlinear output capacitance.

This analysis for the Class-G Doherty PA aligns well with the AM-PM measurement (Figure 57).

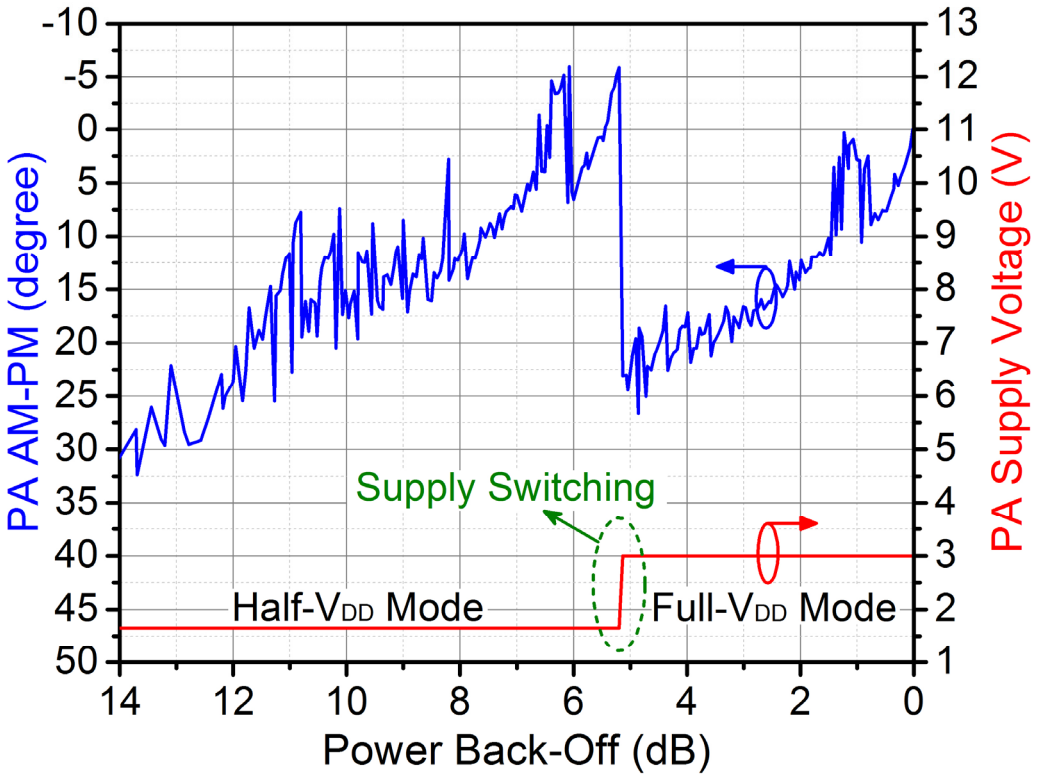


Figure 57 – Measured total PA AM-PM response for the efficiency-optimum codes at 3.71 GHz.

4.2.3 Introduced AM-PM Linearization Technique

Multiple PA AM-PM linearization techniques have been reported. PMOS devices [57],[87] and a MOS-resistor-based distortion canceller [88] can be added at the PA input. Tuned-varactors at the PA output are used for phase compensation [89]. However, it is challenging for these techniques to achieve a good AM-PM compensation over a wide power range, especially when the AM-PM behavior is not monotonic with the Class-G operation (Figure 57). Moreover, adding varactors at the high-voltage-swing PA outputs may directly compromise other PA performance such as P_{out}, efficiency, and PA reliability. In addition, the PA drain nodes experience different output voltage swings during PBO. Since the varactors have different effective capacitances at different PA output voltage swings, controlling those varactors needs complicated P_{out}-dependent LUTs.

We employ tuned varactors at the digital drivers' outputs for dynamic AM-PM compensations. These varactors can change the capacitive loadings of the digital drivers and adjust their delays, which then change the PA output phases. In the implementation, the varactors and digital drivers are properly sized to allow the complete compensation of the PA phase distortions. The varactors are placed at the outputs of the 1^{st}- and 2^{nd}-stage digital drivers, and the varactor control voltages in the main and auxiliary paths are independent, shown as V_{main} and V_{aux} in Figure 48.

The introduced AM-PM linearization technique offers the following advantages. First, it has negligible effects on the PA P_{out} and efficiency, since the varactor-based delay tuning will not affect the digital drivers' output voltage swing, as long as the drivers are not slew-rate limited. This orthogonality between the P_{out} and phase compensation is critical to ensure no PM-AM errors during AM-PM compensation. Moreover, this technique also avoids the PA reliability degradation. The digital drivers use thin-oxide 1.2-V devices, and the varactors use thick-oxide 2.5-V devices. Finally, the varactors at the drivers' outputs always have a constant-envelope PM driving signal during PBO, significantly simplifying the phase compensation LUT.

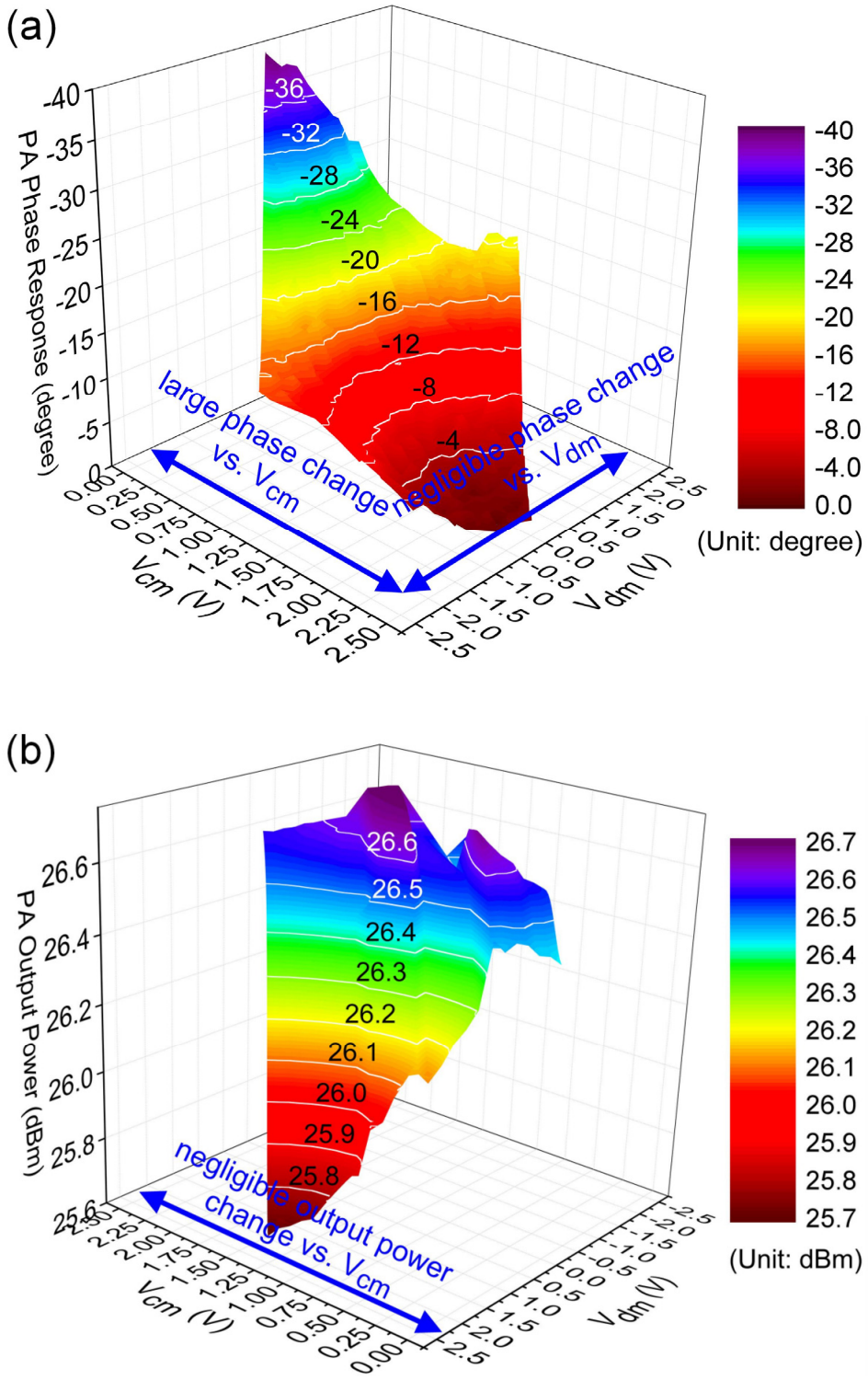
Applying additional DPD can further linearize the PA. Note that the PA linearized by the introduced mixed-signal technique demands DPD signal processing with reduced bandwidth and power consumption.

4.2.4 CW Phase Measurement Results

This section demonstrates the PA performance when tuning the varactor control voltages in the CW measurements. The common-mode and differential-mode varactor control voltages V_{cm} and V_{dm} are defined as $V_{cm} = (V_{main}+V_{aux})/2$ and $V_{dm} = V_{main}-V_{aux}$.

Figure 58a shows the measured PA output phase with respect to V_{cm} and V_{dm} when all the power cells are on at 3.71 GHz. The PA output phase can be adjusted up to 39° by

tuning V_{cm} (Figure 58a), while V_{cm} has marginal effects on the PA P_{out} and efficiency (Figure 58b and Figure 58c).



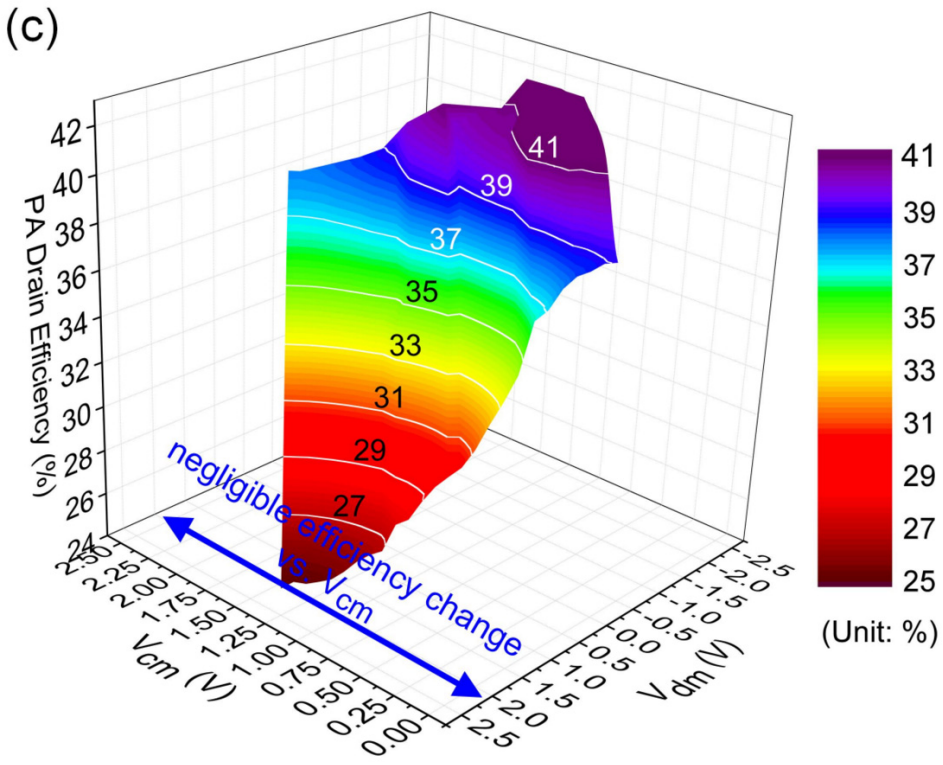


Figure 58 – Measured (a) PA phase response, (b) P_{out}, and (c) DE when adjusting the varactor control voltages with all the power cells on at 3.71 GHz.

4.3 Doherty PA RF Bandwidth Extension and CW Bandwidth Measurement

4.3.1 RF Bandwidth Extension Technique for Doherty PA

The frequency-dependent input and output networks typically limit the RF bandwidth of the Doherty PAs. The state-of-the-art P_{out} 1-dB bandwidth for the fully-integrated CMOS Doherty PAs is around 25% with transformer-based passive networks [43], [75]. Multiple bandwidth extension techniques have been studied with discrete Doherty PAs. The work in [90] extends the Doherty PA bandwidth by changing the phase difference of the two PA paths. The introduced design demonstrates this concept in a fully

integrated CMOS Doherty PA for the first time and achieve the best reported 1-dB P_{out} bandwidth (48%) for a CMOS Doherty PA.

Intuitively, the PA performance at the offset frequencies can be recovered by compensating the phase shifts of the frequency-dependent passives. At an operating frequency higher than the center frequency, the 6-port folded-transformer differential coupler presents <90° phase shift at the auxiliary PA input, and the output C-L-C π-network shows >90° phase shift at the main PA output [75]. To balance this phase difference and achieve a constructive P_{out} combining, the auxiliary path should be delayed with respect to the main path. This can be achieved by increasing V_{dm}, i.e., increasing V_{main} and/or decreasing V_{aux}. Note that this RF bandwidth extension (tuning V_{dm}) is orthogonal to the introduced AM-PM linearization (tuning V_{cm}).

4.3.2 CW Measurement for Doherty PA RF Bandwidth Extension

When all the power cells are turned on, the varactor control voltages are swept at three RF frequencies of 3.71, 4.3, and 5 GHz, and the optimum varactor settings at those three frequencies are determined (Figure 59). Figure 58a shows that the P_{out} 1-dB bandwidth is extended from 1.08 GHz (32% fractional bandwidth) to 1.80 GHz (48% fractional bandwidth) by changing the varactor setting. Note that this is the best reported P_{out} 1dB bandwidth among fully integrated CMOS Doherty PAs. The PA DE at 4.3/5.0GHz is improved from 25.5%/5.3% (varactor setting #1) to 33.3% (varactor setting #2)/24.0%

(varactor setting #3) (Figure 59b). Furthermore, the PA PBO efficiency enhancement by the Class-G Doherty operation is also maintained over this extended RF bandwidth. Figure 60 shows the measurement results at 4.3 GHz and demonstrates 2.84× PA DE improvement at 12 dB PBO.

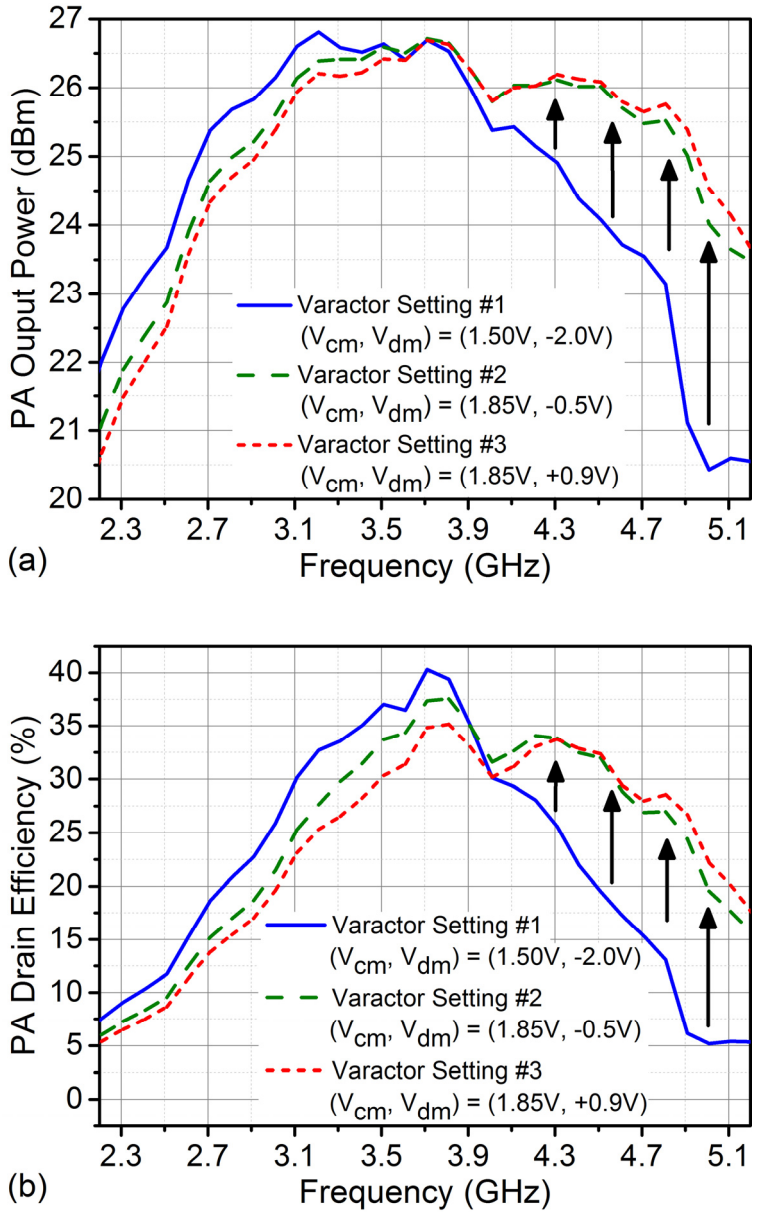


Figure 59 – Measured (a) PA P_{out} and (b) DE for different varactor settings when all the power cells are on at different RF frequencies.

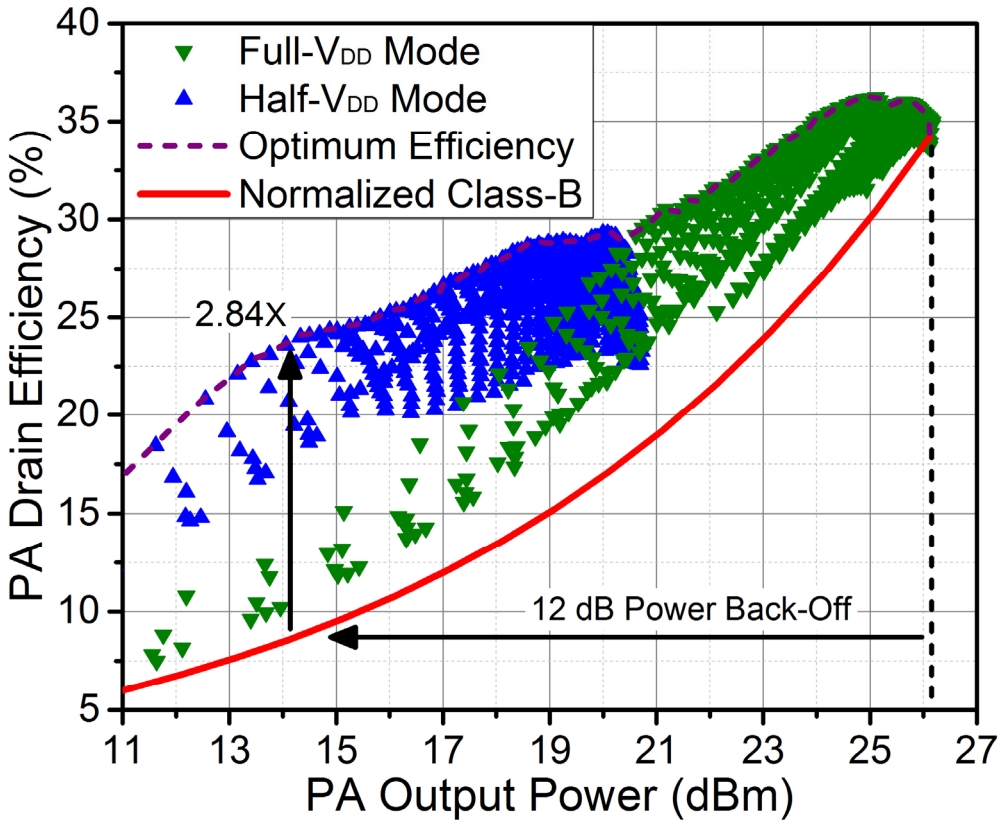


Figure 60 – Measured PA DE at 4.3 GHz showing Class-G Doherty operation and substantial PA PBO efficiency enhancement.

The RF bandwidth extension is largely achieved by tuning V_{dm}. This is verified by comparing the optimum varactor settings (Figure 59). Moreover, the measurement results show that a larger V_{dm} is desired at a higher frequency, aligning well with the theoretical analysis in Section 4.3.1.

4.4 Modulation Measurement Results

This section presents the modulation test results with 1 MSym/s 16-QAM signals (PAPR = 5.4 dB) and 10× oversampling. No additional DPD or feedback linearization is applied.

4.4.1 PA Dynamic AM-PM Linearization

To achieve real-time AM-PM linearization in the modulation tests, the PA output phase is dynamically adjusted by tuning V_{cm} based on the phase compensation LUT generated in the CW measurements, while V_{dm} is kept constant (Figure 61). The varactor control signals are synchronized with other signal paths, i.e., the RF power DAC digital control, the Class-G supply modulator digital control, and the RF input PM signals, using a shared timing flag signal. Figure 62 compares the measurement results before and after applying the dynamic AM-PM linearization. The results show that 3.3 dB EVM and 2.8 dB ACLR improvements are achieved with negligible effects on the PA P_{out} and efficiency. After the linearization, the PA achieves +20.8 dBm peak average P_{out}, 28.8% DE with −24 dB rms EVM, and −28.8 dB ACLR at 3.71 GHz.

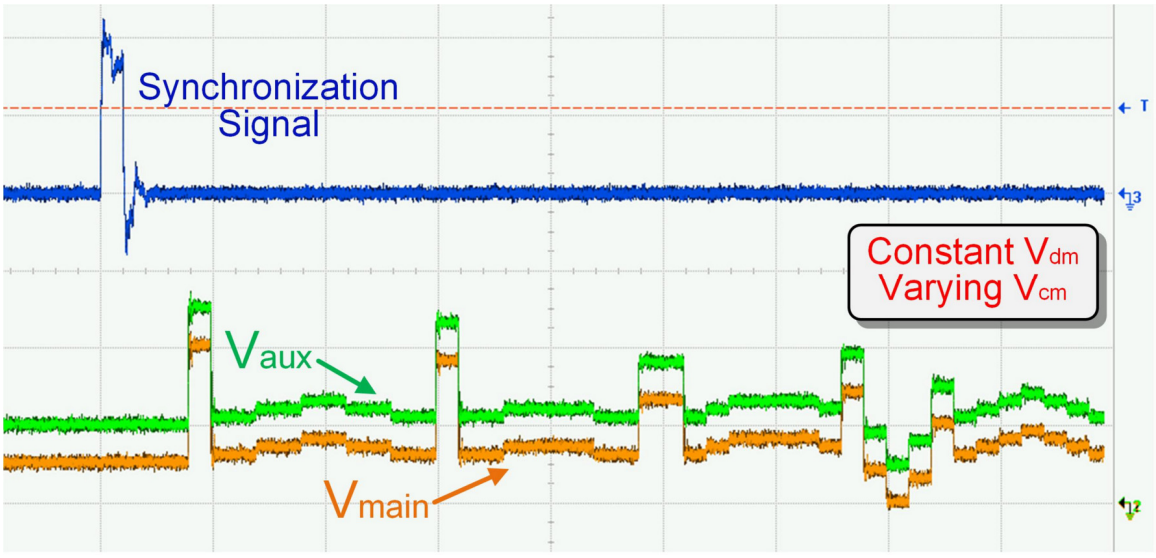


Figure 61 – Measured dynamically tuned varactor control voltages for AM-PM linearization in modulation measurements.

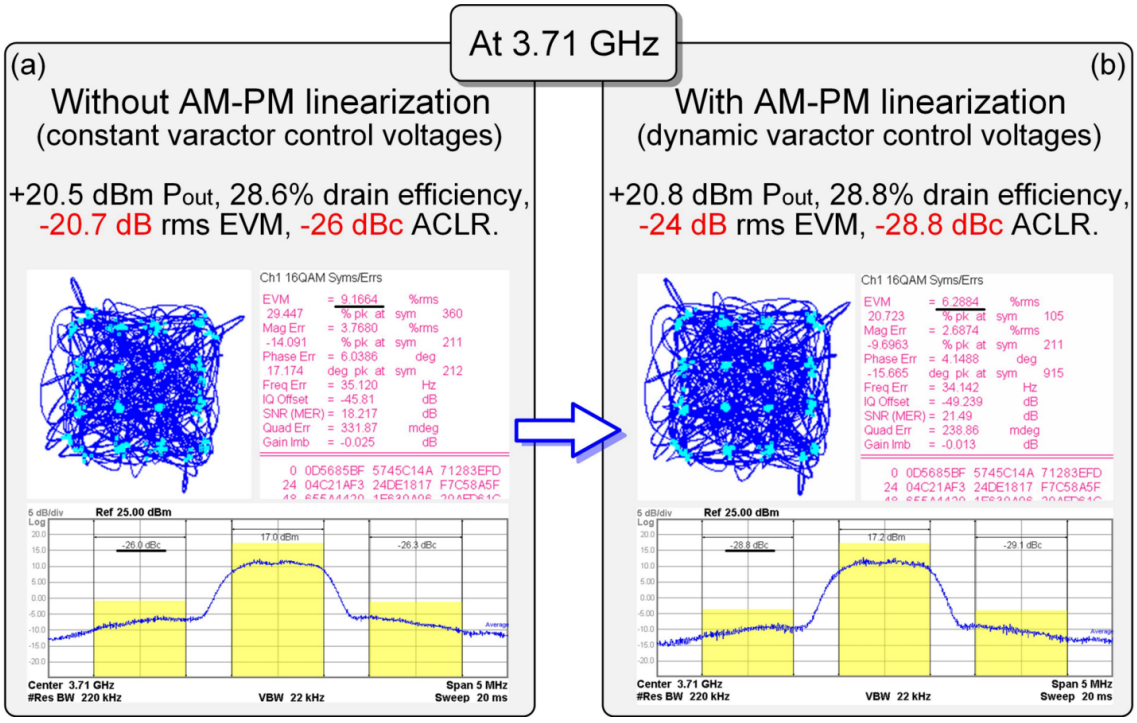


Figure 62 – Measured PA performance at 3.71 GHz (a) with and (b) without AM-PM linearization.

4.4.2 Broadband Doherty PA Operation

The Doherty PA bandwidth extension technique and the reprogrammable main/auxiliary power DACs' digital controls enable a robust broadband Doherty operation. At 4.3 GHz, if the EOCs and AM-PM compensation varactor controls optimized for 3.71 GHz are used, the PA shows compromised performance (Figure 63a). Using the EOCs and varactor controls optimized for 4.3 GHz, the PA P_{out}, efficiency and EVM are all enhanced (Figure 63b). At 4.3 GHz, the PA achieves +20.1 dBm peak average P_{out}, 27.2% DE with −30 dB rms EVM, and −34.7 dB ACLR. Thus, the mixed-signal reconfigurability of the PA substatially improves its frequency agility.

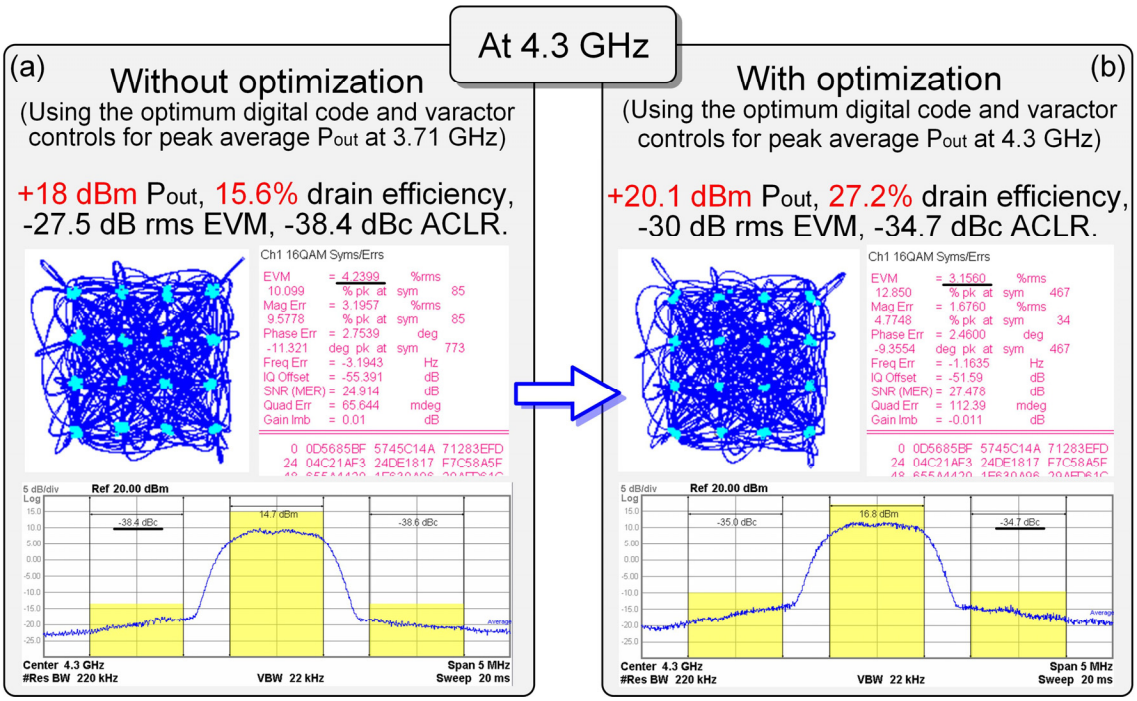


Figure 63 – Optimized broadband Doherty PA operation by mixed-signal reconfigurability.

4.4.3 PA Efficiency Enhancement in Deep PBO

Finally, the PA average P_{out} is gradually reduced to characterize its performance in deep PBO (Figure 64 and Figure 65). The Class-G Doherty PA with dynamic supply switching is compared against the single-supply Doherty PA (static full V_{DD}) and the normalized Class-B operation. Superior PA efficiency is achieved up to the deep PBO for the 16-QAM signal (Figure 64). At 3.71/4.3 GHz, the PA DE is 23.4/21.3% at +14.7/+14.3 dBm average P_{out} and 12.0/12.3% at +9.3/+8.4 dBm average P_{out}, which are 6.1/5.8 dB and 11.5/11.7 dB PBO from the maximum average P_{out}.

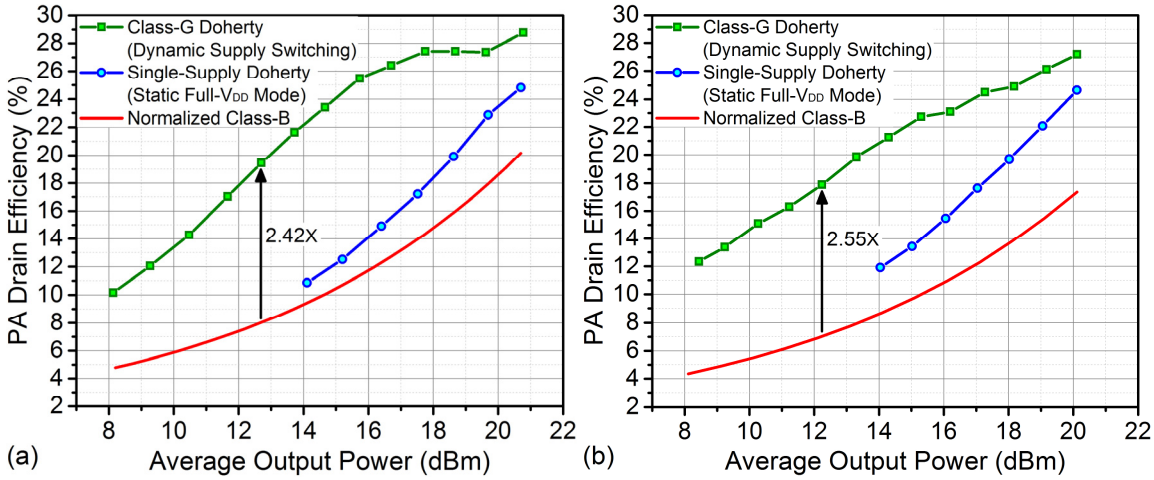


Figure 64 – Measured PA DE when backing-off the average P_{out} in modulation tests at (a) 3.71 GHz and (b) 4.3 GHz.

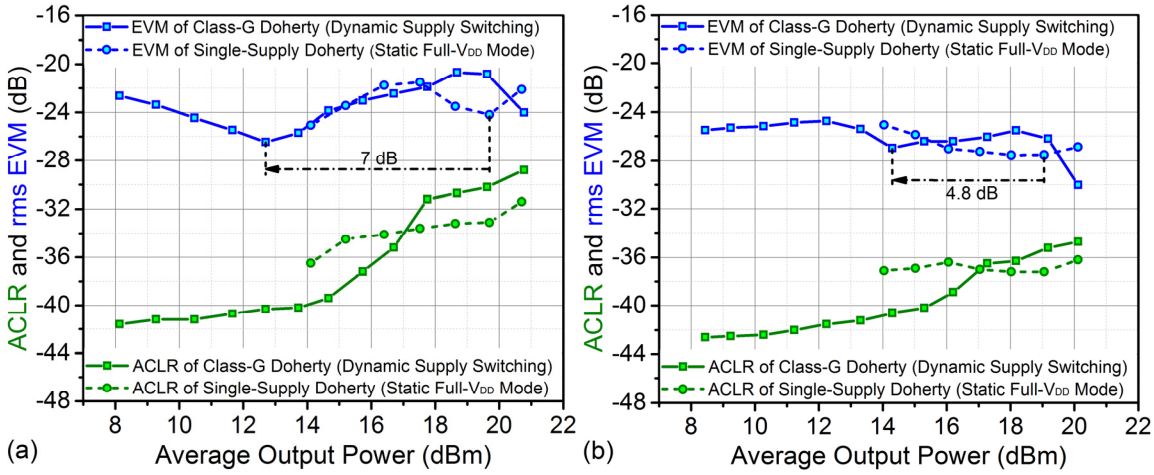


Figure 65 – Measured EVM (in-band linearity) and ACLR (OOB linearity) when backing-off the average P_{out} in modulation tests at (a) 3.71 GHz and (b) 4.3 GHz.

Figure 65 compares the PA EVM (in-band linearity) and ACLR (OOB linearity) performance. Up to the 12 dB PBO of the average P_{out}, the Class-G Doherty PA achieves <−20.7/−24.7 dB rms EVM and <−28.8/−34.7 dB ACLR at 3.71/4.3 GHz, demonstrating excellent in-band and out-of-band linearity behavior over the PBO. A small EVM increase is observed for the average P_{out} lower than +12.7/+14.3 dBm at 3.71/4.3 GHz. This is

mainly due to the power DACs' quantization errors at low P_{out} levels. Note that this EVM increase happens at a much lower P_{out} (approximately 6 dB additional PBO) in the Class-G Doherty PA compared with the single-supply Doherty PA, since the 1-bit Class-G operation allows for denser amplitude interpolation in deep PBO (Figure 53 and Figure 60). The further suppression of this EVM degradation can be achieved by increasing the RF power DACs' bit numbers. For both RF frequencies, in the high-power region (average P_{out} > +17 dBm), a marginal ACLR degradation (maximally 2.9 dB) is observed in the Class-G Doherty PA compared with the single-supply Doherty PA. This is because the dynamic supply switching is more frequent for the measured 16-QAM signal in this P_{out} region and thus contributes more noise.

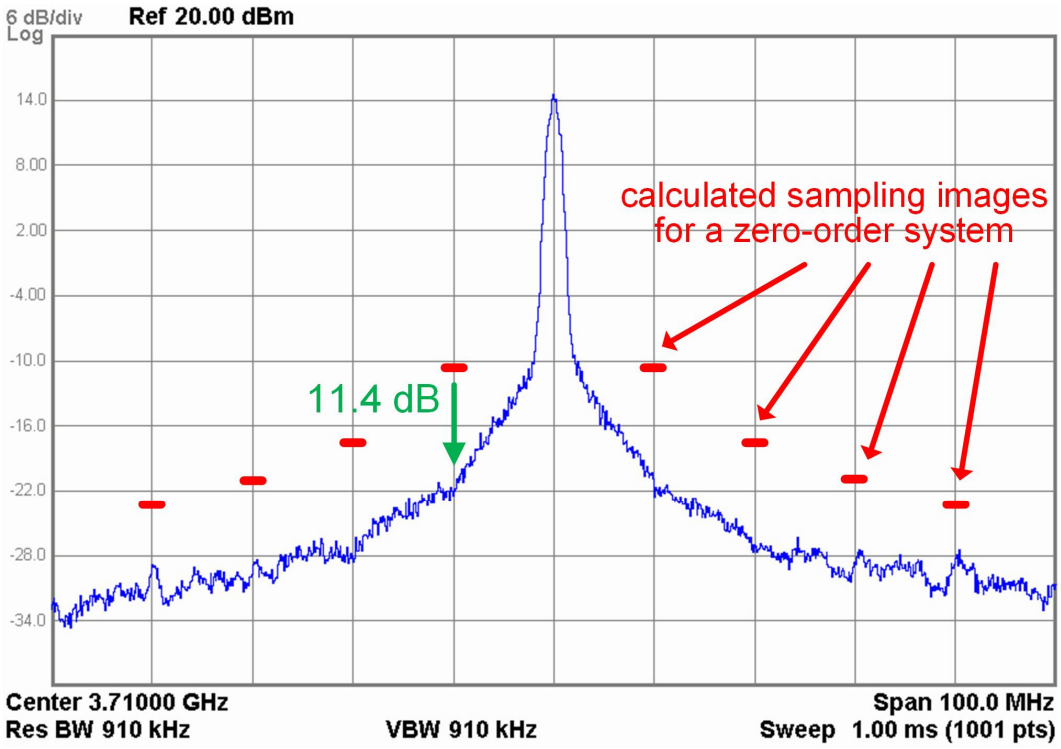


Figure 66 – Measured far-out-of-band spectrum for a +20.8 dBm 1MSym/s 16-QAM signal with 10× oversampling.

The measured far-out-of-band spectrum at the peak average P_{out} for the Class-G Doherty PA is shown in Figure 66. By pulse-shaping the amplitude digital control signals [9], the sampling images are all below −35dBc. The out-of-band noise and the ACLR degradation due to the supply switching can be potentially improved by further reducing the duration and amplitude of the glitches at the Class-G supply modulator output by design optimizations [91].

4.5 Summary

A mixed-signal CMOS PA with a hybrid Class-G Doherty architecture for PBO efficiency enhancement is presented. This design is particularly suitable for system-on-chip integrations in deep-submicron CMOS processes, where the digital controls with fine timing resolutions can be readily derived from the digital baseband [6]. Table 9 compares the introduced work with recently published CMOS PAs having PBO efficiency enhancement. Without using any switch at the PA RF output, the introduced PA demonstrates superior 1.8×/2.6× PA PBO efficiency enhancement at 6/12 dB PBO compared with the Class-B operation. In addition, with the reconfigurability of the Class-G Doherty PA, a mixed-signal linearization technique and Doherty PA RF bandwidth extension are demonstrated for both CW and dynamic modulation signals. The introduced PA achieves the best fractional bandwidth of 48% in all the reported CMOS Doherty PAs.

Table 9 – Performance comparison with other PBO efficiency enhanced CMOS PAs

	Freq. (GHz)	Peak P_{out} (dBm)	Peak η (%)	η at 6 dB PBO (%)	η at 12 dB PBO (%)	η Improve at 6 dB PBO †††	η Improve at 12 dB PBO †††	Average P_{out} (dBm)	Average η (%)	Relative η improve †††	EVM (dB)	ACLR (dB)	Area (mm^2)	CMOS Tech.	Mode Switch	PBO Efficiency Enhancement Technique
A. Shameli T-MTT Jan. '08*	0.9	27.8	34 (DE)	29.2† (DE)	26.4† (DE)	1.7×	3.1×	N.A.	26.5 (DE) WCDMA	N.A.	N.A.	N.A.	2.63	180 nm	dynamic	envelope tracking
D. Kang TMTT Oct. '13	1.85	30.2	48 (PAE)	46†,†† (PAE)	37†,†† (PAE)	1.9×	3.1×	26 16QAM	34.1 (PAE) 16QAM	1.15×	-31.1	-34.2	2.42	180 nm	dynamic	envelope tracking
W. Tai JSSC July '12	2.4	31.5	27 (PAE)	20 (PAE)	10.8† (PAE)	1.5×	1.6×	22.7 16QAM	12 (PAE) 16QAM	1.22×	-28	WiFi mask	3.12	45 nm	dynamic	outphasing + dc current switch
P. A. Godoy JSSC Oct. '12*	2.4	27.7	45.1 (PAE)	38† (PAE)	22† (PAE)	1.7×	2×	20.2 64QAM	27.6 (PAE) 64QAM	1.45×	-31.4	N.A.	4	65 nm	dynamic	outphasing + PA supply switch
B. Koo ISSCC '12**	1.95	30.5	42.1 (PAE)	24† (PAE)	33† (PAE)	1.1×	3.1×	28 WCDMA	36.4 (PAE) WCDMA	1.15×	N.A.	-35	2.7	180 nm	static	switch-based PA stage bypass
Y. Yoon T-MTT Jan. '12**	2.4	23.1	42 (PAE)	30.4† (PAE)	15.9† (PAE)	1.4×	1.5×	23.4 16QAM	18.5 (PAE) 64QAM	1.03×	-25	WLAN mask	0.88	180 nm	static	switch-based PA load reconfiguration
E. Kaymaksut JSSC Sept. '15**	1.9	28.0	34.0 (PAE)	25.5 (PAE)	19.7 (PAE)	1.5×	2.3×	23.4 16QAM	23.3 (PAE) 16QAM	1.16×	-23	-30	3	40 nm	static	switch-based PA load reconfiguration + Doherty
S. M. Yoo JSSC May '13*	2.15	24.3	43.5 (PAE)	36.5 (PAE)	17.8† (PAE)	1.7×	1.6×	16.8 64QAM	33 (PAE) 64QAM	1.8×	-30.8	N.A.	1.68	65 nm	dynamic	Class-G supply switch
K. Onizuka ISSCC '13	1.8	27.2	30 (PAE)	22† (PAE)	9† (PAE)	1.5×	1.2×	21.3 64QAM	18 (PAE) 64QAM	1.18×	-22	-30	5.2	65 nm	dynamic	Class-G supply switch (effective)
L. Ye JSSC Dec. '13	2.2	23.3	43 (DE)	33† (DE)	15† (DE)	1.5×	1.4×	16.8 64QAM	24.5 (DE) 64QAM	1.2×	-28	WLAN mask	6.25 (TX)	65 nm	dynamic	Class-G load switch
This work	**3.71**	**26.7**	**40.2 (DE)**	**37.0 (DE)**	**26.2 (DE)**	**1.8×**	**2.6×**	**20.8 16QAM**	**28.8 (DE) 16QAM**	**1.41×**	**-24**	**-21**	**3.2**	**65 nm**	**dynamic**	**Class-G mixed-signal Doherty**
	4.3	**26.1**	**36.2 (DE)**	**29.3 (DE)**	**23.6 (DE)**	**1.7×**	**2.8×**	**20.1 16QAM**	**27.2 (DE) 16QAM**	**1.61×**	**-30**	**-26.5**				

* requiring off-chip components for PA output matching. ** requiring switches at the PA output.

† read from the reported figures. †† for the strand-alone PA. ††† compared with the Class-B operation.

CHAPTER 5. A COMPACT BROADBAND MIXED-SIGNAL PA IN BULK CMOS WITH HYBRID CLASS-G AND DYNAMIC LOAD TRAJECTORY MANIPULATION

To address the challenges of PBO efficiency/linearity and to further explore the potential of hybrid PAs, a mixed-signal PA architecture with the real-time hybrid operation of Class-G and dynamic load trajectory manipulation (DLTM) is introduced [92], [93]. The introduced hybrid technique brings the following advantages. First, the Class-G operation substantially relaxes the required impedance tuning range (ITR) of the LM network, allowing for a compact and low-loss transformer-based LM network that occupies only a single-transformer footprint. Secondly, DLTM enables PA efficiency enhancement in both Class-G supply modes. Furthermore, a new DLTM operation achieves PA efficiency peaking during PBO as well as PA carrier bandwidth extension. Mixed-signal digitally intensive PA operations ensure the PA output accuracy, including both amplitude and phase aspects. Section 5.1 present the PA architecture. Sections 5.2 and 5.3 show the implementation details and measurement results, respectively.

5.1 Mixed-Signal Hybrid Class-G and DLTM PA Architecture

5.1.1 DLTM Scheme that Achieves PA PBO Efficiency Peaking

In a typical current-mode PA, the PA load impedance for the optimum efficiency (Z_{opt_η}) is usually different from the PA load impedance for the maximum P_{out} (Z_{opt_Pout}).

Z_{opt_η} often has a smaller conductance than Z_{opt_Pout}, resulting in a larger voltage swing at the device output. This enhances the PA efficiency by reducing the dc power waste due to the reduced overlap of current and voltage waveforms. Meanwhile, due to the finite transistor knee voltage, the boosted voltage swing by Z_{opt_η} results in a reduced fundamental output current and thus reduced P_{out}. For field-effect transistors (FETs), the output current is a function of both the device input and output voltages. Figure 67 shows the simulated I-V characteristic of a cascode MOSFET circuit as a PA stage. When the output voltage swings down to the knee voltage during large-signal operation, the common-gate transistor (or even both common-gate and common-source transistors) enters the triode region, leading to a lower output impedance, a substantially reduced output current at the fundamental frequency, and therefore a decreased PA P_{out}.

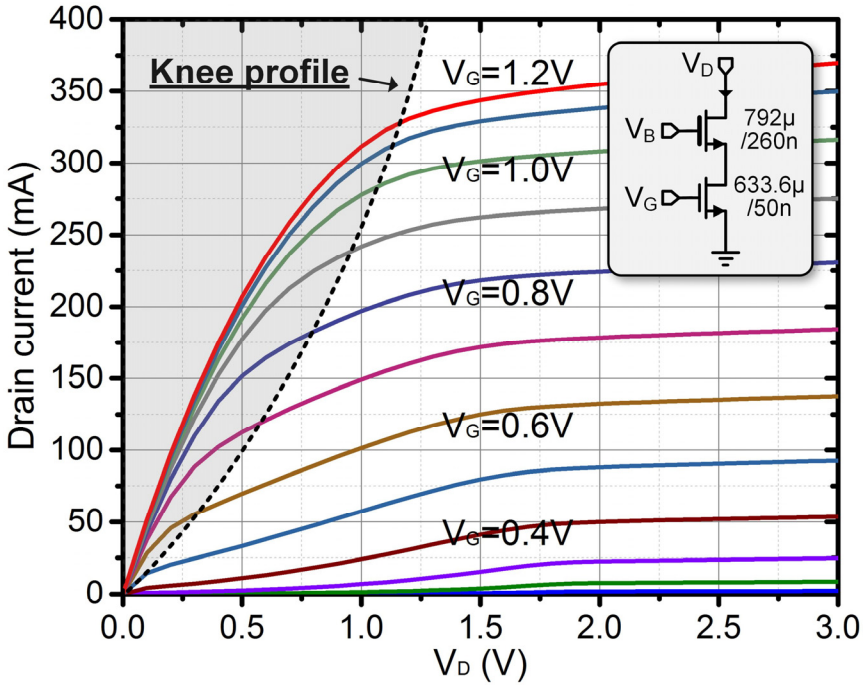


Figure 67 – Simulated I-V characteristic of a cascode MOSFET configuration.

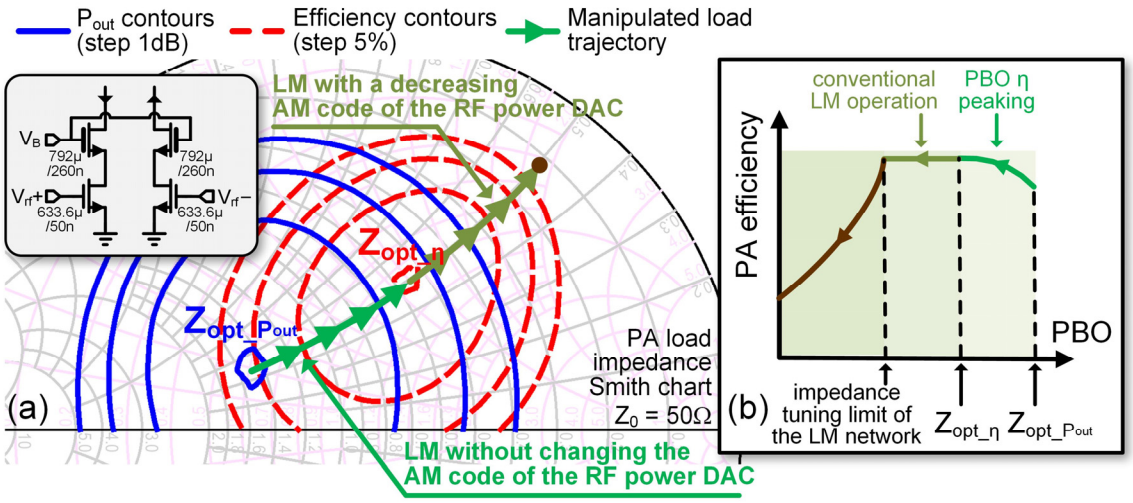


Figure 68 – (a) DLTM operation achieving PA PBO efficiency peaking and (b) its theoretical efficiency curve. The large-signal load-pull simulation result of the cascode circuit in Figure 67 is used here for illustration; it operates in a differential Class-D^{-1} configuration at 2.4GHz.

We exploit the different impedance values of Z_{opt_Pout} and Z_{opt_η} and devise a new DLTM scheme that achieves PA PBO efficiency peaking. The large-signal load-pull simulation results of the previous cascode circuit when it is implemented as an RF power DAC and operates in a differential Class-D^{-1} configuration at 2.4GHz are used for illustration (Figure 68a). The introduced DLTM operation is comprised of two PBO sections. First, the PA performs its PBO by manipulating the PA load impedance to travel from Z_{opt_Pout} to Z_{opt_η}, without changing the AM code of the RF power DAC. During this PBO process, the PA load consecutively meets Z_{opt_Pout} and then Z_{opt_η}, and the PA PBO efficiency peaks up (Figure 68b) in contrast to many conventional PA designs. Next, the conventional LM operation is performed for larger PBO levels, in which the PA scales down its RF output current by decreasing the AM code of the RF power DAC, and the PA

load impedance is simultaneously adjusted by the LM network to achieve a decreasing conductance along a constant-susceptance circle. During this PBO process, the PA PBO efficiency is maintained until the tuning limit of the LM network is reached (Figure 68b).

Sufficient power and efficiency differences between Z_{opt_η} and Z_{opt_Pout} are desired to enhance the effectiveness of the introduced DLTM scheme. These often exist in the battery-powered PAs of mobile devices, in which the knee voltage is a considerable percentage of the PA supply voltage, e.g., about 23% in Figure 67. Moreover, if the PA operates in the device triode region for a considerable amount of time, it tends to present large differences between Z_{opt_η} and Z_{opt_Pout}. Switching-mode PAs ideally operate in the device triode region for a half of the period, making them good candidates for the introduced DLTM scheme. Take the cascode circuit in Figure 67 again as an example, and assume that it operates in the differential Class-D^{-1} configuration. Figure 69 compares the simulated PA output voltage and current waveforms when it is loaded by Z_{opt_Pout} or Z_{opt_η} as the fundamental impedance. The even and odd harmonics are terminated as open and short-to-ground up to the 6^{th} and 5^{th} harmonic, respectively. These two cases show significant differences in their voltage and current waveforms. The case of Z_{opt_Pout} has +26.9dBm PA P_{out} and 56.3% peak PA DE, while the case of Z_{opt_η} has +25.4dBm PA P_{out} and 68.8% peak PA DE (Figure 69a). It is clearly shown that the case of Z_{opt_η} exhibits a higher device output voltage swing, more operating time in the device triode region, and a smaller fundamental RF output current, agreeing well with the analysis.

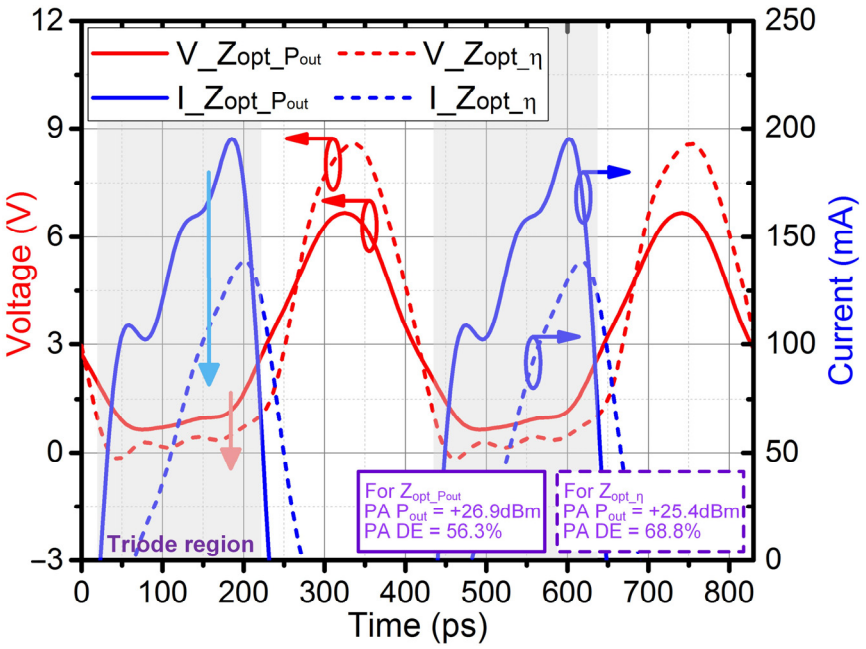


Figure 69 – Simulated drain current and voltage waveforms of the cascode circuit in Figure 67 when it operates in a differential Class-D^{-1} configuration. Results for Z_{opt_η} and Z_{opt_Pout} as the fundamental load impedance are compared. Even and odd harmonics are terminated as open and short-to-ground up to the 6th and 5th harmonic, respectively.

5.1.2 Mixed-Signal Hybrid Class-G and DLTM PA Architecture

To further improve PA efficiency in deep PBO, the introduced new DLTM scheme is further combined with Class-G operation. Figure 70 shows the mixed-signal hybrid Class-G and DLTM PA architecture, which comprises an RF power DAC, a Class-G supply modulator, and an on-chip digitally controlled LM network. The introduced PA operates in a polar fashion (Figure 70). The RF power DAC is driven by the PM RF signal, and the AM is synthesized by dynamically programming the power DAC, the Class-G modulator, and the LM network together. The Class-G operation provides two supply modes for different real-time PA PBO levels. In the high-power region, the PA is in the

full-V_{DD} mode. In deep PBO, the PA is in the half-V_{DD} mode for PA efficiency enhancement. Within each supply mode, the new DLTM operation is performed by the RF power DAC and LM network to enhance PA PBO efficiency.

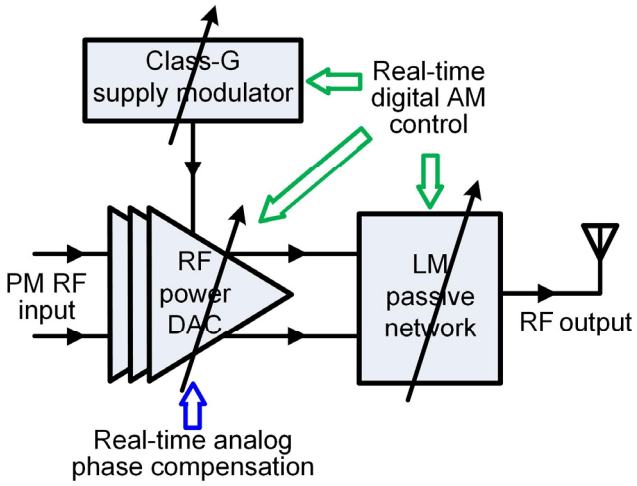


Figure 70 – Mixed-signal hybrid Class-G and DLTM PA architecture.

The hybrid real-time Class-G and DLTM operations for PA PBO efficiency enhancement are explained in details as follows. At the peak PA P_{out} (0dB PBO), the PA supply voltage is in the full-V_{DD} mode, and the PA load impedance is set to Z_{opt_Pout} by the LM network for maximum PA P_{out}. Without changing the AM code of the RF power DAC, the PA first performs its PBO operation by manipulating the load to travel from Z_{opt_Pout} to Z_{opt_η}. As explained previously, the PA efficiency peaks and reaches the maximum value through this process. For larger PBO levels, the power DAC decreases its AM code, and the load is simultaneously adjusted by the LM network that provides a proper conductance along a constant-susceptance circle and cancels the output capacitance of the RF power DAC. The PA PBO efficiency is enhanced until the load tuning limit is reached. At 6dB

PBO, the Class-G operation sets the supply to the half-V_{DD} mode. The above DLTM operation is then repeated for the PBO levels beyond 6dB. *Note that the digitally intensive and reprogrammable nature of the RF power DAC, Class-G supply modulator, and digitally controlled on-chip LM network enables their well synchronized and optimum cooperation in the introduced hybrid PA architecture, which cannot be easily achieved by conventional analog PAs.*

Figure 71 shows the theoretical PBO efficiency curve of the hybrid Class-G and DLTM PA that greatly enhances the PA average efficiency for high-PAPR signals. Compared with a Class-G PA, the hybrid Class-G and DLTM operations enhance the PA PBO efficiency within each supply voltage mode. Different from a conventional LM PA, the hybrid operation substantially extends the effective LM range by using only a 1-bit Class-G supply modulator. This leads to superior PA efficiency in deep PBO and relaxes the required ITR, allowing for simplified, compact, and low-loss LM network designs.

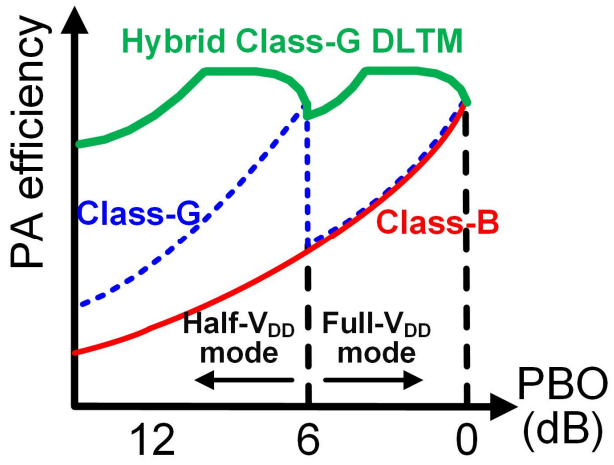


Figure 71 – Theoretical efficiency curve of the hybrid Class-G and DLTM PA.

Mixed-signal PA operation also ensures the accuracy of the PA output signal. This PA minimizes AM-AM distortions by selecting proper digital control codes for the RF power DAC, Class-G supply modulator, and the LM network at different P_{out}. At the same time, AM-PM distortions are compensated by the dynamic analog tuning of the varactors in the digital driver chain. The advantages of this real-time AM-PM linearization technique include sufficient phase correction, low PM-AM distortion, P_{out}-independent phase compensation LUT, negligible impact on PA efficiency, and no reliability degradation.

In addition, the introduced PA architecture extends the PA carrier bandwidth. For a given current-mode PA, its optimum load impedances for the same PA P_{out} at different RF frequencies approximately have the same conductance but different susceptance that cancel the device output capacitance (Figure 72) [81]. Thus, the PA carrier bandwidth is extended by adjusting the PA load impedance along a constant-conductance circle for different operating frequencies.

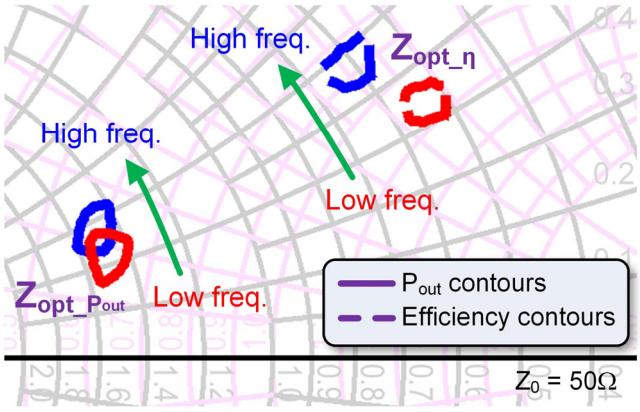


Figure 72 – Load-pull simulation results at different RF frequencies (2.1GHz and 2.8GHz) for the cascode circuit in Figure 67 when it operates in a differential Class-D^{-1} configuration.

5.2 PA Implementation Details

5.2.1 RF Power DAC and Class-G Supply Modulator

Figure 73 shows the proof-of-concept PA in a standard 65nm bulk CMOS process. The PA output stage is a 6-bit binary-weighted differential cascode RF power DAC operating in the Class-D^{-1} mode. The top five most significant bits are thermometer-coded for enhanced matching, and the least significant bit is binary coded to extend the dynamic range of the PA P_{out}.

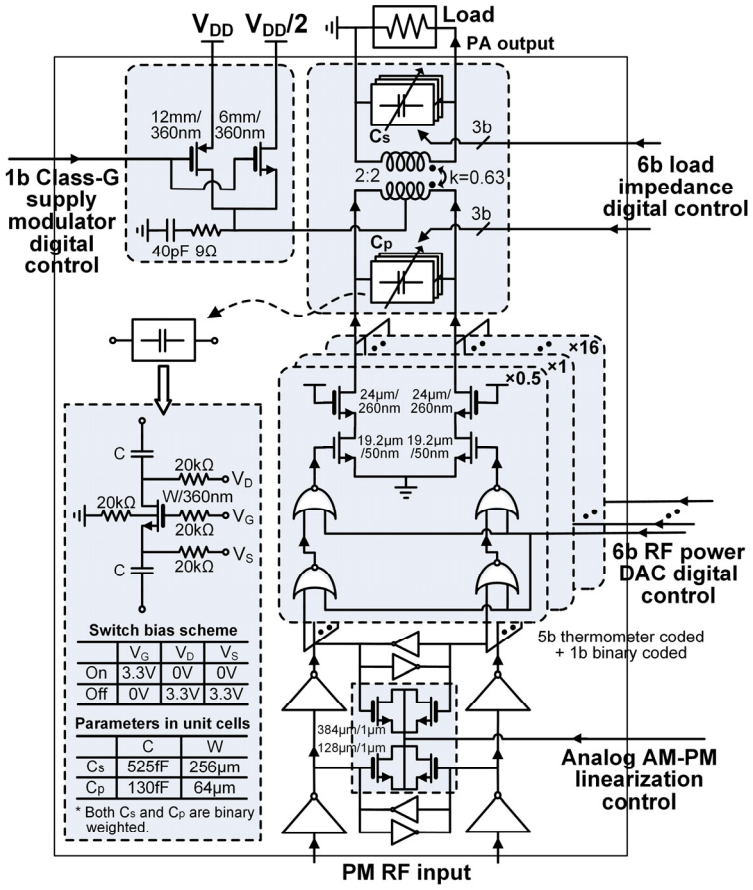


Figure 73 – Simplified schematic of the prototype PA implementation in a standard CMOS 65nm process.

The power DAC is driven by a four-stage 1.2V digital driver chain. Varactors are used at the outputs of the first two digital driver stages to provide real-time analog AM-PM linearization. They are properly sized to offer sufficient phase compensation with negligible PM-AM distortions.

The 1-bit Class-G supply modulator uses NMOS and PMOS switches for 2.8V V_{DD} (full-V_{DD} mode) and 1.55V V_{DD} (half-V_{DD} mode), respectively. The half-V_{DD} value is chosen to be slightly higher than the half of the full-V_{DD} value to compensate the PA knee voltage, whose effects are more pronounced in the half-V_{DD} mode. The simulated on-resistances of the NMOS and PMOS switches are 0.36Ω and 0.35Ω at their operating voltage levels, respectively, ensuring negligible PA efficiency degradation. The simulated efficiency of the Class-G supply modulator is better than 96.3% and 95% for all the PA P_{out} values in full-V_{DD} and half-V_{DD} modes, respectively.

5.2.2 On-Chip Transformer-Based LM Network

The hybrid Class-G and DLTM operation relaxes the requirements on the LM network's ITR. An on-chip transformer-based LM network is adopted in the introduced design (Figure 73). It achieves differential to single-ended conversion and complex impedance tuning with compactness and low passive loss.

The LM network is comprised of an on-chip transformer and two tuning capacitors on its primary and secondary sides (Figure 73), which form a 4^{th}-order network. The

equivalent circuit model in Figure 74 [80] is used for the following analysis. A single-ended model is used here for simplicity. L_p and L_s are the self-inductances of the primary and secondary windings, respectively. L_m is their mutual inductance with a magnetic coupling coefficient of k. C_p and C_s are the tuning capacitances on the primary and secondary sides, respectively. Although on-chip transformers have been extensively used in PA designs, including LM PAs, the following analysis focuses on the characteristics in dynamic load tuner applications, which have not been fully explored in literature.

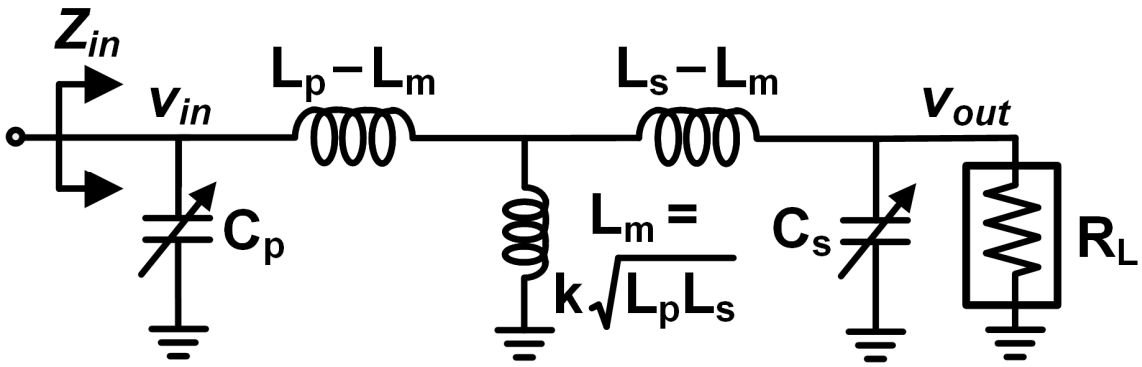


Figure 74 – Analysis model of the on-chip transformer-based LM network.

First, the impedance tuning capability of the transformer-based LM network is studied. The resulting load impedance Z_{in} is derived as

$$\begin{aligned} Z_{in} &= [s^3 R_L C_s (L_p L_s - L_m^2) + s^2 (L_p L_s - L_m^2) + s R_L L_p] / [s^4 R_L C_p C_s (L_p L_s - L_m^2) + s^3 C_p (L_p L_s - L_m^2) + s^2 R_L (C_p L_p + C_s L_s) + s L_s + R_L] \\ &= [s^3 R_L C_s L_p L_s (1-k^2) + s^2 L_p L_s (1-k^2) + s R_L L_p] / [s^4 R_L C_p C_s L_p L_s (1-k^2) + s^3 C_p L_p L_s (1-k^2) + s^2 R_L (C_p L_p + C_s L_s) + s L_s + R_L] \end{aligned} \quad (61)$$

where s=j2πf, and f is the operating frequency. (61) suggests that Z_{in} depends on both C_p and C_s. For more design insights, the Smith chart is used for explanations (Figure 75).

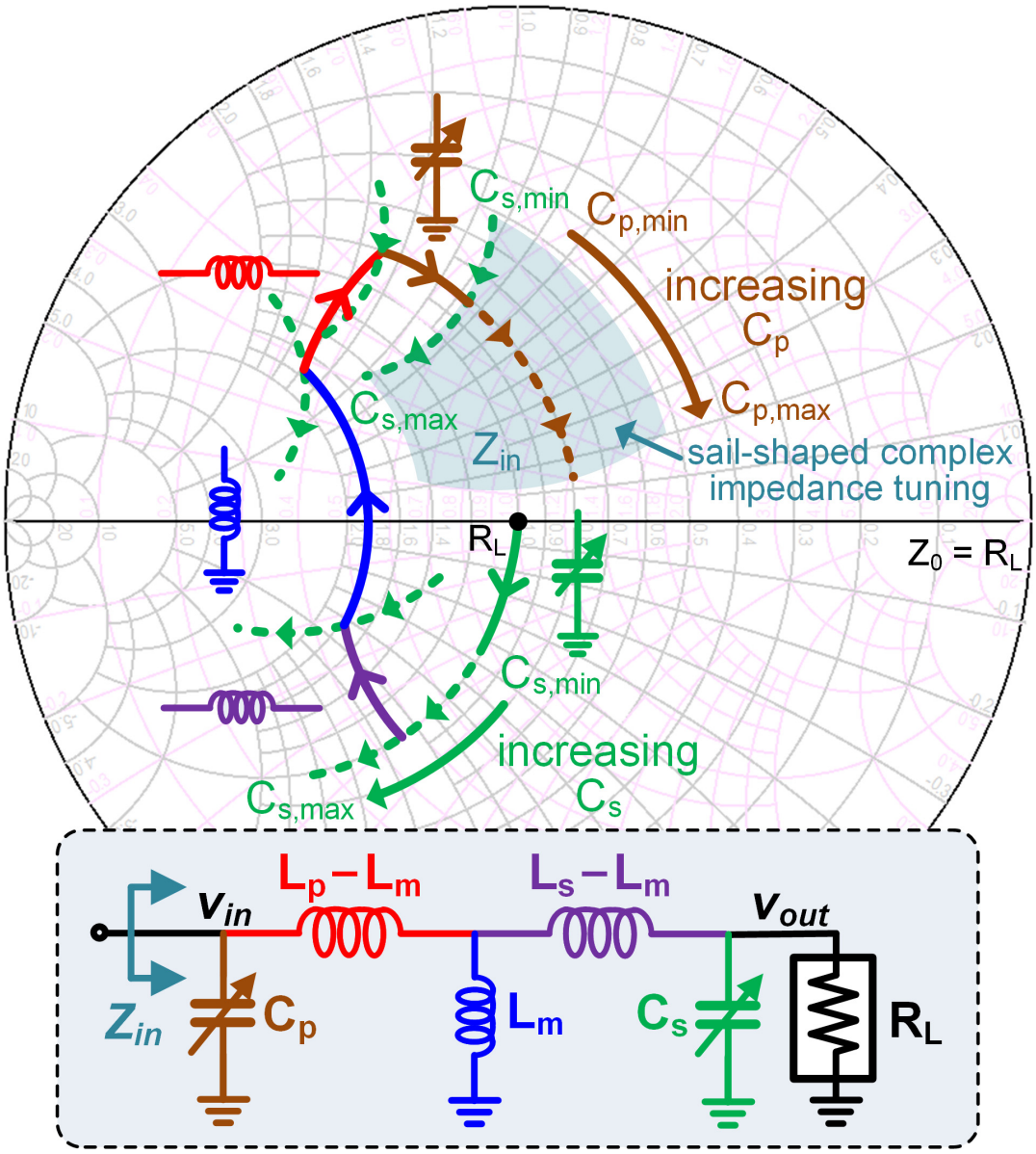


Figure 75 – Smith chart illustration for the impedance tuning characteristic of the transformer-based LM network. The network is assumed to be lossless for simplicity in this figure.

The effect of tuning C_p is straight forward since it moves Z_{in} along constant-conductance circles on the Smith chart. For a given device with a fixed biasing and driving condition, the load-pull impedance at a higher operating frequency has a larger susceptance. In order to extend the carrier bandwidth, C_p should be decreased at higher

operating frequencies (Figure 75). Figure 75 also shows how tuning C_s impacts Z_{in}. Due to the impedance transformations of one series inductor (L_s-L_m), one shunt inductor (L_m), and the other series inductor (L_p-L_m), Z_{in} moves approximately along constant-susceptance circles when C_s is adjusted. During PA PBO, a reduced conductance is desired and C_s thus should be decreased (Figure 75). In summary, the tunings of C_p and C_s create a "sail-shaped" complex impedance coverage on the Smith chart.

Next, the transfer function of the transformer-based LM network is analyzed. The analytical result of v_{out}/v_{in} as labeled in Figure 74 is derived as

$$\frac{v_{out}}{v_{in}} = \frac{R_L L_m}{s^2 R_L C_s (L_p L_s - L_m^2) + s(L_p L_s - L_m^2) + R_L L_p} = \frac{kR_L\sqrt{L_p L_s}}{s^2 R_L C_s L_p L_s (1-k^2) + sL_p L_s (1-k^2) + R_L L_p}. \quad (62)$$

(62) offers two important design insights. As mentioned, C_s should be decreased during PBO so that the PA efficiency is enhanced. First, (62) shows that $|v_{out}/v_{in}|$, i.e., the passive voltage gain, monotonically decreases during this process. This behavior fundamentally makes it possible to maintain the voltage swing at the device output during PBO for efficiency enhancement, while the voltage swing at the final load resistor decreases for PBO. Secondly, (62) shows that the phase of v_{out}/v_{in} monotonically increases when C_s decreases at a given operating frequency. This combines with the PA device AM-PM distortions and constitutes the total PA AM-PM nonlinearity. These two AM-PM distortions may add constructively or destructively, depending on the PA mode, device technology, and circuit topology. In the introduced design, these two AM-PM sources add

constructively, and the total PA AM-PM is compensated by the dynamic tuning of the varactors in the digital driver chain.

In the proof-of-concept PA, the transformer has a 2:2 turn ratio (Figure 76a). Its geometry (outer diameter=397.3μm) and magnetic coupling coefficient (k=0.63) are carefully designed so that a compact layout with a sufficient load tuning range and high passive efficiencies across the load tuning settings is achieved. The tuning capacitors on the two sides of the transformer are each 3-bit binary-weighted switch-controlled metal-oxide-metal capacitor arrays. There are in total 6 bits for configuring the LM network. Switches are designed to withstand large voltage swings with low distortions (Figure 73). They use deep N-well thick-oxide transistors and their gate and bulk are dc biased using large resistors (20kΩ), which makes these two terminals semi-open and boot-strapped for ac operation to relieve the stress [84]. Furthermore, the dc biases of both source and drain are set differently in on and off switch states (Figure 73) [84]. Since a switch-controlled capacitor is most vulnerable to large voltage swings in its off state, this biasing scheme prevents the off switch transistors from forming an undesired channel and enhances its resilience to large voltage swings.

Figure 76b shows the simulated ITR of the implemented on-chip transformer-based LM network, which achieves 2.74× conductance tuning. Figure 77 shows the simulated gain and phase responses when adjusting C_s, which align well with the theoretical analysis. The simulated AM-PM due to the LM network is 24.1° for the whole ITR. The simulated

PE of the LM network is better than 67.4% for all the impedance settings (Figure 78). During PBO, C_s decreases, and the PE first increases and then slightly decreases, which is mainly caused by the decreased and then increased impedance transformation ratio in the introduced LM network design. Such PBO PE peaking also helps with the PA PBO efficiency enhancement.

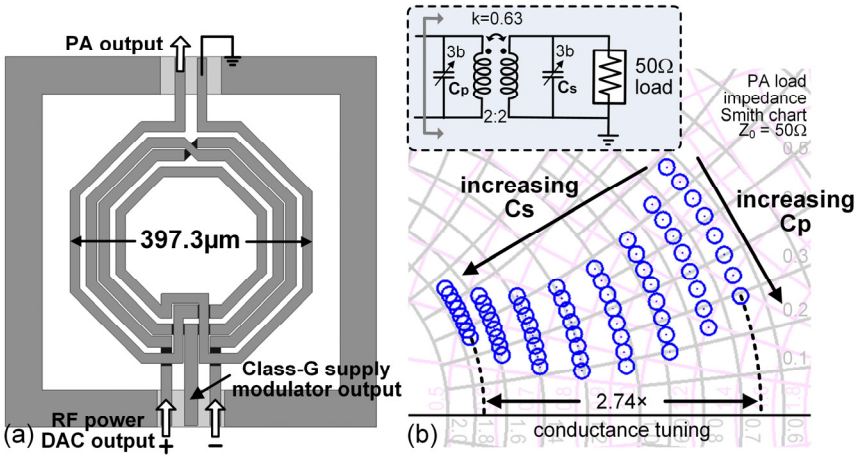


Figure 76 – (a) EM structure of the transformer and (b) simulated ITR of the LM network.

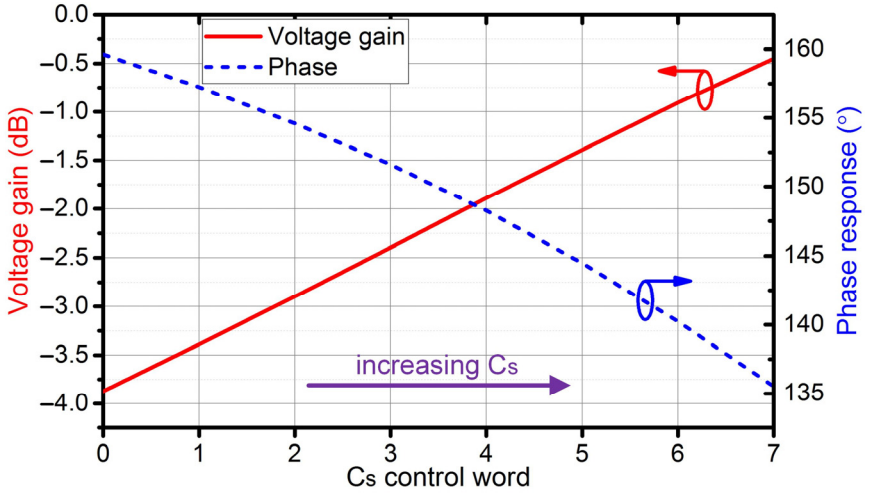


Figure 77 – Simulated voltage gain and phase response of the LM network when C_s is tuned.

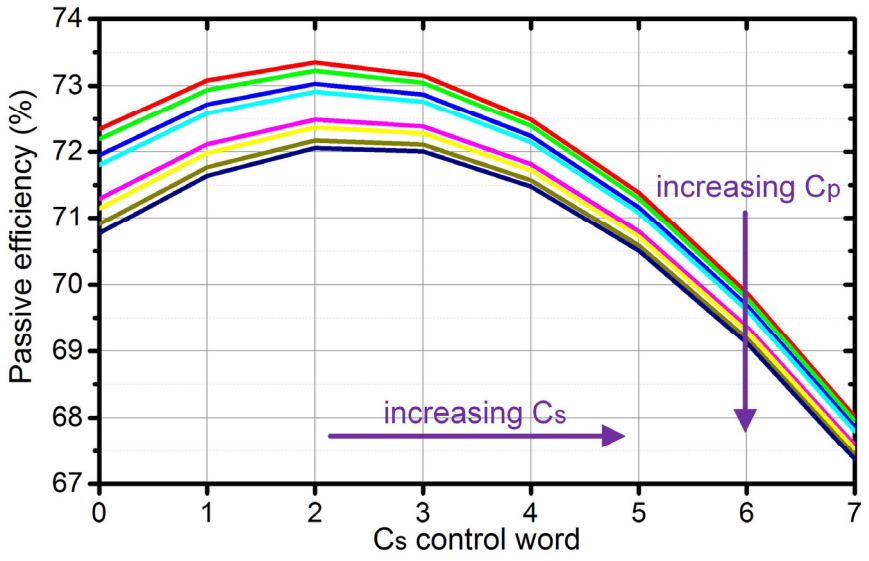


Figure 78 – Simulated PE of the LM network for all the settings.

5.3 Experimental Results

The PA is fully integrated in a standard 65nm bulk CMOS process with a total chip area of only 1.9mm^2 (Figure 79).

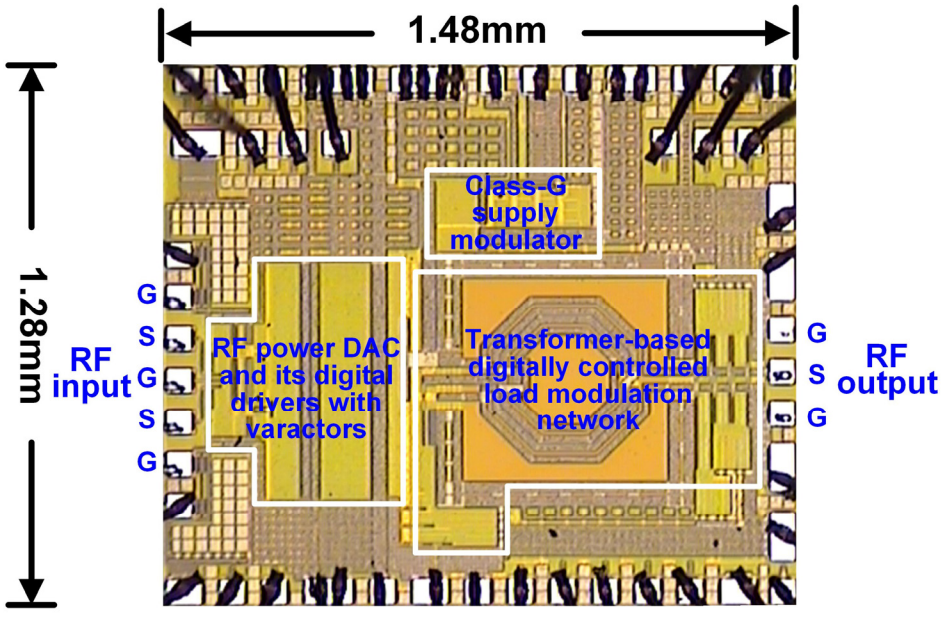


Figure 79 – Chip microphotograph.

5.3.1 CW Measurement

The PA is first characterized using CW signals. Figure 80 shows the measurement results at 2.4GHz. Each symbol represents one combined digital setting for the power DAC, Class-G supply modulator, and LM network. Efficiency-optimum settings are selected for different P_{out} levels (Figure 80). The PA achieves 39% PA DE at +24.6dBm peak P_{out} with a peak DE of 45.6% at +24dBm P_{out}, showing 6.6% (17% relative) efficiency peaking at 0.6dB PBO in the full-V_{DD} mode. Similarly, a PA efficiency peaking of 4% (11% relative) is achieved at 0.7dB PBO in the half-V_{DD} mode. The measured DE at 3/6/9/12dB PBO is 39.9/41.2/34.5/21.8% with 1.45/2.12/2.49/2.18× improvement over an ideal Class-B PA, respectively. These measurements demonstrate the PA PBO efficiency peaking and deep PBO efficiency enhancement by the hybrid Class-G and DLTM operations, agreeing well with the theoretical analysis.

Figure 81 shows the measured PA AM-PM of the efficiency-optimum settings. Class-G supply switching causes an evident phase jump at the full-V_{DD}/half-V_{DD} mode transition. Meanwhile, staircase-shaped AM-PM behaviors are observed in both Class-G supply modes. This is due to the monotonic AM-PM of the LM network, which is discussed in Section 5.2.2. The PA phase response of different varactor control voltages is characterized at peak P_{out}, which forms the AM-PM compensation LUT for the dynamic measurements. Note that the LUT generation is P_{out}-independent for the adopted AM-PM compensation technique, since the varactors at the digital drivers' outputs experience a

constant-envelope PM driving signal during PBO. Such P_{out}-independent LUT significantly reduces the implementation complexity.

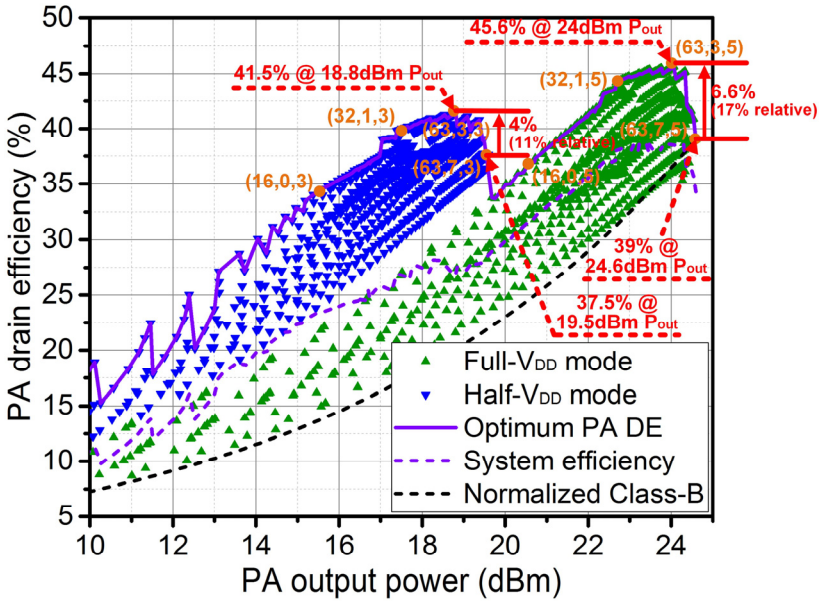


Figure 80 – Measured PA DE at 2.4GHz versus PA P_{out} in CW measurement. Representative control words are shown and they are formated as (power DAC code, C_s code, C_p code).

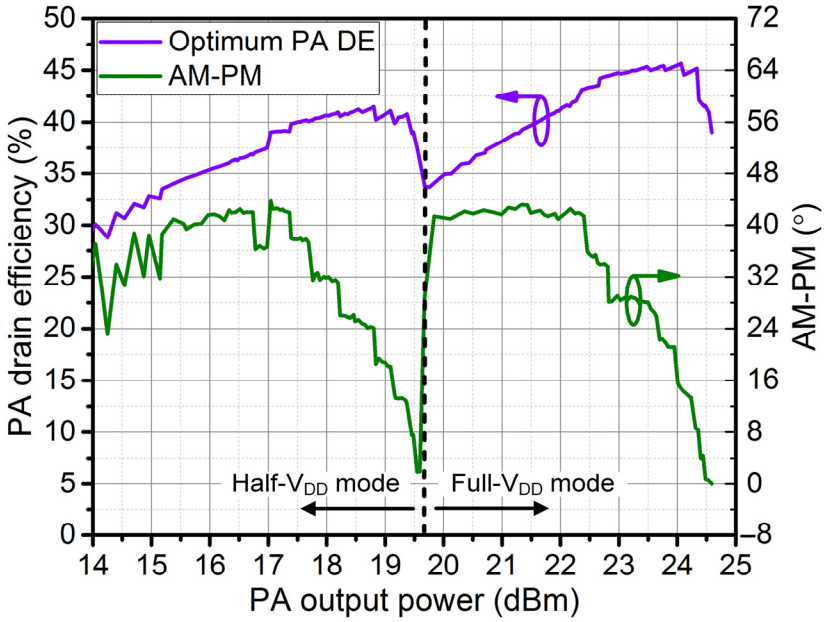


Figure 81 – Measured PA AM-PM of the efficiency-optimum settings at 2.4GHz.

Figure 82 shows the measured PA P_{out} and DE at different RF frequencies when the RF power DAC is fully on. For the load setting achieving the maximum P_{out} at 2.4GHz, the PA has a –1dB P_{out} bandwidth of 1.9–2.9GHz, i.e., 41.7% fractional bandwidth (Figure 82a). By selecting the optimum loads for maximum P_{out} at different RF frequencies, the –1dB P_{out} bandwidth is extended to 1.9–3.3GHz, i.e., 53.8% fractional bandwidth (Figure 82a). Substantial PA DE improvement over the bandwidth is also achieved (Figure 82b). This demonstrates the carrier bandwidth extension by the LM operation. Moreover, the PA PBO efficiency enhancement by the hybrid Class-G and DLTM operations is maintained in a wide RF carrier frequency range. Figure 83 shows the CW measurements at 2.8 GHz and demonstrates 1.53/1.87/1.99/1.81× PA DE improvement over an ideal Class-B PA at 3/6/9/12dB PBO, verifying the benefits of the reconfigurable mixed-signal PA.

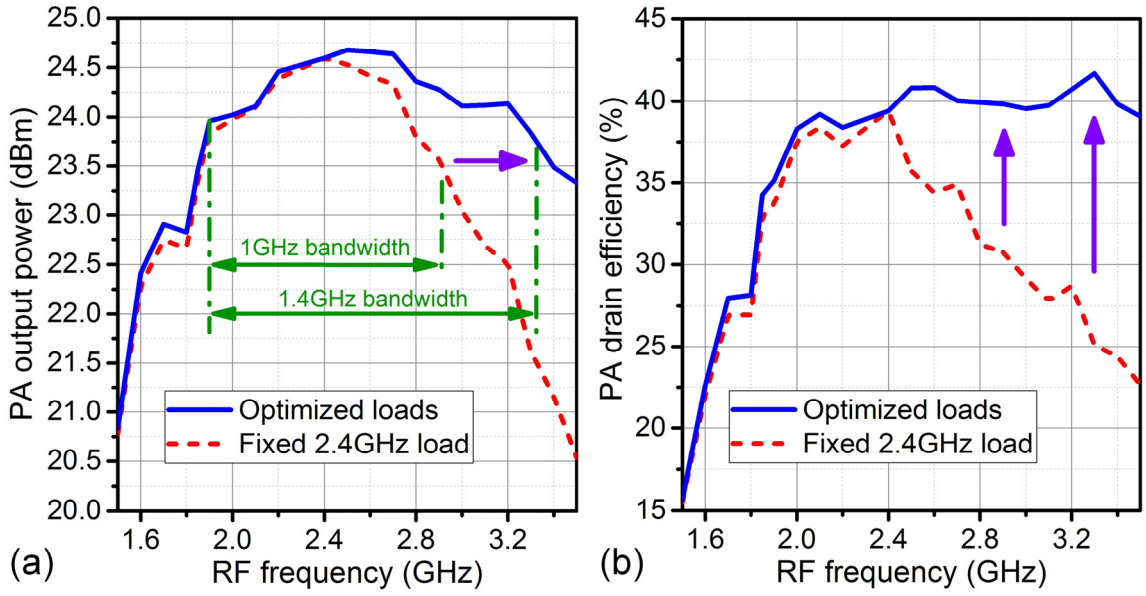


Figure 82 – PA carrier bandwidth extension by LM in CW measurement for (a) PA P_{out} and (b) PA DE.

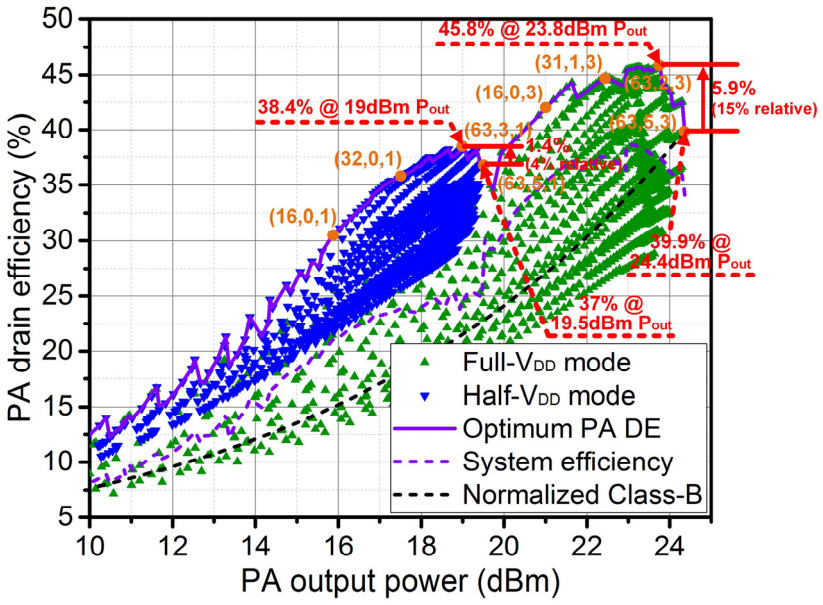


Figure 83 – Measured PA DE at 2.8GHz versus PA P_{out} in CW measurement. Representative control words are shown and they are formated as (power DAC code, C_s code, C_p code).

The measured 2nd/3rd harmonic rejections at peak P_{out} are −46/−31.6dBc and −38.8/−34.1dBc at 2.4GHz and 2.8GHz without additional filtering (Figure 84).

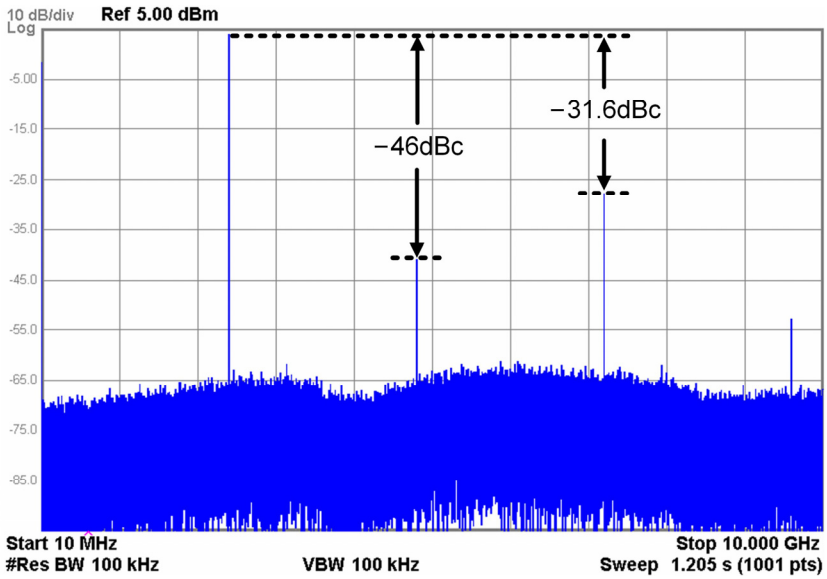


Figure 84 – Measured PA output spectrum for peak CW P_{out} at 2.4GHz without any additional filtering. A 20dB attenuator is used at the PA output in this measurement.

5.3.2 Modulation Measurement

Figure 85 shows the setup for the modulation tests. The PM RF signal, digital AM control signals, and dynamic varactor analog control signal are generated by an arbitrary waveform generator (AWG), a pattern generator, and an arbitrary function generator (AFG), respectively. These three instruments are synchronized with a timing resolution of 1ps by independently tuning the delays of their trigger signals from AFGs (Figure 85 and Figure 86). The PA output signal is demodulated by an oscilloscope with a vector signal analysis (VSA) software. 5× sampled 64QAM (PAPR=7dB) up to 25MSym/s (150Mb/s) and 256QAM (PAPR=7.3dB) up to 12.5MSym/s (100Mb/s) are used in the measurements. No additional predistortion or feedback linearization are applied.

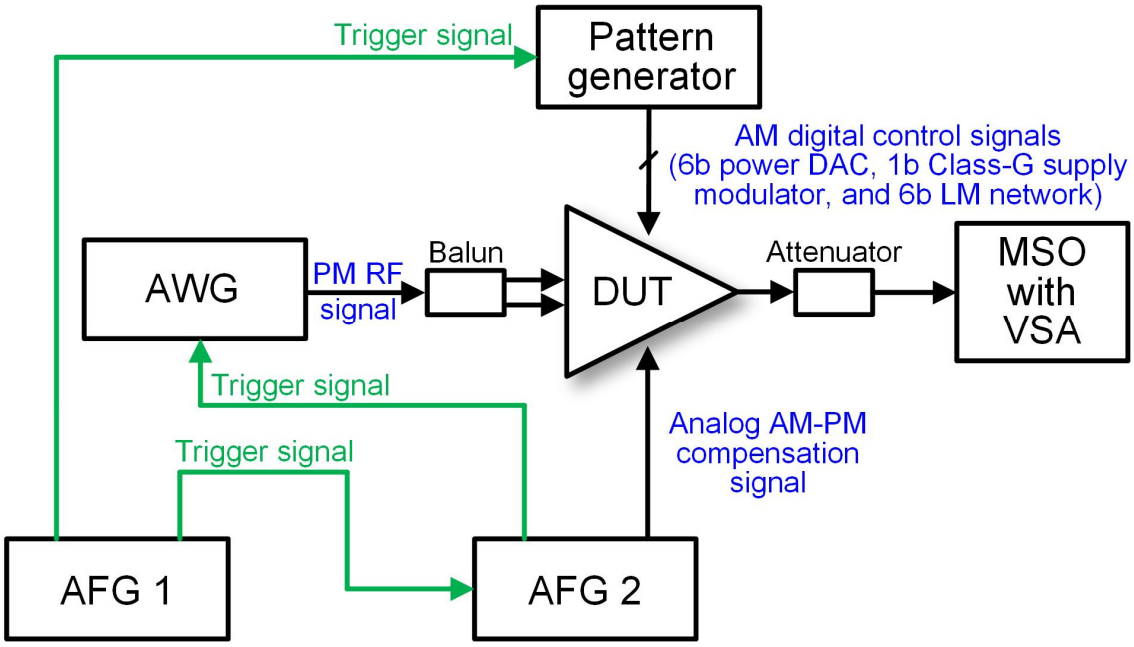


Figure 85 – Simplified measurement setup for modulation measurement.

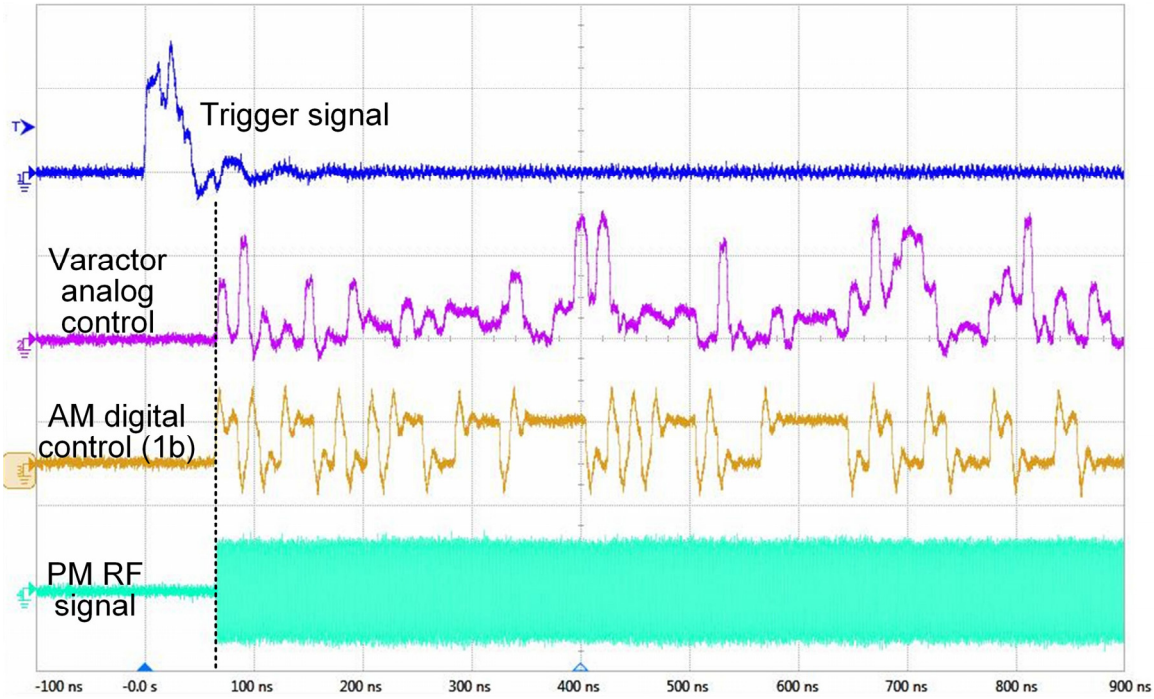


Figure 86 – Waveform examples of the synchronized PM RF signal, digital AM control signal, and dynamic varactor analog control signal at a sampling rate of 100MSa/s.

5.3.2.1 Dynamic AM-PM Linearization

Real-time AM-PM linearization by the dynamic analog tuning of the varactor control voltage is first measured. Compared with a constant varactor control voltage, dynamic analog tuning substantially reduces the rms EVM and ACLR by 10.4/5.3/2.2dB and 6.8/4.1/2.2dB for 5/10/20MSym/s 64QAM at 2.4GHz. These EVM and ACLR improvement values are 10.8/8/4.5dB and 8.4/4.9/2.3dB for 5/10/20MSym/s 64QAM at 2.8GHz, showing consistent improvement in a wide RF carrier frequency range.

Figure 87 compares the measured demodulation results for 10MSym/s 64QAM at 2.8GHz. Before applying dynamic AM-PM linearization, the outer constellation points

rotate with respect to the inner points (Figure 87a), showing AM-PM nonlinearity. This is corrected, together with improved ACLR, by applying the dynamic analog tuning of the varactor control voltage (Figure 87b). Meanwhile, there is negligible change on the PA P_{out} and efficiency due to this AM-PM linearization. Moreover, 256QAM is successfully demodulated after applying dynamic AM-PM linearization (Figure 88), while the demodulated constellation cannot be locked by the VSA software if using a constant varactor control voltage.

With dynamic AM-PM linearization at 2.4GHz, the PA delivers +17.6/+17.3dBm 10MSym/s 64-QAM/256-QAM signals with 27.5/26.7% PA DE, 22.2/21.6% system efficiency including all the on-chip dc power consumption, −29.2/−30.4dB rms EVM, and –25.3/–25.1dBc ACLR. At 2.8GHz, the PA delivers +17.3/+17dBm 10MSym/s 64-QAM/256-QAM signals with 26.2/24.1% PA DE, 20.9/19.3% system efficiency, −31.3/−31.5dB rms EVM, and –26.4/–26.1dBc ACLR. These are the results for the average P_{out} without backing-off the PA peak P_{out}.

AM-PM linearization with deliberate timing mismatch is also characterized. In this measurement, the PM RF signal and AM digital controls remain aligned, while the timing of the dynamic varactor analog control signal is adjusted by tuning the delay of its trigger signal. Figure 89a and Figure 89b show the results at 2.4GHz and 2.8GHz, respectively. The rms EVM is <−24.8/−25.6dB up to ±0.3× symbol period at 2.4/2.8GHz. Significant timing mismatch leads to degraded EVM and ACLR, which can be even worse than the

case with a constant varactor control voltage, i.e., no dynamic AM-PM compensation (Figure 89). This is because the phase adjustment by the dynamic varactor analog control is equivalently additive phase distortions when its timing is excessively misaligned.

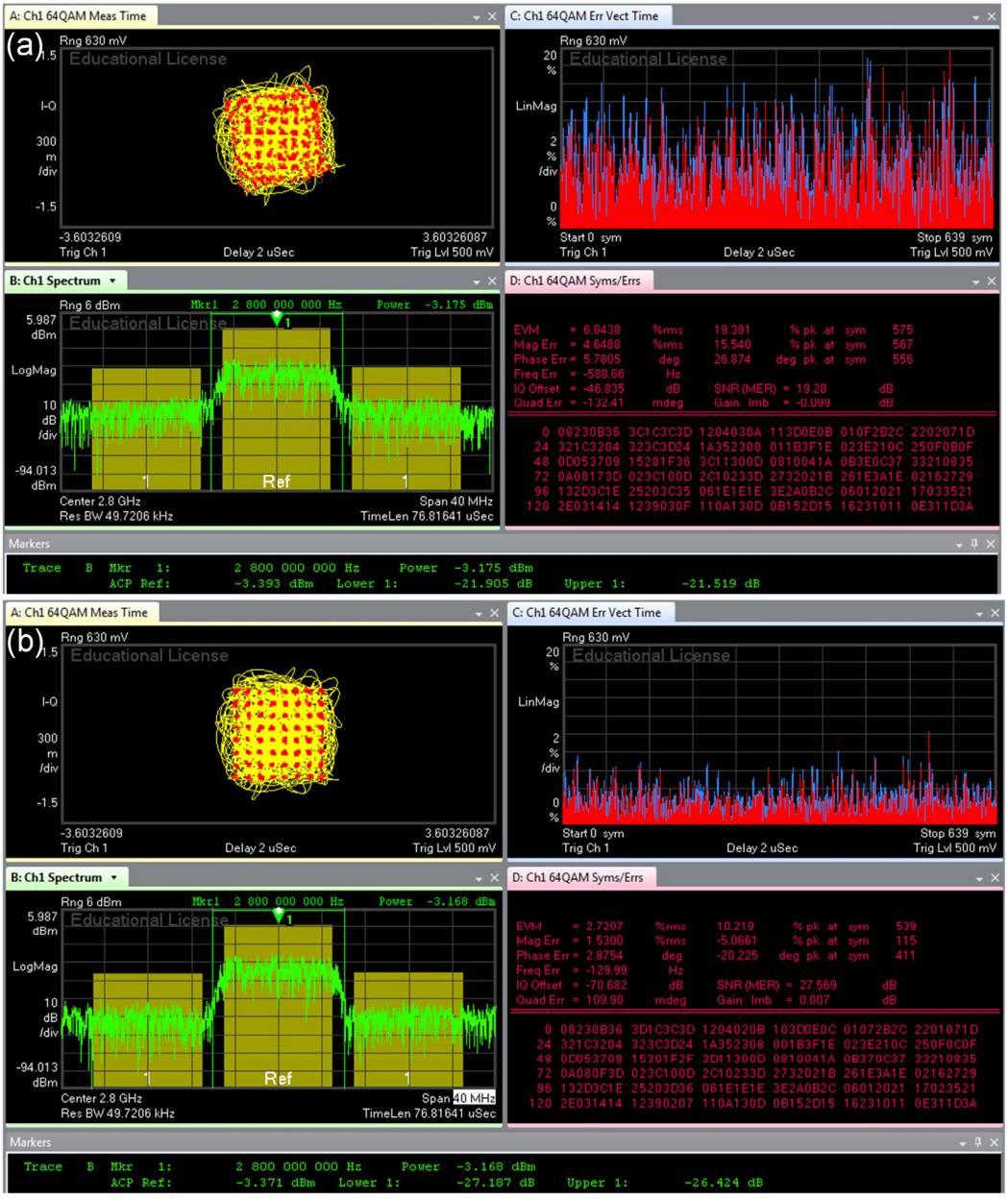


Figure 87 – Measurement results for 10MSym/s 64QAM at 2.8GHz: (a) with a constant varactor control voltage (+17.3dBm average PA P_{out}, 25.5% PA DE) and (b) with the dynamic analog tuning of the varactor control voltage (+17.3dBm average PA P_{out}, 26.2% PA DE).

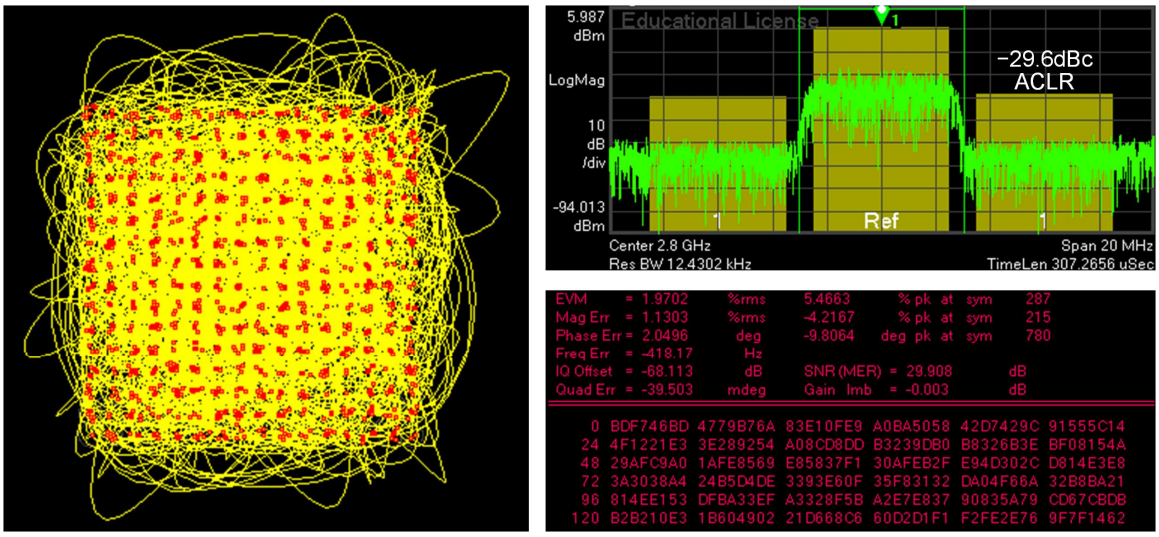


Figure 88 – Measurement results for 5MSym/s 256QAM at 2.8GHz with +17dBm average PA P_{out} by employing the dynamic analog tuning of the varactor control.

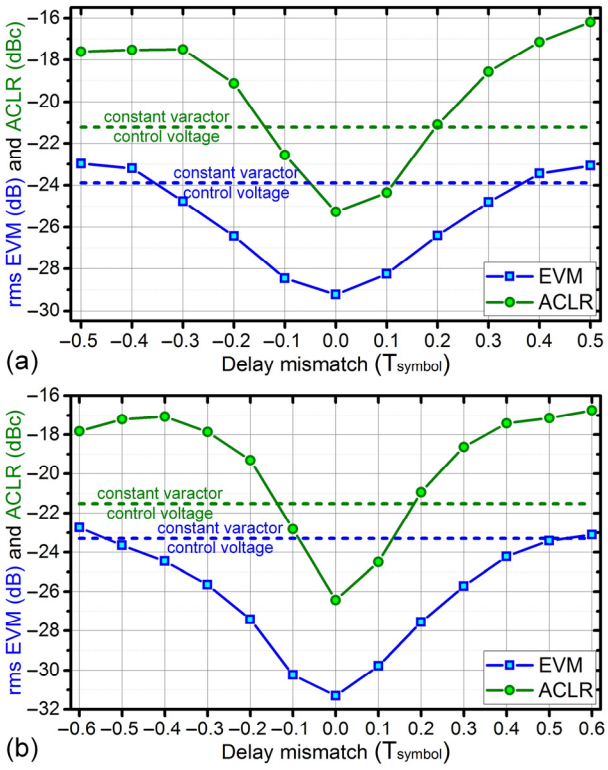


Figure 89 – Measurements with deliberately misaligned dynamic varactor analog control at (a) 2.4GHz and (b) 2.8GHz. The rms EVM/ACLR results for a constant varactor control voltage are shown as dashed lines. 64-QAM signals at 10MSym/s (symbol period T_{symbol}=100ns) are used.

5.3.2.2 Carrier Bandwidth Extension by Mixed-Signal Reconfiguration

Reconfiguring the LUTs of both the AM digital controls and dynamic varactor analog tuning optimizes the performance of the introduced PA at different RF frequencies, which includes the PA P_{out}, efficiency, and linearity. For example, Figure 90 shows the measurement results at 2.8GHz if using the LUTs that are optimized for 2.4GHz. Compared with Figure 87b, 0.23dB PA P_{out}, 5.2% PA DE, 4.9dB rms EVM, and 4.8dB ACLR enhancement are achieved after mixed-signal reconfiguration. This demonstrates that the introduced PA can be in-field digitally reconfigured to deliver its optimum performance at different RF carrier frequencies.

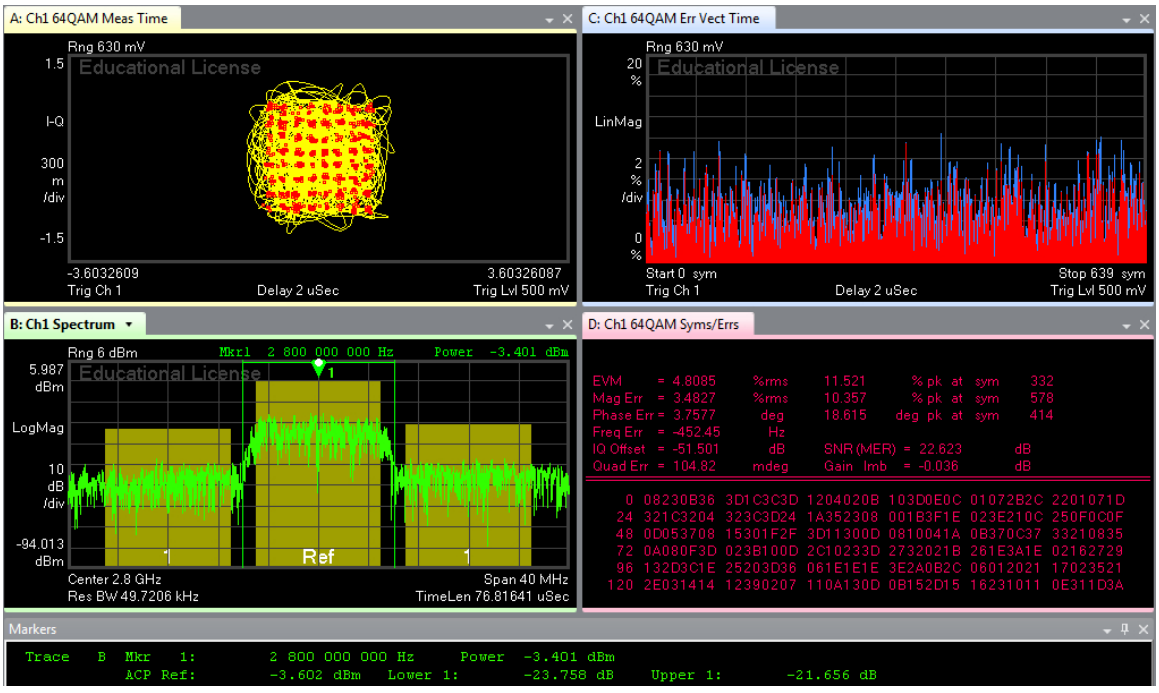


Figure 90 – Measurement results for 10MSym/s 64QAM at 2.8GHz when using LUTs for 2.4GHz. Comparison with the optimum performance at 2.8GHz using 2.8GHz LUTs (Figure 87b) verifies that the mixed-signal reconfiguration of the PA achieves performance optimization at different carrier frequencies.

5.3.2.3 Other Performance at Peak Average PA P_{out}

Figure 91a and Figure 91b show the measured linearity for 64-QAM/256-QAM signals with different symbol rates at 2.4GHz and 2.8GHz, respectively. The rms EVM of 64QAM is below −25dB up to 20MSym/s and 25MSym/s at 2.4GHz and 2.8GHz, respectively. No drastic linearity degradation is observed and the linearity at higher symbol rates can be further improved by refining the setup that provides better timing alignment among mixed-signal paths, including AM digital controls and analog varactor control.

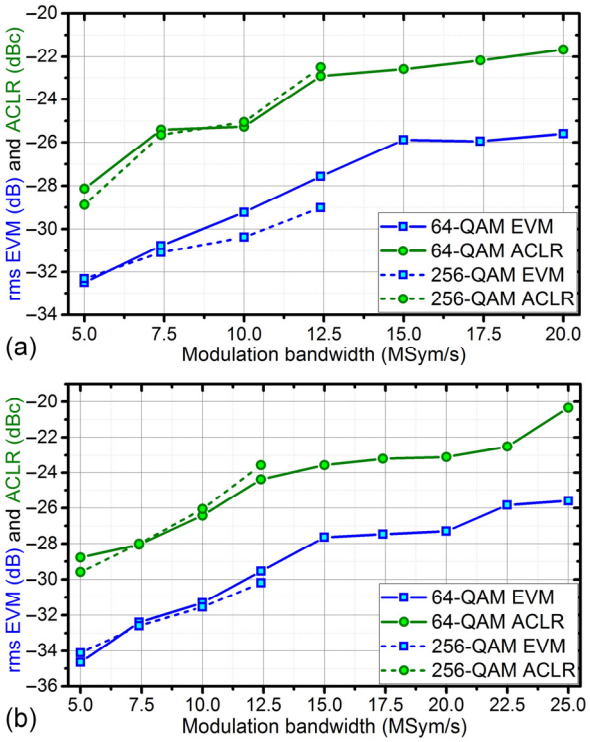


Figure 91 – Measurement results for 64QAM and 256QAM with different symbol rates at (a) 2.4GHz and (b) 2.8GHz.

Figure 92 shows the measured far-out-of-band spectrum of the introduced PA. Sampling images are suppressed below –30.3dBc. The out-of-band noise and the ACLR

degradation due to the supply switching can be improved by further reducing the duration and amplitude of the glitches at the Class-G supply modulator output by design optimizations.

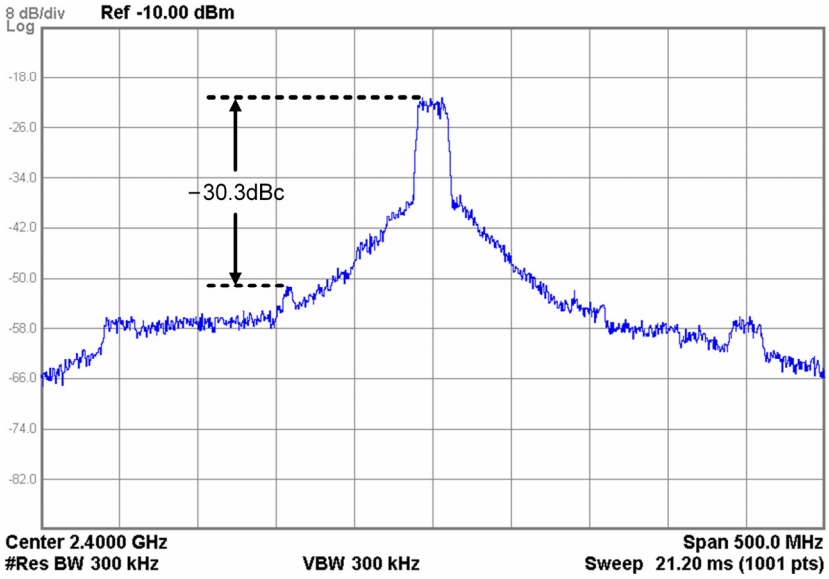


Figure 92 – Measured far-out-of-band spectrum for +17.5dBm 20MSym/s 64QAM at 2.4GHz.

5.3.2.4 Modulation Performance when Backing-Off the Average PA P_{out}

Finally, the average PA P_{out} is reduced to examine the modulation performance in deep PBO. Figure 93 and Figure 94 show the efficiency and linearity results for 10MSym/s 64QAM, respectively. Superior PA average efficiency is achieved up to deep PBO. At 2.4/2.8 GHz, the PA average DE is 23/21.1% at +12.8/+13.6dBm average PA P_{out}, which achieves 2.28/1.82× enhancement over Class-B operation. The rms EVM is lower than −25dB up to the 14dB PBO of average P_{out} at both 2.4GHz and 2.8 GHz, showing excellent in-band linearity performance. EVM and ACLR degradations are observed in deep PBO

(Figure 94). This is mainly due to AM quantization errors at low PA P_{out} levels, which can be improved by increasing the bit number of the RF power DAC.

Compared with recent CMOS PAs with PBO efficiency enhancement (Table 10), the introduced design advances the state-of-the-art PBO efficiency enhancement with high-linearity and a compact area.

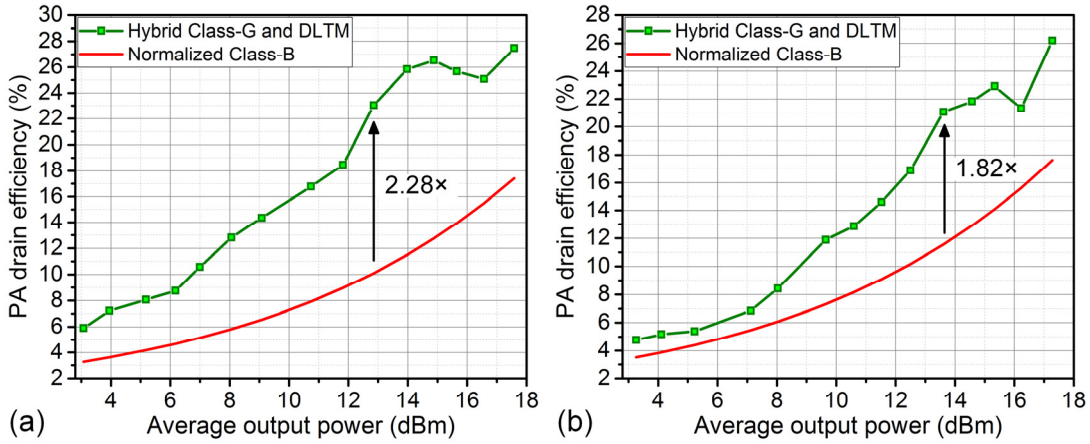


Figure 93 – Measured PA DE when backing off the average P_{out} for 10MSym/s 64QAM at (a) 2.4GHz and (b) 2.8GHz.

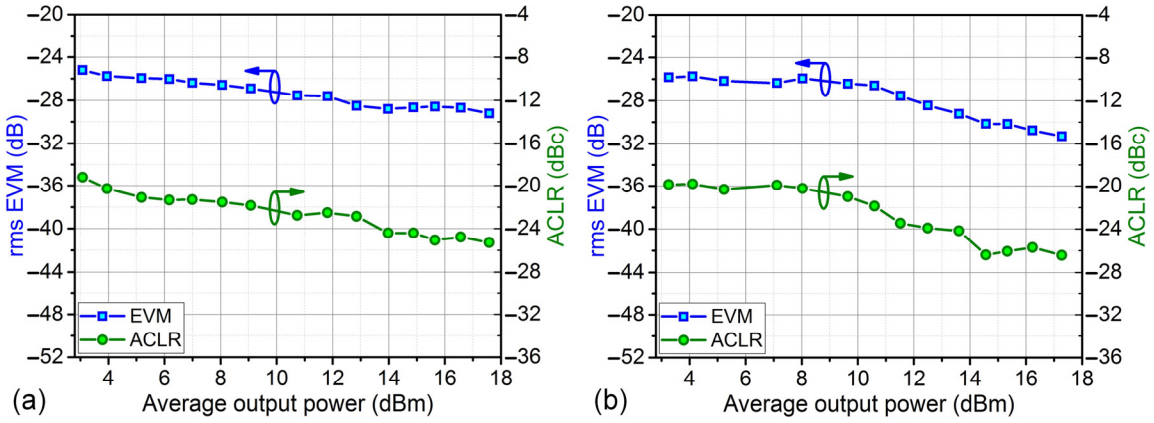


Figure 94 – Measured rms EVM (in-band linearity) and ACLR (OOB linearity) when backing off the average P_{out} for 10MSym/s 64QAM at (a) 2.4GHz and (b) 2.8GHz.

Table 10 – Performance comparison with other PBO efficiency enhanced CMOS PAs

	Freq. (GHz)	Peak P_{out} (dBm)	Peak η (%)	η at 6 dB PBO (%)	η at 12 dB PBO (%)	η improve at 6 dB PBO ‡	η improve at 12 dB PBO ‡	Average P_{out} (dBm)	Average η (%)	η improve for modulation ‡	EVM (dB)	ACLR (dBc)	Area (mm^2)	CMOS Tech.	Mode switch	PBO efficiency enhancement technique
D. Kang T-MTT Oct. '13*	1.85	30.2	48 (PAE)	46†, †† (PAE)	37†, †† (PAE)	1.9×	3.1×	26 16QAM	34.1 (PAE) 16QAM	1.2×	−31.1	−34.2	2.42	180nm	dynamic	ET
S. Hu JSSC May '15	3.8	27.3	30.2 (DE)	21.5 (DE)	9.6 (DE)	1.4×	1.3×	21.8 16QAM	22.1 (DE) 16QAM	1.4×	−25	−21.8	2.1	65nm	dynamic	Doherty
Y. Lu JSSC Dec. '13	2.2	23.3	43 (DE)	33† (DE)	15† (DE)	1.5×	1.4×	16.8 64QAM	24.5 (DE) 64QAM	1.2×	−28	WLAN mask	6.25 (TX)	65nm	dynamic	1b LM
S. M. Yoo JSSC May '13*	2.15	24.3	43.5 (PAE)	36.5 (PAE)	17.8† (PAE)	1.7×	1.6×	16.8 64QAM	33 (PAE) 64	1.8×	−30.8	N.A.	1.68	65nm	dynamic	1b Class-G supply
K. Onizuka ISSCC '13	1.8	27.2	30 (PAE)	22† (PAE)	9† (PAE)	1.5×	1.2×	21.3 64QAM	18 (PAE) 64QAM	1.2×	−22	−30	5.2	65nm	dynamic	1b Class-G supply (effective)
W. Tai JSSC July '12	2.4	31.5	27 (PAE)	20 (PAE)	10.8† (PAE)	1.5×	1.6×	22.7 16QAM	12 (PAE) 16QAM	1.2×	−28	WLAN mask	3.12	45nm	dynamic	outphasing + 3b current
P. A. Godoy JSSC Oct. '12*	2.4	27.7	45.1 (PAE)	38† (PAE)	22† (PAE)	1.7×	2×	20.2 64QAM	27.6 (PAE) 64QAM	1.5×	−31.4	N.A.	4	65nm	dynamic	outphasing + 2b Class-G supply
E. Kaymaksut JSSC Sept. '15	1.9	28.0	34.0 (PAE)	25.5 (PAE)	19.7 (PAE)	1.5×	2.3×	23.4 16QAM	23.3 (PAE) 16QAM	1.2×	−23	−30	3	40nm	static	Doherty + 1b LM
S. Hu JSSC Mar. '16	3.7	26.7	40.2 (DE)	37.0 (DE)	26.2 (DE)	1.8×	2.6×	20.8 16QAM	28.8 (DE) 16QAM	1.4×	−24	−21	3.2	65nm	dynamic	Doherty + 1b Class-G supply
	4.3	26.1	36.2 (DE)	29.3 (DE)	23.6 (DE)	1.7×	2.8×	20.1 16QAM	27.2 (DE) 16QAM	1.6×	−30	−26.5				
This work	**2.4**	**24.6**	**45.6 (DE)**	**41.2 (DE)**	**21.8 (DE)**	**2.1×**	**2.2×**	**17.6 64QAM**	**27.5 (DE) 64QAM**	**1.6×**	**−29.2 10MSym/s**	**−25.3 10MSym/s**	**1.9**	**65nm**	**dynamic**	**1b Class-G supply + DLTM (6b LM)**
											−25.6 20MSym/s	**−21.7 20MSym/s**				
								17.3 256QAM	**26.7 (DE) 256QAM**	**1.6×**	**−30.4 10MSym/s**	**−25.1 10MSym/s**				
	2.8	**24.4**	**45.8 (DE)**	**37.5 (DE)**	**18.4 (DE)**	**1.9×**	**1.8×**	**17.3 64QAM**	**26.2 (DE) 64QAM**	**1.5×**	**−31.3 10MSym/s**	**−26.4 10MSym/s**				
											−25.6 25MSym/s	**−20.3 25MSym/s**				
								17 256QAM	**24.1 (DE) 256QAM**	**1.4×**	**−31.5 10MSym/s**	**−26.1 10MSym/s**				

* using off-chip components for PA output matching. ‡ in comparison with the Class-B operation.

† estimated from the reported figures. †† not including the power consumption of the supply modulator.

5.4 Summary

This chapter presents a mixed-signal PA with hybrid real-time Class-G and DLTM operations. The hybrid PA operations enhance the PA efficiency in deep PBO. Moreover, a new DLTM scheme is introduced to achieve PA PBO efficiency peaking. The real-time mixed-signal PA operation ensures the accuracy of the PA output signal. The digitally controlled LM network substantially extends the PA carrier bandwidth. The introduced PA architecture is particularly suitable for SoC integrations in deeply scaled CMOS processes, which readily offer mixed-signal controls with fine timing resolutions [6]. A prototype in a standard 65nm bulk CMOS process is demonstrated. This is the first LM PA fully integrated in CMOS supporting 256QAM.

CHAPTER 6. A 28GHZ/37GHZ/39GHZ MULTIBAND LINEAR DOHERTY PA FOR 5G MASSIVE MIMO APPLICATIONS

The mm-wave fifth-generation (5G) systems will extensively leverage the massive MIMO architecture to improve the link performance. These array systems will employ many PAs operating at moderate P_{out}, e.g., 16 PAs each with +7dBm P_{out} [94]. The PA power efficiency is of paramount importance in MIMO systems for battery life and thermal management. Due to the spectrum efficient modulations with high peak-to-average power ratios, both PA peak efficiency and PBO efficiency are critical. To achieve 5G Gbps data rates with complex modulations, envelope tracking PAs require high-speed/high-precision supply modulators, and outphasing PAs need high-speed baseband computation, both of which pose substantial challenges in practice. Although Doherty PAs support high data rates, existing silicon mm-wave Doherty PAs exhibit very limited PBO efficiency enhancement, mainly due to inefficient Doherty power combiners and imperfect main/auxiliary PA cooperation [96], [97].

In addition, multiple mm-wave frequency bands, including spectra around 28, 37, and 39GHz, have been opened for 5G development. Multiband operations will greatly facilitate MIMO frequency diversity and future cross-network/international roaming. Together with existing wideband antennas, a single multiband PA will enable future ultra-

compact multiband massive MIMO 5G systems. However, the carrier bandwidth of a conventional Doherty PA is often limited by the Doherty power combiner.

To address these unmet challenges, a fully integrated 28/37/39GHz multiband Doherty PA for 5G massive MIMO applications is introduced [95]. Both PA PBO efficiency and carrier bandwidth are significantly enhanced by a new transformer-based Doherty power combiner. Moreover, a power-aware adaptive uneven feeding scheme provides optimum main/auxiliary PA cooperation. A prototype is implemented in 130nm SiGe BiCMOS. It achieves +16.8/+17.1/+17dBm peak P_{out}, 18.2/17.1/16.6dB peak power gain, 29.4/27.6/28.2% peak collector efficiency (CE), and 20.3/22.6/21.4% peak PAE at 28/37/39GHz. Its Doherty operation achieves 1.72/1.92/1.62× and 3.39/3.86/3.51× efficiency enhancement at 5.9/6/6.7dB PBO over Class-B and Class-A PAs at 28/37/39GHz respectively. Amplifying 3Gb/s 64QAM with high efficiency and linearity is demonstrated in all these three 5G bands.

6.1 A Broadband and Low-Loss On-Chip Doherty Output Network

Figure 95 shows the conventional and introduced Doherty output networks. Compared with conventional designs, the introduced new transformer-based Doherty output network significantly reduces the ITRs in PBO while achieving the same peak P_{out}. This directly improves the PBO PE and enhances the Doherty PA PBO efficiency.

Moreover, the reduced ITR broadens the Doherty PA carrier bandwidth due to the decreased loaded quality factor of the passive network.

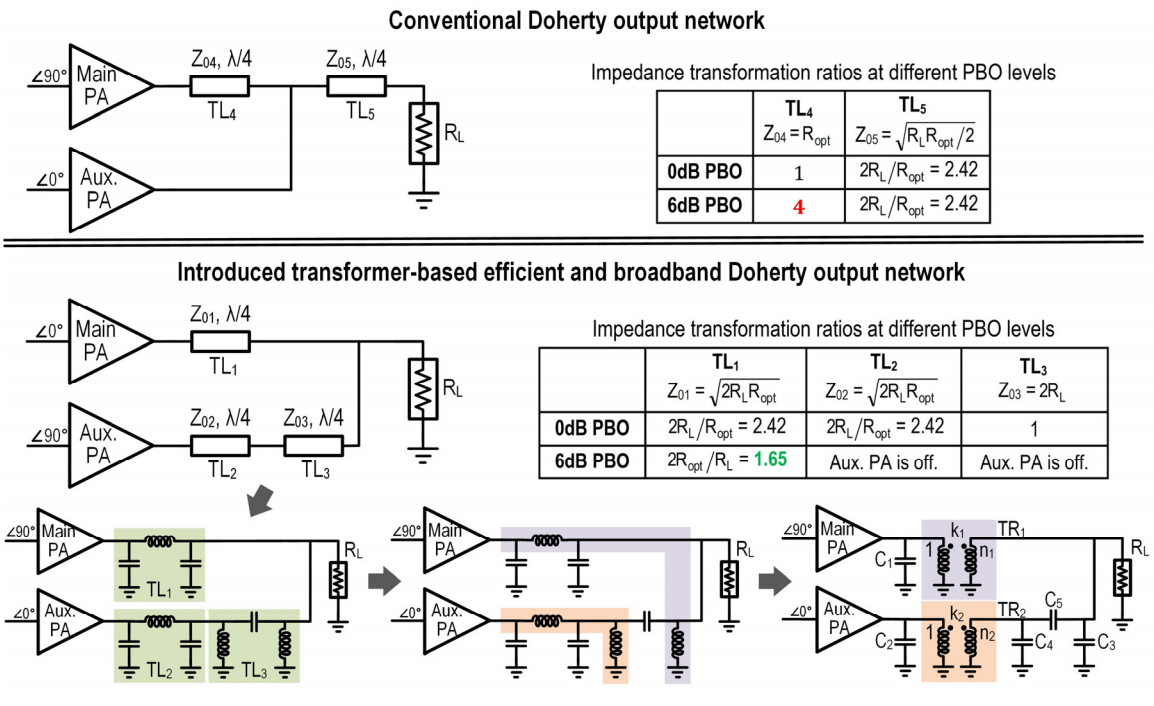


Figure 95 – Introduced transformer-based Doherty power combiner achieving reduced ITRs in PBO with the same peak P_{out} (R_{opt} = 41.3Ω).

The introduced Doherty output network is designed using on-chip transformers to achieve compactness. Transmission lines TL_1, TL_2, and TL_3 are first approximated by low-, low-, and high-pass π-networks, respectively. Then, the four inductors are absorbed into two on-chip transformers. The two shunt inductors from TL_3 form the magnetization inductors, and the series inductors from TL_1 and TL_2 are incorporated as leakage inductors. Three λ/4 TLs are thus realized in a two-transformer footprint. Capacitors C_1, C_2, and C_3 absorb PA device or pad parasitics.

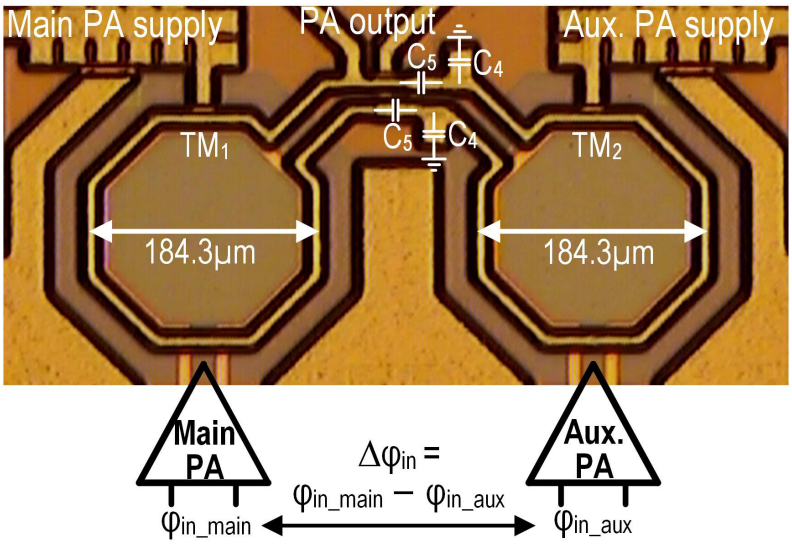


Figure 96 – Microphotograph of the implemented Doherty output network.

Based on this process of network synthesis, the closed-form equations of the design parameters in the introduced Doherty output network are derived for given n_1, k_1, n_2, and load-pull impedance R_{opt}:

$$k_2 = \frac{\sqrt{n_2^2 R_{opt}/(2R_L)+4} - n_2\sqrt{R_{opt}/(2R_L)}}{2}, \tag{63}$$

$$L_{P1} = \frac{k_1\sqrt{2R_L R_{opt}}}{\omega n_1(1-k_1^2)}, \tag{64}$$

$$L_{P2} = \frac{n_1 k_1\sqrt{2R_L R_{opt}}}{\omega n_2^2(1-k_1^2)}, \tag{65}$$

$$C_1 = \frac{n_1}{\omega k_1\sqrt{2R_L R_{opt}}}, \tag{66}$$

$$C_2 = \frac{n_2^2(1-k_1^2)}{\omega n_1 k_1(1-k_2^2)\sqrt{2R_L R_{opt}}}, \tag{67}$$

$$C_3 = (\frac{k_1}{n_1})^2 C_1, \tag{68}$$

$$C_4 = (\frac{k_2}{n_2})^2 C_2, \tag{69}$$

$$C_5 = \frac{1-k_1^2}{\omega n_1 k_1 \sqrt{2R_L R_{opt}}}. \tag{70}$$

3D EM simulations verify the Doherty LM behavior (Figure 97) with enhanced PBO PE (Figure 98) and carrier bandwidth (Figure 99).

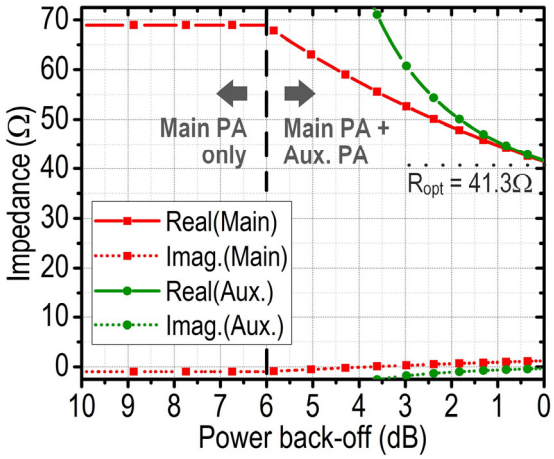


Figure 97 – Effective load impedance for the main and auxiliary PAs based on the EM-simulated Doherty output passive network.

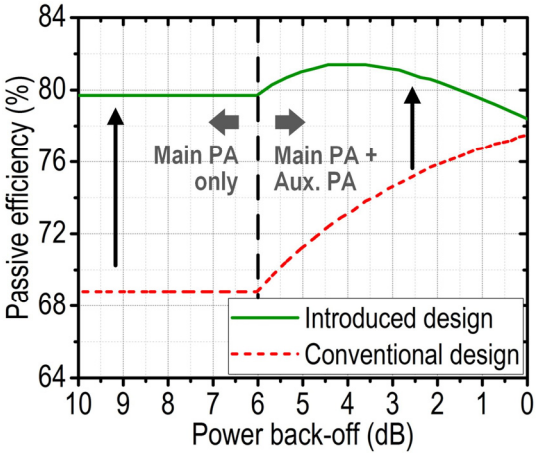


Figure 98 – Simulated PE of the introduced Doherty output network and comparison with a conventional design.

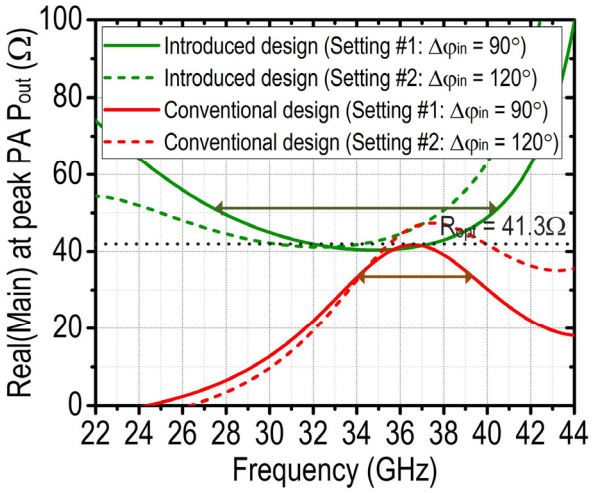


Figure 99 – Simulated bandwidth performance of the introduced Doherty output network and comparison with a conventional design.

6.2 Power-Dependent Doherty PA Uneven-Feeding Scheme

For optimum Doherty operation, the auxiliary PA should provide a rapidly increasing current after it is turned on. Conventionally, this is achieved by adaptively biasing the auxiliary PA [42], [97]. However, adaptive biasing circuit can become challenging for 5G applications, since it is loaded by large PA transistors, and it needs to track the real-time envelope that has ~3× bandwidth expansion over the modulated signal. A power-aware adaptive uneven feeding scheme is introduced (Figure 100). The input conductance of the Class-C auxiliary PA increases noticeably for increased input power (P_{in}), while that of the Class-AB main PA remains almost the same. This effect is leveraged to dynamically modulate the auxiliary driver load and achieve enhanced power gain when Pin increases. Thus, compared with the main path, the auxiliary PA final stage is fed by a larger Pin in the high-power region. This facilitates the rapid auxiliary PA output current

increase and achieves optimum Doherty operation without hardware overhead or modulation rate limitation.

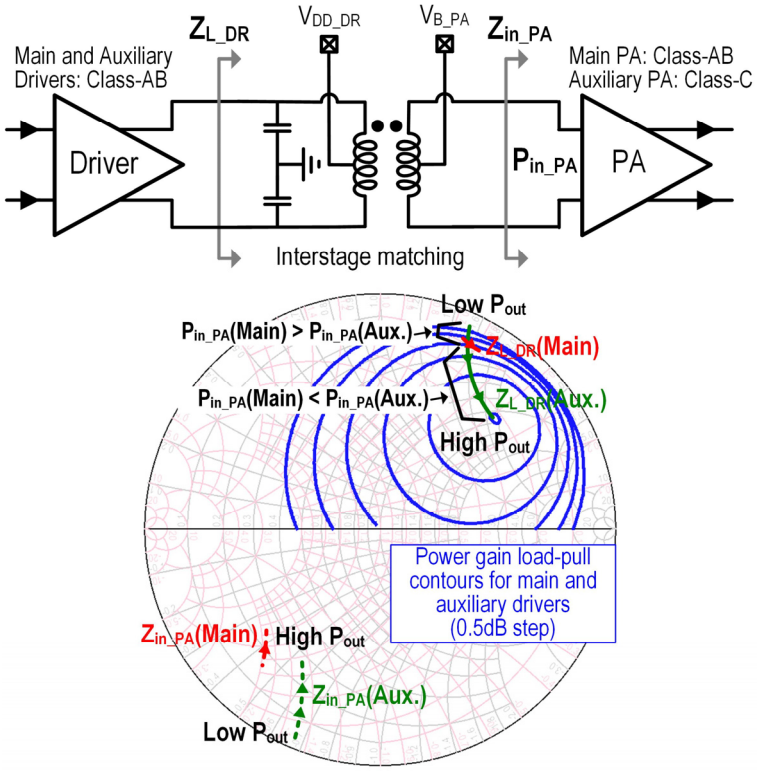


Figure 100 – Introduced power-dependent Doherty PA uneven-feeding scheme.

6.3 Experimental Results

Figure 101 shows the schematic of the PA. An on-chip differential quadrature hybrid first performs input power split and 90° phase shift. The relative phase of main/auxiliary paths is adjusted using 9-section varactor-loaded TLs to further extend the Doherty PA carrier bandwidth (Figure 99) [78], [90]. Different varactor settings are used for 28GHz and 37/39GHz (Table 11). The high-order networks formed by the varactor-loaded TLs also ensure wideband input matching for different settings. Each PA path

comprises a driver stage and a PA stage. The interstage matching is designed to realize the introduced power-dependent uneven-feeding scheme.

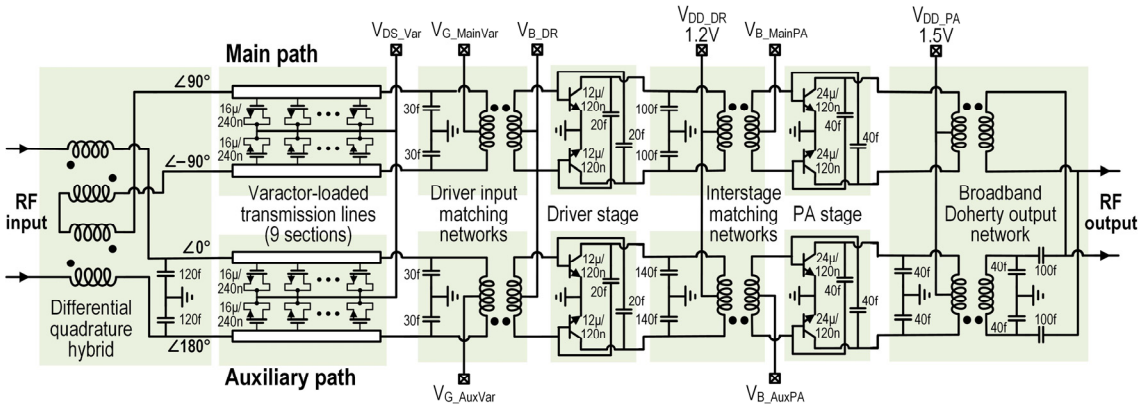


Figure 101 – Schematic of the implemented 28/37/39GHz linear Doherty PA

The PA chip occupies 1.76mm^2 (Figure 102). Measured small-signal S-parameters, saturated P_{out} (P_{sat}), and P_{1dB} for the two settings show broadband performance (Figure 103). The PA achieves a −3dB S_{21} bandwidth of 23.3−39.7GHz (52.1%). The −1dB P_{sat} bandwidth is 27.7% and 33.3% for the two settings, and is collectively 28−42GHz (40%). Figure 104-Figure 106 show the large-signal CW test results. Owing to the introduced Doherty output network and adaptive feeding scheme, superior PBO efficiency improvement is achieved over Class-B and Class-A PAs in all three 5G bands. Excellent amplitude/phase linearity is also observed.

Table 11 – Dual varactor control settings that cover three mm-wave 5G bands

	Target band(s)	$V_{DS\_Var} - V_{G\_MainVar}$	$V_{DS\_Var} - V_{G\_AuxVar}$	$\Delta\varphi_{in} = \varphi_{in\_main} - \varphi_{in\_aux}$
Setting #1	28GHz	0.5	0	120°
Setting #2	37GHz, 39GHz	0	0.5	90°

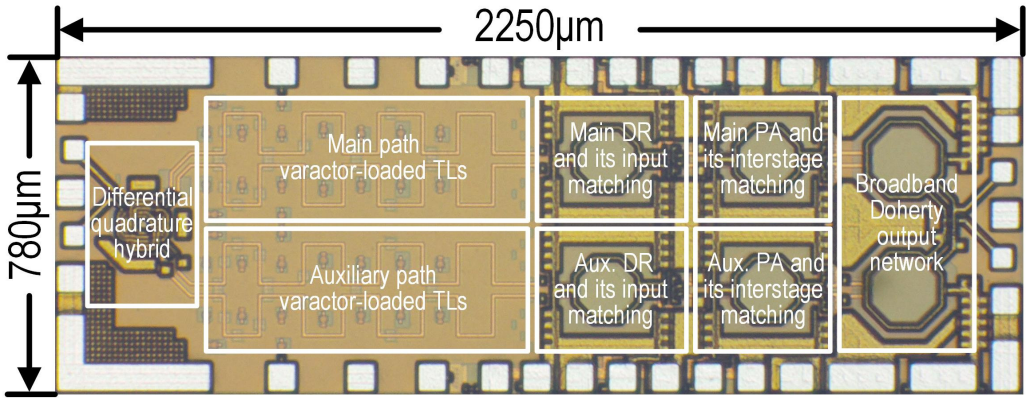


Figure 102 – Chip microphotograph.

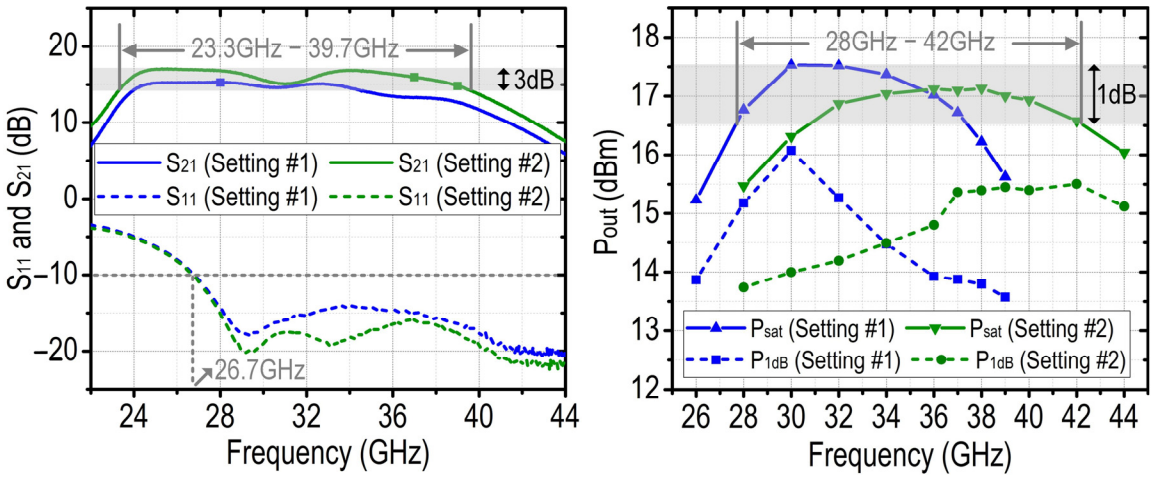


Figure 103 – Measured small-signal S-parameters and large-signal P_{sat}/P_{1dB}.

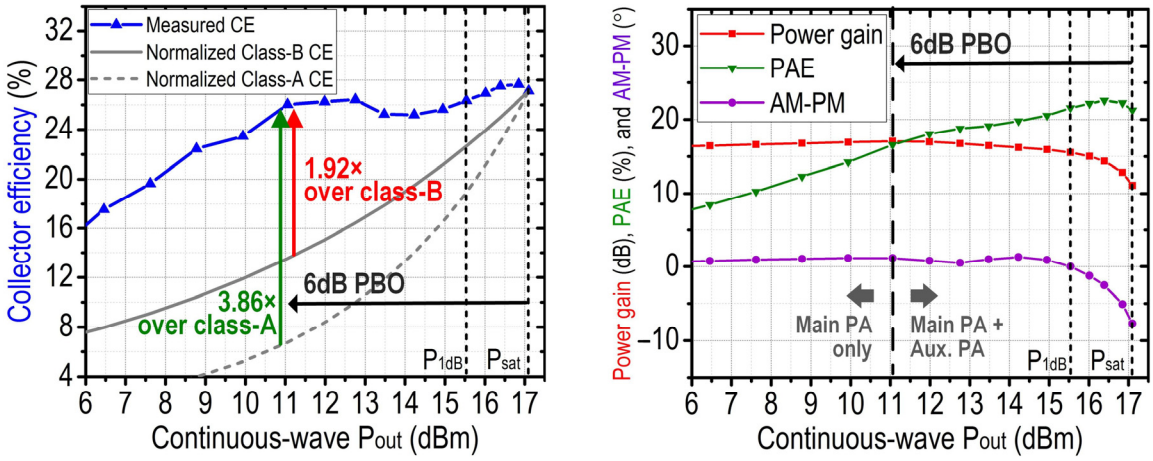


Figure 104 – Measured CW efficiency and linearity performance at 37GHz.

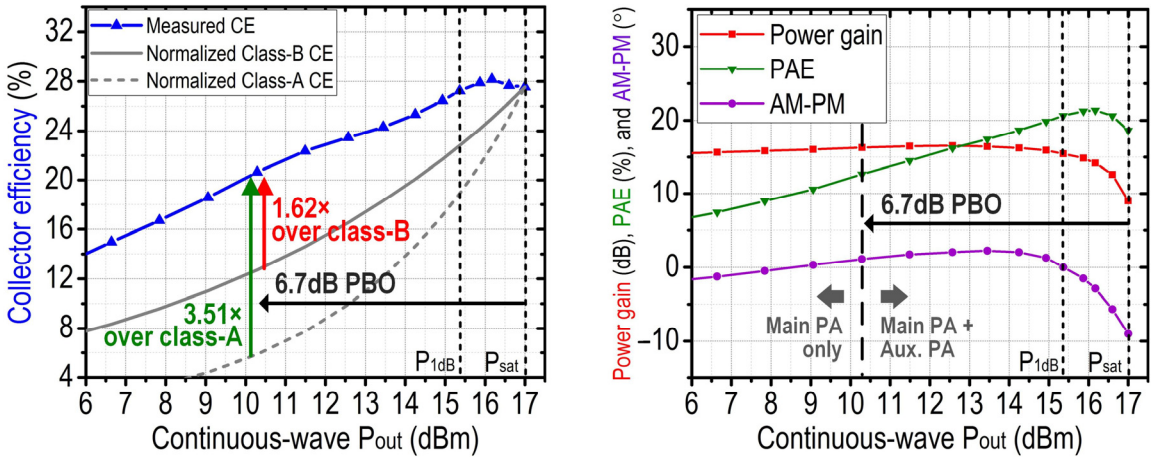


Figure 105 – Measured CW efficiency and linearity performance at 39GHz.

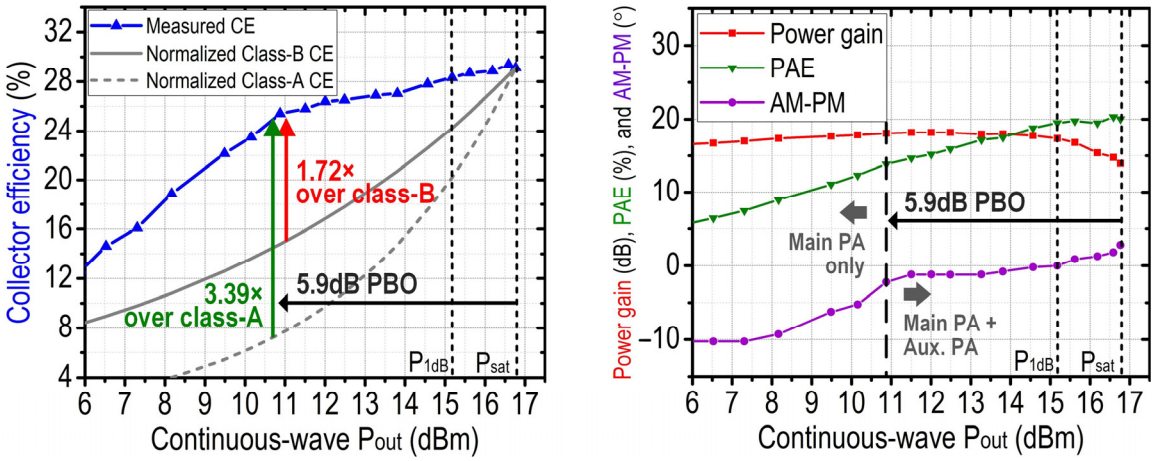


Figure 106 – Measured CW efficiency and linearity performance at 28GHz.

The PA is measured using 0.5GSym/s 64-QAM (3Gb/s) signals (Figure 107-Figure 109). Without predistortion, the EVM and ACLR are better than −27dB and −28.2dBc with average P_{out}>+9.2dBm in all three 5G bands. These 64-QAM tests show substantial PA average efficiency improvement over normalized Class-B and Class-A PAs in all three bands, verifying the multiband Doherty performance in high-speed dynamic operations. The PA also supports 1GSym/s 64QAM (6Gb/s) at 28GHz as the highest demonstrated data rate for 28GHz silicon PAs (Figure 110).

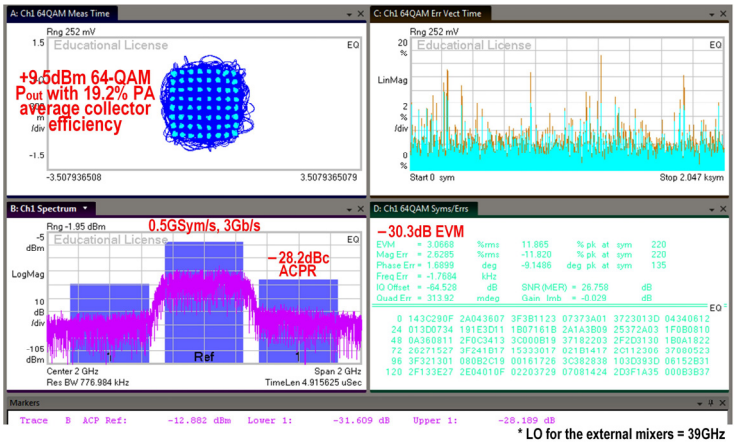


Figure 107 – Measured 500MSym/s 64QAM (3Gb/s) at 37GHz.

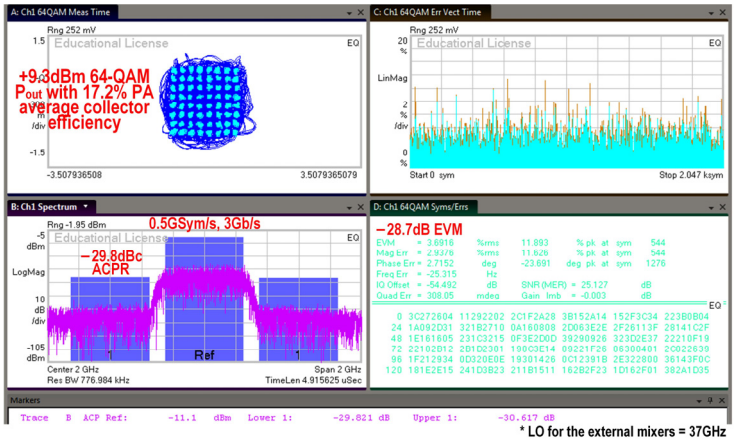


Figure 108 – Measured 500MSym/s 64QAM (3Gb/s) at 39GHz.

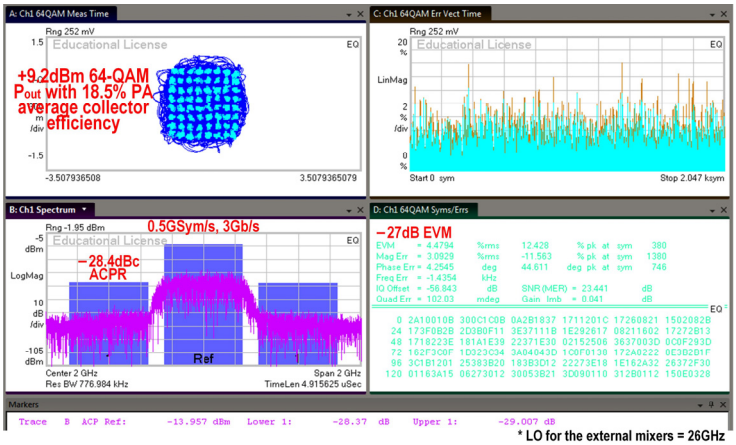


Figure 109 – Measured 500MSym/s 64QAM (3Gb/s) at 28GHz.

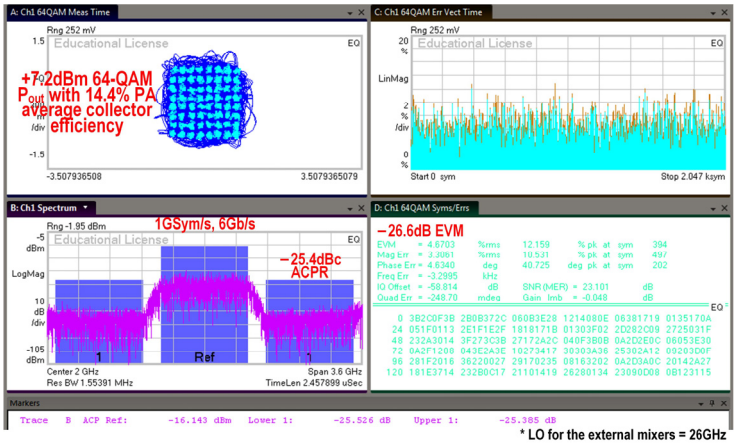


Figure 110 – Measured 1GSym/s 64QAM (6Gb/s) at 28GHz.

6.4 Summary

Table 12 summarizes the performance of the introduced PA. This PA advances the state of the art for Doherty, wideband, and 5G silicon PAs in the mm-wave bands.

Table 12 – Comparison with recently reported mm-wave silicon PAs

	Our work			Mm-wave Doherty PA		Mm-wave wideband PA		5G PA
				A. Agah, JSSC Oct. '13	E. Kaymaksut, T-MTT Apr. '15	C. Chappidi, ISSCC '16	M. Bassi, JSSC July '15	S. Shakib, ISSCC '16
Technology	130nm SiGe			45nm SOI CMOS	40nm CMOS	130nm SiGe	28nm CMOS	28nm CMOS
Architecture	Multiband Doherty			Slow-wave CPW Doherty†	Doherty	Asymmetric combiner	Inductively coupled resonator	Inductive source degeneration
Supply (V)	1.5			2.5	1.5	4	1	1
S_{21} −3dB BW (GHz)	23.3–39.7 (52%)			N.A.	60–81 (30%)	32–60 (61%)*	40–67 (51%)	27–31 (14%)*
P_{SAT} −1dB BW (GHz)	28–42 (40%)			N.A.	58–77 (28%)	40–65 (48%)	46–62 (30%)	28–31 (10%)*
Area (mm²)	1.76			0.64	0.96	1.02	0.33	0.16**
Frequency (GHz)	28	37	39	42	72	55	53	30
Power gain (dB)	18.2	17.1	16.6	7	18.6*	18.8	13	15.7
P_{SAT} (dBm)	+16.8	+17.1	+17	+18	+21	+23.6	+13.3	+14
P_{1dB} (dBm)	+15.2	+15.5	+15.4	+14.5*	+19.2	+19.9	+12	+13.2
Peak η	29.4% CE 20.3% PAE	27.6% CE 22.6% PAE	28.2% CE 21.4% PAE	33% DE 23% PAE	20.7% DE 13.6% PAE	27.7% PAE	16% PAE	35.5% PAE
η @ P_{1dB}	28.3% CE 19.5% PAE	26.4% CE 21.6% PAE	27.2% CE 20.7% PAE	26% DE* 19% PAE*	17.6% DE* 12.4% PAE	15.7% PAE	14% PAE	34.3% PAE
η @ PBO	25.4% CE 13.9% PAE @5.9dB PBO	26% CE 16.6% PAE @6dB PBO	20.6% CE 12.6% PAE @6.7dB PBO	24% DE 17% PAE @6dB PBO	11.5% DE* 7% PAE @6dB PBO	7% PAE* @6dB PBO	5% PAE* @6dB PBO	10% PAE @9.6dB PBO
Modulation results	64-QAM 500MSym/s +9.2dBm −27dB EVM −28.4dBc ACPR 18.5% CE 64-QAM 1GSym/s +7.2dBm −26.6dB EVM −25.4dBc ACPR 14.4% CE	64-QAM 500MSym/s +9.5dBm −30.3dB EVM −28.2dBc ACPR 19.2% CE	64-QAM 500MSym/s +9.3dBm −28.7dB EVM −29.8dBc ACPR 17.2% CE	N.A.	64-QAM 100MSym/s +15.9dBm −25.6dB EVM 7.2% PAE	64-QAM 500MSym/s +12.8dBm −25.5dB EVM	N.A.	64-QAM 250MSym/s +4.2dBm −25dB EVM −26.4dBc ACPR 9% PAE

* Read from the reported figures. ** Without pads. † Statically tuned biasing.

CHAPTER 7. CONCLUSIONS

7.1 Research Summary

Future-generation wireless networks pose unmet challenges for conventional communication circuits and systems. To satisfy the voracious demand for higher data rates using scarce spectrum resources, modern wireless networks often employ sophisticated modulations such as high-order QAM. They routinely require high-quality communication links. Consequently, energy efficiency is often compromised in conventional solutions. Conventional solutions also entail extraordinary challenges when extended to future civilian and defense electronics featuring wide bandwidth.

My approaches to addressing these challenges fuse state-of-the-art mixed-signal techniques with large-signal RF/mm-wave and holistically design active circuits with on-chip EM structures/networks by drawing on knowledge from diverse disciplines including those pertaining to devices, EMs, and microwaves. My research introduces new circuit topologies and system architectures that eliminate the tradeoffs and the limits of conventional solutions. In addition, my approaches are conducive to SoC in silicon for future-generation communication networks.

In the research of energy-efficient communication circuits and systems, my research eliminates the tradeoff between PA efficiency and linearity by fusing state-of-the-art digital and analog (i.e., mixed-signal) techniques with large-signal RF. Furthermore,

my research demonstrates new hybrid mixed-signal PA/transmitter architectures achieving significant efficiency enhancement.

In the research of broadband communication circuits and systems, my research innovates EM structures in silicon to achieve RF/mm-wave passive components and networks with inherently wide bandwidth. Mixed-signal-assisted large-signal RF operations further enable in-field reconfigurations and thus broadband operations for active circuits.

7.2 Key Research Contributions

1. Silicon demonstration of a digital Doherty PA architecture
2. First-time silicon demonstration and analysis of a PCT-based Doherty PA output network
3. First-time comprehensive analysis and silicon verification for the Doherty PA under antenna impedance variations
4. First-time silicon demonstration and analysis of a hybrid Class-G Doherty PA efficiency enhancement technique
5. First-time silicon demonstration and analysis of a mixed-signal PA linearization technique
6. First-time silicon demonstration of a carrier bandwidth extension technique for Doherty PAs

7. First-time silicon demonstration and analysis of a hybrid Class-G and DLTM PA efficiency enhancement technique
8. First-time silicon demonstration and analysis of a PA PBO efficiency peaking technique
9. Comprehensive analysis of transformer-based PA LM networks
10. First-time silicon demonstration of a 28/37/39GHz multiband mm-wave linear Doherty PA for 5G
11. First-time silicon demonstration and analysis of a transformer-based broadband and low-loss on-chip Doherty output network
12. First-time silicon demonstration of a power-dependent Doherty PA uneven-feeding scheme based on a "driver-PA co-design" method

7.3 Research Publications

7.3.1 First-Author Journal Publications

1. S. Hu, S. Kousai, and H. Wang, "A Compact Broadband Mixed-Signal Power Amplifier in Bulk CMOS with Hybrid Class-G and Dynamic Load Trajectory Manipulation," accepted and to appear in *IEEE Journal of Solid-State Circuits (JSSC)*.
2. S. Hu, S. Kousai, and H. Wang, "A Broadband Mixed-Signal CMOS Power Amplifier with a Hybrid Class-G Doherty Efficiency Enhancement Technique," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 51, no. 3, pp. 598–613, Mar. 2016.

3. S. Hu, S. Kousai, J. Park, O. Chlieh, and H. Wang, "Design of a Transformer-Based Reconfigurable Digital Polar Doherty Power Amplifier Fully Integrated in Bulk CMOS," the Special Issue for RFIC, *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 50, no. 5, pp. 1094–1106, May 2015.
4. S. Hu, S. Kousai, and H. Wang, "Antenna Impedance Variation Compensation by Exploiting a Digital Doherty Power Amplifier Architecture," the Special Issue on Power Amplifiers, *IEEE Transactions on Microwave Theory and Techniques (T-MTT)*, vol. 63, no. 2, pp. 580–597, Feb. 2015.

7.3.2 Co-Author Journal Publications

1. J. Park, S. Hu, Y. Wang, and H. Wang, "A Highly Linear Dual-Band Mixed-Mode Polar Power Amplifier in CMOS with an Ultra-Compact Output Network," the Special Issue for CICC, *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 51, no. 8, pp. 1756–1770, Aug. 2016.
2. H. Wang, S. Kousai, K. Onizuka, and S. Hu, "The Wireless Workhorse: Mixed-Signal Power Amplifiers Leverage Digital and Analog Techniques to Enhance Large-Signal RF Operations," *IEEE Microwave Magazine*, vol. 16, no. 9, pp. 36–63, Oct. 2015. (IEEE Microwave Magazine Best Paper Award)
3. T. Chi, J. Luo, S. Hu, and H. Wang, "A Multi-Phase Sub-Harmonic Injection Locking Technique for Bandwidth Extension in Silicon-Based THz Signal Generation," the

Special Issue for CICC, *IEEE Journal of Solid-State Circuits (JSSC)*, vol.50, no.8, pp.1861−1873, Aug. 2015.

7.3.3 First-Author Conference Publications

1. S. Hu, F. Wang, and H. Wang, "A 28GHz/37GHz/39GHz Multi-Band Linear Doherty Power Amplifier for 5G Massive MIMO Applications," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2017.
2. S. Hu, S. Kousai, and H. Wang, "A Compact Broadband Mixed-Signal Power Amplifier in Bulk CMOS with Hybrid Class-G and Dynamic Load Trajectory Manipulation Operations," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2016.
3. S. Hu, F. Wang, and H. Wang, "A Transformer-Based Inverted Complementary Cross-Coupled VCO with a 193.3dBc/Hz FoM and 13kHz $1/f^3$ Noise Corner," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2016.
4. S. Hu, S. Kousai, and H. Wang, "A Broadband CMOS Digital Power Amplifier with Hybrid Class-G Doherty Efficiency Enhancement," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2015. (Chip photo featured on the front cover of February 2016 issue of IEEE Microwave Magazine)
5. S. Hu and H. Wang, "A Hybrid Technique for PA Back-Off Efficiency Enhancement – A Broadband Mixed-Signal Class-G Doherty PA in CMOS," *IEEE Power Amplifier Symposium*, 2015.

6. S. Hu and H. Wang, "A Digital-Intensive Highly-Reconfigurable CMOS Doherty Power Amplifier Resilient to Antenna Mismatch," *Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, 2015.
7. S. Hu, S. Kousai, J. Park, O. Chlieh, and H. Wang, "A +27.3dBm Transformer-Based Digital Doherty Polar Power Amplifier Fully Integrated in Bulk CMOS," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2014. (Best Student Paper Award, First Place)

7.3.4 Co-Author Conference Publications

1. H. Wang, S. Hu, and S. Kousai, "Mixed-Signal Doherty Power Amplifiers in CMOS," invited to the Special Session "Celebrating the 80th Anniversary of the Doherty Patent", *IEEE International Microwave Symposium (IMS)*, 2016.
2. J. Park, S. Hu, Y. Wang, and H. Wang, "A Highly Linear Dual-Band Mixed-Mode Polar Power Amplifier in CMOS with an Ultra-Compact Output Network," *IEEE Custom Integrated Circuits Conference (CICC)*, 2015. (Best Student Paper Award)
3. S. Kousai, K. Onizuka, S. Hu, H. Wang, and A. Hajimiri, "A New Wave of CMOS Power Amplifier Innovations: Fusing Digital and Analog Techniques with Large Signal RF Operations," *IEEE Custom Integrated Circuits Conference (CICC)*, 2014.
4. T. Chi, J. Luo, S. Hu, and H. Wang, "A Multi-Phase Sub-Harmonic Injection Locking Technique for Bandwidth Extension in Silicon-Based THz Signal Generation," *IEEE*

Custom Integrated Circuits Conference (CICC), 2014. (Best Student Paper Award Finalist)

5. H. Wang and S. Hu, "Enhancing Doherty Power Amplifier Operation by A Digitally Reconfigurable Architecture," *IEEE Power Amplifier Symposium*, 2014.
6. J. Park, T. Chi, S. Hu, M. Styczynski, and H. Wang, "A Scalable CMOS Cell Sensor Array," *Semiconductor Research Corporation (SRC) TECHCON*, 2014.

7.3.5 Book Chapter

1. S. Hu, S. Kousai, J. Park, O. Chlieh, and H. Wang, "A Transformer-Based Reconfigurable Digital Polar Doherty Power Amplifier Fully Integrated in Bulk CMOS," *RF and Mm-Wave Power Generation in Silicon*. Academic Press, Elsevier, Dec. 2015.

7.4 Research Awards

- 2016 Georgia Tech ECE Graduate Research Assistant Excellence Award
- 2016 IEEE Microwave Magazine Best Paper Award (Co-recipient)
- 2016 IEEE Solid-State Circuits Society Predoctoral Achievement Award
- 2015 IEEE Microwave Theory and Techniques Society Graduate Fellowship
- 2015 Best Student Paper Award (Co-recipient), IEEE CICC
- 2014 Best Student Paper Award (First Place), IEEE RFIC Symposium
- 2014 Analog Devices Outstanding Student Designer Award

7.5 Future Research

My research has demonstrated the strength of mixed-signal-assisted large-signal RF and innovative on-chip EM structures/networks. I envision that the holistic design philosophy of digital/analog/RF/mm-wave circuits and EM structures/networks will advance future electronics for communication and emerging applications.

Mixed-signal-assisted RF/mm-wave architectures support low-cost and reliable adaptive operation. In addition to energy efficiency and bandwidth enhancement, which have been demonstrated in my previous research, I believe they can also enable many other significant capabilities in future wireless systems. For example, adaptive interference rejection can allow a wireless device to operate in a congested and contested spectral environment. Software-defined reconfiguration can lead to the design of upgradable and widely deployable military wireless infrastructures. New mixed-signal-assisted RF/mm-wave wireless communication systems can be explored for both commercial and military applications. In parallel, intelligent algorithms that leverage machine-learning techniques can be employed to reduce computational cost for adaptive operations.

My research has demonstrated the bandwidth enhancement of a mm-wave 5G PA by innovative on-chip EM structures and networks. Future wireless communication systems are approaching higher frequencies, which open untapped research opportunities for on-chip EM structures and networks, including not only passive components but also

radiating elements. Moreover, designing on-chip EM structures/networks holistically with digital/analog/RF/mm-wave circuits will enable new ways to create, manipulate, and detect the EM signals. This design methodology would enable remarkable features in future wireless communication systems such as the integration of front-end modules in mm-wave massive MIMO 5G systems.

REFERENCES

[1] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Boston, MA, USA: Artech House, 2006.

[2] F. H. Raab, *et al*., "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.

[3] A. A. M. Saleh and D. C. Cox, "Improving the power-added efficiency of FET amplifiers operating with varying-envelope signals," *IEEE Trans. Microw. Theory Techn.*, vol. 31, no. 1, pp. 51–56, Jan. 1983.

[4] Y. S. Noh and C. S. Park, "An intelligent power amplifier MMIC using a new adaptive bias control circuit for W-CDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 967–970, Jun. 2004.

[5] A. Afsahi, A. Behzad, V. Magoon, and L. E. Larson, "Linearized dual-band power amplifiers with integrated baluns in 65nm CMOS for a 2×2 802.11n MIMO WLAN SoC," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 955–966, May 2010.

[6] R. B. Staszewski, *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.

[7] A. Kavousian, D. K. Su, M. Hekmat, A. Shirvani, and B. Wooley., "A digitally modulated polar CMOS power amplifier with a 20MHz channel bandwidth," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2251–2258, Oct. 2008.

[8] C. D. Presti, F. Carrara, A. Scuderi, P. M. Asbeck, and G. Palmisano, "A 25dBm digitally modulated CMOS power amplifier for WCDMA/EDGE/OFDM with adaptive digital predistortion and efficient power control," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1883–1896, Jul. 2009.

[9] S. Kousai and A. Hajimiri, "An octave-range, watt-level, fully-integrated CMOS switching power mixer array for linearization and back-off-efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3376–3392, Dec. 2009.

[10] D. Chowdhury, L. Ye, E. Alon, and A. M. Niknejad, "An efficient mixed-signal 2.4GHz polar power amplifier in 65nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1796–1809, Aug. 2011.

[11] D. Chowdhury, S. V. Thyagarajan, L. Ye, E. Alon, and A. M. Niknejad, "A fully-integrated efficient CMOS inverse Class-D power amplifier for digital polar transmitters," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1113–1122, May 2012.

[12] L. R. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proc. IRE*, vol. 40, no. 7, pp. 803–806, Jul. 1952.

[13] D. K. Su and W. J. McFarland, "An IC for linearizing RF power amplifiers using envelope elimination and restoration," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2252–2258, Dec. 1998.

[14] P. Reynaert and M. S. J. Steyaert, "A 1.75GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.

[15] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, and F. De Flaviis, "A two-point modulation technique for CMOS power amplifier in polar transmitter architecture," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 1, pp. 31–38, 2008.

[16] Y. Li, J. Lopez, P.-H. Wu, W. Hu, R. Wu, and D. Y. C. Lie, "A SiGe envelope-tracking power amplifier with an integrated CMOS envelope modulator for mobile WiMAX/3GPP LTE transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 10, pp. 2525–2536, 2011.

[17] R. Wu, Y. T. Liu, J. Lopez, C. Schecht, Y. Li, and D. Y. C. Lie, "High-efficiency silicon-based envelope-tracking power amplifier design with envelope shaping for broadband wireless applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2030–2040, Sep. 2013.

[18] D. Kang, B. Park, D. Kim, J. Kim, Y. Cho, and B. Kim, "Envelope-tracking CMOS power amplifier module for LTE applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3763–3773, Oct. 2013.

[19] K. Oishi, *et al.*, "A 1.95GHz fully integrated envelope elimination and restoration CMOS power amplifier using timing alignment technique for WCDMA and LTE," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2915–2924, Dec. 2014.

[20] J. Kim, D. Kim, Y. Cho, D. Kang, B. Park, K. Moon, S. Koo, and B. Kim, "Highly efficient RF transmitter over broad average power range using multilevel envelope-tracking power amplifier," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 62, no. 6, pp. 1648–1657, Jun. 2015.

[21] E. McCune, *Dynamic Power Supply Transmitters: Envelope Tracking, Direct Polar, and Hybrid Combinations*. Cambridge, UK: Cambridge University Press, 2015.

[22] M. Hassan, P. M. Asbeck, and L. E. Larson, "A CMOS dual-switching power-supply modulator with 8% efficiency improvement for 20MHz LTE envelope tracking RF power amplifiers," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2013, pp. 366–367.

[23] P. Arno, M. Thomas, V. Molata, and T. Jerabek, "Envelope modulator for multimode transmitters with AC-coupled multilevel regulators," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2014, pp. 296–297.

[24] S. C. Lee, *et al.*, "A hybrid supply modulator with 10dB ET operation dynamic range achieving a PAE of 42.6% at 27.0dBm PA output power," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2015, pp. 42–43.

[25] F. H. Raab, "Average efficiency of Class-G power amplifiers," *IEEE Trans. Consum. Electron.*, vol. CE-32, no. 2, pp. 145–150, May 1986.

[26] J. S. Walling, S. S. Taylor, and D. J. Allstot, "A Class-G supply modulator and Class-E PA in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2339–2347, Sep. 2009.

[27] S. M. Yoo, J. S. Walling, O. Degani, B. Jann, R. Sadhwani, J. C. Rudell, and D. J. Allstot, "A Class-G switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1212–1224, May 2013.

[28] K. Onizuka, S. Saigusa, and S. Otaka, "A 1.8GHz linear CMOS power amplifier with supply-path switching scheme for WCDMA/LTE applications," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2013, pp. 90–91.

[29] H. Chireix, "High power outphasing modulation," *Proc. IRE*, vol. 23, no. 11, pp. 1370– 1392, Nov. 1935.

[30] D. Cox, “Linear amplification with nonlinear components,” *IEEE Trans. Commun.*, vol. 22, no. 12, pp. 1942–1945, Dec. 1974.

[31] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. A. El-Tanani, and K. Soumyanath, “A flip-chip-packaged 25.3dBm Class-D outphasing power amplifier in 32 nm CMOS for WLAN application,” *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1596–1605, May 2011.

[32] S. Moloudi and A. A. Abidi, “The outphasing RF power amplifier: A comprehensive analysis and a Class-B CMOS realization,” *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1357–1369, Jun. 2013.

[33] L. Ding, J. Hur, A. Banerjee, R. Hezar, and B. Haroun, “A 25dBm outphasing power amplifier with cross-bridge combiners,” *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1107–1116, May 2015.

[34] W. H. Doherty, “A new high efficiency power amplifier for modulated waves,” *Proc. IRE*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.

[35] F. H. Raab, “Efficiency of Doherty RF power-amplifier systems,” *IEEE Trans. Broadcast.*, vol. BC-33, no. 3, pp. 77–83, Sep. 1987.

[36] A. Grebennikov and S. Bulja, “High-efficiency Doherty power amplifiers: Historical aspect and modern trends,” *Proc. IEEE*, vol. 100, no. 12, pp. 3190–3219, Dec. 2012.

[37] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho, and B. Kim, “The Doherty power amplifier: Review of recent solutions and trends,” *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 559–571, Feb. 2015.

[38] R. Pengelly, C. Fager, and M. Ozen, “Doherty’s legacy: A history of the Doherty power amplifier from 1936 to the present day,” *IEEE Microw. Mag.*, vol. 17, no. 2, pp. 41−58, Feb. 2016.

[39] M. Elmala, J. Paramesh, and R. Bishop, “A 90 nm CMOS Doherty power amplifier with minimum AM-PM distortion,” *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1323–1332, Jun. 2006.

[40] N. Wongkomet, L. Tee, and P. R. Gray, "A +31.5dBm CMOS RF Doherty power amplifier for wireless communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2852–2859, Dec. 2006.

[41] K. Onizuka, S. Saigusa, and S. Otaka, "A +30.5dBm CMOS Doherty power amplifier with reliability enhancement technique," in *IEEE Symp. VLSI Circuits*, 2012, pp. 78–79.

[42] K. Onizuka, K. Ikeuchi, S. Saigusa, and S. Otaka, "A 2.4GHz CMOS Doherty power amplifier with dynamic biasing scheme," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2012, pp. 93–96.

[43] E. Kaymaksut and P. Reynaert, "Transformer-based uneven Doherty power amplifier in 90 nm CMOS for WLAN Applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1659–1671, Jul. 2012.

[44] W. M. Gaber, P. Wambacq, J. Craninckx, and M. Ingels, "A CMOS IQ digital Doherty transmitter using modulated tuning capacitors," in *Proc. IEEE European Solid State Circuits Conf.*, 2012, pp. 341–344.

[45] C. Zhao, B. Park, and B. Kim, "Complementary metal-oxide semiconductor Doherty power amplifier based on voltage combining method," *IET Microw. Antennas Propag.*, vol. 8, no. 3, pp. 131–136, Feb. 2014.

[46] N. Ryu, S. Jang, K. C. Lee, and Y. Jeong, "CMOS Doherty amplifier with variable balun transformer and adaptive bias control for wireless LAN application," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1356–1365, Jun. 2014.

[47] M. Iwamoto, A. Williams, P. F. Chen, A. G. Metzger, L. E. Larson, and P. M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2472–2479, Dec. 2001.

[48] J. Kim, B. Fehri, S. Boumaiza, and J. Wood., "Power efficiency and linearity enhancement using optimized asymmetrical Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 2, pp. 425–434, Feb. 2011.

[49] Y. Yang, J. Cha, B. Shin, and B. Kim, "A fully matched N-way Doherty amplifier with optimized linearity," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 3, pp. 986–993, Mar. 2003.

[50] W. C. E. Neo, J. Qureshi, M. J. Pelk, J. R. Gajadharsing, and L. C. N. de Vreede, "A mixed-signal approach towards linear and efficient N-way Doherty amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 5, pp. 866–879, May 2007.

[51] H. Golestaneh, F. A. Malekzadeh, and S. Boumaiza, "An extended-bandwidth three-way Doherty power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3318–3328, Sep. 2013.

[52] N. Srirattana, A. Raghavan, D. Heo, P. E. Allen, and J. Laskar, "Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 3, pp. 852– 860, Mar. 2005.

[53] I. Kim, J. Moon, S. Jee, and B. Kim, "Optimized design of a highly efficient three-stage Doherty PA using gate adaptation," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 10, pp. 2562–2574, Oct. 2010.

[54] W. C. E. Neo *et al.*, "Adaptive multi-band multi-mode power amplifier using integrated varactor-based tunable matching networks," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2166–2176, Sep. 2006.

[55] J. Fu and A. Mortazawi, "Improving power amplifier efficiency and linearity using a dynamically controlled tunable matching network," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 12, pp. 3239–3244, Dec. 2008.

[56] H. M. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Design of varactor-based tunable matching networks for dynamic load modulation of high power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 5, pp. 1110–1118, May 2009.

[57] D. Chowdhury, C. D. Hull, O. B. Degani, Y. Wang, and A. M. Niknejad, "A fully integrated dual-mode highly linear 2.4GHz CMOS power amplifier for 4G WiMax applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3393–3402, Dec. 2009.

[58] Y. Yoon, J. Kim, H. Kim, K. H. An, O. Lee, C. H. Lee, and J. S. Kenney, "A dual-mode CMOS RF power amplifier with integrated tunable matching network," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 77–88, Jan. 2012.

[59] B. Koo, T. Joo, Y. Na, and S. Hong, "A fully integrated dual-mode CMOS power amplifier for WCDMA applications," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2012, pp. 82–83.

[60] A. F. Aref and R. Negra, "A fully integrated adaptive multiband multimode switching-mode CMOS power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 8, pp. 2549–2561, Aug. 2012.

[61] Y. Lee and S. Hong, "A dual-power-mode output matching network for digitally modulated CMOS power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1570–1579, Apr. 2013.

[62] G. Tant, A. Giry, P. Vincent, J. D. Arnould, and J. M. Fournier, "A 2.14GHz watt-level power amplifier with passive load modulation in a SOI CMOS technology," in *Proc. IEEE European Solid State Circuits Conf.*, 2013, pp. 189–192.

[63] L. Ye *et al.*, "Design considerations for a direct digitally modulated WLAN transmitter with integrated phase path and dynamic impedance modulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3160–3177, Dec. 2013.

[64] C. S. Perez, M. Ozen, C. M. Andersson, D. Kuylenstierna, N. Rorsman, and C. Fager, "Optimized design of a dual-band power amplifier with SiC varactor-based dynamic load modulation," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 8, pp. 2579–2588, Aug. 2015.

[65] J. Choi, D. Kang, D. Kim, and B. Kim, "Optimized envelope tracking operation of Doherty power amplifier for high efficiency over an extended dynamic range," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 6, pp. 1508–1515, Jun. 2009.

[66] J. H. Kim and C. S. Park, "Analysis and implementation of Doherty power amplifier with two-point envelope modulation," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1353–1364, May 2012.

[67] H. Lee, S. Jang, and S. Hong, "A hybrid polar-LINC CMOS power amplifier with transmission line transformer combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1261–1271, Mar. 2013.

[68] W. Tai, H. Xu, A. Ravi, H. Lakdawala, O. Bochobza-Degani, L. R. Carley, and Y. Palaskas, "A transformer-combined 31.5dBm outphasing power amplifier in 45 nm

LP CMOS with dynamic power control for back-off power efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1646–1658, Jul. 2012.

[69] P. A. Godoy, S. Chung, T. W. Barton, D. J. Perreault, and J. L. Dawson, "A 2.4GHz, 27dBm asymmetric multilevel outphasing power amplifier in 65nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2372–2384, Oct. 2012.

[70] E. Kaymaksut and P. Reynaert, "Dual-mode CMOS Doherty LTE power amplifier with symmetric hybrid transformer," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 1974–1987, Sep. 2015.

[71] Y. Y. Huang, W. Woo, H. Jeon, C. H. Lee, and J. S. Kenney, "Compact wideband linear CMOS variable gain amplifier for analog-predistortion power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 68−76, Jan. 2012.

[72] W. Woo, M. D. Miller, and J. S. Kenney, "A hybrid digital/RF envelope predistortion linearization system for power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 1, pp. 229−237, Jan. 2005.

[73] S. Kousai, K. Onizuka, T. Yamaguchi, Y. Kuriyama, and M. Nagaoka, "A 28.3 mW PA-closed loop for linearity and efficiency improvement integrated in a 27.1dBm WCDMA CMOS power amplifier," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2964–2973, Dec. 2012.

[74] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh, and H. Wang, "A +27.3dBm transformer-based digital Doherty polar power amplifier fully integrated in bulk CMOS," in *Proc. IEEE RF Integrated Circuits Symp.*, 2014, pp. 235–238.

[75] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh, and H. Wang, "Design of a transformer-based reconfigurable digital polar Doherty power amplifier fully integrated in bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1094–1106, May 2015.

[76] S. Hu, S. Kousai, and H. Wang, "Antenna impedance variation compensation by exploiting a digital Doherty power amplifier architecture," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 580–597, Feb. 2015.

[77] S. Hu, S. Kousai, and H. Wang, "A broadband CMOS digital power amplifier with hybrid Class-G Doherty efficiency enhancement," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2015, pp. 44–45.

[78] S. Hu, S. Kousai, and H. Wang, "A broadband mixed-signal CMOS power amplifier with a hybrid Class-G Doherty efficiency enhancement technique," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 598–613, Mar. 2016.

[79] H. Kobayashi, J. M. Hinrichs, and P. M. Asbeck, "Current-mode Class-D power amplifiers for high-efficiency RF applications," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2480–2485, Dec. 2001.

[80] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[81] H. Wang, C. Sideris, and A. Hajimiri, "A CMOS broadband power amplifier with a transformer-based high-order output matching network," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2709–2722, Dec. 2010.

[82] S. Kousai, K. Onizuka, S. Hu, H. Wang, and A. Hajimiri, "A new wave of CMOS power amplifier innovations: Fusing digital and analog techniques with large signal RF operations," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2014, pp. 1–8.

[83] H. Wang, S. Kousai, K. Onizuka, and S. Hu, "The wireless workhorse: Mixed-signal power amplifiers leverage digital and analog techniques to enhance large-signal RF operations," *IEEE Microw. Mag.*, vol. 16, no. 9, pp. 36–63, Oct. 2015.

[84] Y. Yoon *et al.*, "A high-power and highly linear CMOS switched capacitor," *IEEE Microw. Compon. Lett.*, vol. 20, no. 11, pp. 619–621, Nov. 2010.

[85] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer – a new power-combining and impedance-transformation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 316–331, Jan. 2002.

[86] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*, 3rd ed. New York, NY, USA: Oxford University Press, 2010.

[87] C. Wang, M. Vaidyanathan, and L. E. Larson, "A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1927–1937, Nov. 2004.

[88] K. Onizuka, H. Ishihara, M. Hosoya, S. Saigusa, O. Watanabe, and S. Otaka, "A 1.9 GHz CMOS power amplifier with embedded linearizer to compensate AM-PM distortion," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1820–1827, Aug. 2012.

[89] Y. Palaskas, *et al.*, "A 5 GHz 20 dBm power amplifier with digitally assisted AM-PM correction in a 90 nm CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1757–1763, Aug. 2006.

[90] R. Darraji, F. M. Ghannouchi, and M. Helaoui, "Mitigation of bandwidth limitation in wireless Doherty amplifiers with substantial bandwidth enhancement using digital techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 9, pp. 2875–2885, Sep. 2012.

[91] S. Sehajpal, S. S. Taylor, D. J. Allstot, and J. S. Walling, "Impact of switching glitches in Class-G power amplifiers," *IEEE Microw. Compon. Lett.*, vol. 22, no. 6, pp. 282–284, Jun. 2012.

[92] S. Hu, S. Kousai, and H. Wang, "A compact broadband mixed-signal power amplifier in bulk CMOS with hybrid Class-G and dynamic load trajectory manipulation operations," in *Proc. IEEE RF Integrated Circuits Symp.*, 2016, pp. 202–205.

[93] S. Hu, S. Kousai, and H. Wang, "A compact broadband mixed-signal power amplifier in bulk CMOS with hybrid Class-G and dynamic load trajectory manipulation," accepted and to appear in *IEEE J. Solid-State Circuits*.

[94] S. Shakib, H. C. Park, J. Dunworth, V. Aparin and K. Entesari, "A 28GHz efficient linear power amplifier for 5G phased arrays in 28nm bulk CMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2016, pp. 352–353.

[95] S. Hu, F. Wang, and H. Wang, "A 28GHz/37GHz/39GHz multiband linear Doherty power amplifier for 5G massive MIMO applications," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2017, pp. 32–33.

[96] A. Agah, H. T. Dabag, B. Hanafi, P. M. Asbeck, J. F. Buckwalter, and L. E. Larson, "Active millimeter-wave phase-shift Doherty power amplifier in 45nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2338–2350, Oct. 2013.

[97] E. Kaymaksut, D. Zhao, and P. Reynaert, "Transformer-based Doherty power amplifiers for mm-wave applications in 40nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1186–1192, Apr. 2015.

[98] A. Grebennikov and J. Wong, "A dual-band parallel Doherty power amplifier for wireless applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3214–3222, Oct. 2012.

[99] C. R. Chappidi and K. Sengupta, "A frequency-reconfigurable mm-wave power amplifier with active-impedance synthesis in an asymmetrical non-isolated combiner," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2016, pp. 344–345.

[100] M. Bassi, J. Zhao, A. Bevilacqua, A. Ghilioni, A. Mazzanti, and F. Svelto, "A 40–67 GHz power amplifier with 13dBm P_{SAT} and 16% PAE in 28 nm CMOS LP," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1618–1628, July 2015.