DESIGN OF POWER DELIVERY NETWORKS FOR NOISE SUPPRESSION AND ISOLATION USING POWER TRANSMISSION LINES

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DESIGN OF POWER DELIVERY NETWORKS FOR NOISE SUPPRESSION AND ISOLATION USING POWER TRANSMISSION LINES

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Dedicated to my beloved family

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LIST OF SYMBOLS AND ABBREVIATIONS

CCPTL	Constant Current Power Transmission Line
CVPTL	Constant Voltage Power Transmission Line
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistor
IC	Integrated Circuit
PBPTL	Pseudo Balanced Power Transmission Line
PCB	Printed Circuit Board
PDN	Power Delivery Network
PRBS	Pseudo Random Binary Sequence
PTL	Power Transmission Line
RPD	Return Path Discontinuity
SPICE	Simulation Program with Integrated Circuit Emphasis
SSN	Simultaneous Switching Noise
TV	Test Vehicle
VRM	Voltage Regulator Module

SUMMARY

In conventional design of power delivery networks (PDNs), the PDN impedance is required to be less than the target impedance over the frequency range of interest to minimize the IR drop and to suppress the inductive noise during data transitions. As a result, most PDNs in high-speed systems consist of power and ground planes to provide a low-impedance path between the voltage regulator module (VRM) and the integrated circuit (IC) on the printed circuit board (PCB).

For off-chip signaling, charging and discharging signal transmission lines induce return currents on the power and ground planes. The return current always follows the path of least impedance on the reference plane closest to the signal transmission line. The return current path plays a critical role in maintaining the signal integrity of the bits propagating on the signal transmission lines. The problem is that the disruption between the power and ground planes induces return path discontinuities (RPDs), which create displacement current sources between the power and ground planes. The current sources excite the plane cavity and cause voltage fluctuations. These fluctuations are proportional to the plane impedance since the current is drawn through the PDN by the driver. Therefore, low PDN impedance is required for power supply noise reduction.

Alternatively, methods of preventing RPDs can be used to suppress power supply noise. Using a power transmission line (PTL) eliminates the discontinuity between the power and ground planes, thereby preventing the RPD effects. In this approach, transmission lines replace the power plane for conveying power from the VRM to each IC on the PCB. The PTL-based PDN enables both power and signal transmission lines to be referenced to the same ground plane so that a continuous current path can be formed, unlike the power-plane-based PDN. As a result, a closed current loop is achieved, and the voltage fluctuation caused by RPDs is removed in idealistic situations. Without the RPD-related voltage fluctuation, reducing the PDN impedance

is not as critical as in the power-plane-based approach. Instead, the impedance of the PTL is determined by the impedance of the signaling circuits.

To use the PTL-based PDN in a practical signaling environment, several issues need to be solved. First, the dc drop coming from the source termination of the PTL needs to be addressed. The driver being turned on and off dictates the current flow through the PTL, causing the dc drop to be dynamic, which depends on the data pattern. Second, impedance mismatch between the PTL and termination can occur due to manufacturing variations. Third, an increase in the number of PCB traces should be addressed by devising a method to feed more than one driver with one PTL. Lastly, the power required to transmit 1 bit of data should be optimized for the PTL by using a new signaling scheme and adjusting the impedance of the signaling circuit.

Constant flow of current through the PTL is one solution proposed to address the first two issues. Constant current removes the dynamic characteristics of the dc drop by inducing a fixed amount of dc drop over the PTL. Moreover, constant current keeps the PTL fully charged at all times, and thereby eliminates the process of repeatedly charging and discharging the power transmission line. The constant current PTL (CCPTL) scheme maintains constant current flow regardless of the input data pattern. Early results on the CCPTL scheme have been discussed along with the measurements. The CCPTL scheme severs the link between the current flowing through the PTL and the output data of the I/O driver connected to it. Also, it eliminates the charging and discharging process of the PTL, thereby completely eliminating power supply noise in idealistic situations. To reduce any associated power penalty, a pseudo-balanced PTL (PBPTL) scheme is also proposed using the PTL concept. A pseudo-balanced (PB) signaling scheme, which uses an encoding technique to map N-bit data onto M-bit encoded data with fixed number of 1s and 0s, is applied. When the PB signaling scheme is combined with the PTL, the jitter performance improves significantly as compared to currently practiced design approach. The constant voltage PTL (CVPTL) scheme is proposed to reduce the power penalty further. The effectiveness of the scheme is simulated to show promising results.

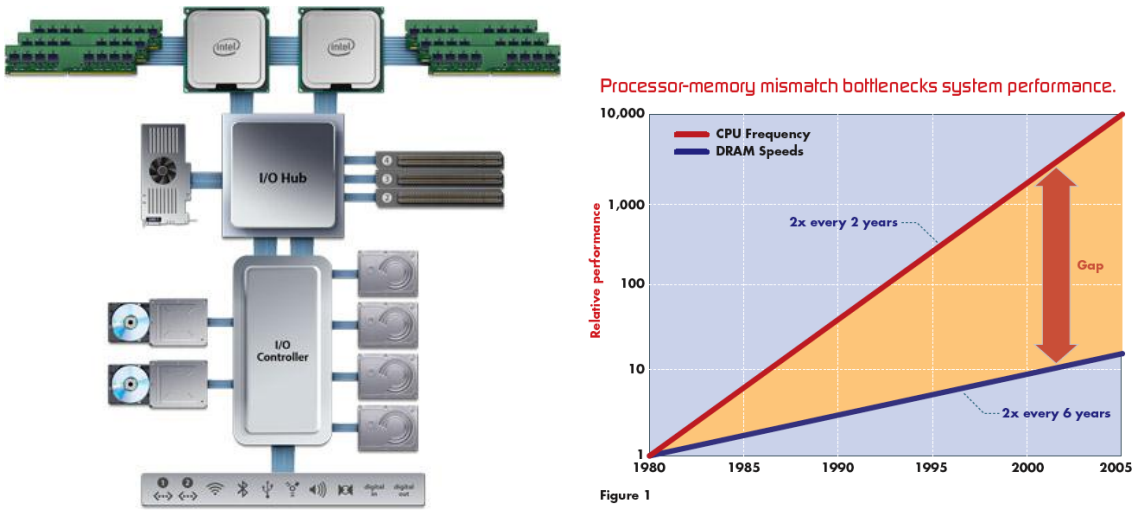
Then, the design methodology for selection and placement of decoupling capacitor is presented. The methodology is calculation-based so that it is computationally less expensive and relatively simple as compared to the use of decoupling capacitor for power plane. Finally, PTL-based grid is suggested for standardized power delivery.

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Over the last several decades, Moore's Law has continued with technology scaling, which has led to more compact devices with higher performance and greater functionality. A contribution has also come from advances in processor architecture, which has made a successful transition from single-core to multi-core computing platforms, as shown in Figure 1.1(a). Now, many-core architecture is being introduced to boost the processor performance even more [1][2]. For the past 20 years, processor and memory has suffered from performance mismatch, and the disparity has been growing continuously, as shown in Figure 1.1(b). The prime reason for this is the division of the semiconductor industry into microprocessor and memory fields [4]. As a result, their technology headed in two different directions: the technology for microprocessor has increased in speed, while the technology for memory has increased in capacity [1]. As a result, memory latency is much greater than processor clock step; a single access to main memory can take hundreds of clock cycles (approximately 150 cycles or more) [5]. To alleviate the bottleneck coming from the processor-memory speed mismatch, current high performance processors include large amounts of on-chip cache [6]. However, the on-chip cache is not able to ultimately replace the off-chip memory due to cost and capacity issues [7]. Therefore, the off-chip communication is inevitable for the memory to supply data that the processor requests, which is now one of the primary obstacles to improved computer system performance.



(a) **(b)**

Figure 1.1 (a) An example of a computer system (Picture courtesy of Apple). (b) Processor-memory performance mismatch (Picture courtesy of [3]).

The performance of the processor-memory interface is dictated by two factors, namely memory speed and memory bandwidth. To accommodate the increasing amount of memory traffic, both factors need to be increased. As the memory bandwidth is the amount of data bits transferred along the off-chip interconnect per second [4], traditional approaches to improving the memory bandwidth include either speeding up the memory clock or increasing the bus bandwidth by increasing the chip-to-chip communication speed (in Hz) and the bus width (in bits), or both [8].

As a result, the off-chip channel data rate has become one of the essential bottlenecks in modern high performance computing systems. The increasing data rate and the shrinking design rule are two key factors contributing to the rising importance of power integrity [9]-[12]. The new manufacturing process technology is compatible with reduced supply voltages, which in turn reduces the supply voltage operating margin [13][14]. Although the reduced supply voltage is highly desirable to reduce the power consumption, the increased quantity of transistors per unit area increases the total power consumption in the integrated system. Moreover, the enhanced data rate contributes to the increasing

power consumption as well. As a result, the PDN current has dramatically increased, as shown in Figure 1.2.

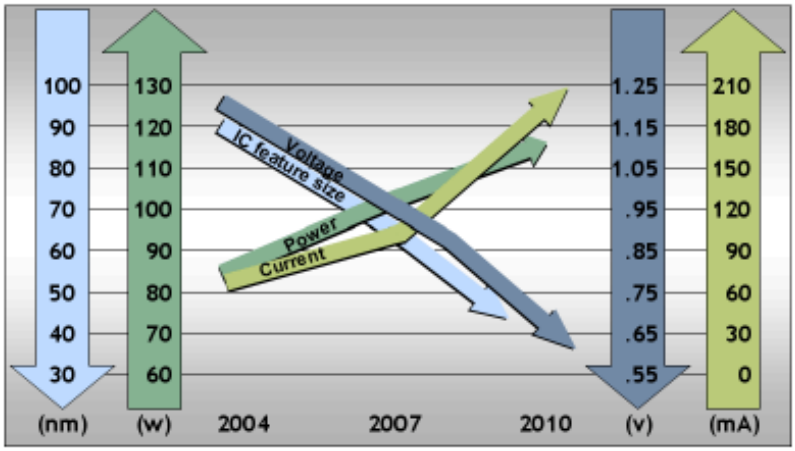


Figure 1.2 Dramatic increase in PDN current with decreasing design rule and voltage levels, and increasing total IC power consumption (Courtesy [12]).

As the inductance in the supply path limits the amount of current deliverable during the switching time interval, the increased amount of transient current per unit time cannot be delivered to the device as quickly as required. Therefore, the voltage at the I/O will drop and the ground potential will rise, and the rise time/fall time of the signal will be seriously impaired [15], which will limit the chip-to-chip communication speed. The contributions of this work are aimed primarily at suppressing fluctuations in supply voltage and ground potential, and achieving near-zero power supply noise.

1.2 Power Delivery Network

A power delivery network (PDN) is the network that connects the power supply to the power/ground terminals of the ICs. Ideally, it provides sufficient voltage and current for the ICs the instant the transistors switch. However, the power delivery network consists of inductive, resistive, and capacitive components, which impedes supplying an infinitely large amount of current in an infinitesimally small amount of time. The series inductance in the supply path induces undesired voltage fluctuation, V_L, through the

mechanism of equation (1) so that the current transients on the power delivery network (PDN) cause power supply noise given by:

$$V_L = L\frac{di}{dt} \tag{1}$$

where di/dt is the rate of change of the current.

In current design of PDN, the PDN impedance is required to be less than the target impedance over the frequency range of interest to hold the noise voltage below the allowed ripple on the power supply. Therefore, low PDN impedance can prevent excessive voltage fluctuations and lead to power supply noise reduction. The target impedance of a PDN to limit the voltage ripple on the power supply is given by [16]:

$$Z_{PDN} = \frac{V_{DD} \times \%ripple}{I_{max}} \tag{2}$$

where V_{DD} is the supply voltage, %ripple is the target percentage of the voltage ripple, and I_{max} is the maximum current. As a result, most PDNs in high-speed systems consist of power and ground planes to provide a low-impedance path between the voltage regulator module (VRM) and the IC on the printed circuit board (PCB), as shown in Figure 1.3. The power delivery network consists of distributed networks of R, L, and C.

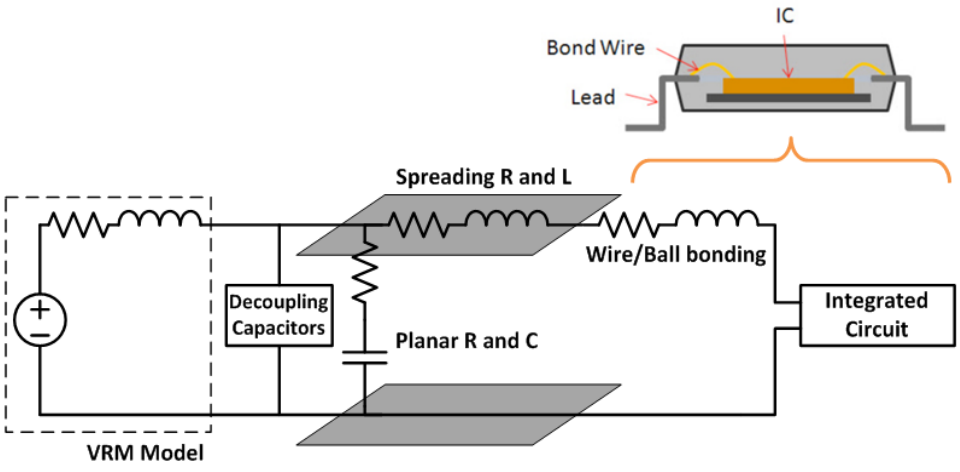


Figure 1.3 Power distribution network using power and ground planes.

For off-chip signaling, charging and discharging signal transmission lines induce return currents on the reference planes. Since the return currents always follow the path of least impedance, the signal transmission lines are referenced to the closest plane [17], as shown in Figure 1.4. To accommodate return current paths for multiple signal traces in the board or package, either ground or voltage plane is used as the reference conductor. The return current path plays a critical role in maintaining the signal integrity of the bits propagating on the signal transmission lines.

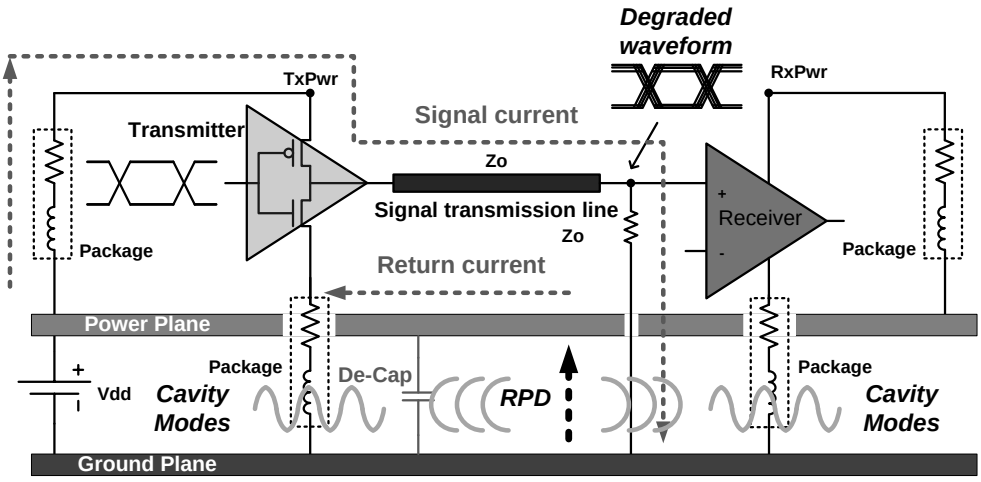


Figure 1.4 Chip-to-chip communication in a power-plane-based system.

Interruption in the return current path leads to return path discontinuities (RPDs) [17][18]. RPDs occur due to via transitions, apertures on the power/ground planes or split planes, to name a few [17]-[26], as shown in Figure 1.5. Even when signal lines are referenced to a continuous plane, RPDs can be induced during either the low-to-high or high-to-low transitions of the driver due to the disruption between the power and ground planes, as shown in Figure 1.5(d). In all of these RPDs, displacement current sources are created between the power and ground planes. The current sources excite the plane cavity so that excessive voltage fluctuations can occur between the planes due to the cavity modes in the structure. These cavity modes can degrade the signal integrity of the waveform as the signal travels along the transmission line, as described in [16].

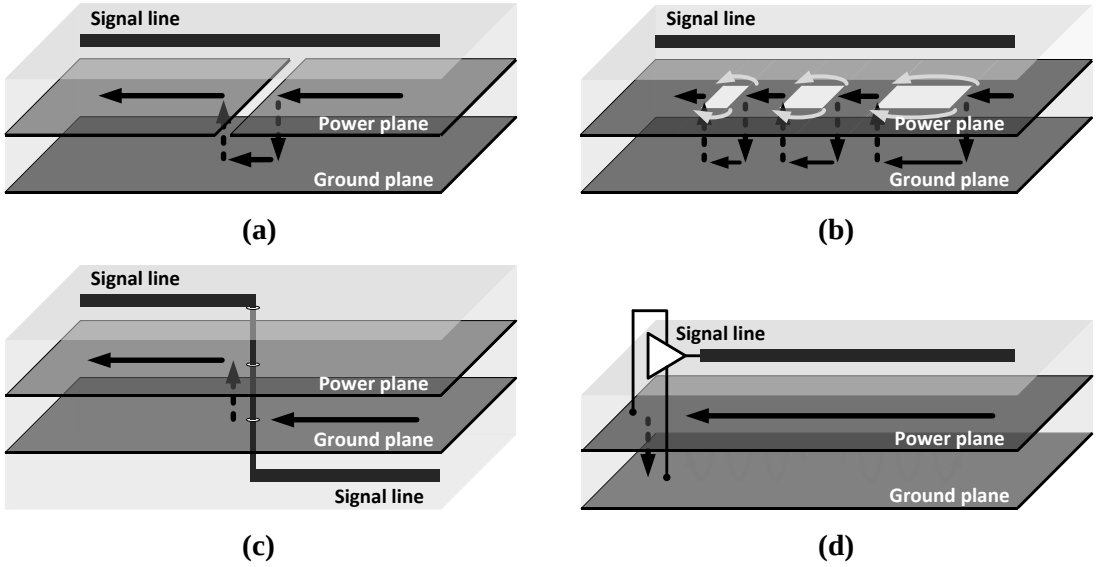


Figure 1.5 Examples of RPDs. (a) Via transition. (b) Apertures on the reference plane. (c) Split plane. (d) Solid plane.

Many researchers have done work to address the RPD issue, which are detailed in [18]. In the case that a signal via transition causes the signal transmission line to reference two different planes, the return current loop is completed by a current path provided by the structure. If two reference planes are at the same potential, shorting vias are connected between the planes around the signal via, as shown in Figure 1.6(a) [26]-[30].

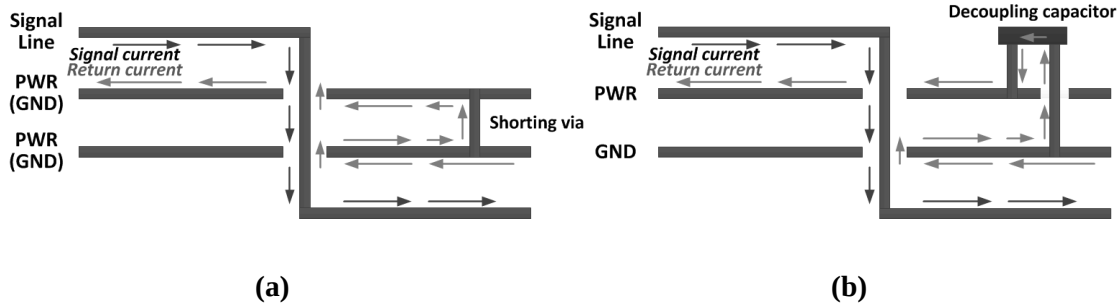


Figure 1.6 Solution to RPDs due to via transition. (a) Shorting via. (b) Decoupling capacitor.

If two reference planes have different voltage levels, the excessive power supply noise induced by the displacement current sources between the power and ground planes

can only be reduced by increasing the capacitance between the planes through new technologies such as thin dielectrics, embedded capacitance, high frequency decoupling capacitors, and so on (Figure 1.6(b)) [31]-[37].

1.3 Decoupling Capacitor

Ideally, the PDN impedance can be reduced by arranging the stack-up order so as to have the Vcc/Vss planes close to the surface, or reducing the board thickness [15]. In addition to reducing the path inductance, decoupling capacitors need to be placed as close to the net as possible. As explained in the previous section, decoupling capacitors are added between the two planes of different voltage levels to provide current paths at the RPD locations and to reduce the PDN impedance over the frequency range of interest.

A decoupling capacitor has resistance and inductance associated with it, which are called as the equivalent series resistance (ESR) and the equivalent series inductance (ESL), respectively [16]. As a result, a decoupling capacitor can be represented as a series RLC circuit, as shown in Figure 1.7.

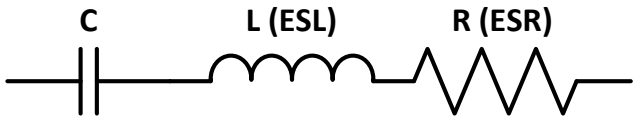


Figure 1.7 Equivalent series RLC circuit of a decoupling capacitor.

The impedance of the capacitor becomes

$$Z_{cap} = R + jwL + \frac{1}{jwC} \tag{3}$$

where R is the resistance (ESR), L is the inductance (ESL), and C is the capacitance of the capacitor. The equation indicates that the inductive impedance increases with increase in frequency. Conversely, the capacitive impedance decreases with increase in frequency. In other words, the capacitive impedance is dominant over the inductance impedance at

low frequency, and vice versa at high frequency. Consequently, the frequency response of the capacitor resembles a V-shaped curve, which is a characteristic of a series resonant circuit, as shown in Figure 1.8. At the frequency where the two impedance components cancel each other, resonance occurs, and the impedance of the capacitor reaches its minimum value that is equal to the equivalent series resistance. The resonant frequency is given by:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{4}$$

Over the frequency range above the resonant frequency, the decoupling capacitor behaves like an inductor.

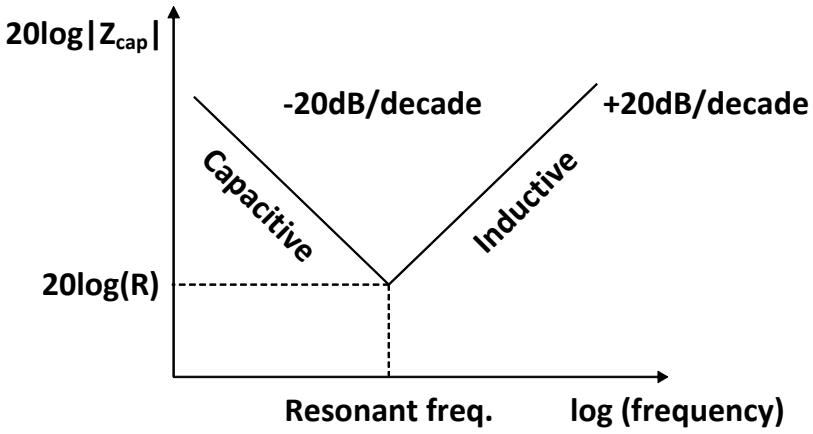


Figure 1.8 Frequency response of a capacitor.

A digital system switches at multiple frequencies, drawing current from the power supply at multiple frequencies. The amount of switching noise depends on the PDN impedance over the frequency range of interest. The role of decoupling capacitors is to hold the PDN impedance below the target impedance, which is determined by the allowed voltage ripple. Since the decoupling capacitor has the minimum impedance at the resonant frequency, the capacitance of the decoupling capacitor is determined based on the PDN impedance profile over the frequency range of interest. If there is a certain

frequency at which the PDN impedance exceeds the target value, a proper decoupling capacitor should be added at a proper location to reduce the PDN impedance to an acceptable level. As a result, low PDN impedance over the frequency range of interest is achieved. Also, decoupling capacitors serve as a charge reservoir for the device when there is a sudden demand for current.

In Figure 1.9, the effect of various components on the PDN impedance is shown by the impedance versus frequency curve. In the frequency range from 1 kHz to 1 MHz, bulk capacitors are used, while ceramic surface mount and embedded capacitors are used up to 1 GHz. In GHz range, the power/ground planes of the package are used to provide decoupling. The inductive slope raises the impedance, while the capacitive slope pulls down the impedance. Therefore, the decoupling capacitors should be selected and placed to comply with the PDN design requirement of the target impedance.

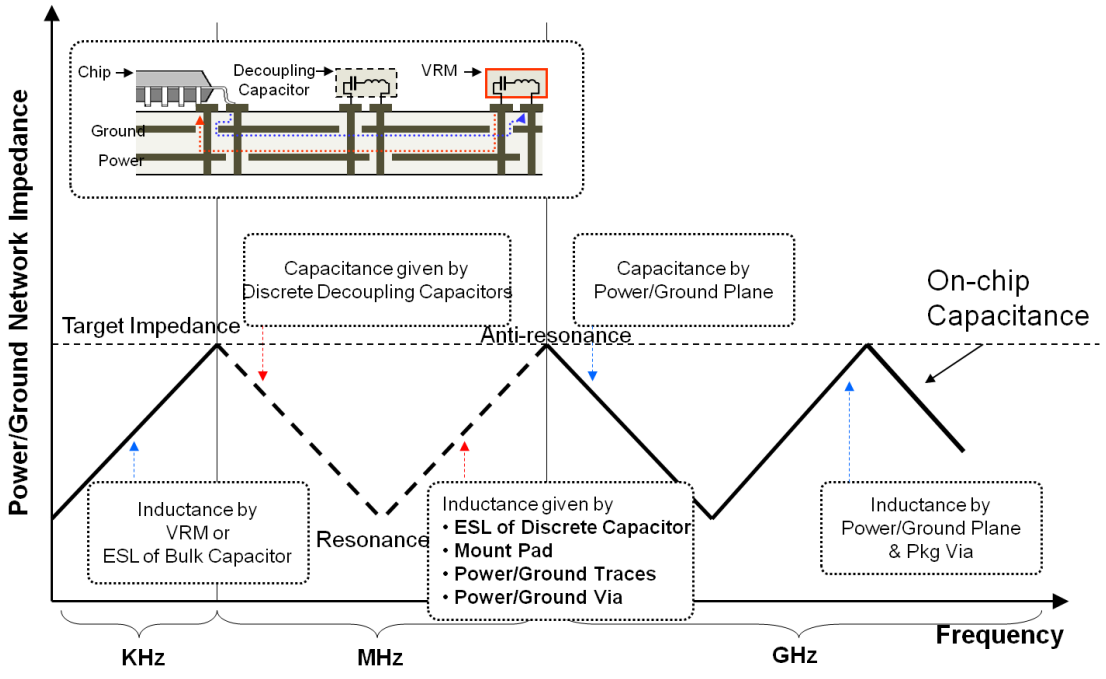


Figure 1.9 Impedance versus frequency in the power delivery network (Picture courtesy of Professor Joungho Kim, KAIST, South Korea and [16]).

1.4 Noise Isolation Techniques: Electromagnetic Band Gap Structure

In modern multifunction designs, it may be required to integrate noise-sensitive analog/RF circuits next to digital circuits. Here, digital switching noise can propagate through power/ground planes and affect analog/RF circuit performance. It is important to block this effect.

One common solution to suppress noise propagation on the PDN is to split the power/ground plane for different types of circuits such as analog and digital circuits. This method may be effective at low frequency, but at high frequency above 1GHz, the electromagnetic coupling occurs over the gap [24][25]. Using two vertically separate power/ground plane pairs for each type of circuit can be a solution, but usually the number of layers is restricted due to the cost and volume of the system.

Other than providing two separate power/ground plane pairs, using an electromagnetic band gap (EBG) structure can be a very efficient method to suppress noise propagation. Especially, an AI-EBG structure proposed in [38] is a two-dimensional periodic structure, whose application can be expanded to control power/ground noise over the target frequency range in mixed-signal systems. It does not require any via making the structure more compact. A unit cell of AI-EBG consists of a metal patch and metal branches, as shown in Figure 1.10(a). Such unit cells are repeated laterally and longitudinally, resulting in a periodic structure. Depending on the size and number of the unit cell, the stop frequency band is determined. The equivalent circuit of the EBG structure is shown in Figure 1.10(b). The metal patch can be represented as an equivalent inductance and capacitance. The capacitance of the branch is negligible so that only an equivalent inductance of the branch is included. The resulting LC network functions as a band-stop filter. Since the EBG structure stops the propagation of electromagnetic waves over a certain frequency band, it can isolate the sensitive analog circuits from the noisy digital circuits even when they share the same board [38]-[44].

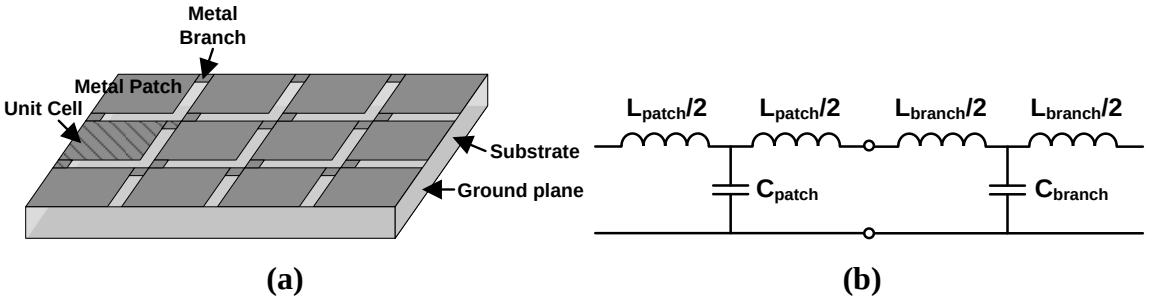


Figure 1.10 EBG structure (a) Physical layout. (b) Equivalent circuit.

Previous work in this area demonstrates that EBG patterns can be used to block power/ground plane noise between digital and analog/RF blocks. That is, an EBG patterned plane can be precisely designed such that a targeted signal frequency cannot spread from one cell to another. Thus, the noise propagation drops off. However, most of the EBG-related research has involved placing the EBG structure on the top plane, though power/ground planes are generally sandwiched between other planes in many realistic cases. In [45] and [46], a simulation result suggests that a problem arises when the EBG structure is placed in between two solid planes; the EBG structure is no longer capable of noise isolation. Therefore, it is important to verify the noise filtering function and explore new design requirements when dealing with an embedded-EBG structure.

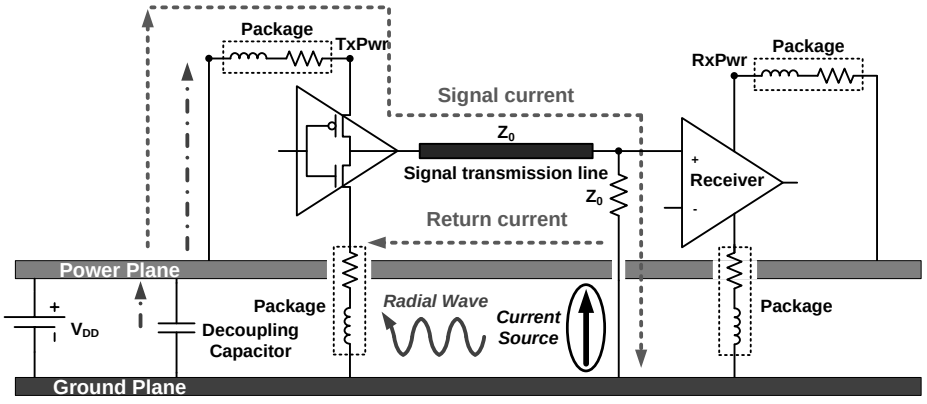
Here, it is important to note that the concept of patterning the power/ground planes to achieve the noise filtering effect is an after thought to mitigate the noise coupling problem.

1.5 Power Transmission Line

Planes are generally used to supply power from the VRM to the IC due to their high frequency characteristics and low dc drop related issues. To accommodate return current paths for multiple signal traces in the board or package, either ground or voltage plane is used as the reference conductor. The problem is that the disruption between the power and ground planes induces return path discontinuities (RPDs) during the data transitions,

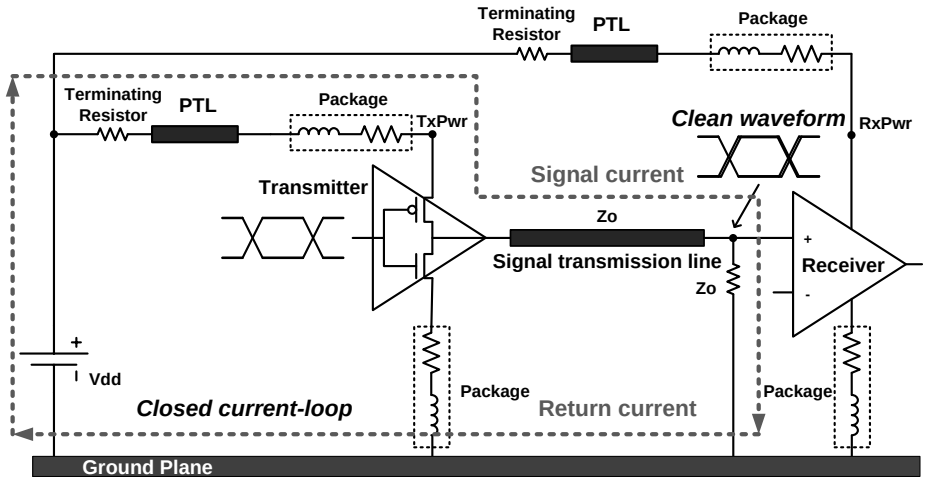
which create displacement current sources between the power and ground planes as shown in Figure 1.11(a) [16]. These sources induce excessive power supply noise, which again requires managing the PDN impedance so as to manage the excessive noise caused by the current transients. The excessive noise can only be reduced by increasing the capacitance requirements through new technologies such as thin dielectrics, embedded capacitance, high frequency decoupling capacitors, and so on [33]-[37], as shown in Figure 1.11(a).

Alternatively, methods for eliminating the RPDs can be employed to suppress power supply noise. In a newly-proposed PDN scheme, transmission lines are used to replace the voltage plane and convey power from the voltage source to the die, which are called as Power Transmission Lines (PTLs), as shown in Figure 1.11(b). The characteristic impedance of PTL is decided based on the characteristic impedance of the signal transmission line, desired eye height at the receiver side, turn-on impedance of I/O driver, to name a few. Since the characteristic impedance of signal transmission line is typically between 25-70 ohms, that of PTL also falls within this range. Hence, the PTL concept enables the use of a high-impedance network for power delivery, which is in direct contrast to the method being currently pursued.



(a)

Figure 1.11 Chip-to-chip communication. (a) Using plane-based PDN. (b) Using PTL-based PDNs.



(b)

Figure 1.11 Continued.

1.6 Contributions

The focus of this research is to design new PDN concepts using power transmission lines to achieve isolation and reduction of the switching noise at the same time for modern multifunction designs. In this regard, the following research has been accomplished, as summarized in Figure 1.12:

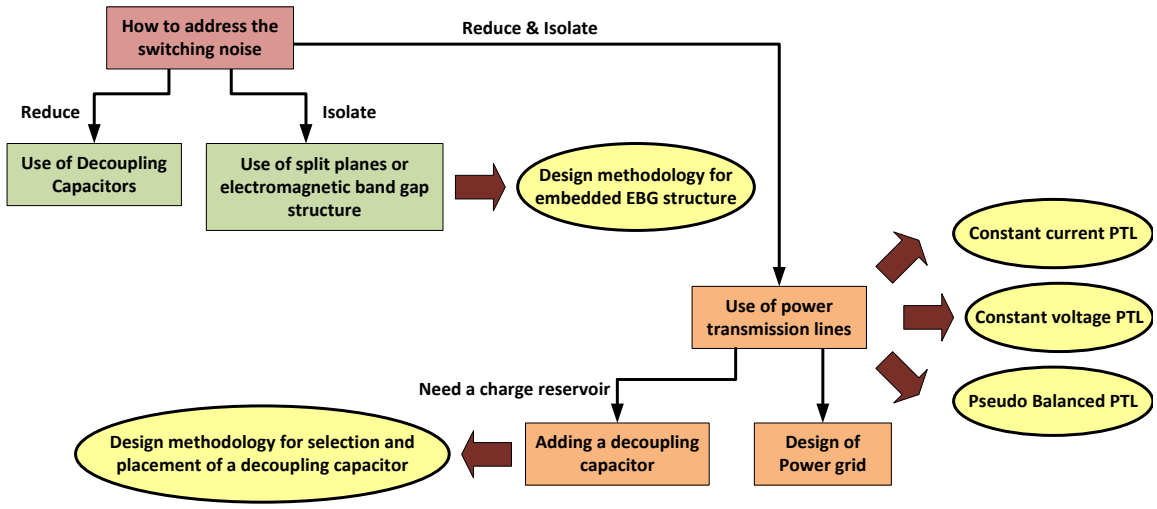


Figure 1.12 Completed research.

1. **Development of a design technique for embedded electromagnetic bandgap structure in load board applications**

   The failure mechanism of the embedded EBG structure has been studied to identify the source of the problem. A new design method to recover the noise filtering function of the embedded EBG structure has been proposed. Design guidelines for the proposed design method which consists of three design parameters, namely potential difference, plane distance, and via number/proximity, has been provided. The proposed solution has been verified through three experimental vehicles, and applied to a prototype multi-layer load board for a gigahertz ADC.

2. **Examination of the limitation of using PTL**

   The advantages of the PTL signaling scheme are expected to include reduction of layer counts and elimination of decoupling capacitors for mitigating RPDs, which lead to lower cost. However, it has been found that using PTL generates other problems such as: 1) output-data-dependent dc drop on the PDN due to the terminating resistance, 2) mismatch effect between the PTL and the termination, 3) line congestion, and 4) increased power consumption. These issues have been investigated using theory and simulation.

3. **Design of the Constant Current Power Transmission Line (CCPTL) scheme**

   The constant current PTL (CCPTL) scheme has been developed to resolve the two issues related to PTL, namely the dynamic dc drop on PDN caused by terminating resistance, and the mismatch effect between the power transmission line and terminating resistor. The proposed CCPTL scheme uses dummy paths to induce constant current through the PTL, which keeps the PTL fully charged all the times. Therefore, The CCPTL scheme severs the link between the current flowing through the PTL and the output data of the I/O driver connected to it. Also, it eliminates the charging and discharging process of the PTL, thereby completely eliminating power supply noise in idealistic situations. The proposed CCPTL scheme has been

applied to the single-ended signaling, and implemented as test vehicles. For comparison, the power plane scheme using constant current through the PDN has also been fabricated. The measurement results of the two test vehicles have been compared, and the effectiveness of the CCPTL scheme has been demonstrated; using the CCPTL scheme provides 36.3% less p-p jitter and 15.1% larger eye amplitude as compared to the power plane scheme. Reasonable correlation between measurements and simulations were observed, showing the trend of signal integrity improvement by using PTL.

4. **Design of the Constant Voltage Power Transmission Line (CVPTL) scheme**

   The constant voltage PTL (CVPTL) scheme has been developed to address the power penalty issue of the CCPTL scheme while maintaining the improved quality of the waveforms. The proposed CVPTL scheme removes the dynamic dc drop on the PDN by using resistor paths. The selective path induces current whose amount is proportional to the number of turned-on I/O drivers. As a result, the CVPTL scheme consumes the same amount of power as the conventional power plane scheme except during the quiescent (quiet) state in which none of the drivers are drawing current from the power supply. Since the PTL in the CVPTL scheme goes through the charging and discharging repeatedly, various impedance-mismatched cases have been simulated to quantify their effect on the eye diagrams. The simulation results have shown that the CVPTL scheme provides larger and wider eye diagrams even with the degradation coming from the impedance mismatch as compared to the conventional power plane scheme. This scheme has not been experimentally demonstrated, but only through simulation.

5. **Design of the Pseudo Balanced Power Transmission Line (PBPTL) scheme**

   A PTL scheme using pseudo-balanced signaling has been developed for multiple I/Os, which is called pseudo balanced PTL (PBPTL). The proposed scheme maintains the method of using constant current but with less power penalty. The

proposed pseudo-balanced signaling scheme has been applied to both the PTL-based and power-plane-based test vehicles. The simulation and measurement results have demonstrated that the proposed signaling scheme yields a significant improvement in signal integrity when combined with PTL. Using PTL improved the eye height by 68.7% and reduced the p-p jitter by 24.2% as compared to using power plane based on the measurement results.

6. **Development of a methodology for the selection and placement of decoupling capacitors for the PTL-based PDN**

   The methodology for the selection and placement of decoupling capacitors for the PTL-based PDN has been developed. Unlike the PDN using a power/ground plane pair, PTL does not depend on the decoupling capacitor to provide return current paths or reduce the PDN impedance at specific locations that have the voltage maxima. The decoupling capacitor serves as a charge reservoir when the VRM is unable to supply the current during the required time interval. Thus, the methodology for estimating the minimum required decoupling capacitor depends on the maximum switching current and the switching time interval. To prevent over-design, a methodology has been developed and presented with an example, which determines the minimum required capacitance and the maximum distance to the ICs for the decoupling capacitor to function properly as charge storage. Measurement results have been included to support the proposed methodology.

7. **Investigation of a uniform PTL grid based PDN**

   Uniform PTL grid has been studied to supply power to multiple I/O drivers in a standardized manner. Preliminary simulations have been performed to investigate the functioning mechanism of the PTL grid and to identify any accompanying issues. A test case has been included.

8. **Tape-out of a custom-designed chip using a 0.18 μm CMOS process**

The transmitters using the CCPTL scheme and the PBPTL scheme were full-custom designed using a 0.18μm CMOS process. The transmitters using power plane were also included in the design for performance comparison. The measurement results have shown that both the CCPTL and PBPTL schemes outperform the power plane at various frequencies, which has been demonstrated using off-the-shelf chips. Using PTL improves the quality of the signal measured at the receiver side.

9. **Tape-out of a 3D chip using 350 nm CMOS process and Tezzaron's TSV/3D technology**

   The application of the proposed CCPTL scheme has been extended to a 3D IC. The transmitters for the CCPTL-based single-ended and differential signaling were designed using 350 nm Global Foundries' technology and Tezzaron's TSV/3D technology. The transmitters for the power-plane-based signaling were also implemented on the same tier to compare the performance of the two PDNs through measurements. Signal and power supply networks of all the transmitters include wire bonds, F2F vias, and TSVs. The goal is to demonstrate the efficacy of using PTL for 3D applications, though measurements could not be made due to the unavailability of the IC on time.

1.7 Dissertation Outline

The rest of this thesis is organized as follows: Chapter 2 presents the proposed design techniques for the embedded EBG structure. To achieve isolation of noise sensitive devices from a noisy device in a system through the PDN, an electromagnetic Band Gap (EBG) patterned power/ground plane is used to provide filtering property to the PDN which transports power to the devices. The limitation of the embedded EBG structure is presented along with the solution. Chapter 3, 4, 5 presents the second approach using PTL for achieving isolation and reduction of the switching noise between

parts in a system. Chapter 3 discusses a newly proposed PDN scheme using power transmission lines (PTLs); the advantages that can be achieved by replacing a voltage plane with PTLs are explored along with the issues associated with the PTLs. To address those issues, the Constant Current PTL (CCPTL) scheme is proposed in Chapter 3. In Chapter 4, the Pseudo-Balanced PTL (PBPTL) scheme is proposed, which induces constant current through the PTL with reduced power penalty. The PBPTL encodes input data to be balanced prior to transmission, and decodes the original information at the receiver. In Chapter 5, the Constant Voltage PTL (CVPTL) scheme is introduced to address the limitation of the CCPTL scheme, which is increased power penalty. Chapter 6 describes a design methodology for the choice and placement of decoupling capacitors. The proposed methodology has been applied to a test vehicle, and the simulation and measurement results are presented. Chapter 7 discusses how the PTL can be laid-out in a grid-form for power delivery to each device in a standardized manner, which simplifies the layout. Future work is proposed in Chapter 8. The dissertation is finally concluded in Chapter 9.

CHAPTER 2

EMBEDDED ELECTROMAGNETIC BAND GAP STRUCTURE IN LOAD BOARD APPLICATIONS

2.1 Introduction

2.1.1 Noise Coupling in Mixed-Signal Systems

To reflect the current trend of communications systems, the speed and resolution of analog-to-digital converters (ADCs) are increasing. These ADCs are very sensitive to noise due to reduced noise and timing margins. For proper characterization and evaluation of such high-speed and high-resolution ADCs, the test environment should be designed with an awareness of signal integrity issues [15]. Since the load board serves as an interface between the device under test (DUT) and automatic test equipment (ATE) during the evaluation of the DUT performance, the load board plays an important role in the test environment. The power distribution on the load board should be able to provide the necessary power to the DUT. Therefore, the suppression of simultaneous switching noise (SSN) on the PDN of the load board is critical for achieving a robust test environment for mixed-signal devices. In multifunction designs such as ADCs, digital switching noise can propagate through power/ground planes and affect analog/RF circuit performance, as shown in Figure 2.1 [47]-[50]. It is important to block this effect.

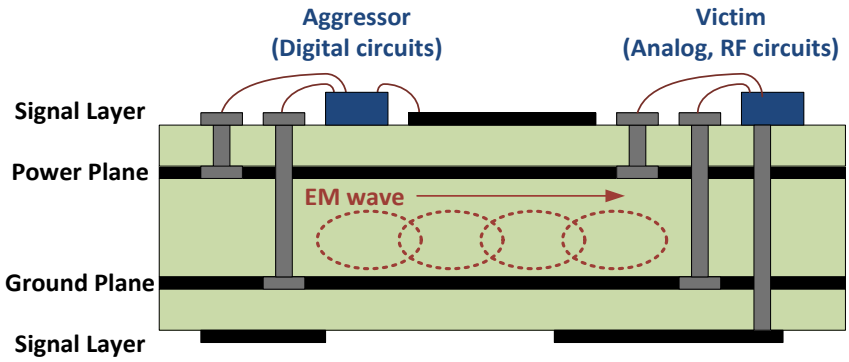


Figure 2.1 Noise generation and coupling in mixed signal systems [43].

2.1.2 Review of Electromagnetic Band Gap Structure

As an alternative method, an electromagnetic band gap (EBG) structure can be used, which is a very efficient technique for the suppression of noise propagation [38]-[44]. The AI-EBG structure proposed in [38]-[40] is a two-dimensional periodic structure, whose application can be expanded to controlling power/ground noise over the target frequency range in mixed-signal systems. Since the AI-EBG structure does not require any additional vias or metal layers, it is more compact as compared to the mushroom-type EBG structure. The unit cell of the AI-EBG structure consists of a metal patch and metal branches. Such unit cells are repeated laterally, resulting in a periodic structure. The size and number of the unit cell determine the target frequency, the stopband bandwidth, and the attenuation level in the stopband. Since the EBG structure stops the propagation of the electromagnetic wave over the target frequency band, it can isolate noise-sensitive analog circuits from noisy digital circuits even when they share a common voltage and ground plane.

2.1.3 Review of Load Board

To reflect the current trend of communications systems, the speed and resolution of ADCs are increasing. These ADCs are very sensitive to noise due to reduced noise and timing margins. For proper characterization and evaluation of such high-speed and high-

resolution ADCs, the test environment should be almost ideal, having negligible noise [47]. Since a load board serves as an interface between DUT and ATE when evaluating the performance of the DUT, the load board plays an important role in the test environment, as shown in Figure 2.2. A robust test environment requires an awareness of signal integrity issues. From a signal integrity point of view, one of the problems with the test cell and DUT interface is a noisy power distribution. The primary function of the PDN is to provide the necessary power to the components on the board, more specifically the DUT. As the output buffers switch simultaneously, the supply voltage will drop and the ground voltage will rise, which is also known as simultaneous switching noise (SSN). To meet the requirement on the supplies of the device, suppression of SSN on the power delivery network (PDN) of the load board is critical. Achieving a low-noise test environment is especially important for testing mixed-signal devices such as ADCs where digital switching noise couples to noise-sensitive analog signals.

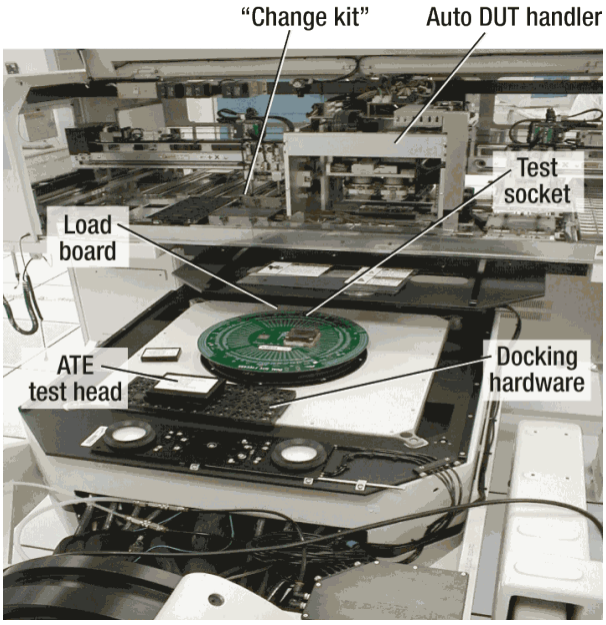


Figure 2.2 A test cell, including the test head, load board, test socket, and auto DUT handler (Picture courtesy of [15]).

2.2 Load Board Design with EBG

2.2.1 Target Load Board

The target device is a low-power, high-performance CMOS ADC that digitizes signals at a 10-bit resolution for a single channel up to 1.5 GHz sampling rate. The target board is a prototype load board for the ADC, which provides an interface between the device and the ATE. Therefore, the target frequency of the EBG structure is 1.5 GHz to prevent the sampling frequency component of the digital circuit being coupled to the analog circuit, which will be kept consistent throughout the chapter. The stack-up information of the target load board is shown in Figure 2.3(a). The board consists of 20 layers: nine signal layers, nine ground planes, one power layer, and one +12V-relay voltage layer. The grey-filled layers indicate ground planes, whereas the white-filled layers are signal layers. To have signal lines referenced to a continuous plane, each signal layer is followed by a solid ground plane. The return current always follows the path of least impedance on the reference plane closest to the signal line.

The top view of the power layer, which is VA+VDR layer, is shown in Figure 2.3(b). It is the 10^{th} layer, which is embedded in between a ground plane and a +12V-relay voltage layer, and consists of analog and digital power planes. They are divided to prevent the noise coupling between the analog and digital circuits through the PDN. The center-located box is where the ADC chip is mounted. Half of the power pins of the ADC are connected to the analog power plane, and the other half are connected to the digital power plane. To explore the level of coupling between the two types of circuits through the power plane, 16 digital power pins of the ADC are considered as noise aggressors, and 15 analog power pins are considered as noise victims. The noise aggressors are located on the digital power plane, while the noise victims are on the analog power plane.

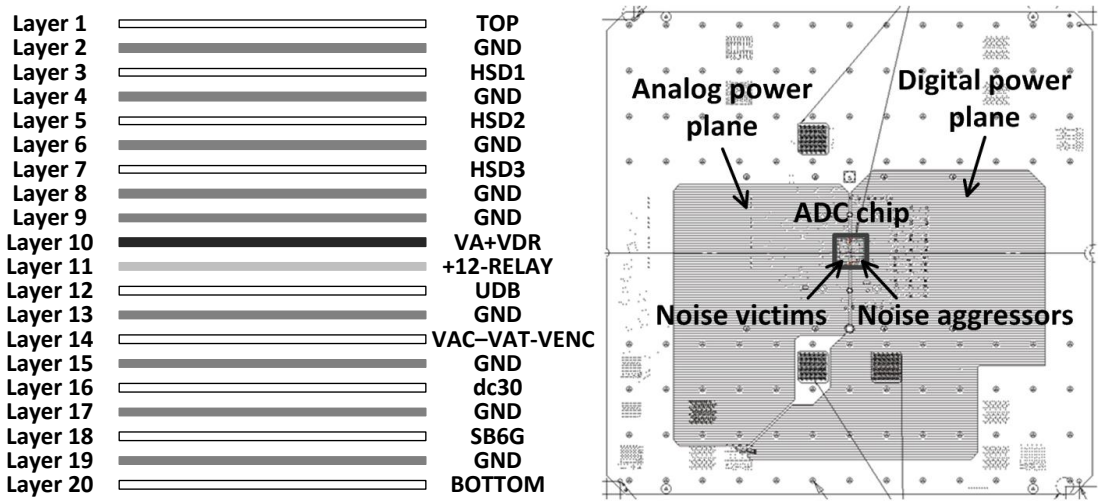


Figure 2.3 ADC load board. (a) Layer stack-up. (b) Top view of the power layer (the VA+VDR layer).

2.2.2 Plane Modification in the Load Board

The top view of the original power layer is shown in Figure 2.4(a). Separate power planes are used for analog and digital circuits to provide isolation. To increase the level of noise isolation between the two split power planes over the desired frequency range, three steps of plane modification were conducted. First, the area of the digital power plane was enlarged. Securing a larger power plane increases the plane capacitance, thereby decreasing the switching noise generated by the same amount of switching current [47]. Second, the gap between the two power planes was increased. The widened separation decreases the capacitance between the two power planes, thereby increasing the impedance. Third, the EBG structure was designed and implemented on the digital power plane, where the noise aggressors are located. The first unit cell was placed to cover 16 digital power pins of the ADC so as to confine the switching noise inside and suppress the noise propagation. By implementing the EBG structure on the digital power plane, the propagation of switching noise is to be suppressed before being coupled to the analog power plane over the plane-split gap. Therefore, the target frequency is the

sampling frequency of 1.5 GHz, and the size of the unit cell is calculated using the plane resonance frequency equation [16]:

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \quad (5)$$

where 'a' and 'b' are the length and width of the rectangular parallel plate waveguide, 'μ' and 'ε' are the permeability and the permittivity of the substrate, and 'm' and 'n' are the wave mode numbers. The resulting size of the unit cell is 26 mm by 26 mm. After placing the first unit cell to include all the noise aggressors, multiple unit cells were repeated laterally starting from the first unit cell. Two rows of unit cells were implemented along the gap between the digital and analog power planes to prevent the noise coupling from the digital power plane to analog power plane. The top view of the modified power layer is shown in Figure 2.4(b). On the other hand, ground planes that are used as reference conductors for other signal layers are kept solid without any patterning to secure the continuous return current paths.

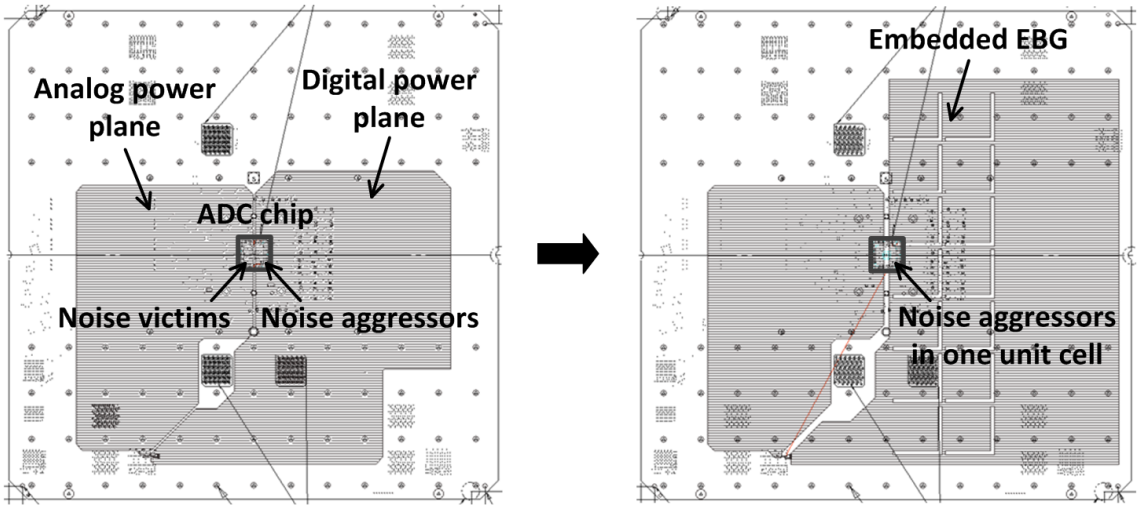


Figure 2.4 Top view of VA+VDR layer of the load board. (a) Before plane modification. (b) After plane modification.

Sphinx [51], a multi-layer finite difference method (M-FDM) [16] based

electromagnetic solver was used to model the load board in the frequency domain. The S_{21} between a noise aggressor and a noise victim before and after the plane modification are simulated to assess the efficacy of the plane modification, as shown in Figure 2.5. Port1 is at one of the 16 digital power pins on the digital power plane, and Port2 is at one of the 15 analog power pins on the analog power plane.

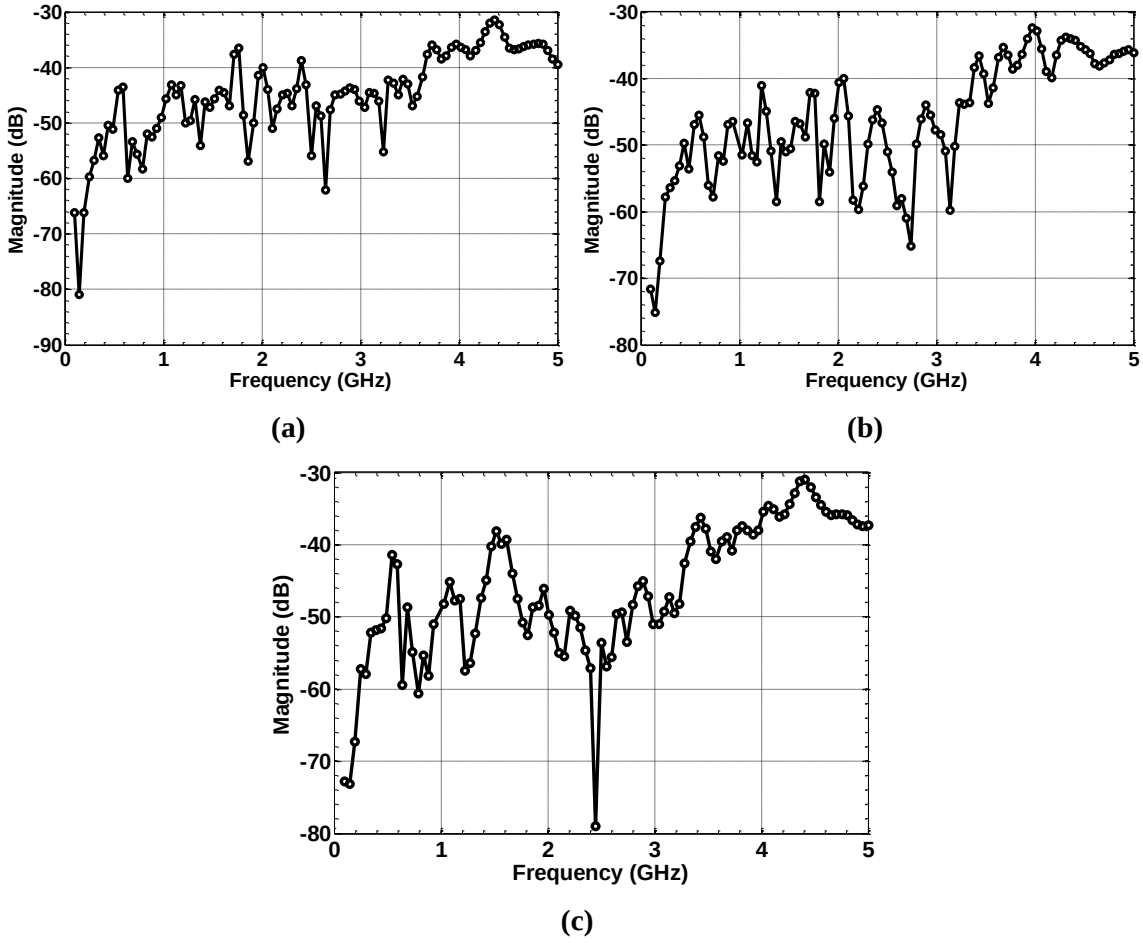


Figure 2.5 Simulated S_{21}. (a) Original. (b) After plane area and gap modifications. (c) After EBG implementation.

In Figure 2.5(a), S_{21} in the original power layer is shown. Due to the gap between the two power planes, the isolation level at low frequencies is below -65 dB. However, as the frequency goes up, the coupling increases so that the magnitude of S_{21} reaches up to -31.48 dB. At 1.5 GHz, the magnitude of S_{21} is -45.69 dB. After enlarging the area of the digital power plane area and widening the gap between the planes, the overall isolation

level has slightly improved, as shown in Figure 2.5(b). However, at 1.5 GHz, the magnitude of S_{21} is -50.77 dB, which is not enough as the isolation level in the stopband. In Figure 2.5(c), S_{21} in the EBG-implemented power plane is shown. Although the EBG structure is implemented to suppress the wave propagation from Port1 to Port2 at 1.5 GHz, the magnitude of S_{21} at 1.5 GHz is -39 dB, which hardly shows any improvement from the original power layer. It can be concluded that the EBG structure fails to function as a filter at the target frequency when implemented on the digital power plane of the load board.

2.3 Analysis of Failure

In this section, the reason for the functional failure of the embedded EBG structure is explored using prototype EBG structures.

2.3.1 Two-Layer EBG Structure

As a baseline for the performance comparison of the EBG structures, a two-layer EBG structure is simulated. The cross section view of the two-layer EBG structure is shown in Figure 2.6(a). The top and bottom copper layers have the thickness of 35.6 μm, and a 165 μm-thick FR4 layer is placed between the two copper layers. The top layer is periodically patterned, as shown in Figure 2.6(b). The unit cells are repeated along the lateral direction, and connected to each other by metal branches. A total of 25 unit cells, 5 rows and 5 columns, are used on the top layer. The total size of the EBG-implemented plane is 135 mm by 135 mm. The bottom layer is a solid plane used as a reference, whose size is 135 mm by 135 mm as well. An EBG layer being backed by a solid plane is a typical configuration of the alternating impedance EBG structure [38].

Two ports are defined. The locations of the ports are shown in Figure 2.6(b); Port1 and Port2 are at the upper left corner and upper right corner between the EBG-implemented plane and the bottom solid plane, respectively. Then, S_{21} is simulated using

Sphinx. As shown in Figure 2.6(c), S_{21} has a stopband formed around 1.5 GHz. At 1.5 GHz, S_{21} has the isolation level of -104.7 dB. For a fair comparison between different structures, the stopband is defined to be the frequency range over which the isolation level is below -75 dB. In this example, the stopband ranges from 1 GHz to 2.7 GHz, implying that the EBG structure functions as desired. The EBG structure stops the propagation of electromagnetic waves by becoming a high-impedance surface around the target frequency. Over the target frequency range, the energy is confined to the excited unit cell.

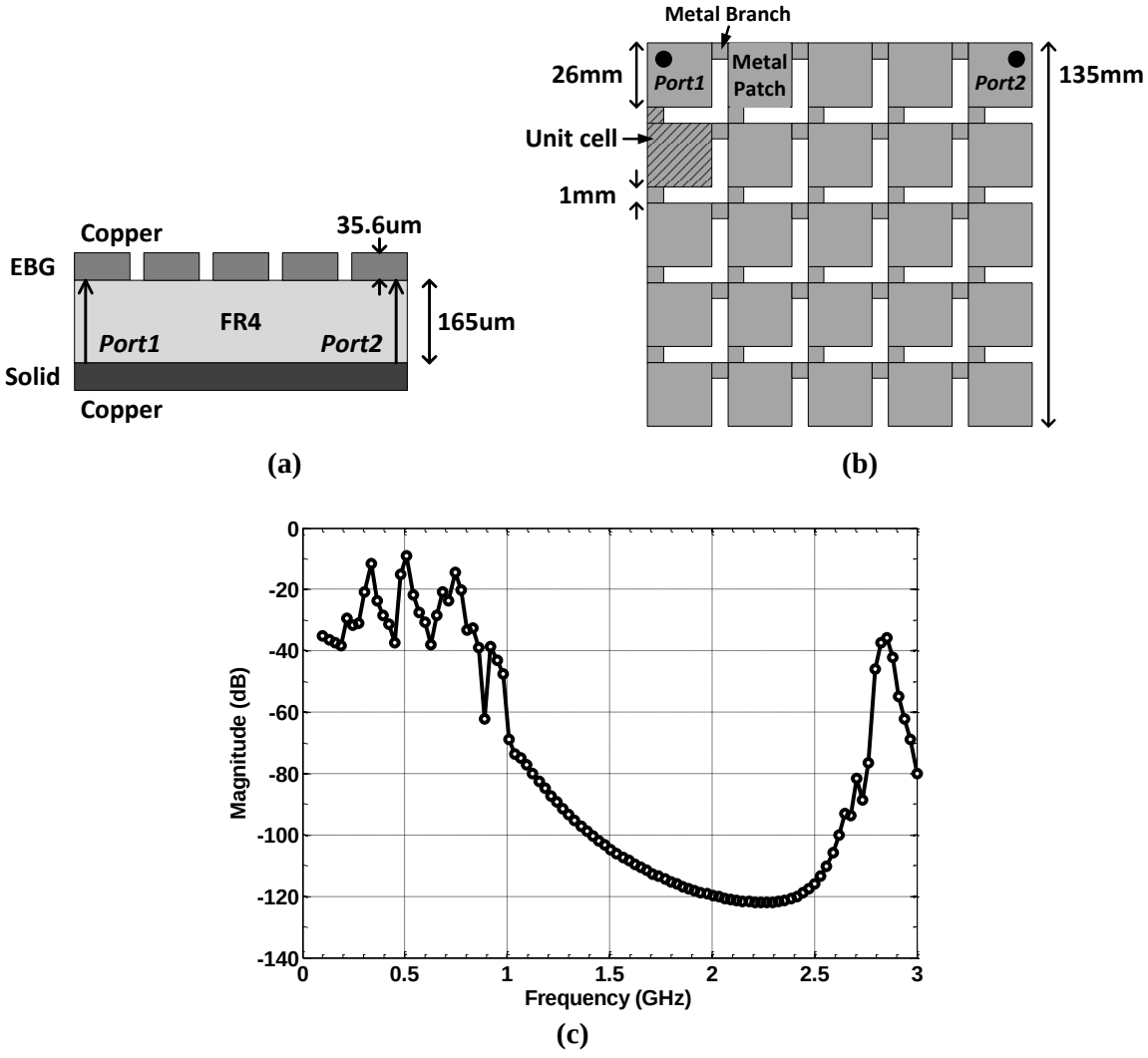


Figure 2.6 Two-layer EBG structure. (a) Side view. (b) Top view with port locations. (c) Simulated S_{21}.

The voltage distribution on the EBG layer when Port1 is excited at 1.5 GHz is shown in Figure 2.7. The hot spot indicated by light color at the upper left corner is where the excitation is applied. At 1.5 GHz, the wave propagation is suppressed so that only the excited unit cell and the neighboring unit cells have voltages higher than ground (0 V), whereas the rest have a near-ground potential. The excitation is mainly confined within the unit cell where the excited port is located. In the simulation, the bottom plane was assumed to be an ideal ground plane so that the voltage distribution of the bottom plane is not shown.

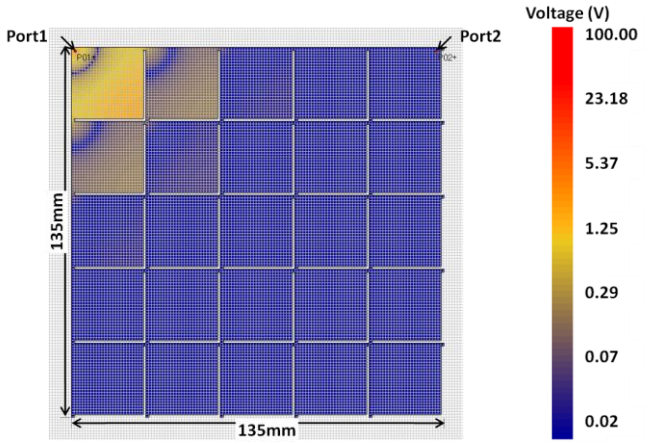
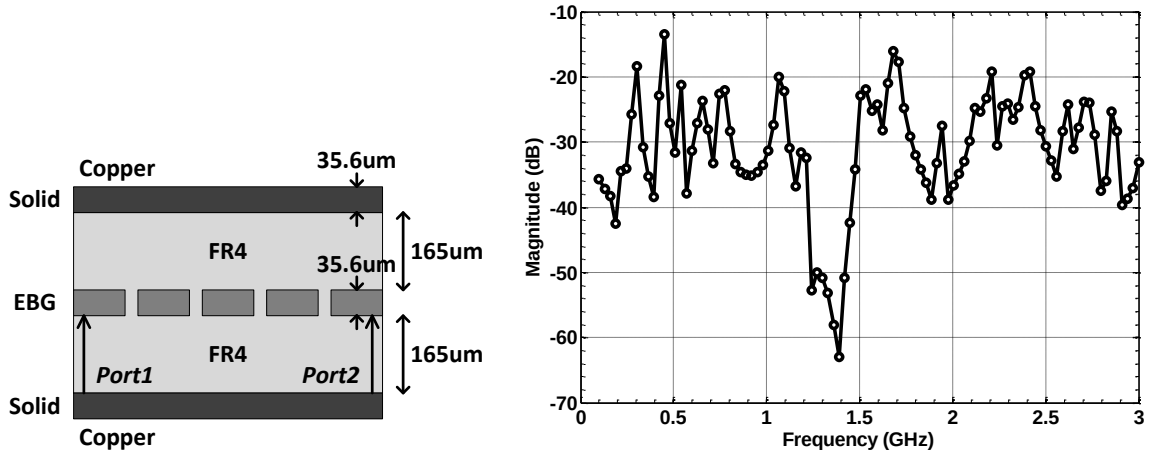


Figure 2.7 Voltage distribution on the EBG layer when Port1 is excited at 1.5 GHz.

2.3.2 Three-Layer EBG Structure: Embedded EBG Structure

When the two-layer EBG structure is covered by a solid plane, a three-layer embedded EBG structure is formed, as shown in Figure 2.8(a). The EBG layer is embedded in between two solid planes, and the structure is mirror-symmetric with respect to the middle EBG layer in terms of physical dimensions. Port1 and Port2 are at the upper left corner and upper right corner between the middle EBG layer and the bottom solid plane, respectively. The potential difference in the upper plane pair and the lower plane pair are independent of each other. As shown in Figure 2.8(b), the stopband in S_{21} becomes so narrow and shallow that it nearly disappears. The isolation level is only

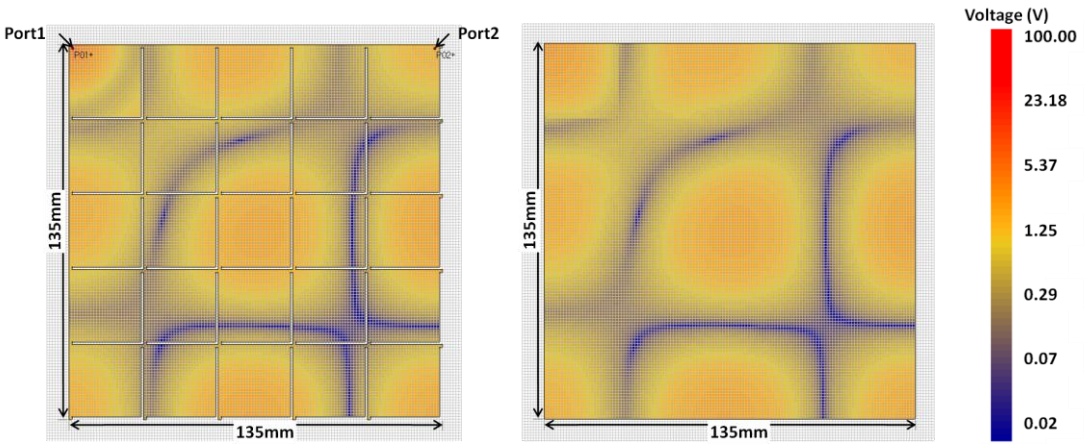
-22.95 dB at 1.5 GHz, which is not enough to suppress the propagation of the target frequency component. The embedded EBG structure fails to block the propagation of the desired frequency component.



(a) **(b)**

Figure 2.8 Three-layer embedded EBG structure. (a) Side view. (b) Simulated S_{21}.

The voltage distributions on the middle EBG layer and the top layer when Port1 is excited at 1.5 GHz are shown in Figure 2.9(a) and (b). As stated above, Port1 is located between the middle EBG layer and the bottom solid plane. Instead of being confined within the excited unit cell, the excitation spreads to the neighboring unit cells, and finally reaches even the most distant unit cell on the EBG layer, which is shown in Figure 2.9(a). The voltage distribution on the top layer is similar to that on the EBG layer, as shown in Figure 2.9(b), which is due to the propagation of electromagnetic waves in the upper plane pair over the target frequency range. Once again, it can be concluded that in the embedded EBG structure, the EBG structure does not provide the filtering property.



(a) **(b)**

Figure 2.9 Voltage distribution on planes when Port1 is excited at 1.5 GHz. (a) EBG layer (lower plane pair). (b) Top plane (upper plane pair).

2.3.3 Analysis of Failure

In the two-layer EBG structure, the EBG structure stops the propagation of electromagnetic waves by becoming a high-impedance surface over the target frequency range. As shown in Figure 2.10(a), the unit cells of the EBG structure resonate at the target frequency and block the propagation of the electromagnetic wave across the EBG layer. It either stays within the unit cell or propagates through the slots of EBG into the surrounding space (solid line), while the rest spread out across the EBG layer (dashed line). From the surface current perspective, the finite size of the metal patch is causing the suppression of current propagation across the EBG layer. In the target frequency range, current on the surface propagates into free space when it encounters any break in the surface [44]. As a result, it fails to spread throughout the EBG layer, and the energy is confined to the unit cell.

However, in the three-layer embedded EBG structure, the unit cell does not resonate as desired due to the top solid plane. The propagating wave from the lower plane pair toward the upper plane pair is affected by the top solid plane, and gets trapped in the upper plane pair. As shown in Figure 2.10(b), the magnetic part of the electromagnetic

wave coming from the excited Port1 propagates through the EBG slot (solid line). Since the propagating wave cannot escape the structure, it either stays in the upper plane pair or propagates back into the lower plane pair through EBG slots or via openings. The lateral- and vertical-propagation of the stopped wave changes the surface current characteristics on the EBG layer. As a result, the filtering property of the EBG structure is lost. The electromagnetic wave with frequencies outside the stopband propagates toward Port2 without any hindrance (dashed line).

The proposed arrangement to address the functional failure of the embedded EBG structure is shown in Figure 2.10(c), and will be explained in detail in the next section.

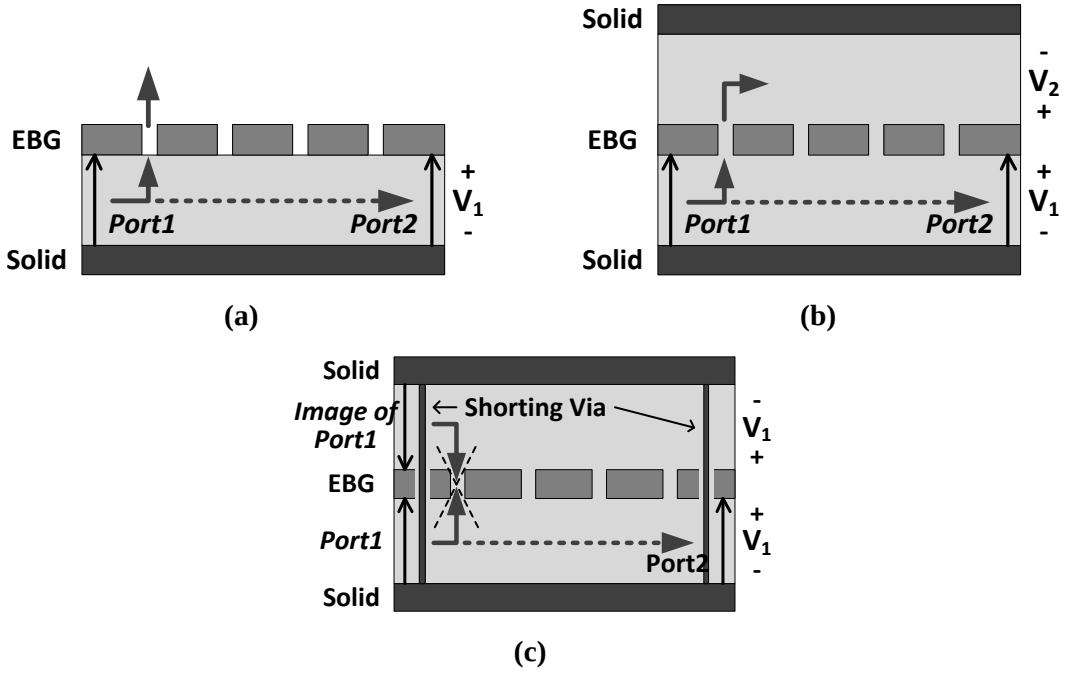


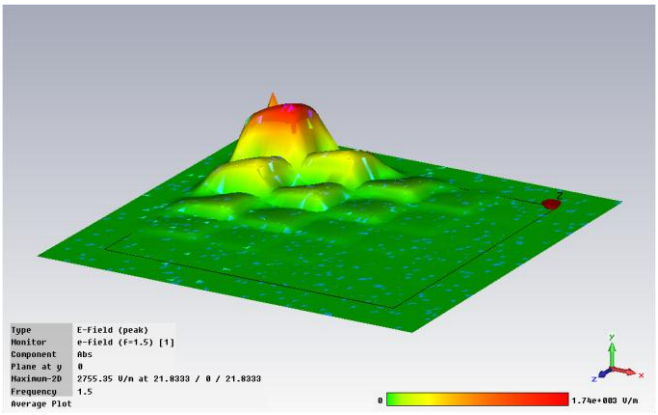
Figure 2.10 Propagation of electromagnetic wave. (a) Two-layer EBG structure. (b) Three-layer embedded EBG structure with the top and bottom planes at different potentials. (c) Three-layer embedded EBG with the top and bottom planes at the same potential.

The electric field distributions between the EBG layer and the bottom solid plane in the two- and three-layer EBG structures at 1.5 GHz are simulated using a commercially available full-wave electromagnetic solver, Microwave Studio by Computer Simulation Technology (CST MWS) [52]. The resulting distributions are compared in Figure 2.11.

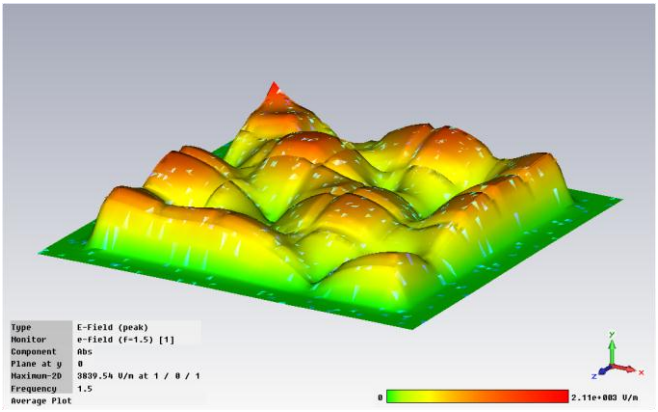
As expected from the voltage distribution shown above, the electric field stays within the excited unit cell and the neighboring unit cells in the two-layer EBG structure, having the local maximum value inside the unit cell. The unit cells which share neither edges nor vertices with the excited unit cell have near-zero electric field. The three-layer embedded EBG structure, on the other hand, has widespread electric field throughout the structure, which was also expected from the voltage distribution from Figure 2.9. In the three-layer embedded EBG structure, even the most distant unit cell from the excited unit cell had a non-zero voltage level, due to the presence of the electric field.

The simulated magnetic field distributions between the EBG layer and the bottom solid plane at 1.5 GHz are presented in Figure 2.12. The magnetic fields have similar distribution tendency as the electric fields. In the two-layer EBG structure, the magnetic field is mostly confined to the excited unit cell and the neighboring unit cells, as shown in Figure 2.12(a). In this case, the local maximum appears around the EBG slots due to the magnetic part of the electromagnetic wave propagating from Port1 toward the upper plane pair through the EBG slots. In the three-layer embedded EBG structure, the magnetic field is fully distributed from the excited unit cell to the most distant unit cell, as shown in Figure 2.12(b), showing that the surface current has spread throughout the structure.

Figure 2.11(c) and Figure 2.12(c) will be addressed along with Figure 2.10(c) in the next section.



(a)



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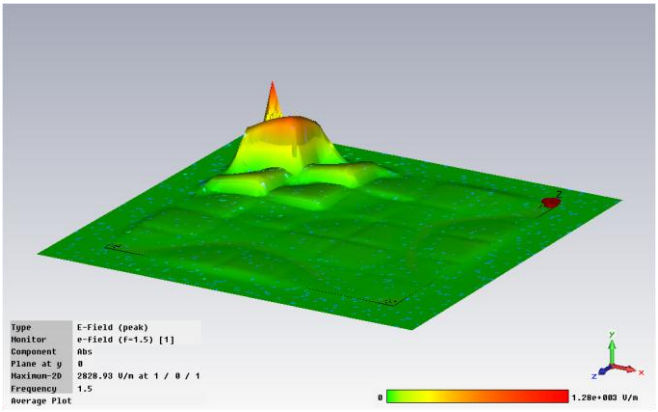
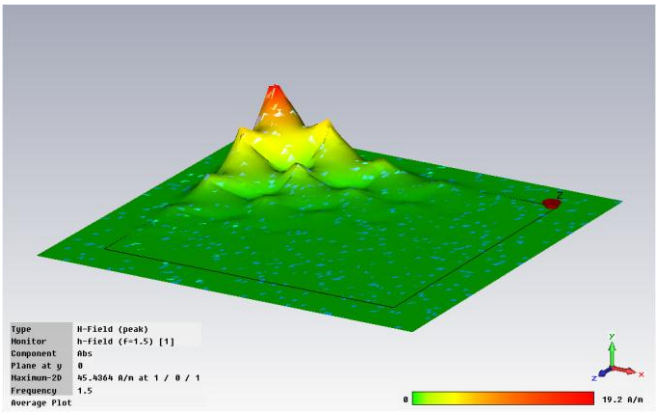
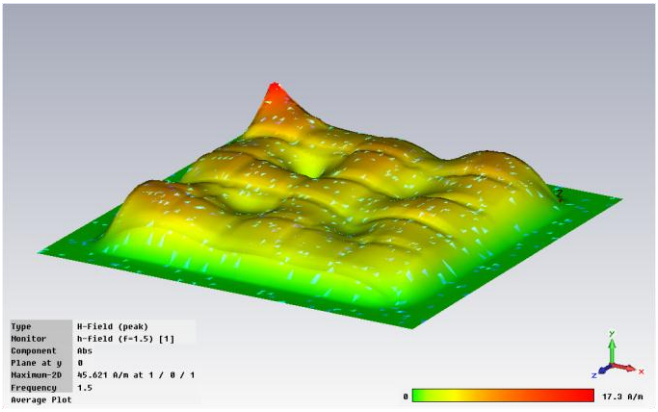


(c)

Figure 2.11 E-field in the lower plane cavity. (a) Two-layer EBG structure. (b) Three-layer embedded EBG structure. (c) Three-layer embedded EBG with vias.



(a)



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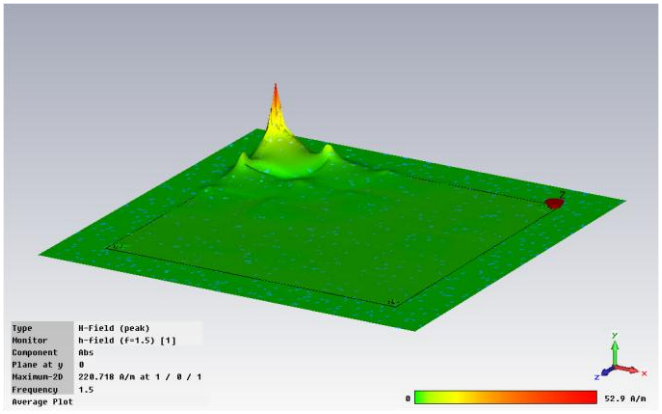


(c)

Figure 2.12 H-field in the lower plane cavity. (a) Two-layer EBG structure. (b) Three-layer embedded EBG structure. (c) Three-layer embedded EBG with vias.

Since the trapped wave in the upper plane pair is causing the functional problem in the three-layer embedded EBG structure, an intuitive solution is patterning the top-most

plane and releasing the trapped wave. In Figure 2.13(a), the same periodic pattern is implemented on the top layer as well as the middle layer. In the target frequency range, part of the electromagnetic wave coming from Port1 propagates into the upper plane pair through the EBG slots and then into the surrounding space through the slots on the top-most layer. The simulated S_{21} in Figure 2.13(b) shows that the stopband around the target frequency is recovered. The isolation level at 1.5 GHz is -111.8 dB. However, this three-layer embedded EBG structure with the slotted top plane cannot be an ultimate solution. As the structure is covered by a solid plane, the same problem will return so that the stopband will disappear again, which prevents the structure from being further embedded.

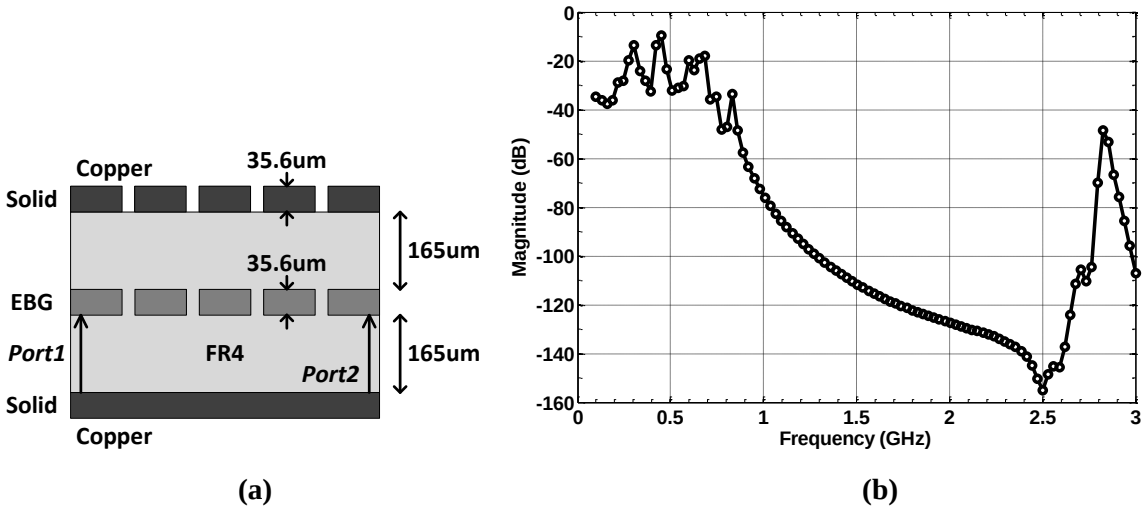


Figure 2.13 Three-layer embedded EBG structure with slotted top plane. (a) Side view. (b) Simulated S_{21}.

2.4 Embedded Electromagnetic Band Gap Configuration

2.4.1 Technical Approach

A method to restore the stopband of the embedded EBG structure is proposed to cancel the propagating component at the EBG slots. This can be achieved by having the planes above and below the EBG layer at the same potential and at equal distance from

the EBG layer. If the potentials of the top and bottom solid planes are the same, the upper and lower plane pair is mirror-symmetric about the middle EBG layer. When Port1 is located between the middle EBG layer and the bottom layer, a mirror image of the excitation is induced between the middle EBG layer and the top layer, as shown in Figure 2.10(c). The magnitude of the image excitation will be the same with the original excitation, but the phase with respect to the middle EBG layer will be reversed. As a result, destructive interference will occur between vertical-propagating components from the upper plane pair and the lower plane pair, cancelling each other out at the EBG slots. The electric and magnetic field distributions of the proposed embedded EBG structure are shown in Figure 2.11(c) and Figure 2.12(c). The distribution patterns are similar to those of the two-layer EBG structure, implying that the proposed EBG structure has regained the filtering property.

The lateral and vertical propagation of the electromagnetic wave over the target frequency range can also be explained by an analogy between the two-layer EBG structure and the microstrip patch array antenna. A unit cell of the two-layer EBG structure is analogous to a microstrip patch antenna, which uses the cavity resonance for radiation at the desired frequency. Throughout this chapter, the term radiation refers to the propagation of the surface wave into free space, which results in a strong near field. Therefore, the two-layer EBG structure corresponds to the array of microstrip patch antennas. Since the lateral dimensions of the two-layer EBG structure are much greater than the vertical dimensions, which is much less than the wavelength, the structure can be reduced to a two-dimensional cavity [16]. The dimensions and electric parameters of the cavity determine the resonant frequency and the far field radiation pattern of the patch antenna [53]. When the antenna is excited at the resonant frequency, the energy radiates due to the fringing field over the edges of the patch. The same principle can be extended to the two-layer EBG structure. As the structure is excited at the resonant frequency, the electromagnetic wave radiates through the slots between the excited unit cell and the

neighboring unit cells. According to the surface equivalence principle, the source of radiation can be represented by equivalent electric and magnetic currents. In Figure 2.14(a) and (b), the equivalent sources of the rectangular cavity are the magnetic currents around the periphery of the patch over the original slots. Figure 2.14(a) illustrates a pair of planes with a thin dielectric. The top plane is used as a rectangular patch, while the bottom plane as a ground plane. Figure 2.14(b) shows the reversed version of the structure in Figure 2.14(a). The equivalent magnetic currents are shown in these two mictrostrip path antenna cases.

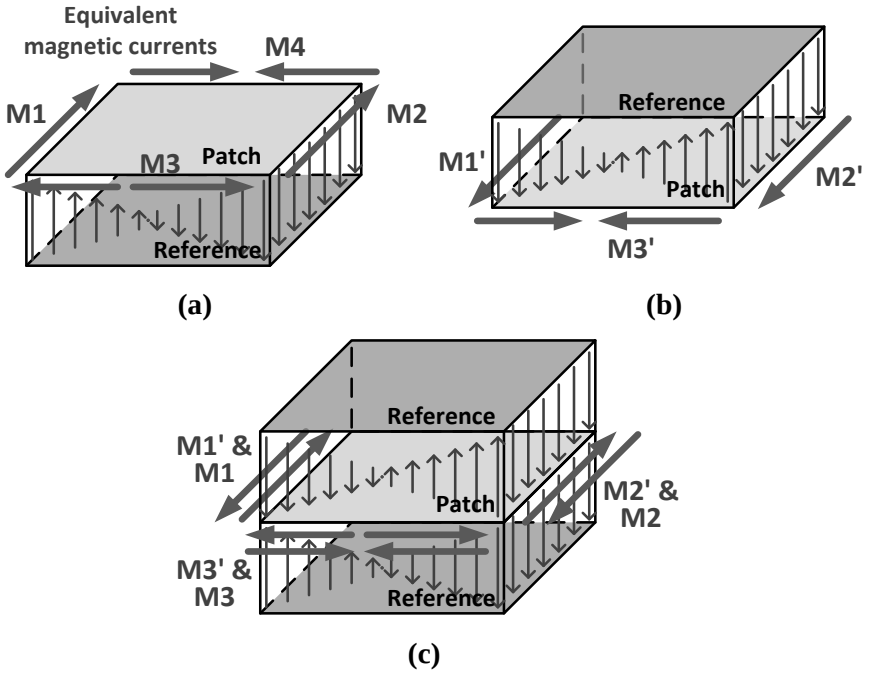


Figure 2.14 Equivalent magnetic current of cavity resonators. (a) Cavity with a lower reference plane. (b) Cavity with an upper reference plane. (c) Stacked cavities sharing the middle patch layer.

A unit cell of the three-layer embedded EBG structure is analogous to placing the rectangular patch in a stripline-like environment. The analogous structure is made when the two microstrip patch antennas in Figure 2.14(a) and Figure 2.14(b) are stacked vertically sharing the middle rectangular patch, as shown in Figure 2.14(c). Here, two sets of the equivalent magnetic currents are shown around the periphery of the patch; one

set is induced by the upper rectangular cavity, and the other set by the lower rectangular cavity. Since the top and bottom reference planes do not have the same potential, the corresponding equivalent magnetic currents have different magnitudes from each other. The resulting equivalent currents of the stacked structure in Figure 2.14(c) become the sum of the equivalent currents of the structures in Figure 2.14(a) and Figure 2.14(b), causing the stacked structure to behave differently during resonance.

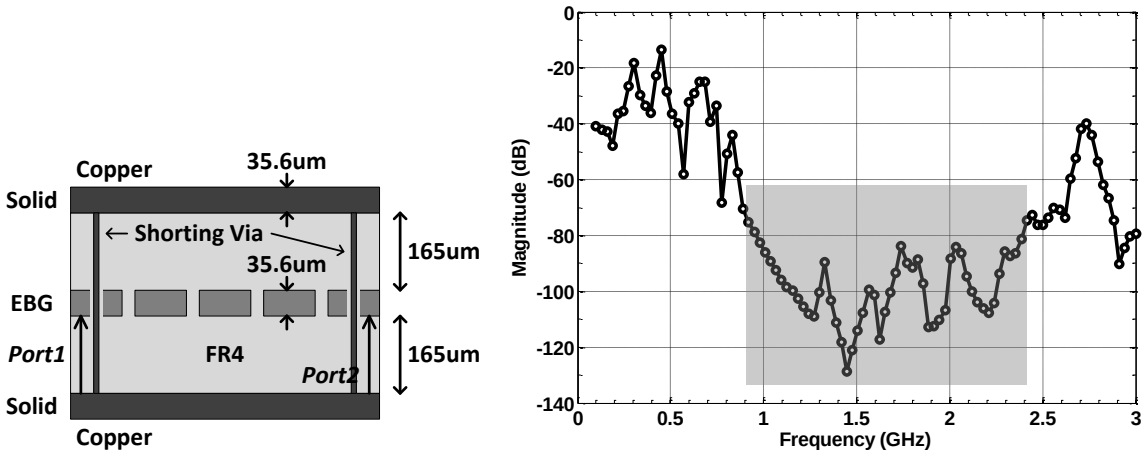
A unit cell of the three-layer embedded EBG structure with vias interconnecting the top and bottom planes is also equivalent to the stacked cavity resonator shown in Figure 2.14(c). Since the top and bottom reference planes are connected by vias, an excitation referenced to the bottom plane induces a mirror-image excitation referenced to the top plane. As a result, the actual excitation and the virtual excitation have the same magnitude, but opposite phases. When an excitation at the resonance frequency is applied, the resulting radiation can be modeled as two sets of equivalent magnetic current around the patch: one set is induced by the upper rectangular cavity, and the other set by the lower rectangular cavity. The components of the two sets have the same magnitude, but opposite phases. Thus, they cancel each other out. In the same manner, the radiated components from the upper and lower plane pair interfere with each other destructively, resulting in poor radiation. Therefore, the three-layer embedded EBG structure with vias is able to suppress the propagation of the electromagnetic wave at the resonant frequency.

2.4.2 Proposed Embedded EBG Structure

The cross section view of the proposed embedded EBG structure is shown in Figure 2.15(a). Via connections are added between the top and bottom solid planes to hold them at the same potential. Six through-hole vias are randomly placed around each port. They are placed near ports so that the image excitation can be as same as the original excitation as much as possible. The port setting was kept identical to the previous three-layer embedded EBG structures. In Figure 2.15(b), the simulated S_{21} is shown. The stopband

around the 1.5 GHz has been restored, and the bandwidth is as wide as that of the two-layer EBG structure. The isolation level at 1.5 GHz is -113.9 dB. This implies that the interaction between the upper and lower plane pair is minimized by the destructive interference. As a result, the desired function of the EBG structure is achieved even in a stripline-like environment. Moreover, when a signal layer comes above the embedded EBG structure, the top solid plane secures the return current paths for signal lines, which could not be achieved by the three-layer EBG structure with the slotted top plane.

The reason that the stopband is not exactly the same as that of the basic two-layer structure is due to the limitation of 6 vias. The isolation level from 1.7 GHz to 2.1 GHz is less than -100 dB, while that in the two-layer structure is greater than -100 dB. Also, the shape of S_{21} over the stop-band is not as smooth as in the two-layer structure. As the number of vias increases, both the depth and shape of the stopband improve; here, the number of vias is one of the key design parameters. This is further explained using simulation results in the following section.



(a) **(b)**

Figure 2.15 Proposed three-layer embedded EBG structure with vias. (a) Side view. (b) Simulated S_{21}.

The voltage distribution of the proposed structure shown in Figure 2.16 demonstrates the functionality. Unlike the voltage distribution of the previous three-layer embedded

EBG structure, the excitation stays inside the excited unit cell and the neighboring unit cells on both the EBG layer and the top plane.

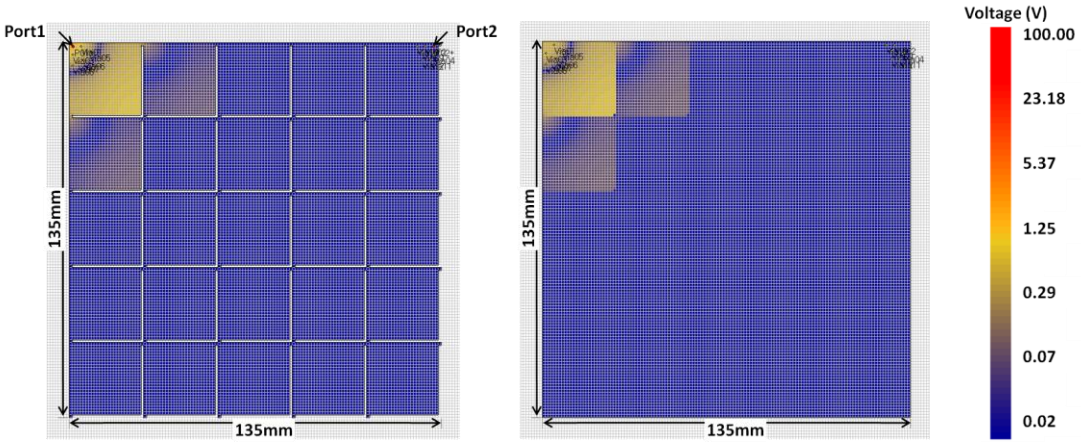


Figure 2.16 Voltage distribution of the two plane pairs with interconnecting vias when Port1 is excited at 1.5 GHz. (a) EBG layer (lower plane pair). (b) Top plane (upper plane pair).

2.4.3 Measurements

To demonstrate the proposed solution, three pre-simulated structures were fabricated on the FR4 substrate, as shown in Figure 2.17. Copper was used for the metal layer, and FR4 was used for the dielectric layer. The thickness of copper was 35.6 μm, and that of FR4 was 165 μm. The feature sizes of the implemented EBG structures were the same as those of the simulated EBG structures: the unit cell size was 26 mm by 26 mm, and the EBG layer consisted of 25 unit cells. Ports 1 and 2 were at the upper left corner and the upper right corner between the EBG layer and the bottom solid plane, respectively. In the case of the three-layer embedded EBG structure with vias, 6 vias were used per port, and they were placed near the ports, as shown in Figure 2.17(c).

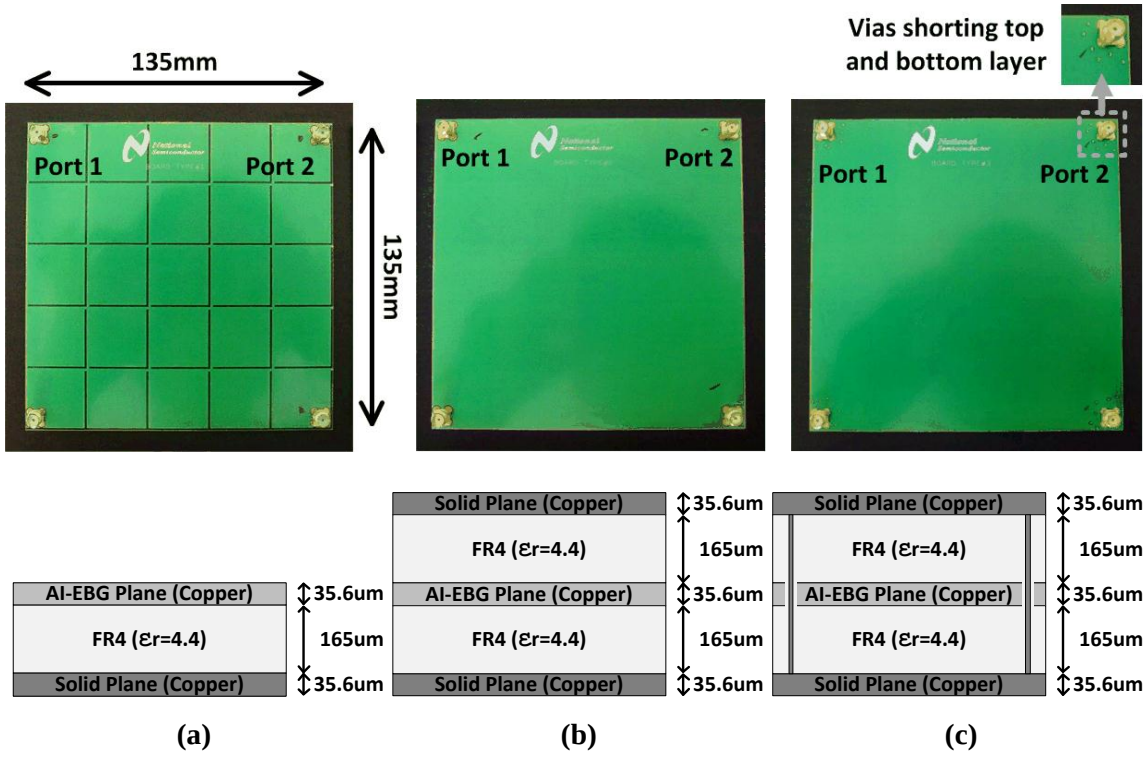
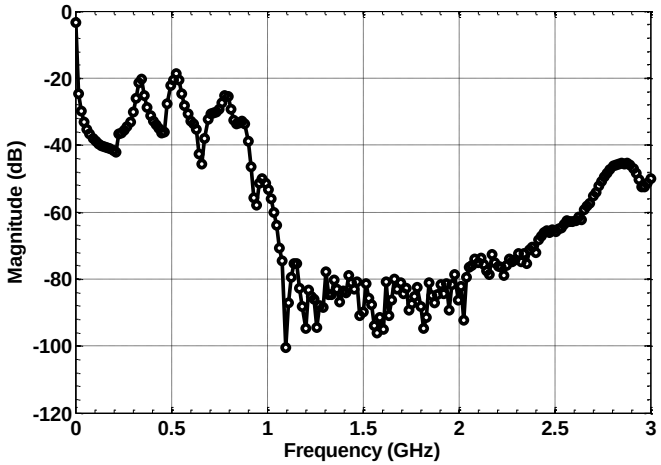
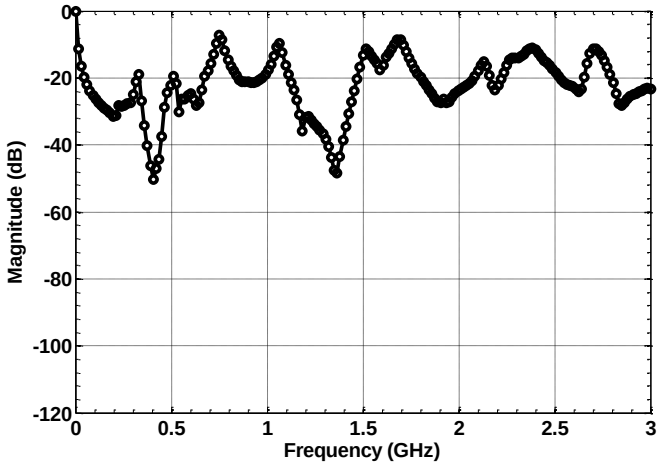


Figure 2.17 Three test vehicles. (a) Two-layer EBG structure. (b) Three-layer embedded EBG structure. (c) Proposed three-layer embedded EBG structure with vias.

An Agilent 8714 ET RF network analyzer was used to measure S-parameters from 1 MHz to 3 GHz. Figure 2.18 shows S_{21} for each type of structure. The target stop frequency was 1.5 GHz. S_{21} of the two-layer EBG structure in Figure 2.18(a) has a stopband from 1.1 GHz to 2.3 GHz with the isolation level greater than -75 dB, whereas S_{21} of the three-layer embedded EBG structure in Figure 2.18(b) does not have the stopband. The magnitude of S_{21} is -12 dB at 1.5 GHz. As expected from previous simulations, with interconnecting vias between the top and bottom planes, the embedded EBG structure regains the stopband whose frequency range is similar to that of the two-layer EBG structure, as shown in Figure 2.18(c). The stopband with the isolation level greater than -75 dB ranges from 1 GHz to 2.5 GHz.



(a)



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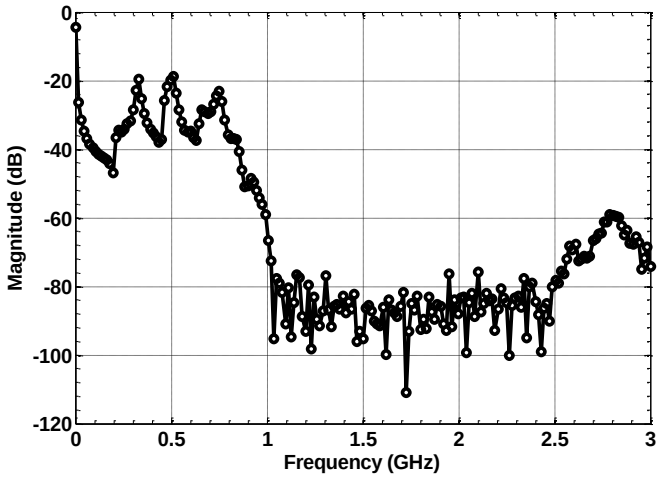


(c)

Figure 2.18 Measurements of S_{21} of three test vehicles. (a) Two-layer EBG structure. (b) Three-layer embedded EBG structure. (c) Proposed three-layer embedded EBG structure with vias.

2.5 Embedded EBG on the Load Board

Following the newly suggested design methodology, the EBG structure was implemented on the power plane, as shown in Figure 2.4, and the layer order was modified to satisfy the arrangement of the proposed embedded EBG structure, as shown in Figure 2.19. Comparing the modified layer stack-up to the original layer stack-up, the layer order of the GND plane, which is the 9th layer, and the VA+VDR power plane, which is the 10th layer, was reversed. Consequently, the power plane was embedded in between two ground planes. The distance from the power plane to each GND plane is the same. The layer modification does not induce any additional return path discontinuity (RPD) because the 7th layer is still referenced to the solid ground plane, which is the 8th layer. All the signal layers have the solid reference ground planes even after the layer order modification. Fifty four vias were used to connect the upper and lower GND planes. The locations of vias were extracted from the original load board. Hundreds of vias were used to connect 9 ground planes in the original load board, but only 54 of them were randomly selected to be used in the modified load board to simplify the simulation.

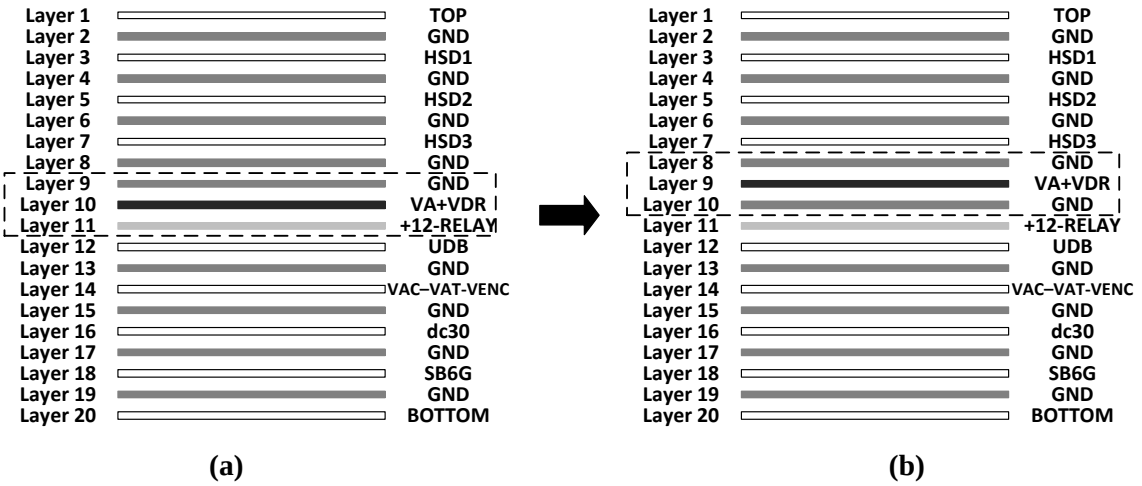
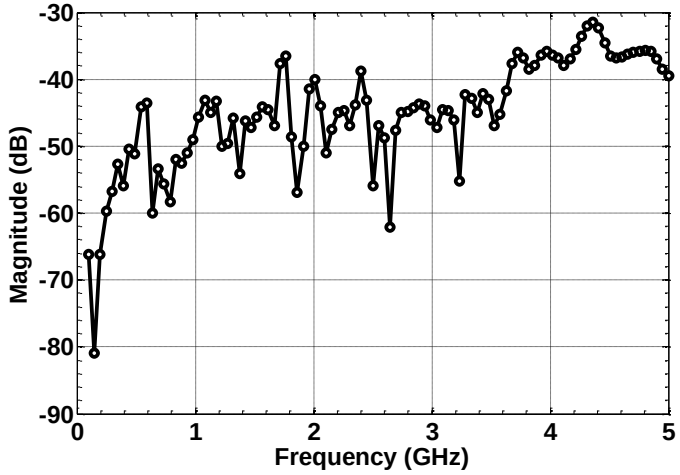


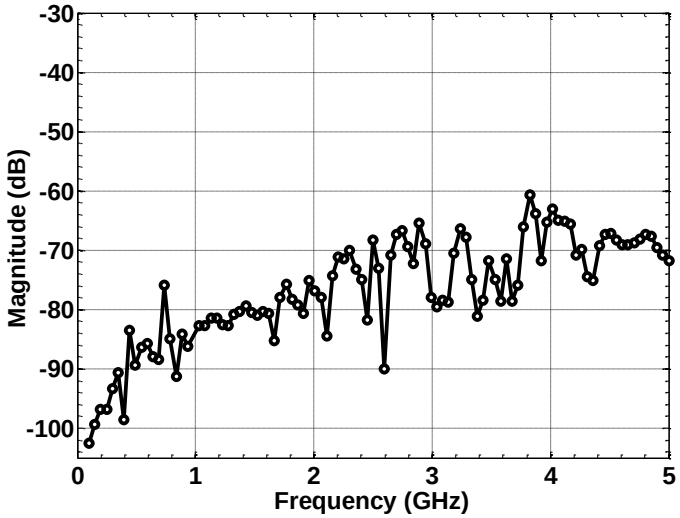
Figure 2.19 Layer stack-up of the load board. (a) Before layer modification. (b) After layer modification.

The port setup is the same as in Section 2.2.2: Port1 is a noise aggressor on the

digital power plane, and Port2 is a noise victim on the analog power plane. In Figure 2.20, S_{21} between one noise aggressor and one noise victim on the modified power plane is shown. The level of coupling is less than -60 dB over the frequency range from 0.1 to 5 GHz. After the EBG implementation and layer modification, S_{21} is reduced down to -81 dB at 1.5 GHz, as shown in Figure 2.20(b). The stopband, over which the magnitude of S_{21} is less than -75 dB, ranges from 0.1 GHz to 2.2 GHz. The reason that the S_{21} in Figure 2.20(b) does not have an explicit stopband is because the victim port (Port2) is not placed in the EBG unit cell. The EBG structure is implemented to inhibit the switching noise propagation from the noise source (power pins for the digital drivers) to the rest of the digital power plane. It leads to the suppression of the inter-plane noise coupling from the digital power plane to the analog power plane over the plane-split gap. Therefore, the isolation level is reduced over the entire frequency range instead of over only the stopband.



(a)



(b)

Figure 2.20 Simulation result of S_{21}. (a) Before plane and layer modification. (b) After EBG implementation and layer modification.

For each noise victim, S_{21} was simulated with all the noise aggressors. This was repeated fifteen times to cover all the noise victims. In Figure 2.21, two sets of bar graphs indicating the magnitude of S_{21} at 1.5 GHz are shown. Each pair of bars represents S_{21} between one noise victim and each of the noise aggressors before and after modification. In Figure 2.21(a), 16 pairs of bars compare the magnitudes of S_{21} at 1.5 GHz between the 2^{nd} analog power pin (noise victim) and the 16 digital power pins (noise aggressors) before and after the plane and layer modifications. The bar graph in Figure 2.21(b) was

obtained at the 11th analog power pin. At both analog power pins, the level of noise isolation increases after the proposed embedded EBG implementation. At the 2nd analog power pin, the average isolation level improves from -52.94 dB to -97.46 dB, and at the 11th analog power pin, it improves from -54.7 dB to -106.4 dB. Similar improvements are achieved at the other analog power pins in terms of isolation level.

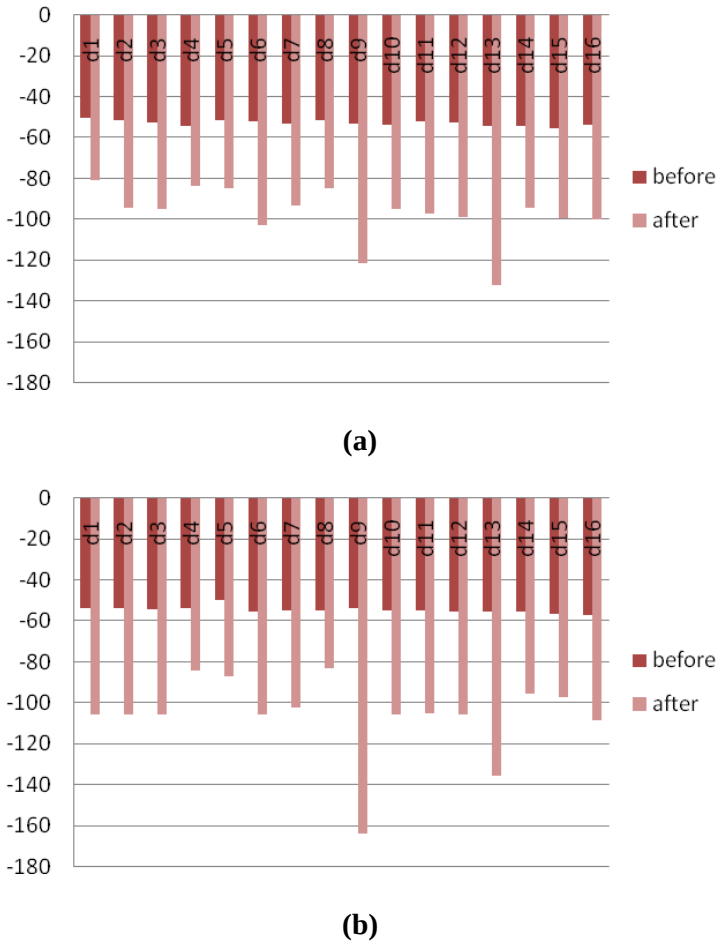


Figure 2.21 S_{21} before and after embedded EBG integration at 1.5 GHz. (a) 2nd analog power pin. (b) 11th analog power pin.

2.6 Design Guidelines

In this section, the design parameters of the proposed embedded EBG structure and their impact on the filtering property are explored in detail.

1) Two solid planes of equal potential should be at equal distances from the middle EBG plane.

For perfect destructive interference, the amount of vertical propagation through the EBG slots should be the same. In the case of a microstrip patch antenna, the radiated power of the rectangular patch depends on the dimensions of the cavity, which consists of a rectangular patch and a corresponding ground plane. For example, when the TM10 mode is the dominant mode, the radiated power can be calculated as:

$$P_{rad} = \frac{k^2 h^2 b^2}{2\eta\pi^2}\left|E_{10}\right|^2 \int_{\phi=0}^{2\pi}\int_{\theta=0}^{\pi/2}\cos^2 K_1 \cdot \mathrm{sinc}^2 K_2 \cdot \{\cos^2\phi + \cos^2\theta \sin^2\phi\} \cdot \sin\theta d\theta d\phi \quad (2)$$

$$K_1 = \frac{ka\sin\theta\cos\phi}{2}, \quad K_2 = \frac{kb\sin\theta\sin\phi}{2}$$

where ‘a’ and ‘b’ are the length and width of the rectangular patch, and ‘k’ and ‘h’ are the wave number and the dielectric thickness, respectively [53]. A similar approach can be applied to the embedded EBG structure to balance the energy propagation coming from the original excitation and the image excitation. Since the thickness of the substrate has an impact on the amount of vertically-propagating energy, it should be the same to have the same amount of the energy propagation from the upper and lower plane pair. This will lead to perfect cancellation, maximizing the noise filtering property of the embedded EBG structure.

As shown Figure 2.22, when *d* increases from 0.2 mm to 0.4 mm, the EBG structure almost loses the stopband even with vias. The isolation level at 1.5 GHz reduces roughly from -120 dB to -60 dB. When *d* is equal to 0.6 mm or 0.8 mm, the stopband is still very narrow and shallow. When *d* is increased to 1.0 mm, the stopband reappears even though the width and depth are not fully recovered as compared to those of the symmetric structure. If *d* increases to be even thicker, the stopband will gradually improve. This is because as *d* gets thicker, the space between the EBG structure and the top solid plane increases and the influence of the top solid plane upon the middle EBG layer decreases.

When *d* is increased to be of the order of centimeters or more, the structure will eventually start behaving like a two-layer EBG structure.

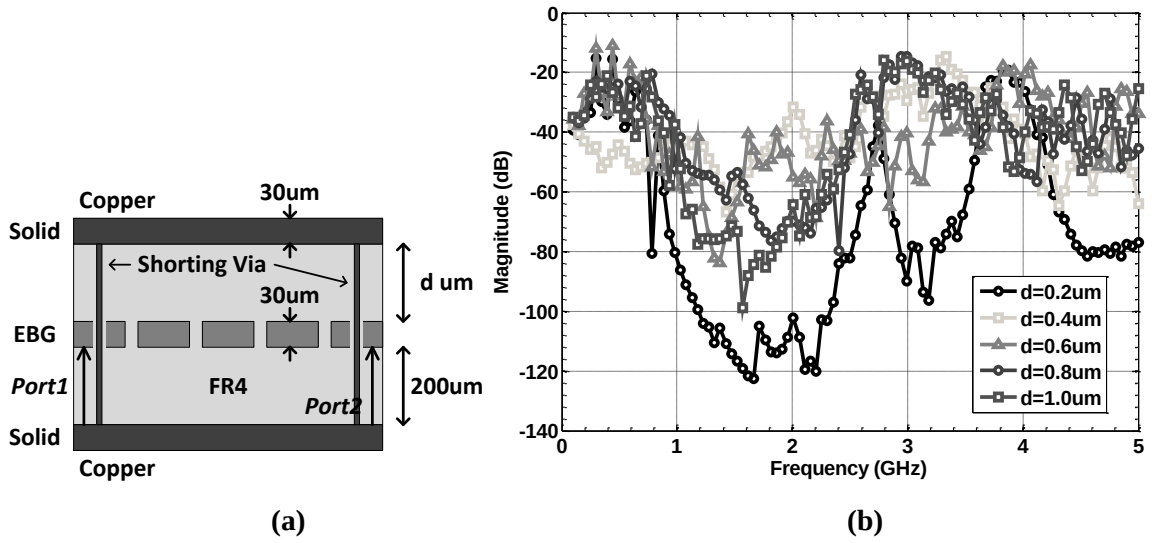


Figure 2.22 Effect of the dielectric thickness. (a)'d' as a design parameter. (b) Simulated S_{21} with various dielectric thicknesses 'd'.

2) As much as possible, lots of via connections should be placed next to nodes at which the source and sink are located.

Since the upper and lower plane pairs share the middle EBG layer, the similarity between the image excitation and the original excitation depends on the dimensions of the plane pairs and the potentials of the two planes. As the potential difference between the two solid planes becomes near-zero, the image excitation can successfully reproduce the original excitation. The perfect destructive interference can then be achieved, which will be followed by improved stopband performance. Interconnecting vias are used to make the top and bottom planes have the same potential especially around the excitation port. Since vias provide the dc connection between the top and bottom solid planes, the number and location of vias are critical design parameters. Two design parameters, which are the number of vias and the proximity of vias to the port, are studied in this section.

By increasing the number of vias, the dc level of the two solid planes will have less discrepancy. Then, the image excitation in the upper plane pair approximates to the

original excitation in the lower plane pair. Figure 2.23(a) depicts three unit cells with three different numbers of vias: 7 vias/port, 3 vias/port, and 1 via/port. Here, vias are shown on the unit cell to illustrate the number of vias per port and per unit cell. Vias are not actually connected to the middle EBG layer, but are connected to the top and bottom solid planes. In Figure 2.23(b), as the number of vias increases from 1 to 3 and 7, the isolation level improves. The increased number of vias leads to smaller potential difference, and the stopband attenuation is therefore improved.

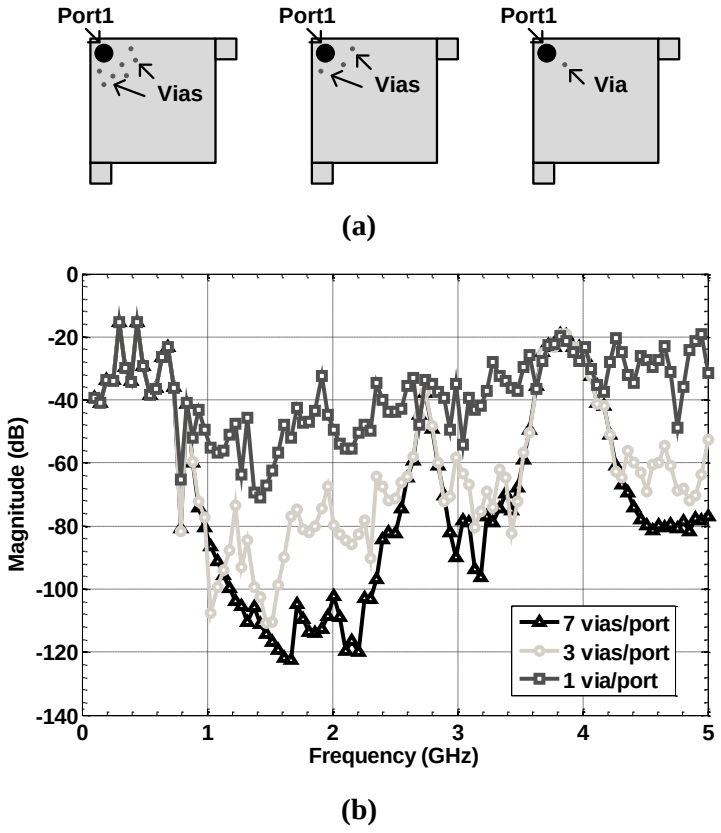
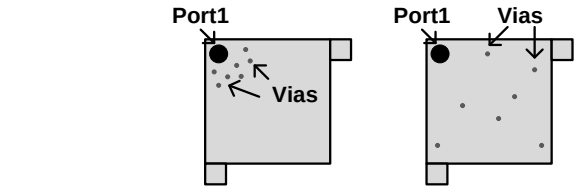


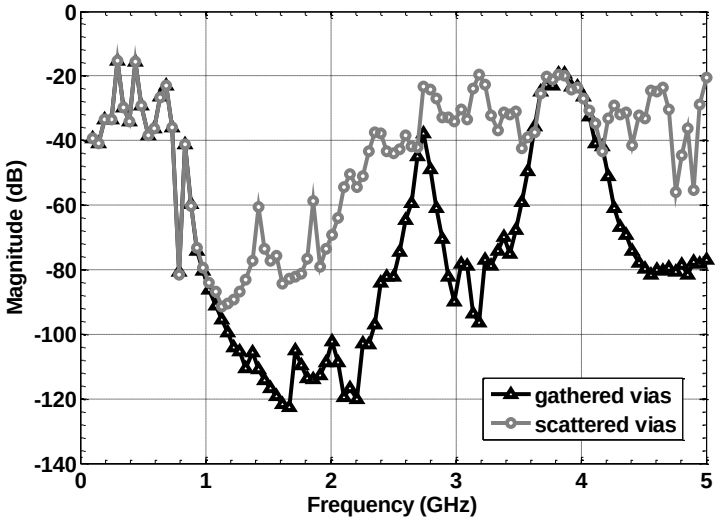
Figure 2.23 Effect of the number of vias. (a) Unit cells with various numbers of vias : 7, 3, and 1 via. (b) Simulated S_{21} with various numbers of vias.

Also, when vias are placed closer to the excited port, the two solid planes will have the same potential around the port in a steadier and more stable manner. In this case, the proximity of vias to each other increases the mutual inductances, thereby increasing the total inductance. However, since the purpose of using vias is to provide a dc connection between the top and bottom planes, the increased mutual inductance does not affect the

functioning of vias, which is there to generate an electrical mirror-image of the excitation. When vias are placed away from the excited port, the voltage symmetry between the upper and lower plane pair will be broken. This will induce the non-perfect cancellation of the two propagating components from the upper and lower plane pair. In Figure 2.24(a), two cases are compared: when vias are closely located around the port versus when vias are scattered inside the unit cell. Both structures have the same number of vias per port: 7 vias/port. Here, the distribution of vias is shown on the unit cell to illustrate the proximity of vias to Port1.



(a)



(b)

Figure 2.24 Effect of the proximity of vias. (a) Unit cells with two kinds of via distribution around the port. (b) Simulated S_{21} with two different distributions of vias.

Vias are not actually connected to the middle EBG layer, but are connected to the top and bottom solid planes. As shown in Figure 2.24(b), the isolation level and bandwidth of the stopband are more shallow and narrow when vias are scattered. The vias that are too

far from the excited and measured ports hardly contribute to providing the symmetry between the upper and lower plane pair. Therefore, via interconnecting the top and bottom planes should be placed close to the ports.

2.7 Summary

A new design technique for an embedded EBG structure has been proposed for load board applications. Three types of structures were used to define the problem and to suggest the solution. Both the problem and solution have been analyzed technically, and the analysis was demonstrated with simulation and measurement of experimental test vehicles. Multi-layer load board for high-speed and high-resolution ADC was designed with the proposed design technique and simulated to demonstrate the effectiveness of the embedded EBG structure in noise suppression and isolation.

The major contributions of this chapter include theoretical and simulation based analysis of the failure mechanism of the embedded EBG structure. Accordingly, a new design method has been proposed to recover the noise filtering function of the embedded EBG structure. It includes the following guidelines: first, an embedded AI-EBG should be sandwiched between planes of equal potential; second, the planes of equal potential should be at equal distances from the object EBG layer; and third, as possible, vias connecting the upper & lower planes should be placed next to noise aggressors. The proposed solution is demonstrated using three experimental test vehicles, which is then applied to a prototype load board for a gigahertz ADC. With the suggested design techniques, the embedded EBG structure can be applied to various mixed-signal boards to control power/ground noise.

CHAPTER 3

CONSTANT CURRENT POWER TRANSMISSION LINE

3.1 Introduction

3.1.1 Power Transmission Line

Current transients on the power delivery network (PDN) cause power supply noise. The increasing operating frequency of integrated circuits (ICs) and the growing power density induce an increase in the amount of transient current drawn from the PDN, contributing to the rising importance of power supply noise [9]-[12]. The power supply noise is a major component of simultaneous switching noise (SSN) in high-speed systems, which can cause functional failures or incorrect bits to be transmitted and received [16].

Most PDNs in high-speed systems consist of power and ground planes to provide a low-impedance path between the voltage regulator module (VRM) and the IC on the printed circuit board (PCB). For off-chip signaling, charging and discharging signal transmission lines induce return currents on the power and ground planes. The return current always follows the path of least impedance on the reference plane closest to the signal transmission line [16]. The return current path plays a critical role in maintaining the signal integrity of the bits propagating on the signal transmission lines.

As described in [17] and [18], interruption in the return current path leads to return path discontinuities (RPDs). The disruption between the power and ground planes induces RPDs during the data transitions even with a solid reference conductor underneath the signal transmission line., which create displacement current sources between the power and ground planes, as shown in Figure 3.1(a) [16]. These sources

induce excessive power supply noise, which requires the reduction of the PDN impedance so as to suppress the excessive noise caused by the current transients. The current solution to this problem is the use of decoupling capacitors or shorting vias at the RPD locations [26]-[32][35]-[37], or the use of new technologies with thin dielectrics between the power and ground planes [33][34]. These are often times expensive solutions.

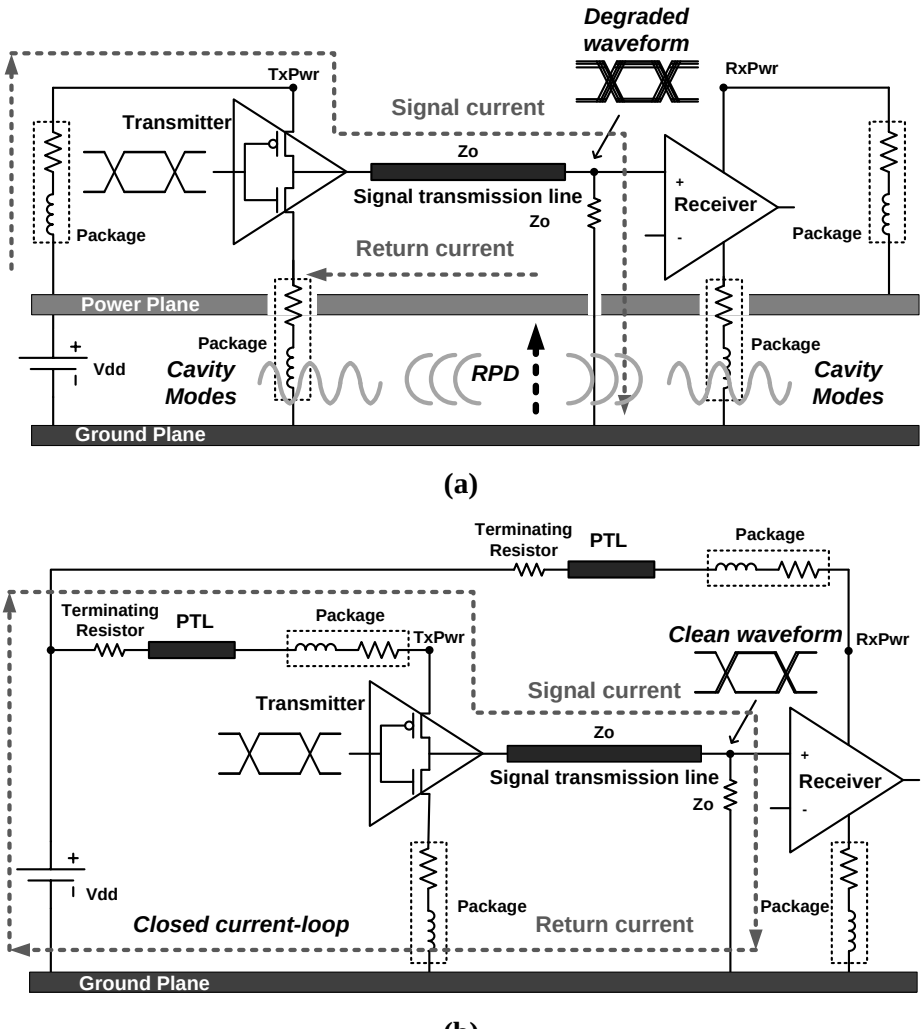


Figure 3.1 Chip-to-chip communication. (a) Plane-based with a power plane as a reference conductor. (b) PTL-based with a ground plane as a reference conductor.

In this chapter, a new solution is proposed to reduce the layer count, remove the effect of cavity modes, and help eliminate the decoupling capacitors for mitigating RPDs.

This solution is based on the Power Transmission Line (PTL) concept [54]. In this approach, transmission lines replace the power plane to convey power from the VRM to each IC on the PCB, and hence are called as Power Transmission Lines. The PTL-based PDN enables both power and signal transmission lines to be referenced to the same ground plane so that a continuous current path can be achieved, as shown in Figure 3.1(b), Therefore, the RPD effects are removed, unlike the power-plane-based PDN, as shown in Figure 3.1(a).

Though using PTLs solves the RPD issue, it generates other problems such as: 1) output-data-dependent dc drop on the PDN due to the terminating resistance, 2) mismatch effect between the PTL and the termination, 3) line congestion, and 4) increased power consumption. Firstly, the state of the output data dictates whether the output driver draws current from the PDN or not, resulting in the fluctuation of the dc level on the PTL. Secondly, using transmission lines can cause impedance mismatch in power transmission lines due to manufacturing variation. Thirdly, if one PTL is used per I/O driver, the number of lines on the PCB doubles and causes congestion. Lastly, as the signaling scheme and the I/O driver are adjusted to accommodate the new PDN, the required power to transmit 1 bit of data changes, requiring careful analysis of the power consumption. To make the PTL feasible in a realistic environment, these issues need to be addressed first, which is the focus of the next section.

3.1.2 Limitations of using Power Transmission Line

The PTL-based signaling scheme is shown in Figure 3.2. In Figure 3.2(a), the PTL is source-terminated with a resistor of 25 ohm matched impedance. The reason for the source termination of the PTL is to prevent multiple reflections when there is an impedance mismatch between the signal transmission line and load-terminating resistor. The other end of the PTL is connected to a signal network, which consists of an I/O driver, a signal transmission line and a terminating resistor. The impedance of the signal

network is carefully designed, considering the PTL impedance and the desired eye height. The PTL and signal transmission lines are referenced to a common ground plane, thereby eliminating RPDs during both transitions of the driver.

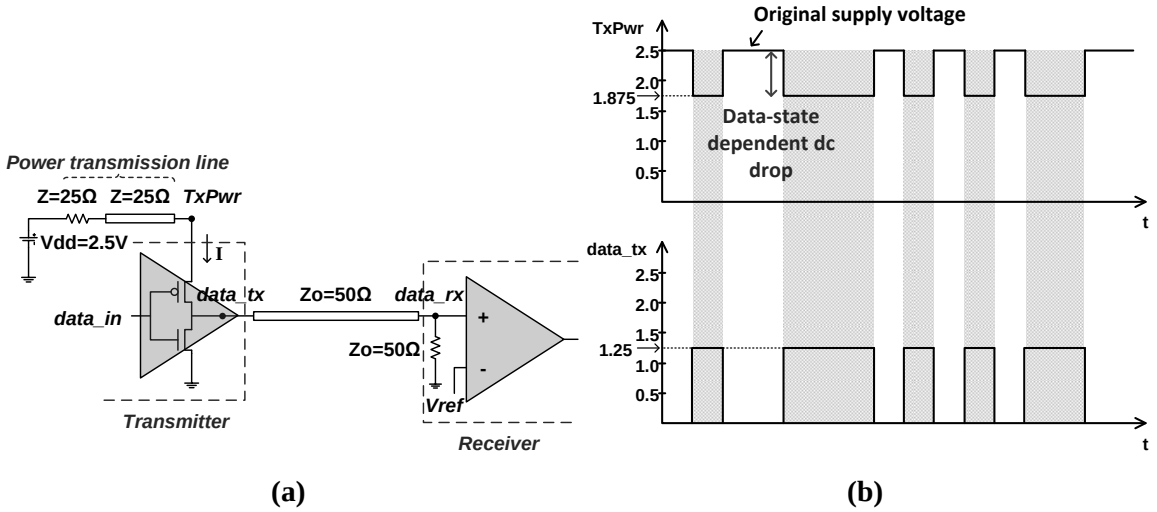


Figure 3.2 Single-ended signaling using PTL. (a) Schematic. (b) Waveform.

An issue that arises with the PTL-based signaling scheme is dynamic dc drop due to the terminating resistance between the voltage supply and the PTL. The state of the output data dictates whether the I/O driver draws current from the PDN or not. In the case of a voltage-mode driver and ground-tied termination, the high state of the output data induces current to flow from the PDN toward the signal transmission line. The current flow results in the dc drop across the source termination of the PTL so that only a fraction of the original supply voltage appears on the power supply node of the I/O driver. On the other hand, the low state of the output data stops the current flow. As a result, the dc drop across the source termination becomes dynamic depending on the state of the output data. This is illustrated in Figure 3.2(b). As the characteristic impedance of the signal transmission line is 50 ohms, the turn-on impedance of the I/O driver is designed to be 25 ohms so as to have the amplitude of the output data equal to one-half of the supply voltage. The dc voltage level at the power supply node (TxPwr) of the I/O driver

alternates between the original supply voltage and a fraction of the original supply voltage, depending on the data state at the output node (data_tx), as shown in Figure 3.2(b).

The dc drop on the PDN during the high state of the output data is different from SSN. It is data state-dependent, while SSN is data transition-dependent. In other words, the dc drop is due to the resistive element, while SSN is mainly due to the inductive element. It is interesting to note that the dc drop does not affect the amplitude of the received data as illustrated in Figure 3.3. When a power plane is used as the I/O PDN, the turn-on impedance of the I/O driver is typically matched to the signal transmission line, which is terminated with the impedance-matching resistor at the far end. Hence, the output voltage swing is one-half of the supply voltage. This impedance matching scheme cannot be applied to the PTL-based I/O PDN because using a PTL requires a source termination. The intervention of the PTL-terminating resistance can be compensated by reducing the turn-on impedance of the I/O driver. When the sum of the PTL-terminating resistance and the turn-on impedance of the I/O driver is matched to the signal transmission line, the received eye height can be maintained to be one-half of the supply voltage.

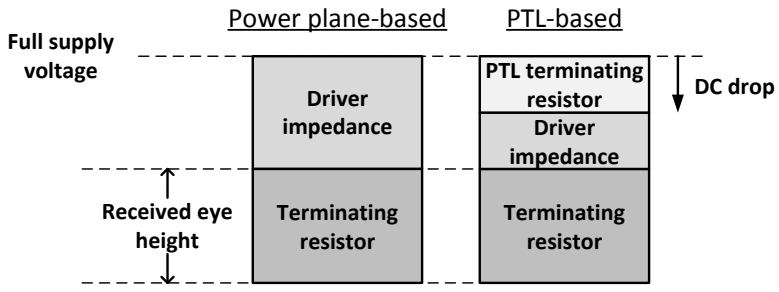


Figure 3.3 Comparison of supply voltage division.

However, the dynamic dc drop shown in Figure 3.2 can create problems if combined with the impedance mismatch in the PTL-based circuit, which comes from manufacturing variations. This can create signal-integrity-related issues, as shown in Figure 3.4. When

the PTL and terminating resistor are mismatched by 20%, as shown in Figure 3.4(a), the PTL is underdriven. Moreover, the balance of impedance between the PTL and the signal network is upset. Depending on the reflection coefficient, multiple reflections go back and forth within the PTL until the steady-state voltage is reached [56]. These multiple reflections induce a staircase-step waveform at the power supply node (TxPwr) of the driver and signal overshoot at the output node (data_tx), as shown in Figure 3.4(a) [56][59].

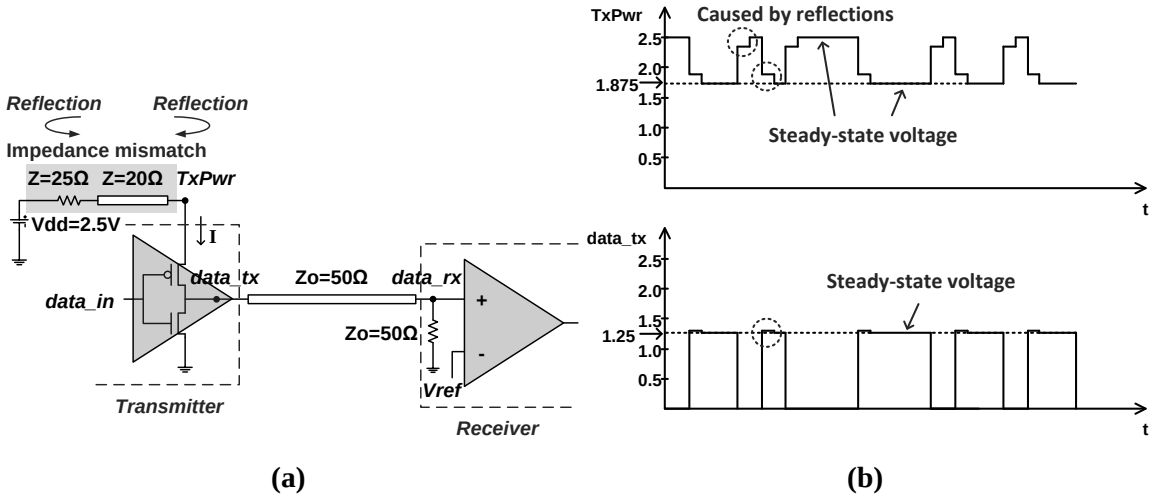


Figure 3.4 Impedance mismatched PTL in single-ended signaling. (a) Schematic. (b) Waveform.

The issue due to the dynamic dc drop becomes even more complicated when a single PTL is used to serve multiple I/O drivers. If one PTL is used to support multiple I/O drivers, the power supply nodes of the drivers need to be tied together, which results in varying current through the PTL based on the data pattern. This affects the dc voltage level at the common power supply node and the amplitude of the transmitted and received signal waveforms. In Figure 3.5, a PTL is used to feed power to two I/O drivers. The power supply node of each driver is connected to the same PTL. Since the output data of the two drivers are independent of each other, there are three possible data patterns in terms of the number of 1s, namely 00, 01/10, and 11. The three possible

combinations result in three different amounts of current through the PTL, which leads to three different dc voltage levels at the TxPwr node, and three different amplitudes of the waveform at the input and output of the signal transmission lines (data1_tx, data2_tx, data1_rx, and data2_rx). Therefore, the PTL-based power distribution scheme needs to be modified to eliminate the data-state-dependent dc drop.

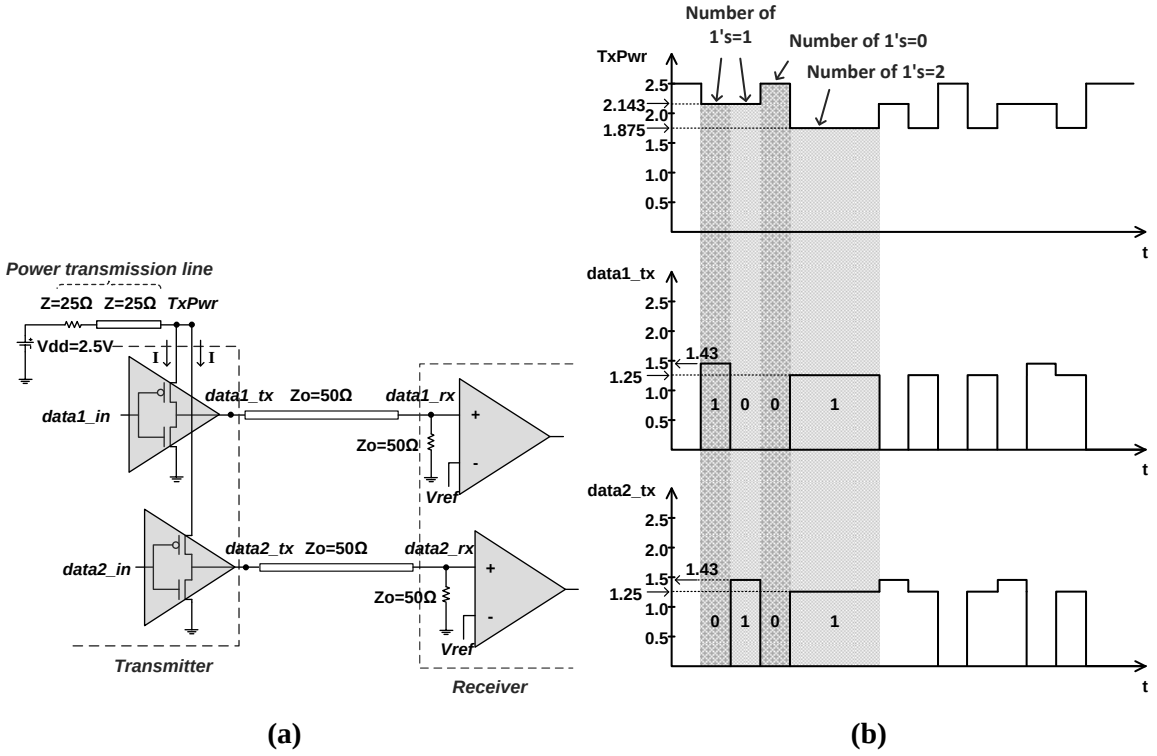


Figure 3.5 Two I/O drivers sharing one PTL. (a) Schematic. (b) Waveform.

Also, an increase in the number of PCB traces should be addressed by devising a method to feed more than one driver with one PTL to relieve the line congestion on the signal layer. Lastly, the power required to transmit 1-bit of data should be optimized for the PTL by using a new signaling scheme and by adjusting the impedance of the signaling circuit.

3.2 Constant Current Power Transmission Line (CCPTL)-Based PDN

The Constant Current PTL (CCPTL) scheme resolves the two issues related to the

PTL, namely dynamic dc drop on the PDN caused by the source termination, and mismatch effect between the PTL and the terminating resistor [55]-[58]. The varying dc drop shown in Figure 3.3 and Figure 3.5 are due to the current flowing through the PTL only during the high state of the output data. To maintain the dc voltage level constant, a current path is required during the low state of the data. In the CCPTL scheme, an additional current path from power to ground is supplemented using a data pattern detector and dummy path, as shown in Figure 3.6(a). The data pattern detector detects the state of the input data. It then determines whether to connect or disconnect the dummy path to the PTL. The dummy path is a resistive path, whose impedance is matched with that of the signal path so as to induce the same amount of current during the low state as during the high state of the data. It can be implemented with transistors whose width and length are optimized to yield the desired resistance. As a result, the dc voltage level at the power supply node (TxPwr) of the driver stays constant regardless of the output data state, as shown in Figure 3.6(b). The dc drop due to the PTL-terminating resistor can be compensated either by reducing the turn-on impedance of the output driver or by increasing the supply voltage. Then, the dc drop at the power supply node (TxPwr) does not reduce the eye height of the transmitted/received signal. Between the two compensation methods, the latter is used during measurements, which will be discussed in a later section.

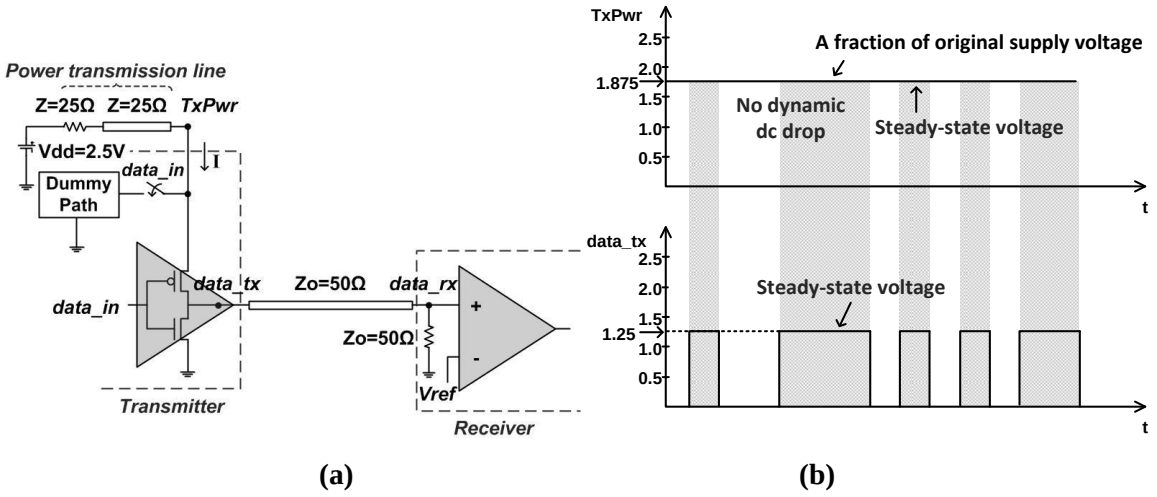
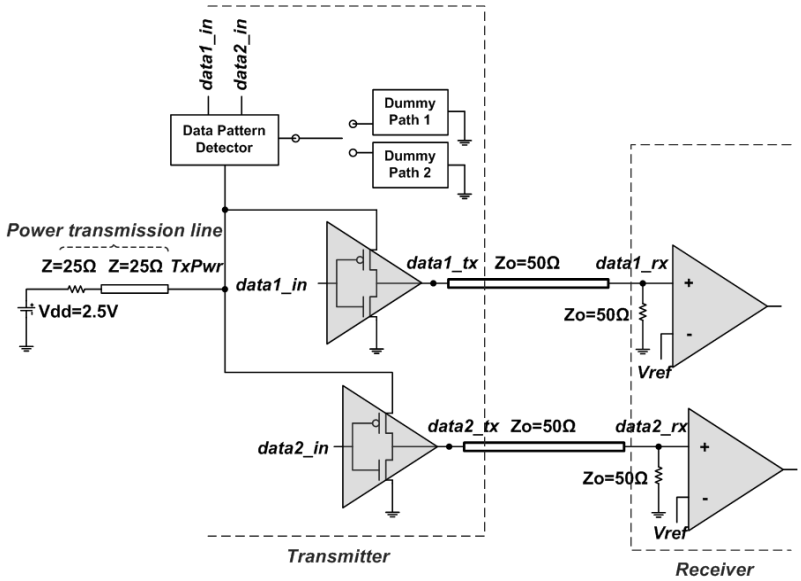


Figure 3.6 Single-ended signaling using CCPTL. (a) Schematic. (b) Waveform.

The constant current through the PTL eliminates the repeated charging and discharging of the PTL. It therefore keeps the PTL always charged so that the PTL behaves as a constant load. As a constant load, the transmission line's response to applied voltage is resistive rather than reactive, despite being comprised purely of inductance and capacitance [60], which excludes the possibility of any impedance mismatch. Consequently, the mismatch effect will not appear on the signal line even when there is an impedance mismatch in the PTL. Even with a 20% impedance mismatch between the PTL and the termination, the dc voltage level at the power supply node (TxPwr) and the amplitude of the signal at the input and output of the signal transmission line (data_tx and data_rx) maintain the steady-state voltages, resulting in the same waveform as in Figure 3.6(b).

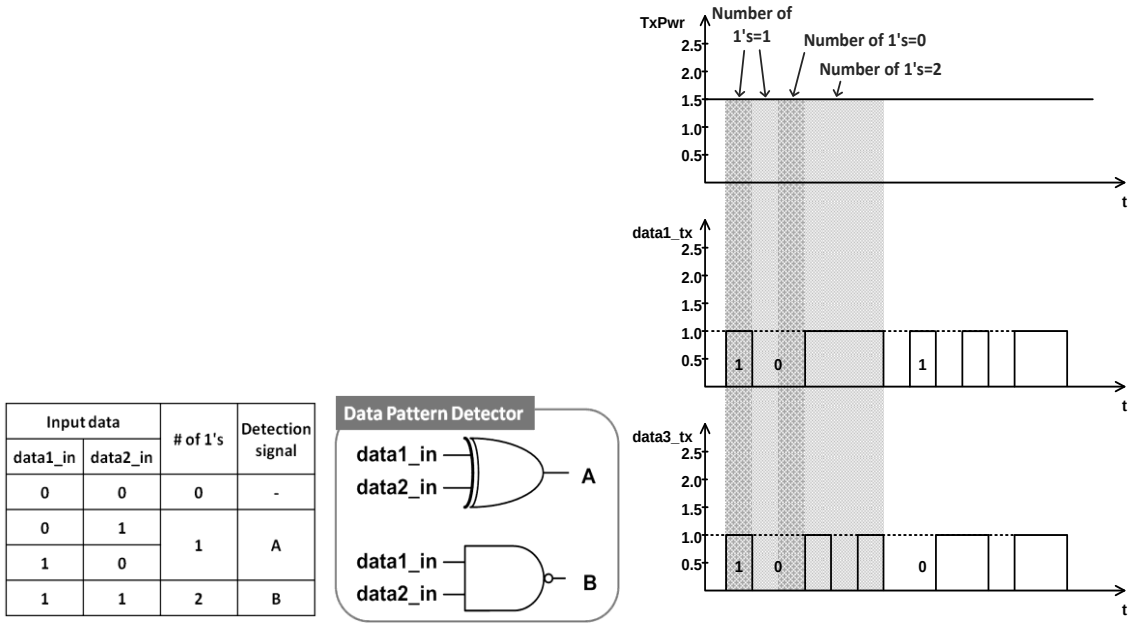
The application of the CCPTL scheme can be extended to support multiple I/O drivers. To feed power to multiple I/O drivers with one CCPTL, a data pattern detector and multiple dummy paths can be used. When the power supply nodes of multiple I/O drivers are tied together, the amount of current through the PTL varies based on the data pattern. Therefore, the number of dummy paths needs to be equal to the number of possible data patterns. Figure 3.7(a) shows the CCPTL scheme used for 2-bit

transmission. Two bits give four different patterns, which are LL, LH, HL, and HH (L stands for the low state, while H for the high state). In terms of the number of high states, three patterns are possible, as indicated in the table in Figure 3.7(b). The maximum PDN current is drawn by the drivers when all the drivers are turned on with all the output data being high, while no current flows when all the drivers are turned off. The data pattern detector detects the number of turned-off drivers and enables the corresponding dummy paths to carry current from the PDN. As a result, the total amount of current drawn from the PDN by either the drivers or the dummy paths will be kept constant regardless of the data pattern. Figure 3.7(c) shows the resulting waveforms; the voltage at the power supply pin (TxPwr node) is constant at 1.5 V, and the amplitudes of the signals at the input and output of the signal line are both 1 V.



(a)

Figure 3.7 Two I/O drivers per CCPTL. (a) Schematic. (b) Data Pattern Detector. (c) Waveform.



(b) **(c)**

Figure 3.7 Continued.

The advantages of the CCPTL signaling scheme include reduction of layer counts and elimination of decoupling capacitors for mitigating RPDs, which lead to lower cost. Also, this scheme provides increased voltage and timing margins that enable the enhancement of the channel data rate. However, potential disadvantages using the presented scheme are increased power consumption and circuit area, which are associated with inducing constant current in the power distribution network. If the PTL is being source-terminated, the dc drop due to the terminating resistance should then be compensated either by reducing the turn-on impedance of the output driver or by increasing the power supply level.

It is important to note that if the same concept is extended to differential signaling, most of these limitations can be resolved because the two complementary signals in differential signaling draw constant current from the PDN by construction. In differential signaling, a natural dummy path is created in the process of transmitting a pair of complementary data bits. However, it doubles the off-chip PCB trace count and the I/O

pin count. The focus of this chapter is on improving signal integrity for single-ended signaling, and therefore includes only the simulation and measurement results of the CCPTL-based single-ended signaling scheme.

3.3 Test Vehicle Design and Modeling

Two test vehicles (TVs) were designed and fabricated to explore the impact of RPDs on signal integrity in the power-plane-based PDN and to demonstrate the efficacy of the PTL-based PDN. Two test boards were custom-designed to incorporate two different PDNs, and an off-the-shelf chip was mounted on each board. A 16-pin QFN-packaged SiGe differential driver was used. For a differential output pin pair, one output pin was connected to a 66-mm long signal transmission line. The signal transmission line was terminated inside the oscilloscope with 50 ohms. The other output pin was directly connected to a 50 ohm resistor to function as a dummy path outside the chip. During the high state of the output data, current flows along the signal transmission line, while during the low state of the output data, the dummy path draws the same amount of current. Therefore, constant current flows through the PDN in both the power-plane-based and PTL-based TVs at all times. Although the power-plane-based PDN does not require a dummy path, the dummy path is still implemented to have all the setup the same between the two TVs except for the PDN. SMA connectors were used to support wide bandwidth for input and output signals.

The top view of the power-plane-based board and the PTL-based board are shown in Figure 3.8. The width and length of the power and ground planes are 96.52 mm and 63.5 mm, respectively. For the PTL-based TV, a 25 ohm transmission line was used as the PTL, and a 25 ohm resistor was used as the source-terminating resistor. The source termination of the PTL is used to reduce the possibility of multiple reflections if the first reflection is initiated by the impedance mismatch between the signal transmission line and load-terminating resistor. The ground plane serves as a reference conductor for the

PTL as well as for the signal transmission line. The only difference between the two TVs is the method used to provide power to the driver.

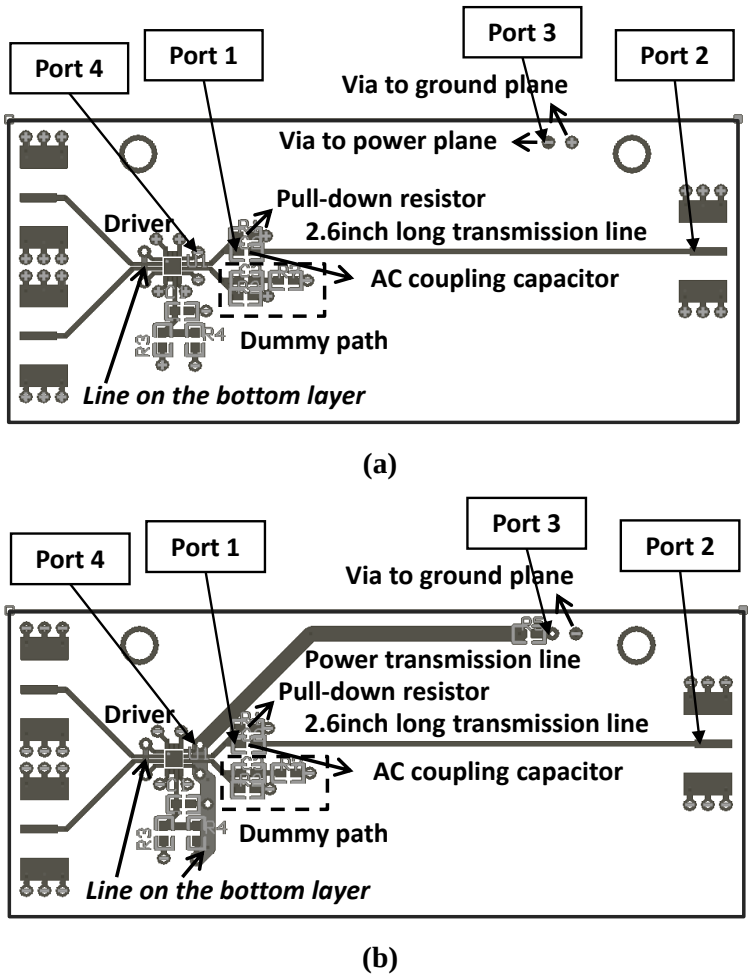


Figure 3.8 Top view of test vehicles. (a) Plane-based test vehicle. (b) PTL-based test vehicle.

The stack-up details of the test boards are shown in Figure 3.9. Copper and FR4 are used for the metal and dielectric layers. The conductivity of copper was assumed to be 5.8×10^{7} S/m. The dielectric constant and loss tangent of FR4 were 4.6 and 0.025, respectively. The power-plane-based board consists of 4 layers, which are signal-power-ground-signal layers. On the other hand, the PTL-based board consists of 3 layers, which are signal/power-ground-signal layers, having both signal and power transmission lines on the top layer. It is important to note that in both boards, the signal transmission line and other connections were placed on the top signal layer, while the bottom signal layer

was nearly empty with only a couple of lines connecting to control and power supply pins. The lines placed on the bottom layer are also shown in Figure 3.8.

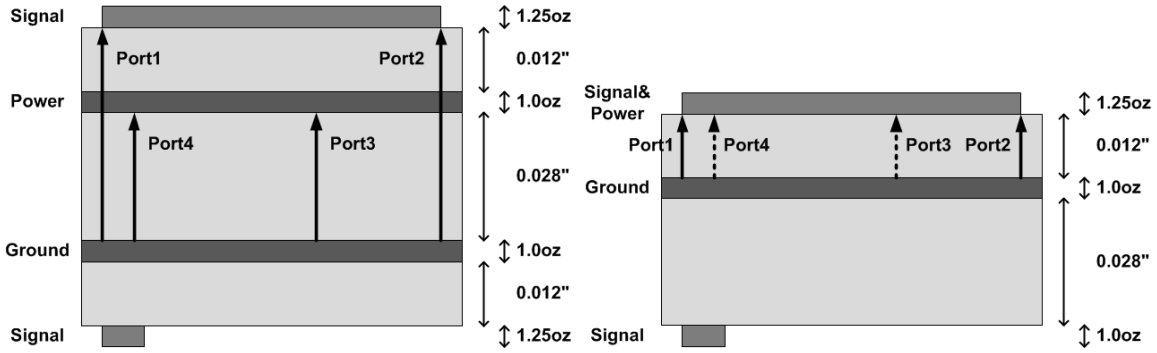


Figure 3.9 Side view of test vehicles. (a) Plane-based test vehicle. (b) PTL-based test vehicle.

In the power-plane-based TV, a cavity is formed between the power and ground planes. The resonant frequency of the structure can be calculated, based on the rectangular waveguide formula defined by:

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \qquad (6)$$

where 'c' is the speed of light, 'a' and 'b' are the width and length of the rectangular structure, 'm' and 'n' are the integers to represent the dominant mode number, and ε_r and μ_r are the relative permittivity and the relative permeability of the substrate [16]. The first half wavelength ($\lambda/2$) resonance of the plane pair occurs at 724.6 MHz. The first four resonant frequencies are summarized in Table 3.1.

Table 3.1 Calculated resonant frequency.

w (mm)	l (mm)	m	n	$f_{\lambda/2}$ (Hz)
96.52	63.5	1	0	7.2459E+08
		0	1	1.1014E+09
		2	0	1.4492E+09
		2	1	1.8202E+09

Sphinx [51], a multi-layer finite difference method (M-FDM) [16] based electromagnetic solver was used to model the two TVs in frequency domain and compare the insertion losses of the signal transmission lines of the two TVs. Here, the insertion loss (IL) is defined as $IL=-20\cdot\log_{10}|S_{21}|$ dB, when Port1 and Port2 are at the input and output of the signal transmission line, using the same reference impedance of 50 ohms. Four ports were defined for each structure, two for the signal line (Port1 and Port2 at input and output) and the other two for the PDN, as shown in Figure 3.8 and Figure 3.9. The reference used for all the ports was the ground plane.

The insertion losses of the signal transmission lines in the two TVs are compared in Figure 3.10. The insertion loss of the PTL-based TV has a smooth negative slope with -2.77 dB insertion loss at 10 GHz. This behavior is expected of a microstrip line with the main contributor to insertion loss being conductor and dielectric loss. On the other hand, the insertion loss of the signal line in the power-plane-based TV has multiple resonances. The first dip in the insertion loss appears at 750 MHz. This frequency corresponds to the $\lambda/2$ resonant frequency of the plane pair. This dip explains why the RPD effect becomes even more severe when the switching frequency of the I/O driver coincides with the cavity resonant frequency of the power/ground plane pair; the waveform suffers from high insertion loss traveling along the signal transmission line. The rest of the dips shown in Figure 3.10 are consistent with the resonant frequencies shown in Table 3.1. The reason that the resonant frequencies of the signal line correspond to the cutoff frequencies of the cavity modes is because those resonances are induced by the coupling between the signal line and the PDN [61]. Therefore, the transmission characteristic of the signal line suffers from non-monotonic variation over frequency, which can create problems for signal integrity. The resonances also cause rapid increase in the insertion loss reaching -6.69 dB at 10 GHz.

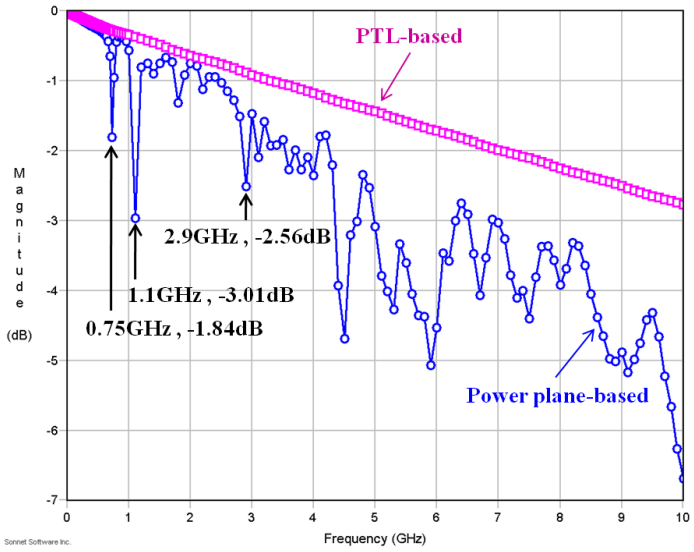
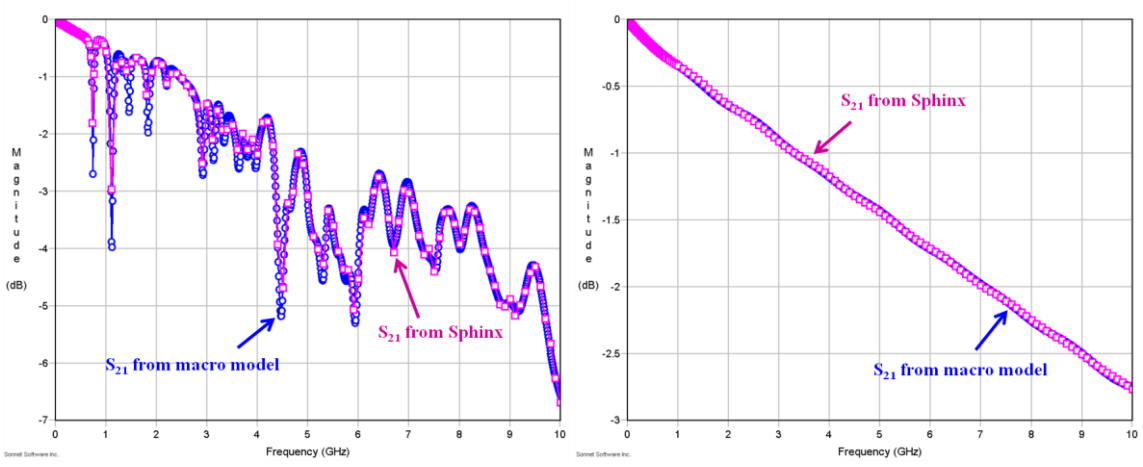


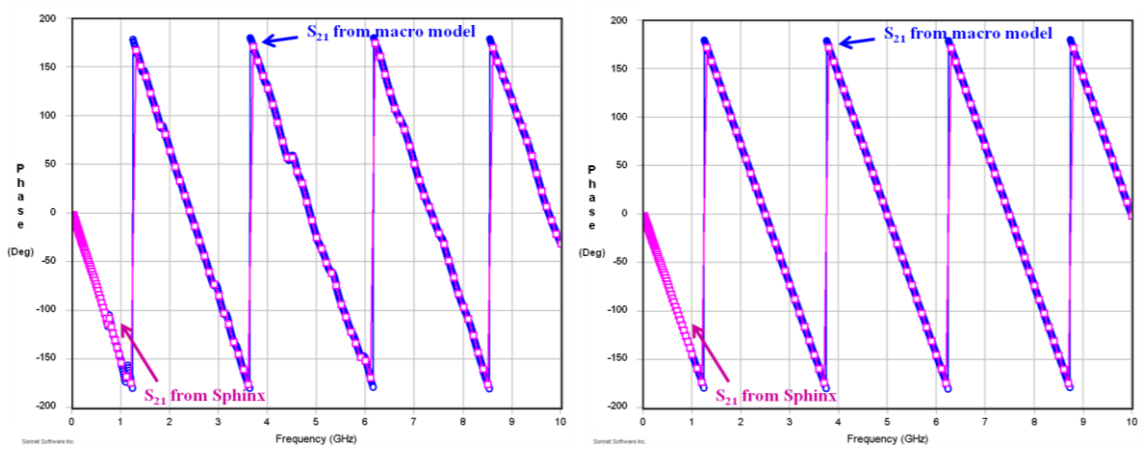
Figure 3.10 Insertion loss of signal transmission line with plane-based PDN and PTL-based PDN.

For time-domain analysis, the frequency samples in the 4×4 scattering matrix of the TV need to be converted into a SPICE (Simulation Program with Integrated Circuit Emphasis)-compatible equivalent circuit. This is important when modeling the coupling between the signal-power network to include the nonlinear effects of the driver/receiver circuitry and their effects on signal and power integrity [16]. A macromodeling tool, IdEM Plus [62], was used to create a macromodel and SPICE netlist from Sphinx's frequency domain response. By using the macromodel, passivity and causality were guaranteed using data certification procedures provided in IdEM Plus, as described in [16]. The frequency response of the macromodel is compared with the original insertion loss data from Sphinx in terms of magnitude in Figure 3.11, which show good agreement for both TVs. As shown in Figure 3.12, good agreement is also observed between the phase data from Sphinx and the macromodel for both TVs. The comparison between the Sphinx data and the macromodel only for the insertion loss is shown in Figure 3.11 and Figure 3.12, although a macromodel for the 4×4 matrix was constructed using IdEM Plus, which includes return loss effects as well.



(a) **(b)**

Figure 3.11 Comparison of magnitude of insertion loss from Sphinx and macromodel. (a) Power-plane-based TV. (b) PTL-based TV.



(a) **(b)**

Figure 3.12 Comparison of phase of insertion loss from Sphinx and macromodel. (a) Power-plane-based TV. (b) PTL-based TV.

The SPICE simulation setup with the macromodel is shown in Figure 3.13. Port1 and Port2 represent the input and output of the signal line, while Port3 and Port4 represent ports on the PDN. A complementary pair of 2^7-1 PRBS (pseudo-random bit stream) data was applied to the differential driver as inputs. One output pin of the driver was connected to Port1 of the macromodel, and the load termination was connected to Port2. The other output pin was connected to a 50 ohm resistor, which functions as the dummy path as described earlier. The dc voltage was supplied to Port3, and the power supply pin

(V_{DD}) of the driver was connected to Port4. CMOS transistors were used to operate as the voltage-mode driver. The IBIS (I/O Buffer Information Specification) model of the device was not used due to its incapability of handling power supply noise [63], and therefore a 0.28 μm CMOS process was used to replicate the behavior of the device. The widths of the transistors were tuned so as to match the output waveform of the CMOS driver with that of the IBIS model as the ideal power and ground was supplied. The simulation setup in Figure 3.13 incorporates the electromagnetic behavior of the test board, the nonlinear characteristic of the I/O driver, and the passive components. The data rate of 1500 Mbps was used to excite the cavity resonance in the plane-based TV.

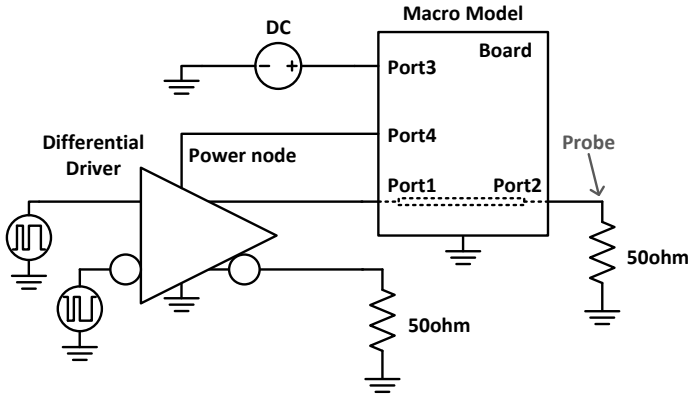


Figure 3.13 SPICE simulation setup using macromodel.

The resulting eye diagrams at the receiver end (Port2) for the two TVs are compared in Figure 3.14. The eye diagram shown in Figure 3.14(a) is when the ideal power and ground supply was applied, which serves as a baseline. The eye diagram shown in Figure 3.14(b) is the result when the power/ground plane pair is used as the I/O PDN. The voltage and timing margin has been reduced due to power supply noise. The eye height and width are 353 mV and 626 psec, respectively. Figure 3.14(c) shows the eye diagram of the received data when the PTL is used as the power supply path. The eye height and width are 488 mV and 640 psec, respectively. As compared to Figure 3.14(b), the eye height is increased by only 38% and the peak-to-peak (p-p) jitter is reduced by 34% by using PTL. The simulation setup did not include the package model of the chip and the

discontinuities due to SMA connectors, cables, and oscilloscope. Therefore, the measurement results can be worse than the simulation results in terms of voltage and timing margin. However, the simulation does show a trend and indicates the advantage of using a PTL for power distribution.

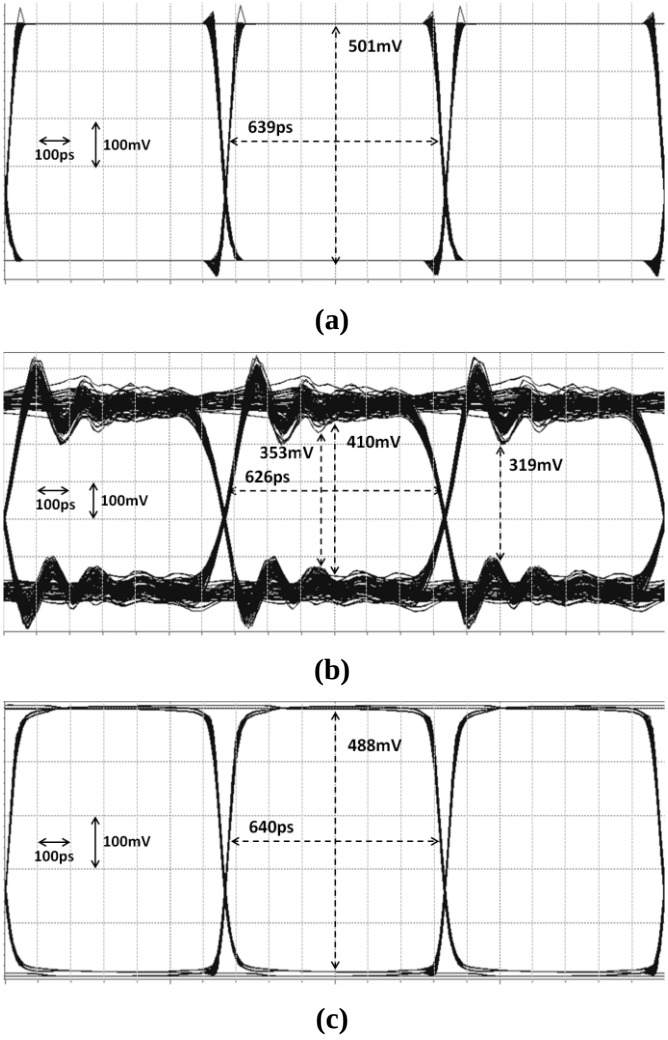


Figure 3.14 Simulated eye diagrams of the received 1500Mbps PRBS. (a) Ideal power supply. (b) Plane-based TV. (c) PTL-based TV.

The TV with an ac coupling capacitor added between the output of the driver and the signal transmission line was simulated as well. The ac coupling capacitor is generally used to suppress the dc current flow and to provide a bias for the oscilloscope. The SPICE simulation setup with the ac coupling capacitor is shown in Figure 3.15. One

output pin of the driver was connected to Port1 of the macromodel through a 0.1 μF capacitor. The other output pin was connected to a 0.1 μF capacitor and 50 ohm resistor in series to function as a dummy path outside the chip. The rest of the setup was kept identical to Figure 3.13.

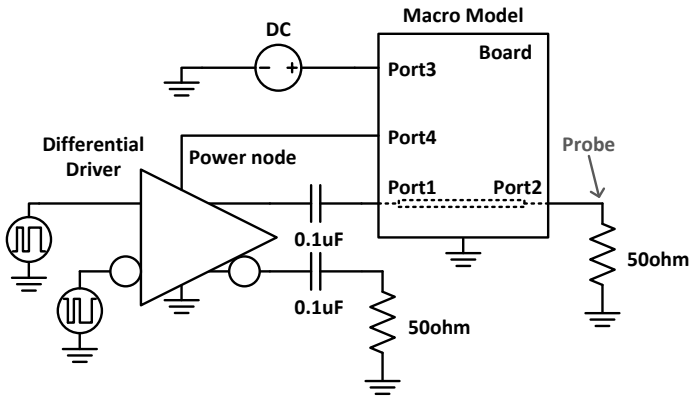
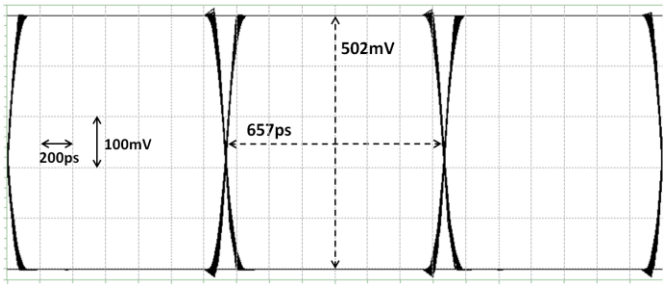
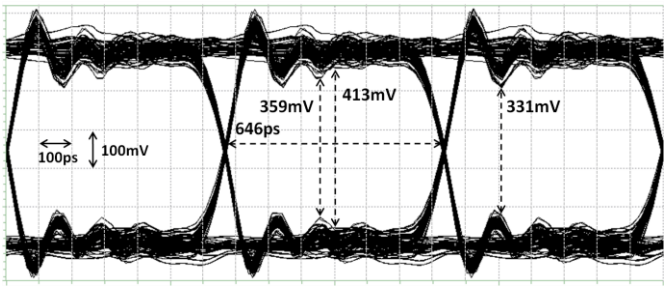


Figure 3.15 SPICE simulation setup with ac coupling capacitors.

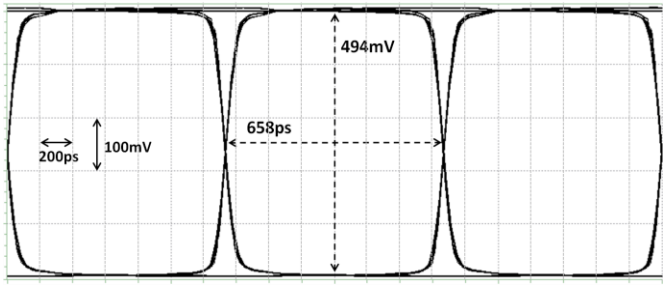
The resulting eye diagrams at the receiver end (Port2) are compared in Figure 3.16. The eye diagram shown in Figure 3.16(a) is the result when the ideal power and ground supply was applied, which serves as a baseline. Figure 3.16(b) and (c) are the eye diagrams of the received output data in the power-plane-based and PTL-based TVs, respectively. With the inclusion of the ac coupling capacitor, the transition crossing point has become closer to 50% of the eye height, which improves the eye width. In Figure 3.16(b), the eye height and width of the power-plane-based TV are 359 mV and 646 psec, respectively. By replacing the power plane with a PTL, the eye height and width become 494 mV and 658 psec, respectively, as shown in Figure 3.16(c). The eye height is improved by 38% and the p-p jitter is reduced by 57%, as compared to Figure 3.16(b).



(a)



(b)



(c)

Figure 3.16 Simulated eye diagrams of the received 1500Mbps PRBS with ac coupling capacitors added. (a) Ideal power supply. (b) Plane-based TV. (c) PTL-based TV.

The PTL-based PDN outperforms the power-plane-based PDN in terms of voltage and timing margins with and without the ac coupling capacitor between the output of the driver and the signal transmission line. The performance improvement is mainly coming from the removal of RPDs by using the PTL. Since the dummy path is replicating the signal network during the low state of the output data, the sum of ac and dc current is maintained the same regardless of the inclusion of ac coupling capacitors in both the TVs. As a result, the ac coupling capacitor does not disturb the function of the CCPTL signaling scheme.

3.4 Measurements and Correlation

Figure 3.17 shows the test environment and measurement set-up along with the port locations from Figure 3.8. Agilent 81133A was used to generate a 2^7-1 PRBS pattern at the desired frequency. A supply voltage of 2.5 V was used for the power-plane-based TV, while 3.98 V was used for the PTL-based TV. Due to the source termination of the PTL, a dc drop occurs across the resistor. Since it causes the device to be supplied with less voltage than the original supply voltage, the dc drop should be compensated either by reducing the turn-on impedance of the output driver or by increasing the supply voltage to maintain the same voltage level at the device and the receiver side as in the power-plane-based TV. The limitation of the off-the-shelf chip precluded the former method so that the latter method was used.

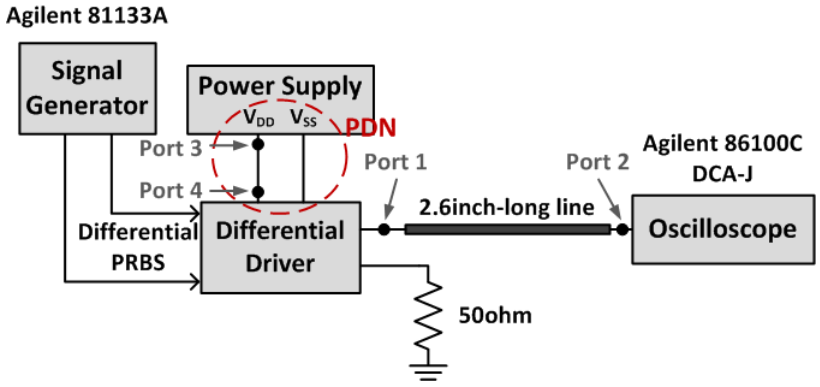
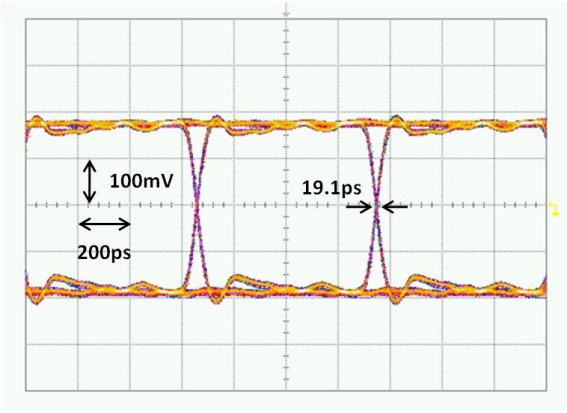


Figure 3.17 Test environment.

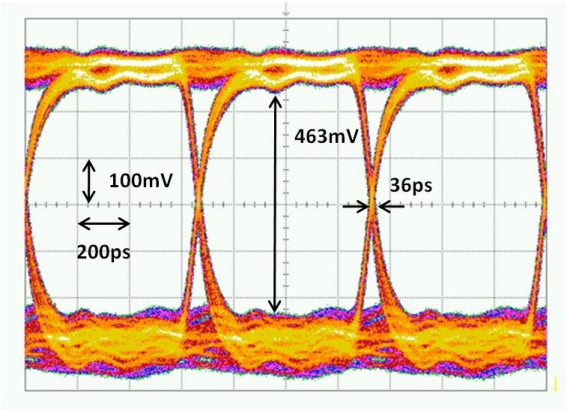
The drivers of both TVs were excited with a 1500 Mbps differential PRBS pattern. The fundamental frequency of the 1500 Mbps PRBS pattern coincided with the resonant frequency of the signal line in the plane-based TV. Eye diagrams were measured at the output of the transmission line (Port2) after the signal traveled a distance of 66 mm along the transmission line, using Agilent 86100C DCA-J oscilloscope. To maintain consistency, 10k samples were used to construct the eye diagram. Two types of jitters were measured using the oscilloscope, namely the root mean square (RMS) jitter and the peak-to-peak (p-p) jitter. The RMS jitter utilizes all the 10k samples for calculation.

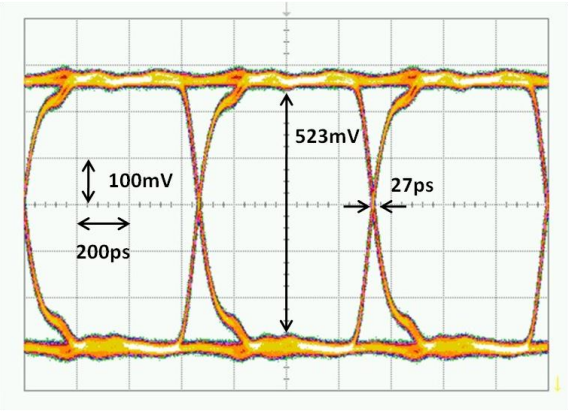
Assuming that the mean is 0, the RMS jitter quantifies the standard deviation of the jitter distribution. This number is more meaningful compared to the p-p jitter which is the distance between the two farthest data points. However, since the jitter is mainly caused by power supply noise, its distribution can be non-Gaussian. In such a case, the p-p jitter is more useful. Hence, both jitters are presented.

Figure 3.18 shows the eye diagram of a 1500 Mbps PRBS at the receiver side in each TV. Figure 3.18(a) is the eye diagram of the signal generator output, and Figure 3.18(b) and Figure 3.18(c) are the eye diagrams at the receiver side in the power-plane-based and PTL-based TVs, respectively.



(a)





(b) **(c)**

Figure 3.18 Measured eye diagrams of the received 1500Mbps PRBS. (a) Signal generator. (b) Power-plane-based TV. (c) PTL-based TV.

The output of the signal generator has an initial p-p jitter of 19.1 psec. The p-p jitter increases to 36 psec in the power-plane-based TV, while it increases to 27 psec in the PTL-based TV. The difference between the p-p jitters in the two TVs is 9 psec, which is a reduction of 25% for the PTL-based TV. The eye height is ~463 mV in the power-plane-based TV, and ~523 mV in the PTL-based TV, which shows an improvement of 13.0%.

In Table 3.2, the measured eye diagrams at 1500 Mbps are compared to the simulation results in terms of voltage and timing window. Good agreement is observed for the eye height between the measurement and simulation results. The measured eye heights are 11.4% and 6.7% larger than the simulated eye heights in the power-plane-based and PTL-based TVs, respectively. This discrepancy can be attributed to manufacturing variation of the stack-up dimensions and the material properties. As the thickness and dielectric constant between the power and ground planes have an influence on the power supply noise, the variation can generate unexpected positive or negative deviation. The p-p jitter from simulation is greater than the p-p jitter from measurement by 4.67 psec in the plane-based TV. In the PTL-based TV, the simulated p-p jitter and the measured jitter are different by less than 1 psec. The simulation results have provided almost the same or larger p-p jitter as compared to the measurement results. The reason for this is due to the discrepancy between the actual device used in the measurement and the driver model used in the simulation. The IBIS model of the device could not be used due to its inability to incorporate power supply noise [63], and therefore the impact of the power supply noise on the signal quality could not be simulated using the IBIS model. Therefore, the device was substituted with a CMOS inverter, which was tuned to generate the same output waveform as the device's IBIS model when ideal power and ground were used. As a result, discrepancies occur between the model and measurements as the supply voltage fluctuates at the power and ground terminals of the driver. In the simulation, the duty cycle of the resulting waveform was less than 50%, which led to the increased p-p jitter. However, the simulation results capture the improvement in eye opening and signal

integrity by using the PTL scheme, similar to the measurement results.

Table 3.2 Comparison of eye opening from simulation and measurement.

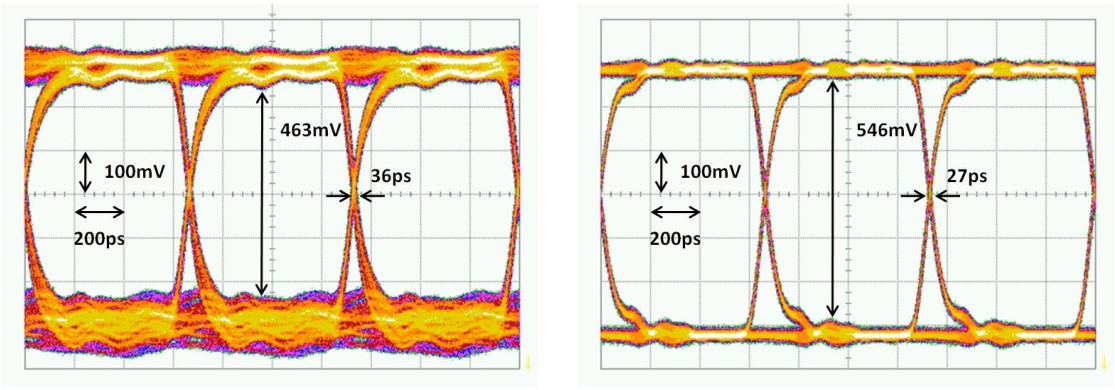
1500Mbps PRBS	Eye height (mV)		P-P Jitter (ps)	
	Simulation	Measurement	Simulation	Measurement
Power Plane	410	463	40.67	36
PTL	488	523	26.67	27

When 3.98 V was used as the supply voltage for the PTL-based TV, the dc voltage level at the power supply pin of the chip equaled 2.498 V, which matches the supply voltage provided to the device in the power-plane-based TV. The increased voltage level for the PTL-based TV raises the power consumption as compared to the plane-based TV. As 3.98 V is 59.2% larger than 2.5 V, the power consumption is 59.2% higher. Here, the amount of current drawn from the PDN is the same in both TVs so as to result in the same eye height at the load end in idealistic situations. Thus, the additional power consumption comes from the increase in the power supply voltage level.

The power consumption issue can be resolved by reducing the turn-on impedance of the I/O driver by custom-designing the CCPTL scheme, or by eliminating the source termination of the PTL. Unless the turn-on impedance of the I/O driver is reduced, the source termination of the PTL requires the increase in the supply voltage level to get the same current level through the signal network as that in the plane-based TV, which leads to the increased power consumption. Since the source termination of the PTL is used to prevent multiple reflections as mentioned in the previous section, it can be removed if the load-terminating resistor is matched well to the characteristic impedance of the signal transmission line.

In Figure 3.19, the received eye diagram of the PTL-based TV without the source termination is compared to that of the power-plane-based TV. Without the source-terminating resistor, no compensation for the dc drop across the PTL is required so that

2.5 V is used as the supply voltage in the PTL-based TV as well as in the plane-based TV. Thus, the same amount of power is consumed in both TVs. The difference between the p-p jitters in the two TVs is 9 psec, which is a reduction of 25% for the PTL-based TV. The eye height is ~463 mV in the power-plane-based TV, and ~546 mV in the PTL-based TV, which shows an improvement of 17.9%.



(a) **(b)**

Figure 3.19 Measured eye diagrams of the received 1500Mbps PRBS. (a) Power-plane-based TV. (b) PTL-based TV without source termination.

As compared to Figure 3.18, the eye height of the PTL-based TV is increased after removing the source termination from 523 mV to 546 mV. This is because the impedance mismatch between the signal transmission line and load-terminating resistor was negligible, thereby minimizing reflections. Also, even though constant current is being drawn from the PDN, current fluctuations are inevitable during data transition. The dc drop over the source-terminating resistor then fluctuates, thereby inducing noise on the power rail. As a result, the PTL without the source-termination has better power integrity, increasing the eye height by 4.4%. However, even with the source-termination, the fluctuation of the power rail is still far less than the SSN-induced supply noise in the plane-based TV. It is important to note that the source termination is instrumental in preventing multiple reflections and ensuring signal integrity due to manufacturing variations, which can cause impedance mismatch at the load.

To reduce the increment in the power supply voltage level when using the source termination, an ac coupling capacitor of 0.1 μF was added between the output of the driver and the signal transmission line, as shown in Figure 3.20. Using an ac coupling capacitor also provides a bias for the oscilloscope without giving a separate dc offset. A 0.1 μF capacitor was also added to the dummy path to replicate the signal network. As a result, the dc current flow was suppressed and the signals became dc-balanced. The required supply voltage level for the PTL-based TV was reduced from 3.98 V to 3.47 V after the inclusion of the ac coupling capacitor. As 3.47 V is 38.8% larger than 2.5 V, the power consumption is also 38.8% higher.

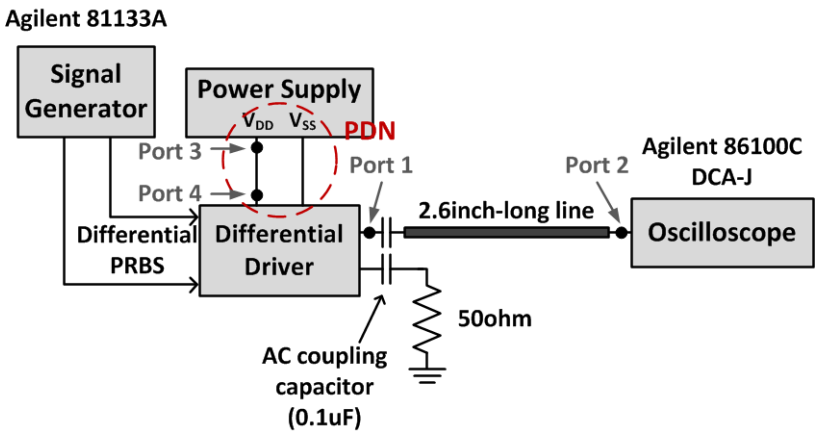
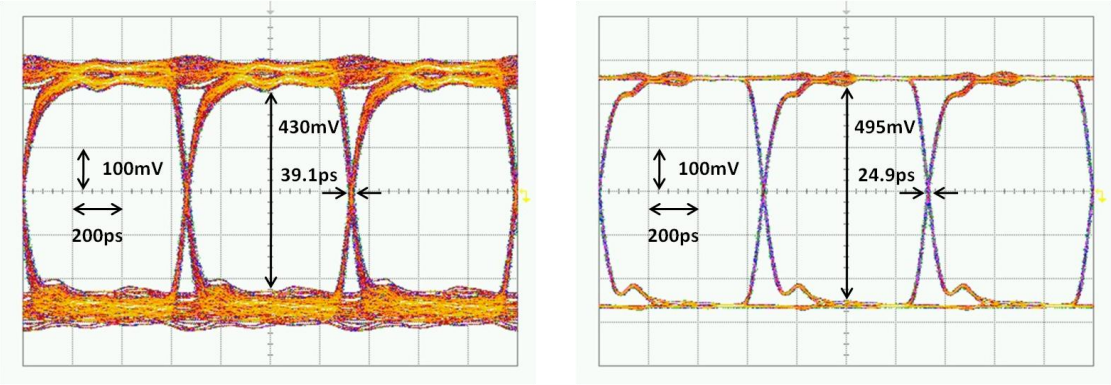


Figure 3.20 Test environment with ac coupling capacitors.

Figure 3.21 shows the eye diagrams at the receiver side when ac coupling capacitors were added to the signal path and the dummy path in both TVs. Figure 3.21(a) and (b) are the eye diagrams of the received 1500 Mbps PRBS in the power-plane-based and PTL-based TVs, respectively. The output of the signal generator has an initial p-p jitter of 19.1 psec, as shown in Figure 3.18(a). The p-p jitter increases to 39.1 psec in the power-plane-based TV, while it increases to 24.9 psec in the PTL-based TV. The difference between the p-p jitters in the two TVs is 14.2 psec, which is a reduction of ~36.3% for the PTL-based TV. The eye height is ~430 mV in the power-plane-based TV, and ~495 mV in the PTL-based TV, which shows an improvement of 15.1%.



(a) **(b)**

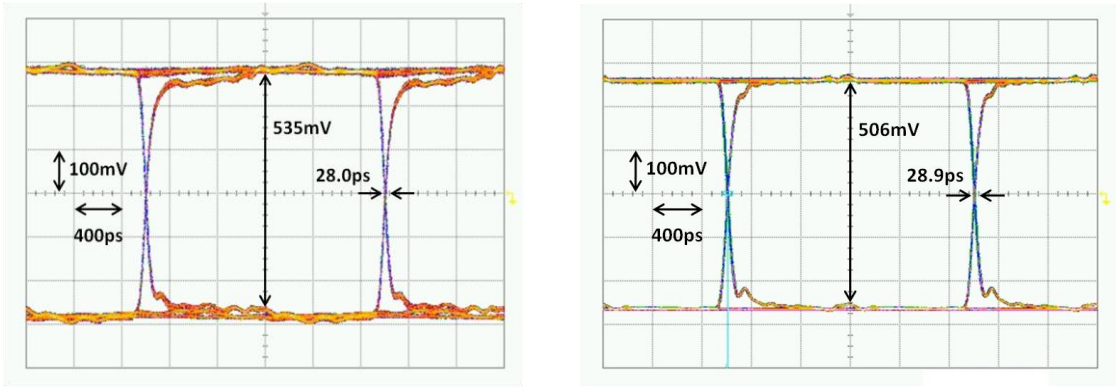
Figure 3.21 Measured eye diagrams of the received 1500Mbps PRBS with ac coupling capacitors. (a) Power-plane-based TV. (b) PTL-based TV.

In Table 3.3, the measured eye openings at 1500 Mbps are compared to the simulation results. Good agreement is observed for the eye height between the measurement and simulation results. The small discrepancy between the measured and simulated eye heights can be attributed to the manufacturing variations in the material properties and the physical dimensions, and the difference in the number of samples used to construct the eye diagrams. In terms of p-p jitter, since the PRBS patterns used in the simulations do not include source jitter, the simulated jitters cannot be directly compared to the measured jitters. Here, a rough estimation can be made by adding the signal generator jitter of 19.1 psec to the simulated jitters. For the power-plane-based TV, the estimated jitter is the sum of 19.1 psec and 20.67 psec, which is 39.77 psec. This jitter value closely matches the measured jitter with an error of 1.7%. For the CCPTL-based TV, the estimated jitter is 27.77 psec, which approximates the measured jitter of 24.9 psec with an error of 11.5%. Although it is not completely accurate to add the two p-p jitters, which are composed of deterministic jitter and random jitter, arithmetically, it gives a rough estimation. To sum up, the simulation results reasonably capture the improvement in performance by using the CCPTL scheme, which is verified by the measured eye diagrams.

Table 3.3 Comparison of eye opening from simulation and measurement with AC coupling capacitors.

1500Mbps PRBS	Eye height (mV)		P-P Jitter (ps)	
	Simulation	Measurement	Simulation	Measurement
Power Plane	413	430	20.67	39.1
PTL	494	495	8.67	24.9

To explore the impact of power supply noise on signal integrity under different data rates, the input data rate was swept from 500 Mbps to 3200 Mbps in steps of 500 Mbps for the PTL-based TV, and in steps of 100 Mbps for the plane-based TV. From 1300 Mbps to 1600 Mbps, a data rate step of 20 Mbps was used to examine the jitter variation around the first resonant frequency of the plane-based TV closely. Starting from 500 Mbps at which the plane-based PDN does not resonate, the eye openings at the receiver sides in both TVs are almost the same, as shown in Figure 3.22. The eye height of the plane-based TV is larger by 5.4% as compared to that of the PTL-based TV. The p-p jitters of the two TVs are different by only 0.9 psec.

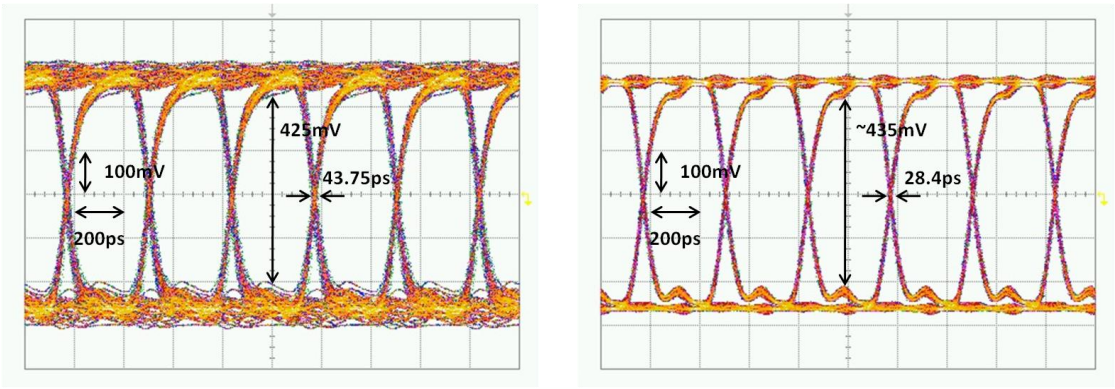


(a) **(b)**

Figure 3.22 Measured eye diagrams of the received 500Mbps PRBS with ac coupling capacitors. (a) Power-plane-based TV. (b) PTL-based TV.

The highest p-p jitter appeared at 3000 Mbps, as shown in Figure 3.23. The eye height is ~425 mV in the power-plane-based TV, and ~435 mV in the PTL-based TV,

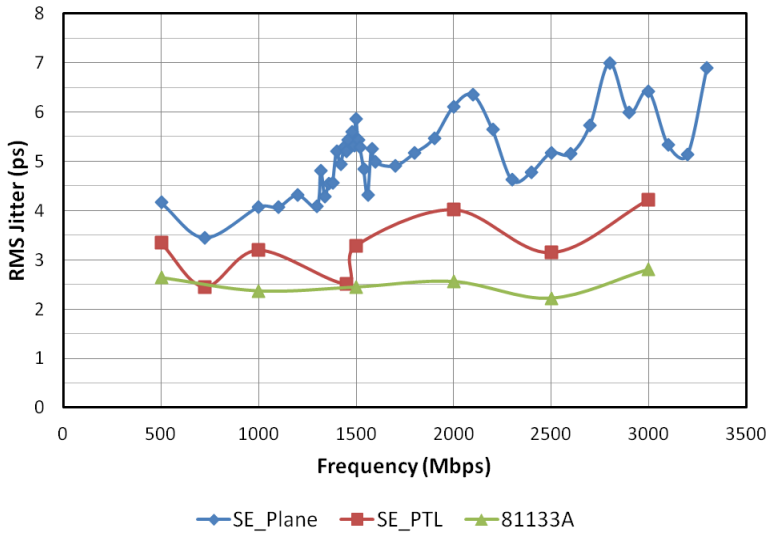
which is an improvement of ~2.4%. The p-p jitter is 43.75 psec and 28.4 psec in the power-plane- and PTL-based TVs, respectively, which is a reduction of ~35%.



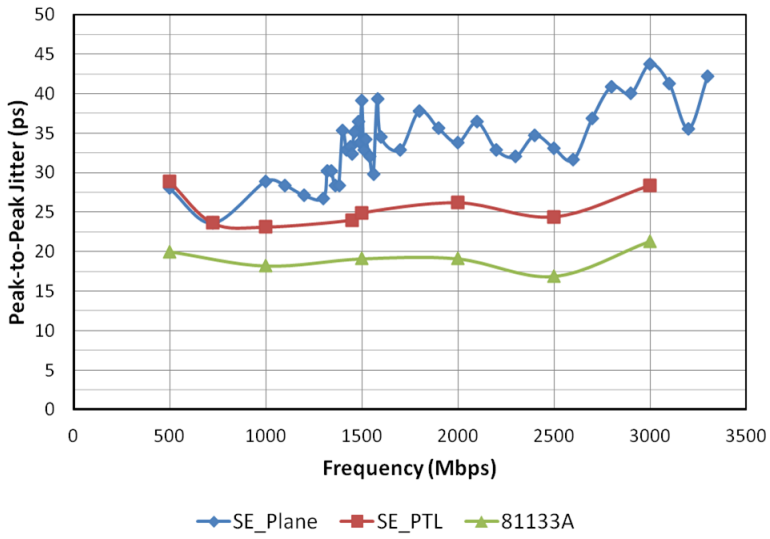
(a) **(b)**

Figure 3.23 Measured eye diagrams of the received 3000Mbps PRBS with ac coupling capacitors. (a) Power-plane-based TV. (b) PTL-based TV.

The RMS and p-p jitters at various data rates are shown in Figure 3.24(a) and (b), respectively. The jitter is plotted along the y-axis, while the data rate is plotted along the x-axis, which bands from 500 Mbps to 3000 Mbps. The line with triangular marker connects the varying jitters of the direct output of the signal generator (Agilent 81133A). The line with rectangular marker (SE_PTL) and the line with circular marker (SE_Plane) indicate the jitters of the PTL-based and plane-based TVs, respectively. Both RMS and p-p jitters of the PTL-based TV have relatively monotonic behavior, whereas those of the plane-based TV have non-monotonic behavior, similar to the insertion loss of the signal line in the plane-based TV.



(a)



(b)

Figure 3.24 Jitter variation over frequency. (a) RMS jitter. (b) Peak-to-peak jitter.

The fundamental frequencies (one-half of the data rate) at which the jitter peaks coincide with the calculated resonant frequencies shown in Table 3.1. The first local maximum jitter appears at 1500 Mbps, which concurs with the first resonant frequency predicted from the frequency-domain modeling. The RMS and p-p jitter at 500 Mbps, 1449 Mbps, 1500 Mbps, and 3000 Mbps are summarized in Table 3.4. The measurement results show that the PTL is effective in increasing the timing margin.

Table 3.4 Summary of measured jitters with ac coupling capacitors.

Data rate (Mbps)	RMS jitter (ps)			Peak-to-peak jitter (ps)		
	Plane	PTL	Reduction	Plane	PTL	Reduction
500	4.17	3.35	-	28	28.9	-
1449	5.20	2.52	51.5%	32.4	24.0	25.9%
1500	5.85	3.28	43.9%	39.1	24.9	36.3%
3000	6.43	4.22	34.4%	43.75	28.4	35.1%

3.4.1 Line Resonance of the PTL

The PTL in the PTL-based TV has its first resonance when the length of the line becomes one-quarter of the wavelength at any frequency, which is the fundamental frequency of that line. Since the two loads at each end of the PTL are different, quarter-wave resonance will occur rather than half-wave resonance. Thus, the resonant points exist at every odd harmonics of the fundamental frequency. Equation (7) can be used to calculate the line resonant frequency of a microstrip line, at which the electrical wavelength becomes 4 times as long as the line length:

$$f_{res} = \frac{c}{\sqrt{\varepsilon_{eff}}} \cdot \frac{1}{4 \times \ell} \tag{7}$$

where c equals the speed of light, ε_{eff} is the effective relative dielectric constant, and ℓ is the length of the transmission line. The length of the PTL is 39.14 mm. This length becomes one-quarter-wavelength long at 985.5 MHz. Therefore, quarter wavelength ($\lambda/4$) resonance occurs at 1.97 Gbps, which leads to a standing wave on the PTL. A minima for the standing wave will appear at one end of the PTL, while the maxima for the standing wave will occur at the other end. In Figure 3.25, the p-p jitter is more closely examined for the PTL-based TV; additional measurements were made between 1500 Mbps and 2500 Mbps based on the calculation of line resonance frequency. Both the TVs with and without the source-termination of the PTL have their local maximum values of p-p jitter

at 2.1 Gbps, which might be coming from the line resonance. Nevertheless, the degradation of p-p jitter due to the PTL resonance is less than that of the power plane. The PTL-based TV still outperforms the plane-based TV in terms of p-p jitter with and without the source termination: the difference of p-p jitter at 2.1 Gbps is 7.6 psec.

Figure 3.25 also includes the jitter frequency spectrum of the power-plane-based TV with a ground plane on top. If the stack-up order in the power-plane-based TV is reversed so that the signal lines are referenced to the ground plane, the structure does not have the RPD effect when a ground-tied load termination is used for the signal transmission line. The performance in terms of signal integrity is therefore similar to the PTL-based TV.

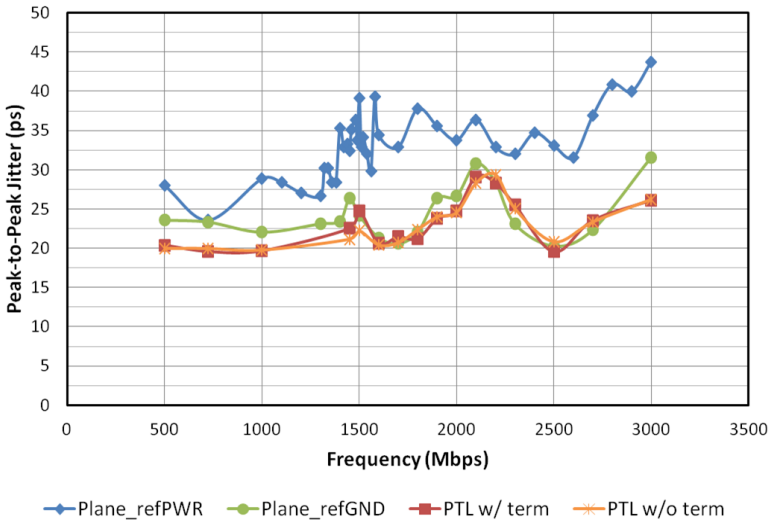


Figure 3.25 Peak-to-peak jitter variation for study of line-resonance.

3.5 Measurement Results with Custom-Designed Transmitter

A test chip was custom-designed and fabricated using a 0.18 μm CMOS process to verify the CCPTL scheme. All pads of the chip were directly connected to the test board by wire bonding, which is also called chip-on-board (COB) assembly. The test board was designed to compare the performance of the CCPTL-based and the plane-based PDNs. For the power-plane-based TV, a pair of 140 mm by 93 mm planes with 0.7 mm FR4

dielectrics was used for power and ground planes. For the PTL-based TV, a 25 ohm signal transmission line was used for PTL along with a source termination of 25 ohm.

Figure 3.26(a) shows the block diagrams of the transmitter A PRBS generator is used to generate 4-bit PRBS pattern with a clock input of the desired frequency. Among 4 bits, a 1-bit data passes through the pre-driver to drive the output buffer, which has relatively large size to be driven by the PRBS generator directly. In the CCPTL-based scheme, the grey-boxed circuitry is added to induce constant current. The 1-bit data is supplied to "control signal generator", which detects the input data pattern and generates the control signals for dummy paths. In 1-bit case, an inverter is used to switch on and off the dummy path. The inverted 1-bit is supplied to the dummy path through the pre-driver as well so as to induce the same amount of current during the off-state of the buffer.

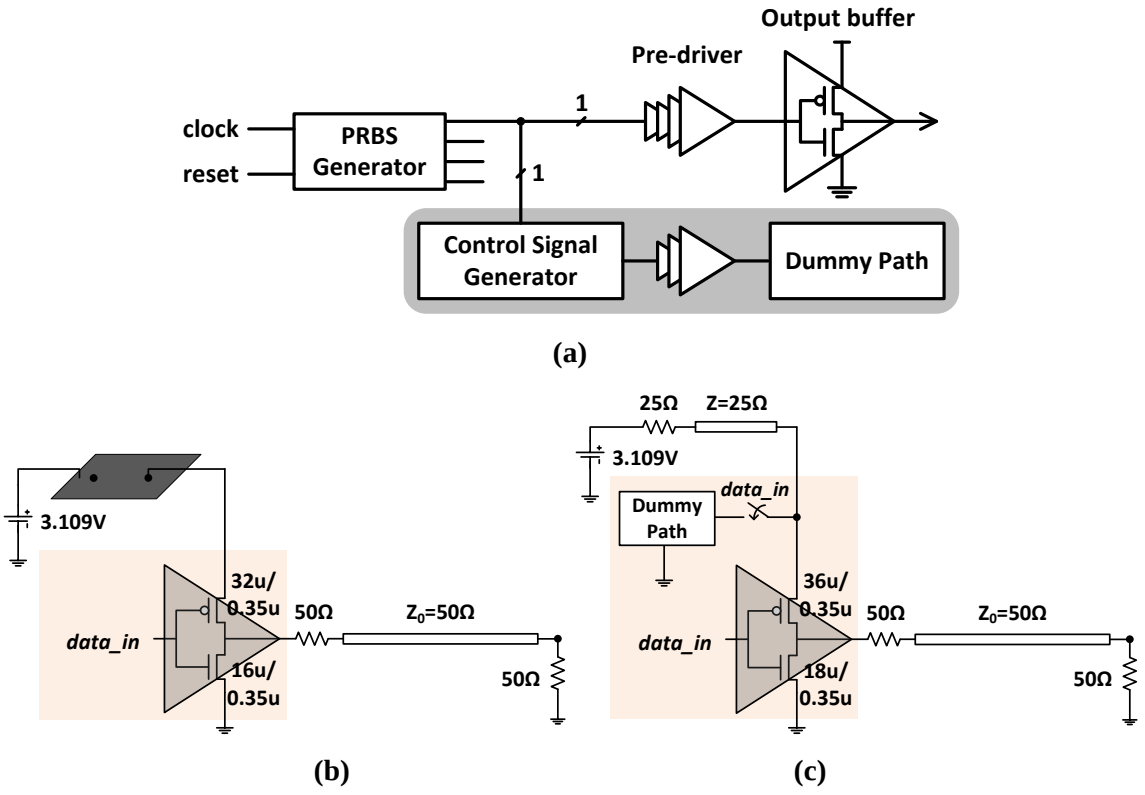
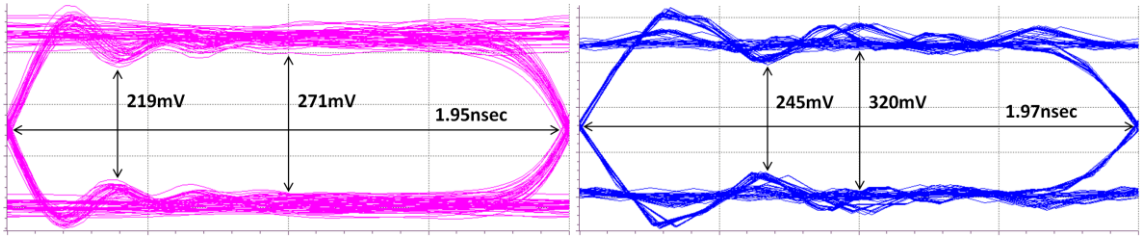


Figure 3.26 (a) Block diagram for 1bit transmission. (b) Output buffer for plane-based TV. (c) Output buffer for PTL-based TV.

Figure 3.26 (b) and (c) show the voltage-mode drivers for the power-plane-based approach and the CCPTL-based approach respectively. The size of the buffer using the PTL-based PDN is slightly larger for less impedance. This is to compensate for the increased impedance in the power supply path due to the source termination of the PTL. As a result, there is no need to increase the supply voltage level for the CCPTL-based TV. Using the same supply voltage, the same eye height can be achieved at the output of the signal transmission line as the power-plane-based TV. The output buffer drives a 50 ohm transmission line through a 50ohm series termination. The transmission line is parallel-terminated at the load by 50 ohms.

Before the measurement, the SPICE simulation of the designed output buffer is performed using a macromodel of the test board. The resulting eye diagrams of a 500 Mbps PRBS waveform at the output of the 203 mm-long signal transmission line are compared in Figure 3.27. Figure 3.27(a) shows the eye diagram of the power-plane-based scheme, which has an eye height of 219 mV and an eye width of 1.95 nsec. The eye diagram of the power-plane-based scheme also has a ringing effect, but the noisy power rail continues throughout the time period. In Figure 3.27(b), the eye diagram of the CCPTL-based scheme has an eye height of 245 mV and an eye width of 1.97 nsec. It has a ringing effect after each data transition, which is damped to reach the steady state. The eye height is improved by 12% and the p-p jitter is reduced by 40% by using the CCPTL scheme.



(a) **(b)**

Figure 3.27 SPICE-simulated eye diagrams. (a) Power-plane-based. (b) CCPTL-based.

The test environment is shown in Figure 3.28. An Agilent 81133A was used to generate a clock at the desired frequency. A supply voltage of 3.11 V and 1.8 V was used for the I/Os and core circuits, respectively. Here, the transmitter of the CCPTL scheme was designed to allow for the voltage drop across the source termination so that the same supply voltage was used to obtain the same signal amplitude as the power-plane-based scheme. The channel length is 84 mm long for traveling signal to be influenced sufficiently by the performance of the PDN.

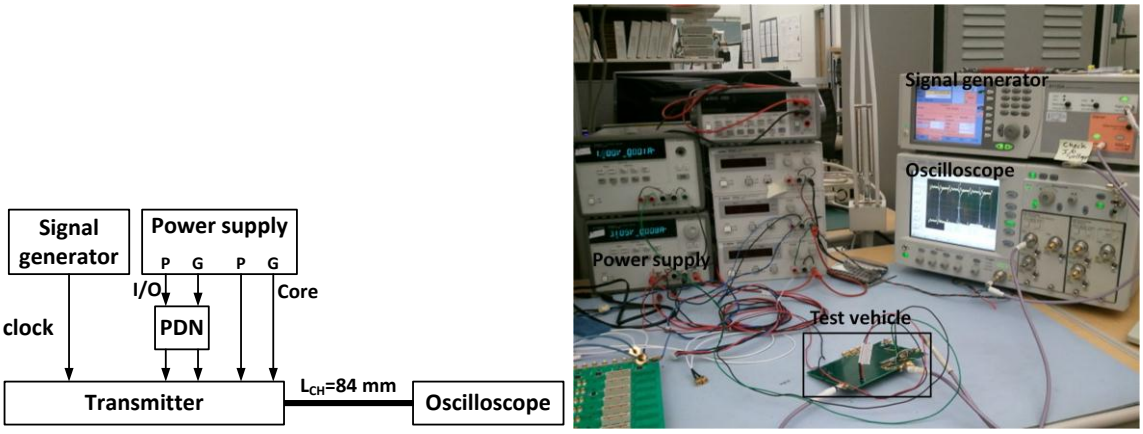
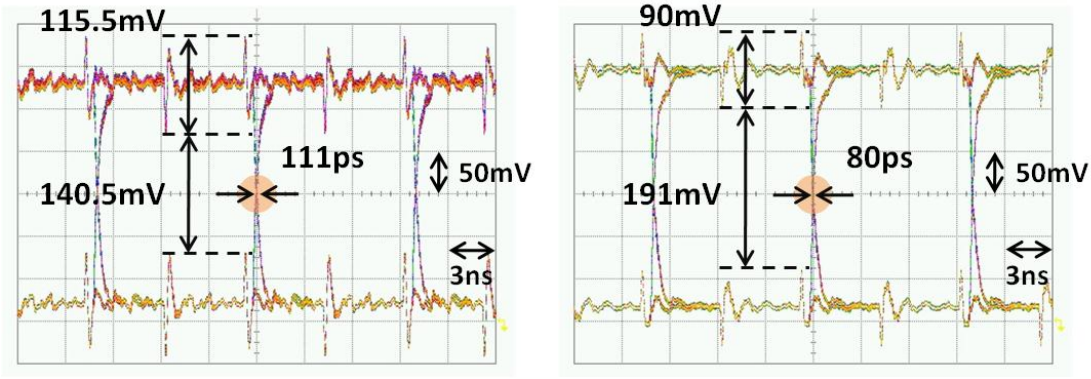


Figure 3.28 Test environment.

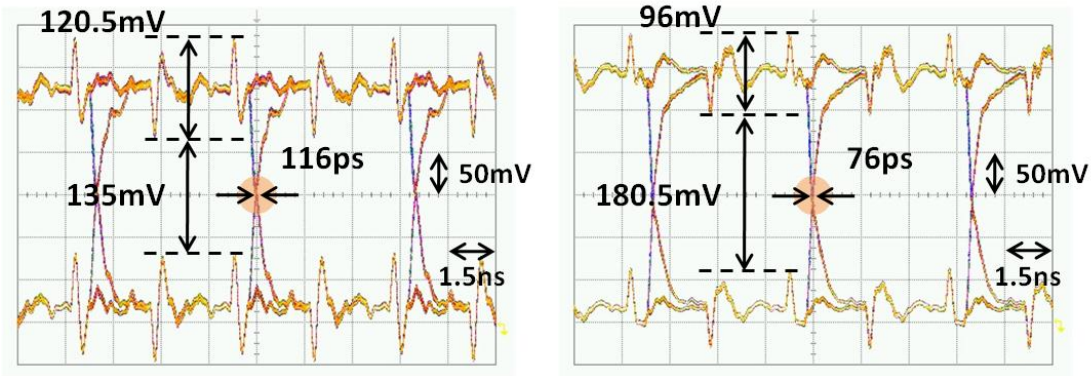
Figure 3.29 shows the eye diagrams of 100 Mbps PRBS. There is a couple of overshoots in the middle of the eye window caused by reflections from impedance discontinuities. They are located at the same timing in both cases so that the cause of the reflection must be the same. However, in the plane-based TV, the size of the overshoot is larger. This is because the voltage fluctuations on the power and ground rail is more serious in the plane-based TV, worsening the overshoot. Using PTL improved the eye height by 36%, and reduced the p-p jitter by 28%.



(a) **(b)**

Figure 3.29 Eye diagrams of 100 Mbps PRBS. (a) Plane-based. (b) PTL-based.

Figure 3.30 shows the eye diagrams of 200 Mbps PRBS. As the eye width decreases with the increasing data rate, the influence of the voltage fluctuation and the overshoot on the eye opening grows. The p-p size of the overshoots is increased by 4.3% and 6.6% in the plane-based and PTL-based TV, respectively. Still, using PTL provides better timing and voltage margins; the eye height is improved by 33.7%, and the p-p jitter is reduced by 34.5%, respectively.

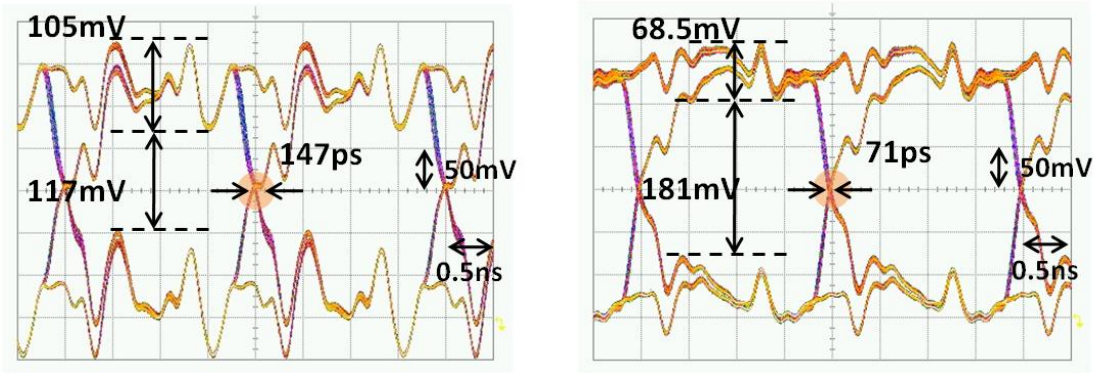


(a) **(b)**

Figure 3.30 Eye diagrams of 200 Mbps PRBS. (a) Plane-based. (b) PTL-based.

Figure 3.31 shows the eye diagrams of 500 Mbps PRBS. The eye shape is distorted with large voltage fluctuations on the power and ground rail. The distortion is less severe

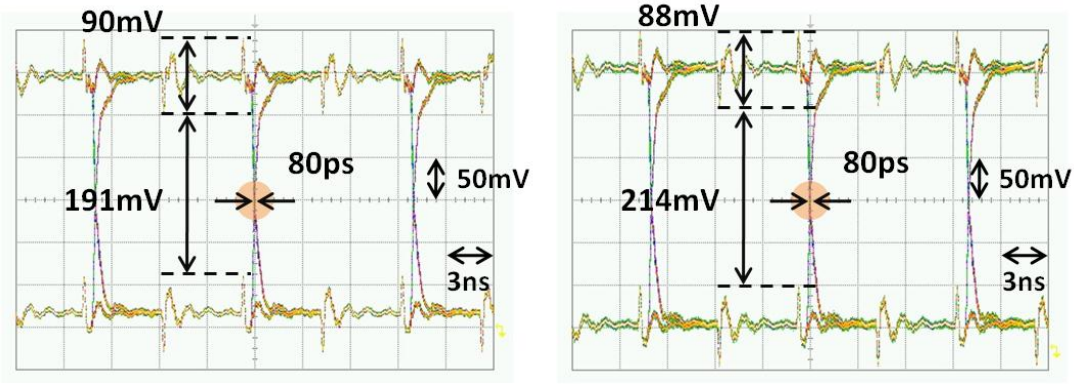
for the eye diagram of the PTL-based TV. By using PTL, the voltage margin is improved by 54.7%, and the p-p jitter is improved by 51.7% which is due to the crossing point in the eye diagram of the plane-based TV being distorted too much. Meanwhile, the crossing point in the eye diagram of the PTL-based TV is still secured.



(a) **(b)**

Figure 3.31 Eye diagrams of 500 Mbps PRBS. (a) Plane-based. (b) PTL-based.

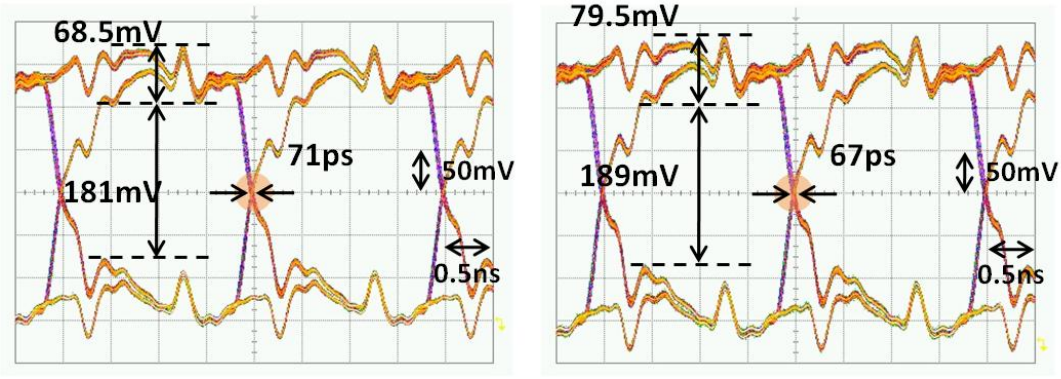
In Figure 3.32, the eye diagrams with and without source termination of the PTL are compared. Figure 3.32(a) shows the same eye diagram as Figure 3.29(b), which is the eye diagram of a 100 Mbps PRBS waveform of the CCPTL-based scheme with a source termination. Figure 3.32(b) shows the eye diagram when the source termination of the CCPTL is removed. As the dc drop across the termination is removed, the eye height is increased from 191 mV to 214 mV. However, the p-p size of the ringing and the p-p jitter remains almost the same, which implies that the signal transmission line is well-matched at the load so that the reflection traveling back to the PTL is minimal.



(a) **(b)**

Figure 3.32 Eye diagrams of 100 Mbps PRBS of the CCPTL-based scheme. (a) With a source termination. (b) Without a source termination.

Figure 3.33 shows the eye diagrams of a 500 Mbps PRBS waveform with and without a source termination for the PTL. Without the source termination, the eye height is increased along with the peak voltage of the ringing, while the p-p jitter is slightly reduced (by 6%). Since the impedance of the circuitry is reduced by the resistance of the source termination, the dc current drawn by the driver is increased, which increases the eye height. During this process, the amount of current fluctuation during the data transition increases, which reveals its negative effect when a 500 Mbps PRBS waveform is used. Therefore, it can be concluded that the role of the source termination becomes more important with an increase in data rate.



(a) **(b)**

Figure 3.33 Eye diagrams of 500 Mbps PRBS of the CCPTL-based scheme. (a) With a source termination. (b) Without a source termination.

Figure 3.34 shows the chip microphotograph. The chip area is 3951 μm × 1875 μm = 7.41 mm^2. The active area of the 1-bit plane-based scheme occupies 3.13×10^{-3} mm^2, while the active area of the 1-bit CCPTL-based scheme occupies 3.73×10^{-3} mm^2. The area difference is coming from the implementation of the pattern detector and dummy path, which is a 19% overhead, as compared to the power-plane-based scheme.

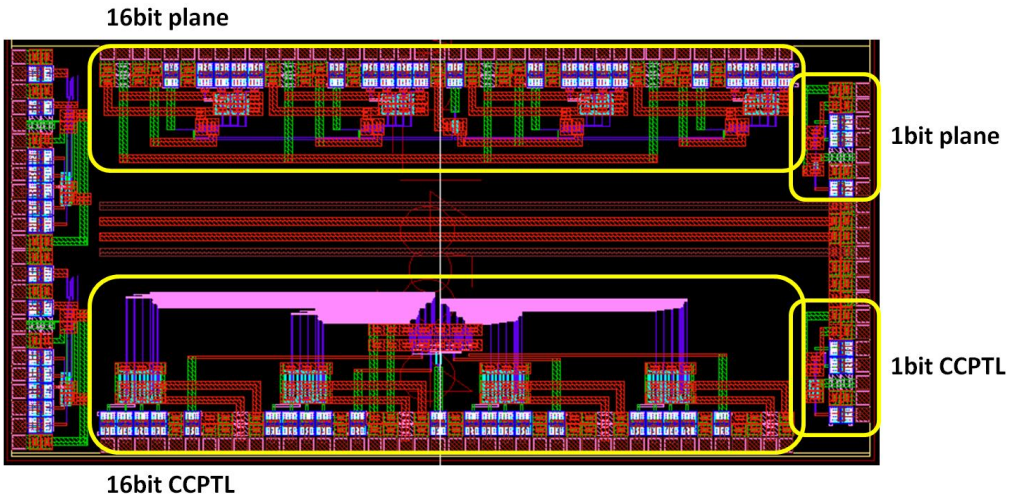


Figure 3.34 Chip layout.

The CCPTL scheme has been extended to 16-bit transmission. Multiple switching buffers will increase the amount of current demand during the data transitions, and thereby worsen the voltage and ground fluctuations. Four transmitters, each for 4-bit transmission, are used to transmit 16-bit data, as shown in Figure 3.35. Control signals are generated from the PRBS output to control the dummy paths. For timing synchronization between the PRBS data and the control signals, edge-triggered D flip-flops are used. In the plane-based scheme, all 16 output buffers are connected to one power plane. In the PTL-based scheme, a single PTL is used to drive four output buffers so that four PTLs are used for 16-bit transmission. The PTLs are not source-terminated, but connected to the power supply directly.

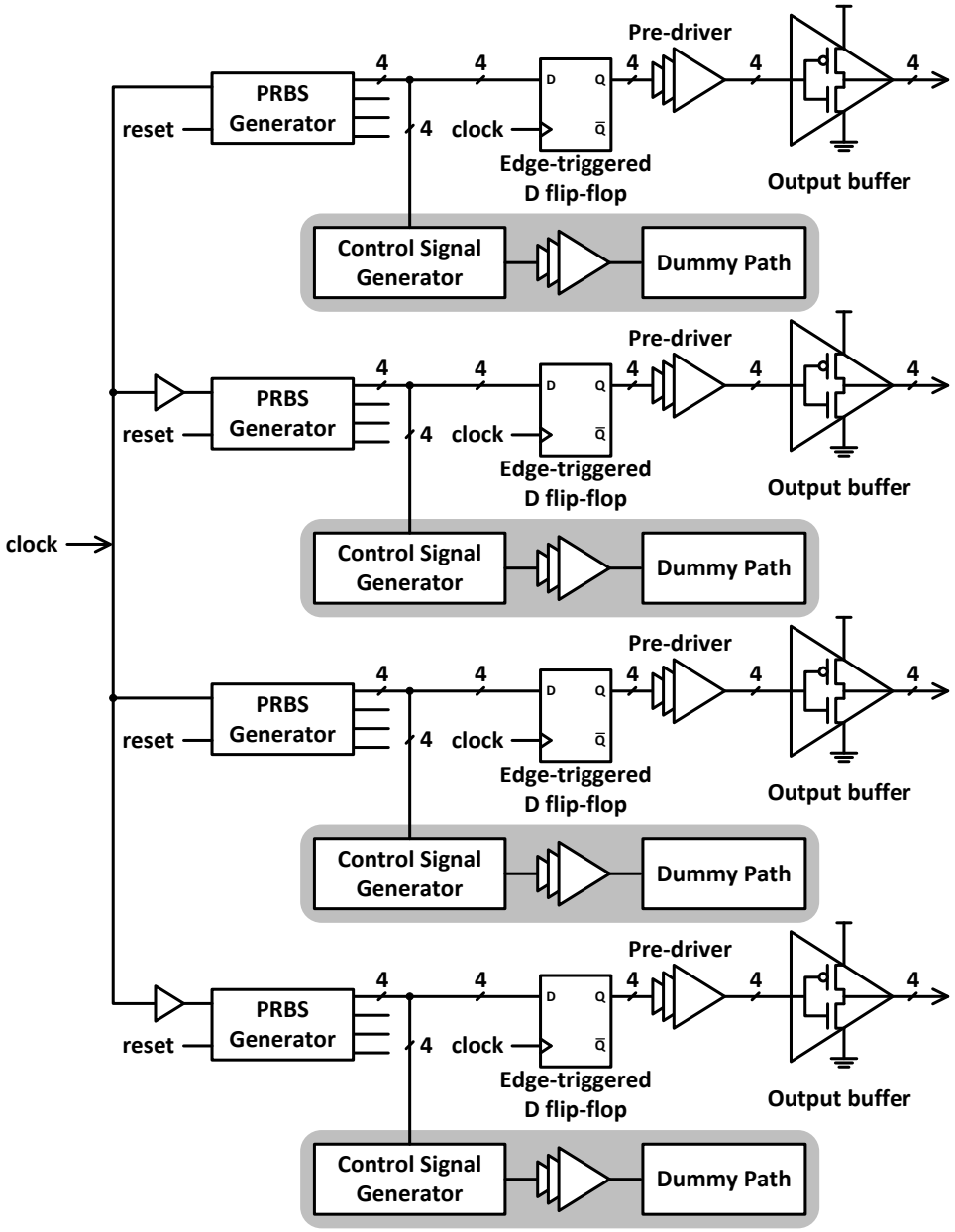
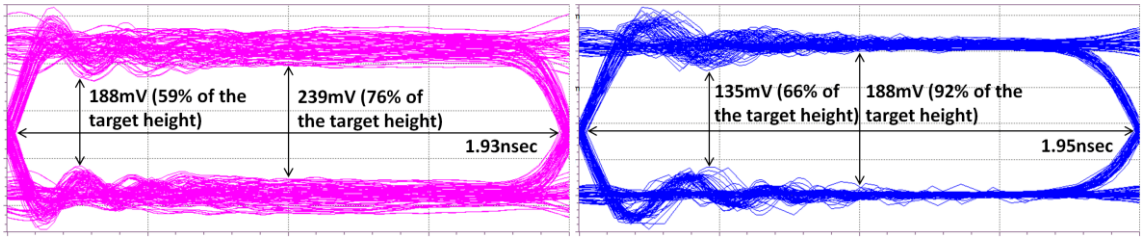


Figure 3.35 Block diagram for 16-bit transmission.

The SPICE simulation of 16-bit transmitter was performed using a macromodel of the test board. The eye diagrams of a 500 Mbps PRBS waveform at the output of the 203 mm-long signal transmission line are compared in Figure 3.36. The target eye height is set different for the power-plane-based and PTL-based output buffers during the design process so that the comparison between the two eye diagrams can be made through the relative eye height. Figure 3.36(a) shows the eye diagram of the power-plane-based

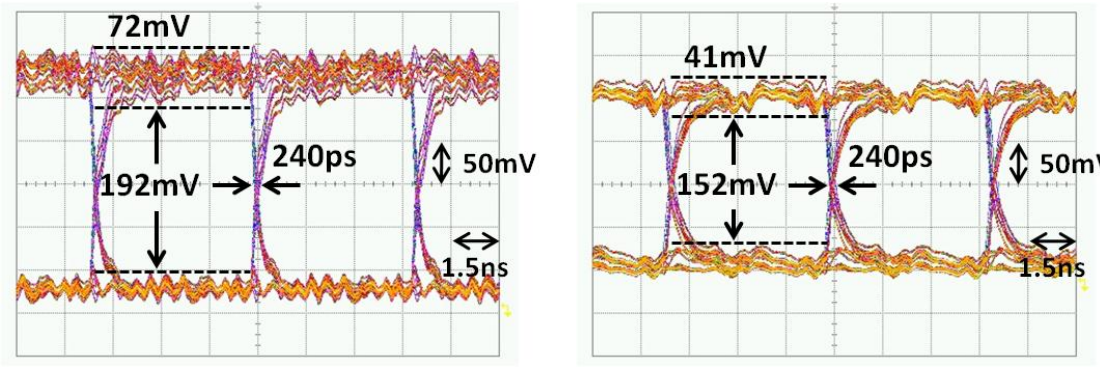
scheme as 15 other output buffers are switching simultaneously. The eye height is 59% of the target amplitude at the edge of the eye window, and the eye width is 1.93 nsec. Figure 3.36(b) shows the eye diagram of the PTL-based scheme, whose eye height is 66% of the target amplitude and whose eye width is 1.95 nsec. The power supply rail (V_{DD} rail) of the power-plane-based scheme is noisier throughout the period of the waveform, resulting in smaller amplitude and larger p-p jitter.



(a) **(b)**

Figure 3.36 SPICE-simulated eye diagrams of 16-bit transmission. (a) Power-plane-based. (b) CCPTL-based.

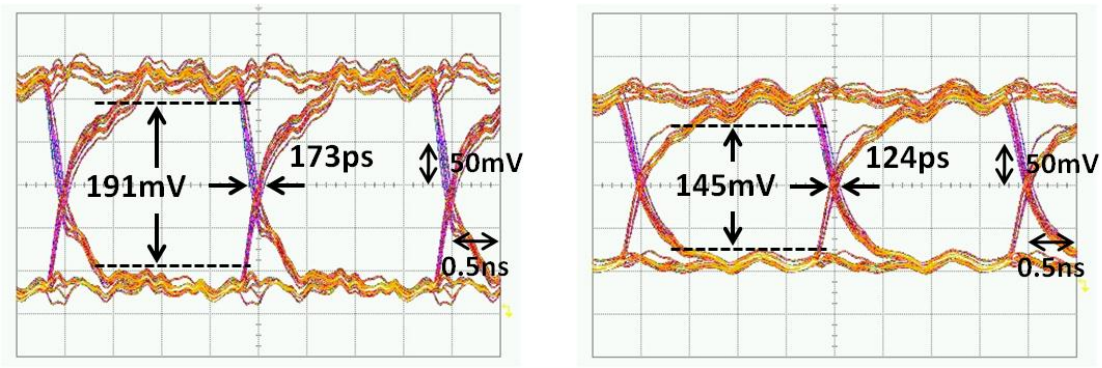
Figure 3.37 shows the eye diagrams of 200 Mbps PRBS. It is important to note that the target eye height for the PTL-based scheme is smaller than that for the plane-based scheme. Therefore, the percentage improvement in the eye height is the important parameter to compare. Based on simulation using ideal power and ground supplies, the target eye height for the plane-based TV is 316 mV, while that for the PTL-based TV equals 204 mV. In the plane-based TV, the eye height is 192 mV, which is 61% of the target height. On the other hand, the eye height of the PTL-based TV equals 152 mV, which is 75% of the target height. This is not an accurate method to compare power integrity, but gives a rough idea of the improvement possible using PTL. The same amount of p-p jitter was measured in both cases.



(a) **(b)**

Figure 3.37 Received eye diagram of 200Mbps PRBS.

Figure 3.38 shows the eye diagrams of 500 Mbps PRBS. The eye height of the plane-based TV is 60% of the target height, while that of the PTL-based TV equals 71%. In terms of p-p jitter, using PTL provides an improvement of 28% compared to using a power plane.



(a) **(b)**

Figure 3.38 Received eye diagram of 500Mbps PRBS.

The layout of the two 16-bit transmitters is shown in Figure 3.34. The active area of the 16-bit plane-based scheme is 2.73×10^{-2} mm^2, and the active area of the 16-bit CCPTL-based scheme is 5.95×10^{-2} mm^2. The area overhead induced by implementing the CCPTL scheme is 118%, which is due to the data pattern detectors and the dummy paths.

3.6 Summary

The first demonstration of the constant current power transmission line (CCPTL) based signaling scheme has been implemented and measured in this chapter. Using PTL resolves the RPD issue, which is the main source of SSN in packages and printed circuit boards. The CCPTL scheme addresses the dynamic dc drop on the power supply network. By adding a dummy path in parallel with the driver, constant current is induced, and it removes the dynamic dc drop along with the charging and discharging process of the PTL during signal transitions. Therefore, the CCPTL scheme is able to deliver noise-free power supply to the IC in idealistic situations, and reduces the layer count. To explore the efficacy of the CCPTL scheme, two TVs were fabricated. Off-the-shelf chips were mounted on the custom-designed test boards, one with a power plane and the other with PTL. Using data rates ranging from 500 Mbps to 3 Gbps, eye diagrams were measured at the far end of the 66 mm-long transmission line. The results show that the PTL improves the quality of the received signal in terms of voltage and timing margin. In terms of correlation, the local maximum jitter appeared at the frequencies where the plane pair was expected to resonate based on the simulation and calculations. The time-domain simulation showed the trend of signal integrity improvement by using the PTL, which was verified using measurements.

CHAPTER 4

PSEUDO BALANCED POWER TRANSMISSION LINE BASED SIGNALING

4.1 Introduction

Recently, on-board chip-to-chip communication is being pushed from several Gbps towards tens of Gbps due to the demand for higher data rate [65]. Single-ended signaling is widely used for memory interface, but it suffers from simultaneous switching noise (SSN), crosstalk, and reference voltage noise [66]. Although differential signaling is free from common-mode noise, it doubles on-chip interconnect count, off-chip printed circuit board (PCB) trace count, and I/O pin count [67], which results in higher cost. To achieve better signal integrity with less expense, studies on pseudo-differential signaling schemes have been undertaken by several researchers [67]-[72]. The original pseudo-differential signaling adds a reference line after a group of data lines, usually limited to four, which results in N+1 physical lines routed in parallel to communicate N signals. Afterward, further improved versions of pseudo-differential signaling schemes have been proposed, which are bus inversion scheme [68], incremental signaling scheme [67][69], balanced coding scheme [70]-[72], and so on.

These signaling schemes still have a limitation in terms of noise reduction due to the power delivery network (PDN). Power planes are generally used to provide a low-impedance path between the voltage regulator module (VRM) and the integrated circuits (ICs) on the printed circuit board (PCB). The problem is that the disruption between the power and ground planes induces return path discontinuities (RPDs) during the data transitions, which create displacement current sources between the power and ground planes, as shown in Figure 3.1(a) [16]. The current sources excite a radial wave between

the planes, which causes the planes to bounce. The resulting power supply noise increases the importance of holding the PDN impedance down, as shown in Figure 4.1, which can only be achieved by increasing the capacitance requirements through new technologies such as thin dielectrics, embedded capacitance, high frequency decoupling capacitors, and so on [33]-[37], as shown in Figure 3.1(a).

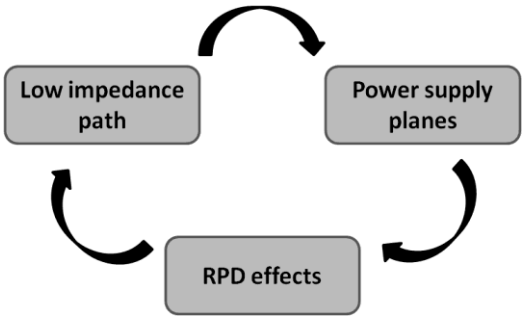


Figure 4.1 Design circle for PDN using target impedance.

Alternatively, methods for eliminating the RPDs can be employed to suppress power supply noise. To eliminate the RPDs, a new PDN design has been proposed in [54]. In the new approach, Power transmission lines (PTLs) are used to supply power to each IC on the PCB or package, as shown in Figure 3.1(b). Using PTLs eliminates the discontinuities between the power and ground planes, thereby preventing the RPD effects [56]. The PTL-based PDN enables both power and signal transmission lines to be referenced to the same ground plane so that a continuous current path can be formed, as shown in Figure 3.1(b). As a result, a closed current loop is achieved and voltage fluctuations caused by the RPDs are removed in idealistic situations. In summary, using PTL reduces the layer count, eliminates the source of SSN, and mitigates the coupling between power and signal networks. Without the RPD-related voltage fluctuation, the design circle associated with the use of target impedance shown in Figure 4.1 can be broken. Instead, the impedance of the PTL is determined by the impedance of the signaling circuits.

As discussed in [56], the PTL-based PDN raises several issues that need to be solved prior to being used in a practical signaling environment, as described in Chapter 3. Constant current through the PTL is one solution proposed to address the first two issues [55]-[58]. In Chapter 3, the use of constant current is demonstrated to be effective. Constant current removes the dynamic characteristics of the dc drop by inducing a fixed amount of voltage drop across the PTL-based PDN. Also, constant current keeps the PTL fully charged at all times, and thereby eliminates the process of repeatedly charging and discharging the power transmission line. The constant current PTL (CCPTL) scheme induces constant current regardless of the input data pattern by adding dummy paths. Nevertheless, it is not an ideal solution due to increased power penalty. To reduce the power penalty while maintaining the merits of using constant current, the pseudo-balanced PTL (PBPTL) scheme has been proposed in [73]. The PBPTL scheme addresses the above issues with lower power penalty than the CCPTL scheme by encoding the original information prior to data transmission, and leads to a better waveform as compared to using power plane with pseudo-balanced signaling scheme.

In this chapter, the design of PDNs using the PBPTL approach is presented in detail. The effectiveness of the PBPTL scheme is then demonstrated by simulation and measurement using two test vehicles (TVs), which are a power-plane-based TV and a PTL-based TV. The functionality of the PTL to convey low-noise power is compared to that of the power plane. Then, the pseudo-balanced signaling scheme is applied to enhance the performance when feeding power to multiple output buffers to drive multiple transmission lines. Two sets of the test vehicles are used: one using an off-the-shelf driver, and the other using a custom-designed transmitter. The simulation and measurement results are presented with further detail to show that use of the PBPTL scheme results in significant improvement of eye opening.

4.2 Pseudo-Balanced Signaling Scheme

In conventional balanced signaling scheme, encoding is performed prior to data transmission. N bits of data are mapped onto ($N+\log_2 N$) bits or less to provide 2^N data patterns with an equal number of 1s and 0s at all times [69]. According to [70], the length of extra bits required for balanced coding is approximately ($0.5 \cdot \log N+1$) for N-bit data. This balanced signaling scheme minimizes the variation of the total driving current through the PDN by controlling the number of high and low states in the output data string. As the total driving current is maintained constant, di/dt can be minimized, and therefore SSN can be reduced [71][72].

To transmit 4-bit information, 6-bit symbols with three 1s and three 0s are required, as shown in Figure 4.2. This results in 50% overhead in terms of off-chip PCB trace and I/O pin count, which is required to maintain an equal number of 1s and 0s in the encoded data word. The disparity between the counts of 1s and 0s is fixed at zero. To reduce such overhead, the pseudo-balanced signaling scheme employs two types of disparity between the counts of 1s and 0s. Let M be the length of the encoded data word, which is pseudo-balanced. M is determined to satisfy the following equation:

$$\begin{aligned} &\frac{M!}{\left(\frac{M}{2}\right)!}+\frac{M!}{\left(\frac{M}{2}-1\right)!} \geq 2^N, \ \ if\ M\ is\ even \\ &\frac{M!}{\left(\frac{M-1}{2}\right)!}+\frac{M!}{\left(\frac{M-1}{2}-1\right)!} \geq 2^N, \ \ if\ M\ is\ odd \end{aligned} \tag{8}$$

In the conventional balanced signaling scheme, only the first term in the left hand side has been used to determine M, while the two terms are included in the proposed scheme. If the minimum M to satisfy the equation is an even number, the difference between the counts of 1s and 0s in M-bit pseudo-balanced data word becomes either 0 or 1. If the minimum M is an odd number, the difference between the counts of 1s and 0s becomes either 1 or 2. By including two types of disparity, fewer extra data bits are required to

cover 2^N data words as compared to using only one type.

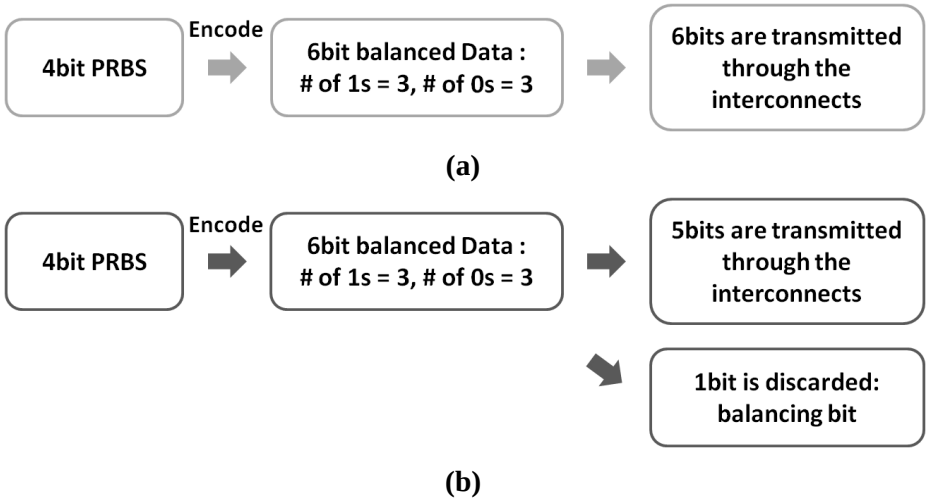


Figure 4.2 Block diagrams of data flow. (a) Conventional balanced signaling. (b) Proposed pseudo-balanced signaling.

For example, when the original data word consists of 4 bits (N=4), the conventional balanced coding scheme requires at least two additional bits, which makes M=6. Using the pseudo-balanced coding scheme, equation (1) is satisfied with M=5, since:

$$\frac{5!}{2!} + \frac{5!}{3!} = 20 \geq 2^4 = 16$$

Thus, the encoded string is 5-bit-long, which is less than the required length for the balanced data word. The 5-bit pseudo-balanced data word can be categorized into two types; the counts of 1s and 0s are either (2, 3) or (3, 2). Since the count of 1s oscillates between 2 and 3, the total driving current also fluctuates between two values. To maintain the total driving current constant, the counts of 1s and 0s need to be maintained constant. To achieve this, a balancing bit is added to the encoded string. When the counts of 1s and 0s are (2,3), the balancing bit becomes 1, while it becomes 0 in the other case. As a result, the counts of 1s and 0s become (3,3) at all times. By adding the balancing bit, two types of disparity are reduced to one, which leads the encoded data word to become balanced. The balancing bit is not transmitted, but terminated at the transmitter after

serving as a parity bit. Therefore, from the PDN's viewpoint, the encoded data are balanced. The number of turned-on drivers connected to the PDN is constant, which induces constant current through the PDN at all times. At the receiver, the received data are pseudo-balanced. An example of symbol transition is shown in Figure 4.3. 4-bit original data are mapped onto 6-bit balanced data words. Here, the 6^{th} bit is the balancing bit. The balanced data turns on 3 out of 6 drivers at all times, resulting in the constant PDN current of 3×I. Only the 5-bit symbol is transmitted and arrives at the receiver, in which the number of 1s is either 2 or 3. The 5-bit pseudo-balanced data word provides enough patterns to uniquely encode the original 4-bit information and to recover it at the receiver.

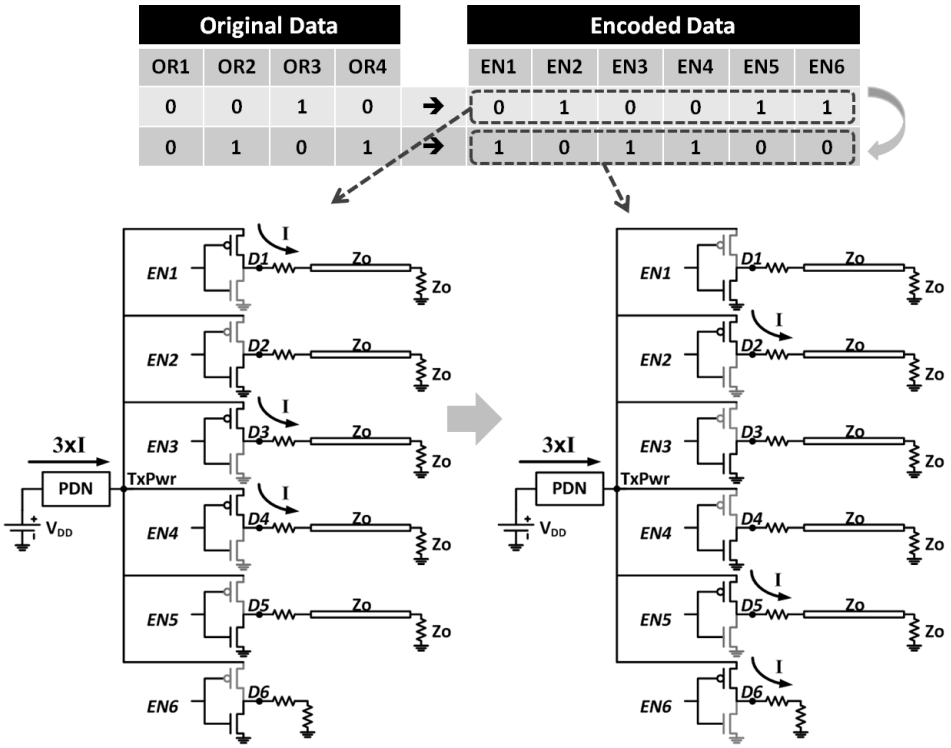


Figure 4.3 An example of symbol transition.

The cases of N being equal to 4, 5, and 6 are summarized in Table 4.1. When N=5, the length of the encoded data word becomes 7 with the balancing bit. The counts of 1s and 0s in the encoded data word are fixed at (3,4) so that the disparity between the counts

of 1s and 0s is one at all times. The data words with unequal but constant numbers of 1s and 0s also keep the total driving current constant, providing a parallel effect to having an equal number of 1s and 0s. Still, the difference between the counts of 1s and 0s should be kept low to minimize the current fluctuations during data transitions.

Table 4.1 Pseudo-Balanced Signaling Scheme With N=4,5,6.

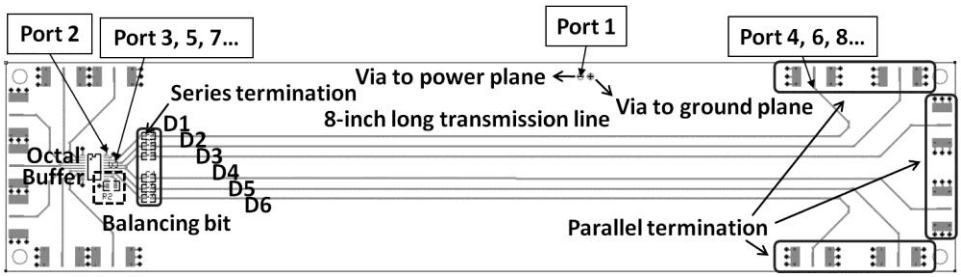
N	Number of patterns	M	(1s, 0s)	Overhead	new M	(1s, 0s)	With balancing bit	(1s, 0s)	Number of patterns	Overhead
4	16	6	(3,3)	50	5	(2,3), (3,2)	→	(3,3)	20	25
5	32	7	(3,4)	40	6	(2,4), (3,3)	→	(3,4)	35	20
6	64	8	(4,4)	33.3	7	(3,4), (4,3)	→	(4,4)	70	16.7

The pseudo-balanced signaling scheme induces constant current through the PDN. Therefore, it is expected to remove the dynamic characteristic of the dc drop across the source termination of the PTL; to eliminate the process of repeatedly charging and discharging the power transmission line by keeping the PTL fully charged; and to reduce the layer count, which leads to lower cost. These advantages will be achieved with reduced power penalty as compared to the CCPTL scheme described in [56]. However, the disadvantage of using the PBPTL scheme is additional circuitry and power required for the encoding and decoding process.

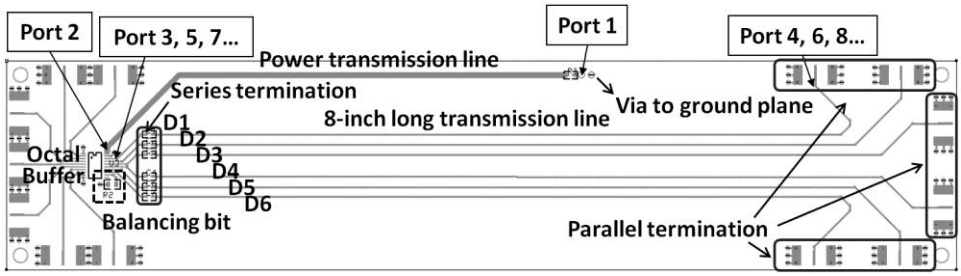
4.3 Test Vehicle Design and Simulation Results

The effectiveness of the PBPTL approach is demonstrated using two TVs (TVs), which are the power-plane-based TV and the PTL-based TV. The top view of the TVs is shown in Figure 4.4. For the power-plane-based TV, a pair of 9.35 inch by 2.05 inch planes with 28 mil FR4 dielectrics is used for power and ground planes. For the PTL-based TV, a 25 ohm transmission line is used to feed power to the drivers. A 20-pin TSSOP-packaged octal driver is mounted on each board. Only 6 drivers are used for this experiment. Each is connected to an 8-inch long signal transmission line. The signal

transmission lines are both series- and parallel-terminated. A series termination of 200 ohm is used to limit the amount of current through the I/O driver and thus reduce the current load of the driver. Then, each signal transmission line is terminated by a 50 ohm load through an SMA connector. A 0.1 μF decoupling capacitor is placed between the power and ground pins of the device to respond to the sudden surge of current during transitions in both TVs. The stack-up details of the test boards are also shown in Figure 4.5. Copper and FR4 are used for metal and dielectric layers. The conductivity of copper is assumed to be 5.8×10^{7} S/m. The dielectric constant and loss tangent of FR4 are 4.6 and 0.025, respectively.



(a)



(b)

Figure 4.4 Top views of the test vehicles. (a) Power-plane-based TV. (b) PBPTL-based TV.

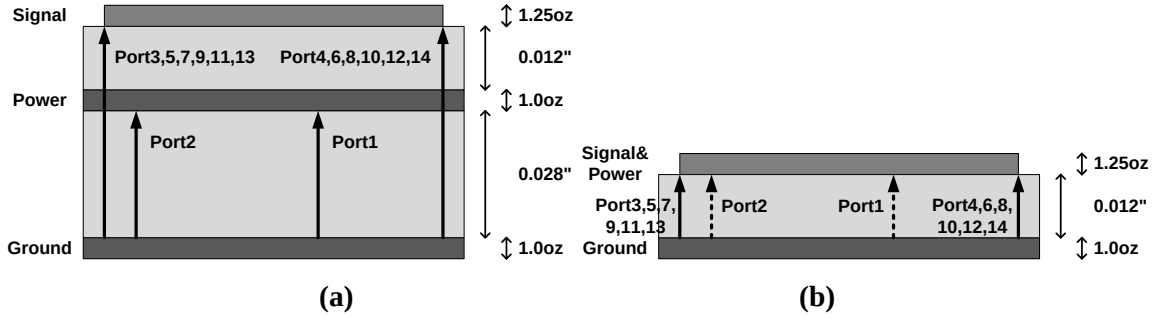


Figure 4.5 Side views of the test vehicles. (a) Power-plane-based TV. (b) PBPTL-based TV.

An electromagnetic solver, Sphinx [51], was used to model the two TVs in frequency domain. Fourteen ports were defined for each structure: two ports for the PDN (port 1 and 2) and twelve ports for six signal transmission lines (port 3, 5, 7, 9, 11, 13 at input and port 4, 6, 8, 10, 12, 14 at output). The reference used for all the ports was the ground plane. In Figure 4.6, the insertion loss between the input and output of a signal transmission line is compared between TV1 and TV2, and between before and after adding a decoupling capacitor to the PDN. The insertion loss of TV1 has multiple resonances, which is the result of the coupling between the power/ground plan pair and the signal transmission line. The first dip appears at 313 MHz, which coincides with the half-wavelength ($\lambda/2$) resonant frequency of the plane cavity. When a 0.1 μF decoupling capacitor with a 2 nH equivalent series inductance (ESL) is added to the power and ground planes in TV1, the decoupling capacitor changes the response of the PDN in the frequency domain. It leads to the change in the insertion loss below 1 GHz, as shown in the zoomed-in plot in Figure 4.6. With and without the decoupling capacitor, the transmission characteristic of the signal line suffers from non-monotonic variation over frequency in TV1, which can create problems for signal integrity. The insertion loss of TV2 has a smooth negative slope with and without the decoupling capacitor. Since there is no coupling between the power supply path and the signal transmission line, the decoupling capacitor added to the PTL does not affect the insertion loss of the signal line. It reaches -10.32 dB at 10 GHz, which is 2 dB less than TV1.

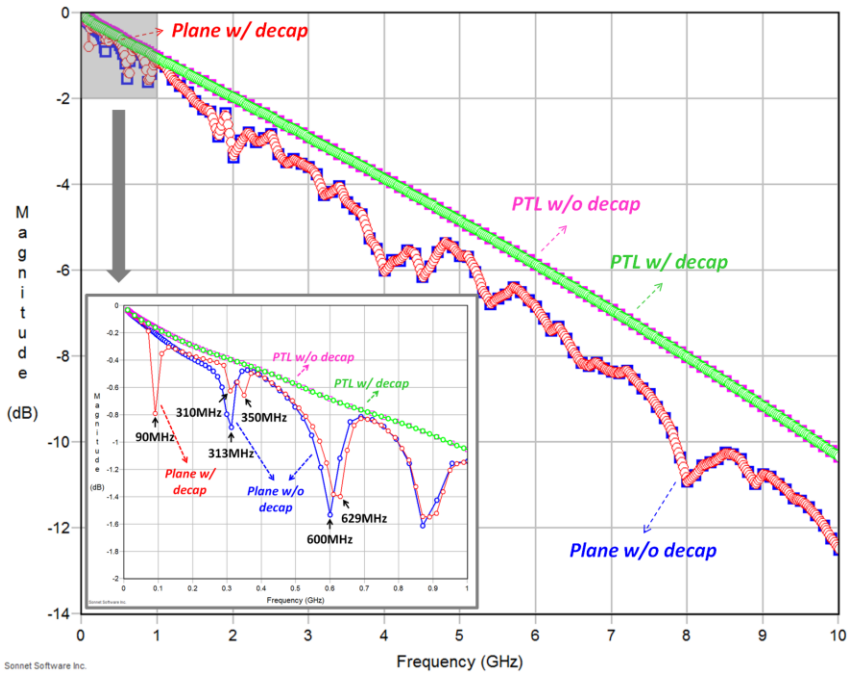
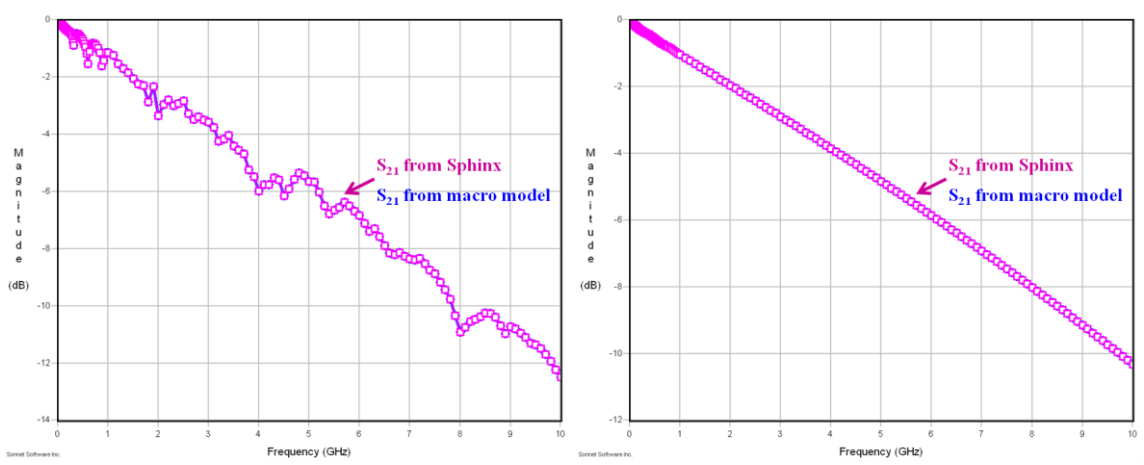


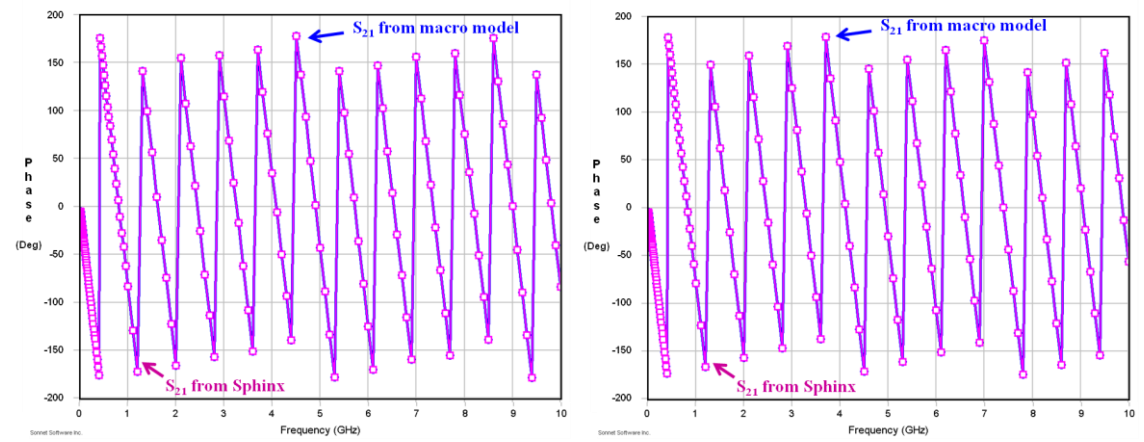
Figure 4.6 Comparison of insertion loss of signal transmission line with and without 0.1uF decoupling capacitor and 2 nH ESL.

For time-domain analysis, the frequency domain response of each TV was converted into a SPICE-compatible equivalent circuit using a macromodeling tool, IdEM Plus [62]. The frequency response of the macromodel is compared with the original insertion loss data from Sphinx in terms of magnitude in Figure 4.7, and in terms of phase in Figure 4.8. Good agreement is observed between both magnitude and phase data from the macromodel and sphinx for both TVs.



(a) **(b)**

Figure 4.7 Comparison of magnitude of insertion loss from Sphinx and macromodel. (a) Power plane-based. (b) PTL-based.



(a) **(b)**

Figure 4.8 Comparison of phase of insertion loss from Sphinx and macromodel. (a) Power plane-based. (b) PTL-based.

The SPICE (Simulation Program with Integrated Circuit Emphasis) simulation setup with the macromodel is shown in Figure 4.9. First five drivers are connected to 50 ohm transmission lines through series terminations. For each series termination, a 200 ohm resistor is used. Each transmission line is load-terminated by 50 ohms. The connection of the 6th driver is determined by the signaling scheme used during testing. For the conventional signaling scheme using PRBS data, the 6th driver is connected to the same 50 ohm transmission line through a series termination as the other five drivers. For the

pseudo-balanced signaling scheme, the 6th driver is connected to the series- and load-terminations directly, carrying the balancing bit. The port setup is the same as in Figure 4.4. Ports 1 and 2, which represent the PDN, are connected to the dc voltage of 5 V and the power pin (VDD) of the driver, respectively. The 0.1 μF decoupling capacitor is added to Port 2 in series with a 2 nH ESL. The value of the parasitic inductance has been determined based on [24]. The 200 ohm series terminations are used to connect the outputs of the drivers and the inputs of the signal transmission lines (Ports 3, 5, 7, 9, and 11). The 50 ohm load terminations are added to the outputs of the signal lines (Ports 4, 6, 8, 10, and 12). The input data rate used is 300 Mbps, which is the maximum operating frequency of the device. The eye diagrams are observed at the output of an 8-inch long signal transmission line.

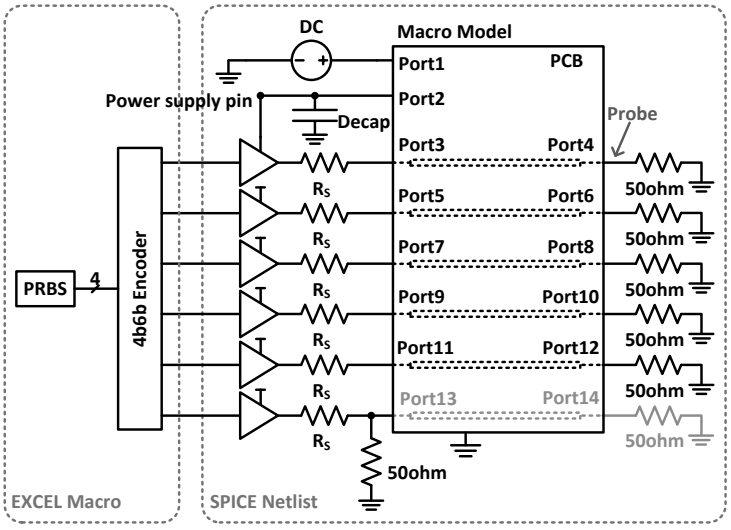
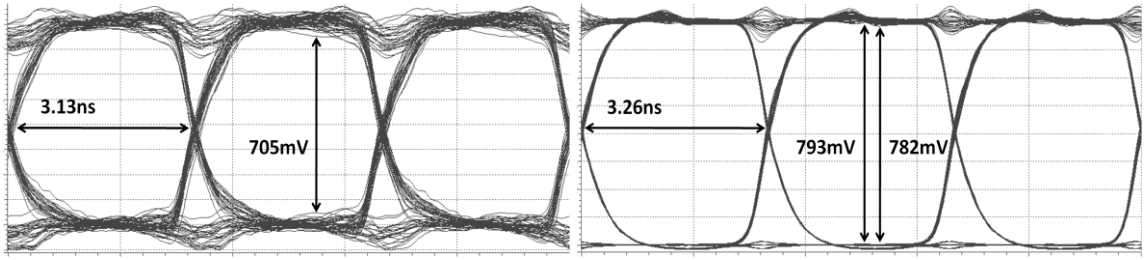


Figure 4.9 SPICE simulation setup.

Figure 4.10 shows the simulated eye diagrams of the PRBS data that has traveled along the 4th 8-inch long trace on TV1 and TV2. The transmission of 6-bit parallel PRBS data is simulated to compare the functionality of power plane and PTL. The power supply and ground rails of TV1 are much noisier so that the voltage and timing margins are reduced. The eye diagram of the power-plane-based TV in Figure 4.10(a) has the eye

height of 705 mV and the peak-to-peak (p-p) jitter of 200 psec, while the eye diagram of the PTL-based TV in Figure 4.10(b) has the eye height of 782 mV and p-p jitter of 70 psec. By using PTL, the eye height is increased by 11% and the peak-to-peak (p-p) jitter is reduced by 65%.



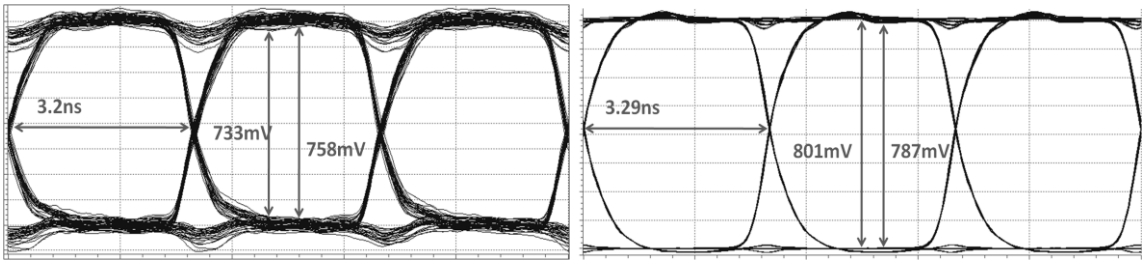
(a) **(b)**

Figure 4.10 Simulated eye diagrams of PRBS data with 200ohm series resistor. (a) Power-plane-based TV. (b) PTL-based TV.

For the pseudo-balanced signaling scheme, the encoded data words are used as input data for the drivers. When 4-bit PRBS data are mapped on to 6-bit balanced data, the 4^{th} data bit sequence is maintained to be the same; the 4^{th} data bit in the balanced data thus has the same sequence as the 4^{th} data bit in the original PRBS data. Then, the eye diagram is measured at the output of the 4^{th} channel (Port 10) throughout this chapter. As a result, the same effect of inter-symbol interference is imposed for comparison between different signaling schemes.

Figure 4.11 shows the eye diagrams of pseudo-balanced data at the output of the 8-inch long trace on TV1 and TV2. The effectiveness of the pseudo-balanced signaling scheme is demonstrated using both TV1 and TV2. Figure 4.11(a) is the eye diagram of TV1 using the pseudo-balanced signaling. As compared to Figure 4.10(a), the input data has become balanced. The use of the balanced data draws constant current from the PDN and therefore lessens the voltage fluctuations on the power supply and ground rails. As a result, the timing and voltage margins are improved by 4% and 35%, respectively as compared to using PRBS data in TV1. When the power plane is replaced by a PTL, the

eye opening is increased from 758 mV to 787 mV and from 3.2 nsec to 3.29 nsec, as shown in Figure 4.11(b). As compared to Figure 4.10(b), the voltage fluctuations on the power supply rail of the PTL during the data transitions are suppressed.



(a) **(b)**

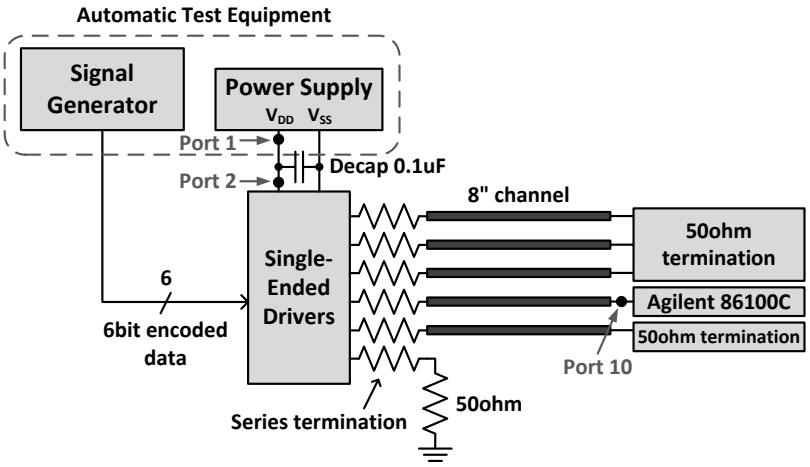
Figure 4.11 Simulated eye diagrams of pseudo-balanced data with 200ohm series resistor. (a) Power-plane-based TV. (b) PBPTL-based TV.

The simulation setup did not include the package model of the device and the effect of wires, vias, and parasitics. Therefore, the measurement results can be worse than the simulation results in terms of voltage and timing margin. Still, the simulation shows the advantage of using PTL for power distribution along with the positive effect of using the pseudo-balanced signaling scheme.

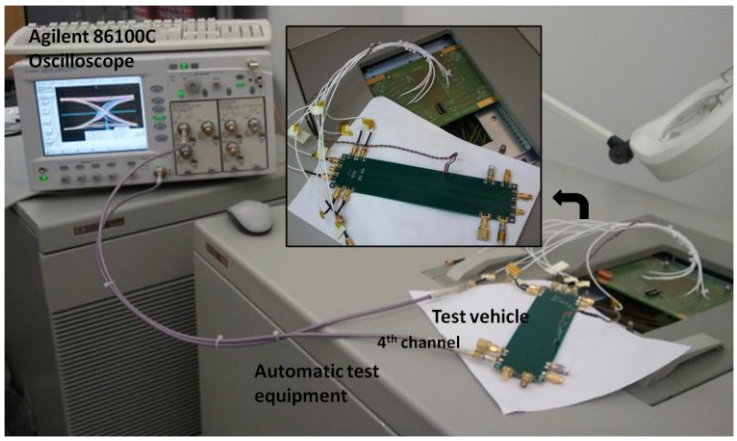
4.4 Measurement Results

The effectiveness of the PBPTL was demonstrated using three TVs: a conventional power-plane-based TV (TV1); a PTL-based TV, in which the PTL is directly connected to the voltage source without termination (TV2); and a PTL-based TV, in which the PTL is source-terminated (TV2'). The test environment is shown in Figure 4.12. An automatic test equipment (ATE) system was used to provide power and ground supply voltages and input data patterns, as shown in Figure 4.12(a). The power supply voltage was 5V, and the target data rate was 300 Mbps. Each driver was connected to an 8-inch long channel through a series termination of 200 ohm to limit the amount of current through the driver and channel. Eye diagrams were measured at the output of the 4^{th} 8-inch long channel,

using Agilent 86100C oscilloscope. The other channels were load-terminated by 50 ohms. Figure 4.12(b) shows the actual test setup in the lab.



(a)

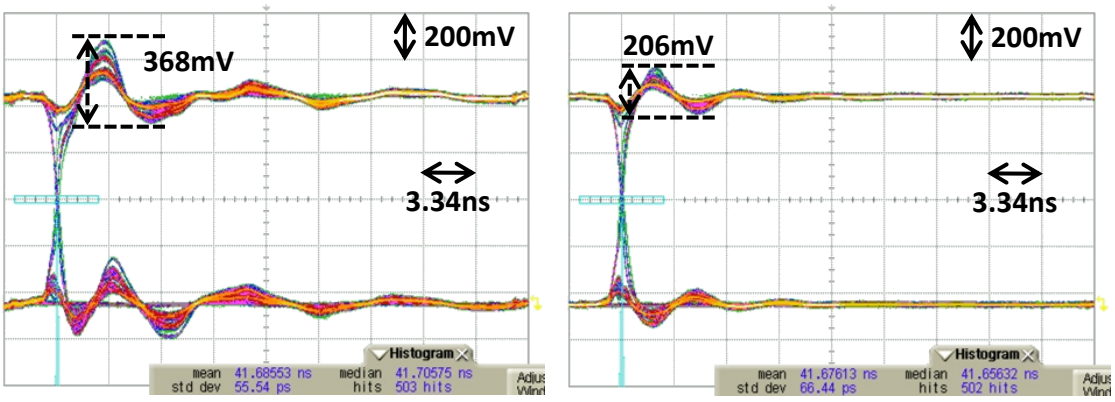


(b)

Figure 4.12 Test environment. (a) Block diagram. (b) Actual setup.

First, the noise characteristics of the output waveform are compared between TV1 and TV2 in Figure 4.13. In TV1, excessive ringing occurs, which is excited by both the negative and positive transitions of the output data, as shown in Figure 4.13(a). When a decoupling capacitor is added between the power and ground planes, the ESL of the decoupling capacitor is in parallel with the plane capacitance and the turn-on impedance of the driver, which forms a parallel RLC circuit. The power supply becomes an under-damped circuit, causing ringing and noise peaking [81]. The peak-to-peak value of the

ringing is 368 mV. Moreover, the decoupling capacitor provides a current path at the RPD location in TV1 so that the impact of the ESL on the waveform is manifested. The ringing continues to about 30 nsec before it is damped. The ringing on the waveform of TV2 is less severe, as shown Figure 4.13(b). Using PTL, a closed current loop is achieved without the decoupling capacitor. Thus, the role of the decoupling capacitor is more of a charge reservoir responding to the sudden surge of charge during the data transitions in TV2, which lessen the impact of the ESL. Without a plane cavity, the power supply of TV2 becomes a series RLC circuit with a larger damping factor when combined with the decoupling capacitor, the turn-on impedance of the driver, and the series/parallel terminations of the signal line. As a result, the peak-to-peak value of the ringing is 206 mV, which is 44% smaller than that of TV1. The damping is achieved faster (less than 10 nsec). The high impedance of the transmission line also contributes to the damping so that the waveform reaches the steady state faster.



(a) **(b)**

Figure 4.13 Noise characteristic with R_S=200ohm. (a) Plane-based TV. (b) PTL-based TV.

Figure 4.14 shows the eye diagrams of PRBS data and balanced data, which are measured at the output of the 4th channel on TV1, TV2, and TV2'. The signal has travelled a distance of 8 inches along the transmission line to reach the output of the line. To maintain consistency, 1k samples were used to construct the eye diagrams, and 8k

samples were used to measure the p-p jitter. First, the eye diagrams of PRBS data versus balanced data are compared for TV1 (Figure 4.14(a) vs. Figure 4.14(b)). The period of the input data is approximately one quarter of the period of the ringing so that the eye diagram of TV1 is deformed by the positive overshoot in both cases. As the input data become balanced, the transitions and fluctuations are better controlled with less variation and more regularity so that the quality of the eye diagram improves. Nevertheless, the difference between the p-p jitters is 15 psec, which is a reduction of 2% for TV1. The quantitative improvement is minimal due to the unresolved RPD effect. The balanced data stabilizes the total driving current to reduce the switching noise, but the RPD still causes the voltage fluctuations between the power and ground planes, which are coupled to the signal being transmitted [10]. Next, the eye diagram of the PRBS data is compared between TV1 and TV2 (Figure 4.14(a) vs. Figure 4.14(c)). The p-p jitter of TV1 is 707 psec, while that of TV2 is 643 psec, which is a reduction of 9.1% by replacing the power plane with a PTL. Also, the improved shape of the eye diagram demonstrates the effectiveness of the PTL in removing the RPDs and thus reducing the power supply noise.

As the balanced signaling scheme is applied to TV2, the p-p jitter becomes 537.8 psec, as shown in Figure 4.14(d), which is an improvement of 22.2% as compared to TV1. For TV2, the p-p jitter is reduced by 16.4% by using the balanced data instead of the PRBS data. The eye diagrams of TV2', which has a 25 ohm termination at the source end of the PTL, are shown in Figure 4.14(e) and Figure 4.14(f). When the PRBS data are used as input data, the eye diagram of TV2' shows the improved jitter performance as compared to TV2. Since the source termination prevents multiple reflections on the PTL, the source-terminated PTL outperforms the un-terminated PTL. However, increased supply voltage level is required to compensate for the DC drop across the termination. In this experiment, the source termination results in a power penalty of 53%. When the balanced data is applied to TV3, the p-p jitter becomes 555.7 psec, which is a degradation

of 20 psec as compared to that of TV2. Once the balanced data are used to induce constant current through the PTL, the source termination is not so effective in improving the waveform, but may cause a reverse effect. Since the multiple data is not fully synchronized, current fluctuations are inevitable during the data transitions. During the transitions, the source termination may induce the current fluctuations and produce negative results. Within TV3, the p-p jitter is reduced by 10.5% by using the balanced data.

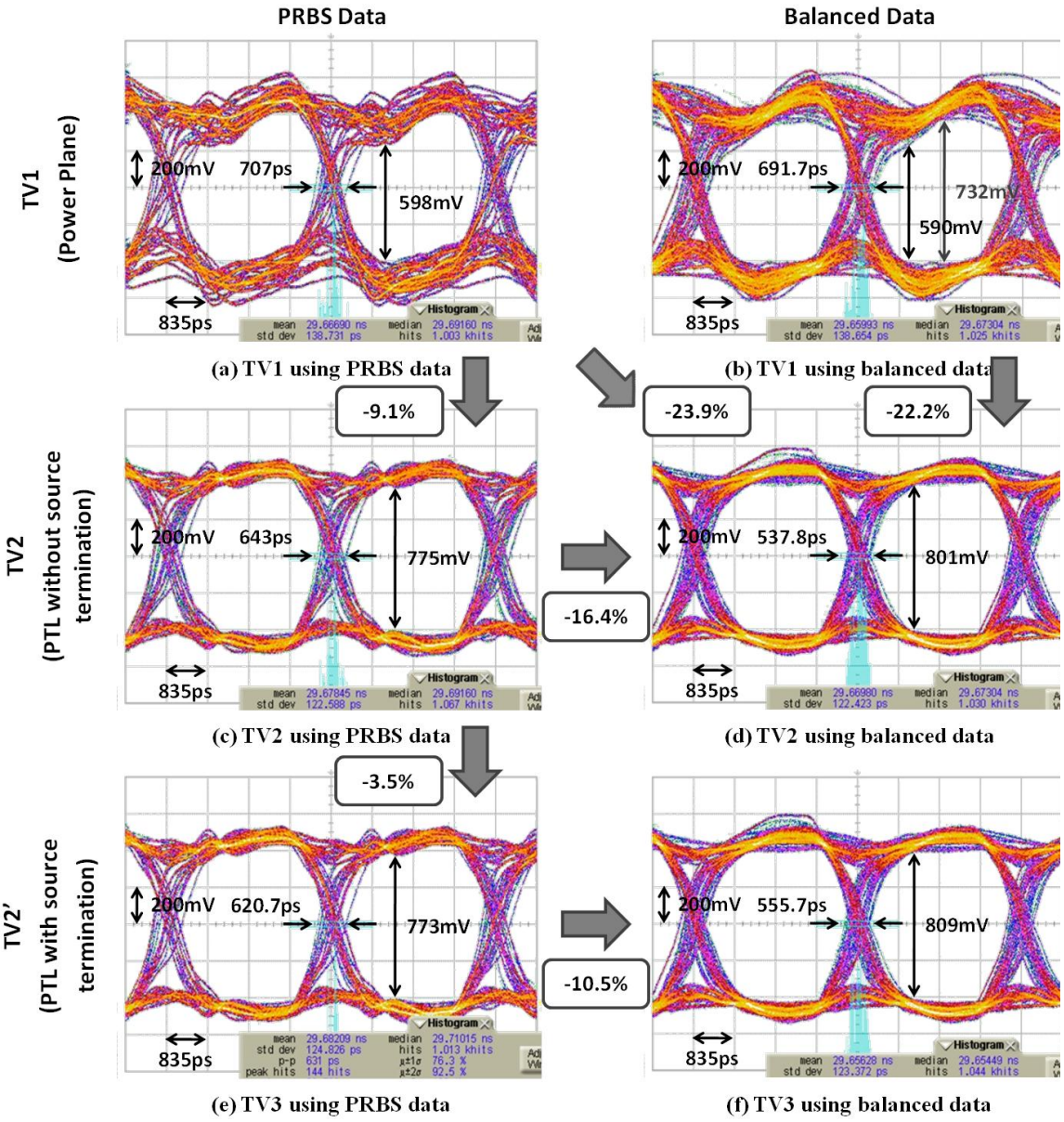
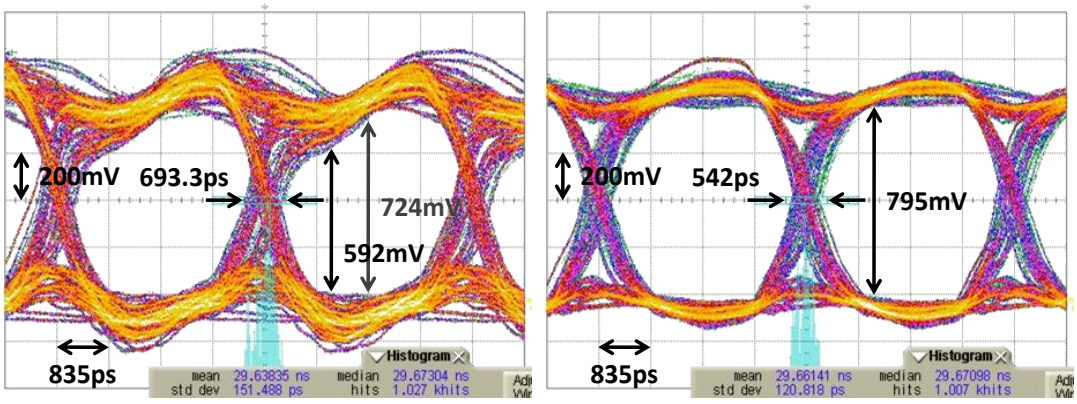


Figure 4.14 Received waveforms. (a) TV1 using PRBS data. (b) TV1 using balanced data. (c) TV2 using PRBS data. (d) TV2 using balanced data. (e) TV3 using PRBS data. (f) TV3 using balanced data.

Finally, the pseudo-balanced signaling scheme is applied to TV1 and TV2. The 6th bit is considered as a balancing bit so that the 6th driver is connected to a resistor whose value equals the sum of the series and parallel terminations. It contributes to drawing constant current from the PTL, but does not increase the PCB trace count. The resulting eye diagrams at the output of the 4th channel on TV1 and TV2 are shown in Figure 4.15.

Between the balanced and pseudo-balanced signaling schemes, the jitter difference is minimal for both TVs: 1.6 psec for TV1, and 4.2 psec for TV2. The eye height is almost the same as well. It can be concluded that the pseudo-balanced signaling scheme induces the same performance as the balanced signaling scheme, but reduces the PCB trace count.



(a) **(b)**

Figure 4.15 Received eye diagrams of pseudo-balanced data. (a) Power plane (TV1). (b) PTL without termination (TV2).

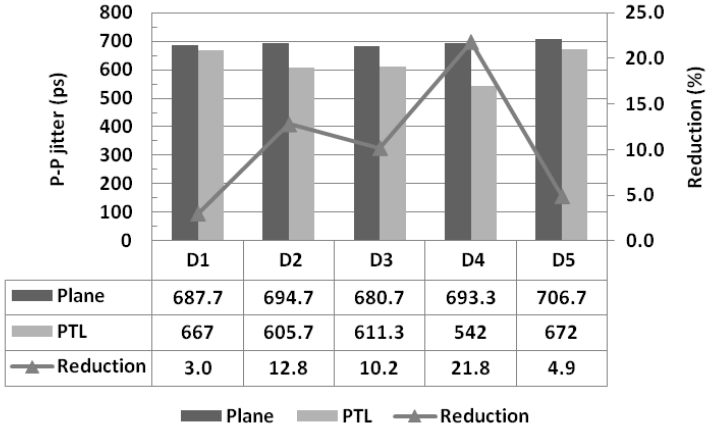
The p-p jitter values of TV1, TV2, and TV2' using three different signaling schemes are summarized in Table 4.2. Using PTL reduced the p-p jitter regardless of the signaling scheme as compared to using power plane. Although the balanced signaling scheme is employed to reduce the power supply noise, it has its limitation when used for TV1. Neither the balanced nor pseudo-balanced signaling scheme solves the RPD issue in TV1. However, those signaling schemes do resolve the issues associated with the PTL so that combining either the balanced or pseudo-balanced signaling scheme with the PTL leads to a significant improvement in terms of p-p jitter. All the p-p jitter values are much worse than what was expected through SPICE simulation. However, the improvement trend has been captured by the simulation.

Table 4.2 Comparison of Peak-to-Peak Jitter (R_{SERIES}=200ohm).

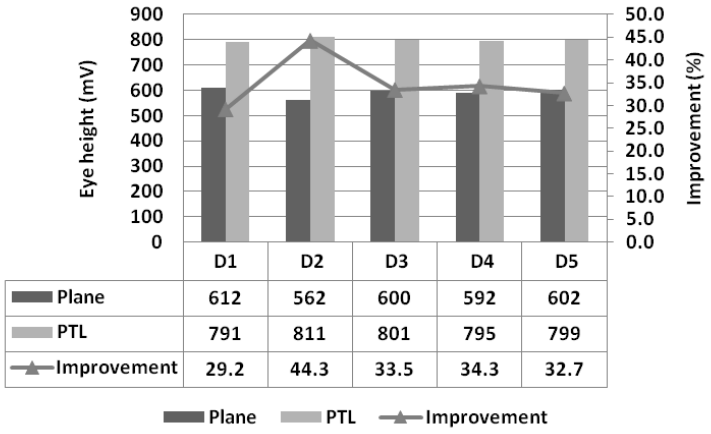
	Plane-based	PTL-based			
		without termination		with termination	
	p-p jitter	p-p jitter	%Δ	p-p jitter	%Δ
Pseudo-random	707 ps	643 ps	-9.1%	620.7 ps	-12.2%
Balanced	691.7 ps	537.8 ps	-22.2%	555.7 ps	-19.7%
Pseudo-balanced	693.3 ps	542 ps	-21.8%	539.3 ps	-22.2%

* %Δ shows the jitter improvement compared to the plane-based TV.

As the pseudo-balanced signaling scheme is applied, the p-p jitter and eye height are measured at the output of all five channels and are compared between TV1 and TV2 in Figure 4.16. The dark grey bar is the measured value of TV1, while the light grey bar is that of TV2. The reduction rate in p-p jitter by using the PBPTL is at least 3%, and at most 21.8%. The improvement in terms of eye height ranges from 29.2% to 44.3%. On average, the PBPTL reduces the p-p jitter by 10.5% and improves the eye height by 34.8%, as compared to using the power plane with the pseudo-balanced signaling scheme. This performance improvement is attributed to eliminating the RPDs and achieving the current balancing. Also, the interaction between the plane capacitance and the parasitic inductance, which has induced the anti-resonance, is prevented so that the improvement becomes even more significant. Since the ESL of the decoupling capacitor has less impact on the waveform, the placement of the decoupling capacitor on the PTL-based board requires less complexity and cost.



(a)



(b)

Figure 4.16 Comparison of p-p jitter and eye height between the power-plane-based and PTL-based TV. (a) P-P jitter. (b) Eye height.

When the required power to transmit 1 bit is assumed to be P, the expected power consumption to transmit 4-bit PRBS data and 6-bit balanced data are compared in Table 4.3. Four bits provide sixteen (=2^4) different data patterns based on the number of high states. The number of high states varies from 0 to 4. The maximum amount of current is drawn from the power supply in the HHHH state, consuming the maximum power. On the other hand, no current flows through the PDN in the LLLL state. When it is assumed that all the data patterns have an equal probability for its occurrence, the expected power consumption to transmit 4-bit PRBS data is 2·P. Using 6-bit balanced data, the number of

high states is constant at 3. As a result, the expected power consumption becomes 3·P. The calculated power penalty is 50%. It is the signaling scheme that imposes the power penalty, not the PTL itself. The pseudo-balanced signaling scheme addresses the issues associated with the PTL with 50% power overhead, which is lower than that required by the CCPTL scheme.

Table 4.3 Comparison of Power Consumption.

Data Pattern		Probability	Power consumption	
			Pseudo random	Balanced
1	LLLL	0.0625	0	0.1875·P
2	LLLH	0.0625	0.0625·P	0.1875·P
3	LLHL	0.0625	0.0625·P	0.1875·P
4	LHLL	0.0625	0.0625·P	0.1875·P
5	HLLL	0.0625	0.0625·P	0.1875·P
6	LLHH	0.0625	0.125·P	0.1875·P
7	LHLH	0.0625	0.125·P	0.1875·P
8	HLLH	0.0625	0.125·P	0.1875·P
9	LHHL	0.0625	0.125·P	0.1875·P
10	HLHL	0.0625	0.125·P	0.1875·P
11	HHLL	0.0625	0.125·P	0.1875·P
12	LHHH	0.0625	0.1875·P	0.1875·P
13	HHLH	0.0625	0.1875·P	0.1875·P
14	HLHH	0.0625	0.1875·P	0.1875·P
15	HHHL	0.0625	0.1875·P	0.1875·P
16	HHHH	0.0625	0.25·P	0.1875·P
Total Power Consumption			**2·P**	**3·P**

* The required power to transmit 1 bit of high state is assumed to be P.

4.4.1 Effects of ESL

In the power-plane-based structure, the objective of adding a decoupling capacitor is to eliminate the effects of the power bus inductance and resistance [76]. The displacement current sources created by the RPDs excite the cavity between the power and ground planes, which leads to excess voltage fluctuations. As the power bus

inductance and resistance becomes higher, transient current through the power supply path cause the voltage fluctuations to worsen, aggravating the RPD effect. The decoupling capacitor is added to alleviate such fluctuations by providing a current path at the RPD location and reducing the inductance in the power supply path, as shown in Figure 4.17. Therefore, the performance of the decoupling capacitor is limited by the ESL, which is against the objective of decreasing the series inductance. Moreover, the ESL interacts with the capacitance of any capacitor in parallel, as shown in Figure 4.17, causing an impedance peak [16].

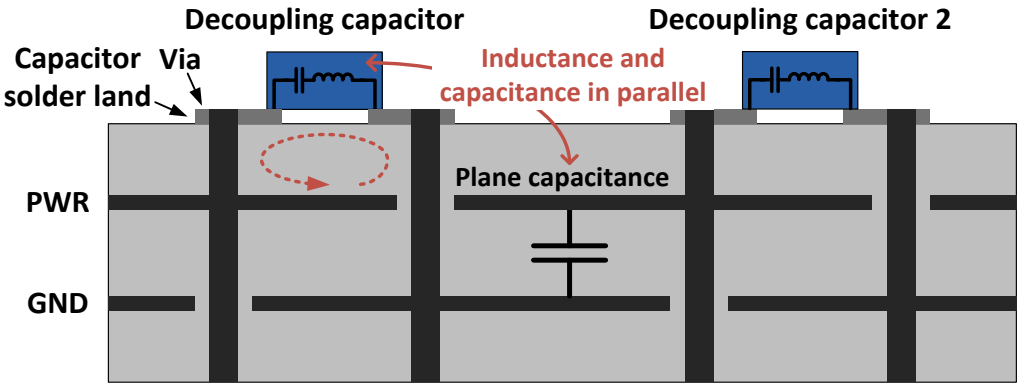
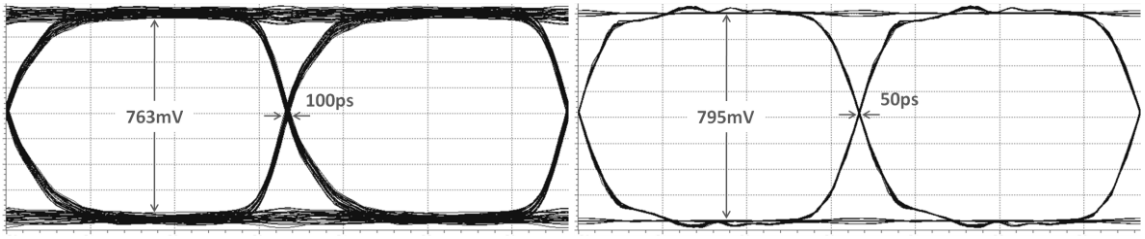


Figure 4.17 Surface mount capacitor connected to the power/ground planes.

On the other hand, a decoupling capacitor added to the PTL is not expected to function as a current path between the power and ground supply network. The decoupling capacitor serves as a charge reservoir to respond to a sudden demand for current. If the decoupling capacitor is placed near the device, the ESL becomes the dominant inductance in the path of current supply from the capacitor. As long as the inductance is less than a minimum value that begins to seriously impede the current supply, the ESL does not have much effect on the waveform in the PTL-based structure. This was shown in the previous measurement results, as in Figure 4.13 and Figure 4.14. By using PTL, the plane cavity was removed along with the power plane so that the interaction between the plane capacitance and the ESL could be prevented, which resolves the limitation of using

decoupling capacitor in the power-plane-based structure.

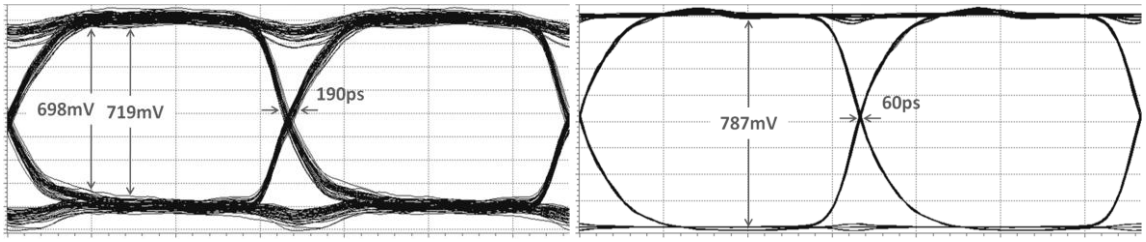
This can be demonstrated using SPICE simulations as well. The TV used in the previous section is employed. The series termination of the signal transmission line is 200 ohms. In Figure 4.18, the eye diagrams of 300 Mbps balanced data measured at the output of the signal transmission line are shown. In this case, an ideal decoupling capacitor of 0.1 μF is added to the PDN. The eye diagram of the power-plane-based TV has reduced voltage and timing margins, but the shape itself is the same with that of the PTL-based TV.



(a) **(b)**

Figure 4.18 Simulated eye diagrams of balanced data (R_S=200ohm and C_{Decap}=0.1uF) (a) Power-plane-based TV. (b) PTL-based TV.

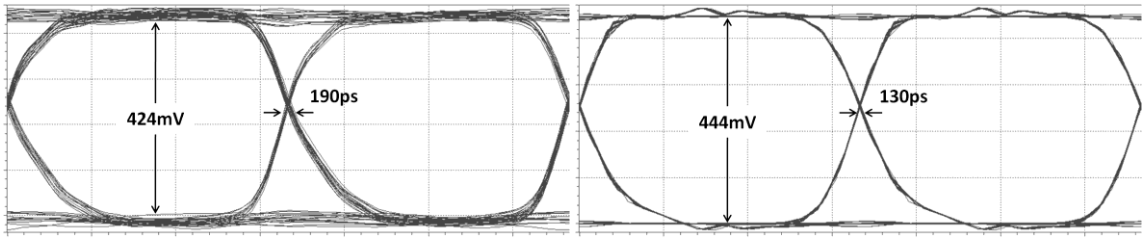
In Figure 4.19, the eye diagrams after adding the ESL of 2 nH are shown. The eye diagram of the power-plane-based TV is shown in Figure 4.19(a). It is affected by the ringing coming from the interaction between the parasitic inductance and the plane capacitance. The eye height and p-p jitter are 719 mV and 190 psec, respectively. The eye height is reduced by 6% due to the parasitic inductance of 2 nH as compared to Figure 4.18(a). On the other hand, the eye diagram of the PTL-based PDN in Figure 4.19(b) maintains almost the same eye opening as that without the parasitic inductance (Figure 4.18(b)). The eye height and width are 787 mV and 60 psec. As compared to the power-plane-based scheme, the eye height is improved by 9%, and the p-p jitter is reduced by 68% by using PTL (Figure 4.18). These simulation results indicate one more advantage for using PTL for power distribution namely, less susceptibility towards the ESL of the decoupling capacitor.



(a) **(b)**

Figure 4.19 Simulated eye diagrams of balanced data (R_S=200ohm, C_{Decap}=0.1uF and ESL=2nH) (a) Power-plane-based TV. (b) PTL-based TV.

As the series resistance of the signal transmission line is increased, the shape distortion of the eye diagram of the plane-based TV becomes more serious. Here, an example with R_S = 450 ohm is presented as well. When an ideal decoupling capacitor is added, the eye diagram of the plane-based TV is similar with that of the PTL-based TV except that the voltage and timing margins are reduced, as shown in Figure 4.20.

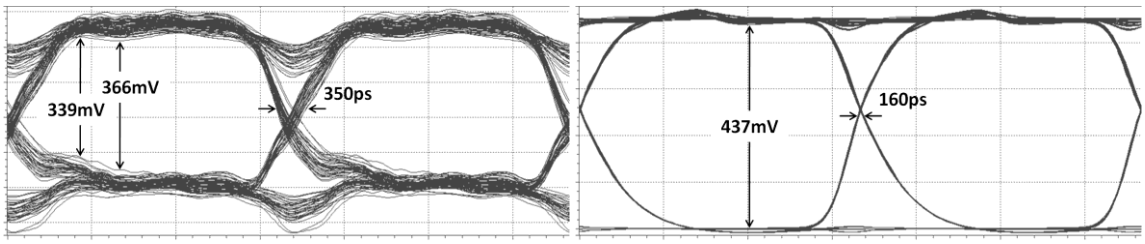


(a) **(b)**

Figure 4.20 Simulated eye diagrams of balanced data (R_S=450ohm and C_{Decap}=0.1uF) (a) Power-plane-based TV. (b) PTL-based TV.

However, with an ESL of 2 nH, the shape distortion occurs on the eye diagram of the plane-based TV, reducing the eye height from 424 mV to 366 mV, as shown in Figure 4.21. This is because the voltage across the load termination of the signal line is reduced with the increased series termination. The voltage fluctuations coming from the RLC parallel circuit are maintained to be almost the same, but the signal-to-noise ratio is reduced, which leads to the degraded eye opening. On the other hand, the eye diagram of the PTL-based TV in Figure 4.21(b) maintains almost the same eye opening as that

without the parasitic inductance (Figure 4.20(b)). The eye height and p-p jitter are 437 mV and 160 psec. The eye height is improved by 19%, and the p-p jitter is increased by 54%, as compared to Figure 4.21(a).



(a) **(b)**

Figure 4.21 Simulated eye diagrams of balanced data (R_S=450ohm, C_{Decap}=0.1uF and ESL=2nH) (a) Power-plane-based TV. (b) PTL-based TV.

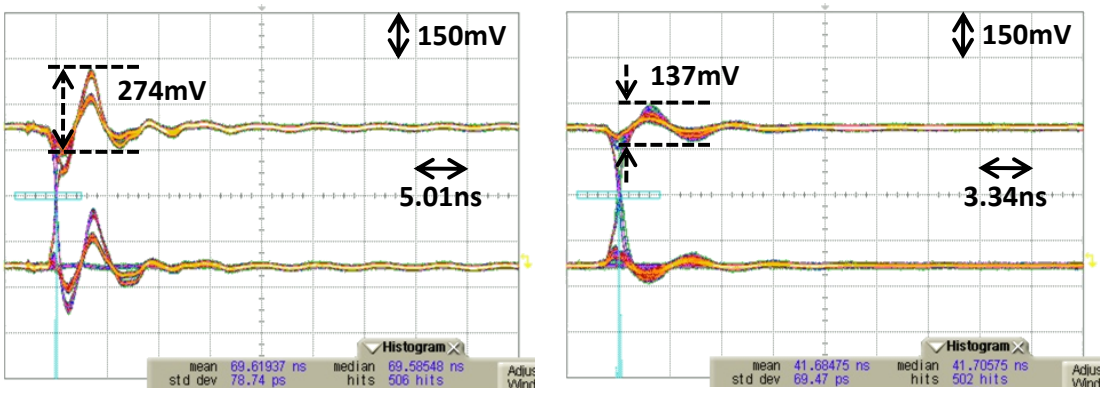
4.5 Additional Test Case: 4b6b PBPTL using Rs = 450ohm

The work in the previous section used a series termination of 200 ohms to limit the amount of current through the I/O driver. In this section, an increased resistance of 450 ohms was used to reduce the current load of the driver further; the reduction ratio increased from one fifth to one tenth. The same TVs shown in Figure 4.4 and Figure 4.5 were used. Using a larger resistance for series termination reduces the peak-to-peak value of the ringing. However, the eye height at the output of the channel is reduced further. The signal-to-ringing ratio is degraded in TV1 so that the advantage of using PTL is emphasized.

A decoupling capacitor of 0.1 μF was added near the power supply pin of the device along with an ESL of 2 nH in series with the decoupling capacitor. First, the simulated eye diagram at Port10 is compared between the two TVs in Figure 4.21. The eye diagram of the power-plane-based TV is shown in Figure 4.21(a). It is largely affected by the ringing coming from the interaction between the parasitic inductance, decoupling capacitor, and plane capacitance. The shape of the eye diagram is distorted losing both the timing and voltage margins. The eye height and width are 366 mV and 350 psec,

respectively. On the other hand, the eye diagram of the PTL-based TV in Figure 4.21(b) has a larger eye opening. The eye height and p-p jitter are 437 mV and 160 psec, which is an improvement of 19% and 54%, respectively, as compared to Figure 4.21(a). The positive and negative noise peaks do occur during transitions, but the size of peaks is much smaller and the steady state is reached faster as compared to the power-plane-based case.

The test environment is the same with that of the previous section as well. In Figure 4.12, only the value of R_S has been changed to 450 ohm. The noise characteristics in the two different environments are compared in Figure 4.22. With the power-plane based PDN, the peak to peak size of the ringing is about 274 mV (Figure 4.22(a)). Until the ringing is damped, about 25 nsec is consumed. The ringing on the waveform of the PTL-based TV is less severe, as shown in Figure 4.22(b). The voltage difference between the positive and negative noise peaks is about 137 mV, and the time until the ringing is damped is less than 10 nsec. Using larger resistance for series termination, the peak-to-peak value of the ringing was suppressed. However, the eye height at the far end of the signal transmission line was reduced further. The signal-to-ringing ratio was therefore degraded in the power-plane-based TV, highlighting the advantage of using PTL.



(a) **(b)**

Figure 4.22 Noise characteristic with R_S=450ohm. (a) Plane-based TV. (b) PTL-based TV.

The measured eye diagrams at the output of the 8-inch long signal transmission line (Port10) are compared in Figure 4.23. The target data rate is retained to be 300 Mbps. For the inputs to the octal driver, 300 Mbps 6-bit balanced data are applied. Figure 4.23(a) shows the output waveform of the ATE. The eye diagram at the receiver side of the power-plane-based TV is shown in Figure 4.23(b). It is seriously deteriorated with positive and negative noise peaks. As the period of input data is shorter than the duration of ringing, the excessive ripples dictate the eye opening. As compared to using a 200 ohm resistor as a series termination, the influence of the ringing on the waveform has increased. Using a larger resistor for a series termination, the peak to peak size of the ringing is reduced, however the eye height at the far end of the signal transmission line is reduced further. As a result, the ratio between the ringing and the eye height is degraded in the plane-based TV. The eye height is 208 mV, and the p-p jitter is 1169 psec. In Figure 4.23(c), the eye diagram of the PTL-based TV is shown. The eye height is 390 mV, which is an improvement of 87.5% when compared to that of the plane-based TV. The p-p jitter is 617.7 psec, which is a reduction of 47.2%. As expected from the noise characteristic, the ringing has much less influence on the eye diagram of the PTL-based TV.

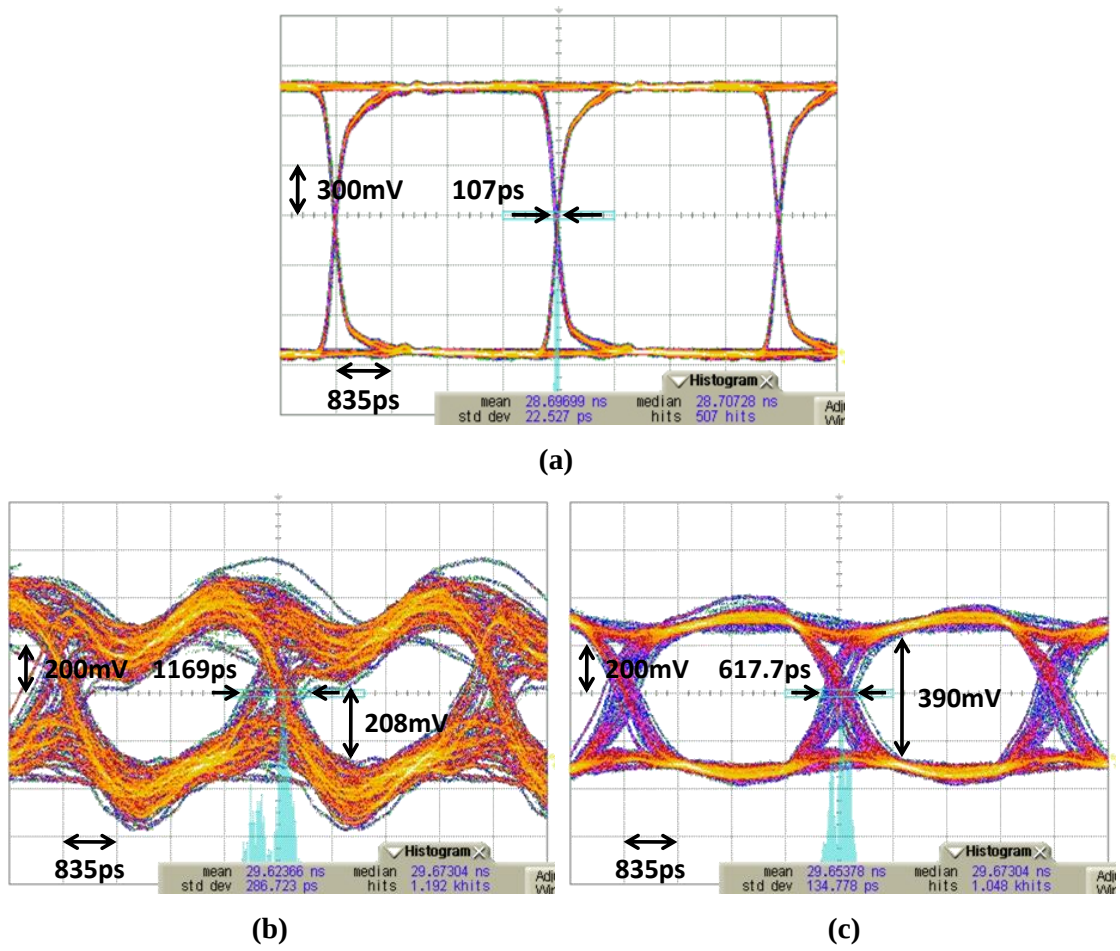
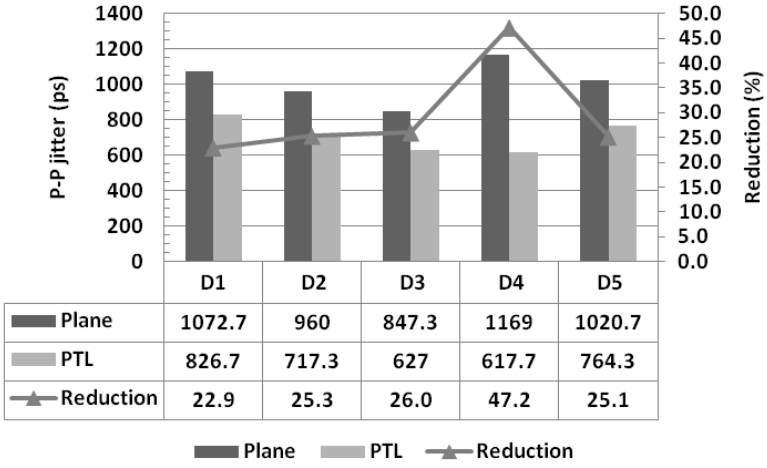
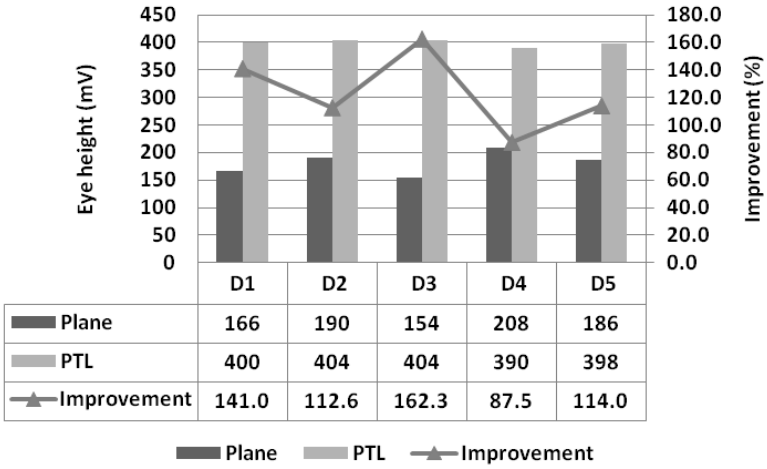


Figure 4.23 Measured eye diagrams of the received 300Mbps pseudo-balanced data. (a) Signal generator. (b) Plane-based test vehicle. (c) PTL-based test vehicle.

The p-p jitters and eye heights for all five signal lines are summarized in Figure 4.24. The dark grey bar in Figure 4.24(a) is the amount of p-p jitter measured at the far end of each channel of the power-plane-based TV, and that in Figure 4.24(b) is the eye height, while the light grey bars represent the amount of p-p jitter and the eye height of the PBPTL-based TV. The improvement by using the PTL is shown by solid lines. The reduction rate in p-p jitter by using PTL is at least 22.9%, and at most 47.2%. The improvement in terms of eye height ranges from 87.5% to 162.3%. Using a PBPTL reduced the p-p jitter by 29.3% and improved the eye height by 123.5% on average compared to using a power plane, as summarized in Table 4.4.



(a)



(b)

Figure 4.24 Comparison p-p jitter and eye height between the power-plane-based and PTL-based TV. (a) P-P jitter. (b) Eye height.

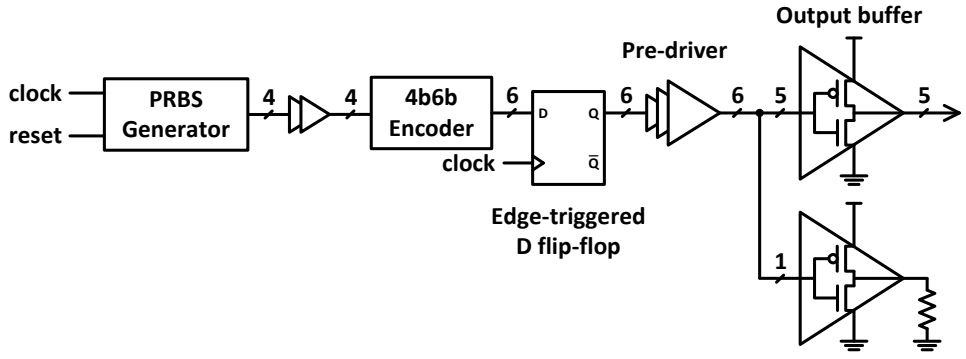
Table 4.4 Comparison of eye openings.

300Mbps	Eye height (mV)			P-P jitter (psec)		
	Plane	PTL	%△	Plane	PTL	%Δ
D1	166	400	+141	1072.7	826.7	-22.9
D2	190	404	+112.6	960	717.3	-25.3
D3	154	404	+162.3	847.3	627	-26
D4	208	390	+87.5	1169	617.7	-47.2
D5	186	398	+114	1020.7	764.3	-25.1
Avg.	180.8	399.2	+123.5	1013.9	710.6	-29.3

4.6 Measurement Results with Custom-Designed Transmitter

A transmitter for the proposed PBPTL scheme is custom-designed and fabricated in a 0.18 μm CMOS process. In Figure 4.25(a), a PRBS generator supplies 4-bit PRBS data to the 4b6b encoder. The encoder maps 4-bit information onto 6-bit symbols with an equal number of 1s and 0s, as shown in Table. The resulting balanced 6-bit data are sampled at the rising edge of the clock signal by the edge-triggered D flip-flop. Therefore, the transition edges of the six signals are timing-aligned with the clock signal. The synchronized and balanced 6-bit data are used to drive the output buffers. Figure 4.25(b) and Figure 4.25(c) show the output buffers used for the power-plane-based and PTL-based TVs, respectively.

The COB assembly technology is used to directly mount the die on the board and provide electrical interconnects using wire bonding. The transmitter is tested with 81-mm long trace on the FR4 board. One board has a pair of 140 mm by 93 mm planes with 0.7 mm FR4 dielectrics to be used as power and ground planes (TV1), while the other board has a 66-mm long source-terminated transmission line with 0.7 mm FR4 dielectrics to be used as a PTL (TV2).



(a)

Figure 4.25 (a) Block diagram for 4b/5b pseudo-balanced signaling. (b) Output buffer for plane-based TV. (c) Output buffer for PTL-based TV.

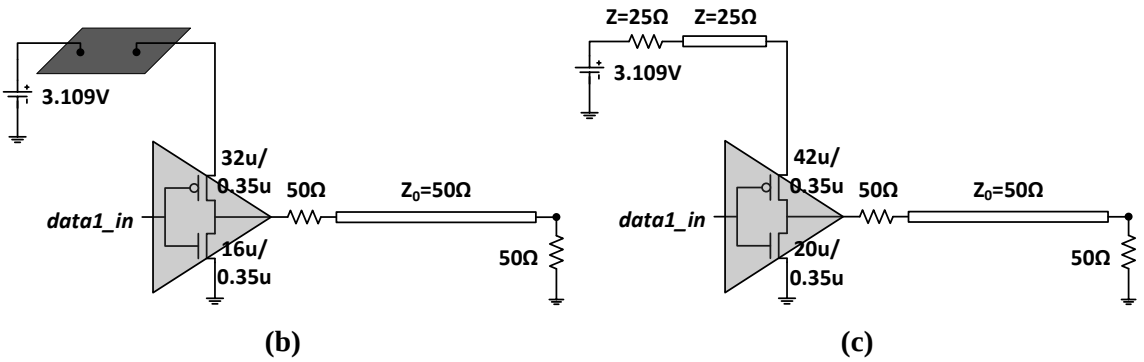
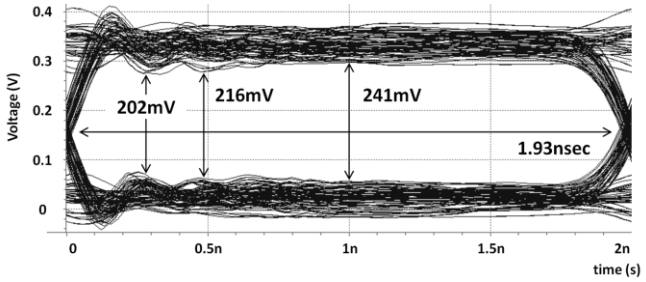
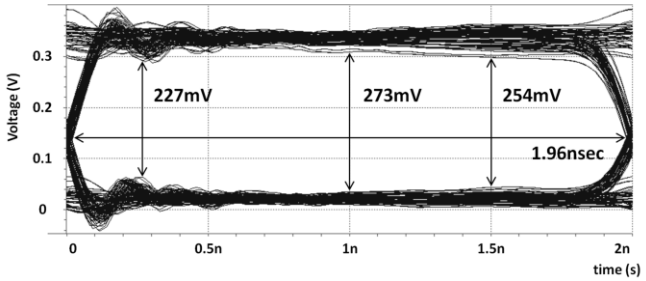


Figure 4.25 Continued.

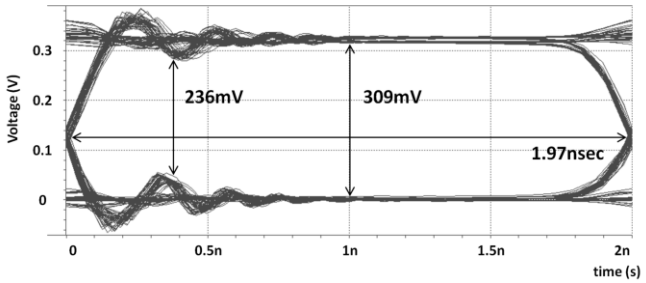
The SPICE simulation is first performed using a macromodel. Figure 4.26 shows the simulation results. The eye diagrams are constructed using the data samples at the output of the signal transmission line. The input data rate is 500 Mbps. Figure 4.26(a) and Figure 4.26(b) show the eye diagrams of the PRBS and pseudo-balanced data for the power-plane-based TV. The transmitter for the 4-bit PRBS data includes the PRBS generator, the pre-drivers, and the output buffers, while the 6-bit balanced data are generated and transmitted by the transmitter shown in Figure 4.25(a). As the input data becomes balanced, the fluctuations on the power and ground voltage rails are suppressed, which leads to the increased voltage and timing margins by 13% and 43%, respectively. Replacing the power plane with a PTL leads to the further improvement in the eye opening, as shown in Figure 4.26(c). The PBPTL scheme increases the eye height by 13% and decreases the p-p jitter by 25%.



(a)



(b)



(c)

Figure 4.26 Simulated eye diagrams. (a) Power-plane-based TV using PRBs data. (b) Power-plane-based TV using pseudo-balanced data. (c) PTL-based TV using pseudo-balanced data.

Figure 4.27 shows the test setup and environment. An Agilent 81133A signal generator was used to provide a clock signal of the desired frequency. For TV1, a supply voltage of 3.11 V was delivered to the I/O circuits through power/ground planes. For TV2, a 25 ohm transmission line was used to feed the same supply voltage of 3.11 V to I/O circuits, sharing a reference ground plane with signal transmission lines. A supply voltage of 1.8 V was used for core circuits of both TVs. Only the I/O PDN is differentiated. Each output buffer drives a 66-mm long transmission line. The signal

transmission lines are both series- and parallel-terminated by 50 ohms. The eye diagram is measured at the output of the 1st signal transmission line after the signal has travelled a distance of 66 mm, using an Agilent 86100C oscilloscope, which provides a parallel termination as well. For the other signal transmission lines, a parallel termination of 50 ohm is used at the far end of each signal transmission line through an SMA connector.

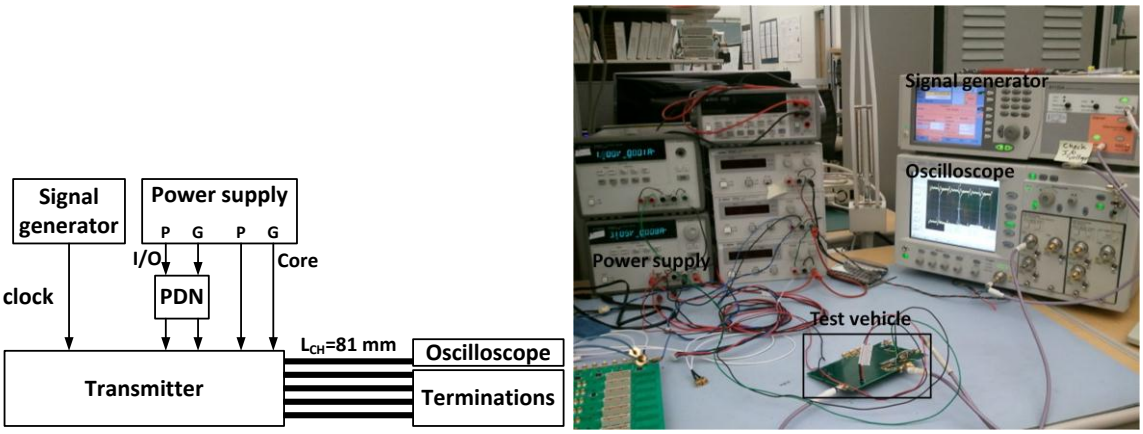


Figure 4.27 (a) Test environment. (b) Actual setup.

Figure 4.28 shows the measurement results. Three different input data rates are used: 100, 300, and 500 Mbps. The eye diagrams of TV2 have small overshoots, which are caused by the impedance discontinuity and mismatch. Those overshoots occur at similar times in a similar fashion on the eye diagrams of TV1. However, they are aggravated due to the RPD-induced voltage fluctuations on the power and ground voltage rails. The eye height decreases with an increase in data rate.

For 100 Mbps, the eye diagram of TV2 has 29% larger eye height and the same p-p jitter as compared to that of TV1 (Figure 4.28(a) vs. Figure 4.28(b)). As the data rate goes up to 300 Mbps, the power and ground voltage rails become noisier, which affects the waveform of TV1 more severely. The eye height of TV1 is 179.5 mV and the p-p jitter is 124 psec at the 50% output swing level, as shown in Figure 4.28(c). Since the crossing point has shifted, the minimum p-p jitter is measured to be 84 psec at the lower voltage

level. The eye height of TV2 is 241.5 mV, which shows an improvement of 35% (Figure 4.28 (d)). The p-p jitter measured at the 50% level is 142 psec, but the minimum value is 84 psec. For 500 Mbps, the resulting eye diagrams of TV1 and TV2 are shown in Figure 4.28(e) and Figure 4.28(f), respectively. The shape of the eye diagram is distorted in both cases. The decreased slew rate causes the duty cycle distortion and increases the p-p jitter. Especially, for TV1, the voltage fluctuations cause the big loss of the voltage margin, reducing the eye height to 159 mV (Figure 4.28(e)). The eye diagram of TV2 has an eye height of 215 mV, which shows an improvement of 35% (Figure 4.28(f)). The p-p jitter is improved by 42% by using PTL. The eye height and p-p jitter of each TV at each data rate are summarized in Table 4.5.

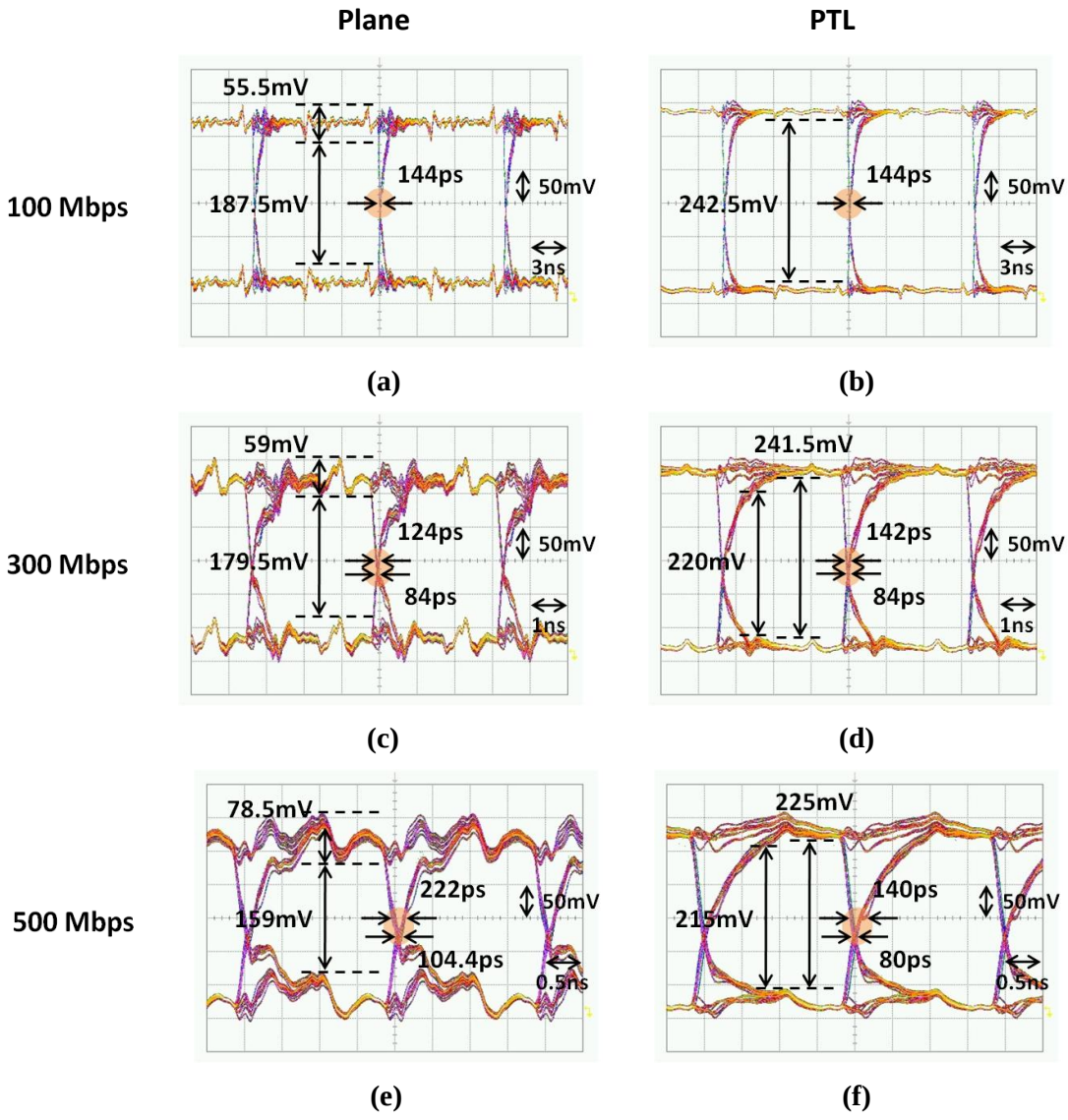


Figure 4.28 Measured eye diagrams. (a) 100 Mbps in TV1. (b) 100 Mbps in TV2. (c) 300 Mbps in TV1. (d) 300 Mbps in TV2. (e) 500 Mbps in TV1. (f) 500 Mbps in TV2.

Table 4.5 Comparison of eye openings.

	Eye height (mV)			P-P jitter (psec)		
	Plane	PTL	%△	Plane	PTL	%Δ
100 Mbps	187.5	242.5	+29	144	144	-
200 Mbps	179.5	220	+23	84	84	-
300 Mbps	159	215	+35	104.4	80	-23

Figure 4.29 shows the chip microphotograph. The active area of both the PB plane-based scheme and the PBPTL scheme is 1.51×10^{-2} mm^2, which includes the PRBS generator, the encoder, the pre-drivers, and the output buffers. The area devoted to the encoder equals 3.29×10^{-3} mm^2, which is 22% of the transmitter area.

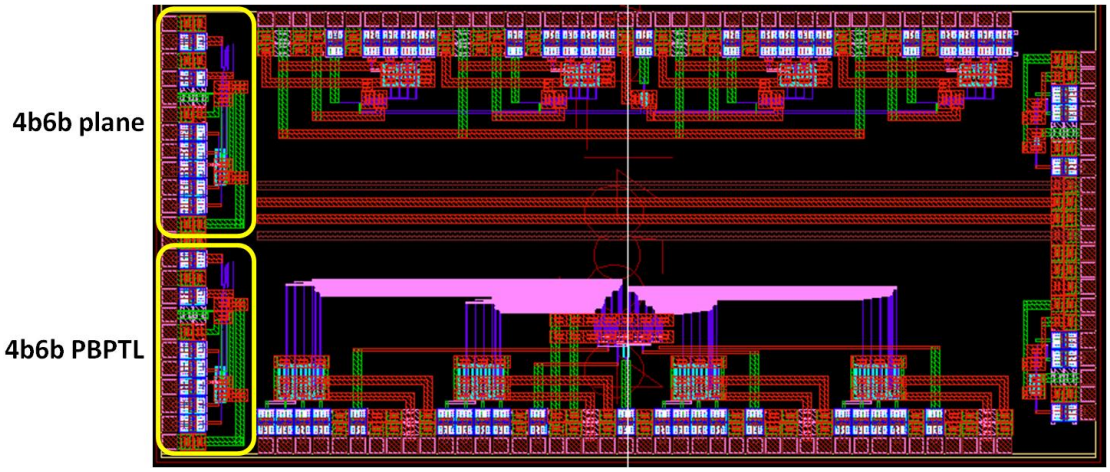


Figure 4.29 Chip layout of the PB plane scheme and the PBPTL scheme.

4.7 Summary

To remove the dynamic DC drop and impedance mismatch effect, the CCPTL scheme has been proposed in the previous research. The CCPTL scheme induces constant current through the PTL, and thus doubles the power consumption. To reduce the power penalty, the pseudo-balanced signaling scheme is proposed. In the case of 4-bit transmission, the PBPTL scheme reduces the overhead in power consumption by 50% as compared to using the CCPTL scheme. In this paper, proof of concept for the PBPTL-based approach is presented. Using PBPTL addresses the issues raised by PTL, which are the dynamic DC drop and the impedance mismatch effect. At the same time, it resolves the RPD issue and reduces the layer count.

Two sets of test vehicles are used. The test vehicles using an octal driver provide a preliminary demonstration of the PBPTL scheme. The simulation and measurement

results indicate that PTL outperforms power plane in terms of power distribution for both PRBS and balanced data. With R_S = 200 ohm, using PBPTL reduces the p-p jitter by 10.5% and improves the eye height by 34.8% on average, as compared to using the power plane with the pseudo-balanced signaling scheme. One more test case is included, in which R_S equals 450 ohm. Using the larger series termination degraded the eye diagrams of the plane-based TV further, which accordingly increased the improvement rate in signal integrity induced by using PTL. To demonstrate the effectiveness of the PBPTL scheme further, test vehicles using a custom-designed transmitter are implemented. The eye diagram is measured at the output of the 8-inch long transmission line, and compared between the power-plane-based and PTL-based test vehicles. The measurement results validate the effectiveness of the PBPTL step by step. The performance improvement by replacing the power plane with the PTL is presented, and the experimental results of using the balanced data instead of the PRBS data follow. The PBPTL the pseudo-balanced signaling scheme is applied to the PTL-based TV to ascertain the merit of the PBPTL scheme, which yields a significant improvement in signal integrity.

CHAPTER 5

CONSTANT VOLTAGE POWER TRANSMISSION LINE

5.1 Introduction

As discussed in Chapter 3, the source-terminated power transmission line (PTL) suffers from the dynamic dc drop on the power supply network. The dynamic characteristic of the voltage drop depends on the state of the data that drives the output buffer. In the case of a voltage-mode driver and ground-tied termination, the high state of the output data induces current to flow through PTL, while the low state of the output data stops the current flow. Thus, only during the high state, a dc drop occurs across the power supply path, and only a fraction of the supply voltage appears at the power supply pin of the driver. The amount of the dc drop depends on the impedance ratio between the power delivery network (PDN) and the signal network. If the load termination of the signal transmission line is tied to ground, the proportion of the PDN impedance to the power-to-ground impedance determines the supply voltage seen at the power supply pin of the driver during the high state of the output data.

When a single PTL is used to feed the supply voltage to multiple drivers, the dc drop issue worsens. In Figure 5.1(a), the PTL scheme for 2-bit transmission is shown. Two bits give four different patterns, which are LL, LH, HL, and HH (L stands for the low state, while H for the high state). In terms of the number of high state, there are three patterns, as indicated in the table in Figure 5.1(b). The input impedance of the signal network seen at the power supply pin changes based on the data pattern. Consequently, when a driver is turned on, the amount of current drawn by that driver is dictated by the states of the other drivers. In Figure 5.1(a), when *data1_tx* is in high state, the turned-on driver draws current from the power supply, whose amount depends on the state of *data2_tx*. If

data2_tx is in high state, the resulting voltage level at the power supply pin becomes 1.875 V, or else it becomes 1.5 V, as shown in Figure 5.1(b). The amplitude of the waveform at the input and output of the signal transmission line also varies with the number of high states. When *data1_tx* is in high state, the amplitude of the signal can be either 1 V or 1.25V. If *data2_tx* is in high state, the amplitude of both *data1_tx* and *data2_tx* equals 1 V. Otherwise, the amplitude of *data1_tx* equals 1.25 V. Not having uniform amplitude during the high state can have a similar effect as voltage fluctuations on the power plane, inducing larger jitter and degrading signal integrity.

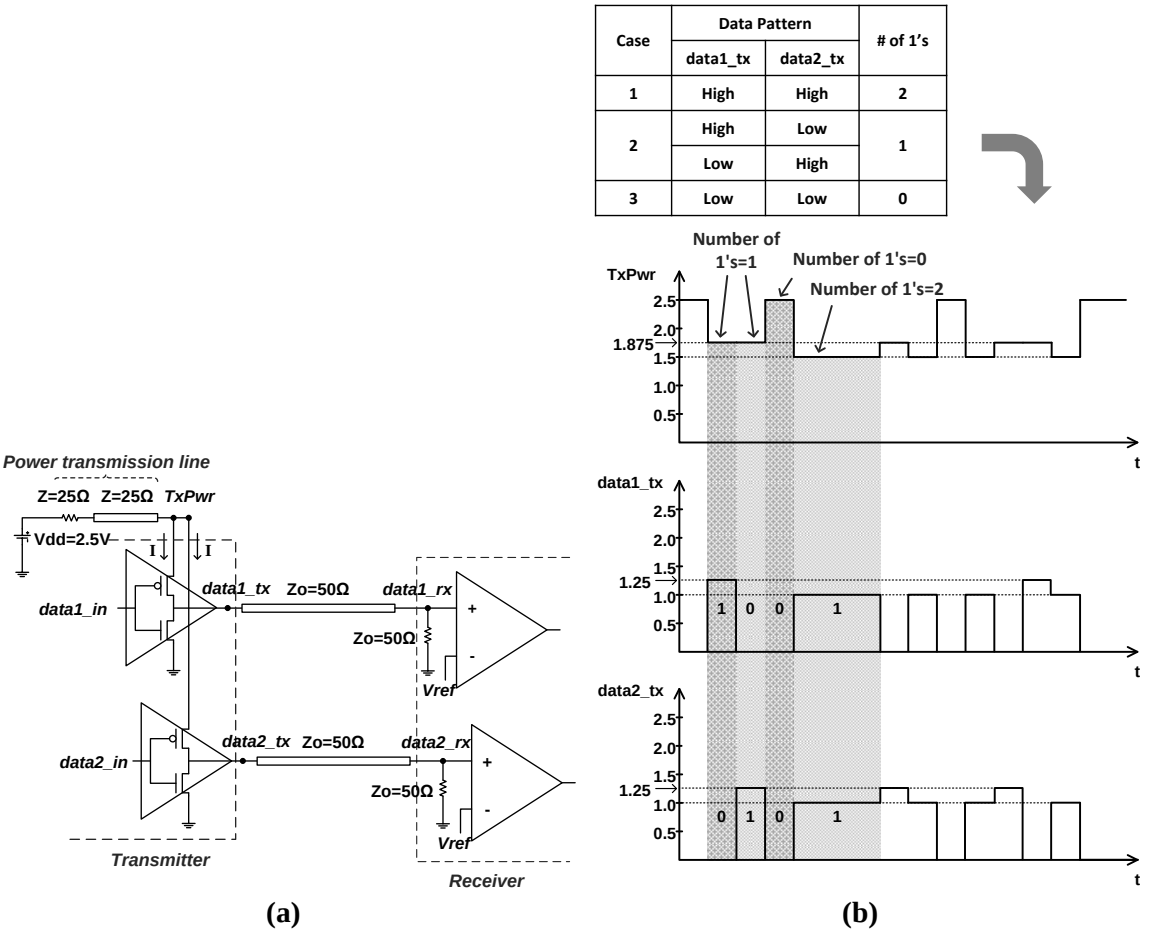


Figure 5.1 Two I/O drivers per PTL. (a) Schematic. (b) Waveforms.

As explained in Chapter 3, the constant current PTL (CCPTL) scheme uses dummy paths to resolve the dc drop problem and the impedance mismatch issue associated with

the PTL. It is demonstrated using both simulations and measurements that constant current through the PTL provides the desirable results. First, the data-pattern-dependent dc drop is eliminated so that the voltage at the power supply pin and the amplitudes of the signals become constant regardless of the data pattern. Moreover, the impedance mismatch effect between the PTL and source termination is alleviated; constant current keeps the PTL fully charged so that the PTL behaves as a constant resistive load.

The limitation of the CCPTL scheme lies in its power consumption. The CCPTL scheme consumes twice as much power as the conventional PDN when the same power supply voltage is used and the same eye height is targeted. As an example, the static power consumption for 4-bit transmission is compared between the power plane scheme and the CCPTL scheme in Table 5.1. The power consumption of the PBPTL scheme is also included to show the reduced power penalty than that of the CCPTL scheme. Still, it consumes 50% more power than the power plane scheme. The dynamic power consumption is not shown because the same amount of consumption is expected for both schemes. To address the increased power penalty issue and reduce the power overhead further, an alternate PTL scheme is proposed in this chapter.

Table 5.1 Static power consumption for 4-bit transmission.

PDN type	Eye height	Power consumption *					Expectation of Power	Power penalty
		HHHH	HHHL	HHLL	HLLL	LLLL		
Power Plane	$V_{DD}/2$	4	3	2	1	0	2	-
CCPTL	$V_{DD}/2$	4	4	4	4	4	4	100%
PBPTL	$V_{DD}/2$	3	3	3	3	3	3	50%
Probability		0.0625	0.25	0.375	0.25	0.0625		

*** It is assumed that when one output buffer draws current from the power supply, power of 1 is consumed.**

5.2 Constant Voltage Power Transmission Line (CVPTL)-Based PDN

The Constant Voltage PTL (CVPTL) scheme is designed to induce current that is directly proportional to the number of turned-on I/O drivers [64]. To create such an environment, multiple resistor paths are implemented between the PTL and the power supply pin of the driver. The resistance of each resistor path is determined to satisfy the following two conditions: 1) the voltage at the power supply pin should be constant, and 2) the current through the PTL should be directly proportional to the number of turned-on I/O drivers. Based on the detected data pattern, a single resistor path is selected and activated. A change in the data pattern brings a corresponding change in the selected resistor path. The resistance of the power supply path is thus controlled to achieve a constant voltage at the power supply pin even with the varying amount of current through the PTL, which is why the new scheme is called as CVPTL. In the CVPTL scheme, the amount of current through the PTL varies with the data pattern, as opposed to the CCPTL scheme. If the number of turned-on drivers shifts from 1 to 2, the current through the PTL doubles so as to keep the amount of current supplied to the turned-on driver constant at all times.

Figure 5.2 shows an example of how The CVPTL scheme works for 2-bit single-ended signaling. Two bits provide three different data patterns based on the number of high state, which are HH, HL/LH, and LL. In the HH state, both drivers are connected to the PTL in parallel, each being supplied with current 'I'. The total current through the PTL then equals '$2\times I$,' and the input impedance of the signal network is '$(R+Z_0)/2$,' where R is the turn-on impedance of the driver and Z_0 is the characteristic impedance of the transmission line. The voltage at the TxPwr node equals '$I\times(R+Z_0)$.' In the HL state, one of the drivers is connected to the PTL drawing current, while the other driver is turned off. To supply the turned-on driver with current 'I' as in the HH state, a resistive path is connected between the output of the PTL and the power supply pin of the driver.

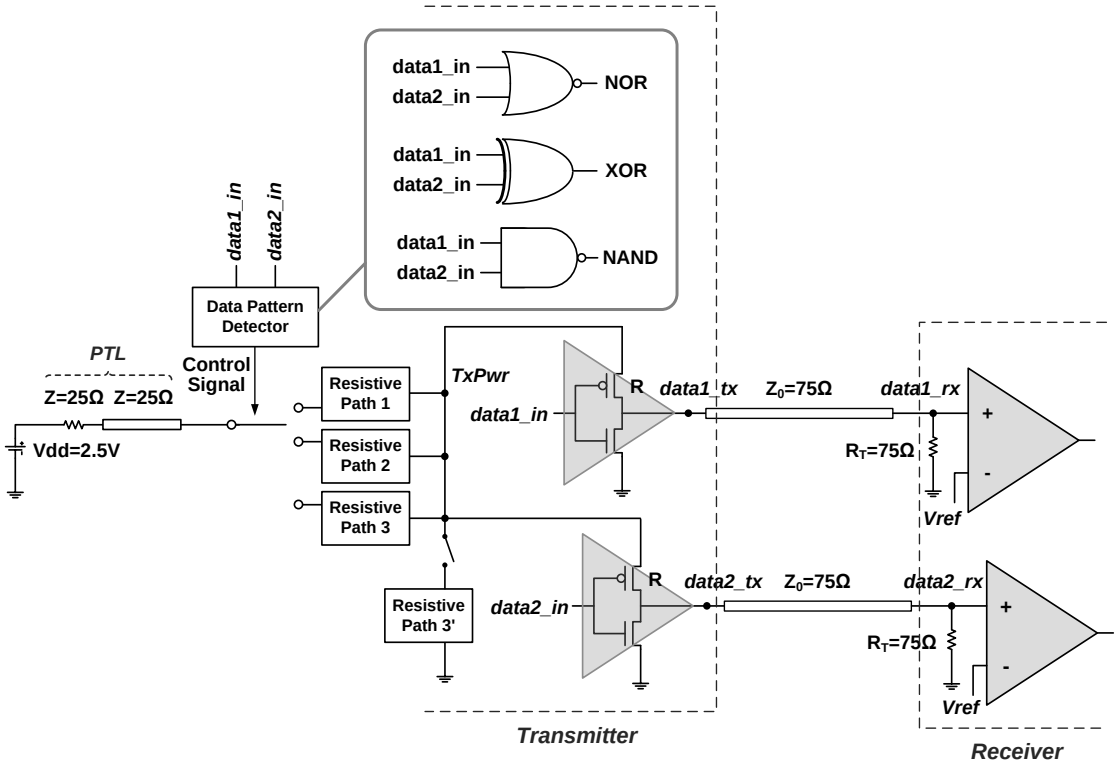
As a results, the voltage of 'I×(R+Z_0)' is achieved at the TxPwr node, which is the same value as in the HH state. So far, the CVPTL scheme consumes the same amount of power with the conventional power plane scheme. In the LL state, no current flows in the conventional PDN scheme. However, the CVPTL scheme draws a certain amount of current to maintain the same voltage level at the power supply node constant regardless of the data pattern. The state of the highest probability among all possible states is the HL state, as shown in Table 5.2, which is based on rough calculations. Accordingly, a dummy path is used to draw current 'I,' which is the amount of current through the PTL in the HL state. Therefore, the power required to transmit 2-bit data using the CVPTL scheme is larger than using the conventional power plane due to the power consumed in the LL state. If the same power supply voltage is used and the same eye height is targeted, the power overhead coming from the CVPTL scheme is 25% for 2-bit transmission, as shown in Table 5.2.

Table 5.2 Comparison of power consumption.

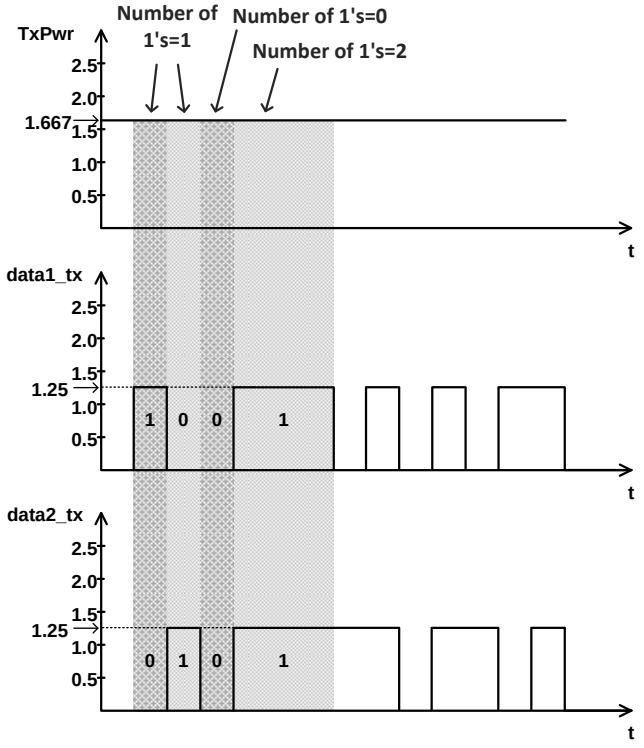
Patterns of 2-bit data	HH	HL/LH	LL	Expected value of power consumption
Probability	0.25	0.5	0.25	
Power plane	2P	P	0	P
CVPTL	2P	P	P	1.25P

In Figure 5.2, the supply voltage equals 2.5 V. The characteristic impedances of the PTL and signal transmission line are 25 ohm and 75 ohm, respectively. The turn-on impedance of the driver is designed to be 50 ohm. The data pattern detector detects the number of high states among the input data string and selects the corresponding resistive path. If both output data are in high state, the data pattern detector selects the first resistive path (Path1). Both drivers are supplied with the current of 16.7 mA. The resulting eye height at the output of each signal transmission line is one-half of the supply voltage. The total amount of current through the PTL equals 33.4 mA. The resistance of

Path1 is 0, and the dc drop across the PTL is 0.83 V. In the 2nd case where the output data are in either the HL state or the LH state, only the turned-on driver draws the current of 16.7 mA from the PTL, resulting in the same eye height of 1.25 V. The amount of current through the PTL is reduced by half, as compared to that in the 1st case. The resistance for Path2 becomes 25 ohm, which results in the dc drop of 0.83 V across the PTL. In the 3rd case where the output data are in the LL state, no driver draws current from the PDN. Thus, the resistive Path3 connects the output of the PTL and the power supply pin, while the resistive Path3' serves as a dummy path. To keep the voltage level at the TxPwr node constant, Path3 and Path3' are designed to induce current to flow through the PTL. The role of the resistive paths is similar to the dummy path in the CCPTL scheme. As the voltage is divided in proportion to the resistance values of Path3 and Path3', they are determined to keep the voltage at the TxPwr node constant at 1.667 V: R_{Path3} equals 25 ohm, and $R_{Path3'}$ equals 100 ohm. The additional power consumption is induced by the induced current flow in the 3rd case. As stated above, taking the probability of each data state into account, the power required to transmit 2-bit data using the CVPTL scheme increases by 25%, as compared to the conventional power plane.



(a)



Case	Input data		I_{PTL}
	data1_in	data2_in	
1	0	0	2I
2	0	1	I
	1	0	
3	1	1	I

(b)

Figure 5.2 Two I/O drivers per CVPTL. (a) Schematic. (b) Waveforms.

5.3 Simulation Results

Figure 5.3 shows two simulated structures. The first structure uses a pair of 42 mm by 30 mm planes with 0.2 mm-thick FR4 dielectric as power and ground planes to supply power to drivers, as shown in Figure 5.3(a). The second structure employs a 4 mm-long transmission line along with an impedance-matching source termination as a PTL, as shown in Figure 5.3(b). For the PTL-based TV, both the CVPTL scheme and the CCPTL scheme are applied and compared. Each simulated structure includes two drivers whose outputs are connected to 37 mm-long transmission lines. A 1 Gbps PRBS (pseudo-random binary sequence) signal is used as input for each driver. Eye diagrams of the signals received at the output of the signal transmission lines (*d1_rx* and *d2_rx*) are presented in Figure 5.4, Figure 5.5, and Figure 5.6. The signal transmission lines of the plane-based TV and the PTL-based TV were modeled in frequency domain using Sphinx [51], respectively. Then, Advanced Design System (ADS) [80] was used to translate the frequency response of each structure into a time domain "black box" subcircuit so that other components such as drivers, terminating resistors, and voltage sources could be added for the time-domain simulation of the whole structure.

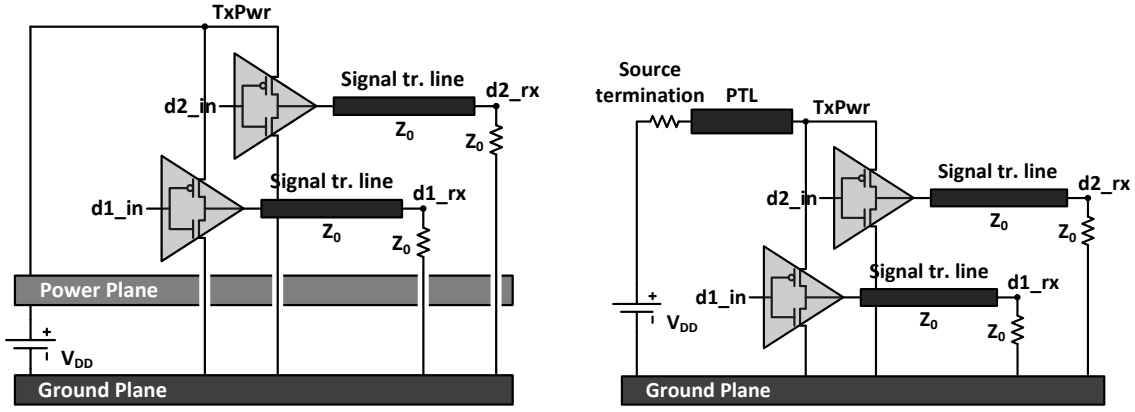
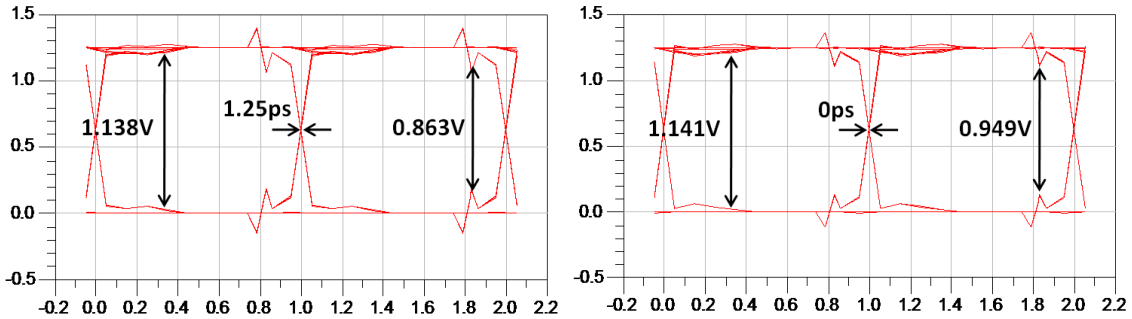


Figure 5.3 Simulated structures. (a) Power-plane-based. (b) PTL-based.

First, the eye diagrams of the CVPTL-based TV are shown in Figure 5.4. The eye height is 1.14 V on average, which is 91.2% of the target eye height. The peak-to-peak

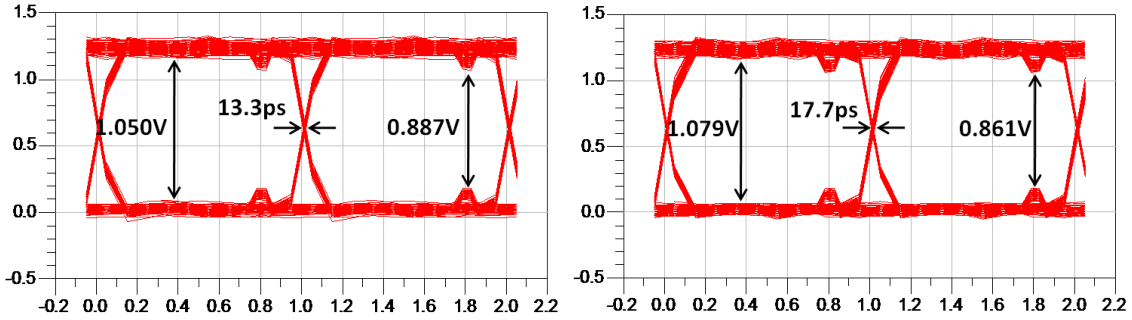
jitter is 0.6 psec on average. Here, the overshoot near the data transition is due to port discontinuity in 3D simulation.



(a) **(b)**

Figure 5.4 Eye diagrams of received data in CVPTL-based TV. (a) data1_rx. (b) data2_rx.

Figure 5.5 shows the eye diagrams of the power-plane-based TV. Apparently, the voltage fluctuations on the power and ground rails are severe due to the return path discontinuity (RPD) effects. The eye height is 1.065 V on average, which is 85.2% of the target eye height. The peak-to-peak jitter is 15.5 psec on average, which is 25.8% larger than that of the PTL-based structure.

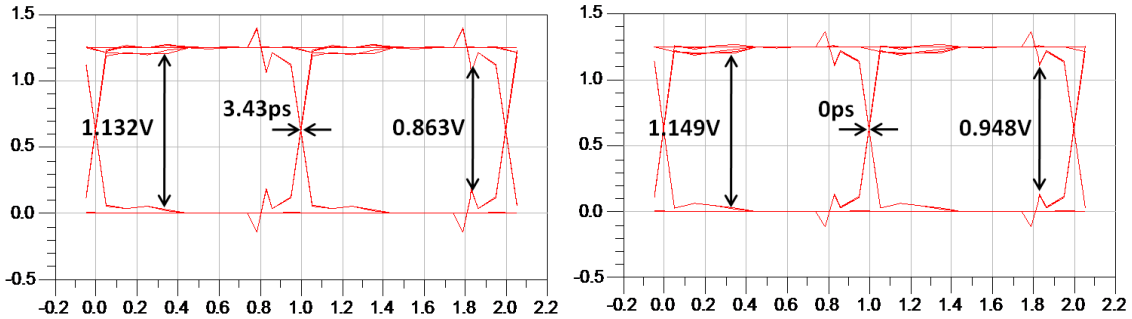


(a) **(b)**

Figure 5.5 Eye diagrams of received data in Power-plane-based TV. (a) data1_rx. (b) data2_rx.

The eye diagrams of the CCPTL-based TV are shown in Figure 5.6 for comparison. The eye height and p-p jitter are 1.141 V and 1.72 psec on average, respectively, which are comparable to those of the CVPTL-based TV. It can be concluded that the CVPTL

scheme reduces the power penalty while maintaining the timing and voltage margins the same as compared to the CCPTL scheme.



(a) **(b)**

Figure 5.6 Eye diagrams of received data in CCPTL-based TV. (a) data1_rx. (b) data2_rx.

The power consumptions along with eye heights and p-p jitters are compared in Table 5.3. For comparison of power consumption, it is assumed that the power 'P' is required in the power-plane-based structure when the target eye height is ½ of V_{DD}. The relative amount of power consumed by the CCPTL scheme is '2·P' due to constant current flowing through the PTL. The CVPTL scheme consumes 'P+α' when the eye height equals ½ of V_{DD}, where 'α' accounts for the power loss in the LL state. In the LL state, both drivers are turned off, not drawing any current in the power-plane-based structure. However, in the CVPTL-based structure, a certain amount of current flows through the PTL to keep the voltage at the power supply pin constant. For 2-bit transmission, 'α' equals 25% of P, while 'α' equals 12.5% of P for 4-bit transmission. The power penalty decreases with increase in the number of data bits, as shown in Figure 5.7. However, for 4-bit transmission, the target eye height is decreased, which is inevitable to implement the resistive paths in the supply current path.

Table 5.3 Comparison of power consumptions, eye heights and jitters.

PDN	Power consumption	Eye height (V)	Jitter at 1Gbps (ps)
Power plane	P	1.065	15.5
CCPTL	2·P	1.141	1.72
CVPTL	P+α	1.140	0.6

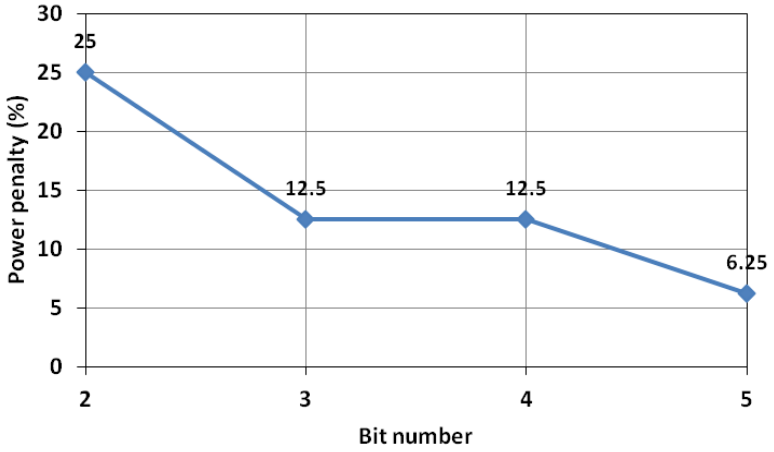


Figure 5.7 Bit number versus % power penalty graph

5.4 Additional Mismatch Effects

Varying the amount of current that flows through the PTL has its merits and demerits. While it reduces the power penalty, it introduces the potential for additional mismatch effect between the PTL and terminating resistor besides the possible mismatch effect between the signal transmission line and the terminating resistor. In Figure 5.8, the components that can induce the impedance mismatch are the load termination of the signal transmission line (R_T) and the source termination of the PTL (R_S). Resistance R_T can cause impedance mismatch in the signal transmission line, while resistance R_S can cause that in the PTL. Simulations have been performed to include variations in R_T of ±10% and R_S of ±20% to account for any manufacturing related effects. This has been done to illustrate the possible combinations of impedance mismatch effects coming from

the power and signal transmission lines. It is also possible that the resistance of PMOS or resistor path deviates from its nominal value. Since they serve as a source-side termination of the signal transmission line along with the PTL components, such deviations will have a similar effect on the eye diagram as R_S with variations. The percentage mismatch of ±20% assigned to R_S is larger than typical, but it has been used to include the mismatch effect coming from the PMOS and resistor path as well.

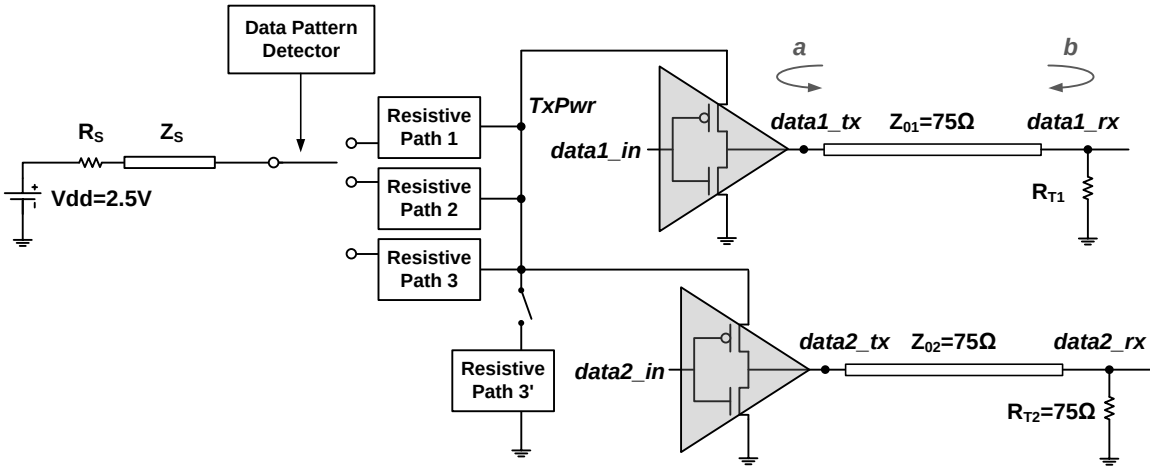


Figure 5.8 Mismatch inducible components in 2-bit I/O scheme with CV-PTL.

The eye height and jitter of each impedance-mismatched case are summarized in Table 5.4. Using the CVPTL scheme, susceptibility to impedance mismatch effect is increased, but the eye diagram of the CVPTL scheme is still larger and wider than that of the power plane scheme.

Table 5.4 Comparison of eye openings and jitters in various mismatch-included cases.

Load termination	%error	Source termination	%error	Eye height (V)				P-P jitter (ps) at 1Gbps			
				CVPTL		Power plane		CVPTL		Power plane	
				d1_rx	d2_rx	d1_rx	d2_rx	d1_rx	d2_rx	d1_rx	d2_rx
R_T	0%	R_S	0%	1.138	1.141	1.050	1.079	1.25	0	13.3	17.7
			-20%	1.177	1.182			8.87	8.87		
			+20%	1.101	1.104			0	4.43		
	-10%	R_S	0%	1.085	1.154	1.000	1.078	4.43	0	13.3	17.7
			-20%	1.116	1.178			8.87	8.87		
			+20%	1.037	1.102			0	4.43		
	+10%	R_S	0%	1.171	1.140	1.095	1.080	4.43	0	13.3	17.7
			-20%	1.210	1.178			4.43	8.87		
			+20%	1.133	1.105			8.87	0		

5.5 Extension to higher number of I/Os

The CVPTL scheme can be extended to more than 2-bit I/Os. For n-bit transmission, it requires ‘n+1’ resistor paths in parallel between the output of the PTL and the power supply pin. Since the possible number of high states in the output data string ranges from zero to n, the number of resistor paths equals ‘n+1’. The data pattern detector selects one resistor path at a time based on the number of high states. Then, each turned-on driver is supplied with the same amount of current in each case. Although the current through PTL varies with the data pattern, the voltage at the power supply pin (TxPwr) and the signal amplitudes at the input and output of the signal transmission line (data1_tx and data1_rx, and so on) should be invariant.

In Figure 5.9, an example of the CVPTL scheme for 4-bit transmission is presented. Four bits provide five different data patterns based on the number of high state regardless of order, which are HHHH, HHHL, HHLL, HLLL and LLLL. Five resistive paths that correspond to each data pattern are implemented. The first four resistive paths are designed to induce the same amount of current in each state as the power-plane-based

scheme. The fifth resistive path serves as a dummy path to induce current through the PTL in the LLLL state, which leads to additional power consumption.

As compared to the CVPTL scheme for 2-bit transmission, the complexity for implementation of the data pattern detector and resistive paths increases, but the power penalty is reduced to 12.5%.

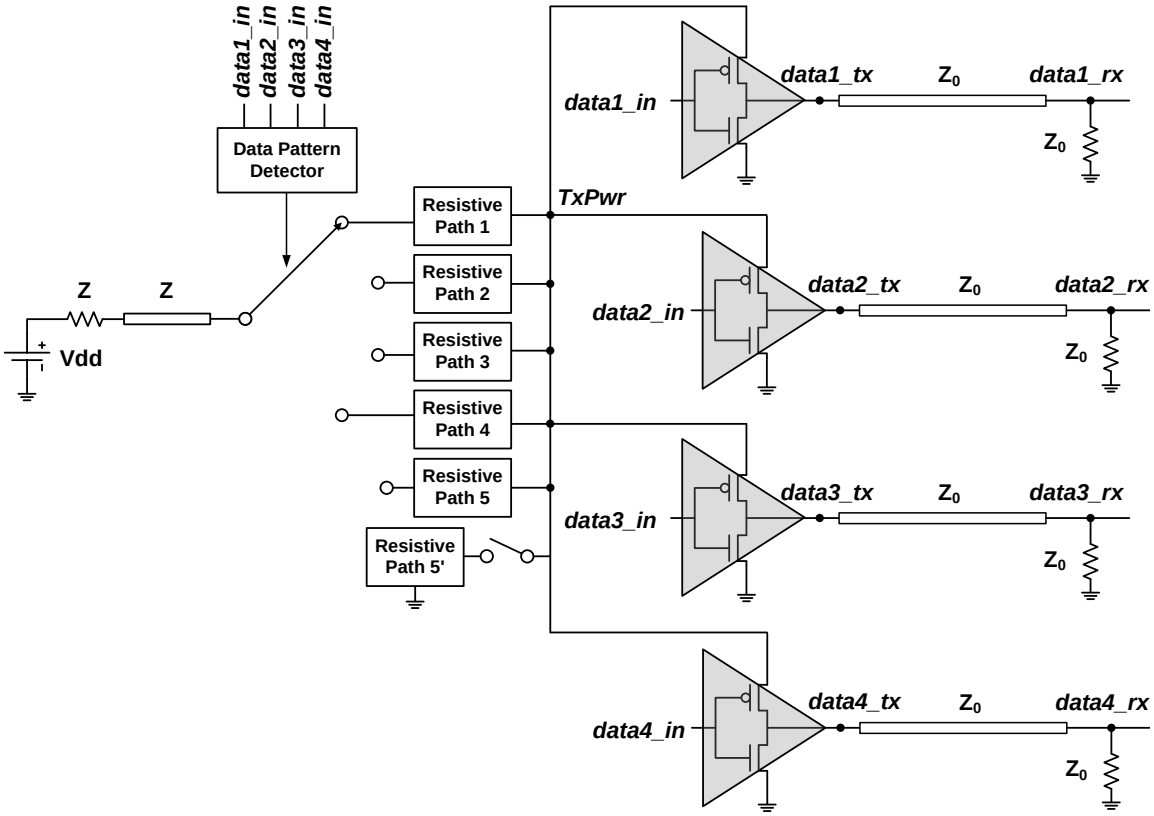


Figure 5.9 CVPTL scheme for 4-bit transmission.

5.6 Summary

The CVPTL scheme varies the amount of current through the PTL and the resistance of the power supply path based on the input data pattern. As a result, two desired effects are achieved. First, the supply voltage at the power supply pin of the driver becomes constant. Although the current through the PTL changes, the resistive path connecting the PTL and the power supply pin also changes accordingly to induce the same dc drop

across the power supply path. Second, the eye heights at the input and output of the signal transmission line are kept constant regardless of the input data pattern. Compared to CCPTL, the same waveforms are achieved with reduced power penalty (25% for 2-bit transmission and 12.5% for 4-bit transmission, instead of 100% for both cases). Without constant current, impedance mismatches or discontinuities in the power supply path have negative effects on the waveform, but the simulation results show that the CVPTL scheme still provides superior jitter performance and larger eye amplitude than the power plane scheme. The proposed scheme is effective when applied to two- or larger-bit single-ended signaling. The analysis of the proposed scheme is theoretical and simulation based only. Test vehicles can be fabricated to confirm the results as a part of future work.

CHAPTER 6

EFFECT OF POWER TRANSMISSION LINE ON DECOUPLING CAPACITOR PLACEMENT

6.1 Introduction

For off-chip signaling, the output buffers drive signal transmission lines and load termination. Charging the signal transmission line requires the current to be supplied through the power delivery network (PDN) during switching of the integrated circuit (IC), but in many cases the current cannot respond quickly to the sudden surge of current due to the high impedance of the voltage regulator module (VRM). Decoupling capacitors are used to increase the current capacity. They serve as charge reservoirs near the device so that the stored charge facilitates the supply of current when the current is demanded by the switching circuits. Decoupling capacitors also provide return current paths between the power and ground planes.

In addition to the previous two functions, decoupling capacitors are used to meet the target impedance at cavity resonances. At the cavity resonance frequencies, the plane impedance increases. To suppress the plane impedance, the impedance profile of the decoupling capacitor, which has the minimum impedance at the resonant frequency, is used [16]. The capacitor that resonates at the cavity resonance frequency has to be chosen. When such capacitors are placed where the impedance needs to be reduced, the impedance can be pulled down at the resonant frequency. However, it induces new anti-resonances caused by the parallel resonance between the equivalent series resistor (ESL) of the decoupling capacitor and the other capacitive components. To remove those anti-resonances, another capacitor is required. Therefore, the methodology for the placement of capacitors requires an iterative process, which can be complex and time-consuming.

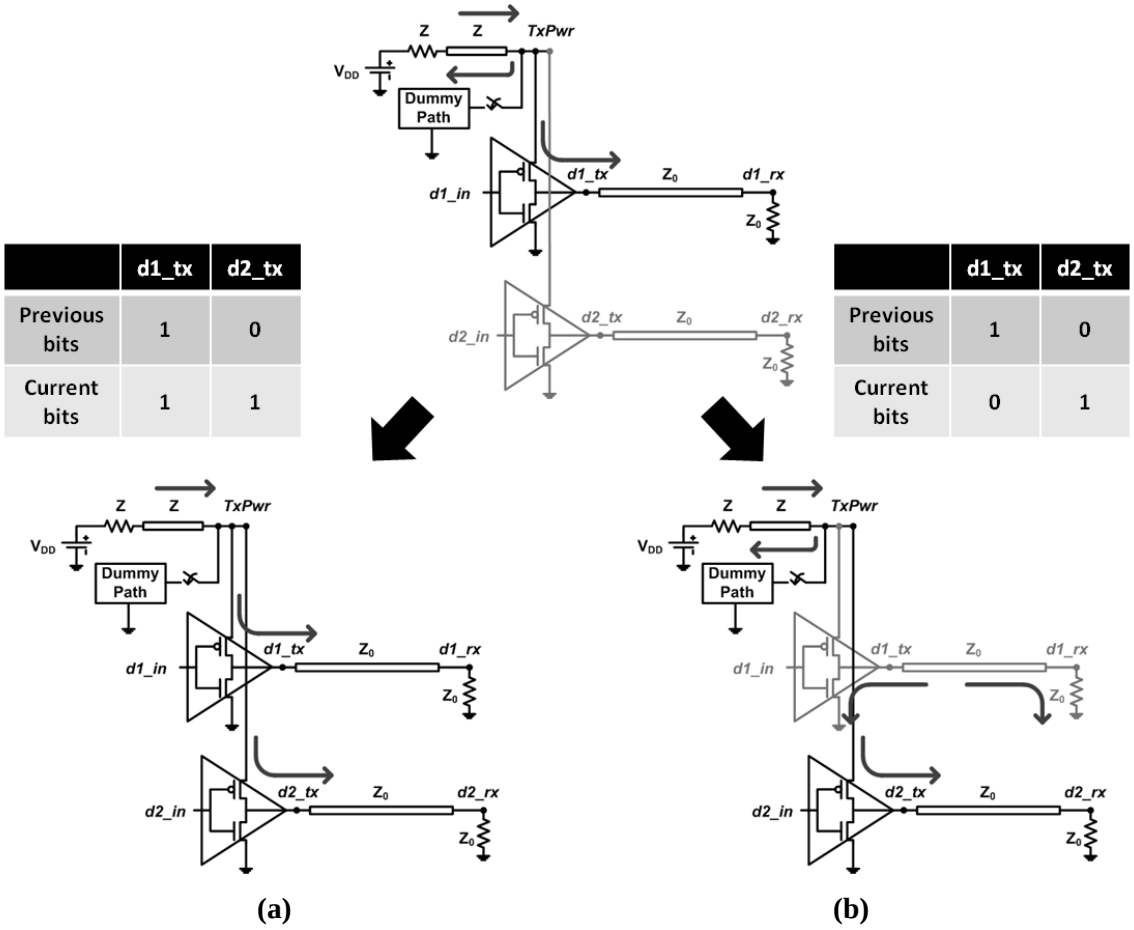
Using a power transmission line (PTL) prevents the cavity resonance so that the capacitor placement can be much simpler than using a power/ground plane pair. Still, the PTL needs decoupling capacitors to be used as charge reservoirs. With a new type of PDN proposed, a new methodology for the selection and placement of capacitors is needed, which is discussed in this chapter.

Although constant current flows through the PTL in the constant current PTL (CCPTL) scheme, current fluctuations during data transitions are inevitable. An example of two switching drivers connected to one PTL is shown in Figure 6.1. The two drivers switch independently, inducing 4 different combinations of data bits. When two data bits (d1_tx, d2_tx) are (1, 0), only the first driver is turned on and draws current from the PTL. As the data bits switch to have a different pattern, the data bits after the transition are called the current bits.

In Figure 6.1, two different data transitions are shown. When the current bits become (1,1) after (1,0), the second driver becomes turned on and draws current, along with the first driver, as shown in Figure 6.1(a). Since the CCPTL scheme is used, the total amount of current drawn from the supply is constant regardless of the data states. However, additional transient current is still needed during data transition to charge the second transmission line. On the other hand, when the current bits become (0,1) after (1,0), the output of the first driver makes a high-to-low transition and that of the second driver switches from low to high, as shown in Figure 6.1(b). The first transmission line is discharged, while the second transmission line becomes charged with the current sourced by the supply. As with the previous bits, current through the dummy path is maintained and results in constant current through the PTL. Still, additional transient current is required to charge the second transmission line as well.

Likewise, the switching drivers continue to draw current from the supply, and the current demand should be satisfied quickly to prevent the drivers becoming current-starved [15]. Decoupling capacitors can be used as a charge reservoir to help the PTL

respond quickly to the current demand. In this chapter, the methodology for the selection and placement of decoupling capacitors for the PTL-based PDN is presented. Unlike the PDN using power/ground plane pair, the PTL does not depend on the decoupling capacitor to provide current path at a RPD location or to reduce the PDN impedance at a voltage maximum to suppress voltage bounce of the power and ground planes. Thus, the goal of the design methodology for the PTL-based PDN is similar to that of the power-plane-based PDN, but less constraints apply.



	d1_tx	d2_tx
Previous bits	1	0
Current bits	1	1

	d1_tx	d2_tx
Previous bits	1	0
Current bits	0	1

Figure 6.1 Charging and discharging of signal transmission lines during data transitions.

6.2 Selection and Placement of Decoupling Capacitors

The required value of the decoupling capacitor depends on the amount of current pulled through the PTL, the rising/falling time, and the supply voltage level [76]. The

relationship of how those factors determine the choice of decoupling capacitor is explained using an example shown in Figure 6.2. One PTL is used to feed the supply voltage to 6 drivers. Among 6 drivers, 3 drivers are always turned on, drawing current through the PTL.

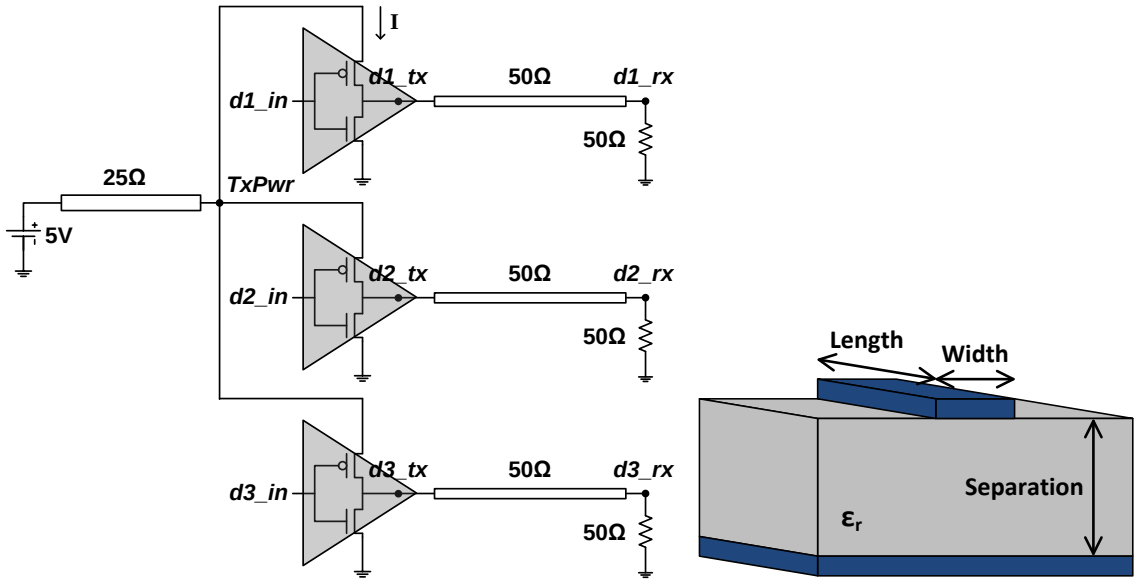


Figure 6.2 An example of one PTL driving three output buffers.

There are two types of capacitances to be charged: power transmission line and signal transmission line. Switching drivers draw current from the power supply to charge the signal transmission line, which represents the transmission of the signal. In the process, the power transmission line needs to be charged as well. Thus, the transient current is given by:

$$I = C\frac{dV}{dt} \tag{9}$$

where *dV* accounts for the voltage change across the capacitor during switching and *dt* is the switching time. To be more specific, *C* can be split into two components, which are C_{PTL} and C_{Sig}, and *dV* is determined accordingly. If there is a load capacitor at the far end of the signal transmission line, charging that capacitor should also be taken into account

during calculation. Without the load capacitor, Equation (12) is expanded to be:

$$I = C_{PTL}\frac{dV_{PTL}}{dt} + C_{Sig}\frac{dV_{Sig}}{dt} \tag{10}$$

where dV_{PTL} is the voltage change across the PTL and dV_{Sig} is the output signal swing at the output of the signal transmission line.

Before determining the value of those parameters, the circuit should be simulated first without any decoupling capacitor. Then, the rise time of the signal being transmitted and the voltage change across the PTL and signal transmission line are obtained. The capacitance of the PTL and signal transmission line can be calculated from the physical dimensions and the material property of the structure. Using all these values, Equation (10) can be used to calculate the required transient current. The choice of decoupling capacitor is determined by:

$$C = \frac{dQ}{dV} = \frac{Idt}{dV_{PTL}} \tag{11}$$

where I is the calculated transient current needed during the switching, dt is the switching time, and dV is the voltage change that the decoupling capacitor will experience. Initially, the decoupling capacitor is charged up to the supply voltage. As multiple switching drivers cause a high surge of current, the voltage droop occurs on the power supply voltage, which equals the amount of voltage fluctuation across the PTL during switching. The decoupling capacitor connected to the PTL sees the voltage difference and discharges to provide the compensation current [77].

Placing decoupling capacitor as close to the power supply pin of the device as possible is a rule of thumb in conventional PDN design. This is to keep the loop area between the voltage supply pin and the ground pin as small as possible, as shown in Figure 6.3. It also enables the decoupling capacitor to supply current quickly when there is a sudden current demand.

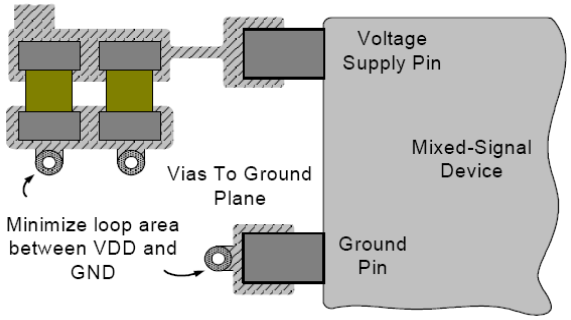


Figure 6.3 Minimizing loop area between VDD and GND (Picture courtesy of [82]).

For the PTL-based PDN, how quickly the demand for current can be met is the most important design criteria when placing decoupling capacitor. Thus, the placement of decoupling capacitors depends on the propagation velocity and the switching time. The propagation velocity is dependent on the dielectric permittivity of the transmission medium, as follows [78]:

$$v_p = \frac{c}{\sqrt{\varepsilon_r}} \tag{12}$$

Dividing the distance between the device and the decoupling capacitor by the propagation velocity equals the one-way propagation delay. For the compensation current from the decoupling capacitor to reach the device, it takes the one-way propagation delay [77]. Therefore, the time delay between the voltage droop and the charge supply from the decoupling capacitor equals the round-trip propagation delay between the power supply pin and the decoupling capacitor. The round-trip delay should be less than half the switching time to be able to respond to the current demand on time.

Multiplying the propagation delay by the switching time gives the distance that the current travels during the switching time. For the round-trip delay to be less than half the switching time, the round-trip distance from the device to the decoupling capacitor should be less than the propagation distance per switching time. As a result, the distance between the device and the decoupling capacitor should be less than half of the

propagation distance per switching time, at most. To ensure the prompt delivery of transient current to the device, placing the decoupling capacitor closer than the requirement is recommended.

If the dielectric used is FR4 with the dielectric constant of 4.6, the propagation velocity is:

$$v_p = \frac{c}{\sqrt{\varepsilon_r}} = \frac{3 \times 10^8}{\sqrt{4.6}} = 6.5 \times 10^7 m/s$$

If the switching time is 1ns, the propagation distance per switching time equals $v_p \times t_r$ = $6.5e^7 \times 1e^{-9}$ = 65 mm. The distance between the decoupling capacitor and the device should be about 65 mm / 2 = 32 mm.

6.3 Test Case: Simulation Results

The methodology for the placement and selection of decoupling capacitor is applied to the test vehicle shown in Figure 6.4. Pads for decoupling capacitor have been placed in eight different locations along the PTL, as shown in Figure 6.4. They are named *Decap 1~8*. *Decap 1* is next to the power and ground pins of the device, while *Decap 8* is the farthest from the device. The distance to the device from each location is summarized in Table 6.1. As mentioned above, the total length of the PTL is 122 mm. In this section, the decoupling capacitor placed at *Decap 1* will be called Decap 1.

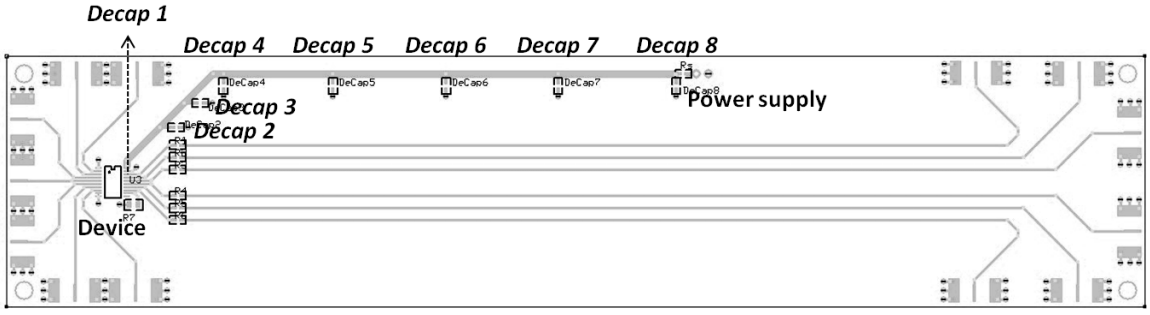


Figure 6.4 Eight different locations of pads for decoupling capacitors on the PTL.

Table 6.1 Distance to the device from each Decap location.

Decap Location	Distance to the device
Decap 1	0
Decap 2	10.7 mm
Decap 3	17.9 mm
Decap 4	28.6 mm
Decap 5	51.4 mm
Decap 6	75.1 mm
Decap 7	98.4 mm

Frequency responses of the PTL with 0.1 μF decoupling capacitor at various locations are simulated and compared in Figure 6.5, which is the transfer impedance of the PTL versus frequency graph. The input data rate to be used in time-domain simulations is 300 Mbps so that the simulated frequency range is from 10 MHz to 3 GHz. The impedance of the PTL without any decoupling capacitor has 4 peaks at 638 MHz, 1.27 GHz, 1.89 GHz, and 2.51 GHz, three of which are harmonics of 638 MHz. This is because the first half wavelength (λ/2) resonance of the PTL occurs at 632 MHz, as calculated by:

$$f_{res} = \frac{c}{\sqrt{\varepsilon_{eff}}} \cdot \frac{1}{2 \times \ell} = \frac{3e8}{\sqrt{3.78}} \cdot \frac{1}{2 \times 122mm} = 632MHz$$

where ε_{eff} is the effective dielectric constant of the microstrip line and ℓ is the length of the PTL. Since both ends of the line are terminated by the same termination of 50 ohms, half wavelength resonance occurs. As the PTL is used to interconnect the power supply and the device, a quarter wavelength (λ/4) resonance is rather expected due to the differing levels of voltage at each end of the transmission line.

When decoupling capacitor of 0.1 μF is added at either source-end or load-end of the PTL, the first three resonant frequencies are slightly shifted to 614 MHz, 1.24 GHz, and 1.82 GHz, respectively. Moreover, additional resonant frequencies are observed. However, as decoupling capacitor is added in the middle of the PTL, the response overlaps with that of the PTL without any decoupling capacitor, which implies that

adding a capacitor in the middle of the PTL does not have much effect on the line impedance. This is because the impedance of the transmission line is dictated by the resistive component at the resonance frequency, which is maintained almost the same with and without the capacitor added in the middle of the line. On the other hand, at the anti-resonance frequency, where the impedance becomes infinity, the decoupling capacitor suppresses the impedance peak. Therefore, the placement of the decoupling capacitor can be determined based on the calculation of the effective distance for charge supply.

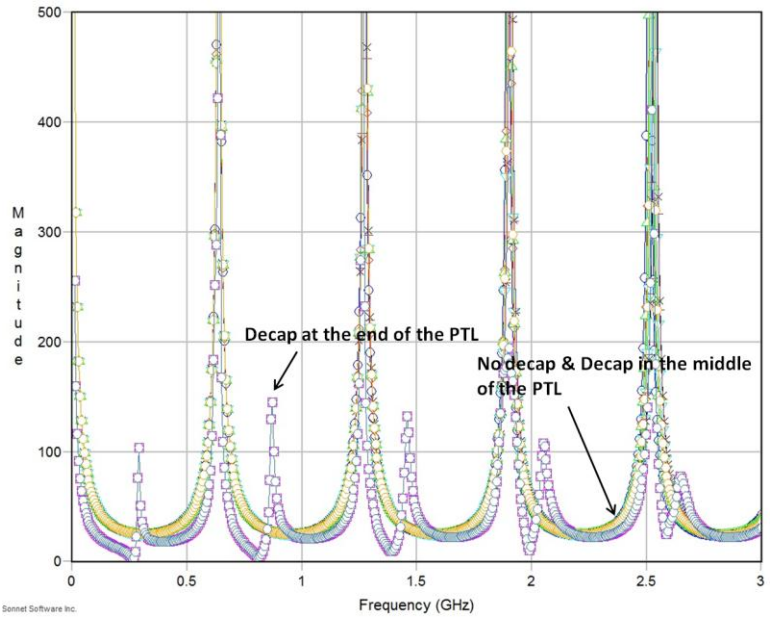


Figure 6.5 Transfer impedance (Z_{21}) versus frequency plot

Decoupling capacitor of sufficient capacitance is used in time-domain simulations to focus on the effect of the decoupling capacitor placement only with 0.1 μF capacitance and 2 nH ESL. The resulting waveforms are shown in Figure 6.6.

The eye diagram is measured at the far end of the signal transmission line, but the dotted line connects connecting each eye diagram to the corresponding location of the decoupling capacitor. When the decoupling capacitor is added at *Decap 1*, the eye diagram has the least noise on the power rail with the best voltage margin. *Decap 2* and

Decap 3 provides similar amount of contribution as *Decap 1*. As the capacitor gets farther from the device, the voltage fluctuation on the power rail starts to increase and the shape of the eye diagram becomes distorted, converging to the shape of the eye diagram without any decoupling capacitor. As calculated above, in this test case, the propagation distance per switching time equals $v_p \times t_r = 6.5e^7 \times 1e^{-9} = 65$ mm. Therefore, the distance between the decoupling capacitor and the device should be about 32 mm. The distance to the device from *Decap 4* equals 28.6 mm, which is the last location whose distance to the device is less than 32 mm. Up to this distance, the eye diagram is in good condition. However, the quality of the waveform is gradually degraded as the decoupling capacitor is placed farther away from the device. *Decap 5*, which is 51.4 mm away from the device, is the starting point for serious voltage fluctuations.

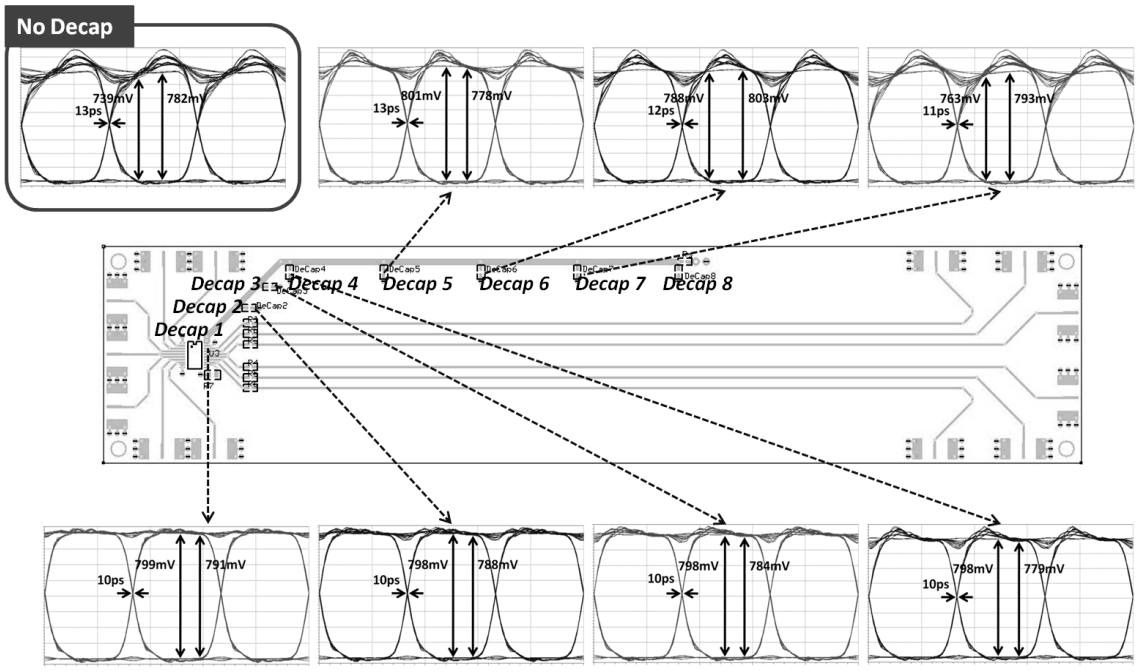


Figure 6.6 Simulated eye diagrams of 300Mbps PRBS.

Now, to select the right amount of capacitance, the input data rate is assumed to be 300 MHz with the switching time of 1 nsec. The device in Figure 6.4 consists of six single-ended drivers. Since balanced data with an equal number of 1s and 0s are used as

input data, three out of six drivers are always turned on. Therefore, at any given time, three drivers are drawing current through the PTL, as shown in Figure 6.2. The calculated capacitances of the PTL and signal transmission line are calculated to be 25.2 pF and 14 pF, respectively. The test vehicle is first simulated without any decoupling capacitor to obtain the amount of voltage drop across the PTL and signal transmission line, which were 0.4 V and 0.1 V, respectively. Equation (10) is then used to calculate the required amount of transient current to charge the transmission lines.

$$I = 25.2p \cdot \frac{0.4}{1n} + (14 \times 3p) \cdot \frac{1.8}{1n} = 85.7mA$$

This value is plugged into Equation (11) along with the transient time of 1 nsec and the maximum voltage dip (dV_{PTL}) on the PTL of 0.4 V. The required value of decoupling capacitor therefore becomes 214 pF. Figure 6.7 shows how the waveform is improved as the decoupling capacitance increases from 10 pF to 500 pF at *Decap 2*; Black eye diagrams are the result with a 10 pF, 100 pF, 250 pF, and 500 pF capacitor, respectively. A grey eye diagram is the waveform with a 0.1 μF capacitor. It is plotted along with each of the black eye diagrams to serve as a baseline. As the decoupling capacitance increases toward 100 pF, the black eye diagram converges to the grey eye diagram. Once 250 pF is reached, additional capacitance does not provide much improvement in terms of eye opening.

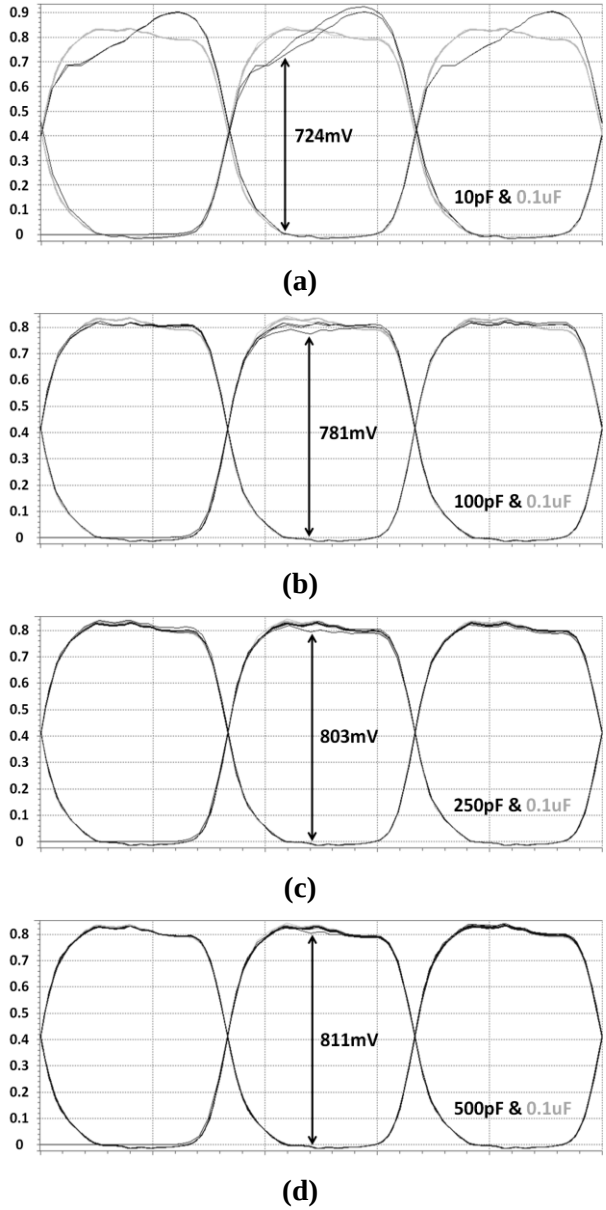
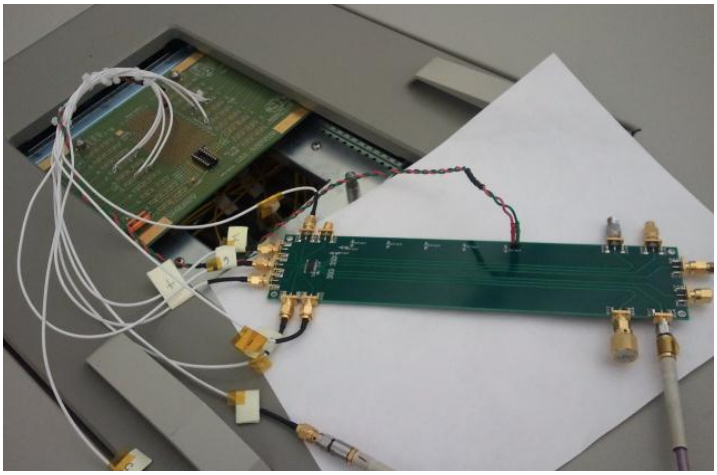


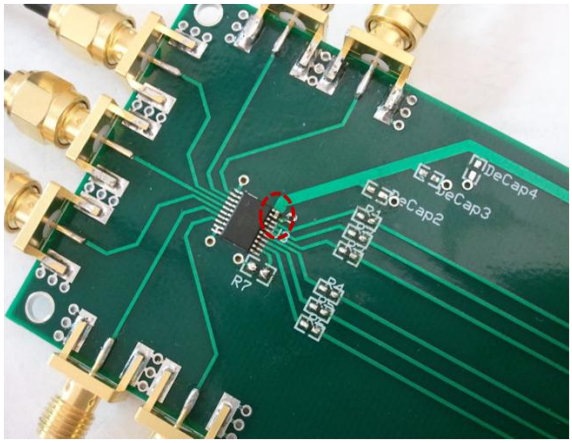
Figure 6.7 Eye diagrams of pseudo-balanced data with various sizes of decoupling capacitor. (a) 10 pF. (b) 100 pF. (c) 250 pF. (d) 500 pF.

6.4 Measurement Results

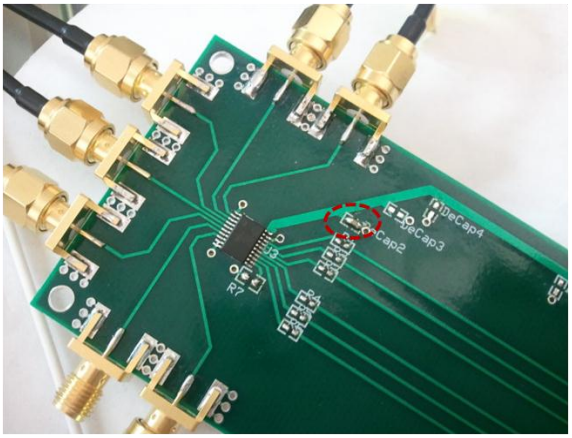
Test vehicles were fabricated with multiple pads for the decoupling capacitor as shown in Figure 6.8(a). Figure 6.8(b) and (c) show decoupling capacitor mounted at *Decap 1* and *Decap 2*, respectively.



(a)



(b)



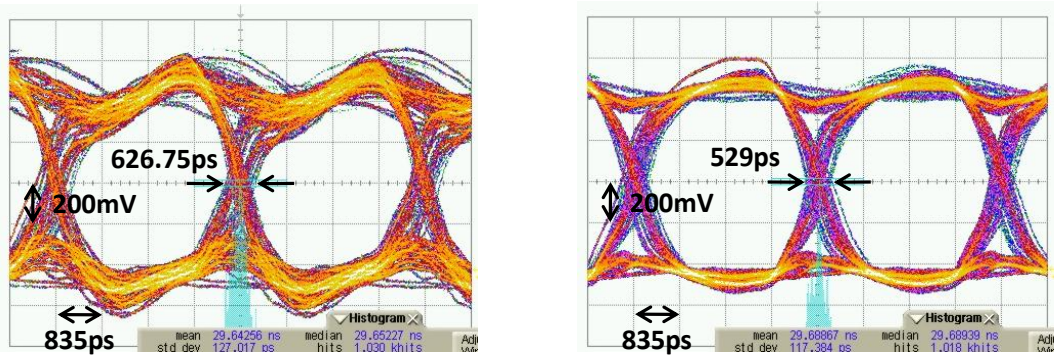
(c)

Figure 6.8 Test vehicle for study of decoupling capacitor. (a) Test vehicle connected to the ATE. (b) Test vehicle with Decap 1. (c) Test vehicle with Decap 2.

Both the power-plane-based and PTL-based test vehicles are used to investigate the effect of the decoupling capacitor placement. Pseudo-balanced signaling scheme has been applied to both test vehicles. Figure 6.9 shows the eye diagrams of pseudo-balanced data of the power-plane-based and PTL-based test vehicle with *Decaps 1~8*. The eye diagram with *Decap 1* has the best timing and voltage margins possible, which becomes a baseline for comparison. The focus is how much the waveform gets degraded as the distance between the decoupling capacitor and the device increases.

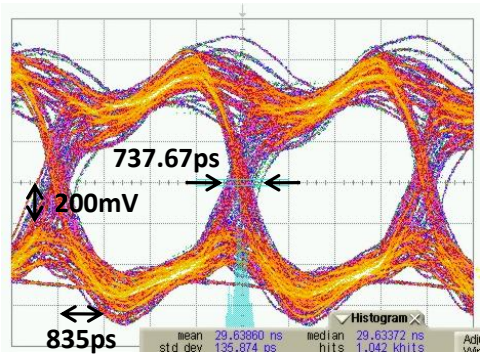
First, the voltage fluctuations on the power and ground rail are much more severe in

the plane-based TV than in the PTL-based TV. Thus, when *Decap 1* is added to the PDN, the PTL-based TV yields better waveform than the plane-based TV. In the plane-based TV, the shape distortion of eye diagram becomes dominant from *Decap 5* location so that the p-p jitter cannot be solely used as a performance indicator anymore, and so does the eye diagram of the PTL-based TV. The decoupling capacitor loses its effectiveness starting from the *Decap 5* location, which is a distance of 51.4 mm from the device, as shown in Table 6.1. This is because the distance of 51.4 mm is not only larger than the target placement radius but close to the multiple of the propagation velocity and the switching time. It is interesting to note that the voltage rail of the PTL-based TV becomes degraded, while the ground rail remains clean and unaffected, which is attributed to the elimination of the plane cavity and the RPDs by using PTL. On the other hand, the voltage fluctuations on the power and ground rails worsen in the plane-based TV, causing further distortion of the waveform.

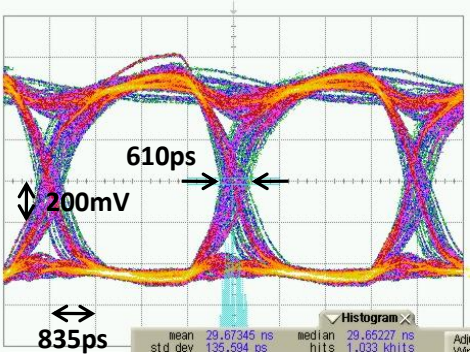


(a) Plane with Decap1 **(b) PTL with Decap1**

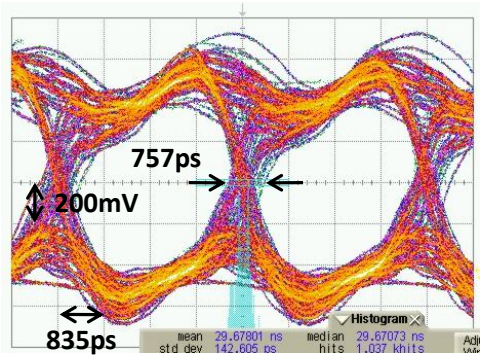
Figure 6.9 Eye diagrams of pseudo-balanced data with decoupling capacitor at various locations.



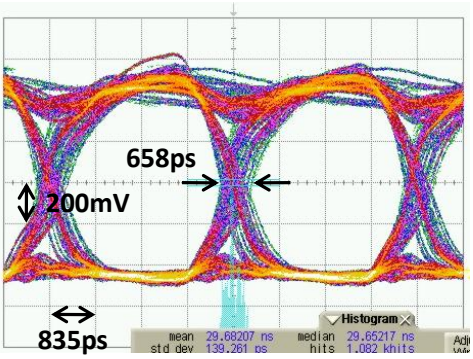
(c) Plane with Decap2



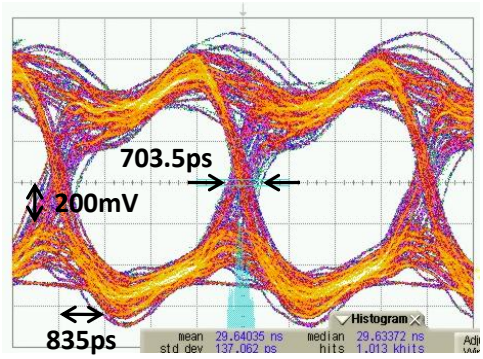
(d) PTL with Decap2



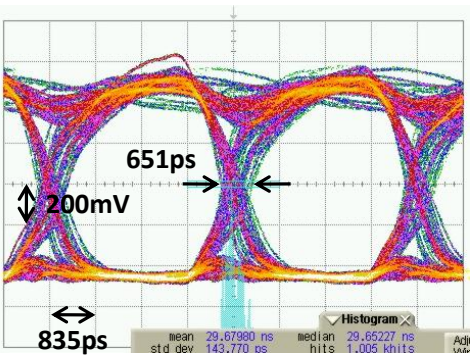
(e) Plane with Decap3



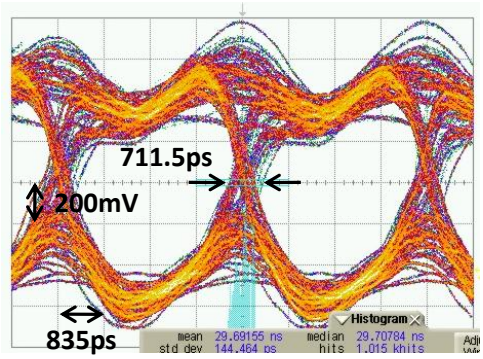
(f) PTL with Decap3



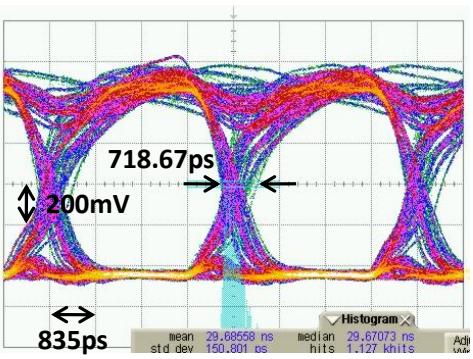
(g) Plane with Decap4



(h) PTL with Decap4

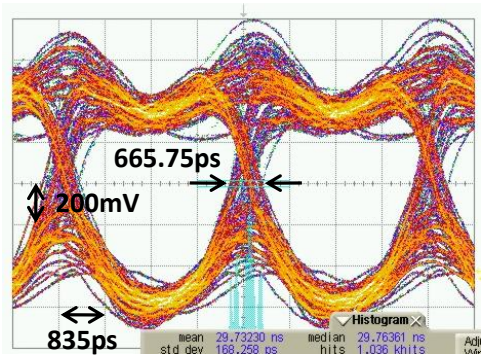


(i) Plane with Decap 5

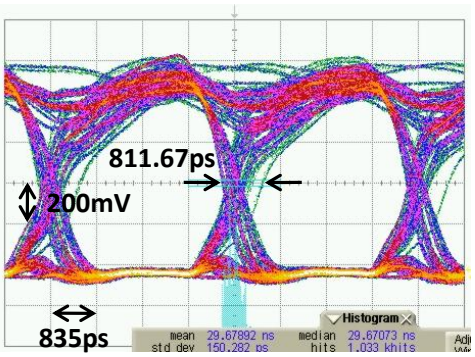


(j) PTL with Decap5

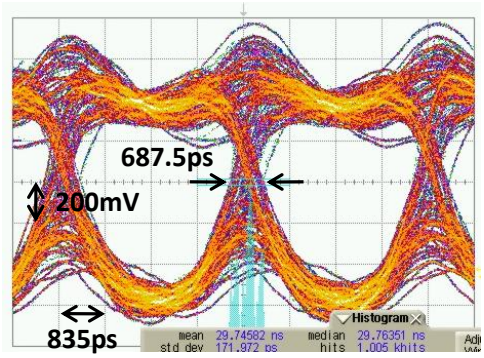
Figure 6.9 Continued.



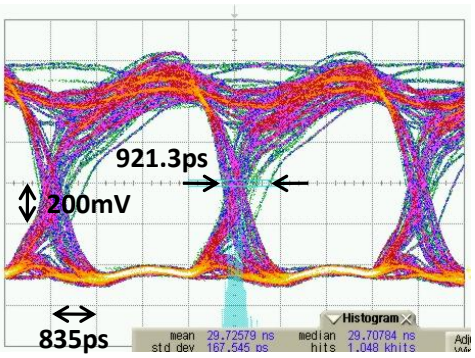
(k) Plane with Decap 6



(l) PTL with Decap6



(m) Plane with Decap 7



(n) PTL with Decap 7

Figure 6.9 Continued.

The p-p jitter is plotted along with the location of the decoupling capacitor in Figure 6.10. Up to *Decap 4*, the waveform of the PTL-based TV has less p-p jitter than the plane-based TV. After the crossover point at *Decap 5*, the plane-based TV outperforms the PTL-based TV. This is because the PTL has higher series inductance in the supply path by the following equation, which limits the amount of current available during switching time [13].

$$L = \frac{\mu \cdot d}{w}$$

In this formula, μ and d are the permeability and the thickness of the transmission medium, and w is the width of the transmission line (or the voltage plane). Thus, without the help of decoupling capacitor, it is difficult for one PTL to convey current to six switching drivers. However, it is important to note that the shape distortion of eye

diagram becomes dominant in the plane-based TV after *Decap 5* location so that the p-p jitter cannot be solely used as a performance indicator anymore.

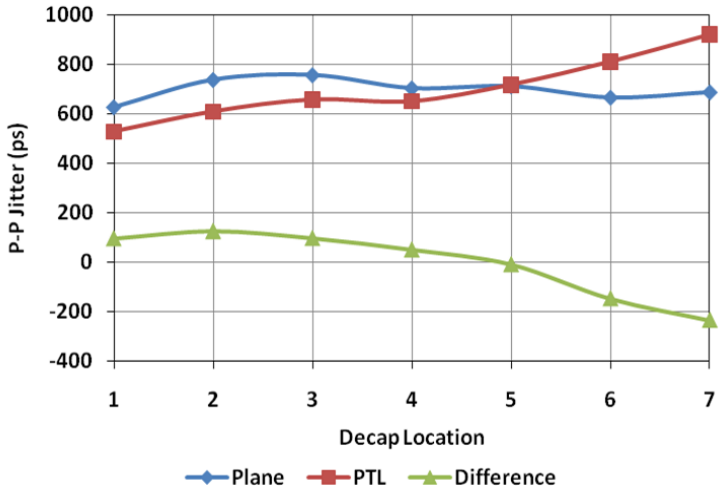


Figure 6.10 P-P jitter versus decoupling capacitor location graph.

Figure 6.11 shows the eye diagrams with various values of decoupling capacitance at Decap 2. The capacitance sweep begins with 10 pF, which is far less than the required capacitance value. The eye diagram has a noisy power supply rail being starved for current. The p-p jitter of using 10 pF is 1153 psec. As the decoupling capacitance increases to 100 pF, there is an improvement of 25%, which is not enough as compared to using a 0.1 μF capacitor. The voltage and timing margins become comparable to those of using 0.1 uF when the capacitance reaches 470 pF. When 470 pF decoupling capacitor is used, the p-p jitter is improved by 26% as compared to using 100 pF, which is 4% larger than that of using a 0.1 uF capacitor. As the decoupling capacitance increases to 1 nF and 22 nF, the fluctuation on the power supply rail becomes continuously suppressed. The p-p jitter moves up and down due to a certain amount of randomness during the construction of the eye diagram, but it stays within 8 % of the p-p jitter of using 470 pF.

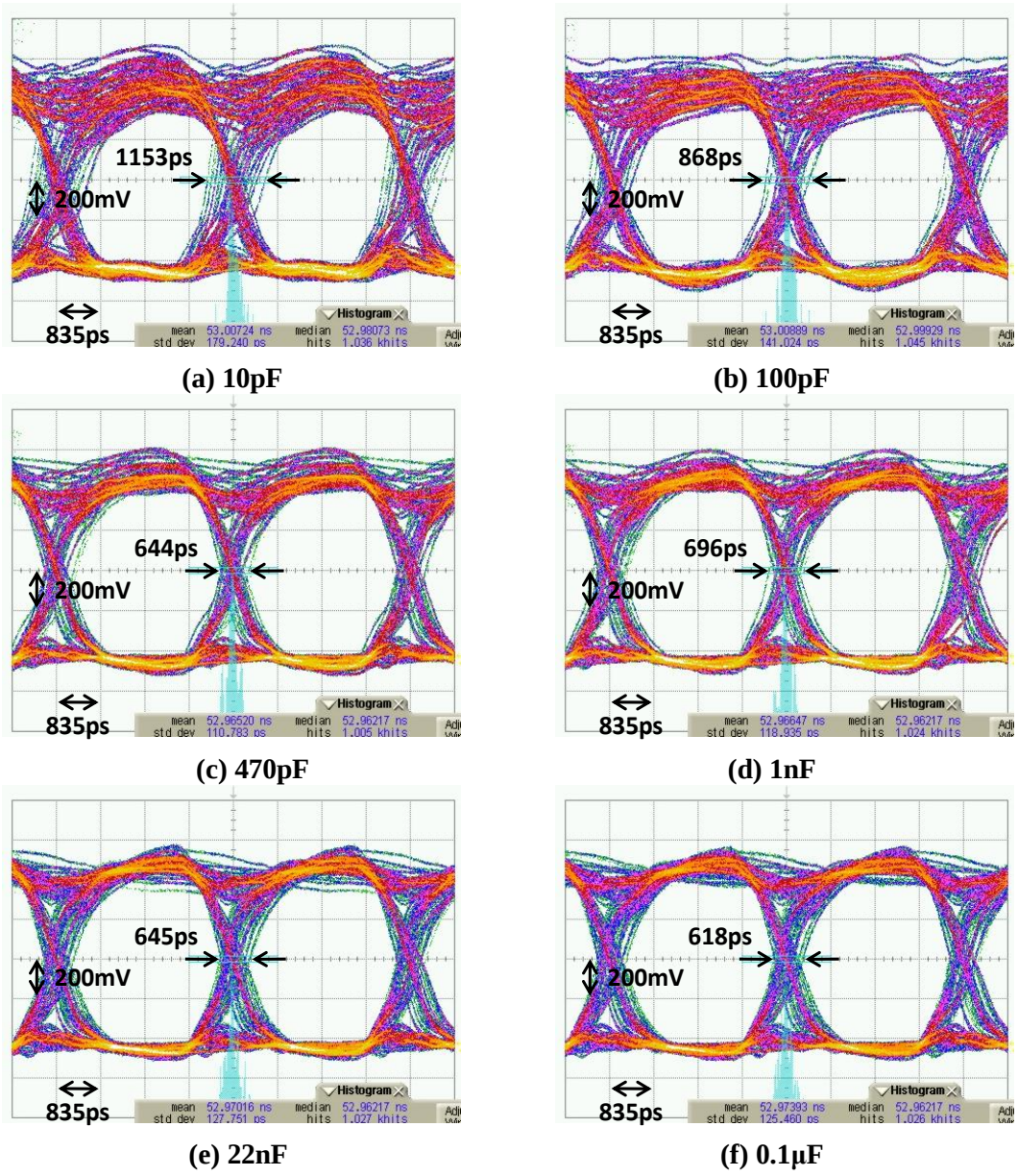


Figure 6.11 Eye diagrams of pseudo-balanced data with decoupling capacitor of various values in the PTL-based TV. (a) 10 pF. (b) 100 pF. (c) 470 pF. (d) 1 nF. (e) 22 nF. (f) 0.1 µF.

The p-p jitter is plotted along with the size of the decoupling capacitor in Figure 6.12. Using 470 pF decoupling capacitor, the p-p jitter reaches a minimum value within the desired range (4% larger than the minimum value). Afterward, the p-p jitter ranges between 618 psec and 696 psec.

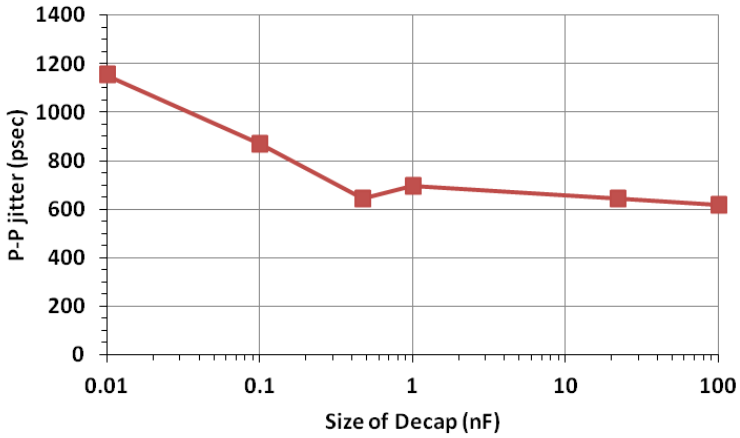


Figure 6.12 P-P jitter versus decoupling capacitance graph.

The selection and placement procedure for the PTL-based PDN is simpler and computationally less expensive, not to mention that much better signal integrity can be obtained than from the plane-based PDN with decoupling capacitor. Moreover, smaller values of capacitance are needed at relatively flexible locations.

CHAPTER 7

STANDARDIZATION OF POWER TRANSMISSION LINE LAYOUT USING A PRE-DEFINED GRID

7.1 Introduction

One advantage of using a power plane is easiness of layout. Because the power plane covers a large area of the board or package, multiple ICs can be placed and connected to the PDN with fewer constraints regarding the layout.

To provide the easiness of layout using PTLs, a uniform PTL grid has been studied to supply power to multiple I/O drivers in a standardized manner. An example of such a PTL grid is shown in Figure 7.1. The PTL grid consists of multiple segments of PTL cascaded in series and placed in parallel. Each is source-terminated near the VRM. Although the PTLs criss-cross to form a grid, not all segments of the grid are used. In Figure 7.1, black lines represent the active PTLs used to connect the VRM and the device, while grey lines are unused components, which are omitted to prevent routing congestion.

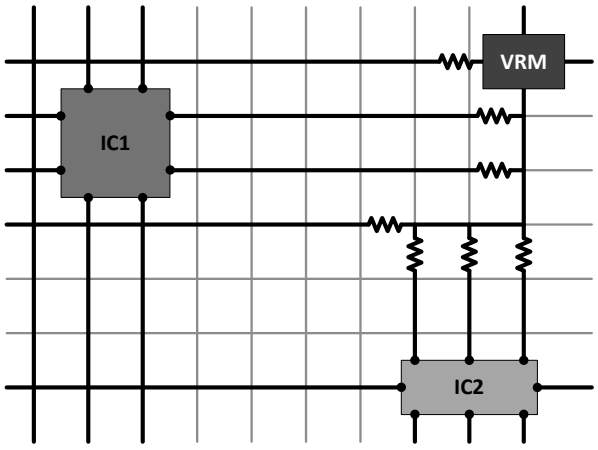


Figure 7.1 An example of PTL grid.

In the previous chapters, one end of the PTL was used as an input, while the other end of the PTL was used as an output, which was connected to the power supply pin of one or more drivers. However, if a PTL grid is employed to feed power to multiple drivers, the drivers will draw current at many different points along the PTL, as shown in Figure 7.1. As a result, there will be a coupling between the drivers through the PTL. Preliminary simulations were performed to study the noise coupling effect on the waveforms in detail. The following design parameters were varied:

- The number of I/O drivers per PTL segment
- The source termination of each PTL segment
- The vertical connection between PTL segments

Based on the simulation results, design guidelines have been developed to achieve the optimized arrangement of the grid.

7.2 Design parameters

First, the effect of an open stub is studied. Figure 7.2 shows the bounce diagram for two different transmission line systems. In Figure 7.2(a), an open stub is connected to the output of a source- and load-terminated transmission line. The bounce diagram shows the multiple reflections until the steady state is reached. Although the first line segment is source-terminated, the reflections cause a ringing effect on the voltage at all the nodes (n_S, n1 and n2). In Figure 7.2(b), the stub is terminated in 25 ohms. After a reflection at the branch point, the steady state is reached, which is achieved much faster than the case in Figure 7.2(a).

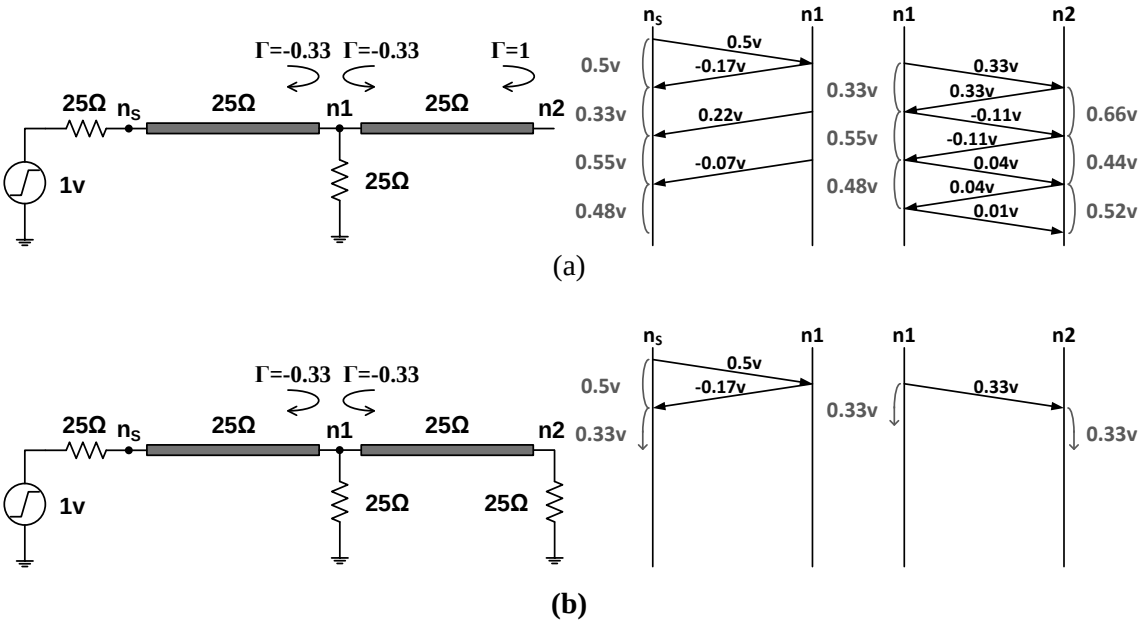


Figure 7.2 Transmission line system and the corresponding bounce diagram. (a) Open stub. (b) Terminated stub.

Figure 7.3 shows the simulated eye diagrams of three different cases. The first case has one segment of PTL connecting the VRM and the power supply pin of a driver, while the second and third cases have two segments of PTL cascaded in series without and with a driver at the end of the second segment, respectively. Figure 7.3(a) shows the schematic and the resulting waveform of the first case, which serves as a baseline. The transistors are simplified with ideal switch models in the simulation. The output buffer drives a 7.15-inch long transmission line, which is terminated by a 50 ohm resistor and a 2 pF capacitor. The waveform is observed at the output of the signal transmission line (d1_rx). The power supply voltage is 2.5 V, and the target eye height is 1.25 V. The eye height of the baseline structure equals 1.244 V and the p-p jitter is 4.46 psec. In Figure 7.3(b), an extra line whose length is the same as the PTL is connected to the power supply node of the driver, which behaves as an open stub. Based on the effect of open stub shown in Figure 7.3(a), the stub is expected to induce multiple reflections. Such reflections affect the voltage at the power supply pin and degrade the waveform at the output of the signal transmission line, as shown in Figure 7.3(b). The eye height is reduced to 1.169 V, and

the p-p jitter is increased to 13.4 psec. Figure 7.3(c) shows the case when the 2nd driver is connected to the end of the second segment of PTL. Adding an extra driver to a PTL causes the load impedance seen by the PTL to change. As a result, the voltage division between the PTL, the driver, the signal transmission line, and the load termination is changed, which reduces the eye height to 1 V. The extra driver at the end of the stub suppresses the voltage fluctuation in the middle of the eye diagram, as shown in Figure 7.3(c).

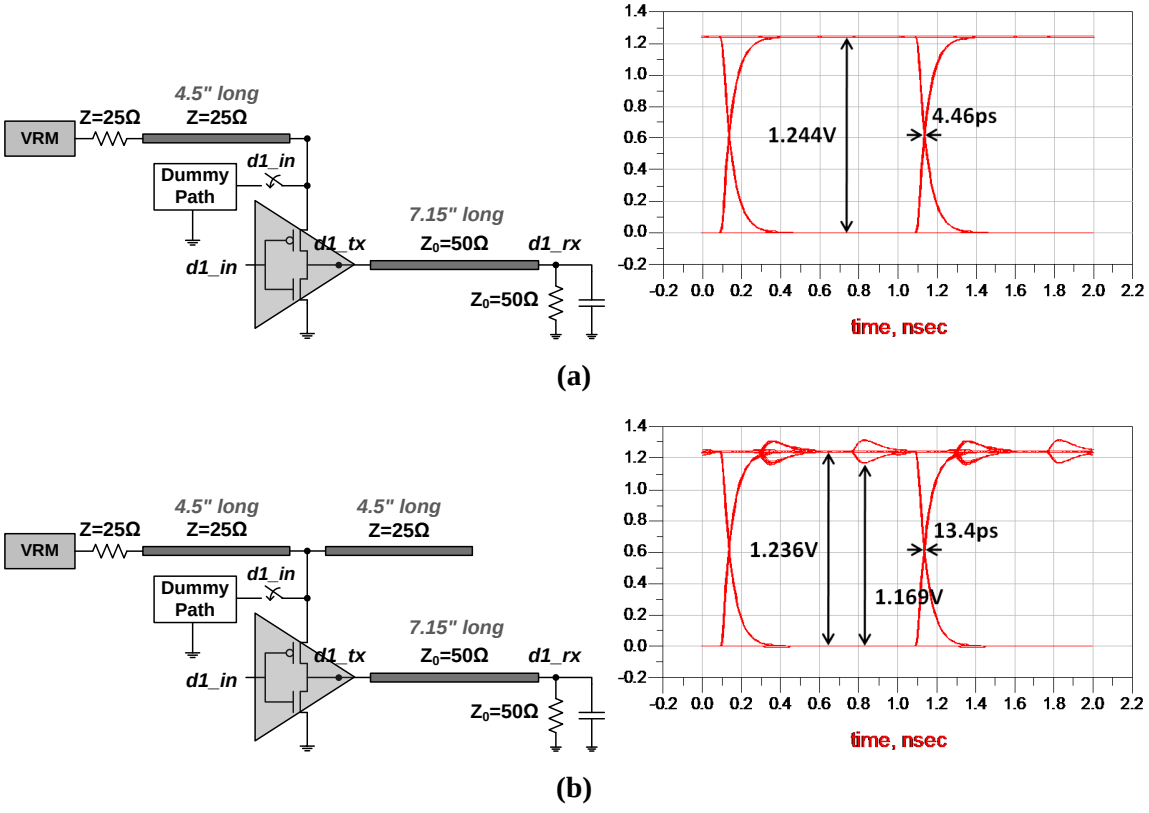
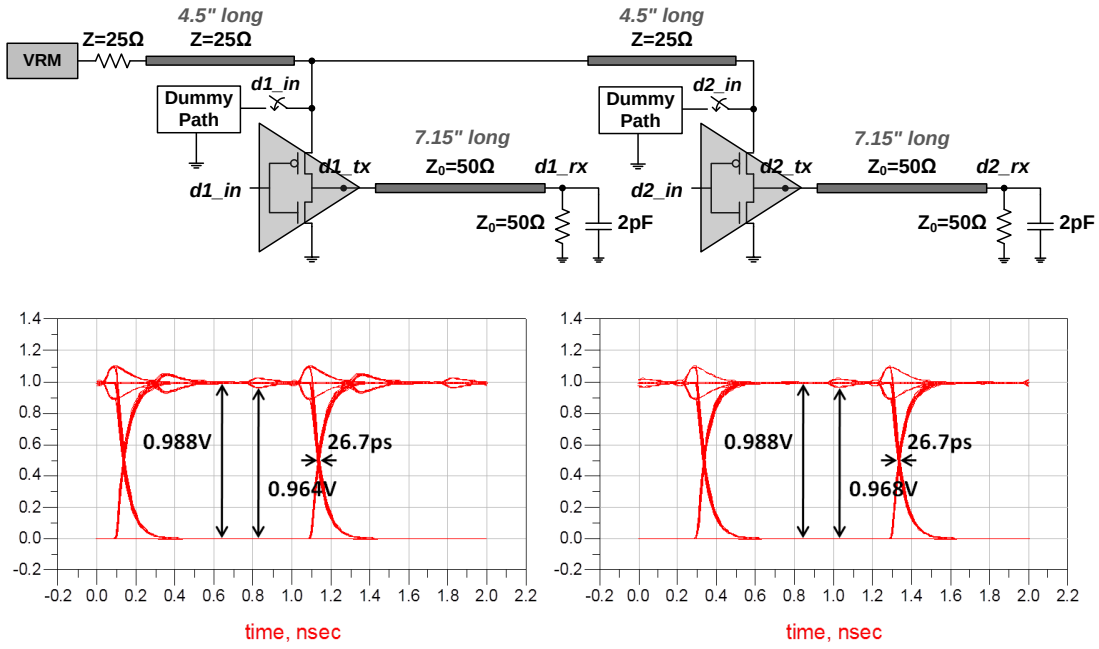


Figure 7.3 Study of adding one more driver to a single PTL. (a) PTL for one driver. (b) PTL with an open stub for one driver. (c) PTL for two drivers.



(c)

Figure 7.3 Continued.

When two segments of PTL are connected to the power supply in parallel, there are two ways of source termination, which are shown in Figure 7.4. Figure 7.4(a) shows the case of one source termination being shared for two PTLs. The characteristic impedance of each PTL is 25 ohm so that the shared source termination of 12.5 ohm is used. At the far end of the signal transmission line, a load capacitance of 2 pF is added to model the input capacitance of the receiver circuit along with a load termination of 50 ohms. The target eye height is 1.25 V. The resulting eye diagram at the far end of the signal transmission line (data1_rx or data2_rx) has an eye height of 1.012 V and p-p jitter of 26.7 psec. On the other hand, Figure 7.4(b) shows the case that each segment of PTL has its own source termination of 25 ohm. The resulting eye diagram has a better opening with eye height of 1.244 V and p-p jitter of 8.9 psec, as compared to Figure 7.4(a).

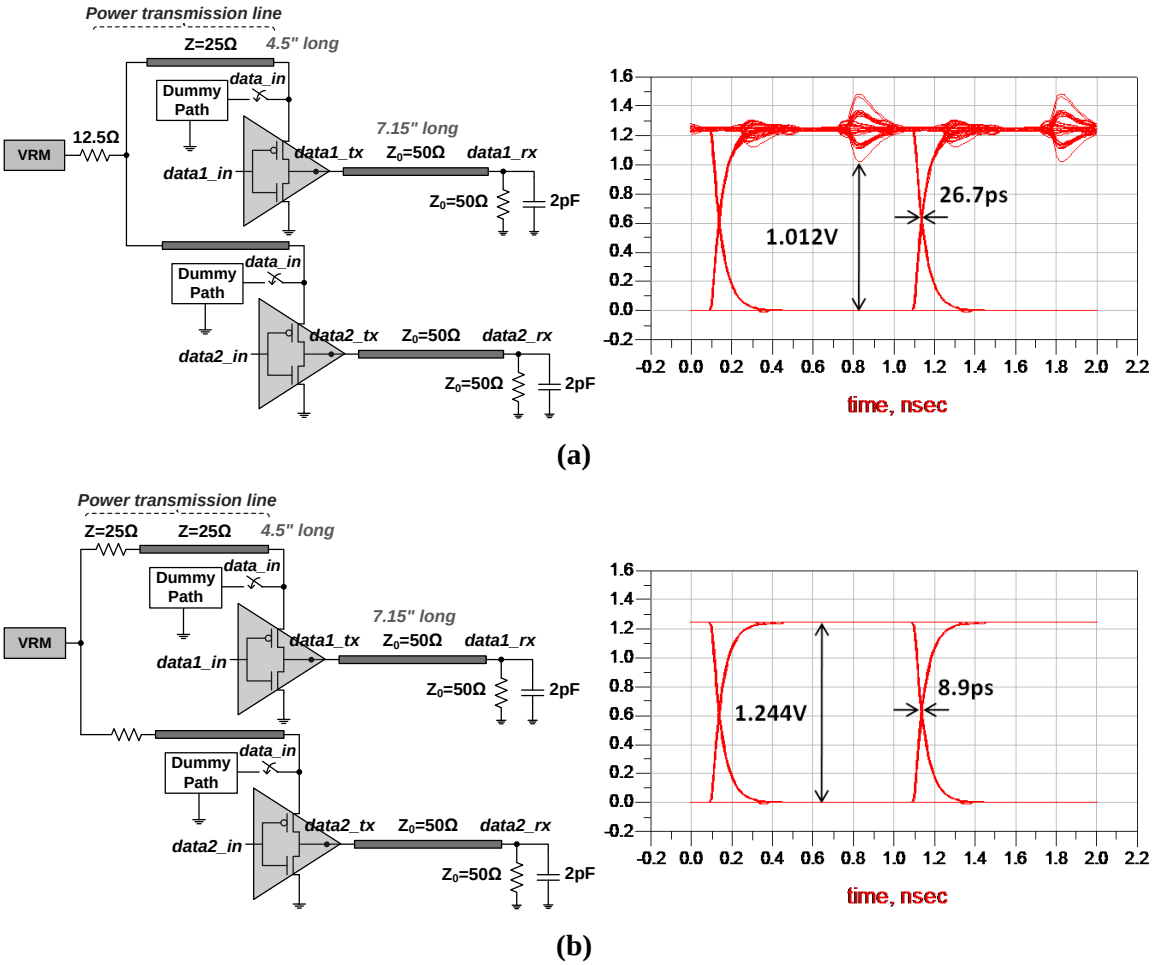


Figure 7.4 Study of source-termination for two PTL branches. (a) Shared source-termination. (b) Separate source-termination.

In Figure 7.5, an example of two PTLs in parallel driving four drivers is shown, which is an extension of Figure 7.3(c) Two segments of PTL are cascaded in series to form a branch, and two branches are connected to the VRM in parallel. The output of each segment is connected to a driver, which results in two drivers per branch. Each segment of PTL is 4.5-inch long so that the length of each branch becomes 9 inch. The eye diagrams are measured at the 1st and 3rd load termination (data1_rx and data3_rx). The eye diagram at data3_rx (Figure 7.5(c)) has less fluctuation on the power supply rail than that at data1_rx (Figure 7.5(b)). This is because the node at the end of the PTL branch offers more stable power than the node at the middle of the PTL branch. The eye

diagrams of the second PTL branch (at data2_rx and data4_rx) are the same with those of the first PTL branch at corresponding positions (data1_rx and data3_rx), respectively.

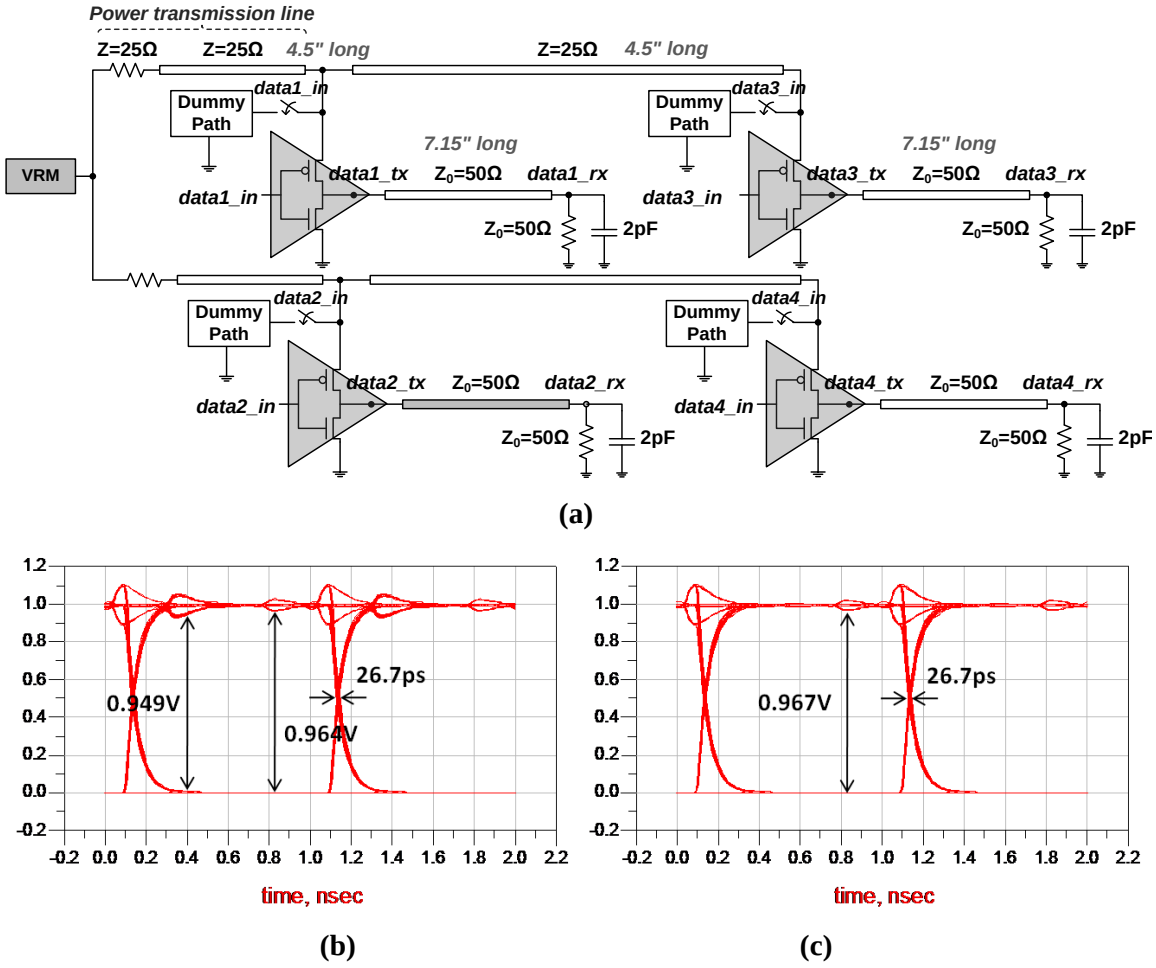


Figure 7.5 Study of two PTL branches driving two drivers respectively. (a) Schematic. (b) Eye diagram at data1_rx. (c) Eye diagram at data3_rx.

When the two branches of PTLs are vertically connected at the middle and end points, as shown in Figure 7.6(a), the effect of the vertical interconnection is studied using a bounce diagram. All six transmission lines have the same length so as to have the same propagation delay. The reflections seen at n_S, n1, n2, and n3 are shown in Figure 7.6(b). The voltage at n1 is determined not only by the incident voltage and the reflected voltage but also by the signals bouncing back from n2 and n3. After five time-of-flight's of the PTL segment, the reflected component from n4 reaches n1, which exponentially

complicates the superimposition of the voltages. It can be concluded that the vertical interconnection increases the susceptibility of the PTL grid to multiple reflections.

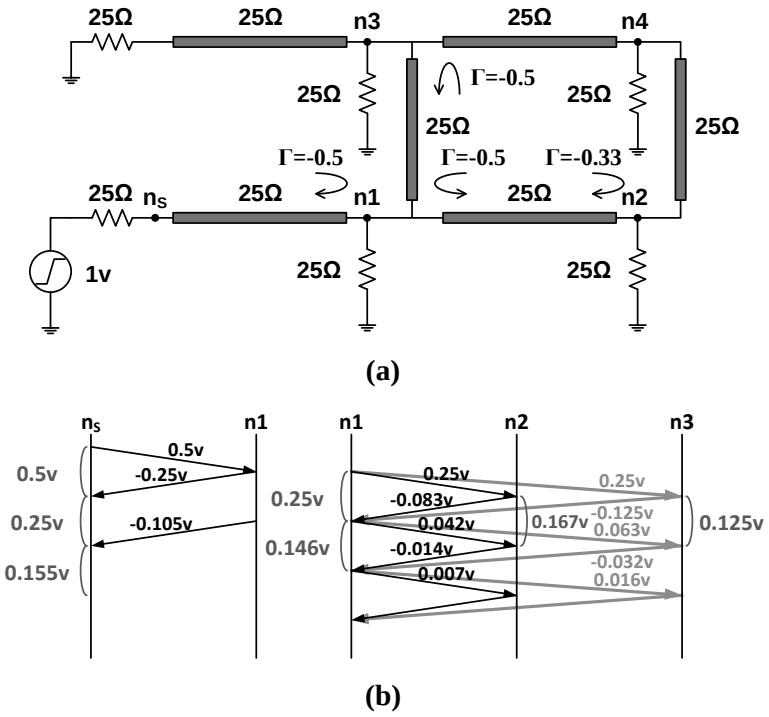


Figure 7.6 PTL grid with vertical interconnections. (a) Schematic. (b) Bounce diagram.

Figure 7.7 shows an example of 4-bit transmission using the PTL grid with vertical interconnections. In Figure 7.7(a), all four drivers are coupled through the PTL and share the power supply voltage. If the voltage drop across the vertical interconnection is induced during the data transition, current flows along the vertical interconnection to level out the potential difference. As a result, the voltage fluctuation caused by one driver propagates to affect the other drivers through the PTL. The power supply rail becomes more susceptible to the switching noise.

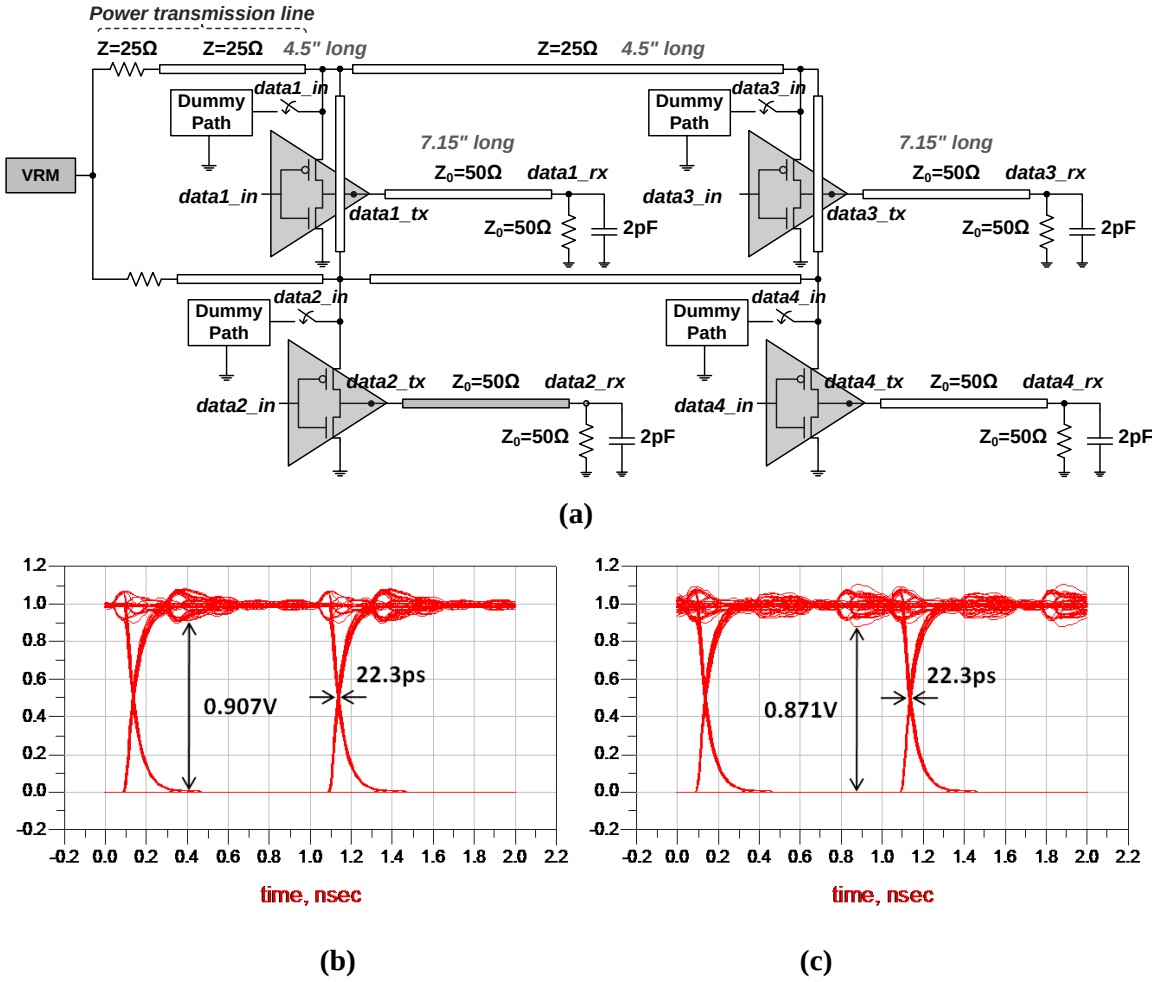


Figure 7.7 Study of two PTL branches with vertical connections. (a) Schematic. (b) Eye diagram at data1_rx. (c) Eye diagram at data3_rx.

In Figure 7.8, the case of having an unequal number of I/O drivers connected to two branches of the PTL grid is shown. The foremost driver of the second PTL branch is removed from the circuit. The first branch of PTL is kept the same to supply power to two drivers. The eye diagram at data1_rx (Figure 7.8(b)) has not changed as compared to that in Figure 7.5(b). Since the first and second branches of PTLs are isolated, removing one driver from the second branch does not affect the waveforms of the drivers connected to the first branch. In Figure 7.8(c), the eye diagram at data4_rx is shown. In this case, one-to-one correspondence is established between the PTL and the 4th driver so that the eye diagram is improved with the voltage fluctuation on the power supply rail

suppressed. The eye opening has become as large as that in Figure 7.3(a).

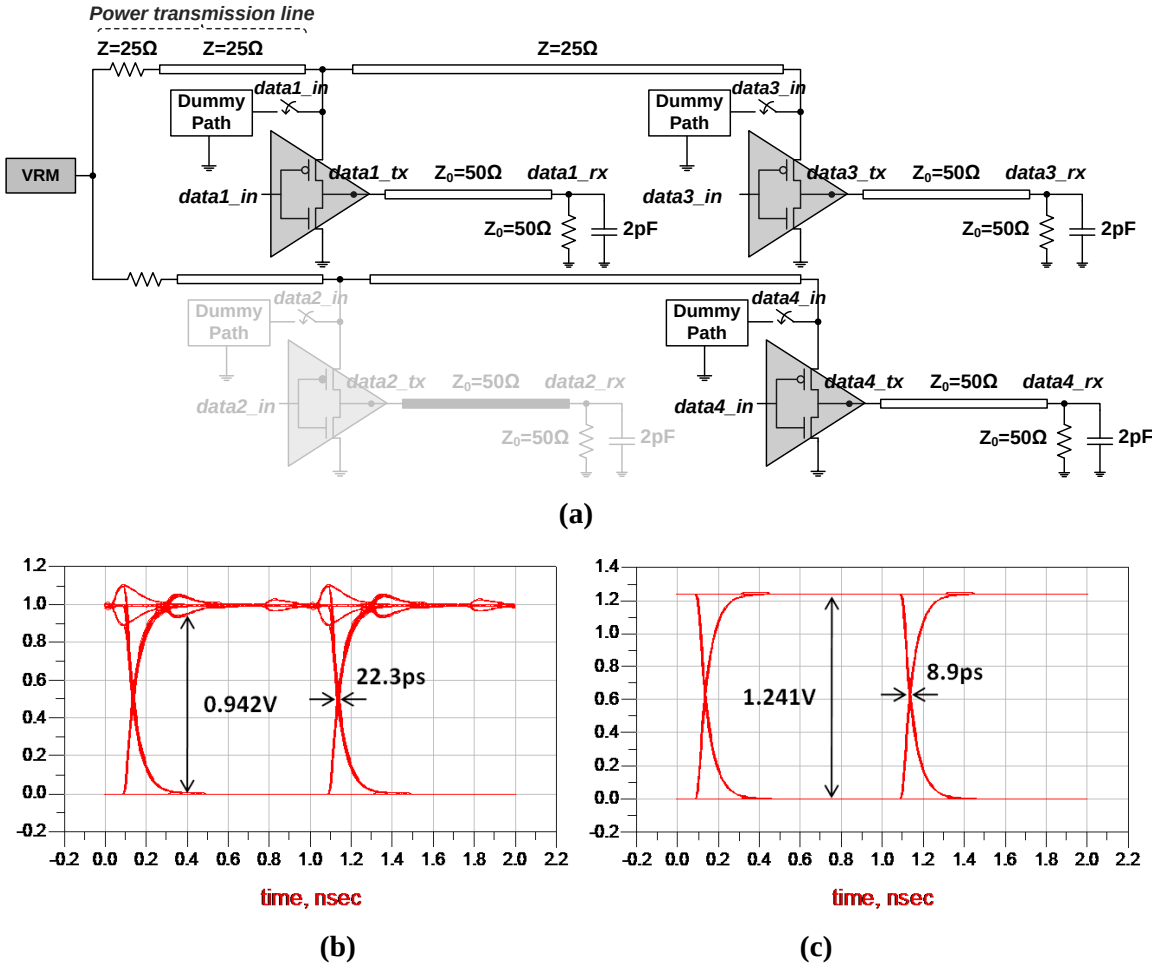


Figure 7.8 Study of two PTL branches without vertical connections. (a) Schematic. (b) Eye diagram at data1_rx. (c) Eye diagram at data4_rx.

In Figure 7.9, the foremost driver of the second PTL branch is removed from the circuit shown in Figure 7.9(a). In this example, the first and second branches of PTL are vertically connected so that the removal of one driver has an impact on the rest of the drivers. The voltage distribution along the second PTL branch becomes different from that along the first PTL branch so that an electrical potential difference is induced between the two ends of the first vertical interconnection. As a result, current flows to equalize the potentials, which leads the eye heights of the three drivers to become uniform regardless of which PTL they are physically connected to. In Figure 7.9(b) and

(c), the eye diagram at data4_rx is degraded more severely than that at data1_rx, unlike the case without the vertical interconnections.

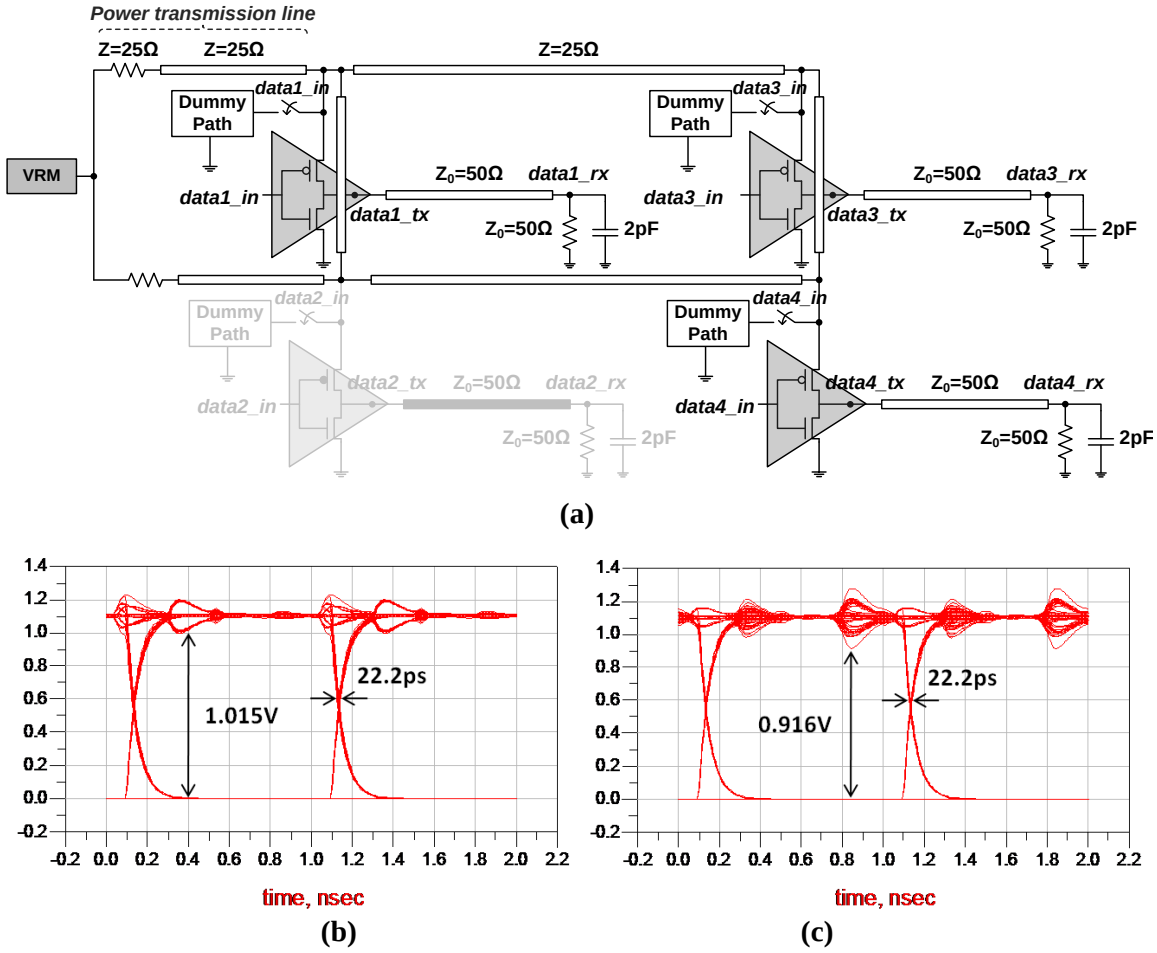


Figure 7.9 Study of two PTL branches with vertical connections. (a) Schematic. (b) Eye diagram at data1_rx. (c) Eye diagram at data4_rx.

As explained with various examples, the manner in which the PTL is routed to feed the supply voltage to the driver determines the quality of the waveform at the output of the signal transmission line, which can be summarized as follows:

1. When multiple drivers are being connected to a PTL segment, the farthest output of the PTL segment should not be left open.
2. Each PTL segment should have its own source termination.
3. Connecting two different PTL segments should be avoided unless it is necessary.

Therefore, the manner in which each driver is connected to the PTL should be based on the target eye height and the required voltage and timing margins of each I/O driver. Some signals are required to have tighter timing accuracy, while the others are allowed to have relatively less accuracy. Those requirements can be reflected in the routing of PTLs.

7.3 Test Case: Simulation Results

The power grid structure shown in Figure 7.1 has been simulated with eight drivers connected at the numbered nodes, as shown in Figure 7.10(a). Each driver is connected to an 8-inch long transmission line, which is terminated by a 50 ohm load resistor and a 2 pF load capacitor, as shown in Figure 7.10(b). Each numbered node on the PTL grid is connected to one driver and one corresponding dummy path to form a CCPTL scheme. The length of one PTL segment is 120 mil to achieve the line spacing equal to twice the line width. All the PTL segments are connected to the power supply pins of drivers to prevent an open stub, which only degrades power and signal integrity. Also, any connection that can possibly function as a vertical interconnection is removed. The resulting PTL grid is indicated by black thick lines. Grey thick lines are the signal transmission lines, which are routed on a different layer.

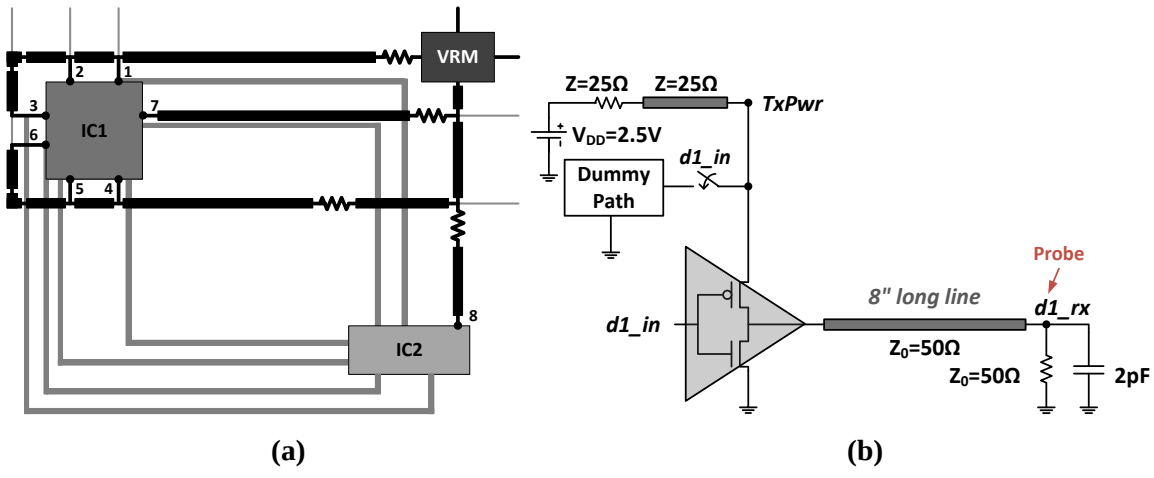
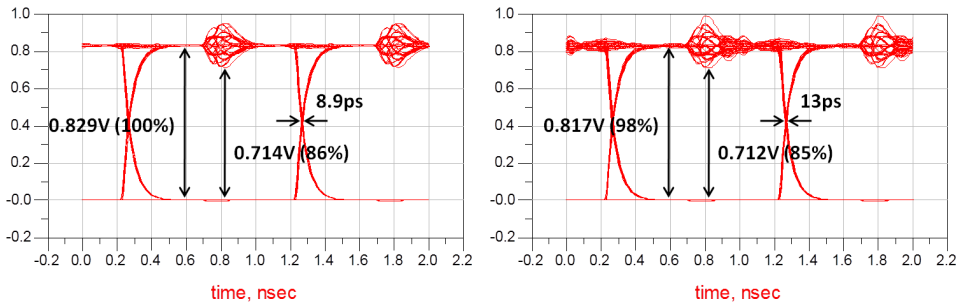


Figure 7.10 Test case. (a) PTL grid with numbered nodes to which drivers are connected. (b) Driver model used for the test.

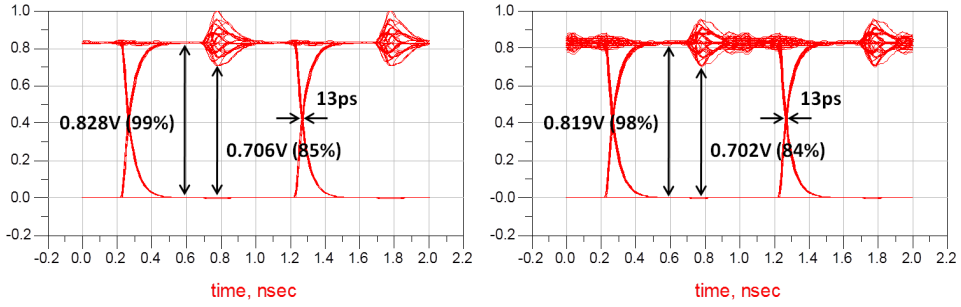
The first PTL branch consists of multiple segments cascaded in series, supplying power to Driver1, 2, and 3. The second branch feed the supply voltage to Driver4, 5, and 6. The difference between the first and second PTL branches is that the first branch is source-terminated near the VRM, while the source-termination of the second branch is placed 600 mil away from the VRM. Moreover, two other PTL branches are connected to the intermediate section between the source termination and the VRM, which feed power to Driver7 and 8, respectively.

Each driver has its own environment so as to yield a different eye diagram from other drivers. The eye diagrams at the outputs of the 8 inch long signal transmission lines are simulated. The eye diagrams of the first branch are shown in Figure 7.11(a), (b), and (c), while those of the second branch are shown in Figure 7.11(d), (e), and (f). The percentage eye height of the target height is shown along with the absolute value. As the first branch is better source-terminated without any interference from the VRM to the source termination, the eye diagrams have relatively larger eye openings. Comparing the eye diagrams of three drivers connected to the first branch (d1_rx, d2_rx, and d3_rx), the voltage margin decreases as the PTL segment for the driver is placed farther away from the VRM.



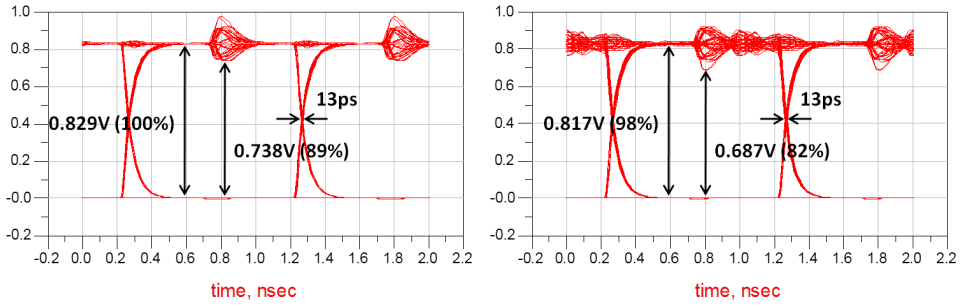
(a) d1_rx **(d) d4_rx**

Figure 7.11 Eye diagrams of the test case. (a) d1_rx. (b) d2_rx. (c) d3_rx. (d) d4_rx. (e) d5_rx. (f) d6_rx.



(b) d2_rx

(e) d5_rx

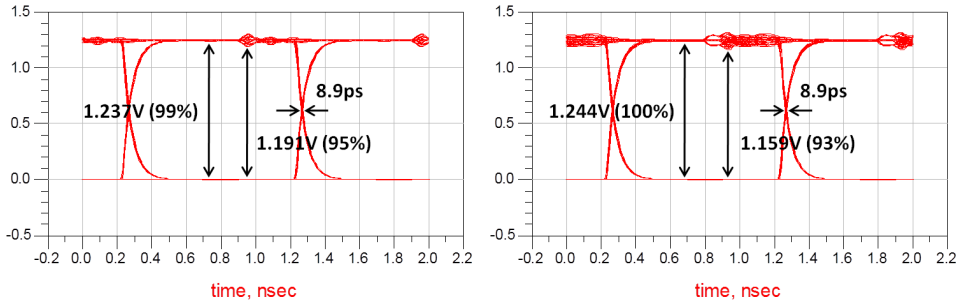


(c) d3_rx

(f) d6_rx

Figure 7.11 Continued.

As expected, the eye diagrams at d7_rx and d8_rx shown in Figure 7.12(a) and (b) have better eye opening than the previous six eye diagrams. The 7th and 8th drivers have their own PTL, having a one-to-one connection. The difference between them is that the PTL for the 7th driver has branched off from the main PTL, which is headed to the 8th driver. As compared to the previous six eye diagrams, the quality of the waveform is better with the least voltage.

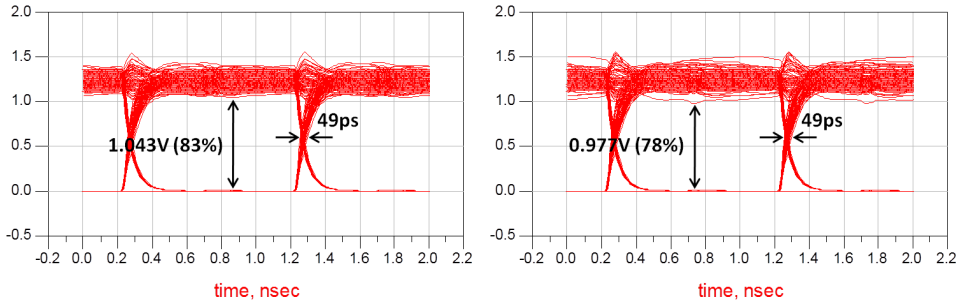


(a) d7_rx

(b) d8_rx

Figure 7.12 Eye diagrams of the test case (one-to-one connection). (a) d7_rx. (b) d8_rx.

The eye diagrams of the power-plane-based scheme are shown in Figure 7.13. As in the PTL-based scheme, the eight drivers switch simultaneously, drawing current from the PDN, which is a power and ground plane pair. Here, the ground plane is assumed to provide an ideal ground, while the power plane suffers from a voltage bounce, which corrupts the signal through the 8 inch long transmission line. The target eye height is the same with that of Figure 7.12(a) and (b). The eye diagram of the PTL-based scheme has a normalized eye height of 100% and a p-p jitter of 8.9 psec, while that of the plane-based scheme has a normalized eye height of 81% and a p-p jitter of 49 psec. Using a well-designed PTL grid, better voltage and timing margins can be achieved than using a power plane.



(a) d7_rx **(b) d8_rx**

Figure 7.13 Eye diagram of the plane-based TV. (a) d7_rx. (b) d8_rx.

7.4 Summary

The PTL grid is introduced in this chapter along with simulation results of a test case. A design methodology has not been developed, but design guidelines are presented for better arrangement of both the PTL segments and the drivers. First, the source termination should not be shared. One-to-one correspondence between the source termination and the PTL branch should be secured. Second, an open stub should be eliminated. The far end of the PTL branch should be connected to the power supply pin of a driver, instead of being left open. Otherwise, the fully-reflected component bounces

back to the preceding PTL segments, causing a ringing effect on them. Third, the PTL branch should not form a loop. To prevent this, any connection that can possibly be a vertical interconnection should be removed. Otherwise, multiple reflected components reach the branch point from multiple directions, which worsens the voltage fluctuation and the waveform degradation.

As shown in the test case, the target eye height and the voltage and timing margins vary depending on the manner in which each driver is connected to the PTL. Therefore, the layout of the driver and the PTL grid can be optimized by matching the requirements of each driver to the characteristic of each node on the PTL grid. The methodology for such optimized layout of the PTL grid can be developed as a part of future work.

CHAPTER 8

FUTURE WORK

8.1 Demonstration of the Constant Voltage PTL scheme

The CVPTL scheme, which employs selective resistor paths between the PTL and the power supply pin of the driver, had been presented in Chapter 5. Simulations were performed to investigate the concept of the scheme, but its application to a practical test case has not been shown yet. To further validate the proposed idea, implementation of the test vehicle using the CVPTL scheme is needed to demonstrate its effectiveness.

When using off-the-shelf chips for proof-of-concept, several things need to be taken into account. First, the timing synchronization between the input data and the control signals should be achieved. The control signals select a resistor path that corresponds to the current data pattern. Before the current data reaches the output buffer, the control signals should have been generated and switched on the correct resistor path. Also, the impedance of each resistor path should be designed with caution. There must be impedance mismatches due to manufacturing variations. Therefore, low-resolution design needs to be employed to be less susceptible to mismatches.

8.2 Three Dimensional Power Delivery Network

As 3D-IC integration technologies mature, new design techniques appropriate for 3D-IC integration are strongly required, especially from power delivery. Due to the increased number of chips stacked vertically, more current will be drawn from the power delivery network, causing more power noise coupling through the entire power delivery network. This will worsen the simultaneous switching noise (SSN). Thus, the ability of the power delivery network to provide clean power becomes more important in a 3D-IC

system.

Based on the advantages of using PTL, supplying power to I/O circuits in 3D-IC system can be a promising solution. The CCPTL based I/O drivers were taped-out using 350 nm Global Foundries' technology and Tezzaron's TSV/3D technology. The process of manufacturing TSVs and stacking dies are explained in [79]; The TSVs are manufactured in a via-first process. Trenches are etched into the silicon and filled with Tungsten. Then devices and metal layers are patterned. Next, wafers are flipped and bonded. Finally, one wafer is thinned until the trenched TSVs are revealed from the backside. This produces a two-layer face-to-face bonded stack that uses TSVs for IO.

The side view of the stacked dies based on Tezzaron's F2F and TSV stacking technology and Amkor's wirebond packaging is shown in Figure 8.1. Two dies are face-to-face (F2F) connected, and the F2F vias will have negligible parasitics. The designed driver is located on the top tier of the stacked dies, but the stacked dies are flipped when being put to wire bonding. TSVs will be placed beneath the I/O pad cells on the bottom tier, which will be through the upper substrate in Figure 8.1. Hence, the power/ground and signal for the designed driver travels through a wire, TSV, and F2F via. A conventional I/O driver is implemented on the same bottom tier, and will be power-supplied through a plane. This driver will provide a baseline for performance comparison between the two PDNs during measurements. The efficacy of using PTL in 3D applications was planned, but could not be demonstrated since the fabrication and package/board design could not be completed on time.

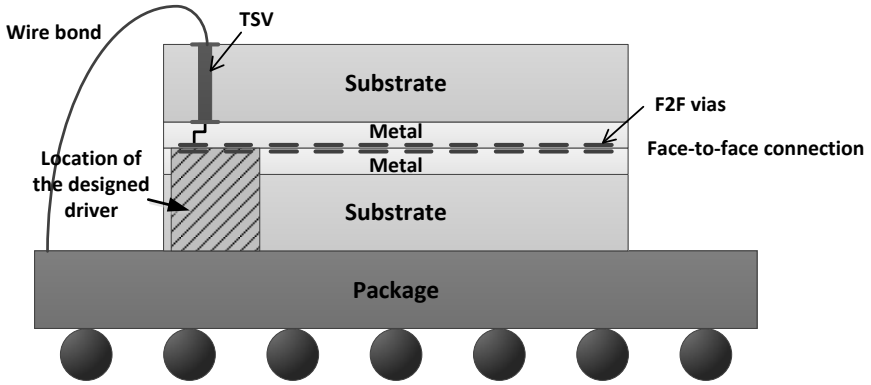


Figure 8.1 Side view of the stacked dies and the location of the designed I/O driver.

The CCPTL scheme, which has been presented in Chapter 3, has been implemented for 1-bit and 2-bit transmission. The schematic of the designed transmitter for 1-bit transmission is shown in Figure 8.2(a). Simulated eye diagrams are shown in Figure 8.2(b) and (c). A dummy path is connected to the power node of the driver. The input, *D* is inverted to be used as a control signal for the dummy path. Buffers are included in front of the driver to match the transition time between *D* and *Db*. These buffers are sized to balance the duty cycle and rising/falling times as well. The transistor sizes of the driver and dummy path are determined to have the desired impedances. In simulation, 1.5 V is supplied to the drivers, and 1 Gbps PRBS is used. Figure 8.2(b) and (c) show the eye diagrams at the output of the transmitter and at the input of the receiver, respectively. The signal has traveled a distance of 5.57 inches along the transmission line to reach the receiver. Here, the transmission lines with an ideal ground plane are used so that the voltage fluctuations and waveform degradation are not shown. The eye heights are 750 mV, which is 100% of target eye height in both diagrams. The timing width is 998 psec. It shows that the CCPTL scheme suppresses the power supply noise to near-zero in idealistic situations.

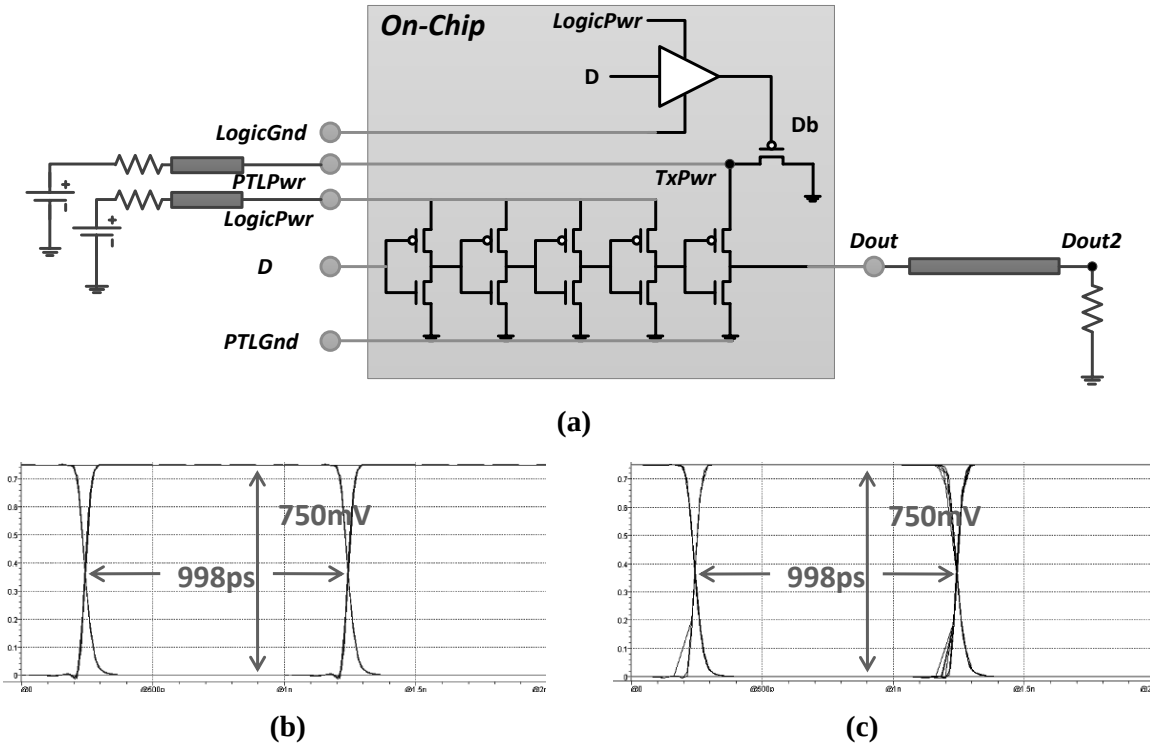
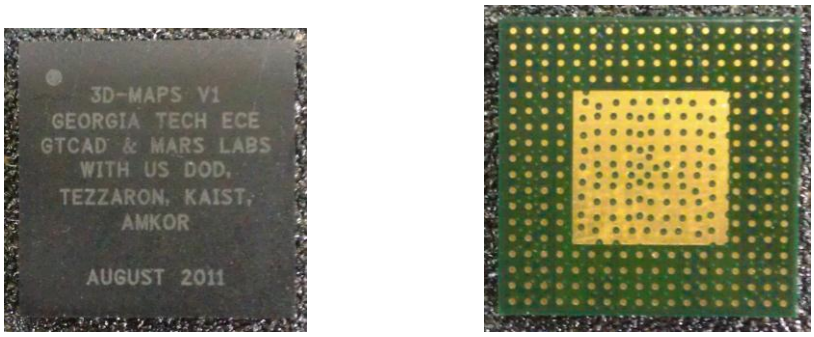


Figure 8.2 The CCPTL-based transmitter (a) Schematic. (b) Simulated eye diagram at the output of transmitter. (c) Simulated eye diagram at the input of receiver.

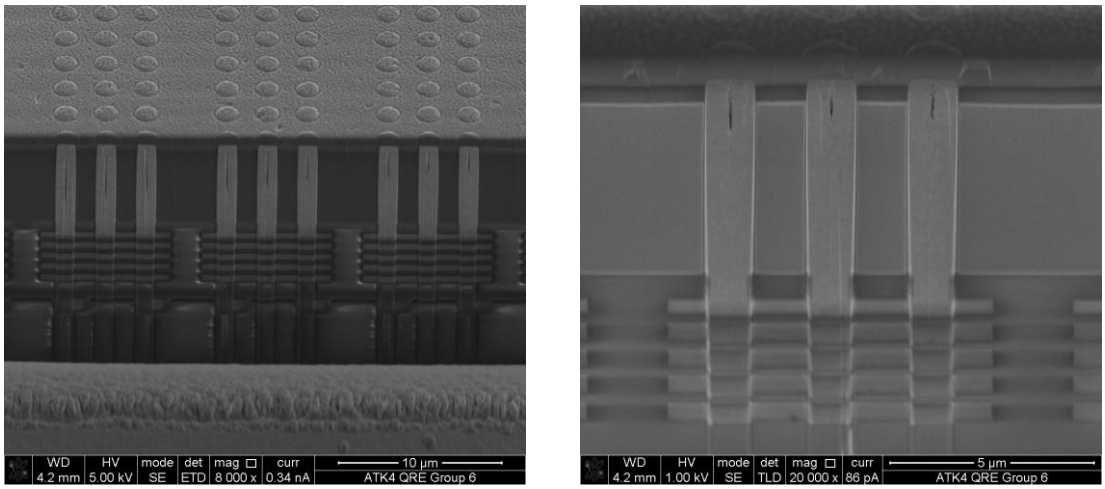
A transmitter for differential signaling was designed as well. For comparison, power-plane-based schemes are implemented for 1-bit and 2-bit single-ended signaling, and differential signaling.

Recently, the packaged die was fabricated but has not been mounted on the board yet. The top and bottom view of the package is shown in Figure 8.3. The test board for the custom-designed 3D chip needs to be designed and fabricated. The measurements need to be made and analyzed to validate the effectiveness of the CCPTL scheme with a TSV in its power supply path, as shown in Figure 8.4; to quantify the performance improvement over using a power plane by using the CCPTL scheme in terms of signal quality obtained at the receiver; and to compare the effect of TSV on signal integrity in the PTL-based and plane-based structure.



(a) **(b)**

Figure 8.3 Packaged die. (a) Top view. (b) Bottom view.



(a) **(b)**

Figure 8.4 (a) Side view of raw die. (b) TSVs connecting the top and bottom dies.

8.3 Other works

As the PCB trace count doubles, the affordable spacing between lines will become smaller, increasing the interference between the electromagnetic waves along transmission lines. Therefore, the crosstalk issue should be examined closely to prevent the degradation of the signals traveling along the transmission lines.

The source termination of the PTL has been resistive throughout this research, but other types of termination can be considered as well.

CHAPTER 9

CONCLUSION

The performance of a system depends heavily on the communication speed between integrated circuits. Single-ended signaling is widely used for memory interfaces, but it suffers from simultaneous switching noise, crosstalk, and reference voltage noise. Even with other signaling schemes that remedy the shortcomings of the singled-ended signaling, there still is a limitation in terms of noise reduction due to the power delivery networks (PDNs). These include techniques such as differential signaling. The disruption between the power and ground planes based on the low target impedance concept induces return path discontinuities during the data transitions, which create displacement current sources between the power and ground planes. These sources induce excessive power supply noise which can only be reduced by increasing the capacitance requirements through new technologies such as thin dielectrics, embedded capacitance, high frequency decoupling capacitors etc.

This dissertation primarily focused on developing new PDN schemes to isolate and reduce the switching noise on the PDN so as to prevent the noise coupling and propagation in a system. Two approaches have been used: one for suppressing the noise propagation by implementing an embedded EBG structure on the PDN, and the other for minimizing the noise generation by replacing the power plane with power transmission lines. The new PDN design proposed in this dissertation using power transmission lines (PTLs) enables both power and signal transmission lines to be referenced to the same ground plane so that a continuous current path can be formed. Extensive simulations and measurements are shown, using the PTL approach to demonstrate enhanced signal integrity as compared to the currently practiced approaches.

9.1 Contributions

Based on these objectives, the contribution of this research can be summarized as follows:

- **Development of a design technique for embedded electromagnetic band gap (EBG) structure in load board applications:** A configuration for embedded EBG is developed to suppress the propagation of SSN from noisy digital circuits to noise-sensitive analog circuits in mixed-signal systems. The problem of EBG losing its functionality when embedded in multiple layers has been analyzed. The design methodology has been proposed to be applied to practical PCB designs, and verified through the measurement of prototype test vehicles.

- **Design of the Constant Current Power Transmission Line (CCPTL) scheme:** To enable the new design for power delivery network (PDN) based on the PTL concept, the PTL-related issues are discussed first. The first signaling scheme proposed to address the issues associated with PTL is the Constant Current Power Transmission Line (CCPTL) scheme. It induces constant current through the PTL so that the CCPTL could be free from any impedance mismatch or discontinuity in the power supply path as well as from dynamic dc drop on the PDN. Test vehicles using off-the-shelf chips have been implemented to demonstrate the effectiveness of the CCPTL scheme. Then, custom-designed transmitters have been implemented in a 0.13 μm CMOS process. The measurement results show that the CCPTL scheme improves the quality of the received signal significantly in terms of voltage and timing margins.

- **Design of the Constant Voltage Power Transmission Line (CVPTL) scheme:** To address the dynamic dc drop with the reduced power penalty, the Constant Voltage Power Transmission Line (CVPTL) scheme has been proposed. It provides multiple

resistor paths implemented between the PTL and the power supply pin of the driver. The resistance of the power supply path is thus controlled to achieve a constant voltage at the power supply pin even with the varying amount of current through the PTL. The use of the CVPTL scheme increases the susceptibility of the PTL to the impedance mismatch effect so that multiple cases with large impedance mismatch have been simulated to quantify the performance degradation. Theoretical and simulation based analysis have shown that the CVPTL scheme outperforms the power plane scheme.

- **Design of the Pseudo Balanced Power Transmission Line (PBPTL) scheme:** A balanced signaling concept has been adopted to address the dynamic dc drop and the impedance mismatch issue of PTL. General balanced signaling has been modified to minimize the overhead in terms of off-chip PCB trace and I/O pin count while maintaining the same level of effectiveness, which is called pseudo-balanced signaling. It has been combined with PTL so as to further enhance the signal integrity. Pseudo-Balanced Power Transmission Line (PBPTL) scheme has been developed to induce constant current with reduced power penalty (e.g, 50% overhead in power consumption for 4-bit transmission). The PBPTL scheme has extended the application of the PTL-based PDN to multiple I/O drivers naturally by encoding the multiple bits of information prior to data transmission. The effectiveness of the scheme has been demonstrated through simulations and measurements. Both the off-the-shelf chip and custom-designed transmitter have been used to confirm the results.

- **Development of a methodology for the selection and placement of decoupling capacitors:** A methodology for the selection and placement of decoupling capacitors has been developed for the PTL-based PDN. The decoupling capacitor is needed to serve as a charge reservoir as the sudden demand for current is too large to be handled by PTL. Thus, the goal of the design methodology for the PTL-based PDN is

to determine the minimum amount of capacitance and maximum distance between the capacitor and the device so that the capacitor can supply sufficient amount of current to the device on time. Measurement results have been included to support the proposed methodology.

- **Investigation of the uniform PTL grid to supply power in a standardized manner:** To supply power to multiple I/O drivers in a standardized manner, the concept of uniform power grid using PTLs has been presented. The use of the periodically-arranged PTLs can ease PCB layout. The variable design parameters have been identified, and the effects of them on the waveform are investigated using simulations.

9.2 Publication

9.2.1 Journals

- Suzanne Huh and Madhavan Swaminathan, "Pseudo Balanced Power Transmission Line," to be submitted to IEEE Transactions on Circuits and Systems I, Nov. 2011.
- Suzanne Huh, Madhavan Swaminathan, and David Keezer, "Constant Current Power Transmission Line based Power Delivery Network for Single-Ended Signaling," IEEE Transactions on Electromagnetic Compatibility, vol. PP, no. 99, pp. 1-15, 2011.
- Suzanne Huh and Madhavan Swaminathan, "A Design Technique for Embedded Electromagnetic Band Gap Structure in Load Board Applications," IEEE Transactions on Electromagnetic Compatibility, vol. PP, no. 99, pp. 1-14, 2011.
- Nithya Sankaran, Suzanne Huh, Sunghwan Min, Madhavan Swaminathan and Rao Tummala, "Suppression of Vertical Electromagnetic Coupling in Multilayer Packages," IEEE Transactions on Advanced Packaging, in press, 2011.

9.2.2 Conferences

- Suzanne Huh and Madhavan Swaminathan; “Are Power Planes Necessary for High Speed Signaling?,” accepted to DesignCon, 2012.
- Suzanne Huh, Madhavan Swaminathan, David Keezer; “Design of Power Delivery Networks using Power Transmission Line for Multiple I/Os using Pseudo-Balanced Signaling,” accepted to IEEE 20th conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2011.
- Suzanne Huh, Madhavan Swaminathan, David Keezer; “Pseudo-Balanced Signaling Using Power Transmission Line for Parallel Links,” IEEE International Symposium on Electromagnetic Compatibility (EMC), pp. 871-876, Aug. 2011.
- Suzanne Huh, Madhavan Swaminathan, David Keezer; “Low-Noise Power Delivery Network Design using Power Transmission Line for Mixed-Signal Testing,” IEEE 17th IEEE International Mixed-Signal, Sensors, and Systems Test Workshop (IMS3TW), 2011.
- Suzanne Huh, Madhavan Swaminathan, David Keezer; “Constant Current Power Transmission Line based Power Delivery Network for Single-Ended Signaling with Reduced Simultaneous Switching Noise,” IEEE Workshop on Signal Propagation Interconnects (SPI), pp. 47-50, May 2011. (Nominated for Best Paper Award)
- Suzanne Huh, Daehyun Chung and Madhavan Swaminathan; "Near Zero SSN Power Delivery Networks Using Constant Voltage Power Transmission Lines," IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS), pp. 1-4, Dec. 2009.
- Suzanne Huh, Daehyun Chung and Madhavan Swaminathan; "Achieving Near Zero SSN Power Delivery Networks by Eliminating Power Planes and Using Constant Current Power Transmission Lines," IEEE 18th conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), pp.17-20, Oct. 2009.

- Fidel Muradali, Suzanne Huh, and Madhavan Swaminathan, "Load-Board/PCB Noise Suppression via Electromagnetic Band Gap Power Plane Patterning," IEEE 17th Asian Test Symposium (ATS), pp.195, Nov. 2008.
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- Nithya Sankaran, Suzanne Huh, Madhavan Swaminathan and Rao Tummala, "Suppression of Vertical coupling using Electromagnetic Band Gap structures," IEEE 17th conference on Electrical Performance of Electronic Packaging (EPEP), pp. 173-176, Oct. 2008.

9.2.3 Invention Disclosure

- Suzanne Huh and Madhavan Swaminathan, "Constant Current Power Transmission Line Based Power Delivery Network for Single-Ended Signaling with Reduced Simultaneous Switching Noise," Invention Disclosure ID: 5563, Mar. 2011, Provisional Patent Application filed by Georgia Tech.
- Suzanne Huh, Daehyun Chung, and Madhavan Swaminathan, "Constant Current Power Transmission Line and Constant Voltage Power Transmission Line," Invention Disclosure ID: 4967, Sept. 2009, Provisional Patent Application filed by Georgia Tech.

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