MODELING, DESIGN, FABRICATION AND RELIABILITY CHARACTERIZATION OF ULTRA-THIN, GLASS BGA PACKAGE-TO-BOARD INTERCONNECTIONS

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MODELING, DESIGN, FABRICATION AND RELIABILITY CHARACTERIZATION OF ULTRA-THIN, GLASS BGA PACKAGE-TO-BOARD INTERCONNECTIONS

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In memory of my aunt, Late Indira Singh,

Dedicated to parents and extended family…

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SUMMARY

The trend towards ultra-miniaturization, high interconnection densities with minimal power consumption at low cost is driving the need for large, thin, high-stiffness substrate technologies capable of lithographic design rules below 5µm and inducing low stress on ultra-low K dielectrics while retaining high dimensional stability. Low-CTE organic and silicon interposers have been proposed to address some of these concerns and achieve chip-level reliability at larger die sizes and reduced I/O pitches, below 40µm. However, such advanced substrates face critical reliability challenges at board level due to large CTE mismatch with the organic PCB. Glass substrates have emerged as a promising alternative to organic and silicon interposer packages due to their tailorable coefficient of thermal expansion (CTE), high dimensional stability and surface smoothness, outstanding electrical properties and low-cost panel-level processability.

The primary focus of this thesis work is to: i) demonstrate for the first time drop and fatigue performances of large, thin, glass packages directly mounted on PCB with conventional BGAs at 400µm SMT pitch; and ii) evaluate scalability of solder-based interconnections to larger body sizes or finer BGA pitches with low- and high-CTE glass packages and the most advanced interconnection materials. In addition to glass packaging, two key innovations are introduced. First, in the form of reworkable circumferential polymer collars providing strain relief at critical locations of high strain concentration in the solder joint. Second, in the form of novel Mn-doped SACM^{TM} solder to provide superior drop test performance without degrading thermomechanical reliability.

Finite-element modeling (FEM) was used to investigate the effectiveness of circumferential polymer collars as a strain-relief solution to improve fatigue performance. The models were built in 2D geometries to study the warpage response and predict the fatigue life of SAC105 interconnections at 400 µm pitch with an 18.5mm × 18.5mm glass package that was SMT-assembled onto an organic printed circuit board. The assemblies

with polymer collars not only indicated lower net package warpage, but also showed between 40 – 70 % improvements in fatigue life, as predicted by Coffin-Manson and Engelmaier-Wild models.

Daisy-chain test vehicles were designed to carry out systematic evaluation of 1) polymer collars on reliability performance of low- and high-CTE glass packages; 2) thermomechanical reliability of SACM^{TM} with system-level considerations, 3) drop and thermomechanical reliability of SACM^{TM} with considerations of pad surface finishes.

Experimental results from the first test vehicle demonstrated a 2X improvement in drop performance and 30% improvement in fatigue life. Failure analysis was performed using characterization techniques such as confocal surface acoustic microscopy (C-SAM), optical microscopy, X-ray imaging, and scanning electron microscopy / energy dispersive spectrometry (SEM/EDS). Model-to-experiment correlation was performed to validate the effectiveness of polymer collars as a strain-relief mechanism. For the second test vehicle, a baseline stencil-based paste printing process for fabrication of 250µm BGAs at 400µm pitch had to be developed to evaluate the SACM^{TM} solder which is currently available in paste form only. Shadow-Moiré warpage analysis was performed to explain the BGA balling and assembly yield. Thermal cycling test is ongoing, has reached 1000 thermal cycles, and will be pursued until failure. Fabrication of test wafers was completed on the third test vehicle and a systematic evaluation plan for comprehensive reliability testing was outlined for future work. These reliability studies demonstrated glass packaging as an ideal system integration platform for high performance, potentially enabling direct attach to the board of ultra-large, high-density 2.5D glass interposer packages.

CHAPTER 1

INTRODUCTION

Transistor scaling, which began in 1949, has made electronics the largest global industry with a $1.4T market in 2015 [1]. Advances in semiconductor technologies following Moore's Law have enabled integration of more than a billion transistors in a single integrated circuit (IC), resulting in rapid miniaturization of devices such as microprocessors that are used in today's servers, personal computers and mobile devices. While packaging of these devices was traditionally perceived as bringing minimal value to these applications, it now plays a key role in integration of heterogeneous functions as required by emerging electronic systems. Recent trends to miniaturized systems such as smartphones and wearables, as well as the rise of autonomous vehicles relying on smart in-car systems, have brought unprecedented integration challenges with escalating performance, functionality, and cost requirements impossible to meet by transistor scaling alone. A novel system scaling approach has been proposed by Georgia Tech to address these challenges and to achieve complete integration of heterogeneous microsystems, starting the "System Moore" era [1].

1.1 Transistor scaling to system scaling trends in microelectronics packaging

Consumer and high-performance applications have been aggressively driving advances in device technologies over the last decades to meet the escalating needs for high bandwidth and transmission speeds at low power and low cost. Transistor scaling, following Moore's Law, has enabled continuous advancements in logic and memory integrated circuits (ICs), including the introduction of ultra-low-K dielectrics to minimize

on-chip parasitics [2]. It also gave rise to the System-on-Chip (SOC) technology consisting of monolithic integration of multiple functions such as digital, analog, and radio-frequency circuitries in an IC. SOC focuses solely on the device integration and optimization of its performance, which means packaging brings little value and may be eliminated by wafer-level fan-out and embedding technologies. However, SOC integration faces many challenges from design and process complexity, bringing yield and cost issues, and limiting its applicability for complete system integration with many heterogeneous functions. Transistor scaling has also slowed down in recent years, diverging from Moore's Law, with no further cost reduction beyond the 14nm node, forcing the semiconductor industry to rethink its integration strategy.

More-than-Moore technology was subsequently pursued to achieve higher functional densities and integrate components at module level, such as vertically stacked ICs and packages (SIP) technology. Vertical stacking of thinned silicon ICs using standard wire-bonding and flip-chip technologies was proposed to address design complexities and latency issues observed in SOC. In SIP, through-silicon vias (TSVs) were implemented to achieve 3D integration while providing design flexibility and miniaturization. This, however, means that the performance of the system relies on the processing power of the ICs. Subsequently, this approach faces the same integration limitations as SOC [2]. The gap between transistor scaling (qualified by the gate length of a transistor) and system scaling (represented by off-chip interconnection pitch), shown in Fig. 1.1, indicates the need for a new paradigm for system integration and miniaturization [3].

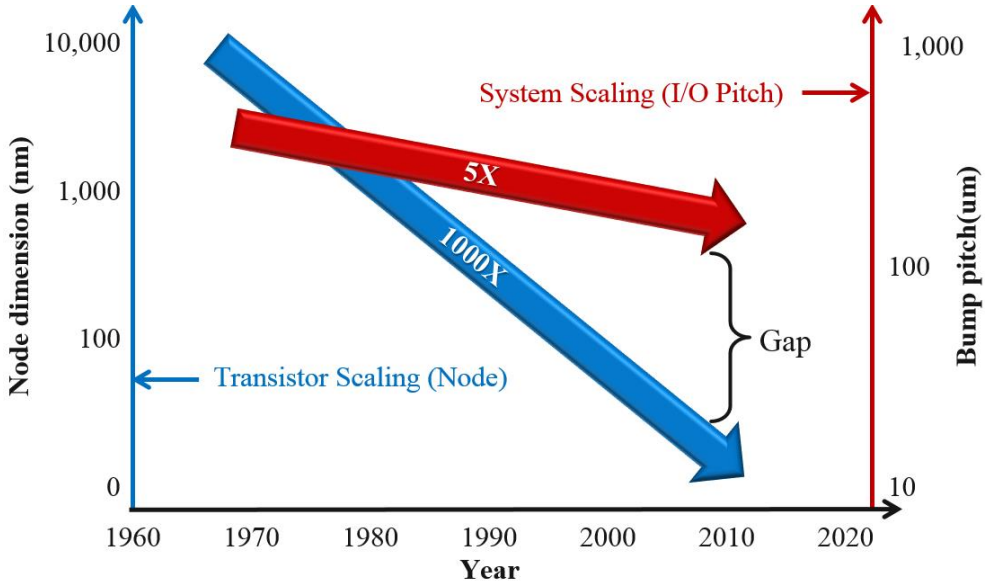

Figure 1.1: Gap between transistor and system scaling [3].

To address this fundamental challenge, the 3D Systems Packaging Research Center at Georgia Tech has been pioneering System-on-Package (SOP) to achieve complete system integration and miniaturization. The schematic of Fig. 1.2 introduces System Moore as the new frontier for system scaling, beyond Moore's and More than Moore's Laws. In the SOP approach, components, package, and system board are co-designed to realize all required heterogeneous functions of emerging electronic systems. Packaging now becomes a key enabler to reduce the overall system cost and size, thus it can add value to the system. An example reflecting this change is the recent trend of "die split" where large devices are split into multiple smaller ones to significantly improve yields and optimize cost [4]. Functionality is then reconstructed through the substrate with high-density die-to-die interconnections at pitches close to matching back-end-of-line (BEOL) technology. Advancing packaging technologies is therefore critical in the realization of SOP to enable next-generation ultra-miniaturized heterogeneous systems, from smartphones to autonomous vehicles and cloud computing.

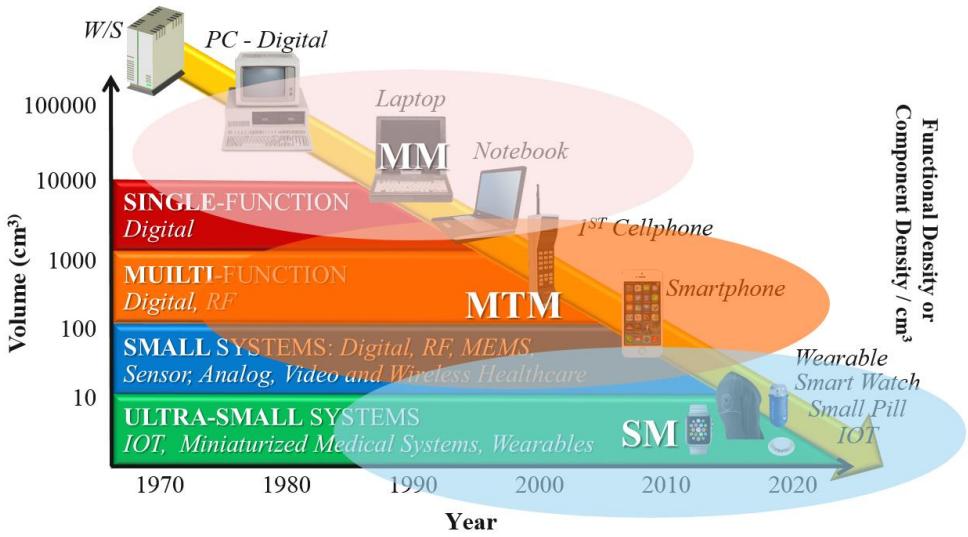

Figure 1.2: Increasing functional densities for next-generation ultra-small systems: system scaling by System Moore (SM) for heterogeneous integration beyond More of Moore (MM) and More than Moore (MTM) [1].

1.2 Board-level Interconnections and Reliability Requirements

Typical packaging solutions in Moore's Law era consisted in integration of Si devices onto organic packages, then assembled onto a system board using low-cost, surface-mount (SMT) compatible technologies. For the last two decades, solder-based ball grid array (BGA) interconnections have been the primary technology of choice for SMT assembly of microprocessor packages to printed circuit boards (PCBs). Package-to-board interconnections in modern consumer electronic products such as smartphones have to meet both drop and thermomechanical reliability requirements, as defined by JEDEC standards [5, 6]. The drop performance is conditioned by the ability of the solder material to absorb shock energy, driving towards soft solders with lower elastic modulus and yield strength.

The mismatch in coefficients of thermal expansion (CTE) between package and board brings cyclic strains in solder joints with variations in temperature acting as thermal loading. These strains are given by the equation below [7]:

$$\Delta\gamma\ \alpha\ \frac{L_{DNP}(\alpha_{PWB} - \alpha_{pack})\Delta T}{h} \qquad \text{(Eq. 1.1)}$$

in which L_{DNP} is the distance to the neutral point (DNP), between solder joint and the center of the package; h is the solder height; ΔT is the temperature change during each loading cycle; and α_{pack} and α_{PWB} are the CTEs of the package and PCB, respectively, as illustrated in Fig. 3. Accumulation of plastic strains under thermal cycling results in crack initiation and propagation in solder joints and, ultimately, in fatigue failures. Thermomechanical reliability is therefore conditioned by the ability of the solder material to prevent and accommodate plastic deformation, which is superior in hard solders with higher elastic modulus and yield strength.

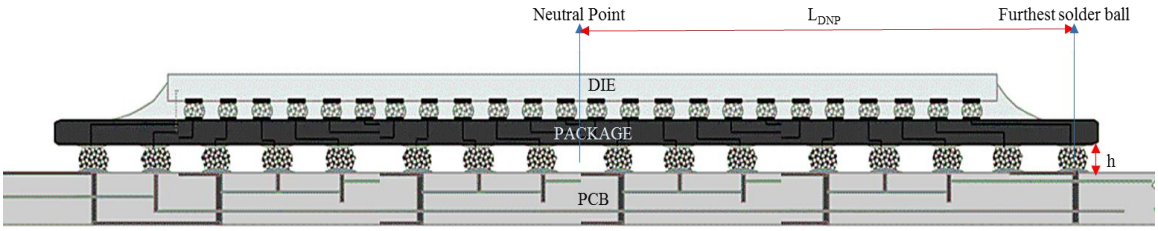

Figure 1.3: Die-package-board interconnections with large LDNP and low stand-off height.

Drop and thermal cycling reliabilities are consequently driving opposite material requirements for solders, but are equally critical to satisfy, bringing challenges for interconnection material design.

Reworkability is also highly desirable at board level, preventing the use of underfills, traditionally implemented to improve thermomechanical reliability at chip level.

1.3 Board-level reliability challenges with evolution of substrate technologies for system scaling

Demands for thinner consumer electronic products have led the trend for package thickness reduction. However, such reduction exacerbates substrate warpage, degrading SMT assembly yield and, subsequently, reliability. Further, increasing functional densities in emerging applications are driving the need for greater I/O count, and subsequently for larger die sizes at finer I/O pitches. Current packages are consequently expected to migrate to sizes larger than 20 mm x 20 mm with progressive reduction in pitch to below 40µm. Organic and silicon substrates with CTEs matching to Si chips have, therefore, gained momentum to meet chip-level reliability requirements and minimize stresses on low-K dielectrics. Such large, low-CTE substrates still have to be mounted onto a PCB, displacing the CTE mismatch to board level. To accommodate the increase in I/O count, the BGA pitch also needs to reduce to 400µm and below, further aggravating solder strains as per equation 1.1, and board-level reliability concerns. To address these challenges, an additional package layer was introduced between the low-CTE interposer and PCB to redistribute pitch and mitigate reliability. This 3-layer hierarchy, however, degrades electrical performance by increasing interconnect parasitics, and adds to the cost of the overall system. More recently, silicon interposers have gained importance in high-performance split-die applications as they satisfy sub-5µm lithographic design rules required for high-density die-to-die interconnections. These interposers frequently exceed 30mm x 40mm in body size, bringing unprecedented challenges for board-level thermomechanical reliability.

A novel 2-level packaging solution enabling direct, SMT interconnection of large and thin packages to the board is thus highly sought after by the semiconductor industry, as illustrated in Fig. 1.4.

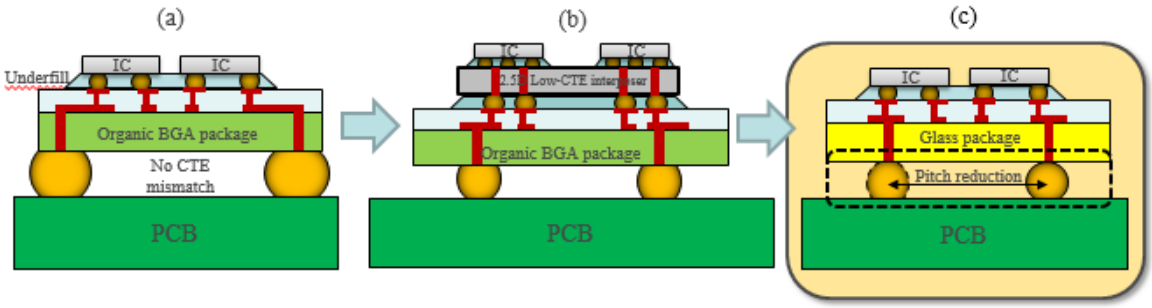

Figure 1.4: Traditional package approach (a) IC – organic BGA – PCB, current package (b) IC – low-CTE interposer – organic BGA – PCB, and new package approach (c) IC – large and thin glass package – PCB.

Glass substrates have emerged as a promising alternative to organic and silicon substrates for system scaling, owing to their:

- Excellent electrical properties, including low-dielectric constant, high resistivity, and low insertion losses as compared to silicon;
- Superior dimensional stability as compared to organic, enabling micron-level lithographic design rules;
- Tailorable CTE from silicon (~3ppm/K) to organic (14-17 ppm/K);
- High modulus and intrinsic strength for lower warpage as compared to organic;
- Panel-level to roll-to-roll processability for low cost [8, 9].

Benefitting from these unique properties, glass packaging can potentially address all aforementioned challenges for system scaling. The tailorable CTE and high modulus can mitigate warpage introduced by thickness reduction. Further, the tailorable CTE can

optimize chip- and board-level reliability. With glass, the desired 2-level hierarchy can therefore become possible, which has yet to be fully demonstrated.

1.4 Research objectives

The primary goals of this work are to: 1) demonstrate board-level reliability of large, thin, low- and high-CTE glass packages directly mounted on PCB with conventional BGAs at 400µm SMT pitch; and 2) evaluate scalability of solder-based interconnections in a 2-level hierarchy to larger body sizes or finer BGA pitches. The critical performance metrics associated with the research objectives, beyond prior art, are summarized in Table 1.1.

Table 1.1: Research objectives beyond prior art.

Metrics	**Conventional package**	**Current package**	**Research objectives**
Package size	Small up to 15mm x 15mm	Medium to large: up to 30mm x 40mm	18.5 mm × 18.5 mm
SMT pitch	> 500 µm	400 – 500 µm	400 µm
CTE mismatch	None	Large	Small to large
Hierarchy	Two-level	Three-level	Two-level
Manufacturability	SMT-compatibility	SMT-compatibility	SMT-compatibility Reworkability

1.5 Unique approach addressing technical challenges

The technical challenges faced by package-to-board interconnections in advanced package architectures can be summarized as follows:

- Aggravated solder strains and warpage with large, thin substrates at finer I/O SMT pitches, degrading thermomechanical reliability;
- Balanced drop and thermal cycling performances.

Proposed solutions also need to maintain SMT-compatibility and reworkability, as well as have minimal system-level impact.

Benefitting from its unique mechanical properties, glass is proposed to realize the research objectives and achieve, for the first time, board-level reliability of glass BGA packages at 18.5 mm x 18.5mm body size, 100µm thickness and 400µm SMT pitch. In GT-PRC's previous work at board level, superior thermal cycling reliability was demonstrated at 7.2mm x 7.2mm body size, passing up to 1300 thermal cycles with low-CTE glass [10]. This work was extended to 18.5mm x 18.5 mm but no clear conclusions could be reached from previous thermal cycling evaluation [13]. The drop test performance of glass BGA packages was never addressed.

In addition to glass packaging, two key innovations are introduced to further improve drop test and thermal cycling performances of glass BGA packages with minimal changes to current infrastructures and processes: 1) circumferential polymer collars; and 2) doped, lead-free solder alloys. The cross-section schematic of Fig. 1.5 illustrates the novelty of the proposed approach.

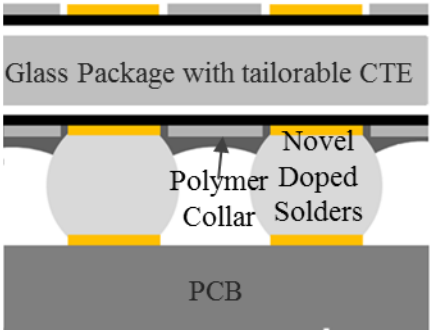

Figure 1.5: Unique approach for board-level reliability of large, thin glass BGA packages.

Circumferential polymer collars as reworkable underfills

Epoxy-based underfills with silica fillers have traditionally been used to improve thermomechanical reliability of solder-based interconnections at chip level. Underfills provide strain relief in solder joints by mechanically coupling device to package over the entire die footprint and mitigating their CTE mismatch. Application of underfills at board level is however undesirable as it compromises reworkability and has a strong system-level impact with alteration of substrate warpage and subsequent effect on chip-level reliability. Reinforced polymer collars have been proposed in wafer-level packaging (WLP) as a partial underfilling solution providing strain relief solely in locations of highest stress concentration, where failure would normally originate in the solder joints during thermal cycling. The Spheron^{TM} technology has been demonstrated to effectively improve fatigue life of solders by 30-50% [11, 12].

Georgia Tech PRC and its industry partner Namics Corporation Inc. have recently extended this concept at board level with a new class of filler-free epoxies with low modulus and high CTE. Circumferential polymer collars can be formed with varied thicknesses around the BGA solder joints by a spin-coating process, as shown in Fig. 1.6. The collar thickness was optimized as a trade-off between providing effective strain relief and meeting assembly manufacturability constraints of SMT compatibility and reworkability [13].

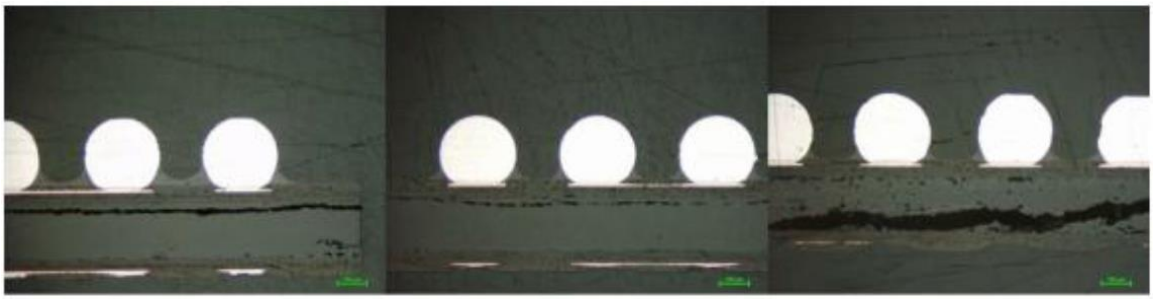

Figure 1.6: Optimization of collar thickness to provide best compromise of strain relief and reworkability [13].

This work goes beyond previous empirical studies by investigating the fundamental strain-relief mechanisms through modeling and experimental validation, with considerations of plastic strain distributions in solder BGAs and of substrate warpage.

Doped lead-free solder alloys

The ban of lead in 2006 by the Restriction of Hazardous Substances (RoHS) and the Waste Electrical and Electronic Equipment (WEEE) directives forced the semiconductor industry to drop their interconnection material of choice: eutectic tin-lead solder. Extensive research has been carried out to identify suitable lead-free replacements matching the outstanding physical properties, fatigue performance and manufacturability of eutectic tin-lead solder [14]. Among the potential candidates, SnAgCu (SAC) alloys have become prevalent over other lead-free solder systems benefitting from their low cost and superior properties such as relatively low melting point, excellent wettability, superior corrosion resistance and tailorable modulus and yield strength with variation of Ag content [15, 16]. Soft solders with low Ag content such as SAC105 are found more suitable for drop testing due to their lower yield strength, modulus, and higher ductility; while hard solders with higher Ag content such as SAC305, are more favorable to thermal cycling, as illustrated in Fig. 1.7 [17].

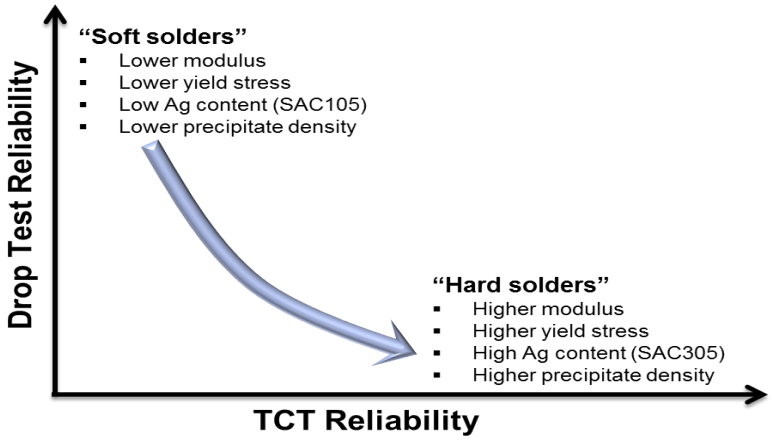

Figure 1.7: Contrasting solder requirements for drop test and thermomechanical reliability.

Improvements in fatigue life with standard SAC alloys thus come at the cost of the drop performance, which is equally critical in consumer products. Advances in solder materials are, therefore, required to achieve balanced thermomechanical and drop reliability. Solder properties are highly dependent on the alloy composition and microstructure, and can be selectively tailored by minor addition of other elements without affecting processability. Recently, Indium Corporation proceeded with systematic evaluation of dopants such as Ti, Ni, Bi, Y, Ni or Zn to optimize the properties of standard SAC alloys. This work resulted in the development of the Mn-doped SACM^{TM} alloy, which enables improved drop test performance as compared to SAC 105 with similar fatigue life than SAC305 [18]. However, the SACM^{TM} alloy is currently commercially available in paste form only, thus limiting its applicability to pitches of 500µm and above in high-volume manufacturing. In this work, the SACM^{TM} solder is evaluated, for the first time, at 400µm SMT pitch.

The proposed unique approach realizes the research objectives with novel strain-relief mechanisms and innovations in solder materials to improve board-level reliability of

ultra-thin glass BGA packages, and further extend the applicability of standard solder-based interconnections in package size and SMT pitch.

1.6 Thesis Tasks and Organization

The research accomplished in this thesis work is organized into six chapters. Chapter 1 introduced the transistor and system scaling trends, recent evolution of substrate technologies bringing reliability challenges at board level, the research objectives and unique approach proposed to address the technical challenges.

Chapter 2 consists of a detailed review of the state-of-the-art of board-level interconnection technologies. Prior art on polymer collars as a strain-relief mechanism as well as solder doping for improved drop and thermal cycling performances is also reported.

Chapter 3 summarizes finite element modeling pursued to gain an understanding of the fundamental mechanisms by which polymer collars improve thermomechanical reliability, including warpage considerations. The solder fatigue life predicted with both Coffin-Manson and Engelmaier-Wild models is reported as guidelines for the experimental evaluation of Chapter 4.

Chapter 4 details the design, fabrication and assembly of three test vehicles. The specific research tasks associated to each test vehicle (TV) are:

i) TV1: evaluation of the effect of polymer collars on the thermomechanical and drop performance of low- and high-CTE glass BGA packages;
ii) TV2: evaluation of thermomechanical reliability of glass BGA packages with doped solder alloys, comparing SACM^{TM} with standard SAC305 and SAC105;

iii) TV3: drop and accelerated thermal cycling tests with SACM^{TM}, considering the effect of pad surface finish.

Chapter 5 reports the results of reliability evaluations on the three test vehicles, with detailed failure analysis using characterization techniques such as confocal surface acoustic microscopy (C-SAM), optical microscopy, X-ray imaging, and scanning electron microscopy/energy dispersive spectrometry (SEM/EDS). Model-to-experiment correlation highlighting the effectiveness of polymer collars in relieving solder strains is also detailed.

Chapter 6 gives a summary of the overall research, aligning results with the defined research objectives. The chapter concludes with suggestions for future work, towards system-level reliability.

CHAPTER 2

LITERATURE REVIEW

This chapter starts with an overview of IC packaging and interconnection technologies along with an overview of the recent advances in multichip packaging with fine pitch and high I/O density. Material and process innovations to address fine-pitch challenges, such as advanced solders, pad surface finishes, and underfills for enhancing reliability performance are highlighted. Innovations to address reliability concerns through a variety of compliant interconnections pursued both in universities and industry are also briefly summarized. Finally, board-level reliability research previously accomplished at GT-PRC is reviewed.

2.1 Evolution of IC packaging

This section summarizes the evolution of electronics packaging from traditional single-chip packages to the complex state-of-the-art multi-chip packages driven by miniaturization, functionality and a dramatic increase in bandwidth requirements in high-performance systems. With reduced interconnection pitches and increasing package sizes, need for advances in board-level interconnections is further reinforced.

2.1.1 Traditional packaging

IC packaging evolved with small outline (SO) and single-chip packages (SCPs) that were individually attached to the PCB in order to meet the electrical, mechanical, and thermal requirements for low I/O applications. Dual-in-line (DIP) and quad-flat packages (QFN), later introduced for commercial use, consisted of metal leads that are distributed along the sides for interconnections. In the late 1980s, the limited I/O capability of DIP and

QFN for very large scale systems integration (VLSI) applications in low-end microprocessor and memory devices, led to the developments in area-array packaging. In the pin grid array (PGA) packages, higher I/O count could be achieved by distributing the pins throughout the package surface [4]. IBM was the first to demonstrate high-aspect ratio PGA packages made of low-temperature co-fired ceramic (LTCC) modules that are still currently in use for some high-performance computing applications [17]. In the mid-1990s, Intel also manufactured computer chips using PGA packages [18]. However, with PGA, the interconnection pitch reached its practical manufacturing limit and could not be further scaled down below 1mm.

Alternatively, the pins were replaced with solder balls to form ball grid arrays (BGA), significantly boosting the interconnection density. Conventionally, with PGA, mounting was performed using the through-hole method, in which the leads are inserted into holes drilled in printed circuit boards and soldered to the other side. However, with BGA, surface-mount devices (SMD) could be directly mounted onto the system board with pre-defined solder pads (with surface finish) by a pick-and-place machine and reflow (melting and cooling the solder under a specific temperature profile) to create adherence and electrical connections. Thus, surface-mount technology (SMT) advanced as a primary technique to directly mount packages onto PCB. This method enables reliable assembly of smaller components with high I/O density at lower cost and increased high-volume production throughputs. Furthermore, other added benefits include higher alignment error tolerance, double-sided circuit board placement, and overall better mechanical attributes.

The escalating yield and manufacturability challenges with large ICs eventually led to their partitioning into multiple devices that are then packaged into a multi-chip package

or multi-chip modules (MCM) as shown in Fig. 2.1 (a). IBM has pioneered the ceramic-based MCM for certain application-specific ICs (ASIC) and high-performance server systems [19]. Furthermore, Stacked ICs and Packages (SIP) enabled 3D stacking of multiple ICs for system miniaturization either by stacking of bare or packaged ICs by traditional wire-bonding or flip-chip technologies or by stacking of through silicon vias (TSVs) as shown in Fig 2.1 (b). TSV-enabled vertical chip-to-chip or chip-to-package interconnection reduces the interconnection length, thereby reducing signal latency. However, SIP has several limitations including heat generation, stress management, process integration, and fabrication of TSVs. Addressing the short-comings of SIPs, innovations in 2.5D and 3D package architectures are coming to the forefront.

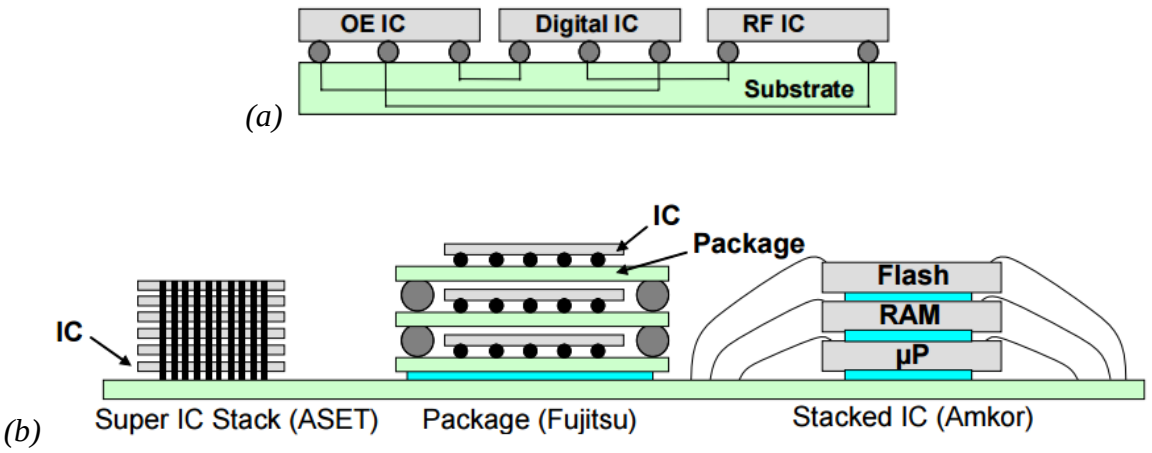

Figure 2.1: Schematic representation of (a) multi-chip module, (b) stacked IC and package.

2.1.2 Recent advances in multi-chip packaging

With emerging trends towards miniaturization and system scaling, over the last decade, 2.5D and 3D package integration are gaining prominence in the quest for low-latency, ultra-high I/O density, low-power interconnection, shorter off-chip interconnection pitch, large package sizes, and low cost.

In a typical 2.5D architecture, the ICs are integrated side-by-side through multiple layers of intertwined copper wirings and metalized through package vias (TPVs) in the interposer or package. Copper traces featuring ultra-fine lines and spaces allow for short interconnections between ICs, enabling high-speed signal transmission. The dies are interconnected by standard reflow or thermocompression bonding (TCB) techniques on high-density interposers then assembled onto organic substrates. Finally, SMT assembly of the organic substrate connects the die to the system board. In 2010, Xilinx demonstrated successful 2.5D integration with heterogeneous dies on a Si interposer as shown in Fig. 2.2 (a) [20]. SK Hynix's HBM in Fig. 2.2 (b) also illustrates this 3-level hierarchy with 4HBM stacks and a GPU assembled on a 30mm x 38mm Si interposer [21].

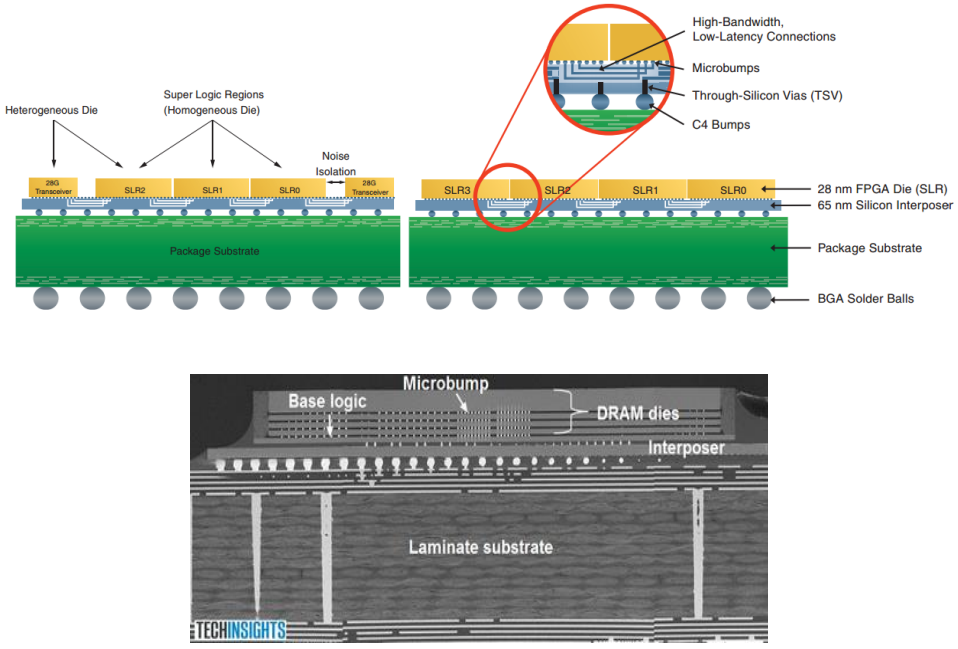

Figure 2.2: 2.5D silicon interposer from (a) Xilinx and (b) Hynix.

Si, however, suffers from high signal losses due to dielectric and conductor losses and high cost due to small 300 mm size wafer processing and manufacturing. Further, in order to compensate for the CTE mismatch between Si and organic PCB, there is a need

for an additional organic BGA package between interposer and system board. Low-CTE organic interposers are being developed to overcome the limitations of Si interposers, but are fundamentally limited in I/O density. In both cases, concerns over board-level thermomechanical reliability are further aggravated by the recent trends towards SMT pitch scaling, below 400µm, reduced substrate thicknesses and larger packages sizes.

Glass substrates have emerged as a promising alternative to organic and silicon interposer packages due to their tailorable CTE, high dimensional stability and surface smoothness, outstanding electrical properties and low-cost panel-level processability. GT-PRC has been pioneering glass packaging research since the last six years and has demonstrated 2.5D packages (Fig. 2.3), composed of ultra-thin glass, 100µm in thickness. Glass substrates are readily available both in low-CTE (3.8 ppm/°C) and high-CTE (9.8 ppm/°C) in large panel sizes or roll-to-roll form. Through glass vias at as low as 30µm pitch and fine-pitch RDL with microvias at less than 10µm enable 40µm chip-level I/O pitches in development and 20 µm pitch in research [22].

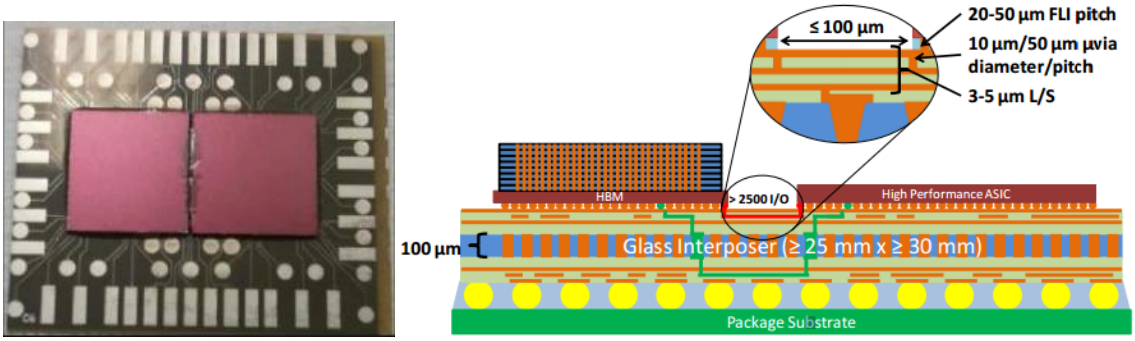

Figure 2.3: Georgia Tech's 2.5D Glass Interposer Package.

The packaging industry has been innovating several other interconnection techniques including Intel's Embedded Multi-die Interconnect Bridge (EMIB), fan-out wafer-level packaging platform (FOWLP), Amkor's Silicon-Less Integrated Module

(SLIM), and Silicon Wafer Integrated Fan-out Technology (SWIFT) which are also briefly reviewed.

Intel EMIB (Embedded Interconnect Bridge)

EMIB simplifies the 2.5D approach for high-density interconnections between heterogeneous dies on a single package. The key innovation in this technology is that instead of utilizing a silicon interposer with TSVs, a small silicon bridge is embedded with multilayer RDL in the package, enabling very high density die-to-die interconnections. Intel announced availability of EMIB technology to 14nm foundry customers in 2015. EMIB aims at cost-effective fabrication by eliminating Si interposer with TSV while also reducing the number of assembly steps as shown in Fig. 2.4 [23].

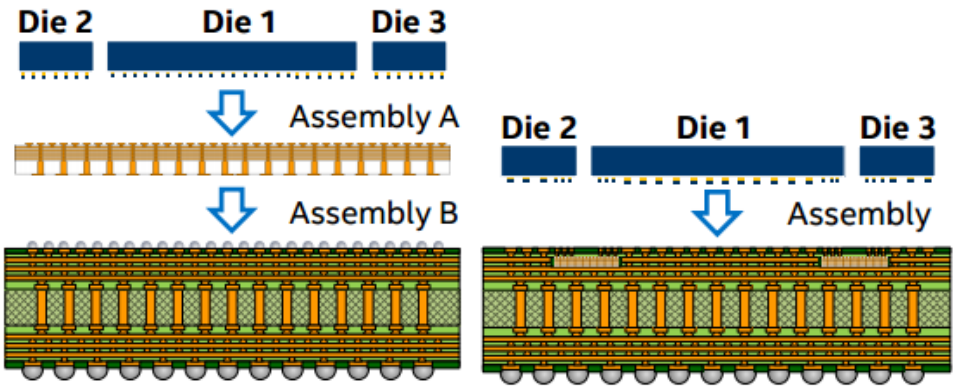

Figure 2.4: Conventional 2.5D assembly (left), Intel's EMIB assembly (right).

FOWLP (Fan-out Wafer-Level Packaging)

FOWLP provides a versatile platform for 2D, 2.5D and 3D integration with higher I/O density at low cost. It also offers advantages over conventional wafer-level packaging (WLP) such as more real estate for higher I/O counts, testability by probing pads on fan-out wafers to evaluate known good dies (KGD), protection from the mold compound that prevents die sidewalls from chipping/cracking during SMT assembly, heterogeneous integration with actives and passives with fine line and space for high-density routability. Therefore, FOWLP enables miniaturization with

smaller form factors, eliminating the need for chip-package interconnections and substrates, thereby enabling excellent electrical performance due to shorter interconnections, leading to lower parasitics. Steps to achieve FOWLP are shown in Fig. 2.5 (Courtesy of Beth Keser, Qualcomm) [24]. Companies such as TSMC, STATS ChipPac, Infineon and Nanium have developed their own variations of FOWLP [25].

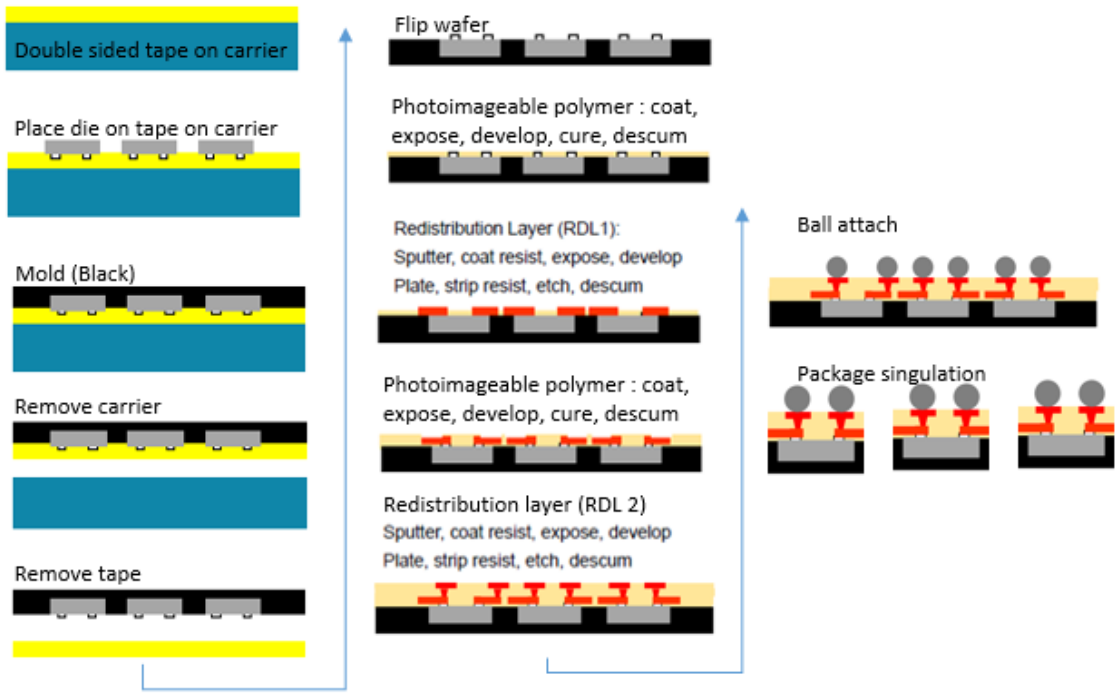

Figure 2.5: Process flow to achieve FOWLP - Courtesy of Beth Keser (Qualcomm Inc.), Guest Lecture on WLP, CPMT

In 2015, Amkor Technology Inc. announced their SLIM and SWIFT technologies (Fig. 2.6). Like EMIB, SLIM is an alternative approach eliminating Si interposer, improving upon 2.5D and fan-out design. It is a dies-last package technology, offering compact form factors with highest level of integration, combining traditional back end of the line (BEOL) and assembly fan-out architectures. SWIFT, on the other hand, addresses shortcomings associated with conventional fan-out. High performance is attributed to integration of advanced polymer-based dielectrics, heterogeneous integration of multi-dies,

interconnection densities below 2/2µm line and space, Cu-pillar interconnections at 30µm pitch and capability of large package body sizes [26, 27].

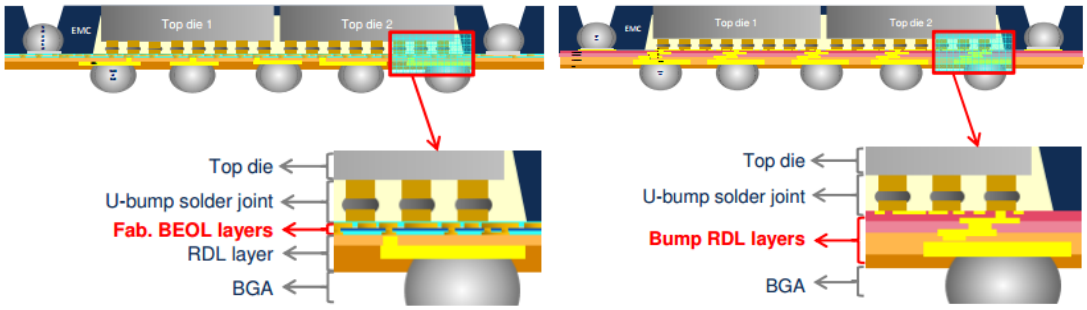

Figure 2.6: Amkor Technology Inc's SLIM (left) and SWIFT (right).

2.2 Recent material developments in board-level interconnections

With all the aforementioned state-of-the-art technologies, a common emerging trend is the aggressive scaling of interconnection pitches at chip level and shift to larger package body sizes. Therefore, improving thermomechanical performance at board level without degrading reliability at chip level is a grand engineering challenge. In parallel, with the SMT pitch scaling below 400µm, concerns over board-level reliability are further aggravated due to higher solder strains and warpage. Advances in material development in existing technologies at the board-level including pad surface finishes, standard SAC solders and underfills are studied in this section.

As mentioned in Chapter 1, BGAs generally composed of standard SAC alloys are used to form metallurgical joints between the copper pads on the package and the board. The copper pads are generally covered by a thin layer of surface finish providing a suitable surface for soldering and formation of intermetallics (IMCs). Upon reflow, the solder melts above its melting point, wetting the surface of the copper pad. During wetting, the melt partially dissolves the thin surface finish and the underlying elements, up to their solubility

limits, forming IMCs due to diffusion phenomenon [28]. In this interfacial reaction, the growth kinetics that determine the IMC thickness are governed by the parabolic growth law:

$$L = (Dt)^{\frac{1}{2}} \qquad \text{(Eq. 2.1)}$$

where 'L' is the average thickness of the IMC layer, D is the temperature dependent diffusion coefficient, and 't' represents the time. IMCs are generally composed of ordered alloy phases of two or more metals in a narrow compositional range. They are vital in providing mechanical joint strength and chemical stability [29].

2.2.1 Advances in pad surface finishes

Pad surface finishes play a critical role in determining reliable solder joint formation with excellent solderability and IMC formation. Some traditionally used surface finishes include hot air solder leveling (HASL), organic solderability preservative (OSP), immersion Sn (ImSn) and immersion Ag (ImAg).

HASL, despite its excellent solderability and low cost, is non-uniform and, hence, not suitable for fine-pitch applications. OSP has a short operating window between assembly stages and is highly prone to oxidation [30]. ImSn has concerns with tin whisker formation and ImAg requires special handling and is more expensive [31]. Table 2.1 highlights the critical attributes and summarizes the pros and cons of the above mentioned surface finishes.

Table 2.1: Summary of pros and cons of HASL, OSP, ImSn and Imag [31].

Surface finish attributes	**HASL**	**OSP**	**ImSn**	**ImAg**
Solderability				
Long shelf life				
Surface oxidation				
Tin whisker formation concerns				
Applicability at fine-pitch				
Uniformity/flatness				
Low cost				

Addressing the technical limitations of above-mentioned pad finishes, two popular technologies in practice today are electroless nickel immersion gold (ENIG) and electroless nickel electroless palladium immersion gold (ENEPIG). With these surface finishes, two predominant intermetallics are formed, Cu_6Sn_5, and Ni_3Sn_4. Table 2.2 summarizes the primary and secondary IMCs formed with SAC solders with OSP, ENIG and ENEPIG surface finishes [32].

Table 2.2: Primary and secondary IMCs formed with common pad surface finishes

Surface Finish	**Primary IMCs**	**Secondary IMCs**
OSP	Cu_6Sn_5	Cu_3Sn
ENIG	Cu_6Sn_5, Ni_3Sn_4	$(Cu,Ni)_6Sn_5$, Cu_3Sn, Ni-Sn-P, Ni_3P
ENEPIG	Cu_6Sn_5 , Ni_3Sn_4	$(Cu,Ni)_6Sn_5$, Cu_3Sn, Ni-Sn-P, Ni_3P

During reflow, the solder dissolves the thin protective gold layer and some portion of the Ni (in ENIG and ENEPIG), which also acts as diffusion barrier between the solder

and copper, retarding excessive IMC growth. Fig. 2.7 indicates the finer IMC thickness in cases of ENEPIG in comparison to ENIG after reflow and 1000 hours of thermal aging at 125°C. Several literature studies have indicated higher reliability with ENEPIG in comparison to ENIG, in both thermal cycling and drop test [33, 34, and 35]. In case of ENEPIG (and EPAG), the palladium (Pd) layer further acts as an advanced diffusion barrier [36].

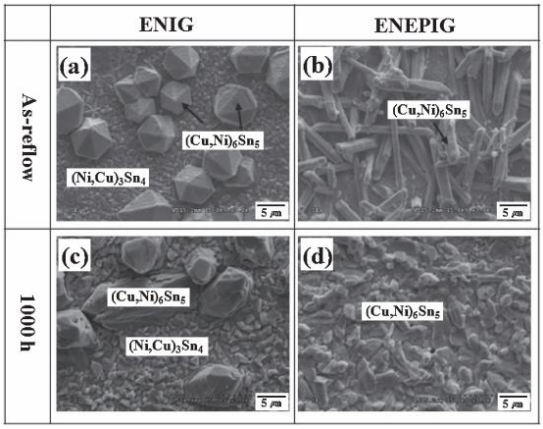

Figure 2.7: IMC thickness for ENIG and ENEPIG after reflow (a) and (b); and after 1000 hours of thermal aging (c) and (d).

The thickness of the IMC formed is dependent on the reflow time and number of reflow cycles as shown in Fig. 2.8 [37]. According to the standards defined in JEDEC, JESD22-A104D, two additional reflows are required before initiating thermal cycling reliability testing [38]. The IMCs grow further during thermal ageing or cycling. Presence of continuous brittle IMC layers often serves as ideal initiation sites for crack origin and propagation leading to interfacial fractures [39].

IMC thickness is therefore a critical factor in determining the interfacial strength between the solder and the surface finish. Further, with the low % (1 – 4%) of silver in SAC alloys, brittle needle-shaped Ag_3Sn are formed in addition to Cu_6Sn_5, which are

known to be detrimental to reliability performance [40]. Thus, lower IMC thickness is desired for both TCT and drop test reliability.

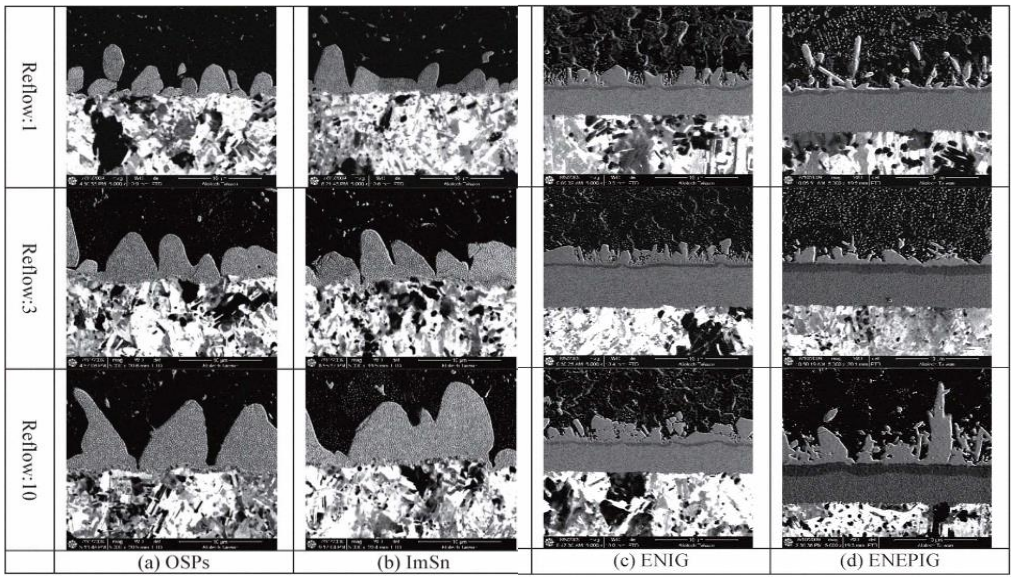

Figure 2.8: Progression of IMC growth after multiple reflow cycles with various pad surface finishes.

In emerging high-performance systems, the 'die split' trend is driving the need for high-density interconnections at sub-5um pitch. ENIG and ENEPIG, with nickel thicknesses, ~5 to 7µm, finishes impede their pitch scalability and applicability with sub-10µm gaps between traces. New, ultra-thin surface finish technologies with a fine control of extraneous plating are thus required to enable high-density wiring at finer pitches, and meet the integration and performance needs of tomorrow's computing systems. The electroless Pd autocatalytic Au (EPAG) finish has been developed by Atotech GmBH as a novel solution for fine-pitch applications. With thicknesses in the 50-150nm range, it enables a gap loss between traces of less than 5%, while improving insertion losses |S21| at 67 GHz by 1 dB [41]. EPAG therefore is an ideal finish for chip assembly, but its board-level reliability performance is yet to be qualified.

2.2.2 Advances in standard solders by doping

Besides the advances in pad surface finishes, developments in solders by refining microstructure with introduction of dopants have been extensively researched. Standard SAC alloys with doped alloying elements such as Germanium (Ge), Nickel (Ni), Manganese (Mn), Cerium (Ce), Bismuth (Bi), Titanium (Ti), and Yttrium (Y) have been recently studied due to their low melting points and low solid solubilities in the dominant phase within the rich β-Sn matrix [42]. After reflow and solidification, doping is reported to refine solder microstructure by making the grains finer, and improving the tensile and creep resistance in lead-free solders. Precipitation of heterogeneous intermetallic compounds along the interfaces can hinder dislocation motion, reduce grain boundary sliding and increase fracture resistance [43, 44].

Lin et al. have studied alloying modifications of SAC105 (Sn-1.0Ag-0.5Cu) with Mn and Ti to analyze the resulting microstructure and solidification behavior. It was found that the Mn and Ti dopants dramatically reduce the required undercooling for initiating crystal nucleation, and refine the extended volume fraction of pro-eutectic Sn. Addition of Mn and Ti refined the morphology of Sn dendrites by formation of heterogeneous IMCs such as $MnSn_2$ and Ti_2Sn_3, which also hindered the formation of detrimental intermetallics such as Ag_3Sn and suppressed the thickness of Cu_6Sn_5. The microstructures of SAC305, SAC105, and SAC 105 with 0.15Mn, 0.5Mn, 0.15Ti and 0.5Ti are shown in Fig. 2.9 a–f. With dopants, finer precipitates with inclusions of heterogeneous IMCs along the grains can be observed in Fig. 2.9 c-f [45].

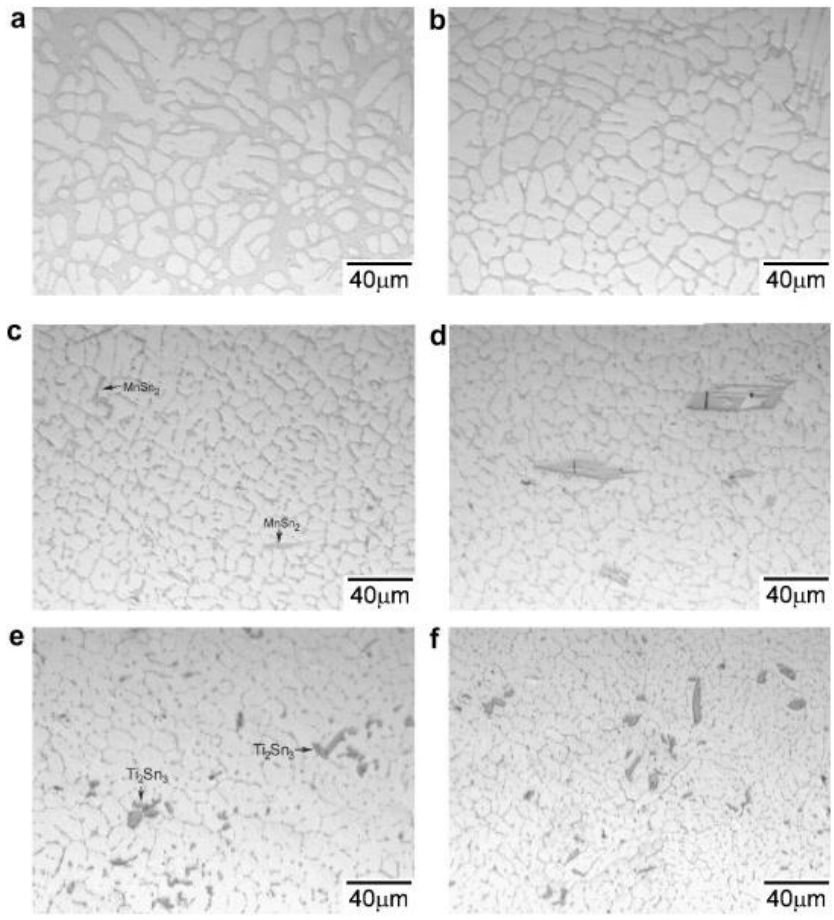

Figure 2.9: Microstructures of (a) SAC305, (b) SAC105, (c) SAC105 + 0.15Mn, (d) SAC105 + 0.5Mn, (e) SAC105 + 0.15Ti and (f) SAC105 + 0.5Ti [45].

Formation of heterogeneous IMC is attributed to reduction in undercooling by 4°. Consistent with classical thermodynamics explanation, with lower undercooling, the driving force or Gibbs free energy for formation of non-faceted heterogeneous IMC is lower than that of faceted or crystalline IMCs like Cu_6Sn_5 and Ag_3Sn. The cooling curve shown in Fig. 2.10 for low Ag SAC alloy and simplified pseudo-binary phase diagram illustrates the shift in eutectic and reduced undercooling (ΔT) with introduction of Mn or Ti. The extended volume fraction of β-Sn, although by reducing the elastic modulus, benefits drop performance, distribution of hard heterogeneous $MnSn_2$ and Ti_2Sn_3 provides a strengthening effect improving the fatigue life of the solder [45].

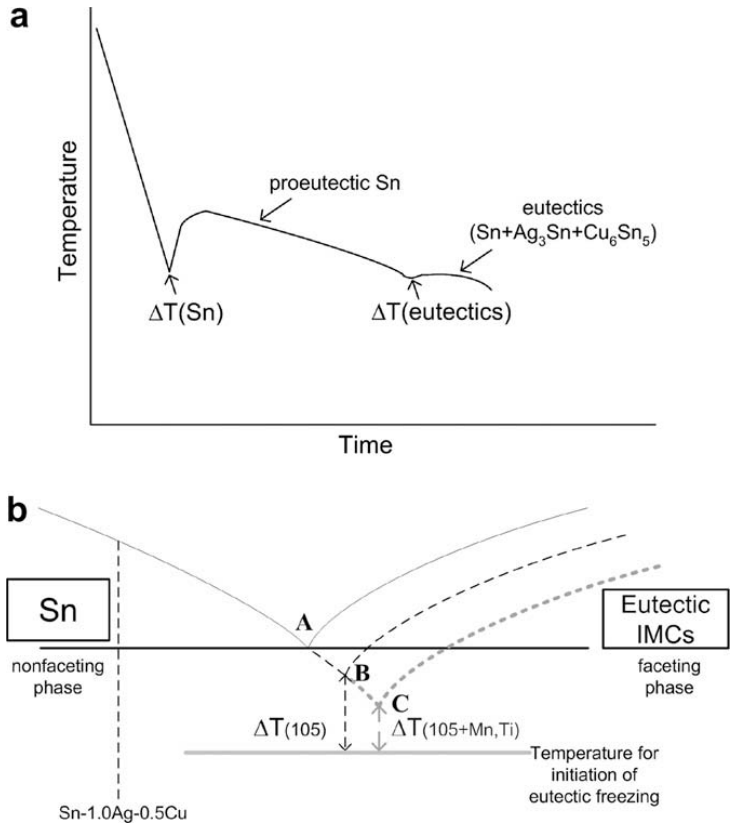

Figure 2.10: Cooling curve (a) for low Ag SAC solder and (b) simplified binary phase diagram with variation in undercooling.

Liu and Lee (Indium Incorporation) have investigated various dopants in SAC alloys including Ge, Ni, Mn, Ce, Bi, Y, and Ti. With SAC305, SAC387, SAC105 and Sn37Pb as reference, the study of 17 different variations of SAC alloys with dopants revealed SAC105 + .13% Mn as the best proposition for balanced drop test and thermal cycling reliability. The drop test results for this study are detailed in Fig. 2.11 [46].

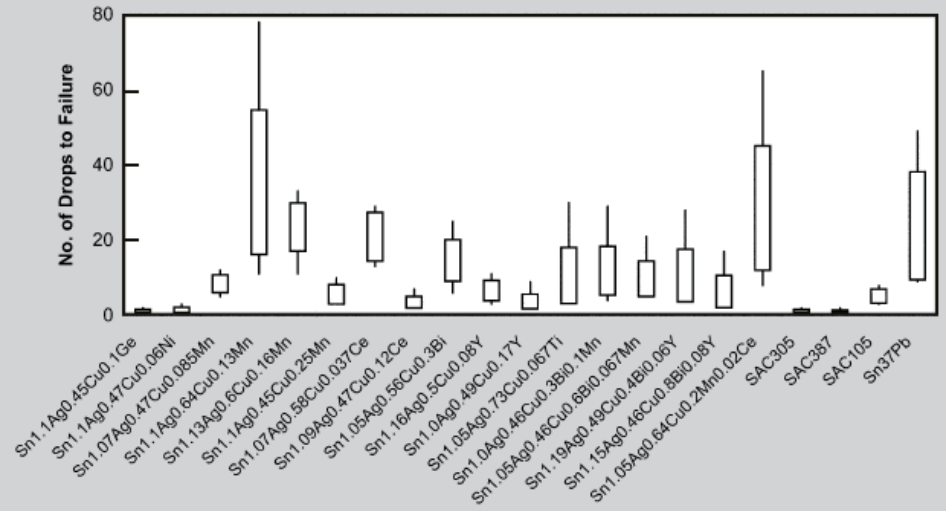

Figure 2.11: Drop test reliability of SAC solder with dopants.

Based on their experimental findings, Indium commerciallized SACM^{TM} in 2015 as an alternative low Ag content standard SAC solder, addressing the trade-offs between excellent thermal cycling fatigue life and drop shock resistance. Even with low Ag content (1%), SACM^{TM} delivers better thermal cycling reliability than that of SAC305 while also offering upto 7x improvements in drop test reliability in comparision to SAC105. The Weibull distrubution plot for thermal cycling results achieved with SnPb, SAC105, SAC305 and SACM are shown in Fig. 2.12 [47]. The superior performance of SACM was attributed to refined microstructure and enhanced interfacial bond strength with inhibition of rapid IMC growth.

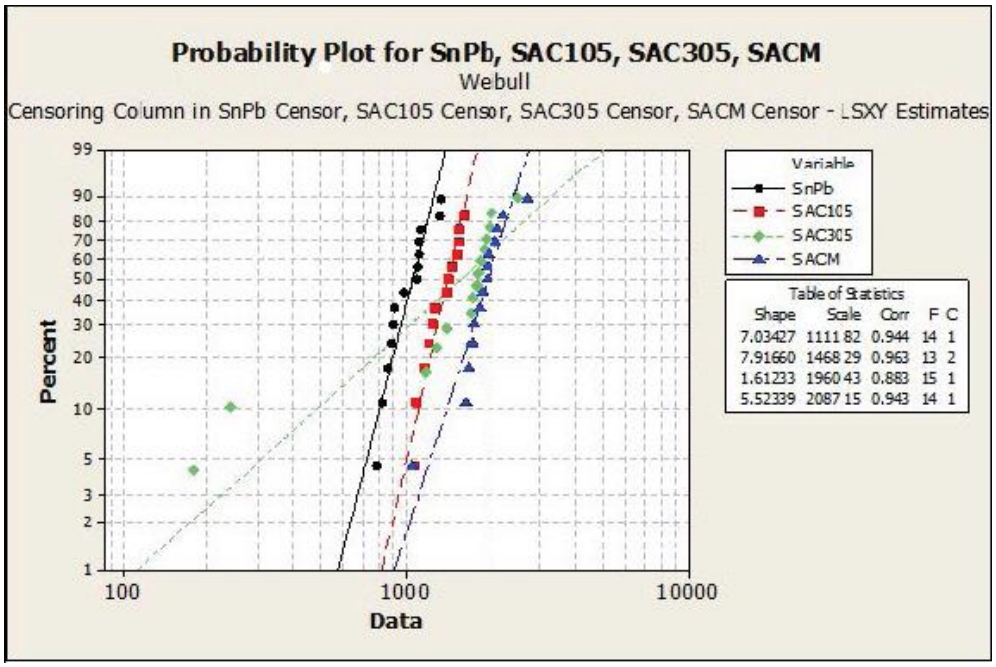

Figure 2.12: Thermal cycling results for SnPb, SAC105, SAC305 and SACM^{TM}.

Lee et. al also confirmed lower IMC thickness in SACM on either sides of the solder joint as indicated in Fig. 2.13, with NiAu and OSP pad surface finishes [47]. SACM, however, is currently available in only paste form limiting its applicability at pitch sizes above 500µm.

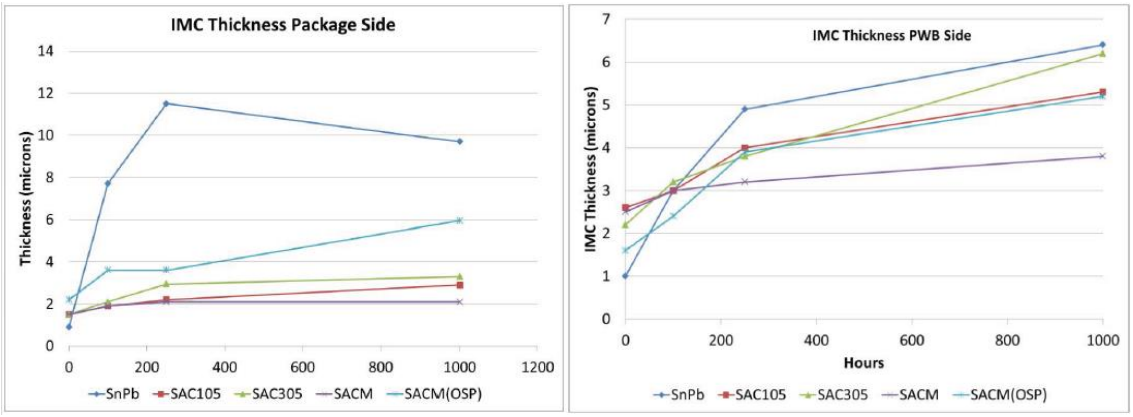

Figure 2.13: IMC thickness on package and PCB side.

2.2.3 Advances in underfill materials

Underfills are primarily used to enhance reliability of chip-level interconnections by redistributing the stresses away from the solder joints. Underfills prevent reworkability, which is an important criterion for board-level assembly. Therefore, they are not widely used for board-level interconnections. Few recent advances in underfills that are of interest are briefly highlighted here.

Novel underfills have been in development for solder joint protection, while ensuring low warpage in ultra-low K dielectrics. Henkel has produced Loctite 3536, which is an advanced low-temperature fast-curing underfill, delivering excellent protection for solder joints, specifically against mechanical strains produced under shock and vibrational testing [48]. Namics Inc. has also manufactured novel SUF underfills with advanced fillers that have high modulus of elasticity and low-glass transition temperatures, enhancing thermal cycling performance and impact resistance [49].

Delo GmbH also offers a commercially available, application-friendly, novel encapsulant that acts both as an underfill and overmold solution (Fig. 2.14). After the component assembly is completed, the procedure involves a two-step application process with dam stacking along the peripheral region with high-viscosity beads and then dispensing low-viscosity fill compound, followed by low-temperature curing.

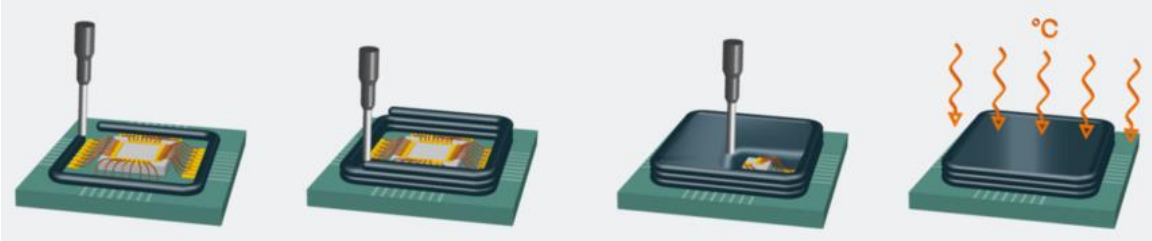

Figure 2.14: Delo's novel encapsulant that acts as underfill and overmold.

The encapsulant material is formulated on the basis of novel anhydride-curing epoxies which show excellent resistance to moisture absorption and chemicals at elevated temperatures. This enables encapsulation and formation of a hermetic seal in a single process for the entire panel (or a single part) with uniformity, while also ensuring minimum voiding and warpage related concerns. Furthermore, the curing kinetics can be tuned for low-temperature curing or quick high-temperature curing based on specific assembly requirements [50].

2.3 Strain-relief by compliant interconnections

In order to improve reliability of both chip- and board-level interconnections, a variety of compliant interconnections have been reported in the literature. These interconnection approaches mitigate stresses by accommodating the differential expansion through their displacement from high compliance.

Compliant solder balls

The effective modulus of solder balls can be reduced by replacing bulk of the metal core with low-modulus polymers. BGA arrays are fabricated with a polymer core (Fig 2.15) formed by co-polymerization of divinylbenzene, encompassed by two alternating metal plating layers of copper and nickel, a thin silver-tin solder layer and a final doped nickel layer. The relatively high CTE of the polymer core redistributes the strain uniformly with stress concentration in the middle. The first nickel layer forms a barrier between copper and solder layers, while the doped nickel controls IMC between the solder ball shell and the copper pad on the package side. A 2x – 3x improvement in thermal cycling test was observed in comparison to SAC305. A major limitation of this approach is the complex and expensive fabrication of the solder balls [51].

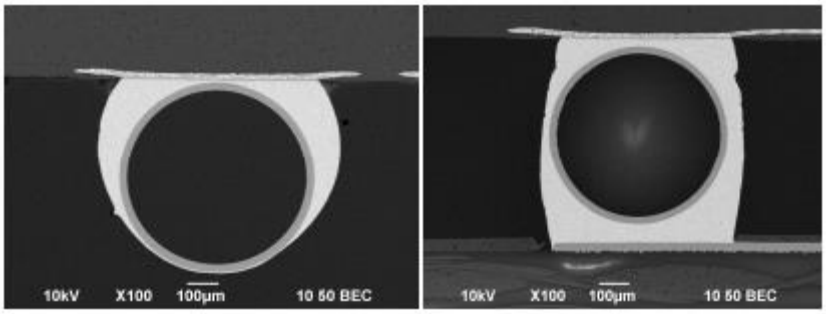

Figure 2.15: Cross-section of polymer core solder ball after balling (left) and assembly (right).

Other approaches such as embedding the solder balls in a stress redistribution layer [52] and printed silicone bumps [53] have also been demonstrated to add compliance and alleviate stresses within the interconnection structure.

Compliant metal interconnections

Compliant interconnections accommodate the CTE mismatch between the die and the substrate during the thermal cycling by easily moving or deforming in the *x*, *y*, and *z* directions to provide stress and strain relief in the interconnection. By undergoing differential displacement that mechanically decouples the die from the substrate, these interconnections have been demonstrated to improve reliability performance [52]. The Computer Aided Simulation of Packaging Reliability (CASPAR) Lab at Georgia Tech has pioneered such interconnections by modeling, design and validation through experimental prototypes to demonstrate the feasibility of such an interconnection system. Figure 2.16 shows a schematic and SEM images of the 3-arm fan structured interconnect (top) vs. simulation model (bottom) [53].

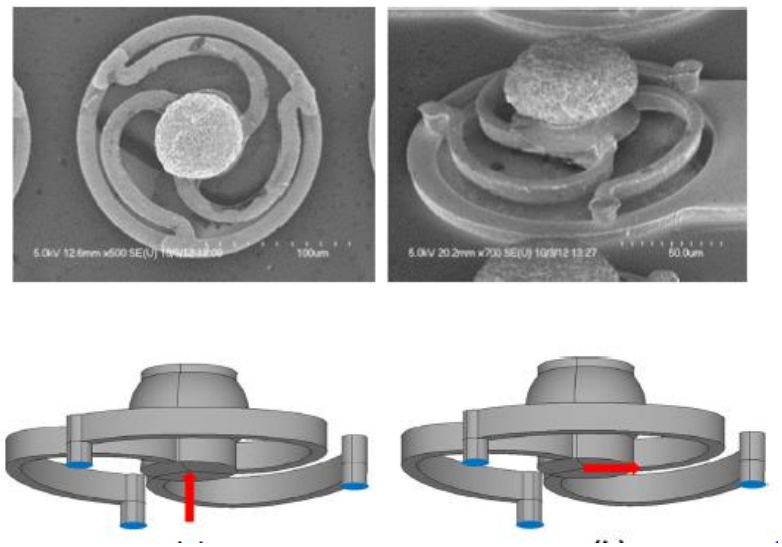

Figure 2.16: Multi-path complaint structures - SEM image (top), simulations (bottom).

Similar metal-based compliant interconnections fabricated using thin-film fabrication processes have also been reported by others. These include the micro-spring [56], and stress-engineered compliant interconnections [57] as shown in Fig. 2.17. The metal used in both of these structures is molybedenunchromium (MoCr) which is known to have a large stress gradient of 2GPa/µm that aids in the creation of compliant structures which provide the strain-relief mechanism.

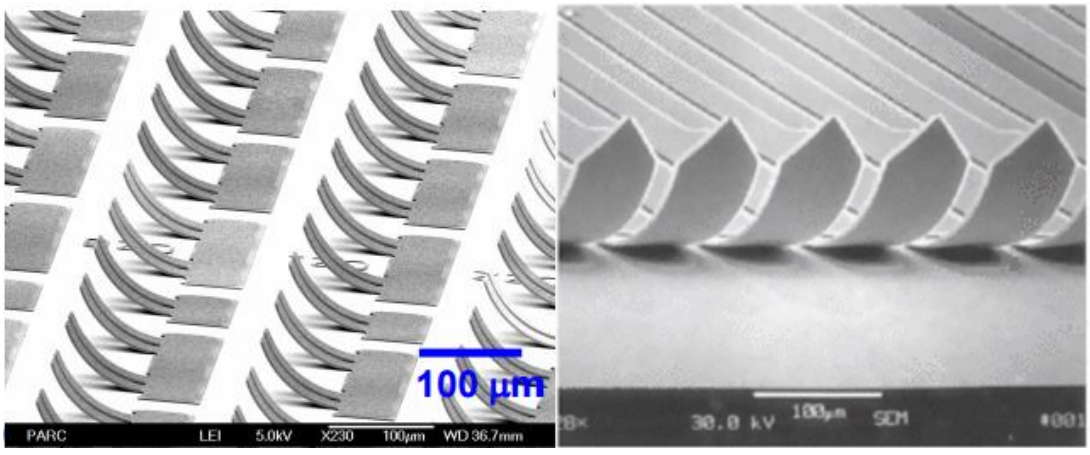

Figure 2.17: Micro-spring (left) and stress-engineered compliant interconnections (right).

Other compliant wafer-level packaging approaches have been demonstrated at chip level, that may also be applicable at board level, including: copper pillar by Advanpack Solutions (APS, Singapore) [58], bed of nails by the Institute of Microelectronics (IME, Singapore) [59], double-ball wafer-level packaging (WLP) technology by NEC and Fraunhofer (IZM) [60], compliant interconnects by Tessera [61], and ELAStec WLP by Infineon and IZM [62].

2.4 Previous research at GT-PRC on package-to-board interconnections

Compliant micro-wire arrays

Novel-stress-relief structures using copper micro wire arrays (MWA) as shown in Fig. 2.18 were explored as a unique low-cost SMT-compatible, stress-relief solution for reliable package-to-board interconnections. The MWA were pre-fabricated in ultra-thin carriers and then assembled as a stress-relief interlayer in between the package and the PWB. The MWA dramatically reduced interconnection strains even with large package sizes (18.5 mm x 18.5 mm) at 400μm pitch without the need for board-level underfill [63].

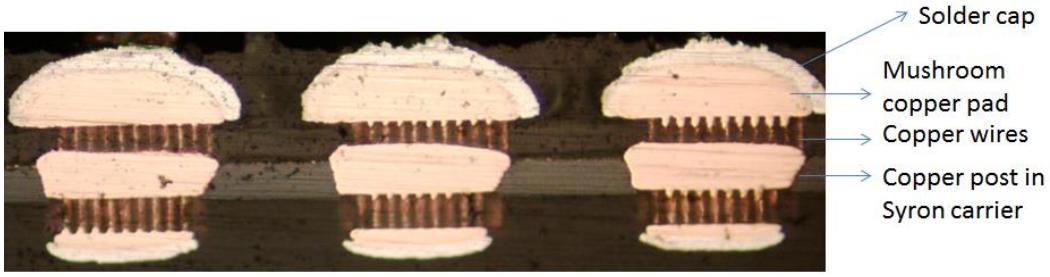

Figure 2.18: Cross section of MWA interconnections.

Dielectric build-up layers for stress buffering

GT-PRC also demonstrated the use of low-modulus dielectric build-up layers on either side of the glass to enhance the thermomechanical reliability of packages by

providing stress relief. This approach was demonstrated with 7.2mm x 7.2mm and 18.5mm x 18.5mm packages, with low- and high-CTE, 3.8-9.8 ppm/K, glass substrates. Regardless of its CTE, glass was shown to have better reliability than silicon at board level, achieving up to 1500 thermal cycles before the first occurrence of joint failure. The build-up layers act as stress buffers absorbing the shear deformation from the CTE mismatch between package and PCB.

Circumferential polymer collars

The interfacial region between the solder joints and the pads on the package side is critical due to the high interfacial stresses and the presence of brittle intermetallic compounds that form at this junction. The circumferential polymer collar serves to block shear deformation of the solder joint at this interface, shifting the regions of high plastic strain away from the interface. In this manner, the polymer collar acts as a partial underfill and maintains the reworkability of the assembly.

2.5 Summary

The evolution of IC packaging from single-chip to multi-chip packaging with recent advances in 2.5D and 3D interposers, fan-out packages and other innovations are reviewed. Interconnection reliability is identified as a key challenge to enable the trend to fine pitch. Several innovations in interconnections materials, structures and processes are emerging to address fine-pitch interconnection reliability. Critical challenges related to low interconnection strains without underfills, simultaneous TCT and drop-test reliability, package and process design to minimize warpage need to be addressed to extend the reliability of interconnections to finer pitches.

CHAPTER 3

FINITE-ELEMENT MODELING FOR STRAIN-RELIEF MECHANISM WITH POLYMER COLLARS

This chapter reports the results of finite-element (FE) modeling, using ANSYS^{TM} 15.0, to provide a fundamental understanding of strain-relief mechanisms with circumferential polymer collars. Warpage of low- and high-CTE glass packages after SMT assembly was evaluated with and without polymer collars. The fatigue life of SAC105 was finally predicted using strain-based Coffin-Manson and Engelmaier-Wild models. The modeling was performed parametrically, using a 2D plain-strain approximation.

3.1 Geometric Model

To investigate the thermomechanical reliability of glass BGA packages at 18.5 mm × 18.5 mm body size, a 2D half-symmetry model of a 100µm-thick package was created from the center to the edge. Modeling was performed with ANSYS. Symmetry boundary conditions were applied to the left boundary of the model, which represented the center of the package, and the bottom corner was pinned to prevent rigid body motion. To understand the strain relief provided by the circumferential polymer collars, the warpage behavior of the substrate and the fatigue life or number of cycles to failure of the solder interconnections were studied.

A unit section of the FE modeled glass package with laminated dielectric build-up layers (ZEONIF ZS-100 by Zeon Corporation), mounted on PCB with SAC105 BGAs at 400µm pitch and circumferential polymer collars is shown in Fig. 3.1. The collar was modeled with a thickness of 110um, optimized in previous work by GT-PRC to maintain

SMT compatibility and reworkability while providing maximum strain relief [13]. For accuracy of fatigue life predictions, solder balls, collars and copper pads were identified as critical locations, and therefore, the mesh was refined within those components.

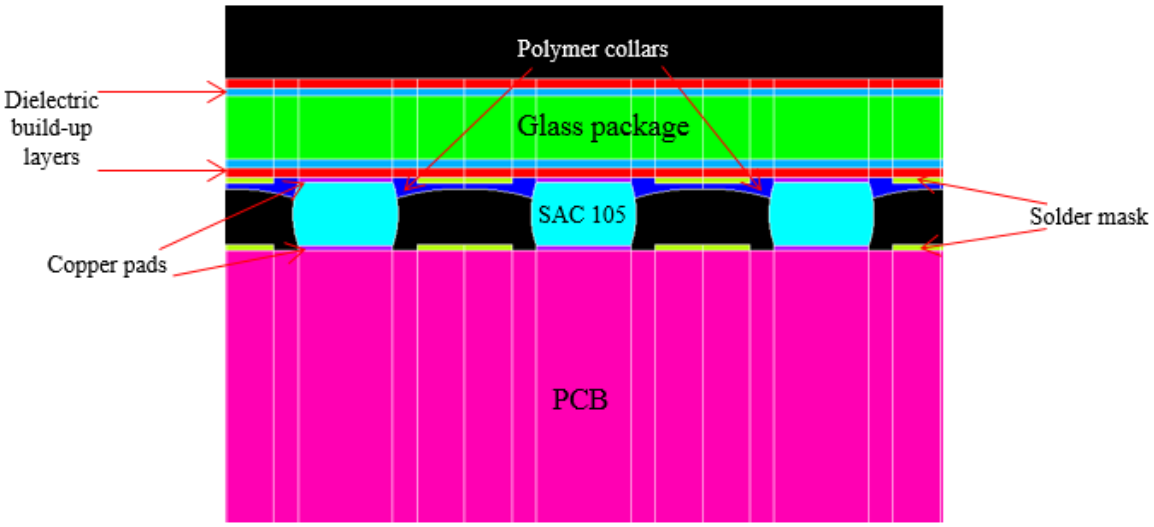

Figure 3.1: Unit section of glass BGA package in 2D half-symmetry FE model.

3.2 Material Models and Stress-Free Temperatures

Fabrication of the glass packages with polymer dielectric build-up layers, BGA balling, polymer collar formation, as well as board-level assembly, occurs over different temperature regimes. During SMT assembly, mechanical coupling between package and board is established when solder solidifies and forms interconnections. Mismatch in CTE between the lower CTE package and the higher CTE organic PCB causes warpage and plastic strains in solder joints upon temperature excursion. These plastic strains accumulate under thermal cyclic loading, leading to crack initiation, crack propagation and fatigue failure. Thus, it is critical to understand the mechanical behavior of the package materials and adequately represent them in the model. All package materials, with the exception of metals, were considered elastic and temperature independent, and were modeled with the

physical properties given in Table 3.1 [13]. Plasticity of copper was represented with a bilinear elastic-plastic law with isotropic kinematic hardening (tangent modulus of 1034 MPa and yield stress of 172.4MPa). The SAC105 solder was considered viscoplastic in the considered temperature range, and modeled with Anand's unified constitutive law, capturing time-independent plasticity and creep of the solder. Anand's model parameters for SAC105 are shown in Table 3.2 [64]. Properties of the collar material from Namics Corporation are not listed here due to proprietary reasons as it is still in development phase.

Table 3.1: Properties of modeled materials [11].

Material	**Modulus (GPa)**	**CTE (ppm/^{o}C)**	**Poisson's Ratio**
Low-CTE glass	77	3.8	0.22
High-CTE glass	74	9.8	0.23
ZEONIF build-up layer (Zeon)	7	21	0.30
Solder mask	13.45	4.5	0.30
Copper	121	17.3	0.30
FR-4 (PCB)	24	17	0.30

Table 3.2: Anand's model parameters for SAC105 solder [64].

Anand's Parameters	Units	Value
A	s^{-1}	5200
Q/R	K	10150
Ξ	-	6.0
M	-	0.18
S	MPa	30
N	-	0.008
h_0	MPa	34000
A	-	1.62
s_0	MPa	23

Materials are assigned stress-free temperatures to mimic the fabrication and assembly processes. Stress-free temperature can be defined as the temperature at which components of an assembly do not exhibit deformations from their pre-assembled shapes [65]. In FEM simulations, it is critical to account for realistic reference conditions for accurate modeling both with and without collars. In typical SMT assemblies, the stress-free temperature is generally assumed to be close to the freezing point of the solder because package-to-board coupling initiates as solder starts solidifying. However, this does not apply in the presence of underfills or adhesives, even partial ones like polymer collars. Underfills and adhesives are typically epoxy-based polymers, characterized by their glass transition temperature (T_g) at which the polymer changes from a hard, glassy state to a soft, compliant, rubbery state. In assemblies with underfills or adhesives, it has been demonstrated that the warpage behavior was dominated by the forces applied by the underfill material [66]. The glass transition temperature of the underfill then provides a better representation of the stress-free temperature, as demonstrated in [67]. Although

polymer collars are only partial underfilling, their case was treated as in assemblies with continuous underfill or adhesive layers. The stress-free temperature was therefore assigned as the T_g of the collar material as a first approximation.

3.3 Thermal Loading Conditions for Thermomechanical Simulations

With the basic understanding of Section 3.2, different stress-free temperatures were set based on the presence or absence of circumferential polymer collars. In assemblies without a polymer collar, the stress-free temperature was assumed to be of 170°C, at which SAC105 is expected to start solidifying. In assemblies with collars, the stress-free temperature was assumed to be of 130°C, near the T_g of the polymer collar material. The modeled assemblies were first subjected to a drop in temperature from 260˚C to 25˚C to simulate the cool-down phase of the SMT reflow process. Five thermal cycles between -40˚C and 125˚C were then applied, following JESD22-A106B thermal shock standards [68]. The ramp-up and ramp-down times were of 1 min each, and the dwell time at each temperature extreme was of 5 min, as shown in Fig. 3.2. From the thermal cyclic loading, the accumulated plastic strain per cycle in solder joints was used to predict their fatigue life and provide design guidelines for reliability.

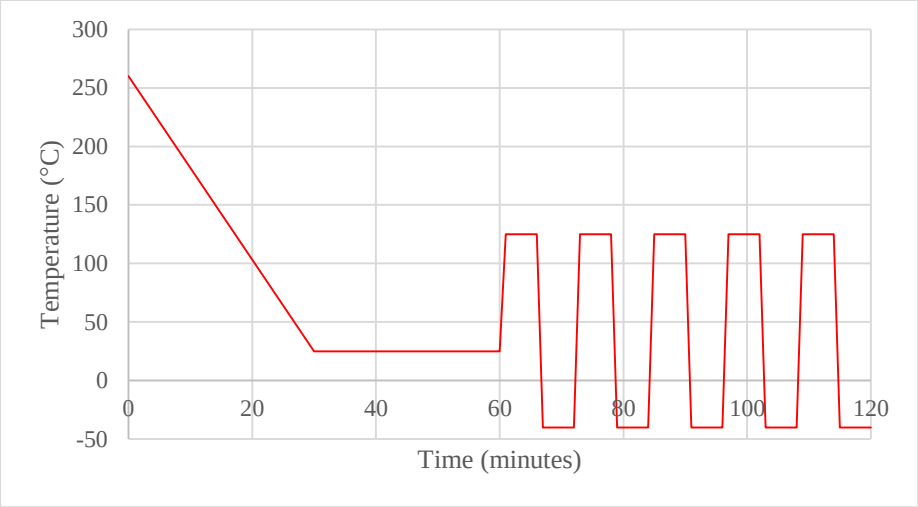

Figure 3.2: Thermal loading applied in modeling of glass BGA package thermomechanical reliability.

3.4 Effect of Polymer Collars on Glass Package Warpage Behavior

The warpage behavior of substrates is conditioned by both their CTE and modulus. To understand the effect of polymer collars on warpage, the warpage response of glass BGA packages to thermal cycling in the conditions of Fig 3.2 was captured, with and without polymer collars. The warpage convention of JEDEC22-B112A standard was used, as illustrated in Fig. 3.3 [69]. All warpage results presented in this section are from the center to the edge of the package.

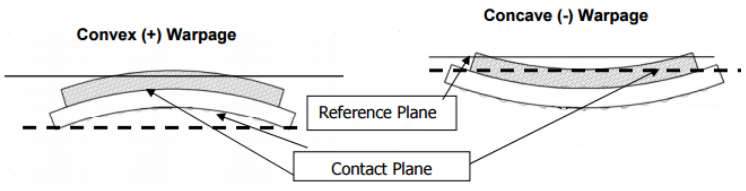

Figure 3.3: JEDEC-defined package warpage convention.

At low temperatures, the organic PCB shrinks more than the glass package, giving the assembly a ‘dome-shaped’ positive or convex warpage. At higher temperatures, the PCB expands and acquires a ‘bowl-shaped’ negative or concave warpage. The warpage

response for a high-CTE glass package on board is shown at the temperature extremes of -40°C and 260°C in Fig. 3.4.

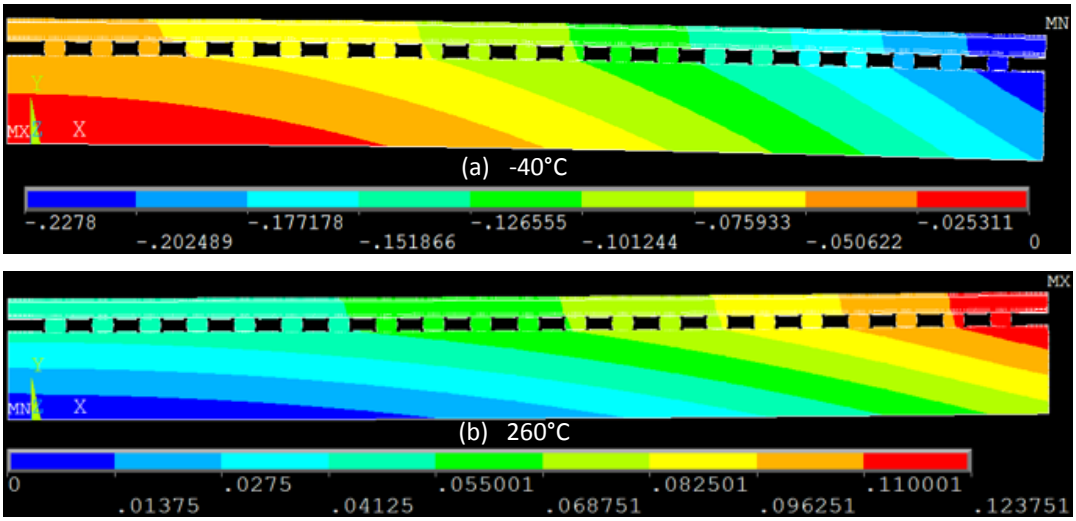

Figure 3.4: (a) Convex warpage at -40°C, (b) concave warpage at 260°C.

Results of net warpage as a function of temperature are plotted in Fig. 3.5 for low- and high-CTE packages, with and without polymer collars. From the plot, it can be inferred that higher net warpage is, as expected, obtained for low-CTE glass substrates due to highest CTE mismatch with the organic board. Regardless of the glass CTE, the warpage curve shifts down in presence of polymer collars, indicating lower net warpage.

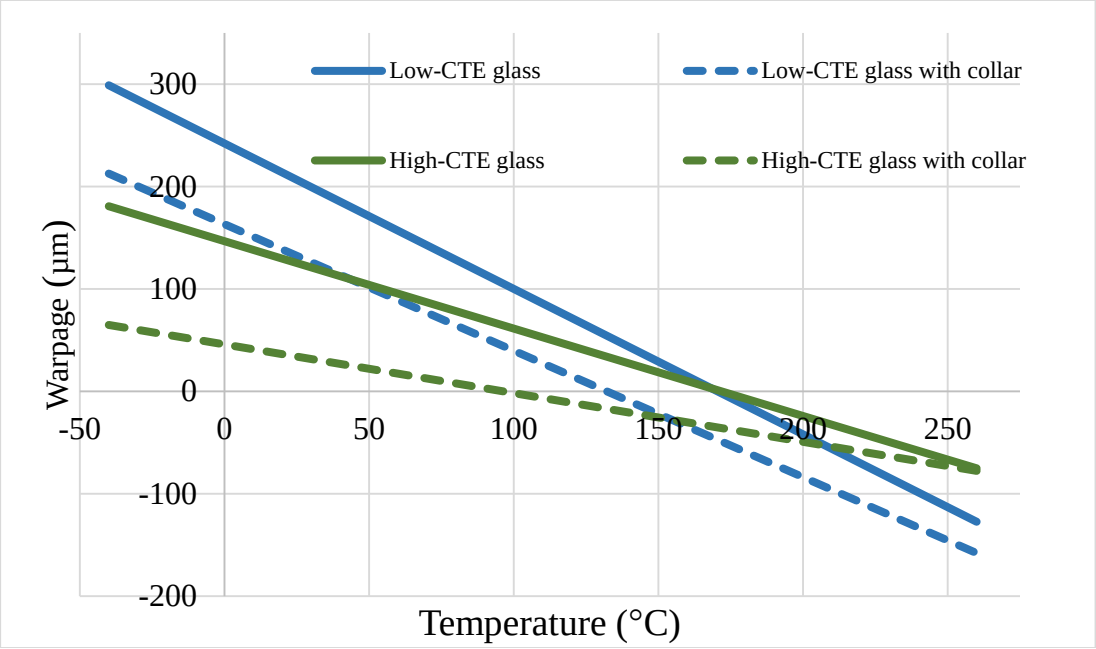

Figure 3.5: Warpage behavior for low- and high-CTE BGA packages with and without circumferential collars.

The slope of each of these curves corresponds to the amount of CTE mismatch between package and board. The model predicts that polymer collars marginally increase the overall CTE of the substrate. In the case of low-CTE glass, the warpage trends with and without collars run almost parallel to each other with slopes -1.42, and -1.23 respectively. On the other hand, the effect of the collars on high-CTE glass substrates was much more prominent because the CTE of the substrate was closer to that of the board. The slopes with and without collars on high-CTE glass substrates were -0.85 and -0.47 respectively. The warpage range over the thermal cycling temperatures should correspond to the amount of plastic strain accumulated per cycle, and thus the fatigue life, which is explored in the next section.

3.5 Effect of Polymer Collars on the Fatigue Life of Solders

Although evidence of the effectiveness of polymer collars in improving thermomechanical reliability of solder-based interconnections has been provided at wafer-level, for example with the Spheron^{TM} technology introduced in Chapter 1, the fundamental strain-relief mechanisms are not explained in literature. This section focuses on addressing this gap through fatigue modeling.

Fatigue models can be divided into five major categories based on damage metrics . These damage metrics include: i) stress-based, ii) plastic strain-based, iii) creep strain-based, iv) energy-based, and v) damage accumulation-based [70]. Fatigue from CTE mismatch in solders is generally related to accumulated plastic strain from models. Coffin-Manson, Solomon, Engelmaier and Miner models have proposed the prediction of solder fatigue life using the plastic strain range in one thermal loading cycle as damage metrics.

The equivalent plastic strain range in the outermost solder joint of the modeled low- and high-CTE glass BGA packages was consequently extracted after thermal cycling. Two primary trends are observed depending on the presence of polymer collars, as shown in Fig. 3.6, which shows the total accumulated plastic strain in the outermost solder joint in (a) the without collar case and (b) the with collar case. In the absence of collars, the maximum nodal plastic strains are located in the top region of the solder ball. In the absence of any strain-relief, this top region presents ideal sites for crack initiation and propagation as highlighted in Fig 3.6 (a). In the presence of collars, high strain concentrations are observed in three different sites. First, near the top of the BGA towards the center of the package (highest strains); second, near the inside corner where the collar ends; and third, near the bottom of the BGA, away from the package center, as shown in Fig 3.6 (b).

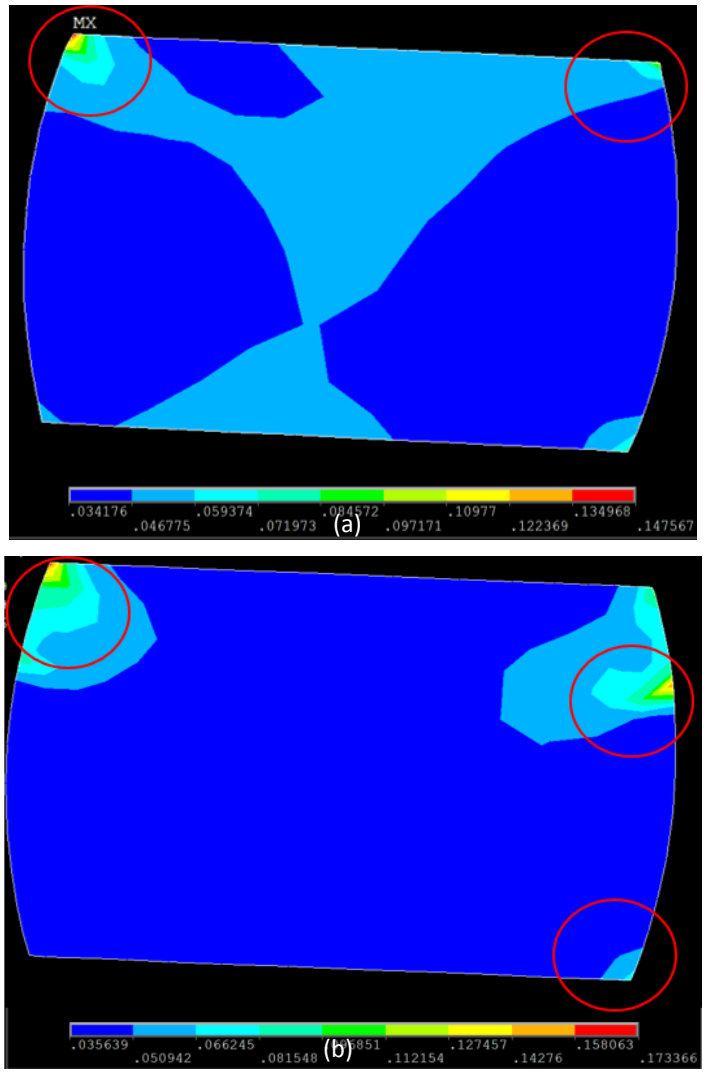

Figure 3.6: (a) Plastic strain distribution in the outermost solder joint (a) without collars and (b) with collars. Show package side and board side on the figure. Thicker red circles.

Near the top interfacial region, the circumferential collars encompass regions of high stress concentration and redistribute the shear strains, preventing cracks from initiating and propagating in the first location. Under any cyclic loading, it has been well established that cracks only initiate at points of acute angles near the interfacial region between pad and solder [71, 72]. The circumferential collars make an obtuse angle with the free surface edge of the solder joint, preventing crack initiation at the second location of high strain concentration in absence of any significant solder voiding. Failures are

therefore expected to occur in the third location of high strain concentration, on the PCB side. Moving to the next solder joint towards the center of the package, less damage was accumulated, as shown in Fig. 3.7, signifying failures expected in the corner interconnections, with and without collars. These predictions are well aligned with the experimental results presented in Chapter 5.

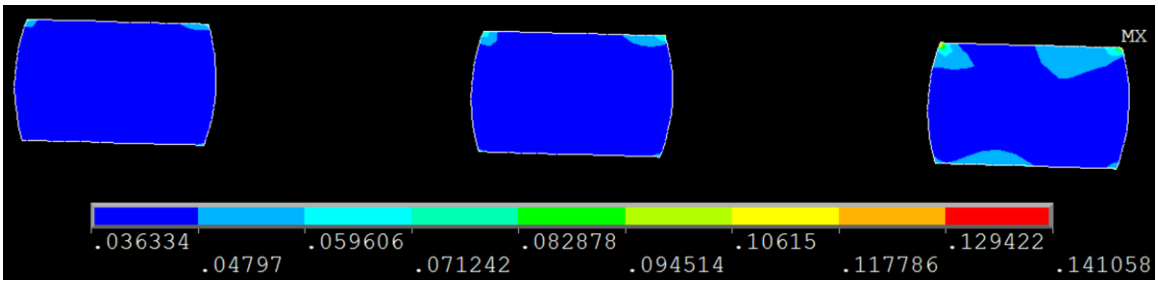

Figure 3.7: Decreasing plastic strain in solder joints moving towards the package center.

With the above understanding, the plastic strain range was extracted from the top-left corner of the outermost solder joint towards the package center in the absence of polymer collars. With polymer collars, the plastic strain range was extracted from the bottom-right region, away from the package center.

The fatigue life of the solder joints was first estimated using the popular Coffin-Manson equation [73] which is an empirical fit to determine low-cycle fatigue life below 10,000 thermal cycles:

$$N_f = \left(\frac{2*\theta}{(\Delta\gamma_p)}\right)^{1/a} \qquad \text{(Eq. 3.1)}$$

where N_f is the number of cycles to failure, 'a' is the fatigue strength exponent assumed to be 0.5413, θ is the fatigue ductility coefficient assumed to be 0.2516 [74], and $\Delta\gamma_p$ is the plastic strain range, which was obtained using the NL,EPEQ command over the fifth thermal cycle. Table 3.3 shows the extracted plastic strain range values for all considered package variations. The number of cycles to failure is plotted in Fig. 3.8.

Table 3.3: Plastic strain range values with and without collars.

Package Material	Plastic Strain Range (no collar)	Plastic Strain Range (with collar)
Low-CTE Glass	1.312×10^{-2}	1.090×10^{-2}
High-CTE Glass	0.680×10^{-2}	0.535×10^{-2}

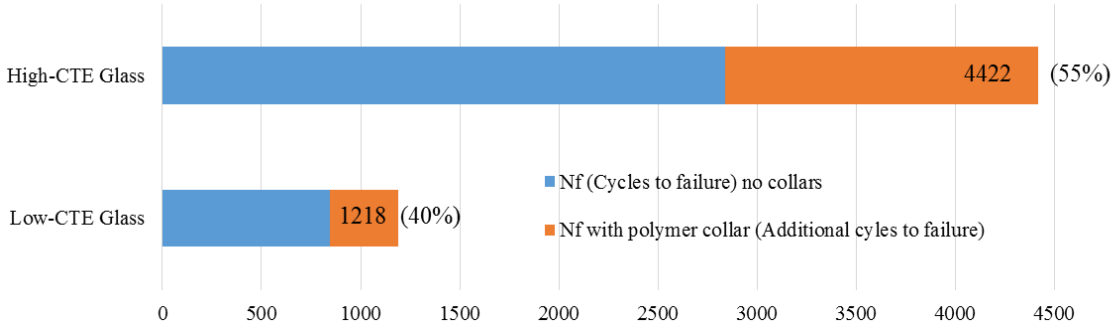

Figure 3.8: Fatigue life predictions using Coffin-Manson model

The Engelmaier fatigue model improves on the Coffin-Mason and Solomon's models by including cyclic frequency effects and temperature effects. The Engelmaier-Wild model (Eq. 3.2 and 3.3) can be used to determine the number of cycles to failure [75, 76]:

$$N_f = 0.5 \times \left(\frac{2\Delta\varepsilon_f}{\Delta\varepsilon_p}\right)^{1/c} \quad \text{(Eq. 3.2)}$$

$$\frac{1}{c} = c_0 + c_1 T_{SJ} + c_2 * \ln\left(1 + \frac{t_0}{t_d}\right) \quad \text{(Eq. 3.3)}$$

where $\Delta\varepsilon_f$ is the fatigue ductility coefficient, $\Delta\varepsilon_p$ is the strain range amplitude, c is the fatigue strength exponent, c_0, c_1, c_2, t_0 are solder-specific constants with experimentally determined values in Table 3.4, T_{SJ} is the mean cyclic thermal solder-joint temperature (42.5°C), and t_d is the half-cycle dwell time in minutes (15 min). Literature reported material cons

Table 3.4: Material constants for SAC105 [16].

Solder	ε_f	c_0	c_1	c_2	t_0
SAC105	0.225	.480	9.3e-4	-1.92e-2	500

From the above equations, a fatigue strength exponent, *c*, of 0.4516 is obtained, yielding the fatigue life predictions, plotted in Fig. 3.9.

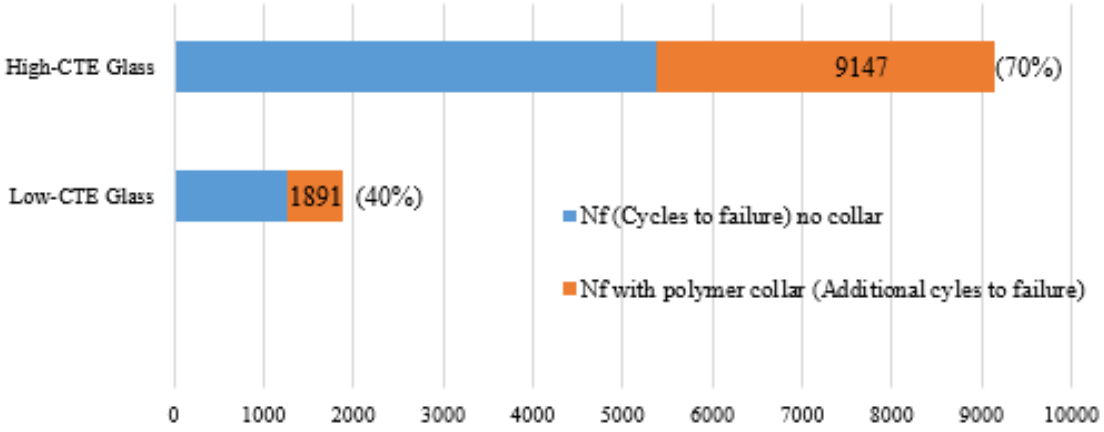

Figure 3.9: Fatigue life predictions using Engelmaier-Wild model.

Based on the fatigue life predictions with both Coffin-Manson and Engelmaier-Wild models, all package configurations would survive over a 1000 cycles, satisfying JEDEC reliability standards. The fatigue life was predicted to be better with high-CTE glass substrates, as expected, due to the lower CTE mismatch with the board. Polymer collars were also predicted to improve fatigue life by 40-55% or 40-70%, based on predictions with the Coffin-Manson or the Engelmaier-Wild model, respectively. This fatigue life improvement is due to strain redistribution and reduction in CTE mismatch. Model-to-experiment correlation is presented and further discussed in Chapter 5.

CHAPTER 4

TEST VEHICLES DESIGN, FABRICATION AND ASSEMBLY

Design rules for the three daisy-chain test vehicles used in this study of board-level reliability are detailed in this chapter. The research goals associated with each test vehicle are then summarized. Fabrication and assembly processes are finally presented with a detailed analysis of BGA balling and assembly yields, explained by consideration of substrate warpage.

4.1 Test Vehicle 1 (TV1) – Strain relief with polymer collars

This test vehicle was designed to evaluate drop and thermomechanical reliability of low- and high-CTE 100µm-thick glass BGA packages, 18.5mm x 18.5mm in body size. This test vehicle also aims at investigating the effect of circumferential polymer collars on the drop and fatigue performances of solders. A schematic cross-section of the glass BGA package is shown in Fig 4.1, with a single metallization on either side of the glass core for ease of processability and improved fabrication yield.

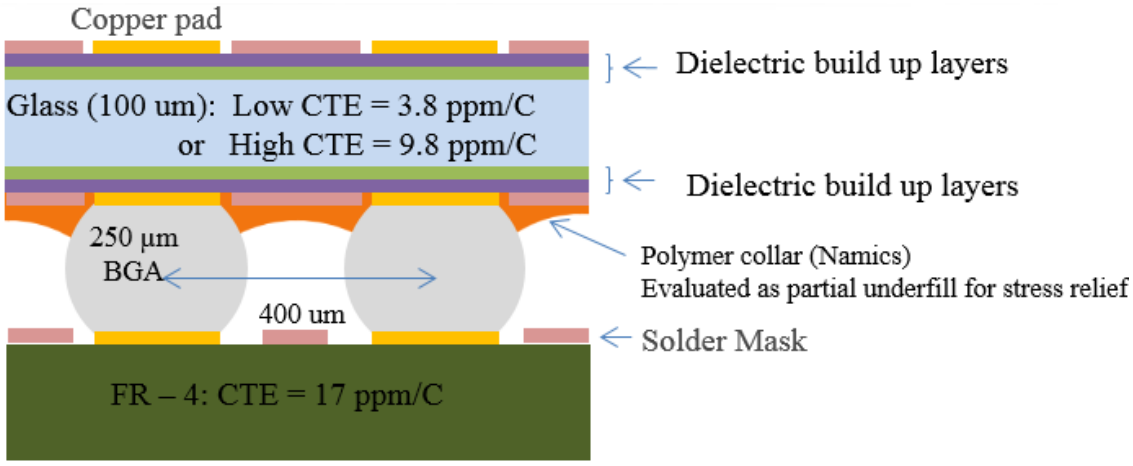

Figure 4.1: Glass BGA package stack-up of TV1.

4.1.1 Design and Fabrication of Glass BGA Substrates

Glass packages were designed with a body size of 18.5mm x 18.5mm to accommodate a 45 x 45 area array of daisy-chained BGA interconnections at 400µm pitch, as shown in Fig. 4.2. The diameter of the solder balls was chosen as 250µm, consistent with current industry standards for board-level interconnections at this pitch. The substrate metallization subsequently consisted of patterned dogbone daisy-chain structures with a pad diameter of 225µm. A solder mask defined (SMD) passivation was finally designed with openings of 180µm. The design was kept symmetrical with respect to the glass core to balance warpage. This glass package coupon design was then panelized to fit in a 150mm x 150mm substrate.

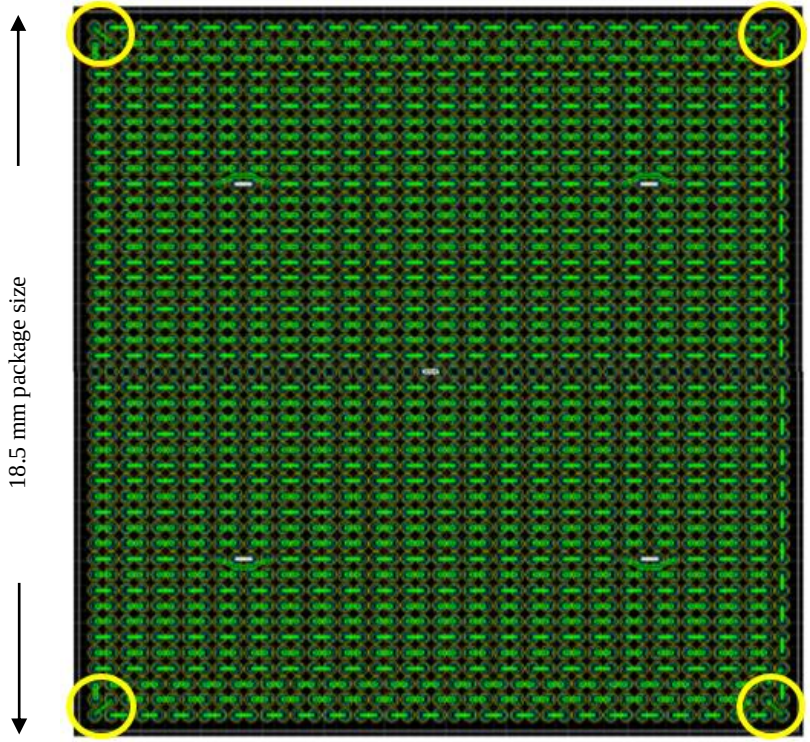

Figure 4.2: Glass BGA package design for board-level reliability evaluation.

The designed glass substrates were fabricated independently of this research [13], but process flow and stack-up material specifications are summarized in Fig. 4.3 and Table

4.1 for reference. Process-of-record fabrication processes were applied with standard semi-additive processes [13]. The glass packages were fabricated on 150mm x 150mm low- and high-CTE glass substrates that are 100µm thick provided by Asahi glass. Dielectric build-up layers were then formed on either side of the glass substrates by double-sided lamination of two layers of Zeon ZIF ZS-100 with a nominal thickness of 22.5µm. The surface of ZIF is suitable for electroless plating of copper seed layer, which allowed the use of semi-additive process (SAP). SAP utilizes electrolytic plating of lithographically defined patterns on the copper seed layer to pattern the daisy-chain structures with a copper thickness of 10-12µm. An additional layer of ZS-100 was used as passivation layer with openings to the SMD pads formed by laser drilling. Standard ENEPIG surface finish was finally applied on the copper pads by Atotech GmbH with industry-controlled plating processes. The metalized glass panels were then sent to Nanium for attachment of 250µm SAC105 solder BGAs by ball drop, followed by singulation by mechanical blade dicing.

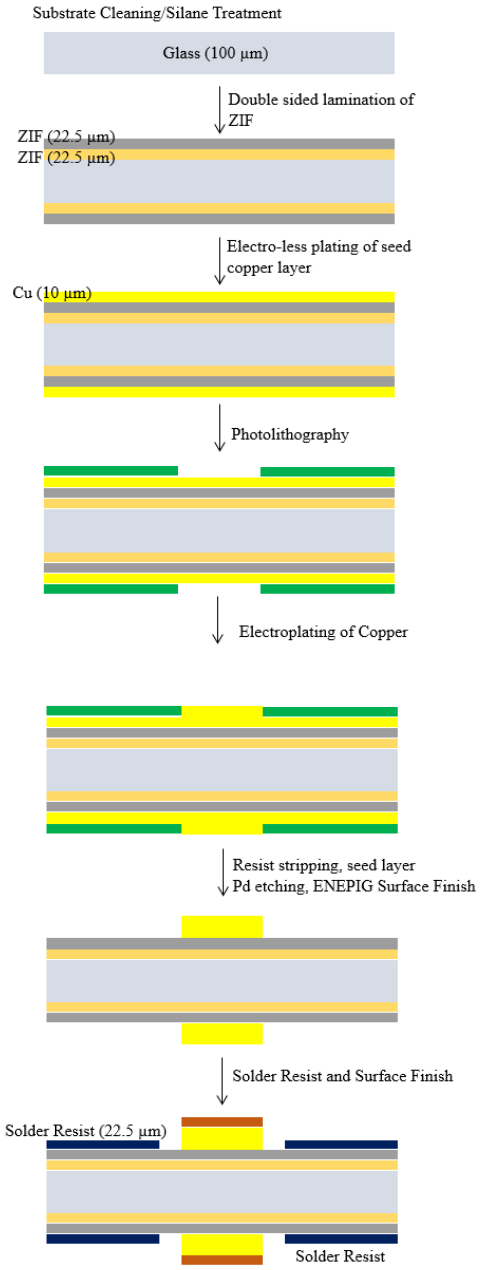

Figure 4.3: Glass BGA package TV1 fabrication process flow

Table 4.1: TV1 glass substrate stack-up.

Parameter	Material Description
Substrate Core	Low- & high-CTE glass (Asahi EN-A1 & CF-XX)
Core Thickness	100µm
Build-up Layers	ZIF 22.5µm ZIF 22.5µm (Zeon)
Solder Resist	ZIF 22.5µm – SMD
Metal Layers	BGA daisy chain pattern with 25% Cu coverage
Cu Surface	Bondfilm – 10µm Cu thickness
Surface Finish	ENEPIG (Atotech Germany)
BGA Balling and Dicing	250µm SAC105 BGA (Nanium)

4.1.2 PCB Design for Thermal Cycling and Drop Test

The BGA area array on the glass substrates consists of 2025 solder balls, divided in a network of 52 daisy chains. A single-layer PCB board was designed for thermal cycling test, with matching daisy-chain structures including 4 corner circuits comprising 6 BGAs each, and 48 inner chains, as indicated by the circles in Fig. 4.4. The copper pads are non-solder mask defined (NSMD) with a diameter of 225µm and passivation openings of 340µm

Fabrication of the designed drop and thermal cycling test boards was outsourced. Electroless nickel, electroless palladium, immersion gold (ENEPIG) surface finish was applied on the copper pads in both cases.

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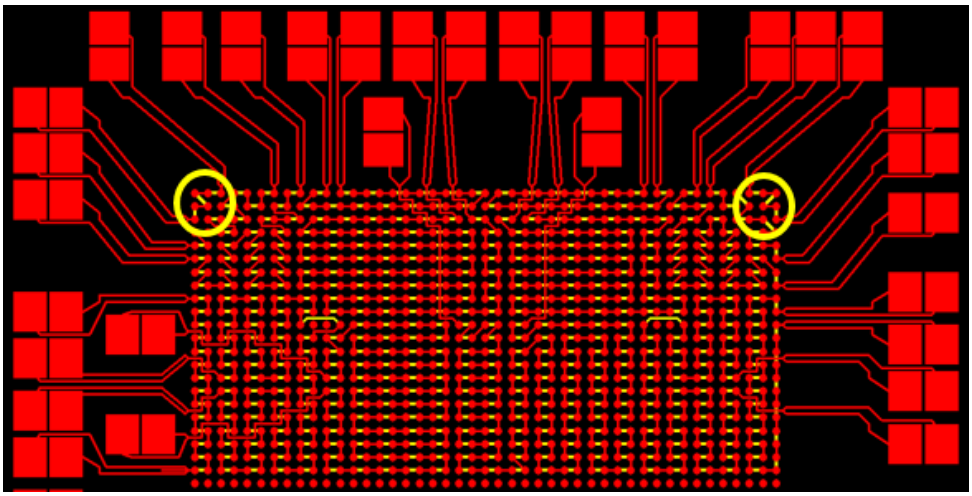


Figure 4.4: PCB board design with 4-point probing pads

Test boards used in drop test of microelectronics package must be designed in accordance with JEDEC JESD22-B111 standards [17]. However, these recommendations only consider package sizes up to 15mm in length or width, smaller than the body size considered in this study. A drop test board accommodating larger package sizes was designed by Qualcomm as an extension of JEDEC requirements. Symmetric about the center, the board enables testing of four BGA package assemblies in the configuration of Fig. 4.5.

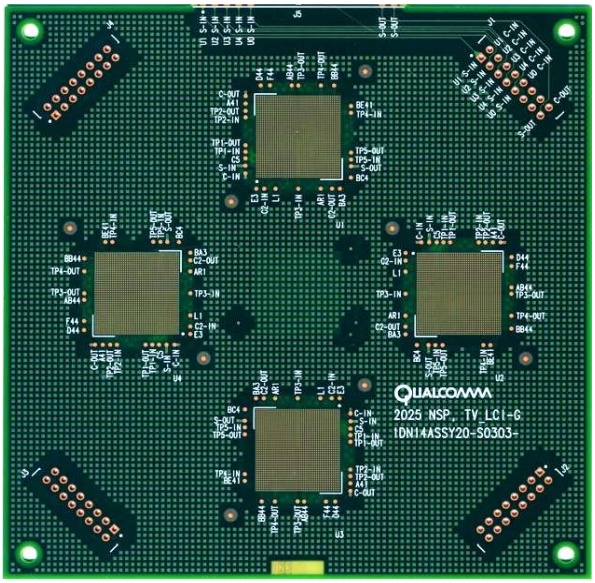


Figure 4.5: Board design for drop testing of 18.5mm x 18.5mm glass packages.

The daisy chain layout consisted of 2 daisy chains for each package: 1 corner daisy chain stitching 6 power I/Os per corner; and 1 inner daisy chain running through all signal I/Os, as indicated in Fig. 4.6 with red and blue lines respectively.

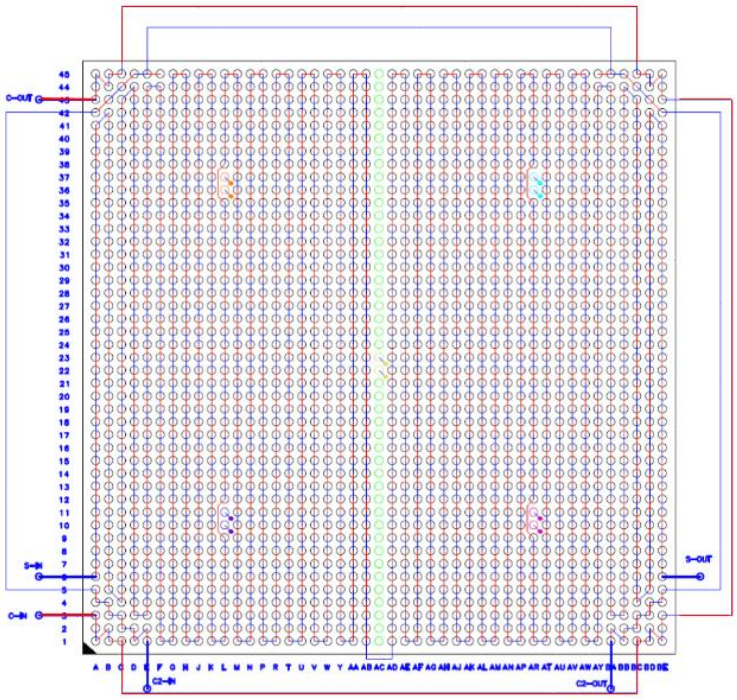


Figure 4.6: Daisy-chain layout for drop test with corner daisy chain in red and inner daisy chain in blue.

4.1.3 Glass package pre-characterization

The glass BGA packages were selected for reliability testing based on fabrication and balling yields of the substrates. After singulation, optical microscopy, X-ray and confocal surface acoustic microscopy (C-SAM) imaging were used to inspect for any fabrication-related process defects such as blistering and delamination of the dielectric build-up layers; and BGA balling defects such as missing balls, improper wetting, and non-uniform bump height. These characterization methods were systematically applied to identify known-good glass substrates for reliability evaluation. The C-SAM analysis of a

low-CTE sample shown in Fig 4.7 indicates the absence of glass-based defects in the form of chipping or cracking. Prior to SMT assembly, the edges of all known-good glass packages were coated with a filler-free polymer (provided by Namics Inc.) for edge protection.

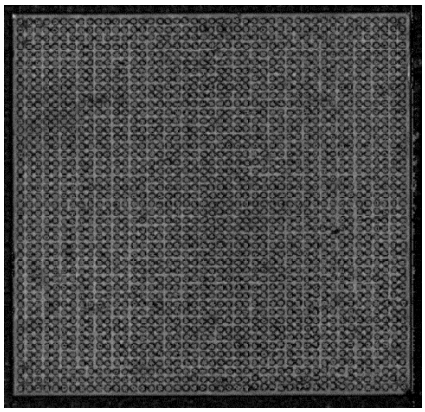


Figure 4.7: C-SAM image of a low-CTE glass package with suitable structural integrity.

4.1.4 Polymer Collar Formation

Formation of circumferential polymer collars around the solder BGAs by spin-coating of advanced filler-free epoxy-based materials from Namics Corporation has been optimized and demonstrated in [13]. The coating profile was optimized for uniformity and desired polymer height. The final height of the coated material is conversely proportional to the spin-coating speed, therefore enabling a fine control of the collar thickness. An ideal thickness of 110μm was recommended based on considerations of strain relief and reworkability [13]. The spin coating profile was optimized accordingly with a rate of 500 rpm applied for 20s after which the spin rate was increased to 1000 rpm for 30 sec to improve uniformity [13]. Polymer collars were formed on singulated 18.5mm glass packages with this process, as shown in Fig. 4.8. The BGA glass packages were then oven-dried at 70˚C for one hour to allow for evaporation of part of the solvent content.

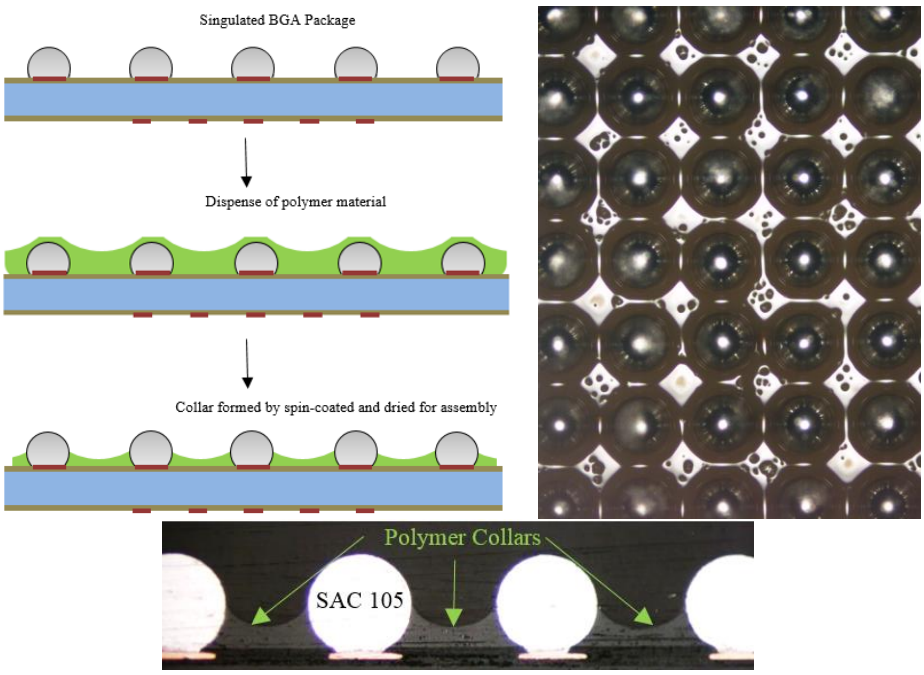


Figure 4.8: Process flow of polymer collars formation (top left) and optical microscope image of spin-coated glass package (top right), cross-section of an 18.4mm interposer with uniform collar formation achieved after spin-coating profile optimization [13].

Polymer residues on the top of the solder balls were wiped clean with acetone to prevent any degradation of assembly yield from contamination.

4.1.5 SMT Assembly Process

The glass packages were then assembled onto dedicated PCBs for thermal cycling and drop test, respectively. The thermal cycling assemblies were built using the Finetech Matrix fineplacer with a placement accuracy of ±3 µm, and a 20mm x 20mm pre-leveled vacuum-locked spring gimbal tool. No-clean tacky flux was applied on the PCB prior to pick-and-place. The reflow conditions were optimized to match the reflow profile of standard SMT processes and minimize BGA voiding. A total of 20 samples were assembled, equally divided between low- and high-CTE glass substrates. Polymer collars were applied on half the packages, as described in Table 4.2.

For drop test, silicon dummy dies, 12mm x 12mm in size, and 100µm in thickness were attached to the top of the glass packages with capillary underfill prior to board assembly to emulate a more realistic warpage behavior. SMT assembly of the drop test samples was carried out by Qualcomm in an industry line. A total of 56 samples, comprising of 40 low-CTE and 16 high-CTE glass packages, with and without polymer collars, were put in test. All sample configurations assembled are detailed in Table 4.2. Out of the 56 samples assembled, a total of 47 samples yielded fully, giving an overall yield of ~84%.

Table 4.2: SMT assembly yield for sample configurations in TCT and drop test

Sample Type	Low-CTE Glass		High-CTE Glass	
	No collar	Collar	No Collar	Collar
TCT	5/5	5/5	5/5	5/5
Drop Test	14/20	17/20	16/16	-
Assembly yield	76%	88%	100.00%	100.00%

X-ray characterization on non-yielded samples showed no major assembly-related defects. All joints were well formed, with no non-wet or unformed solders and no head-on-pillow defects as can be seen in Fig. 4.9. The yield loss is presumably due to fabrication process defects, such as discontinuities in the routing layers.

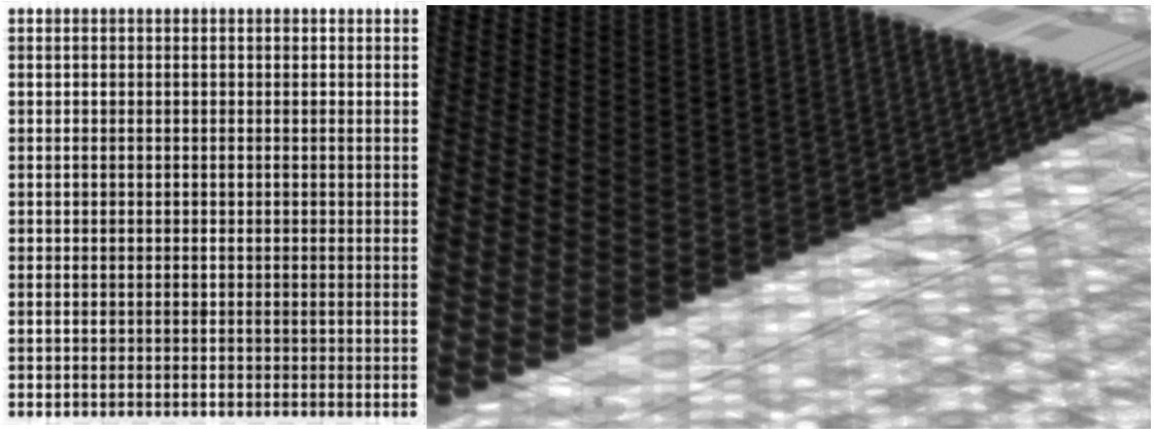


Figure 4.9: X-ray characterization of non-yielded drop-test sample.

4.2 Test Vehicle 2 (TV2) - TCT Evaluation of Mn-Doped Solder SACM™

This test vehicle was dedicated to the evaluation of the thermomechanical performance of Mn-doped SAC solder. It was designed to emulate a single-chip microprocessor package for smart mobile applications. A comprehensive study of the fatigue life of BGA interconnections in such realistic test vehicle was carried out with the following considerations: 1) low- and high-CTE multilayered glass substrates, at a body size of 18.5mm; 2) variations in solder material composition, including Mn-doped SACM™ as well as SAC105 and SAC305 for reference; and 3) variations in die thickness to alter warpage. Polymer collars were concurrently applied to assess the limitations of standard BGA technology with today's most advanced materials and strain-relief mechanisms.

4.2.1 Design of Daisy-Chain Test Die

The test die was designed at a standard size of 10mm x 10mm for high-end Application Processors (AP), with 1856 signal I/Os at 40/80 µm pitch in 4 peripheral staggered rows and 3592 power I/Os at 150 µm pitch in a central area array, for a total of

5448 I/Os, as illustrated in Fig. 4.10. These test dies with daisy-chain structures were fabricated on 300 mm wafers by Advanced Semiconductor Engineering Inc. (ASE), and bumped with industry-standard copper pillar interconnections. The copper pillars, 28µm in diameter, are composed of a 17µm copper height, a 3µm Ni barrier layer, and a 17µm SnAg solder cap.

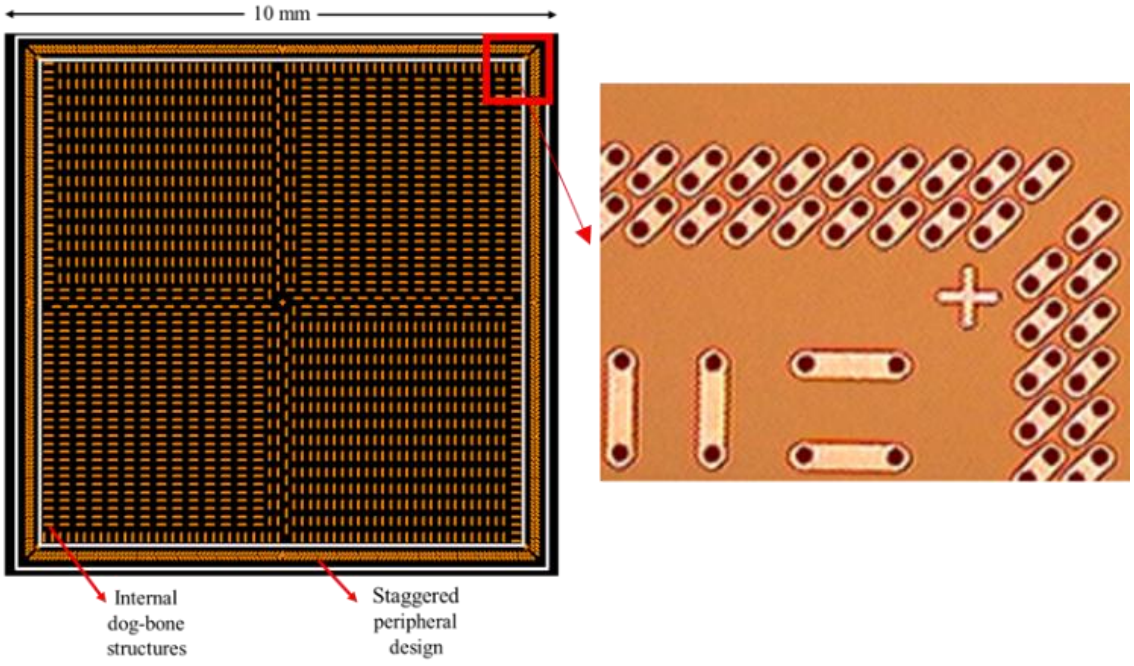


Figure 4.10: Daisy-chain test die fabricated by ASE (left) and magnified view of the die corner (right) (Images courtesy of ASE).

4.2.2 Four Metal Layer Glass Package Design

A four metal layer substrate was designed towards the evaluation of system-level reliability of glass packages. The design of the top layer accommodates the die footprint with testable daisy chains including all 5448 chip I/O interconnections. The BGA design was kept same as in TV1 with a 45 x 45 area array of daisy-chained interconnections, apart from the

diameter of the copper pads and SMD solder-mask openings, changed to 260µm and 220µm, respectively. The layout of both top- and bottom-most layers is shown in Fig. 4.11.

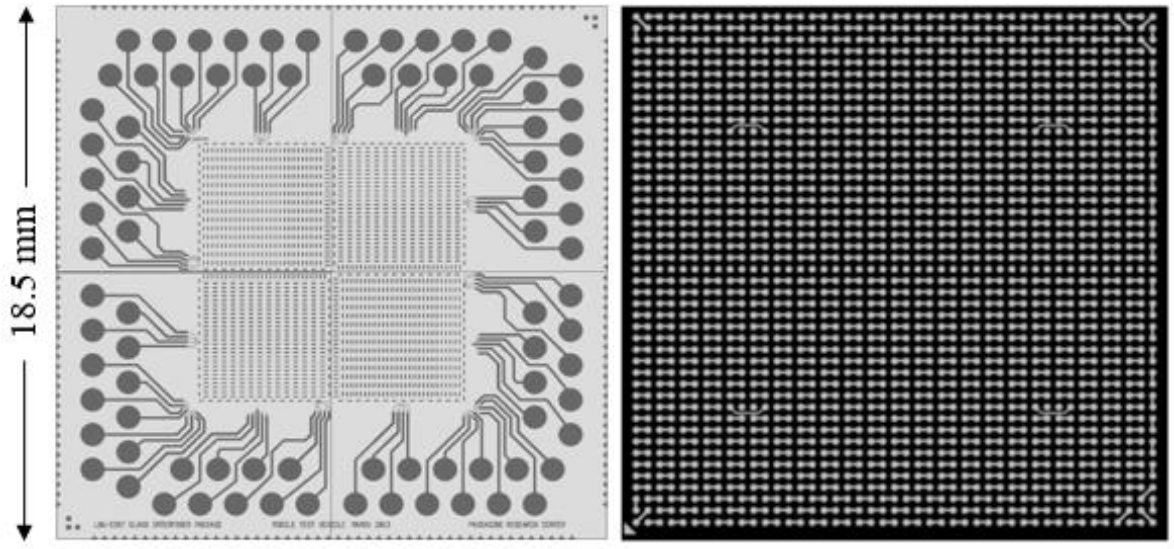


Figure 4.11: Glass substrate test vehicle design with (left) die side, and (right) BGA side

The chip- and board-level daisy chains are not connected in the absence of through-package-vias (TPVs) and can be tested independently. Additional metal layers consisting of a dummy mesh pattern with 80% copper coverage were implemented for a more accurate warpage representation. This test vehicle, therefore, enables concurrent reliability evaluation of chip- and board-level interconnections, in realistic conditions. A schematic cross-section of the four metal layer stack-up and design rules is shown in Fig. 4.12.

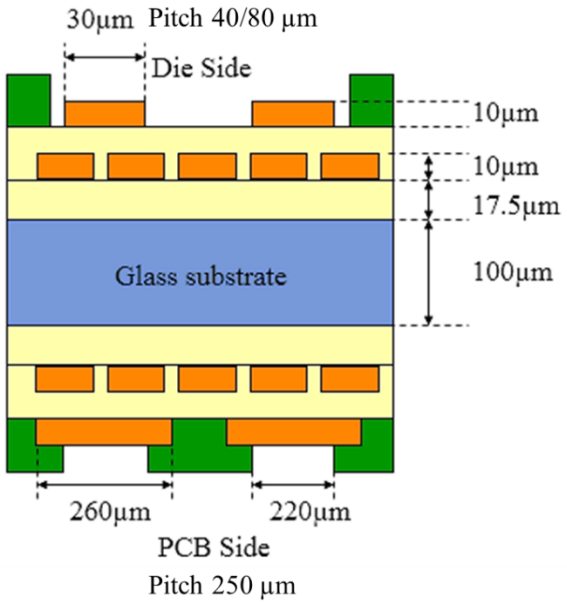


Figure 4.12: TV2 glass package stack-up and design rules.

Low- and high-CTE glass substrates, 6 inch x 6 inch in size, and 100µm in thickness, were fabricated using established fabrication processes, independently of this research. Dielectric layers of ZEONIF™ ZS-100 (ZIF), 17.5µm in thickness, were first laminated onto the glass substrates, then cured in a furnace at 180°C. To create four metal layers, two SAP steps were performed. The first SAP step was responsible for patterning of the inner metal mesh layers with a copper thickness of 10-12µm. ZS-100 was used again as the dielectric layer between first and second metallization. The second SAP step completed the patterning of the chip and BGA interconnects of Fig. 4.12. An additional layer of ZS-100 was applied as passivation to define landing and probing pads. The passivation layer used is a dry-film based material provided by Hitachi Chemical, which can be processed at a low temperature of 180°C. Novel electroless palladium autocatalytic gold (EPAG) surface finish was finally plated on the exposed pads by Atotech GmbH with a production-controlled process. This surface finish metallurgy was selected for its applicability to fine-pitch traces, with 7µm gaps between traces in the current design.

Standard Ni-based finishes such as ENEPIG are not scalable to sub-20µm trace gaps, and therefore not applicable. A cross-sectional expanded view of the four-metal layer fabricated substrates is shown in Fig. 4.13, while Table 4.3 provides a summary of the test vehicle design rules, materials and stack-up.

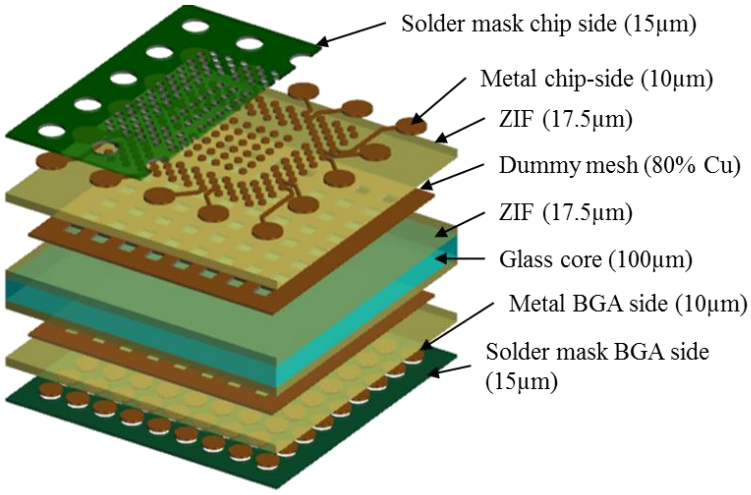


Figure 4.13: Expanded view of 18.5mm x18.5mm 4-metal layer glass substrates.

Table 4.3: Fabrication parameters and materials description for fabrication of 4-metal layer glass BGA packages.

Parameters	**Description**
Substrate core	Low- & high-CTE glass (AGC EN-A1 & CF-XX)
Build-up layers	ZIF 17.5µm/ZIF 17.5µm
Solder mask	15µm dry-film – SMD (Hitachi)
Metal layers	4ML with 80% Cu coverage on inner metal mesh (BGA dogbone pattern)
Surface finish	EPAG (Atotech GmBH Germany)
BGA	250µm @ 400µm pitch (paste printed)
Solder	SACm^{TM}, SAC305, SAC105 (Indium)
Die thickness (TCB)	100µm, 200µm
Underfill (FLI)	50µm

The same PCB board as introduced in section 4.1.2 for thermal cycling test was used again in this study.

4.2.3 Chip-level assembly

To fully understand the effect of warpage on board-level assembly yield and reliability, variations in die thickness were introduced. Test dies, 100µm and 200µm in thickness, were assembled on glass substrates with a dip-flux die-to-panel thermocompression bonding process, using a Finetech FINEPLACER Matrix semi-automatic flip-chip bonder with a placement accuracy of ±3µm. Bonding was achieved with a constant stage temperature of 100°C, a tool head peak temperature of 360°C on the die side at a heating rate of 6K/s, and an applied pressure of 0.9MPa throughout the process. A fully populated 6 inch x 6 inch glass substrate is pictured in Fig. 4.14 to illustrate this process. The assemblies were then underfilled the 8410-219 capillary underfill provided by Namics Corporation by manual dispensing using a single dot pattern, followed by curing at 165°C for one hour. Chip-level assembly was completed on two low-CTE and half of a high-CTE glass panel, for a total of 90 parts, with excellent yield.

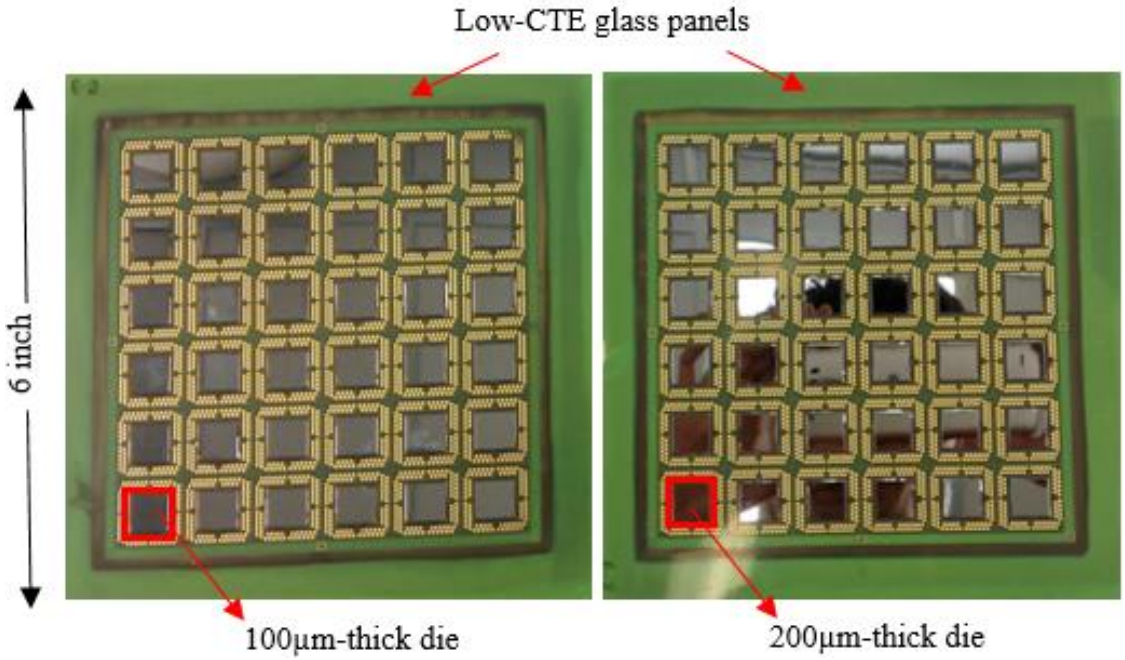


Figure 4.14: Chip-level assembly on low-CTE glass substrates by thermocompression bonding at panel level.

4.2.4 BGA Balling Process Development and Optimization

For evaluation of the new Mn-doped SACm™ solder, only available in paste form, and its comparison to the performance of SAC305 and SAC105 alloys, a BGA balling process by solder paste printing was first developed and optimized. Paste printing is seldom applied at such fine SMT pitch of 400µm, considered too challenging in achieving adequate paste release rates, good solder volume uniformity and high balling yields. Stencil design, paste printing procedure, optimization of the reflow profile as well as systematic characterization of the balling yield were carried out to establish a baseline process that could be trusted for this reliability study.

4.2.4.1 Stencil design

BGA balling was performed with a Ni electroformed (Ni-E) stencil with a proprietary nano-coat™ from MET Technology Inc. The stencil design (Fig. 4.15) was

completed in accordance with IPC-7525A standard [77]. For BGA, the equations (4.1) and (4.2) for the aspect and area ratio, respectively, are defined based on the aperture and thickness of the stencil:

$$Aspect\ Ratio = \frac{Width\ of\ Aperature}{Thickness\ of\ Stencil} \tag{4.1}$$

$$Area\ Ratio\ (for\ BGA) = \frac{Diameter\ (Circular\ Aperature)}{4 * Stencil\ Thickness} \tag{4.2}$$

For a Ni-E stencil, the minimum aspect and area ratio requirements are 1.1 and 0.5, respectively. A standard laser cut stencil requires the aspect and area ratio to be greater than 1.5 and 0.66, respectively, and thus would not meet our paste printing specifications for 250µm BGAs at 400µm pitch.

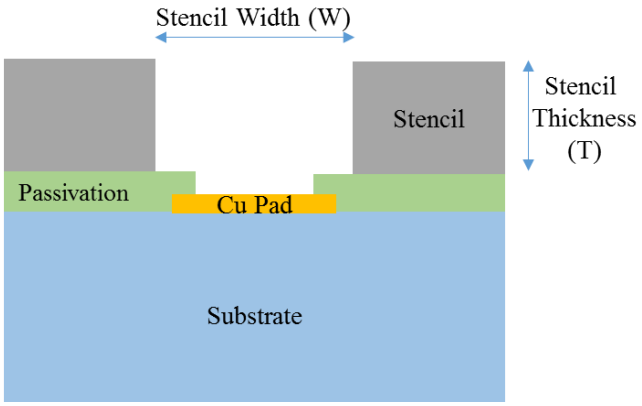


Figure 4.15: Schematic of the stencil for BGA balling by paste printing.

The total volume for one solder ball in a circular aperture opening can be given as:

$$\begin{aligned} Total\ volume = {} & Volume\ occupied\ by\ the\ \ stencil\ aperature \\ & + Volume\ occupied\ in\ passivation\ opening \\ & + Paste\ Shrinkage\ (during\ reflow) \end{aligned} \tag{4.3}$$

Considering the metal loading in the solder pastes of 88.5%, calculations were adjusted with considerations of the solder paste flux shrinkage during reflow. The designed

stencil thickness was of 5 mils (127.4 µm) with apertures of 11.81 mils (300 µm), yielding an aspect ratio of 2.42 and an area ratio of 0.61.

4.2.4.2 Paste printing and reflow

Paste printing was accomplished with a semi-automatic MPM manufactured SPM Screen Printer, and a standard 12-inch metal squeegee after optimizing parameters for the stencil height, the squeegee pressure and the print stroke length. Table 4.4 lists the recommended print parameters by Indium for the printer operation [78]. Optical inspection (Fig. 4.16) confirmed excellent paste transfer efficiency with a uniform deposit and good paste-to-pad alignment, and no observed bridging.

Table 4.4: Suggested parameters for stencil based paste printing (Indium Corporation).

Parameter	**Value**
Print speed	25-100 mm/sec
Squeegee pressure	0.018 – 0.027 kg/mm of blade length
Underside wipe	At least every 5 prints

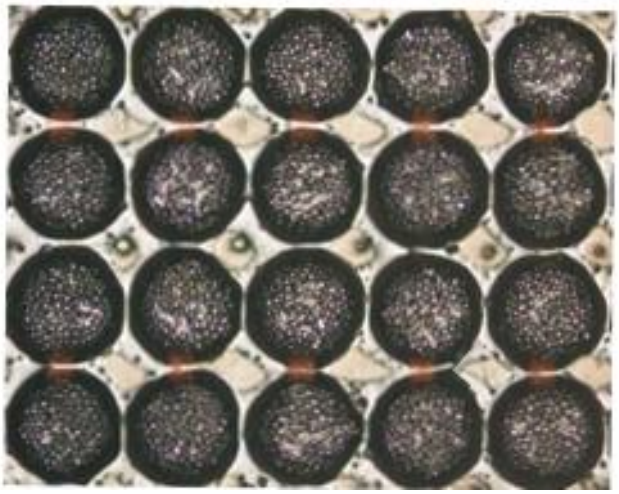


Figure 4.16: Optical inspection of as-printed BGAs with good paste release, uniform deposit, good paste-to-pad alignment and no observed bridging.

4.2.4.3 Reflow optimization

Use of linear ramp rate or ramp-to-spike reflow profiles (Fig. 4.17) is known to reduce reflow-based defects such as solder beading and aggravated hot slump leading to solder bridging [65]. To achieve acceptable wetting and solderability, a peak temperature 15 to 30°C higher than the solder melting point and a time of 45–60 sec above the liquidus temperature are considered ideal. A five-zone Electrovert Omniflow reflow oven was programmed to meet the aforementioned conditions recommended by Indium, as confirmed by wireless thermocouple measurements.

The reflow conditions were optimized to minimize solder voiding using Cu-clad FR-4 boards, patterned with solder mask passivation to match the glass test vehicle BGA design. The temperature profile and conveyor speed were varied, and the formed solder balls were subsequently observed by X-ray microscopy. Results from this evaluation are reported in Table 4.5. A gradual reduction in the occurrence and size of voids can be observed from Board 1 through 4.

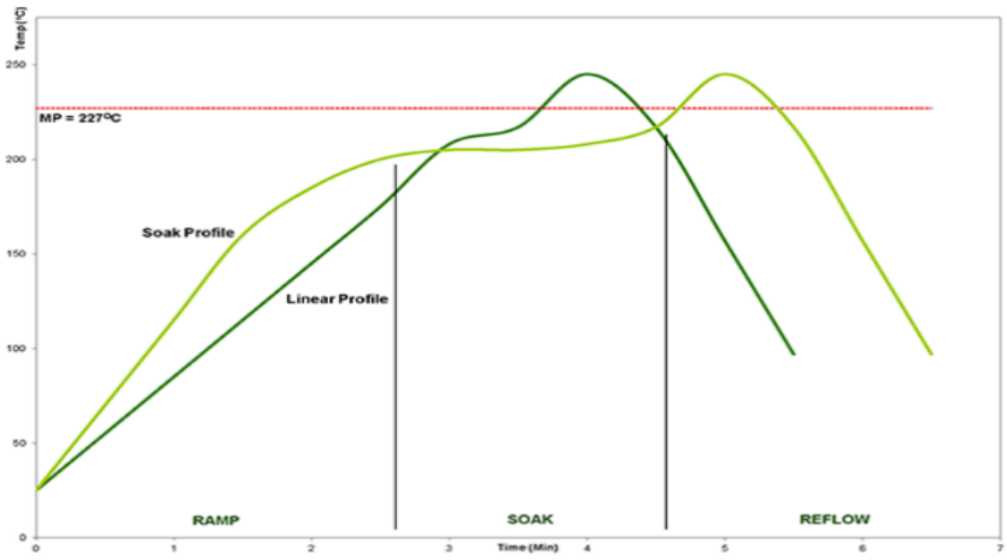
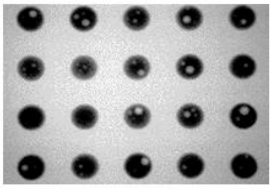
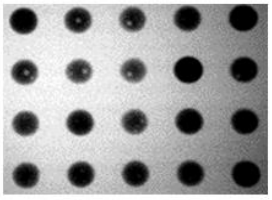
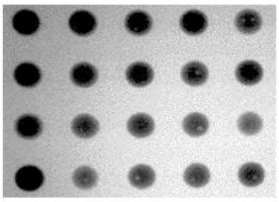
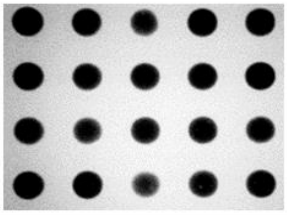


Figure 4.17: Recommended reflow profile for SAC305 solder paste [65].

Table 4.5 Reflow optimization for minimization of solder voiding:

Board #	Reflow (°C) Zone 1 to 5	Speed (inch/ min)	Voiding inspection (X-ray image)
1	85→150 →190→ 250→275	10	
2	85→140 →195→ 230→260	12	
3	85→140 →195→ 220→250	14	
4	85→140 →195→ 220→250	12	

BGA balling was performed on individual test glass coupons with optimized reflow conditions. These coupons were again imaged by X-ray microscopy to inspect for solder voiding, beading or bridging, with no observable defects as indicated in Fig. 4.18.

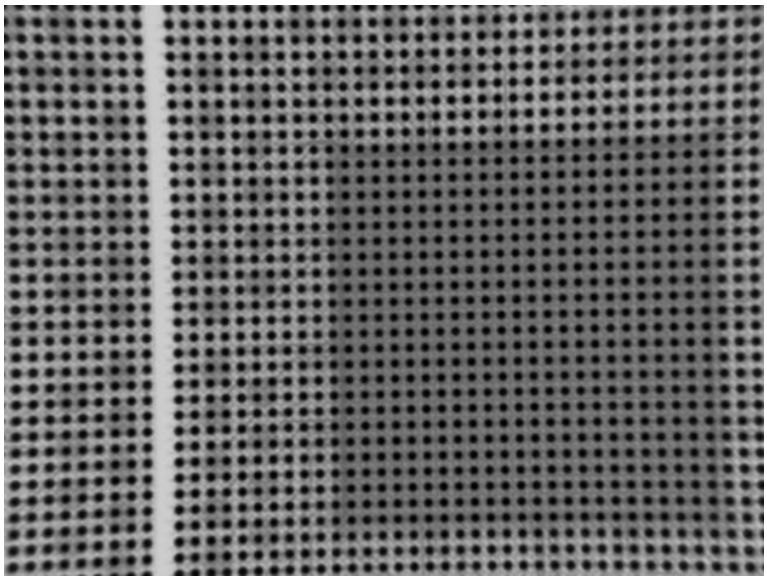


Figure 4.18: X-ray characterization after BGA balling and reflow showing no solder voids, bridging or beading.

Optical inspection was carried out to further assess uniformity in BGA size, misalignments, and bridging or missing solder balls. The solder ball diameter and height were precisely measured by 3D profilometry as shown in Fig. 4.19.

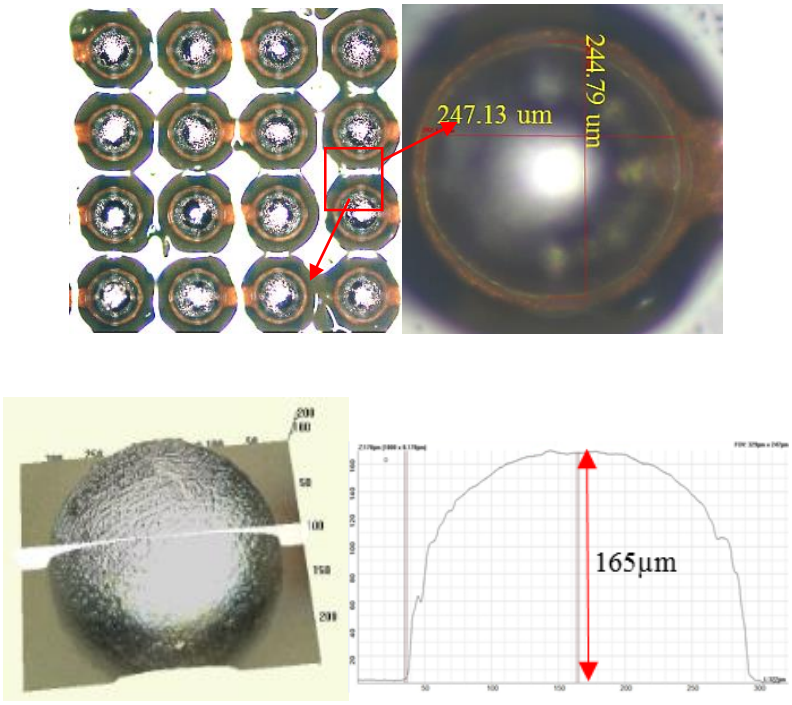


Figure 4.19: Optical inspection (top) and 3D profilometry (bottom) indicating precise dimensions of the paste printed solder balls after reflow.

The achieved ball diameter, averaged over 20 measurements from three different samples, was in the range of 243-247μm as reported in Table 4.6, within 2% tolerance of the stencil calculations.

Table 4.6: Ball diameter of paste printed BGAs: design vs. actual.

Ball diameter	**Value**
Target	250 μm
Stencil calculation (300μm opening with 5 mil thickness)	248 μm
Measured	243-247 μm
Variation	1-5 μm

4.2.4.4 Ball shear evaluation

To confirm good wetting and solderability, ball shear tests were conducted on balled glass test coupons. The ball shear force was compared to that of SAC105 BGAs, formed by a standard industry ball-drop process. Solder balls from the corners of the sample, edges and the center region were sheared, with an average strength of 5.4 kgf/mm^2, as reported in Fig. 4.20. The shear force was found comparable to that of the ball-drop BGAs with minor discrepancies that can be explained by variations in alloy composition, surface finish, and subsequent interfacial reaction.

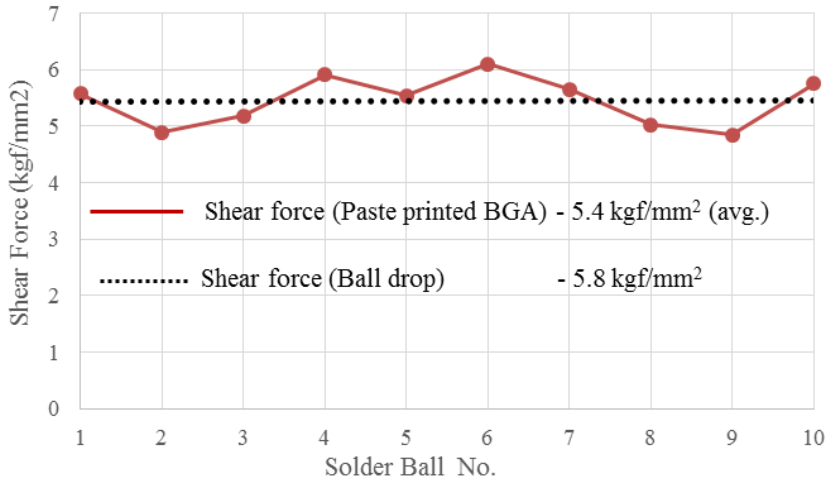


Figure 4.20: Measured ball shear strength for the paste-printed vs. ball-drop BGA balls.

4.2.4.5 BGA balling and yield evaluation

To allow for evaluation of the three target solder alloys, the glass panels were quartered by CO_2 laser at Micron Laser Technology, after chip-level assembly, as shown in Fig. 4.21.

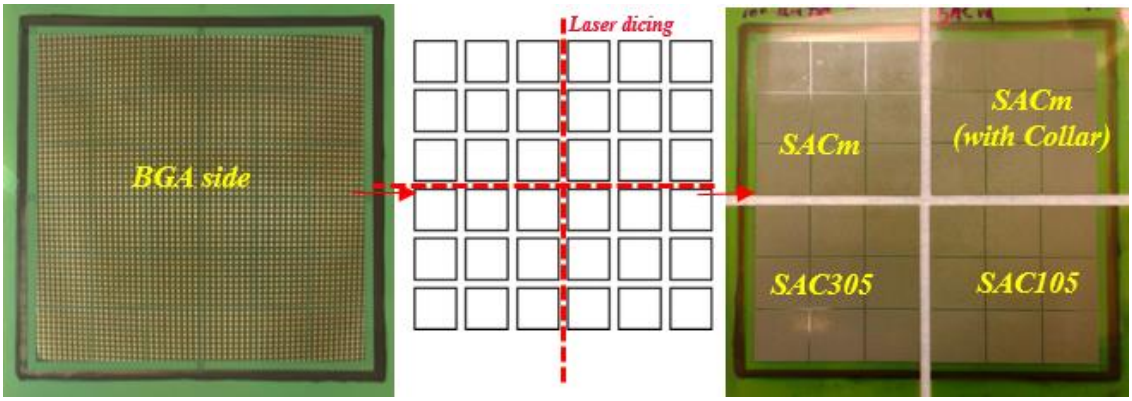


Figure 4.21: Laser dicing of glass panels into quarters and BGA balling with SACM, SAC305 and SAC105.

BGA balling was completed on the two low-CTE and one-half high-CTE panels with SACm™, SAC305 and SAC105 solders using optimized paste printing and reflow parameters. A quarter of each of the low-CTE panels, balled with SACM, was reserved for polymer collar fabrication to investigate its combined effectiveness with the doped solder

alloy on further improving thermal cycling reliability. The BGA balled substrates were finally laser diced for singulation into individual glass BGA packages, ready for SMT assembly.

Evaluation of the BGA balling yield is reported in Table 4.7. On the low-CTE samples, excellent yield was achieved, apart from minor non-uniformities in BGA size near the corners of the panels. On the high-CTE samples, the observed yield loss was caused by massive solder bridging. The latter can be attributed to the aggravated warpage as a result of higher CTE mismatch between the low-CTE (2.7 ppm/°C) die and the high-CTE glass substrate (9.8 ppm/°C).

Table 4.7: BGA balling yield on reliability glass substrates.

Type	Solder	Balling yield
Low-CTE glass (with 100µm-thick die)	SACM	18/18
	SAC305	8/9
	SAC105	6/9
Low-CTE glass (with 200µm-thick die)	SACM	18/18
	SAC305	7/9
	SAC105	9/9
High-CTE glass (with 100µm-thick die)	SACM	11/18
% total BGA balling yield		86%

4.2.4.6 Shadow-Moiré warpage response

To confirm this theory, Shadow-Moiré interferometry measurements were taken after BGA balling on both low- and high-CTE glass substrates, from 30°C to 150°C, to study their warpage behavior, as shown in Fig. 4.22.

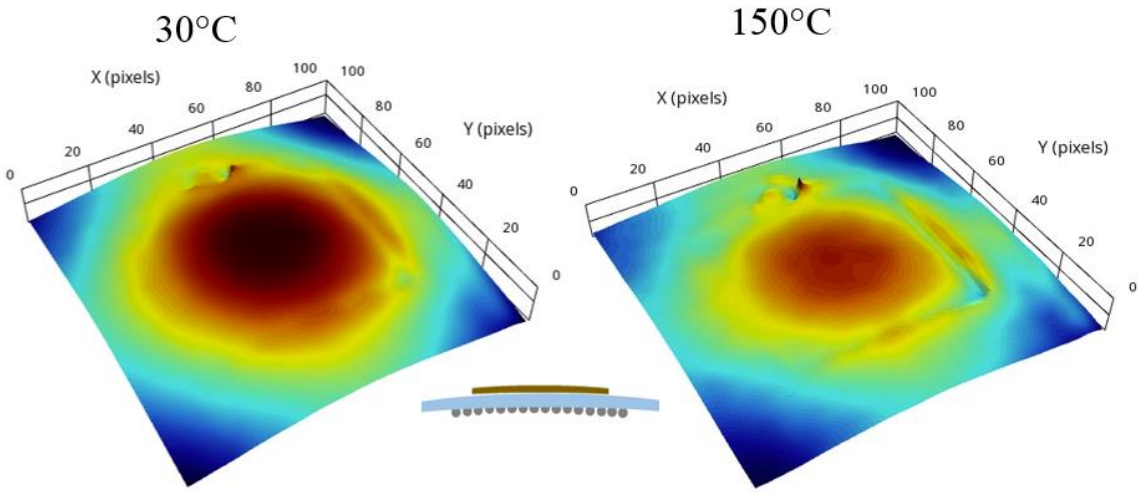


Figure 4.22: Warpage behavior by Shadow-Moiré interferometry on a low-CTE glass package with a 100µm-thick die.

JEDEC-defined full-field warpage signatures along the diagonals of the measured packages are plotted in Fig. 4.23. The warpage results indicate an expected higher net warpage of high-CTE samples compared to their low-CTE counterparts.

Warpage of a poorly yielded high-CTE sample was found significantly greater than that of a yielded sample, with 263µm instead of 198µm room-temperature warpage, demonstrating the prevalent role of warpage in degradation of the BGA balling yield. These discrepancies in warpage response can be attributed to visible variations in underfill fillet size, as reported in [67].

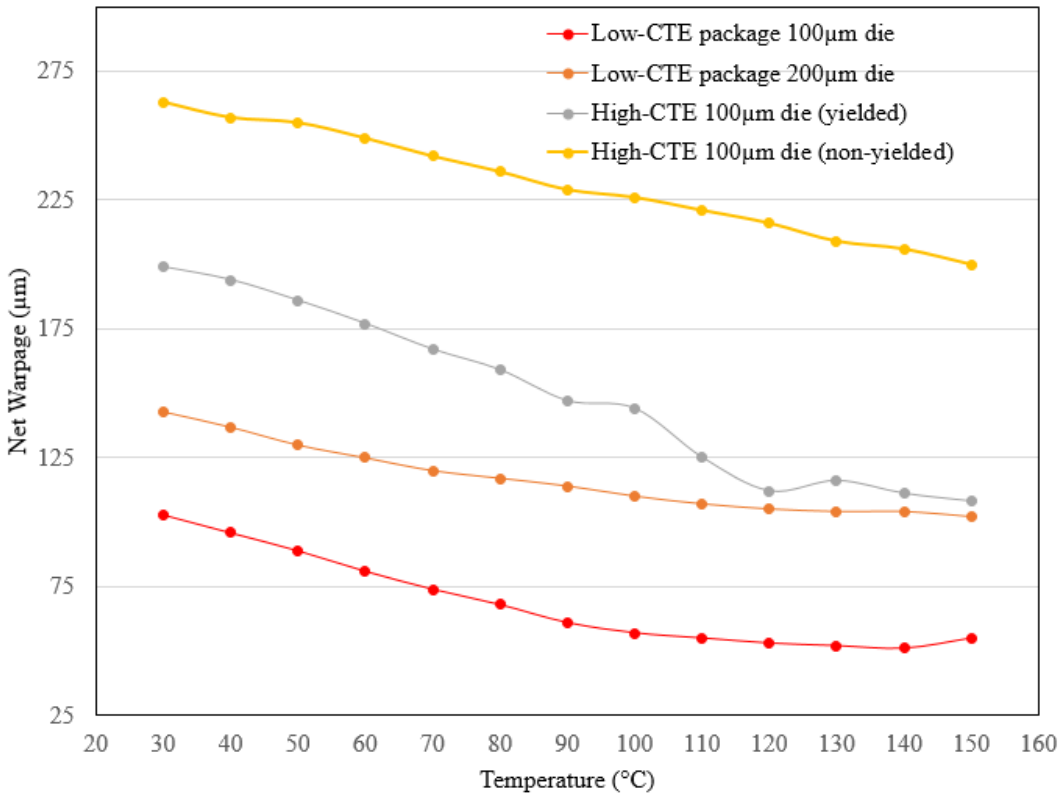


Figure 4.23: Net warpage temperature response of low- and high-CTE glass packages with considerations of BGA balling yield.

4.2.4.7 Solder paste flux residue removal

After reflow, low amounts of paste flux residue were noticed on the surface of the substrates, around the solder balls. Although, the solder paste from Indium is no-clean rated, any surface contamination would impede fabrication of the circumferential polymer collars. Flux residue cleaning was therefore necessary. Cleaning by ultra-sonication in an acetone bath produced the best results of all tested methods, as illustrated in Fig. 4.24. The samples were cleaned again with isopropyl alcohol and baked at 150°C for one hour to remove any moisture, prior to board-level assembly. Polymer collars were fabricated using the process of section 4.1.5.

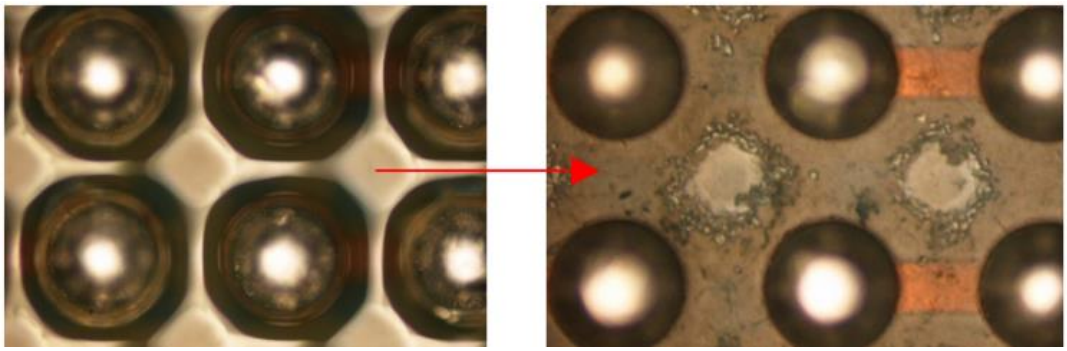


Figure 4.24: BGA before (left) and after (right) paste flux residue removal.

4.2.5 Board-level assembly and yield evaluation

The BGA balled packages were then assembled onto the boards with ENEPIG surface finish, using the Finetech Matrix fineplacer with a 10 mm x 10 mm tool and no-clean tacky flux. Consistent with standard SMT processes, the optimized reflow conditions were used to minimize BGA voiding. X-ray characterization was performed to confirm that all joints were well formed, with no non-wet, unformed solders and no head-on-pillow defects, as confirmed in Fig. 4.25.

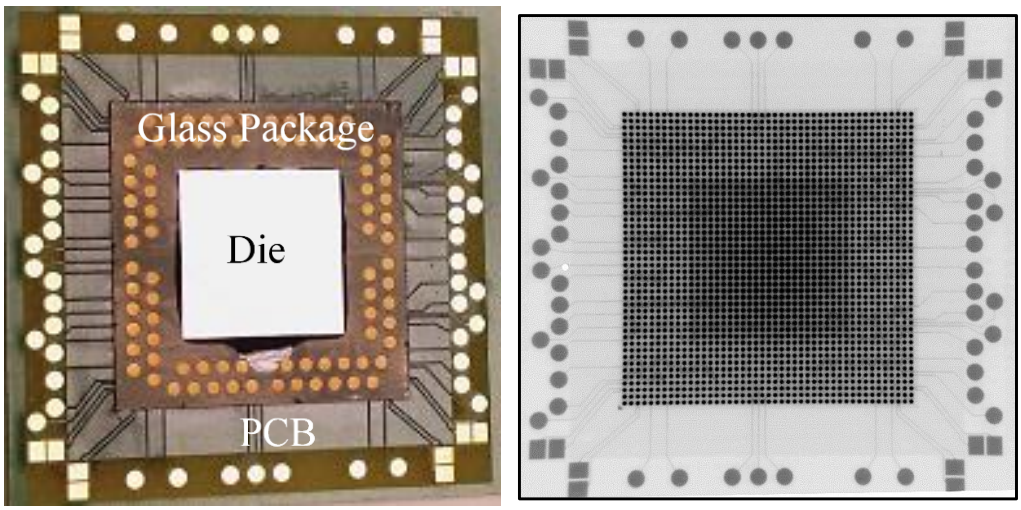


Figure 4.25: Single-chip glass package mounted on PCB: (left) optical imaging, and (right) X-ray imaging.

Suitable intermetallic formation was confirmed by cross-sectioning and scanning electron microscopy and energy dispersive spectrometry (SEM/EDS) elemental analysis of the joint's composition. In the case of SAC305 interconnections shown in Fig. 4.26 as an example, expected formation of Cu_6Sn_5 was confirmed on the package side with ultra-thin nickel-free EPAG surface finish, while both $(Cu,Ni)_6Sn_5$ and Ni_3Sn_4 were formed with ENEPIG finish on PCB side.

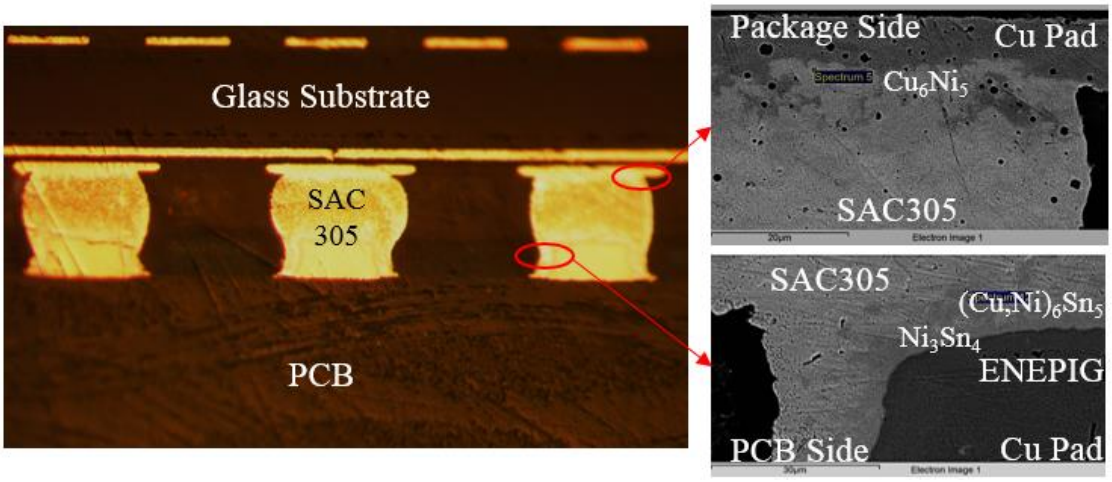


Figure 4.26: Optical and SEM/EDS characterization of paste-printed BGA after board-level assembly.

A total of 56 samples were assembled. After SMT assembly, electrical measurements of the daisy-chain resistances confirmed a 91% yield, with the following yield loss:

- 2 out of 50 low-CTE samples due to insufficient fluxing;
- 3 of the high-CTE packages due to warpage-related challenges during pick-and-place assembly.

Detailed yield results are recapped in Table 4.8., along with the thermomechanical reliability evaluation plan, considering variations in die thickness, solder alloy composition and application of polymer collars.

Table 4.8: Summary of SMT Assembly Yield and Thermal Cycling Test Plan.

Package Type	**Solder Alloy**	**Assembly Yield**	**No. of TCT Samples**
Low-CTE glass (with 100µm-thick die)	SACM	7/7	5
	SACM with collar	6/6	5
	SAC305	5/6	3
	SAC105	4/5	3
Low-CTE glass (with 200µm-thick die)	SACM	7/7	5
	SACM with collar	7/7	5
	SAC305	6/6	3
	SAC105	6/6	3
High-CTE glass (with 100µm-thick die)	SACM	3/6	3
% Total SMT assembly yield		51/56 = 91%	35

Shadow-Moiré interferometry measurements were taken after board-level assembly (Fig. 4.27) from the backside of the PCB. The results confirm lowest net warpage on the high-CTE samples, due to lower CTE mismatch between the package and the organic PCB. A maximum net warpage of 119µm was measured on the low-CTE glass samples with 100µm-thick die. The low-CTE packages with polymer collars, both with 100 and 200µm-thick dies show lower net warpage, compared to samples without collars in the evaluated temperature range of 30°C to 150°C. This indicates a potential improvement in board-level reliability performance without any significant system-level impact.

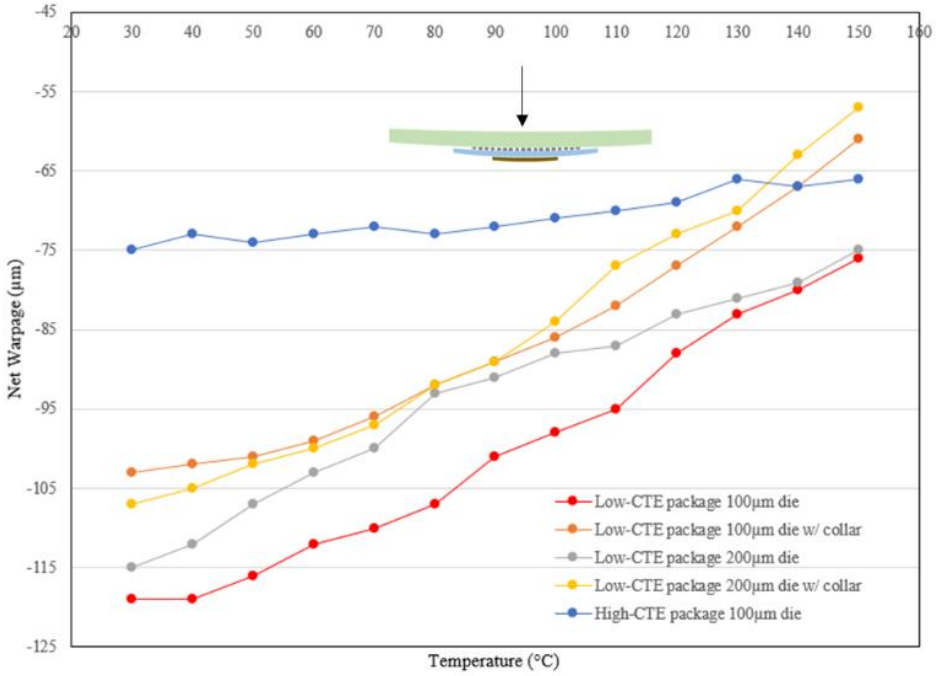


Figure 4.27: Net warpage response after board-level assembly, measured from PCB backside.

4.3 Test Vehicle 3 (TV3) – Evaluation of SACM, with Considerations of Surface Finishes

This test vehicle was designed for a comprehensive study of the drop and thermal cycling performance of SACm solder, including considerations of pad surface finish and interfacial reactions. Si wafers were chosen instead of glass substrates to accelerate failures and reduce the test time. A schematic cross-section of the test vehicle recapping the design rules is provided in Fig 4.28.

A total of 6 wafers were fabricated, 4 for thermal cycling test (TCT) with same BGA design as in TV2, and 2 for drop testing. The design rules and daisy chain stitching were slightly altered, with passivation openings of 230 instead of 220 µm, and copper pad diameter of 350 instead of 260 µm. These design rules match that of an existing test vehicle

at same BGA pitch and package body size. Design of multi-layered drop test boards is complex and not the focus of this research, explaining this decision.

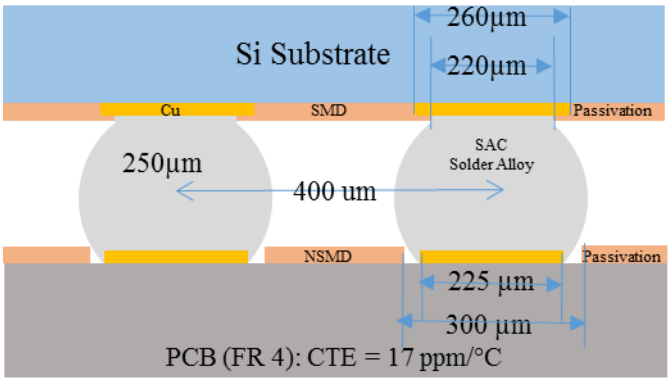


Figure 4.28: TV3 silicon substrate stack-up for thermal cycling test.

4.3.1 Test Vehicle Fabrication

Silicon wafers, 700µm in thickness, were fabricated with the process flow of Fig. 4.29. They were first cleaned with 10% H_2SO_4 to etch the oxide layer. A thin conductive seed layer of Ti-Cu, composed of 50nm Ti and 200nm Cu, was deposited. Dogbone structures were patterned by standard SAP process to a copper thickness of 10-12µm, followed by seed layer etching. The passivation layer used is silicon nitride, about 1µm in thickness. A thin layer of oxynitride was first deposited to promote adhesion prior to deposition of the SiN blanket. The passivation openings were photo-defined, and plasma etching was applied to remove any contamination on the surface of the copper pads. EPAG and ENEPIG surface finishes were finally plated by Atotech GmbH, ENEPIG was used as reference as it enables best drop and fatigue performances of all current finish materials [79]. EPAG is however evaluated in the interest of advanced packaging with high-density interconnections at sub-5µm pitches.

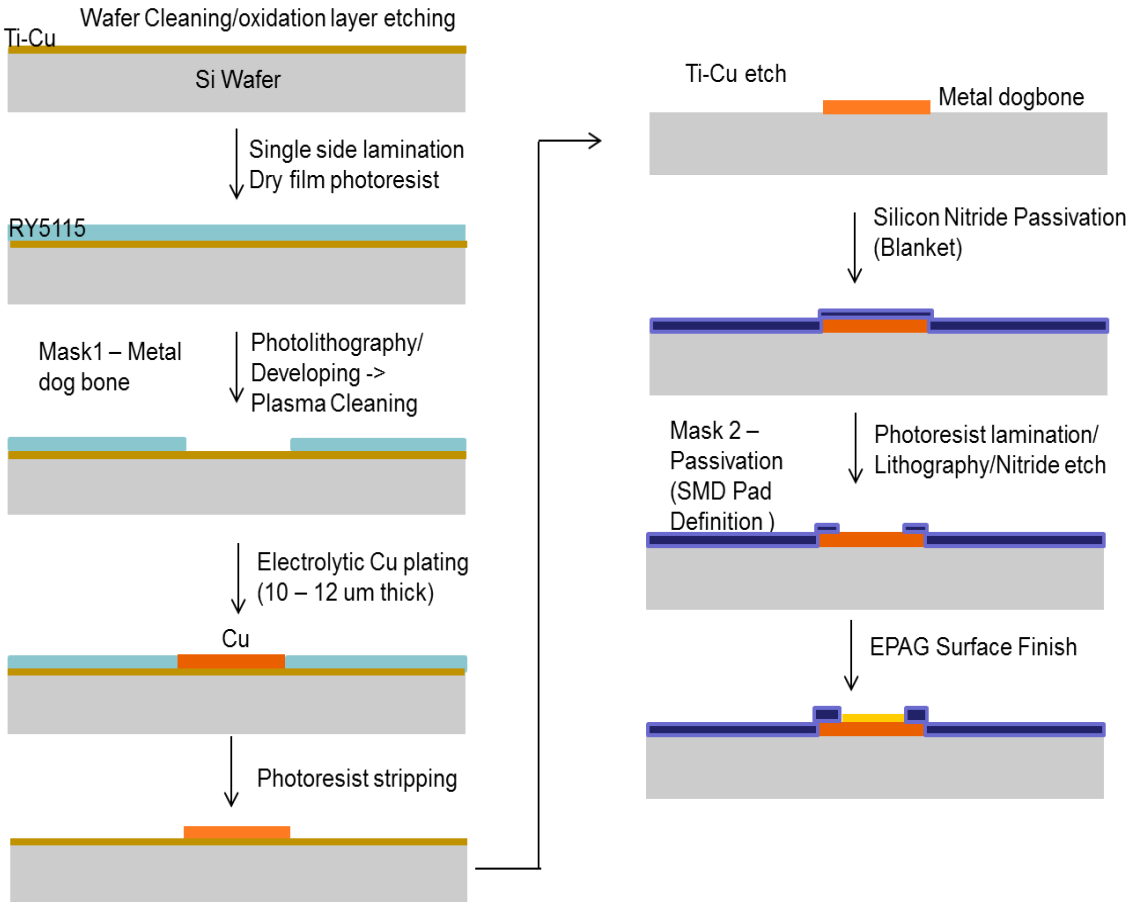


Figure 4.29: Process flow for Si TV fabrication

After fabrication, all wafers were inspected by optical microscopy for quality and uniformity. Optical pictures of a TCT and drop test sample with EPAG surface finish are shown in Fig. 4.30, with BGA pads defined by the nitride passivation.

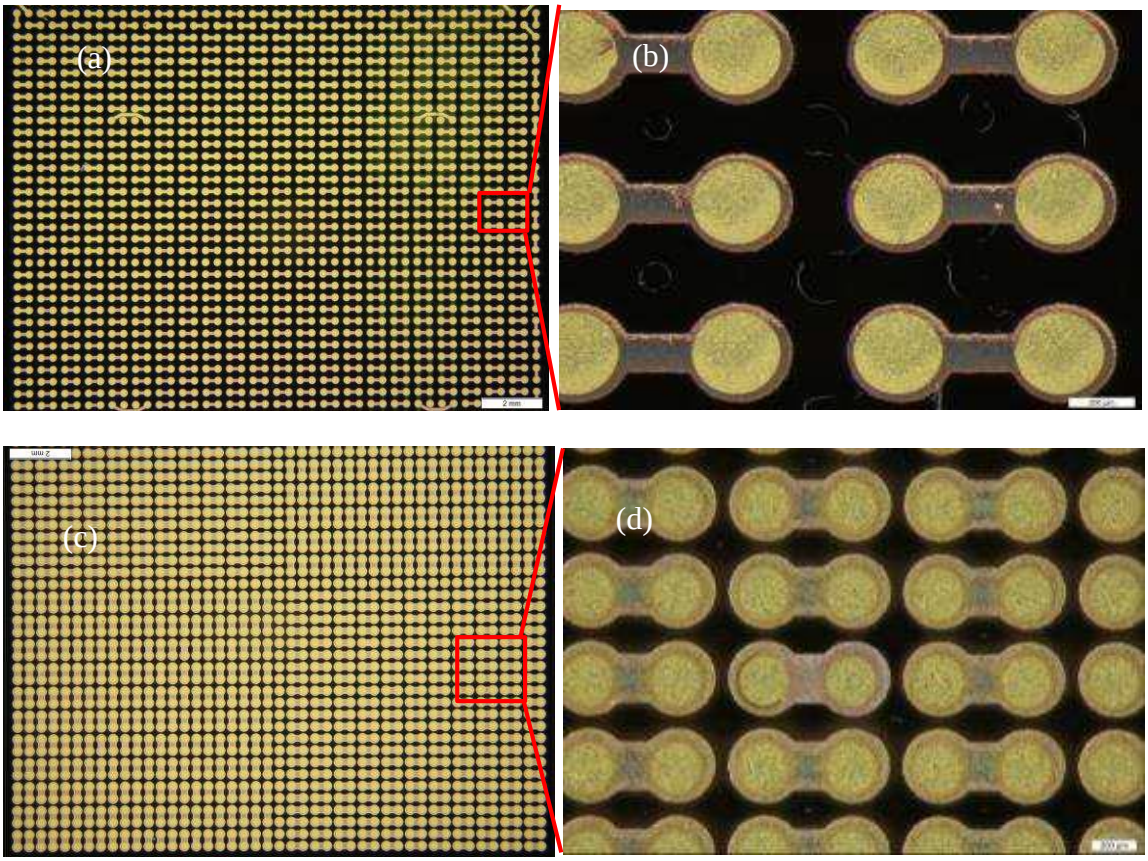


Figure 4.30: TCT sample (a), magnified in (b); Drop test sample (c), magnified in (d). [Images courtesy of Atotech GmbH, Germany]

A comprehensive experimental plan was designed as shown in Table 4.9 to fully characterize the drop and fatigue performances of the novel SACm solder. Different combinations of surface finish are considered with EPAG and ENEPIG applied on the package, and ENEPIG and OSP on the PCB board. OSP is the surface treatment of choice in cost-sensitive applications, while ENEPIG remains prevalent in high-performance systems. In the proposed plan, the reliability performance of SACm is selectively benchmarked against that of reference SAC alloys: SAC305, giving best thermomechanical reliability, and SAC105, giving best drop reliability.

Table 4.9: Experimental plan for comprehensive reliability evaluation and benchmark of SACm solder with TV3.

TCT Wafer #	Surface Finish ATOTECH	Surface Finish (Board Side Assembly) SVTronics	Solder type
1	EPAG	½ ENEPIG + ½ OSP	SAC305
2	EPAG	½ ENEPIG + ½ OSP	SACm
3	ENEPIG	ENEPIG	½ SAC305 + ½ SACm
4	EPAG	½ ENEPIG + ½ OSP	Thermal Aging [t_0, 250 hrs, 500 hrs, 1000 hrs] $^1/_3$ SAC 105 + $^1/_3$ SAC 305 + $^1/_3$ SACm

Drop Test Wafer #	Surface Finish ATOTECH	Surface Finish (Board Side Assembly) PCB Universe	Solder type
1	EPAG	½ ENEPIG + ½ OSP	½ SAC105 + ½ SACm
2	ENEPIG	½ ENEPIG + ½ OSP	¼ SAC105 + ¼ SACm

A stencil was designed and acquired for BGA balling by paste printing of TV3. Due to outsourcing of some fabrication tasks, BGA balling, assembly and reliability characterization could not be addressed, and will be pursued as future work. Results of reliability testing and detailed failure analysis of TV1 and TV2 are, however, reported in Chapter 5.

CHAPTER 5

RELIABILITY TESTING AND FAILURE ANALYSIS

This chapter presents results from reliability evaluation and failure analysis of the first two test vehicles introduced in Chapter 4. Fatigue and drop performances were comprehensively characterized for TV1, with detailed failure analysis to identify the predominant failure modes. The model predictions from Chapter 3 are correlated to experimental results to conclude on the fundamental strain-relief mechanism with polymer collars. Results of thermal cycling test to date are summarized for TV2.

5.1 TV1 Reliability Evaluation and Failure Analysis: Effect of Polymer Collars

Thermal cycling and drop reliability of low- and high-CTE glass BGA packages at 18.5mm body size is demonstrated in this section. The effect of circumferential polymer collars on the board-level reliability performance is quantified and explained based on failure analysis.

5.1.1 Thermal Cycling Test Results

5.1.1.1 Procedure and Failure Criteria

Thermal cycling test (TCT) was conducted following JEDEC JESD22-A104D standard, between temperatures of -40°C and 125°C with a dwell time of 15 min at each temperature extreme, completing one cycle/hour. The resistance of each daisy chain of the test vehicles was monitored every 100 cycles. The failure criteria were either an increase in the chain resistance by 20% or electrically open daisy chain. The profile for thermal cycling is shown in Fig 5.1.

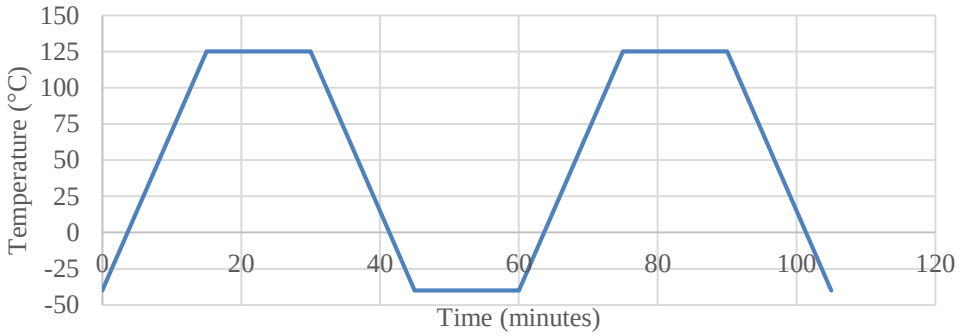


Figure 5.1 Temperature profile for thermal cycling test.

5.1.1.2 Test Results

A total of 20 samples were put into TCT, 10 each of low-CTE and high-CTE glass, 5 of each were with and without collars. Electrical measurements taken after every 100 cycles confirmed that all sample configurations qualified a minimum of 1000 thermal cycles. To date and over the course of a year, the high-CTE samples have survived 4600 cycles with stable daisy chain resistances, as shown in Fig 5.2. Testing of these samples is still ongoing and will be pursued until failure. However, the first failure in low-CTE samples was recorded at 1100 cycles on account of higher CTE mismatch to the board. Table 5.1 summarizes the number of cycles to failure of low-CTE samples, with and without collars, as well as the failure distribution between corner and inner daisy chains. As expected, the majority of failures affected corner daisy chains.

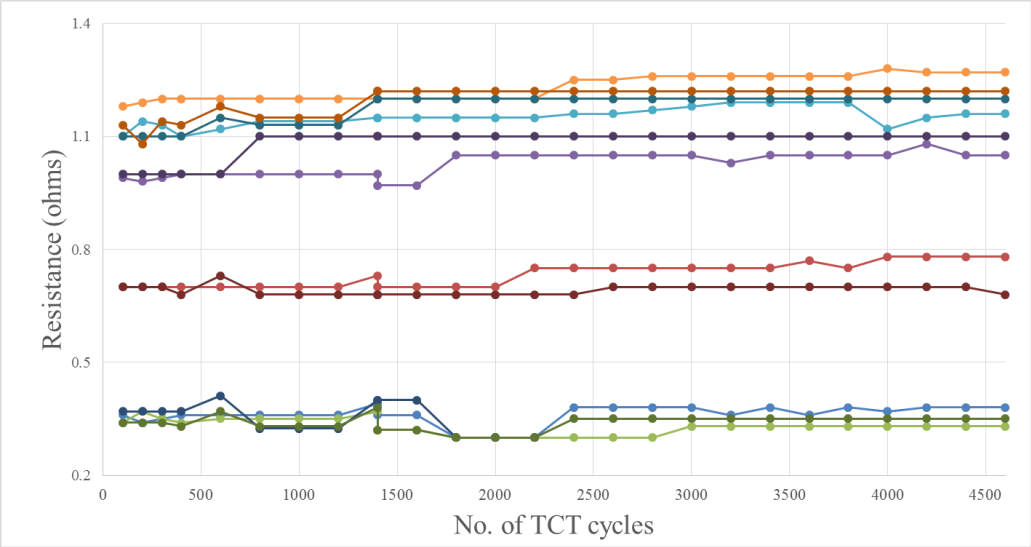


Figure 5.2: Daisy-chain resistances of a high-CTE sample, stable across 4600 thermal cycles.

Table 5. 1 Failure distributions in low-CTE glass samples.

	Failed Sample#	**Corner chains**	**Inner chains**	**Failed @**
No collars	1a	3/4	2/46	1100
	1b	2/4	1/46	1100
	1c	2/4	2/46	1100
	1d	1/4	1/46	1200
	1e	1/4	0/46	1200
With collars	**Failed Sample #**	**Corner chains**	**Inner chains**	**Failed @**
	2a	2/4	2/48	1400
	2b	2/4	1/46	1400
	2c	1/4	1/46	1400
	2d	1/4	0/46	1500
	2e	1/4	0/46	1600

Low-CTE samples systematically failed between 1100 and 1200 cycles without polymer collars, but only experienced failure after 1400-1600 cycles with collars. Polymer collars, therefore, bring a 30% improvement in the fatigue life of the SAC105 BGA interconnections, as shown in Fig. 5.3.

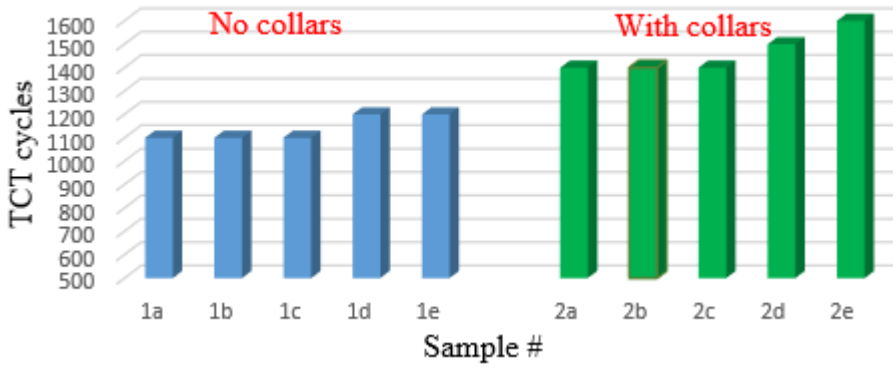


Figure 5.3: Bar graph of first failure in low-CTE samples.

5.1.1.3 Failure Analysis and Characterization

Failure analysis of the TCT samples was performed with three characterization methods:

i) C-SAM to inspect the structural integrity of the glass package;

ii) Cross-section and optical analysis of failed interconnections to determine the predominant failure modes;

iii) SEM-EDS characterization to investigate and conclude on failure mechanisms.

C-SAM Characterization

C-SAM was carried out on failed samples to verify the structural integrity of glass and confirm that no chipping, cracking or delamination occurred in the substrates during thermal cycling. No defects could be observed as confirmed by the scans of Fig 5.4, comparing a failed TCT sample to a similar glass package with severe cracking.

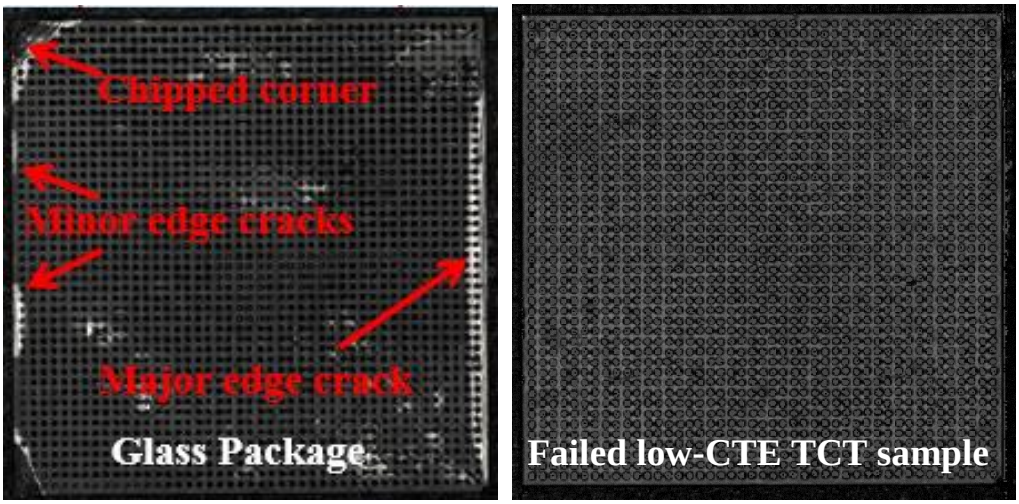


Figure 5.4: C-SAM of reference sample (left) with defects, and failed low-CTE sample after 1400 cycles (right).

Optical inspection

To identify the predominant failure modes, the samples were molded in epoxy resin for cross-sectioning. Capillary underfill was applied to prevent any solder smearing during polishing. Two distinct failure locations were observed depending on the presence of polymer collars.

Without collars, cracks in the solder joints were found to initiate close to the IMC-to-solder interface on the glass package side, and propagate in the bulk of the solder (Fig. 5.5). Across all the corner and inner circuit BGA interconnections inspected on 4 samples, no cracks were observed on PCB side.

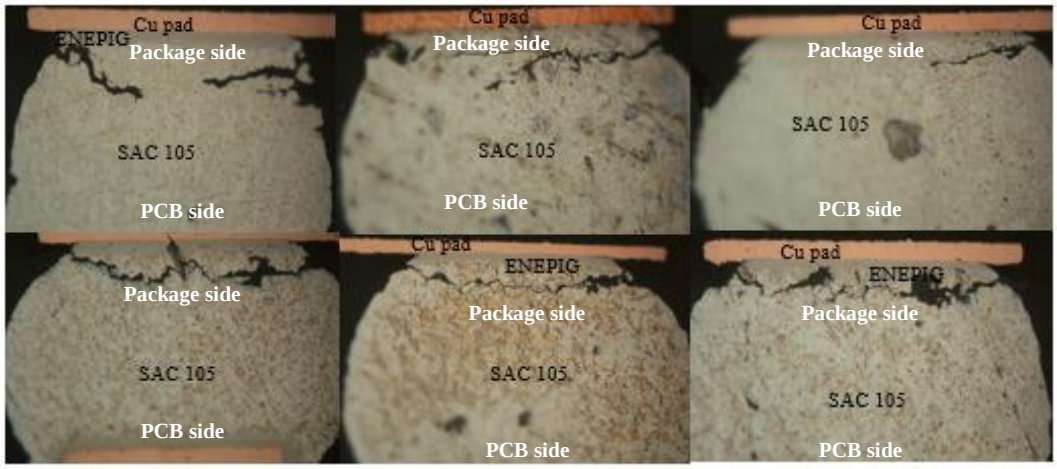


Figure 5.5: Cross-section of failed low-CTE samples without collars.

In samples with collars, cracks initiated at the IMC-to-solder interface on PCB side, and then penetrated in the bulk of the solder, as shown in Fig 5.6. Similarly, no cracks were observed in any other location in the presence of collars.

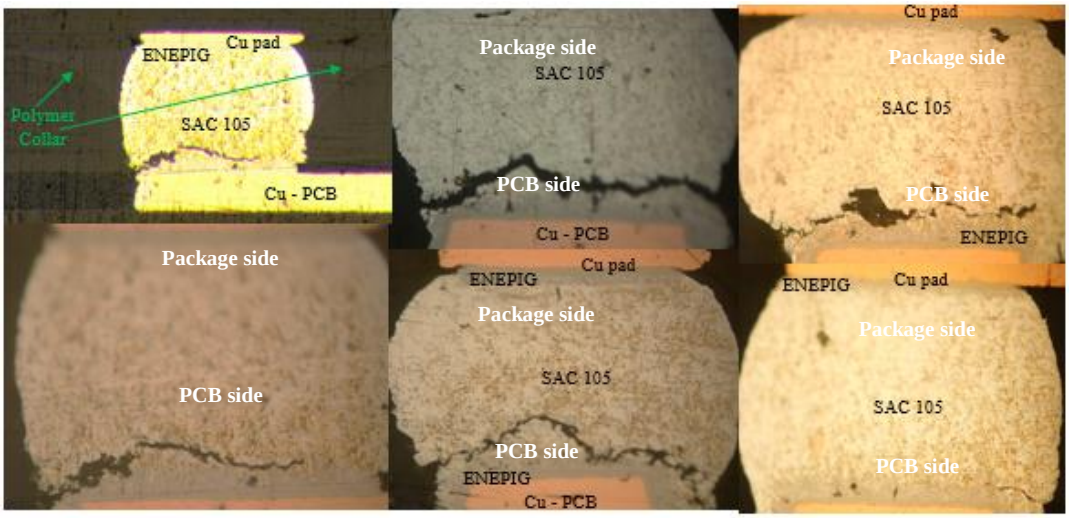
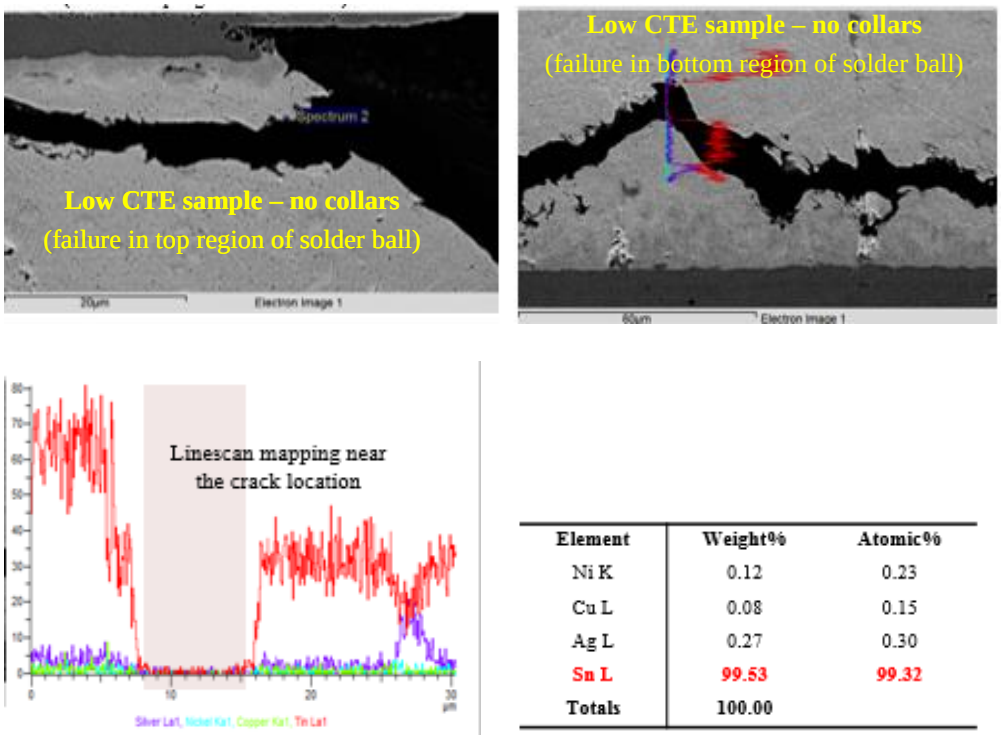


Figure 5.6: Cross-section of failed low-CTE samples with collars.

Scanning Electron Microscopy

The cross-sections were finally imaged by SEM to confirm the failure mechanisms previously identified. While cracks originated at the interface between intermetallics and residual solder, multiple linescan mapping (Fig. 5.7) indicated that they indeed propagated in the bulk of the solder.



Element	Weight%	Atomic%
Ni K	0.12	0.23
Cu L	0.08	0.15
Ag L	0.27	0.30
Sn L	99.53	99.32
Totals	100.00	

Figure 5.7: SEM/EDS data showcasing failure locations in low-CTE samples.

From failure analysis, it can be deduced that the collar protects the regions of critical strain concentration shifting cracks from top to the bottom region of the solder ball delaying failure thereby improving TCT performance.

5.1.1.4 Correlation with modeling results

The modeling results for warpage trends and the predicted fatigue life of SAC105 solder were investigated in this section.

Warpage characterization

In order to confirm the warpage trends from modeling data, Shadow-Moiré measurements were carried out on low-CTE samples with and without polymer collars. Modeling and experimental warpage results are plotted in Fig. 5.8. Warpage measurements confirm reduction in net warpage with polymer collars, in the evaluated temperature range from 30°C to 160°C. Further, the change of slope observed in experiments indicates an

increase in effective CTE of the package with addition of polymer collars, as predicted by the model. Trend lines were added in Fig. 5.8. (a) as dashed lines for more direct comparison of the slopes for each warpage trend. While modeling and experiments converge on the global effect of polymer collars, large discrepancies are observed in net values. These discrepancies can be due to inaccurate representation of the real mechanical behavior of some of the modeled materials, in particular the FR-4 PCB.

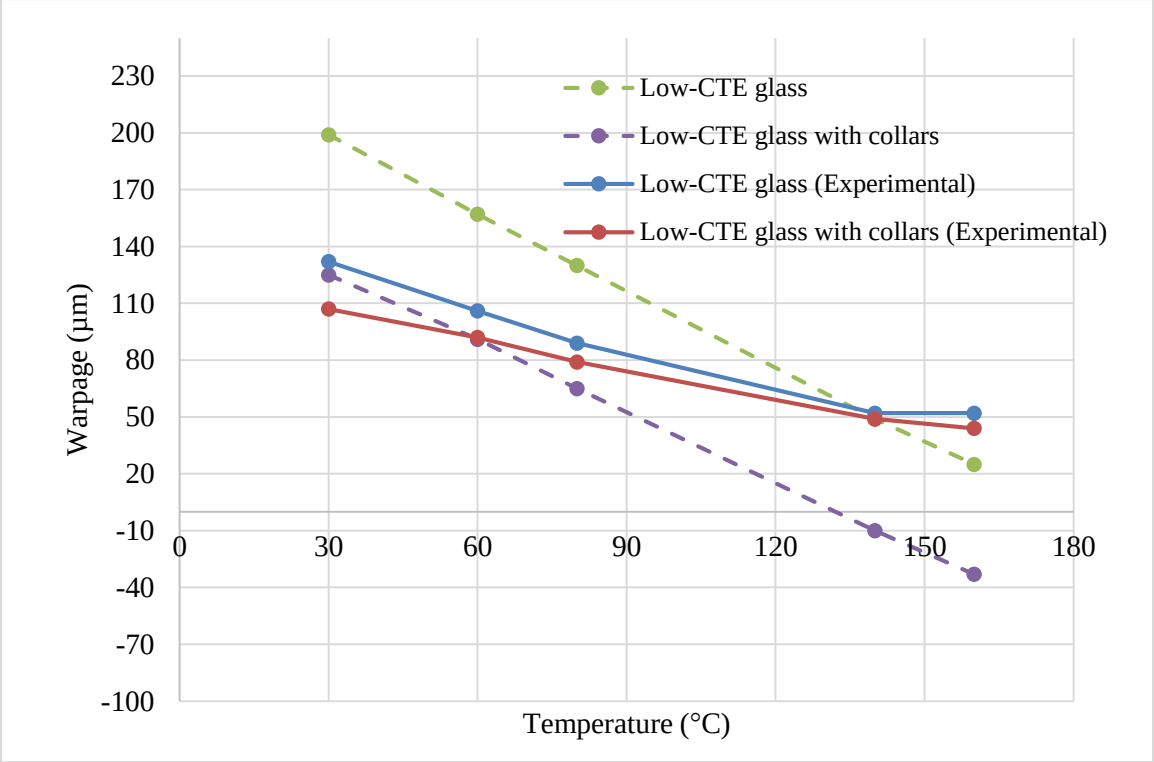


Figure 5.8: Warpage trends for low-CTE samples with and without collars from (a) modeling, and (b) experiments.

3D contour plots and displacements along the diagonals at 30°C are shown in Fig 5.9.

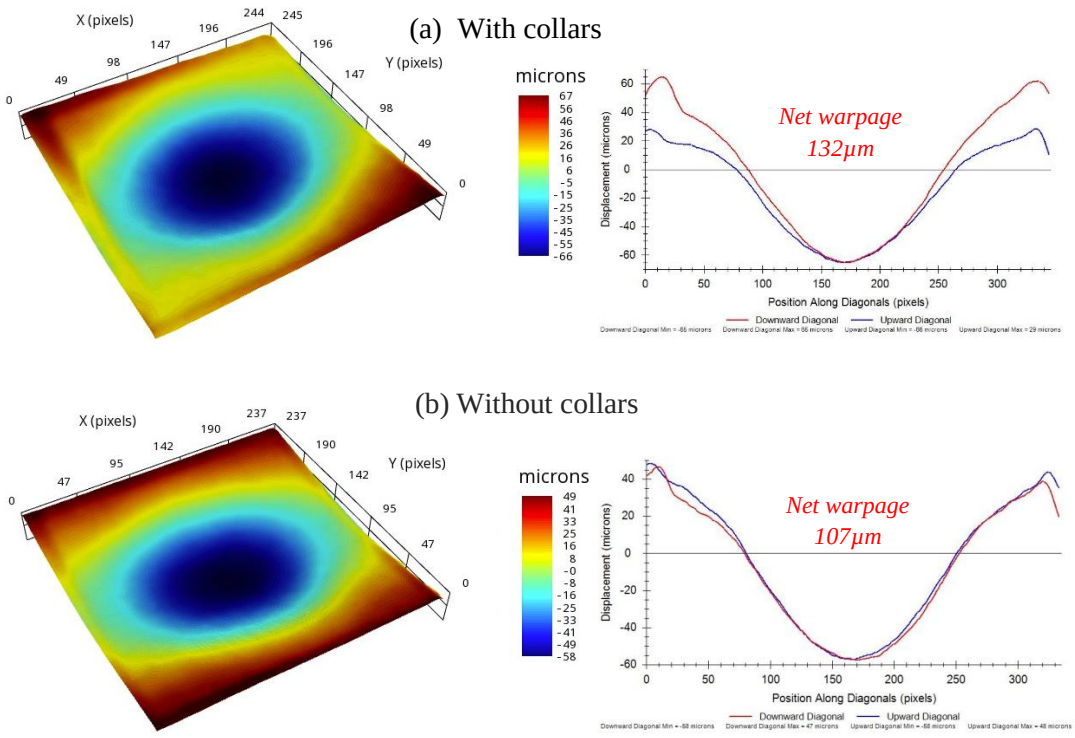


Figure 5.9: Shadow-Moiré 3D contour plot at 30°C and corresponding displacements along the diagonals for low-CTE glass packages (a) with and (b) without collars.

Fatigue Life of SAC105

Based on the fatigue life of low-CTE glass packages is compared to calculations with both Coffin-Manson and Engelmaier-Wild models from Chapter 3 in Table 5.2 with good correlation.

Table 5.2: Fatigue life of SAC105 interconnections: calculations vs. experimental.

Glass Package	N_f **Coffin-Manson**	N_f **Engelmaier-Wild**	**Experimental (Mean value)**
Low-CTE	843	1255	1140
Low-CTE with collar	1188	1892	1460
High-CTE	2839	5378	*> 4600 (still in test)*
High-CTE with collar	4422	9147	*> 4600 (still in test)*

Predictions of preferential failure location from analysis of solder strains were found accurate. In the absence of collars, high strain concentrations were observed on

package side where all solder cracks were located, as illustrated in Fig. 5.10 (a). In the presence of collars, higher strains were again seen on package side, at the pad interface and where collars meet solder. Both sites were ruled out as critical failure locations on account of compressive stresses from the collars and geometrical singularities, respectively, as detailed in section 3.5. Failures were, therefore, expected in the third-most high-strain location highlighted in Fig 5.10 (b): the pad-to-solder interface on PCB side. Cracks were only observed at the bottom of the solder joints, confirming the model predictions.

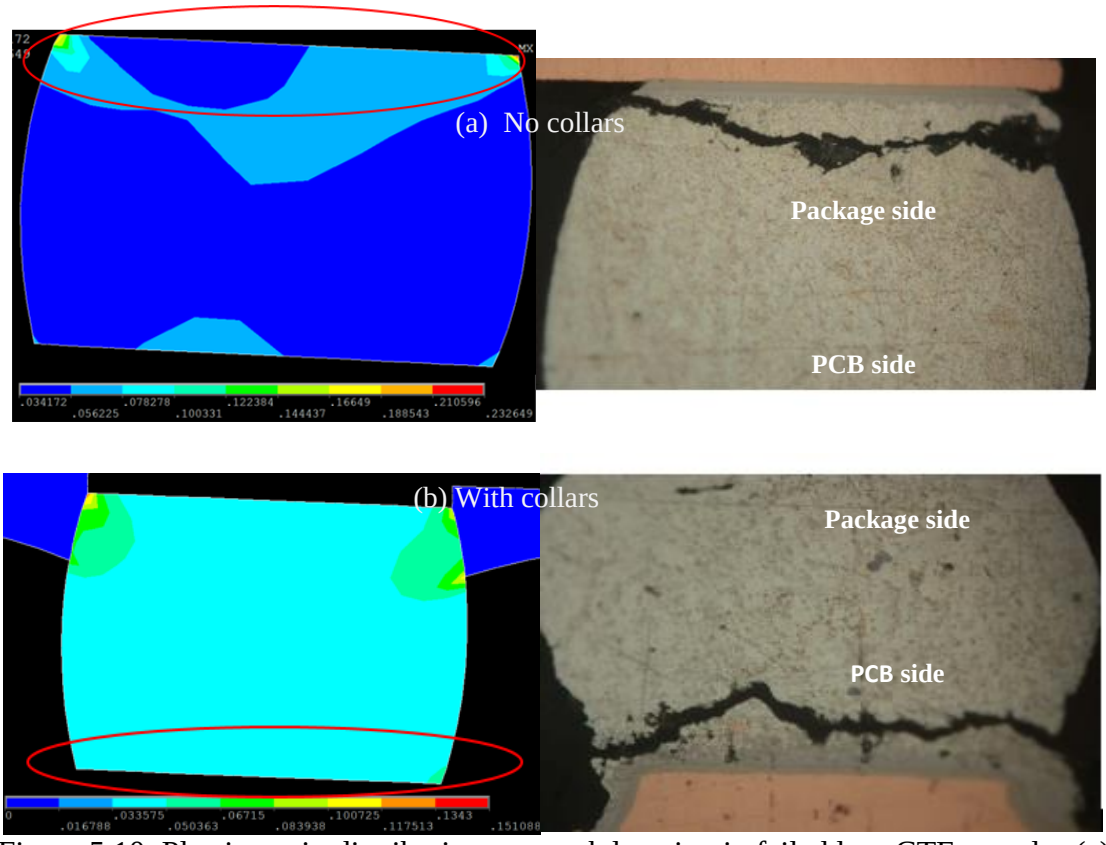


Figure 5.10: Plastic strain distribution vs. crack location in failed low-CTE samples (a) without collars, and (b) with collars.

Further, a low number to no solder cracks were consistently observed during inspection of the failed samples moving towards the inner circuit, regardless of the

presence of collars. Lower strain concentrations were predicted by the 2D simulations, explaining this trend. This result is illustrated in Fig. 5.11.

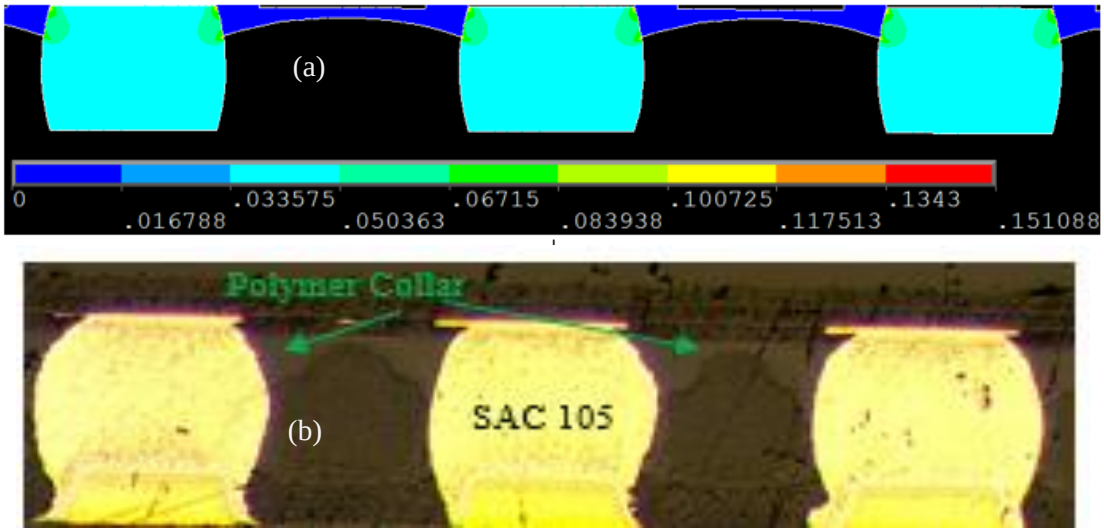


Figure 5.11: Plastic strain distribution and cross-section of BGAs from the inner circuit in low-CTE samples with polymer collars.

5.1.2 Drop Test Results

5.1.2.1 Drop Test Procedure

Drop testing was performed with respect to JEDEC JESD22-B111 using a Lansmont shock test machine. Boards were mounted to the shock table, with components facing down as shown in Fig. 5.12. Test boards were subjected to a 1500-G, 0.5ms duration shock pulse. The resistance of both chains of each package was monitored in-situ at a rate of 250 kHz. Testing concluded at 200 drops.

As per JEDEC standards, failures were defined as instances of discontinuity in resistance measurements which were verified by at least more instances in the next five drops. All samples were manually probed at the end of the test to verify the fails recorded in-situ.

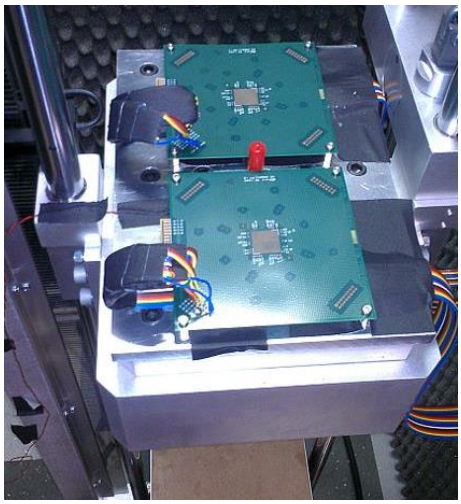


Figure 5.12: Drop test boards mounted to the shock machine, wired for in-situ resistance monitoring.

5.1.2.2 Drop Test Results

The sample configurations placed in drop testing is shown in Table 5.3, with a total of 12 boards evaluated with up to 4 samples mounted on each board. Daisy-chain resistances were measured by the data acquisition (DAQ) system during each drop cycle.

Table 5.3: Drop test evaluation plan.

In Test	Low-CTE Glass		High-CTE Glass
	No Collars	Collars	No Collars
# of Boards	4	4	4
# of Samples	14	16	16

Daisy-chain failures were established based on the following criteria: a) a 20% increase in daisy-chain resistance, b) the corner daisy chain to survive at least 40 drops, and c) no failure of the signal daisy chain for at least 200 drops.

The drop test results for the corner and signal circuits are summarized and explained in Table 5.4. For the corner circuit, marginal failures were observed on both low- and high-CTE samples without collars. Approximately 50% of the corner nets failed before 200 drops across all samples. However, for the low-CTE samples with polymer collars, the first

failure was observed at 84 drops which is more than twice the expected failure past the 40th drop cycle. No failures on the signal circuit were detected. One failure at 162 drops reported for a low-CTE polymer-collar sample was not confirmed after test, likely due to a wiring issue on the DAQ system. These results indicate that polymer collars improve the drop performance of both corner and inner signal circuits by 2X.

However, high-CTE samples without collars appear to have three failure distributions: a fail at six drops, likely due to latent manufacturing defects, and failures at 47 & 54 drops which is 50% lifetime of the next distribution, failing past 100 drop cycles. These discrepancies are not well understood but might be related to variability in the fabrication processes.

Table 5.4: Summary of drop test results.

Sample/ Variable	Corner Circuit				
	# of Fails	1st Fail Cycle #	Nominal 5% Fail	β	η
Low CTE, No Polymer Collars	8/15	24	23	1.456	179
Low CTE, Polymer Collars	7/16	84	73	2.739	217
High CTE, No Polymer Collars	7/16	6	10	0.705	558
Sample/ Variable	Signal Circuit				
	# of Fails	1st Fail Cycle #	Nominal 5% Fail	β	η
Low CTE, No Polymer Collars	0/13	--	--	--	--
Low CTE, Polymer Collars	1/15	162	--	--	--
High CTE, No Polymer Collars	0/16	--	--	--	--

PASS MARGINAL FAIL

A Weibull failure distribution was fitted, as plotted in Fig. 5.13. A low Weibull slope (β) suggests a wide range of variability caused by a yield issue at time t_0 possibly due to process defects in substrate fabrication. In addition, due to the low number of samples and the wide failure distribution, absolute values of unreliability may not be used and hence the conclusions on the effect of glass CTE remain unclear.

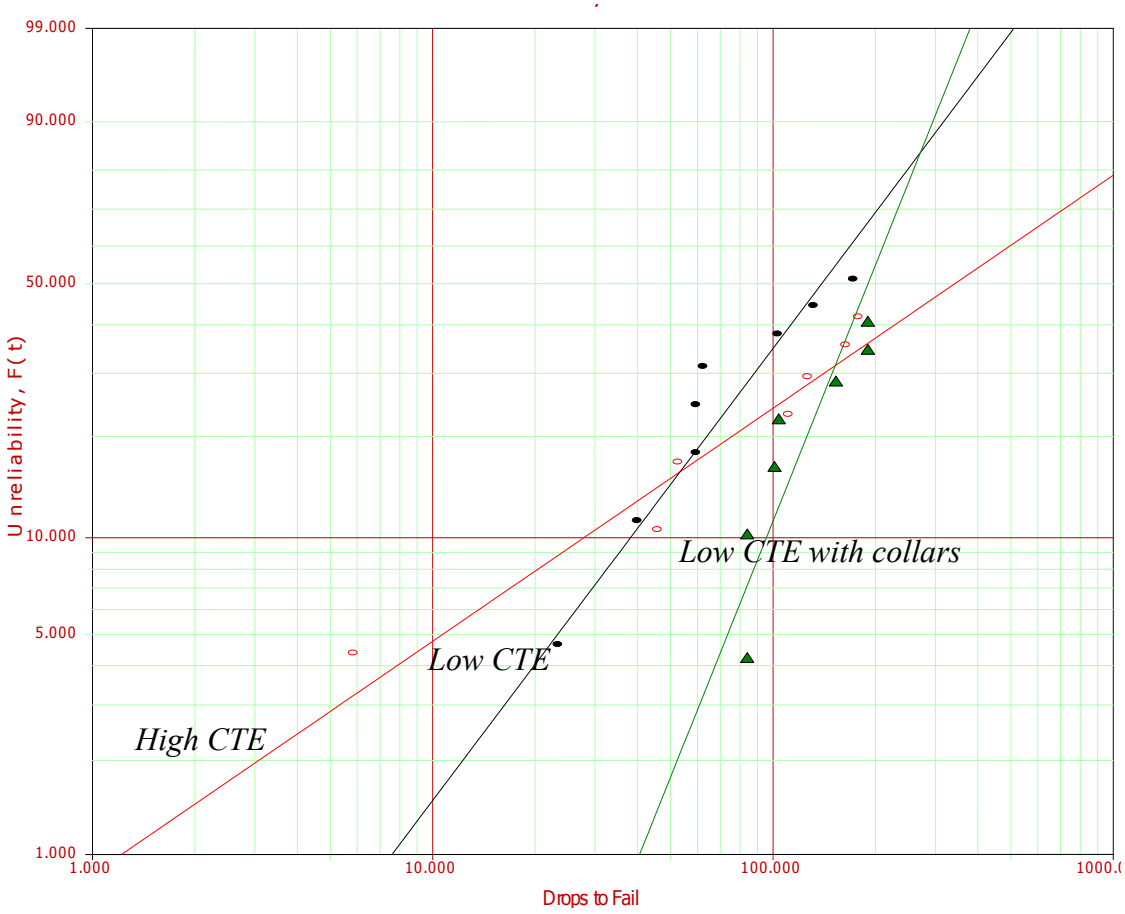


Figure 5.13: Weibull failure distribution plot for drop testing of glass BGA packages.

5.1.2.3 Failure Analysis

Failure analysis of the drop test samples was performed again with three characterization methods (CSAM, optical microscopy and SEM/EDS) similarly to the TCT samples.

C-SAM Characterization

After drop testing, all samples were subjected to C-SAM inspection with a 230 MHz transducer. No delamination or any sign of cohesive glass cracking could be observed despite minor initial defects. The polymer applied to protect the glass edges was therefore effective in preventing crack propagation. However, C-SAM using a lower frequency 50 MHz transducer with a better penetration depth showed signs of non-coplanarities on a reference sample as highlighted by the red oval in Fig. 5.14. These non-coplanarities resulted from warpage of the attached 12mm x 12mm 100μm-thick die from non-uniform underfilling.

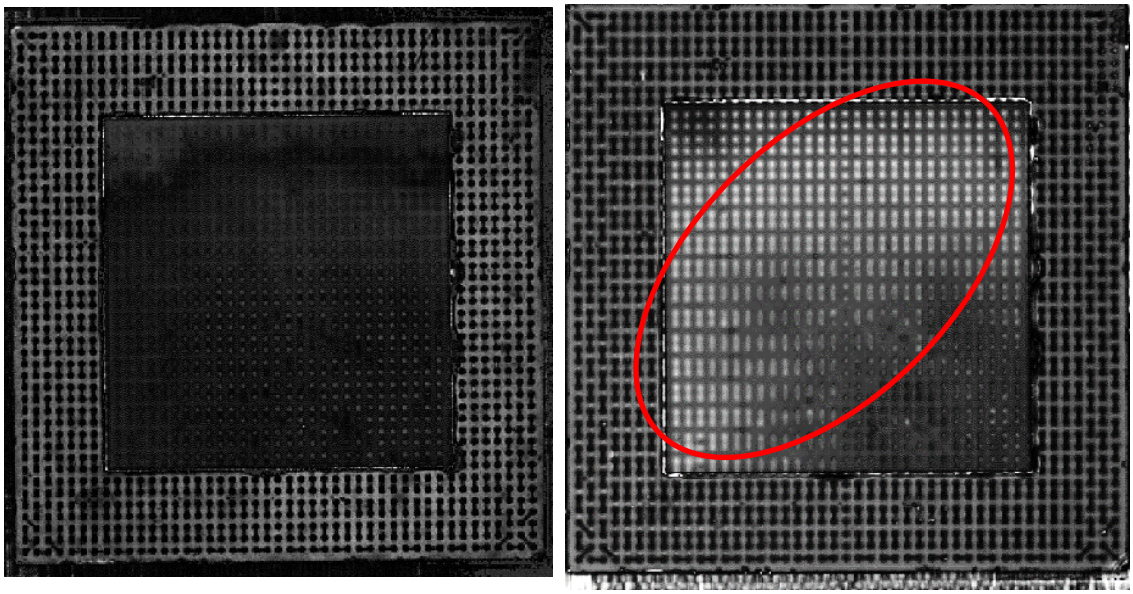


Figure 5.14: C-SAM characterization of drop test sample with 230 MHz (left) and 50 MHz (right) transducers.

Optical Characterization

The failed samples were singulated from the test boards, underfilled to prevent solder smearing during polishing and molded in epoxy resin for cross-sectioning, to identify the prevalent failure modes. Inspection of the solder balls in individual rows

indicated a general trend that defects attenuated towards the inner circuit from the corners, which is expected as the BGA gets closer to the neutral point.

Table 5.5 recaps the observed failure modes, where Mode 1 (Fig. 5.15) failure in the Cu routing layer was found most predominant among all sample types. For Mode 1, if the crack failure was not in-plane, it went undetected and the next row of solder balls was then inspected. This process was repeated for up to three consecutive rows. Several other studies have indicated Mode 1 failure to be a common failure mechanism for drop test reliability [80, 81].

A crack in the copper trace is initiated at the point where there is critical stress concentration. In the presence of strong intermetallic adhesion strength, the failure migrates to the thin copper trace where stress exceeds its ultimate strength [81]. Mode 2 failures were found to be near the Cu-Ni interface as confirmed through SEM-EDS characterization.

Table 5.5: Failure distribution of drop test samples.

Sample/Variable	**Total samples polished**	**Mode 1**	**Mode 2**
High CTE no collars	4	3	3
Low CTE with collars	2	1	-
Low CTE no collars	2	1	-

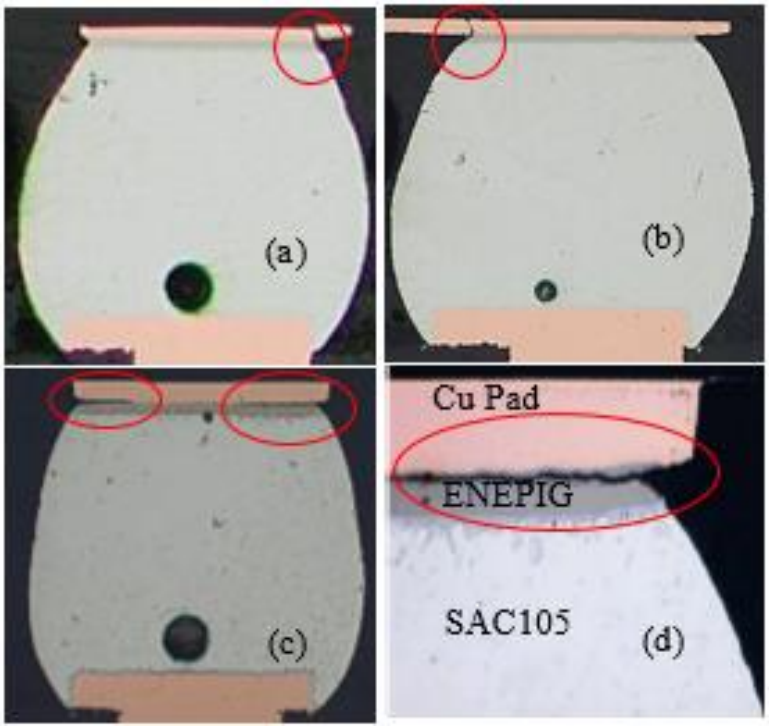


Figure 5.15: Optical images of cross sections of failed drop test samples with: (a, b) Mode 1 failure: crack in the Cu routing layer; and (c, d): Mode 2 failures: crack in the Ni layer near the Cu-Ni interface.

More importantly, for low-CTE samples with polymer collars, no Mode 2 failures were observed. This can be explained by compressive stresses applied by the polymer collars near the surface finish that protect against Mode 2 failure. Moreover, polymer collars couple the interface between solder ball and copper pad, acting as a partial underfill that blocks shear deformation, and redistributing the load to reduce overall plastic strains. Further analysis was carried out by SEM to determine the cause of Mode 2 failures in the high-CTE samples without collars as it is not a standard failure mechanism.

SEM-EDS Characterization

For all high-CTE samples, multiple linescan mappings for Mode 2 failures using SEM-EDS characterization indicated that cracks occurred where the concentration of Cu drastically decreases near the Cu-Ni interface in the bulk Ni region itself as shown in Fig.

5.16. Under mechanical stresses from drop testing, it was observed that the cracks initiated and migrated in the Ni-rich phase in ENEPIG, as it is more brittle than Cu [82]. A quantitative analysis of nickel phosphorus layers in the ENEPIG surface finish confirmed the phosphorus content to be in the expected 8-9% range. Excellent solderability was confirmed with good IMC formation achieved during BGA balling.

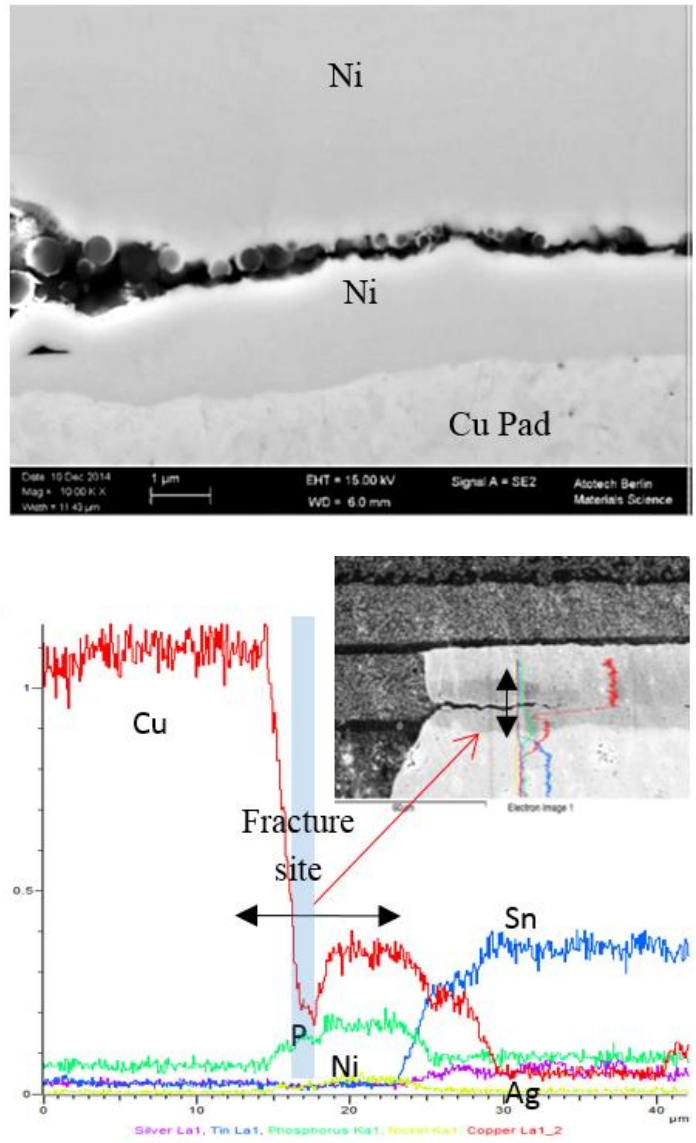


Figure 5.16: SEM image (top, courtesy of Atotech) and EDX characterization of Mode 2 fracture (bottom).

Several point scan mappings at the pad edge tip, as highlighted by the red circle in Fig. 5.17, reveal necking of the SMD-defined ZIF material at the surface finish-Cu pad interface. Such necking causes stress concentration, which may be the principal cause for crack initiation in the Ni layer.

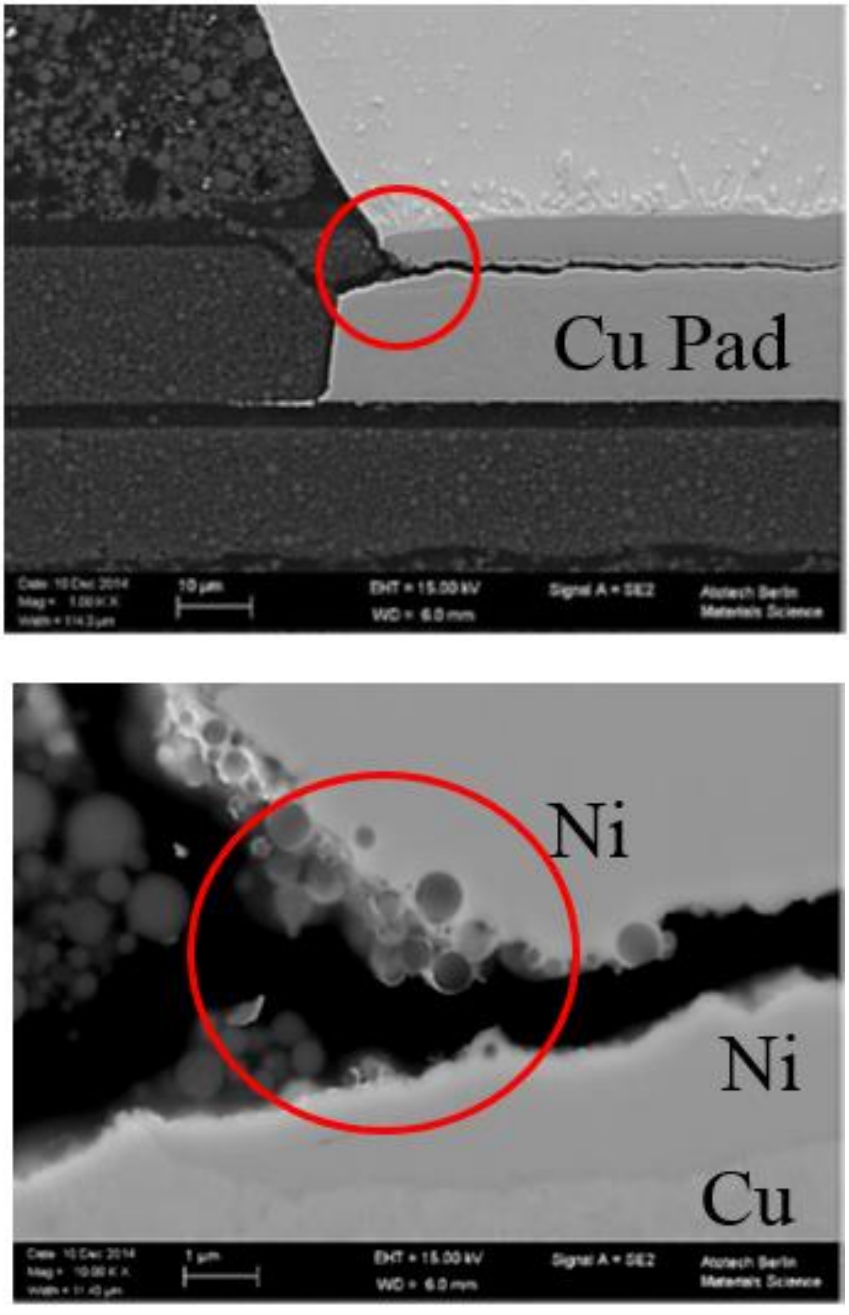


Figure 5.17: Necking at pad edge tip (top), magnified view of fillers (bottom) indicating some ZIF residue on the copper pad. (Images courtesy of Atotech.)

Point scan mappings at central sites away from the crack tip, indicated by the red circles (site 1 and site 2) in Fig. 5.18, reveal the presence of small fillers from the ZIF material at the Ni and Cu pad interfaces. The samples with the SMD-defined ZIF material were fabricated by laminating the ZIF film over the Cu pads and laser drilling openings to expose the Cu pad surfaces. Plasma etching was subsequently applied to remove any contamination from the pad surface. Inadequate or ineffective cleaning may have caused ZIF residues on the Cu pads onto which the ENEPIG surface was plated, creating a clear path for crack propagation and contributing to Mode 2 failures.

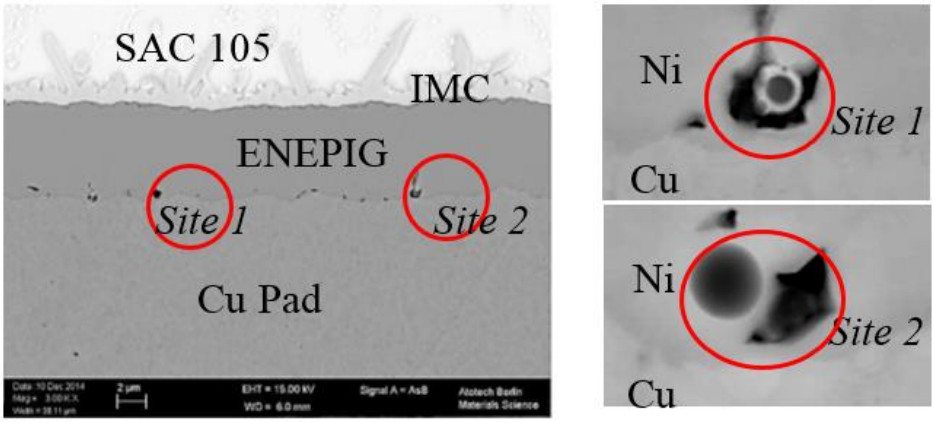


Figure 5.18: ZIF fillers at central sites (left), magnified view of fillers - site 1 (top right), site 2 (bottom right). (Images courtesy of Atotech.)

This constitutes the first demonstration of drop test reliability of glass BGA packages. No glass-specific failures modes were observed, mode 1 matching expectations, while mode 2 was declared process-related. Improvement in drop performance by 2X with polymer collars was demonstrated. Polymer collars therefore constitute a key technology to achieve balanced drop and thermomechanical reliability, while maintaining SMT compatibility and reworkability.

5.2 TV2 Thermal Cycling Test: Evaluation of Mn-doped SAC solder

BGA balling of TV2 samples was realized with an in-house stencil-based paste printing process. To build confidence in the balling process and its applicability towards reliability evaluation, a low-CTE glass package without die assembly was first cycled. Thermal cycling test was conducted following the procedure and failure criteria outlined in section 5.1.1.1, and in the same conditions as previously. Electrical resistances were monitored every 100 thermal cycles. The test sample passed 1500 thermal cycles before failure, exceeding the fatigue life of TV1 low-CTE samples by 300-400 cycles. This can be explained by: 1) higher relative CTE of TV2 on account of greater number of metallizations and increased copper coverage, and 2) better expected fatigue performance of SAC305 as compared to SAC105 solder. This preliminary evaluation, although it was performed on a single sample, is consistent with the results presented in the previous section. BGA balling by paste printing was therefore continued as planned.

All samples in test have passed 1000 thermal cycles to date with stable daisy-chain resistance values. Electrical measurements for corner circuit #1 are plotted in Fig. 5.19. This test is still ongoing and will be pursed until failure.

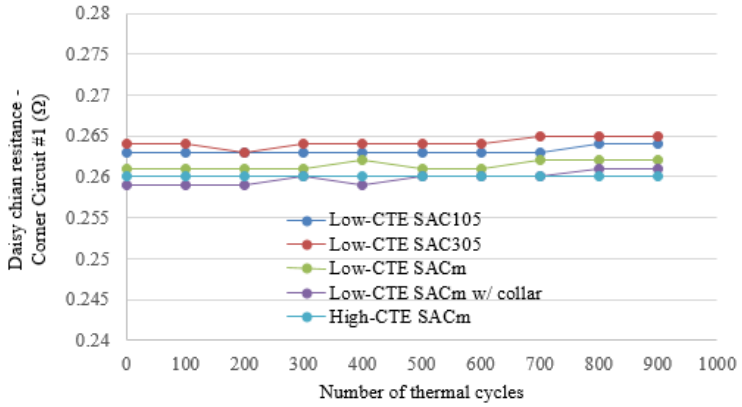


Figure 5.19: Resistance measurements for corner daisy chain #1 in assemblies with 100µm-thick die.

CHAPTER 6

SUMMARY AND CONCLUSIONS

This chapter summarizes the overall research work conducted to enhance board-level reliability of glass BGA package-to-board interconnections with circumferential polymer collars and doped solders. Feasibility of direct SMT assembly of glass packages on board without an intermediate organic package is highlighted. Recommendations for future work pertaining to related board-level reliability research is also briefly discussed.

6.1 Research Summary

In the first part of the study, thermomechanical and drop test reliability were demonstrated with 18.5mm x 18.5mm, 100µm-thick glass BGA packages at 400µm pitch. Circumferential polymer collars were introduced as partial reworkable underfills to reduce local ~~stress~~ strain concentration at critical points in solder joints. Finite-element modeling was used to gain a fundamental understanding of the strain-relief mechanism with polymer collars, and their effectiveness in board-level reliability. In the second part of the study, board-level reliability is further explored with innovations in solder materials, and pad surface finish metallurgies with consideration of system-level reliability.

Research tasks defined to address specific technical challenges are summarized in Table 6.1.

Table 6.1: Technical challenges vs. research tasks.

Technical Challenge	Research Task
Aggravated solder strains	1. Modeling and demonstration of strain relief with polymer collars (TV1)
Balanced thermal cycling and drop test reliability	2. TCT reliability with Mn-doped SACM™ (TV2)
	3. TCT & drop test with SACM with consideration of surface finish (TV3)

6.1.1 Finite-Element Modeling

FEM was used to investigate the effect of circumferential polymer collars on thermomechanical reliability of Si, and low- and high-CTE glass packages. A 2D plane strain approximation model was used to analyze and predict i) the warpage behavior of package assemblies with and without polymer collars, and ii) the fatigue life of SAC105 solder. Polymer collars can be considered as a partial underfill. The stress-free temperature was therefore assigned as the Tg of the collar material in their presence, as a first approximation. A fundamental understanding of the mechanisms by which polymer collars reduce warpage and improve fatigue life was established. Based on modeling results, lowest net warpage was observed on package assemblies with polymer collars on account of an increase in effective CTE of the package. Fatigue life predications using Coffin-Mason and Engelmaier-Wild models indicated a 40-70% improvement in TCT reliability in presence of collars. Collars redistribute solder strains across the solder ball and prevent cracks from initiating and propagating in the two locations of highest strain concentration at the top of the BGA by providing additional compressive stresses. The likeliest failure location is, therefore, shifted to the bottom region, with lower strain levels, and, subsequently, increased fatigue life.

6.1.2 Summary of Task 1 results

TV1 was designed to i) fully demonstrate board-level reliability of 100µm-thick glass BGA packages, 18.5mm x 18.5mm in body size, and ii) investigate the effect of circumferential polymer collars on the reliability performance of solders. Thermal cycling and drop tests were conducted on a representative number of assemblies, followed by detailed failure analysis.

During TCT, all sample configurations qualified a minimum of 1000 thermal cycles with SAC105 solder BGAs. The low-CTE samples without collars recorded first failure at 1100 cycles, and all failed between 1100-1200 cycles. Samples with collars recorded first failure at 1400 cycles and failed between 1400-1600 cycles. Polymer collars were, therefore, demonstrated to provide a ~30% improvement in average TCT performance. Such fatigue life numbers, so close to the required 1000 cycles, indicate minimum scalability of standard solder approaches to larger package sizes or finer SMT pitches with low-CTE glass. However, the high-CTE samples are still in test with stable daisy-chain resistance values till 4600 cycles. Thermal cycling will be continued until failure. High-CTE glass therefore constitutes a promising platform for integration of high-performance systems as it can accommodate high-density interconnections to support split dies, while maintaining outstanding board-level reliability.

Failure analysis of the low-CTE samples without collars by optical and SEM/EDS imaging confirmed crack initiation at the IMC-to-solder interface on the package side and subsequent propagation into the bulk of the solder. However, crack origination was observed to be systematically shifted to the bottom of the solder in presence of collars, with delayed failures resulting in improved TCT performance as predicted by modeling.

Shadow-Moiré warpage characterization, performed on low-CTE samples with and without collars, indicated similar trends as observed in modeling with a reduction in net warpage in presence of collars. In addition, the fatigue life predictions made by Coffin-Manson and Engelmaier-Wild models were within deviations, between 22-26% and 10-15%, respectively, with the experimental results.

During drop testing, all samples passed the JEDEC-based drop test standards, with the corner circuits surviving 40 drops and the inner chains passing 200 drops. However, the samples with polymer collars showed a 2X improvement in performance. Polymer collars locally apply compressive stresses on the redistribution layers, delaying their failures. The fitted Weibull failure distribution indicated a marginal effect of glass CTE, while polymer collars clearly enhanced both TCT and drop test reliabilities. No glass-specific failure mechanisms were observed as the predominant failure mode revealed by optical, SEM/EDS and C-SAM characterizations, cracks in the copper wiring layers, correlated with standard failure mechanisms reported for silicon and laminate packages.

6.1.3 Summary of Task 2 results

TV2 was designed to evaluate the fatigue performance of the novel Mn-doped SACM solder alloy by Indium Corporation, and its use in conjunction with polymer collars to further improve board-level reliability of low-CTE glass BGA packages, with minimum system-level impact. TCT reliability of large, single-chip glass substrates, emulating an application processor package, was investigated with considerations of assembly yield and warpage.

To accurately emulate the system-level response, silicon test dies, 10mm in size and 100-200µm in thickness, were assembled on the glass packages by thermocompression bonding, followed by capillary underfilling. BGA balling with stencil printing was developed and optimized at 400µm pitch to enable evaluation of the SACM alloy, only available in paste form, and its comparison to standard SAC105 and SAC305. Optical, X-ray and SEM/EDS characterizations were performed to optimize the reflow profile to achieve excellent solderability, suitable intermetallic formation and minimal voiding.

Shadow-Moiré warpage measurements were used to characterize and analyze the BGA balling and board-level assembly yields of 86% and 91%, respectively. As expected, more significant warpage was observed on high-CTE glass packages after chip-level assembly, highly conditioned by the underfill fillet size, degrading the BGA balling yield due to bridging of the solder paste. At board-level, low-CTE packages predictably presented greater warpage than high-CTE packages. The application of polymer collars was again found to reduce warpage, with subsequent reliability improvements. The assemblies were then subjected to thermal cycling at -40/125°C, and passed 900 cycles with stable daisy chains to date. This reliability evaluation is still ongoing and will be pursued until failure.

Recommendations for assembly sequence chip last vs. chip first

To address the warpage-related yield loss experienced with high-CTE samples, the assembly sequence may be modified as described in Fig. 6.1, with a chip-last approach. Such assembly sequence, combined with optimized thermocompression bonding profiles, has been proven efficient for warpage mitigation of 30 mm x 40mm of 2.5D silicon interposers in high-performance computing [83].

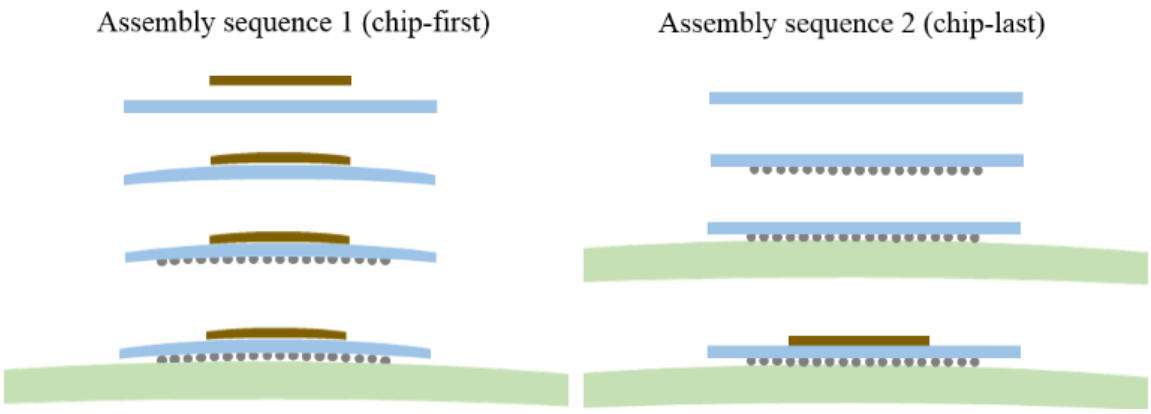


Figure 6.1: Assembly sequence modification from chip first (left) to chip last (right) for high-CTE glass BGA packages.

6.1.4 Summary of Task 3 results and considerations for future work

TV3 was designed and fabricated to comprehensively evaluate the drop and fatigue performances of the SACM solder, with considerations of surface finish metallurgies. The next steps in this research are to print and form the BGA balls, complete board-level assembly and perform reliability characterization. The results from this study aim at providing the best materials and process conditions for balanced thermomechanical and drop test reliability with minimum system-level impact. Suggested future work includes the following:

- Investigating EPAG and ENEPIG as surface finish options on the package side with variations of ENEPIG and OSP on the board side for TCT and drop testing;
- Evaluating SACM solder with SAC305 as reference for TCT, and SAC105 as reference for drop testing;
- Characterizing microstructural and intermetallic evolution under thermal aging (t_0, 250, 500 and 1000 hours) with combinations of pad surface finishes including EPAG, ENEPIG, OSP, and solders including SACM, SAC305 and SAC105.

This research is a critical fundamental building block towards the design and demonstration of 2.5D glass BGA packages at 30mm x 40mm body size. Low-CTE glass substrates were found close to their limit in package size and SMT pitch at 18.5mm size, and are therefore not ideal for this application. Provided chip-level reliability can be maintained, high-CTE glass is a promising solution to achieve direct assembly to the board at such large package size while supporting high interconnect densities, necessary for high-performance logic-to-logic and logic-to-memory communications. Optimization of the

assembly sequence and unit processes for warpage and reliability mitigation will also be instrumental in achieving this grand challenge.

6.2 Conclusions

This research demonstrates the board-level reliability of next-generation 2D, 2.5D and 3D glass interposer and packages that are directly assembled on the board without the need of an intermediate package. Two major innovations, polymer collars and doped SACM solders, are explored to accomplish the research objectives. The samples showed excellent TCT and drop test reliability, confirming the performance enhancements with polymer collars and doped solders. The data also validate model-to-hardware correlations for the material, design and process innovations.

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