THE DESIGN OF SIGE INTEGRATED CIRCUIT COMPONENTS FOR EXTREME ENVIRONMENT SYSTEMS AND SENSORS

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THE DESIGN OF SIGE INTEGRATED CIRCUIT COMPONENTS FOR EXTREME ENVIRONMENT SYSTEMS AND SENSORS

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SUMMARY

The objective of this research is to understand how the performance of state-of-the-art silicon-germanium (SiGe) BiCMOS processes may be leveraged in the implementation of electronic systems for extreme environment applications and sensors.

This work begins by providing a background investigation of the total-dose radiation tolerance of a third generation complementary SiGe:C BiCMOS technology platform. Tolerance is quantified under proton and X-ray radiation sources for both the *npn* and *pnp* HBT, as well as for an operational amplifier built with these devices. Furthermore, a technique known as junction isolation radiation hardening is proposed and tested with the goal of improving the SEE sensitivity of the *npn* by reducing the charge collected by the subcollector in the event of a direct ion strike. To the author's knowledge, this work presents the first design and measurement results for this form of RHBD.

The proceeding chapters detail the design of three independent systems, including: 1) a charge amplification channel developed as part of a remote electronics unit for the lunar environment, 2) variable bias circuitry for a self-healing radar receiver, and 3) an ultra-fast x-ray detector for picosecond scale time-domain measurements of evolving chemical reactions. The first two projects capitalize on the wide-temperature performance and radiation tolerance of the SiGe HBT, allowing them to operate under extreme environmental conditions reliably and consistently. The third design makes use of the high-frequency capabilities of the HBT, particularly in current-mode logic (CML) configurations. These studies will help to improve understanding of the design practices and constraints necessary for cutting-edge electronics system design using SiGe BiCMOS platforms.

A significant amount of this work has been published or submitted for publication at various refereed conferences and journals, including IEEE Transactions on Nuclear Science [4, 14], IEEE Aerospace Conference [13], and IEEE Aerospace and Electronic Systems Magazine [15]. More specifically, details of this dissertation can be found in the following refereed publications:

1. The Effects of X-Ray and Proton Irradiation on a 200 GHz/90 GHz Complementary (*npn* + *pnp*) SiGe:C HBT Technology (Chapter 2, also published in [4])
2. Junction Isolation Single Event Radiation Hardening of a 200 GHz SiGe:C HBT Technology Without Deep Trench Isolation (Chapter 3, also published in [14])
3. A Monolithic, Wide-Temperature, Charge Amplification Channel for Extreme Environments (Chapter 4, also published in [13])
4. A New Approach to Designing Electronic Systems for Operation in Extreme Environments: Part I - the SiGe Remote Sensor Interface (Chapter 4, also published in [15])

CHAPTER I

INTRODUCTION

1.1 Motivation

Silicon-germanium (SiGe) BiCMOS technology continues to receive significant interest as a candidate for extreme environment electronics applications, and is particularly well-suited for operation in the cryogenic temperature and radiation-rich conditions typically found in space exploration. Cost considerations force customers in this niche market to look to technologies with a high potential for integration while placing very stringent constraints on their ability to operate reliably for long periods of time under harsh conditions. Within such constraints SiGe has been demonstrated to excel [1]. The fabrication steps required to build a self-aligned SiGe HBT are compatible with the low-cost CMOS processes that have historically dominated the market, allowing analog and RF systems to be easily integrated with the digital electronics required to control them. In addition, the SiGe HBT has been shown to be extremely resilient to total dose effects induced by the ionizing radiation that permeates the space environment [2-4].

1.1.1 Single Event Effects Hardening

Despite their numerous advantages, commercially-available, bulk SiGe HBTs are especially prone to single event effects (SEE). These arise when a high-energy ion collides with the silicon near the device. Electron-hole pairs are produced in great numbers along the track of the ion through the substrate, which, when collected by the device, can produce voltage transients substantial enough to corrupt data. Previous

studies have shown unhardened SiGe Gb/s digital logic to have high saturated cross sections and low upset thresholds by virtue of the charge collection dynamics within the lightly-doped substrate [5]. In many high-performance SiGe technology platforms some degree of substrate isolation is achieved through the use of 8 μm deep trench isolation (DTI) which surrounds the subcollector. While the DTI does serve to insulate the subcollector from ion deposited charge outside of the DTI boundaries, it also confines those same charges when an ion strikes the device within the DTI boundary.

One particularly simple form of device-level radiation hardening by design (RHBD) intended to improve this effect consists of an n-type implant surrounding the DTI. By applying a positive DC bias to the "n-ring" external to the DTI, it can effectively shunt charge away from the sensitive collector node for outside DTI strikes [6]. The main limitation of this RHBD technique has proven to be the DTI itself, however, due to the fact that an emitter-center strike (worst case for SEU) leaves the majority of free electrons in a location where the n-ring cannot collect them. The present work investigates the effects of using a new junction isolation hardening scheme on the charge collection dynamics of a third-generation, high-performance SiGe BiCMOS technology that does not employ deep trench isolation.

1.1.2 Extreme Environment Electronics

The design methodologies used to build electronic systems for space have historically changed very little mission-to-mission, for good reason. When venturing beyond the atmosphere, such value is placed on first-pass mission success that efficiency and performance must by necessity be considered secondary priorities to simplicity and reliability. Within this engineering trade-space, it is no small feat for a new design

approach to scale the barriers to entry and claim position amidst the tried and true "flight qualified" space technologies. As technological capabilities continue to advance and ambitions expand, however, the advantages associated with adopting new and innovative approaches become increasingly difficult to ignore. This trend is readily apparent when considering recent developments in the area of cold-capable integrated circuit (IC) technologies.

Currently, the extreme temperature and radiation conditions endured by NASA exploration missions are circumvented by the use of centralized system architectures installed within protective "warm electronic boxes" (WEBs) (Figure 1). While WEBs are capable of effectively mitigating the temperature problem, they do so at substantial cost.

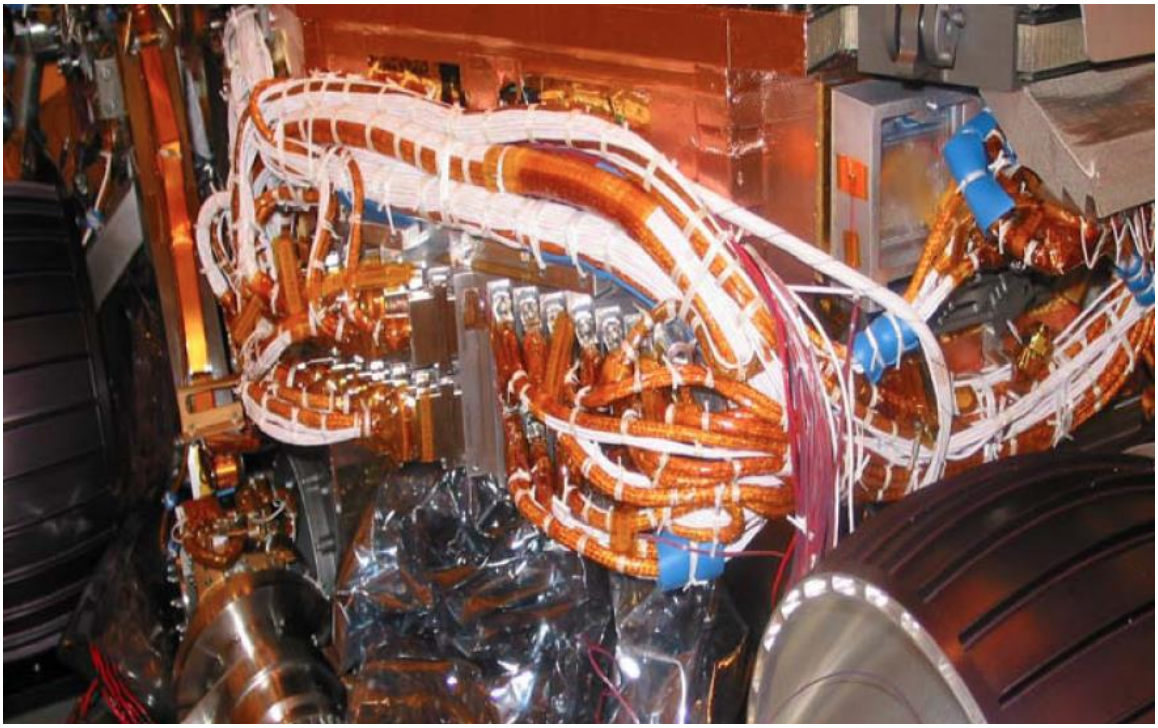

Figure 1: Cabling for the Centralized System Architecture of the Mars Exploration Rover (MER).

Excessive point-to-point wiring, increased system weight and complexity, elevated power budgets, lack of modularity, and perhaps most importantly an overall reduction in system reliability are all results of this well-entrenched design paradigm. The engineer's ability to create a truly distributed, modular electronics system within such architectures is limited at best, raising the question: would the advantages of a departure from this design strategy, specifically by directly attacking the issues faced by operating electronics in wide-temperature and/or radiation environments, outweigh the associated costs?

To determine the answer to this question, the "SiGe Integrated Electronics for Extreme Environments" project (SiGe EEE) was funded under the NASA Exploration Technology Development Program (ETDP). Its task was to develop electronic systems in state-of-the-art SiGe platforms to meet the challenges posed by complex initiatives such as planetary colonization. The Remote Health Node (RHN), originally designed at BAE Systems for the envisioned X-33 space plane, was chosen as a starting point in order to demonstrate the numerous advantages that can be potentially leveraged. The original RHN design sought modularity by combining multiple types of sensor interfaces into a single hardware implementation that was usable throughout a spacecraft or exploration vehicle to provide mission critical environmental and health data to engineers in an efficient, reliable manner .

Advancing this concept one step further, the SiGe EEE has sought to develop a fully integrated version of the RHN that not only reduces its form-factor and power draw dramatically, but also completely eliminates the need for isolation from the environment by dispensing with the WEB. The SiGe Remote Electronics Unit (REU) is intended to be housed within a single connector or multi-chip package and utilized throughout the space

vehicle in quantity, as required by the modern sensor systems used in such vehicles [7].

1.1.3 Self-Healing Electronics

An emerging area of research that shares many common themes with those in extreme environment applications is "self-healing" electronics. The idea that with the proper diagnostic circuits and feedback networks, an electronic system could determine its current state and make adjustments to maintain itself within specification is not new [8, 9]; SiGe, however, presents a unique opportunity to monolithically merge the RF, analog, and digital components of such a system into a low-cost system-on-chip (SoC). This capability can be applied for a wide-range of purposes, including the improvement of manufacturing yield, the widening of operating temperature ranges, and the prevention of system failure caused by rising levels of ionizing radiation damage.

Self-Healing Mixed-Signal Integrated Circuits (HEALICs) is a program under the Defense Advanced Research Projects Agency (DARPA) aimed at the development of techniques to maximize the number of fully operational mixed-signal SoCs on an individual wafer that meet all performance goals in the presence of extreme process variations and environmental conditions. Under this program, and in close collaboration with Northrop Grumman, the SiGe team at Georgia Tech is developing an 8-18 GHz radar transceiver utilizing techniques specifically for this purpose.

1.1.4 Ultra-Fast X-Ray Detection

One of the driving forces behind the success of SiGe technologies has been the performance of the HBT itself. Third generation platforms with cutoff frequencies in excess of 200 GHz have enabled SiGe to push the limits of RF performance while

maintaining its high capacity for integration and subsequent low cost. Digital gate delays in one of these platforms have been measured as low as 3.9 ps [10]. For this reason, SiGe technology represents the state-of-the-art in silicon-based ultrafast circuits, and thus is particularly relevant to fast electronics for x-ray detector applications in which the measurement resolution is ultimately determined by the combination of the speeds of the stimulating source and the detecting electronics.

Because x-rays scatter off of the electrons inside molecules, they have been used for years to experimentally map the time-domain response of excited chemical samples and their reactions [11]. The current state-of-the-art can achieve resolutions on the order of picoseconds. There are two paths towards fast time resolution: ultra-fast pulsed x-ray sources combined with comparatively slow detectors, or longer pulses of x-rays combined with ultra-fast detectors. There is a broad overlap in the science that can be obtained between the two approaches. SiGe presents an excellent opportunity to explore just how fast these detectors can be engineered to perform for this purpose.

1.2 Purpose of Research

The SiGe HBT is widely regarded as a proven component in cold-capable electronics [12], however when considering the needs of space-based applications, complexities arise that cannot be handled by bipolar devices alone. The power advantages of CMOS can rarely be ignored, and as such these systems must be built upon a foundation of careful design technique, accurate modeling, and thorough simulation. Particularly important to these applications is the robustness of the biasing schemes and adherence to layout techniques designed to eliminate the possibility of catastrophic system failures. Secondarily, the heavy dependence of space exploration missions on sensor electronics

necessitate that these systems remain accurate and reliable within a vast range of environmental conditions. Development of these cold-capable, integrated systems is an area of research that has yet to be fully explored to date.

Additional focus for this research is aimed at leveraging other advantages of SiGe BiCMOS technologies to push the limits of the current state-of-the-art. The level of integration attainable by the inclusion of a high-speed bipolar device within a CMOS platform allows for very unique mixed-signal systems to be designed monolithically. Third-generation SiGe technologies exhibit HBT cutoff frequencies in excess of 200 GHz, enabling the implementation of cutting-edge RF systems and bipolar digital logic with gate delays as low as 6.5 ps. This research will aim to improve understanding of how these capabilities can be leveraged to create fully-integrated systems that exceed the current capabilities of experimental systems, particularly x-ray detectors, in ways that will enable new discoveries to be made at time-domain resolutions that have yet to be achieved to date.

1.3 Objectives and Contribution of this Work

This thesis contributes to the understanding of radiation effects in the SiGe HBT and the methods of design and optimization for extreme environment sensor systems, self-healing RF systems, and high-speed detectors. These designs consist of: (1) a monolithic charge amplification channel for use in extreme environment applications [13], (2) wide-temperature, digital-analog biasing circuitry for use as the main method of control for an IC self-healing process, and (3) an ultra-fast x-ray detector designed to achieve time resolutions of 10 ps or smaller.

Silicon-germanium (SiGe) BiCMOS technology platforms have proven invaluable for

implementing a wide variety of digital, RF, and mixed-signal applications in extreme environments such as space, where maintaining high levels of performance in the presence of low temperatures and background radiation is paramount. Chapter 2 of this work focuses on the investigation of the total-dose radiation tolerance of a third generation complementary SiGe:C BiCMOS technology platform. Tolerance is quantified under proton and X-ray radiation sources for both the *npn* and *pnp* HBT, as well as for an operational amplifier built with these devices. In Chapter 3, a technique known as junction isolation radiation hardening is proposed and tested with the goal of improving the SEE sensitivity of the *npn* in this platform by reducing the charge collected by the subcollector in the event of a direct ion strike.

The research documented in Chapter 4 presents the design of a monolithic charge amplification channel for use as a piezoelectric sensor front-end in extreme environments such as the lunar surface and Mars. My role in this research supported the conception, design, measurement, and final integration of the charge amplifier into a 16-channel remote sensing interface.

Chapter 5 of this thesis details the development of a self-healing 8-18 GHz radar system. Specifically, the construction of wide-temperature digital-analog biasing circuits and amplifiers to provide stable references for the RF chain are presented. These circuits are individually characterized, and subsequently integrated to show a fully functional receiver that is capable of self-healing for both yield and a wide range of environments and conditions.

The final research, presented in Chapter 6, describes the design of an ultra-fast x-ray detector leveraging the high frequency capabilities of the SiGe HBT in particle physics

research. My responsibilities covered the conception and design of the entire system based on requirements defined by the capabilities of the particle accelerator at Argonne National Labs. This systems main specification is to achieve sub-10 ps time resolution without the need for expensive modifications to the beam line. To conclude, Chapter 7 summarizes the results of this work, as well as presents possible extension of this research for future follow-on work.

CHAPTER II

TOTAL DOSE CHARACTERIZATION

2.1 SiGe BiCMOS Technology Overview

The complementary SiGe:C HBT technology (Figure 2) under investigation was developed by IHP, and integrates isolated *pnp* SiGe HBTs with f_T / f_{max} values of 90 GHz / 125 GHz into a core 0.25 μm 200 GHz / 200 GHz *npn* SiGe BiCMOS platform [16]. The performance of the carbon-doped *npn* SiGe HBTs, which are built using a novel collector design without deep trench isolation, is not significantly affected by the additional *pnp* fabrication steps. Furthermore, the performance of the *pnp* SiGe HBTs is enhanced by reducing phosphorous diffusion via carbon doping, as is commonly practiced in *npn* SiGe HBTs.

The uniquely designed subcollector of the *npn* SiGe HBT is fully contained within the sidewalls of the STI, thereby reducing the collector-substrate junction area and eliminating deep trench isolation entirely, reducing cost dramatically [17]. The low complexity, 10-mask process also takes advantage of the use of a single active area without isolation between the active emitter and collector contact regions, thereby lowering collector resistance and decreasing capacitive coupling to the substrate [16].

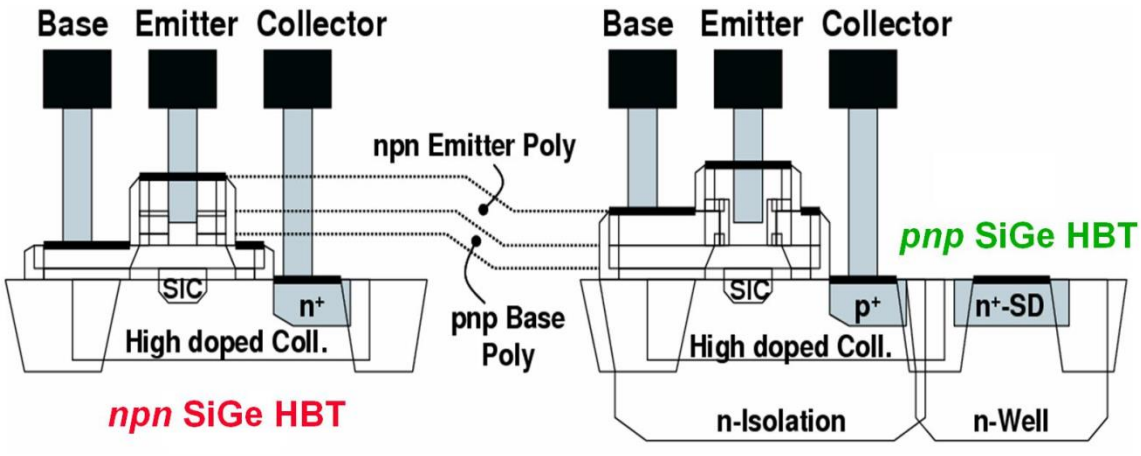

Figure 2: Cross sectional diagram of the 3rd generation 200 GHz / 90 GHz *npn* and *pnp* structure.

2.2 Test Conditions and Facilities

X-ray irradiation was performed at Vanderbilt University using an ARACOR model 4100 10-keV X-ray source, at a dose rate of 0.54 krad(SiO_2)/s. In addition, 63-MeV proton irradiation was performed at the Crocker Nuclear Laboratory, University of California at Davis, at a dose rate of 1.05 krad(SiO_2)/s. The proton dosimetry measurements, which are accurate to about 10%, used a 5-foil secondary emission monitor calibrated against a Faraday cup. The radiation source exhibited beam spatial uniformity of roughly 15% over a 2.0 cm radius circular area [18]. The data presented here were collected over a six month period including two separate experiments on multiple samples at each facility.

In both cases the SiGe HBTs were wire-bonded into 28-pin DIP packages for biasing purposes and were measured at room temperature in incremental dose steps. Both grounded and forward-active ($I_C \approx 1$ mA, $V_{CB} = 0$ V) bias conditions were used during irradiation on devices with varying emitter geometry. The forward-active bias condition was tested to more closely emulate the effects of total dose radiation on an operating circuit in space. AC devices were subject to X-ray exposure under a passive bias

condition (floating), with S-parameter measurements taken before exposure and after returning from the facility at Vanderbilt.

2.3 Current Feedback Operational Amplifier

A current-feedback operational amplifier utilizing only *npn* and *pnp* SiGe HBTs in the investigated technology is shown in Figure 3, with various figures-of-merit under normal operation summarized in Table 1. This type of amplifier offers a high slew rate while its design conveniently decouples gain from bandwidth [19]. The diode-connected SiGe HBTs followed by the emitter-follower stage act as a voltage buffer between the non-inverting and inverting inputs. Wilson current mirrors are used to convert the input current differential into a high-impedance voltage output and a push-pull voltage buffer enables the amplifier to drive low-impedance loads [20, 21].

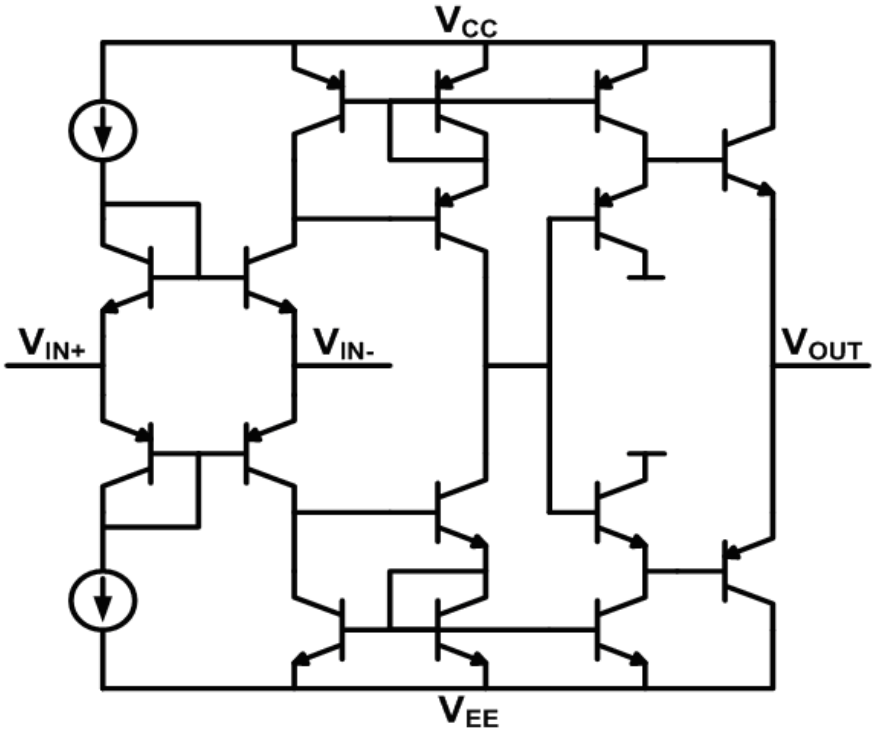

Figure 3: Schematic of the current feedback operational amplifier utilizing only *npn* and *pnp* HBTs.

Table 1: Current Feedback Operational Amplifier Characteristics

Power Supply	+/- 2.5 V
Designed Bias Current	1 mA
Quiescent Power	54 mW
Transresistance	20.6 kΩ
Unity Gain Bandwidth	200 MHz
Positive Slew Rate (C_L = 51 pF)	+ 414 V/μs
Negative Slew Rate (C_L = 51 pF)	- 327 V/μs

The amplifier was irradiated with all terminals grounded to a total X-ray dose of 1.8 Mrad(SiO_2). For measurement and biasing purposes, the circuit was mounted and wire-bonded on a custom-made printed circuit board containing resistive feedback networks, supply decoupling capacitors, and SMA launchers for the input and output signals. Measurements were made both before and after irradiation at three distinct bias conditions, including: unity gain with a 1.0 mA input tail current, finite gain with a 100 μA tail current, and finite gain with a 10 μA tail current.

2.4 Total Dose Radiation Results

Figures 4 and 5 depict the forward and inverse mode Gummel characteristics for both *npn* and *pnp* (A_E=0.42x0.84 μm^2) devices with increasing X-ray and proton dose, respectively. The bias condition during exposure had little impact on total incurred damage, and as such these and all subsequent results are shown for the forward-active case only. The characteristic increase in base current density with increasing ionizing radiation dose has been previously documented and is caused by the production of generation-recombination (G/R) centers near the emitter-base (EB) spacer [22]. Also previously documented in a different, lower-performance C-SiGe technology is the noticeable discrepancy between the excess base current of the irradiated *npn* and *pnp*

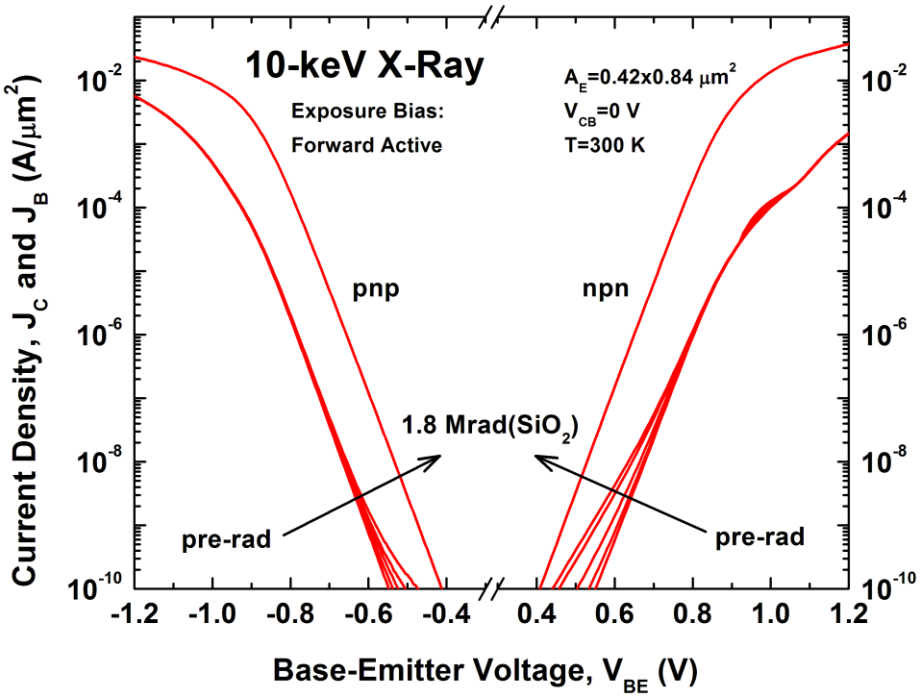

Figure 4: Forward mode *npn* and *pnp* Gummel characteristics from forward-active 10-keV X-ray exposure up to 1.8 Mrad(SiO_2), at a dose rate of 0.54 krad(SiO_2)/s.

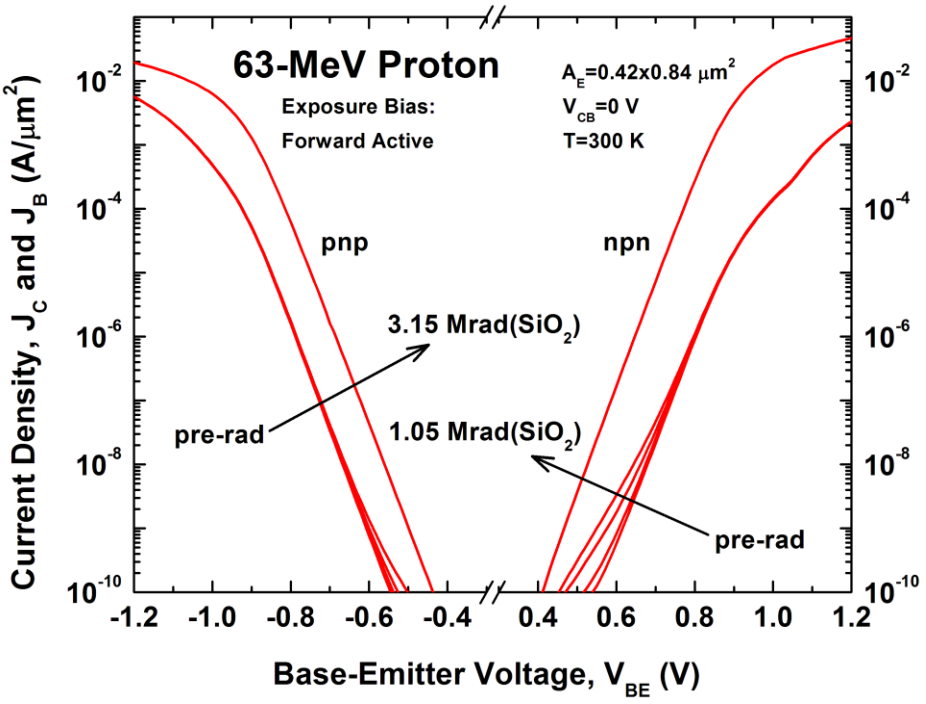

Figure 5: Forward mode *npn* and *pnp* Gummel characteristics from forward-active 63-MeV proton exposure up to 1.05 Mrad(SiO_2) and 3.15 Mrad(SiO_2), at a dose rate of 1.05 krad(SiO_2)/s.

SiGe HBTs at fixed total dose [4, 23].

The change in base current density across total dose at a fixed V_{BE} of 0.6 V can be seen in Figures 6-8, with Figure 6 and Figure 7 comparing the radiation response of the technology being investigated with previously reported results from a similar 200 GHz *npn*-only technology under X-ray and proton irradiation conditions, respectively [24]. For a device operating in inverse mode, the shallow trench isolation (STI) separating the base from the extrinsic collector is the primary region where damage will induce excess base current [22]. The forward and inverse mode excess base currents for the *npn* devices are comparable, indicating similar contributions from the G/R centers at the EB spacer and STI interfaces. Inverse mode data for the *pnp* devices, however, contained high levels of base current at low bias prior to irradiation and are not presented here. The technology

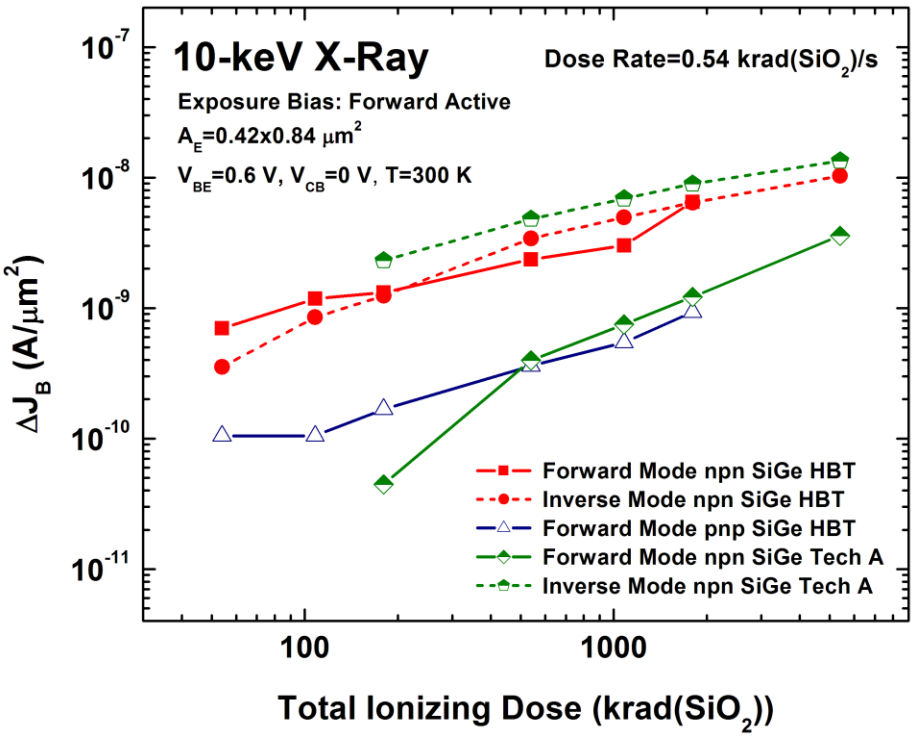

Figure 6: Excess base current, ΔJ_B, plotted as a function of 10-keV X-ray dose for both complementary structures and a comparable *npn*-only 200 GHz technology.

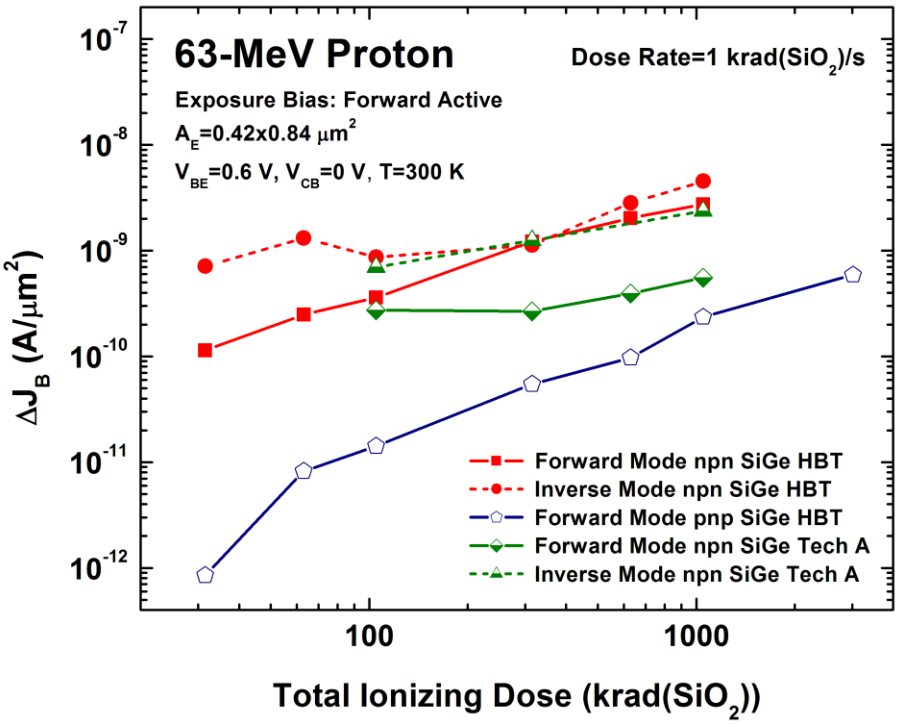

Figure 7: Excess base current, ΔJ_B, plotted as a function of 63-MeV proton dose for both complementary structures and a comparable *npn*-only 200 GHz technology.

under investigation showed slightly more radiation-induced base current from both radiation sources compared with the *npn*-only technology, particularly in forward mode, though neither exhibited substantial damage [4].

Figure 8 offers a direct comparison between X-ray and proton radiation responses for the npn and pnp HBTs. It can be seen that protons produced nearly a decade less excess base current at low dose, with the responses converging as dose increased. Normalized current gain curves are plotted in Figures 9 and 10, illustrating the effects of total dose exposure in a more circuit-relevant context. The gain degradation for the npn devices becomes non-negligible only at current densities more than two decades above that of the pnp, which remains nearly unaffected by ionizing radiation above current densities of 1.0 μA/μm2 [4].

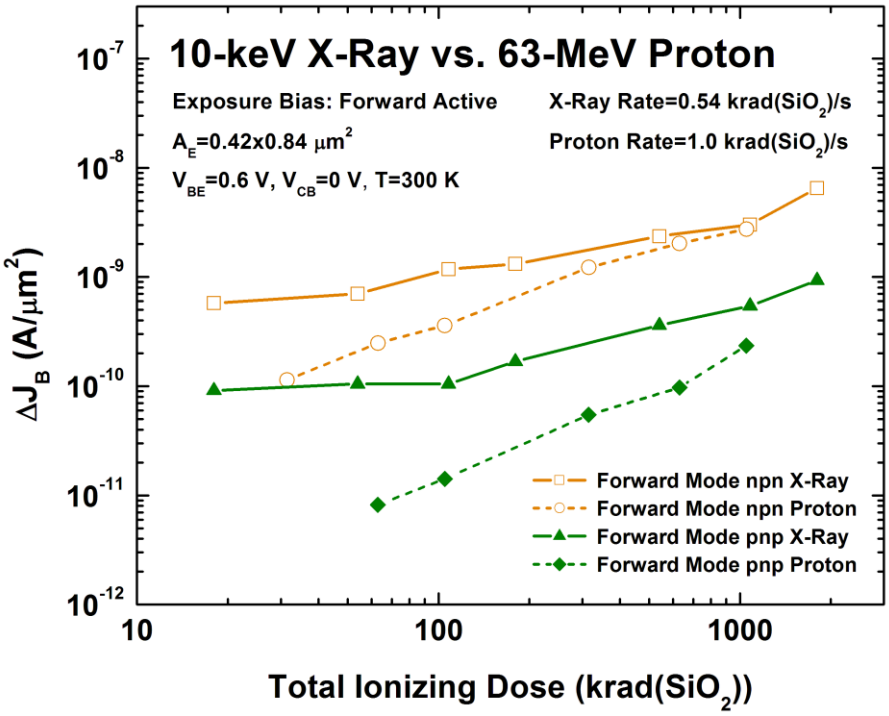

Figure 8: Excess base current, ΔJ_B, plotted as a function of 10-keV X-ray and 63-Mev proton dose for both *npn* and *pnp* structures.

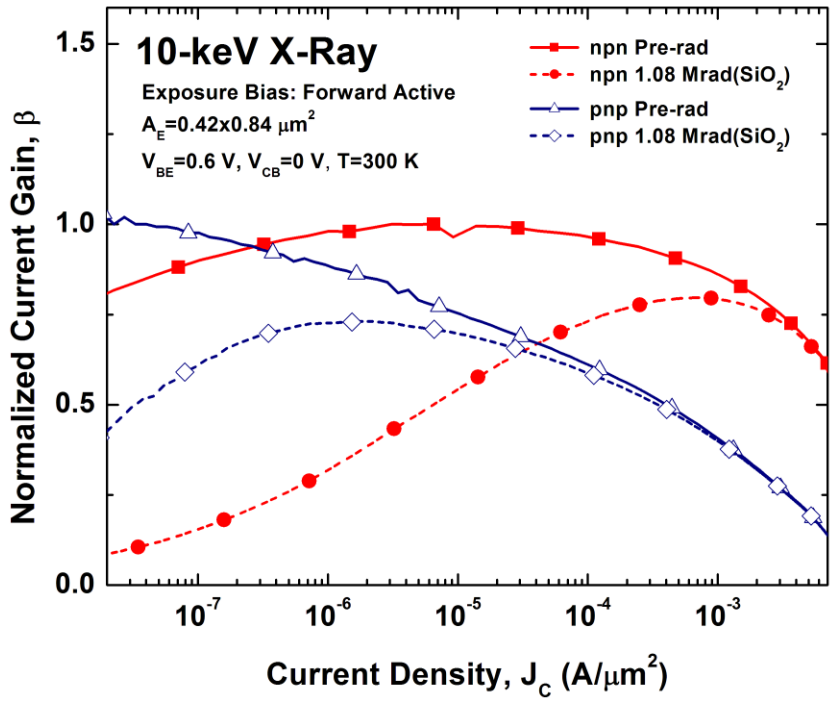

Figure 9: Normalized gain plotted against collector current density for *npn* and *pnp* HBTs before and after 10-keV X-ray exposure at a dose rate of 0.54 krad(SiO_2)/s.

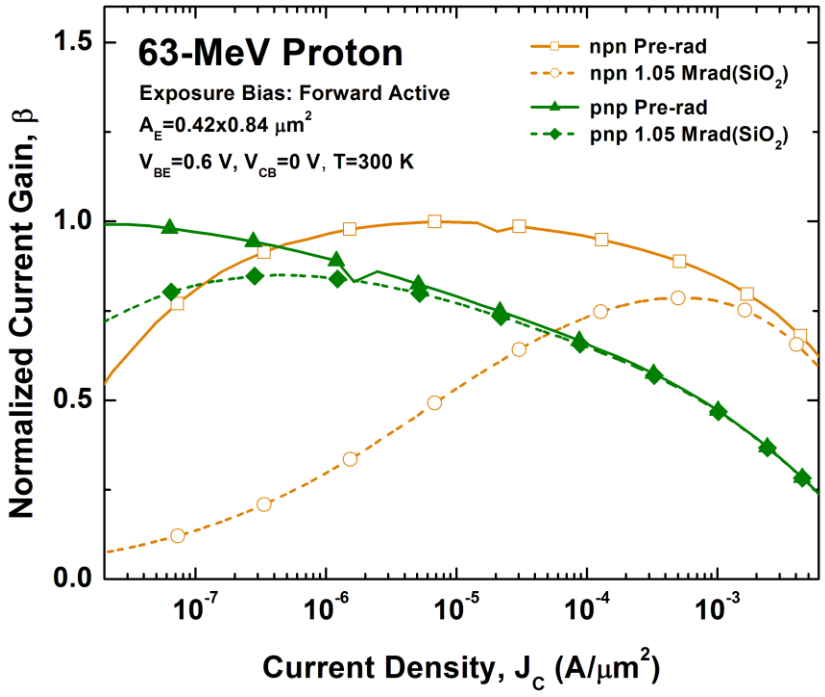

Figure 10: Normalized gain plotted against collector current density for *npn* and *pnp* HBTs before and after proton 63-MeV proton exposure at a dose rate of 1.05 krad(SiO_2)/s.

AC characterization was performed pre- and post-radiation on custom-designed structures under X-ray total dose exposures up to 1.8 Mrad(SiO_2). The data shown in Figures 11 and 12 are for emitter geometries of 0.63x0.84 μm^2 on all devices except the forward mode *pnp* data, which were obtained from a device with an emitter geometry of 1.26x0.84 μm^2. AC response was similar for all device sizes, showing only slight deviations across total dose that are well within the bounds of measurement error. The collector-base junction bias was held at 0 V for all measurements and the reported data have been normalized to peak f_T for the *npn* devices [4].

Pre- and post-irradiation measurements were made on the current feedback operational amplifier in a unity gain configuration with 1.0 mA bias current. The amplifier showed no degradation in performance metrics up to a dose of 1.8 Mrad(SiO_2). In order to

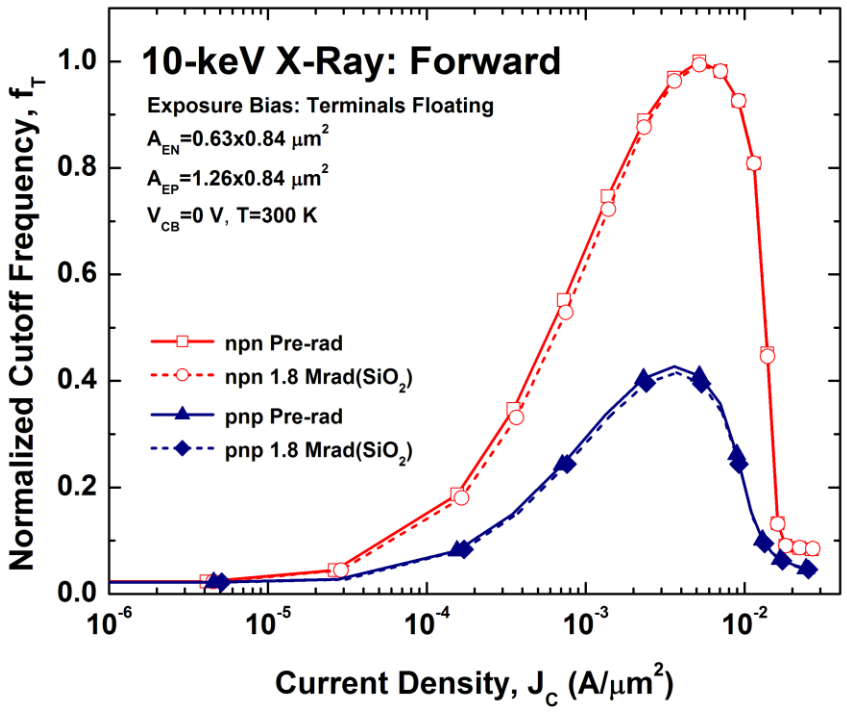

Figure 11: Forward mode unity gain cutoff frequency plotted against collector current density for *npn* and *pnp* SiGe HBTs before and after X-ray exposure.

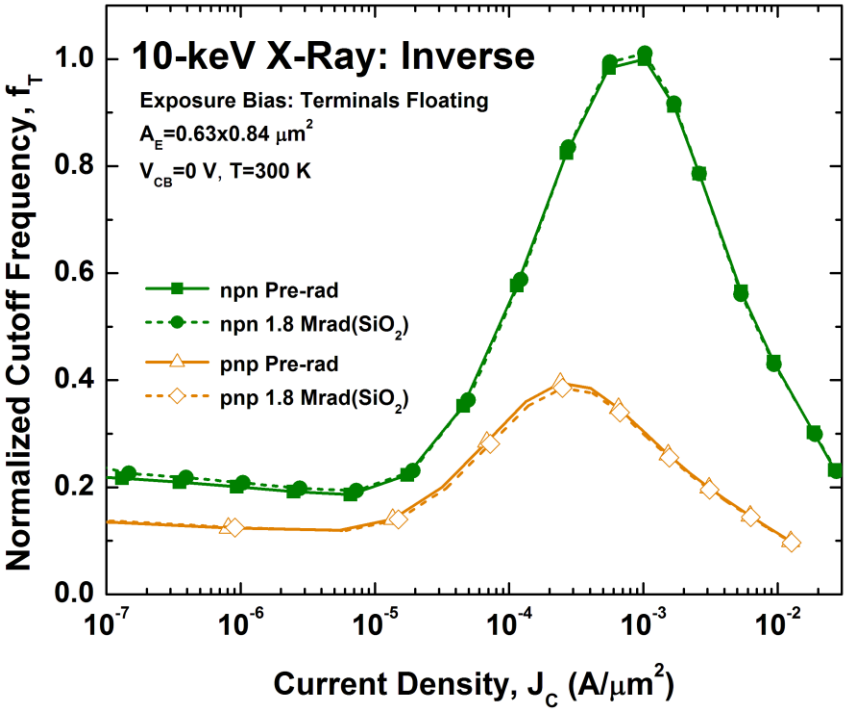

Figure 12: Inverse mode unity gain cutoff frequency plotted against collector current density for *npn* and *pnp* SiGe HBTs before and after x-ray exposure.

probe the effects of the radiation damage at lower current densities, a second experiment was performed. This time the amplifier was configured in a finite gain mode (roughly 30 dB) with tail currents of 100 µA and 10 µA, and was again irradiated to a total dose of 1.8 Mrad(SiO_2). Figure 13 shows the pre- and post-radiation gain curves for both bias conditions. It is readily apparent that despite being biased in a manner that would induce noticeable *npn* gain reduction (25% at $J_C \approx 60$ µA/µm^2) in the individual active devices, the amplifier suffers no ill effects as a result of radiation exposure. The f_{-3dB} remains constant at 400 Hz and 5 kHz for bias currents of 10 µA and100 µA, respectively, with no low frequency gain degradation in either case [4].

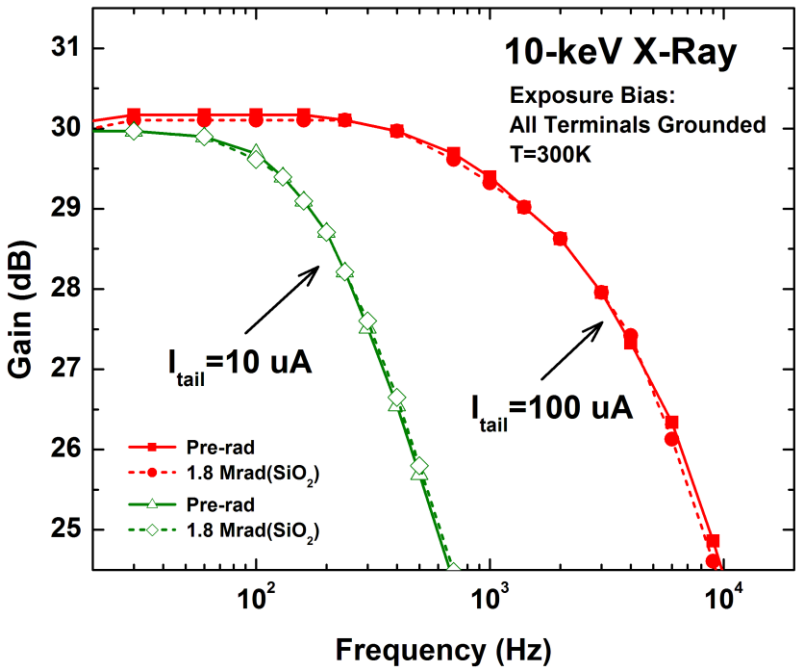

Figure 13: Gain plotted against frequency before and after X-ray irradiation for two low current density bias conditions. Collector current densities are 570 µA/µm^2 and 57 µA/µm^2, respectively.

2.5 TID Discussion

The results of the comparison between *npn* and *pnp* devices indicate that the *pnp* SiGe HBTs tend to suffer less damage than their *npn* counterparts, all else being equal. As reported in [25], this can be attributed to the fact that the introduction of radiation-induced positive oxide charge in a *pnp* transistor will accumulate the n-type base region close to the EB spacer, and because recombination occurs more readily when the electron and hole densities are approximately equal, effectively reduce the rate of recombination at that location. This is in contrast to the p-type base region of an *npn* device, which tends to deplete in the presence of positive oxide charge. Assuming a similar contribution to excess base current due to traps at the Si-SiO_2 interface of the EB spacer, this difference could potentially account for the higher total dose tolerance of *pnp* SiGe HBTs [4].

In the circuit context investigated, the amplifier's closed-loop gain and bandwidth are maintained despite reduction in gain for the active devices at low bias currents. This can be at least partially explained by specific characteristics of the circuit topology itself. The gain stage of the current-feedback amplifier consists of two Wilson current mirrors, which together mirror the currents through the inverting input node, pushing them into a high-impedance output and providing voltage gain. A simplified Wilson current mirror is shown schematically in Figure 14. Typical bipolar cascode current mirrors, while providing high output impedance, suffer from the effects of systematic gain error stemming from the finite β_F of the bipolar transistor [4, 26].

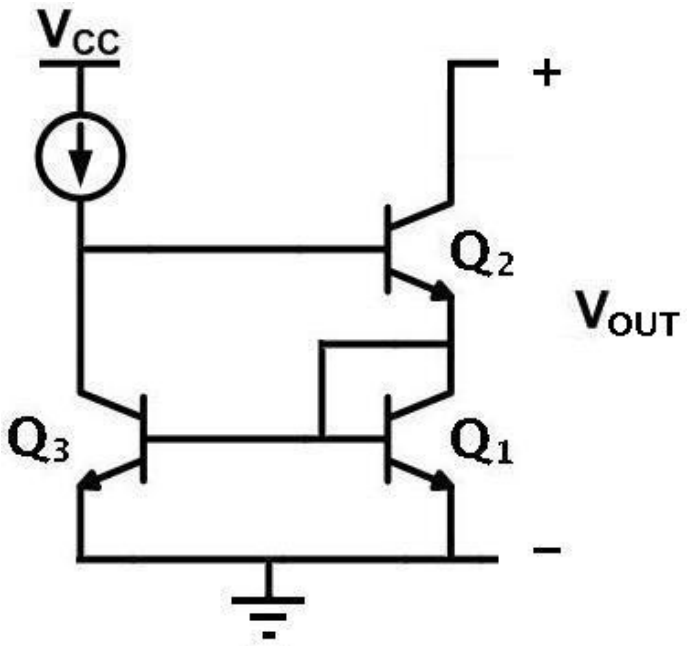

Figure 14: Simplified schematic of the *npn* Wilson current mirror.

When $\beta_F >> 1$,

$$\varepsilon_{cascode} = -\frac{4}{\beta_F + 4} \tag{1}$$

Changes in β_F, as are induced by radiation damage for instance, will directly alter the gain error of such stages. The Wilson current mirror mitigates this drawback by providing a feedback path. The current that enters the base of Q_2 produces an emitter current equal to $I_{B2}(\beta_F + 1)$. This current is then mirrored back to Q_3 through Q_1, maintaining I_{C2} such that it is nearly equal to the input current, resulting in less dependence on any changes in β_F. The systematic gain error of the Wilson current mirror due to finite current gain is calculated as [4, 26],

$$\varepsilon_{Wilson} = -\frac{2}{\beta_F^2 + 2\beta_F + 2} \tag{2}$$

The gain of the Wilson current mirror also depends on its output impedance, which is directly proportional to β_0 and is calculated approximately as:

$$R_o \approx \frac{\beta_0 r_{o2}}{2} \tag{3}$$

For the current-feedback amplifier, however, the output impedance of the gain stage is in fact the parallel combination of an *npn* and a *pnp* Wilson current mirror. Assuming that r_o and β_0 are both smaller for the *pnp* (whose β_0 does not change significantly at such bias conditions due to irradiation), the output impedance, and therefore the gain, will remain relatively constant for any changes induced in $\beta_{0,npn}$. These trends are consistent with the measured post-irradiation data. A die photo of the current feedback operational amplifier is shown in Figure 15 [4].

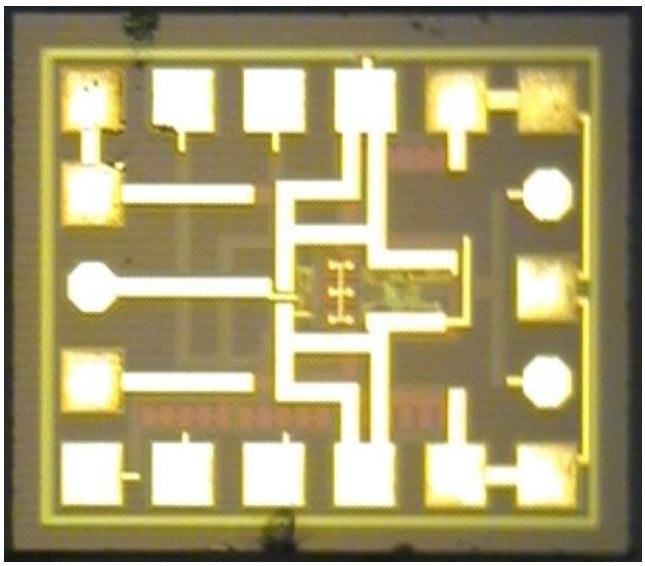

Figure 15: Die photo of the current-feedback operational amplifier.

CHAPTER III

SINGLE EVENT HARDENING

3.1 Junction Isolated Design

The implementation of junction isolation in the IHP design kit required very few violations of standard design rules. The standard HBT cell already included a p-well substrate contact ring surrounding the STI of the device. All that was necessary was to add a diode junction surrounding that p-well. The design layer chosen was an n-type implant that extends deeper than the subcollector implant used in the HBTs structure. Multiple variants were constructed to determine how aggressively spaced the ring could be from the intrinsic device before electrical malfunctions such as punch-through were detected.

Figures 16 and 17 show schematic cross-sections for the unhardened and junction isolation hardened SiGe HBTs, respectively. For reference, each include dotted lines indicating where DTI would normally be present in a comparable 3rd generation technology. The junction-isolated structures shown in Figure 17 were comprised of three variants, with junction widths ranging from 2.2 μm to 2.9 μm. Figure 18 shows top-down schematic views of the unhardened and junction isolation hardened HBTs. Implementing the junction isolation increases the area of the HBT from roughly 54 μm^2 to 155 μm^2 [14].

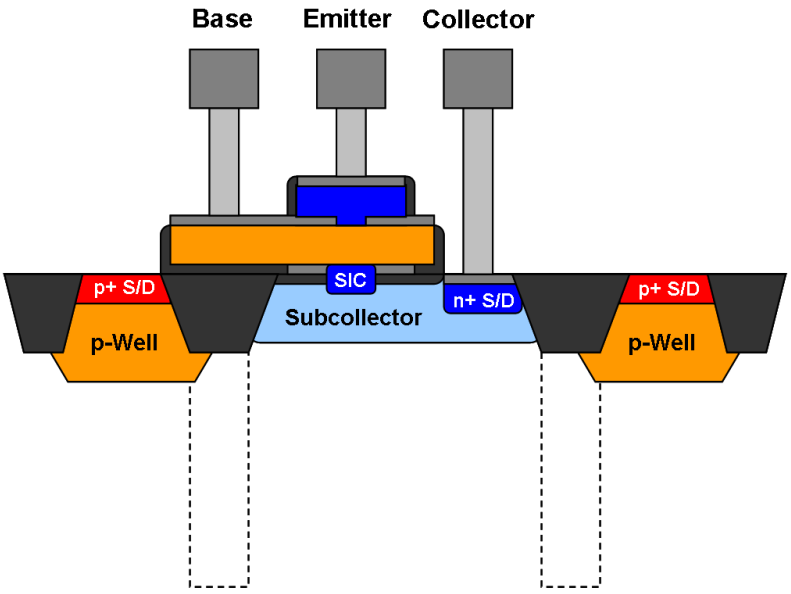

Figure 16: Schematic cross-section of the basic *npn* SiGe HBT. The location of typical deep trench isolation in comparable SiGe technologies is represented by the dotted lines.

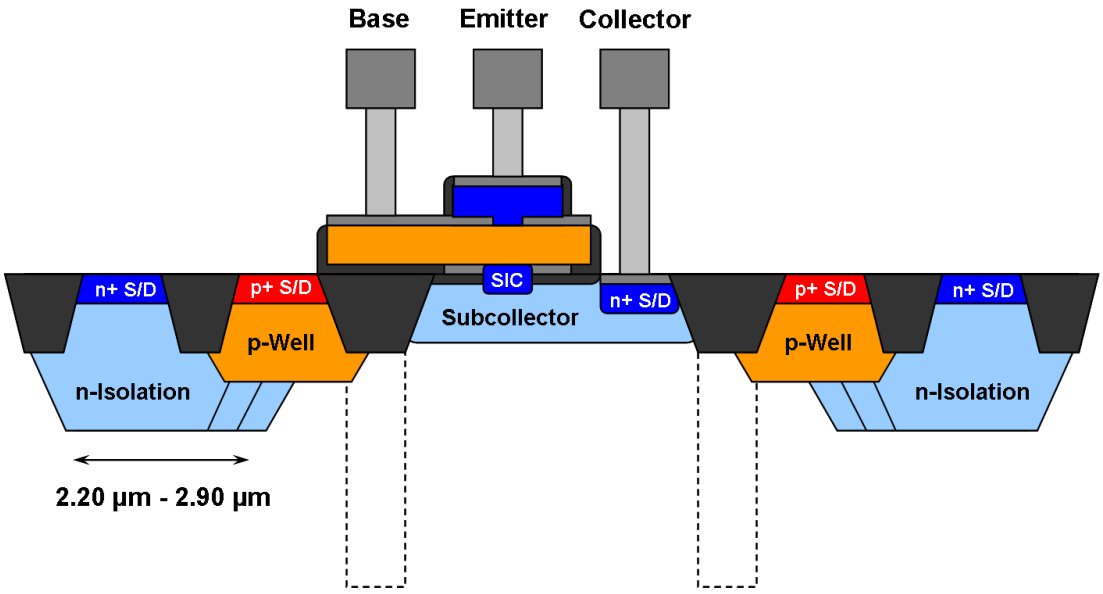

Figure 17: Schematic cross-section of the hardened *npn* SiGe HBT structure showing junction-isolation RHBD variants from 2.2 µm to 2.9 µm wide. The location of typical deep-trench isolation in comparable SiGe technologies is represented by the dotted lines.

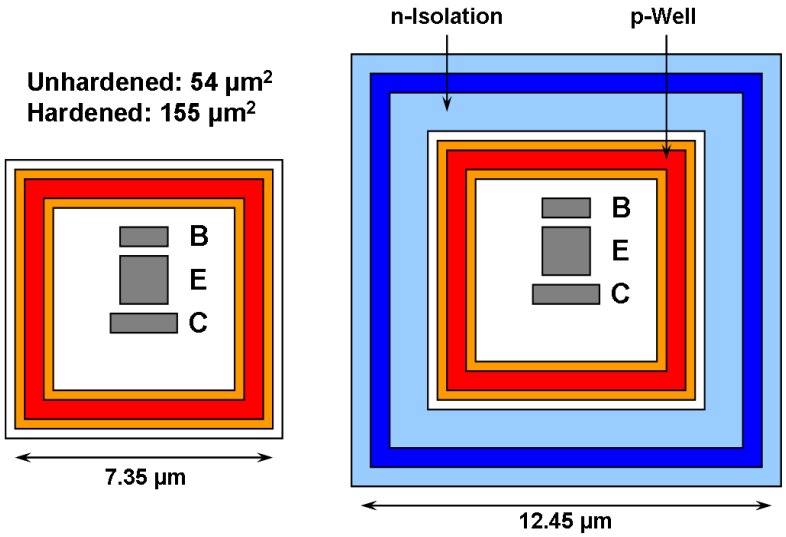

Figure 18: Top-down schematic view of the unhardened (left) and hardened (right) SiGe HBT structure. The junction isolation is shown in blue.

3.2 Test Conditions and Facilities

To determine the effectiveness of the junction isolation RHBD approach, Ion Beam Induced Charge Collection (IBICC) measurements were performed at Sandia National Laboratories, New Mexico with a 36-MeV normal-incidence 16O ion (LET of 7 MeV-cm^2/mg). Charge collection was measured simultaneously on all four terminals connected to amplifier chains composed of Ortec 142A charge sensitive amplifiers and Ortec 671 spectroscopy amplifiers. The testing methodology used is described in detail in [5]. The base, emitter, and substrate terminals of each device were grounded while the collector and n-implant (for RHBD devices) were biased at 3.0 V to emulate typical circuit operating conditions. To assess total ionizing dose performance, 63 MeV proton irradiation was performed at Crocker Nuclear Laboratory, University of California at Davis, using a dose rate of 1 krad(SiO_2)/s. All terminals were grounded during exposure and were measured at room temperature in incremental dose steps up to 1.05 Mrad. For both experiments the SiGe HBTs were wire-bonded into 28-pin DIP packages [14].

3.3 Single Event Radiation Results

Initial tests on the junction-isolated structures were aimed at determining whether the presence of the RHBD had any negative effect on basic device performance metrics. Figure 19 shows forward Gummel characteristics for three RHBD variants, as well as the control (unhardened) structure (A_E = 0.21x0.84 μm^2). No significant differences in DC performance were seen for any of the four tested variants. The n-implant was biased at 3.0 V during all measurements for consistency. As shown in Figure 20, which plots normalized unity-gain cutoff frequency against collector current density for the control, the 2.2 μm RHBD device, and the 2.55 μm RHBD device, no impact on AC performance was observed. For both the DC and AC measurements, V_{CB} was held at 0 V [14].

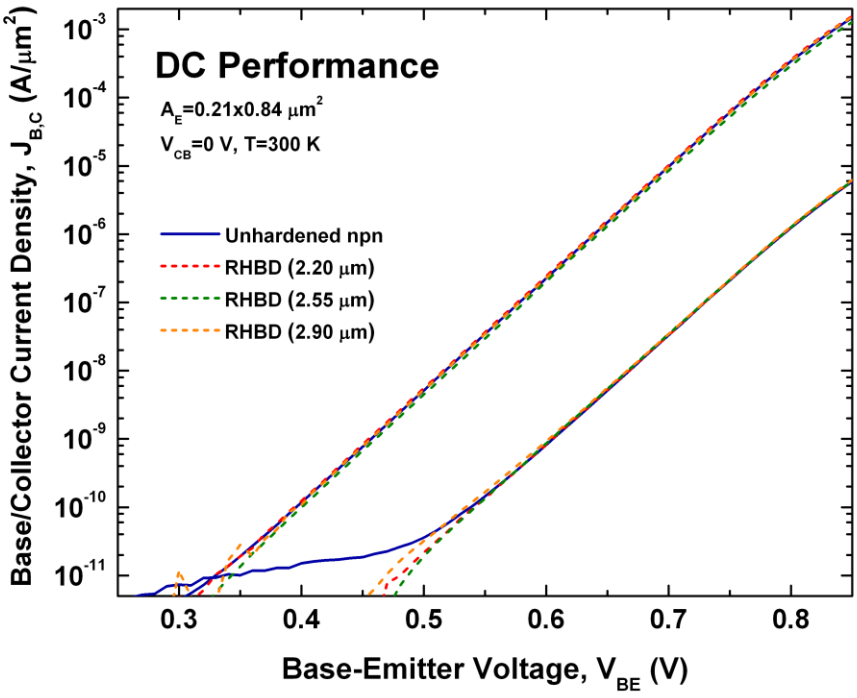

Figure 19: Forward mode Gummel characteristics for the unhardened *npn* SiGe HBT as well as three variants of RHBD devices.

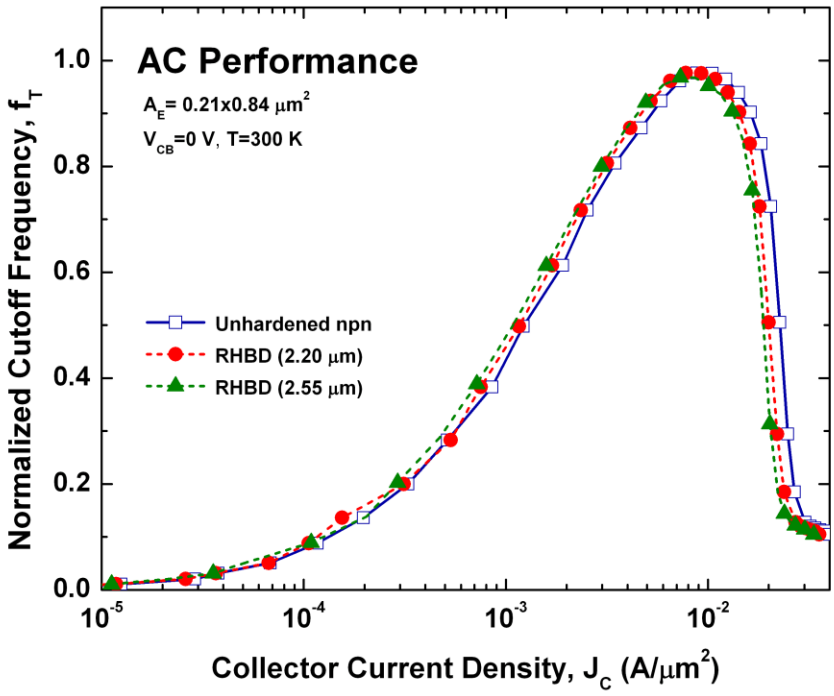

Figure 20: Normalized cutoff frequency plotted against collector current density for the unhardened *npn* SiGe HBT as well as two variants of n-ring hardened devices.

Further qualification of the proposed SEE hardening technique required that the TID tolerance of the devices be verified. Figure 21 shows forward Gummel characteristics for the two structures. On the left is a control SiGe HBT irradiated to 1.05 Mrad and showing base current degradation in incremental dose steps. On the right is the 2.2 μm junction-isolated RHBD device, irradiated to a maximum dose of 1 Mrad. The increasing base current with total ionizing dose has been previously documented and is the result of the production of traps near the emitter-base (EB) spacer [22]. Figure 22 plots normalized current gain against collector current density from the same datasets. As in the previous figure, the control results are shown on the left, while the 2.2 μm RHBD device results are shown on the right. The gain degradation curves are almost indistinguishable, indicating as expected that the addition of the junction isolation has no effect on the TID

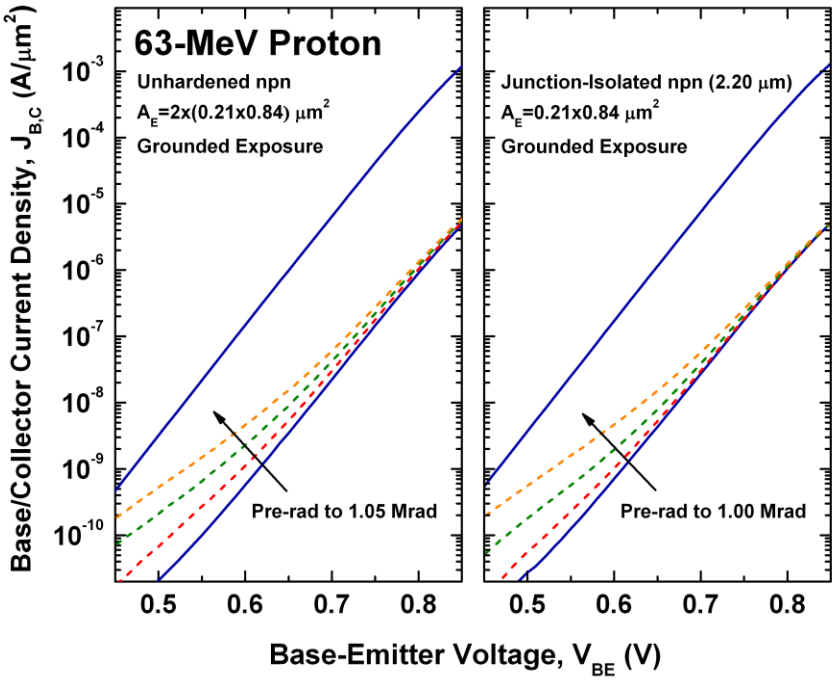

Figure 21: Forward-mode Gummel characteristics for proton irradiated devices with (right) and without (left) junction isolation RHBD.

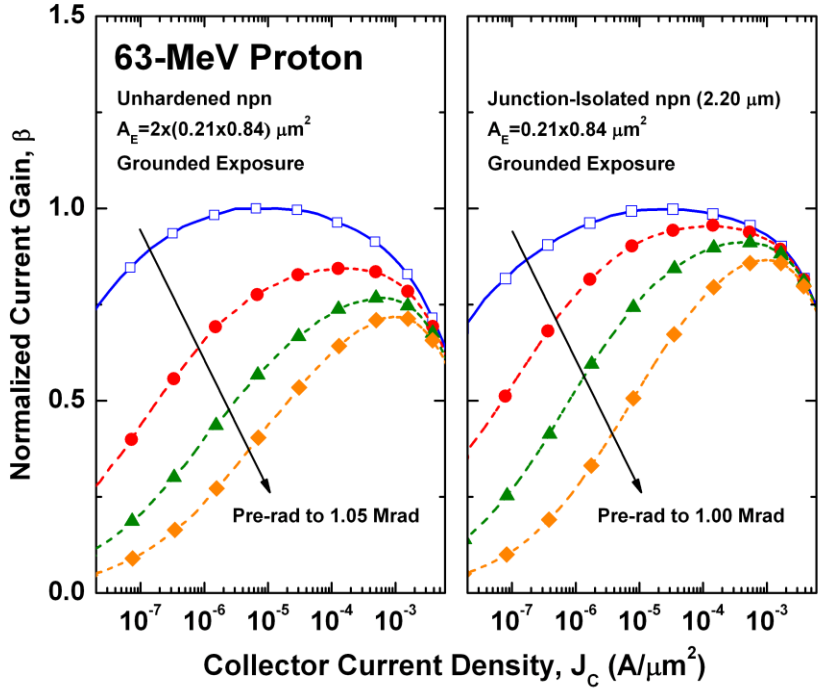

Figure 22: Normalized current gain vs. collector current density for proton irradiated devices with (right) and without (left) RHBD.

tolerance of the device [14].

To determine whether the junction isolation RHBD would fulfill its intended purpose, IBICC testing was performed on all device variants and the control. Figure 23 illustrates the substantial reduction in charge collection afforded by this new hardening technique. The curves represent a 2 μm wide slice in the x-direction through the center of the device, while the contours in Figures 24 and 25 represent the entire surface. Each dataset consists of numerous scans of the area containing the DUT, and for each x-y location, only the maximum collected charge is plotted (subtracting outliers). Clearly the pn-junction isolation in the hardened devices, starting at roughly ±4 μm, absorbs a substantial amount of charge for strikes in its vicinity. Observe as well the 25% reduction in charge

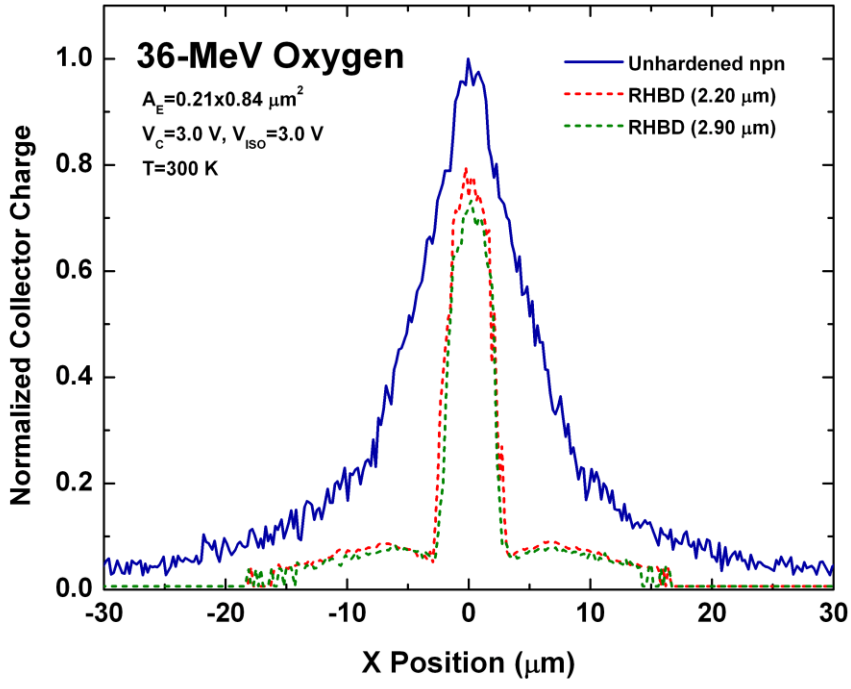

Figure 23: Charge collection in the subcollector during oxygen microbeam irradiation for both the unhardened *npn* SiGe HBT and two RHBD variants.

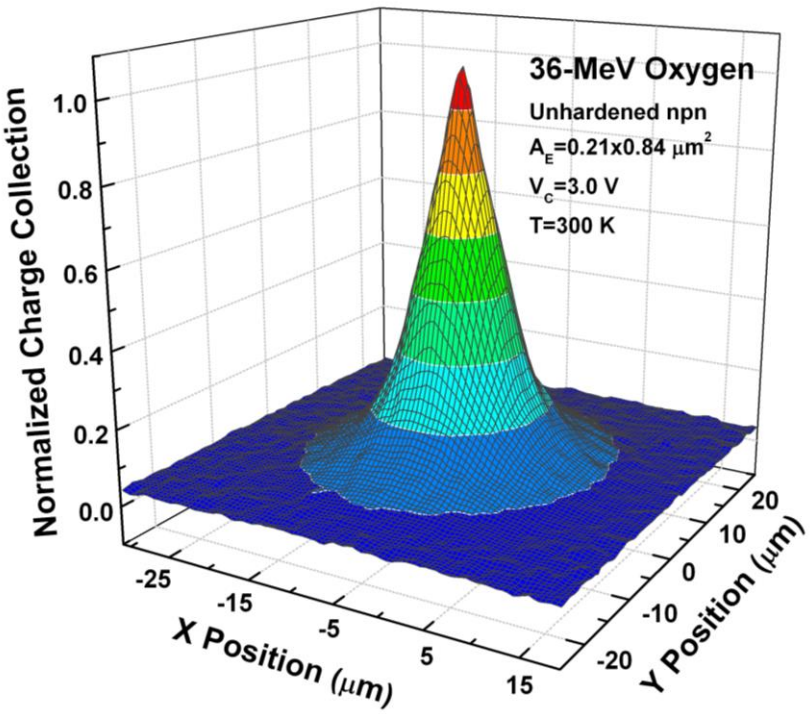

Figure 24: Normalized collected charge for the unhardened *npn* SiGe HBT as a function of strike location.

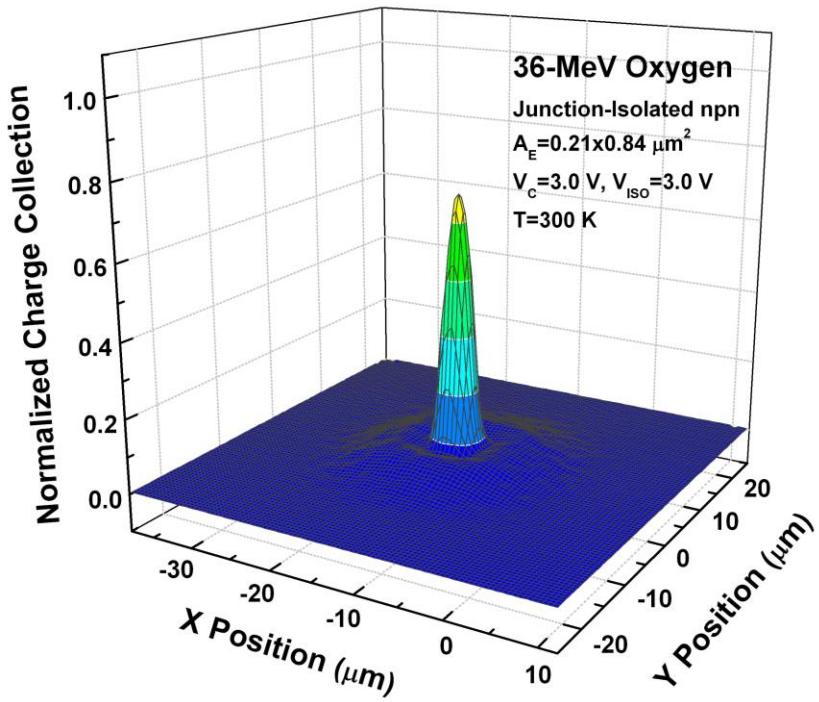

Figure 25: Normalized collected charge (to the peak of Figure 23) for the RHBD *npn* SiGe HBT as a function strike location.

The two hardened variants exhibited only small differences, with the more aggressive 2.9 μm n-ring design achieving a slightly better charge collection profile. Figure 26 plots the same charge collection data integrated over the x-axis. The RHBD SiGe devices showed nearly a 70% reduction in integrated charge collection over the control device. Figure 27 shows the best achieved results using more traditional third-generation n-ring RHBD outside of the DTI (e.g., in IBM SiGe 8HP) [6]. The present results represent the most effective transistor layout-level RHBD demonstrated to date in SiGe. While there is an incurred device area penalty for SEU mitigation incurred by the present RHBD approach, as shown in Figure 18, this should have minimal impact for actual circuit design complexity or net circuit real estate, given that SiGe circuits are typically not transistor-area limited [14].

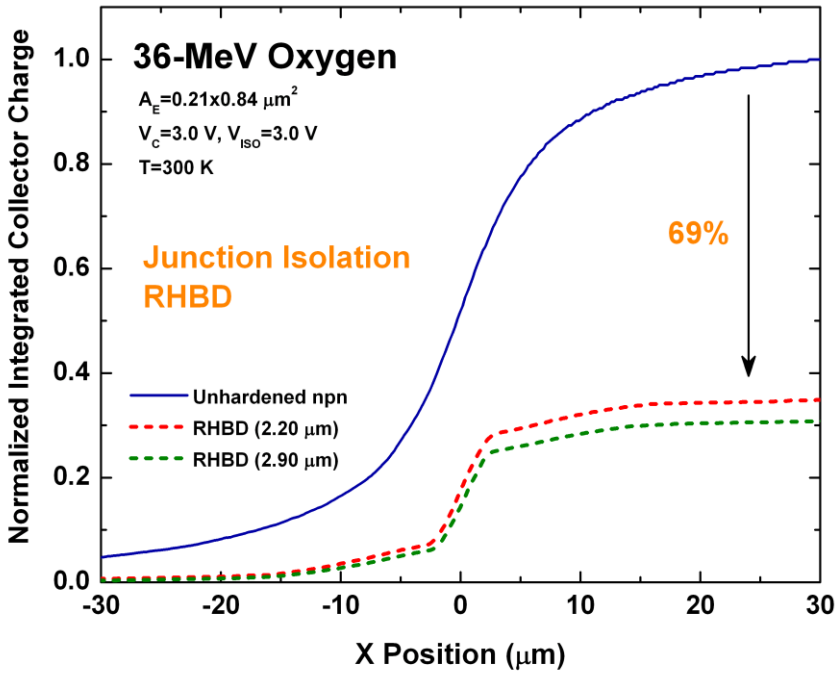

Figure 26: Integrated charge across ion strike location for both the unhardened *npn* SiGe HBT and two RHBD variants with shallow trench isolation.

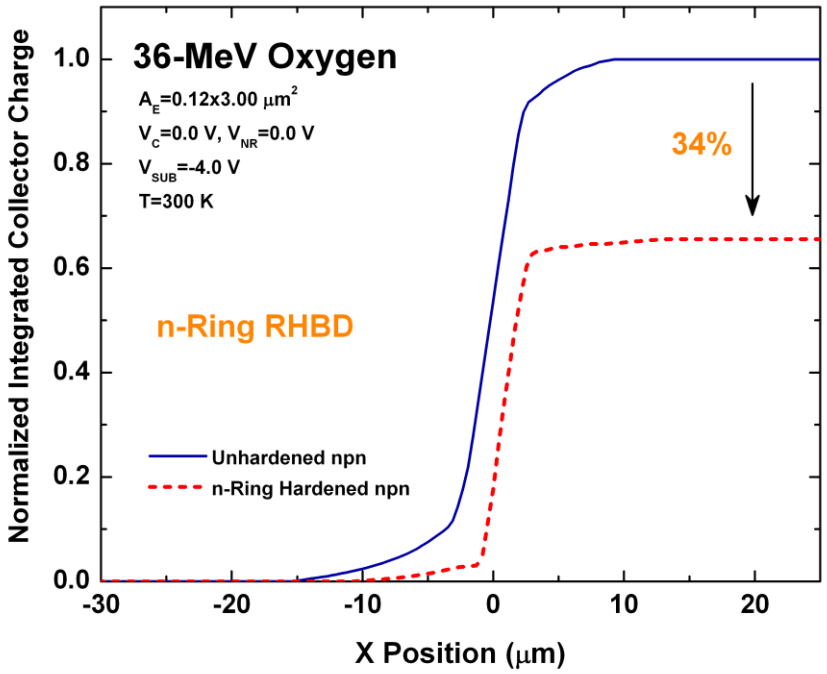

Figure 27: Integrated charge across ion strike location for both unhardened and n-ring hardened 8HP SiGe HBTs with deep trench isolation.

3.4 SEE Discussion

This investigation shows that device-level SEU hardening of most 3rd generation SiGe HBT technologies can be hindered by the presence of deep trench isolation. By the addition of a simple yet effective junction isolation RHDB scheme into a SiGe process without DTI, we have developed an effective hardening technique capable of helping mitigate both outside DTI strikes and inside DTI strikes. The junction isolation RHBD was able to reduce the peak collected charge from a center striking 36-MeV oxygen ion to a mere 128 fC, and achieve the most effective device-level reduction of total integrated charge in a SiGe HBT to date. These advantages are obtained at no penalty to other performance metrics, with no process modification, and with only a modest area penalty [14].

CHAPTER IV

CHARGE AMPLIFICATION CHANNEL

4.1 Introduction

The SiGe Integrated Electronics for Extreme Environments research group (SiGe EEE) was established under the NASA Exploration Technology Development Program (ETDP) to develop electronic systems in state-of-the-art SiGe platforms to meet the challenges posed by complex initiatives such as lunar colonization. The Remote Health Node (RHN), originally designed at BAE Systems for the X-33 spacecraft, was chosen as a starting point in order to demonstrate the numerous advantages that can be leveraged in an integrated BiCMOS process.

The original design, shown in Figure 28, sought modularity by combining multiple types of sensor interfaces into a single hardware implementation usable throughout a spacecraft or exploration vehicle to provide mission critical data to engineers in an efficient, reliable manner [27]. Advancing this concept one step further, the SiGe EEE team has developed an integrated version of the RHN, not only reducing form-factor and power by substantial margins, but also completely eliminating the need for isolation from the environment [7]. The entire SiGe Remote Electronics Unit (REU) is designed to be housed within a single connector (Figure 29) or multi-chip package, and utilized throughout the spacecraft or surface vehicle as required by a mission's sensor payload.

Piezoelectric sensing represents one of many common applications that stand to benefit from such a modular system design approach. This proposal describes the design

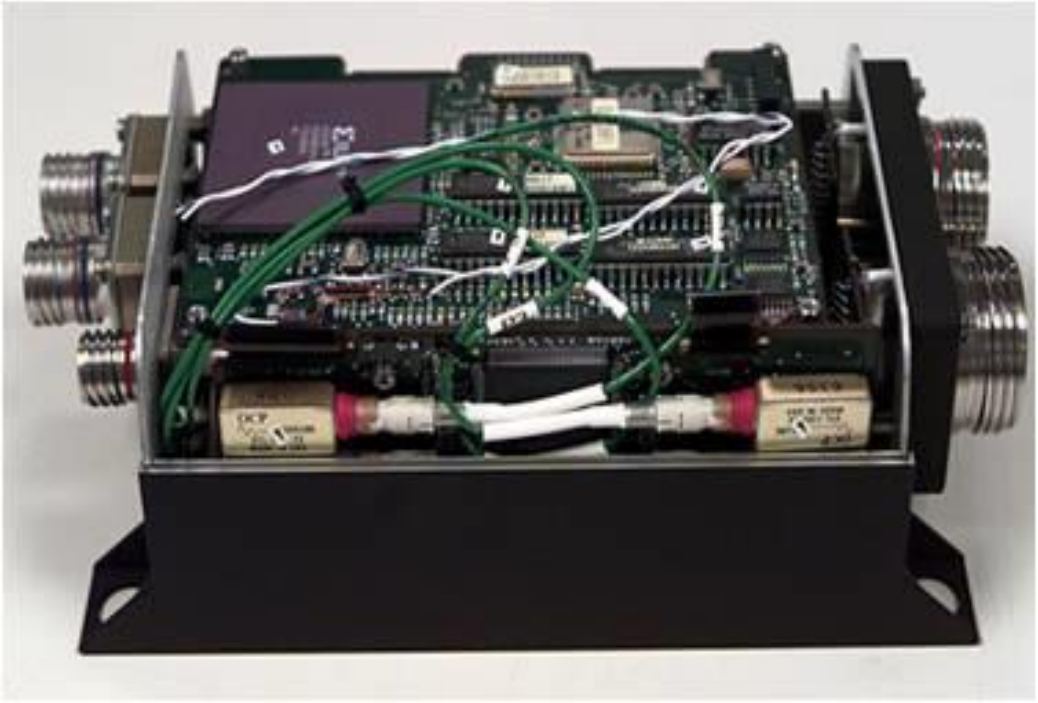

Figure 28: Original implementation of the Remote Health Node developed by BAE Systems.

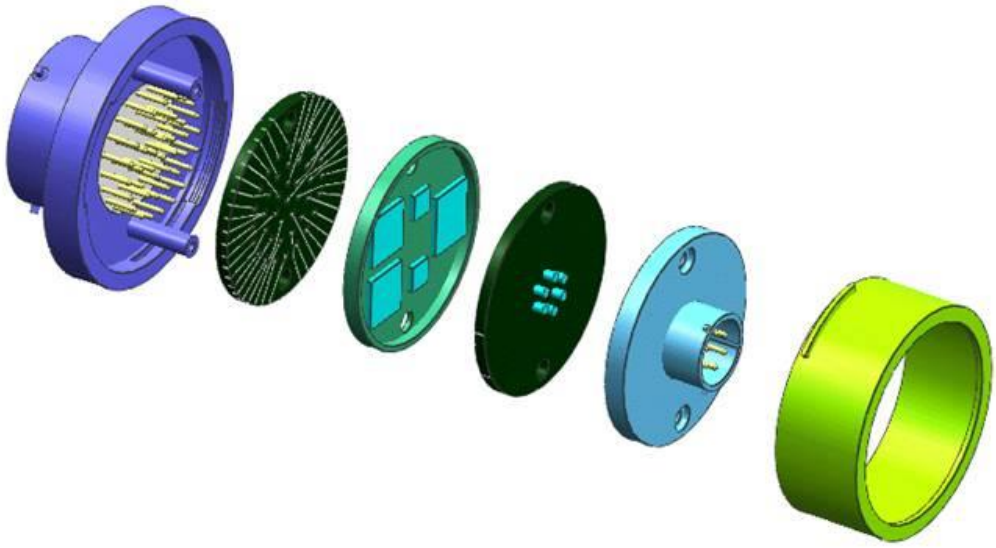

Figure 29: Rendering of the new Remote Electronics Unit connector housing.

and measurement of a SiGe charge amplification channel developed as a part of the much larger Remote Electronics Unit (REU) for space system avionics platforms. The channel was designed in a 1st generation SiGe technology platform as a fully monolithic solution, with the exception of the passive network required for charge amplification. The signal path consists of a low-offset, high-input impedance op-amp, a variable gain switched capacitor amplifier with a sample-hold stage, a 6th order Butterworth filter, and a voltage level shifter. Two programmable shift registers provide gain control, calibration, and offset compensation through an 8-bit voltage DAC. Special consideration was given to wide-temperature biasing, which is provided in part by an exponential curvature-compensated bandgap reference. The layout occupies a total area of 2.61 x 0.84 mm2 and consumes only 13.2 mW of power. This represents a significant improvement over the original RHN design.

4.2 Technology Platform

The BiCMOS technology chosen for the development of the Remote Electronics Unit was the IBM SiGe 5AM platform, which integrates a 50 GHz, self-aligned *npn* HBT into a 0.5 µm CMOS process. An SEM cross-section of the SiGe HBT is shown in Figure 30. The platform includes 1.35 fF/µm2 metal-insulator-metal (MIM) capacitors, low temperature-coefficient polysilicon resistors, and four layers of metallization for routing, including a thick, analog copper top metal. While the SiGe HBT used in the process has been shown to possess favorable performance metrics at low temperatures due to the beneficial effects of the Ge-grading-induced drift field [12], it was still necessary in initial phases of the project to produce accurate, reliable models for both the SiGe HBT and CMOS devices used in the design for temperature ranges well beyond those available

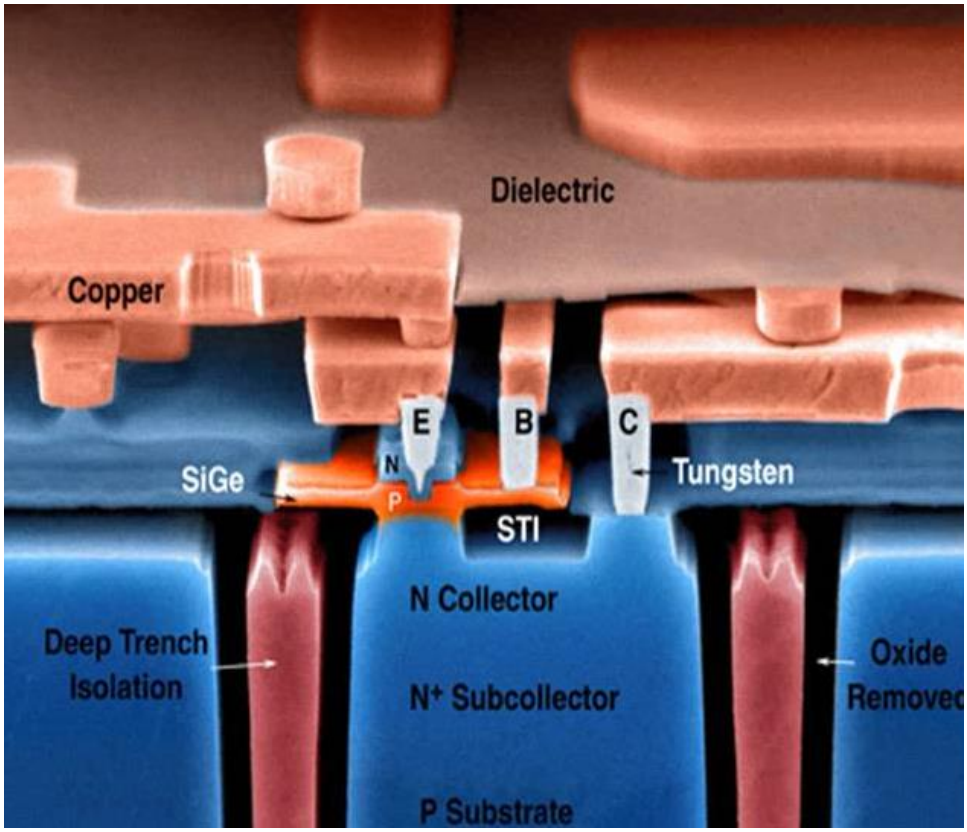

Figure 30: SEM cross-section of a SiGe HBT [12].

in the basic IBM process (-55ºC to 120ºC).

In addition to wide-temperature performance, reliability of active devices at cryogenic temperatures was carefully examined in early phases of the project. It has been shown that SiGe HBTs exhibit robust operation under stress at both cryogenic and high temperatures with no indication of reliability degradation [28]. It is well documented, however, that the performance of nFET devices can be compromised by hot carrier effects (HCE), and that these effects are exacerbated at cryogenic temperatures [29]. To mitigate this potential reliability issue and to simultaneously reduce leakage effects from radiation-induced shallow-trench oxide interface traps, a minimum nFET gate length of 1 µm was enforced for all designs. No such requirement was enforced for the gate lengths

of the pFETs, as they are inherently less susceptible to both HCE and leakage effects caused by ionizing radiation exposure. SiGe HBTs have also been shown to possess resilience to total ionizing dose effects, due primarily to the vertical structure of the device, where dose levels exceeding 1 Mrad(SiO2) have produced little observable effect in device performance (both DC and AC) at bias levels of interest [30, 31]. nFETs do not share this tolerance, however, and some consideration for bias levels with respect to expected radiation dose is required in order to ensure that the drain-source leakages at the edges of the shallow trench isolation (STI) do not adversely affect circuit performance. In general the nFETs in this technology do not exhibit enough performance degradation up to the specified 100 krad(SiO2) to pose a major challenge for circuit design, and the previously mentioned 1 µm minimum gate length imposed for the project serves to mitigate the issue even further.

Consideration also had to be given to the susceptibility of BiCMOS circuits to potential latch-up events caused by heavy ion irradiation. When p-type and n-type (nFET or HBT) devices are placed in close proximity, latch-up can occur when the parasitic transistor formed between the pFET n-well and the n-type devices enters a high-current, positive feedback state [32]. Particularly in a radiation environment, an ion strike to the vicinity of this parasitic transistor can cause a latch-up state to occur where it may not have in a terrestrial setting. Careful layout techniques, including liberal use of n-well contacts, substrate contacts, and guard bands, were used throughout the circuit designs to harden against this phenomenon. Figure 31 shows two examples of these layout techniques as they were implemented for this project [15].

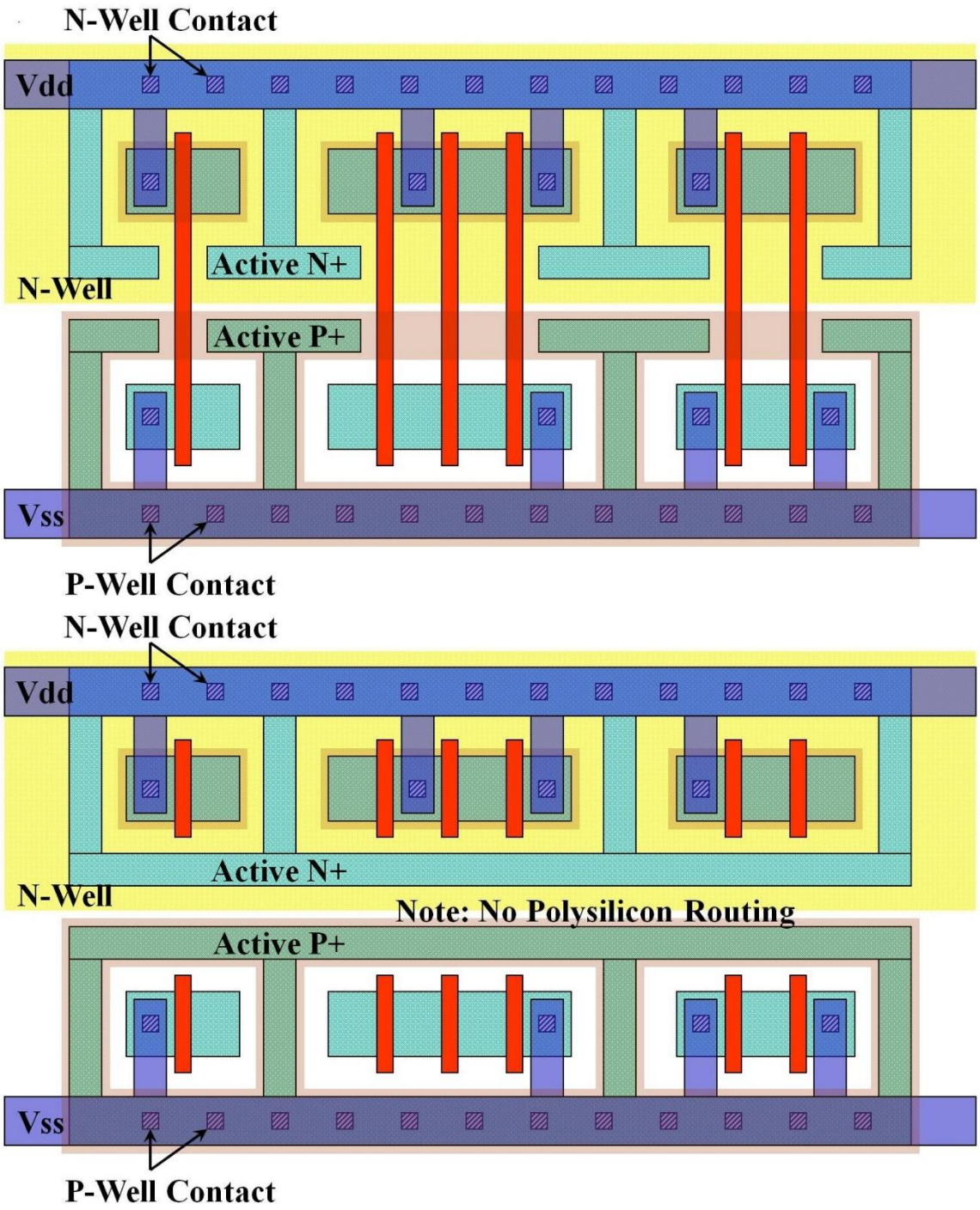

Figure 31: Digital layout with additional well contacts and partial (top) or full (bottom) guard rings.

4.3 Channel Architecture

A charge amplifier functions by converting charge stored on a capacitor to voltage at its output node. The nature of this process allows a charge amplifier to maintain signal integrity in highly capacitive environments that would normally prohibit a voltage amplifier from properly functioning due to strong attenuation of the AC data presented by the sensor. The range of applications for such amplifiers is broad. The advantages are illustrated simply by considering a system in which the sensor and amplifier cannot be placed in close proximity. A charge amplifier's inherent insensitivity to input load capacitance, C_{in}, allows it to process signals across long lengths of capacitive cabling and provide flexibility and modularity to an otherwise limited system. These advantages are leveraged to good effect in extreme environments, where distributed signal processing may not always be practical [33].

The complete charge amplifier channel architecture is shown schematically in Figure 32 with the finalized 2.62 x 0.86 mm^2 layout shown in Figure 33. The design is based loosely on the original BAE implementation consisting entirely of off-the-shelf components. The new charge amplifier is fully monolithic, with the exception of the feedback resistor and capacitor (R_f and C_f) on the channel front-end. For charge amplification, the output voltage is determined to first order solely by the amount of charge provided by the sensor and the size of the amplifier's feedback capacitance, as:

$$V = \frac{Q_{in}}{C_f} \tag{4}$$

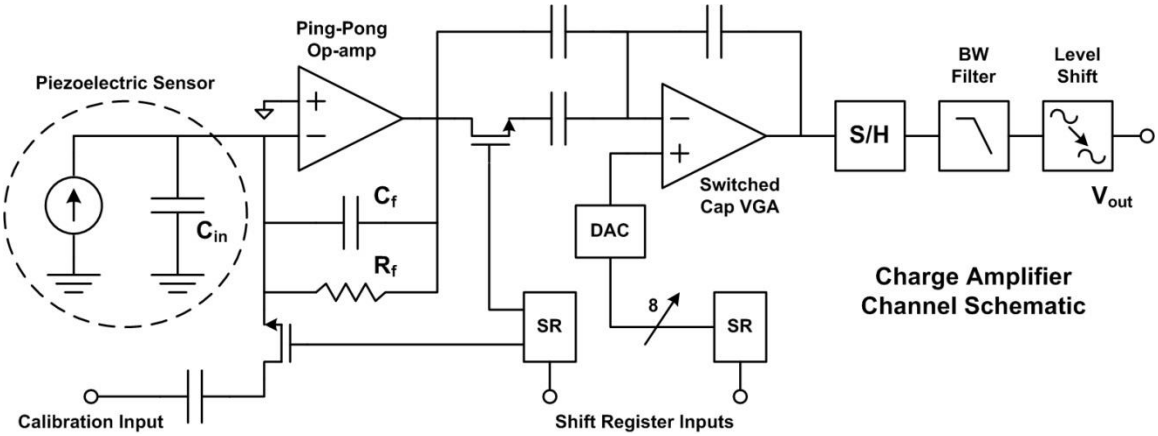

Figure 32: Schematic design of the full charge amplifier channel, including a basic lumped element model for the piezoelectric sensor input.

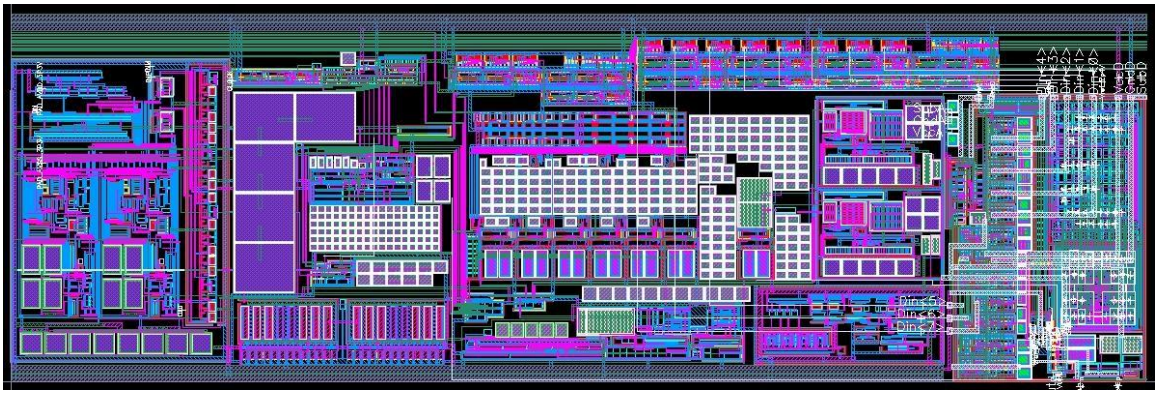

Figure 33: Complete charge amplifier layout.

Constrained by the need to amplify relatively large charge amplitudes at low frequencies with a maximum rail voltage of 3.3 V, a 33 nF capacitor and a 10 MΩ resistor were chosen for the feedback network, neither of which could be fabricated on-chip within a reasonable die area. Details of the individual integrated circuit blocks are found in the sections that follow.

4.3.1 Ping-Pong Amplifier Input Stage

A fundamental requirement for precision charge amplification is to present a high input impedance to the output of the piezoelectric sensor such that charge loss to the input of the initial gain stage is minimized. The finite current gain of bipolar devices (available in a BiCMOS process) make them less effective in this respect, so an amplifier design with a common-source, nFET input stage was chosen to act as the channel's front-end. In previous design iterations, it was also determined that offset would represent one of the biggest challenges in the channel architecture. Within BAE's off-the-shelf solution, offset was easily negated with coupling capacitors between each gain stage. Unfortunately, monolithic designs are not capable of integrating the large capacitors required for low frequency AC coupling due to the large silicon die areas they require. Application of a technique known as auto-zeroing (AZ) was used to mitigate this issue.

Figure 34 depicts a block level diagram of the AZ technique as described by Enz and Temes in [34]. Cancellation of offset is accomplished by sampling the shorted inputs of the operational amplifier (switch closed) to determine the input referred V_{os}. This value is stored on a capacitor in the sample-and-hold block such that when V_{in} is sampled, the stored voltage is subtracted from the amplified output. The end effect is cancellation of the internal offset of the amplifier and a substantial reduction in 1/f noise. Despite these advantages, some increase in the noise floor will be introduced due to aliasing of the transients generated by the switching process [34].

Because the amplifier operates in two distinct phases, sampling and amplifying, it is not inherently capable of utilization in a continuous-time application. Conversion of the AZ architecture to a continuous time solution was accomplished by implementing the

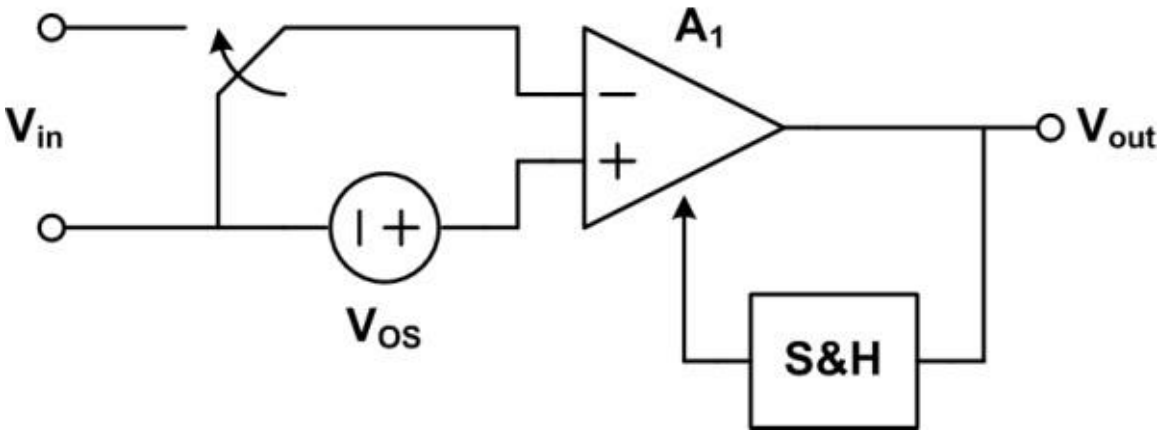

Figure 34: Block diagram representation of the autozeroing technique [34].

ping-pong configuration depicted in Figure 35. The topology consists of two identical AZ amplifiers, switch networks, sample-and-hold filters, and switch drivers. When switched out of phase, at any given time one of the amplifiers is sampling its offset while the other is amplifying its autozeroed input. As a whole, the amplifier acts in a continuous fashion [35, 36]. Measured results across temperature are shown in Figure 36, with the complete frontend exhibiting no more than 40 μV of offset across a 180˚C temperature range. Details of the individual circuit blocks are fully described in [37].

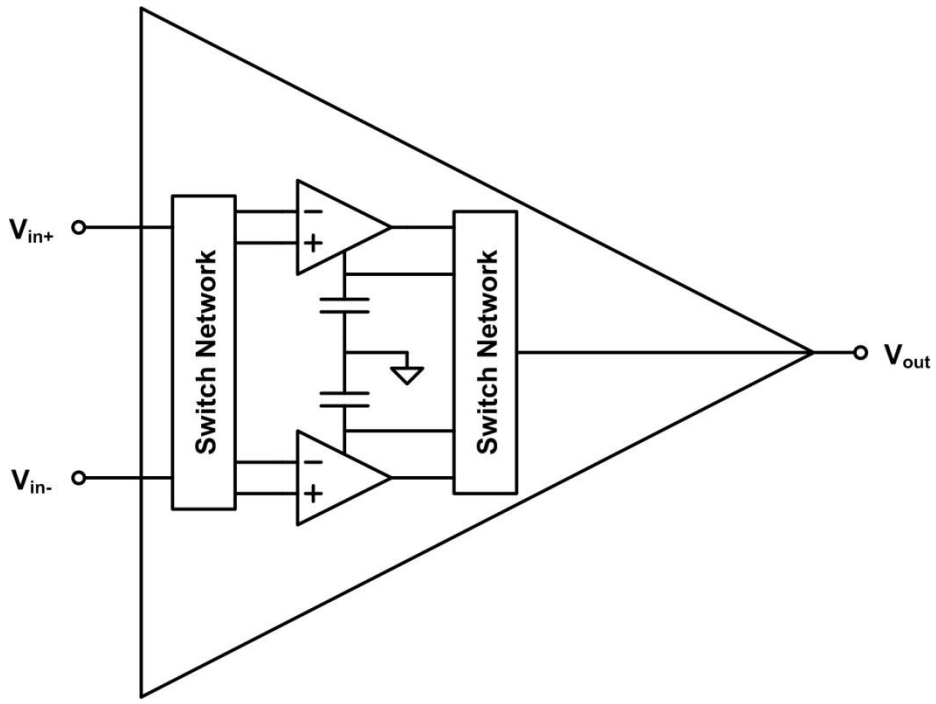

Figure 35: Block diagram of the ping-pong auto-zero operational amplifier [36].

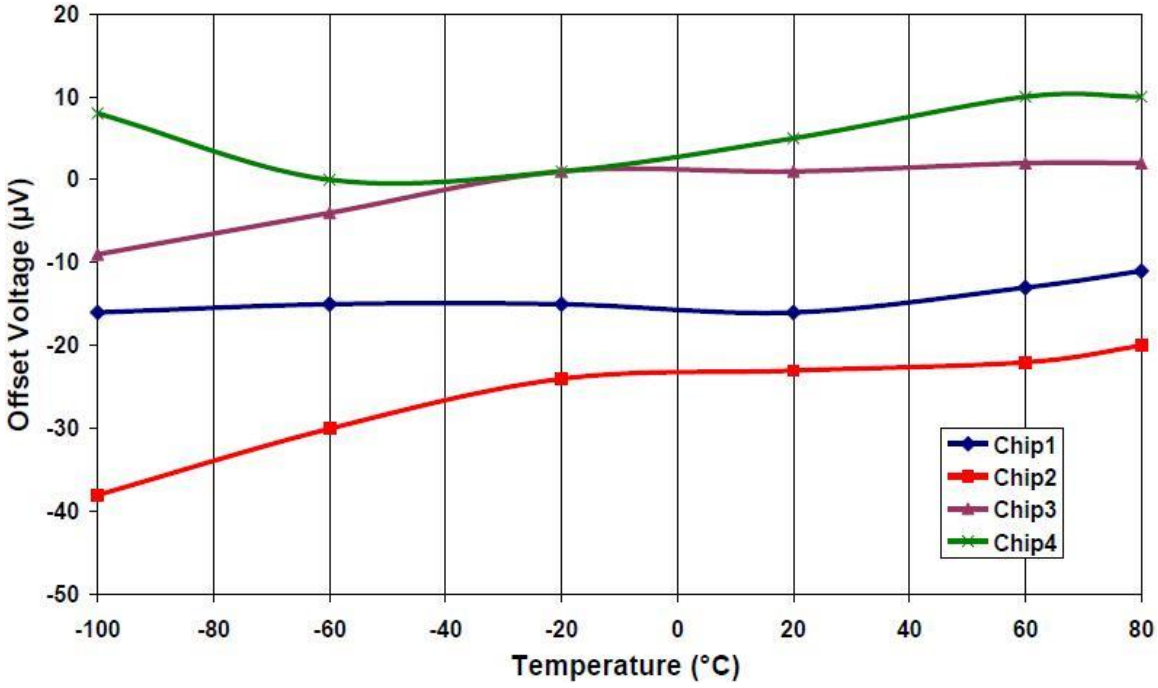

Figure 36: Offset vs. temperature measured for four ping-pong op-amps [33].

4.3.2 Switched-Capacitor Variable Gain Amplifier

Applying the same auto-zeroing principles utilized in the ping-pong front end, the second stage of the charge amplifier channel minimizes voltage offset using a feedback path to a nulling input. The schematic design is shown in Figure 37. Two gain states (A_V = 10 and A_V = 50) are realized in the capacitive feedback network, with the high gain feedback path being programmable through an nFET gate controlled by one of the two shift registers used in the channel. The other MOS gates are clocked continuously by signals from a clock generator that takes a single-ended 83.125 kHz signal and produces the various phases necessary to alternate the amplifier between its zeroing and amplification states. In the sampling state, the output of the main amplifier is fed back through a secondary opamp where the offset voltage is stored on C_{null}. This voltage is then cancelled during the amplification phase by a nulling differential pair in the main amplifier [34]. Figure 38 shows Monte Carlo offset results for 25 samples, taking into account normal process variation. The simulations show an average offset of 13.6 mV.

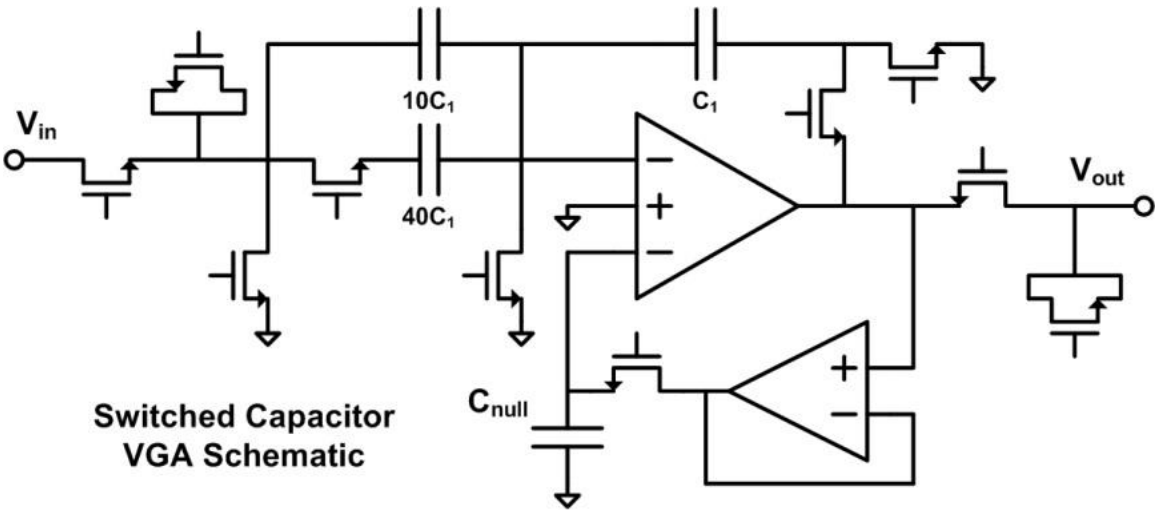

Figure 37: Schematic design of the switched capacitor variable gain amplifier.

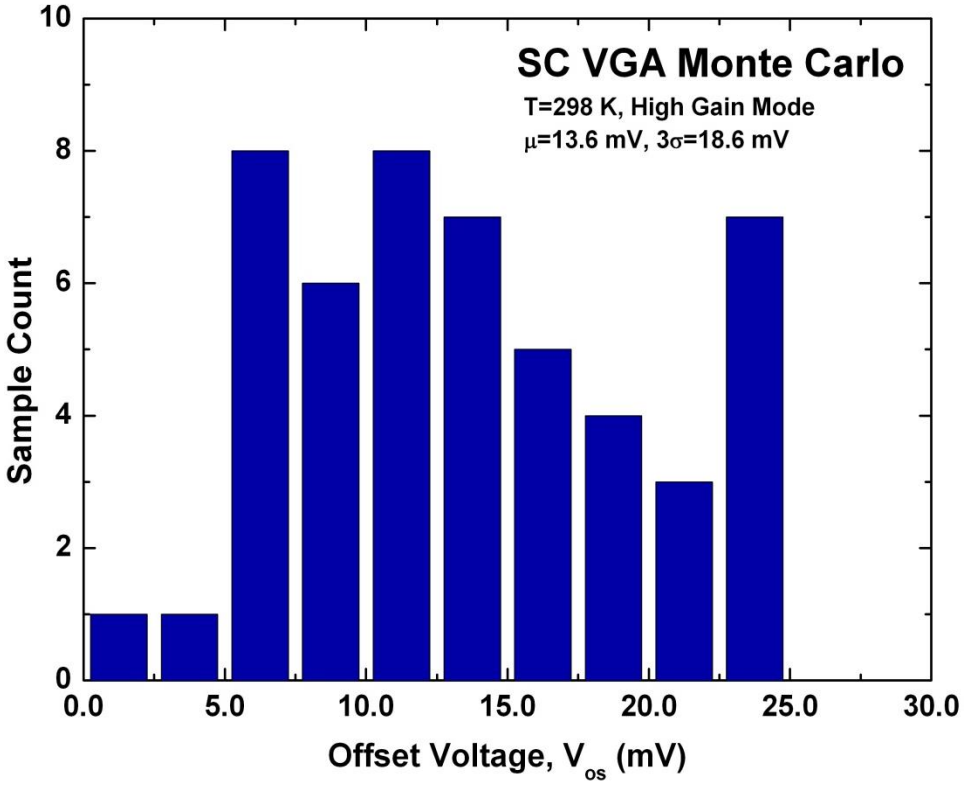

Figure 38: Monte Carlo (25 samples) offset voltage simulation results for the SC VGA in high gain mode.

In a final effort to guarantee that the charge channel signal following amplification would not "rail" in any gain configuration, the reference voltage provided for the entire switched capacitor VGA was produced from an 8-bit calibration DAC controlled by the second programmable shift register (shown in Figure 32). The voltage DAC was designed for stability across the full temperature specification and produces a stable, adjustable reference that calibrates out offset drift in the channel caused by environmental factors. Unlike the input stage, the VGA does not employ a ping-pong architecture. Instead, the output is filtered by a sample-hold amplifier switched out of phase with the VGA before it is sent to the Butterworth filter.

4.3.3 Sixth Order Switched Capacitor Butterworth Filter

The original specification for the charge amplifier channel called for programmable filtering at three distinct cutoff frequencies up to 5 kHz. To this effect, a 6th order low-pass switched capacitor Butterworth filter was designed, and serves to filter high-frequency signals such as the switching noise introduced by the previous channel stages and to prevent aliasing of the ADC that processes the channel output. The Butterworth architecture is a popular method for designing high-order and high-selectivity (high-Q) filters and operates by transforming the desired transfer function into cascaded first- and second-order stages. It has the advantage of reduced sensitivity to quantization of its coefficients and provides good phase response [38].

The Butterworth filter schematic is shown in Figure 39. Its three bi-quad stages utilize custom op-amps with MIM capacitor feedback networks. The MOS switches are controlled by a clock divider circuit that produces the clock phases necessary for its operation. The final implementation of the channel utilizes three clock frequencies for the Butterworth filter (665 kHz, 332.5 kHz, and 83.125 kHz) which are divided by a clock-to-cutoff frequency ratio of 100:1. A standalone version of the filter was extensively

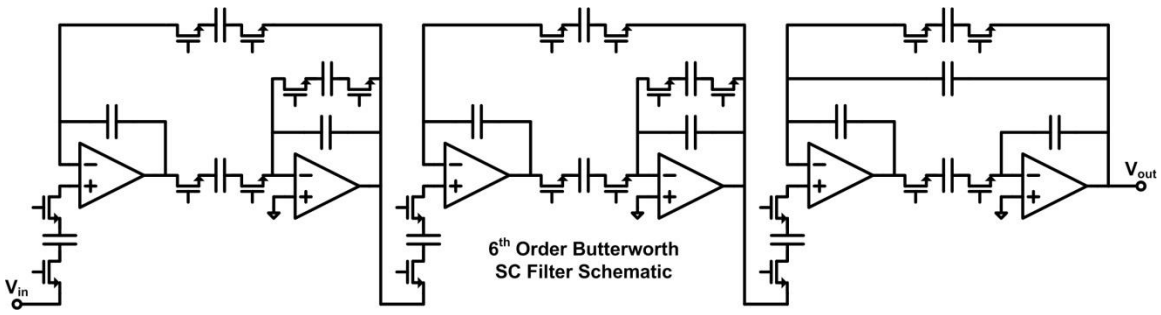

Figure 39: Schematic design of the sixth order Butterworth switched capacitor filter [38].

tested across the full specified temperature range (-180ºC to 125ºC) with consistent results attributable to the use of temperature stable biasing techniques, as described in the next section. The output of the Butterworth feeds a post-filter composed of a single op-amp and feedback network. The post-filter places two poles above the corner frequency to assist in the reduction of clock feed through [38].

4.3.4 Wide-Temperature Bandgap Reference

The development of stable biasing techniques represents one of the most important challenges in the design of reliable integrated circuits for extreme environments. These references serve as the foundation upon which the rest of the system relies, and it is of the utmost importance to ensure that they are designed with the specific needs of each analog circuit block in mind. A designer's success in this area is heavily dependent on the quality of the available device models, and most often these models do not remain accurate below the lowest military temperature specification of -55ºC. For the scope of this project, the development of models preceded any subsequent work on analog circuits.

The BiCMOS voltage reference most heavily utilized in the charge channel was first conceived by Lee [39] and consists of an exponentially curvature-compensated design which uses the inverse relationship of an HBT's base-emitter voltage (V_{be}) to temperature to compensate the typical behavior of a proportional to absolute temperature (PTAT) current source. This design was refined and tested in the current technology platform in [40], and is shown schematically in Figure 40. The output voltage, taken from the positive side of R2, can simply be defined as:

$$V_{out} = I_{PTAT} R_2 + V_{be,Q1} \tag{5}$$

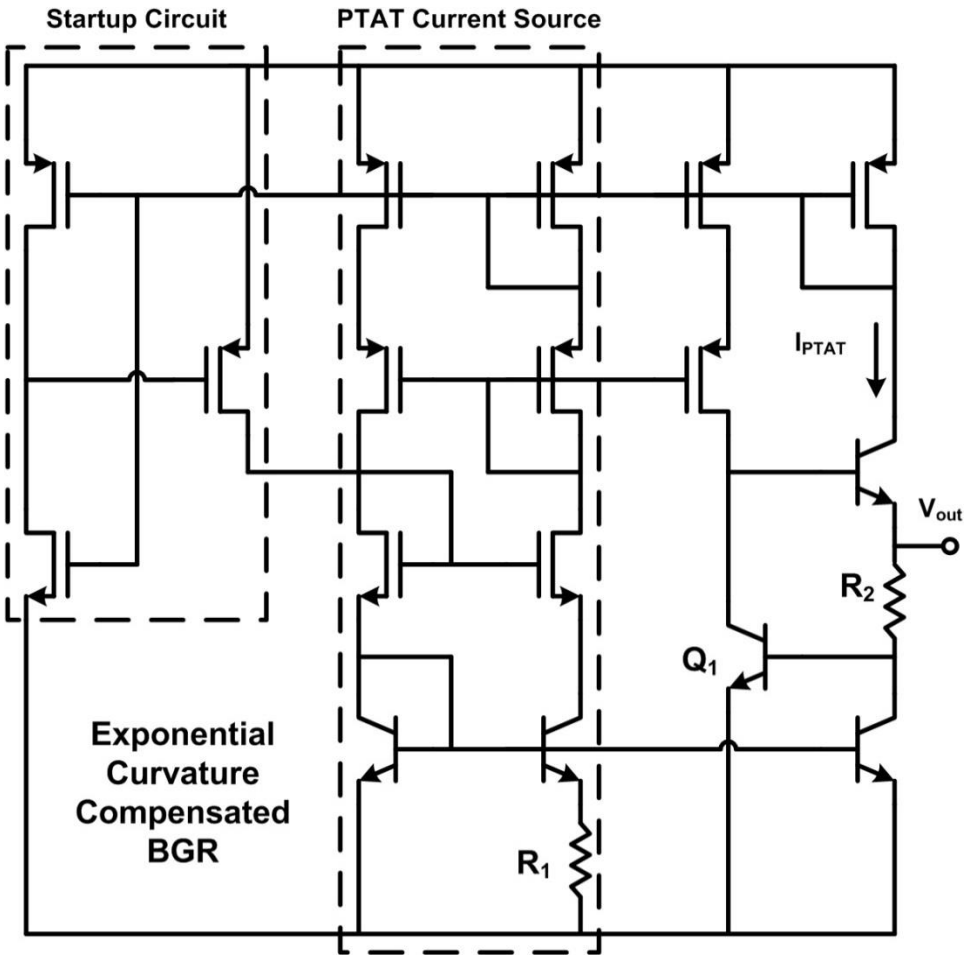

Figure 40: Schematic design of the exponential curvature-compensated bandgap reference.

As ambient temperature rises, the current provided by the PTAT current source and mirrored through R2 rises proportionately. The placement of Q1, however, allows the exponential decrease in V_{be} with temperature to compensate. In this way, the design is able to maintain a stable output voltage across extremely wide temperature ranges. The BGR fabricated for this project was tested from -180ºC to 27ºC, achieving an impressive best case temperature coefficient of 28.1 ppm/ ºC [40].

4.4 Channel Characterization

Preliminary verification of channel functionality was performed with the full analog remote sensor interface, including all sixteen channels and the analog-to-digital converter, wirebonded into a 121-pin grid array package (PGA). The package was mounted onto a custom designed printed circuit board and stimulated using a Keithley 6221 AC Current Source. The chip was designed to receive all of its clocking and control signals from the remote digital control interface, but it was necessary to provide those signals externally prior to proving functionality of the full REU. National Instrument's SignalExpress software package was used to provide synchronized clocks and data strings to the various components, while the SC VGA and Butterworth clocks were supplied by a Tektronix AFG3252 Arbitrary Function Generator.

Figure 41 shows functionality of the programmable offset correction built into the switched capacitor VGA. Each consecutive waveform represents an increment of four in the calibration shift register. For the purpose of the measurement, the channel was operating in low gain mode with an input square wave frequency of 1 kHz and amplitude of 2.5 μA. Integration of this square wave by the charge amplifier front end produces the familiar triangle wave output seen in the plot. The full scale voltage range following the level shifter at the end of the channel is 0 to 1.2 V, which is required by the design of the ADC. This data, and all subsequent data presented in this section, were taken at room temperature.

In Figure 42, waveforms are shown for each of the gain states of the charge channel. Both originated from a 1 kHz, 500 nA square wave input. The noise that is apparent in the low-gain waveform is caused, at least partially, by the long signal lines required to

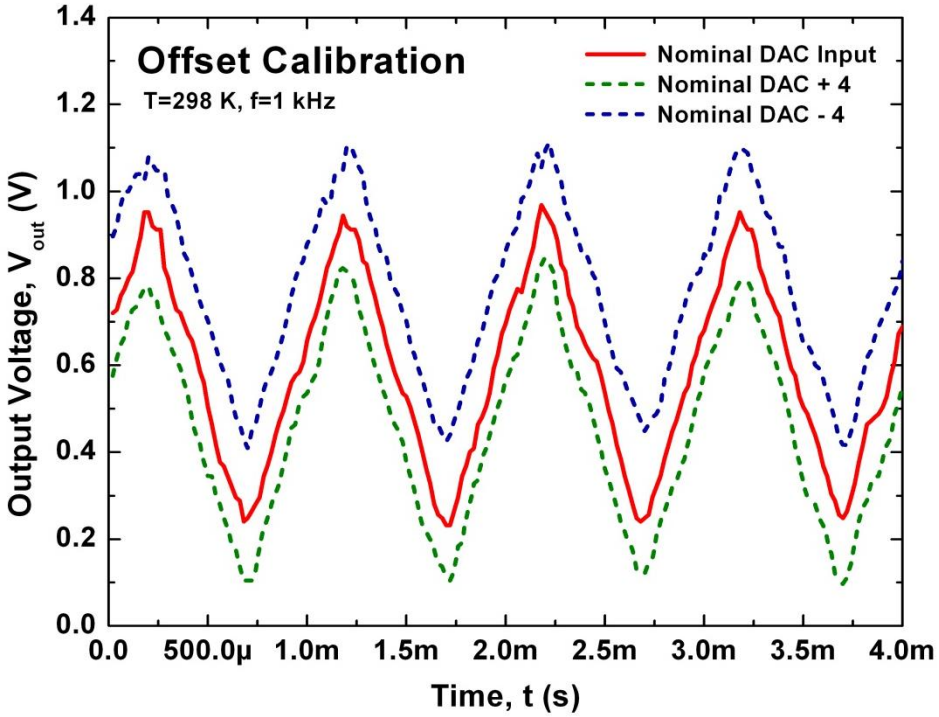

Figure 41: Output voltage vs. time showing the offset calibration capability of the SC VGA.

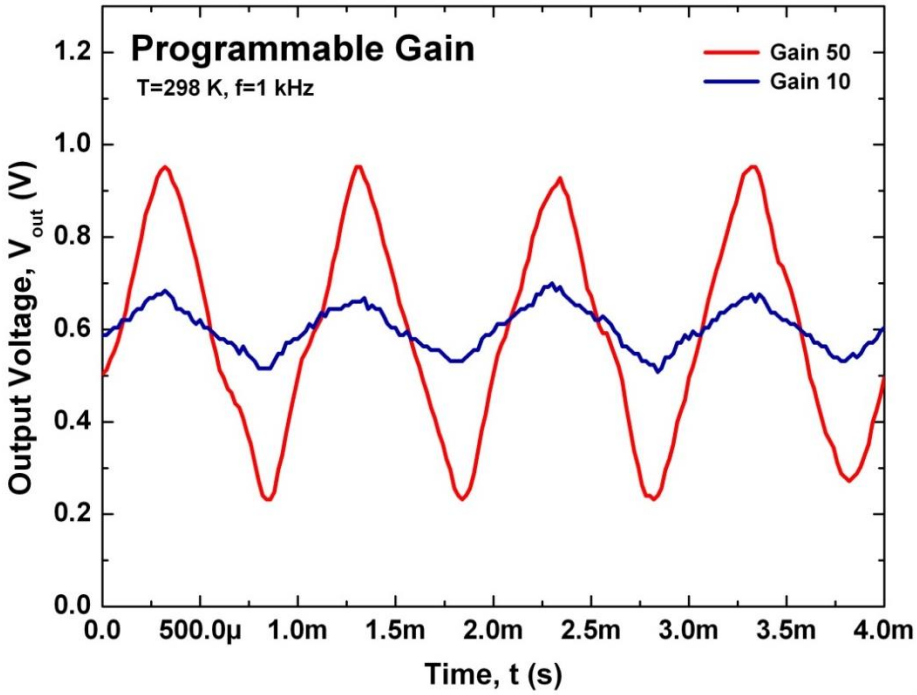

Figure 42: Output voltage vs. time showing the channel's programmable gain functionality.

measure the charge channel stand-alone. In the completed multi-chip module (presently in fabrication), it is expected that noise levels will decrease substantially. Figure 43 depicts all three filtering frequencies of the Butterworth filter in operation. The 1 kHz input signal is not attenuated for the two higher corner frequency cases. As the corner frequency dips below 1 kHz, however, the higher frequency harmonics are removed and the output is converted to a sine wave.

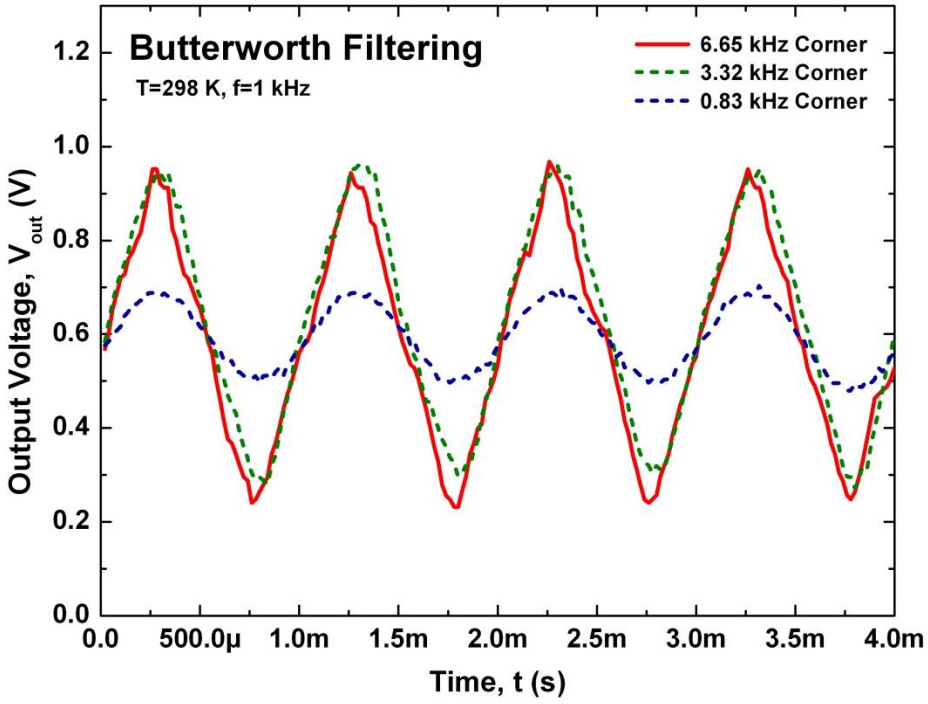

Figure 43: Output voltage vs. time showing three Butterworth corner frequency settings.

The wide-temperature performance of the charge amplification channel was characterized using a custom built nitrogen dewar designed at Vanderbilt University (shown in operation in Figure 44) [41]. The dewar was designed to allow simultaneous cryogenic operation and broad beam irradiation through the inclusion of a port that could be mounted directly to the beam line at Texas A&M University. Cryogenic operation of the charge channel was verified across a number of metrics, and radiation testing was performed across the full temperature specification to ensure reliable performance under each combination of operating conditions.

Initial qualification of the channel over temperature was performed standalone. Figure 45 shows the voltage output of the charge channel for an alternating current input. As with the previous measurements, the channel was operated in low gain mode with an input square wave frequency of 1 kHz and amplitude of 2.5 µA. The temperature in the dewar was varied from 100 K (-187 °C) to 343 K (70 °C). Under these conditions, the channel exhibited no sign of signal degradation across the measured range. This was verified for all settings of the channel up to frequencies of 5 kHz.

Further qualification was performed with the channel attached to the remote sensor interface's ADC. These measurements focused on validation of the noise and resolution of the channel both across temperature and under radiation. Figure 46 depicts the 8-bit calibration codes (in decimal) necessary to center the output of the charge channel across temperature. The switched capacitor VGA exhibits a slightly negative offset drift across the full temperature range, spanning a maximum of 7 steps in high gain mode. This represents offset drift of 2.7% of the 8-bit calibration range.

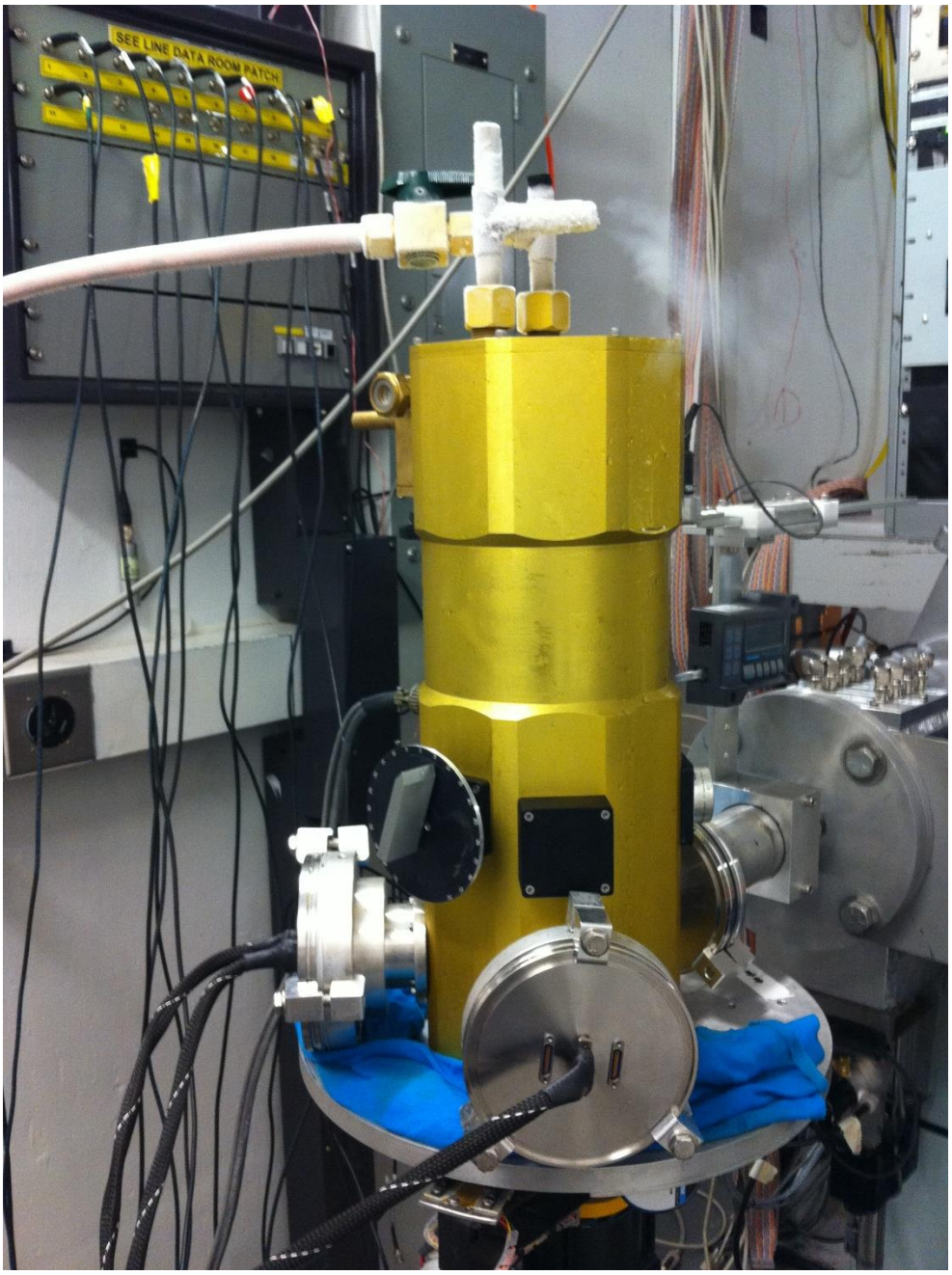

Figure 44: The custom nitrogen dewar used the measure the RSI under simultaneous cryogenic and radiation conditions.

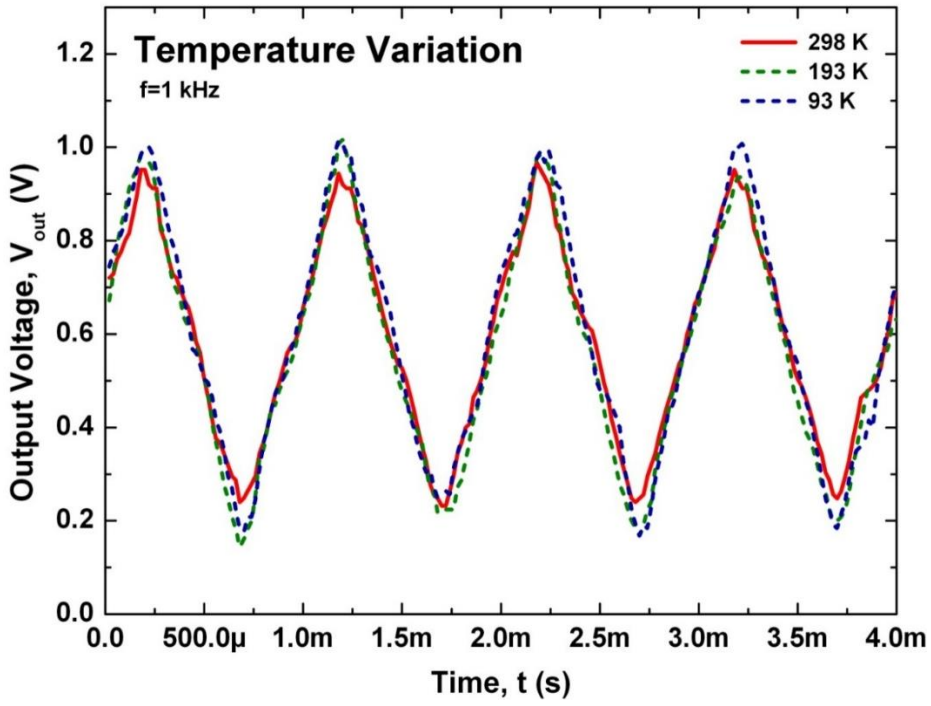

Figure 45: Output voltage vs. time for a square wave input at temperatures from 93 K to 298 K.

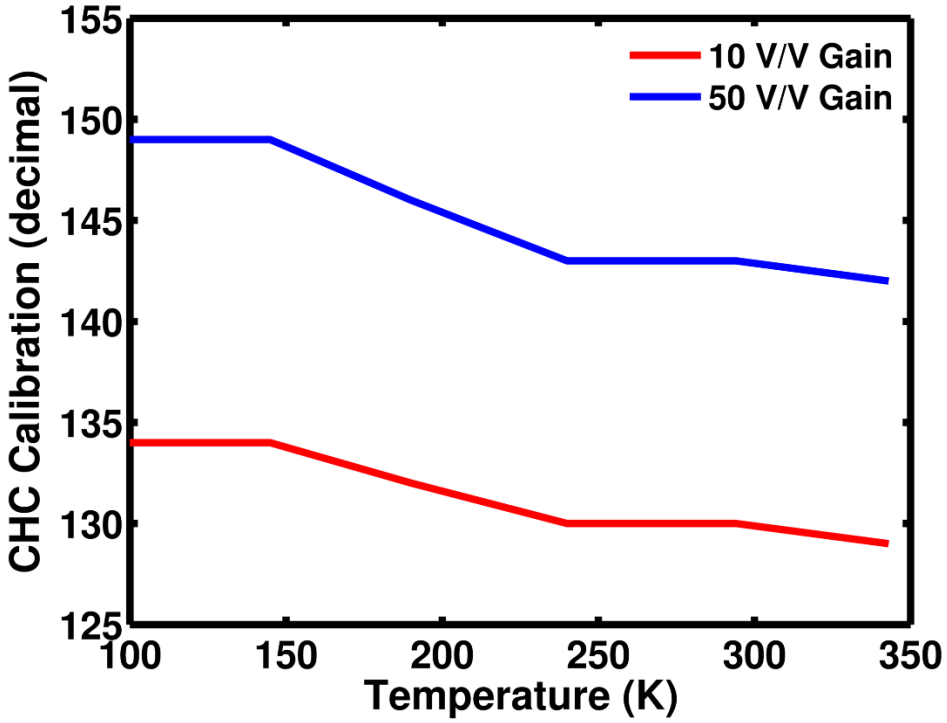

Figure 46: Calibration code (in decimal) used to center the charge channel output across temperature for both high and low gain settings [42].

Effective charge amplification for modern piezoelectric sensors typically requires resolution on the order of pico-Coulombs. This level of resolution is highly dependent upon the input impedance of the system and quality of the analog-digital conversion. The resolution of the charge channel was characterized as a function of temperature by inputting an AC current source of fixed amplitude and converting that current to integrated charge. To determine the change in charge over time (ΔQ), the input current amplitude was integrated as:

$$\Delta Q = \int_0^{\frac{1}{2f}} A\cos(2\pi f t)dt = \frac{A}{\pi f} \tag{6}$$

This result was used to calculate channel resolution using (7).

$$Resolution\left(\frac{Q}{LSB}\right) = \frac{\Delta Q}{\Delta LSB} \tag{7}$$

Similar to the previous measurements, temperature was varied from 100 K to 343 K inside the dewar. Figure 47 plots the resolution for multiple temperature points using both gain configurations. In the low gain setting, the minimum detectable charge amplitude remains below 0.6 pC/LSB with some variation across temperature, while in high gain this value drops to a steady 0.1 pC/LSB [42].

The charge channel was lastly characterized for noise performance and sensitivity, with the results shown in Figure 48. For these measurements, the channel input was shorted internally to a DC reference voltage, and ADC samples were taken at the output for approximately 5 seconds. The RMS noise was taken as the standard deviation of the

AC coupled output, and sensitivity (or input referred noise floor) was calculated by multiplying the RMS noise by the channel resolution. The RMS noise varied from 10-30 LSBs from 100 K to 343 K, and the RMS sensitivity remained roughly constant around 10 pC for the low gain state and 2 pC for the high gain state [42].

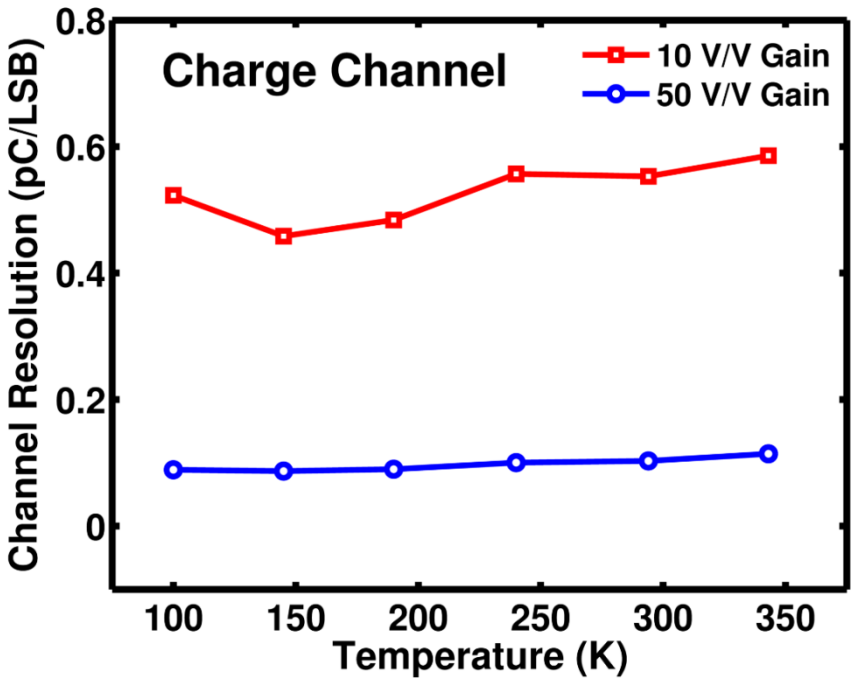

Figure 47: Charge channel resolution (pC/LSB) plotted against temperature from 100 K to 343 K [42].

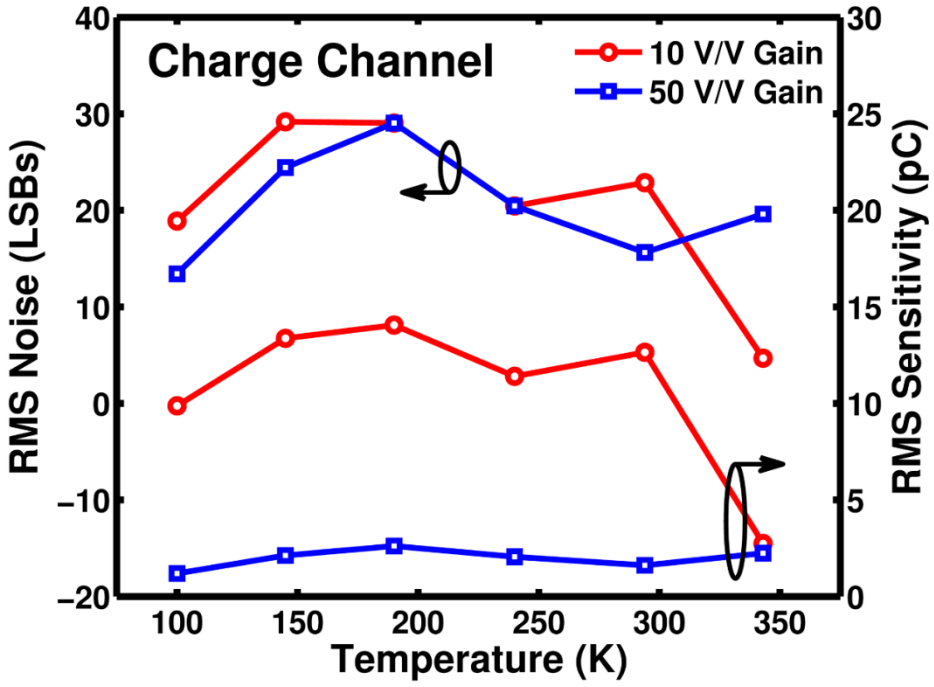

Figure 48: Charge channel noise (LSBs) and sensitivity (pC) as a function of temperature from 100 K to 343 K [42].

4.5 Summary

This section has described the design and measurement of a programmable, charge amplification channel for use as a piezoelectric sensor front-end in extreme environments. As a part of the 16-channel remote analog sensor interface shown in Figure 49, the channel was designed to be fully monolithic (with the exception of the front-end feedback) and to operate reliably in the environmental conditions present on the lunar surface. These conditions include temperatures ranging from -180ºC to 120ºC and ionizing radiation exposure not to exceed 100 krad(SiO2) over a complete mission cycle.

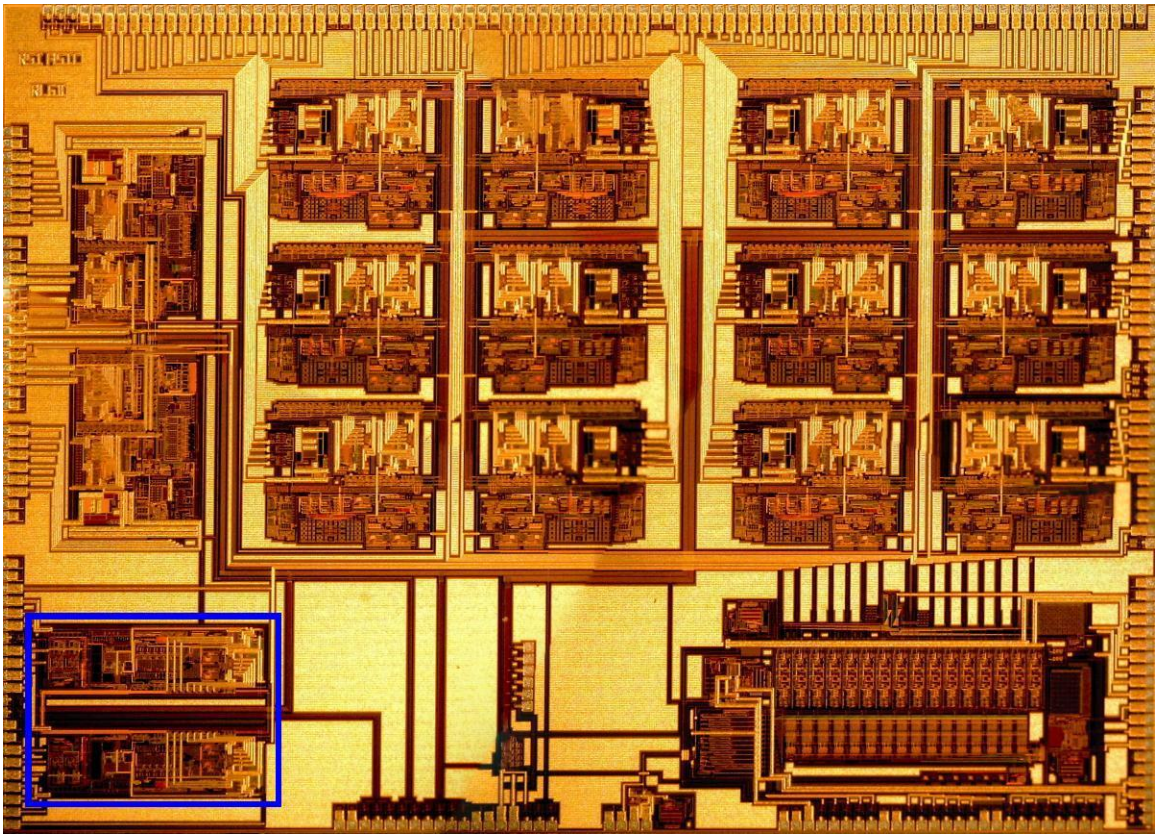

Figure 49: Fully integrated, 16-channel analog remote sensor interface with two charge channels highlighted (bottom left).

The channel was designed to amplify charge signals as small as 200 pC up to frequencies of 5 kHz using two programmable gain states, offset calibration, and programmable filtering. Characterization of the circuit has proven its basic functionality in all respects.

The charge amplification channel, and the entire remote electronics unit described, stands to offer significant advantages to mission engineers seeking to reduce payload, power consumption, and ultimately cost, while enjoying the benefits of a temperature and radiation hardened BiCMOS technology. The unprecedented modularity of the solution will ultimately provide valuable flexibility in the placement of sensors and sensor interfaces to monitor all manner of systems critical to the health of a mission.

CHAPTER V

HEALICS RECEIVER CHAIN

5.1 Introduction

A conceptual block diagram of the HEALICS receiver chain developed at Georgia Tech in collaboration with Northrop Grumman is shown in Figure 50. The complete receiver is designed to cover the X-band (8-12 GHz) and Ku-band (12-18 GHz) frequency ranges. A wideband LNA [43] amplifies an input that switches between the RF signal and an amplitude-locked test source [44]. The output is fed to a wideband mixer [45], an ADC, and is finally analyzed by a baseband processor (not included in the design). The processor determines whether the gain, linearity, and noise of the amplified test signal is within specification, and modifies the bias points of the various blocks in the receiver chain in a feedback process that "heals" the receiver's critical parameters.

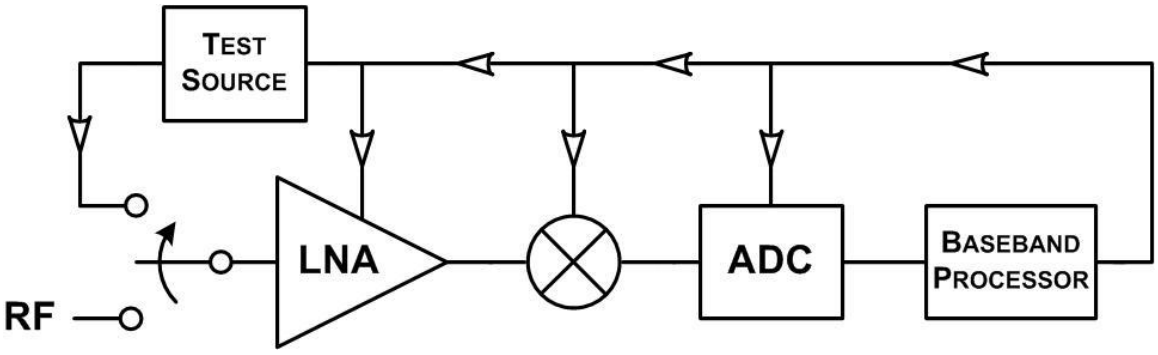

Figure 50: Conceptual block diagram of a self-healing receiver chain.

The self-healing capability is designed to increase yield to above 95% where the aggressive design specifications would typically cause a much lower resulting yield. While this represents the main cost driver, it comes with the additional advantage of allowing the receiver to extend its environmental operating ranges to previously impossible specifications by adjusting for performance deviations due to temperature swings and radiation damage.

5.2 Digital-Analog Conversion

Bias to the receiver blocks is provided by multiple 8-bit digital-analog converters (DACs) that receive incremental adjustments from the baseband processor. These DACs cannot benefit from the healing process, and thus must be designed carefully to maintain consistent performance across temperature. To achieve this stability, the exponential curvature-compensated bandgap reference described in Section 4.3.4 was designed in the more advanced Jazz SBC18 technology, which incorporates a 200 GHz HBT into a 0.18 µm CMOS platform. Two DAC variants were produced (voltage and current), differing only in their output stage circuits.

For each variant, the three most significant bits are first converted into a seven bit thermometer code representation as described in Table 2. This has the effect of reducing switching glitches by preventing bits D_5 and D_6 from pulling down the output when switching to 0 as the input binary code increases (or vice versa for decreasing binary code). The conversion was implemented with custom logic gates designed to prevent single-event latch up and custom driver and delay cells to further reduce glitching and improve speed. The logic used to implement the conversion in is shown in Figure 51, with bit C_3 obtained directly from D_7. The logic was simulated, and remained

Table 2: Thermometer Code Logic Table

Binary			Thermometer Code						
D_7	D_6	D_5	C_6	C_5	C_4	C_3	C_2	C_1	C_0
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

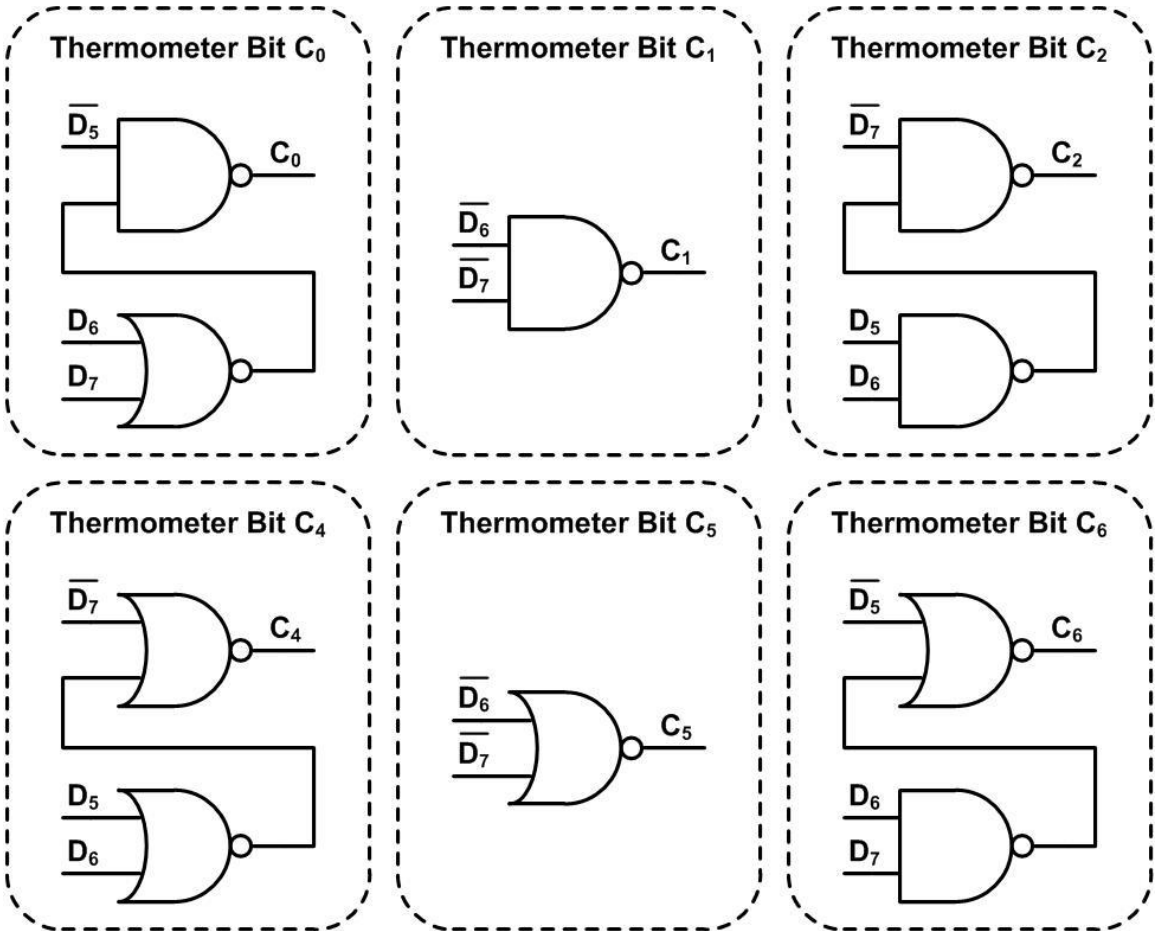

Figure 51: Schematic diagram of the digital logic used in the thermometer conversion.

operational, across a temperature range from -180ºC to 120ºC.

Following the decoding logic, 12 bits are provided to the DAC core. The core is based on an R-2R resistor ladder design with 7 thermometer bits accounting for the MSBs of the digital input. Figure 52 depicts the entire circuit, which is shared between the voltage and current DAC implementations. The core divides a reference current (I_{ref}) between two outputs (i_p and i_n) depending on the state of twelve digitally controlled switches. Branch current magnitudes are controlled by multiplying the base device size used in the 1X switches. Careful layout techniques were used for both the CMOS and resistors to ensure good matching and improve the linearity of the DAC. These techniques include symmetric metal routing and the use of dummy devices to reduce edge effects.

The differential currents produced from the core are then converted to the appropriate voltage or current, depending on the needs of the circuit. Two output stages were designed to satisfy this conversion. The voltage DAC utilizes a two-stage opamp with resistive feedback to convert i_p and i_n into a voltage output, while the current DAC

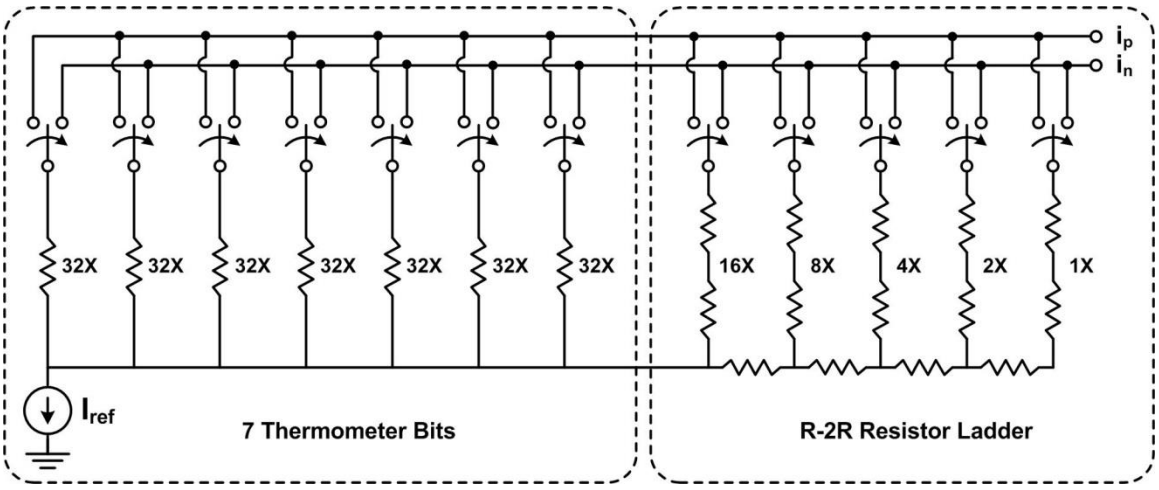

Figure 52: Schematic diagram of the DAC core.

utilizes current mirrors to multiply its inputs to useful levels. These stages are described in the following sections.

5.3 Voltage DAC Output Stage

Figure 53 depicts a simplified schematic of the output stage. Input currents i_p and i_n from the DAC core are applied to well-matched resistive dividers, producing an output voltage proportional to the difference between them. Voltages v_p and v_n at the input of the amplifier vary as:

$$v_p = V_{DD} - i_n R_p \tag{8}$$

$$v_n = V_{out} - i_p R_f \tag{9}$$

Setting $v_p = v_n$ and solving for V_{out} yields:

$$V_{out} = V_{DD} - i_n R_p + i_p R_f \tag{10}$$

The resistors were sized to provide an output swing from 1.0 V to 3.8 V at a resolution of 10.9 mV (Figure 54). This range provides all of the flexibility necessary to bias and heal the RF blocks in the receiver chain at a maximum power draw of 8.8 mW.

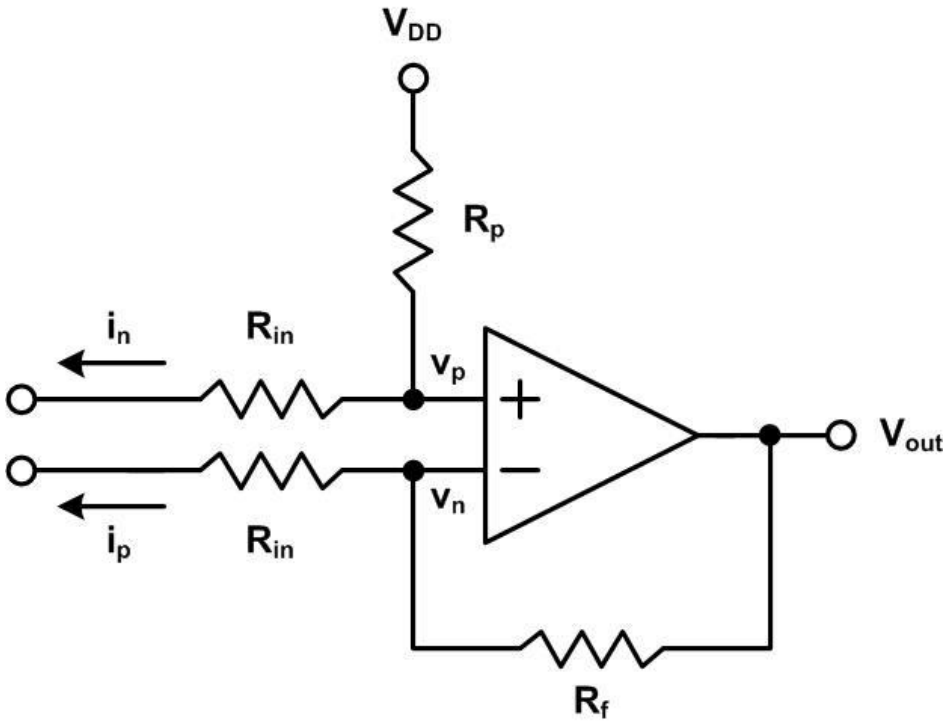

Figure 53: Simplified output stage for the HEALICS voltage DAC.

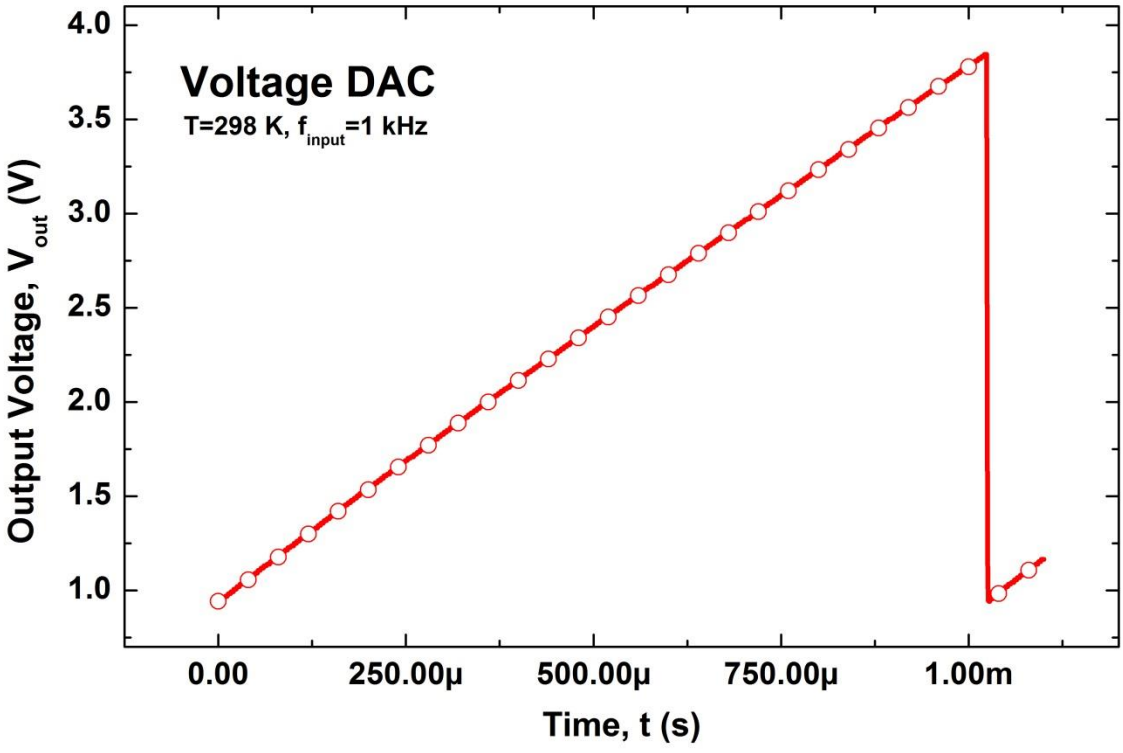

Figure 54: Simulated output of the voltage DAC with a ramped input code.

5.4 Current DAC Output Stage

The current DAC achieves conversion of the differential inputs through the use of multiple current mirrors, depicted in Figure 55. The currents are fed with opposite polarity to a common node where a DC bias current (i_{Bias}) is simultaneously applied to center the mid-range output. This current is multiplied by a subsequent mirror, providing a full-scale output range from 1.5 mA to 9.0 mA. The entire current DAC, including the core circuits that are common between the DAC variants, consumes 4.0 mW (not including the output power provided to the relevant receiver block). A simulated ramp output is shown in Figure 56. The current DAC can achieve a resolution of 29.3 uA when utilizing all 8-bits at its input.

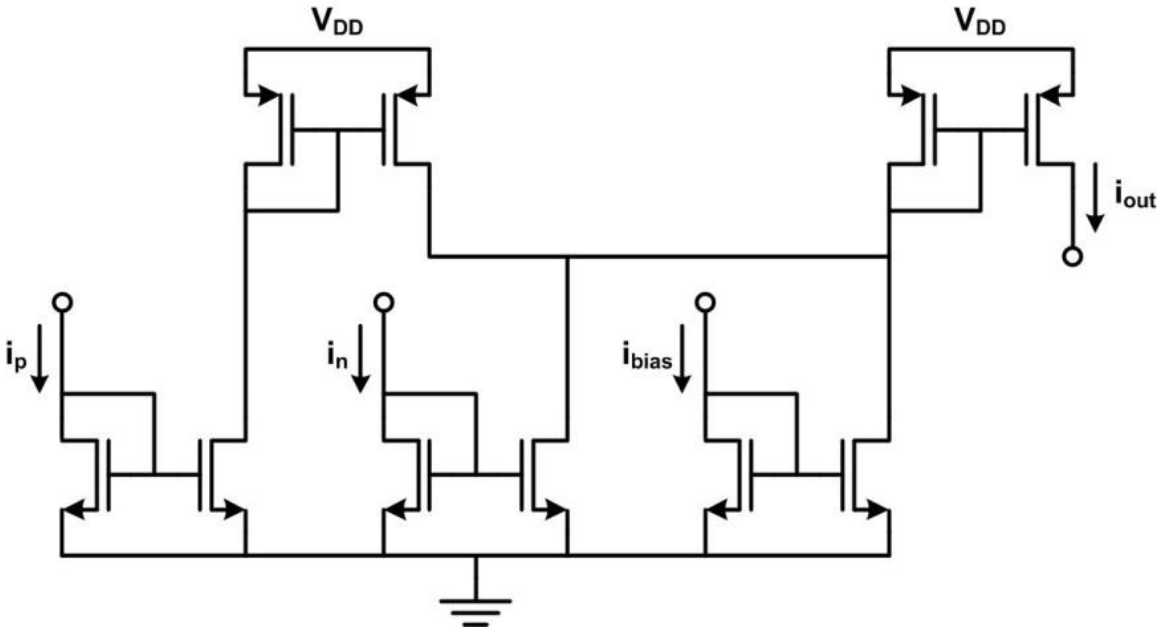

Figure 55: Output stage schematic for the HEALICS current DAC.

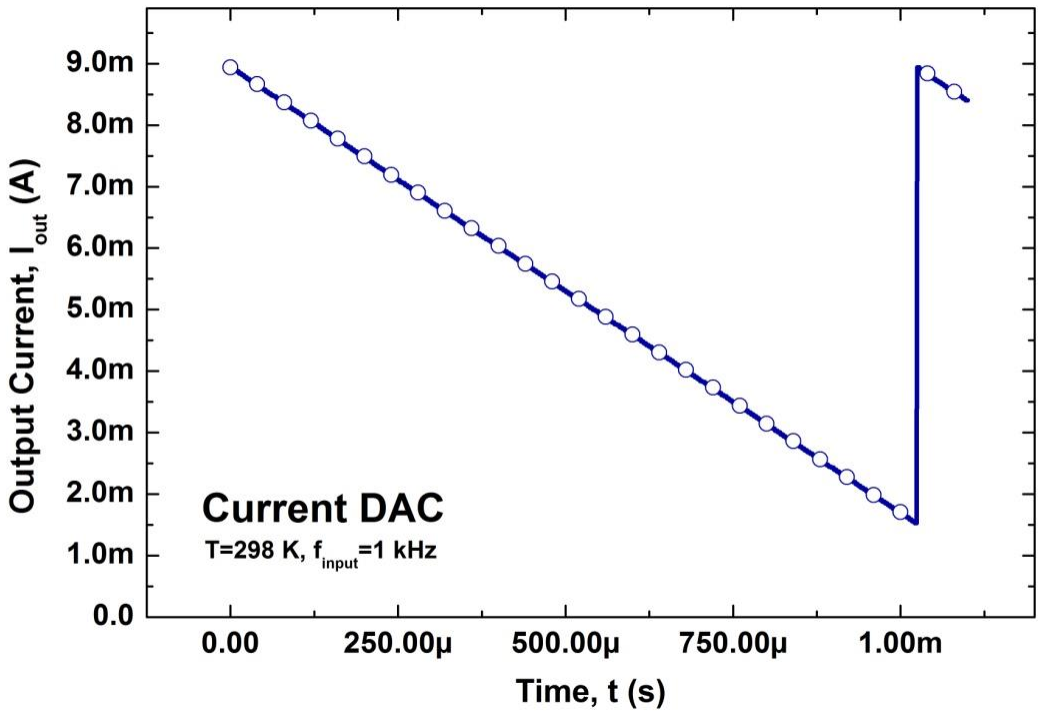

Figure 56: Simulated output of the current DAC with a ramped input code.

5.5 DAC Measurement Results

The voltage and current DACs were measured standalone to verify their functionality prior to integration with the full RF chain. Figure 57 depicts measured results from the voltage DAC. Input codes were stepped from 0 to 255 at a frequency of 1 MHz while the output voltage was measured with an oscilloscope. Table 3 summarizes the results of the measurements. Similarly, Figure 58 depicts measured results from the current DAC, and Table 4 summarizes the performance parameters. The output current was driven across a 100 Ω external resistor. The resistor voltage was measured with an oscilloscope and subsequently converted to current. Note that the slope of the current is reversed with respect to the simulation results due to a reversal of the input code in the final design.

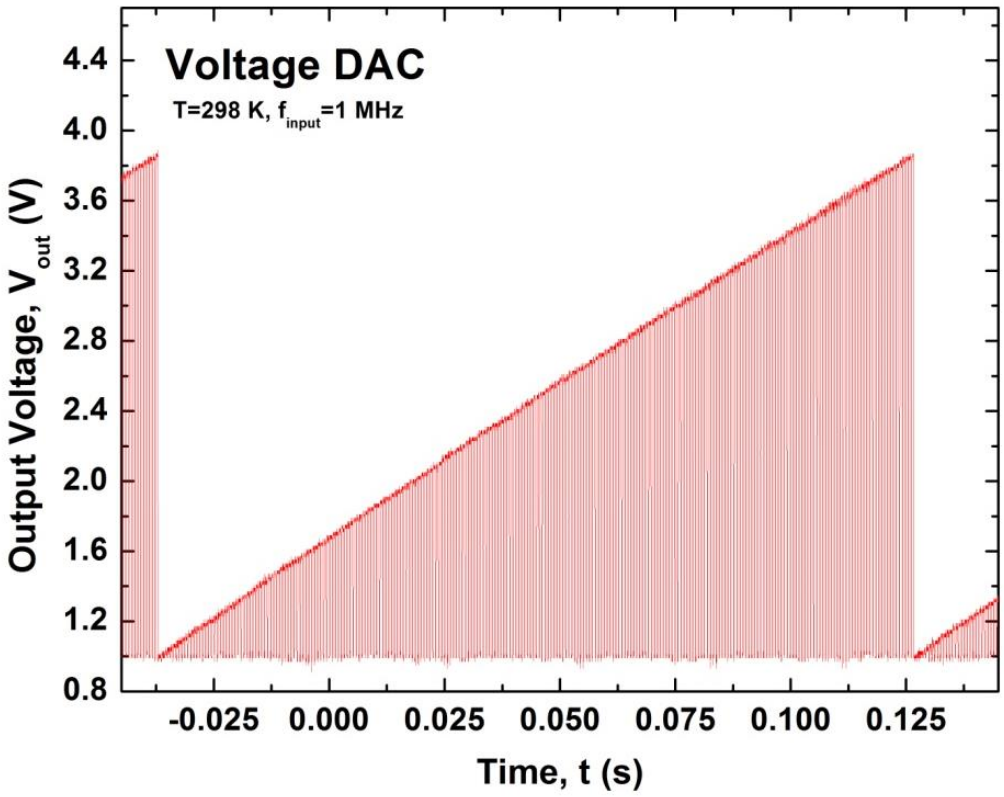

Figure 57: Measured performance of the voltage DAC with stepped input code at a frequency of 1 MHz.

Table 2: Summary of Voltage DAC Characteristics

Output Range	1.0 V – 3.9 V
Step Size	11.3 mV
Quiescent Power	8.8 mW (max)

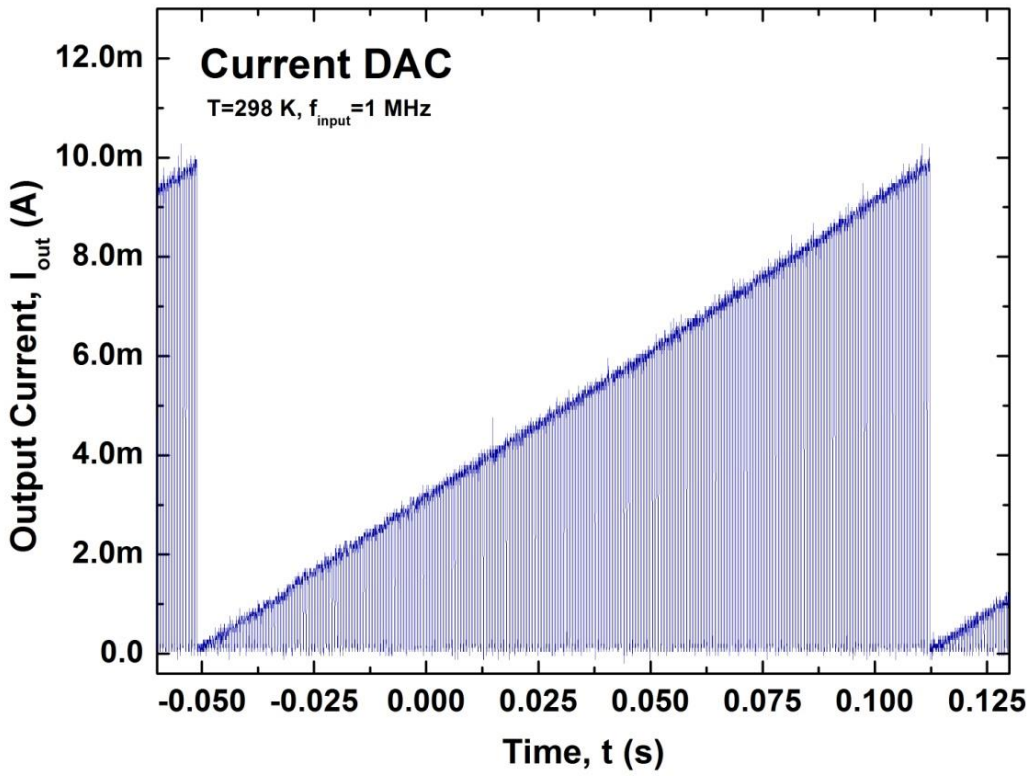

Figure 58: Measured performance of the current DAC with stepped input code at a frequency of 1 MHz.

Table 3: Summary of Current DAC Characteristics

Output Range	0.0 mA – 10 mA
Step Size	39.1 uA
Quiescent Power	4.0 mW (excluding output)

5.6 Receiver Chain Healing Results

The full RF chain was implemented on a 4.3 mm x 2.7 mm die, shown in Figure 59, and bonded to a printed circuit board for characterization. DC bias was delivered through SMA connectors and RF signals were measured by directly probing the RF pads on the die. Baseline results were measured, including gain and image rejection ratio, then healing was performed by adjusting the bias conditions provided to the LNA and mixer by the various voltage and current DACs in the design. In total, 15 DACs we're utilized.

Figures 60 and 61 show the measured gain pre- and post-healing at 10 GHz and 16 GHz, respectively. Each of the measurements described in this section were performed by Duane Howard, Prabir Saha, and Subu Shankar at the Georgia Institute of Technology and are pending publication. At 10 GHz, a gain improvement of approximately 10 dB was achieved, while an 18 dB improvement was achieved at 16 GHz. This represents a very significant delta in performance and validation that the system gain can be effectively improved if the system is operating out of specification. A similar result was obtained for image rejection, which showed a 12 dB improvement post-healing at 10 GHz and 18 GHz. The results of these measurements are shown in Figures 62 and 63.

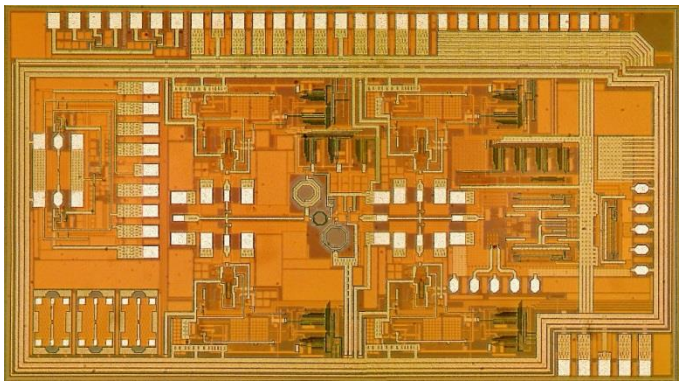

Figure 59: The full Healics receiver chain designed in the Jazz SBC18 SiGe platform.

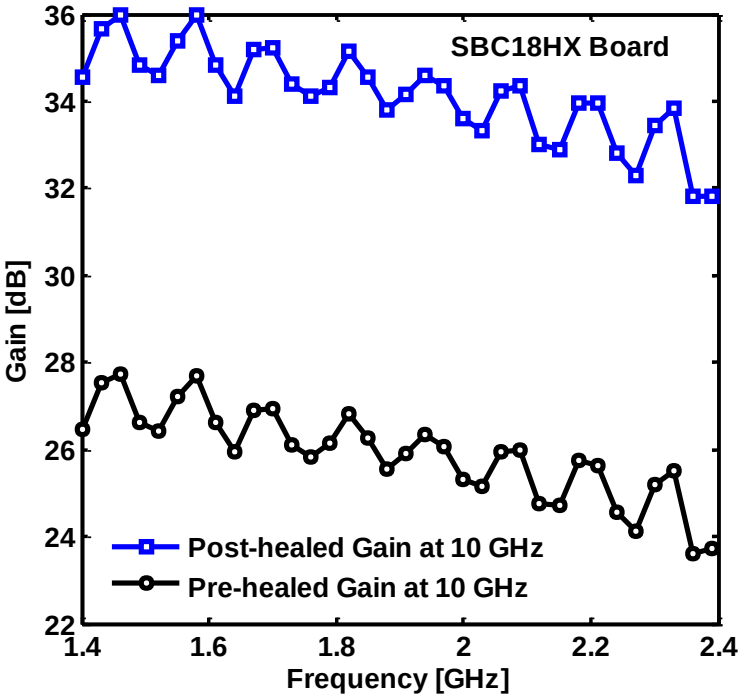

Figure 60: Measured pre- and post-healed gain for the Healics RF chain at 10GHz.

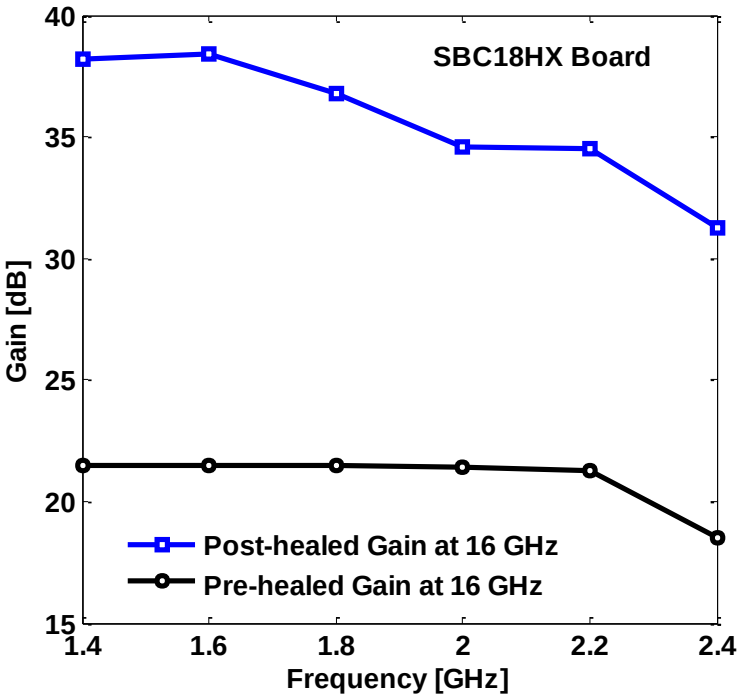

Figure 61: Measured pre- and post-healed gain for the Healics RF chain at 16GHz.

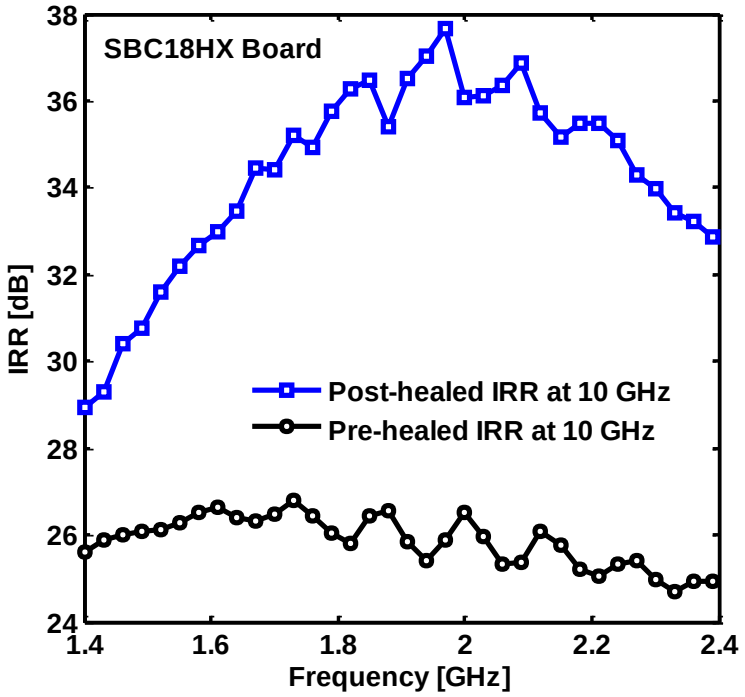

Figure 62: Measured pre- and post-healed IRR for the Healics RF chain at 10GHz.

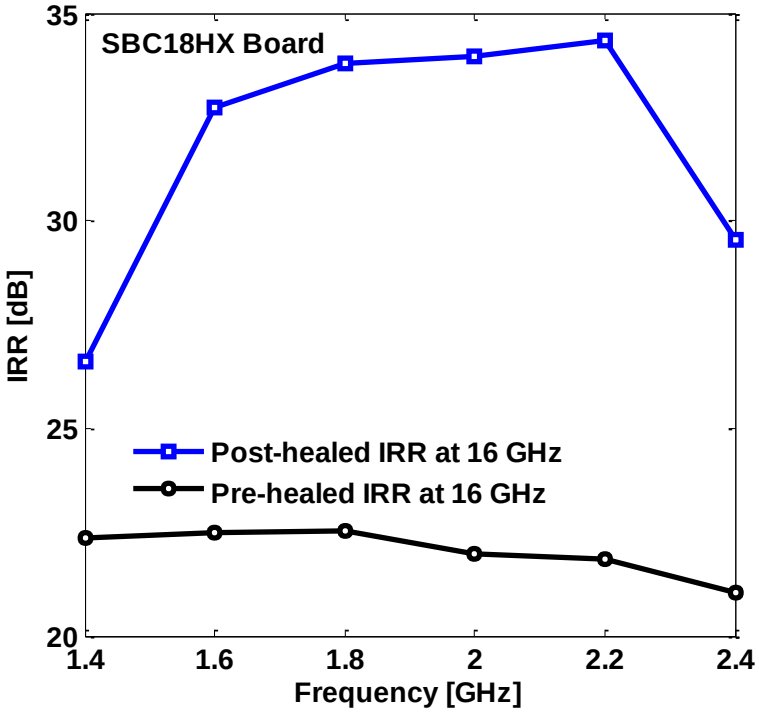

Figure 63: Measured pre- and post-healed IRR for the Healics RF chain at 16GHz.

5.7 Summary

This chapter described the design of the supporting analog circuitry necessary to provide variable bias to a self-healing RF receiver. Specifically, two flavors of digital-analog converters were fabricated, each with design techniques to make them stable in a variety of environmental conditions. The receiver was designed to operate from 8-18 GHz and be able to heal its relevant performance metrics based on measurements taken at its output by a baseband processor. The capability to heal enables the receiver to improve its own chip-to-chip yield as well as improve its ability to maintain itself within specification during changes in environmental conditions such as ambient temperature and background radiation.

The DACs performed well, with good linearity, low power consumption, and sufficient resolution to allow for fine control of tuning parameters. A total of 15 DACs were used to bias the entire receiver chain, which, using the proper algorithms, was able to heal its gain by as much as 18 dB and its image rejection ratio by as much as 12 dB. Ongoing measurements of the receiver chain will seek to validate its ability to heal other parameters, such as noise figure, however the existing data shows that the analog bias circuitry was effective in providing control of the individual circuit blocks to a degree that allowed a wide range of parameter control.

CHAPTER VI

ARGONNE X-RAY DETECTOR

6.1 Introduction

The major category of chemical reactions which can be explored with ultra-fast detectors is studied using pump-probe experiments [11]. A chemical trigger is applied that typically consists of a laser pulse, which can be made very short (in the 100's of femtoseconds range) using titanium sapphire systems. Alternatively, pulsed electric or magnetic fields can be used as the trigger, although this experiment will focus solely on laser stimuli. The pump initiates the chemical reaction, and at a later time the rearrangement of the electrons on the molecules is probed with an x-ray photon, revealing the electrical state of the sample. The samples in pump-probe experiments scatter only weakly, even when probed with a very bright x-ray source, and thus for the experiments of interest (photon counting) total flux is an important concern.

At x-ray synchrotrons, ultra short pulses are created by slicing out short time durations of the overall pulse. In this manner only a fraction (5% or so) of the total x-rays are used. It is difficult to process two photon hits in a single pixel if they arrive within picoseconds of each other: a fact that contributes to an additional loss of flux. Detectors have a path to mitigate this loss by making the pixel sizes smaller, and hence having more independent pixels per area, but this gain comes at an engineering cost in complexity. At present we consider pixel sizes of a few hundred microns as a compromise. Ultimately to regain flux count, experiments can be averaged by repetitively pulsing the laser and

collecting many sets of data. The ultra-fast x-ray detector described in this section is the result of an ongoing collaboration between Georgia Tech and Argonne National Labs (ANL) in Chicago, IL.

6.2 System Architecture

The speed requirements of an x-ray detector array with sub-10 ps resolution, as defined by ANL's experimental needs, necessitated the selection of a very high speed SiGe process to provide the foundation for the design. To that end, IBM's 8HP BiCMOS platform proved ideal, boasting a 200 GHz HBT with integrated 0.18 µm CMOS devices. One of the fastest available switching architectures in a bipolar process is the emitter-coupled logic (ECL) inverter, which consists of a resistively loaded differential pair biased near the peak-f_T current density of the HBT. The output of the differential pair, taken from the collectors of the HBTs, is connected to the base of a common-collector device that can drive larger capacitive loads. Previous investigations have yielded gate delays as low as 3.9 ps [10]. This structure forms the basis of the detector's timing chain and is shown in Figure 64.

The pixel architecture is initially triggered by a laser pulse on the pump diode. A high-speed trans-impedance amplifier converts the diode response to a voltage, which then feeds a comparator. The complete detector chain is shown in Figure 65. If the response is strong enough, the comparator propagates a rising edge into the ECL inverter chain, beginning the timing sequence. The length of the inverter chain (27 stages) was chosen based on the size of the timing window desired for the experiment. In this case, a window of approximately 200ps was desired. A duplicate of the pump diode detector chain waits for an x-ray photon to strike the probe diode and initiate the latching sequence. When that

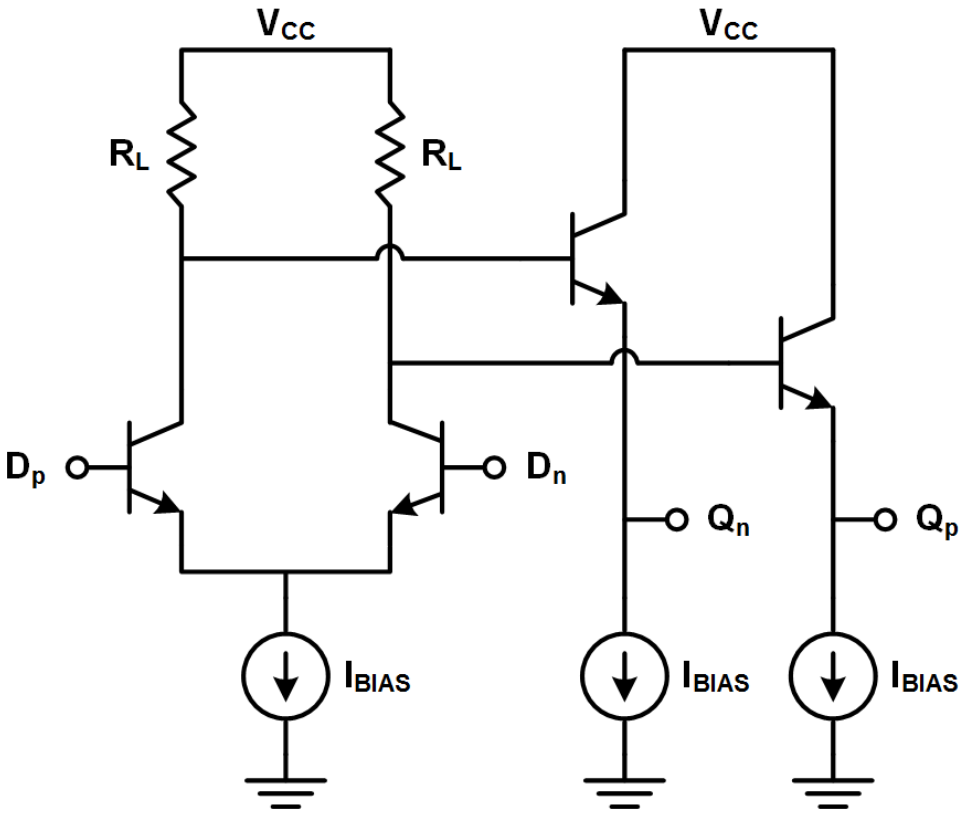

Figure 64: Simplified emitter-coupled logic inverter.

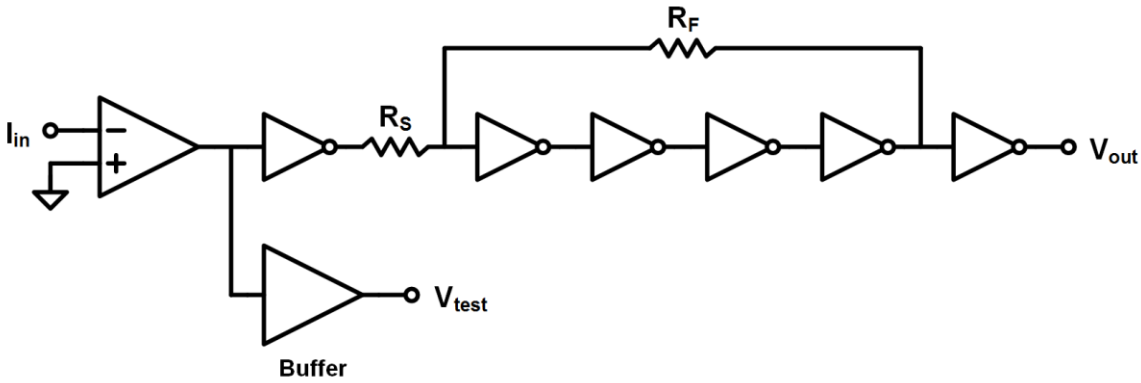

Figure 65: Block diagram of the transimpedance amplifier and comparator chain.

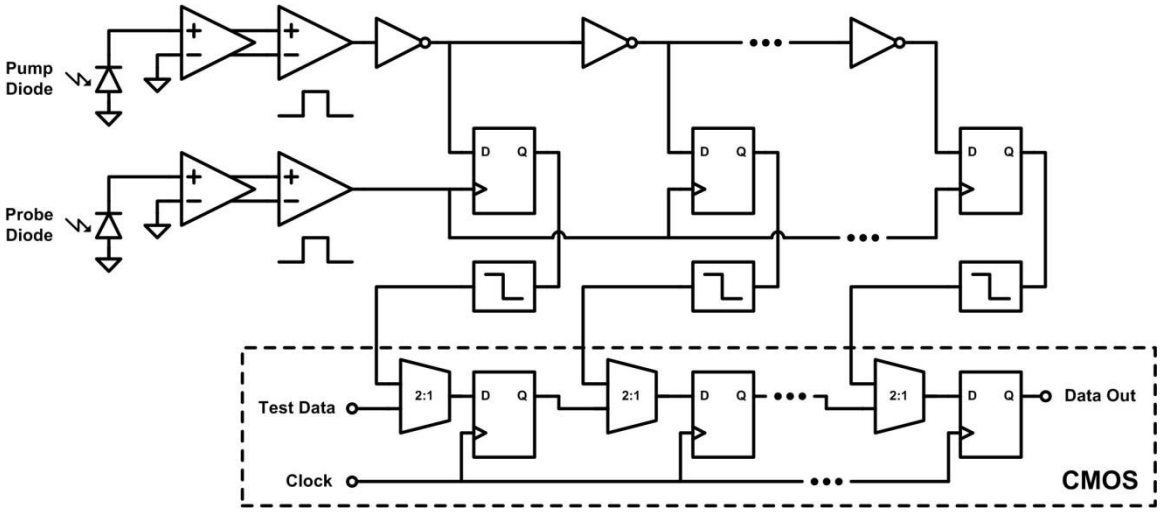

Figure 66: Block diagram for the detector pixel.

event is detected, the D-flip-flops (DFFs) latch in the current outputs of the inverter chain. This snapshot quantifies the time that has passed between the initial laser pulse and the probe signal with a resolution equal to the delay of the individual inverter stages.

In order to reduce pixel area and power consumption, the outputs of the DFFs were level shifted, multiplexed, and connected to CMOS DFFs that can be clocked out much slower than the bipolar-based logic. These circuits are comprised of digital cells from the IBM design kit. The full pixel was copied to form a 1x4 array, allowing spatial information to be gathered about the x-ray photons scattered by the sample. Initial simulations indicate power consumption on the order of 300 mW per pixel, which necessitated careful supply routing and thermal management.

Layouts for the individual timing stage, the 27-gate chain, and the entire 4-pixel array are shown in Figure 67, 68, 69, respectively. The timing stage includes the ECL inverter, probe latch, level shifter, and CMOS readout circuitry. It was designed in a manner such that stages could be laid side-by-side with minimal necessary connections between to reduce chip area for large timing chain implementations. Despite this, the 27-stage pixel

with the laser/x-ray detector chains, biasing circuitry, and power routing still occupies a substantial area, covering 0.3 mm x 0.3 mm. Diodes were included in the 4-pixel array to allow for system verification with a tunable laser source, which will provide the pump and probe pulses for timing calibration. The final designs will include an RF pad for connection to a diode specifically designed to detect x-ray photons.

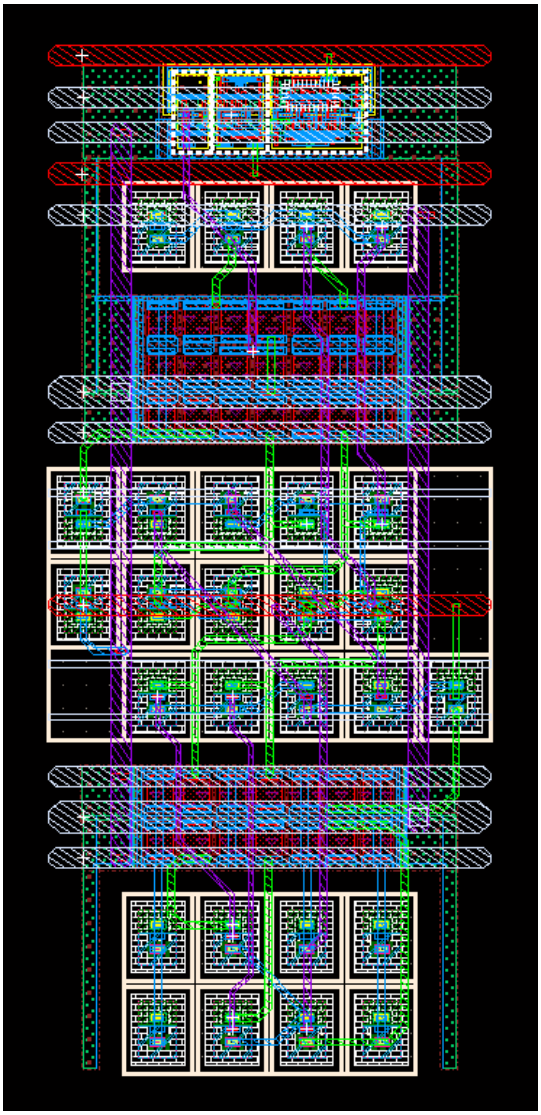

Figure 67: Layout of the ECL inverter, latch, and CMOS readout circuitry for one timing stage.

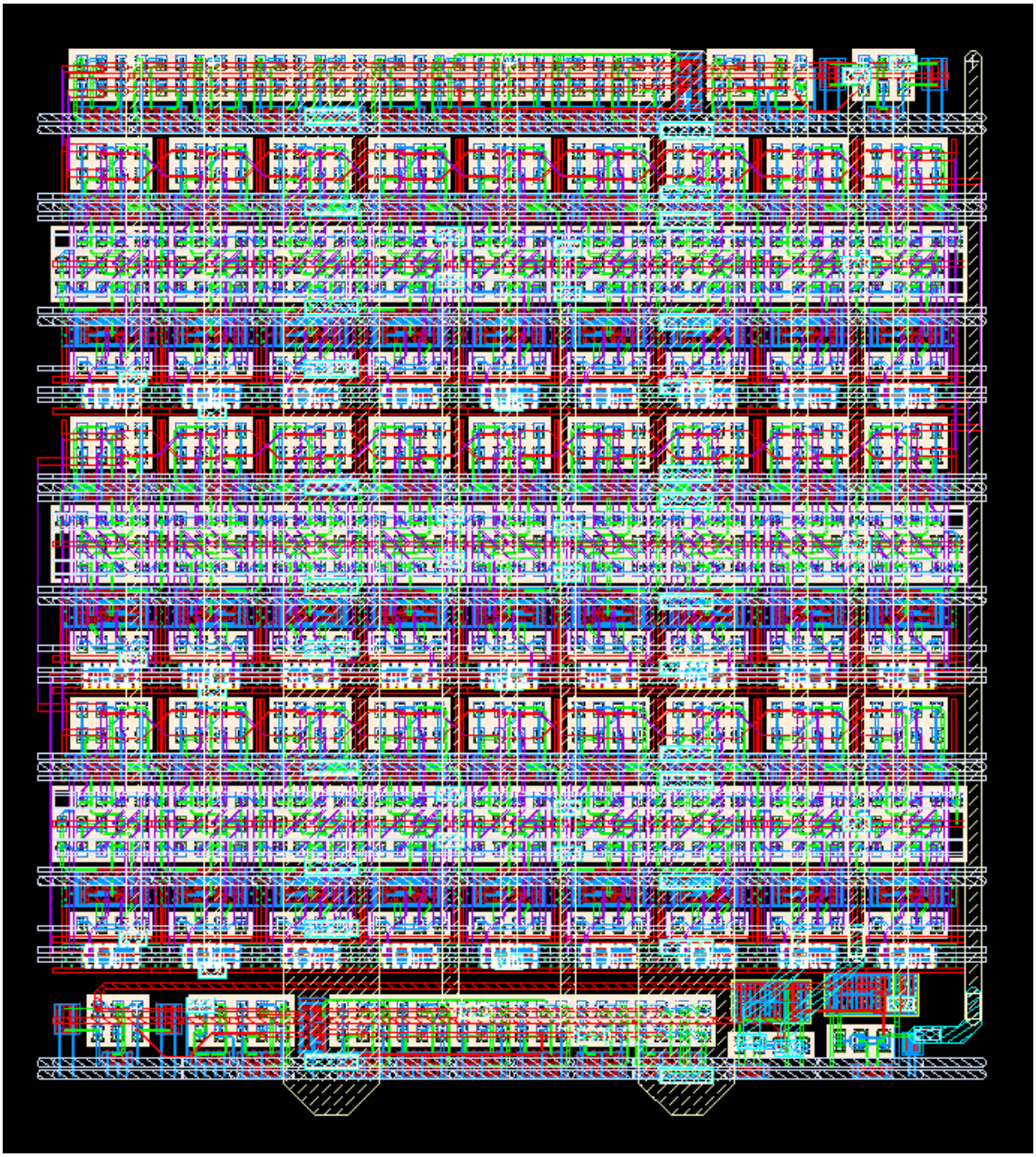

Figure 68: Layout of a 27-stage pixel capable of capturing timing data in a 200 ps window.

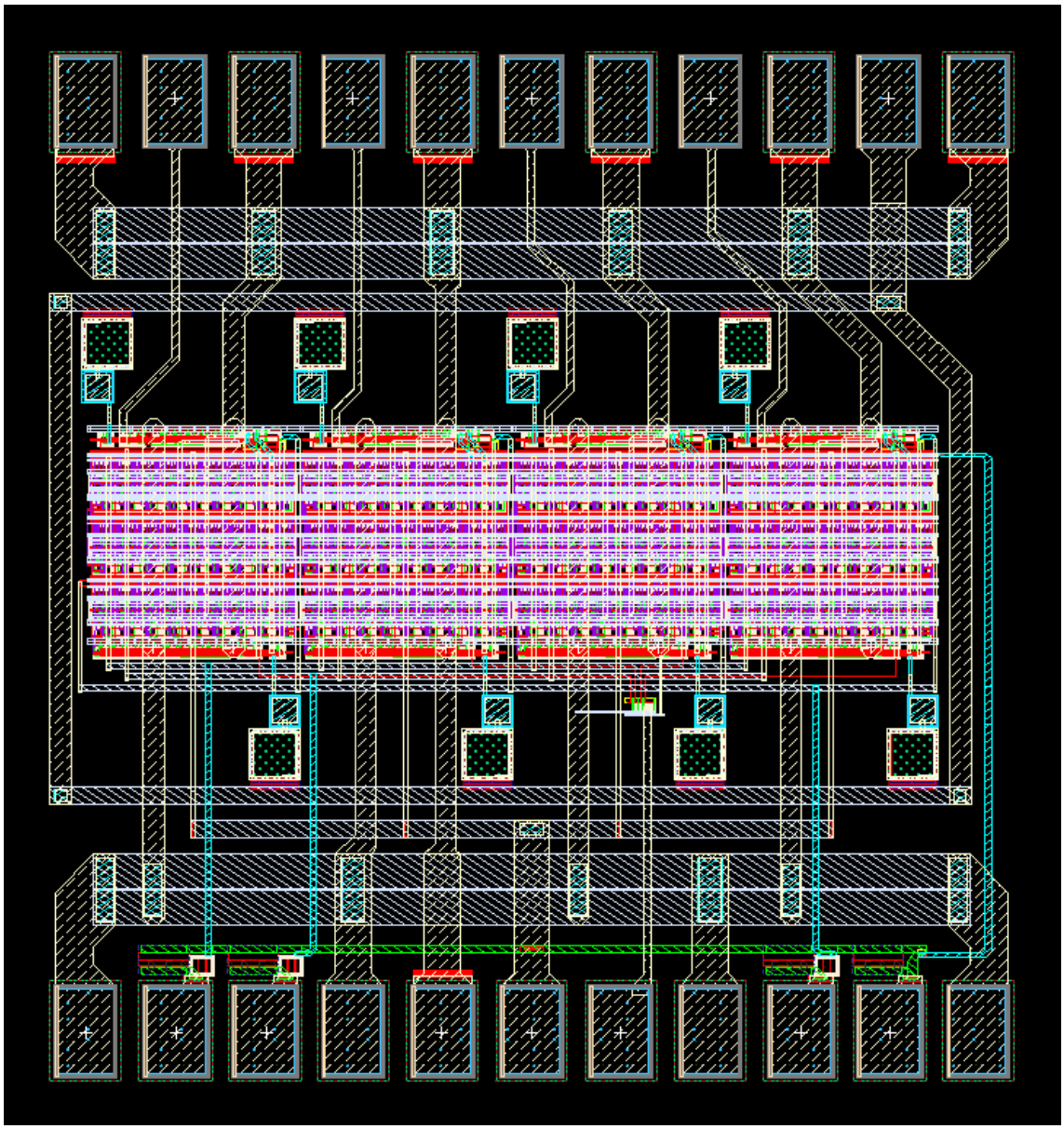

Figure 69: Layout of the 4-pixel ultrafast x-ray detector, including start and stop pulse diodes, biasing, and digital I/O.

6.3 Simulation Results

The x-ray detector was designed as a completely self-contained system. Input and output signals were minimized such that the detector could be measured with a minimal amount of external hardware. For instance, the entire pixel array and all of its sub-blocks are current biased with a single mirrored current source. Digital I/O pads provide Schmitt triggering and level shifting of digital signals and power is distributed through a network of interconnects designed to handle the significant power consumption of the system and its many sub-systems. The simulations presented in this section were performed as if they were real-world measurements. No ideal sources were used with the exception of the highest level inputs, and no sub-systems were simulated apart from the main system. This was done in order to validate the operability of the detector with a high degree of confidence. Parasitic extracted simulations were performed on sub-systems to ensure the layouts were optimized for speed, however the full systems were not able to be simulated in this manner due to their size.

Figure 70 depicts two exponential current pulses designed to simulate a photon strike on the interface diodes. The first pulse indicates the pump strike, which is typically induced by a laser simultaneous to the excitation of the sample. At the onset of this pulse, the detector will begin timing through the chain of ECL gates as long as the pulse size is sufficient to trip the front-end transimpedance amplifier and comparator. For the purposes of these simulations, a peak pulse current of 200 uA was used. The second pulse, which occurs exactly 24 ps later, is indicative of one or more x-ray photons striking the probe diode from the sample. This pulse will trigger the latches at each delay stage to latch in their current values and stop the timing process.

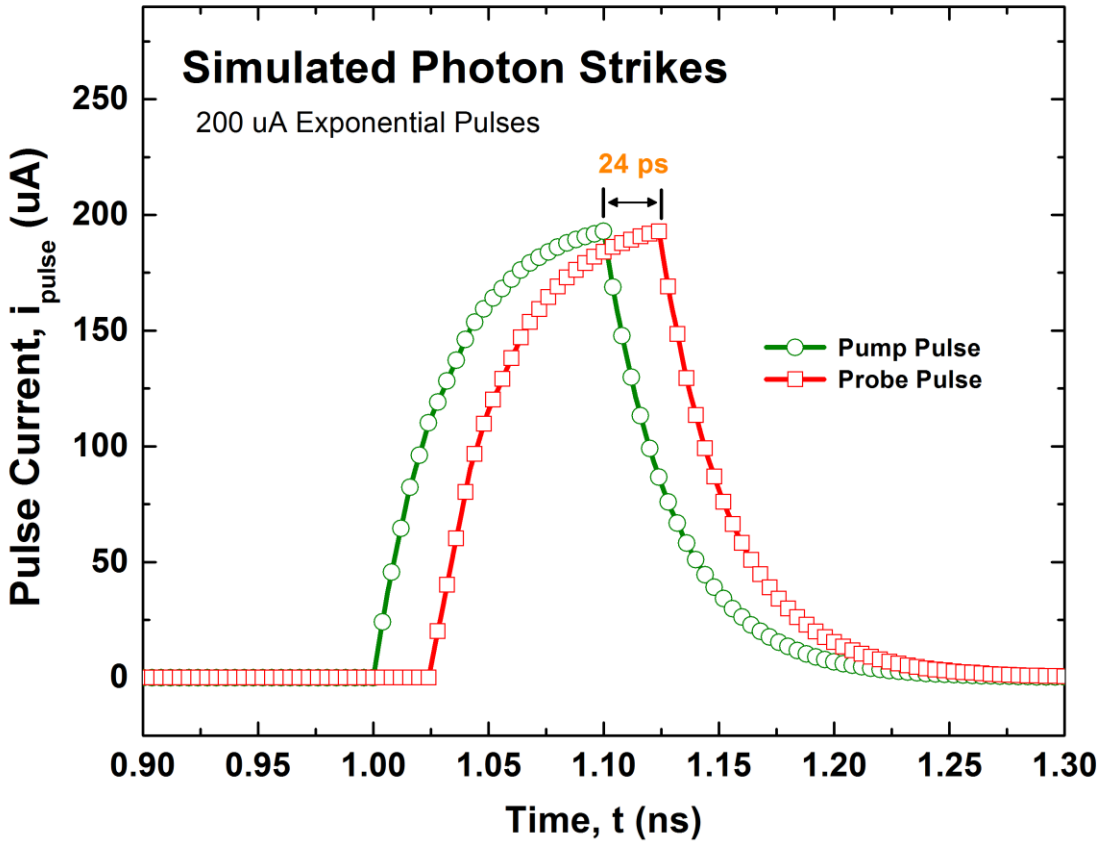

Figure 70: Simulated photon strikes on the pump and probe diodes using 200 uA peak exponential current pulses with a 24 ps delay.

The propagation of the pump pulse through the detector chain is shown in Figure 71. This plot shows the exponential current waveform through the diode, occurring at 1 ns. After some delay, the signal has propagated through the TIA and the series of inverters configured as a high-speed comparator. Once the comparator output is tripped (at roughly 1.1 ns), the ECL stages begin to trigger one-by-one with a stage delay of 6.5 ps. It would be expected that four stages would be tripped before the probe pulse is propagated through an identical detector chain 24 ps later. A pixel with a total of nine stages was used for the purpose of these simulations.

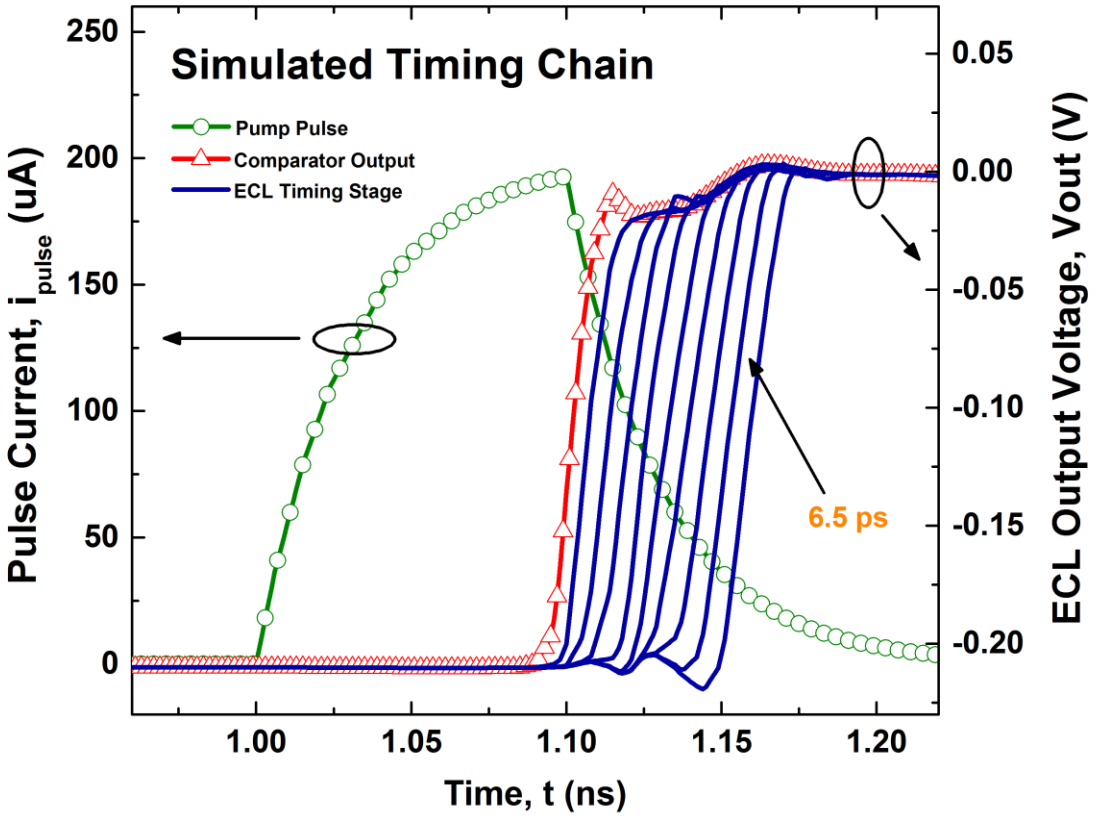

Figure 71: Simulated timing sequence, including pump pulse, comparator trigger, and 9 ECL stages with an average stage delay of 6.5 ps.

Once the probe pulse latches in the current state of the timing chain, each of the latch outputs take on their output voltage levels and hold them until the data can be clocked out of the system. Figure 72 shows the outputs of the nine latches in the system as the latch signal arrives. As expected, four of the nine latches in the chain are triggered within the 24 ps delay. Note that the outputs of the delay stages are inverted prior to arriving at the latch outputs. The final stage of the measurement, which takes a total of ~200 ns, involves clocking out the captured data through the CMOS readout circuitry. Figure 73 describes this process. First, one clock pulse latches in the data from the ECL

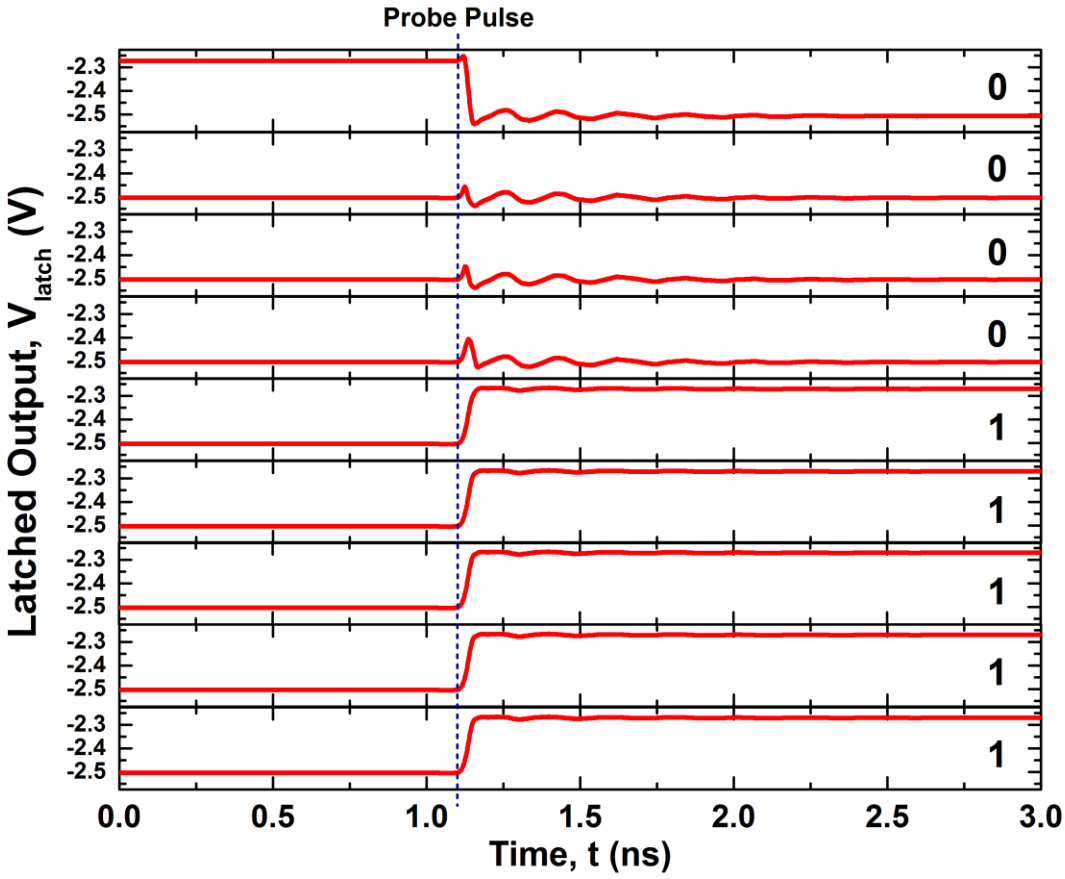

Figure 72: Simulated output of 9 delay stages after a probe pulse (inverted). The pulse occurs 24 ps after the pump pulse, yielding a dataset of "000011111".

to the CMOS latches. The select bit is then changed such that each subsequent clock pulse will move the data one stage down the chain, as opposed to bringing in fresh data from the ECL. The bits are read out in reverse order from a Schmitt-triggered I/O pad at a frequency of 100 MHz. The readout from these simulations (000011111), indicates that the delay between the pump and probe pulses was somewhere between 19.5 ps and 26 ps. This result validates the timing chain for a simulated pulse delay of 24 ps.

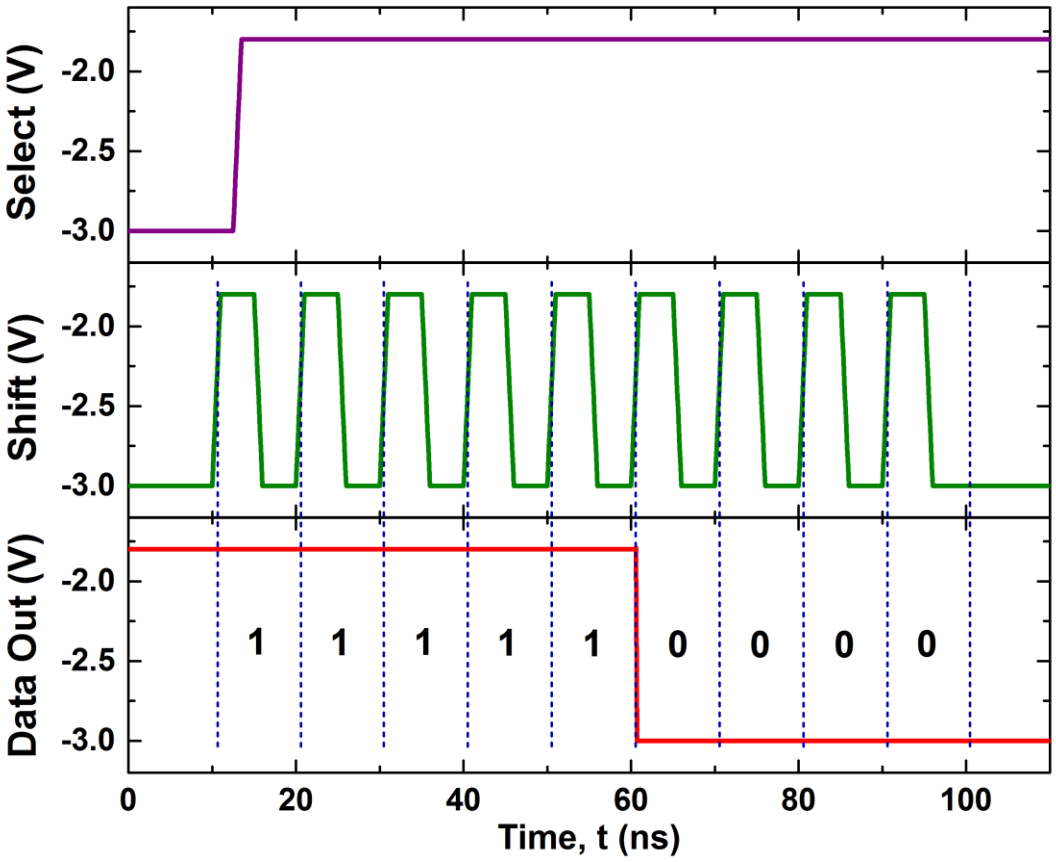

Figure 73: Simulated readout of the detector chain after a 24 ps delay pump-probe stimulus showing the "Select" signal (top), "Shift" clock (middle), and "Data Out" signal (bottom).

6.4 Summary

This chapter described the design and simulation of an ultra-fast x-ray detector built for use in pump-probe experiments. The targeted stage delay of less than 10 ps was achieved using finely tuned ECL inverters, which had a simulated stage delay of 6.5 ps. The system was verified using a 24 ps delay pump-probe series fed into a nine stage pixel. The resulting data indicated a delay between 19.5 ps and 26 ps, consistent with expectations. The final 4-pixel system was taped out, however unexpected funding circumstances precluded the final measurement verification of the system. Despite this,

these findings represent a compelling case for the use of high-speed SiGe technology platforms in ultra-fast photon detection systems. Their low cost enables their consideration as an alternative to expensive beam-line modifications that are currently used to accomplish similar results.

CHAPTER VII

CONCLUSION

7.1 Summary of Contributions

The present research is focused on providing insight into the design of SiGe integrated circuit components for extreme environment systems and sensors. The advantages of advanced SiGe platforms lend themselves well to the requirements of space-based platforms. In particular, they possess significant resistance to radiation and perform optimally at very low temperatures. In addition to these characteristics, they can be utilized at the necessary speeds to be leveraged in both high-precision analog systems and high-speed RF systems. The feasibility of fabricating a sensor interface for space-based platforms was demonstrated, which required the use of custom wide temperature models and robust biasing techniques. A high-frequency RF receiver was also fabricated using similar techniques to demonstrate the feasibility of a system that could both detect and heal its own operating parameters dynamically. Lastly, an ultra-fast x-ray detector was designed and modeled to show that, in the highest performance spectrums, SiGe could be leveraged to provide a low cost alternative to established radiation beam line measurement techniques. The specific contributions include:

1. Investigation of the total-dose radiation tolerance of a third generation complementary SiGe:C BiCMOS technology platform. Tolerance is quantified under proton and X-ray radiation sources for both the npn and pnp HBT, as well as for an operational amplifier built with these devices.

2. Development of a technique known as junction isolation radiation hardening with the goal of improving the SEE sensitivity of the npn in this platform by reducing the charge collected by the subcollector in the event of a direct ion strike.

3. Design of a monolithic charge amplification channel for use as a piezoelectric sensor front-end in extreme environments such as the lunar surface and Mars. Specific contributions included the conception, design, measurement, and final integration of the charge amplifier into a 16-channel remote sensing interface.

4. Development of wide-temperature digital-analog biasing circuits and amplifiers to provide stable references and tuning capabilities to a self-healing 8-18 GHz radar system. These circuits were individually characterized, and subsequently integrated to show a fully functional receiver that is capable of self-healing for both yield and a wide range of environments and conditions.

5. Design of an ultra-fast x-ray detector leveraging the high frequency capabilities of the SiGe HBT in particle physics research. The system achieved sub-10 ps measurement resolution with the goal of providing an alternative to traditionally expensive modifications to the beam line at Argonne National Laboratories.

7.2 Future Work

The research presented in this thesis are the discoveries and results of investigating the use of SiGe BiCMOS technology platforms for various applications related to extreme environments and sensing. Several opportunities for future research exist along each of the major project paths that could further our understanding of the applicability of SiGe to these conditions. They are summarized below.

A fully monolithic charge amplification channel was designed and built as part of a larger remote sensor interface for the lunar surface and Mars. The system was robust against the environmental conditions common to these types of missions, however its architecture was based upon a dated application and was developed simply as a proof of concept. As new mission objectives evolve with far more specific environmental and functional specifications, the opportunity to tailor the building blocks to a task that exists on NASA's road map presents itself. Future robotic and manned missions envisioned by NASA will require hardness to total dose exposures of 5 Mrad and higher. These kinds of requirements have yet to be satisfied for complete electronics systems without significant concessions of weight and power for warm box protection.

A self-healing radio frequency receiver was also demonstrated. Many opportunities exist for the refinement of the diagnostic and healing processes, as well as the study of applications where such capabilities would add value. For instance, the ability of an RF receiver to heal itself during the course of a space mission, which can be specified to last up to 30 years, would be highly invaluable to the exploration community. Radiation damage and wide temperature swings can severely limit the ability of electronics to perform optimally, and a system that could recognize its own drift from specification, and

more importantly correct for it, would be well received. A study on the effectiveness of this approach has yet to be performed under radiation.

Lastly, an ultra-fast x-ray detector with time resolution of 6.5 ps was realized in simulation. Further study of this concept would be required to achieve a useful implementation for sub-10 ps pump-probe experiments. This study would certainly involve measurement and validation of the completed system, but just as importantly the refinement of a number of aspects of the design. For instance, the per-pixel area of the array is too large to achieve a high resolution map of an evolving chemical process. Reduction of the design size and simplification of the necessary circuitry would help achieve a more realistic objective. In addition, the power consumption of a high density array of the existing pixels would be impractically large. Exploration of newer, faster HBT technologies with lower peak-f_T bias currents could enable such an approach in the future.

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