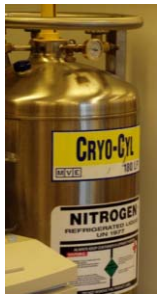

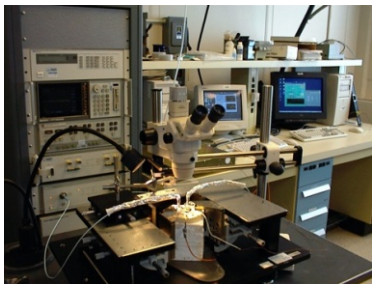

Characterization of LDMOS Devices in the Deep Cryogenic Regime

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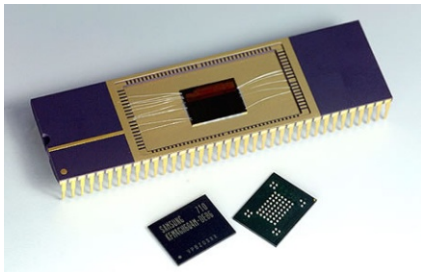
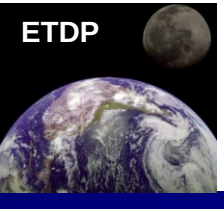
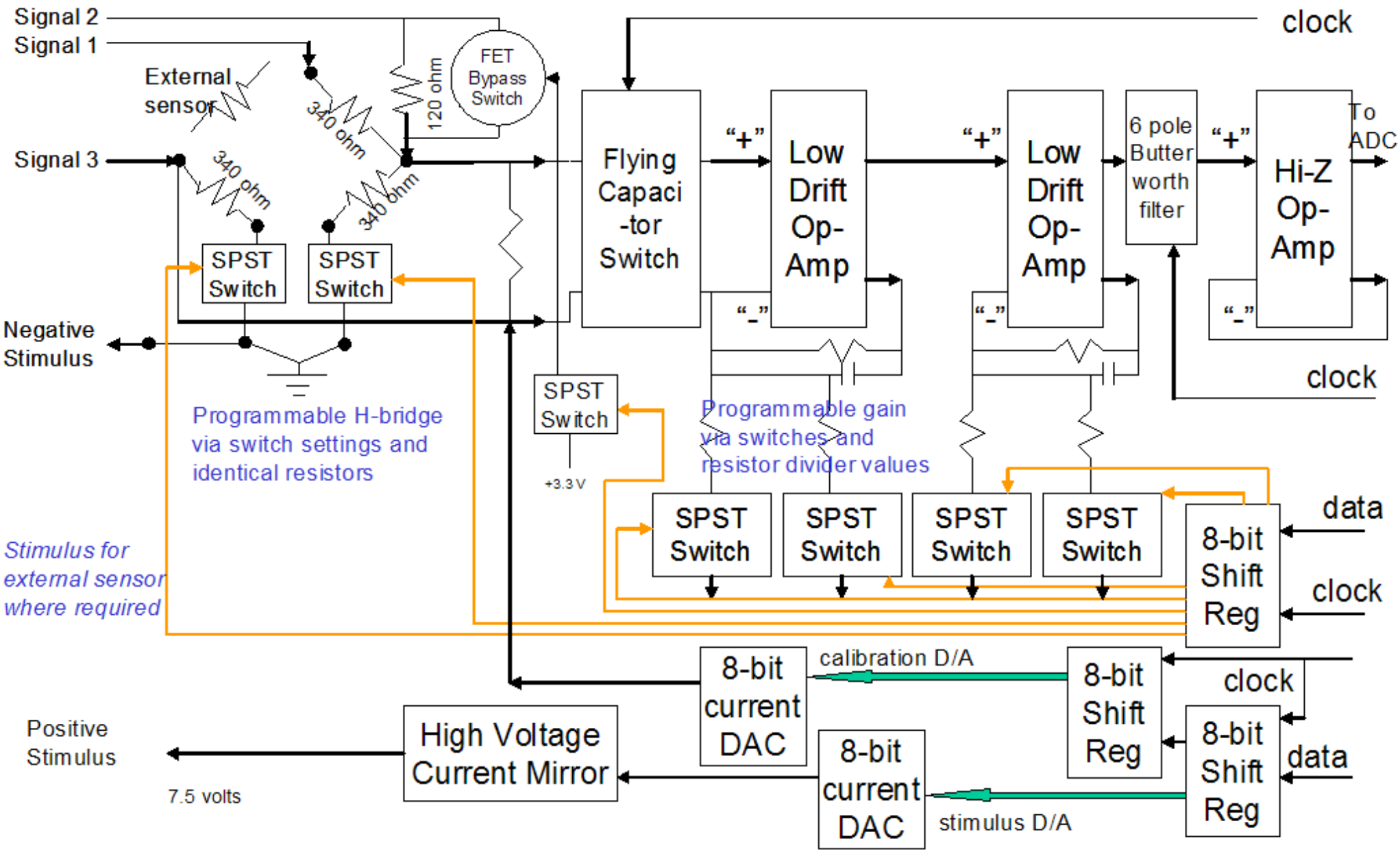




Motivation

- A team consisting of universities and industrial partners is designing mixed signal circuits to be used in the next generation shuttles (Ares series)
- One of the primary circuits being designed is a remote health monitoring system to be placed all over the craft, keeping track of various parameters such as temperature, pressure etc.
- Specifically, this project pertains to studying and modeling LDMOS devices (designed by JPL) used in the above circuits
- The model has to work down to -180 C enabling low temperature, extreme environment circuit design for aerospace applications
- The first step in modeling is to understand the device behavior in detail and characterize them as per model requirements

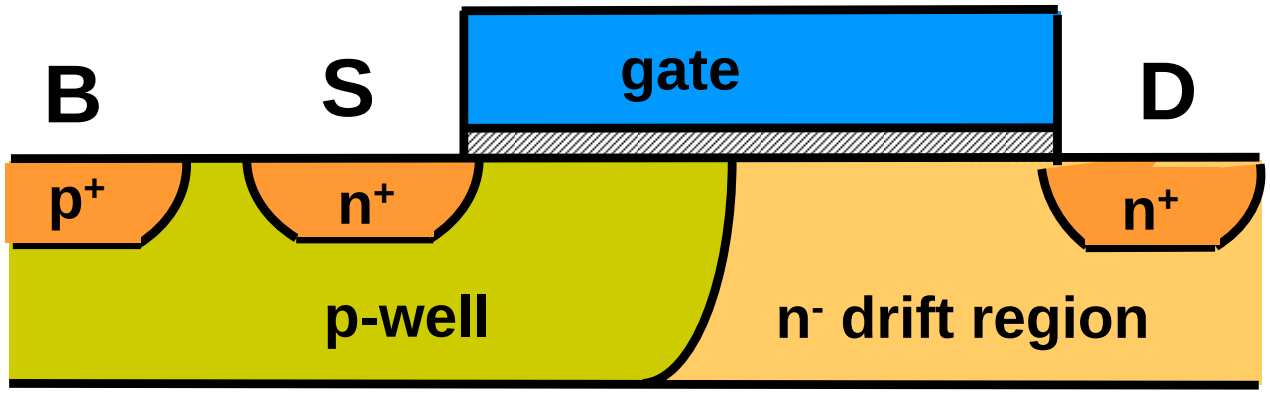
Current Overall Architecture



Introduction to LDMOS devices

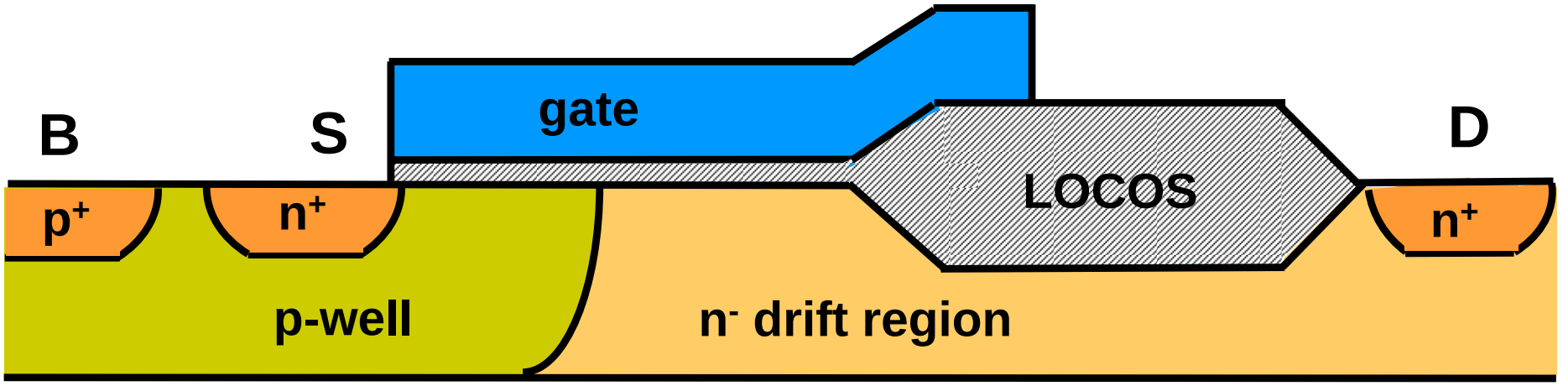
- Lateral structure aids in integration of the device with low voltage circuitry
- Used extensively in switch-mode power supplies, power amplifiers
- Applications in Cell-phone base stations, automotive circuits, consumer electronics etc.
- Can be HV-LDMOS or LV-LDMOS, i.e. drain voltage can range between 12 V to 1200 V

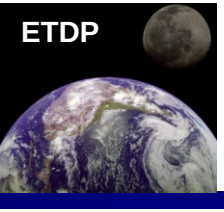
Device Physics



LV-LDMOS

HV-LDMOS

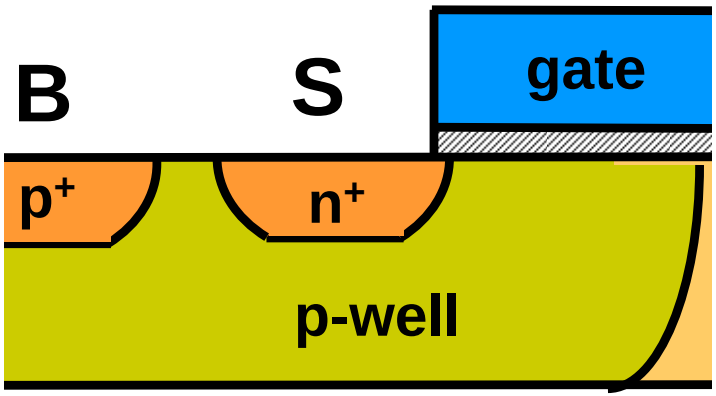


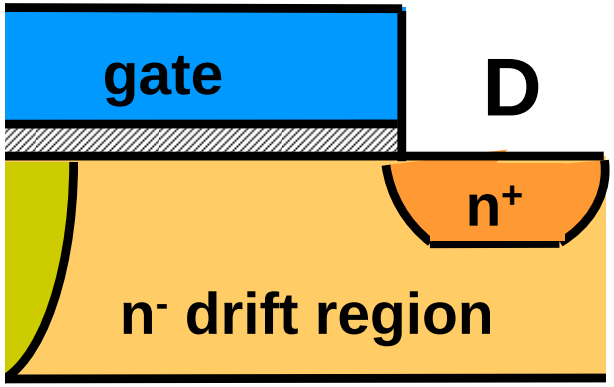


Device Physics

- Above the threshold voltage of the channel region, electrons flow from the source through an inversion channel towards the drift region
- With the gate extending over the drift region, an accumulation layer forms at the surface underneath the thin gate-oxide of the drift region
- After a certain point gate bias shielded by thick oxide (LOCOS/STI)
- Consequently, the electrons gradually flow into the bulk of the drift region
- Towards the drain, in the thick-field-oxide drift region, the electrons are spread out across the whole body of the drift region

Physical Effects in LDMOS devices





Channel region:

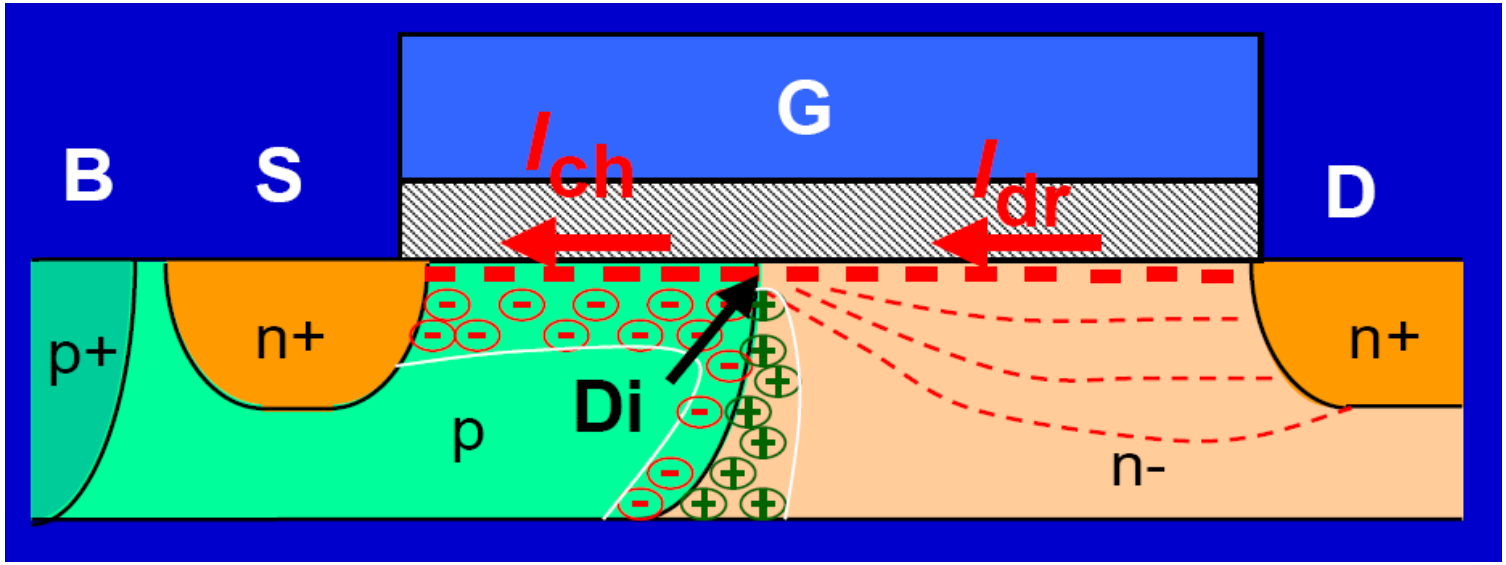
- mobility reduction due to vertical electric field
- velocity saturation
- channel length modulation
- DIBL
- avalanche

Drift region:

- accumulation
- depletion
- bulk current
- mobility reduction due to vertical electric field
- **Quasi-saturation**
- avalanche

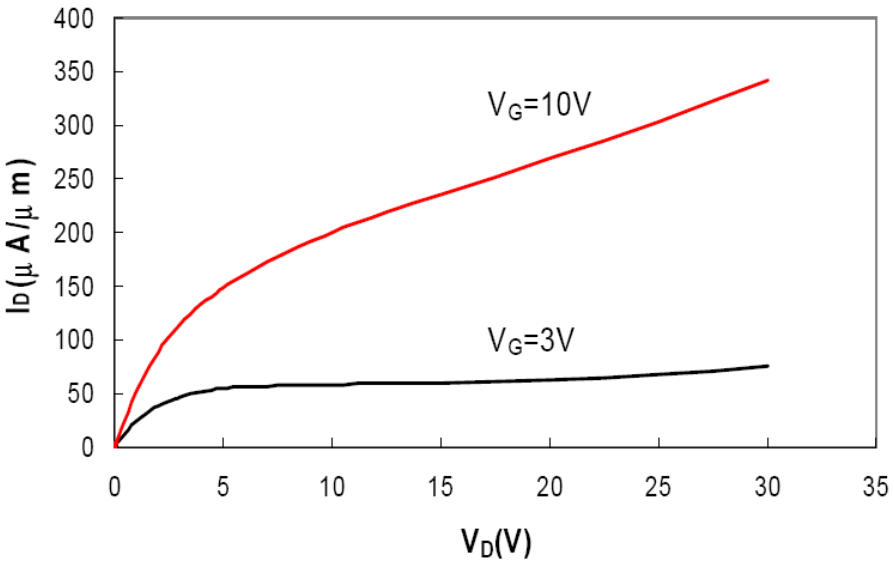
Quasi-saturation

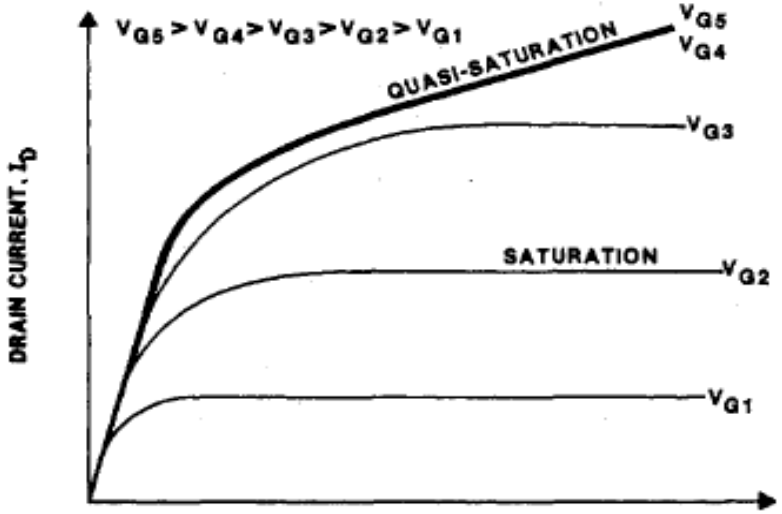
- LV LDMOS devices – absence of thick field oxide drift region and thus have a relatively short drift region
- In these devices, the conductivity of the drift region is always larger than that of the channel region, so that saturation of the current is controlled by the channel region



Quasi-saturation

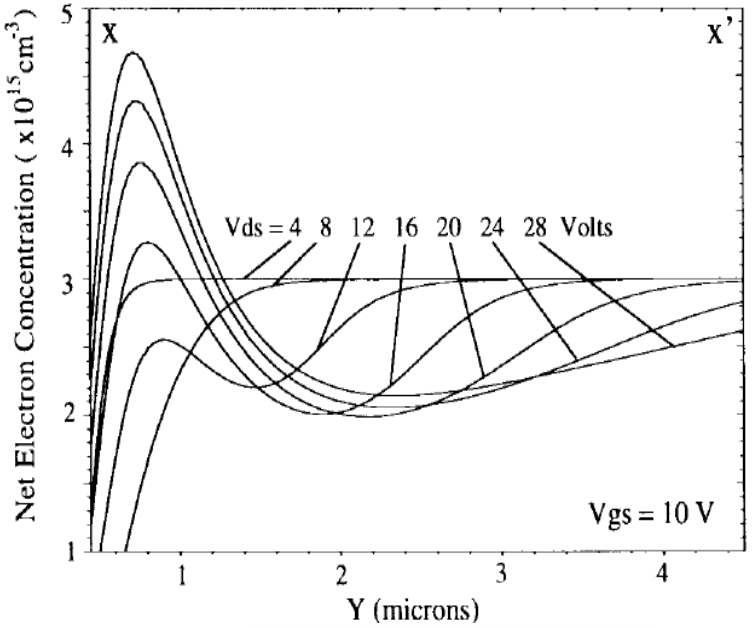
- But, in HV LDMOS devices, the current-voltage characteristics are affected at high gate-bias conditions
- For high Vgs, the increase of saturation current with increasing Vgs diminishes, which indicates the onset of quasi-saturation
- The reason is attributed to velocity saturation happening in the drift region

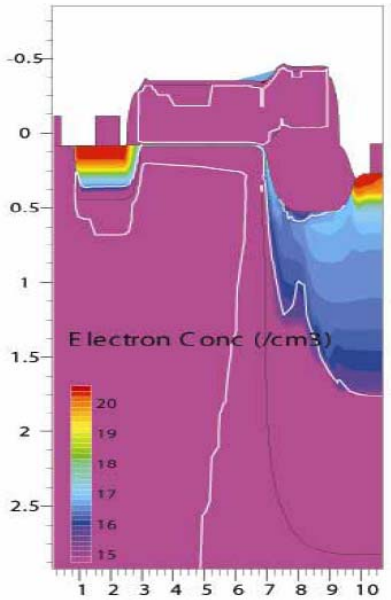




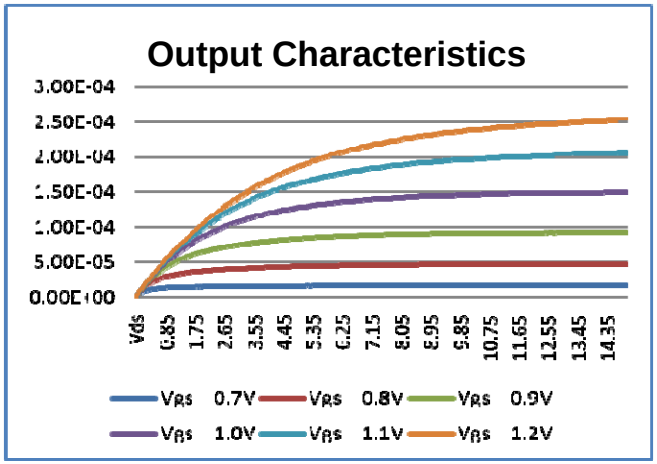
Quasi-saturation

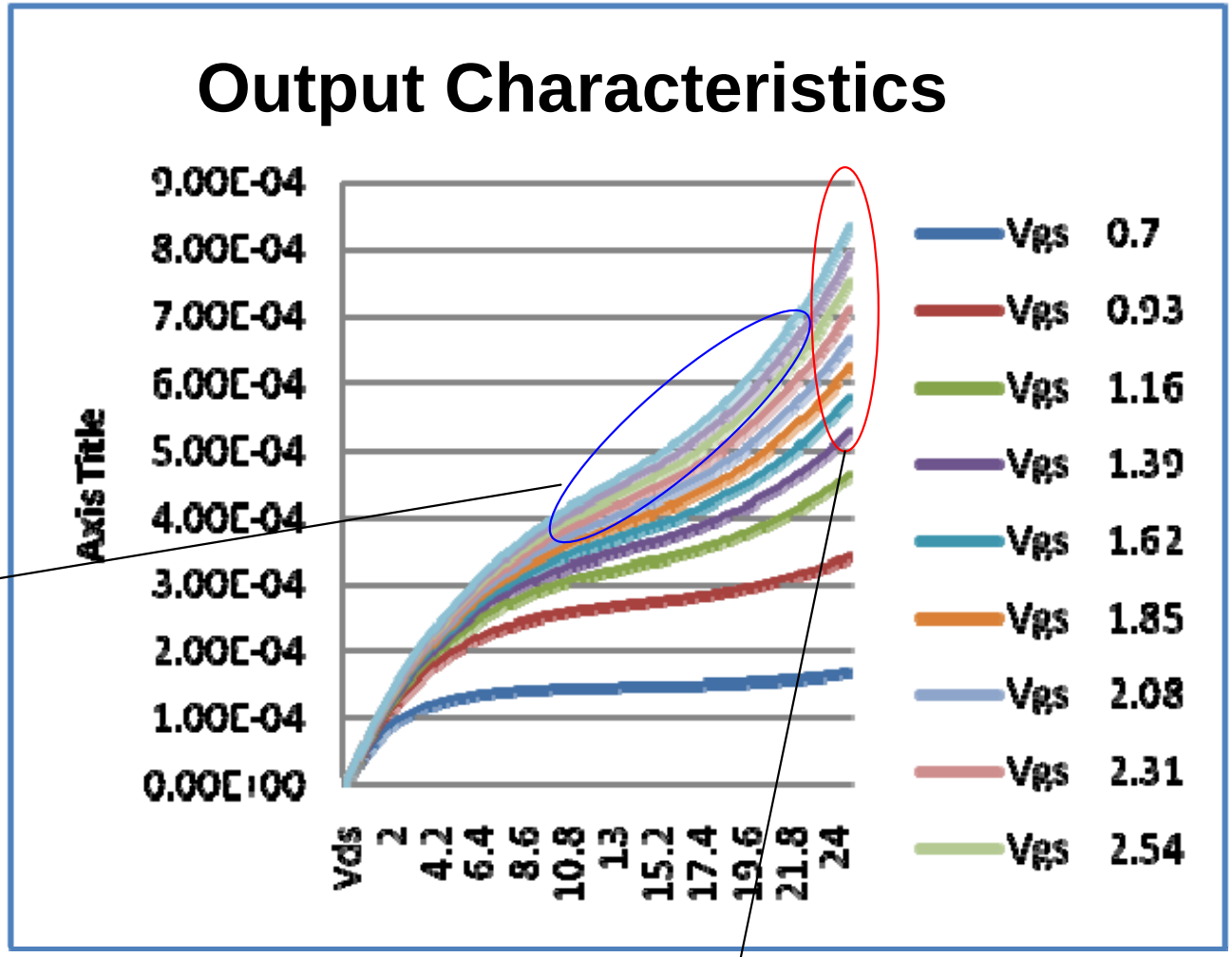
- **Observations such as Dipole charge build-up effect (Evans, 1997) support the velocity saturation theory**
  - **Current density is *α* to electron velocity, concentration and cross-section area**
  - **In the drift zone, when the channel is formed electrons are spreading from very narrow sections to wider ones towards the drain**
  - **To keep the current constant the electron concentration has to compensate the area increase; meaning the electron concentration is high for narrow sections and decreases progressively as the section increases**
- **TCAD simulations show the drift region flooded with electrons during the quasi-saturation phase**





Quasi-saturation in JPL's device





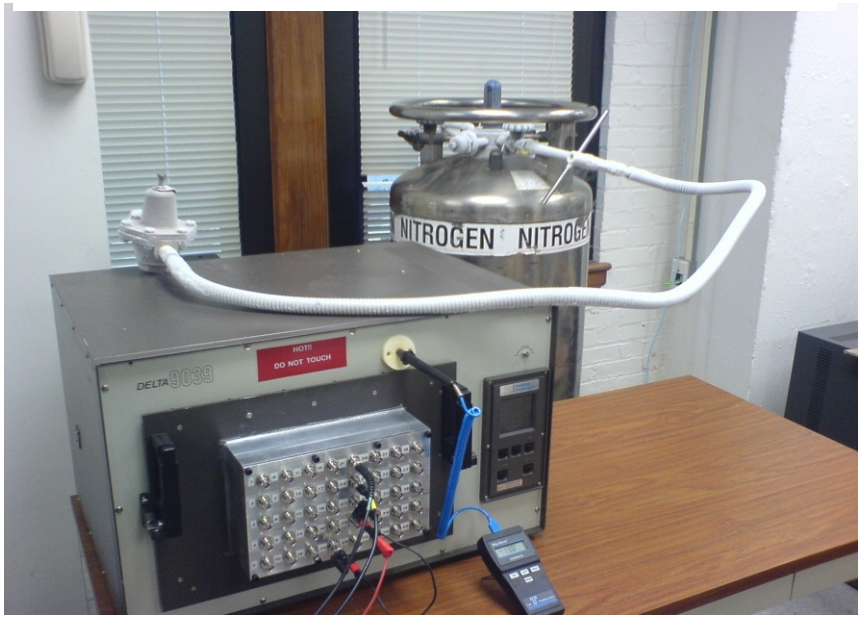
Quasi-saturation effect

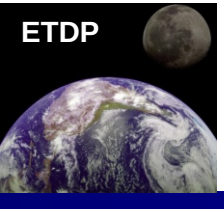
Dimensions:
L = 2u
W = 4.35u
Drift = 40.45u

Avalanche breakdown

Device Characterization

- Keithley-4200 system used for DC and CV measurements
- Cryogenic testing is performed in an environment chamber



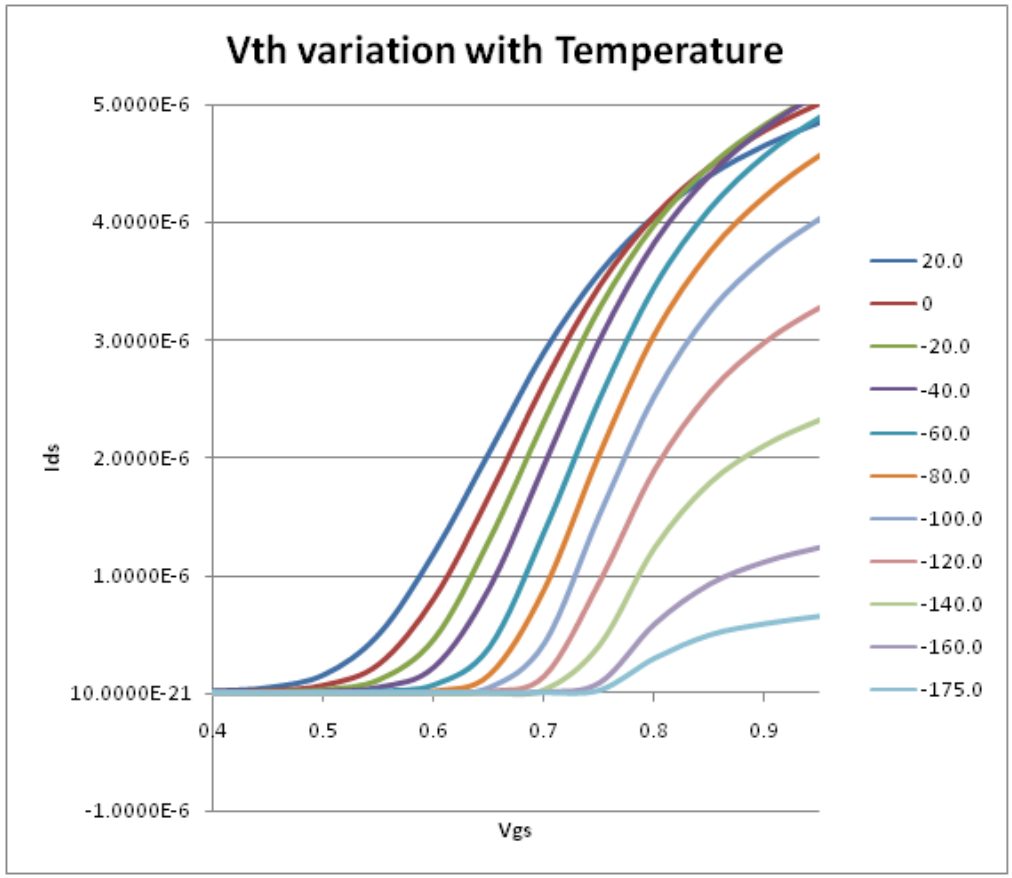


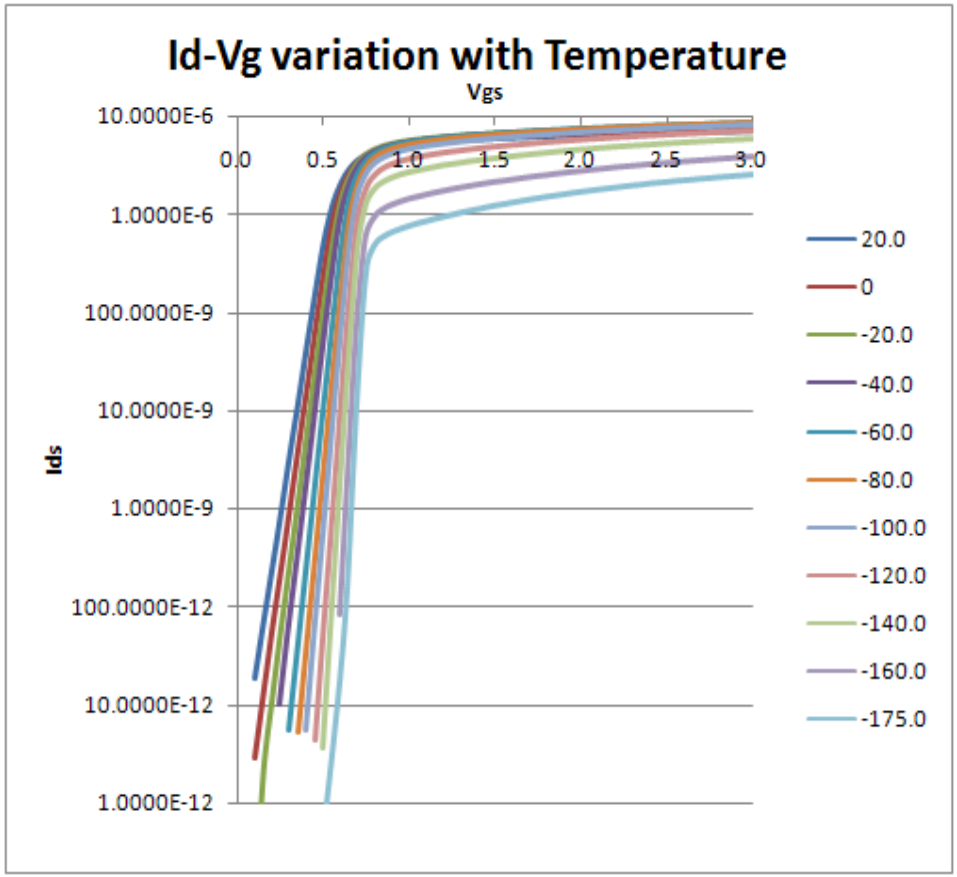
LDMOS Characterization

- LDMOS devices have been characterized as per MOS 20 requirements
- Device with only one gate length is required – "golden device" is to be identified as per breakdown voltage, Ron, SOA requirements
- Cryo characterization performed down to -180 C in steps of 30 C
- Interesting results have emerged from the cryogenic data

Cryo Characterization - Results

Vgs = 0 – 3.0 V, Vds = 0.1 V, Vsb = 0 V

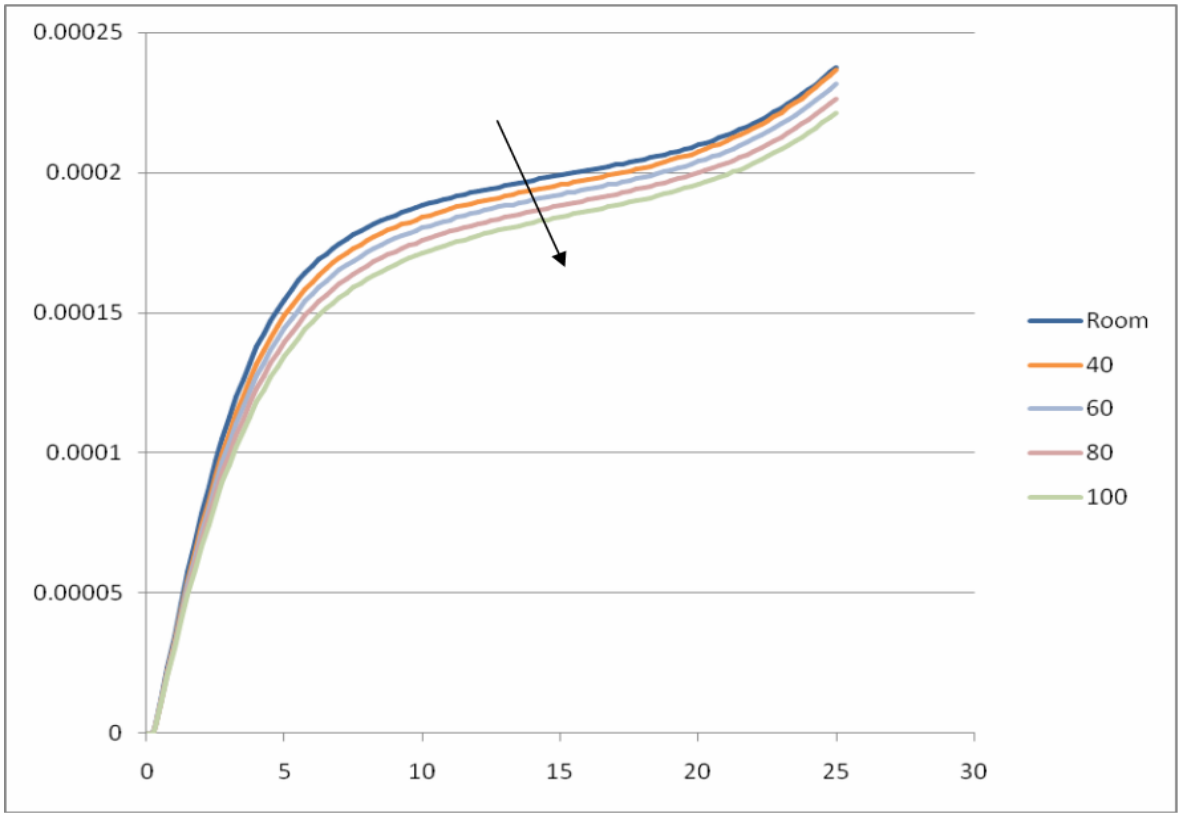




Variation of Vt as expected

Cryo Characterization - Results

High temperature characterization

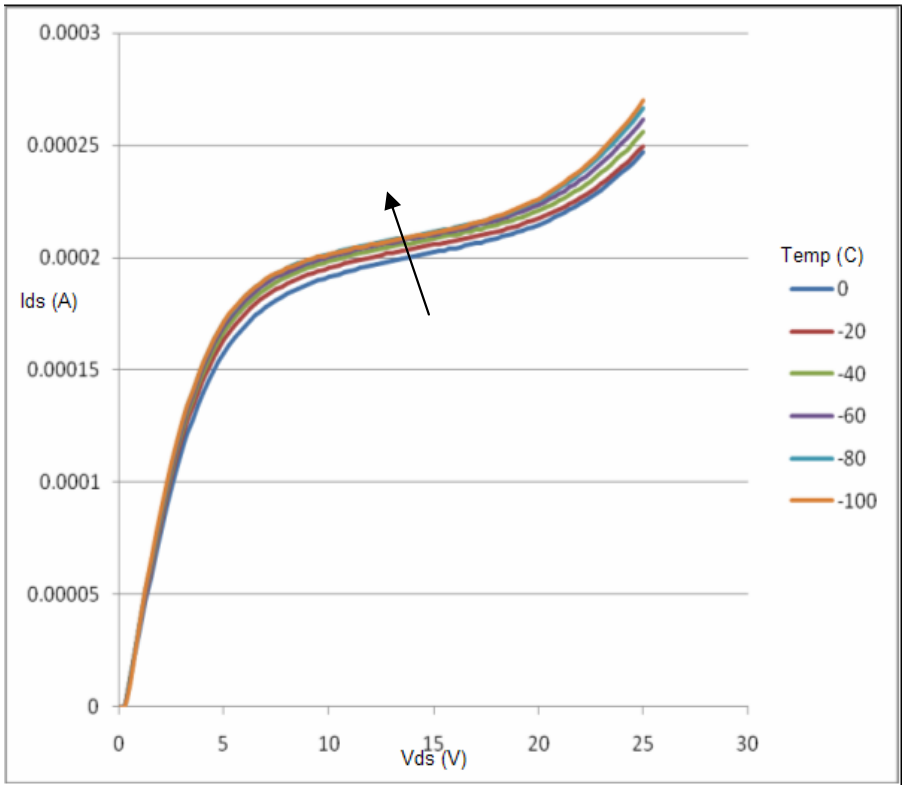


Vgs = 2.5 V,
Vds : 0 – 25 V

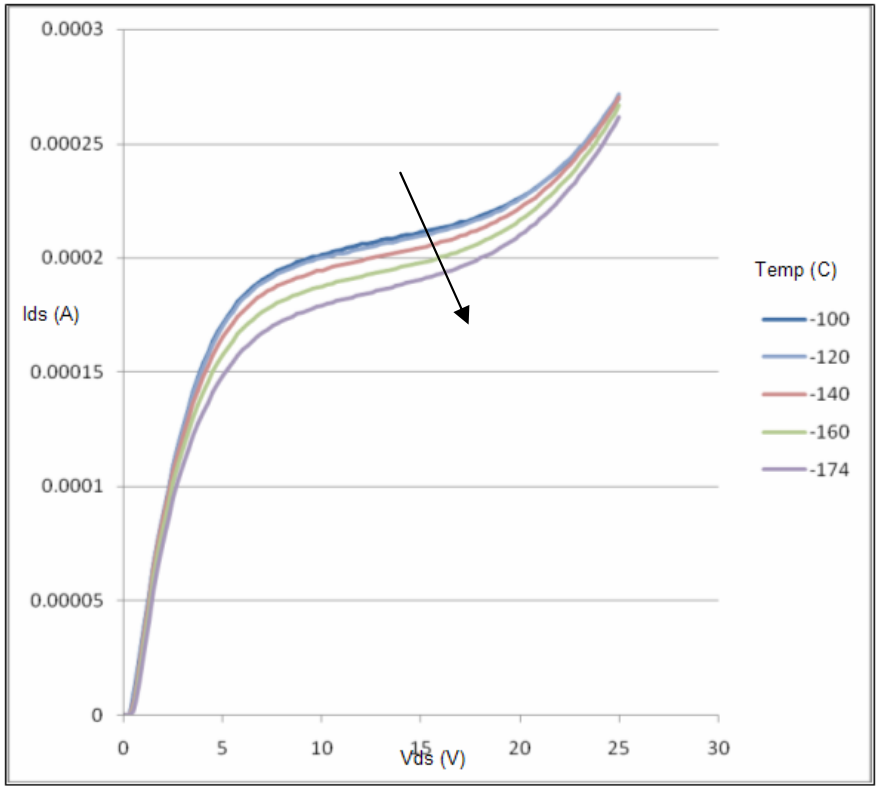
- **When temperature is increased, the drain current decreases just as expected in MOS devices**

Cryo Characterization - Results

Cryo characterization – Regime 1 (0 C to -100 C)

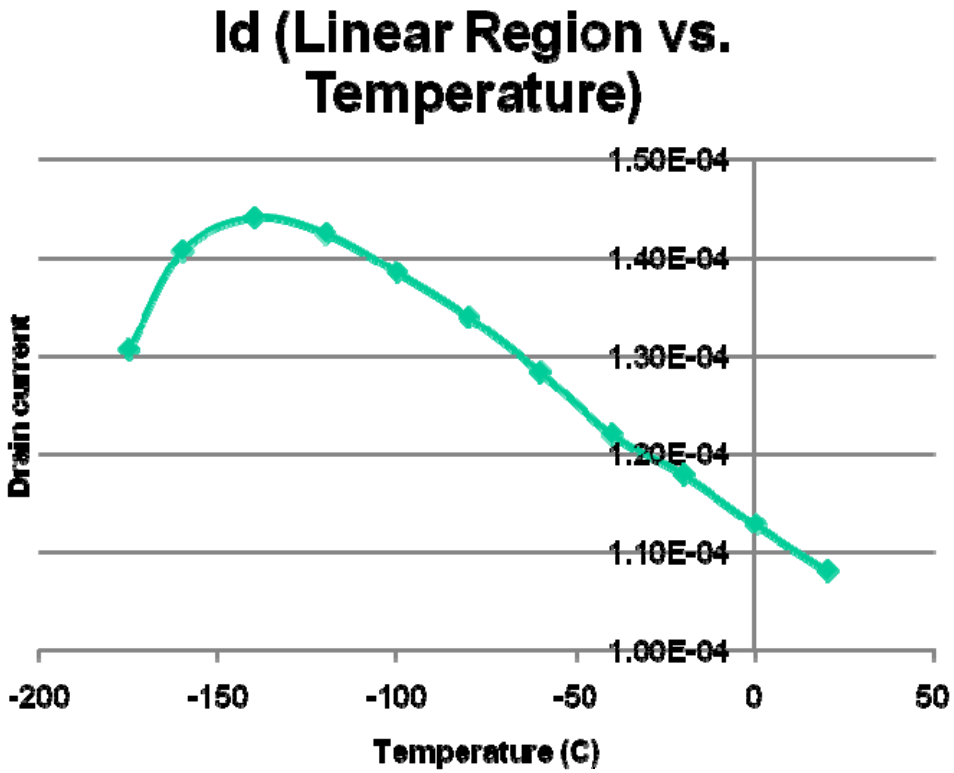


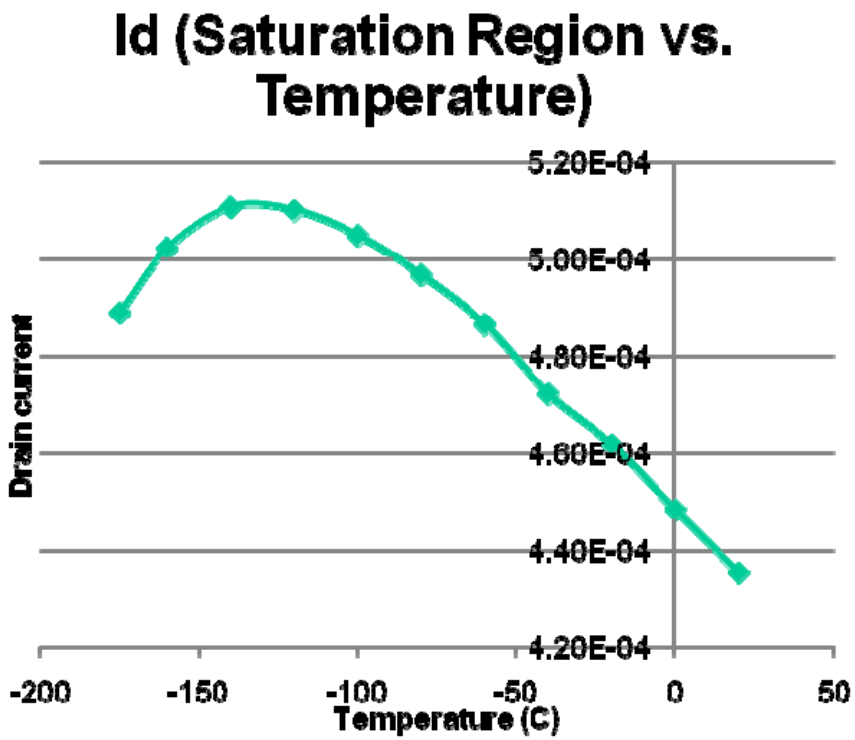
Cryo characterization – Regime 2 (-100 C to -174 C)



Vgs = 2.5 V, Vds : 0 – 25 V

Cryo Characterization - Results



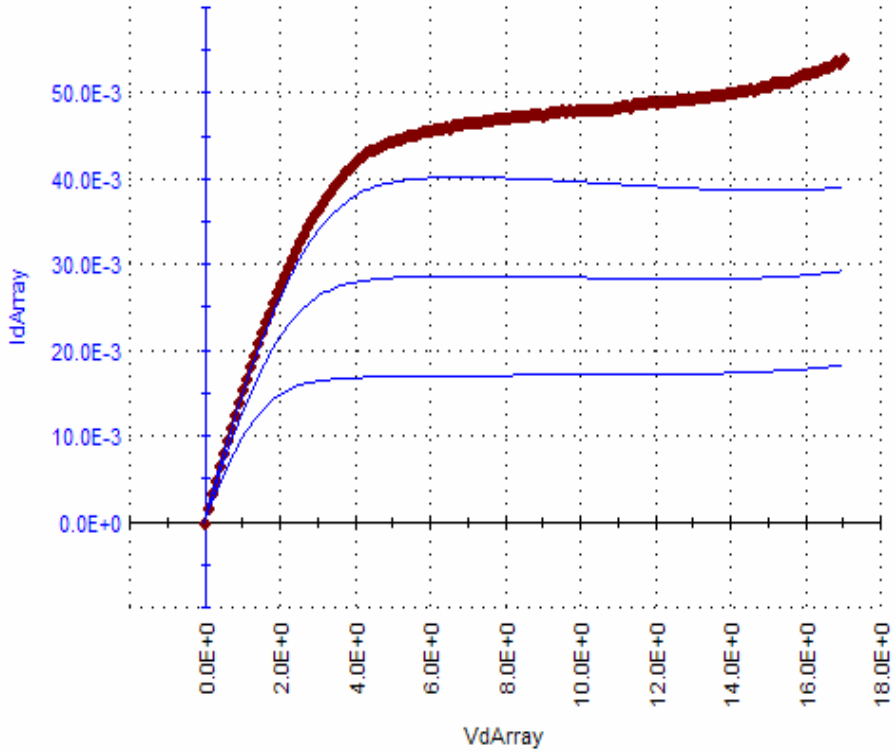


- Non-monotonic behavior
- MOSFETs generally display monotonicity even at temperatures lower than 20 K

Self-heating?

- An important consideration in high voltage devices is self-heating
- But it is ruled out due to the following reasons:
  - No characteristic drop in current in higher drain biases
  - Low current linear region also shows similar non-monotonic behavior
  - Verified with pulsed measurements

Typical self heating behavior in MOSFETs

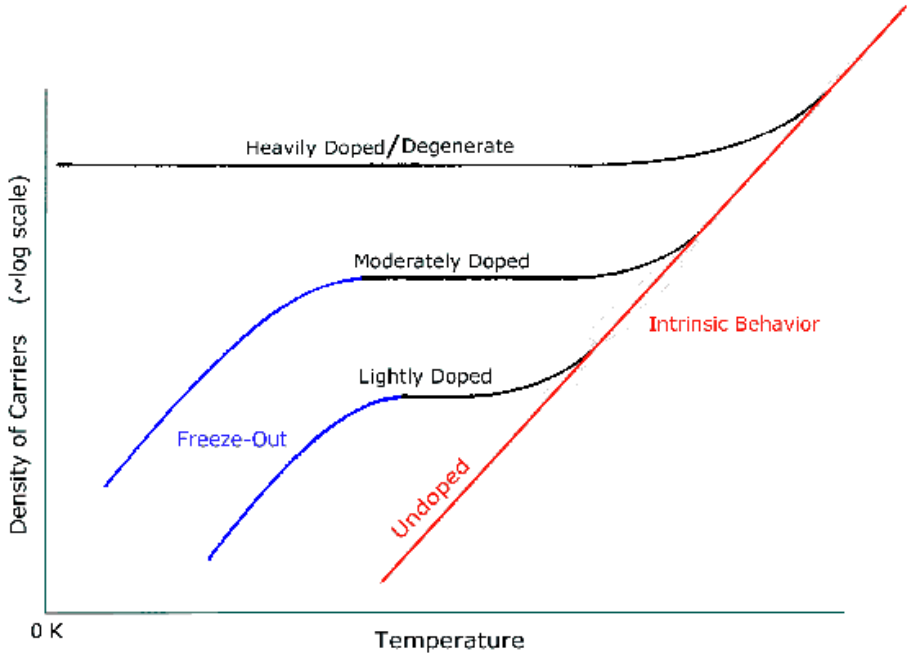


Blue – Normally measured device exhibiting self-heating
Brown – Pulsed device, no self-heating

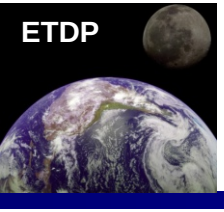
Cryo Characterization - Results

- Postulated to be the carrier freeze-out phenomenon happening in the drift region
- Transition varies between -90 C and -110 C depending on device (amount of n-well overlap under gate)

Carrier behavior with temperature

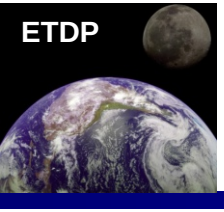


The black portion is roughly considered the usable temperature range



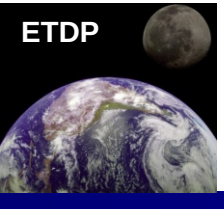
Physics of Freeze-Out

- Ionization energy is an important parameter
- Dopants usually require some energy (usually thermal) to ionize and produce carriers in the semiconductor
- If temperature is too low, dopants will not be sufficiently ionized and there will be insufficient carriers (freeze-out)
- Si MOSFETs can operate to the lowest temperatures because the carriers needed for conduction in the channel can be ionized by an electric field from the gate



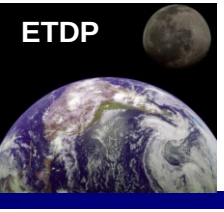
Physics of Freeze-Out

- Si MOSFETs and CMOS circuits are often used at deep cryogenic temperatures, below the freeze-out of Si (< 40K)
- But in the LDMOS devices, the gate's electric field is shielded from the drift region, which is doped low to start with
- This creates lower ionization of carriers in the drift region as the temperature is decreased and we can therefore see current considerably decreasing after a transition temperature
- Deep cryo operation of LDMOS devices has not been reported previously to our knowledge



Summary

- LDMOS devices were studied and characterized from +100 C to -180 C
- It was observed that impurity freeze-out starts at temperatures of ~ -100 C to -120 C
- Self-heating was ruled out due to the fact that drain current decreased in the linear regime also
- In general, MOSFETs can work at low cryo temperatures without freeze-out
- In LDMOS devices, the combination of the lightly doped drift region and the shielded gate leads to impurity freeze-out at considerably higher temperatures
- The current degradation is an important consideration for extreme environment circuit design
- Device engineering would help in pushing the transition temperature lower (such as reducing the depth of STI, increasing drift layer doping etc)
- The model that is currently under development at Arkansas incorporates this freeze-out phenomenon



Thank you!

Questions?