Design, Fabrication, and Characterization of Nano-scale Cross-Point Hafnium Oxide-Based Resistive Random Access Memory

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Design, Fabrication, and Characterization of Nano-scale Cross-Point Hafnium Oxide-Based Resistive Random Access Memory

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Non-volatile memory (NVM) is a form of computer memory in which the logical value (1 or 0) of a bit is retained when the computer is in its' powered off state. Flash memory is a major form of NVM found in many computer-based technologies today, from portable solid state drives to numerous types of electronic devices. The popularity of flash memory is due in part to the successful development and commercialization of the floating gate transistor. However, as the floating gate transistor reaches its' limits of performance and scalability, viable alternatives are being aggressively researched and developed. One such alternative is a memristor-based memory application often referred to as ReRAM or RRAM (Resistive Random Access Memory). A memristor (memory resistor) is a passive circuit element that exhibits programmable resistance when subjected to appropriate current levels. A high resistance state in the memristor corresponds to a logical '0', while the low resistance state corresponds to a logical '1'. One memristive system currently being actively investigated is the metal/metal oxide/metal material stack in which the metal layers serve as contact electrodes for the memristor with the metal oxide providing the variable resistance functionality. Application of an appropriate potential difference across the electrodes creates oxygen vacancies throughout the thickness of the metal oxide layer, resulting in the formation of filaments of metal ions which span the metal oxide, allowing for electronic conduction through the stack. Creation and disruption of the filaments correspond to low and high resistance states in the memristor, respectively. For some time now, HfO_2 has been researched and developed to serve as a high-k material for use in high performance

CMOS MOSFETs. As it happens, HfO_2-based RRAM devices have proven themselves as viable candidates for NVM as well, demonstrating high switching speed (< 10 ns), large OFF/ON ratio (> 100), good endurance (> 10^6 cycles), long lifetime, and multi-bit storage capabilities. HfO_2-based RRAM is also highly scalable, having been fabricated in cells as small as 10 x 10 nm^2 while still maintaining good performance. Previous work examining switching properties of micron scale HfO_2-based RRAM has been performed by the Vogel group. However, a viable process for fabrication of nano-scale RRAM is required in order to continue these studies. In this work, a fabrication process for nano-scale cross-point TiN/ HfO_2/TiN RRAM devices will be developed and described. Materials processing challenges will be addressed. The switching performance of devices fabricated by this process will be compared to the performance of similar devices from the literature in order to confirm process viability.

Chapter 1

Introduction

1.1 Motivation

Semiconductor digital logic devices, key components in major computing and information technologies, have transformed many aspects of human society over the past four to five decades. Semiconductor memory devices in particular are partially responsible for both the speed of operation as well as the massive data storage capabilities exhibited by modern computers, portable electronics, and many other important commercial applications. The semiconductor technology industry has long been engaged in an aggressive trend of downscaling components in pursuit of higher performance speed, higher density of both devices and data, lower power consumption, and increased functionality of electronic products and systems. Consequently, non-volatile memory (NVM) products have been developed and manufactured down to a ~16 nm critical dimension. However, a number of serious challenges face scaling to the < 10 nm dimension in order to achieve ever higher data and code storage capabilities [1]. As one possible solution for these challenges, alternative memory technologies based on material systems which demonstrate programmable resistance, or 'memristive', characteristics are being researched and in some cases developed. One such NVM alternative is resistive random access memory , or RRAM. HfO_2 -based RRAM has demonstrated excellent switching characteristics as well as potential scalability. In this work, the design, fabrication, and characterization of nano-scale cross-point HfO_2 -based RRAM will be discussed towards the aim of enabling continued studies intended to

develop a fundamental understanding of the impact of nano-scale dimensions on filament formation. In the following chapter, a brief background on NVM will be provided, along with discussions about memristance, resistive switching mechanisms, and basic metal-oxide RRAM functionality. In chapter 2, a successful process for fabrication of nano-scale cross-point HfO_2-based RRAM will be described, as well as processing challenges identified and addressed along the way. In chapter 3, the performance of the RRAM devices will be characterized and compared with the performance of similar devices from previous works, with a focus on the impact of scaling on fundamental device performance metrics. In the last chapter, conclusions as well as suggestions for further work will be offered.

1.2 Non-volatile memory

Computer memory can be separated into two broad classifications: volatile and non-volatile. Volatile memory requires a powered state in order to maintain data storage capabilities. Two baseline forms of volatile memory are dynamic random access memory (DRAM), which achieves a high memory density by storing bits of information on individual capacitors within an integrated circuit, and static random access memory (SRAM), which has very fast reading and writing capabilities and stores a single bit of information on multiple transistors simultaneously [2,3]. Non-volatile memory on the other hand, while generally exhibiting reduced performance capabilities as compared to volatile memory [4], allows for data retention in the powered-off state, which makes it a very desirable form of data storage for a wide range of electronics applications including consumer, automotive, computing, and communication. The explosion in these markets over the past decades, particularly in the portable electronics market, has driven the

success of a form of NVM called flash memory, which stores one or more bits of information on a single floating-gate transistor. Flash memory has allowed for an excellent compromise between cost, reliability, and performance capabilities such as data density, programming speed, and retention [4,5].

1.3 Flash memory

Flash memory in its modern forms evolved in the 1980's from a type of memory called EPROM (erasable programmable read-only memory) that required exposure to UV light in order to execute the erase procedure (the term 'flash' arose from the fact that the data in an entire memory array could be erased very quickly, i.e. in a 'flash'). Improvements on EPROM technology eventually led to the development of the two main forms of flash memory in the memory market today: NOR flash and NAND flash. Both types owe their success in part to the flexibility of the program and erase operations [4,5]. NOR flash memory can be both programmed and erased on the individual cell (single device) level, while offering comparatively low storage densities compared to NAND. NAND flash also consists of individually programmable cells, however the erase procedure must be performed on blocks of cells simultaneously. NAND on the other hand offers much greater storage densities as compared to NOR, and has therefore become the dominant form of flash memory [6].Both forms exhibit good endurance (i.e., the capability of retaining information after many program/erase/read cycles) as well as retention (capability of maintaining stored information for long periods of time), and have the floating gate transistor as their primary functional basis. Figure 1.1 below shows the general structure of a floating gate transistor.

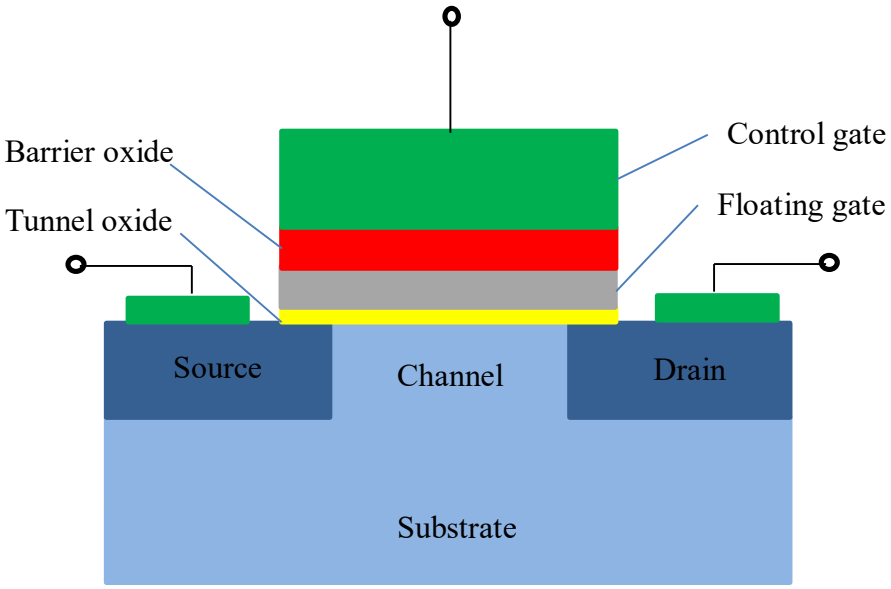


Figure 1.1. Cross-section of a floating gate transistor .

The basic operating principle of any floating gate transistor involves the ability to have its' threshold voltage (i.e., the minimum voltage differential between the gate and the source terminals required to achieve conduction between the source and drain terminals) controllably altered between different magnitudes which in turn correspond to different logic states of the cell. The "program" and "erase" operations for an individual NAND flash cell (i.e., a floating gate transistor) correspond to inducing the desired change in the value of the threshold voltage for the cell. For single-bit cells, these threshold voltage values and their corresponding conductive states correspond to logical 1's or 0's stored as part of a binary digital byte or word. The "read" operation for an individual cell consists of applying a gate voltage to the transistor between the known low and high values of the threshold voltage, then measuring the resulting current that flows through the cell[6].

Program and erase operations on a floating gate transistor consist of generation or removal of charge on the floating gate, facilitated by injection onto or removal of electrons from the gate, respectively. Both the program and erase operations consist of application of the appropriate voltage across the control gate, source, and drain terminals of a floating gate transistor such as that in Figure 1.1. This causes electrons to tunnel back and forth from the floating gate through the tunnel oxide in a direction consistent with the operation being performed. The key functionality lies in the fact that the floating gate acts as potential well. Once a charge has been applied to it, electrons cannot escape without the application of an external electric field (see Figure 1.2 below) [5]. The two primary electron tunneling mechanisms used for the program and erase operations in a NAND flash cell are direct tunneling and Fowler-Nordheim (FN) tunneling .

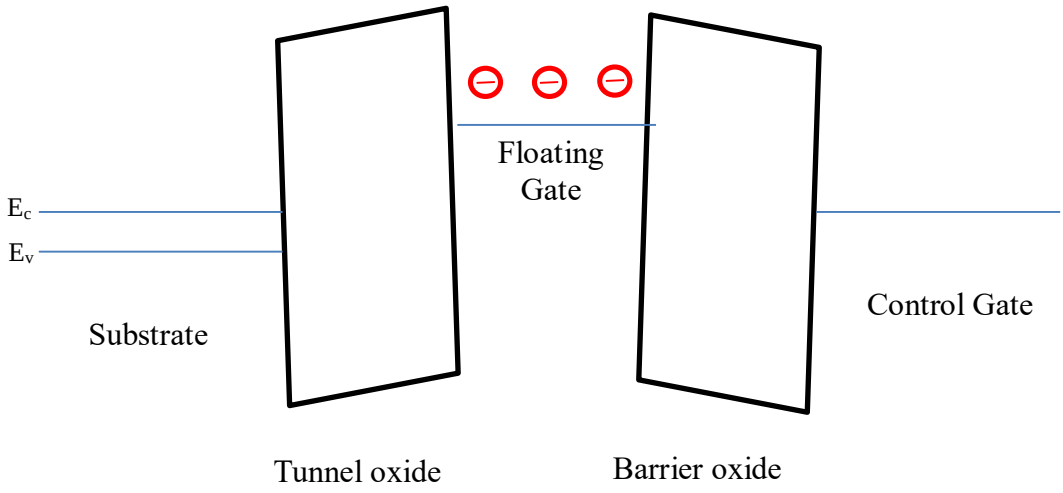


Figure 1.2 Energy band diagram of a floating gate transistor showing electrons trapped on the floating gate.

The FN tunneling mechanism occurs when large magnitude electric fields are directed through a thin oxide. The energy band diagram for the oxide becomes very steep at high

energies, resulting in a higher probability of an electron being able to pass through the barrier. Figure 1.3 shows an energy band diagram of the primary tunneling mechanisms in a floating gate transistor.

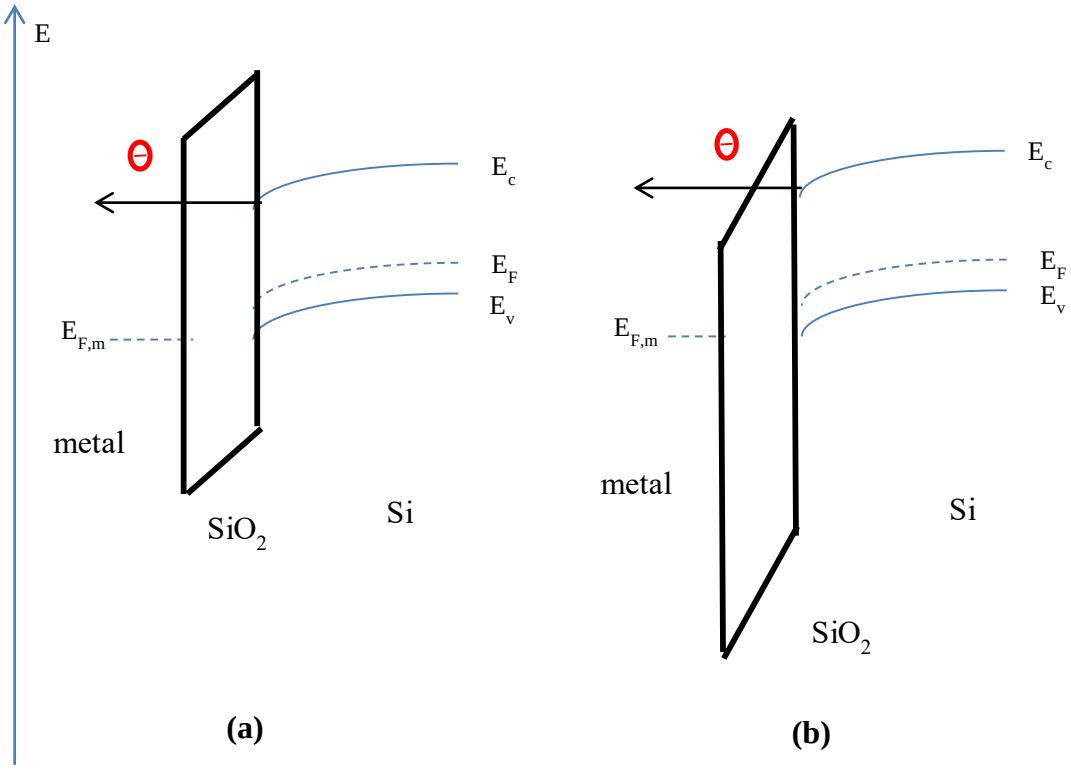


Figure 1.3 Tunneling mechanisms in a floating gate transistor (a) direct tunneling (b) FN tunneling

Although the operating mechanisms for popular and successful forms of flash memory such as NAND –type memory cells are well understood, flash memory faces emergent challenges as the trend toward further device scaling in relentless pursuit of higher device density and increased performance in the microelectronics industry continues. These challenges will be discussed in the following section.

1.4 Future of flash memory

The semiconductor technology industry has long been engaged in an aggressive trend of downscaling components in pursuit of higher performance speed, higher density of both devices and data, lower power consumption, and increased functionality of electronic products and systems. Currently, flash memory products have been developed and manufactured down to a ~16 nm critical dimension. However, a number of serious challenges face scaling to the < 10 nm dimension in order to achieve ever higher data and code storage capabilities [1]. Key challenge areas include:

1. *Performance, reliability, and endurance requirements*: Reducing the thickness of the tunneling oxide and control dielectric have been key processing parameters driving lower power consumption, shorter program/erase times, and increased device density. However, a bottleneck has occurred at the ~10 nm thickness range, below which serious problems emerge. Some of these problems include unwanted injection of electrons into the tunnel oxide during erase operations and loss of adequate control over the conduction channel due to undesirably low capacitive coupling between the channel and the tunneling oxide layer. Thinner oxides also become more prone to charge leakage and defect formation due to voltage stress, both of which reduce performance quality over time [4,8].

2. *Increased data storage density*: Limits on device dimensions and therefore device density are naturally imposed due to increasing cell-to-cell electrical interference and breakdown between word lines as size decreases. Additionally few-electron storage issues arise due to thinner oxide layers, which limits data density as well as increasing potential for unwanted electrical noise [1].

Potential solutions to this range of issues include the development of multi-bit storage capabilities, as well as development of novel 3-D architectures in order to increase overall memory efficiency as well as data and device densities. Alternative material systems and memory technologies such as RRAM which exploit memristive characteristics are being explored as well. This novel memory application as well the property of memristance will be examined more closely in the sections that follow.

1.5 Memristance and memristive systems

As just stated, novel forms of NVM with memristors as the functional basis are being researched and developed as one of the possible solutions for driving the continued increase in data density and device performance in the NVM market.

In 1971, Leon Chua predicted the existence of a fourth passive circuit element called a memristor ("memory resistor"), which exhibited behavior he called memristance ("memory resistance"). Through a quasi-static expansion performed on Maxwell's equations of electromagnetism analogous to that performed in order to derive the relationships between voltage and current for resistors, magnetic flux and current for inductors, and voltage and charge for capacitors, Chua established a relationship between flux-linkage and charge which he predicted would be demonstrated by memristors [7,10]:

$$M(q) \equiv \frac{d\varphi(q)}{dq} \tag{1.1}$$

,where M is memristance, φ is the flux linkage and q is the charge. The voltage across a charge-controlled memristor is then given by

$$v(t) = M(q(t))i(t) \tag{1.2}$$

,where v is the voltage, t is time, and i is the current. The reference to "memory" in the term "memristor" comes from the fact that the value of the memristance at any time t_0 depends on the time integral of the current (i.e., the charge q) through the memristor from time $t = -\infty$ to $t = t_0$. Thus, while a memristor behaves as an ordinary resistor at any time t_0, its' resistance value is determined by the complete past history of the current through the memristor. As equation 1.2 shows, for linear passive circuit elements the memristance is constant and therefore indistinguishable from standard electrical resistance. When M is a function of q however, the resistance becomes non-linear, and Chua found that no combination of non-linear passive resistive, capacitive, or inductive components could reproduce the i-v characteristics of a memristor [7,10]. Five years later in 1976, Chua and Kang generalized the memristor concept by introducing a broad class of non-linear dynamical systems they termed memristive systems, which are described by the following equations [8,9]:

$$v = R(w, i)i \tag{1.3}$$

$$\frac{dw}{dt} = f(w, i) \tag{1.4}$$

, where R is the resistance, f is a function, w is a set of state variables, and R and f can be explicit functions of time. At the time of these publications, Chua and Kang suggested that many systems could be described as memristive, including certain electrochemical cells, nerve axon membranes, thermistors, discharge tubes, and others, though no system had ever been formally identified as such.

The first passive physical system demonstrably exhibiting memristance as such was announced in a Nature journal article in 2008 by Waser, et.al., and was created by

R.S. Williams and his research team in the Hewlett-Packard labs [8,10]. Their memristor structure was a metal-metal oxide-metal material system, consisting of a cross-point array of 40 nm wide platinum wires, with 40 nm cubes of titanium dioxide (TiO_2) at each cross-point, which themselves consisted of two layers : a perfectly stoichiometric lower layer (2:1 Ti to O), and an oxygen deficient upper layer of TiO_{2-x} ($x \approx 0.05$) (see Figure 1.4 below). The mechanism for the memristive behavior is as follows: application of a positive voltage to electrode in contact with the TiO_{2-x} region of the

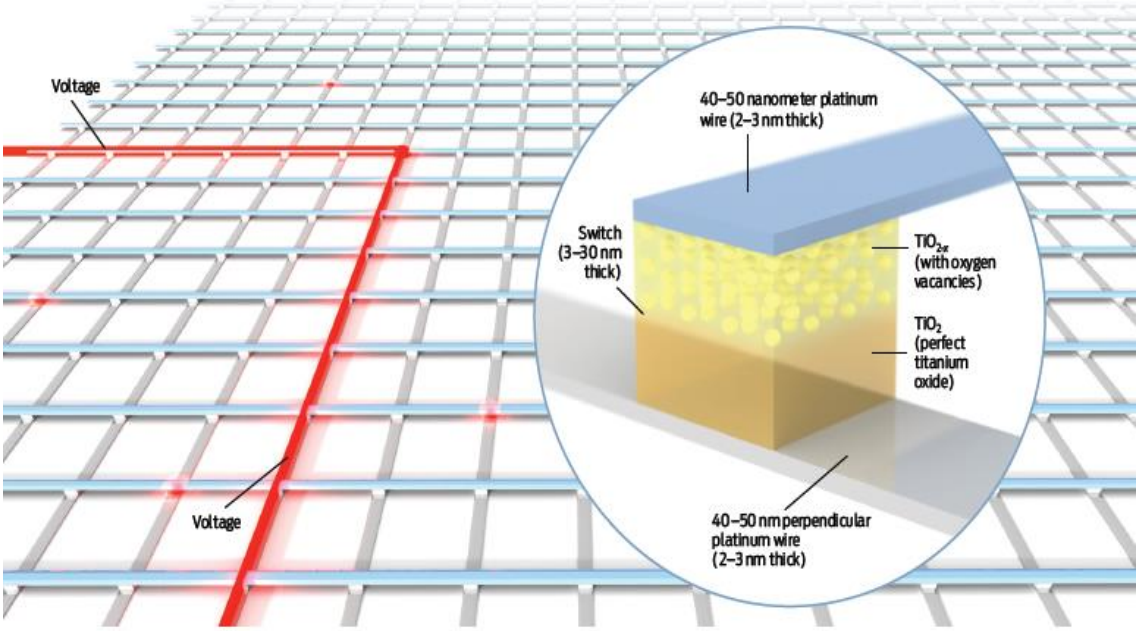


Figure 1.4. Cross-point configuration of TiO_2-based memristors showing structure and composition of a single memristor cell. © 2008 IEEE

cell causes oxygen vacancies from this O-deficient region to migrate towards the stoichiometric region (Figure 1.5.a). This migration in turn causes the boundary between the two layers to migrate away from the more positive voltage source towards the less positive source, functionally increasing the length of the metal-oxide region consisting of conductive TiO_{2-x} as opposed to insulating TiO_2. The increased effective concentration of

TiO_{2-x} then functionally reduces the resistance in the memristor by increasing the length of the conductive region, thereby enhancing electronic current through the cell. Application of a negative voltage has the reverse effect, i.e. the oxygen vacancies migrate towards the oxygen deficient region once again, thus effectively increasing the percentage of insulating TiO_2 in the memristor, thereby increasing the resistance through the cell (Figure 1.5.b). What makes this system memristive is the fact that no migration of

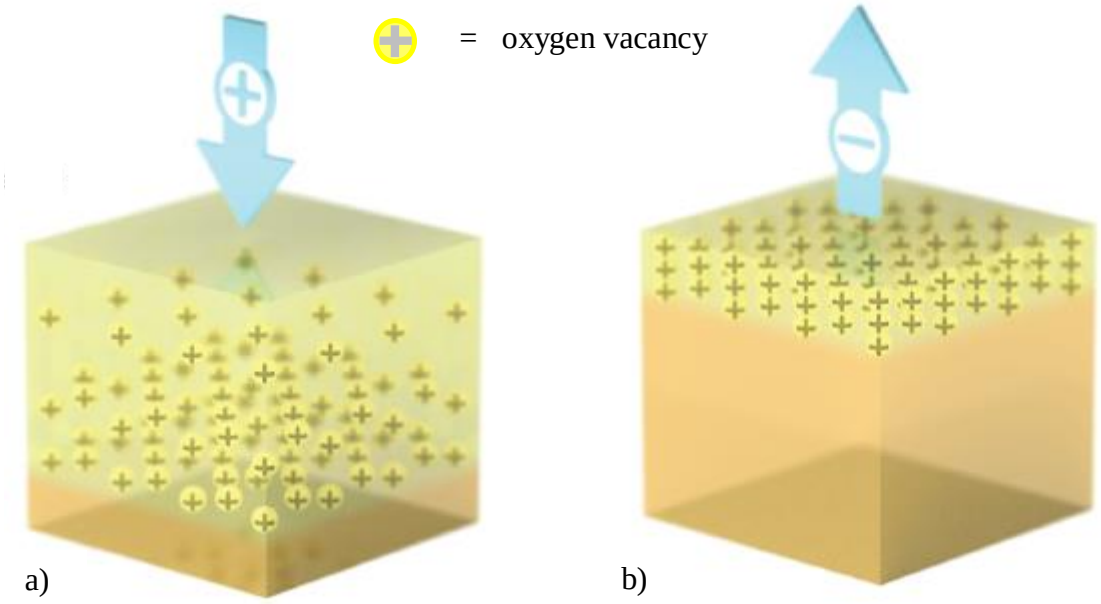


Figure 1.5 Operation of TiO_2-based memristors a) Application of a positive voltage to the TiO_{2-x} region of the cell causes the oxygen vacancies to migrate towards the opposite electrode, thereby increasing the effective length of the conductive region of the cell. b) Reversing the voltage polarity has the opposite effect, restoring the insulating effect of the TiO_2 by increasing its' effective concentration in the cell. © 2008 IEEE

oxygen ions occurs if no voltage is being applied. Hence, the switch "remembers" its' most recent resistance state. The relationship between voltage and current for these memristors is modeled by the equations

$$v(t) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right)i(t) \qquad (1.5)$$

$$\frac{dw}{dt} = \mu_V \frac{R_{ON}}{D} i(t) \tag{1.6}$$

where R_{ON} is the resistance in the sub-stoichiometric region, w is the distance which the boundary between the layers has traveled(defined on the interval [0,D]), R_{OFF} is the resistance in the stoichiometric region, and μ_V is the mobility of the oxygen vacancies. R_{ON} and R_{OFF} are treated as resistances connected in series, and D is the complete width of the metal-oxide region of the cell[8]. As equation 1.5 implies, the overall resistance of the cell decreases as the boundary between the different regions moves from w=0 to w=D. Additionally, the i-v characteristics of these cells showed hysteretic (non-linear) behavior under various voltage application regimes, which eventually provided the clue that led Williams and his team to connect this behavior to the memristance that Chua had theorized 40 years earlier [10].

As it happened, the switching behavior was fast, occurred over very small distance ranges (3-30 nm), and had significant off/on resistance ratios (approx. 1000) which remained stable for very long periods of time[10]. This made it apparent to Williams and others that this new memristive system (or others that functioned in a similar fashion), could represent a viable candidate as a form of NVM or any other computing systems whose functionality requires various resistance states, principally by exploiting the hysteretic i-v behavior as a form of resistive switch [10,11].

1.6 Memristive Systems as NVM

In addition to the memristive system described above, many other similar material systems classifiable as memristive have been researched , i.e., metal-insulator-metal (MIM) stacks which exhibit variable resistance[11,12]. While the physical driving force

is usually electrically induced, functionality of the resistive switching mechanisms exhibited by these MIM stacks can vary quite distinctively [11]. For example, mechanical forces can be utilized to induce memory effects, or changes in ferromagnetic domain polarization, or changes in phase, e.g., change between amorphous and crystalline phases [11]. Redox-reaction-based mechanisms in these systems are a common means of resistance change, and these mechanisms can be broadly classified as falling into three categories: change in resistance due to a redox reaction induced by electrochemical metallization, valence change, or thermochemical mechanisms[11]. These classifications and their mechanisms are briefly described in the following sections.

1.6.1 Electrochemical mechanism

In these systems, the resistive switching mechanism involves the electrochemical dissolution of one electrode metal and its' subsequent deposition at the other electrode. An individual MIM cell consists of an electrochemically active electrode such as Ag, Cu, or Ni, and an inert electrode such as Pt, Ir, W, or Au. Sandwiched between the two metals is a solid electrolyte capable of conducting metal ions. Prior to switching, a cell is in its' high resistance state. The switch to a low resistance state results from the formation of a metallic conductive filament through the insulating region, which can be characterized in three steps[11,13]:

1. Dissolution at the active electrode by the reaction

$$M \rightarrow M^{n+} + ne^{-} \qquad (1.7)$$

2. Migration of the M^{n+} cations through the electrolyte under the influence of an applied electric field.

3. Reduction and electrocrystallization of the metal ions at the inert electrode surface according to the reaction

$$M^{n+} + ne^{-} \rightarrow M \quad (1.8)$$

Interestingly, this resistance change mechanism was predicted by Chua in his original 1971 paper [7].

1.6.2 Valence change mechanism

In valence change systems, the resistance change in the MIM cell is induced through a valence change of metal cations present in the insulator layer. Typical examples of this mechanism are found in MIM structures that contain transition metal oxides as the insulator[11]. Application of a voltage of the appropriate magnitude and polarity at one of the electrodes can induce diffusion of oxygen anions through the insulator layer. The ionization process for oxygen can be described by

$$O_O = V_O^{\cdot\cdot} + O^{"} \quad (1.9)$$

where standard Kroger-Vink notation is used to describe lattice occupancy and charge conditions. As a result of the presence of positively charged oxygen vacancies, a conductive "trail" of metal cations remains which allows for electronic conduction through the stack, by the reactions

$$V_O^{\cdot} = V_O^{\cdot\cdot} + e' \quad (1.10)$$

$$V_O = V_O^{\cdot} + e' \quad (1.11)$$

The creation of a conductive pathway thereby changes the resistance state of the MIM cell from a high resistance to a low resistance state after application of the voltage. The

reverse reaction, i.e. the change back to a high resistance state, is governed by recombination of oxygen anions with unoccupied oxygen vacancies by the reverse of reaction 1.12 [14].

1.6.3 Thermochemical mechanism

The thermochemical resistance change mechanism results from local Joule heating effects which occur in the insulator due to high current resulting from a voltage applied across the electrodes. If a large enough electric field is applied across the insulator, electrical breakdown, i.e., a shift to a conductive state, can occur [15]. After breakdown, the insulator is in a low resistance state until such time as the film can be recovered in some way, e.g., by subsequent application of another voltage.

It is important to note that more than one of these mechanisms can contribute to the resistance change in a particular system, and isolation of one of the mechanisms as being the dominant one, where possible, will depend on the nature of the particular switching system. Also, analytical models for key values associated with switching tend to be particular to specific material systems, making generalization of the overall mechanisms even more challenging [14,16].

1.6.4 Resistive random access memory as NVM

NVM applications that exploit resistance change mechanisms have come to be generally referred to as resistive random access memory (RRAM or ReRAM). The exploitation of the resistance changes described above in pursuit of a viable form of next-generation NVM technology requires that any RRAM application meets certain general performance specifications [11]. These include:

1.*Write operation*: the write operation for an RRAM cell should be in the range of a few hundred millivolts to a few volts in order to not only be CMOS compatible, but to provide an advantage over typical flash programming voltages.

2. *Read operation*: Read voltages in general must be capable of being small enough such that application of the voltage does not induce resistance change in the cell. This necessity introduces a challenge to the low magnitude requirement for the write voltage due to fact that the read voltage cannot be less than approximately one-tenth of the write voltage for practical reasons of circuit design.

3. *Resistance ratio*: the ratio of R_{off}/R_{on} must be > 10 in order to allow for technologies that incorporate small and efficient sense amplifiers, making them effective cost competitors with flash memory.

4.*Endurance*: flash memory can endure up to 10^7 write cycles, depending on the particular type. RRAM cells would need to be at least approximately this robust in terms of endurance in to order to be viable commercially.

5. *Data retention* :universal NVM standards require data retention times to be >10 years up to a thermal stress of 85° C, and electrical stress due to a constant stream of read voltage applications. Again RRAM cells would have to at least approximately match these specifications in order to be competitive in the NVM market.

Various forms of RRAM utilizing a MIM structure with transition metal oxides serving as the insulating layer have proven to be up to the challenge of matching these

performance requirements in many cases. The properties and functionality of metal oxide RRAM will be examined in more detail in the following section.

1.7 Metal Oxide RRAM

As mentioned in the previous section, MIM RRAM in which metal oxides serve as the insulator have demonstrated the potential to serve as viable NVM applications. Across a range of material systems, RRAM cells of this type have demonstrated CMOS-compatibility, very fast read/write speeds, excellent endurance, and very low power/energy consumption consistent with the general standards for viability discussed in the previous section [11,16]. Additionally, it is envisioned that RRAM cells could be readily stacked into a 3-D cross-point architecture, providing the potential to contribute to a revolution not only in memory technology, but to play a key role in next-generation computing system architectures as well[10,16].

A variety of metals and metal oxides have been characterized for RRAM electrodes and switching layers, respectively. Common insulator materials are binary metal oxides such as TiO_2 or HfO_2. Different materials in varying combinations exhibit different switching characteristics. Common metal (electrode) and binary metal oxide (insulator) materials are shown in figure 1.6 below [16].

In the following section, the basic principles behind the general functionality of a metal oxide RRAM cell as a resistance-switching memory device will be described.

1.8 Metal Oxide RRAM Functionality

The principle behind the basic functionality of any RRAM cell is controllable switching between a high resistance state (HRS) and a low resistance state

(LRS). Through application of a voltage of the appropriate magnitude and polarity at an electrode, the resistance state in the insulator can be changed, leaving the device in a

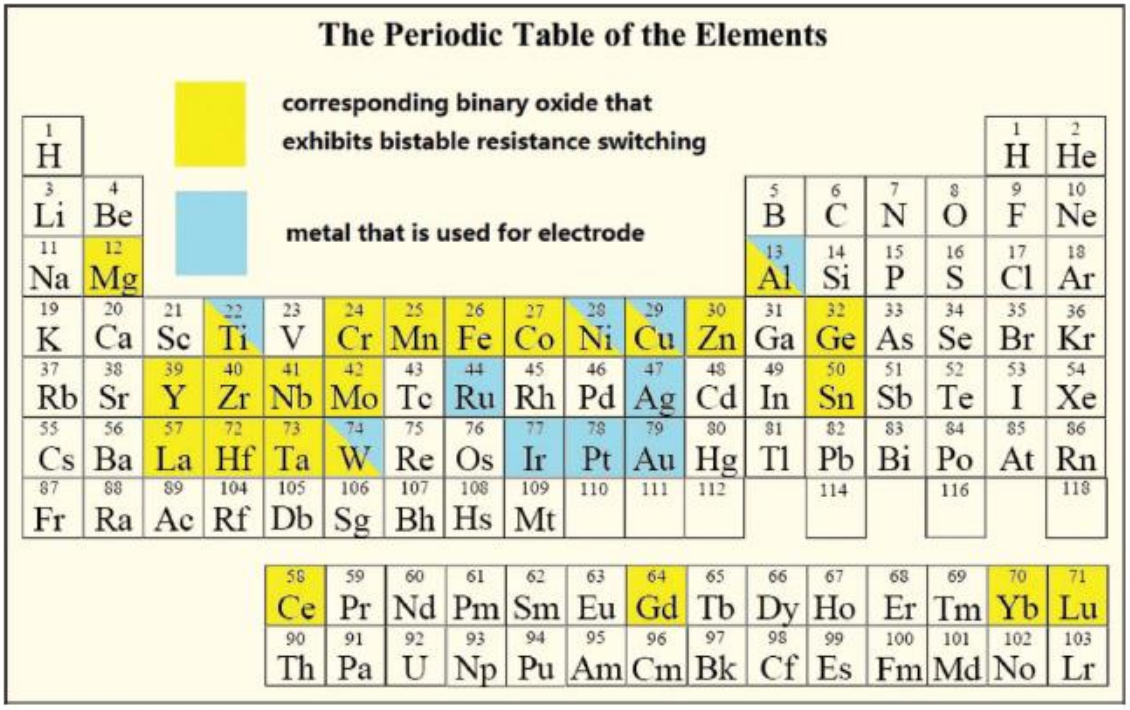


Figure 1.6 Periodic table showing common RRAM electrode (blue) and binary metal oxide (yellow) materials © 2012 IEEE.

stable altered state with respect to its' resistance, where the HRS corresponds to the OFF state, (low current) and the LRS to the ON state (high current). The change from the HRS to the LRS is often referred to as the "set" process, while the shift from LRS to HRS is called "reset". Metal oxide RRAM devices fall broadly into several categories with respect to switching mode as well. If the set and reset operations depend on the polarity of the applied voltage, this is referred to as bipolar switching, due to the necessity of applying two opposite voltage polarities in order to a complete a single ON/OFF cycle. Switching that depends only on the magnitude of the applied voltage and not the polarity is referred to as unipolar switching. When switching behavior is neither polarity- nor

magnitude- dependent, the switching is called non-polar. General i-v characteristics for both the unipolar and bipolar switching modes are shown in figure 1.7 below.

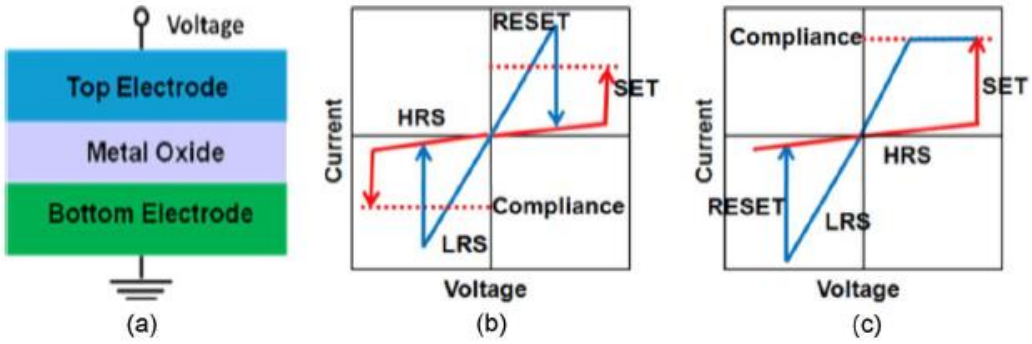


Figure 1.7 a) Diagram of a typical metal oxide RRAM cell. b) Schematic of typical current-voltage characteristics of unipolar switching c) Schematic of a typical current-voltage characteristics of bipolar switching. © 2012 IEEE

For all switching modes, a maximum value of the current allowed to flow through the device, (a "compliance" current), is imposed during the forming and set operations in order to control characteristics of the conductive filament formed during the operation. The forming operation as well the conductive filament will be discussed next.

The application of a voltage across the RRAM cell induces a resistance switching event which is generally agreed upon to correspond to the formation or disruption of a conductive filament (CF) resulting from breakdown of the dielectric layer [16,17,18]. A switch to a LRS corresponds to initial formation or re-formation of a CF, while a switch to HRS corresponds to a disruption of the filament. For some material systems, fresh (i.e., never switched) cells require an initial higher voltage "forming" step in order to form the CF and thereby enable subsequent switching. Set/reset operations in these systems typically occur at lower voltages than that required for the forming step[17]. Application of the forming voltage results in the initial creation of the CF through electrically and

thermally induced diffusion of oxygen anions. A conductive pathway for electrons consisting of oxygen vacancies then remains across the metal oxide layer after the voltage is removed (Figure 1.8a). Reset and set operations, respectively, correspond to the disruption and subsequent re-formation of the CF in the CF/electrode interface region (Figure 1.8b)[19].

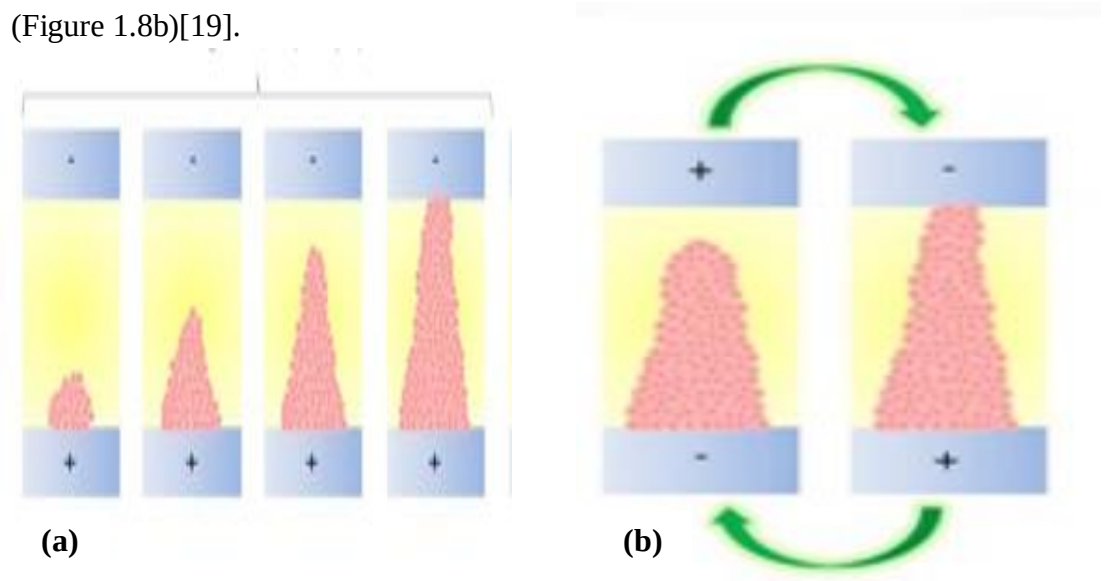


Figure 1.8 RRAM conductive filaments a) Initial formation of a CF during the forming step. b) Schematic showing set/reset operations, which correspond to repeatable formation and disruption of the CF near the insulator/electrode interface, respectively. (Lanza, 2014)

Elimination of the higher voltage initial forming step is sometimes possible through use of appropriate design and processing parameters and insulator/electrode materials and compositions as well [16,20,21]. This is a desirable characteristic for any RRAM application as it allows for reduced energy consumption due to the removal of the necessity to include a higher voltage forming step prior to regular operation.

In the next section, conduction mechanisms through the formed CF will be examined more closely.

1.9 Conduction in Metal Oxide RRAM Cells

The nature of the conduction through the CF in a metal oxide RRAM cell depends on what resistance state the cell is currently in. In the LRS, cells exhibit a linear i-v relationship, typical of ohmic conduction [16,18,22]. In the HRS however, a variety of conduction models may apply, depending on the particular material system in question. Parameters such as dielectric properties of the insulator, fabrication conditions used to create the cell, and properties of the oxide/electrode interface all effect the nature of the formation of the CF. These then determine both the transition between the HRS and LRS as well as the nature of the attendant electron conduction that occurs during set/reset operations [16].The possible conduction paths for electrons traveling through metal oxide RRAM cells in the high resistance state are listed below (see Figure 1.9). Regardless of which form of conduction is dominant for a certain type of cell, electrons will always choose the least resistive path from cathode to anode.

1. *Schottky emmission*: electrons acquire enough thermal energy to overcome the oxide energy barrier and travel directly into the conduction band.(Fig. 1.9.1)

2. *Fowler-Nordheim tunneling (FN)*: when the magnitude of the applied electric field is high enough, band bending in the oxide energy barrier can allow for electrons to tunnel through the narrow portion of the energy barrier into the conduction band. (Fig. 1.9.2)

3. *Direct tunneling*: if the oxide layer is thin enough, application of a voltage across the cell allows for electron tunneling directly from one electrode to another. (Fig. 1.9.3)

If enough defects are present in the oxide layer (e.g. oxygen vacancies), then a variety of trap-assisted conduction mechanisms become possible. In these cases, the path of an individual electron through the oxide layer will always begin with conduction from an electrode to a trap (Fig. 1.9.4), and end with conduction from a trap to an electrode (Fig. 1.9.8). Trap-assisted conduction mechanisms include:

4. *Poole-Frenkel emission*: this occurs when an electron already in a trap acquires enough energy to enter the conduction band (Fig. 1.9.5).

5. *FN-like tunneling*: this effect can occur when an electron is able to enter the conduction band directly from a trap under the influence of a large electric field (Fig. 1.9.6).

6. *Trap-assisted tunneling*: depending on the wave functions of the electrons in question, electrons can "hop" from trap to trap occupying either localized energy states, or in the case of overlapping states, in conduction that resembles metallic conduction (Fig. 1.9.7).

In the next section, the conduction mechanism in metal oxide RRAM cells with HfO_2 as the insulator will be examined in more detail, as this form of RRAM is not only heavily investigated in the research community, but is also the form developed and characterized in the present work.

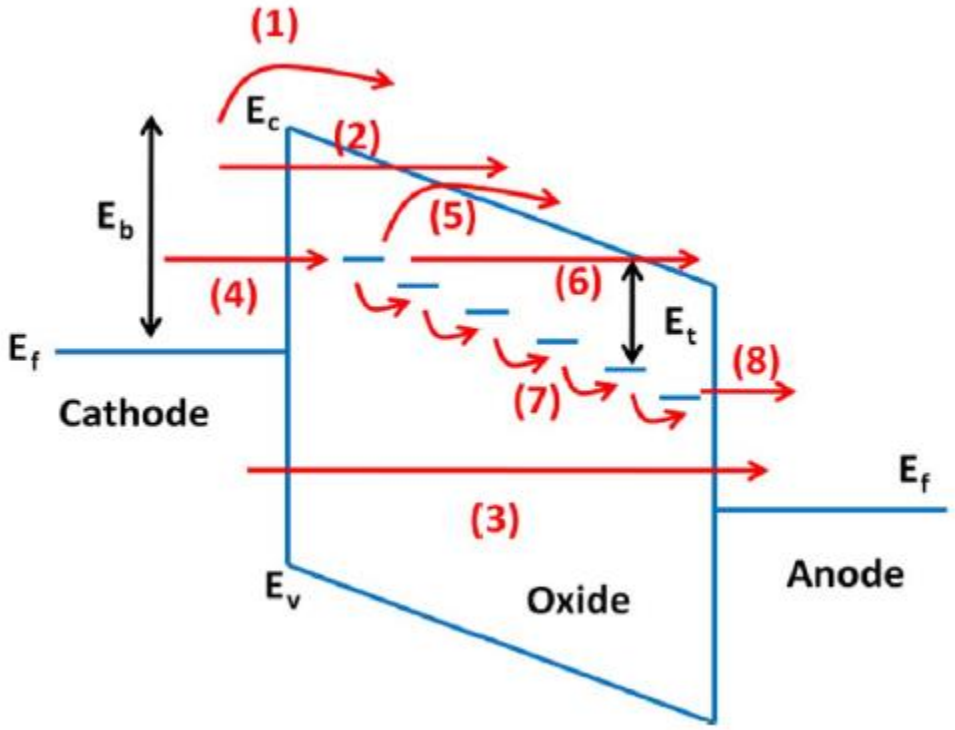


Figure 1.9 Conduction mechanisms through a metal oxide RRAM cell in the HRS (1).Schottky emmission (2).Fowler-Nordheim tunneling (FN) (3).Direct tunneling (4) Conduction from an electrode to a trap (5).Poole-Frenkel emission (6).FN-like tunneling (7).Trap-assisted tunneling(8) Conduction from a trap to an electrode. © 2012 IEEE

1.10 HfO_2-based RRAM

For some time now, HfO_2-based dielectric films have been researched and developed to serve as high-k materials for use in high performance CMOS MOSFETs[16]. For this reason, HfO_2 was a natural candidate for further examination with respect to serving as the insulator material in a metal oxide RRAM cell as well. As it happens, a variety HfO_2-based RRAM devices have proven themselves as viable candidates for NVM[16]. In particular, TiN/Ti/HfO_x/TiN stacks have been shown to demonstrate high switching speed (< 10 ns), large OFF/ON ratio (> 100), good endurance (> 10^6 cycles), long lifetime, and multi-bit storage capabilities[16,23]. HfO_2-based metal

oxide RRAM stacks have also proven themselves to be highly scalable, having been fabricated in cells as small as 10 x 10 nm^2 while still maintaining good performance [16,24].As the focus of this paper is on TiN/HfO_2/TiN RRAM, both the mechanisms for CF formation and electronic conduction in this system will be described in more detail in this section.

When a forming voltage is initially applied across a TiN/HfO_2/TiN cell in a fresh state, in the low bias regime electronic current is dominated by trap-assisted tunneling through oxygen vacancies already present in the insulator layer around HfO_2 grain boundaries (GB's)[18]. Continuing to increase the magnitude of the applied voltage results in the generation of new vacancies at a rate governed by

$$G = G_0 e^{\left(-\frac{(E_A - bF)}{kT}\right)} \tag{1.12}$$

where G is the defect generation rate, G_0 is a rate constant, E_A is the activation energy required to produce an oxygen vacancy, b is a bond polarization factor, F is the magnitude of the applied electric field, k is the Boltzmann constant, and T is the local temperature. We see that generation of new vacancies is strongly influenced by increasing the applied voltage, which increases the magnitude of the electric field across the insulator, lowering the energy barrier for generation of new vacancies.

New vacancy generation also occurs preferentially around already-existing vacancies in the growing CF. This is due to the fact that electron transfer through an individual trap causes distortion of the surrounding lattice, with consequent emission and absorption of phonons that then tend to increase the local temperature. Additionally, the generation of new oxygen vacancies further distorts the lattice, which tends to lower the

activation energy for creation of additional new vacancies. This positive feedback cycle of more vacancies allowing more tunneling, which then leads to higher temperatures and lower activation energies for new vacancy generation, eventually results in formation of the CF consisting of sub-stoichiometric hafnia (HfO_x), which then serves as a permanent conduction sub-band for the electrons[18,25].

Both during CF formation and set/reset operations, the rate of formation/disruption of a filament is also governed by the diffusion rate D, and recombination rate R, of oxygen anions around the CF region, where

$$D = D_0 e^{\left(\frac{-\left\{E_D - Q\frac{\lambda}{2}[F+F_L]\right\}}{kT}\right)} \tag{1.13}$$

and

$$R = R_0 e^{\left(\frac{-E_R}{kT}\right)} \tag{1.14}$$

with D_0 and R_0 the rate constants associated with diffusion and recombination respectively, E_D and E_R the activation energy required for oxygen diffusion and recombination respectively, Q the charge on an oxygen ion, λ the hopping distance to the nearest neighbor lattice site, F the applied electric field, and F_L the local electric field determined by oxygen anions and vacancy charge states[25].

During forming and set/reset operations, oxygen anions both diffuse away from and recombine in the bulk oxide around the CF region [24].After the formation of the CF, the subsequent set/reset operations occur at lower voltages due to smaller values of activation energies required for diffusion and recombination as compared to the energy required for vacancy generation [25]. Consequently, reversible disruption and re-

formation of the CF corresponds to the diffusion of oxygen anions both by Joule heating and electric-field-induced drift over a relatively short distance (~ 1 nm([18,22])) towards or away from the insulator/electrode interface (see Fig.1.8b) [18].

Due to the fact that larger temperatures increase both the rate of creation of new vacancies as well as the rate of diffusion of oxygen ions through the insulator, the values of the compliance current chosen for the forming operation have a significant effect on the size of a newly formed CF, with larger compliance currents leading to larger temperatures, which result in CF's with larger average cross-sectional areas[24].

Bersuker, et. al. formulated an empirical model for the basic conduction mechanisms for a TiN/HfOx/TiN RRAM cell in various resistance states which agreed well with experimental data[18].During the forming step, electronic conduction was found to occur predominantly by multi-phonon trap assisted tunneling (TAT) through oxygen vacancies present in the dielectric layer. In the model, capture of an electron at a trap is associated with the release of energy by phonon emission of

$$\Delta E = m\hbar\omega_0 \tag{1.15}$$

where m is the total number of released phonons, and ω_0 is the frequency of a single phonon. Additionally, release of an electron from an individual vacancy is associated with a gain of energy due to phonon absorption of

$$\Delta E = n\hbar\omega_0 \tag{1.16}$$

where n is the total number of absorbed phonons. Figure 1.10 below shows an energy band diagram for the multi-phonon TAT of an electron through the dielectric layer.

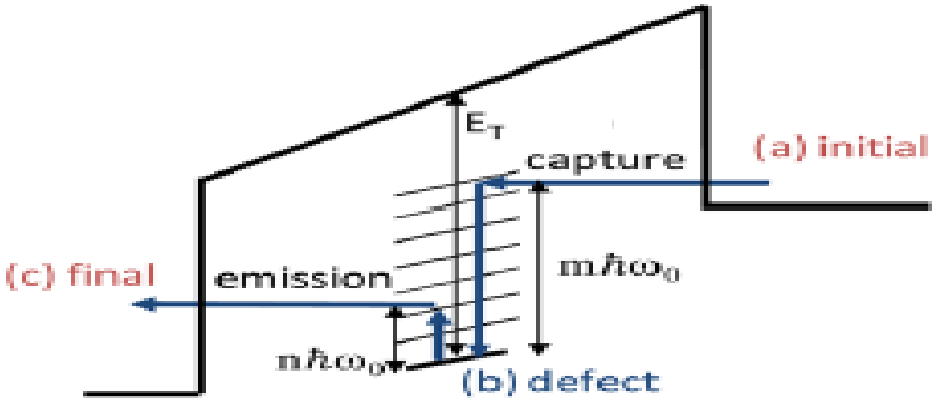


Figure 1.10 Capture and emission of an electron in the multi-phonon TAT model for HfO_x in TiN/HfO_x/TiN RRAM. Copyright 2011, AIP Publishing LLC

Conduction through a path consisting of oxygen vacancies then is described by

$$I_p = \frac{q}{\tau_{C,max}+\tau_{E,max}} \tag{1.17}$$

where I_p is the electronic current through a percolation path, q is the charge on an electron, and $\tau_{C,max}$ and $\tau_{E,max}$ are the time constants associated with capture and emission of an electron to and from the slowest trap on the path, respectively. Time constants are calculated by accounting for each phonon and absorption and emission event, which are themselves determined by a number of factors such as energy levels and density of states at both traps and electrodes, as well as tunneling and occupation probabilities for an electron. As mentioned previously, conduction through a formed filament was found to be essentially metallic (ohmic) in nature [18].

In the next section, the fundamental performance metrics of metal oxide RRAM will be discussed, along with the effects of scaling on these metrics.

1.11 Fundamental performance metrics for HfO_2 RRAM

For any metal oxide RRAM cell, the fundamental device performance metrics are the magnitudes of the LRS, the HRS, the forming voltage, and the reset current (i.e., the current required to initiate the reset operation). How these metrics are related to key processing and material characteristics of a RRAM cell as well as the effects of dimensional scaling on overall cell performance will be discussed in the following.

As conduction through the RRAM cell is related to formation of conductive filaments as discussed previously, control of the size of the CF during the forming step becomes of key importance with respect to subsequent cell performance metrics, particularly with respect to the magnitudes of the LRS, HRS, and reset currents. Because the current travels through a filament which occupies a small region of the electrode, current density through an individual cell will be strongly affected by the size of the CF.As mentioned previously, increasing the magnitude of the compliance current used during the forming step increases the number of oxygen vacancies produced in the insulator layer, and therefore the cross-sectional size of the CF. This relationship between compliance current and filament area for a TiN/HfOx/TiN cell is shown in fig. 1.11 below [22]. Naturally, as the filament area changes, the current density flowing through the cell during the set and reset operations will change accordingly, and hence the power consumption per set/reset operation for a single cell will change as well. Because power consumption is directly related to cost and reliability of electronic devices, control of filament size therefore becomes a key factor in the consideration of the design of an economically viable RRAM cell.

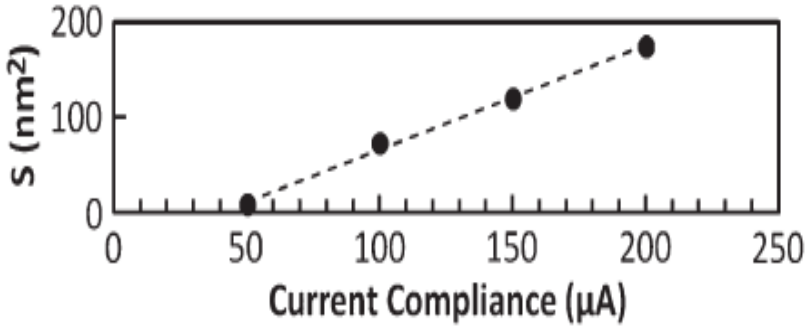


Figure 1.11 Relationship between compliance current and CF cross-sectional area (S) for TiN/HfOx/TiN RRAM. Circles are experimental data values, while the dashed line is a linear fitting. © 2013 IEEE

The larger a filament becomes, the lower the current density through the filament for a given applied voltage becomes. However, for larger filaments, it is also the case that larger current magnitudes are required during the reset operation in order to achieve sufficient oxidation of the filament tip [16,19]. As will be discussed further below, a larger filament will also result in both a larger-magnitude HRS as well as a smaller-magnitude LRS, which will then improve the value of the OFF/ON ratio for the cell. This will come at a cost of greater power consumption however, due to the necessity of a larger compliance current during forming, as well as for a larger reset current during every reset operation. Hence, a trade-off exists between filament size, performance capabilities, and power consumption for a RRAM cell.

As the functionality of a RRAM cell lies in the control of the resistance to electronic conduction through a cell, a viable analytical model of the resistance becomes an important aspect of successful development of a robust RRAM technology as well.

Puglisi, et.al. have proposed an empirical expression for the resistance (R) consistent with experimental data for the TiN/HfOx/TiN system as below[22],

$$R = R_{SET}\left(e^{\left(\frac{x}{\kappa}\right)} - \frac{x}{t_{Ox}}\right) \quad (1.18)$$

$$R_{SET} = \rho_{Hf,CF}\frac{t_{Ox}}{S} \quad (1.19)$$

,where x is the length of the oxidized (recovered) portion of an existing filament, κ is an empirical factor based on a TAT simulation model of current through the insulator from [18], $\rho_{Hf,CF}$ is the resistivity of the filament, t_{Ox} is the thickness of the HfO_2 film, and S is the cross-sectional area of the filament.

The relationship of the filament with the fundamental performance metrics mentioned above will be further examined in the following sections.

1.11.1 LRS

LRS is the value of the resistance through the cell when the CF is in the ON, i.e., non-oxidized state. As equation 1.18 for HfO_x RRAM shows above, LRS corresponds to the condition where x = 0, and therefore is equivalent to $R_{SET,}$ which is essentially ohmic conduction. As R_{SET} is inversely proportional to filament area S, LRS values should decrease with increasing filament area, i.e., with increasing magnitude of the compliance current. Figure 1.12 for Ag/HfO_x/Pt RRAM demonstrates this relationship[26].

Additionally, as LRS is controlled mainly by filament properties, the magnitude of the LRS should be independent of electrode area for a given HfO_x thickness and filament size (i.e., compliance current). The trend in LRS with electrode size is shown for various metal oxide RRAM systems in Fig.1.13(a)[16].

Generally speaking, the more times a cell is switched, the larger the number of oxygen vacancies in the disrupted region becomes, eventually leading to a permanent LRS or ON state for an individual cell, a characteristic sign of device failure[16].

1.11.2 HRS

The magnitude of the HRS in a HfOx RRAM cell that has previously undergone a forming operation is primarily controlled by the distance x (equation 1.18) near the

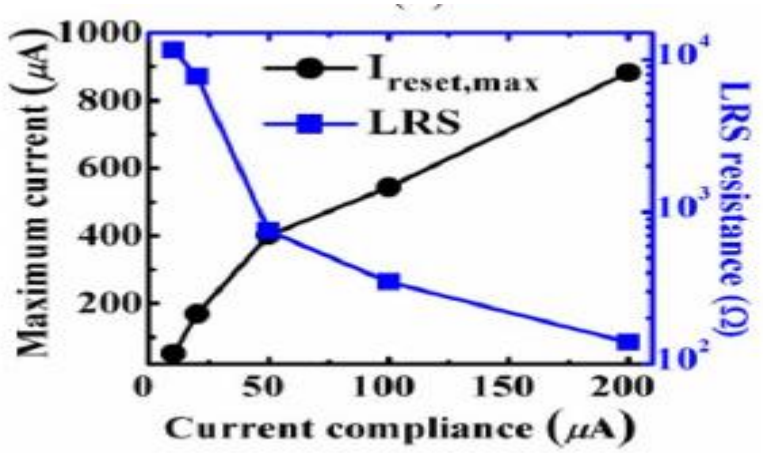


Figure 1.12 Relationship between compliance current and LRS for Ag/HfOx/Pt RRAM. The blue curve shows decreasing LRS with increasing compliance current. ©2014 IEEE

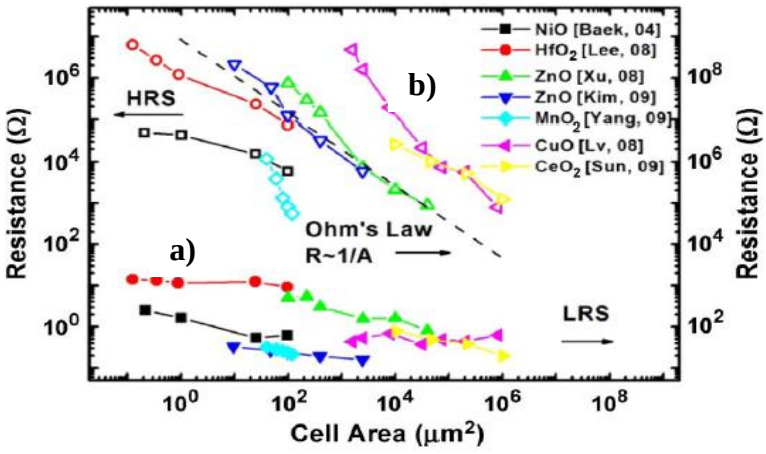


Figure 1.13 a) Relationship between cell area and LRS for a variety of metal oxide RRAM systems (HfO_2 shown in red). b) Relationship between cell area and HRS for a variety of metal oxide RRAM systems. © 2012 IEEE

insulator/electrode interface region over which a filament has been re-oxidized, and thus effectively 'ruptured' in terms of electrical performance [16,18,19,22].Variation in these distances is related to the magnitude of the reset voltage[22], and also by the stochastic nature of the diffusion/recombination of atoms[16]. Equation 1.18 suggests that the total magnitude of the HRS in this system can be thought of as the sum of two series resistances, one resistance due to the length of the ruptured filament, and one resistance due to the remaining unaffected length[22]. The resistance associated with the re-oxidized filament tip (ruptured region) is represented by the exponential term, i.e., an increase in the length x of the re-oxidized region of the filament corresponds to an exponential increase in resistance, while the resistance through the remainder of the filament is ohmic [22].

The HfO_x RRAM HRS shows variability not only with length of the disrupted region but with device area as well, generally increasing with decreasing cell area (see fig. 1.13 (b) above). Set and reset voltages show a slight increase in magnitude with decreasing cell area [24], which can therefore lead to larger diffusion and recombination rates by equations 1.13 and 1.14 respectively. These larger rates therefore result in a larger value of x in equation 1.18, and correspondingly to a larger value of the HRS after reset. While filamentary current describes the resistance characteristics of RRAM cells reasonably well, it is also probable that direct tunneling through the dielectric layer occurs simultaneously with filamentary current. Therefore, another reason for increased HRS with decreasing device area could be that area-dependent direct tunneling dominates the total current through the cell as the total cell area approaches the total area of the switching layer over which conductive filaments have been formed.

1.11.3 Forming Voltage

Forming voltage is a fundamental performance metric for a metal oxide RRAM cell due to the fact that material systems requiring a forming step cannot undergo regular set/reset operations until a CF has been formed. The magnitude of the forming voltage then naturally becomes an important consideration. As larger forming voltages mean more power consumption per cell, reducing this value as much as possible becomes advantageous in order to reduce overall power consumption.

For a HfO_2 RRAM cell, the magnitude of the forming voltage is significantly affected by oxide thickness [24].Figure 1.14 below shows change in forming voltage with thickness of HfO_2 films, with the inset indicating the disappearance of a forming step altogether when the oxide thickness is reduced to 2 nm.

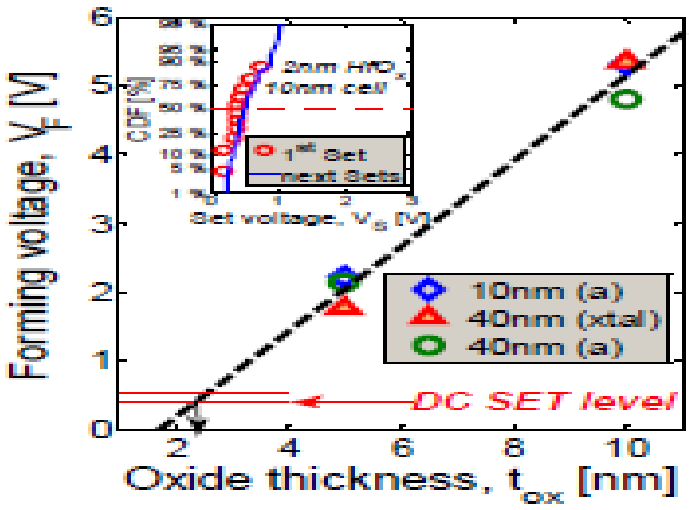


Figure 1.14 a) Relationship between oxide thickness and forming voltage for HfOx RRAM. ©2011 IEEE

The presence of defects in the un-switched HfO_2 –based metal oxide RRAM cell also plays an important role in determining the magnitude of the forming voltage required to form a CF[16,24]. As mentioned previously, the CF is initially formed due to voltage stress build-up that occurs preferentially at hafnia GB's. Reduced electrode area naturally corresponds to a reduced number of GB's present in the un-switched insulator near the electrode/insulator interface. Because new defect generation occurs preferentially at pre-existing defect sites, the reduced number of pre-existing defects present in the reduced cell area thereby increases the amount of voltage stress required to initiate new defects, which then increases the magnitude of the forming voltage required to produce CF's in smaller cells. This effect is demonstrated in [24], in which it was found that for larger cell sizes, crystalline hafnia required lower forming voltages as opposed to amorphous hafnia, while for smaller cells, this condition is reversed, with amorphous hafnia cells exhibiting the smaller forming voltages [24]. Figure 1.15 below shows the trend in forming voltage magnitude with electrode area for both crystalline and amorphous hafnia [24].

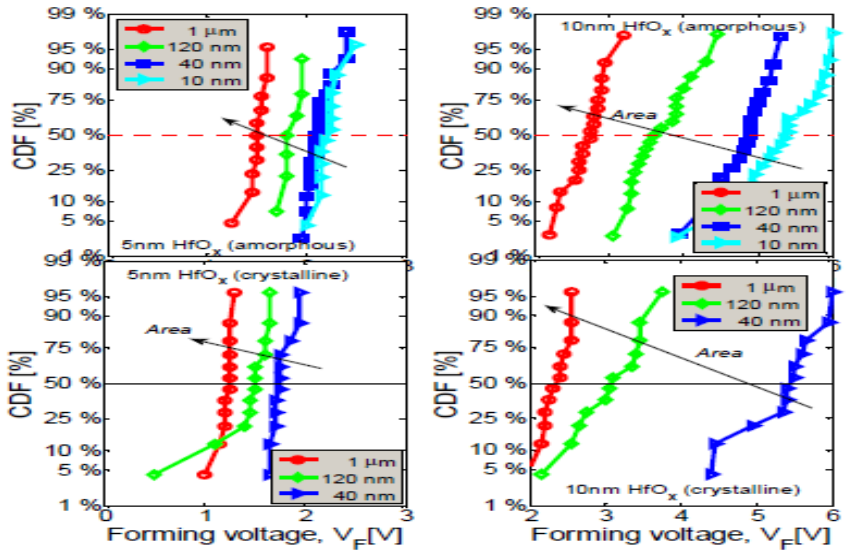


Figure 1.15 Data for both amorphous and crystalline HfO_x RRAM showing increasing magnitude of the forming voltage with increased hafnia thickness and decreased cell area ©2011 IEEE.

1.11.4 Reset Current

The magnitude of the reset current is a key parameter for economically viable RRAM functionality because maximum power consumption during set/reset operations will naturally occur during the reset operation, i.e. during the transition from the LRS to the HRS. Due to a temperature gradient across the insulator generated during the forming step, the CF tends to be smaller at the forming cathode (see fig.1.8).Concurrently, a larger resistance to electronic current is therefore experienced in this region, leading to higher temperatures generated during the reset voltage sweep which then contribute both to the re-oxidization of the filament tip as well as significant current noise due to structural instability associated with the diffusion/recombination process [18]. For HfO_2 RRAM systems, magnitude of the reset current has been found to trend linearly with the magnitude of the compliance current, and therefore with CF size (see fig 1.16 below).

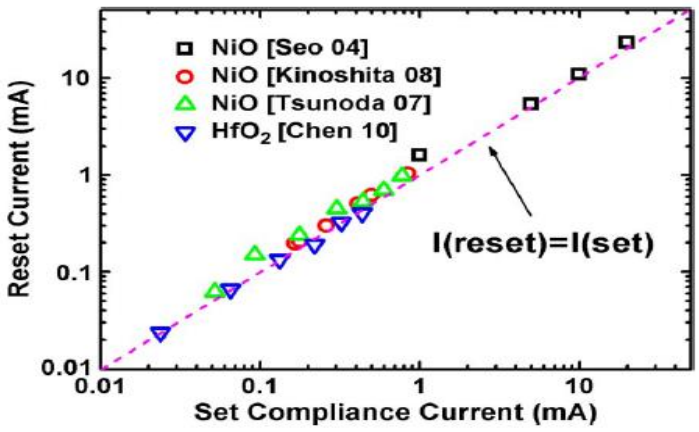


Figure 1.16 Data for NiO and HfO_2 RRAM systems showing linear relationship of reset current with compliance current. (HfO_2 RRAM shown in blue). © 2012 IEEE

Consequently, the best strategy for minimizing power consumption of a metal oxide RRAM cell is to reduce the magnitude of the compliance current.

Reset current plays an important role in scaling considerations as well. As current through a RRAM cell in the LRS is primarily filamentary, the amount of current required in the reset operation to induce filament tip rupture is roughly the same regardless of cell area. However, as cell area is reduced, current density naturally goes up, which can cause problems of unwanted high temperature during device operation due to power handling considerations in memory cell selection or current limiting devices associated with the memory cell, which then can have various negative effects on the performance of the cell or of a circuit of which it is a part [16].The primary strategy for addressing this challenge for scaled devices is again to reduce the magnitude of the reset current by reducing the magnitude of the compliance current.

1.12 Thesis overview

In this chapter, a background was provided on non-volatile memory, and in particular the form of NVM typically referred to as flash memory. Different tunneling mechanisms employed in the operation of flash cells were described as well as challenges facing the continued scaling and performance improvements for flash. Memristors were then discussed from a theoretical and historical perspective, and the suggestion made that memristive systems could offer one way forward for the NVM market. A memristive system generally referred to as metal oxide RRAM, in particular metal oxide RRAM with HfO_2 as the oxide material, was described with respect to functionality, conduction mechanisms, and fundamental performance metrics, as RRAM of this type has proven to be a viable candidate for addressing the scaling issues associated with NVM and flash. In

this work, a fabrication process for nano-scale cross-point TiN/ HfO_2/TiN RRAM devices will be developed and described. Materials processing challenges will be addressed. The switching performance of devices fabricated by this process will be compared to the performance of similar devices from the literature in order to confirm process viability. In chapter 2, the design and fabrication process as well as processing and design challenges that were identified and addressed during development will be presented and described. In chapter 3, the electrical performance of these RRAM cells will be characterized and compared with the performance of similar devices from the literature, with a focus on the connection between device area and switching behavior. Chapter 4 provides conclusions as well as suggestions for future work.

Chapter 2

DESIGN AND FABRICATION OF HfO_2 RRAM

In this chapter, the design and fabrication process of the RRAM will be explained. Descriptions and the associated processing overviews for two designs (design 1 and design 2) will be provided, as well as descriptions of the relevant design and processing challenges that emerged and how these challenges were addressed in order to successfully fabricate nano-scale cross-point HfO_2 -based RRAM.

2.1 RRAM Device Design Considerations

A significant design challenge associated with RRAM as a viable NVM application is related to uniformity of the switching behavior [16]. This necessitates strict control over formation of the CF, due to the strong connection between size of the CF and the magnitudes of all of the fundamental performance metrics of the RRAM cell. As mentioned in the previous chapter, there is a strong connection between compliance current and the CF. Additionally, strict control of the forming current is necessary in order to achieve stable multi-level switching, which could greatly increase data density through controlling the size or number of the CF's[16].

A variety of design solutions have been researched to address the issue of strict control of CF size, many of which involve the inclusion of current limiters such as transistors or diodes in the design of a memory device cell in order to limit current overshoot during the forming operation[11,16]. While integration of these devices into the memory cell design can effectively offer more precise control over the current through the MIM stack, new problems with scaling limits and parasitic electrical effects

due to the presence of the current limiting elements then arise, greatly magnifying the already significant challenge of achieving all of the benchmarks for viable NVM applications mentioned in chapter 1.

A possible alternative to the inclusion of a current limiting device in a memory cell is the arrangement of the RRAM cells in a cross-point array in a manner similar to that shown in figure 1.4. If the memristive system being employed has a significantly high degree of non-linearity in the switching behavior, the resulting OFF/ON ratio for an individual cell can be high enough to exhibit desirable resistance read-out characteristics while simultaneously preventing unwanted leakage currents from the cell during read-out or programming of itself or of neighboring cells. This effect then also eliminates the space and power requirements associated with the inclusion of a current limiting device on a per-cell basis. The simple cross-point structure also shows great potential for stacking of memory cell arrays in three dimensions, thereby making significantly increased data density possible by increasing overall device density [10,11,12,16].

For these reasons, a cross-point design was chosen as the primary design of the HfO_2 RRAM described in this work.

2.2 Design 1

Design 1 was a 5-lithography-level cross-point device structure employing both optical and direct-write lithography for feature patterning. The cells were arranged in arrays consisting of nine device cells each (see fig.2.1(a)). Nominal electrode widths ranged from 40 nm – 1 μm (1 electrode size per array). In order to facilitate the patterning of nano-scale electrodes, a hydrogen silsesquioxane (HSQ) -based negative

electron beam lithography (EBL) resist was chosen (product name XR-1541). Due to the difficulty associated with complete removal of HSQ, however, an additional positive EBL resist, poly-methyl-methacrylate (PMMA), was used as a sacrificial under-layer, in a process similar to that used for patterning Si nano-wires in previous work [27].Fig 2.1(b) shows a cross-section of a single device array.

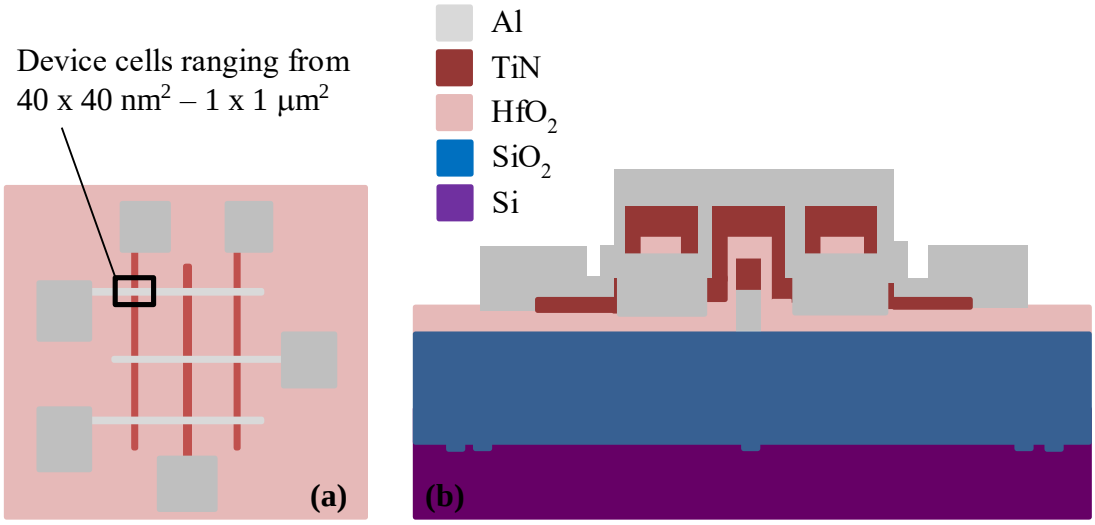


Figure 2.1.Design 1 RRAM (a) Top view of a single 9-cell cross-point device array (b) Cross-section of a 9-cell cross-point device array.(Figures not to scale)

2.3 Process development

In order to determine appropriate processing parameters that would result in device features as close as possible to the nominal design values, process development experiments were performed in order to develop process steps that would produce the desired feature sizes, as well as stable, functional post-etch device patterns in both resist and metal stacks. These experiments are described in the following.

2.3.1 Determination of electron beam dosage for patterning HSQ

For design 1, the electrodes were initially patterned in the HSQ over-layer through EBL, then the pattern was subsequently transferred to the PMMA under-layer with a low pressure O_2 etch, and finally to the metal stack with a Cl/Cl_3 etch. Hence, control of electrode size is primarily determined by the electron beam dosage chosen for the initial patterning in HSQ. HSQ has been under investigation as a negative EBL resist since 1997due to its' demonstrated ability to produce stable sub-20-nm features with good etch resistance, low line edge roughness, and small molecular size [28, 29].HSQ is an oligomer with a cage-like structure with the general formula $[HSiO_{3/2}]_n$, which in a resist solution forms a random network of partially connected structures. Upon exposure to an electron beam, the Si-H bonds are broken, subsequently forming unstable Si-OH groups which then condense, breaking down the cage-like network and forming a linear network of strong SiO bonds[30].

A key step in establishing the correct dosage that will result in the desired electrode size in HSQ after e-beam exposure is establishing what is called a base dose. The base dose for an exposure is essentially a dosage standard that represents complete exposure of the HSQ, i.e., a more or less complete reaction of all the oligomers in the resist, thus leading to a maximum post-exposure thickness. The base dose can then be used as a reference in the tool control code with respect to any desired changes in beam dosage in single exposure, or between different exposures used to monitor resist performance. To establish the base dose, an appropriate dosage range is chosen based on material data sheets, and a set of structures whose feature size is easily measured are exposed to the entire dosage range. Subsequent measurement of the exposed features can

then help identify the dosage at which complete exposure was achieved. This dose can then be identified as a base dose value. By using a base dose as a basis for identifying an optimal dosage range for an exposure, the desired feature sizes for patterns can be more readily achieved. Data for base dose determination for HSQ exposure as determined from the exposure and subsequent height measurement of 75 x 75 μm^2 is shown in Fig. 2.2 below. Note that a base dose of 2000 $\mu C/cm^2$ was chosen for electrode patterning for design 1.

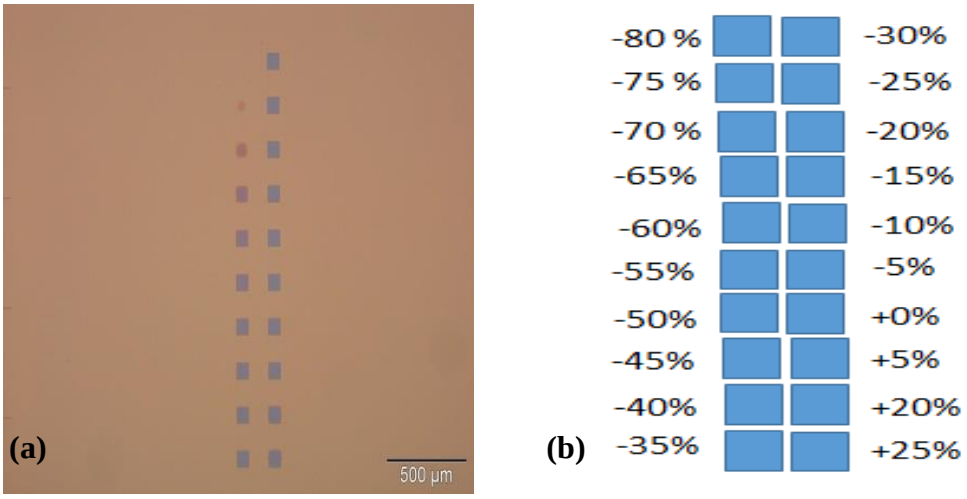


Figure 2.2 Base dose determination (a) Post-exposure characterization squares of patterned HSQ. The blueish squares are more fully exposed, while the reddish and/or incomplete squares are under-exposed. (b) Typical dosage assignments for an exposure. +0% corresponds to choice of reference dose in the tool code. The dosage that led to greatest feature height then becomes the base dose for subsequent exposures.

Once a base dose has been established, an appropriate dosage range for exposure of the desired structures can then be chosen. A range of doses is often chosen to account for the stochastic nature of the beam/resist reaction, or to optimize exposure conditions for a particular sample or feature. Confirmation of desired feature sizes can be confirmed by SEM (Figure.2.3)

The processing steps for design 1 are described in the following section (for recipe details, see Appendix A).

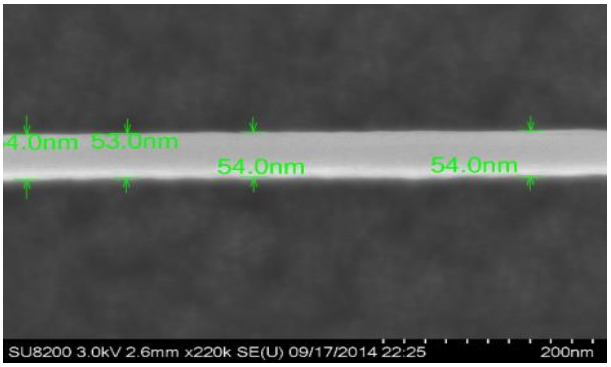


Figure 2.3 SEM image of a design 1 RRAM electrode structure patterned in HSQ on PMMA.

2.3.2 Design 1 Process Flow

- **Substrate cleaning**: Test-grade p-type Si wafers are cleaned by standard AMI cleaning (acetone rinse to remove organic contaminants, methanol rinse to remove any ionic species present on surface, isopropyl alcohol (IPA) rinse to remove any remaining residues).
- **Patterning of EBL alignment marks**: wafer-level and die-level alignment marks must be etched into the Si wafer in order to facilitate pattern alignment between the EBL levels. Etched marks are preferable to metal marks in order to simplify mark detection during subsequent processing on the JEOL 9300FS electron beam lithography system. In order to produce the etch pattern, positive EBL resist (PMMA (6%)) is used as the resist mask. After exposure, the wafer is developed in a 1:1 methyl-isobutyl-ketone (MIBK)/IPA bath , then rinsed in IPA and dried with N_2.

- **Etching of EBL alignment marks into Si wafer**: with the wafer- and die- level alignment marks patterned in the PMMA(6%) ,deep reactive ion etching (DRIE) is performed on the wafer + resist pattern through alternating passivation/etch steps in SF_6/C_4F_8 plasmas, respectively. Approximate desired final mark depth in Si of 2-3 μm can be confirmed by profilometry performed on test patterns.
- **Resist strip**: after the Si etch, the resist mask is stripped by 30 min. soak in 1165 resist remover at a temperature of 120° C.
- **Deposition of buffer oxide**: after an AMI clean, PECVD SiO_2 is deposited on the wafer at a nominal thickness of 300 nm in order to electrically isolate MOR cell arrays devices from the Si substrate.
- **Bottom electrode metallization**: a metal bi-layer of 70 nm of PVD –deposited TiN on 100 nm of evaporation-deposited Al serves as the bottom electrode. The higher –conductivity Al layer is included to enhance electronic conduction through the MIM cells.
- **Patterning of bottom electrodes**: in order produce the electrode structures, first the above-mentioned EBL resist bi-layer is spun in two steps, the first step being the spinning of a PMMA(2%) under-layer and the second being the spinning of the HSQ. After the resist layers are applied, the electrodes are patterned by the JEOL in the negative resist only (top layer), then developed in a 25% tetra-methyl ammonium hydroxide (TMAH) solution. The PMMA under-layer between the electrode structures is then etched away by reactive ion etching (RIE) in a low-pressure O_2 plasma, and finally the metal electrodes are patterned by RIE in a

Cl/Cl_3 plasma. The bi-layer resist mask is then removed in a sonicated acetone bath. Figure 2.4 below illustrates the steps involved in electrode patterning.

- **Descum**: in order to ensure the removal of any remaining resist residue from the surface of the newly patterned bottom electrode, a brief etch is performed in an O_2 plasma.
- **Deposition of active dielectric**: deposition of the 5 nm-thick HfO_2 film which will serve as the switching layer is performed by atomic layer deposition (ALD)
- **Top electrode metallization**: a metal bi-layer of 100 nm of evaporation-deposited Al on 70 nm of PVD –deposited TiN serves as the top electrode of the MIM structure.
- **Patterning of top electrodes**: patterning of the top electrodes follows a similar series of steps as indicated in Fig.2.4 below
- **Patterning of openings in the dielectric layer**: in order to facilitate metal –to-metal contact between the surface of a bottom electrode and the metal pad which will serve as its' electrical contact,20 x 20 μm^2 openings are patterned in the dielectric film using optical lithography. A negative photoresist (NR-9) is spun onto the wafer, then given a pre-exposure bake at 150°C for 1 minute. The wafer is then exposed using a 365 nm wavelength, post-baked at 100°C for 1 minute, and the resulting pattern is then developed in RD-6.
- **Etching of openings in the dielectric layer**: electrode openings are etched in a 6:1 buffered oxide etch (BOE) solution for 2 minutes.
- **Descum**: in order to ensure the removal of any remaining residue from the surface of the bottom electrode, a brief etch is performed in an O_2 plasma.

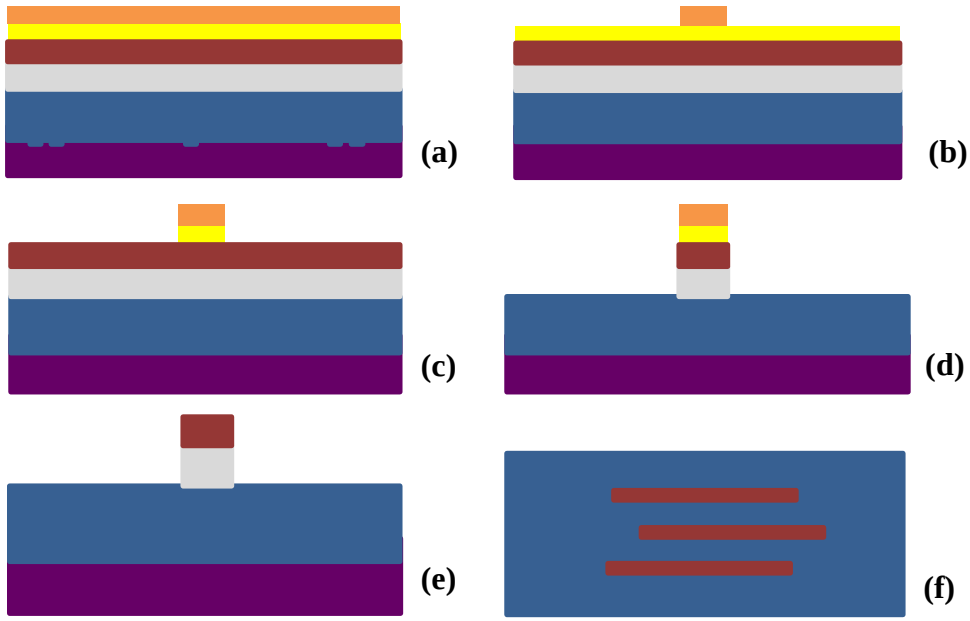


Figure 2.4 EBL patterning of bottom electrodes for design 1 (a)Spinning of PMMA/HSQ bi-layer (b)Patterning of HSQ by EBL (c) Patterning of PMMA by oxygen plasma etch (d) Patterning of Al/TiN bi-layer by chlorine plasma etch (e)PMMA/HSQ bi-layer stripped in acetone (f) Overview of completely patterned electrodes

- **Electrical contact/text/border patterning**: the electrical contact pads, device cell labels and borders, are patterned in NR-9 by optical lithography, using the same steps as those used for patterning the openings in the dielectric layer.
- **Contact pad metallization**:450 nm of Al is then deposited onto the patterned wafer.
- **Lift-off**: removal of the resist under-layer and unwanted metal regions is performed by soaking in acetone.
- **Forming gas anneal**: finished wafers are then annealed in forming gas (90% N_2, 10% H_2) for 30 min. at 400°C.

2.4 Characterization of Design 1 Outcomes

Once design 1 devices were successfully fabricated, their electrical performance was characterized by taking current-voltage measurements as described below. Physical characterization of test structures fabricated in order to analyze current through the device cells was also performed in order to develop strategies for process improvement.

For the first run design of 1, overall yield of devices that exhibited any switching behavior,(repeatable or not), was quite low. Typical current-voltage behavior for a design 1 memory cell regardless of electrode size or physical location on a wafer was characterized by uniform low currents across a wide voltage range as indicated in Figure.2.5. As this behavior indicated a process-level issue, the fabrication process was

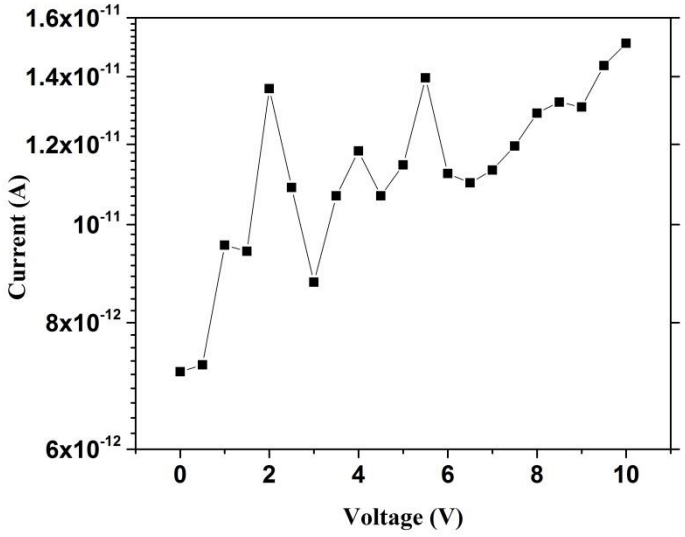


Figure 2.5 Typical current-voltage performance of design 1 RRAM.

repeated in order to ensure that no fabrication errors had occurred, with similar outcomes. In order to get a deeper sense of the poor electrical performance in the finished devices, several locations on individual device cells from the second run were examined for i-v performance. Conductivity was found to be poor through the bottom and top electrodes as opposed to the contact pads, i.e., measurements between either contact-electrode locations or electrode-electrode locations showed negligible conduction. As standard post-process-step cleaning approaches of electrodes were performed during processing of both bottom and top electrodes, other possible effects due to resist residues were taken under consideration. Closer examination of the literature revealed cross-linking of the PMMA under-layer under sufficiently large EBL beam dosages as a possible culprit preventing through-cell conduction. Test structures were then designed and fabricated in order to examine the effect on post-processing electrode conductivity for a range of EBL beam dosages performed on the resist bi-layer. The following section will discuss the PMMA cross-linking issue as well as the conductivity experiment in more detail.

2.5 Effect of beam dosage on PMMA cross-linking

As indicated previously, PMMA was chosen as a sacrificial under-layer for the purpose of facilitating the easy removal of HSQ, which is known for being difficult to remove completely after being exposed and developed [27]. However, PMMA can serve as a high resolution positive or negative EBL resist, depending on the choice of EBL dosage. Positive feature patterning involves scission of polymer bonds by the exposure medium, while negative patterning relies instead on cross-linking. If a PMMA film is exposed to an electron beam dosage approximately 30 times higher than the dosage required for positive feature patterning of the film, the crosslinking effect between

PMMA chains dominates as opposed to the scission effect that dominates at more moderate doses [31,32].This cross-linking then makes subsequent removal of the exposed and developed PMMA highly resistant to standard solvents and etchants[31].

Upon learning this information, it was suspected that the dosages chosen to pattern the HSQ may have been sufficient to cross-link the PMMA under-layer, thus rendering the resist removal techniques used in the design 1 process flow insufficient to remove the cross-linked PMMA that would be present after the HSQ exposure due to cross-linking. This cross-linked residue could then naturally serve as a powerful insulator, limiting or even preventing through-thickness conduction through both the top and bottom electrodes, or prevent complete removal of the HSQ over-layer.

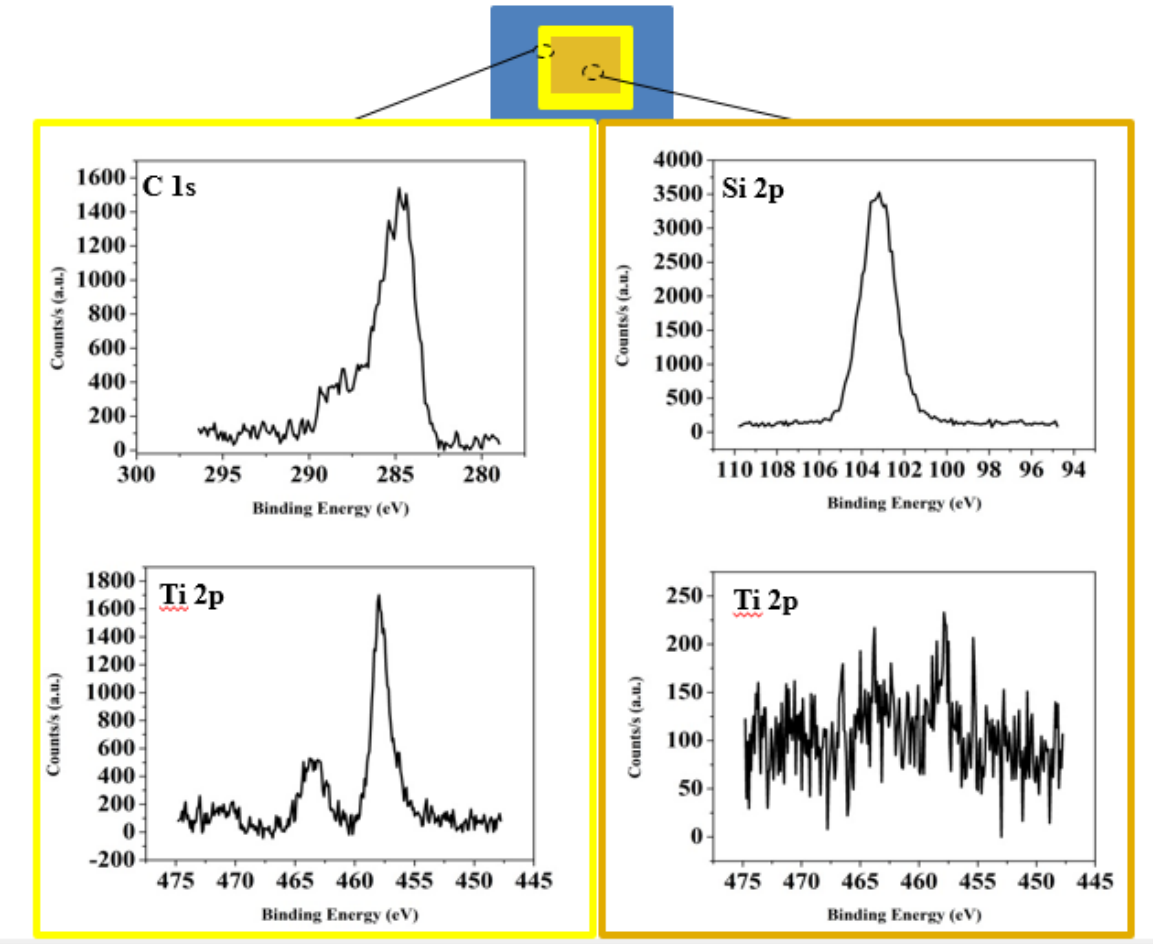
In order to explore the effects of the chosen HSQ exposure dosage on the PMMA under-layer, an experiment was performed in order to examine the electrode surfaces for the presence of PMMA residue after exposure of the HSQ/PMMA bi-layer to an electron beam dosage sufficient to pattern stable structures ranging from 50 nm- 10 μm in width in HSQ, using the same process parameters as those used in fabrication of design 1 devices. Physical and electrical characterization was performed on 200 x 200 μm^2 TiN test structures processed simultaneously in the same manner. Typical results of XPS and electrical resistivity tests performed on test structures exposed over a dosage range of 2000-6000 $\mu C/cm^2$ are shown in Figure.2.6 and Table 2.1 below respectively. Test structure surfaces often showed two distinct regions after resist removal steps were performed (see Fig. 2.6). The XPS data from the outer region suggests that a carbon residue still remained after cleaning (presumably due to cross-linked PMMA), although the Ti signal from the metal beneath was present. More importantly, however, is the

presence of a strong Si signal from the inner region of the test structure surface (beige inner square). The strong remaining presence of Si after cleaning presumably indicates bonding between the PMMA and HSQ that occurs during exposure,or that the inability to remove the cross-linked PMMA under-layer somehow then hindered the removal of the HSQ over-layer as well. In support of the XPS data which confirmed heavy residue remaining after cleaning, the resistivity measurements taken on the test structure surfaces shown in Table 2.1 clearly show values of the resistivity approximately 2 orders of magnitude larger than what is expected from TiN with no insulating resist residue present. These results were typical for the entire selected dosage range.

These results made it clear that additional steps would be required in the process flow in order to ensure the removal of the remaining PMMA+HSQ residues and thus to achieve a reasonable device yield at process end. This was problematic however, as the etchants necessary to ensure complete removal of the HSQ would also severely damage both the electrode metals as well as the buffer and functional oxides beneath. The solution chosen for this processing challenge was to create a new design that would not require the use of HSQ for patterning of the electrodes. This second design (design 2) will be discussed in the following sections.

2.6 Design 2

As mentioned above, the primary motivation for design 2 was to eliminate the use of HSQ, in order that the issue of the relative difficulty of its' complete removal could be avoided. However, a cross-point device configuration and similar device sizes (nanometer through micron scale range) were still required.



(a) **(b)**

Figure 2.6 XPS data for two different regions on the surface of a TiN test structure after removal of exposed and developed HSQ/PMMA. (a) Outer region (yellow) shows presence of carbon residue, though Ti signal is still present (b) Inner region (beige) shows presence of HSQ residue (SiO) thick enough to mask the XPS signal from the Ti underneath.

Hence, a design that used a high resolution positive EBL resist for the active device area patterning as opposed to negative resist became the goal. The final EBL resist chosen was PMMA. The processing steps for design 2 are described in the following section (for recipe details and tool control codes, see Appendix B). Fig 2.7 shows an overview and cross-section of the relevant modifications made to the basic device cell design.

Table 2.1 Resistivity of TiN after PMMA/HSQ Removal

Dosage ($\mu C/cm^2$)	TiN Resistivity ($\mu\Omega$-cm)
0	110-170
2000	22,871
3000	19,180
4000	19,277
5000	19,258
6000	18,943

2.6.1 Design 2 Process Flow

- **Substrate cleaning**: test-grade p-type Si wafers are cleaned by standard AMI cleaning.
- **Patterning alignment marks**: alignment marks are produced in a fashion similar to that in design 1 in different locations apropos to design 2, having similar dimensions and still serving the same function (wafer- and die- level alignment between multiple lithography levels).
- **Etching of alignment marks into Si wafer**: alignment marks are etched in the same fashion as in design 1.
- **Resist strip**: after the Si etch, the resist mask is stripped by 30 min. soak in 1165 resist remover at a temperature of 120° C.

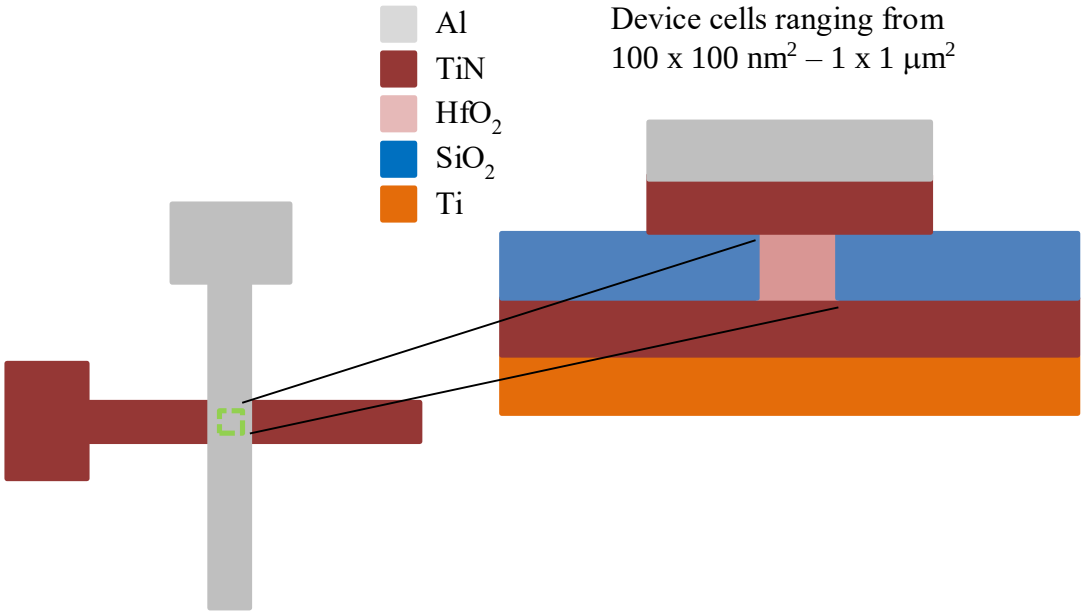


Figure 2.7 Single device cell for design 2. Device cell arrays still consist of 9 cells in cross-point configurations, however individual cells are now patterned with positive EBL resist to create holes in SiO_2 which are then filled with the dielectric switching material (HfO_2)

- **Deposition of buffer oxide**: after an AMI clean, PECVD SiO_2 is deposited on the wafer at a nominal thickness of 300 nm in order to electrically isolate device devices from Si substrate.
- **Bottom electrode metallization**: a metal bi-layer of 100 nm of PVD –deposited TiN on 100 nm of PVD –deposited Ti serves as the bottom electrode. The extra Ti layer is added in order to improve electron conduction through the entire MIM cell.
- **Patterning of bottom electrodes**: in order produce the electrode structures, first optical negative photoresist NR-9 is spun onto the wafer, then given a pre-exposure bake at 150°C for 1 minute. The wafer is then exposed using a 365 nm wavelength, post-baked at 100°C for 1 minute, and the resulting pattern is then

developed in RD-6. The metal layers are then etched away by RIE in a Cl/Cl_3 plasma.

- **Descum**: in order to ensure the removal of any remaining resist residue from the surface of the newly patterned bottom electrode, a brief etch is performed in an O_2 plasma
- **Deposition of buffer oxide**: after an AMI clean, PECVD SiO_2 is deposited on the stack at a nominal thickness of 300 nm. This layer is deposited in order to electrically isolate devices from one another as well as prevent leakage current from the bottom electrode directly to the top electrode during set/reset.
- **Patterning of device cell openings**: first , PMMA(6%) is spun onto the sample and pre-baked before exposure for 1 min. at 180° C. After the resist is applied the openings are patterned, and subsequently developed in a 1:1 MIBK:IPA solution at room temperature for 2 minutes.
- **Etching of SiO_2 buffer layer**: to create the device openings, the SiO_2 is etched in a C_4F_8 plasma, followed by a brief O_2 plasma "flash" performed to remove any fluorocarbon residues that remain on the base or sidewalls of the etched hole.
- **Resist strip**: after the SiO_2 etch, the resist mask is stripped by 30 min. soak in 1165 resist remover at room temperature.
- **Deposition of active dielectric**: deposition of the 5 nm-thick dielectric film which will serve as the switching layer is performed by ALD.
- **Top electrode metallization**: a metal bi-layer of 400 nm of evaporation-deposited Al on 100 nm of PVD –deposited TiN serves as the top electrode of the MIM structure.

- **Patterning of top electrodes**: patterning of the top electrodes follows the same series of steps as those above used to pattern the bottom electrodes.
- **Descum**: in order to ensure the removal of any remaining resist residue from the surface of the newly patterned bottom electrode, a brief etch is performed in an O_2 plasma
- **Patterning of bottom electrode openings**: in order to facilitate good probe contact with the bottom electrode, openings are patterned in the SiO_2 film using optical lithography. A negative photoresist (NR-9) is spun onto the wafer, then given a pre-exposure bake at 150°C for 1 minute. The wafer is then exposed using a 365 nm wavelength, post-baked at 100°C for 1 minute, and the resulting pattern is then developed in RD-6.
- **Descum**: in order to ensure the removal of any resist residue from the surface of the bottom electrode, a brief etch is performed in an O_2 plasma
- **Anneal**: finished wafers are then annealed in N_2 for 30 min. at 600°C.

2.7 Characterization of Design 2 Outcomes

Once design 2 devices were successfully fabricated, their electrical performance was characterized (see chapter 3 for data and characterization details). While device yield was low, enough devices exhibited complete on/off cycles and/or repeatable switching to allow for characterization of the devices as viable RRAM, as well as comparison with the literature with respect to the performance metrics described in chapter 1.

2.8 Chapter Summary

In this chapter, design considerations for RRAM were briefly discussed. Next, a first device design and fabrication process was described as well as the emergent challenges identified and addressed. The chosen solution was a second design that showed significantly improved performance outcomes. Characterization of these devices with the respect to the relationship between the device area, conductive filament, and fundamental performance metrics will be provided in the next chapter, along with comparison to the performance of similar devices from the literature.

Chapter 3
CHARACTERIZATION OF HfO_2 RRAM

Nano-scale cross-point HfO_2 RRAM devices fabricated as described in the previous chapter demonstrated switching characteristics in good agreement with previous work done involving similar devices over similar size ranges. Device performance analyzed with respect to the fundamental performance metrics described in chapter 1 will be presented below, and these data compared to those from the literature, in order to confirm process viability.

3.1 Switching parameter analysis

As mentioned previously, device yields for both design 1 and design 2 were low, with design 2 devices exhibiting more frequent and repeatable switching as compared to design 1. Analysis of the fundamental switching parameters of design 2 devices as well as the effects of scaling on these parameters will be discussed in the following sections.

3.1.1 Forming, set, and reset voltages

As expected, forming voltage magnitudes were larger than those required for the set and reset operations, due to the necessity of forming an entire conductive filament as opposed to only re-oxidation and disruption of the CF tip (see Figure 3.1) .However, while values of the forming and set/reset voltages for the micron scale devices (Fig. 3.1.(a)) agree well with those found in [22] and [24], devices in the nanometer dimension range show somewhat higher values for these parameters. One reason for this variation could include the absence of a metallic “gettering” layer at the electrode/oxide interface such as was

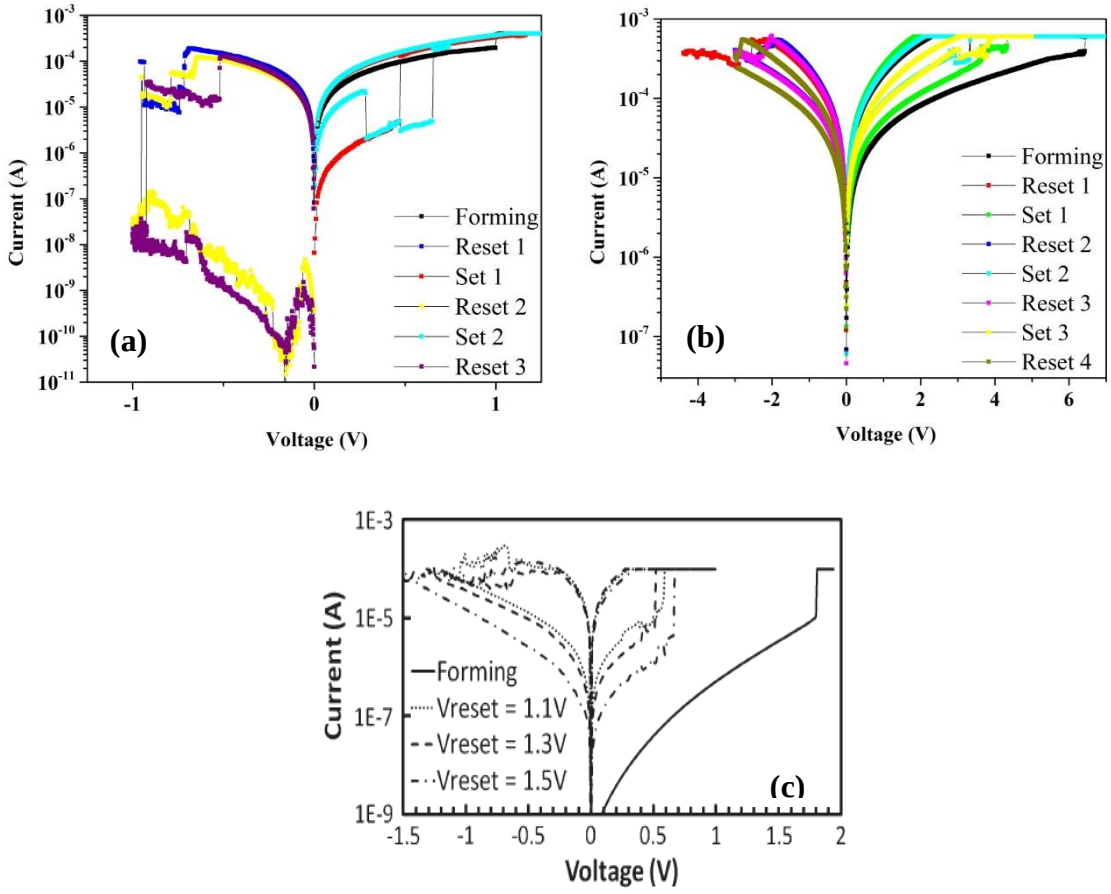


Figure 3.1 Current-voltage curves for HfO_2 RRAM (a) 1x1 μm^2 device area (b) 300 x 300 nm^2 device area (c) 7x7 μm^2 device area © 2013 IEEE

used in [24]. Layers such as these are generally added in order to promote the transformation of the oxide from a stoichiometric to a sub-stoichiometric state by acting as an oxygen reservoir, lowering the energy barrier for oxygen vacancy formation and thereby promoting the formation of the CF at lower voltages. Explanations involving film contaminants are also plausible. These include incomplete etching of SiO_2 or the presence of fluorocarbon contaminants introduced into the device region during the SiO_2 etching step. Thin SiO_2 or fluorocarbon films could then lead to larger energy

requirements for defect formation and subsequent diffusion and recombination in the contaminant + dielectric film. This would subsequently lead to larger forming and set/reset voltage magnitudes in devices capable of switching behavior. Absence of these contaminant films in the larger device areas would be explained by the improved etching performance that results from the natural increase in etchant species available for reaction in the larger area devices. Additionally, larger forming voltages would result from EBL beam dosages insufficiently large to achieve nominal cell area values, resulting in smaller device areas that require larger forming voltages as described previously. For the micron scale device areas, patterned features smaller than the nominal value would have a negligible result on the number of GB's present in the final device area as compared to nanometer scale device areas.

Average forming voltage magnitude also increased with decreasing electrode area (Figure 3.2) in a fashion similar to HfO_x RRAM from the literature (compare the data in Figure 3.2 with those found in Figure 1.15).

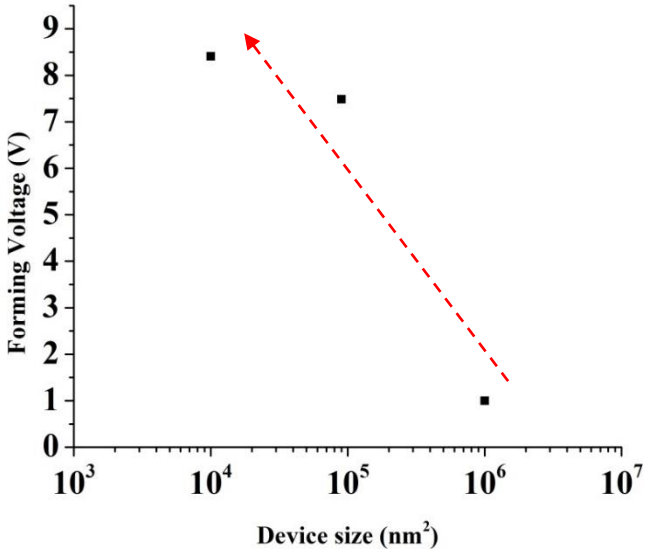


Figure 3.2 Average forming voltage vs device area.

3.1.2 LRS and HRS

Figure 3.1 confirms that current through the cells is approximately ohmic prior to the switch from a HRS or fresh state to the LRS for all device sizes, as evidenced by the linear behavior of the i-v curves in the pre-switching regions. Consistent with data from the literature, the average magnitudes of the LRS for the HfO_x RRAM devices of all sizes were approximately in the kΩ range. LRS magnitudes also showed little change with electrode area, confirming the essentially filamentary nature of conduction through a cell in the LRS (Figure 3.3). (Compare these LRS magnitude data with those for HfO_2 RRAM LRS in Figure 1.13). Also as expected, average LRS magnitudes for the devices showed an overall increase with decreasing value of the compliance current (Figure 3.4), consistent with the connection between larger compliance current and larger filament area,(Fig.1.11), and therefore lower resistance through the filament (Fig. 1.12).

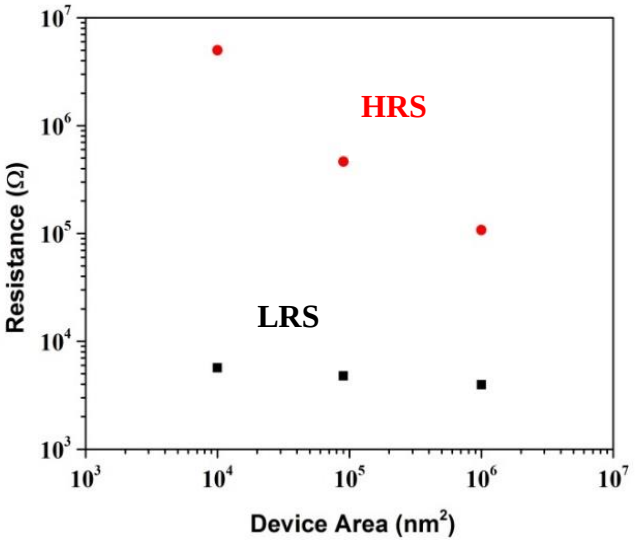


Figure 3.3 Change in average resistance state magnitudes with device area

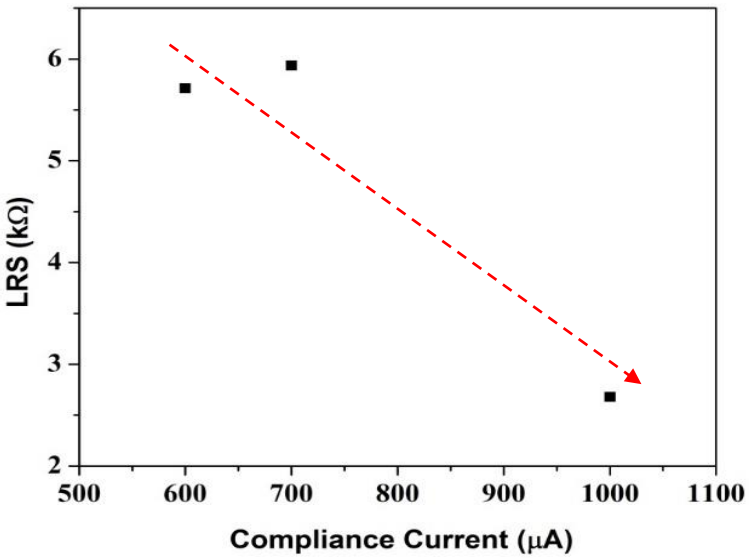


Figure 3.4 Change in average LRS magnitude with compliance current magnitude for a 300 nm device.

Values of the HRS were at least two orders of magnitude larger than the LRS magnitudes for all device sizes, consistent with the exponential increase in the resistance predicted by equation 1.18 after reset (Figure 3.3). Additionally, the magnitude of the HRS increased with reset voltage (Figure 3.5), confirming that larger reset voltage magnitudes generate longer re-oxidized filament tips which correspond to larger values of the resistance after reset [22]. Additionally, HRS data were also consistent with respect to trends in magnitude with respect to electrode area, i.e., decreasing electrode area showed a corresponding increase in average HRS magnitude (Figure 3.3).

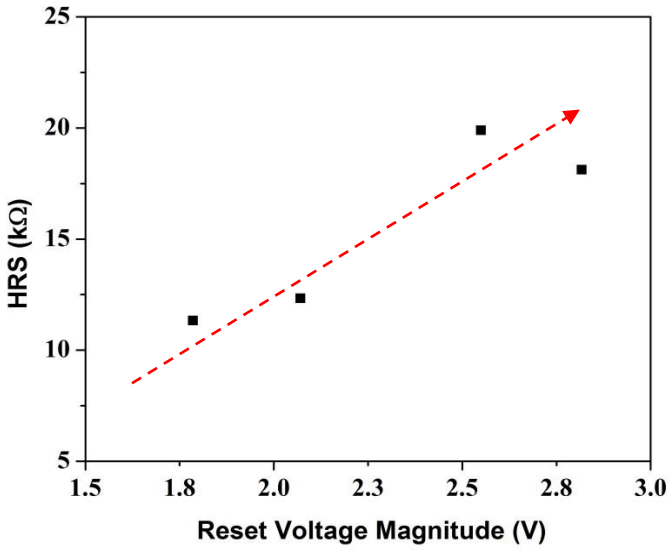


Figure 3.5 Change in average HRS magnitude with reset voltage magnitude during switching for a 300 nm device.

3.1.3 Reset current

Values for the reset current trended according to expectation, with larger compliances requiring larger reset currents in order to rupture the corresponding larger filaments generated during the forming step (Figure 3.6). (Compare these data to those in Fig. 1.16) .This relationship highlights the importance of minimizing compliance currents in order to minimize power consumption per switching cycle by minimizing reset current magnitudes.

3.2 Chapter Summary

In this chapter, the devices were electrically characterized with respect to the fundamental performance metrics of forming voltage, high and low resistance states, and reset currents, as well as the change in these metrics with device area and the connection

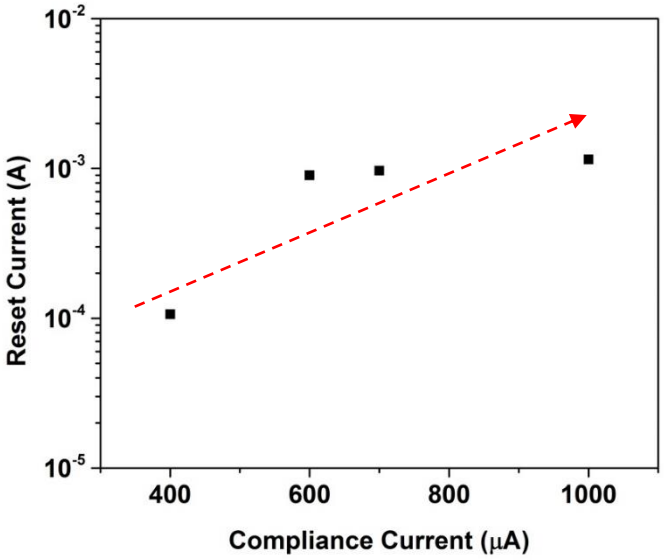


Figure 3.6 Average reset current vs. compliance current.

of these behaviors with properties of the conductive filament. The performance was found to be generally consistent with data for similar devices from the literature, thereby validating the design 2 process flow. In chapter 4, conclusions and suggestions for future work will be offered.

Chapter 4

CONCLUSIONS AND FUTURE WORK

4.1 Conclusions

Two designs for HfO_2 RRAM were realized and characterized. Design 1 was ineffective due to formation of resist residues possibly resulting from PMMA cross-linking occurring during EBL patterning. Cross-linking of the PMMA under-layer resulted from the necessity of the electron beam dosage being sufficiently high to pattern stable electrode structures in HSQ. PMMA+HSQ residues then prevented through-thickness electronic conduction in both the bottom and top electrodes, preventing switching in device cells. Design 2 addressed this issue by removing the need for HSQ by relying on positive as opposed to negative patterning of the electrodes. Design 2 devices exhibited switching which is reasonably consistent with previous work, despite showing poor yield and switching reliability.

4.2 Future Work

An optimized fabrication process based on design 2 could be used to perform further studies on nano-scale cross-point HfO_2 RRAM. Several improvements to the design and process should be implemented in order to improve device yield and performance. These improvements include:

- Inclusion of a Hf or Ti gettering layer at the insulator/electrode interface in order to reduce switching voltage magnitudes by lowering the energy barrier to oxygen vacancy formation in the oxide.

- Optimize the recipe parameters of the SiO_2 etching step in order to ensure complete removal of SiO_2, thus improving switching reliability and device yield.
- Optimize the EBL device area patterning process steps in order to ensure nominal device areas and therefore appropriate forming voltage magnitudes.
- Ensure protection against contamination during any annealing steps, thus preventing contamination of either SiO_2 or HfO_2 films. Avoidance of contamination of the SiO_2 could allow for thinning of the SiO_2 buffer layer by reducing unwanted current leakage due to contaminants. The thinner layer would then require shorter etch times as well as improve other process and performance optimization possibilities.

Different dielectric compositions, such as Ti-doped HfO_2 could be employed as well, in order to remove the necessity of a forming voltage. Different electrode and interface materials such as graphene or one of the transition metal dichalcogenides could be examined in order to determine any effects on the switching performance that may result. Also, physical methods such as TEM could be used to further examine the geometry and formation behaviors of the CFs in nanometer scale RRAM.

APPENDIX A

PROCESS FLOW FOR DESIGN 1 RRAM

The 5 level lithography process developed for fabrication of nanoscale HfO_2 RRAM is described in detail in the following pages. All tools mentioned can be found in the Institute for Electronics and Nanotechnology clean rooms at the Georgia Institute of Technology.

- Substrate cleaning: Test-grade p-type Si wafers are cleaned by standard AMI cleaning.

  -Acetone rinse

  - Methanol rinse

  -Isopropyl alcohol (IPA) rinse
- Spin coat EBL resist: PMMA(6%) on CEE

  -RPM: 1500

  -Ramp rate: 750 rpm/s

  -Hold time: 60 s
- Pre-exposure bake: 180° C , 90 s
- Patterning of wafer and die level EBL alignment marks: JEOL 9300 FS (See figure A.1 below for typical alignment mark locations. See Appendix B for sample job and schedule files used to create magazine files.)

  -Magazine file: ebmarks.mgn

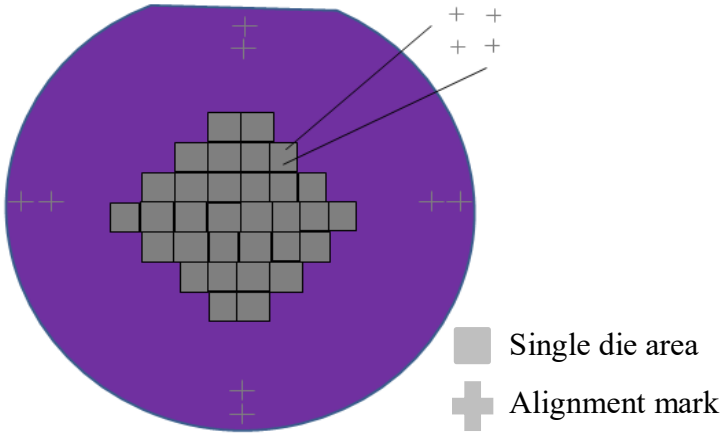


Figure A.1 EBL wafer-level and die-level alignment marks

- Develop exposed PMMA: soak exposed wafer in 1:1 MIBK/IPA solution

  -Soak time: 2 m

  -Rinse in IPA

- Etch Si: STS ICP DRIE

  -Recipe: dbb_si

  -Number of cycles: 39

- Strip PMMA: soak exposed wafer in heated 1165 resist remover

  -Soak time: 30 m

  - Soak temperature: 120° C

- Deposition of 300 nm of SiO_2: standard oxide recipe on Oxford PECVD

  -Deposition time: 4 m 43 s

  -Deposition temperature: 300° C

- Deposition of 100 nm of Al: Denton Explorer

  -Deposition rate: 1Å/s

- Deposition of 70 nm of TiN: Denton RF/DC Sputterer

  -Recipe: BHASTA1RF

  -Pre-sputter power: 400 W

  -Sputter power: 400 W

  -N_2/Ar : 47/3 sccm

  -Rotation: 50

  -Sputter time: variable

- Spin coat EBL resist: PMMA(2%) on CEE

  -RPM: 4500

  -Ramp rate: 1500 rpm/s

  -Hold time: 60 s

- Pre-exposure bake: 180° C , 90 s

- Spin coat EBL resist: HSQ(6%) on CEE

  -RPM: 3000

  -Ramp rate: 1500 rpm/s

  -Hold time: 60 s

- Patterning of bottom electrodes: JEOL 9300 FS (See figure A.2 below for sample bottom electrode array)

  -Magazine file: be_03.mgn

- Develop exposed HSQ: soak exposed wafer in TMAH (25%) (Tetra-methyl ammonium hydroxide)

  -Soak time: 30 s

  -Rinse in de-ionized (DI) water

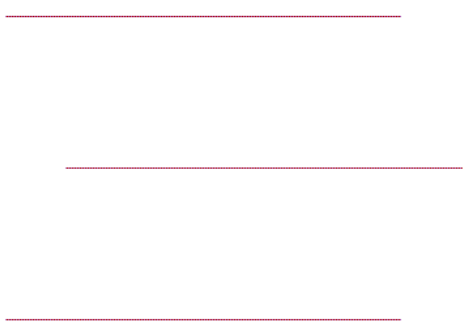


Figure A.2 Sample bottom electrode pattern
(single device array)

- Etch PMMA: Vision RIE

  -Power: 100 W

  - O_2 pressure: 15 mTorr

  -Time: 10-20 s (varies with PMMA thickness)

- Etch Al/TiN bi-layer: Unaxis RIE

  -Power: 300 W

  -BCl_3/Cl_2 : 30/5 sccm

  -Time: approx. 8 m (varies with metal thicknesses)

- Strip PMMA/HSQ: soak wafer in acetone or heated 1165 resist remover

  -Soak time: 2-30 m

  - Soak temperature (optional, if using 1165 ONLY): 120° C

- Descum: remove resist residue in O_2 plasma, Vision RIE

  -Recipe: standard descum recipe

  -Time: 20 s

- Deposition of HfO_2: Cambridge NanoTech Plasma ALD

  -Deposition temperature: 250° C

  -Hf precursor: tetrakis dimethylamido hafnium

  -O precursor: DI water

- Deposition of 70 nm of TiN: Denton RF/DC Sputterer

  -Recipe: BHASTA1RF

- Deposition of 100 nm of Al: Denton Explorer

  -Deposition rate: 1Å/s

- Spin coat EBL resist: PMMA(2%) on CEE

  -RPM: 4500

  -Ramp rate: 1500 rpm/s

  -Hold time: 60 s

- Pre-exposure bake: 180° C , 90 s

- Spin coat EBL resist: HSQ(6%) on CEE

  -RPM: 3000

  -Ramp rate: 1500 rpm/s

  -Hold time: 60 s

- Patterning of top electrodes: JEOL 9300 FS (See figure A.3 below for sample top electrode array)

  -Magazine file: te_03.mgn

- Develop exposed HSQ: soak exposed wafer in TMAH (25%) (Tetra-methyl ammonium hydroxide)

  -Soak time: 30 s

-Rinse in de-ionized (DI) water

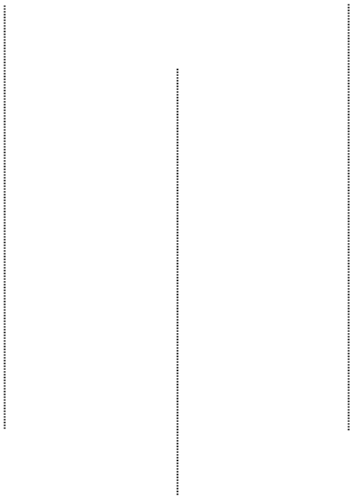


Figure A.3 Sample top electrode pattern
(single device array)

- Etch PMMA: Vision RIE

  -Power: 100 W

  - O_2 pressure: 15 mTorr

  -Time: 10-20 s (varies with PMMA thickness)

- Etch TiN/Al bi-layer: Unaxis RIE

  -Power: 300 W

  -BCl_3/Cl_2 : 30/5 sccm

  -Time: approx. 8 m (varies with metal thicknesses)

- Strip PMMA/HSQ: soak wafer in acetone or heated 1165 resist remover

  -Soak time: 2-30 m

  - Soak temperature (optional, if using 1165 ONLY): 120° C

- Descum: remove resist residue in O_2 plasma, Vision RIE

-Recipe: standard descum recipe

-Time: 20 s

- Spin coat OL resist: NR-9 on SCS G3

  -RPM: 2000

  -Ramp rate: 500 rpm/s

  -Hold time: 60 s

- Pre-exposure bake: 150° C , 60 s
- Patterning of bottom electrode openings: Karl Suss TSA Mask Aligner (See figure A.4 below for sample bottom electrode opening array)

  -Exposure wavelength: 365 nm

  -Exposure dose: 190 mJ/cm^2

Figure A.4 Sample bottom electrode opening pattern (single device array)

- Post-exposure bake: 100° C , 60 s
- Develop exposed NR-9: soak exposed wafer in RD-6

  -Soak time: 20 s

  -Rinse in de-ionized (DI) water
- Buffered oxide etch (BOE) of HfO_2: Soak in 6:1 BOE solution

  -Soak time: 2 m
- Strip NR-9: soak wafer in acetone

  -Soak time: 2 m
- Descum: remove resist residue in O_2 plasma, Vision RIE

  -Recipe: standard descum recipe

  -Time: 20 s
- Spin coat OL resist: NR-9 on SCS G3

  -RPM: 2000

  -Ramp rate: 500 rpm/s

  -Hold time: 60 s
- Pre-exposure bake: 150° C , 60 s
- Patterning of contacts and array labels/boundaries: Karl Suss TSA Mask Aligner

  -Exposure wavelength: 365 nm

  -Exposure dose: 190 mJ/cm^2
- Post-exposure bake: 100° C , 60 s
- Develop exposed NR-9: soak exposed wafer in RD-6

  -Soak time: 20 s

  -Rinse in de-ionized (DI) water

- Deposition of 450 nm of Al: Denton Explorer

  -Deposition rate: 1Å/s

- Strip NR-9/Al : soak wafer in acetone (see fig. A.5 below for completed sample array)

  -Soak time: approx.2 m

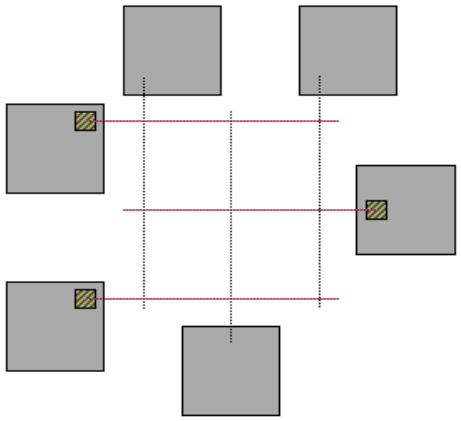


Figure A.5 Single completed device array
(array labels and boundaries not shown)

APPENDIX B

PROCESS FLOW FOR DESIGN 2 RRAM

The 5 level lithography process developed for fabrication of nano-scale cross-point HfO_2 RRAM is described in detail in the following pages. All tools mentioned can be found in the Institute for Electronics and Nanotechnology clean rooms at the Georgia Institute of Technology.

- Substrate cleaning: Test-grade p-type Si wafers are cleaned by standard AMI cleaning.

  -Acetone rinse

  - Methanol rinse

  -Isopropyl alcohol (IPA) rinse
- Spin coat EBL resist: PMMA(6%) on CEE

  -RPM: 1500

  -Ramp rate: 750 rpm/s

  -Hold time: 60 s
- Pre-exposure bake: 180° C , 90 s
- Patterning of wafer and die level EBL and OL alignment marks: JEOL 9300 FS (See figure B.1 below for typical alignment mark locations for a single device array.)

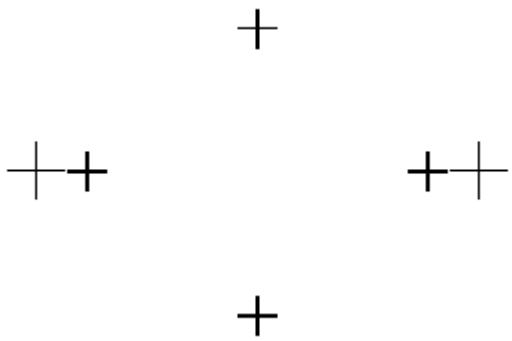


Figure B.1 EBL and OL alignment marks (single device array, entire pattern not shown)

- Job file for patterning of EBL and OL alignment marks on JEOL 9300 FS:

```
JOB/W 'NEBL1',4                    %JEOL job label and cassette specifications

GLMPOS P=(0,40000), Q=(0,-40000)   %This code block specifies the size
GLMP 3.0, 1200.0                   % and orientation of large (global)
GLMQRS 3.0, 1200.0                 % marks used by the JEOL 9300FS
                                   % for wafer level alignment

PATH DEVIN2                        % This command specifies a calibration
                                   % routine for the JEOL 9300FS

ARRAY ( 25000, 2, 200) / ( 20000, 10, 200)   %This code block defines the
    CHMPOS M1=(0,0)                          % locations and shot dosages
    CHMARK 3.0, 30.0                         % for the characterization
    ASSIGN P(10)->((1,1),SHOT11)             % structures
    ASSIGN P(10)->((1,2),SHOT12)
    ASSIGN P(10)->((1,3),SHOT13)
    ASSIGN P(10)->((1,4),SHOT14)
    ASSIGN P(10)->((1,5),SHOT15)
    ASSIGN P(10)->((1,6),SHOT16)
    ASSIGN P(10)->((1,7),SHOT17)
    ASSIGN P(10)->((1,8),SHOT18)
    ASSIGN P(10)->((1,9),SHOT19)
    ASSIGN P(10)->((1,10),SHOT20)
    ASSIGN P(10)->((2,1),SHOT21)
    ASSIGN P(10)->((2,2),SHOT22)
    ASSIGN P(10)->((2,3),SHOT23)
```

```
      ASSIGN P(10)->((2,4),SHOT24)
      ASSIGN P(10)->((2,5),SHOT25)
      ASSIGN P(10)->((2,6),SHOT26)
      ASSIGN P(10)->((2,7),SHOT27)
      ASSIGN P(10)->((2,8),SHOT28)
      ASSIGN P(10)->((2,9),SHOT29)
      ASSIGN P(10)->((2,10),SHOT30)
AEND

; Global alignment marks for JEOL          %This code block defines the
                                           % locations and shot dosages used
ARRAY (-42750,2,2500)/(0,1,0)              % for global JEOL alignment
      CHMPOS M1=(10000,0)                  % mark patterning
      CHMARK 3.0,15.0
      ASSIGN P(2) -> ((*,*),SHOT2)
AEND

ARRAY (40250,2,2500)/(0,1,0)
      CHMPOS M1=(-10000,0)
      CHMARK 3.0,15.0
      ASSIGN P(2) -> ((*,*),SHOT2)
AEND

ARRAY (0,1,0)/(42750,2,2500)
      CHMPOS M1=(0,-10000)
      CHMARK 3.0,15.0
      ASSIGN P(2) -> ((*,*),SHOT2)
AEND

ARRAY (0,1,0)/(-40250,2,2500)
      CHMPOS M1=(0,10000)
      CHMARK 3.0,15.0
      ASSIGN P(2) -> ((*,*),SHOT2)
AEND

; Large alignment marks for optical levels

ARRAY (-16250,2,32500)/(0,1,0)             %This code block defines the
      CHMPOS M1=(-10000,0)                 % locations and shot dosages
      CHMARK 3.0,15.0                      % for large optical
      ASSIGN P(2) -> ((*,*),SHOT2)         % lithography alignment
AEND                                       % mark patterning



ARRAY (0,1,0)/(11179,2,22358)
```

```
        CHMPOS M1=(0,-10000)
        CHMARK 3.0,15.0
        ASSIGN P(2) -> ((*,*),SHOT2)
AEND

;Chip level alignment marks                    %This code block defines the
                                               %locations and shot dosages
ARRAY (-13910,5,6045)/(9460,5,3965)            %for chip level JEOL
        CHMPOS M1=(0,0)                        % alignment mark patterning
        CHMARK 3.0,15.0
        ASSIGN P(3) -> ((*,*),SHOT1)
AEND

;Pattern

ARRAY (0,1,0)/(0,1,0)                          %This code block defines the
        CHMPOS M1=(0,0)                        %locations and shot dosages
        CHMARK 3.0,15.0                        % for small optical
        ASSIGN P(4) ->((*,*),SHOT1)            % lithography alignment
AEND                                           % mark patterning

PEND

;Layer Definition

LAYER 1

P(10) 'nellis7medsq.v30'                       %This code block defines the
SPPRM 4.0,,,,1.0,1                             %patterns (.v30 files) used above

P(2) 'EBL_Global_Mark.v30'
SPPRM 4.0,,,,1.0,1

P(3) 'nellis7cmark.v30'
SPPRM 4.0,,,,1.0,1

P(4)'new_ebl1.v30'
SPPRM 4.0,,,,1.0,1


STDCUR 2; 2 nA current

; Shot modulation alignment for marks           %This code block defines the
                                               %dosages used for the
SHOT1:MODULAT((1,5))                           % patterns above
SHOT2:MODULAT((0,0))
```

; Shot modulation for 75 um characterization squares

SHOT11: MODULAT ((0,-80))
SHOT12: MODULAT ((0,-75))
SHOT13: MODULAT ((0,-70))
SHOT14: MODULAT ((0,-65))
SHOT15: MODULAT ((0,-60))
SHOT16: MODULAT ((0,-55))
SHOT17: MODULAT ((0,-50))
SHOT18: MODULAT ((0,-45))
SHOT19: MODULAT ((0,-40))
SHOT20: MODULAT ((0,-35))
SHOT21: MODULAT ((0,-30))
SHOT22: MODULAT ((0,-25))
SHOT23: MODULAT ((0,-20))
SHOT24: MODULAT ((0,-15))
SHOT25: MODULAT ((0,-10))
SHOT26: MODULAT ((0, -5))
SHOT27: MODULAT ((0, 0))
SHOT28: MODULAT ((0, 5))
SHOT29: MODULAT ((0, 20))
SHOT30: MODULAT ((0, 25))

END

- Schedule file for patterning of EBL and OL alignment marks on JEOL 9300 FS:

MAGAZIN 'NEBL1' % Initializes the schedule file for the job labeled 'NEBL1'

#1 ← %Specifies the beginning of a cassette block
%and the substrate to be used for pattern writing.
%4A ← % Specifies window "A" on the 4" wafer cassette
JDF 'new_rram_ebl1',1 ← %Job deck file name and layer specification
ACC 100 ← %Accelerating voltage=100 kV
CALPRM '100kv_2na' ← %Specifies calibration parameter file
DEFMODE 2 ← %Specifies deflection stage used for pattern writing
RESIST 650 ← %Defines the base dose for exposure of resist
SHOT A,6 ← %Shot time and pitch specifications
GLMDET C ← %JEOL global mark detection routine
CHMDET S ← %JEOL chip mark detection routine
CHIPAL V1 ← %JEOL chip mark arrangement
HSWITCH OFF,ON ← %Beam height detection routines
END 1 ← % End of code block

- Develop exposed PMMA: soak exposed wafer in 1:1 MIBK/IPA solution

  -Soak time: 2 m

  -Rinse in IPA

- Etch Si: STS ICP DRIE

  -Recipe: dbb_si

  -Number of cycles: 39

- Strip PMMA: soak exposed wafer in heated 1165 resist remover

  -Soak time: 30 m

  - Soak temperature: 120° C

- Deposition of 300 nm of SiO_2: standard oxide recipe on Oxford PECVD

  -Deposition time: 4 m 43 s

  -Deposition temperature: 300° C

- Deposition of 100 nm of Ti: PVD 75

  -Power: 300 W

  - Ramp-up rate: 600 W/m

  -N_2/Ar : 1/19 sccm

  -Rotation: yes

  -Hold time: 7 m

  - Ramp-down rate: 999 W/m

- Deposition of 100 nm of TiN: PVD 75

  -Power: 300 W

  - Ramp-up rate: 600 W/m

  -N_2/Ar : 1/19 sccm

-Rotation: yes

-Hold time: 11 m

- Ramp-down rate: 999 W/m

- Spin coat OL resist: NR-9 on SCS G3

  -RPM: 2000

  -Ramp rate: 500 rpm/s

  -Hold time: 60 s

- Pre-exposure bake: 150° C , 60 s

- Patterning of bottom electrodes: Karl Suss TSA Mask Aligner (See figure B.2 below for sample bottom electrode array)

  -Exposure wavelength: 365 nm

  -Exposure dose: 190 mJ/cm^2

Figure B.2 Sample bottom electrode pattern (single device array)

- Post-exposure bake: 100° C , 60 s

- Develop exposed NR-9: soak exposed wafer in RD-6

  -Soak time: 20 s

  -Rinse in de-ionized (DI) water

- Etch Ti/TiN bi-layer: Unaxis RIE

  -Power: 300 W

  -BCl_3/Cl_2 : 30/5 sccm

  -Time: approx. 8 m (varies with metal thicknesses)

- Strip NR-9: soak wafer in acetone

  -Soak time: 2 m

- Descum: remove resist residue in O_2 plasma, Vision RIE

  -Recipe: standard descum recipe

  -Time: 20 s

- Deposition of 300 nm of SiO_2: standard oxide recipe on Oxford PECVD

  -Deposition time: 4 m 43 s

  -Deposition temperature: 300° C

- Spin coat EBL resist: PMMA(6%) on CEE

  -RPM: 1500

  -Ramp rate: 750 rpm/s

  -Hold time: 60 s

- Pre-exposure bake: 180° C , 90 s

- Patterning of device cell openings: JEOL 9300 FS (See figure B.3 below for locations of openings for a single device array.)

  -Magazine file: new_rram_ebl2.mgn

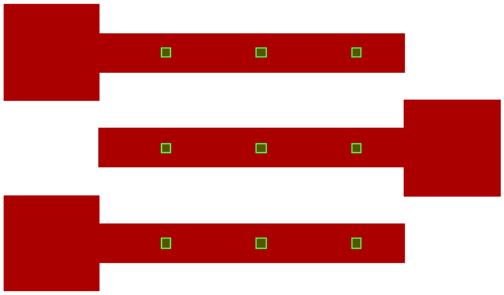


Figure B.3 Sample device cell opening pattern (single device array, bottom electrodes shown for reference purposes)

- Develop exposed PMMA: soak exposed wafer in 1:1 MIBK/IPA solution

  -Soak time: 2 m

  -Rinse in IPA

- Etch SiO_2: Plasma Therm ICP DRIE

  -Recipe: C4F8_OX

  -Time: 2 m 30 s

- O_2 clean step (fluorocarbon film removal): Plasma Therm ICP DRIE

  -Coil power: 800 W

  -Platen power: 40 W

  -O_2: 50 sccm

  -Pressure: 15 mTorr

  -Time: 5 s

- Strip PMMA: soak exposed wafer in heated 1165 resist remover

  -Soak time: 30 m

- Soak temperature: 120° C

- Deposition of HfO_2: Cambridge NanoTech Plasma ALD

  -Deposition temperature: 250° C

  -Hf precursor: tetrakis dimethylamido hafnium

  -O precursor: DI water

- Deposition of 100 nm of TiN: PVD 75

  -Power: 300 W

  - Ramp-up rate: 600 W/m

  -N_2/Ar : 1/19 sccm

  -Rotation: yes

  -Hold time: 11 m

  - Ramp-down rate: 999 W/m

- Deposition of 400 nm of Al: Denton Explorer

  -Deposition rate: 1Å/s

- Anneal: SSI RTP

  -Time: 30 m

  -Temperature: 600° C

- Spin coat OL resist: NR-9 on SCS G3

  -RPM: 2000

  -Ramp rate: 500 rpm/s

  -Hold time: 60 s

- Pre-exposure bake: 150° C , 60 s
- Patterning of top electrodes and labels: Karl Suss TSA Mask Aligner (See figure B.4 below for sample top electrode array)

  -Exposure wavelength: 365 nm

  -Exposure dose: 190 mJ/cm^2

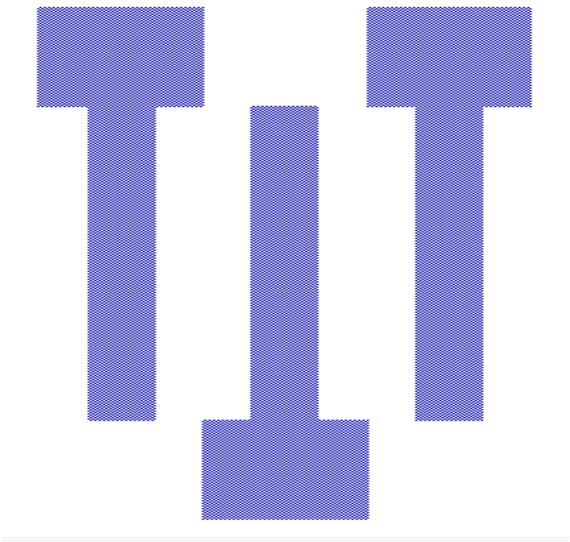


Figure B.4 Sample top electrode pattern (single device array)

- Post-exposure bake: 100° C , 60 s
- Develop exposed NR-9: soak exposed wafer in RD-6

  -Soak time: 20 s

  -Rinse in de-ionized (DI) water
- Etch TiN/Al bi-layer: Unaxis RIE

  -Power: 300 W

  -BCl_3/Cl_2 : 30/5 sccm

  -Time: approx. 8 m (varies with metal thicknesses)

- Strip NR-9: soak wafer in acetone

  -Soak time: 2 m

- Descum: remove resist residue in O_2 plasma, Vision RIE

  -Recipe: standard descum recipe

  -Time: 20 s

- Spin coat OL resist: NR-9 on SCS G3

  -RPM: 2000

  -Ramp rate: 500 rpm/s

  -Hold time: 60 s

- Pre-exposure bake: 150° C , 60 s

- Patterning of bottom electrode openings: Karl Suss TSA Mask Aligner (See figure B.5 below for sample bottom electrode opening array)

  -Exposure wavelength: 365 nm

  -Exposure dose: 190 mJ/cm^2

Figure B.5 Sample bottom electrode opening pattern (single device array)

- Post-exposure bake: 100° C , 60 s

- Develop exposed NR-9: soak exposed wafer in RD-6

  -Soak time: 20 s

  -Rinse in de-ionized (DI) water

- Buffered oxide etch (BOE) of HfO_2: Soak in 6:1 BOE solution

  -Soak time: 2 m 30 s

- Strip NR-9: soak wafer in acetone

  -Soak time: 2 m

- Descum: remove resist residue in O_2 plasma, Vision RIE

  -Recipe: standard descum recipe

  -Time: 20 s

Figure B.6 below shows a sample of a completed device array.

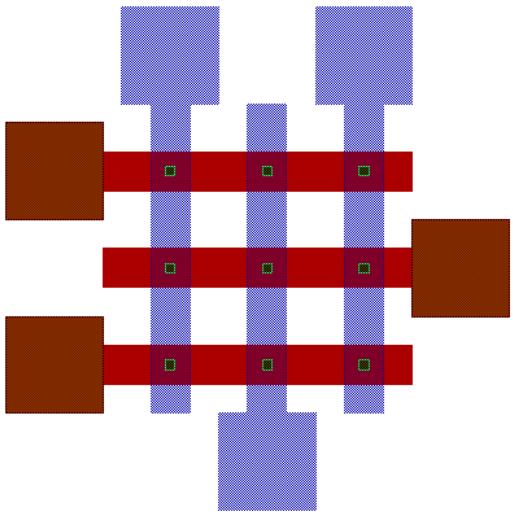


Figure B.6 Single completed device array
(array labels and boundaries not shown)

REFERENCES

[1] "Process Integration, Devices and Structures," International Technology Roadmap for Semiconductors, 2013.

[2] B. Keeth, R.J. Baker, B. Johnson, F. Lin, "An Introduction to DRAM," in *DRAM Circuit Design: Fundamental and High-Speed Topics*, 1st ed. Hoboken, New Jersey, USA: John Wiley & Sons, 2008, ch. 1, sec.1 ,pp.1-5.

[3] IBM Corp., Armonk, New York, USA, "3-D Hybrid Stacked SRAM Cell To Be Built By European Scientists" Available: http://www.zurich.ibm.com/news/14/compose3.html. Accessed :February 23, 2016.

[4] R. Bez., E. Camerlenghi, A. Modelli,A. Visconti, " Introduction to Flash Memory" ,in *Proceedings of the IEEE*, 2003, p.489.

[5] P. Pavan, R. Bez., P. Olivo, E. Zanoni, "Flash Memory Cells – An Overview" ,in *Proceedings of the IEEE*, 1997, p.1248-49.

[6] *Keithley Application Note Series, no. 3177*, Keithley Instruments Inc., Cleveland, OH.,2012,p.1.

[7] L. O. Chua, "Memristor - the missing circuit element," *IEEE Trans. Circuit Theory*,vol.18, 1971, pp.507–519.

[8] D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, "The Missing Memristor Found," *Nature*,vol.453, 2008, pp.80-83.

[9] L. O. Chua, S.M. Kang, "Memristive devices and systems," *Proceedings of the IEEE*, 1976, pp.209–223.

[10] R.S. Williams, "How We Found the Missing Memristor,"*IEEE Spectrum*, 2008, pp.29-35.

[11] R. Waser, R. Dittman, G. Staikov, K. Szot, "Redox-Based Resistive Switching Memories-Nanoionic Mechanisms, Prospects, and Challenges," *Advanced Materials*, vol.21, 2009, pp. 2632–2663.

[12] J.J. Yang, D.B. Strukov, D.R. Stewart, "Memristive Devices for Computing", *Nature Nanotechnology*,vol.8,2012, pp.13-24.

[13] M.N. Kozicki and M. Mitkova, "Memory Devices Based on Mass Transport in Solid Electrolytes," in Nanotechnology (Volume 3: Information Technology 1), Ed: R. Waser, Wiley–VCH Verlag GmbH & Co.KGaA, Chapter 16, 2008, pp.485–575.

[14] L.Liu, B. Chen, B. Gao, F. Zhang, Y. Chen, X. Liu, Y. Wang, R. Han, J. Kang, "Engineering Oxide Resistive Switching Materials for Memristive Device Application," *Appl. Phys. A, Materials,* vol.102, 2011,pp. 991–996.

[15] J. J. O'Dwyer, "The Theory of Electrical Conduction and Breakdown in Solid Dielectrics," Clarendon, Oxford , 1973.

[16] H. S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, "Metal-Oxide RRAM," *Proceedings of the IEEE,* vol. 100, 2012,pp. 1951-1970.

[17] J.J. Yang, F. Miao, M.D. Pickett, D.A.A. Ohlberg, D.R. Stewart, C.N. Lau, R.S. Williams, "Mechanism of Electroforming of Metal Oxide Resistive Switches", *Nanotechnology*,vol.20,2009,215201.

[18] G. Bersuker, D.C. Gilmer, D. Veksler, P. Kirsch, L. Vandelli, A. Padovani, L. Larcher, K. McKenna ,A. Shluger, V. Iglesias, M. Porti, M. Nafria, "Metal Oxide Resistive Switching Mechanism Based On Conductive Filament Properties," *J.Appl.Phys.*,vol.110,2011,124518.

[19] M. Lanza, "A Review on Resistive Switching in High-k Dielectrics :A Nanoscale Point of View Using Conductive Atomic Force Microscope,"*Materials*,vol.7, 2014,pp.2155-2182.

[20] Y.S. Chen, T. Y. Wu, P.J. Zheng, P.S. Chen, H.Y. Lee, C.H. Lin, F. Chen, M.J. Tsai, " Forming-free HfO_2 Bipolar RRAM Device with Improved Endurance and High Speed Operation," *VLSI Technology, Systems, and Applications*, 2009.

[21] B. Chakrabarti, " Investigation of Metal Oxide Dielectrics for Non- Volatile Floating Gate and Resistance Switching Memory Applications," Ph.D., Dept. of Materials Science and Eng., University of Texas , Dallas, Tx., 2013.

[22]F.M. Puglisi, L. Larcher, G. Bersuker, A. Padovani, P. Pavan, "An Empirical Model for RRAM Resistance in Low- and High-Resistance States," *IEEE Electron Device Letters*,vol.34 ,2013,no. 3,pp. 387-389.

[23] H. Y. Lee, P.S. Chen, T.Y. Wu, Y.S. Chen, C.C. Wang, P.J. Zheng, C.H. Lin, F. Chen, C.H. Lien, M.J. Tsai, "Low Power and High Speed Bipolar Switching With a Thin Reactive Ti Buffer Layer in Robust HfO_2 - Based RRAM," *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2008,pp. 297–300.

[24] B. Govoreanu, G.S. Kar, Y.Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I.P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, O. Richard, T. Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D.J. Wouters, J.A. Kittl, M. Jurczak, "10 x10 nm^2 Hf/HfOx Crossbar Resistive RAM With Excellent Performance, Reliability and Low-Energy Operation," *Tech. Dig. Int. Electron Device Meeting*, Washington, DC, 2011,pp. 729–732.

[25] B. Butcher, G. Bersuker, L. Vandelli, A. Padovani, L. Larcher, A. Kalantarian, R. Geer, and D. C. Gilmer, "Modeling the effects of different forming conditions on RRAM conductive filament stability," in *Proceeding of IMW*,2013,pp. 52-55.

[26] Fang Yuan, Zhigang Zhang, Liyang Pan, and Jun Xu, "A Combined Modulation of Set Current With Reset Voltage to Achieve 2-bit/cell Performance for Filament-Based RRAM,"*JEDS*, vol.2 ,no. 6,2014,pp.154 – 157.

[27] K.D. Cantley, " Artificial Neural Systems Using Memristive Synapses and Nano-crystalline Silicon Thin-film Transistors," Ph.D., Dept. of Materials Science and Eng., University of Texas , Dallas, Tx, 2011.

[28] H. Namatsu, Y. Takahashi, K. Yamazaki, T. Yamaguchi, M. Nagase, and K. Kurihara, "Three-dimensional Siloxane Resist for the Formation of Nano-patterns With Minimum Linewidth Fluctuations," *JVST B*, 1997,pp.69-76.

[29] A.E. Grigorescu, C.W. Hagen, "Resists for Sub-20-nm Electron Beam Lithography With a Focus on HSQ: State of the Art," *Nanotechnology Topical review*, vol. 20, 2009.

[30] C. L. Frye, W.T. Collins, "The Oligomeric Silsesquioxanes, $[HSiO_{3/2}]_n$,"*Journal of the American Chemical Society*,vol.92 no.19, 1970,pp.5586-5588.

[31] I. Zailer, J. E. F. Frost, V. Chabasseur-Molyneux, C. J. B. Ford and M. Pepper, "Crosslinked PMMA as a High-Resolution Negative Resist for Electron Beam Lithography and Applications for Physics of Low-Dimensional Structures,"*Semicond. Sci. Technol.*,vol. 11, 1996,pp. 1235-1238.

[32] H. Duan , D. Winston, J. K.W. Yang, B.M. Cord, V.R. Manfrinato, and K. K. Berggren, "Sub-10-nm Half-Pitch Electron-Beam Lithography by Using Poly(methyl methacrylate) as a Negative Resist," *J. Vac. Sci. Technol. B* ,vol.28, 2010,pp.58-62.