FORCED CONVECTION IN MICROCHANNELS WITH NANOSTRUCTURES ON ONE WALL

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FORCED CONVECTION IN MICROCHANNELS WITH NANOSTRUCTURES ON ONE WALL

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To my husband

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

New electronic devices are faster than ever before, incorporate a higher level of integration, and as a result, need to dissipate higher heat fluxes. Active cooling is the only possible method of thermal management for these devices. A new type of microchannel heat sink has been developed and evaluated in this study. The device consists of silicon microchannels on whose bottom surfaces multi-walled carbon nanotubes are grown. The objective of the study is to investigate the effect of carbon nanotubes on the heat transfer characteristics. The heat sink size is 15 mm $\times$ 15 mm $\times$ 0.675 mm. It contains two microchannel designs. One consists of eight channels of cross section 682 μm $\times$ 50 μm; the other has six channels of cross section 942 μm $\times$ 50 μm. The heat sink is incorporated in an open loop flow facility, with water as the coolant. Six different configurations are compared. Two have no nanotubes, two have closely spaced nanotubes, while the last two designs have widely spaced nanotubes. The tests utilize an infrared camera as well as thermocouples placed in the flow for characterization. The heat transfer characteristics are compared for the different cases.

CHAPTER 1

INTRODUCTION

Engineers and scientists in the past century have developed world-altering inventions. The atom bomb in 1941 brought the world abruptly into the nuclear age, changing war and peace forever. Sputnik and the subsequent men on the moon in the 1950's and 1960's changed the dreams of children everywhere. While Tang and dehydrated foods can be found in almost every household in the United States and the Cold War gave us bomb shelters on every college campus, these adventures in engineering did not change the world as much as the transistor. Everyone alive at the time remembers where they were when man landed on the moon but few can recall the news covering Brattain, Bardeen, and Shockley when they invented the transistor at Bell Laboratories in 1949. Even after Noyce developed planar transistor technology in 1959 and Kilby incorporated two transistors and a resistor into the first integrated circuit few people realized the impact this work would have on the world. Today patients can have medical records faxed to a hospital in seconds even if they are thousands of miles from home, and doctors can collaborate on surgeries over the Internet. Children can call their parents on a cell phone when the coach cancels soccer practice, instead of waiting in the rain. People can record favorite television shows every week without having to remember to put in the tape. Daily lives have changed drastically in the past twenty years not because of nuclear material or dehydrated ice cream but because thousands of transistors and resistors can be packaged into a microchip.

During the first forty-five years of the integrated circuit the world became accustomed to faster, better, and cheaper electronic devices. Microelectronics designers are shifting from individually packaged chips to the system-on-board and the system-on-package architectures. Early computers required an entire room, more computing power now fits in a briefcase. Soon the motherboard in the desktop computer may fit entirely in a single package the size of today's larger integrated circuits. If these trends continue the next forty-five years of the integrated circuit should be very interesting indeed.

Today, the major obstacles facing microelectronics designers in their quest for faster, better, cheaper systems are the problems encountered when these components are packaged. Packaging involves connecting, powering, and protecting the system and its related components from both external hazards and internally generated heat. Connecting and powering the components can be complex but protecting the system from both internal and external hazards can be the most important and difficult packaging challenge. The 2003 International Technology Roadmap for Semiconductors estimates that high performance chips would likely produce 80 W/cm^2 by 2006. If this chip were packaged with no heat lost to the external environment, after one minute it would reach temperatures in excess of 2000 °C from its power alone. Obviously current integrated circuit materials will not survive at these temperatures. In order to make these systems viable, engineers and scientists need to find extremely high temperature materials, or they will need to incorporate thermal management in packaging designs.

1.1 Background

Most electronic systems currently on the market require thermal management beyond the capabilities of passive systems such as heat spreaders or natural convection. Many high performance systems rely on forced convection air-cooling through

the use of fans and heat sinks. Researchers agree that these methods will not be sufficient for the new generation of electronic systems [24]. Thermal management research during the past ten to fifteen years includes work on liquid cooling using microchannels, immersion, jet impingement, and spray cooling. Liquid cooling techniques show impressive results in laboratory prototypes. Several challenges remain however in low cost, reliable, and practical implementation of these. Some of these include uneven cooling, high power requirements, and space constraints [16] [18].

Direct immersion cooling using dielectric coolants has been explored by a number of investigators [17] [20]. Both single phase and phase change cooling have been investigated. Accessibility to equipment and cost and weight of coolant have so far restricted the widespread use of this cooling method.

Research in microchannels shows promise as well [21] [23] [25]. Microchannels offer enhanced surface area for chip-level cooling. There are still obstacles to widespread microchannel use [8]. Many designs have high pressure drop through the channels, often above 400 kPa. Coolant leakage is also a major problem for many microchannel designs. There are also problems with the thermal interface between the channels and the heat source. Many researchers have investigated different microchannel geometries and many show promising results [22] [27]. Some researchers have decreased the pressure drop through channels by layering the channels. Fluid handling and thermal interface resistance are the two major obstacles for most microelectronics cooling techniques utilizing liquids. These problems will most likely be solved by proper packaging design. Although this project focuses on surface enhancement of microchannels, packaging issues were carefully considered during the design of the device.

1.2 Nanotubes

The objective of this work is to use Multi-Walled Carbon Nanotubes (MWNTs or nanotubes) to enhance the surface of the microchannels. Recent measurements of Single-Walled Carbon Nanotubes (SWNTs) have reported thermal conductivities in excess of 1000 W/mK [11] [26]. Populating the walls of microchannels with nanotubes provides nanofins that may enhance thermal transport.

Sumio Iijima at the NEC Laboratory in Tsukuba, Japan discovered nanotubes in 1991 [13]. Sumio Iijima and Donald Bethune at IBM Almaden in California independently discovered SWNTs in 1993 [7] [14]. Researchers around the world started studying the physical and electrical properties of nanotubes. Richard Smalley and his team at Rice University were well prepared to study SWNTs because of their successful work on the related Buckminsterfullerene or Bucky Ball. They were able to make nanotube ropes or aligned bundles [6] and study the physical properties. Early studies of nanotube properties were limited by the purity of the nanotubes and the available equipment. Researchers were initially interested in the quantum effects of SWNTs, but recent experiments show that SWNTs are also extremely flexible [10].

SWNTs and nanotubes have both been used for a variety of applications. Researchers found that adding SWNTs to plastics in automotive fuel systems can reduce static charge build-up [9]. Researchers at IBM have succeeded in using SWNTs to emit photons [19]. Most researchers agree that because of the amazing properties of nanotubes they will change the world of nano-research more than any other nano-structure. Nanotubes make a logical heat transfer surface enhancement structure for silicon devices. There are several companies that produce nanotubes [1] [2] [3], but only one commercial company could grow nanotubes on a substrate at the time of this work [4].

CHAPTER 2

DEVICE DESIGN

2.1 Constraints

In order to design a silicon microchannel device that would utilize nanotubes and be fabricated at Georgia Tech there were several external factors to consider. The first set of constraints was imposed by the limits of the nanotube manufacturer. Nanolab can only deposit carbon nanotubes on a clean silicon substrate, any silicon oxide inhibits nanotube growth. Also, because of time constraints Nanolab could only change one variable between the first nanotube design and the second nanotube design. Nanolab can grow nanotubes with the same diameter and length but with different spacing. The available nanotube height under these considerations is 15 μm $\pm$ 5 μm. The available diameter is 100 nm $\pm$ 5 nm as quoted by Nanolab. This meant that the channels had to be shallow enough to force the water to flow through the nanotubes and not directly over them. The second set of constraints came from the test set-up. In order to seal the device in a flow-loop the tops of the channels need to be flat. This meant that Nanolab would have to make a Kapton mask to mark off the parts of the device that would not have nanotubes. The channel geometry had to be conducive to the mask process. The third set of constraints came from the manufacturing capabilities at Georgia Tech combined with the availability of the machines. These constraints led to the final device design described below.

2.2 Channel Geometry

Assuming steady state, laminar flow through smooth channels, Equations 2.1, 2.2, and 2.3 give the pressure drop through rectangular channels.

$$\triangle P = \frac{\rho f L V^2}{2 D_h} \tag{2.1}$$

$$f = \frac{64}{\mathrm{Re}_D} \tag{2.2}$$

$$D_h = \frac{4 A_c}{P} \tag{2.3}$$

where $\triangle P$ is the pressure drop through the channels in kPa, L is the length of the channel in mm, f is the friction factor given in Equation 2.2, D_h is the hydraulic diameter given in Equation 2.3 in mm^2, ρ is the density of water in $\mathrm{kg/m}^3$, and V is the flow rate, equal to 167 m/s for this evaluation. Also, Re_D is the Reynold's number, A_c is the cross-sectional area of the channel in mm^2, and P is the wetted perimeter of the channel in mm. With a constant channel height of 50 μm figure 2.1 compares the pressure drop through several different channel widths.

Using the assumptions stated above, Equation 2.4 estimates the convective heat flux coefficient for the same rectangular channels compared above.

$$h = \frac{Nuk}{D_h} \tag{2.4}$$

where k, the thermal conductivity of silicon equals 148 W/mk, D_h is the hydraulic diameter, evaluated using Equation 2.3, and Nu is the Nussult number interpolated from table 8.1 in reference [15]. Figure 2.2 compares the convective heat transfer coefficient for different channel widths.

Figure 2.3 shows the completed channel design. The right side of the device has 8 channels, each channel is 682 μm wide and the left side has 6 channels, each channel is 942 μm wide. The channel region is 9500 μm long. The device is 675 μm thick.

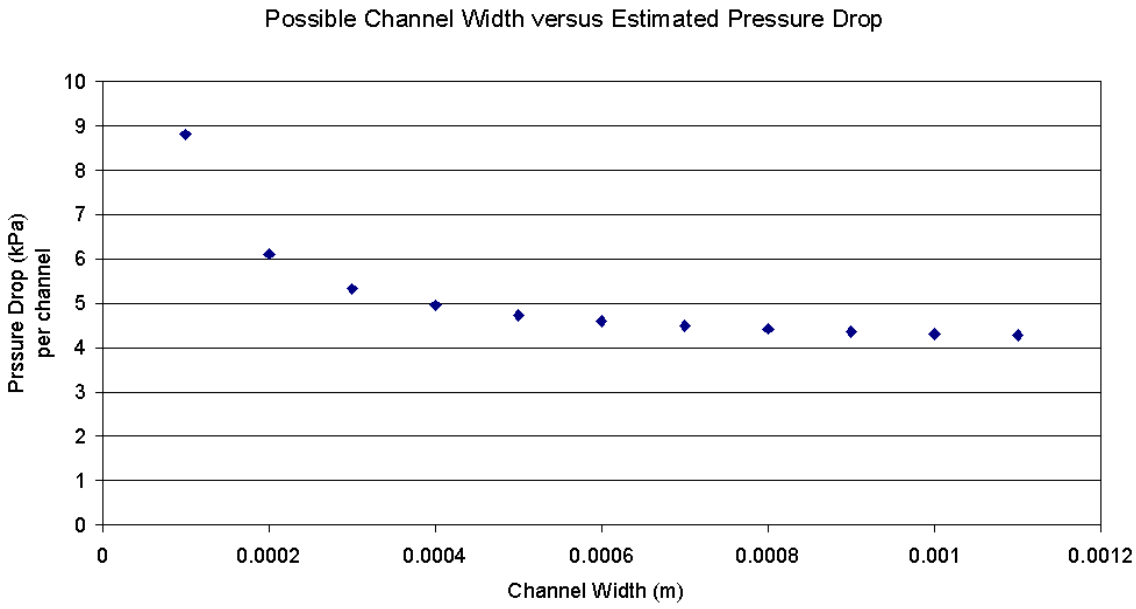

Figure 2.1: Comparison of possible channel widths to estimated pressure drop.

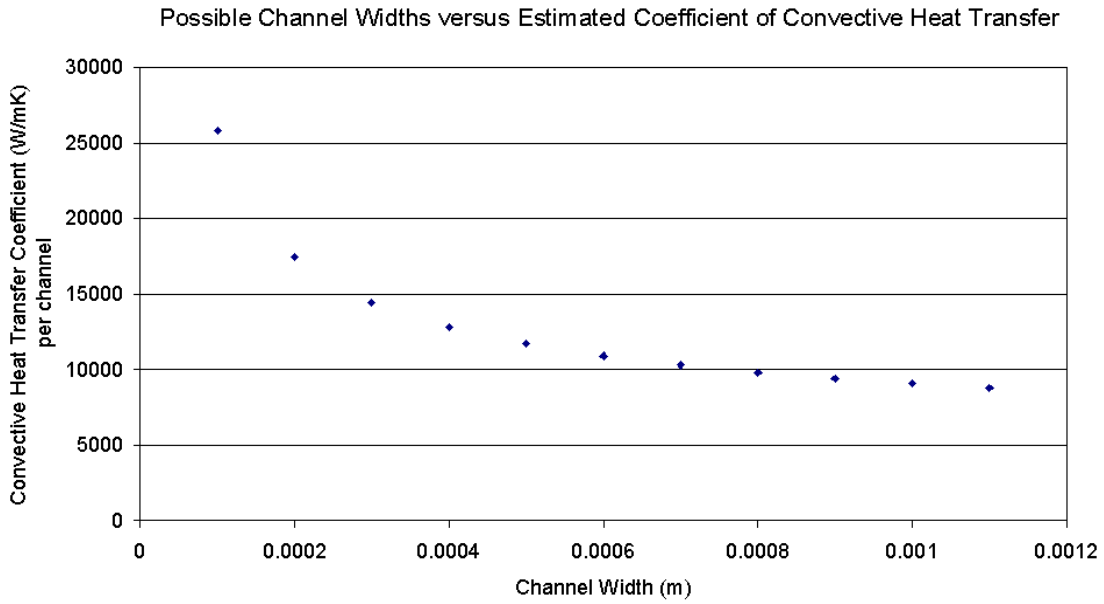

Figure 2.2: Comparison of possible channel widths to the estimated heat transfer coefficient

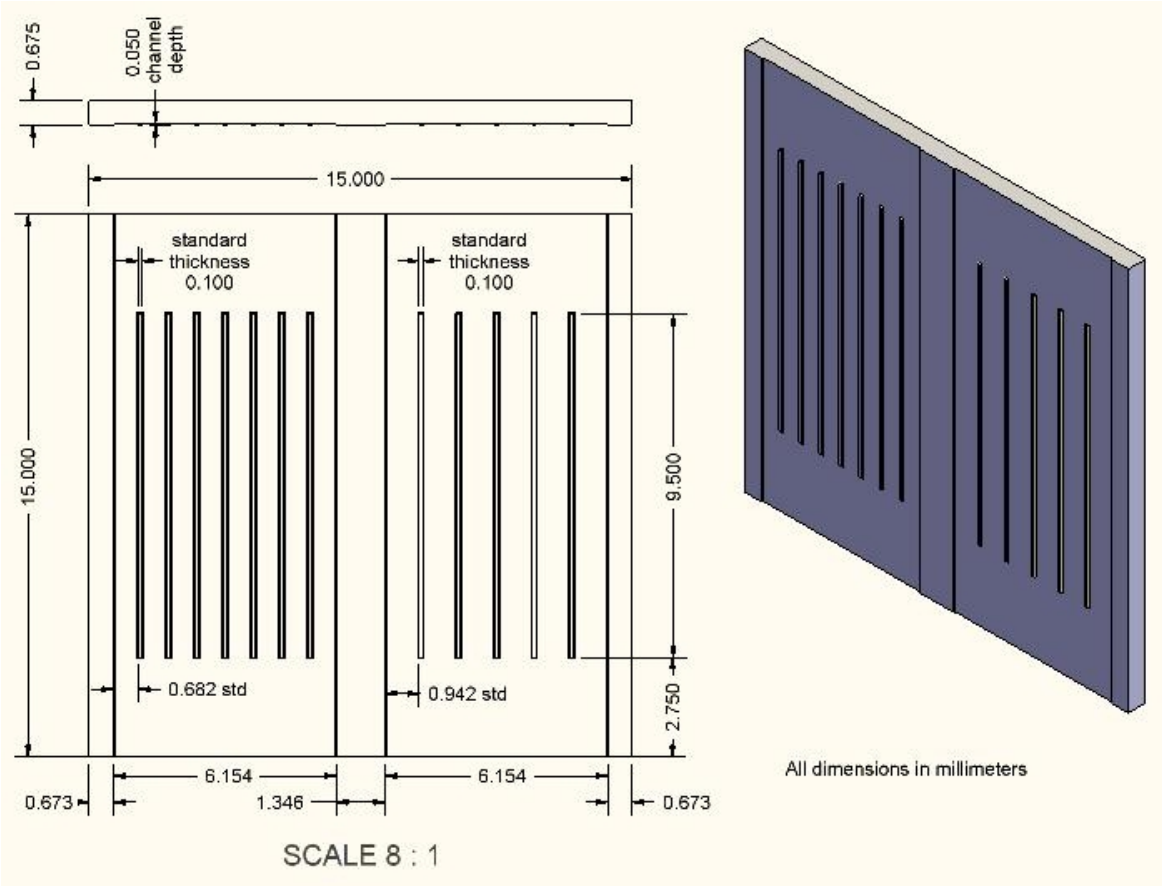

Figure 2.3: CAD drawing of the device fabricated at the Georgia Tech cleanroom

2.3 Addition of Nanotubes

After device Fabrication Nanolab deposited dense nanotubes on three devices. The nanotubes have a diameter of 100 nm $\pm$ 5 nm and a height of 15 μm $\pm$ 5 μm, as quoted by Nanolab. The nanotubes are 30% of the height of the channels. Nanolab also deposited sparse nanotubes on two devices. The sparse nanotubes have the same dimensions as the dense nanotubes. See chapter 7 for complete device characterization.

CHAPTER 3

DEVICE FABRICATION

3.1 Mask Fabrication and Photolithography

Device fabrication occurred at the Microelectronics Research Center (MiRC). After completion of the device design, the next step in the fabrication process is the mask. Using the mask layout shown in Figure 3.1 the MiRC mask making shop fabricated the completed mask using a quartz template. Figure 3.2 shows the completed mask. The long, thick black lines separate the devices and the short, thin lines are the tops of the channels.

The mask is made for use with positive photoresist. Positive photoresist becomes soluble when it is exposed to light. The mask is therefore dark where the photoresist should remain after development. The first step in the fabrication process involves using the STS Plasma Enhanced Chemical Vapor Depositor (PECVD) to deposit a 1 μm thick layer of silicon dioxide on the wafer. The PECVD uses radio frequency (RF) induced plasma to react different gases and deposit silicon dioxide. This process takes 30 minutes per wafer. Figure 3.3 shows the STS PECVD at the MiRC clean room.

After the silicon dioxide deposition step is complete each wafer is dried for 5 minutes in an oven set to 120 °C before spinning photoresist on the wafers. The drying step is important because any moisture on the wafer could cause the photoresist to develop incorrectly. The CEE Model 100 CB Spinner shown in Figure 3.4 spins the wafer at 3000 revolutions per minute in order to evenly deposit a thin layer of Shipley 1813 photoresist on each wafer.

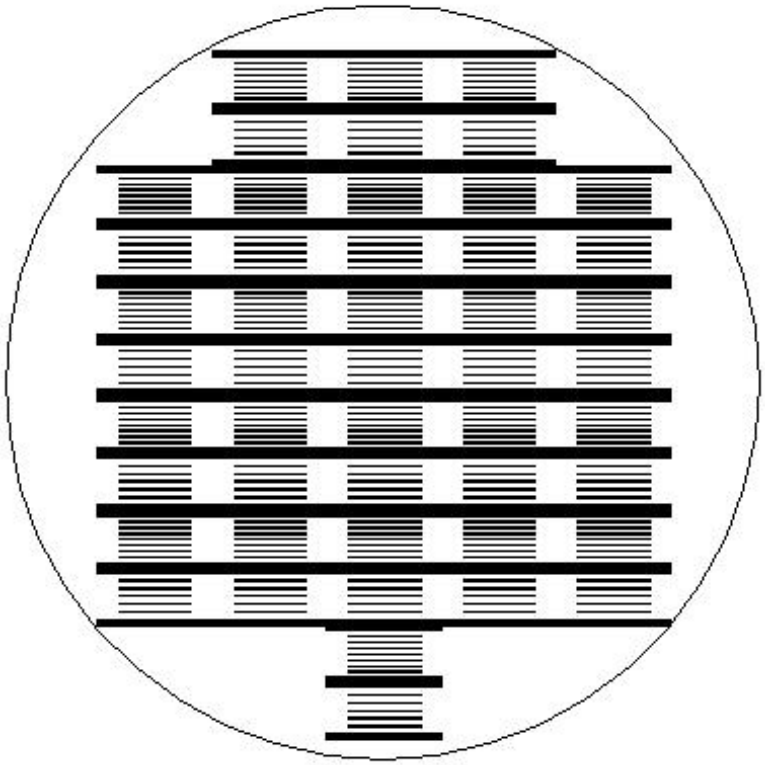

Figure 3.1: CAD drawing of the mask used to fabricate the devices

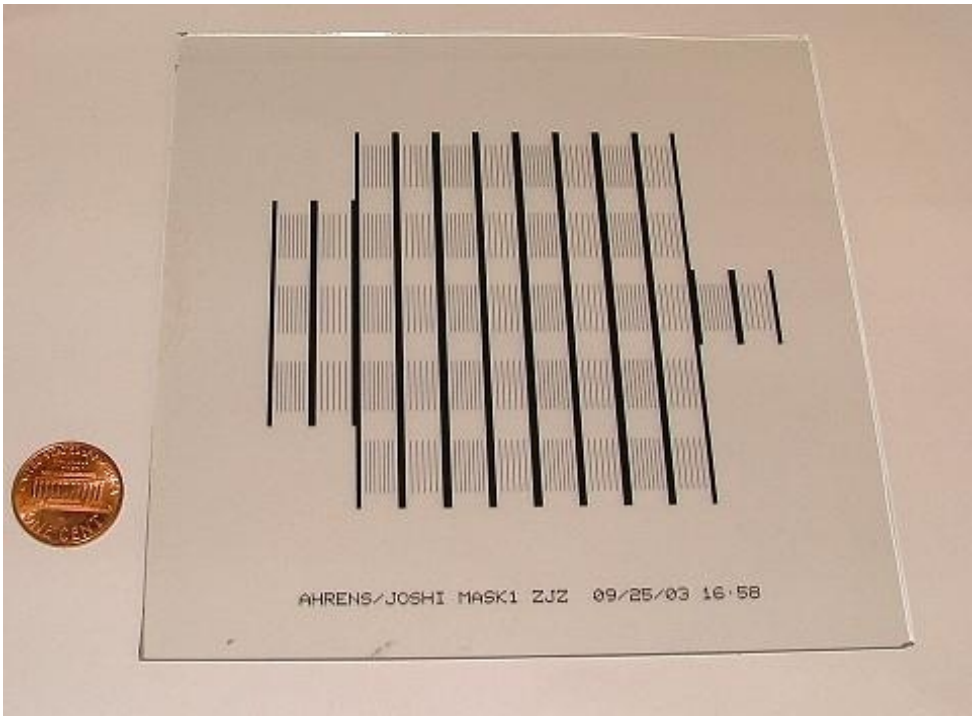

Figure 3.2: Photograph of the completed quartz mask, designed for use with positive photoresist.

Figure 3.3: Silicon dioxide depositor used to deposit a 1 μm thick layer of silicon dioxide on each wafer

Figure 3.4: Photoresist spinner and hot plate used to spin a thin layer of photoresist on each wafer and dry the wafer after deposition

After the photoresist is applied each wafer is again heated to dry the photoresist. Once the photoresist is completely dry it can be patterned. The Karl Suss MA-6 Mask Aligner in Figure 3.5 aligns the wafer and the quartz mask. Then using a bright ultra-violet light the wafer is exposed. Each wafer is then chemically developed to remove the exposed photoresist. To assure proper exposure the wafer and mask must be clean.

3.2 Etching and Quality Control

After exposing the wafers and developing the photoresist they are again heated in the oven for ten minutes. This ensures they are dry before the etch process. Any moisture or unexposed photoresist on the back of the wafer can cause serious damage to the etcher. The Plasma-Therm Inductively Coupled Plasma (ICP) etcher shown in Figure 3.6 has two chambers. The left chamber is designed for silicon dioxide and polymer etching. The right chamber uses a proprietary process for deep silicon

Figure 3.5: Mask alignment tool used to expose the photoresist with the mask pattern

trench etching. Both chambers use RF induced plasma and various gases to etch the surface of the wafer.

During the first etching step the left chamber removes the silicon dioxide layer wherever it is not covered by developed photoresist. During the second etching step the right chamber removes the silicon wherever it is no longer covered by silicon dioxide. The right chamber also removes most of the remaining photoresist. This process requires approximately four hours per wafer and results in uniform channels with rectangular cross sections. Figure 3.7 shows a scanning electron microscope (SEM) image of the channels.

After completing the etching process the Tencor Alphastep 500 profilometer shown in Figure 3.8 is used to check the depth and surface roughness of the channels. The profilometer uses a small needle to trace the surface of the wafer. The needle moves up and down with surface roughness. Five wafers were fabricated, but after the channel depth check only 3 wafers were determined satisfactory.

Figure 3.6: Inductively Coupled Plasma etcher used in a 2-step process to etch rectangular channels into the silicon

Figure 3.9 shows a 15.2 cm diameter completed wafer. Each of the satisfactory wafers has an average channel depth between 40 μm and 50 μm. The surface roughness varies from wafer to wafer because the etching machine was altered slightly between wafers. The profilometer shows that the surface roughness varies from $\pm$ 0.2 μm to $\pm$ 0.4 μm for the channels. The black ring around the edge of the wafer results from the clamping process used in the ICP during the etching process.

3.3 Device Separation

After the wafers were determined satisfactory they were separated into devices using the scribe and break method. This involves using a diamond tipped scribe to carefully initiate a crack in the silicon wafer. Then by causing the crack to perpetuate through the silicon, the devices are separated. This process takes practice and patience, but gives the devices a nice edge and a fairly consistent size. This process is preferable to a wafer dicing saw because the saw can contaminate the device with

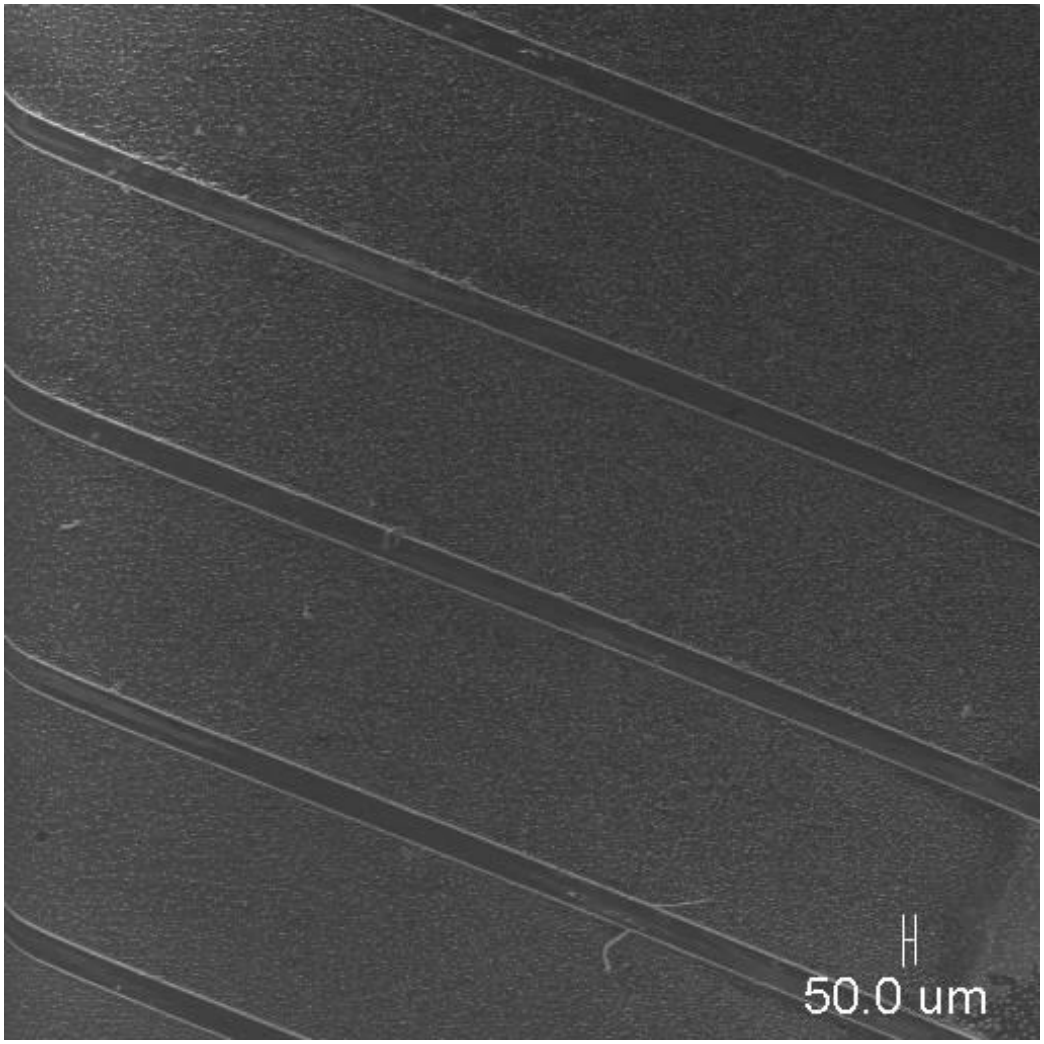

Figure 3.7: A scanning electron microscope image of the channels after fabrication

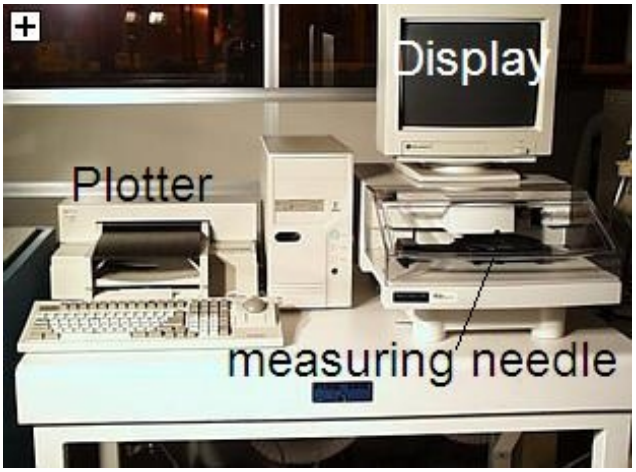

Figure 3.8: The profilometer used to determine the surface roughness of the channels

Figure 3.9: A photograph of the completed 15.2 cm diameter wafer with clamping marks

a fine dust. This dust could cause problems during nanotube deposition. Figure 3.10 shows a section of wafer after the scribe and break process.

Figure 3.11 shows two completed devices. The device on the right does not have nanotubes and the device on the left has dense nanotubes. The nanotubes appear as black sections of the device. Without the use of a microscope the devices with the sparse nanotube spacing look the same as the devices without nanotubes. The devices are now complete and ready for testing.

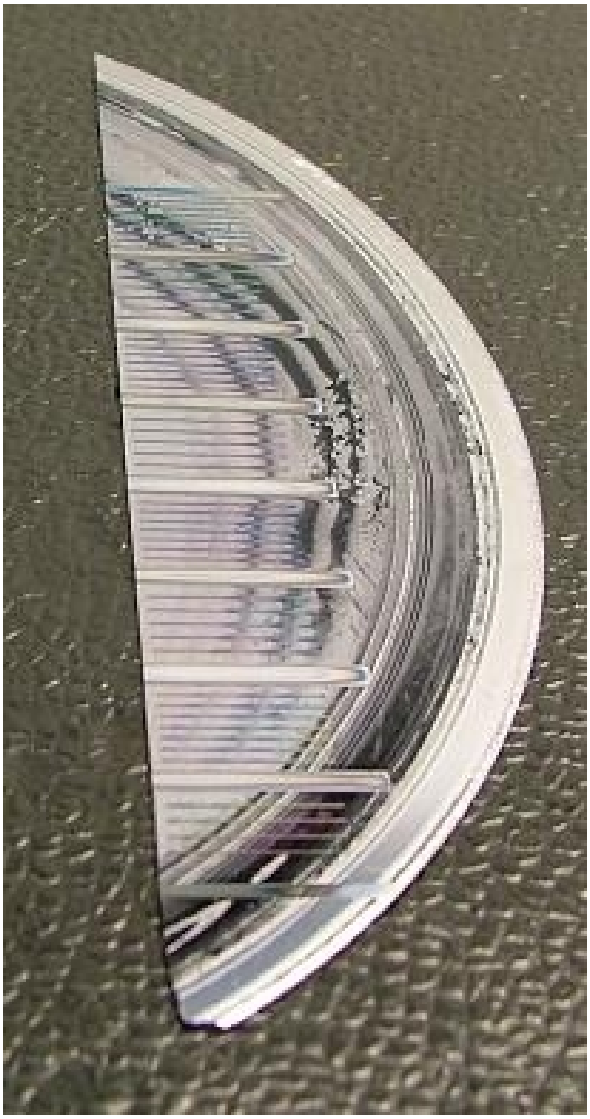

Figure 3.10: A photograph of a section of the 15.2 cm diameter wafer after the scribe and break process

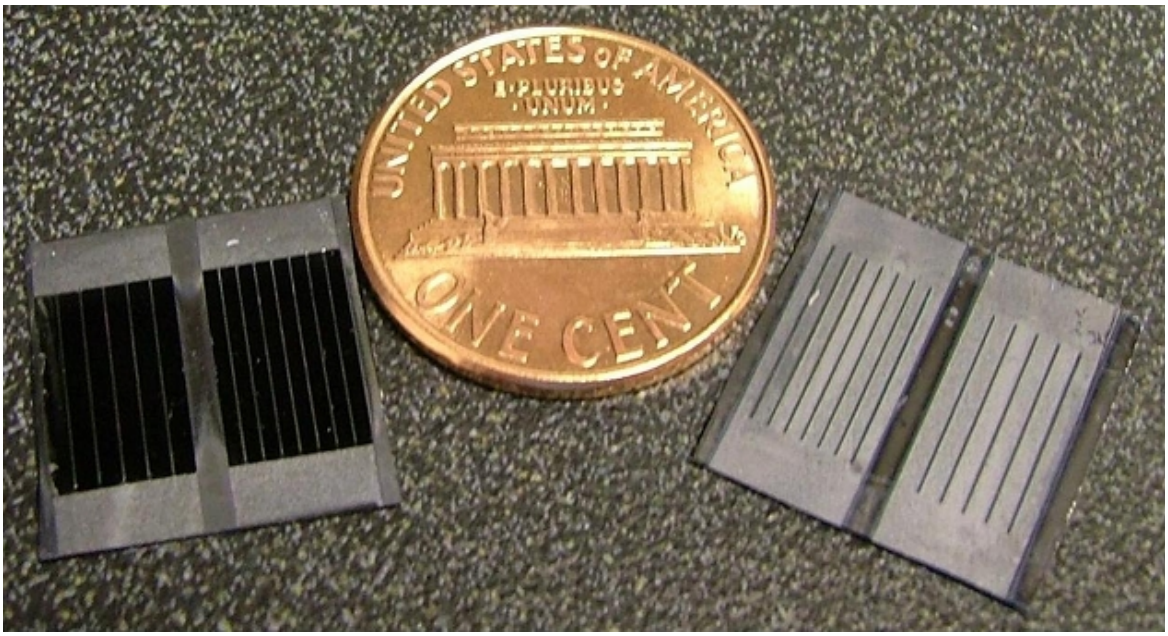

Figure 3.11: Two of the silicon devices. The device on the left has dense nanotubes and the device on the right has no nanotubes. The sides of the devices near the penny have narrow channels, and the sides of the devices away from the penny have wide channels.

CHAPTER 4

DATA COLLECTION

4.1 Software

A specialized program written with LabVIEW 7 Express, a product of National Instruments, collects temperature data during device testing. The program records the test data in a text file, easily convertible to Microsoft Excel. The user can input a heading for the data file as well as the time step used to determine the data collection rate. The user interface provides real-time digital readings as well as a graph of the data during the test. Upon completion of the test the user is prompted to save the data. Figure 4.1 shows the user interface for this program. Appendix A contains the block diagram of the program. The block diagram is the source code represented in graphical form.

4.2 Hardware

The LabVIEW program runs on a computer attached to an Agilent data acquisition/switch unit via a general purpose interface bus (GPIB) cable. The device tests utilize six thermocouples. Five of the thermocouples are 0.51 mm diameter copper/constantan (type T) and one is a 0.079 mm diameter Chromel/Alumel (type K) thermocouple. The Agilent data acquisition/switch unit comes with a NIST traceable calibration certificate. The Agilent unit has an inherent uncertainty of $\pm$ 1 °C for temperature readings. This error results from internal switching error, transducer error, and the thermocouple reference junction error. Copper/constantan (type T) thermocouples and Chromel/Alumel (type K) thermocouples have an uncertainty of $\pm$ 0.5 C. Therefore the total uncertainty for the thermocouple readings is $\pm$1.5 °C.

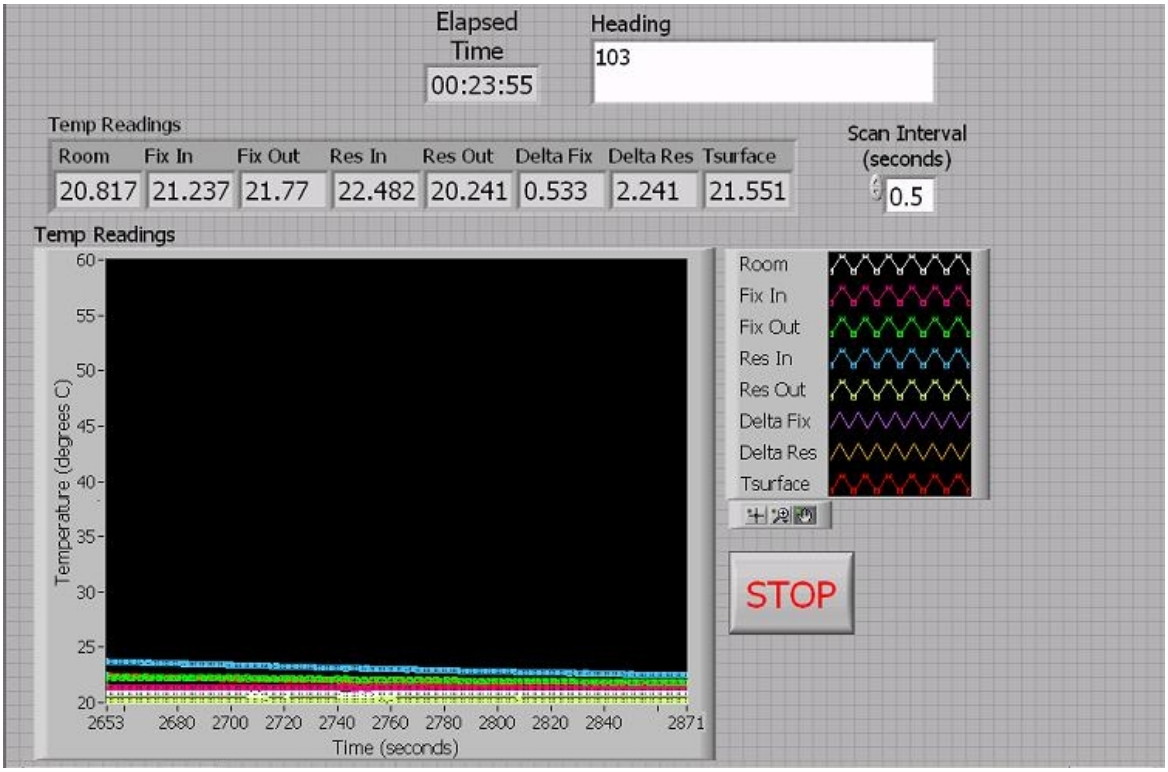

Figure 4.1: User interface of data acquisition program

Figure 4.2: Agilent data acquisition/switch unit provides the physical connection between the thermocouples and the data acquisition software

Figure 4.2 shows the Agilent data acquisition/switch unit.

Figure 4.3 shows the graduated cylinder used for flow tests performed to obtain a voltage versus current relationship for the pump. This test is described in detail in chapter 6. The cylinder has an uncertainty of ± 1 mL.

The power supply from Agilent used to power the heater and the pump during the device tests has an uncertainty of ± 0.25 W. This uncertainty can be calculated from the information given by the supplier using Equation 4.1,

$$w_P = \left[(I \cdot w_E)^2 + (E \cdot w_I)^2 \right]^{\frac{1}{2}} \tag{4.1}$$

where w_P is the uncertainty in the power reading in W, w_E is the error in the voltage reading given by the supplier, w_I is the error in the current reading given by the supplier, I is the current reading of the machine during usage, considered 0.5 A for this test, and E is the voltage reading of the machine during usage, considered 16 V for this test. These values were chosen for I and E because they are larger than the values used during device testing. The uncertainty of the voltage reading is ± 0.5 % of 27 V, and the uncertainty of the current reading is ± 0.5 % of 3 A as given by Agilent. This is the same power supply used for the flow rate tests described in chapter 6. Figure 4.4 shows the front panel of the power supply.

An infrared camera from Quantum Focus Inc. provides imaging during device

Figure 4.3: Graduated cylinder used in flow tests has an uncertainty of ± 1 mL

Figure 4.4: Power supply used to power the heater and the pump during testing has an uncertainty of ± 0.25 W

tests as well as data for the thermal interface test described in chapter 6. During usual operating procedures the camera performs a two temperature calibration to determine the emissivity correlation for the material being imaged. The camera uses a thermoelectric stage to heat the object being imaged to a known temperature. It then records the emissivity of the object at two drastically different temperatures. Tests are commonly performed using 50 °C and 150 °C. The uncertainty of the camera during this type of operation is ± 0.25 °C. The camera can also be used with a one temperature calibration. During this type of operation the uncertainty of the camera is ± 2 °C. Figure 19 shows the infrared camera. The manufacturer quotes the uncertainties assumed here.

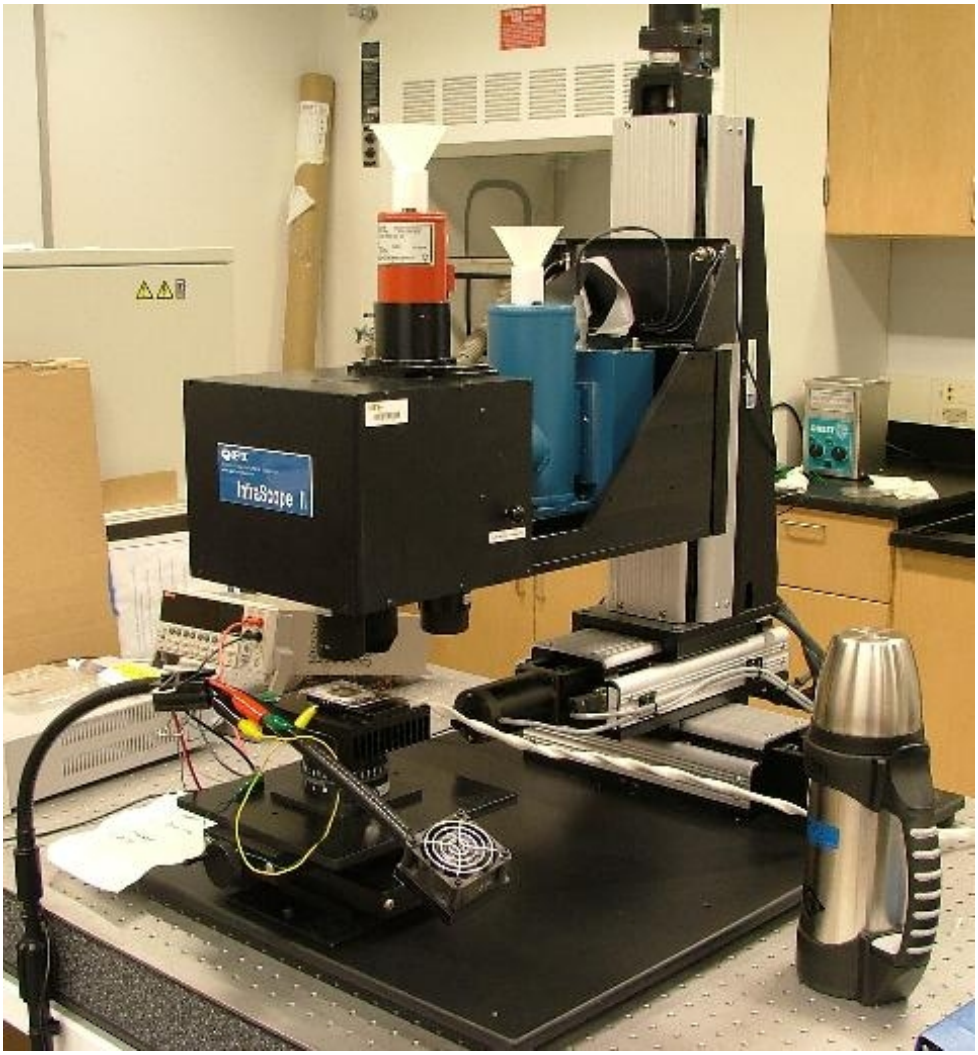

Figure 4.5: Infrared camera from Quantum Focus Inc.

CHAPTER 5

PROTOTYPE TEST FIXTURE

As a proof-of-concept and to determine possible leakage paths, a prototype test fixture was built to test a prototype device. The prototype test fixture consists of two polycarbonate sections. The bottom section is designed to contain the prototype device and provide a fluid path. The top section is designed to seal the fluid in the prototype device and provide a visual and infrared window to the fluid as it flows through the device.

5.1 Window Test

The prototype test fixture contains a window for viewing the fluid flowing through the device. In order for the infrared camera to image through the window, the material of the window must be transparent in the near infrared. The visible spectrum is from 0.7 μm to 0.4 μm and the near infrared spectrum is from 100 μm to 0.7 μm [5]. Figure 5.1 shows the transparency of quartz. Quartz lets through much of the visible spectrum but does not transmit much in the infrared spectrum. Figure 5.2 shows the transparency of silicon. Silicon is commonly used for infrared imaging because it transmits much of the infrared spectrum. Figure 5.3 shows the transparency of sapphire. Sapphire is often used for infrared imaging. It is also often used for visual imaging.

Tests performed on samples of these materials using the infrared camera support the use of a sapphire window in the test fixture. The samples tested include a sapphire circle 9.5 mm in diameter, another sapphire circle 13 mm in diameter, a quartz square 15 mm on a side, and a silicon square 15 mm on a side. The sapphire

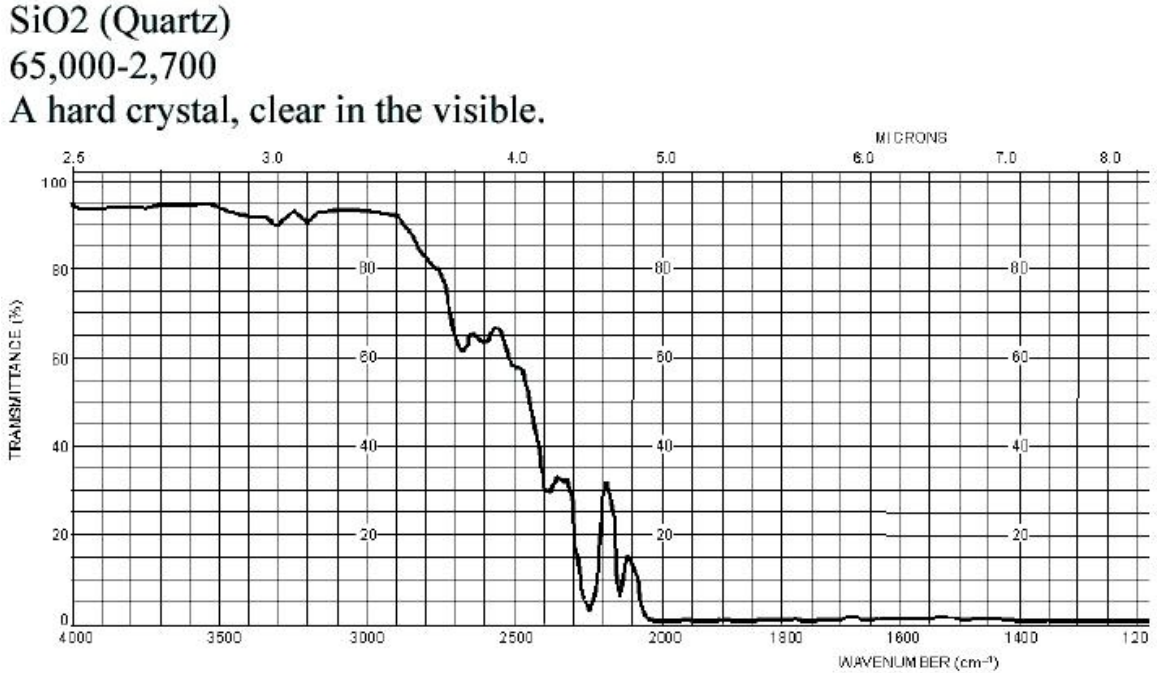

Figure 5.1: Transmittance of quartz versus wave number [5]

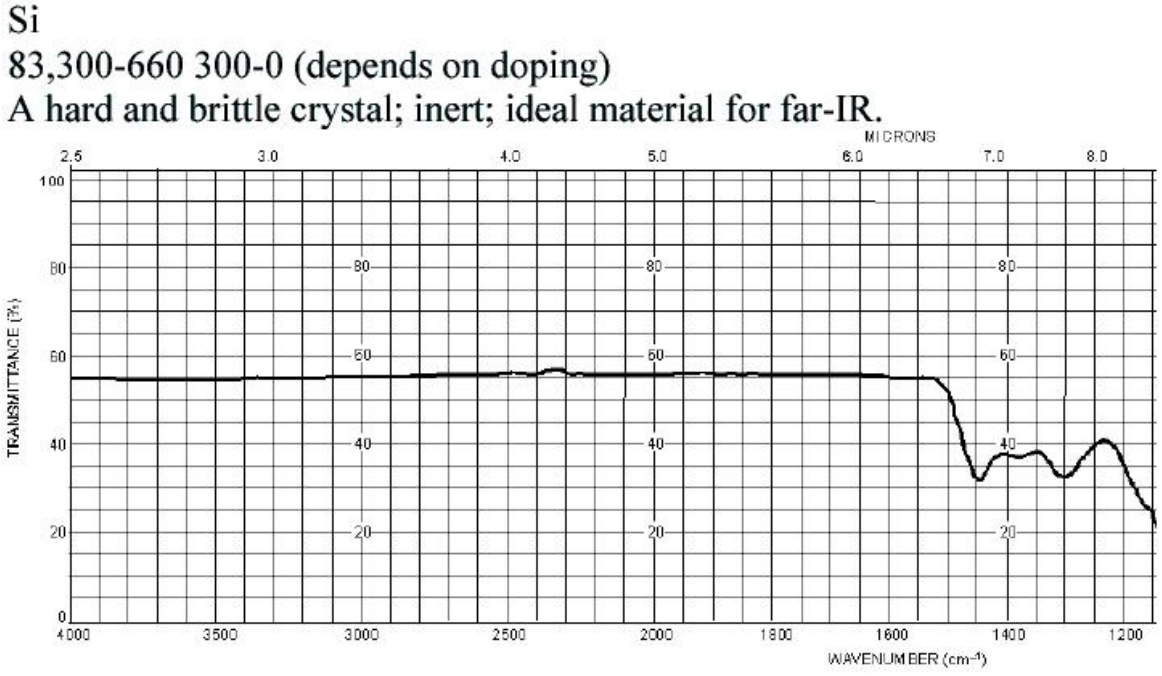

Figure 5.2: Transmittance of silicon versus wave number [5]

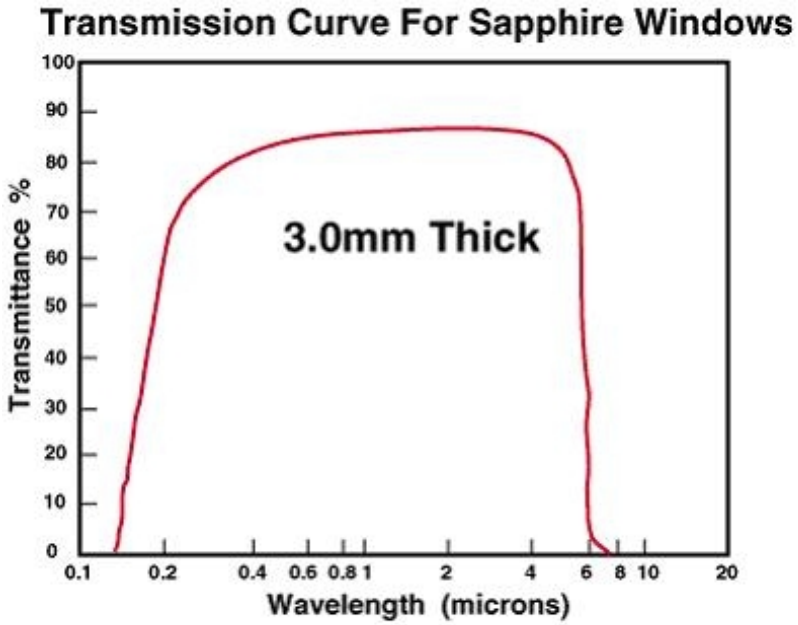

Figure 5.3: Transmittance of sapphire versus wavelength [5]

samples are 0.5 mm thick. The quartz square is 0.66 mm thick, and the silicon square is 0.4 mm thick.

5.2 Test procedure

After placing the samples on the infrared camera stage and performing a two temperature calibration the reference radiation image in Figure 5.4 was recorded. This image shows the locations of the samples. Figure 5.5 shows the stage and samples at 100 °C, this image ensures proper camera calibration.

The materials are then raised off of the infrared camera stage using wooden stands approximately 5 mm thick. The samples are aligned with the earlier radiation reference image. The centers of the samples now show the camera stage temperature as seen by the camera through the sample material. The material showing the most accurate stage temperature will give the most accurate readings during the device test and should be used as the window in the test fixture.

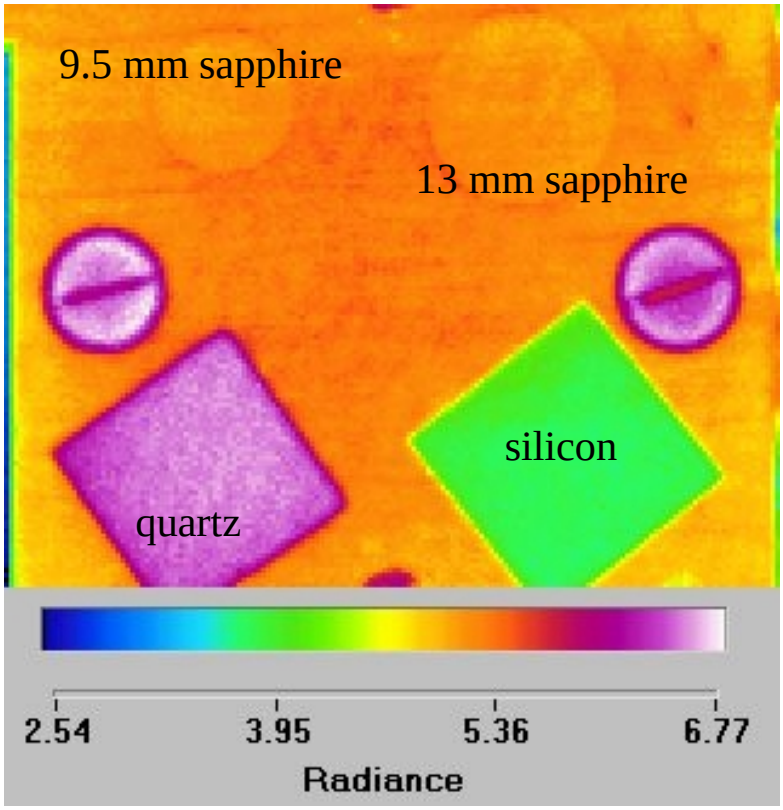

Figure 5.4: Reference radiation image of sapphire, silicon, and quartz samples produced by the infrared camera

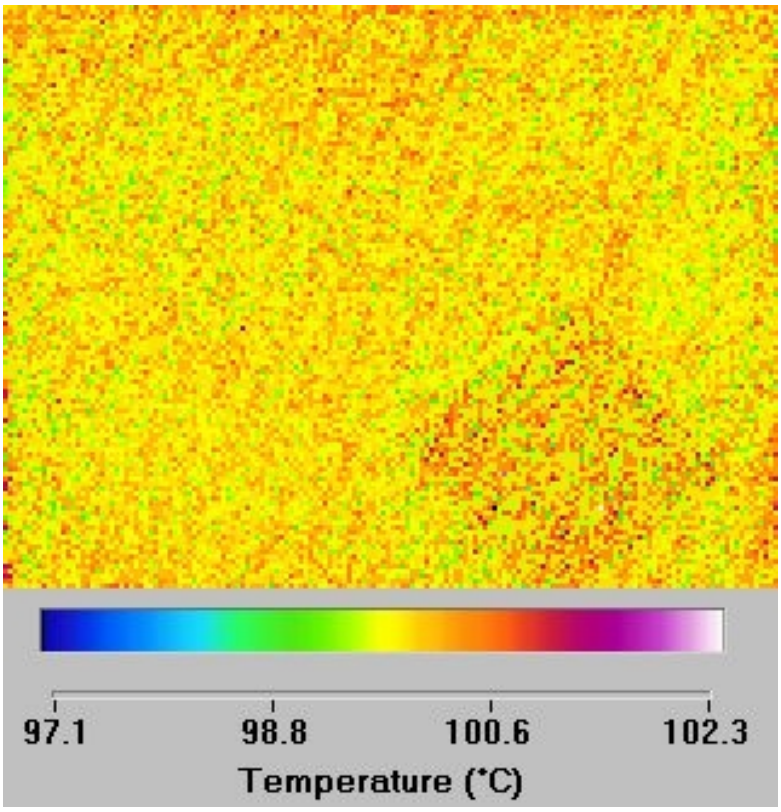

Figure 5.5: The image produced by the infrared camera with the camera stage and material samples at 100 C

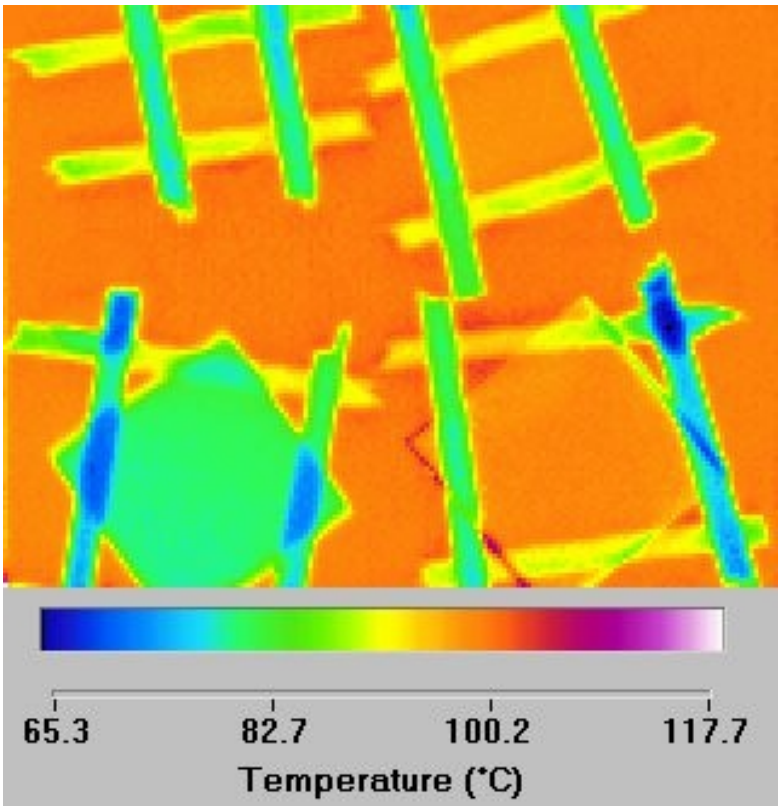

Figure 5.6: The image produced by the infrared camera with the camera stage at 100 C after the material samples were raised off the stage using wooden stands

5.3 Results

Figure 5.6 shows the camera stage at 100 °C through the samples after the introduction of the wooden stands. The silicon and the sapphire show the known stage temperature, but the quartz shows a stage temperature of approximately 80 °C. This is a difference of 20 °C and is unacceptable for the device tests. Figure 5.7 shows the same image as Figure 5.6 with a stage temperature of 80 °C, and Figure 5.8 shows a stage temperature of 50 °C.

These pictures show that as the temperature of the stage drops the quartz still gives the worst reading with a 20 °C average difference. Figure 5.8 shows that the silicon is not as good as the sapphire at 50 °C. This is undesirable because the initial tests will be run with water temperatures no greater than 50 °C. The sapphire is

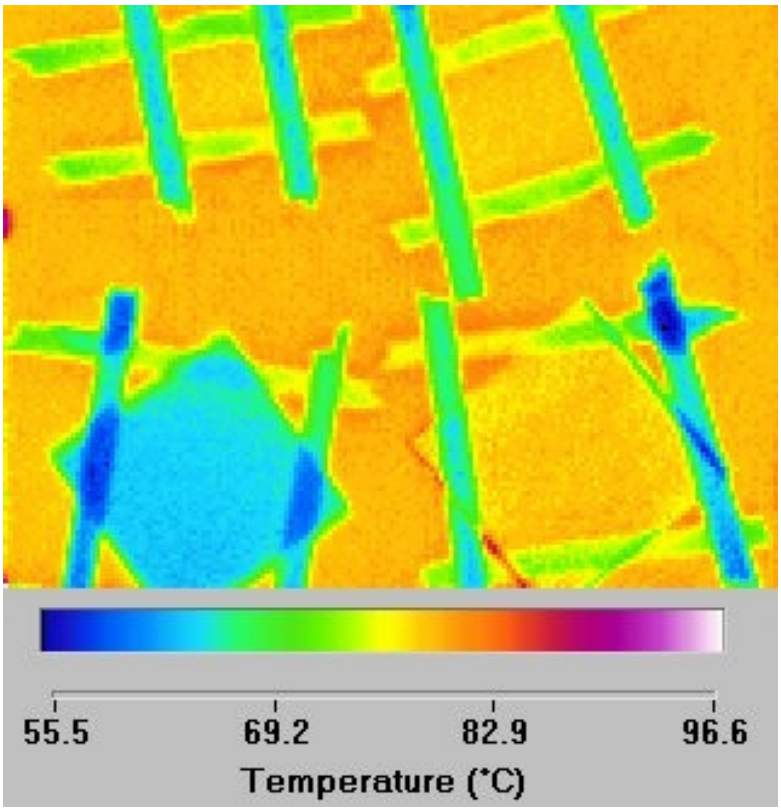

Figure 5.7: The image produced by the infrared camera with the camera stage at 80 C after the material samples were raised off the stage using wooden stands

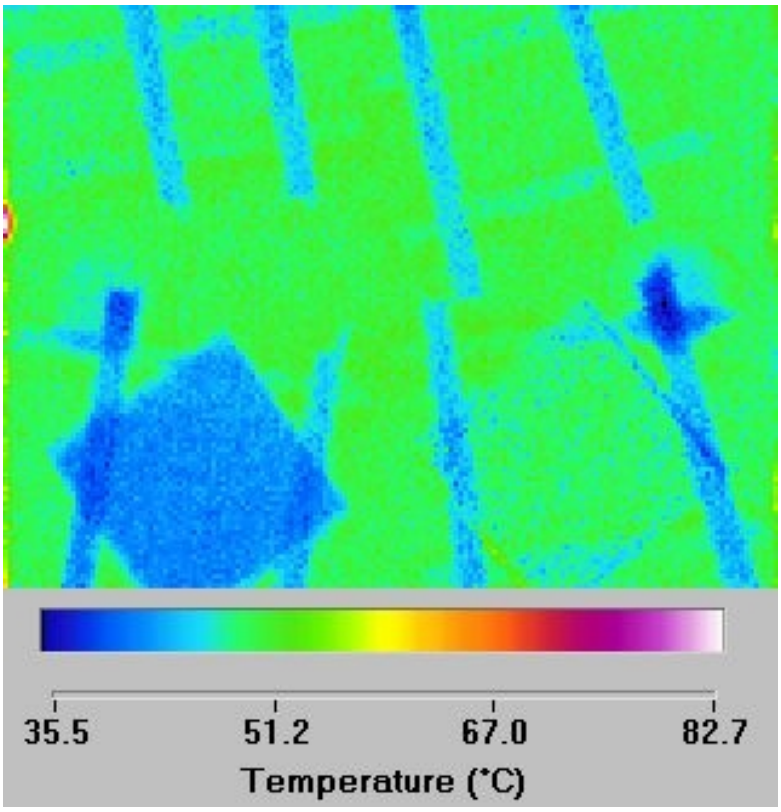

Figure 5.8: The image produced by the infrared camera with the camera stage at 50 C after the material samples were raised off the stage using wooden stands

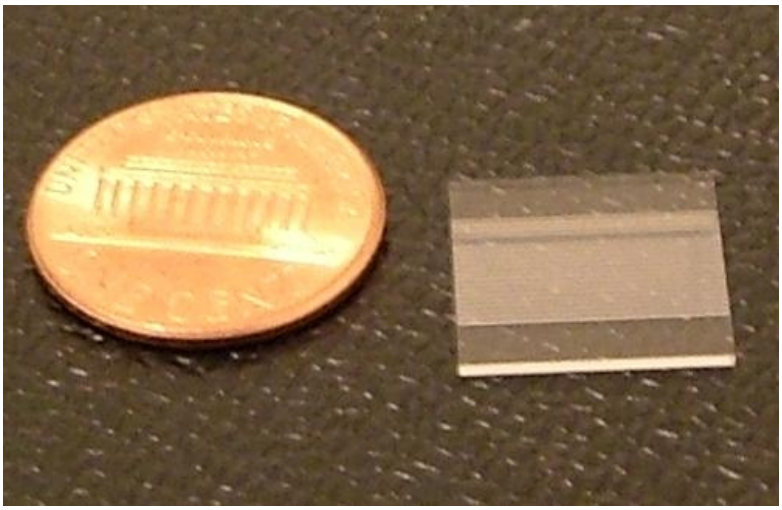

Figure 5.9: Prototype device made of quartz fabricated with a wafer dicing saw

the only material that will not interfere with the infrared imaging and also allow for visible tests. The design of the test fixture allows these windows to be reused.

5.4 Prototype Device

The prototype device provides proof-of-concept for the fluidics portion of the device test. The prototype device is fabricated from quartz using a wafer dicing saw. The prototype device consists of 20 square channels 0.15 mm deep and 0.15 mm wide. Utilizing Equations 2.1, 2.2, and 2.3 in chapter 2, the estimated pressure drop through these channels is 2 kPa per channel. This represents half of the estimated pressure drop per channel for the silicon device. Figure 5.9 shows the completed prototype device.

5.5 Flow Test of Prototype Fixture

The prototype test fixture was attached to the pump described in chapter 6 using stainless steel Swagelok fittings and Swagelok plastic tubing with stainless steel tubing inserts. The test fixture utilizes several specially cut Neoprene rubber gaskets. The first gasket is 0.08 cm thick and sits under the prototype device to ensure proper

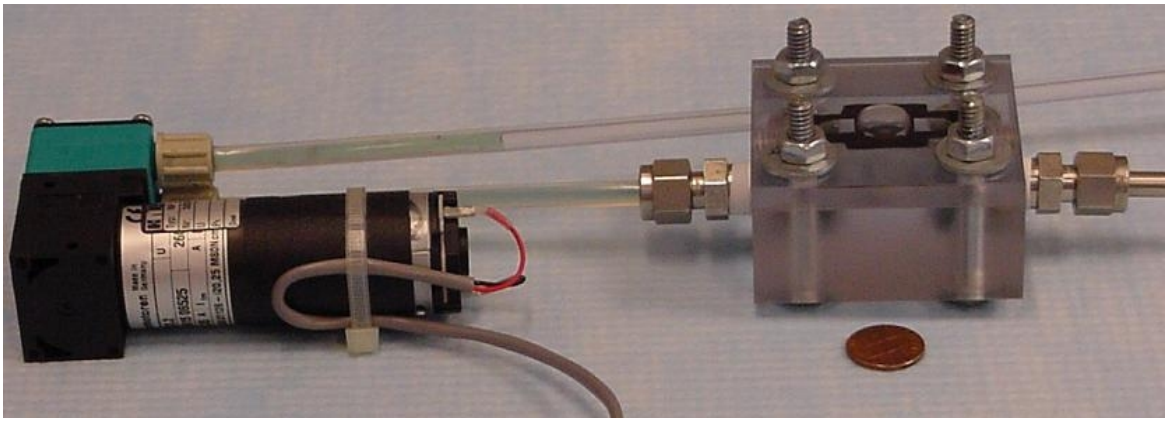

Figure 5.10: The prototype test fixture and device attached to the pump for fluid tests

sealing. In the final test fixture this gasket is replaced with the heater and heater insulation. See chapter 6 for a schematic of this configuration. The second Neoprene rubber gasket is also 0.08 cm thick and is placed between the bottom of the test fixture and the lid of the test fixture. This gasket provides sealing around the device. A similar gasket is used in the final test fixture design. Figure 5.10 shows the pump and prototype fixture.

Because the estimated pressure drop through the prototype device is less than the estimated pressure drop through the final device, the flow rate was increased for the prototype leak tests. The flow rate for these tests was determined using the same method described in chapter 6. The flow test showed no leakage through the prototype fixture.

CHAPTER 6

FLOW LOOP DESIGN

The flow loop is an open-flow loop designed specifically to test the device described in chapter 2. The flow loop design focused on providing consistent conditions for each test. The heater, thermal interface material, and pump were all chosen to ensure test repeatability. The water flows from the bottom of the reservoir to the pump then through the pulse dampener. From the pulse dampener the water flows through the test fixture, containing the device, and returns to the reservoir. Figure 6.1 shows the flow loop during tests, the arrows show the direction of the flow.

6.1 Test Fixture

The test fixture is the most complex part of the flow loop. The bottom section of the fixture contains the heater, the insulation, the thermal interface material, and the device. It also provides the fluid interface to the device. The top section of the fixture holds the sapphire window described in chapter 5. A specially cut 0.08 cm Neoprene rubber gasket sits between the two sections. The two sections then clamp together to provide a leak-free fluid path through the device. Figure 6.2 shows the assembled test fixture with a device in place.

6.2 Heater

The heater consists of 0.81 mm diameter copper wire and 0.16 mm diameter nickel chromium wire. The copper wire is bare and the nickel chromium wire is coated with a thin layer of proprietary insulation from Wiretronic, Inc. The electrically insulating coating melts at 205 °C. The first step in the heater fabrication process

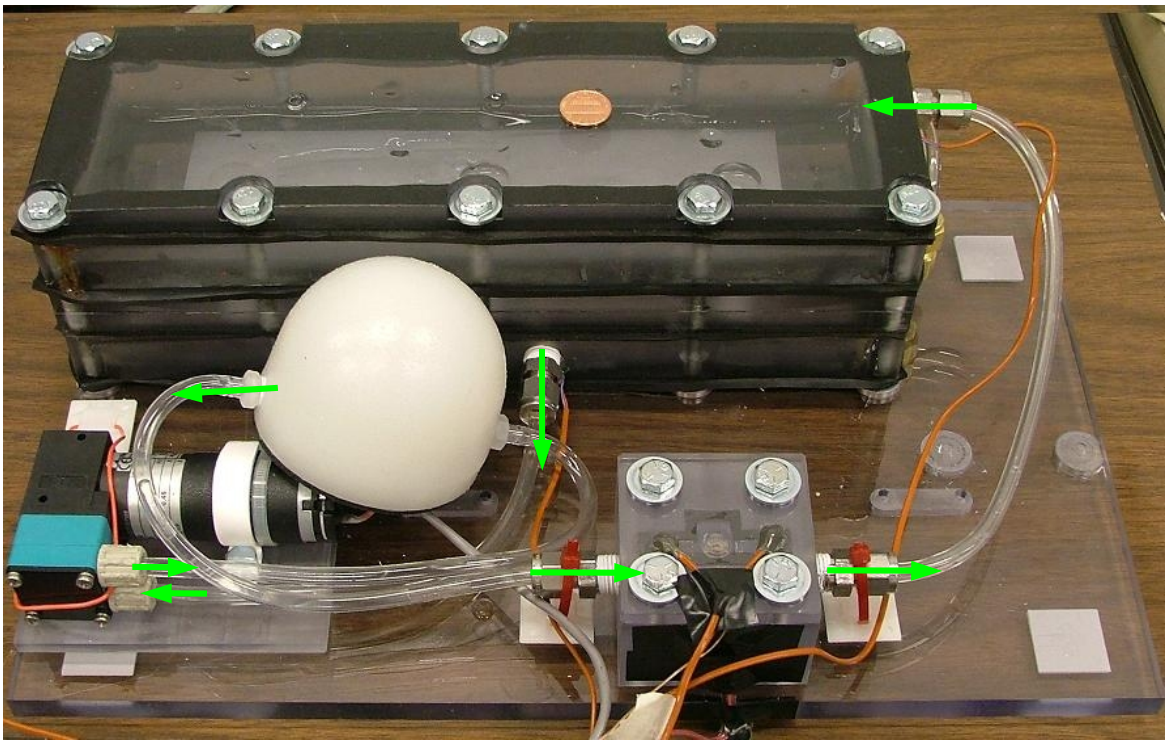

Figure 6.1: Completed flow loop during device testing, the green arrows indicate flow direction during testing.

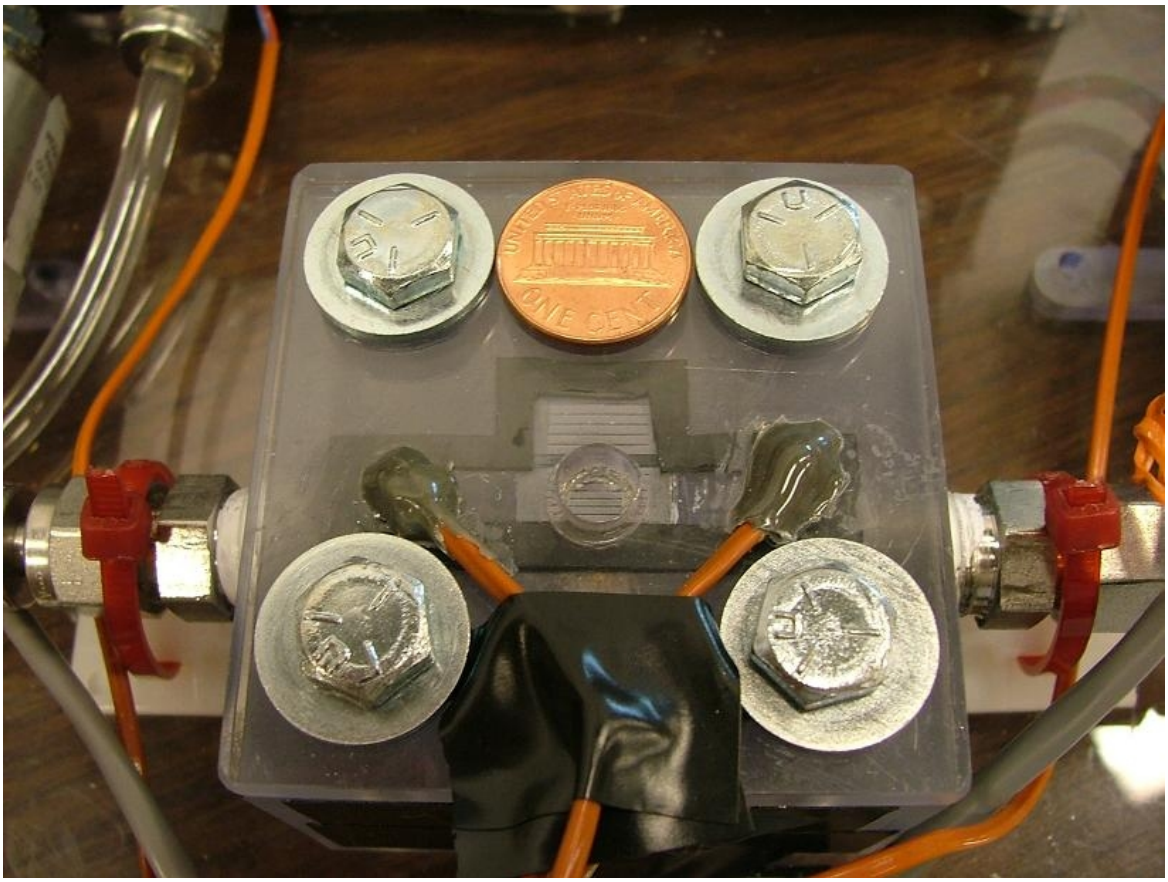

Figure 6.2: Complete, assembled test fixture during tests

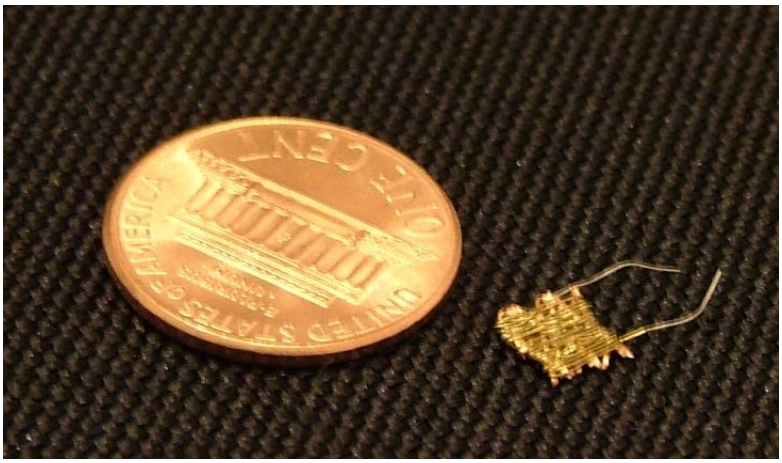

Figure 6.3: Nickel chromium wire resistance heater used for device testing, provides heat fluxes above 20 W/cm^2

involves coiling 15 cm of copper wire. This coil must be flattened to remove air gaps and improve thermal conductivity through the heater. During the second step of the fabrication process 38 cm of nickel chromium wire is wrapped tightly around the copper wire coil. The heater, shown in Figure 6.3, provides 31 Ω of resistance and can produce heat fluxes in excess of 20 W/cm^2. The heater is a square 0.6 cm on a side with a thickness of 0.05 cm.

6.3 Insulation

Thermally insulating silicone adhesive with a thermal conductivity of 0.19 W/mK and a melting temperature of 205 °C holds the heater in the test fixture. The silicone also holds the 0.079 mm diameter thermocouple, described in chapter 4, used to measure the heater surface temperature during testing. The polycarbonate test fixture has a melting temperature of 100 °C. The silicone protects the polycarbonate test fixture from melting during testing. Figure 6.4 shows the heater and thermocouple after installation in the test fixture.

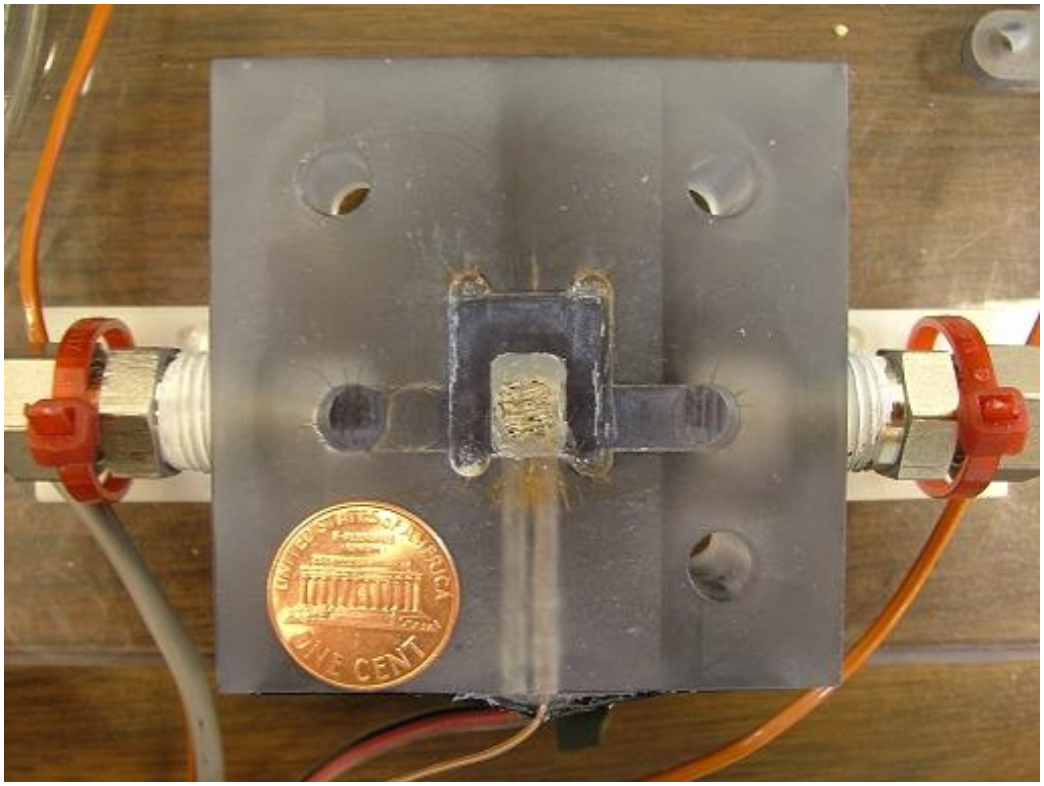

Figure 6.4: Open test fixture without device

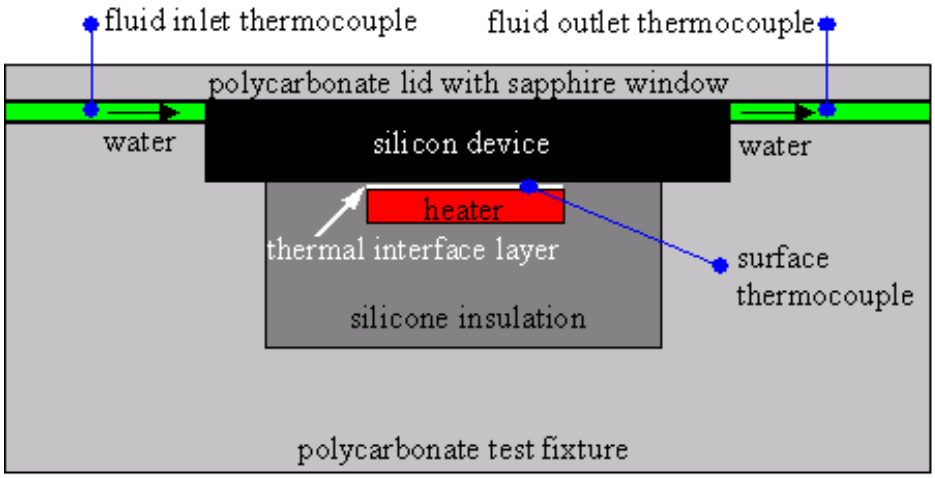

Figure 6.5: Side view drawing of heater installed in the test fixture with a thermal interface layer (not to scale), the thermocouple locations are specified.

6.4 Interface

Figure 6.5 shows a side view schematic of the heater installed in the test fixture. This figure indicates the locations of the thermocouples during testing described further in the following section. The thermal interface material between the heater and the device is a uniform layer of 0.05 mm thick aluminum with a 0.01 mm thick coating of the proprietary material Thermaphase, from Laird Thermal, on both sides. The Thermaphase becomes a highly viscous liquid at 52 °C. This material fills the gaps between the heater and the device to provide a conductive thermal boundary. The interface material has an effective thermal conductivity of 258 W/mK as quoted by the manufacturer.

Tests performed using the infrared camera described in chapter 4 show the repeatability of the test fixture assembly process using the interface material shown in Figure 6.6. Using the equivalent thermal resistance method of evaluation the actual thermal conductivity of the device/heater interface can be described by equation 6.1,

$$T_d = T_s - q_{in}\left(\frac{L_i}{k_i A_h} + \frac{L_d}{k_d A_h}\right) \tag{6.1}$$

where T_d is the temperature at the top of the silicon device, T_s is the temperature of the heater, q_{in} is 7.2 W, the power provided by the heater, L_i is 0.07 mm, the thickness of the interface material, L_d is 0.675 mm, the thickness of the device, A_h is 0.36 cm^2, the cross-sectional area of the heater, k_d is 148 W/mK, the thermal conductivity of the silicon, and k_i is the thermal conductivity of the interface material, 258 W/mK as quoted by the manufacturer. Using the same heater, power, and silicon device for each test makes it possible to assume that the values for T_s, q_{in}, k_d, L_d, and A_h are constant for each test.

The test involved assembling the test fixture with a piece of thermal interface and a silicon device as it would be assembled for the final testing. Then the heater is turned to the maximum power used for the final tests. The infrared camera then images the top of the silicon device. The test was repeated five times using the same silicon device with a new piece of thermal interface material for each test. Each image recorded by the infrared camera showed an average device temperature of 100 °C ± 2 °C. These tests show that the thermal interface material and the test assembly process provide a repeatable interface layer thermal conductivity between the heater and the silicon device

6.5 Thermocouples

The flow loop contains five thermocouples. Two thermocouples are installed in the test fixture lid to measure the temperature of the fluid as it enters and exits the device. Two thermocouples are installed in the reservoir to measure the fluid temperature as it enters and exits the reservoir. The fifth thermocouple measures the temperature between the heater and the device. Another thermocouple, not connected to the flow loop, measures the room temperature throughout the tests.

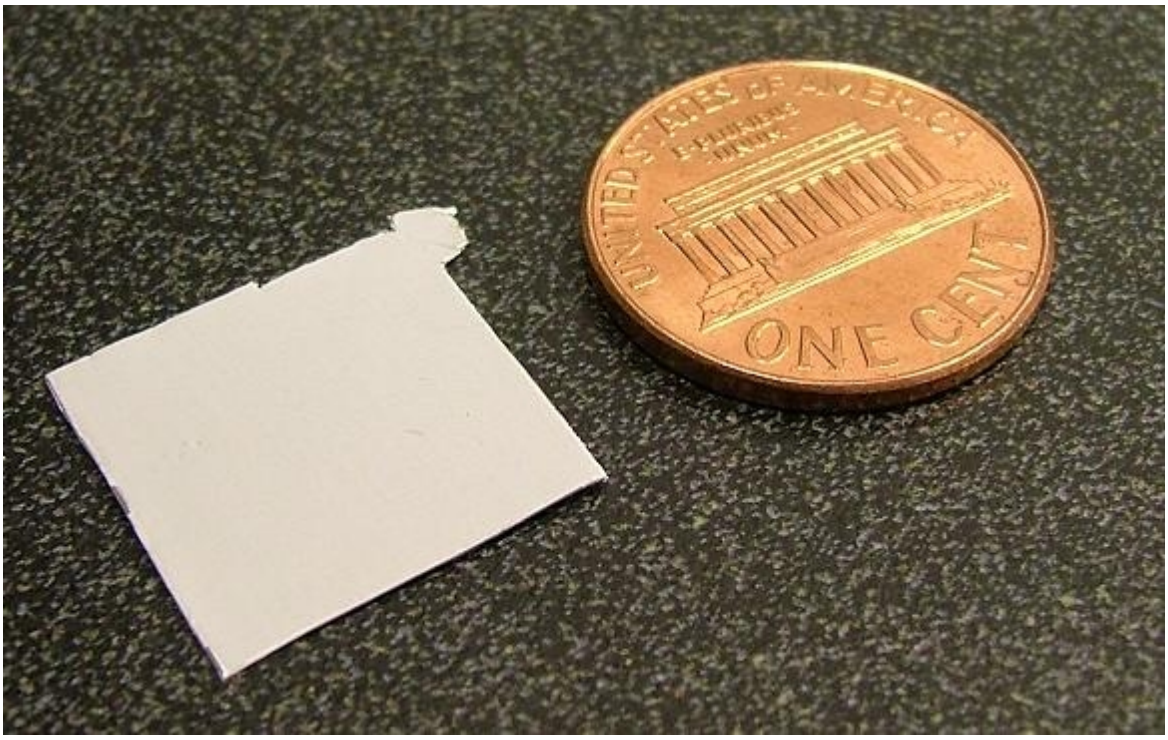

Figure 6.6: Thermaphase on aluminum foil from Laird Thermal provides a consistant interface between the heater and the device.

Figure 6.7: Diaphragm pump and pulse dampener used for device tests.

6.6 Pump and Pulse Dampener

The flow loop also contains the pump and pulse dampener shown in Figure 6.7. The pump is a diaphragm pump from KNF Neuberger, Inc. It can produce a pressure head of 240 kPa (34.8 psi) with a maximum flow rate of 2.83 x 10^{-5} m^3/s (1698 mL/min). The pulse dampener from Cole Parmer Instrument Company reduces the pulsation in the flow caused by the diaphragm pump.

The graduated cylinder described in chapter 4 and shown in Figure 4.3 was used to perform flow rate tests. These tests were performed to determine a flow rate

versus voltage relationship for the pump through the test fixture and device. The pump was turned on to the desired voltage then the water was allowed to flow into the graduated cylinder for two minutes. The amount of water in the cylinder was recorded. The test was repeated 4 times for pump inputs of 5 V, 6 V, 7 V, 8 V, and 9 V. The test was repeated 4 times for each pump input for a device with nanotubes and a device without nanotubes. The voltage versus flow rate equation shown in equation 6.2 was similar for each device.

$$U = 2.9P - 5.3 \tag{6.2}$$

where U is the flow rate in ml/min and P is the power supplied to the pump in Volts.

6.7 Reservoir

The flow loop also contains the reservoir shown in Figure 6.8. The reservoir holds 1.13 L of water. The reservoir also contains a fill hole, air hole, drain hose, and filter paper. The filter paper from Whatman removes particles larger than 2.5 μm from the fluid. Particles could clog the flow path through the devices. The filter paper was changed when it appeared dirty or after several tests involving the devices with nanotubes.

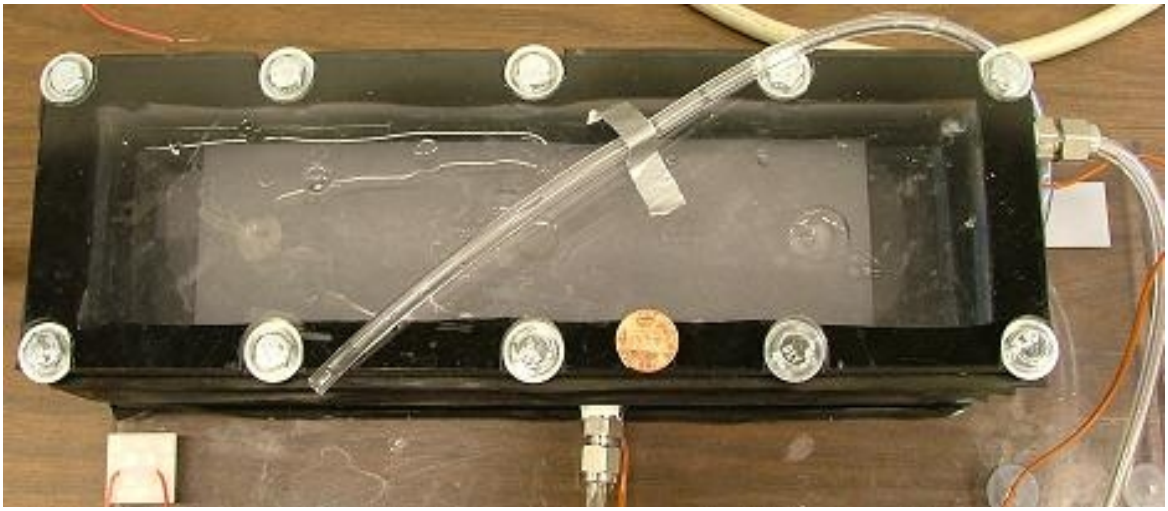

Figure 6.8: Coolant reservior in the flow loop

CHAPTER 7

DEVICE CHARACTERIZATION

7.1 Images Prior to Testing

Images from a Hitachi Scanning Electron Microscope (SEM) were used to characterize the devices. In order to use the SEM the specimen must be mounted to a conductive mount with electrically conductive carbon tape. Figure 7.1 shows a device ready for the SEM. It is very important to keep the devices clean and free from oils. Any insulating substance on the device might cause poor SEM images. The devices were only handled while wearing gloves.

Images of the devices were recorded before and after testing to determine the average surface area of the nanotubes before and after testing. These images show that the nanotube spacing is consistent. The nanotube density was determined by recording random images in different locations on the devices and counting the number of nanotubes present in each image. The scale on the image is used to determine the overall image size. The following expression was used to determine the average nanotube spacing for each device,

$$N = \frac{n}{A_c} \tag{7.1}$$

where N is the number of nanotubes per μm^2, n is the number of nanotubes counted in each image, and A_c is the cross-sectional area visible in the picture in μm^2. The blue squares in Figure 7.2 show the approximate locations of the images used to determine the density of the nanotubes. Figure 7.3 shows one image used to determine the density of the dense nanotubes. Figure 7.4 shows one image used to determine the density of the sparse nanotubes. The bright white spots circled in red on the image

Figure 7.1: Device prepared for imaging with the SEM

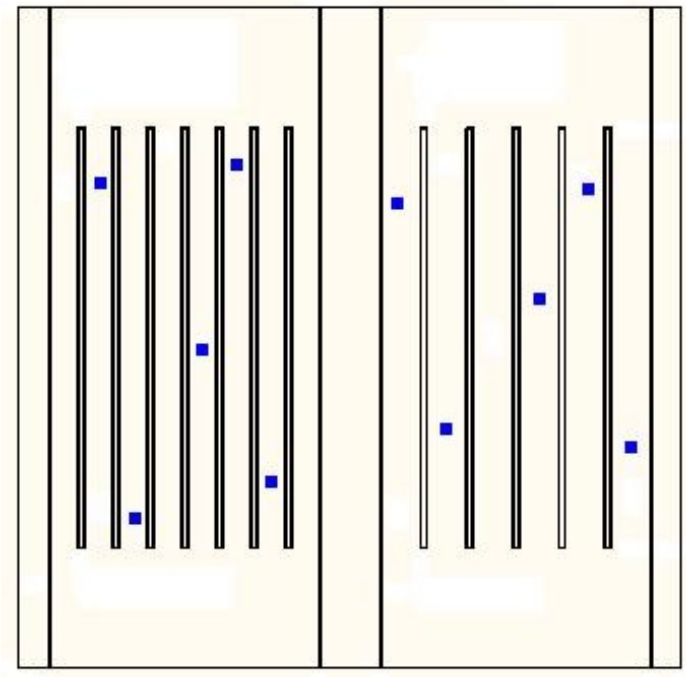

Figure 7.2: Blue squares show the approximate locations of SEM images used to determine nanotube density

are examples of the spots described below.

The average nanotube density for the dense nanotube devices is approximately five nanotubes per μm^2. This density gives 2.5×10^8 nanotubes per device for the narrow channels and 2.6×10^8 nanotubes per device for the wide channels. The average nanotube density for the sparse nanotube devices is approximately 0.04 nanotubes per μm^2. This density gives 1.9×10^6 nanotubes per device for the narrow channels and 2×10^6 nanotubes per device for the wide channels.

During nanotube imaging bright spots on the wafers were noticed. These spots were present both on the areas with and without nanotubes. The spots may have resulted from dust particles present on the wafers during the patterning and etching process. Figure 7.5 shows an average image of the spots. The density of the spots was determined using the same process used to determine the density of the nanotubes. There are 4×10^3 spots per device for the narrow channels and 4.2×10^3 spots per

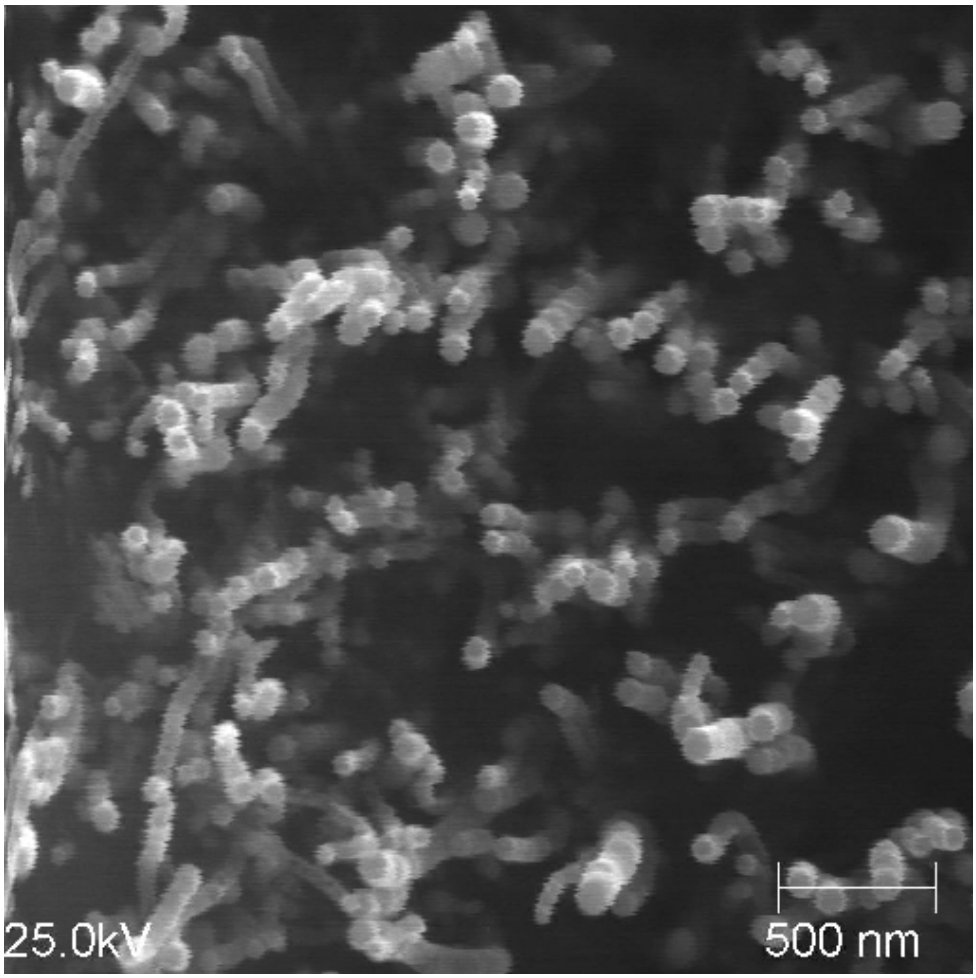

Figure 7.3: A sample SEM image of the dense nanotubes before testing used to determine the nanotube density

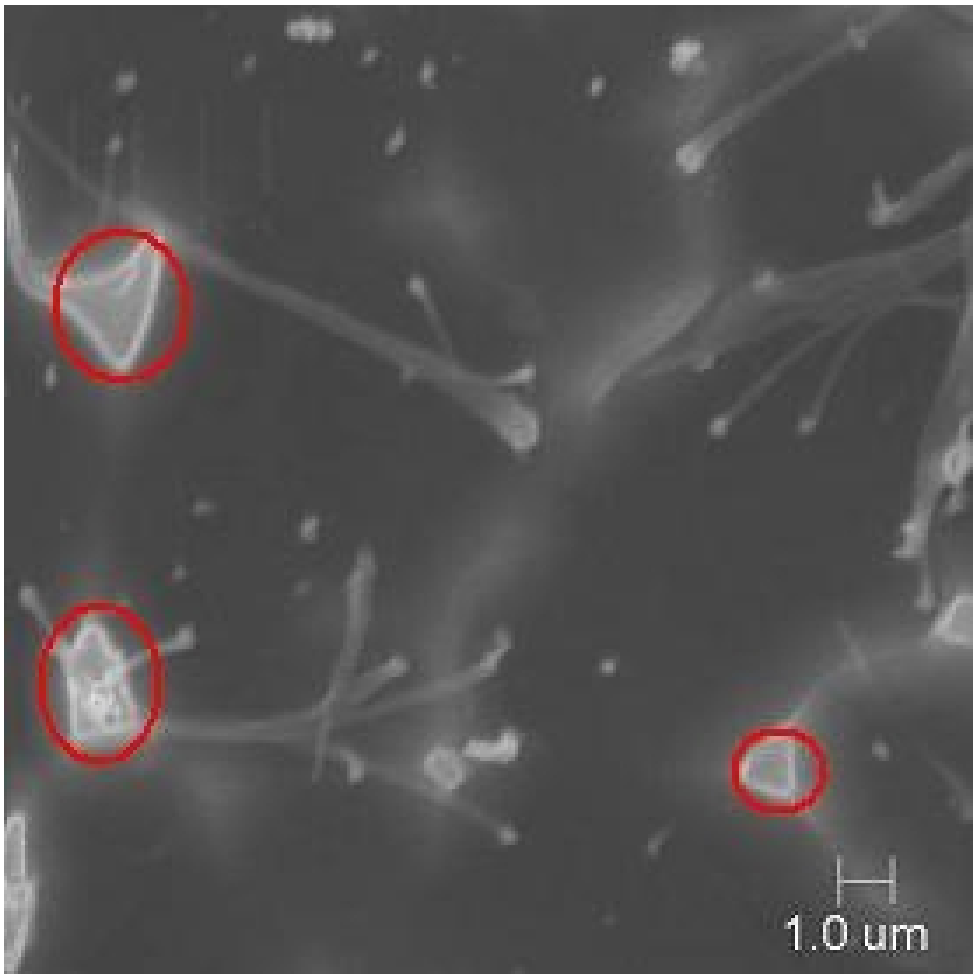

Figure 7.4: A sample SEM image of the sparse nanotubes before testing used to determine the nanotube density, the red circles indicate white spots described below.

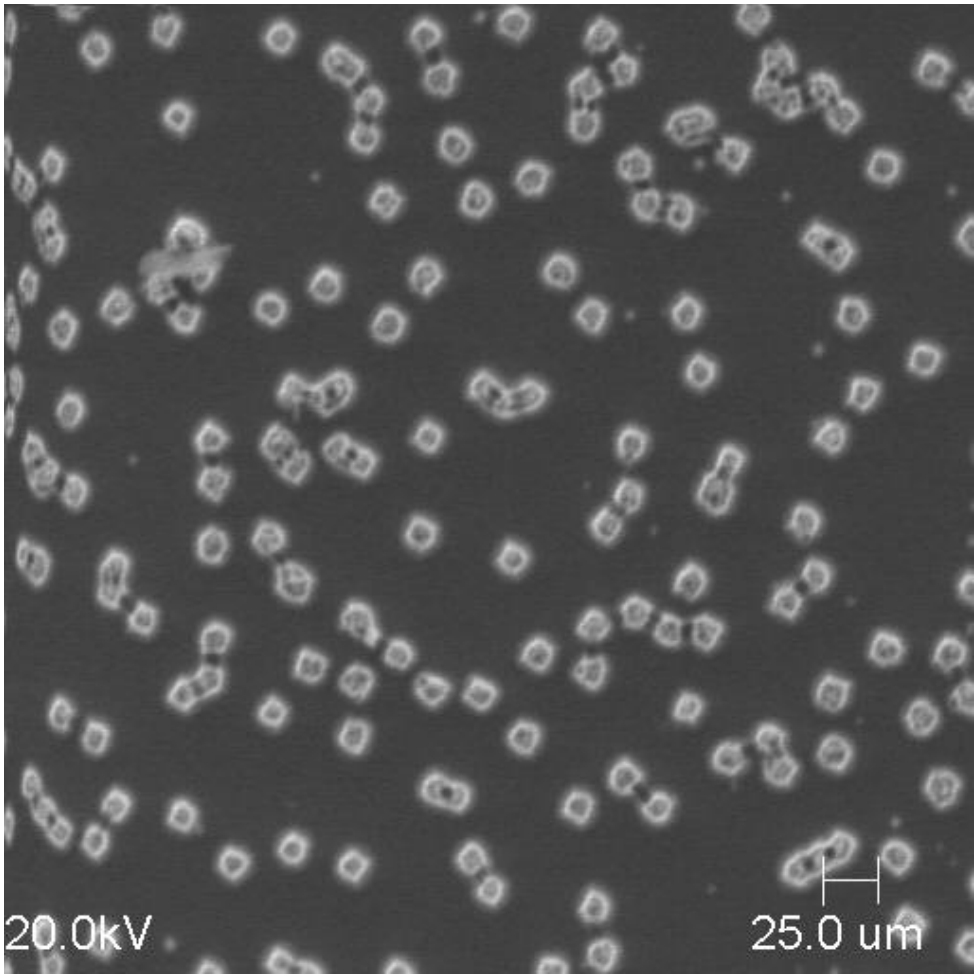

Figure 7.5: A sample SEM image of the white spots used to determine the density of the spots

device for the wide channels.

Using the profilometer the spots were determined to be between 200 and 400 nm tall. This represents less than 1 % of the height of the nanotubes. Using the design drawings and Equation 7.2, the surface area of the narrow channels is 51.2 mm^2 and the surface area of the wide channels is 53.1 mm^2.

$$A_c = W_c L_c M \tag{7.2}$$

where A_c is the bottom surface area of the channels covered with nanotubes in mm^2, W_c is the width of the channels in mm, L_c is the length of the channels in mm, and M

is the number of channels per device. Similarly Equation 7.3 was used to determine the surface area of the nanotubes,

$$A_n = 2\pi r h \tag{7.3}$$

where A_n is the surface area of a single nanotube or spot in mm^2, r is the radius of a nanotube or spot in mm, and h is the height of a nanotube or spot in mm. A_n equals 4.7×10^{-7} mm^2 for a nanotube and 1.4×10^{-5} mm^2 for a white spot. This value is then used in equation 7.4 to determine the overall surface area increase over the estimated surface area of a device,

$$A_s = A_n \cdot N_d \tag{7.4}$$

where A_s is the total surface area of the nanotubes in the device in mm^2, A_n is the surface area of a single nanotube from equation 7.3 in mm^2, and N_d is the number of nanotubes per device. Adding A_s to A_c from Equation 7.2 gives the total fluid exposed bottom surface area of each device configuration. The spots increase the surface area slightly over the surface area calculated in equation 7.2. The bottom surface area of the narrow channels with the spots is 51.3 mm^2 and the bottom surface area of the wide channels with the spots is 53.2 mm^2. The sparse nanotubes increase the bottom surface area of the channels more than the spots. The bottom surface area of the narrow channels with sparse nanotubes and spots is 52.2 mm^2 and the bottom surface area of the wide channels with sparse nanotubes and spots is 54.1 mm^2. The dense nanotubes increase the bottom channel surface area the most. The bottom surface area of the narrow channels with dense nanotubes and spots is 169.3 mm^2, an increase of 118 mm^2 over the estimated area of the channel bottom without nanotubes. The bottom surface area of the wide channels with dense nanotubes and spots is 175.6 mm^2, an increase of 122.4 mm^2. This represents an almost 230 % increase in bottom surface area over the channels without nanotubes.

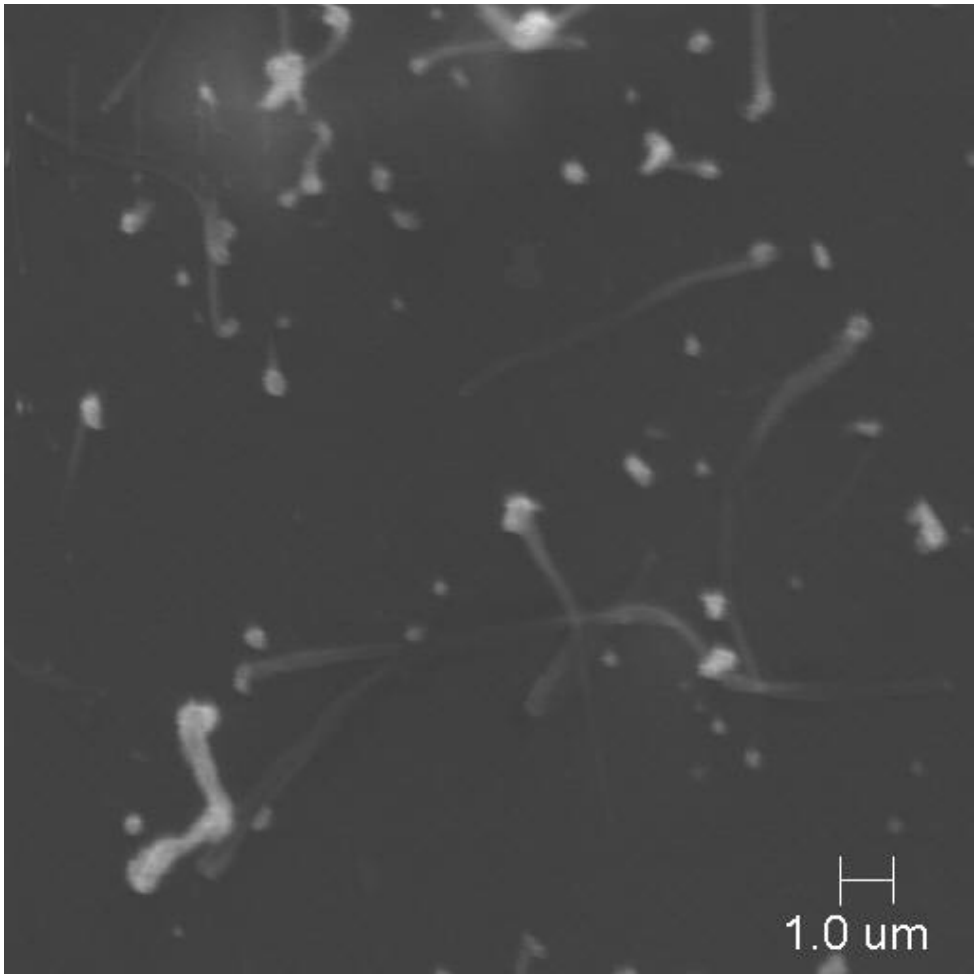

Figure 7.6: A sample SEM image of the sparse nanotubes after testing

7.2 Images After Testing

Images of the nanotubes after testing are also recorded. Figure 7.6 shows the sparse nanotubes after testing. There is no discernible difference between the images before and the images after testing for the sparse nanotubes.

The images of the dense nanotubes after testing showed a remarkable difference. Figure 7.7 shows the dense nanotubes after testing. The nanotubes seem clumped together after testing. They are not wet in this image. It seems that testing causes them to be attracted to one another. The scope of this project did not allow for much investigation into this interesting observation. It is significant

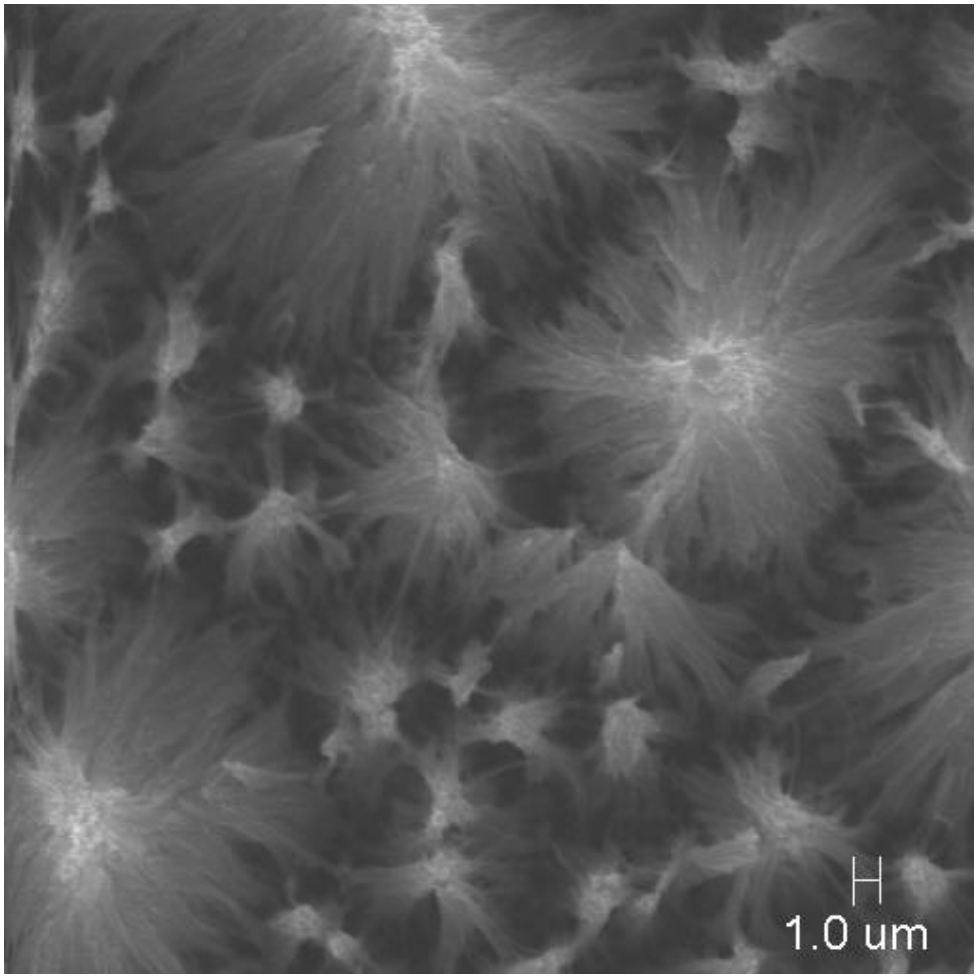

Figure 7.7: A sample SEM image of the dense nanotubes after testing

to note that while they appear to be affected by the tests, the density of the nanotubes does not change as a result of testing. This answers two key questions. The nanotube interface with the silicon substrate is strong enough to withstand the water flow. Also, it appears as though some water must be flowing through the nanotubes. Recommendations regarding this observation are discussed later.

CHAPTER 8

DEVICE TESTING AND INTERPRETATION

8.1 Objectives and Assumptions

The device tests were designed to obtain the surface temperature of the device and the mean fluid temperature during device cool-down. The mean fluid inlet temperature used in section 8.3 is assumed to be the average of the device inlet fluid temperatures for all the tests as measured by the thermocouple in the test fixture lid. The mass flow rate of the fluid and the fluid properties are assumed to be the same for each test. The mass flow rate is 1.36×10^{-4} kg/s $\pm$ 1.67×10^{-5} kg/s for all the tests. This value was determined from the tests described in section 6.6. The fluid properties are taken at the average mean fluid temperature during the tests. As discussed in chapter 6, the interface between the heater and the device is assumed to be the same between tests, and the thermal conductivity of the silicon is assumed invariant between tests.

8.2 Procedure

The tests consist of three steps. First, the pump is turned on, water flows through the system for one minute. Then the heater is turned on to 5.4 W $\pm$ 0.25 W. The heater remains on for 10 minutes while the system reaches steady state conditions. Steady state conditions are assumed when the standard deviation of the mean fluid temperature during a 1 minute period is less than 0.5 °C. Finally, the heater is turned off. The LabVIEW program discussed in chapter 4 records the thermocouple data throughout the test and for 5 minutes after the heater is turned off. Table 8.1 shows the device geometries tested.

Table 8.1: Details of device tests

Device Number	Channel Width (μm)	Nanotube Density
101	682	no nanotubes
102	942	no nanotubes
201	682	no nanotubes
202	942	no nanotubes
111	682	2.5 x 10^8/device
112	942	2.5 x 10^8/device
211	682	2.5 x 10^8/device
212	942	2.5 x 10^8/device
121	682	1.9 x 10^6/device
122	942	1.9 x 10^6/device
221	682	1.9 x 10^6/device
222	942	1.9 x 10^6/device

The infrared camera is used to image the device periodically throughout the test. The information from the infrared camera is compared to the thermocouple data to ensure proper readings. The infrared camera also allows for limited flow pattern interpretation during the tests. The images recorded by the infrared camera show variations in temperature across the device channels or along the length of the channels.

8.3 Data Interpretation

The tests were designed to acquire data for use with a transient energy balance. This method is commonly called the lumped capacitance method. This method uses the assumption that the temperature gradients within the solid are negligible at any instant during the transient process. This assumption can never be completely satisfied, however in this case the resistance to conduction within the silicon is small compared to the heat transfer between the silicon and the water. The lumped capacitance method can be applied to two phases of the tests, the heat-up phase, and the cool-down phase. For both phases the lumped capacitance method begins with

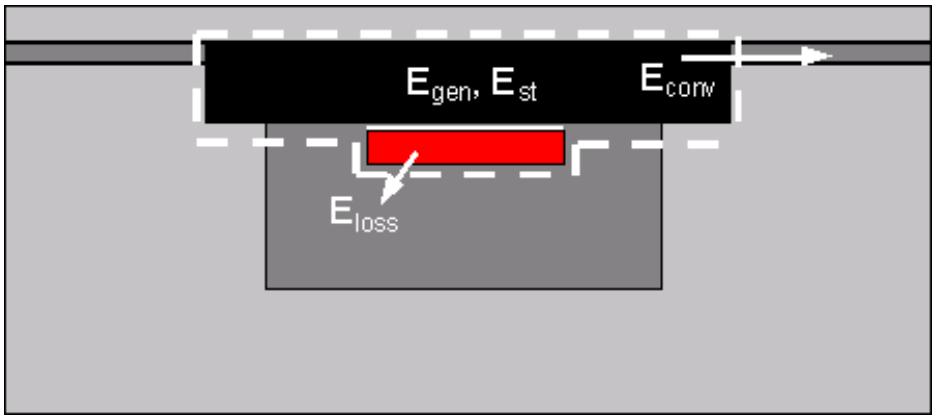

Figure 8.1: A side-view schematic drawing of the heater in the test fixture (not to scale). The white dashed lines show the control volume boundaries.

the energy balance. The cross sectional schematic in Figure 8.1 shows the control volume considered for the evaluation.

8.3.1 Analysis of Transient Heat Transfer During the Heat-Up Phase

The explanation of the heat-up phase using the lumped capacitance method begins with the energy balance in Equation 8.1

$$\dot{E}_{gen} = \dot{E}_{st} + \dot{E}_{loss} + \dot{E}_{conv} \tag{8.1}$$

where $\dot{E}_{gen}$ is the energy input from the heater, 5.4 W for this evaluation, $\dot{E}_{st}$ is described in Equation 8.2, $\dot{E}_{loss}$ represents energy lost through conduction to the insulation, and $\dot{E}_{conv}$ is given in Equation 8.3.

$$\dot{E}_{st} = \rho V c_p \frac{dT}{dt} \tag{8.2}$$

$$\dot{E}_{conv} = hA(T_s - T_{m,i}) \tag{8.3}$$

where h is the convective heat transfer coefficient between the water and the device, A is the surface area of the device in contact with the water, T_s is the surface temperature of the device, and $T_{m,i}$ is the mean fluid inlet temperature of the water. Using the value of θ in Equation 8.4, Equation 8.5 results from substitution into

Equation 8.1

$$\theta = T_s - T_{m,i} \tag{8.4}$$

$$\frac{d\theta}{dt} = \frac{\dot{E}_{gen} - \dot{E}_{loss}}{\rho V c_p} + \frac{hA}{\rho V c_p}\theta \tag{8.5}$$

Using the separation of variables and integration combined with the initial condition $\theta(0) = 0$ Equation 8.6 shows the results of solving the non-homogeneous, linear differential equation. Equation 8.7 results from rewriting Equation 8.6. Then Equation 8.9 results from using the definition of $\dot{E}_{conv}$ given in Equation 8.8 and simplifying.

$$\theta(t) = \frac{\dot{E}_{gen} - \dot{E}_{loss}}{hA}(1 - e^{(-\frac{hA}{\rho V c_p}t)}) \tag{8.6}$$

$$\dot{E}_{conv} = (\dot{E}_{gen} - \dot{E}_{loss})(1 - e^{(-\frac{hA}{\rho V c_p}t)}) \tag{8.7}$$

$$\dot{E}_{conv} = \dot{m}c_p(T_{m,o} - T_{m,i}) \tag{8.8}$$

$$T_{m,o} - T_{m,i} = \frac{\dot{E}_{gen} - \dot{E}_{loss}}{\dot{m}c_p}(1 - e^{(-\frac{hA}{\rho V c_p}t)}) \tag{8.9}$$

where $T_{m,o}$ is the fluid temperature at the device outlet, and $T_{m,i}$ is the fluid temperature at the device inlet. For these tests $\dot{m}$, c_p, and $\dot{E}_{gen}$ are invariant between tests. Assuming $\dot{E}_{loss}$ is also the same for each test and utilizing the value $T_{e\max}$ as the maximum fluid temperature at the device outlet, Equation 8.10 results, this is the key to showing enhancement.

$$\frac{T_{m,o} - T_{m,i}}{T_{m,o\max} - T_{m,i}} = \frac{\dot{E}_{gen} - \dot{E}_{loss}}{\dot{m}c_p(T_{m,o\max} - T_{m,i})}(1 - e^{(-\frac{hA}{\rho V c_p}t)}) \tag{8.10}$$

8.3.2 Analysis of Transient Heat Transfer During the Cool-Down Phase

During the cool-down phase of the tests the heater is turned off. The evaluation for the cool-down phase is therefore similar to the evaluation for the heat-up phase, without the $\dot{E}_{gen}$ term. The energy balance for the cool-down phase can be expressed by Equation 8.11

$$\dot{E}_{st} = -\dot{E}_{conv} \tag{8.11}$$

where $\dot{E}_{st}$ is described by Equation 8.12. Where ρ, V, and c_p are taken at 28 °C and are equal for each test. T_s is the temperature of the heater and the silicon device interface as measured with the thermocouple described in chapter 6. Equation 8.13 represents $\dot{E}_{conv}$. Thus Equation 8.11 can be rewritten as shown in Equation 8.14.

$$\dot{E}_{st} = \rho V c_p \frac{dT}{dt} \tag{8.12}$$

$$\dot{E}_{conv} = hA(T_s - T_{m,i}) \tag{8.13}$$

$$\rho V c_p \frac{dT}{dt} = -hA(T_s - T_{m,i}) \tag{8.14}$$

Using the value of θ in Equation 8.15, Equation 8.16 follows from substitution of Equation 8.15 into Equation 8.14. Separation of variables and integration shows that the solution is of the form shown in equation 8.17. Then using the initial condition Equation 8.18 follows, where T_0 is the temperature of the device surface at the beginning of the cool-down phase. Equation 8.19 results from substitution of Equation 8.15 into Equation 8.18. This relationship is the key to showing enhancement between devices.

$$\theta = T_s - T_{m,i} \tag{8.15}$$

$$0 = \frac{d\theta}{dt} + \frac{hA}{\rho V c_p}\theta \tag{8.16}$$

$$\theta(t) = Ce^{(-\frac{hA}{\rho V c_p}t)} \tag{8.17}$$

$$\theta(t) = (T_0 - T_{m,i})e^{(-\frac{hA}{\rho V c_p}t)} \tag{8.18}$$

$$\frac{T_s(t) - T_{m,i}}{T_0 - T_{m,i}} = e^{(-\frac{hA}{\rho V c_p}t)} \tag{8.19}$$

8.3.3 Definition of Enhancement

For the heat-up phase, a plot of the non-dimensional value in Equation 8.20 versus time in seconds will give the thermal time constant τ_f in Equation 8.21. During the heat-up phase, a device with a higher thermal time constant is more resistant to change in the thermal environment and therefore takes longer to heat the water. A

device geometry shall be considered an enhancement over another geometry if the thermal time constant is more than 1.5 times smaller. For the cool-down phase of the tests a plot of the non-dimensional value in Equation 8.22 versus time in seconds will give the thermal time constant τ_t in Equation 8.23. A device with a higher τ_t value is more resistant to changes in the thermal environment. During the cool-down phase of the device tests a device with a higher thermal time constant will take longer to cool-down. Because of the error inherent in the test configuration a device geometry shall be considered an enhancement over another geometry if the thermal time constant is more than 1.5 times smaller.

$$\frac{\theta}{\theta_f} = \frac{T_{m,o} - T_{m,i}}{T_{m,o\max} - T_{m,i}} \tag{8.20}$$

$$\tau_f = \frac{\rho V c_p}{hA} \tag{8.21}$$

$$\frac{\theta}{\theta_i} = \frac{T_s(t) - T_{m,i}}{T_0 - T_{m,i}} \tag{8.22}$$

$$\tau_t = \frac{\rho V c_p}{hA} \tag{8.23}$$

8.3.4 Data Evaluation

In order to assure that erroneous or inconsistent data points are not considered during analysis Chauvenet's criterion was applied to the thirty data points during the heat-up phase and to the forty data points during the cool-down phase of each test [12]. The data points from each test of similar device geometry were then averaged. The resulting data points were used for analysis. This method helps remove testing error.

CHAPTER 9

RESULTS

9.1 Data from Tests

Table 8.1 shows the device geometries tested. Two samples of each device geometry were each tested twice. Figure 9.1 shows a sampling of the raw surface temperature data from different geometries for the entire test run. Figure 9.2 shows the fluid temperature at the device outlet and the device inlet for the same tests. The samples shown here are representative of all 24 tests. Figure 9.2 shows a slight but negligible change in the fluid inlet temperature throughout the tests.

9.2 Data after Analysis

After applying Chauvenet's criterion and averaging data from like geometry tests the following comparisons could be made. Figure 9.3 compares the readings from the thermocouple placed between the heater and the device for the wide channel and narrow channel geometries for the devices without nanotubes. Figure 9.4 shows the same thermocouple readings for the different channel widths for the devices with dense nanotubes. Figure 9.5 shows the heater, device thermocouple readings for the different channel widths for the devices with sparse nanotubes. These figures represent the entire test run, with a constant flow rate of 1.36 x 10^{-4}kg/s $\pm$ 1.67 x 10^{-5} and a heater power of 5.4 W $\pm$ 0.25 W.

Figure 9.6 shows the outlet fluid temperature for the first 15 s of heat-up. Heat-up begins when the heater power is turned on. The sample rate for the tests is 0.5 s so the heat-up phase of testing begins at 60.5 s. Figure 9.7 shows the non-dimensional value given in Equation 8.20 versus time in seconds. This information is utilized to

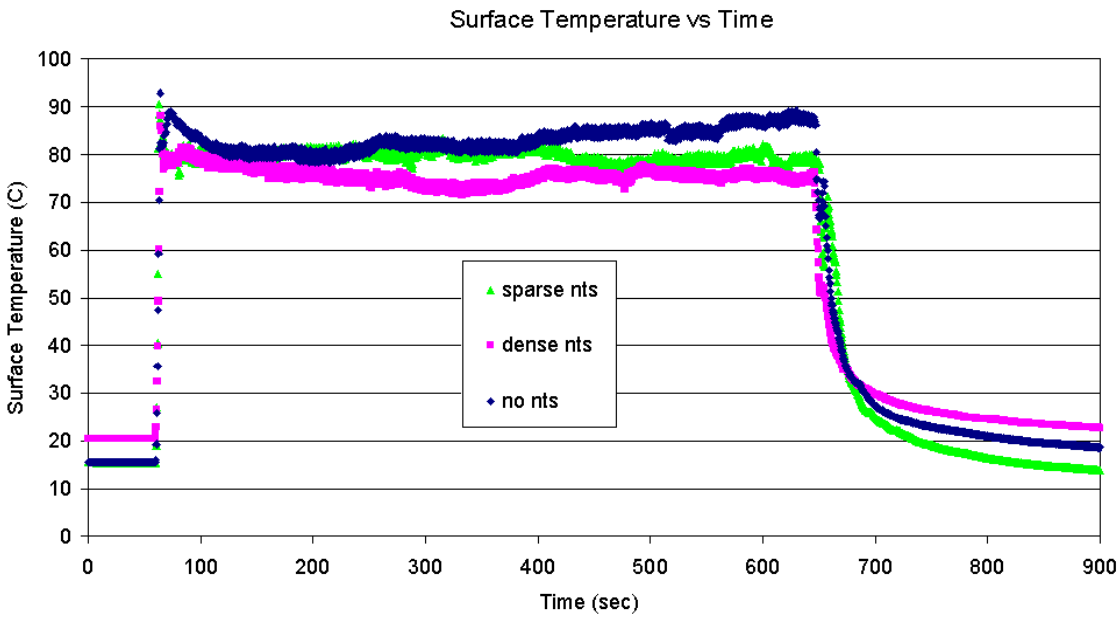

Figure 9.1: Sampling of the surface temperature versus time for three entire device tests

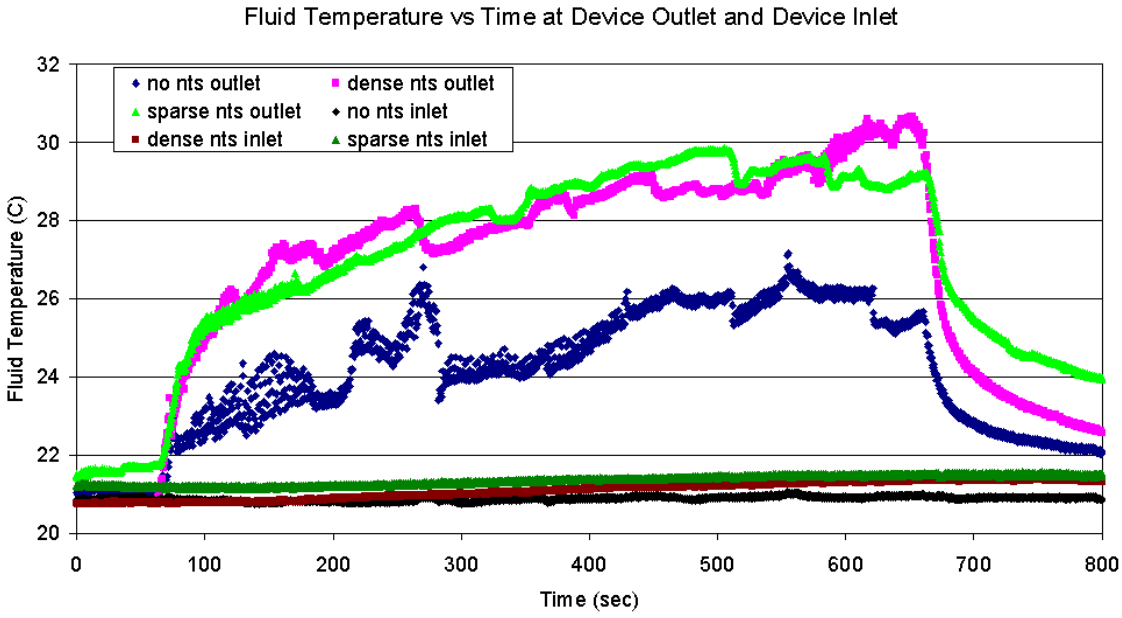

Figure 9.2: Sampling of the fluid temperature at the device inlet and outlet versus time for three entire device tests

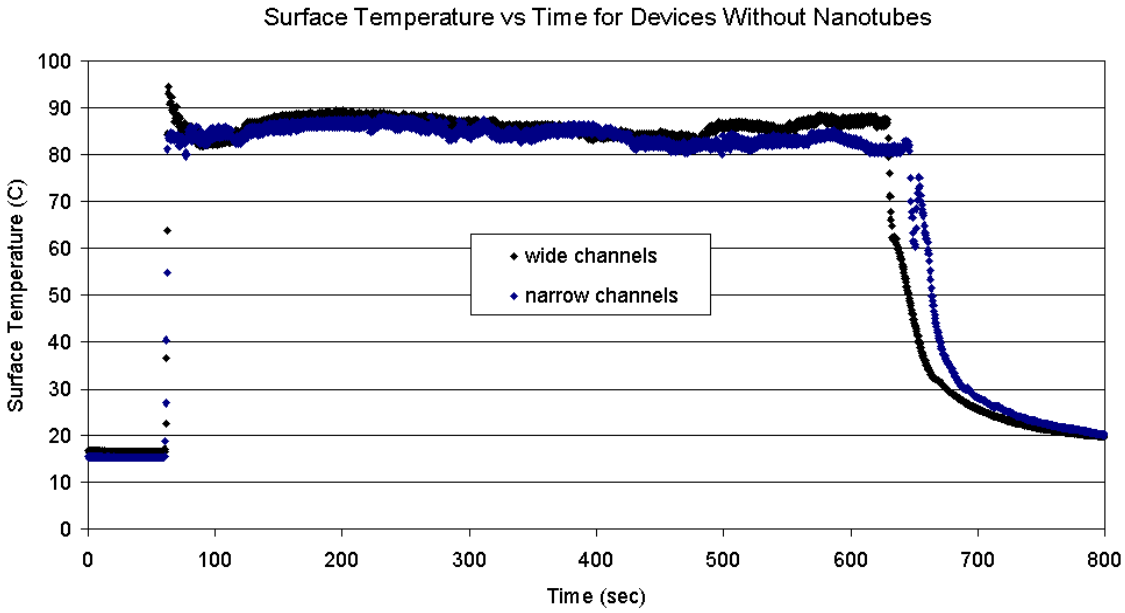

Figure 9.3: Device surface temperature vs time for the devices without nanotubes comparing channel widths

Table 9.1: Thermal time constants for each device geometry for the heat-up phase of testing

Device Geometry	Thermal Time Constant (seconds)
No Nanotubes	20
Sparse Nanotubes	9.5
Dense Nanotubes	9.4

determine the thermal time constants for the devices during the heat-up phase of the tests. Table 9.1 shows the thermal time constants for the devices with no nanotubes, sparse nanotubes, and dense nanotubes.

Figure 9.8 shows the heater, device interface thermocouple data for the first 20 s of cool-down, after the heater power is turned off. The sample rate is 0.5 s for these tests. The beginning of the cool-down phase of the test is therefore assumed to start at 660.5 s. As discussed in chapter 8, plotting the non-dimensional value given in

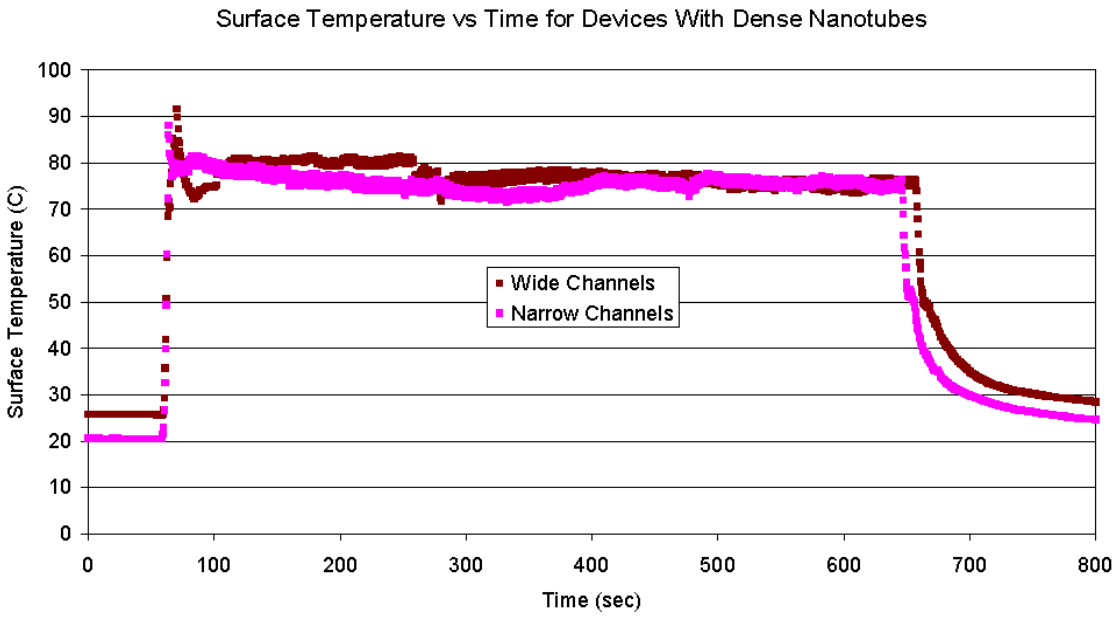

Figure 9.4: Device surface temperature vs time for the devices with dense nanotubes comparing channel widths

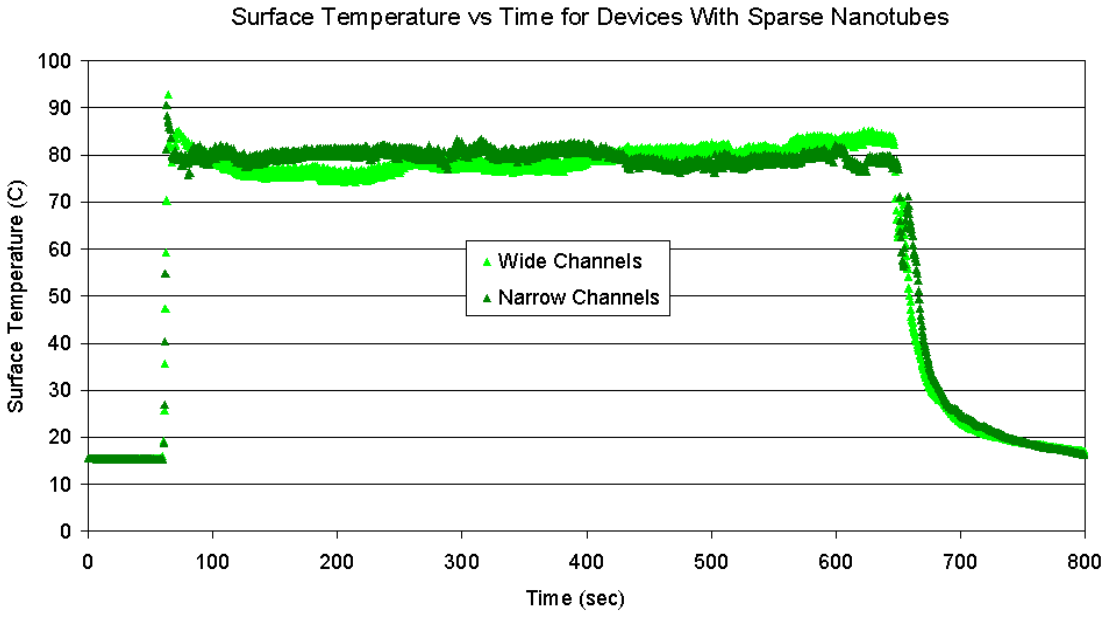

Figure 9.5: Device surface temperature vs time for the devices with sparse nanotubes comparing channel widths

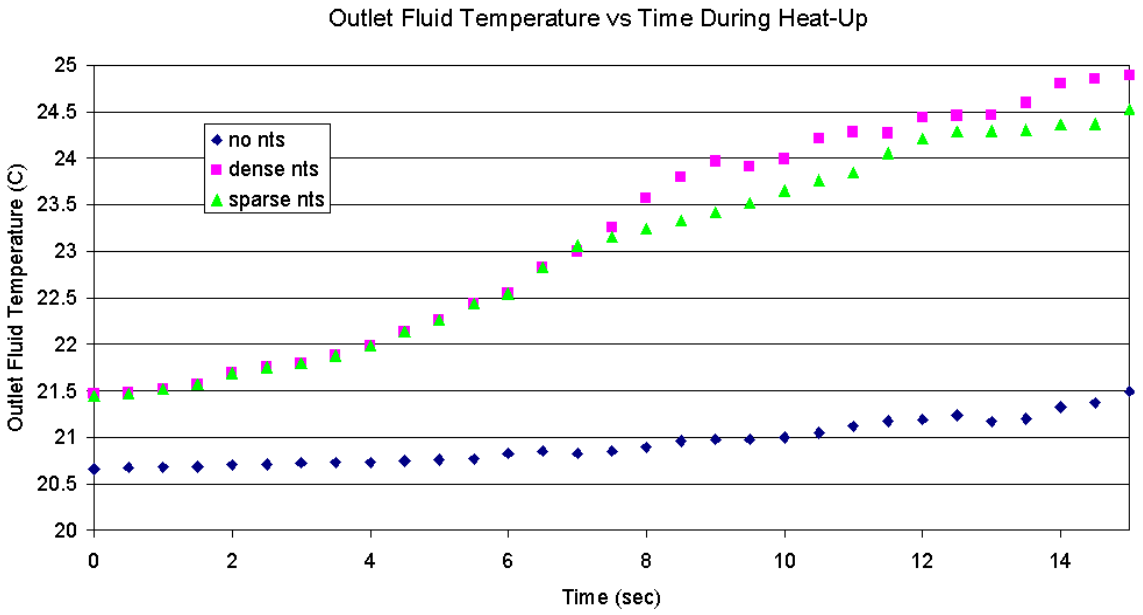

Figure 9.6: Outlet temperature during the first 15s of heat-up for each device geometry

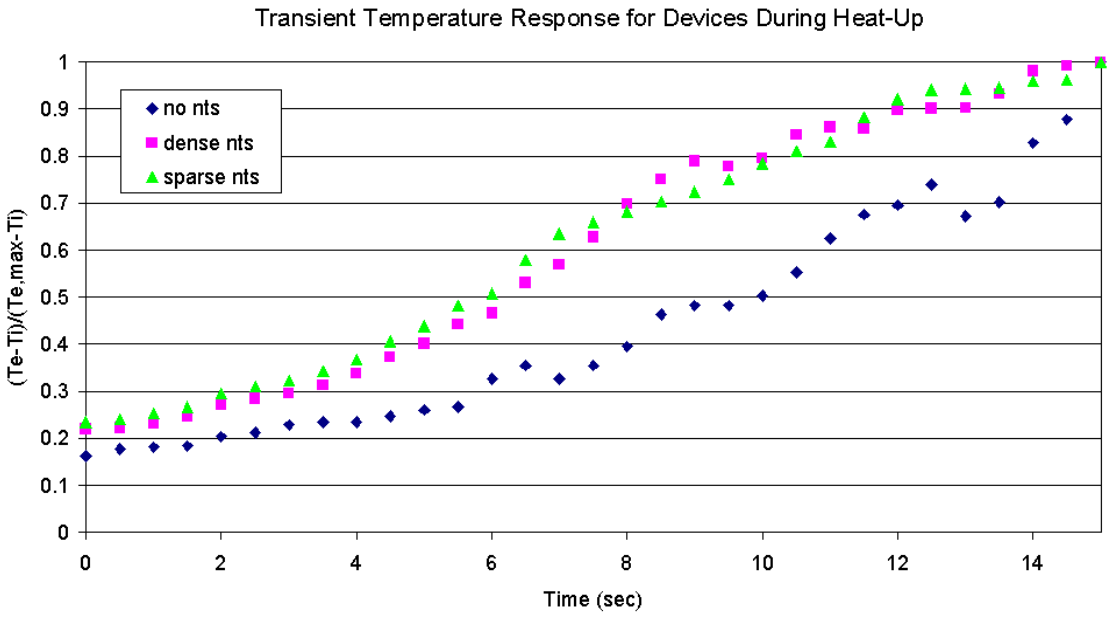

Figure 9.7: Transient temperature responses for each device geometry for the heat-up phase of testing

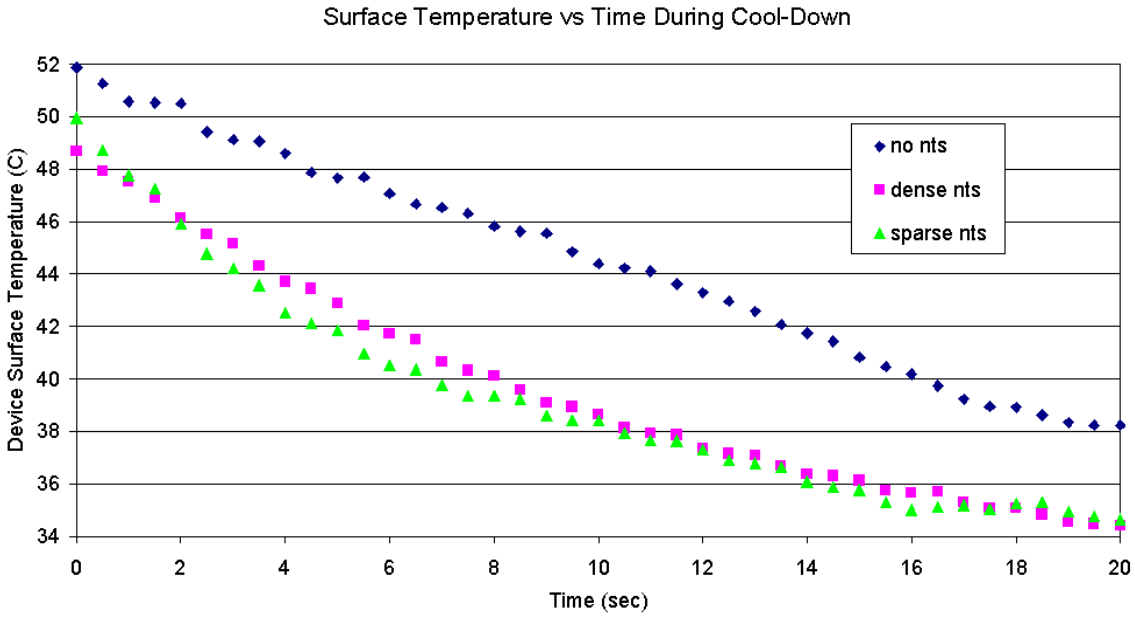

Figure 9.8: Device surface temperature vs time for devices with no nanotubes, dense nanotubes, and sparse nanotubes

Equation 8.22 versus the time in seconds gives the thermal time constant for the cool-down phase of the tests. This value allows for better comparison between geometries than comparing surface temperature. Figure 9.9 shows the non-dimensional plot of the same twenty seconds shown previously. This figure shows an average of the channel widths for the devices without nanotubes, the devices with dense nanotubes, and the devices with sparse nanotubes.

Using this plot we can obtain a thermal time constant for the devices. Table 9.2 shows the value of the thermal time constants for the devices without nanotubes, the devices with dense nanotubes, and the devices with sparse nanotubes.

As a final check of the energy balance the heat transfer due to convection must be less than the power provided by the heater. Equation 9.1 is used to calculate the heat transfer from the device due to convection.

$$q_{conv} = \dot{m} c_p (T_{f,o} - T_{f,i}) \tag{9.1}$$

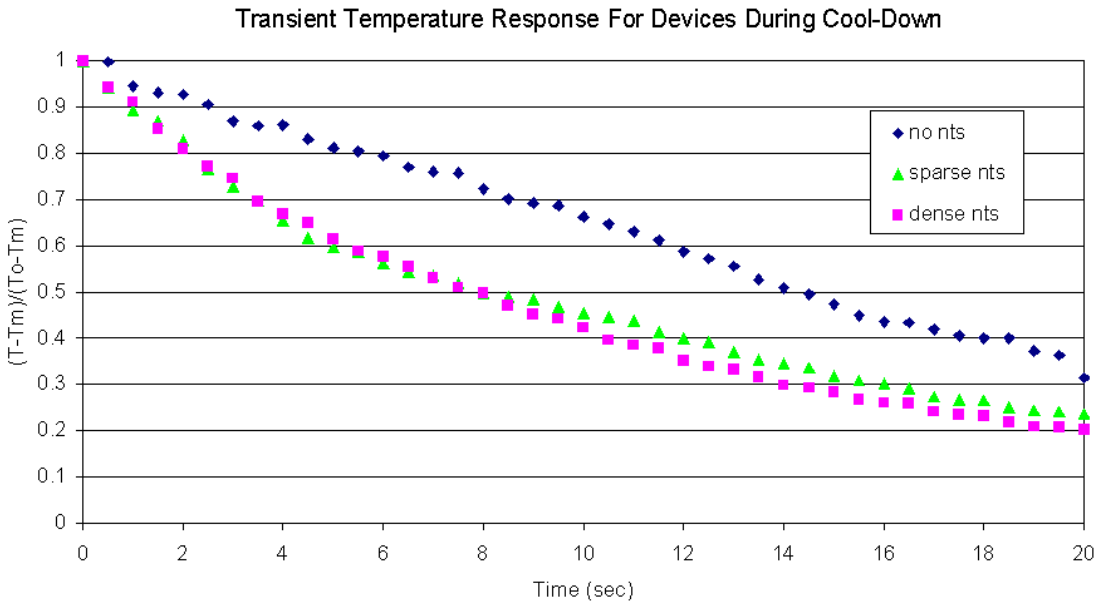

Figure 9.9: Transient temperature response of the devices corresponding to different thermal time constants

Table 9.2: Thermal time constants for each device geometry for the cool-down phase of testing.

Device Geometry	Thermal Time Constant (seconds)
No Nanotubes	21
Sparse Nanotubes	12
Dense Nanotubes	11.5

where $\dot{m}$ is the mass flow rate, 1.36 x 10^{-4} kg/s $\pm$ 1.67 x 10^{-5} kg/s, c_p is the specific heat of water at the average fluid temperature in J/kgK, $T_{f,o}$ is the outlet fluid temperature, and $T_{f,i}$ is the fluid inlet temperature. The heater provides 5.4 W of power for each test. Table 9.3 below shows that for the steady state period of the tests the average q_{conv} for each device is below this value. Any heat input from the heater not reflected in the heat transfer due to convection is lost through conduction to the test fixture and radiation to the environment.

Table 9.3: The heat transfer due to convection for each device geometry.

Device Geometry	Average q_{conv} for Steady State (W)
No Nanotubes	4.6 $\pm$ 0.32
Sparse Nanotubes	4.8 $\pm$ 0.32
Dense Nanotubes	4.9 $\pm$ 0.32

CHAPTER 10

CONCLUSIONS AND RECOMMENDATIONS

10.1 Conclusions

The data obtained from these tests do not show a significant difference between the wide channel geometry and the narrow channel geometry. The tests also do not show a difference between the devices with sparse nanotubes and the devices with dense nanotubes The tests do show a difference between the devices without nanotubes and the devices with nanotubes during the heat-up and cool-down phases of testing. During the heat-up phase of testing the thermal time constant for the devices with dense nanotubes is less than half the thermal time constant for the devices without nanotubes. During the cool-down phase of the testing the thermal time constant for the devices with dense nanotubes is almost half the thermal time constant for the devices without nanotubes. The devices with nanotubes therefore respond more quickly to changes in the thermal environment. Although an optimized design cannot be determined from these tests, the data suggest that the nanotubes enhance the thermal properties of the silicon microchannel devices.

The data also show a higher surface temperature for the devices without nanotubes during the steady state portion of the test. The average heater, device interface temperature for the devices without nanotubes is 84°C, while it is 80°C for the devices with sparse nanotubes and 78°C for the devices with dense nanotubes. These data, combined with the different thermal time constants, suggest that the convective heat transfer coefficient for the devices with nanotubes may be better than the convective heat transfer coefficient for the devices without nanotubes. The heat transfer due to

convection calculations futher support this conclusion. The higher heat transfer due to convection for the nanotube devices imply an improved convective heat transfer coefficient over the devices without nanotubes. The data also show a sharp increase in the heater, device interface temperature immediately following the heater power-on step during testing. This increase likely results from the thermocouple placement during testing. The thermocouple is not in direct contact with the device surface. There is therefore a small time step between the time the heater heats up to the time that the water begins to convect the heat away from the device.

The infrared camera showed pulsations in the flow as well as bubble formation during the tests. It is unclear whether these bubbles are caused by boiling of the water or by deaeration of the water during testing. The surface temperature underneath the device was 80 °C ± 5 °C and this test does not measure the pressure in the fixture during testing so boiling may be a possible explanation. Deaeration would also be a plausible explanation based on the increased water temperature and the pulsation in the flow. It is interesting to note that the bubbles often form in lines along the channels. Figure 10.1 shows an image of the bubbles with the infrared camera. The device channels are aligned up and down in this image. Figure 10.2 shows a photograph of the bubbles during testing at high heater power.

10.2 Recommendations

There are two overall projects, which could logically follow this one. One would analyze boiling, and the other would focus on single-phase flow. The variables for each test are the same.

Since the nanotube density seems to be a viable variable for increasing thermal properties, it is logical to assume that there is an optimal density. This would be for a given height and diameter. There would likely also be an optimal height and an optimal diameter. Optimizing these variables for thermal properties in single-phase

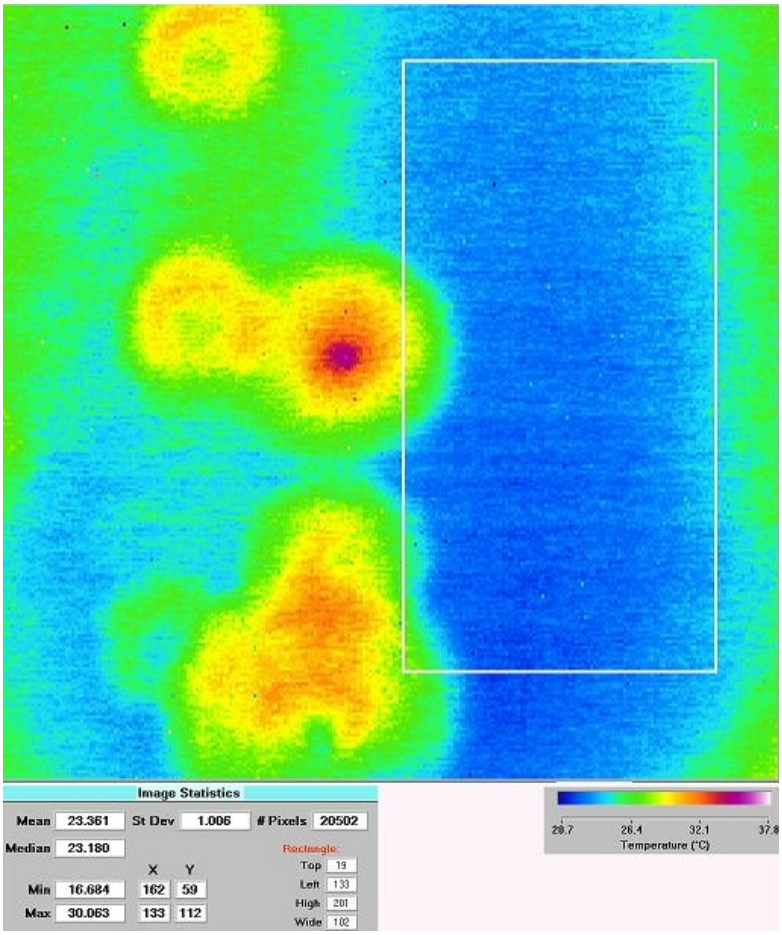

Figure 10.1: An infrared image of bubbles in the device during testing, the values inside the white box are noted in the bottom left corner. The water flow is from bottom to top.

Figure 10.2: A photograph of bubbles in the device during testing, the water flow is from left to right. The circle in the center of the photo is the 9.5 mm sapphire window.

flow would not necessarily mean they would be optimized for boiling conditions.

In order to determine the best nanotube design for single phase flow the flow loop and test fixture would need to be changed. The first issue is the pulsation of the pump. There are gear pumps with almost no pulsation; one of these would have to be used to maintain single-phase flow. The water should be deaerated prior to testing to reduce bubble formation. In order to test the devices under realistic heat fluxes the power supplied by the heater should be increased. A heater similar to the heater used would work but the insulation around it will not. The silicone insulation melts at 205 °C and the electrically insulating coating on the wire also melts at this temperature. Without water flow the heater quickly rose to 150 °C after twenty seconds. There are high temperature insulating epoxies that would work for this application. One that can withstand temperatures up to at least 400 °C should be used. There are also other wire coating options that would remain electrically insulating at higher temperatures. The nanotube design could be a viable solution for single-phase heat transfer in a closed package if the flow rate is high enough to control boiling. Other coolants might also reduce boiling, without causing a loss in the heat transfer. These issues would have to be considered in the package design.

The SEM images of the dense nanotubes after testing showed that the water affects the nanotubes. This effect should be studied further in order to understand the complete role of the nanotubes in fluidic heat transfer. Different coolants may affect the nanotubes in drastically different ways. Knowledge of this interaction would be especially important if the coolant is more viscous than water or if the coolant contains any particles.

A nanotube project focused on boiling should consider drastically different nanotube dimensions than a project focused on single-phase flow. The SEM images of the nanotubes used in these tests showed that the nanotubes bend over and clump together after testing. A well-aligned, up and down nanotube design would likely

offer better boiling enhancement than the nanotubes used in this project.

This project shows that nanotubes affect micro scale systems as well as nano scale systems. Nanotubes could indeed have a great impact on the future of microelectronics cooling. However, none of these advantages will be realized until packaging challenges are met. This project shows that nanotubes affect thermal properties of silicon devices, but they will remain experimental without leak-free fluid packaging.

After determining the optimal device design and nanotube configuration of the silicon device the process should be examined for high temperature substrates. Most of the high temperature electronics designers are moving away from silicon. In order to address the needs of these designers microelectronics cooling devices need to move away from silicon as well.

Ideally an optimized device will eventually be built into a high temperature electronic device. The fluid handling and electrical connections will both be included in the device packaging. The package will also have to protect the device and fluid components from the external environment. The design will have to solve the problems of heat removal and leakage as well as large temperature gradients and different material coefficients of thermal expansion. This package design will pose the largest challenge for the future of the high temperature microelectronics industry. Perhaps one of these complex future packages will contain a nanotube device.

APPENDIX A

PROTOTYPE DEVICE CAD DRAWING

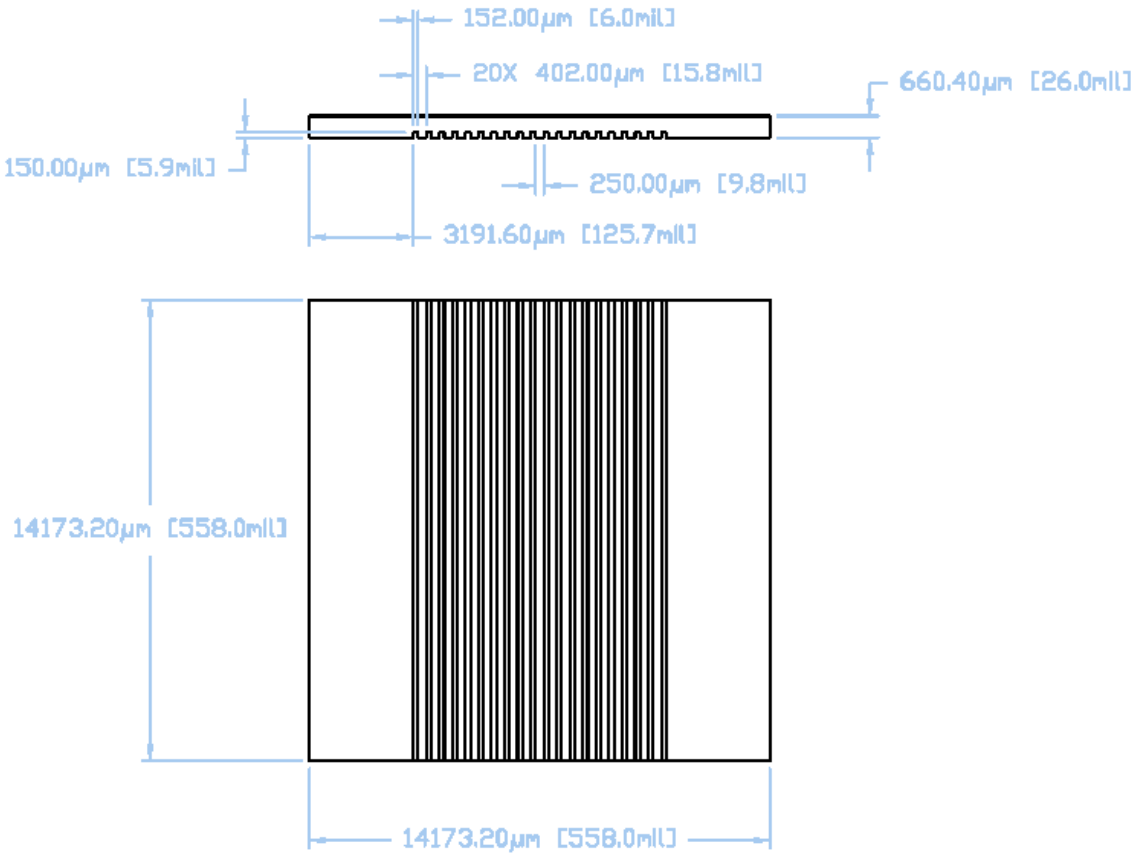

Figure A.1: Prototype CAD Drawing

APPENDIX B

LABVIEW BLOCK DIAGRAM

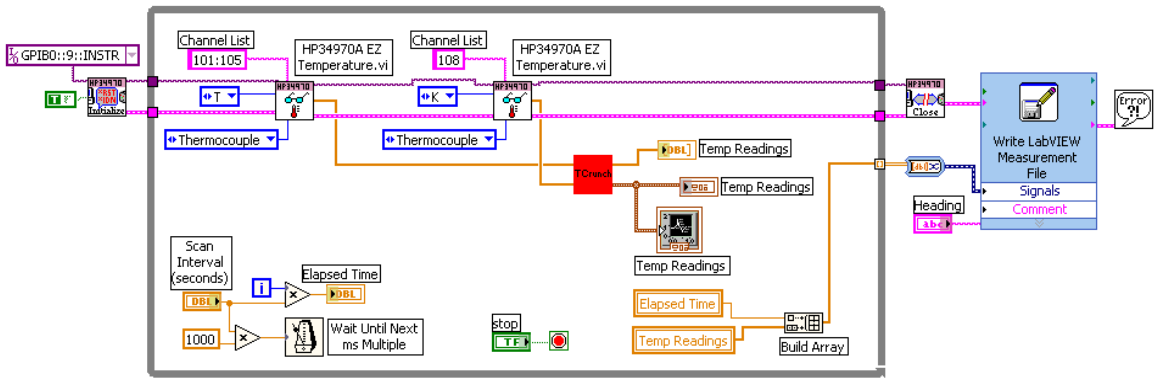

Figure B.1: Block diagram for LabVIEW data acquisition program

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