MODULAR AND SCALABLE DC-DC CONVERTERS FOR MEDIUM-/HIGH-POWER APPLICATIONS

A Dissertation
Presented to
The Academic Faculty

By

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology

August 2017

MODULAR AND SCALABLE DC-DC CONVERTERS FOR MEDIUM-/HIGH-POWER APPLICATIONS

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To my beloved wife Pengna Shen.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my advisor Professor Maryam Saeedifard for supporting me during the past five years. Her patient guidance, encouragement, and advice helped me at various stages along the journey of my doctoral studies. I would like to thank her for allowing me to pursue various research projects and providing insightful discussions and suggestions about the research.

Furthermore, I would like to thank Professors Thomas Habetler, Ronald Harley, Sakis Meliopoulos, and Amirnaser Yazdani for serving in my examination committee and for their insightful comments and suggestions to my thesis. I also would like to thank Professor Deepak Divan for his constructive feedback to my dissertation proposal. I am extremely grateful to Professor Oleg Wasynczuk at Purdue University for his motivation and immense knowledge. His inspiration and support are especially helpful to me during the first few semesters of my graduate program.

I am fortunate to have the opportunity to work with many exceptional fellow graduate students. Special thanks goes to Dr. Jiangchao Qin, Dr. Hao Chen and Liyao Wu for many insightful discussions I have had with them and to Dr. Yi Deng and Qichen Yang for their help on the development of the laboratory prototype. I also would like to thank my friends Dr. Nan Liu, Dr. Suman Debnath, Dr. Zhaoyu Wang, Jinyuan Tian, Xiangyu Han, Chanyeop Park, Chen Jiang, Jingfan Sun, Hang Shao, Cheng Gong, and Liran Zheng for their friendship and help during the course of my doctoral studies.

Finally, I would like to thank my parents and wife for their unconditioned love and constant support.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

In recent years, advanced MVDC (medium-voltage direct-current) and HVDC (high-voltage direct-current) power collection and transmission are becoming increasingly important in power systems. As the DC grids evolve, the interconnection of DC grids will become essential in the future. A DC-DC converter that is suitable for high-voltage/power is a key enabling technology for future DC networks. The DC-DC Modular Multilevel Converter (DC MMC) which has originated from the AC-DC MMC circuit topology, is an attractive converter topology for interconnection of medium-/high-voltage DC grids.

The objective of this research is to address the technical challenges associated with the operation and control of the DC MMC. To this end, a mathematical model of the DC MMC is proposed to determine the AC and DC components of the arm current, phase current, and Sub-Module (SM) capacitor voltage ripple in steady state. This thesis presents the design considerations for the DC MMC to meet the electrical specifications while satisfying the design constraints. The accuracy of the developed model and the effectiveness of the design approach are validated based on the simulation studies in the PSCAD/EMTDC software environment.

Proper operation of the DC MMC necessitates injection of an AC circulating current to maintain its SM capacitor voltages balanced. The AC circulating current, however, needs to be minimized for efficiency improvement. This thesis proposes a closed-loop control strategy for the half-bridge SM based DC MMC to simultaneously regulate the output DC-link voltage/current, maintain the SM capacitor voltages balanced, and minimize the AC circulating current for arbitrary voltage conversion ratio and power throughput. To address the power derating issue of the DC MMC, an enhanced control strategy is developed, which in conjunction with the full-bridge SMs, increases the power transfer capability and reduces the AC circulating current. A laboratory prototype is developed to experimentally validate the proposed control strategies.

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

1.1 Background

The abundant and low-carbon renewable energy resources such as offshore wind energy offers significant environmental and economic benefits [1]. U.S. Department of Energy projects that 35% of the U.S. electricity will be delivered by wind energy by 2050 [2]. The collection and transmission of the decentralized renewable energy from remote area to urban area is a major challenge [3]. In recent years, advanced MVDC (medium-voltage direct-current) and HVDC (high-voltage direct-current) power collection and transmission are becoming increasingly important in power systems [4–6]. The MVDC/HVDC is better suited for medium/long-distance power transmission as it offers many advantages over the traditional AC architecture including [7, 8]:

- DC submarine or underground cables do not consume reactive power, allowing long distance transmission of bulk energy.
- A bipolar HVDC line requires only two insulated sets of conductors. Compared to the AC lines of comparable power capacity, HVDC lines offers reduced construction cost and power losses.
- Sending and receiving end frequencies of a HVDC system are independent.
- Power flow is fully defined and controlled.

Traditionally, HVDC grids are developed for point-to-point bulk energy transmission with a converter station at each end. As the DC grids evolve, interconnection of DC grids will become essential in the future. Possible scenarios of incorporating individual DC grids includes:

- Interconnection of two HVDC systems. Since the existing HVDC systems are developed independently, the operating voltage could be different. Incorporating a mixture of DC grids with different voltage levels requires DC-DC converter to exchange power between DC networks [9, 10].

- Interconnection of a MVDC collection system and HVDC transmission system. Traditionally, the interconnection among wind turbines is achieved based on MVAC network via sub-sea cables. As the capacity of wind farms and power rating of individual wind turbines increase, a significant higher current in collection networks and longer power transmission distance between turbines are required. High transmission power losses motivate a transition from AC architecture to MVDC collection network for offshore wind farms of large capacity [10].

- Interconnection of a established HVDC system and a regional multi-terminal MVDC network to form a large DC network [11–14].

A DC-DC converter that is suitable for high-voltage/power is a key enabling technology for future DC networks as power flow control and voltage adjustment must be achieved. Specifically, DC-DC converters for future DC networks need to meet the following requirements [10]:

- Bidirectional power flow.

- High efficiency.

- High voltage/power rating.

In the technical literature, a few DC-DC converters developed for high-voltage/power applications have been reported. Among them, a modular DC-DC converter that is developed based on the concept of the well-known DC-AC modular multilevel converter (MMC) has gain increasing popularity.

1.2 Literature Review

This section summarizes the state-of-the-art DC-DC converters, which are suitable for medium-/high-voltage applications. The converter topologies are categorized into non-isolated and isolated ones. In the isolated topologies, electrical isolation between the high-voltage and the low-voltage sides is provided by an intermediate medium-/high-frequency transformer. Moreover, the state-or-the-art single-stage DC-DC modular multilevel converter topology and its variations are surveyed. The main advantages and disadvantages of each topology are also discussed in this chapter.

1.2.1 Non-isolated DC-DC Converter Topologies

A resonant DC-DC converter capable of bidirectional power flow is proposed in [15] for MW level HVDC applications. A unidirectional version of the resonant converter is studied in [16]. The application of the resonant DC-DC converter in DC grids is studied in [17]. Fig. 1.1 shows a bidirectional SCR-based resonant DC-DC converter. This converter is comprised of two thyristor-based full bridges interconnected by a capacitor. Two LCL resonant networks are incorporated to enable soft-switching of the thyristor valves. The resonant DC-DC converter features the following properties:

- The converter allows step-up and step-down operations and bidirectional power flow enabled by the back-to-back connection of thyristors.
- All thyristors are switched at zero-current resulting low switching losses [17].
- The voltage conversion is achieve without a transformer.

Nevertheless, due to the resonant nature of this converter, the following drawbacks pose challenges for high-power applications:

- High current stress on the resonant components, thereby, increasing the power losses on the passive components.

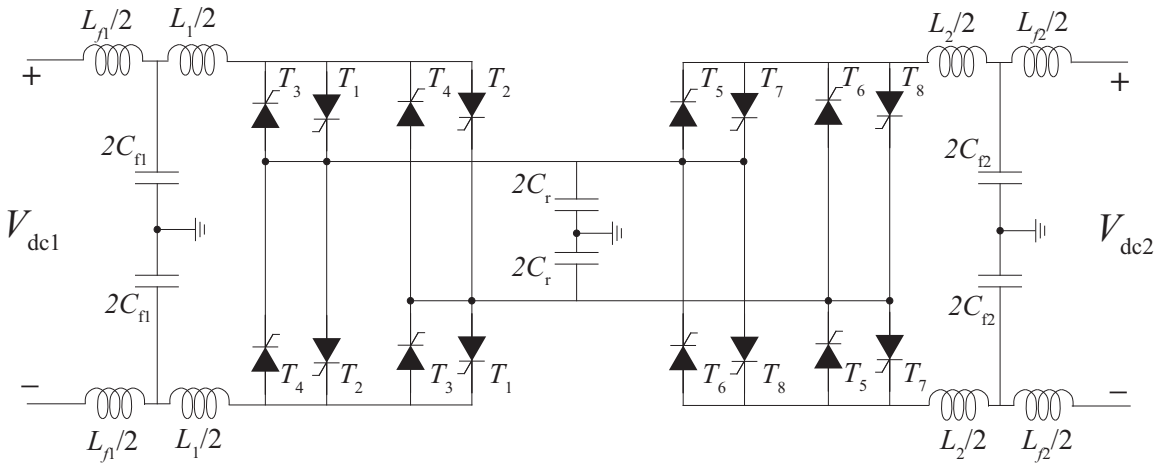


Figure 1.1: Circuit diagram of a SCR-based resonant DC-DC converter.

- High voltage and current stresses on the thyristors.
- Power control is achieve by switching frequency variation, which poses challenges on the design of passive components.

A step-up unidirectional resonant converter utilizing IGBT switches and modules consisting of inductor, capacitor, and diode is proposed in [18]. The switched capacitor soft-switching resonant DC-DC converter is shown in Fig. 1.2. The converter achieves high step-up ratio by connecting a number of cascaded capacitor clamped modules. The converter features soft-switching in all active switches and diodes, thus offering high efficiency. However, the resonant capacitors experience different voltage stress under steady-state operation. Consequently, the converter does not offer full modularity. Moreover, due to its poor output voltage regulation, a second stage DC-DC converter is required to regulate the output voltage. The aforementioned drawbacks limit the application of the IGBT-based switched capacitor soft-switching resonant DC-DC converter in high-voltage/power applications.

A class of multilevel DC-DC converters that are derived from the conventional low-voltage and low-power converters (buck, boost, or buck-boost) is proposed in [19–22] for HVDC applications. Circuit diagram of the bidirectional buck-derived DC-DC con-

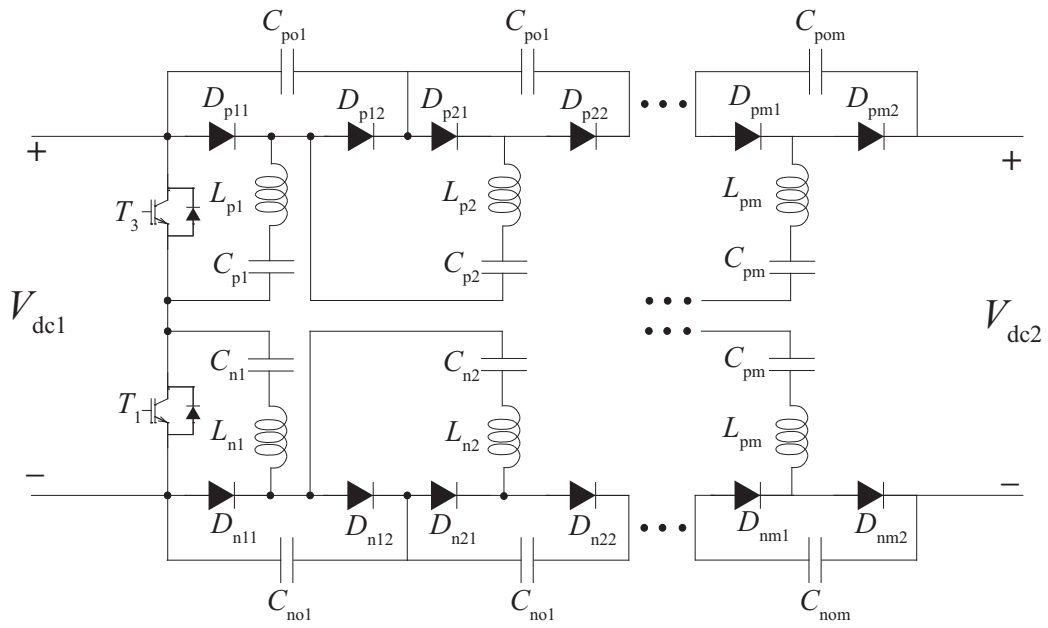


Figure 1.2: Circuit diagram of the switched capacitor soft-switching resonant DC-DC converter.

verter is shown in Fig. 1.3. This converter is derived from the conventional synchronous buck converter by replacing the semiconductor switches by a number of series-connected capacitor-clamped switches. This class of converters avoids direct series connection of semiconductor switches, therefore any complex balancing circuit is eliminated [19]. The main advantage of the buck-derived converter is the low voltage stress on semiconductor switches and low electro-magnetic interference (EMI). Nevertheless, a major drawback is inherently shared by the conventional converter derived topologies. The input/output inductor carries full DC current. The high current stress on the inductor poses challenges on magnetic design and results in bulky magnetic cores and additional power losses.

A resonant step-up DC-DC converter that is derived based on the Marx generator principle is proposed in [23, 24]. Fig. 1.4 shows the Marx derived DC-DC converter with N capacitor stages. The converter charges the capacitors in parallel and discharges them in series [23]. The main advantage of this converter is that a high step-up ratio can be achieve by cascading multiple capacitor stages without using a transformer. However, the current stress on the input inductor, diode, and switch is high. Moreover, this converter have some

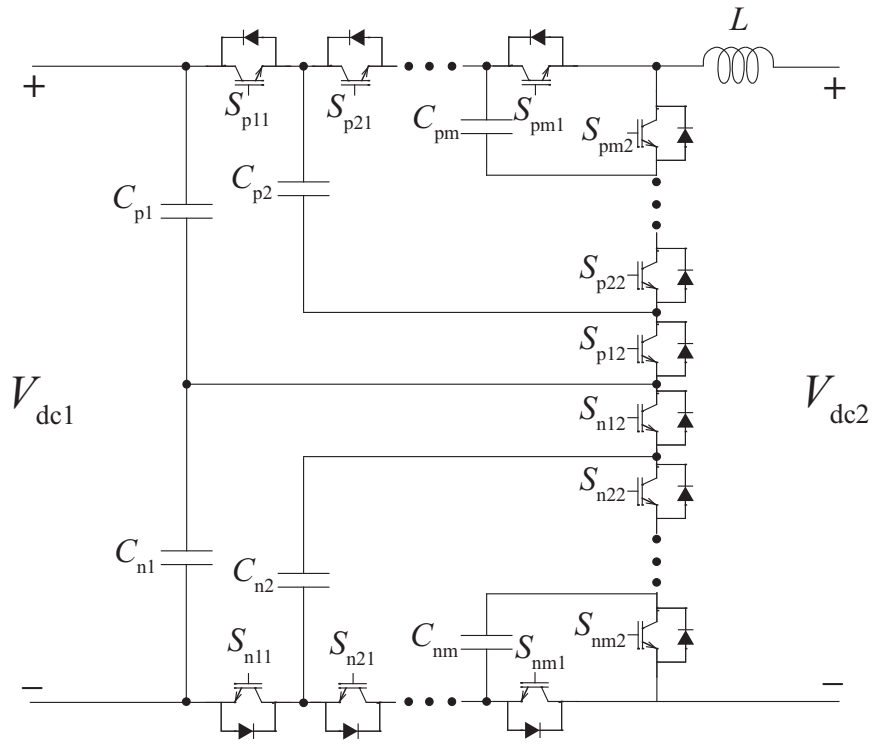


Figure 1.3: Circuit diagram of the bidirectional buck-derived multilevel DC-DC converter.

common drawbacks as a switched capacitor topology:

- The converter offers poor output voltage regulation, thus a secondary stage is required to regulate the DC voltage.
- The voltage stress of the capacitor is at least the full input voltage.
- The converter is not fully modular.

1.2.2 Isolated DC-DC Converter Topologies

Isolated DC-DC converters are widely used in DC-DC power conversion applications where the galvanic isolation is provided by an AC transformer. The dual-active-bridge (DAB) DC-DC converter that was originally proposed in [25] is a potential converter topology for medium-/high-power applications. The DAB converter includes two active-bridges that are

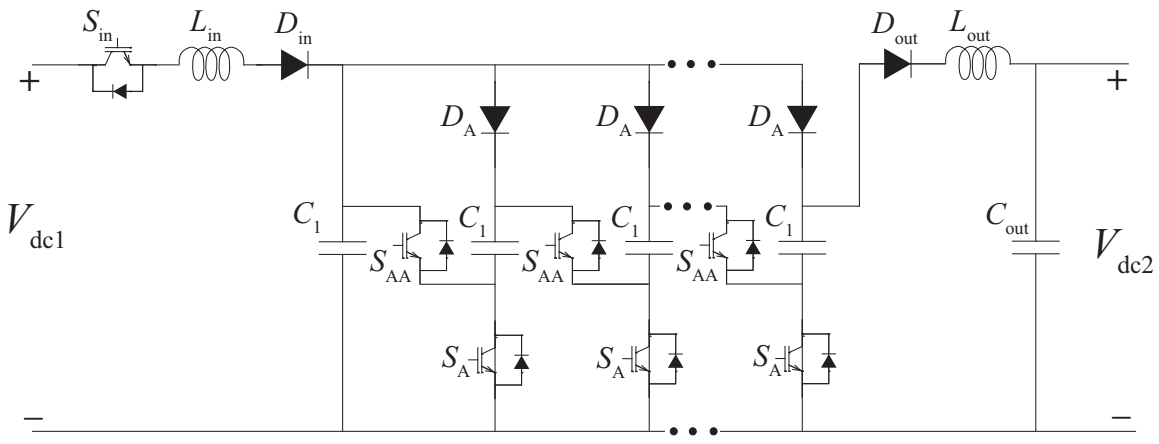


Figure 1.4: Circuit diagram of the unidirectional resonant step-up Marx DC-DC converter.

interconnected by a medium-frequency AC transformer. Depending on the design criteria, the DAB converter can be configured using single-phase bridge [25–29] or three-phase bridge [25, 30–33]. A three-phase bridge DAB converter is shown in Fig. 1.5 where a three-phase AC transformer is used to interconnect the primary and secondary active bridges. The leakage inductance of the intermediate transformer is utilized as the energy transferring element and the maximum power flow is limited by the leakage inductance [25]. The DAB converter is capable of bidirectional power flow, which is achieved by controlling the phase shift angle between the two active bridges and the output voltage magnitude of each individual active bridge [34]. The switches in the active bridges can be switched at zero voltage and/or zero current for a certain operating range. Various control strategies are proposed to extend the soft-switching range and minimize the transformer current of the DAB converter [35–40]. Moreover, a high-voltage conversion ratio for step-up or step-down operation can be achieved by selecting the turns ratio of the transformer.

Nevertheless, the DAB converter have some disadvantages that limit its use in high-voltage/power applications:

- The active bridges need to be rated at the full converter power and voltage. Consequently, for high-voltage/power applications, series and/or parallel connection of semiconductor switches are required to satisfy the voltage and current requirements.

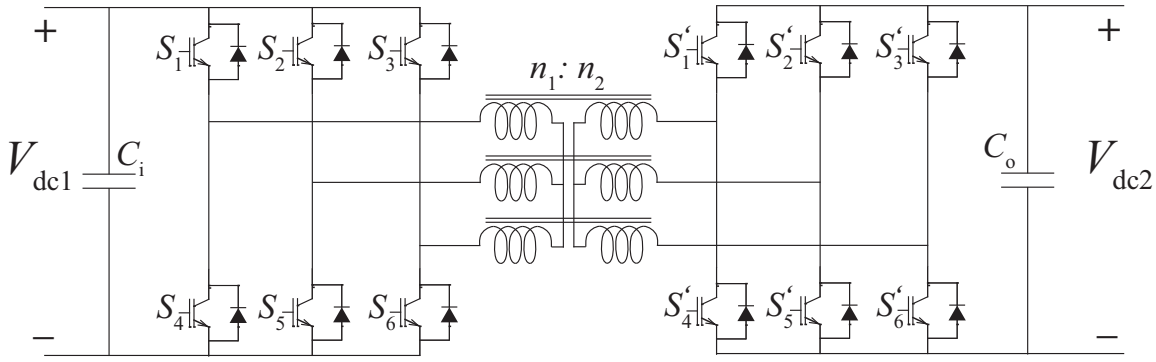


Figure 1.5: Circuit diagram of a bidirectional three-phase DAB converter.

- For high voltage applications, high insulation requirement for the intermediate transformer may introduce additional parasitic components that further increase the switch rating requirement and switching losses [18].

To apply the DAB converter in high-power applications, the idea of connecting multiple DAB converter units in series and/or parallel to increase the voltage and current ratings without using series-connected semiconductor switches has been proposed [41–43]. A input-series-output-parallel (ISOP) DAB converter is shown in Fig. 1.6 in which identical DAB modules are connected in series and parallel. The modular design allows easier scalability for the system [44]. Moreover, improved system reliability can be achieved by inserting redundant modules [43]. However, the main drawback of the series/parallel connection of DAB converters is that a high number of low-power transformers need to be isolated from the high-voltage DC side. This high insulation requirement consequently leads to high cost and volume.

In 2002, Lesnicar and Marquardt proposed the concept of DC-AC modular multilevel converter (MMC) [45] in which a number of identical half-bridge submodules (SM) are switched to generate a multilevel AC voltage waveform. The concept of using multiple low-voltage SMs to replace the switches in the conventional DAB converter has gain increasingly popularity [34, 46–48]. An MMC-based DAB converter is shown in Fig. 1.7. In contrast to the ISOP DAB converter, the DAB converter based on the MMC concept does

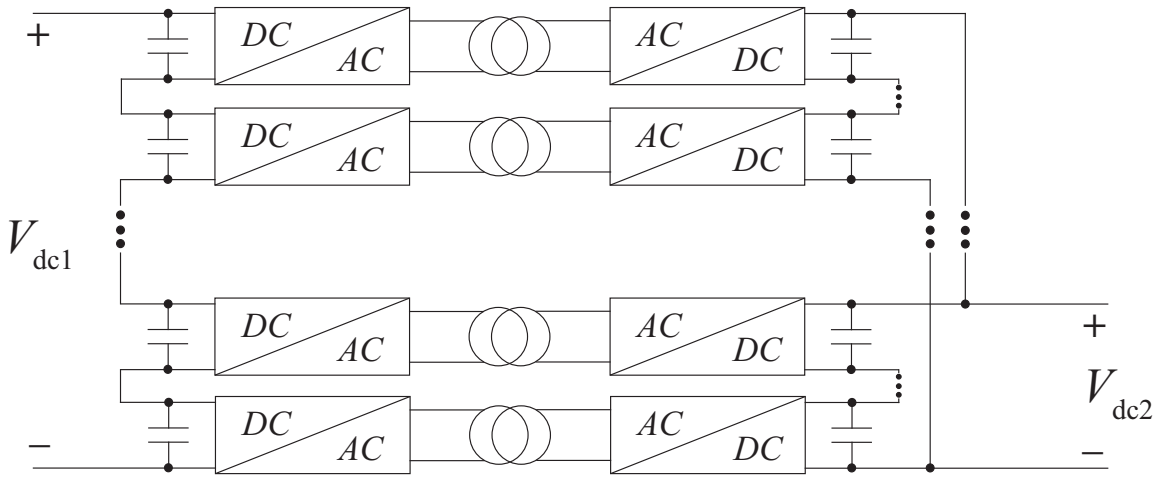


Figure 1.6: Circuit diagram of an input-series output-parallel DAB converter.

not require multiple low-power transformers. Instead, a multilevel or a two-level voltage waveform is generated across the transformer winding. The MMC-based DAB converter topology offers inherent DC fault blocking capability and easy adoption of power rating. The series connection of semiconductor switches is avoided. However, the use of two fully rated DC-AC stages results in poor utilization of total installed SM ratings, thereby increasing the cost, volume and power losses [49].

1.2.3 DC-DC Modular Multilevel Converter Topologies

The DC-AC MMC has become the most attractive converter topology for high-voltage and high-power applications since its introduction in 2002. An extensive research effort has been made to address the technical challenges associated with its operation and control [50–57]. The salient features of the DC-AC MMC make it suitable for various applications including High-voltage DC (HVDC) transmission systems [58–62], variable speed drives [63–69], flexible AC transmission systems (FACT) [70, 71], and static synchronous compensator (STATCOM) [72–75]. The salient features of the MMC are:

- Fully modular and scalable enabled by the use of identical low-voltage SMs. High-voltage rating can be easily achieved by series connection of a large number of SMs.

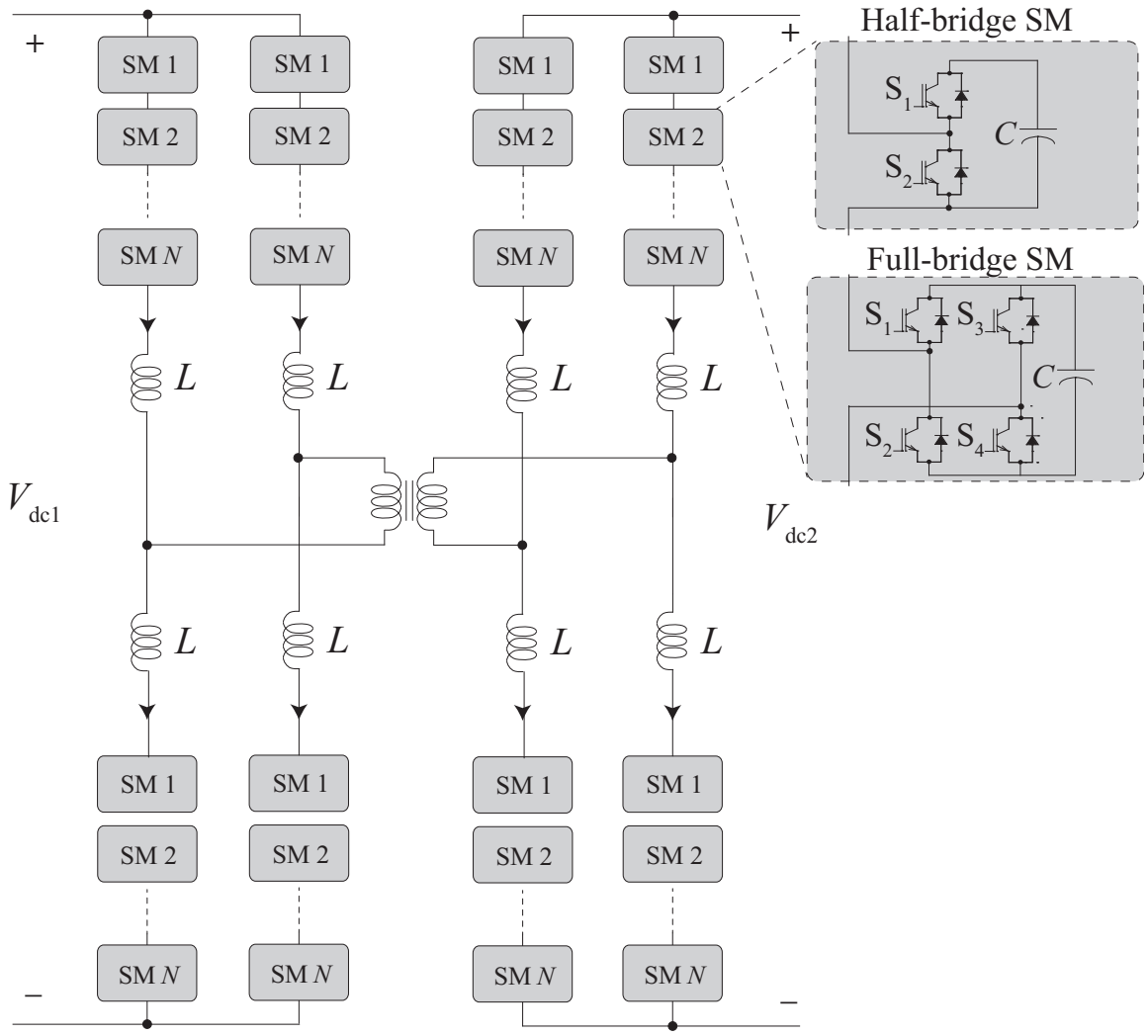


Figure 1.7: Circuit diagram of the MMC-based DAB converter.

- Low total harmonic distortion (THD) in the output AC waveforms enabled by the multilevel architecture. The low THD significantly reduces the requirement for AC side filtering.

- Low EMI due to the low dv/dt and di/dt.

- Improved reliability enabled by introducing/enabling redundant SMs.

In 2013, the concept of single-stage DC-DC modular multilevel converter (DC MMC) that is inspired by the DC-AC MMC was proposed in [76, 80]. The single-stage DC MMC inherits the salient features of the DC-AC MMC and is a potential converter topology for medium-/high-power DC-DC conversion systems, e.g., interconnection of DC grids.

Fig. 1.8 depicts the generic circuit topology of the DC MMC. The DC MMC is constructed based on a series connection of a number of identical half-bridge SMs. In contrast to the AC-DC MMC, the DC MMC relies on an AC circulating current to exchange active AC power between the upper and lower arms of each phase-leg to maintain energy balance of the SM capacitors. Therefore, the DC MMC need to have at least a DC loop and an AC loop. In the generic topology shown in Fig. 1.8, a band-stop filter is installed at the output DC terminal to prevent the AC circulating current from flowing to the DC terminal. A band-pass filter is also installed to establish a low impedance path for the AC circulating current [76]. Under steady-state operation, each arm generates an AC and a DC voltage component. The DC voltage component dictates the DC-link voltage while the AC voltage component drives an AC circulating current to exchange energy between the upper and lower arms.

In contrast to the MMC-based isolated DC-DC converter, the DC MMC offers the following advantages:

- The intermediate AC transformer is eliminated, thereby, lead to a significant reduction in the requirement on magnetic design.

- Step-up and step-down modes of operation are enabled by using full-bridge SMs.

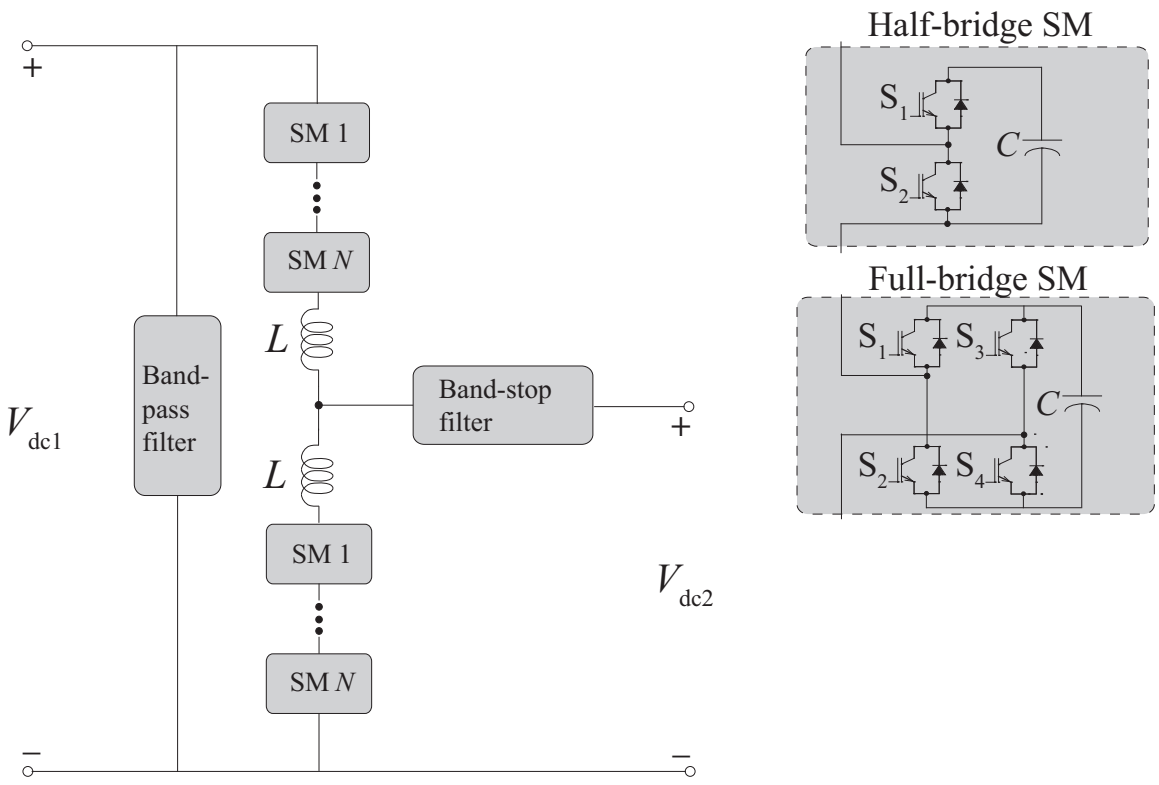


Figure 1.8: Circuit diagram of the tuned filter DC MMC.

- The multi-frequency power conversion process enabled by the AC circulating eliminates the use of two cascade fully rated DC-AC MMCs. The utilization ratio of the total installed SMs is increased significantly and up to 50% of reduction in cost and power losses is achieved [49].

Based on the DC MMC concept proposed in [76], various DC MMC circuit topologies have been proposed in the literature. A polyphase DC MMC is shown in Fig. 1.9 where multiple phase legs are employed to increase power rating of the converter [80]. The phase legs of the DC MMC operate in a interleaving manner such that each of the phase-leg only carries a portion of the total DC power. The interleaving operation also improves the DC voltage and current ripple as the AC current components are canceled at the DC terminal. The polyphase DC MMC employs inductive band-stop filters shown in Fig. 1.9. The multiphase structure allows the AC circulating current to flow among the phase legs, thereby, eliminating the need for a band-pass filter.

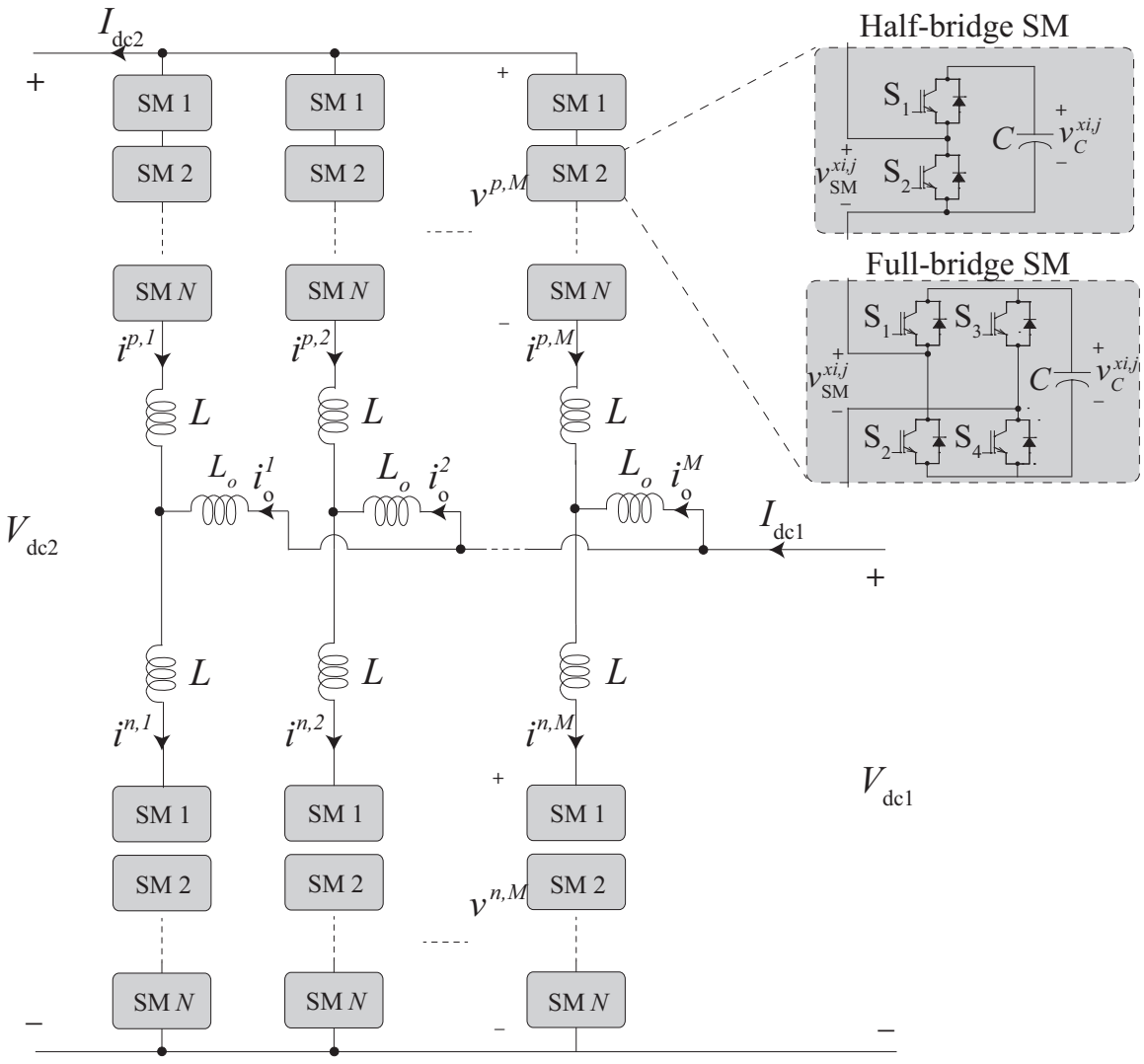


Figure 1.9: Circuit diagram of the polyphase unipolar DC MMC.

A two-phase-leg bipolar DC MMC that is constructed by symmetric connection of two unipolar DC MMC is depicted in Fig. 1.10 [49]. In the bipolar DC MMC, the midpoint of two unipolar DC MMC are connected together through reactive elements, establishing a path for the AC circulating current to flow within the converter. The two-phase structure allows the use of coupled inductors at the DC link 2 terminal. In the coupled inductor core, the flux produced by the DC component is canceled, which results in significantly reduced cost and complexity in the magnetic design. The bipolar DC MMC is able to step-down the voltage from DC-link 1 to DC-link 2 if only half-bridge SMs are installed. The step-up operation is enabled by installing full-bridge SMs in the outer arms allowing negative voltage insertion. Moreover, the DC fault blocking capability can also be realized by the full-bridge SMs [49]. It should be noted that the number of SMs in the outer (k) and inner (r) arms is a design and optimization variable and does not necessarily need to be equal.

Several DC MMC topologies that utilize alternative filtering options have been proposed to reduce the volume and cost due to the magnetics of the inductive filter. A DC MMC that utilizes a cross-connected capacitor between the upper and lower arms is depicted in Fig. 1.11 [81], in which an AC current path is enabled by the arm inductor along with the cross-connected capacitor. In this topology, the output inductor is eliminated. However, a high voltage stress of at least one half of the high-voltage side is seen by the capacitor [81]. In [82], the cross-connected capacitor is replaced by series-connected SMs that generate a DC and an AC voltage component. The active cross-connected branch overcomes the voltage stress problem in the topology proposed in [81]. Nevertheless, the active cross-connected branch requires additional semiconductor devices as well as capacitors, which increase the cost, volume, and operational losses of the converter. A DC MMC that utilizes active filter as the band-stop filter is shown in Fig. 1.8 [83]. The use of the active filter eliminates the passive inductive or capacitive filter in the DC MMC. However, the active filter requires series connection of a number of full-bridge SMs. Therefore, the total semiconductor device count is increased significantly, resulting in increased cost and power

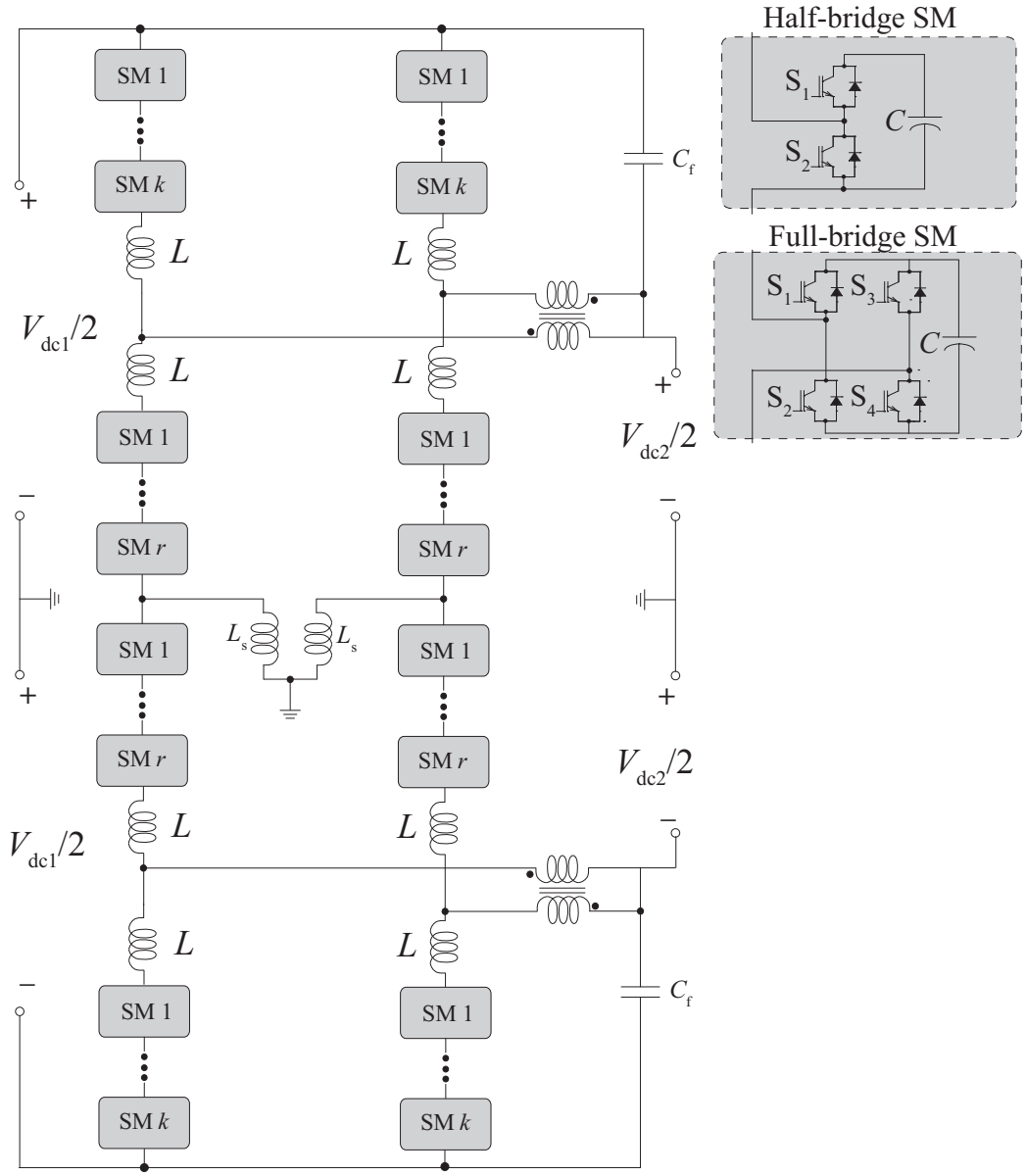


Figure 1.10: Circuit diagram of the bipolar DC MMC.

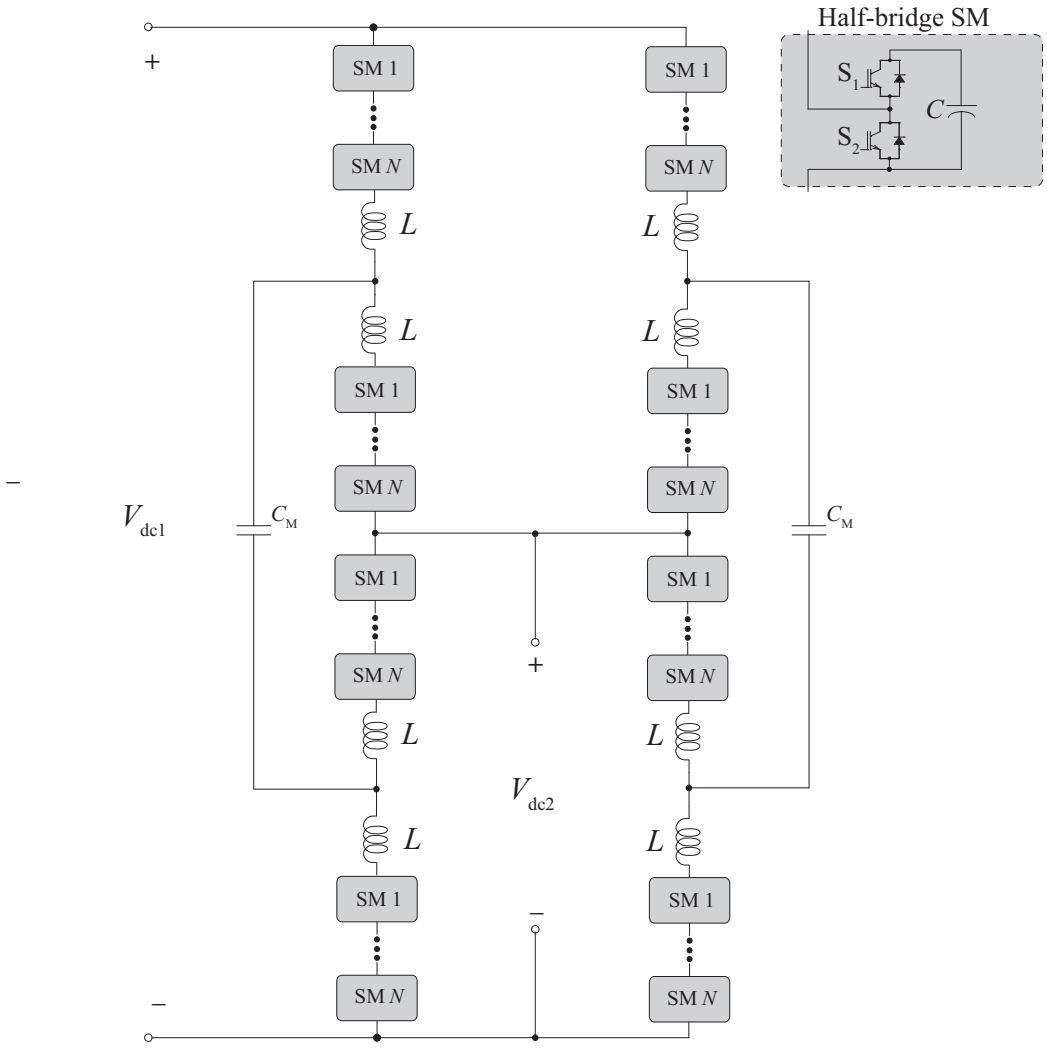


Figure 1.11: Circuit diagram of the DC MMC with capacitive filter.

losses.

The operation and dynamic model of the DC MMC are studied in [84–86]. Several control strategies are proposed in the literature. An AC circulating current control strategy to maintain the power balance between the upper and lower arms of each phase-leg of the DC MMC has been proposed in [49]. This control strategy preserves the amplitude of the AC voltage component of the upper arm and actively controls the AC voltage component of the lower arm such that the power balance between the upper and lower arms is maintained and the phase angle of the circulating current remains in phase with the upper arm AC voltage. The open-loop control strategy proposed in [49] guarantees power balance of the upper and lower arms. Nevertheless, it does not minimize the AC circulating current since the minimum AC circulating current is not necessarily always in phase with the upper arm AC voltage. Reference [87] proposes an improved open-loop control strategy in which the AC circulating current can be regulated at different phase angles for either the upper or the lower arm, by assigning arbitrary splitting of VAR generation between upper and lower arms. The control strategy proposed in reference [87] can achieve minimized AC circulating current by splitting VAR generation between the upper and lower arms. However, this control strategy requires tunning of weighting parameters for different voltage conversion ratios and power throughputs to achieve a minimized AC circulating current.

1.3 Problem Statement

Recently, research effort has been made to address the technical challenges associated with the operation and control of the DC MMC [49, 76, 80, 84–87]. Nevertheless, there are still barriers for the implementation of the DC MMC. One of the major challenges of the DC MMC is the design of the converter. The DC MMC exploits an AC circulating current to exchange active AC power between the upper and lower arms of each phase-leg to maintain its SM capacitor voltages balanced. Since both frequency and amplitude of the AC circulating current in the DC MMC can be chosen arbitrarily, their values affect the con-

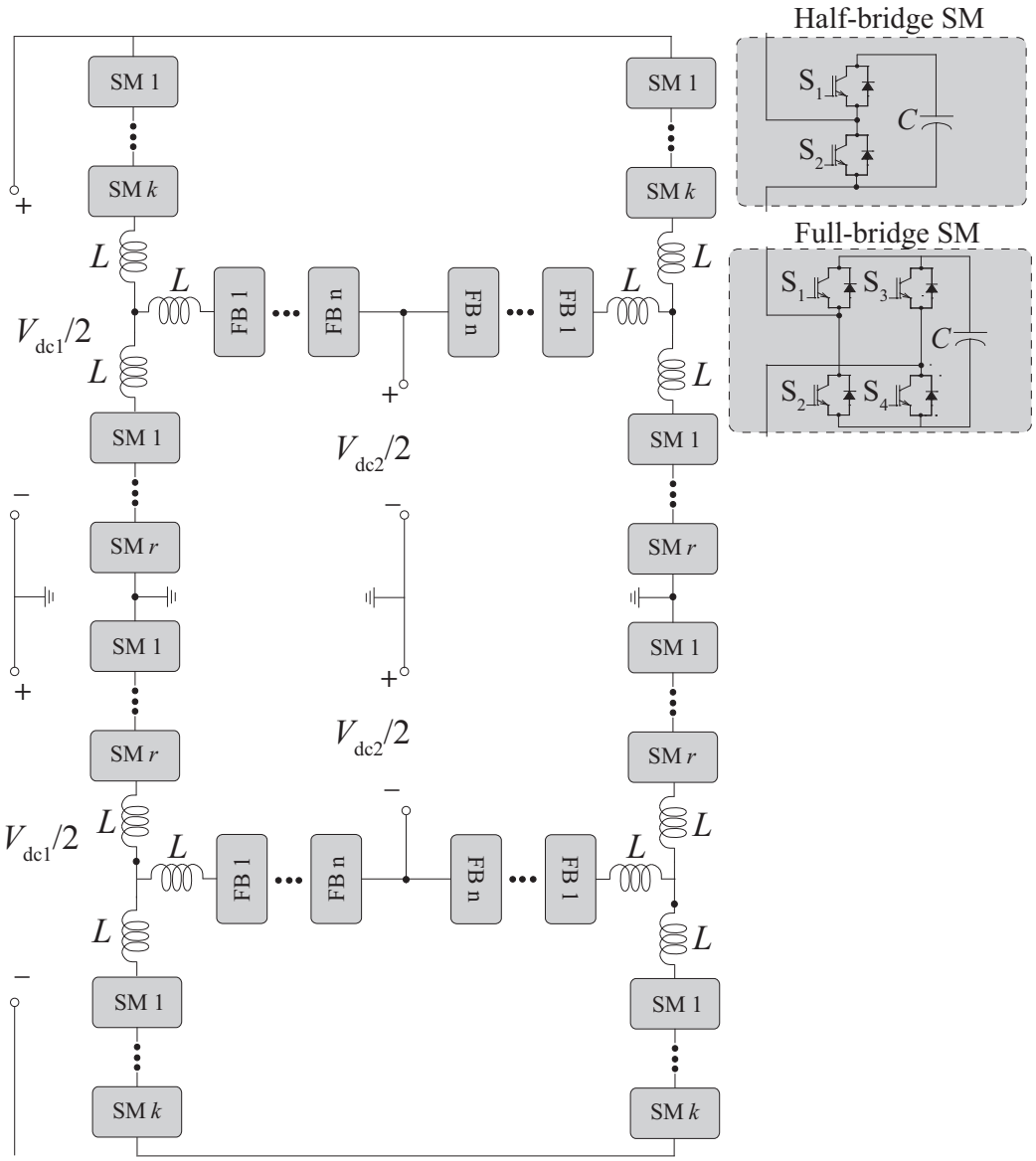


Figure 1.12: Circuit diagram of the DC MMC with active filters.

verter efficiency and the size of passive components. Furthermore, the DC MMC topology inherently requires a large phase filtering inductor to remove the AC component presented in the phase current [49]. However, an over-sized inductor will add to the system cost and size/volume. A design procedure to size the passive components and to select the operating frequency is a critical step to optimize the converter performance. Since the basics of operation of the DC MMC are significantly different from the DC-AC MMC, the developed passive component sizing methods for the DC-AC MMC in [88–90] are not applicable to the DC MMC.

In addition, the arm active AC power needs to be actively regulated to follow the arm DC power component. The conventional SM capacitor sorting and selection algorithm combined with an open-loop controller [91, 92] employed for AC-DC MMC can only guarantee the SM capacitor voltage balancing within each arm. To maintain the power balance of the SM capacitors of the upper and lower arms within each phase-leg of the DC MMC, a closed-loop control strategy is required. Moreover, the converter power losses and the rating value of the power devices are directly associated with the amplitude of the arm current. The arm current contains a DC component and an AC component which is injected to maintain the SM capacitor energy balance. Therefore, the AC circulating current must be minimized. In summary, the closed-loop control strategy should regulate the DC-link voltage/current, maintain the SM capacitor energy balance, and minimize the AC circulating current. Moreover, the DC MMC experiences power derating issue as the voltage conversion ratio deviates from 0.5. The derating problem is caused by the reduced headrooms of the AC voltage components of the upper and lower arms and is worsen when the voltage conversion ratio is close to unity or zero. Therefore, to preserve the power transfer capability over a wide range of voltage conversion ratio for the DC MMC, there is a need for an advanced control strategy.

1.4 Thesis Scope

This thesis is focused on the control and design of the DC MMC. The DC MMC depends on the multi-frequency power transfer mechanism to maintain its SM capacitor energy balance. A mathematical model in the phasor domain is developed to describe the steady-state operation of the DC MMC. Based on the mathematical model, this thesis presents the design considerations for the DC MMC to achieve high efficiency while satisfying the design constraints. Design equations to determine the size of passive components are developed. Subsequently, a systematic approach is developed such that based on certain given design constraints, the size of passive components as well as the operating frequency of the converter can be determined. Accuracy of the developed model and the design approach is validated based on simulation studies in the PSCAD/EMTDC software environment.

This thesis also proposes a closed-loop control strategy for the half-bridge SM based DC MMC to simultaneously regulate the output DC-link voltage/current, maintain the SM capacitor voltages balanced, and minimize the AC circulating current for arbitrary voltage conversion ratio and power throughput. The control strategy consists of an outer loop DC-link current controller to regulate the low-voltage-side DC-link current combined with an inner-loop power balance controller to maintain the power balance of the upper and lower arms. Both current and voltage regulation strategies are presented. A current regulation strategy offers quick and smooth changes in power transfer between the interconnected DC grids while the voltage regulation strategy offers quick dynamic control over the DC voltage. The proposed control strategy guarantees proper bidirectional operation of the DC MMC. Moreover, an enhanced control strategy is developed, which in conjunction with the full-bridge SMs, increases the power transfer capability and reduces the AC circulating current. Performance and effectiveness of the proposed control strategies are evaluated based on simulation studies in the Matlab Simulink software environment.

A 3.5-kW laboratory prototype is developed and built to experimentally validate the

proposed control strategy. The design considerations of the prototype is presented in the thesis.

1.5 Outline of the Thesis

Chapter 2 presents the architecture and operation of the DC MMC circuit topology. Operation of the DC MMC with the half-bridge and full-bridge SMs are discussed. The derivation of the steady-state model in the phasor domain is presented. Moreover, the dynamics of the SM capacitor voltage is analyzed. Simulation results are provided to validate the proposed model.

Chapter 3 proposes a closed-loop control strategy for the half-bridge SM based DC MMC configuration. Two types of SM capacitor energy imbalance in a DC MMC are analyzed. An AC circulating current needs to be injected and regulated to mitigate the Type II imbalance. The power balance mechanism for a half-bridge SM-based MMC is discussed and a closed-loop control strategy is presented. Simulation results are provided to demonstrate the performance of the proposed controls strategy.

Chapter 4 presents a closed-loop control strategy for the full-bridge SM based DC MMC configuration. The DC MMC relies on an AC voltage component in each arm to drive an AC circulating current. The power transfer capability and amplitude of the AC circulating current of the DC MMC is closely coupled with the available AC voltage headroom. Full-bridge SM are utilized to extend power transfer capability and reduce the AC circulating current. A closed-loop control strategy is proposed for the full-bridge based DC MMC. Simulation results are presented to validate the proposed control strategy.

Chapter 5 explores a constraint-oriented design approach for the DC MMC. The operating frequency has a significant impact on the size of the passive component and power losses of the converter. Design constraints are identified and design equations are presented for the arm inductor, inductive filter, and SM capacitor. Subsequently, a systematic design approach are presented to select the operating frequency and the size of the passive

components. Simulation results are provided to validate the design approach.

Chapter 6 presents the development of a DC MMC laboratory prototype. The DC MMC is designed based on the systematic design approach presented in Chapter 5. A constant-voltage DC load and a DC power supply are connected to the DC links of the DC MMC to mimic two interconnected DC grids. The experimental results are presented to demonstrate the proposed mathematical model and control strategies.

Chapter 7 summarizes the contributions of the this thesis and outlines the future work in the related areas.

CHAPTER 2

OPERATION PRINCIPLE OF THE DC MMC

The single-stage DC MMC that is derived from the AC-DC MMC circuit topology inherits the salient features of the DC-AC MMC. The chief advantage of the single stage DC MMC over the traditional two-stage DC-AC-DC MMC based converter is reduced converter cost and losses. In addition, a significant reduction in magnetic rating is realized in DC MMC relative to the two-stage topology.

The circuit topology and operation of the DC MMC differ from the DC-AC MMC in the following ways [93]:

- Each arm of the DC-AC MMC containing N SMs is divided into two arms: a upper arm and a lower arm.
- An additional filter network (passive or active) is added to prevent the AC current from entering the DC link.
- An AC circulating current is injected and controlled to enable energy transfer between the upper and lower arms.

In this chapter, the principle of operation of the DC MMC is presented. A phasor-domain model is developed to describe the steady-state operation of the DC MMC. The dynamics of the SM capacitor voltage is also presented.

2.1 The DC-DC Modular Multilevel Converter

The circuit diagram of an M-phase-leg DC MMC is shown in Fig. 2.1, in which the DC-link 2 voltage, V_{dc2}, is larger than the DC-link 1 voltage, V_{dc1}.

The DC MMC consists of two arms per phase-leg, i.e., an upper arm (represented by superscript "p") and a lower arm (represented by superscript "n"). Each arm consists of

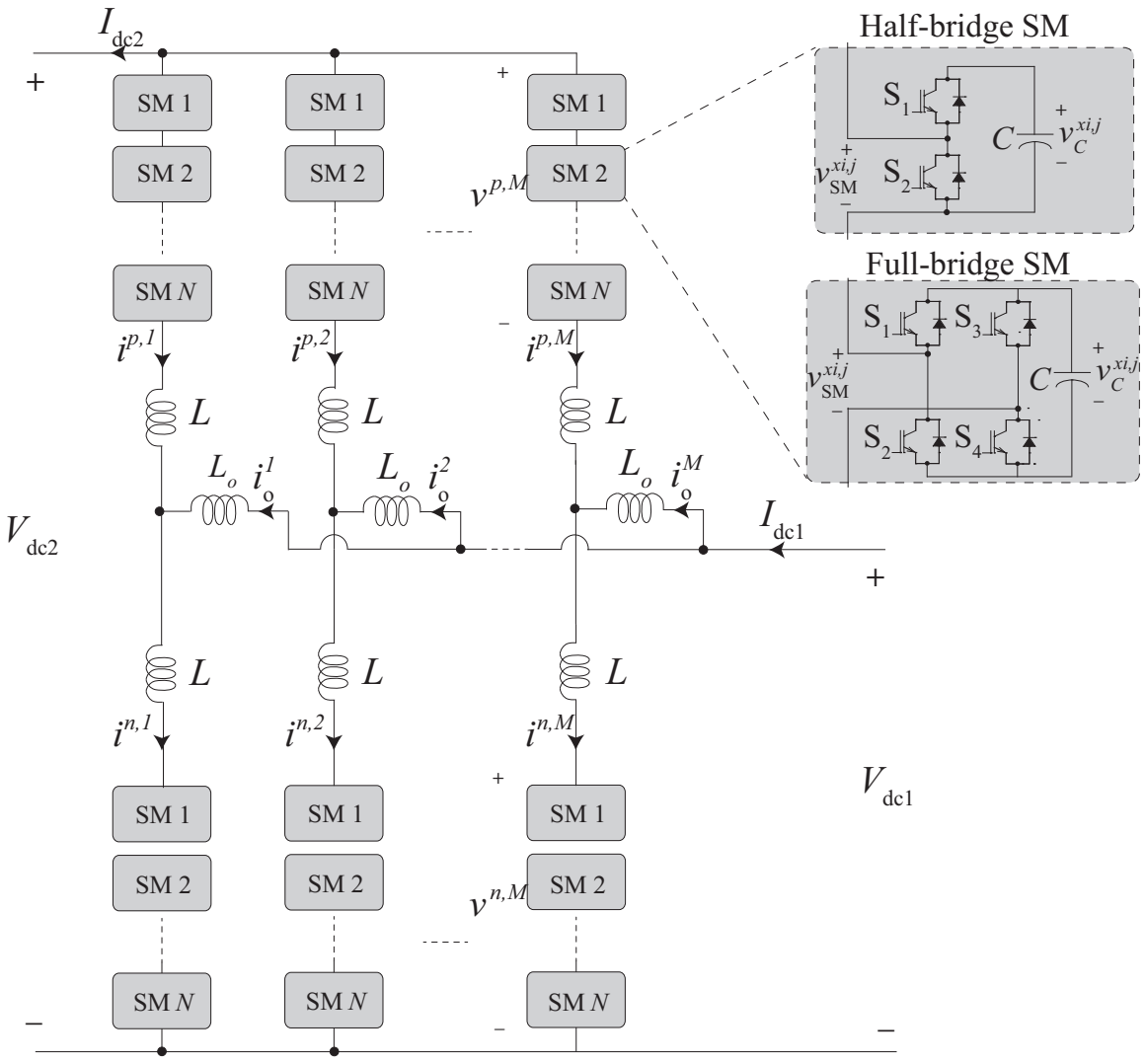


Figure 2.1: Circuit diagram of an *M*-phase-leg DC MMC.

series connection of N SMs and an arm inductor L. The output terminal/mid-point of each phase-leg is connected to the converter DC-link 1 terminal via the phase filtering inductor L_{o}.

Each arm of the DC MMC may consist of the half-bridge, the full-bridge, or a combination of half-bridge and full-bridge SMs depending on the design and optimization criteria of the converter. The half-bridge SM offers a lower semiconductor device count whereas the full-bridge SM enables fault-blocking capability, step-up operation, and reduced AC circulating current, which will be discussed in detail in Chapter 5.

The half-bridge SM in Fig. 2.1 can provide two voltage levels across its output terminal, i.e., zero or $v_{\mathrm{C}}^{xi,j}$, $x \in \{p,n\}$; $i \in \{1,2,...,N\}$; $j \in \{1,2,...,M\}$, depending on the switching states of its complementary switches S_1 and S_2. The two switching states of a half-bridge SM are:

- $S_1 = 1$ and $S_2 = 0$: ON-state or inserted,
- $S_1 = 0$ and $S_2 = 1$: OFF-state or bypassed.

The full-bridge SM in Fig. 2.1 can provide three voltage levels across its output terminal, i.e., zero, $v_{\mathrm{C}}^{xi,j}$, or $-v_{\mathrm{C}}^{xi,j}$, $x \in \{p,n\}$; $i \in \{1,2,...,N\}$; $j \in \{1,2,...,M\}$, depending on the switching states of its two complementary switch pairs (S_1, S_2) and (S_3, S_4). The three switching states of a full-bridge SM are:

- $S_1 = S_4 = 1$ and $S_2 = S_3 = 0$: POSITIVE-state,
- $S_1 = S_4 = 0$ and $S_2 = S_3 = 1$: NEGATIVE-state,
- $S_1(S_2) = S_3(S_4) = 1$ and $S_2(S_1) = S_4(S_3) = 0$: OFF-state or bypassed.

The DC MMC exploits an AC circulating current component to enable energy transfer between the upper and lower arms. To prevent leakage of the AC circulating current to the DC terminal and to facilitate effective active AC power transfer between the upper and

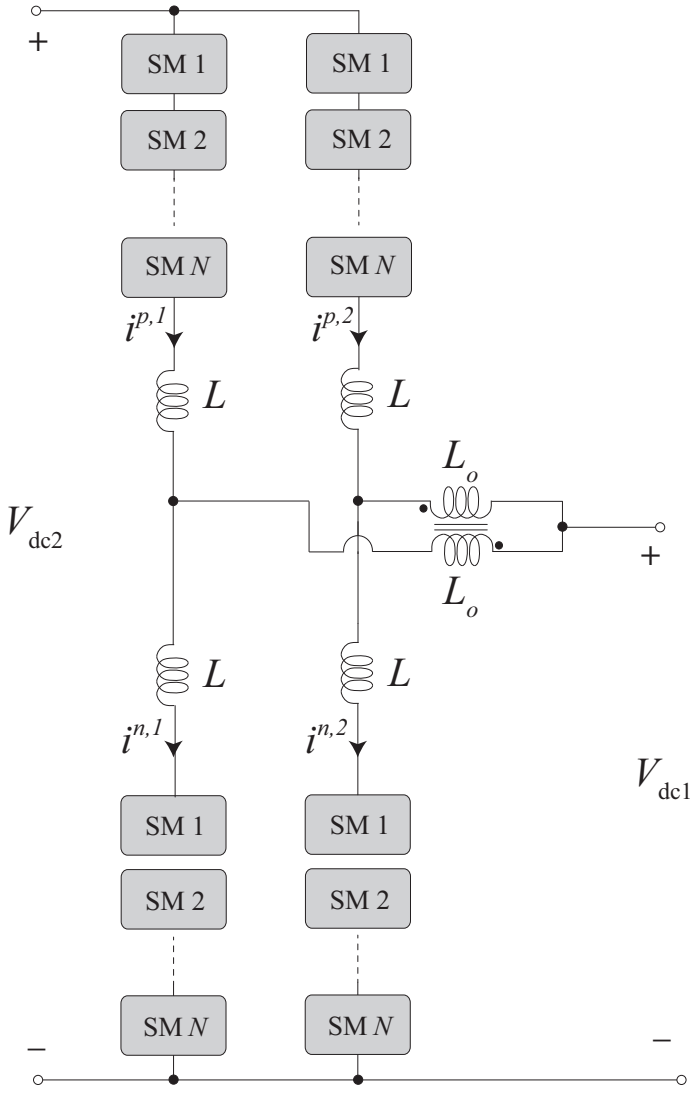


Figure 2.2: Circuit diagram of a 2-phase-leg DC MMC.

lower arms, L_o should be sufficiently large such that the ripple component of the phase currents becomes negligible.

The schematic of a two-phase-leg DC MMC is shown in Fig. 2.2. The two-phase-leg configuration enables the use of a differential mode chock as the output filter where a large magnetizing inductance is seen by the AC current component. The flux produced by the DC current component is canceled in the magnetic core, thereby minimizing the core volume (no energy storage is required) [93]. For three or more phase legs, a zig-zag transformer can be utilized as the output filter.

The number of phase legs of the DC MMC is chosen based on the power rating requirement. For high-power applications, multiple phase legs might be required to increase the power rating of the converter. For the case of $M = 1$, a series LC filter is inserted to establish a path for the AC circulating current [94]. For the case of $M > 1$, the phase legs operate in an interleaved manner, i.e., the gating signals among phase legs are identical with a phase shift of $\frac{2\pi}{M}$.

2.2 Principle of Operation

The DC MMC consists of multiple capacitor clamped SMs whose average voltages are maintained at the nominal value during normal operation. By controlling the switching states of the SMs (insert or bypass the SM capacitors), each arm of the DC MMC synthesizes a multilevel voltage waveform, which comprises of an AC and a DC component. The DC voltage component dictates the DC link voltages and drives a DC current to bidirectionally transfer power between the DC links 1 and 2. The AC voltage component drives an AC circulating current to exchange active AC power between the upper and lower arms. The frequency of the arm AC voltages, ω, which hereafter is referred as the operating frequency, is a design/control parameter of the converter and can be chosen arbitrarily.

2.2.1 Principle of Orthogonal Power Flow

The DC MMC relies on the principle of orthogonal power flow to transfer energy and maintain power balance of its SM capacitors. The principle of orthogonal power flow is conceptualized in Fig. 2.3, where the sender and receiver are comprised of n voltage sources in various frequencies, respectively. A series RL impedance is placed in between the sender and receiver. The power of the sending side is analyzed to illustrate the power flow of a multi-frequency power transmission system. The total voltage of the sender is

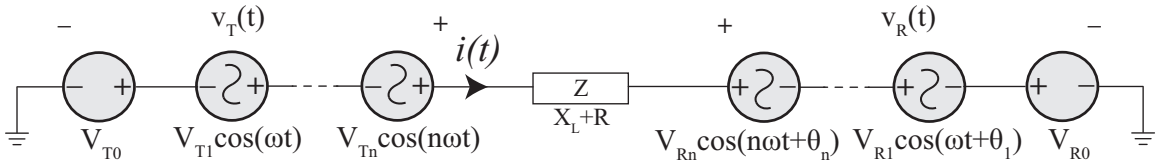


Figure 2.3: A multi-frequency power transmission system.

expressed by:

$$v_T(t) = V_{T0} + V_{T1}cos(\omega t) + V_{T2}cos(2\omega t) + \cdots + V_{Tn}cos(n\omega t). \tag{2.1}$$

The current is expressed by:

$$i(t) = I_0 + I_1cos(\omega t + \varphi_1) + I_2cos(2\omega t + \varphi_2) + \cdots + I_ncos(n\omega t + \varphi_n). \tag{2.2}$$

The instantaneous power of the sender is defined as:

$$p(t) = v_T(t)i(t). \tag{2.3}$$

The active power of the sender is defined as the mean value of the instantaneous power. The mean value of the cross product terms with different frequencies are zero, leaving only the voltage current product terms with the matching frequency. The active power of the transmitting end is expressed by:

$$P = \frac{1}{2\pi}\int_0^{2\pi} p(t)dt = V_{T0}I_0 + \frac{V_{T1}I_1}{2}cos(\varphi_1) + \frac{V_{T2}I_2}{2}cos(\varphi_2) + \cdots + \frac{V_{Tn}I_n}{2}cos(\varphi_n). \tag{2.4}$$

Equation 2.4 reveals that the active power is generated only if the voltage and current have matching frequency. Consequently, the active power flow at different frequencies are decoupled from each other. The unique feature of a multi-frequency system enables a converter to control the active power generated at different frequency independently [94]. It should be noted that the DC power is generated by voltage and current at zero frequency thus can also be controlled independent of all other AC active powers.

In DC MMC, each arm generates a DC power to transfer energy between the DC links.

To maintain the voltage balance of the SM capacitors, an AC power is generated and controlled in each arm to compensate for the energy disturbance caused by the DC power transmission.

2.2.2 Steady-state Model

A large-signal model of the DC MMC is developed in the phasor domain to describe its steady-state operation. The following assumptions are made in the model derivation:

- The number of SMs of each arm is sufficiently large such that the AC voltage component of the upper and lower arms only contain fundamental frequency components.
- The converter components are ideal and lossless, i.e., input power equals to the output power.
- The capacitor voltages of the SMs within the same arm are maintained balanced by an active capacitor voltage sorting and selection algorithm.

In deriving the steady-state model of the converter, for the sake of simplicity, only one phase-leg is considered. Nevertheless, the mathematical model of one phase-leg can be extended to the case of an M-phase-leg DC MMC.

Fig. 2.4 shows the corresponding equivalent circuit of a single phase-leg of the DC MMC, where $v^x_{\rm dc}$ and $v^x_{\rm ac}$ represent the DC and AC components of the arm voltage, respectively, $i^x_{\rm dc}$ and $i^x_{\rm ac}$ represent the DC and AC components of the arm current, respectively, $i_{o,\rm dc}$ represents the DC component of the phase current, and $i_{o,\rm ac}$ represents the AC component of the phase current, which should be ideally equal to zero. The cascaded SMs within each arm are represented by ideal controllable voltage sources. The voltage conversion ratio of the converter is defined as:

$$D = \frac{V_{\rm dc2}}{V_{\rm dc1}}, \tag{2.5}$$

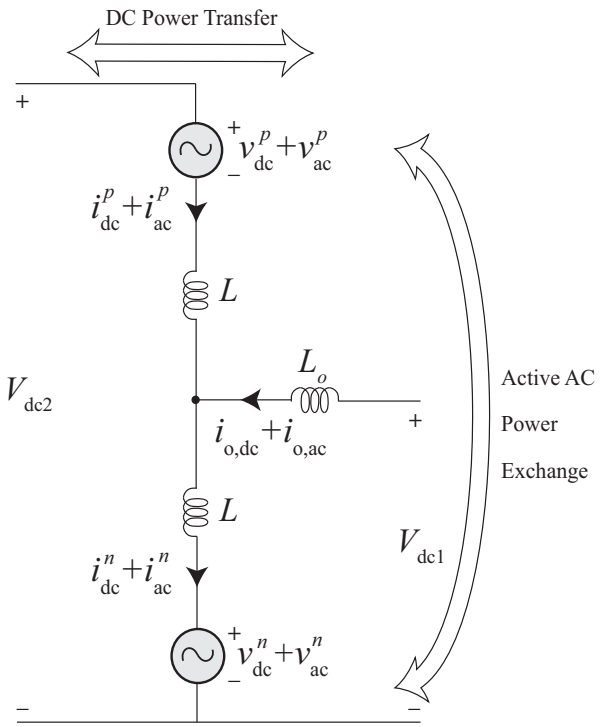


Figure 2.4: Equivalent circuit of one phase-leg of the DC MMC.

In the following analysis presented in this section, the AC voltage and current component are transformed into the phasor domain:

$$\tilde{v}_{ac}^{p} = V_{ac}^{p}\angle\phi, \tag{2.6a}$$

$$\tilde{v}_{ac}^{n} = V_{ac}^{n}\angle 0, \tag{2.6b}$$

$$\tilde{i}_{ac}^{p} = I_{ac}^{p}\angle\phi_p, \tag{2.6c}$$

$$\tilde{i}_{ac}^{n} = I_{ac}^{n}\angle\phi_n, \tag{2.6d}$$

$$\tilde{i}_{o,ac} = I_{o,ac}\angle\phi_o, \tag{2.6e}$$

where V_{ac}^{p} and V_{ac}^{n} represent the amplitudes of the AC voltage component of the upper and lower arms, respectively, I_{ac}^{p} and I_{ac}^{n} represent the amplitudes of the AC current component of the upper and lower arms, respectively, I_{ac}^{o} represent the amplitude of the AC component of the phase current, and ϕ, ϕ_p, ϕ_n, ϕ_o represents the phase angles of the upper arm voltage AC component, the upper arm current AC component, the lower arm current AC

component, and the phase current AC component with respect to the lower arm voltage AC component, respectively. In the AC analysis presented in this section, the phase angles of voltages/currents are represented with respect to the AC component of the lower arm voltage.

In the equivalent circuit shown in Fig. 2.4, the DC voltage component of each arm is a function of D. The AC voltage component of the upper and lower arms may have different amplitude. Since the converter consists of M identical phase-legs, the rated DC power is equally shared among the phase-legs.

Based on the superposition principle, the converter phase-leg equivalent circuit can be decomposed into DC and AC sub-circuits. To derive the DC equations, a DC equivalent circuit of a single phase-leg is obtained and shown in Fig. 2.5. The DC equivalent circuit is obtained by disabling the AC voltage sources shown in Fig. 2.4 such that the inductors are represented as short circuit. Based on the assumption of a lossless conversion, the upper and lower arm voltage and current DC components can be represented by:

$$v_{\mathrm{dc}}^{p} = V_{\mathrm{dc2}} - V_{\mathrm{dc1}}, \tag{2.7}$$

$$v_{\mathrm{dc}}^{n} = V_{\mathrm{dc1}}, \tag{2.8}$$

$$i_{\mathrm{dc}}^{p} = -\frac{I_{\mathrm{dc2}}}{M}, \tag{2.9}$$

$$i_{\mathrm{dc}}^{n} = \frac{I_{\mathrm{dc2}}}{M}\left(\frac{V_{\mathrm{dc2}}}{V_{\mathrm{dc1}}} - 1\right). \tag{2.10}$$

The upper and lower arm DC power can be represented by:

$$P_{\mathrm{dc}}^{p} = \left(\frac{V_{\mathrm{dc1}}}{V_{\mathrm{dc2}}} - 1\right)\frac{P}{M}, \tag{2.11}$$

$$P_{\mathrm{dc}}^{n} = -P_{\mathrm{dc}}^{p} \tag{2.12}$$

where P is the converter output power and is considered positive when power flows from the DC-link 1 to the DC-link 2.

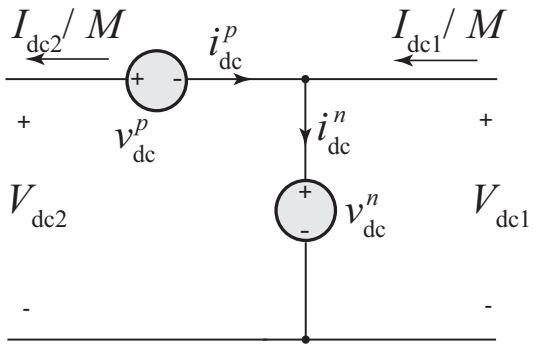


Figure 2.5: DC equivalent circuit of one phase-leg of the DC MMC.

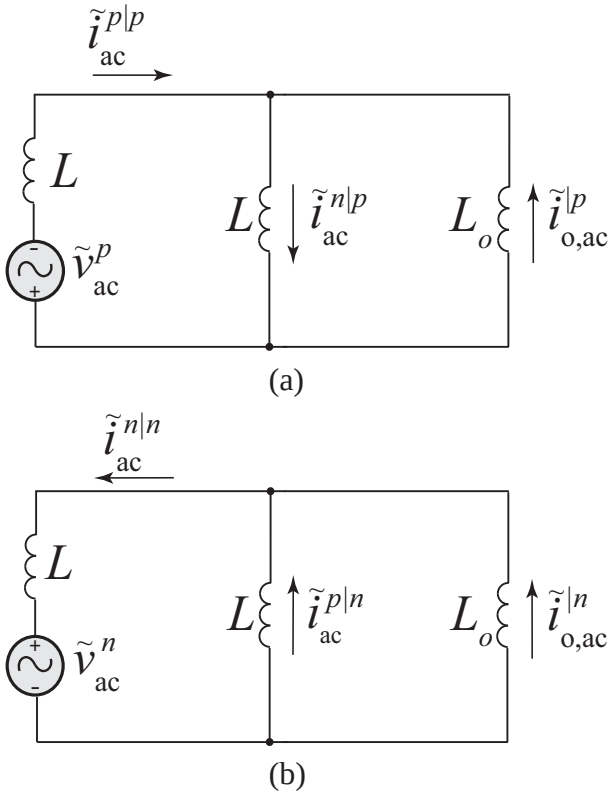


Figure 2.6: AC equivalent circuit of: (a) the upper and (b) lower arms.

Two AC equivalent circuits are derived by disabling the DC voltage sources in Fig. 2.4. Since none of the converter DC terminals carries any AC component under normal operation, for the AC analysis, they can be represented as short circuits. The AC equivalent circuit of the upper arm, shown in Fig. 2.6(a), is obtained by enabling only the upper arm AC voltage source and the AC equivalent circuit of the lower arm, shown in Fig.

2.6(b), is obtained by enabling only the lower arm AC voltage source. In this way, the AC component of the arm currents and the phase current produced by the AC voltages of the upper and lower arms are analyzed separately. In Fig. 2.6, $\tilde{i}_{\mathrm{ac}}^{p|p}$ and $\tilde{i}_{\mathrm{ac}}^{p|n}$ represent the AC components of the upper arm current produced by the AC voltages of the upper and lower arms, respectively, $\tilde{i}_{\mathrm{ac}}^{n|p}$ and $\tilde{i}_{\mathrm{ac}}^{n|n}$ represent the AC components of the lower arm current produced by the AC voltages of the upper and lower arms, respectively, and $\tilde{i}_{\mathrm{o,ac}}^{|p}$ and $\tilde{i}_{\mathrm{p,ac}}^{|n}$ represent the AC components of the phase current produced by the AC voltages of the upper and lower arms, respectively. Based on the equivalent circuits of Figs. 2.6(a) and (b), the following equations are derived for the AC components of the arms and phase current:

$$\tilde{i}_{\mathrm{ac}}^{p} = -\frac{(X_L + X_{L_o})\tilde{v}_{\mathrm{ac}}^{p} + X_{L_o}\tilde{v}_{\mathrm{ac}}^{n}}{j(X_L^2 + 2X_L X_{L_o})}, \tag{2.13}$$

$$\tilde{i}_{\mathrm{ac}}^{n} = -\frac{(X_L + X_{L_o})\tilde{v}_{\mathrm{ac}}^{n} + X_{L_o}\tilde{v}_{\mathrm{ac}}^{p}}{j(X_L^2 + 2X_L X_{L_o})}, \tag{2.14}$$

$$\tilde{i}_{o,\mathrm{ac}} = \left(\frac{X_L}{X_L + X_{L_o}}\right)\frac{\tilde{v}_{\mathrm{ac}}^{p} - \tilde{v}_{\mathrm{ac}}^{n}}{j\left(X_L + \frac{X_L X_{L_o}}{X_L + X_{L_o}}\right)}, \tag{2.15}$$

where $X_L = \omega L$ is the arm inductive reactance and $X_{L_o} = \omega L_o$ is the phase inductive reactance.

The arm AC active power can be calculated by:

$$P_{\mathrm{ac}}^{x} = \mathrm{Re}(\tilde{v}_{\mathrm{ac}}^{x}\tilde{i}_{\mathrm{ac}}^{x*}), \tag{2.16}$$

where $\tilde{i}_{\mathrm{ac}}^{x*}$ represents the complex conjugate of the upper and lower arm current AC components. By substituting $\tilde{i}_{\mathrm{ac}}^{p}$ from (2.13) and $\tilde{i}_{\mathrm{ac}}^{n}$ from (2.14) into (2.16), the arm AC active power are represented by the following equations:

$$P_{\mathrm{ac}}^{p} = \frac{X_{L_o}}{2(X_L^2 + 2X_L X_{L_o})} V_{\mathrm{ac}}^{p} V_{\mathrm{ac}}^{n} sin(\phi), \tag{2.17a}$$

$$P_{\mathrm{ac}}^{n} = -P_{\mathrm{ac}}^{p}, \tag{2.17b}$$

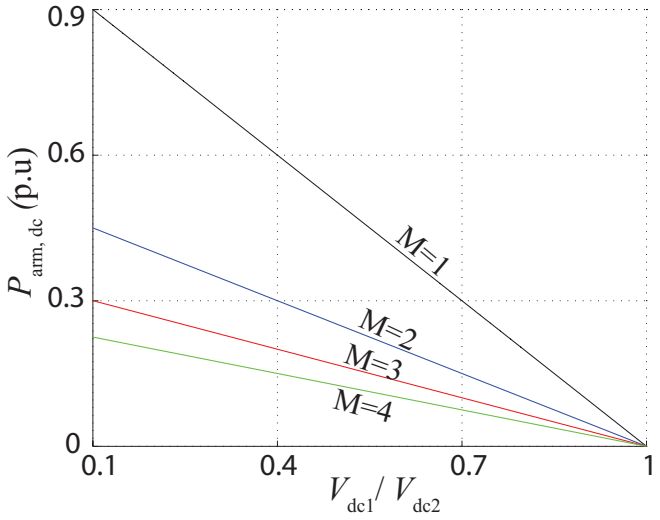


Figure 2.7: Arm DC power versus conversion ratio to transfer one per unit power.

2.2.2.1 Power Balance Constraint

The AC component of the arm current in the DC MMC serves as a mean for exchanging power between the upper and lower arm of each phase-leg. To maintain steady-state power balance of each SM capacitor, summation of the active AC power and DC power flowing through each arm must be equal to zero. By equating AC and DC powers for each arm, the power balance constraint is represented by the following equation:

$$(\frac{V_{\text{dc1}}}{V_{\text{dc2}}} - 1)\frac{P}{M} = -\frac{X_{L_o}}{2(X_L^2 + 2X_L X_{L_o})} V_{\text{ac}}^p V_{\text{ac}}^n sin(\phi). \tag{2.18}$$

Fig. 2.7 presents the effects of the conversion ratio on the arm power for various number of phase-legs to transfer one per unit power. As the conversion ratio increases, the DC power transferred by each arm decreases. Consequently, the AC power required to maintain the power balance of each SM capacitor voltage reduces.

2.2.2.2 SM Capacitor Voltage Balancing

The SM capacitor voltages need to be maintained balanced. Under normal operation of the DC MMC, two types of SM capacitor voltage imbalances exist:

- Type I: the imbalance amongst the SM capacitor voltages in the same arm, and
- Type II: the deviation of average SM capacitor voltages between the upper and lower arms.

Type I imbalance, which also exists in the conventional DC-AC MMC, is due to unequal charge/discharge of the SM capacitors in the same arm. Extensive research effort has been made to mitigate Type I imbalance. The most common method of mitigating Type I imbalance is the selection method that sorts and selects SMs to be inserted/bypassed based on the arm current direction [95]. In contrast, Type II imbalance that is caused by DC power transfer between the DC links is unique to the DC MMC [96]. As shown in Fig. 2.4, the DC power can be transfered bidirectionally between the DC links. The energy stored in the SM capacitors of one arm will quickly deplete and saturate the other arm of the same phase-leg, if each arm produces only a DC current. Consequently, the average voltage of the SM capacitors in the upper and lower arms will deviate from the nominal value even though the voltages of SM capacitors are maintained balanced within the same arm. To mitigate Type II imbalance, the DC MMC exploits an AC circulating current to enable active AC power exchange between the upper and lower arms and to offset the voltage deviation of the SM capacitors caused by the DC power transfer. The AC circulating current needs to be actively controlled to maintain the average capacitor voltages of the upper and lower arms at the nominal value. The closed loop control strategy will be discussed in Chapter 3.

2.2.3 Dynamics of the SM Capacitor Voltages

The dynamics of the sum of the SM capacitor voltages in the upper or lower arm, derived in [97], are:

$$\frac{\mathrm{d}v^{\Sigma p,n}}{\mathrm{d}t} = \frac{N}{C} m^{p,n} i^{p,n}, \tag{2.19}$$

where C is the SM capacitance, $v^{\Sigma p,n}$ is the sum of SM capacitor voltages of the upper or the lower arm, and $m^{p,n}$ represents the insertion index of the upper or the lower arm.

The sum of the SM capacitor voltages is given by:

$$v^{\Sigma p,n} = N v_{C,\text{nominal}} + N\Delta v_C^{p,n}, \tag{2.20}$$

where $v_{C,\text{nominal}}$ represents the nominal value of the SM capacitor voltage and $\Delta v_C^{p,n}$ represents the ripple component of the SM capacitor voltage of the upper or lower arm. The SM capacitance C is normally sized sufficiently large such that $|\Delta v_C^{p,n}| \ll V_{\text{dc2}}$.

The insertion indices of the upper and lower arms are expressed by:

$$m^p = \frac{(V_{\text{dc2}} - V_{\text{dc1}}) + V_{\text{ac}}^{p,\text{ref}} \cos(\omega t + \phi^{\text{ref}})}{V_{\text{dc2}}}, \tag{2.21}$$

$$m^n = \frac{V_{\text{dc1}} + V_{\text{ac}}^{n,\text{ref}} \cos(\omega t)}{V_{\text{dc2}}}, \tag{2.22}$$

where $V^{p,\text{ref}}$ and $V^{n,\text{ref}}$ represent the reference for the amplitude of the AC component of the upper and lower arms, respectively, ϕ^{ref} represents the reference for the phase angle of the AC component of the upper arm voltage, and ω represents the converter operating frequency.

The arm currents can be expressed by:

$$i^p = -\frac{I_{\text{dc2}}}{M} + I_{\text{ac}}^p \cos(\omega t + \phi_p), \tag{2.23}$$

$$i^n = \frac{I_{\text{dc2}}}{M}\left(\frac{V_{\text{dc2}}}{V_{\text{dc1}}} - 1\right) + I_{ac}^n \cos(\omega t + \phi_n). \tag{2.24}$$

Substituting for $m^{p,n}$ from (2.21) - (2.22) and $i^{p,n}$ from (2.23) - (2.24) into (2.19) and integrating both sides of the results, the SM capacitor voltage ripple component can be expressed by:

$$\Delta v_C^p = X_{\text{C}}\left[\left(1 - \frac{V_{\text{dc1}}}{V_{\text{dc2}}}\right) I_{\text{ac}}^p \sin(\omega t + \phi_p) - \frac{V_{\text{ac}}^{p,\text{ref}} I_{\text{dc2}}}{M V_{\text{dc2}}} \sin(\omega t + \phi^{ref}) + \frac{I_{\text{ac}}^p V_{\text{ac}}^{p,\text{ref}}}{4 V_{\text{dc2}}} \sin(2\omega t + \phi^{\text{ref}} + \phi_p)\right], \tag{2.25}$$

$$\Delta v_C^n = X_C[\frac{V_{dc1} I_{ac}^n}{V_{dc2}} \sin(\omega t + \phi_n) + (\frac{V_{dc2}}{V_{dc1}} - 1)\frac{V_{ac}^{n,ref} I_{dc2}}{M V_{dc2}} \sin(\omega t) + \frac{I_{ac}^n V_{ac}^{n,ref}}{4 V_{dc2}} \sin(2\omega t + \phi_n)], \quad (2.26)$$

where $X_C = 1/\omega C$ represents the SM capacitive reactance.

As shown in (2.25) and (2.26), the ripple component of the SM capacitor voltages of the upper and lower arms include one fundamental component term as well as a second-order harmonic term. The amplitude of the fundamental term depends upon the ratio of the input and output DC-link voltages. The magnitude of the SM capacitor voltage ripple in the upper and lower arms is a function of the conversion ratio. As the conversion ratio deviates from 0.5, the magnitudes of the SM capacitor voltage ripple of the upper and lower arms become different. Therefore, it is important to size X_C to ensure the magnitudes of the SM capacitor voltage ripple in both arms stay below the design constraint.

2.3 Simulation Validation

The proposed mathematical model of the DC MMC is validated by simulation studies. A half-bridge SM-based two-phase-leg DC MMC model is constructed in the Matlab Simulink software environment. The control strategy proposed in Chapter 3 in current regulation mode is adopted. The simulated waveforms for the DC MMC operating at various voltage conversion ratios are presented in three case studies. The simulated and analytical results of the peak-to-peak SM capacitor voltage ripple in the upper and lower arms, the peak-to-peak magnitude of the arm current, the peak-to-peak magnitude of the phase current, and the reference phase shift angle to maintain energy balance of the SM capacitors are compared to verify the accuracy of the proposed large-signal model. The parameters of the study system are listed in Table 2.1.

Table 2.1: Parameters of the Study System

Converter Parameters	**Value**
Number of phase legs, M	2
Number of SMs per arm, N	4
SM capacitor, C_{SM}	2.4 mF
Arm inductor, L	0.65 mH
Phase filtering inductor, L_{o}	400 mH
Operating frequency, ω	360 Hz
DC-link 2 voltage, V_{dc2}	8 kV

2.3.1 Case I: Steady-state Operation at $D = 0.8$

Figs. 2.8-2.9 show the simulated waveforms of the DC MMC operating at $D = 0.8$, transferring $P = 2$ MW and $P = -2$ MW, respectively. In the simulation results presented in this section, waveforms of only phase-leg 1 are shown due to the symmetric structure of the converter. As shown in Figs. 2.8(c) and 2.9(c), the voltage ripple of the upper arm capacitors is less than that of the lower arm capacitors due to the non-linear relationship between the voltage conversion ratio and the SM capacitor voltage ripple. As shown in Figs. 2.8(d) and 2.9(d), the AC current component of the upper and lower arms are equal because sufficiently large phase filtering inductors guarantee negligible phase current ripple shown in Figs. 2.8(e) and 2.9(e). $\phi = 155°$ and $\phi = 204°$ are required to ensure energy balance of the SM capacitors for $P = 2$ MW and $P = -2$ MW as shown in Figs. 2.8(g) and 2.9(g), respectively.

The comparison between the simulated and analytical results for $P = 2$ MW and $P = -2$ MW are summarized in Tables 2.2-2.3, respectively. As demonstrated in the tables, the errors associated with the analytical results obtained based on the proposed mathematical model are less than 7% compared to the simulated results.

2.3.2 Case II: Steady-state Operation at $D = 0.6$

Figs. 2.10-2.11 show the simulated waveforms of the DC MMC operating at $D = 0.6$, transferring $P = 3$ MW and $P = -3$ MW, respectively. As shown in Figs. 2.10(c) and

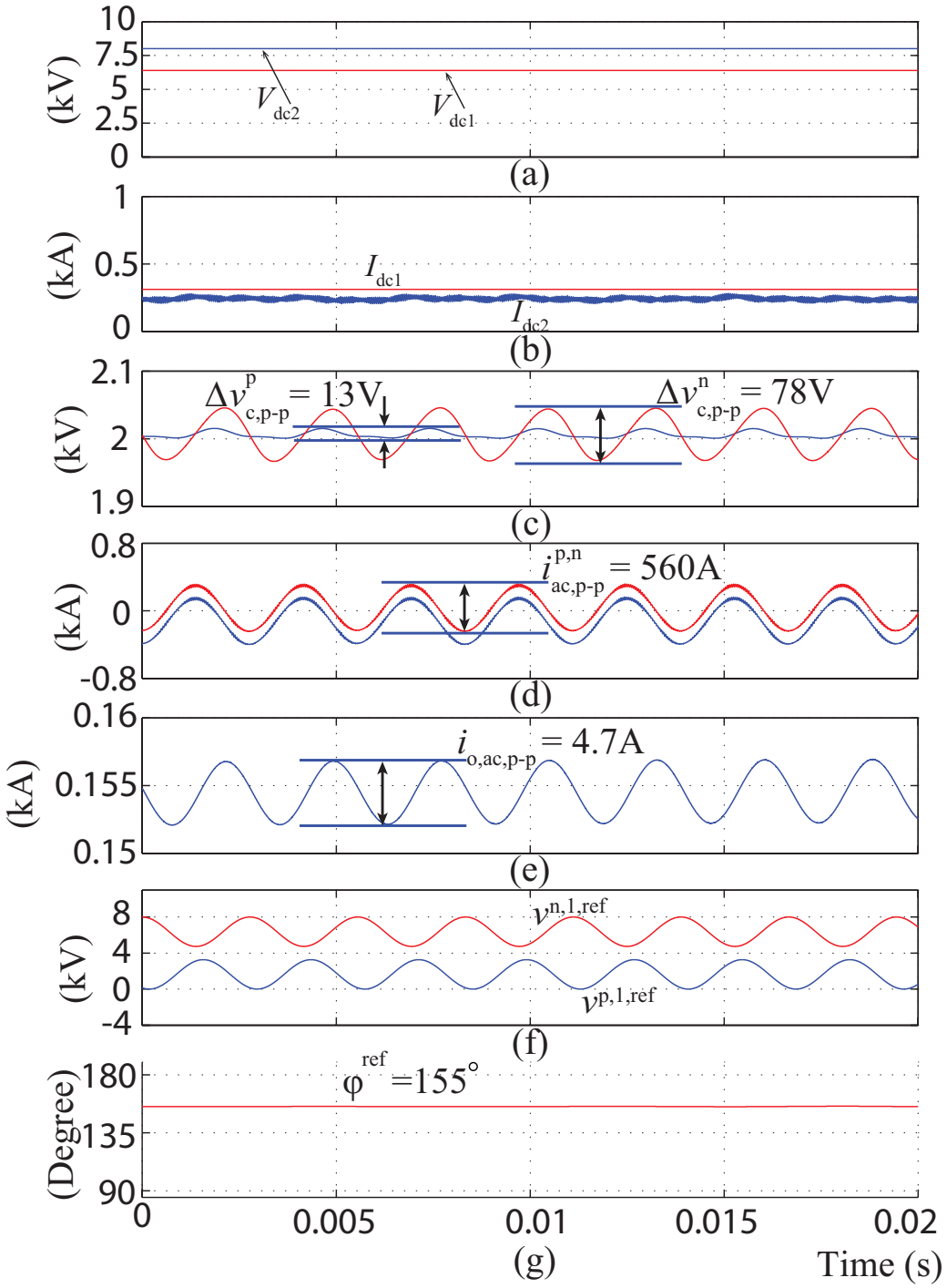


Figure 2.8: Steady-state converter waveforms for $P = 2$ MW when D=0.8: (a) input and output DC voltages, (b) input and output currents, (c) SM capacitor voltages of the upper and lower arms of phase-1, (d) upper and lower arm currents of phase-1, (e) phase current of phase-1, (f) upper and lower arm reference voltages of phase-1, and (g) reference phase shift.

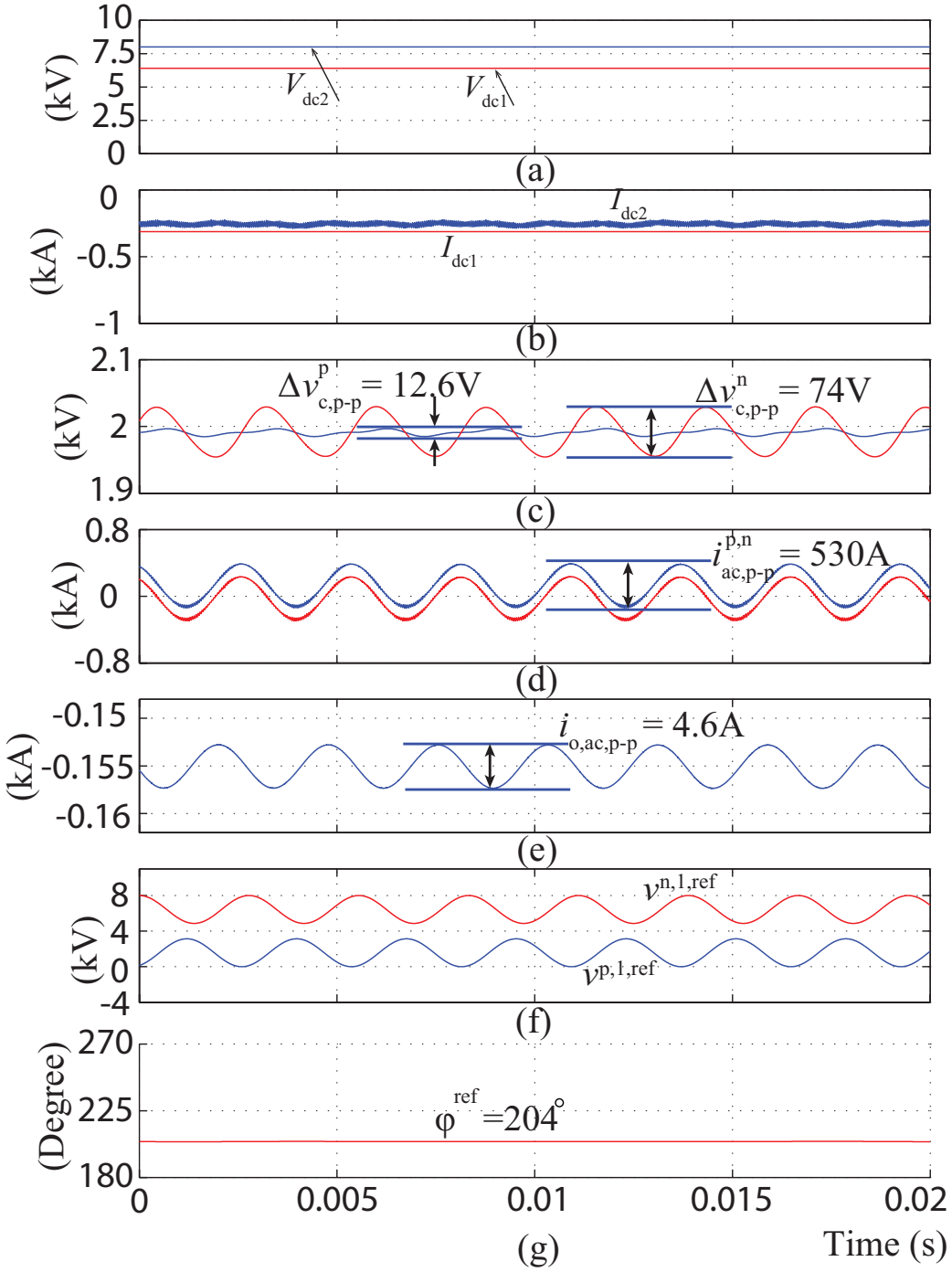


Figure 2.9: Steady-state converter waveforms for $P = -2$ MW when D=0.8: (a) input and output DC voltages, (b) input and output currents, (c) SM capacitor voltages of the upper and lower arms of phase-1, (d) upper and lower arm currents of phase-1, (e) phase current of phase-1, (f) upper and lower arm reference voltages of phase-1, and (g) reference phase shift.

Table 2.2: Simulation and Analytical Results of the DC MMC at $D = 0.8$ and $P = 2$ MW

	Simulation	**Analytical**	**Error**
Upper arm SM capacitor voltage (peak-to-peak value)	13 V	13.4 V	3%
Lower arm SM capacitor voltage (peak-to-peak value)	78 V	78.2 V	0.25%
AC current component of the upper and lower arm (peak-to-peak value)	0.56 kA	0.54 kA	3.5%
AC current component of the phase current (peak-to-peak value)	4.7 A	4.57 A	2.5%
Reference phase-shift angle	155°	152°	1.9%

Table 2.3: Simulation and Analytical Results of the DC MMC at $D = 0.8$ and $P = -2$ MW

	Simulation	**Analytical**	**Error**
Upper arm SM capacitor voltage (peak-to-peak value)	12.6 V	13.4 V	6.3%
Lower arm SM capacitor voltage (peak-to-peak value)	74 V	78.2 V	5.2%
AC current component of the upper and lower arm (peak-to-peak value)	0.53 kA	0.54 kA	1.8%
AC current component of the phase current (peak-to-peak value)	4.6 A	4.56 A	0.8%
Reference phase-shift angle	204°	208°	1.9%

2.11(c), the voltage ripple of the upper arm capacitors is less than that of the lower arm capacitors but the difference is smaller compared to the $D = 0.8$ case. The average SM capacitor voltage of the upper and lower arms are maintained at 2 kV indicating that the energy balance is maintained. The arm currents of the upper and lower arms consist of an AC and a DC component as shown in Figs. 2.10(d) and 2.11(d). The AC current component is controlled to maintain the energy balance of the SM capacitors while the DC current component is controlled to deliver DC power to the DC-link. $\phi = 161°$ and $\phi = 200°$ are generated by the controller to maintain the energy balance of the SM capacitors for $P = 3$ MW and $P = -3$ MW as shown in Figs. 2.10(g) and 2.11(g), respectively.

The comparison between the simulated and analytical results for $P = 3$ MW and $P = -3$ MW are summarized in Tables 2.4-2.5, respectively. As demonstrated in the tables, the

errors associated with the analytical results obtained based on the proposed mathematical model are less than 7% compared to the simulated results.

Table 2.4: Simulation and Analytical Results of the DC MMC at $D = 0.6$ and $P = 3$ MW

	Simulation	**Analytical**	**Error**
Upper arm SM capacitor voltage (peak-to-peak value)	40 V	38.4 V	4%
Lower arm SM capacitor voltage (peak-to-peak value)	72 V	73.5 V	5.2%
AC current component of the upper and lower arm (peak-to-peak value)	0.798 kA	0.788 kA	1.2%
AC current component of the phase current (peak-to-peak value)	9.5 A	9.26 A	2.5%
Reference phase-shift angle	161°	159°	1.2%

Table 2.5: Simulation and Analytical Results of the DC MMC at $D = 0.6$ and $P = -3$ MW

	Simulation	**Analytical**	**Error**
Upper arm SM capacitor voltage (peak-to-peak value)	36 V	38.4 V	6%
Lower arm SM capacitor voltage (peak-to-peak value)	79 V	73.5 V	6.9%
AC current component of the upper and lower arm (peak-to-peak value)	0.799 kA	0.788 kA	1.3%
AC current component of the phase current (peak-to-peak value)	9.5 A	9.26 A	2.5%
Reference phase-shift angle	200°	201°	0.5%

2.3.3 Case III: Steady-state Operation at $D = 0.4$

Figs. 2.12-2.13 show the simulated waveforms of the DC MMC operating at $D = 0.4$ transferring $P = 2$ MW and $P = -2$ MW, respectively. As shown in Figs. 2.12(c) and 2.13(c), the voltage ripple of the upper arm capacitors is greater than that of the lower arm capacitors in this case. $\phi = 161°$ and $\phi = 199°$ are required to ensure energy balance of the SM capacitors for $P = 2$ MW and $P = -2$ MW as shown in Figs. 2.12(g) and 2.13(g), respectively.

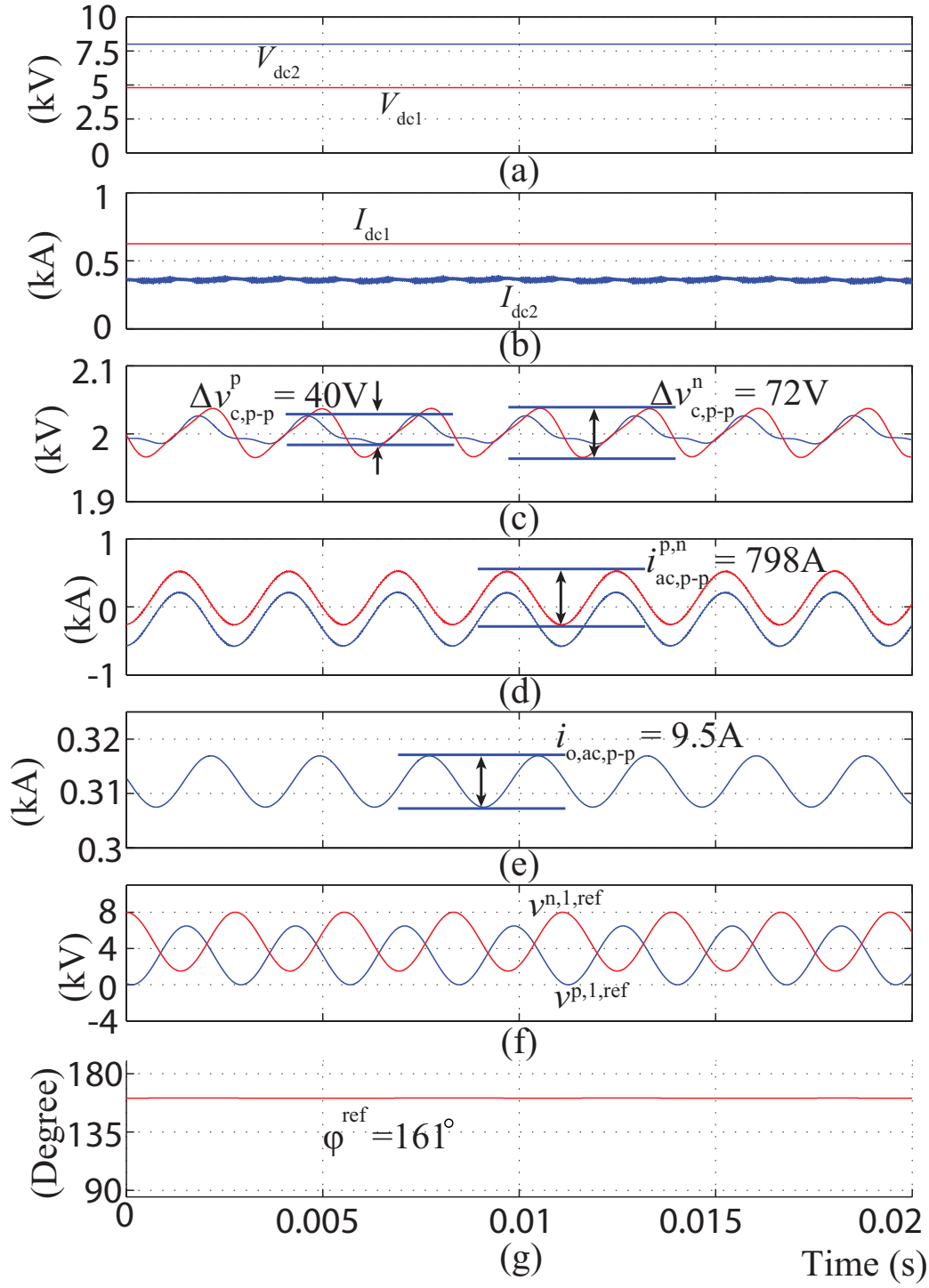


Figure 2.10: Steady-state converter waveforms for P = 3 MW when D=0.6: (a) input and output DC voltages, (b) input and output currents, (c) SM capacitor voltages of the upper and lower arms of phase-1, (d) upper and lower arm currents of phase-1, (e) phase current of phase-1, (f) upper and lower arm reference voltages of phase-1, and (g) reference phase shift.

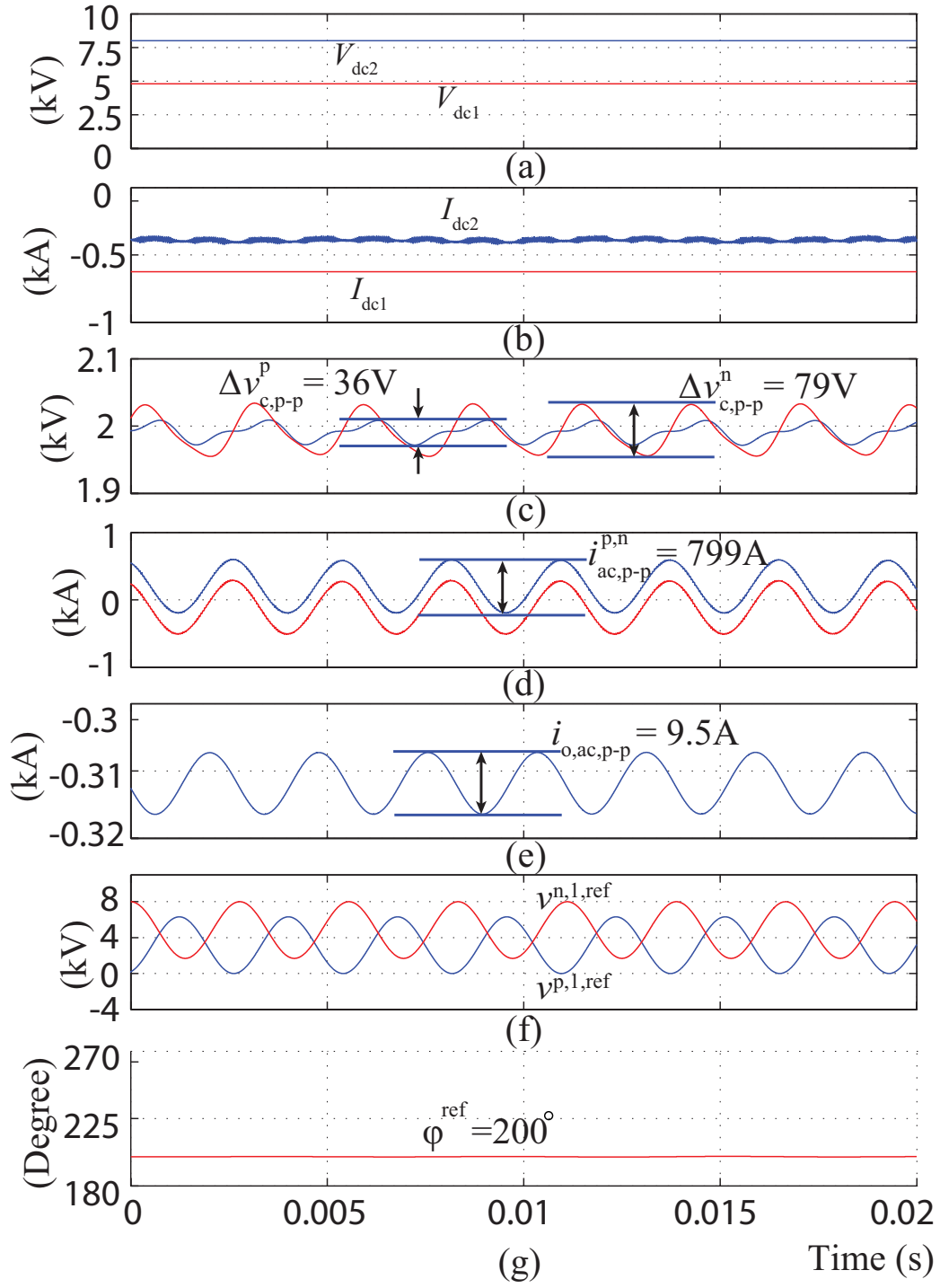


Figure 2.11: Steady-state converter waveforms for $P = -3$ MW when D=0.6: (a) input and output DC voltages, (b) input and output currents, (c) SM capacitor voltages of the upper and lower arms of phase-1, (d) upper and lower arm currents of phase-1, (e) phase current of phase-1, (f) upper and lower arm reference voltages of phase-1, and (g) reference phase shift.

The comparison between the simulated and analytical results for $P = 3$ MW and $P = -3$ MW are summarized in Tables 2.6-2.7, respectively. As demonstrated in the tables, the errors associated with the analytical results obtained based on the proposed mathematical model are less than 7% compared to the simulated results.

Table 2.6: Simulation and Analytical Results of the DC MMC at $D = 0.4$ and $P = 2$ MW

	Simulation	**Analytical**	**Error**
Upper arm SM capacitor voltage (peak-to-peak value)	79 V	74 V	6.3%
Lower arm SM capacitor voltage (peak-to-peak value)	37 V	39 V	5.4%
AC current component of the upper and lower arm (peak-to-peak value)	0.8 kA	0.802 kA	0.25%
AC current component of the phase current (peak-to-peak value)	9 A	9.3 A	3.3%
Reference phase-shift angle	161°	159°	1.2%

Table 2.7: Simulation and Analytical Results of the DC MMC at $D = 0.4$ and $P = -2$ MW

	Simulation	**Analytical**	**Error**
Upper arm SM capacitor voltage (peak-to-peak value)	72 V	74 V	2.7%
Lower arm SM capacitor voltage (peak-to-peak value)	40 V	39 V	2.5%
AC current component of the upper and lower arm (peak-to-peak value)	0.798 kA	0.802 kA	0.5%
AC current component of the phase current (peak-to-peak value)	9.6 A	9.3 A	3.1%
Reference phase-shift angle	199°	201°	1%

2.4 Chapter Summary

This chapter presents the architecture and operation principle of the single stage DC MMC. The DC MMC features reduced converter cost and operating losses as compared to the traditional DC-AC-DC MMC based converter. Only half-bridge SM is required for bidirectional step-down operation whereas full-bridge SM enables step-up operation.

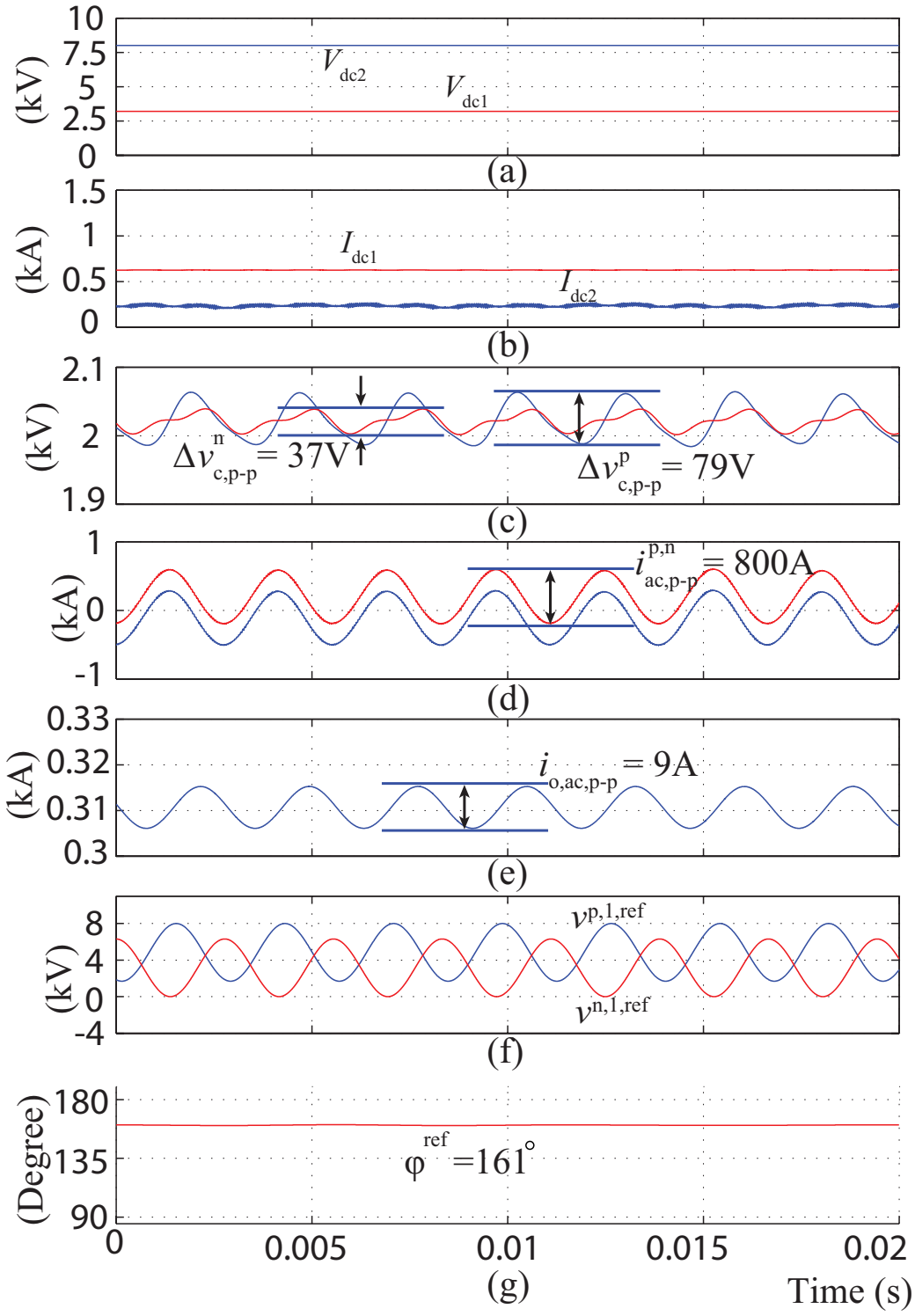


Figure 2.12: Steady-state converter waveforms for P = 2 MW when D=0.4: (a) input and output DC voltages, (b) input and output currents, (c) SM capacitor voltages of the upper and lower arms of phase-1, (d) upper and lower arm currents of phase-1, (e) phase current of phase-1, (f) upper and lower arm reference voltages of phase-1, and (g) reference phase shift.

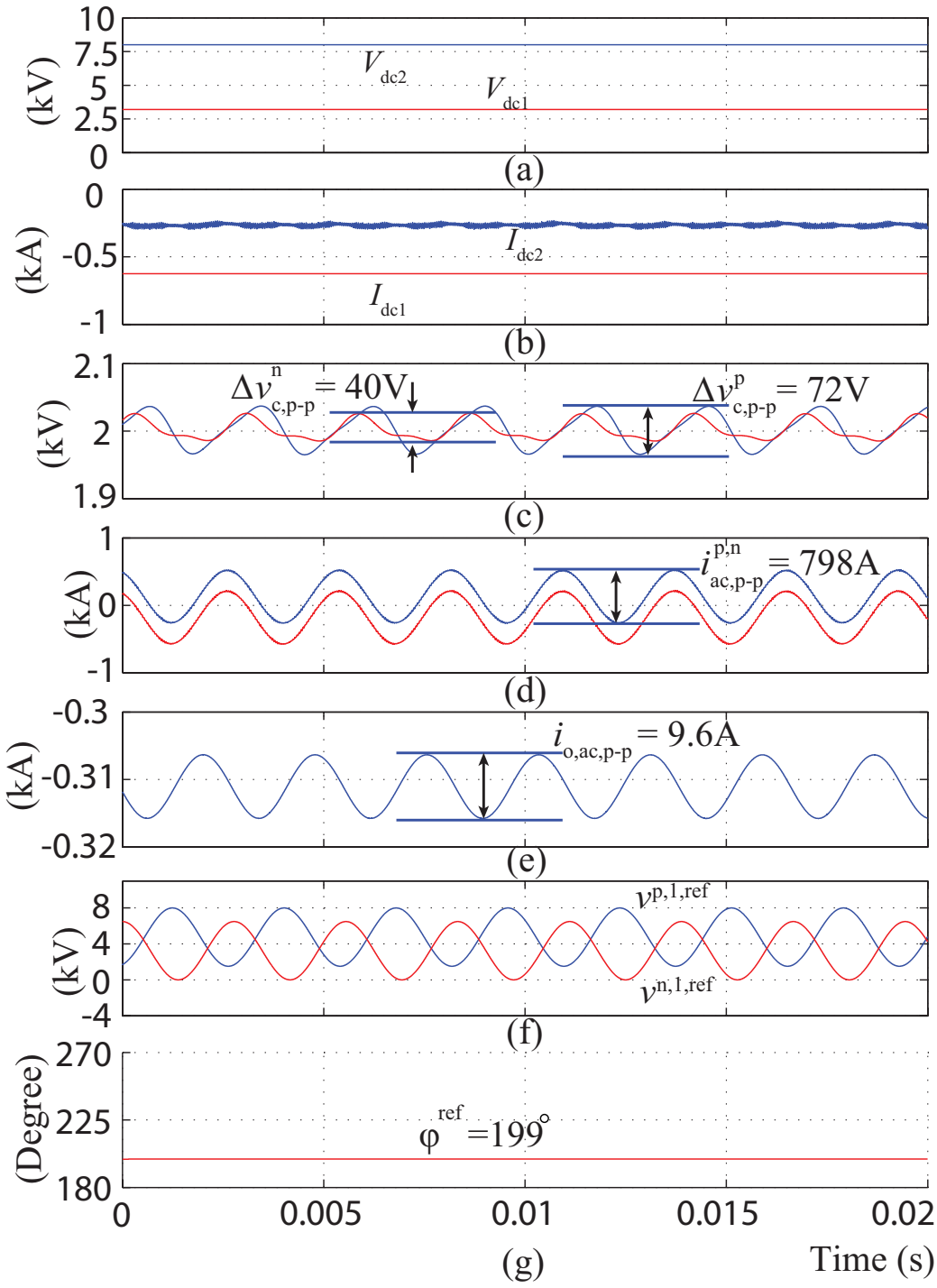


Figure 2.13: Steady-state converter waveforms for $P = -2$ MW when D=0.4: (a) input and output DC voltages, (b) input and output currents, (c) SM capacitor voltages of the upper and lower arms of phase-1, (d) upper and lower arm currents of phase-1, (e) phase current of phase-1, (f) upper and lower arm reference voltages of phase-1, and (g) reference phase shift.

The DC MMC relies on the principle of orthogonal power flow to transfer power between its DC links and maintain capacitor voltage balance of its SMs. The steady state model that is derived in the chapter reveals the power balance constraint of each arm. A shift of the DC operating point of the DC MMC may impose a significant change of its power balance condition. It is essential to control the AC circulating current to maintain the power balance of the converter.

A mathematical model is developed for the DC MMC. The accuracy of the proposed model is validated in simulation studies at various operation conditions.

CHAPTER 3

CLOSED-LOOP CONTROL OF THE HALF-BRIDGE SM BASED DC MMC

The DC MMC relies on AC active power to maintain the average voltage of its SM capacitors at nominal value. Dynamically varying DC load power may shift the AC active power that is necessary to maintain the energy balance of the SM capacitors. An open-loop control strategy is incapable of tracking dynamically changing load conditions. Consequently, the average SM capacitor voltages deviate from the nominal value.

Fig. 3.1 shows the SM capacitor voltages of a DC MMC, when subjected to a power change under open-loop control. Initially, the converter operates under steady state transferring -2.5 MW power. At $t = 0.02$ s, the load ramps down to -1.5 MW, which in turn shifts the AC power required to maintain the energy balance of the SM capacitors. Consequently, the energy stored in the SM capacitors are no longer balanced, resulting in divergence of the average SM capacitor voltages from the nominal value.

In this chapter, a close-loop control strategy is developed to simultaneously regulate the output DC-link current/voltage, maintain the SM capacitor voltages balanced, and minimize the AC circulating current for any arbitrary voltage conversion ratio and power throughput. The control scheme consists of a DC-link current/voltage regulator to regulate the low-voltage-side DC-link current/voltage combined with a power balance controller to maintain the power balance between the upper and lower arms.

The DC MMC based on half-bridge SMs features low semiconductor losses and device count. The close-loop control strategy developed in this chapter is focused on the half-bridge configuration. Consequently, step-down operation with bidirectional power transfer is covered in this chapter.

Performance and effectiveness of the proposed control strategy are evaluated based on simulation studies in the Matlab Simulink software environment. Moreover, a laboratory

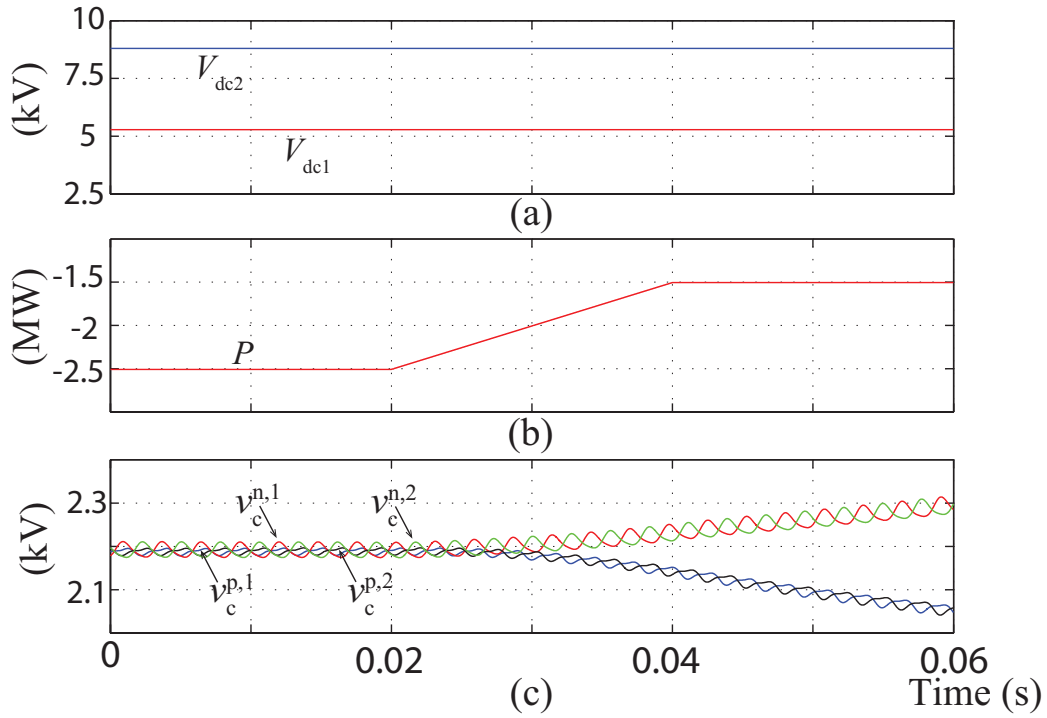


Figure 3.1: SM capacitor voltage divergence subsequent to a load power change: (a) DC link voltages, (b) reference converter load power, and (c) SM capacitor voltages.

prototype is developed and built to experimentally validate the proposed control strategy. The details of the experimental validation will be covered in Chapter 6.

3.1 Development of the Closed-loop Control Strategy

3.1.1 SM Capacitor Voltage Balancing Strategy

As discussed in Chapter 2, both DC and active AC power components flow in each arm of the DC MMC. The mismatch between the DC and AC active powers causes Type II SM capacitor imbalance, which leads to unequal average SM capacitor voltage between the converter arms.

As shown in (2.11), the arm DC power is fixed by external variables, i.e., V_{dc1}, V_{dc2}, and P. To satisfy (2.18), the arm active AC power should be actively controlled to track the arm DC power in the upper and lower arms. To control the arm active AC power, V_{ac}^{p}, V_{ac}^{n}, and ϕ are controlled to inject an AC circulating current.

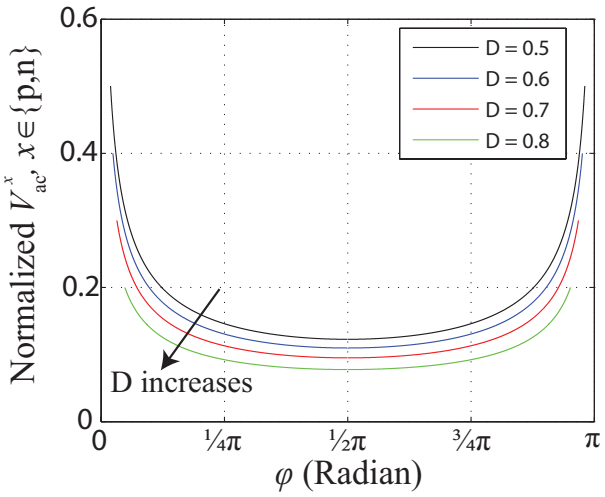
Equation (2.18) reveals two possible control strategies to maintain the power balance of each arm:

- Strategy 1: maintain ϕ constant and change V_{ac}^{p} and V_{ac}^{n} to accommodate changes in V_{dc1}, V_{dc2}, and P;
- Strategy 2: maintain V_{ac}^{p} and V_{ac}^{n} constants and change ϕ to accommodate changes in V_{dc1}, V_{dc2}, and P.

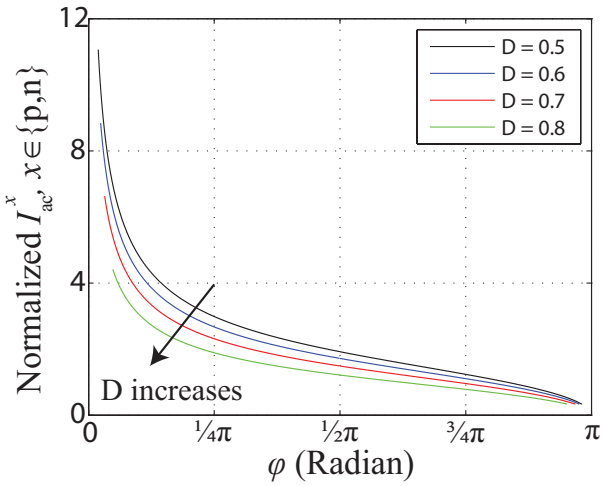
Both strategies are equally valid in maintaining the average SM capacitor voltages balance of the arms. Nevertheless, Strategy 2 is preferred for two reasons: (i) it is capable of minimizing the injected AC circulating current by maintaining V_{ac}^{p} and V_{ac}^{n} at their maximum attainable values and (ii) it avoids over-modulation by maintaining the peak value of arm voltages at constants.

From the power loss, device rating and cost perspectives, it is essential to minimize the amplitude of the injected AC circulating current. Fig. 3.2 illustrates the impact of ϕ on V_{ac}^{p}, V_{ac}^{n}, and the AC circulating current. In Fig. 3.2, it is assumed that a positive 1 p.u. power is transfered. Based on Fig. 3.2, four important facts are revealed:

- The required V_{ac}^{p} and V_{ac}^{n} to maintain the power balance is symmetric with respect to $\phi = \frac{\pi}{2}$.
- The required V_{ac}^{p} and V_{ac}^{n} increases as ϕ deviates from $\frac{\pi}{2}$ in both directions and reaches the maximum as ϕ approaches 0 or π for various D.
- The amplitude of the AC circulating current to maintain the power balance decreases as ϕ increases and reaches the minimum at $V_{\text{ac}}^{x} = V_{\text{ac,max}}^{x}$, $x \in \{p, n\}$ for various D.
- The required ϕ to drive the minimum AC circulating current is different for various D.



(a)



(b)

Figure 3.2: Impact of ϕ on (a) the amplitude of the AC component of the arm voltage and (b) the AC circulating current for various D.

Consequently, for $P > 0$, to minimize the AC circulating current while maintaining the power balance between the upper and lower arm for various D, two conditions must be satisfied:

- The converter must operate in the region of $\phi \in [\frac{\pi}{2}, \pi)$.
- V_{ac}^{p} and V_{ac}^{n} must be maintained at their maximum attainable values for various D.

Similarly, for $P < 0$, the converter must operate in the region of $\phi \in (\pi, \frac{3\pi}{2}]$. This analysis implies that Strategy 2 is the preferred control strategy for the DC MMC as it can always

maintain V_{ac}^{p} and V_{ac}^{n} at their maximum attainable values, regardless of P and D. In contrast, although Strategy 1 can also maintain the power balance in the arms, it lacks the ability to minimize the AC circulating current. As P changes, the required ϕ to inject the minimized AC circulating current also varies. Consequently, maintaining ϕ at a constant value does not always produce a minimized AC circulating current.

3.1.2 The Maximum Attainable Amplitude of the Arm Voltages

It is assumed that during normal operation, the capacitor voltages of the SMs are maintained at $\frac{V_{\text{dc2}}}{N}$. For proper operation of the converter, the following constraints must be satisfied:

- The half-bridge SM can only insert a positive voltage in the ON-state, thus the instantaneous arm voltage must be greater than zero.
- The maximum instantaneous arm voltage must be smaller than the DC-link 2 voltage.

Therefore, the maximum amplitudes of the AC component of the upper and lower arm voltages are determined by:

$$V_{\text{ac,max}}^{p} = \text{Min}[v_{\text{dc}}^{p}, (V_{\text{dc2}} - v_{\text{dc}}^{p})], \tag{3.1}$$

$$V_{\text{ac,max}}^{n} = \text{Min}[v_{\text{dc}}^{n}, (V_{\text{dc2}} - v_{\text{dc}}^{n})]. \tag{3.2}$$

Fig. 3.3 shows the maximum attainable amplitude of the AC component of the upper and lower arm voltages versus D. As shown in Fig. 3.3, the AC components of the voltages of the upper and lower arms have the same maximum attainable value for a given D. $V_{\text{ac,max}}^{p}$ and $V_{\text{ac,max}}^{n}$ reach the maximum at $D = 0.5$. As the conversion ratio moves away from 0.5, $V_{\text{ac,max}}^{p}$ and $V_{\text{ac,max}}^{n}$ decrease linearly in both directions.

3.1.3 The Closed-loop Control Strategy

The proposed closed-loop control strategy for the DC MMC involves three tasks:

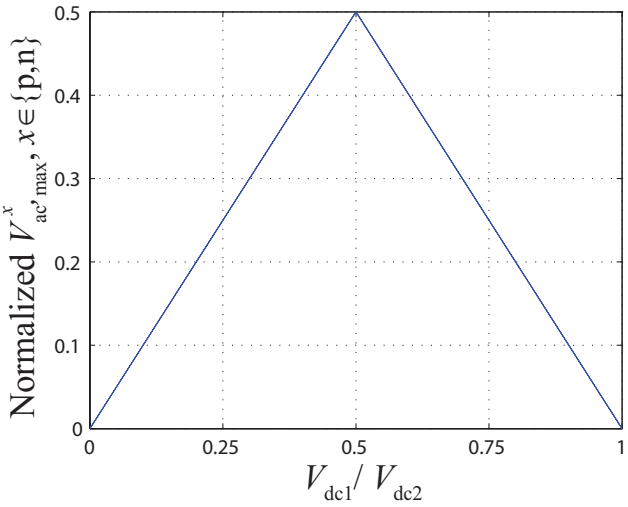


Figure 3.3: The maximum attainable amplitude of the AC component of the arm voltages versus the voltage conversion ratio.

- Minimization of the voltage divergence between the SM capacitors in the upper and lower arms of each phase-leg.
- Minimization of the AC circulating current required to maintain the power balance of the upper and lower arms.
- Regulation of the DC-link power.

The modulation signals for the upper and lower arms of each phase-leg are expressed by:

$$v^{p,\text{ref}} = v_{\text{dc}}^{p,\text{ref}} + V_{\text{ac}}^{p,\text{ref}} cos(\omega t + \phi^{\text{ref}}), \tag{3.3}$$

$$v^{n,\text{ref}} = v_{\text{dc}}^{n,\text{ref}} + V_{\text{ac}}^{n,\text{ref}} cos(\omega t). \tag{3.4}$$

Fig. 3.4 shows the overall block diagram of the proposed control strategy in current regulation mode, which consists of a phase current regulator combined with an arm power balance controller. $v_{\text{dc}}^{p,\text{ref}}$ and $v_{\text{dc}}^{n,\text{ref}}$ are generated by the DC-link current regulator while $V_{\text{ac}}^{p,\text{ref}}$, $V_{\text{ac}}^{n,\text{ref}}$, and ϕ^{ref} are generated by the arm power balance controller to maintain the SM capacitor voltages balanced. The control strategy shown in Fig. 3.4 is designed for interconnecting two DC power grids. Consequently, the DC-link current regulator is applied

as the outer loop controller to achieve a fast and smooth control in the power throughput of the converter. Since the phase current of each phase-leg is regulated independently, the proposed control strategy can be easily scaled up for an arbitrary number of phase legs. In case of $M > 1$, the DC-link current is equally split amongst the M phases. An evenly distributed DC current among the phases is essential for preventing core saturation in the coupled inductor and the zigzag grounding transformer where the DC fluxes produced by different phase currents should be perfectly canceled.

To regulate the phase/DC-link current at its reference value, the DC-link current regulator employs a Proportional-Integral (PI) compensator that acts on the difference between the reference and measured i_o generating $v_{\mathrm{dc}}^{n,\mathrm{ref}}$ to facilitate bidirectional DC power transfer. $v_{\mathrm{dc}}^{p,\mathrm{ref}}$ is determined by subtracting $v_{\mathrm{dc}}^{n,\mathrm{ref}}$ from V_{dc2} to satisfy the KVL in the DC loop formed by V_{dc2}, v_{dc}^{p} and v_{dc}^{n}.

As shown in Fig. 3.4, the arm power balance controller maintains the power balance between the upper and lower arms such that the deviation of the average SM capacitor voltages is minimized. To this end, a voltage error is generated by comparing the average of the sum of the SM capacitor voltages between the upper and lower arms. This error indicates the magnitude of Type II imbalance between the upper and lower arms. Since the ripple component of each SM capacitor voltage in a DC MMC mainly consists of fundamental and second-order harmonic frequency terms, two notch filters are utilized to remove the ripple components from the measured sum of SM capacitor voltage. A PI compensator acts on the error to generate ϕ^{ref} that drives an active AC power to minimize the deviation of the SM capacitor voltages of the upper and lower arms.

To minimize the AC circulating current, $v_{\mathrm{dc}}^{p,\mathrm{ref}}$ and $v_{\mathrm{dc}}^{n,\mathrm{ref}}$ generated by the DC-link current regulator are substituted into (3.1) and (3.2) to determine $V_{\mathrm{ac,max}}^{p}$ and $V_{\mathrm{ac,max}}^{n}$. The maximum attainable AC components of the arm voltages are applied by the power balance controller such that $V_{\mathrm{ac}}^{p,\mathrm{ref}} = V_{\mathrm{ac,max}}^{p}$ and $V_{\mathrm{ac}}^{n,\mathrm{ref}} = V_{\mathrm{ac,max}}^{n}$. In this way, the maximum attainable values of V_{ac}^{p} and V_{ac}^{n} are always applied for arbitrary D and P.

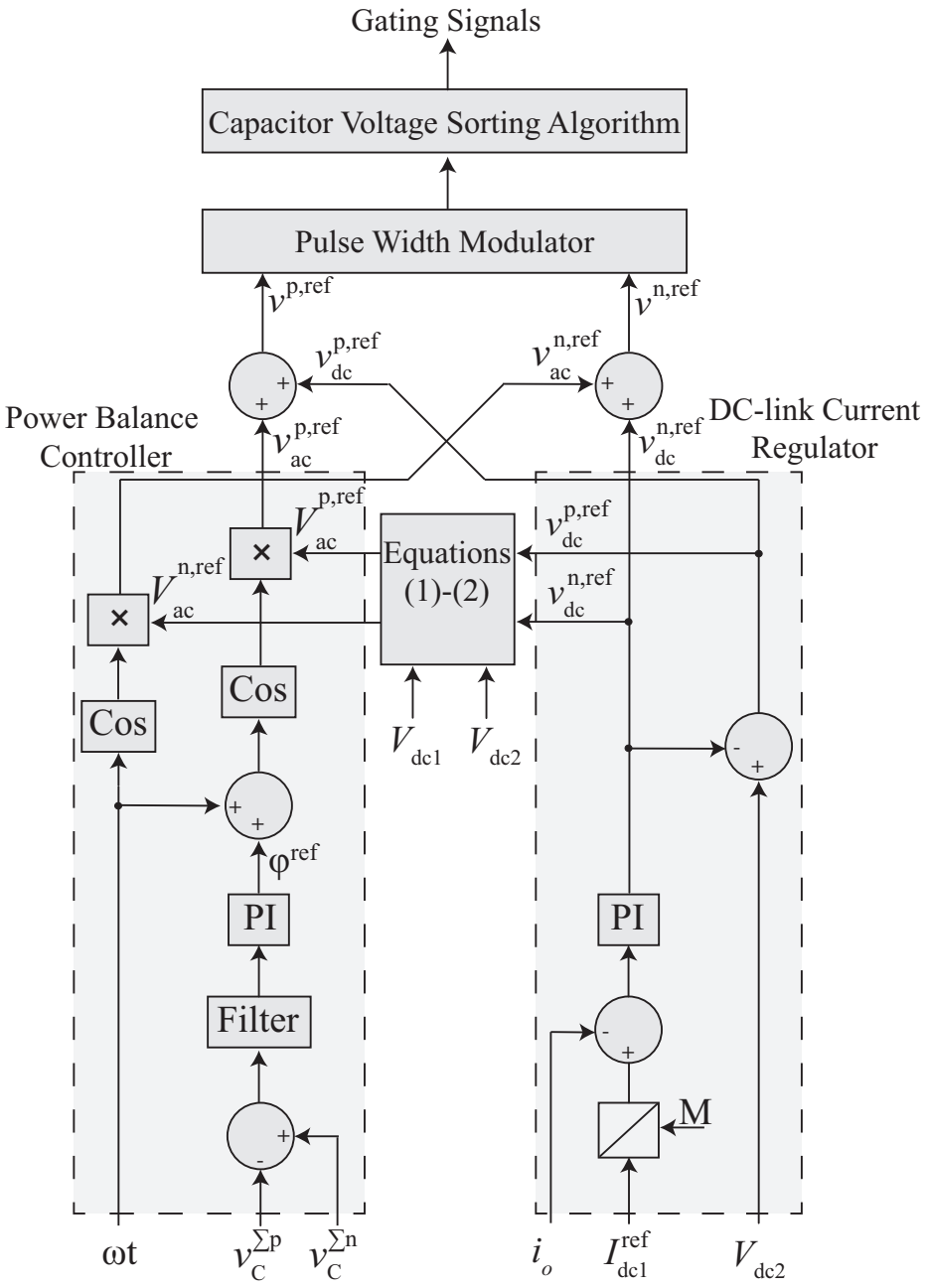


Figure 3.4: Overall block diagram of the proposed closed-loop control strategy in the current regulation mode.

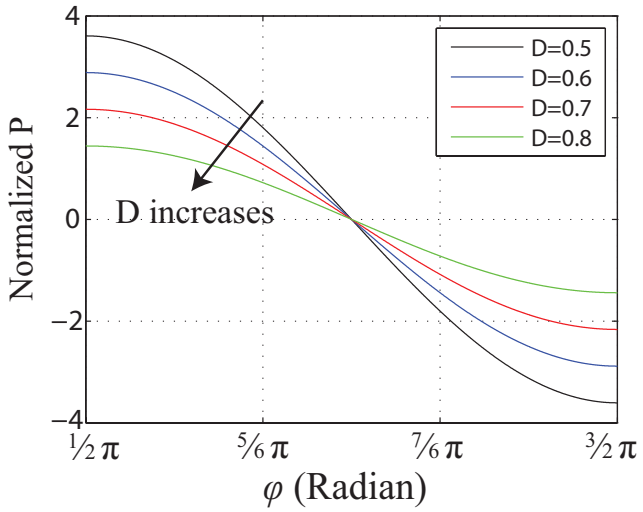


Figure 3.5: Normalized converter power throughput versus ϕ.

Fig. 3.5 demonstrates P versus ϕ for various D. In Fig. 3.5, it is assumed that the maximum attainable arm voltages are applied to achieve a minimized AC current. Based on the reference P (by controlling $I_{\text{dc1}}^{\text{ref}}$), a unique ϕ is required to maintain the power balance of the upper and lower arms. As shown in Fig. 3.5, the DC MMC operates in the region of $\phi \in [\frac{\pi}{2}, \pi)$ for $P > 0$ and in the region of $\phi \in (\pi, \frac{3\pi}{2}]$ for $P < 0$. The maximum positive power is delivered at $\phi = \frac{\pi}{2}$ while the maximum negative power is delivered at $\phi = \frac{3\pi}{2}$. It should be noted that, due to the fact that $V_{\text{ac,max}}^{p}$ and $V_{\text{ac,max}}^{n}$ are reduced as D increases, the maximum P decreases as D increases.

For applications where a voltage regulation is desired, the DC-link current regulator is replaced with a DC-link voltage regulator. The overall block diagram in voltage regulation mode is shown in Fig. 3.6. The DC-link voltage regulator is comprised of an outer voltage regulation loop and an inner current regulation loop, which employ two PI compensators. In the block diagram shown in Fig. 3.6, the DC-link 1 voltage is regulated assuming that a voltage source is connected to the DC-link 2. Similar to the current control mode, $v_{\text{dc}}^{p,\text{ref}}$ and $v_{\text{dc}}^{n,\text{ref}}$ are generated by the DC-link voltage regulator. The power balance controller is identical to that of the current control mode.

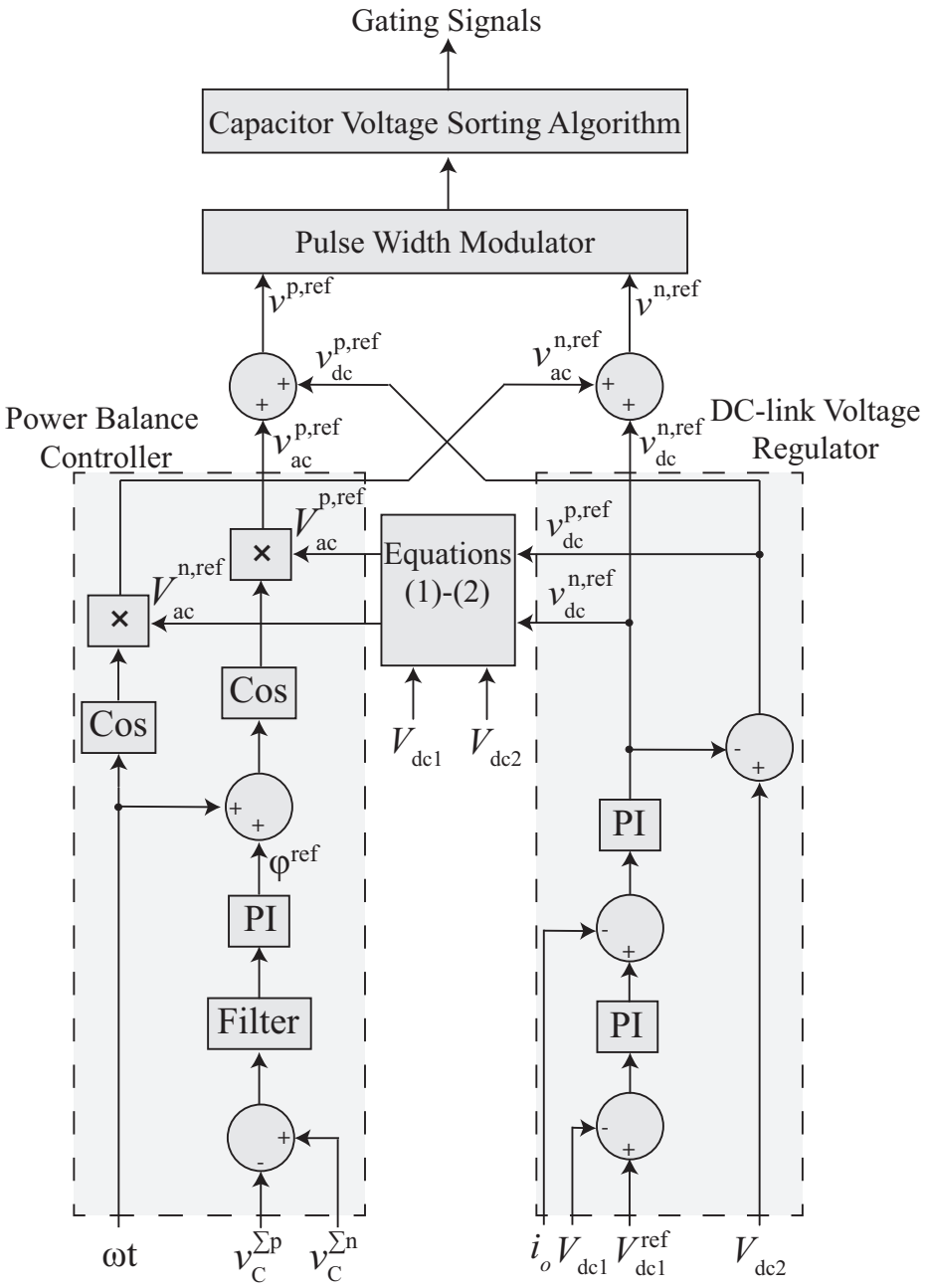


Figure 3.6: Overall block diagram of the proposed closed-loop control strategy in voltage regulation mode.

3.2 Simulation Results

To demonstrate performance and effectiveness of the proposed closed-loop control strategy, a switched model of a two-phase-leg DC MMC of Fig. 2.2 is constructed in the Matlab Simulink. The proposed closed-loop control strategy in both current and voltage control modes is implemented. The parameters of the study system are listed in Table 3.1.

Table 3.1: Parameters of the Study System

Converter Parameters	**Value**
Number of phase legs, M	2
Number of SMs per arm, N	4
SM capacitor, C_{SM}	4.2 mF
Arm inductor, L	0.8 mH
Phase filtering inductor, L_{o}	260 mH
Operating frequency, ω	360 Hz
Rated power throughput, $\|P\|$	5 MW
DC-link 1 voltage, V_{dc1}	5.28 kV
DC-link 2 voltage, V_{dc2}	8.8 kV

3.2.1 Case I: Current Regulation Mode

For the current regulation mode validation, the low-voltage and high-voltage sides of the DC MMC are modeled by two voltage sources to mimic interconnection of two DC grids at different voltage levels. The converter operates at $D = 0.6$ and is controlled to exchange a commanded power between its two DC links. The SPWM strategy in conjunction with the sorting algorithm is adopted to generate the gating signals while maintaining the voltage balance of the SM capacitors within the same arm. The parameters of the PI compensators employed in the controller are summarized in Table 3.2.

The simulated waveforms for the study system in current regulation mode are shown in Fig. 3.7. Initially, the two-phase-leg DC MMC system is in steady state and $I_{\text{dc1}}^{\text{ref}}$ is set to -0.95 kA such that $P = -5$ MW is transferred. As shown in Fig. 3.7(b), at $t = 0.03$ s, I_{dc1} is ramped up from -0.95 kA to +0.95 kA within 20 ms. This change corresponds to a power

Table 3.2: Controller Parameters in the Current Control Mode

Control Parameters	Value
Proportional gain of the current regulator	2
Integral gain of the current regulator	150
Proportional gain of the power balance controller	0.6
Integral gain of the power balance controller	8

flow reversal from -5 MW to 5 MW from DC-link 1 to DC-link 2.

Fig. 3.7(c) illustrates the SM capacitor voltages of both phase legs. The average voltages of the SM capacitor are maintained balanced under steady state. As the DC power command changes, the active AC power of the upper and lower arms required to maintain the SM capacitor voltage balancing also changes. Consequently, subsequent to the power flow reversal command, the average voltages of the SMs in the upper and lower arms diverge from each other . This deviation caused by the sudden change of the DC power flow is quickly mitigated by the arm power balance controller within less than 40 ms as shown in Fig. 3.7(c). It should be noted that the magnitude of the SM capacitor voltage ripple is a function of D. Consequently, the ripple magnitude of the SM capacitor voltages varies as P changes due to the fact that the voltage conversion ratio of the DC MMC is adjusted to accommodate the change in P.

Figs. 3.7(e) and (f) illustrate the reference voltages of the upper and lower arms of phase legs 1 and 2, respectively, in which the actions of the closed-loop controller is demonstrated. The controller performs the following functions:

- The DC components of $v^{p,\text{ref}}$ and $v^{n,\text{ref}}$ are controlled to regulate I_{dc1}. Between $t = 0$ s and $t = 0.03$ s when the converter operates in steady state and $P = -5$ MW, the DC component of $v^{n,\text{ref}}$ is greater than V_{dc1} to facilitate negative power flow. After $t = 0.03$ s when the direction of $I_{\text{dc1}}^{\text{ref}}$ is reversed, the DC component of $v^{n,\text{ref}}$ is reduced to reverse the direction of I_{dc1} as shown in Figs. 3.7(e) and (f). The DC-link currents are well regulated by the closed-loop control strategy as illustrated in Fig. 3.7(b).

- The amplitudes of the AC components of $v^{p,\text{ref}}$ and $v^{n,\text{ref}}$ are maintained at their max-

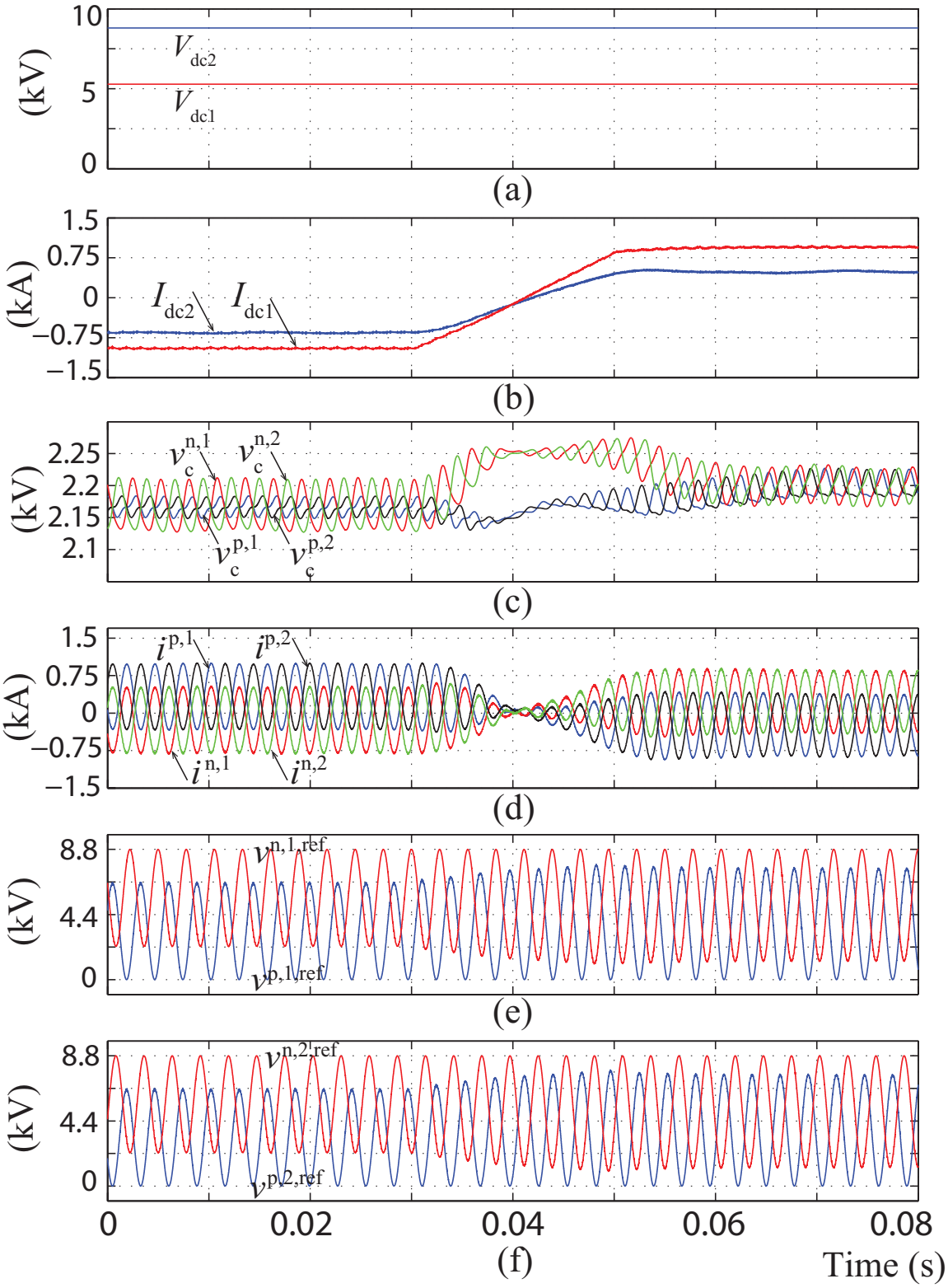


Figure 3.7: Simulated converter waveforms in current regulation mode under power ramp: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) arm voltage reference of phase-leg 2.

imum values. As demonstrated in Figs. 3.7(e) and (f), the peak voltages of the upper arms are maintained at 8.8 kV while the minimum voltage of the lower arms is maintained at 0 V. Consequently, the magnitude of the AC circulating current is minimized. It should be noted that since the amplitudes of the arm voltages are maintained at their maximum values, over-modulation of the arm voltages is avoided regardless of the operating condition of the converter.

- ϕ is controlled to minimize voltage deviation of the SM capacitors in the upper and lower arms. Between $t = 0$ s and $t = 0.03$ s, the AC component of $v^{p,\text{ref}}$ leads that of $v^{n,\text{ref}}$ to facilitate active AC power flow from the upper arm to the lower arm. ϕ is reduced during the transient to accommodate the change of direction of P. As the direction of P is reversed, the active AC power flow between the arms is reversed as well. Once the converter reaches steady state, the AC component of $v^{p,\text{ref}}$ lags that of the $v^{p,\text{ref}}$ to facilitate active AC power flow from the lower arm to the upper arm.

The simulated waveforms of the DC MMC system under power step change is shown in Fig. 3.8. Initially, the two-phase-leg DC MMC system is in steady state $P = -5$ MW is transferred. As shown in Fig. 3.8(b), at $t = 0.01$ s, a step-up change in P from -5 MW to +5 MW occurs. Subsequently, the power balance of the converter is re-established by the controller and the SM capacitor voltages are regulated back to their nominal value. Moreover, the circulating current is maintained at its minimum.

To verify the stability of the proposed control strategy, simulation study for the system when subjected to a disturbance is performed. The simulated waveforms of the DC MMC system are given in Fig. 3.9 where $P = -2.5$ MW is transferred. At $t = 0.1$ s, 5% disturbance in V_{dc1} is initiated. As shown in Fig. 3.9 (a), in 0.01 s after the disturbance, the DC-link currents are regulated back to the reference value by the current regulator. The average voltages of the SM capacitors also experience a transient due to the disturbance. Nevertheless, the power balance controller regulates the average voltage of the SM capacitors back to the nominal value in 0.015 s.

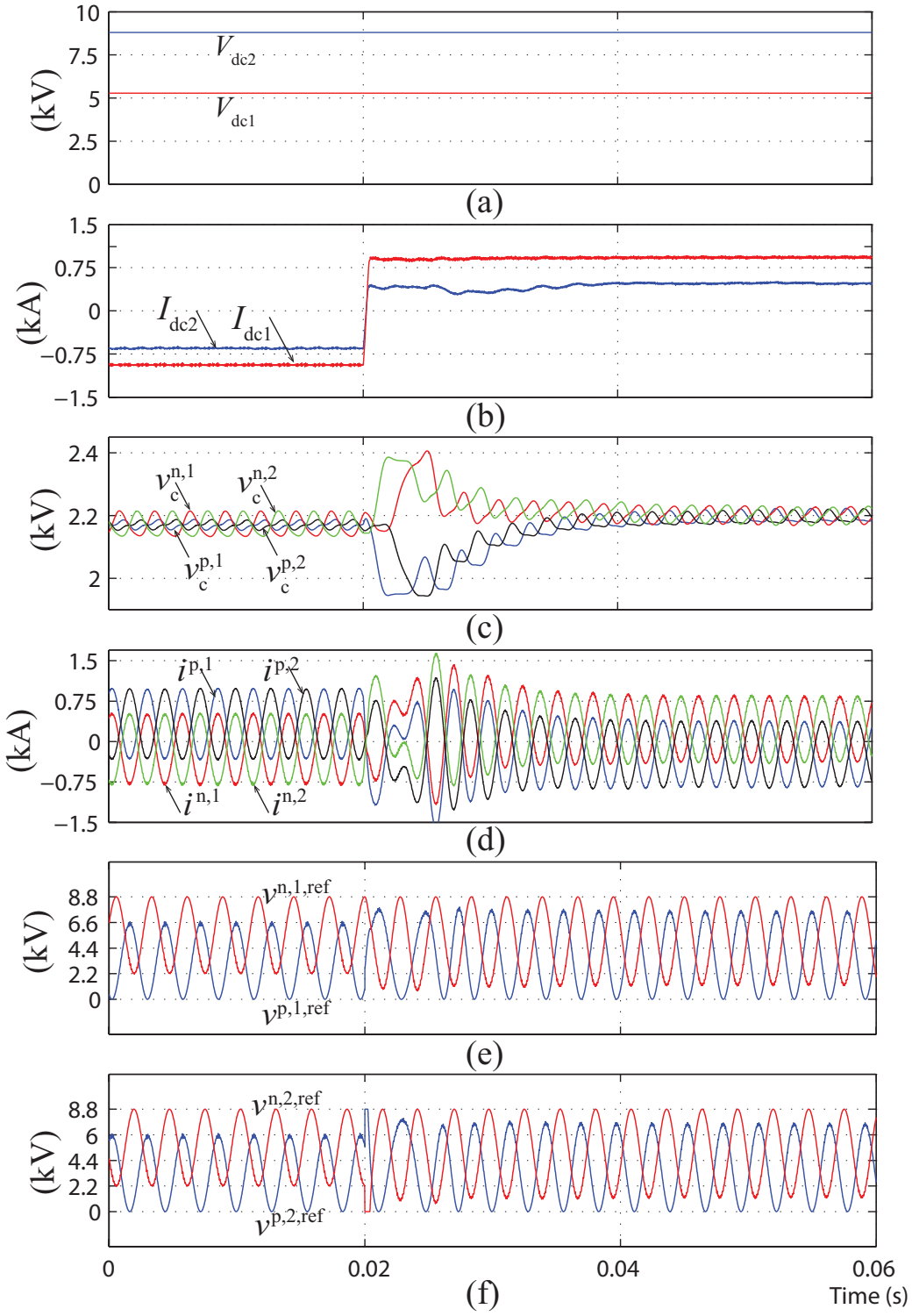


Figure 3.8: Simulated converter waveforms in current regulation mode under power step change: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) arm voltage reference of phase-leg 2.

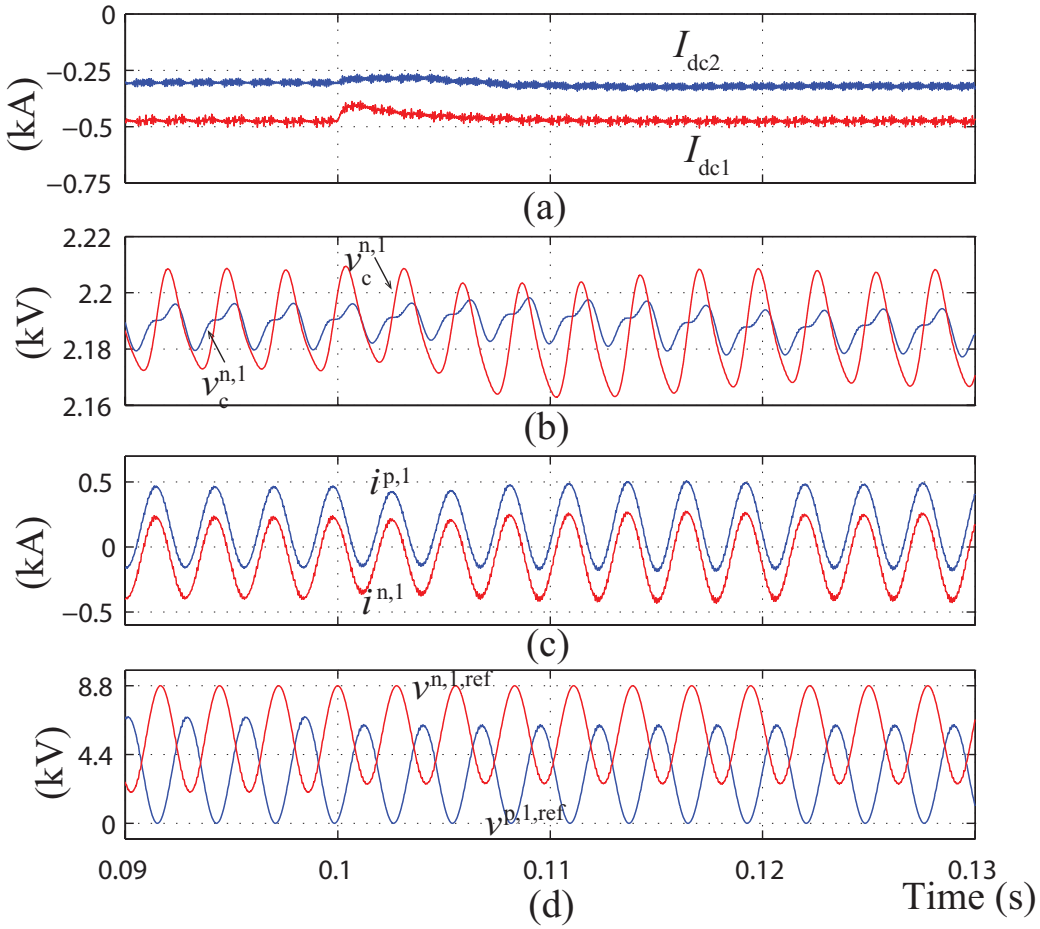


Figure 3.9: Simulated waveforms for 5% disturbance in V_{dc1} initiated at t=0.1 s, where P=-2.5 MW is transferred: (a) DC link 1 and 2 currents, (b) SM capacitor voltages of the upper and lower arms of phase-leg 1, (c) arm currents of phase-leg 1, and (d) arm voltage reference of phase-leg 1.

3.2.2 Case II: Voltage Regulation Mode

To validate the proposed control strategy in voltage regulation mode, a resistive load is connected to the DC-link 1 terminal while a DC voltage source is connected to the DC-link 2 terminal. The simulated waveforms of the DC MMC under the voltage regulation mode control are illustrated in Fig. 3.10. As shown in Fig. 3.10(a), initially, the conversion ratio of the converter is $D = 0.7$, corresponding to 5 MW load power. A DC voltage step-down from $D = 0.7$ to $D = 0.6$ occurs at $t = 0.03$ s. Subsequent to the voltage step change, the SM capacitor voltages become unbalanced. The power balance controller is able to re-establish power balance and to regulate the SM capacitor voltages back to their nominal value quickly as shown in Fig. 3.10(c). The simulation study verifies that the proposed control strategy regulates the DC-link voltage while balancing the SM capacitor voltages.

3.2.3 Case III: Comparative Evaluation of the AC Circulating Current

Steady-state performance of the proposed control strategy is compared with the traditional control strategy in which ϕ^{ref} is maintained at $\frac{3\pi}{2}$ to maximize the power transfer capability and $V_{\text{ac}}^{p,\text{ref}}$ and $V_{\text{ac}}^{n,\text{ref}}$ are controlled to maintain the SM capacitor voltages balanced. Figs. 3.11 and 3.12 present the simulated steady-state waveforms of the DC MMC system using the proposed and the traditional control strategies, respectively. Although both control strategies enable the DC MMC system to transfer -2.5 MW as shown in Figs 3.11(b) and 3.12(b), the proposed control strategy produces much less AC circulating currents as shown in Figs. 3.11(d) and 3.12(d). The proposed control strategy produces 0.26 kA RMS current in the upper arm and 0.24 kA RMS current in the lower arm. In contrast, the traditional control strategy produces 0.55 kA RMS current in the upper arm and 0.52 kA RMS current in the lower arm. Compared to the traditional control strategy, the proposed strategy reduces the arm RMS current by around 50% in this case. In addition, compared to the traditional control strategy, the SM capacitor voltage ripple produced by the proposed control strategy is also smaller, which is due to the reduced AC circulating current.

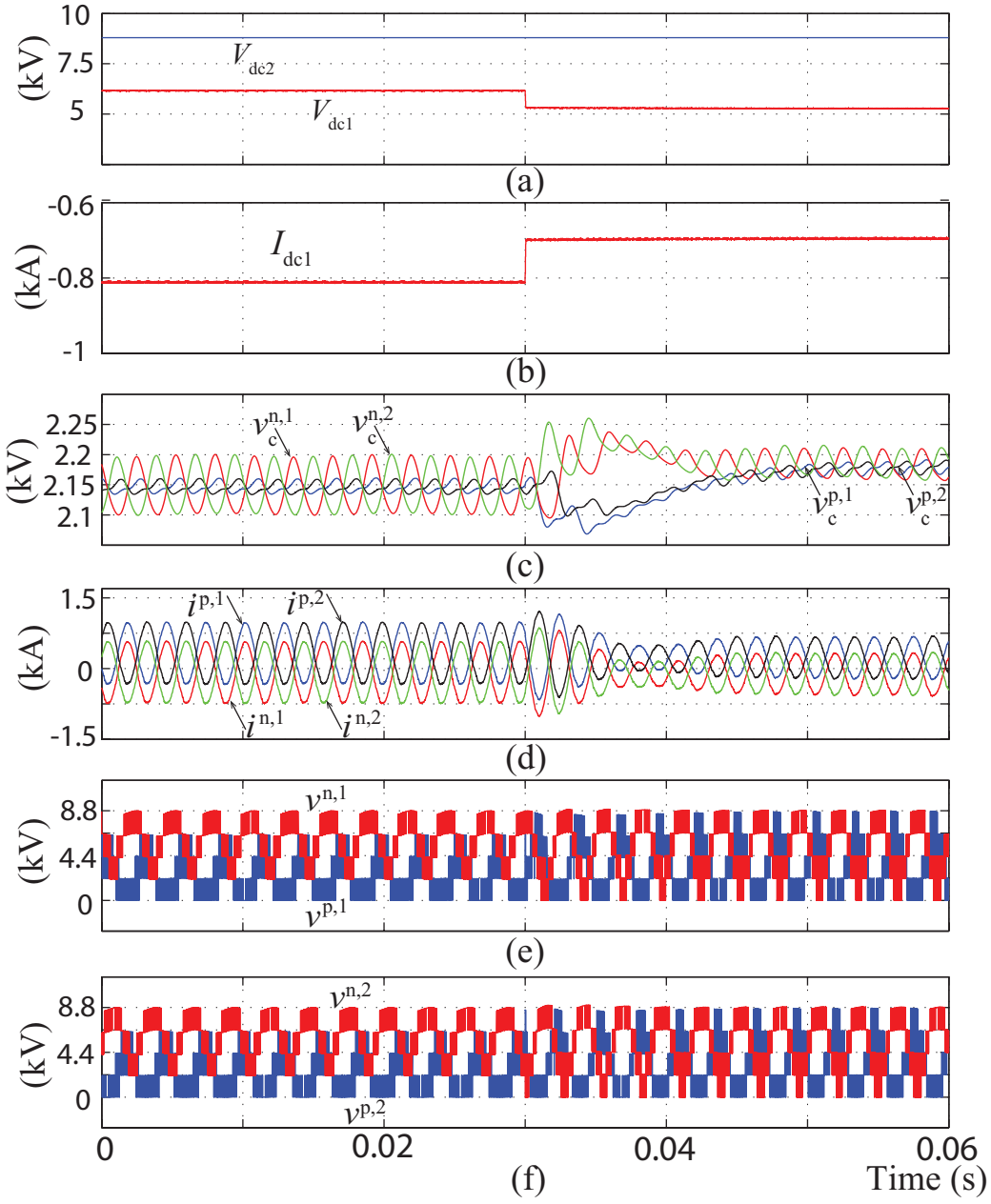


Figure 3.10: Simulated converter waveforms in voltage regulation mode under voltage step change: (a) DC links 1 and 2 voltages, (b) DC links 1 current, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage of phase-leg 1, and (f) arm voltage of phase-leg 2.

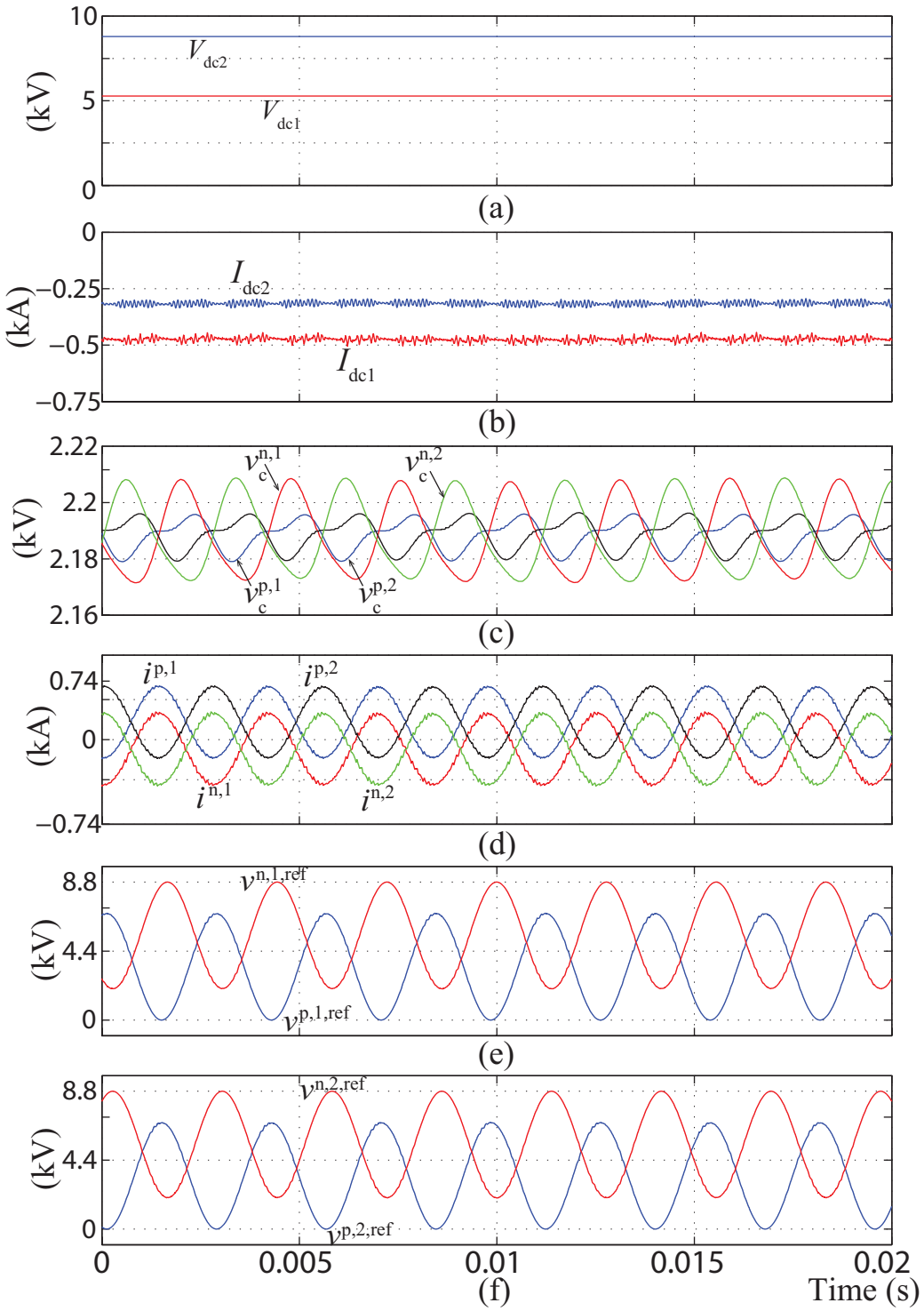


Figure 3.11: Simulated converter waveforms using the proposed control strategy: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) arm voltage reference of phase-leg 2.

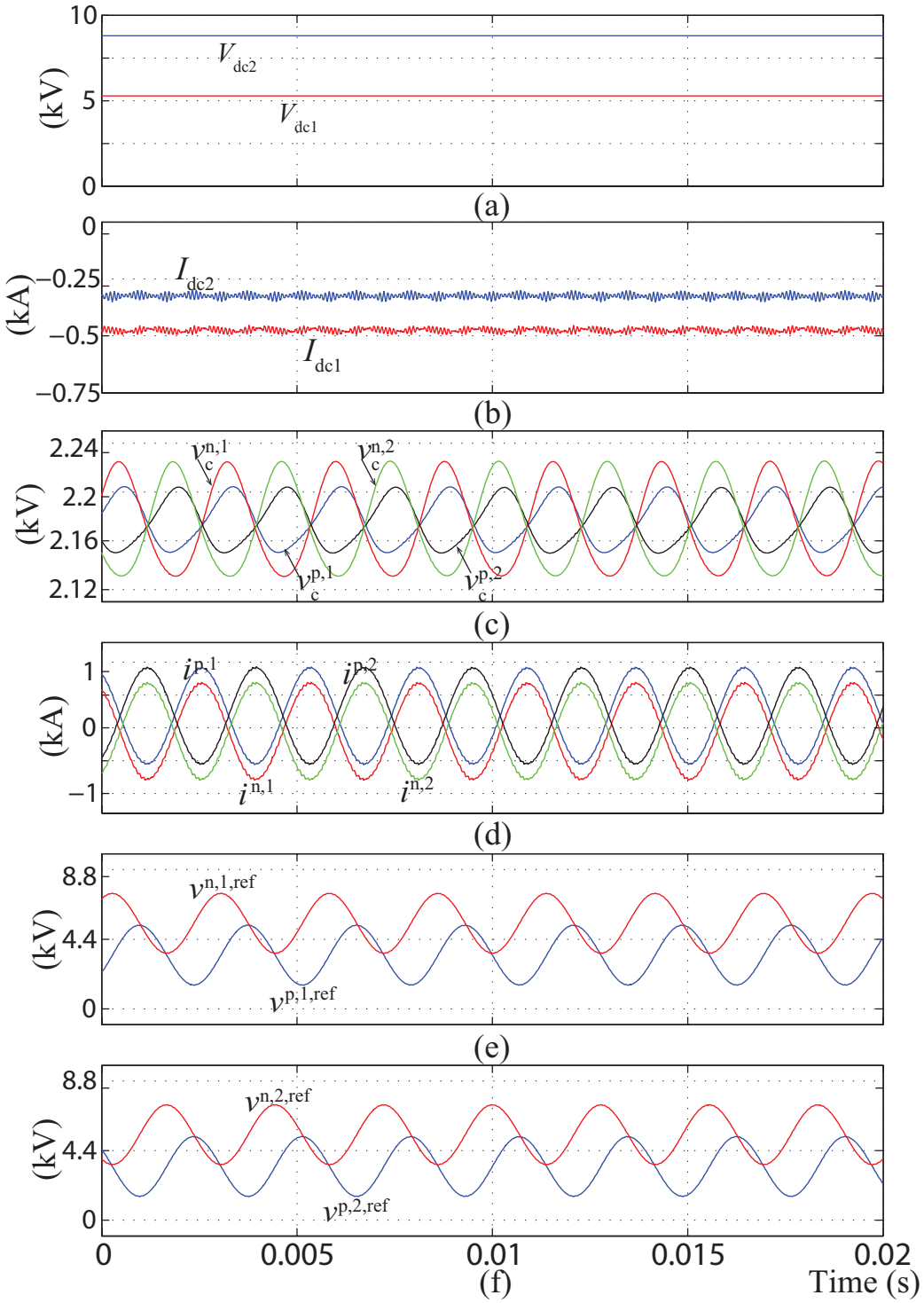


Figure 3.12: Simulated converter waveforms using traditional control strategy: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) arm voltage reference of phase-leg 2.

The reduction in the AC circulating current stems from the fact that the proposed control strategy applies the maximum attainable amplitude of the arm AC voltage, as depicted in Figs. 3.11(e) and (f). In contrast, as shown in Figs. 3.12(e) and (f), since the traditional control strategy maintains ϕ^{ref} at $\frac{3\pi}{2}$, only a portion of the maximum attainable amplitude of the arm AC voltage is utilized.

3.3 Chapter Summary

In this chapter, a closed-loop control strategy for the DC MMC is proposed. The proposed control strategy guarantees proper bidirectional operation of the converter in buck and boost modes of operation. Both the current mode control and voltage mode control are validated simulation studies. Simulation results confirm the capability of the proposed control strategy to simultaneously regulate the DC-link current/voltage, maintain the SM capacitor voltages balanced, and minimize the AC circulating current.

CHAPTER 4

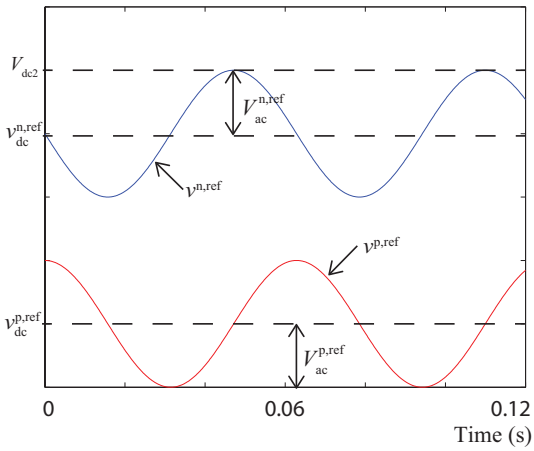
AN ENHANCED CLOSED-LOOP CONTROL STRATEGY WITH CAPACITOR VOLTAGE ELEVATION FOR THE FULL-BRIDGE DC MMC CONFIGURATION

An AC voltage component is generated in each arm to drive an AC circulating current. The available headrooms of the amplitude of the AC voltage components are dictated by the voltage conversion ratio. For a half-bridge SM based DC MMC, the minimum attainable arm voltage is zero. In addition, the SM capacitor voltages are maintained at $\frac{V_{\text{dc2}}}{N}$. Consequently, the maximum attainable arm voltage is V_{dc2}. Therefore, as the voltage conversion ratio approaches to unity or zero, the headroom of the amplitudes of the arm AC voltages diminishes. The power transfer capability and the AC current component of each arm of the DC MMC are closely related to the amplitudes of the AC voltage component in each arm. Hence, the DC MMC experiences a reduced power transfer capability as the voltage conversion ratio deviates from 0.5.

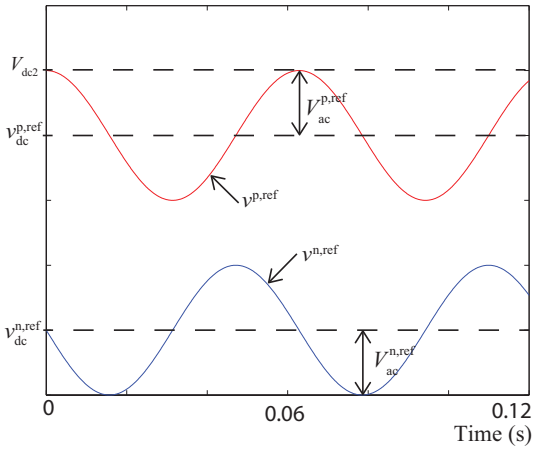
This chapter exploits the full-bridge SMs in the DC MMC to extend the arm AC voltage amplitudes. An enhanced closed-loop control strategy is proposed for the full-bridge SM based DC MMC that utilizes the concept of elevated SM capacitor voltages. Two major advantages are achieved by applying the proposed control strategy: (i) the converter power transfer capability is extended; and (ii) the AC current component and voltage ripple of the SM capacitors of each arm are reduced significantly. Simulation results are presented to validate the performance of the proposed control strategy.

4.1 The Minimum AC Circulating Current and Maximum Converter Power

Fig. 4.1 conceptualizes the relationship between the AC and DC voltage components of the upper and lower arms for $D > 0.5$ and $D < 0.5$. The instantaneous values of the upper and lower arm voltages, v^p and v^n, are restricted by two constraints for the half-bridge SM



(a)



(b)

Figure 4.1: Representative upper and lower arm voltage waveforms of the DC MMC for (a): $D > 0.5$ and (b): $D < 0.5$ (assuming half-bridge SMs)

based DC MMC:

- Constraint I: In traditional control strategies, the average SM capacitor voltage is maintained at $V_{C,nominal} = \frac{V_{dc2}}{N}$, consequently, $v^{p,n} \leq V_{dc2}$ has to be satisfied.

- Constraint II: The half-bridge SMs cannot insert negative voltage. Consequently, $v^{p,n} \geq 0$ need to be satisfied.

Two scenarios are illustrated in Fig. 4.1 for the arm voltages:

- For $D > 0.5$, $V_{ac}^{n,ref}$ is limited by the maximum arm voltage and $V_{ac}^{p,ref}$ is limited by the minimum arm voltage.

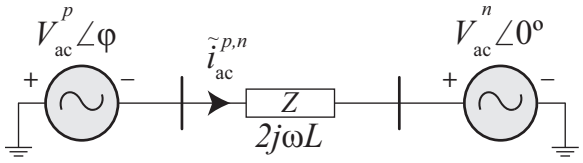


Figure 4.2: AC Equivalent circuit of one phase-leg of the DC MMC.

- For $D > 0.5$, $V_{\text{ac}}^{p,ref}$ is limited by the maximum arm voltage and $V_{\text{ac}}^{n,ref}$ is limited by the minimum arm voltage.

As D approaches to unity or zero, the available headrooms for $V_{\text{ac}}^{p,ref}$ and $V_{\text{ac}}^{n,ref}$ significantly decrease due to the aforementioned constraints for the half-bridge SM based DC MMC. The limitations on v^p and v^n pose two challenges on the operation of the DC MMC for D near unity or zero:

- The minimum value of the AC circulating current is restricted.
- The maximum converter power P decreases as D approaches unity or zero.

In the DC MMC, the phase inductive filter L_0 is designed sufficiently large such that $i_{o,ac}$ is negligible. Based on the single phase equivalent circuit shown in Fig. 2.4, an AC equivalent circuit shown in Fig. 4.2 is derived by neglecting $i_{o,ac}$. The assumption of negligible $i_{o,ac}$ is validated in simulation and experimental results. Since $i_{o,ac}$ is sufficiently small, in the AC equivalent circuit shown in Fig. 4.2, the AC current components of the upper and lower arms are equal. In this chapter, the AC current component of each phase-leg is termed as AC circulating current.

Based on Fig. 4.2, the AC circulating current is represented by:

$$\tilde{i}_{\text{ac}}^{p,n} = -\frac{V_{\text{ac}}^{p}\angle\phi + V_{\text{ac}}^{n}\angle 0^{\circ}}{2\,j\omega L}. \tag{4.1}$$

By expanding (4.1), the AC circulating current is expressed by:

$$\tilde{i}_{\text{ac}}^{p,n} = \frac{j[V_{\text{ac}}^{p}cos(\phi) + V_{\text{ac}}^{n}] - V_{\text{ac}}^{p}sin(\phi)}{2\omega L}. \tag{4.2}$$

The amplitude of the AC circulating current is expressed by:

$$I_{\text{ac}}^{p,n} = \frac{1}{2\omega L}\sqrt{(V_{\text{ac}}^{p})^2 + (V_{\text{ac}}^{n})^2 + 2V_{\text{ac}}^{p}V_{\text{ac}}^{n}cos(\phi)}. \tag{4.3}$$

Equation (4.3) is rearranged to:

$$I_{\text{ac}}^{p,n} = \frac{1}{2\omega L}\sqrt{(V_{\text{ac}}^{p} - V_{\text{ac}}^{n})^2 + 2V_{\text{ac}}^{p}V_{\text{ac}}^{n}(1 + cos(\phi))}. \tag{4.4}$$

Assuming $P > 0$, the active AC power delivered to the lower arm to maintain the SM capacitors energy balance is expressed by:

$$P_{\text{ac}}^{p} = \frac{1}{2\omega L}V_{\text{ac}}^{p}V_{\text{ac}}^{n}sin(\phi). \tag{4.5}$$

As discussed in Chapter 3, P_{ac}^{p} and P_{ac}^{p} need to be actively controlled to track the arm DC power determined by (2.11). Therefore, in steady state, P_{ac}^{p} and P_{ac}^{p} are fixed for a given set of P, D and V_{dc2}. As shown in (4.4), the magnitude of the AC circulating current contains a quadratic term and a cross-product term. Once P_{ac}^{p} and P_{ac}^{n} are determined, the cross-product term is fixed for a given ϕ. Therefore, minimizing $I_{\text{ac}}^{p,n}$ necessities the elimination of the quadratic term. Consequently, the first necessary condition for minimizing the AC circulating current is derived as:

$$V_{\text{ac}}^{p} = V_{\text{ac}}^{n}. \tag{4.6}$$

Based on the analysis presented in Chapter 3, the second necessary condition of minimizing AC circulating current is derived as:

$$\phi \in \begin{cases} [\frac{\pi}{2}, \pi); P > 0 \\ (\pi, \frac{3\pi}{2}]; P < 0 \end{cases} \tag{4.7}$$

Assuming (4.6) is satisfied, (4.4) and (4.5) can be rewritten as:

$$I_{\text{ac}}^{p,n} = \frac{1}{2\omega L}\sqrt{(2V_{\text{ac}}^{p,n})^2(1+cos(\phi))}, \tag{4.8}$$

$$P_{\text{ac}}^{p} = \frac{1}{2}(V_{\text{ac}}^{p,n})^2 sin(\phi). \tag{4.9}$$

As ϕ approaches to π, $I_{\text{ac}}^{p,n}$ approaches to zero. However, a greater $V_{\text{ac}}^{p,n}$ is required to maintain $P_{\text{ac}}^{p,n}$ at a constant. Consequently, the minimum AC circulating current is attained when the maximum $V_{\text{ac}}^{p,n}$ is applied. For the half-bridge SM based DC MMC, the maximum $V_{\text{ac}}^{p,n}$ is determined by (3.1) and (3.2). To further reduce the AC circulating current, $V_{\text{ac}}^{p,n}$ should be increased beyond its constraints.

In addition to the AC circulating current, the maximum converter power is also coupled with V_{ac}^{p} and V_{ac}^{n}. Assuming L_{o} is sufficiently large, the maximum converter power is attained at $\phi = \frac{\pi}{2}$:

$$P_{\text{max}} = \frac{M}{2\omega L(1-D)} V_{\text{ac}}^{p} V_{\text{ac}}^{n}, \tag{4.10}$$

where P_{max} represents the maximum converter power.

Fig. 4.3 illustrates the impact of D on the maximum converter power for a half-bridge SM based DC MMC. As shown in the figure, the power transfer capability of the DC MMC with half-bridge SM is peaked at $D = 0.5$. As D deviates from 0.5, the power transfer capability is decreased dramatically due to the diminished V_{ac}^{p} and V_{ac}^{n}. It should be noted that the maximum converter power reduces faster as D approaching zero compared to D approaches unity. At $D = 0.1$, P_{max} is decreased to less than 10% of the rated converter power. In DC grid applications, it is desired to maintain the power transfer capability of the converter constant over the entire operating range of the converter. As shown in (4.10), to increase P_{max} for a given D, V_{ac}^{p} and V_{ac}^{n} must be increased beyond their limits.

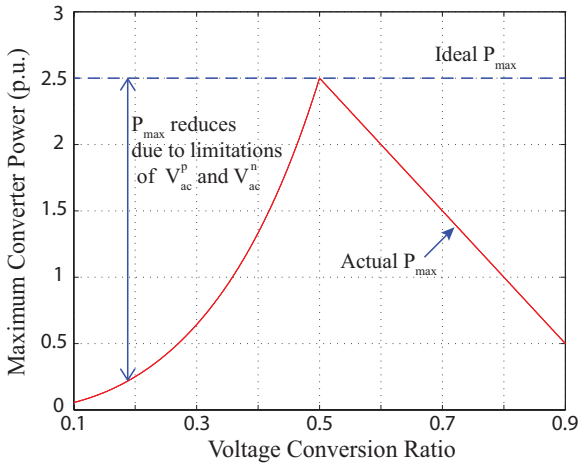


Figure 4.3: Maximum converter power versus voltage conversion ratio for the half-bridge SM based DC MMC.

4.2 The Proposed Control Strategy

Due to Constraint II of the arm voltage, the minimum arm voltage is limited to zero. To further increase V_{ac}^{p} and V_{ac}^{n}, a negative voltage needs to be inserted. Consequently, full-bridge SMs are employed to extend the range of V_{ac}^{p} and V_{ac}^{n} beyond their limits at zero. The minimum arm voltage for full-bridge SM based DC MMC is expressed by:

$$v_{\text{min}}^{p} = -N_{\text{FB}}^{p} V_{\text{C}}^{p}, \tag{4.11a}$$

$$v_{\text{min}}^{n} = -N_{\text{FB}}^{n} V_{\text{C}}^{n}, \tag{4.11b}$$

where N_{FB}^{p} and N_{FB}^{p} represent the number of full-bridge SMs in the upper and lower arms, and V_{C}^{p} and V_{C}^{n} represent the average SM capacitor voltages of the upper and lower arms, respectively. The number of full-bridge SMs to be used in each arm is a design/optimization problem. A higher ratio of full-bridge SM used in each arm produces a smaller $v_{\text{ac,min}}^{p}$ and/or $v_{\text{ac,min}}^{n}$. However, higher power losses and cost are incurred since the full-bridge SM contains four active switches. In general, if the converter is designed to operate above $D = 0.5$, the full-bridge SMs are needed for the upper arm to extend the range of V_{ac}^{p}, which is limited by the minimum arm voltage. Similarly, if the converter is designed to operate below $D = 0.5$, full-bridge SMs are need for the lower arm to extend the range of V_{ac}^{n}. In

this chapter, it is assumed that $N^p_{\mathrm{FB}} = N^n_{\mathrm{FB}} = N$ is used in each arm.

The use of full-bridge SMs extends $v^p_{\min}$ and $v^n_{\min}$ due to Constraint II of the arm voltage. However, extending only the minimum arm voltages results in an unequal V^p_{ac} and V^n_{ac}, which leads to a significant increased AC circulating current as shown in (4.4). To satisfy (4.6), the maximum arm voltages also need to be increased. The maximum voltage of each arm is expressed by:

$$v^p_{\max} = NV^p_{\mathrm{C}}, \tag{4.12a}$$

$$v^n_{\max} = NV^n_{\mathrm{C}}. \tag{4.12b}$$

As shown in (4.12), since the number of SM is fixed, V^p_{C} and V^n_{C} need to be elevated to increase $V^p_{\mathrm{ac,max}}$ and $V^n_{\mathrm{ac,max}}$. In the DC MMC, an infinite number of stable operating points exists. It is not necessary to maintain $V^{p,n}_C$ at $V_{C,nomimal}$. Therefore, the average value of SM capacitor voltages of the upper and lower arms can be regulated at arbitrary values if the power balance constrain of (2.18) is satisfied.

Consequently, the maximum arm voltage can be extended by elevating the average SM capacitor voltage of the upper and lower arms. Elevation coefficients are introduced as:

$$\zeta^p = \frac{V^p_C}{V_{C,nomial}}, \tag{4.13a}$$

$$\zeta^n = \frac{V^n_C}{V_{C,nomial}}, \tag{4.13b}$$

where $V_{C,nomial} = \frac{V_{\mathrm{dc2}}}{N}$. The maximum arm voltage is then expressed as:

$$v^p_{\max} = \zeta^p NV_{C,nomial}, \tag{4.14a}$$

$$v^n_{\max} = \zeta^n NV_{C,nomial}. \tag{4.14b}$$

It should be noted that V^p_C and V^n_C not necessarily need to be equal. The elevation coefficients of the upper and lower arms can be chosen at different values for converter optimization. In this chapter, for the sake of simplicity, $\zeta^p = \zeta^n = \zeta$ is assumed.

The elevated SM capacitor voltage effectively extends the headrooms of the arm volt-

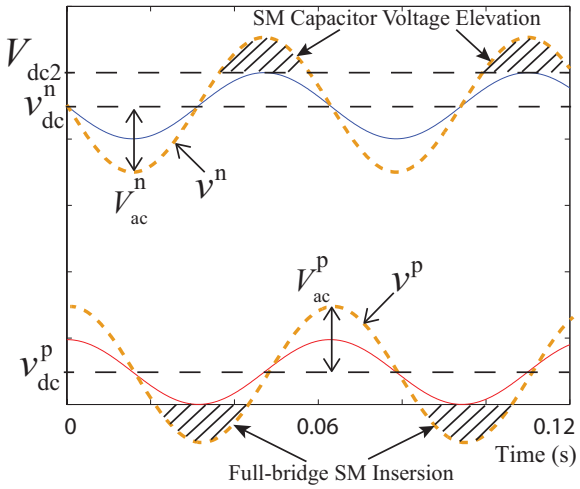


Figure 4.4: Representative waveforms of the arm voltages (solid line: the half-bridge SM based practice; dashed line: the proposed solution).

ages. Fig. 4.4 illustrates the representative waveforms of the arm voltages using the proposed solution and the standard half-bridge SM based practice. By employing full-bridge SMs in conjunction with the elevation of SM capacitor voltage of the upper and lower arms, the AC voltage amplitudes of both arms can be extended equally such that (4.6) is satisfied. The maximum amplitudes of the AC voltage component of the upper and lower arms with SM capacitor voltage elevation are expressed as:

$$V^{p,n}_{\text{ac,max}} = \begin{cases} \min[(\zeta^n N V_{C,nomial} - v^n_{\text{dc}}), (v^p_{\text{dc}} + \zeta^p N^p_{\text{FB}} V_{C,nomial})]; D \geq 0.5 \\ \min[(\zeta^p N V_{C,nomial} - v^p_{\text{dc}}), (v^n_{\text{dc}} + \zeta^n N^n_{\text{FB}} V_{C,nomial})]; D \leq 0.5 \end{cases} \tag{4.15}$$

Fig. 4.5 illustrates the impact of the elevation coefficient on the the maximum converter power of the DC MMC at various D for the full-bridge SM based DC MMC. As shown in Fig. 4.5, the converter power is increased significantly with the elevation of SM capacitor voltage. The effects of the SM capacitor voltage elevation is more significant for $D > 0.5$. A 10% increment of $V^{p,n}_C$ translates to approximately 300% of P_{max} increasing at $D = 0.9$. The maximum converter power is elevated above 1 p.u. for $D \in [0.2, 0.9]$ with a 20% elevation of the average SM capacitor voltages.

Fig. 4.6 illustrates the impact of the elevation coefficient on the AC circulating current at

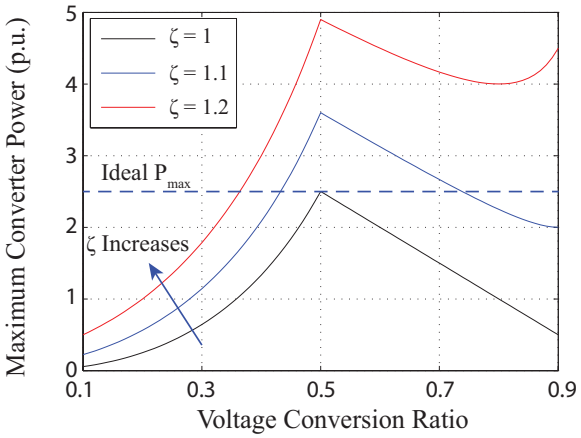


Figure 4.5: Normalized maximum converter power versus voltage conversion ratio for the full-bridge based DC MMC with SM capacitor voltage elevation.

$D = 0.2$ for the full-bridge SM based DC MMC. In Fig. 4.6, it is assumed that $V_{\text{ac}}^{p,n}$=$V_{\text{ac,max}}^{p,n}$ determined by (4.14) is applied to minimize the AC circulating current. For $\zeta = 1$, $V_{\text{ac}}^{p,n}$ is limited to 0.2 p.u. at $D = 0.2$. Consequently, the minimum AC circulating current is restricted to 2.1 p.u. when the maximum $V_{\text{ac}}^{p,n}$ is applied. To further reduce the AC circulating current, ζ is increased to extend the range of $V_{\text{ac}}^{p,n}$. As shown in the figure, a 20% elevation of $V_C^{p,n}$ results in approximately 50% reduction of the AC circulating current. The significant reduction of the AC circulating current directly translates to reduced power losses of the converter.

4.3 The Realization of the Proposed Control Strategy

The modulation signals for the upper and lower arms of each phase-leg are expressed by:

$$v^{p,\text{ref}} = v_{\text{dc}}^{p,\text{ref}} + V_{\text{ac}}^{p,\text{ref}} cos(\omega t + \phi^{\text{ref}}), \tag{4.16}$$

$$v^{n,\text{ref}} = v_{\text{dc}}^{n,\text{ref}} + V_{\text{ac}}^{n,\text{ref}} cos(\omega t). \tag{4.17}$$

Fig. 4.7 shows the overall block diagram of the proposed control strategy in current regulation mode that consists of a phase current regulator combined with an arm power balance controller. $V_{\text{ac,max}}^{p,\text{ref}}$ and $V_{\text{ac,max}}^{n,\text{ref}}$ are functions of ζ, D, and V_{dc2} and can be determined

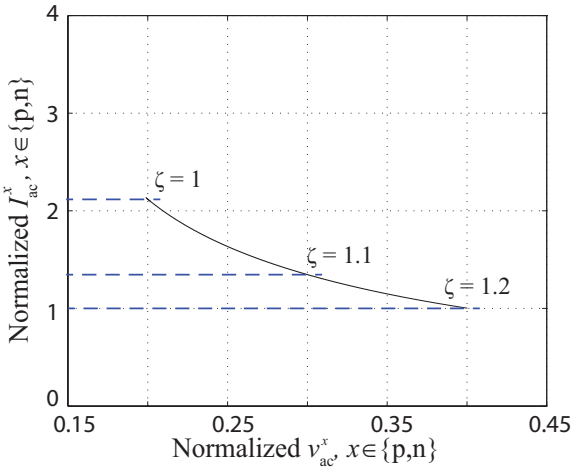


Figure 4.6: Normalized amplitude of the AC circulating current versus normalized arm voltages at $D = 0.2$ for the full-bridge based DC MMC with SM capacitor voltage elevation.

by (4.14). To minimize the AC circulating current, $V_{\text{ac}}^{p,\text{ref}} = V_{\text{ac}}^{n,\text{ref}} = V_{\text{ac,max}}^{p,n}$ are enforced by the control strategy.

To regulate the phase/DC-link current at its reference value, the DC link current regulator employs a Proportional-Integral (PI) compensator that acts on the difference between the reference and measured i_o generating $v_{\text{dc}}^{n,\text{ref}}$ to facilitate bidirectional DC power transfer. As shown in Fig. 4.7, the arm power balance controller maintains the power balance between the upper and lower arms such that the deviation of the average SM capacitor voltages is zero. The elevation coefficient is applied to the modulator to regulate the average SM capacitor voltages of the upper and lower arms. It should be noted that maintaining the energy balance of the SM capacitor voltages does not necessarily requires a zero difference of the average SM capacitor voltage between the upper and lower arms. The energy balance of the SM capacitors is maintained as long as the difference of the average SM capacitor voltages of the upper and lower arm remains constant and P is regulated. For $\zeta^p \neq \zeta^n$, a non-zero value of the difference of the SM capacitor voltages between the upper and lower arms are required for proper operation of the DC MMC.

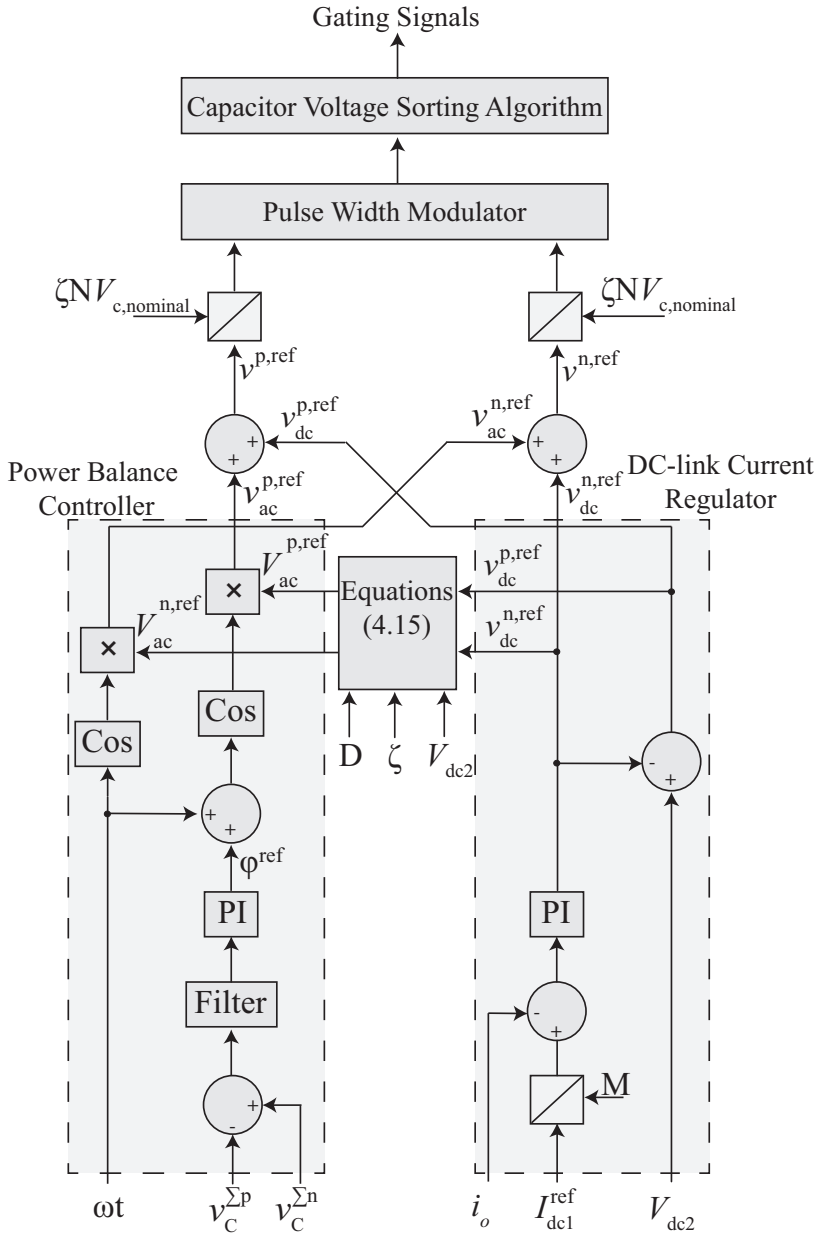


Figure 4.7: The overall control block diagram of the proposed elevated SM capacitor voltage control strategy.

4.4 Simulation Study

To demonstrate the performance and effectiveness of the proposed control strategy using elevated SM capacitor voltages, a switched model of a two-phase-leg DC MMC of Fig. 2.2 using full-bridge SMs is constructed in Matlab Simulink. It should be noted that in the simulation studies presented in this section, full-bridge SMs are installed in both the upper and lower arm to simulate cases for both $D > 0.5$ and $D < 0.5$. In practice, selection of the number of full-bridge SMs should be based on the intended operating conditions and the design optimizations. The low-voltage and high-voltage sides of the DC MMC are modeled by two voltage sources to mimic interconnection of two DC grids at different voltage levels and a current regulation strategy is employed.

The converter parameters of the study system are listed in Table 4.1. Four cases are presented to:

- Demonstrate the performance of the proposed control strategy in terms of regulating converter power and maintaining the SM capacitor energy balance.
- Demonstrate the capability of the proposed control strategy in reducing the AC circulating current and SM capacitor voltage ripple by providing comparative evaluations.
- Demonstrate the capability of the proposed control strategy in extending power transfer capability of the DC MMC.

Table 4.1: Converter Parameters

Converter Parameters	**Value**
Number of phase legs, M	2
Number of SMs per arm, N	4
SM capacitor, C_{SM}	4.2 mF
Arm inductor, L	0.6 mH
Phase filtering inductor, L_{o}	260 mH
Operating frequency, ω	360 Hz
DC-link 2 voltage, V_{dc2}	8 kV

4.4.1 Case I: Steady-state Operation at $D = 0.2$

The first case presents steady-state operation of the full-bridge SM based DC MMC using the proposed elevated SM capacitor voltage control strategy at $D = 0.2$. The simulated waveforms are compared with that of the DC MMC using half-bridge SMs and the control strategy proposed in Chapter 3. The operating condition of the DC MMC is shown in Table 4.2.

Table 4.2: Operating Condition for the Half-bridge SM Based DC MMC at D=0.2

Operating Condition	**Value**
Power throughput, P	1.1 MW
Voltage conversion ratio, D	0.2

Fig. 4.8 presents the simulated converter waveforms of the DC MMC in steady state at $D = 0.2$. As shown in Fig. 4.8(a), V_{dc1} is maintained at 1.6 kV and $P = 1.1$ MW of power is transfered. The average SM capacitor voltages of the upper and lower arms are regulated at 2 kV as shown in Fig. 4.8(b). Since half-bridge SMs are utilized, the minimum arm voltages are restricted to zero and the maximum arm voltages are restricted to V_{dc2}. As shown in Figs. 4.8(e) and (f), the maximum attainable V_{ac}^{p} and V_{ac}^{n} are applied to minimize the AC circulating current.

The simulated converter waveforms of the DC MMC using full-bridge SMs in conjunction with the elevated SM capacitor voltage control strategy are illustrated in Fig. 4.9. The operating condition of the DC MMC is given in Table 4.3.

Table 4.3: Operating Condition for the Full-bridge SM Based DC MMC at D=0.2

Operating Condition	**Value**
Power throughput, P	1.1 MW
Voltage conversion ratio, D	0.2
Elevation coefficient, ζ	1.2

In the simulation, V_{dc1} is maintained at 1.6 kV and $P = 1.1$ MW of power is transfered. $\zeta = 1.2$ is adopted and $V_{\text{ac}}^{p,n,\text{ref}} = V_{\text{ac,max}}^{p,n}$ determined by (4.14) is applied to the converter.

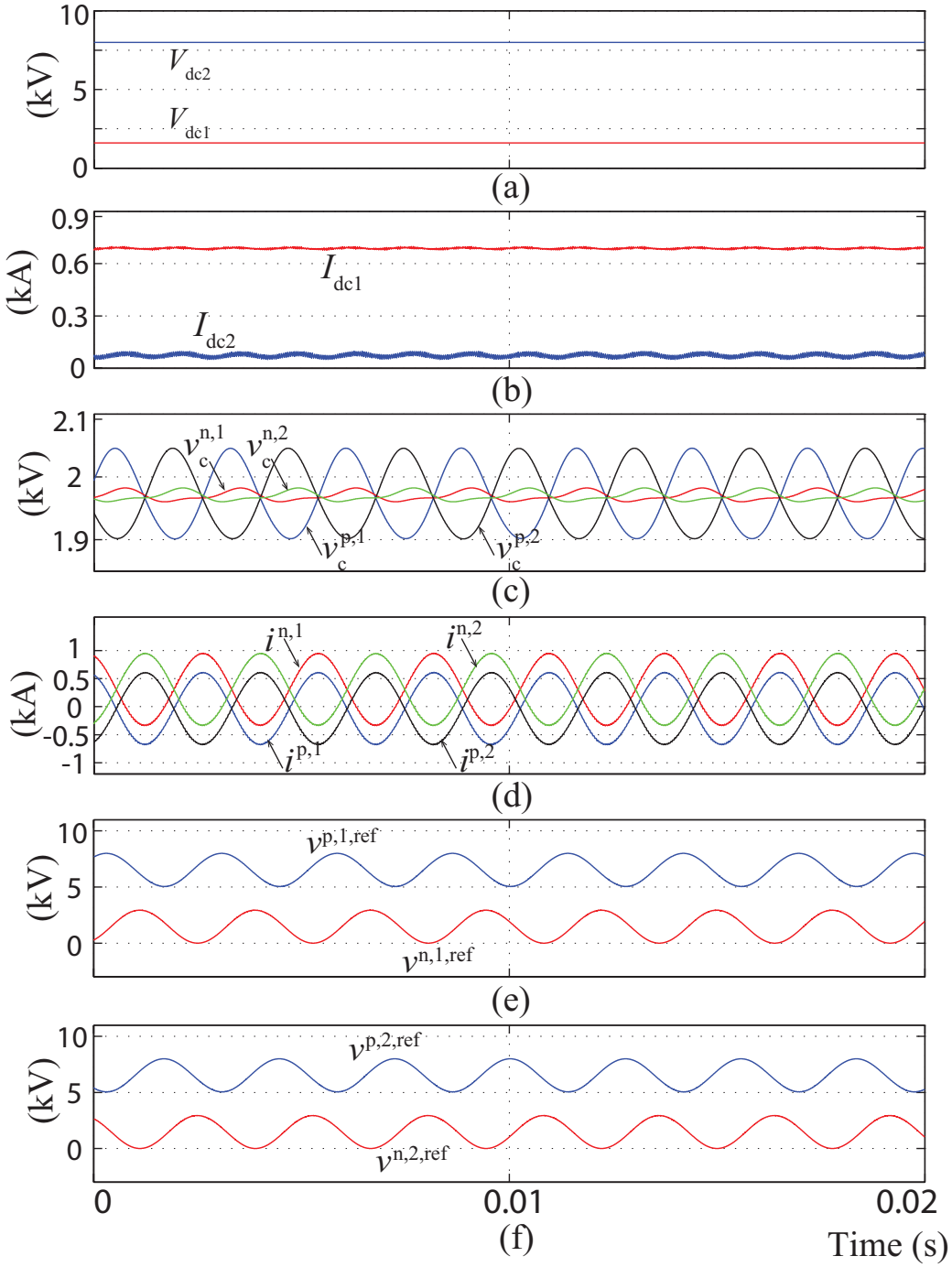


Figure 4.8: Simulated converter waveforms using the half-bridge SMs at $D = 0.2$: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) arm voltage reference of phase-leg 2.

The average SM capacitor voltages of the upper and lower arms are regulated at 2.4 kV as shown in Fig. 4.9(c). Due to the elevation of the SM capacitor voltages, $v^{p,\text{ref}}$ is raised above V_{dc2} and $v^{n,\text{ref}}$ is below zero as shown in Figs. 4.9(e) and (f). The AC circulating current shown in Fig. 4.9(e) is significantly less than that shown in Fig. 4.8(e). The comparison of the AC circulating current and SM capacitor voltage ripple between the half-bridge and full-bridge based DC MMC are summarized in Table 4.4. The full-bridge based DC MMCs with a 20% elevation of $V_C^{p,n}$ produces 55% less AC circulating current compared to the half-bridge SM based DC MMC. In addition, the SM capacitor voltage ripple of the upper and lower arms are also reduced in the full-bridge based DC MMC using the proposed control strategy. As shown in Table 4.4, 65% and 26% reduction of the SM capacitor voltage ripple are achieved in the upper and lower arms, respectively.

Table 4.4: Comparative Evaluation of the DC MMC at $D = 0.2$

	Half-bridge DC MMC	**Full-bridge DC MMC**
Upper arm SM capacitor voltage	145 V	50 V
Lower arm SM capacitor voltage	23 V	17 V
Amplitude of AC circulating current	1.3 kA	0.58 kA

4.4.2 Case II: Steady-state Operation at $D = 0.8$

Case II presents the comparative evaluation between the half-bridge and the full-bridge SM based DC MMCs using the proposed control strategy. The operating condition of the half-bridge and full-bridge based converters are listed in Table 4.5 and 4.6. In the simulation presented in this case, V_{dc2} is maintained at 6.4 kV and $P = 3.5$ MW is transfered. The simulated steady-state waveforms of the half-bridge and the full-bridge SM based DC MMCs are presented in Fig. 4.10 and Fig. 4.11, respectively. In the full-bridge SM based DC MMC, $\zeta = 1.2$ is used. As shown in Figs. 4.11(e) and (f), $v^{n,\text{ref}}$ is greater than V_{dc2} whereas $v^{n,\text{ref}}$ is less than zero for $D = 0.8$.

Table 4.7 illustrates the performance comparison between the half-bridge and the full-bridge SM based DC MMCs. As shown in the table, 20% elevation of the average SM

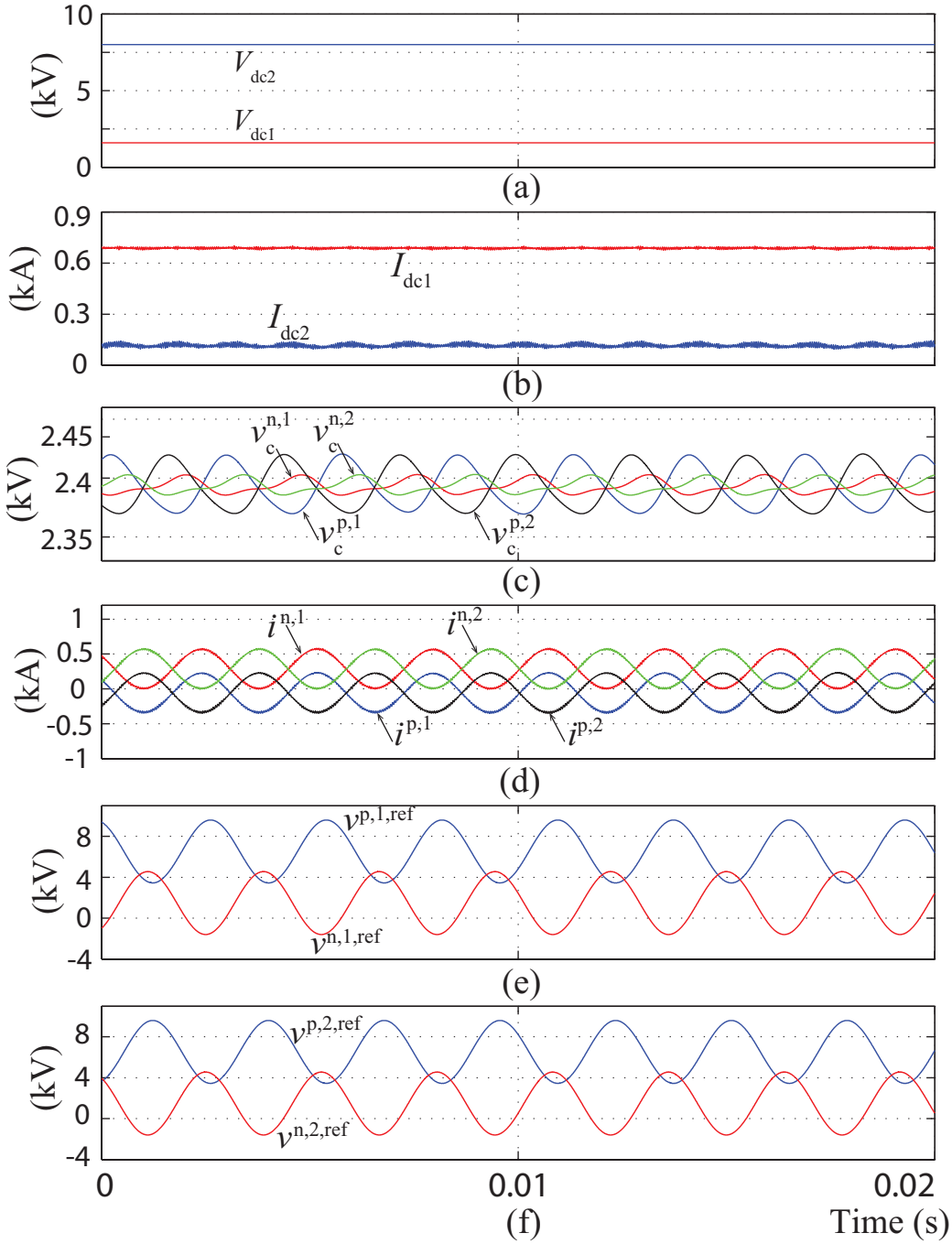


Figure 4.9: Simulated converter waveforms using the proposed control strategy with the full-bridge SMs at $D = 0.2$: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) arm voltage reference of phase-leg 2.

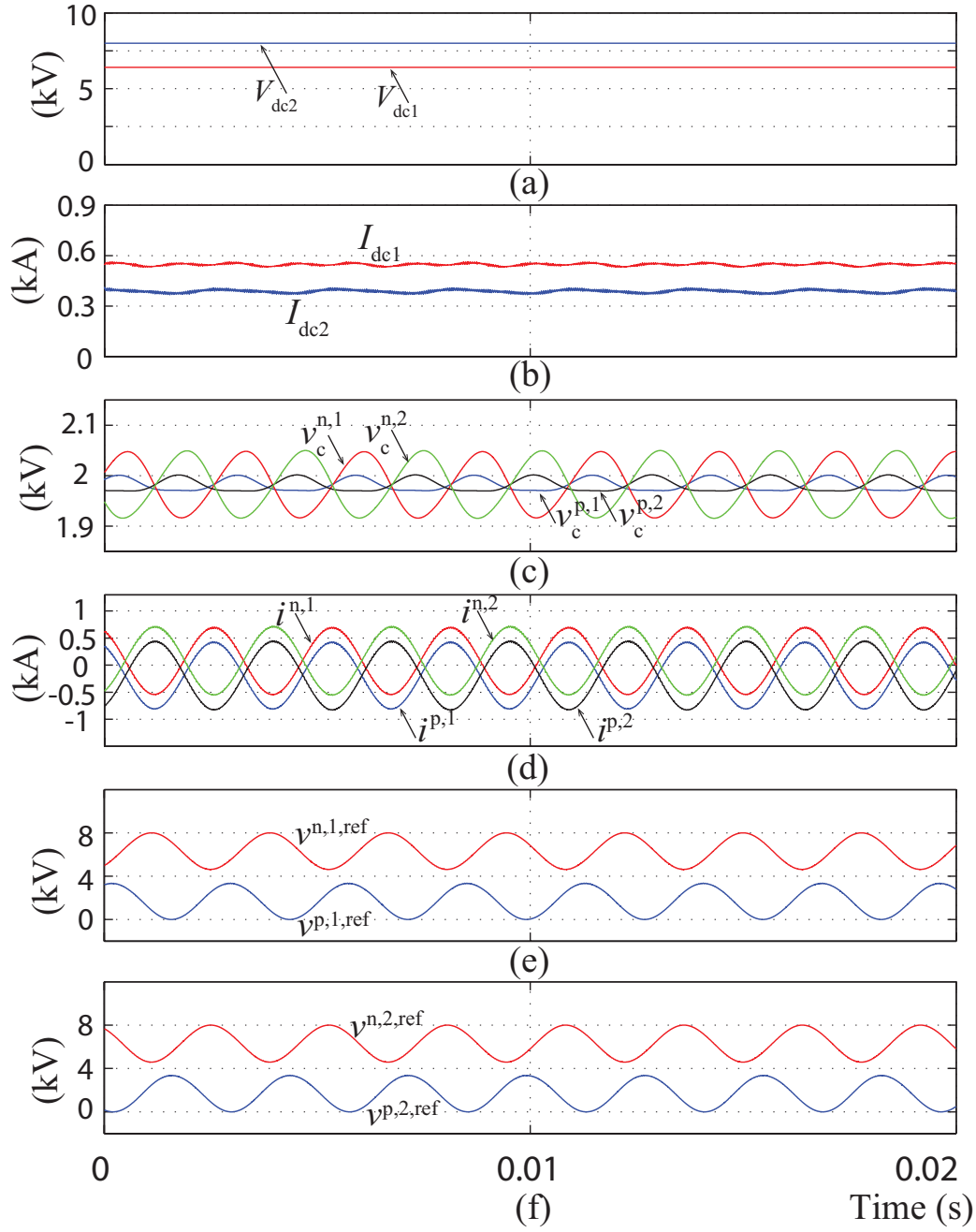


Figure 4.10: Simulated converter waveforms using the half-bridge SMs at $D = 0.8$: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) arm voltage reference of phase-leg 2.

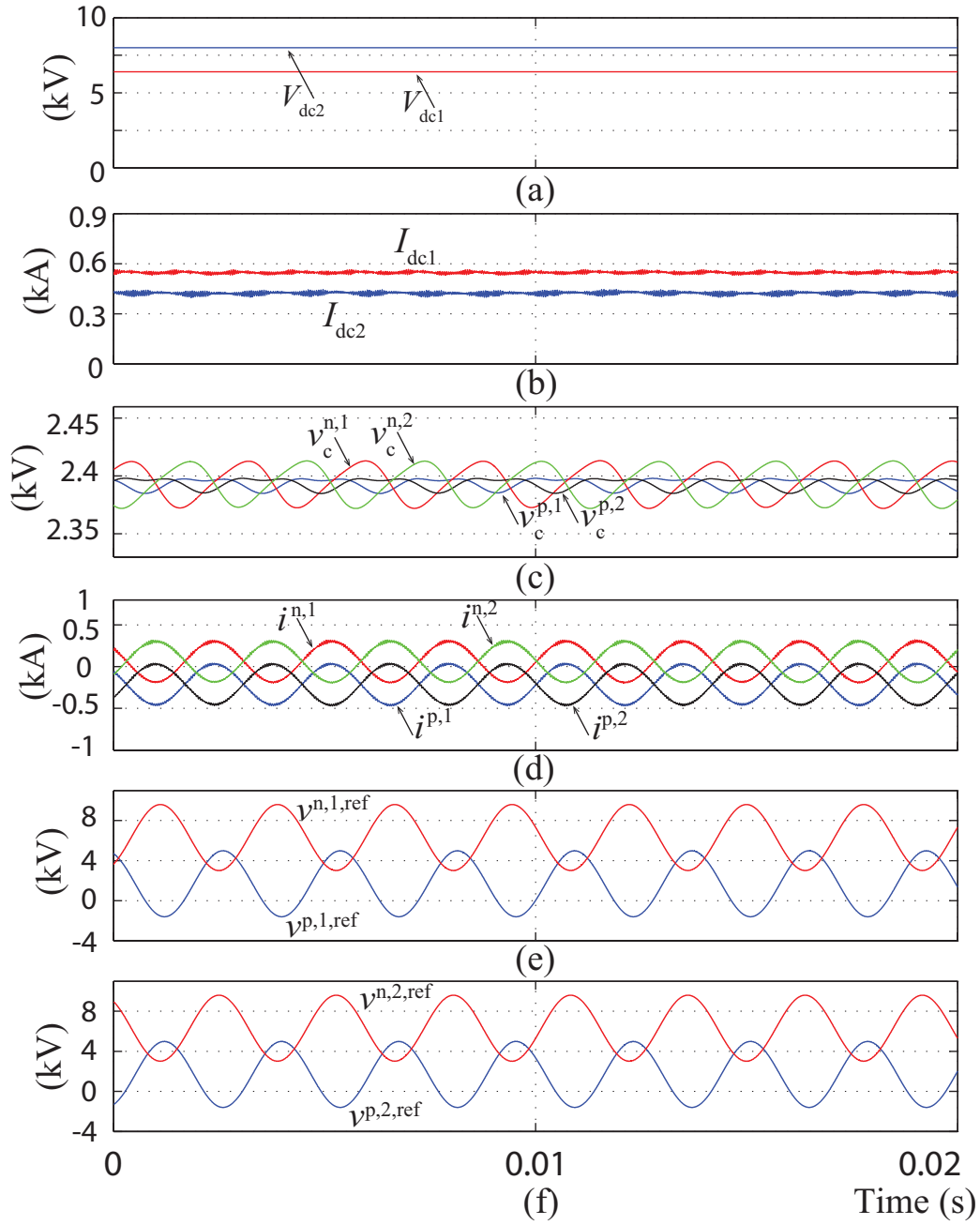


Figure 4.11: Simulated converter waveforms using the proposed control strategy with the full-bridge SMs at $D = 0.8$: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) arm voltage reference of phase-leg 2.

Table 4.5: Operating Condition for the Half-bridge SM Based DC MMC at D=0.8

Operating Condition	**Value**
Power throughput, P	3.5 MW
Voltage conversion ratio, D	0.2

Table 4.6: Operating Condition for the Full-bridge SM Based DC MMC at D=0.8

Operating Condition	**Value**
Power throughput, P	3.5 MW
Voltage conversion ratio, D	0.2
Elevation coefficient, ζ	1.2

capacitor voltages translates to 56% reduction in the AC circulating current, 53% reduction in the upper arm capacitor voltage ripple, and 61% reduction in the lower arm capacitor voltage ripple.

Table 4.7: Comparative Evaluation of the DC MMC at $D = 0.8$

	Half-bridge DC MMC	**Full-bridge DC MMC**
Upper arm SM capacitor voltage	30 V	14 V
Lower arm SM capacitor voltage	130 V	50 V
Amplitude of AC circulating current	1.25 kA	0.54 kA

4.4.3 Case III: Dynamic Response at $D = 0.8$

Case III is designed to validate the proposed control strategy dynamically by applying a power step change. In the simulation, $\zeta = 1.2$ is applied. Initially, the two-phase-leg DC MMC system is in steady state and $I_{\mathrm{dc1}}^{\mathrm{ref}}$ is set to +0.55 kA such that $P = +3.5$ MW is transferred. As shown in Fig. 4.12(b), at $t = 0.05$ s, I_{dc1} is stepped down from +0.55 kA to -0.55 kA. This change corresponds to a power flow reversal from +3.5 MW to -3.5 MW from DC-link 1 to DC-link 2.

Fig. 4.12(c) illustrates the SM capacitor voltages of both phase legs. The average voltages of the SM capacitor are maintained at $V_C^{p,n} = 2.4$ kV due to a 20% of elevation. As the DC power command changes, the active AC power of the upper and lower arms required to maintain the SM capacitor voltage balancing also changes. Consequently, subsequent to

the power flow reversal command, the average voltages of the SMs in the upper and lower arms diverge from each other. This deviation caused by the sudden change of the DC power flow is quickly mitigated by the arm power balance controller within less than 40 ms as shown in Fig. 4.12(c).

Fig. 4.12(e) illustrates the reference voltages of the upper and lower arms of phase legs 1. As demonstrated in the figure, V_{ac}^{p} and V_{ac}^{p} are maintained at their maximum attainable values for $\zeta = 1.2$, determined by (4.14).

Fig. 4.12(f) illustrates ϕ prior and subsequent to the power step change. ϕ is controlled to minimize capacitor voltage deviation of the SM capacitors of the upper and lower arms. To satisfy (4.7), ϕ is maintained in the region of $[\frac{\pi}{2}, \pi)$ between $t = 0$ s and $t = 0.05$ s for $P > 0$. Subsequent to the power step change at $t = 0.05$ s, ϕ is moved to the region of $(\pi, \frac{3\pi}{2}]$ for $P < 0$.

4.4.4 Case IV: Maximum Converter Power Increase at $D = 0.2$

Case IV demonstrates capability of the full-bridge based DC MMC to extend P_{max} by applying the proposed SM capacitor voltage elevation strategy. Initially, the DC MMC system is in steady state and $I_{\text{dc1}}^{\text{ref}}$ is set to +0.62 kA such that $P = +1$ MW is transferred. Between $t = 0$ s to $t = 0.08$ s, ζ is set to 1. Consequently, the SM capacitor voltages are maintained at $V_{C,nominal}$ as shown in Fig. 4.13(c) and $V_{\text{ac}}^{p,n,\text{ref}} = 1.6$ kV is maintained for $D = 0.2$ shown in Fig. 4.13(e). As shown in Fig. 4.13(b), at $t = 0.03$ s, I_{dc1} is stepped up from +0.62 kA to 0.94 kA. This change corresponds to a power step up from +1 MW to +1.5 MW from DC-link 1 to DC-link 2. Subsequent to the power step change, the the following events occur:

- The step change of P from 1 MW to 1.5 MW necessities an increase of $P_{\text{ac}}^{p,n}$.
- A divergence occurs between the SM capacitor voltages of the upper and lower arms shown in Fig. 4.13(c), which indicates the energy balance of the SM capacitors is disturbed.

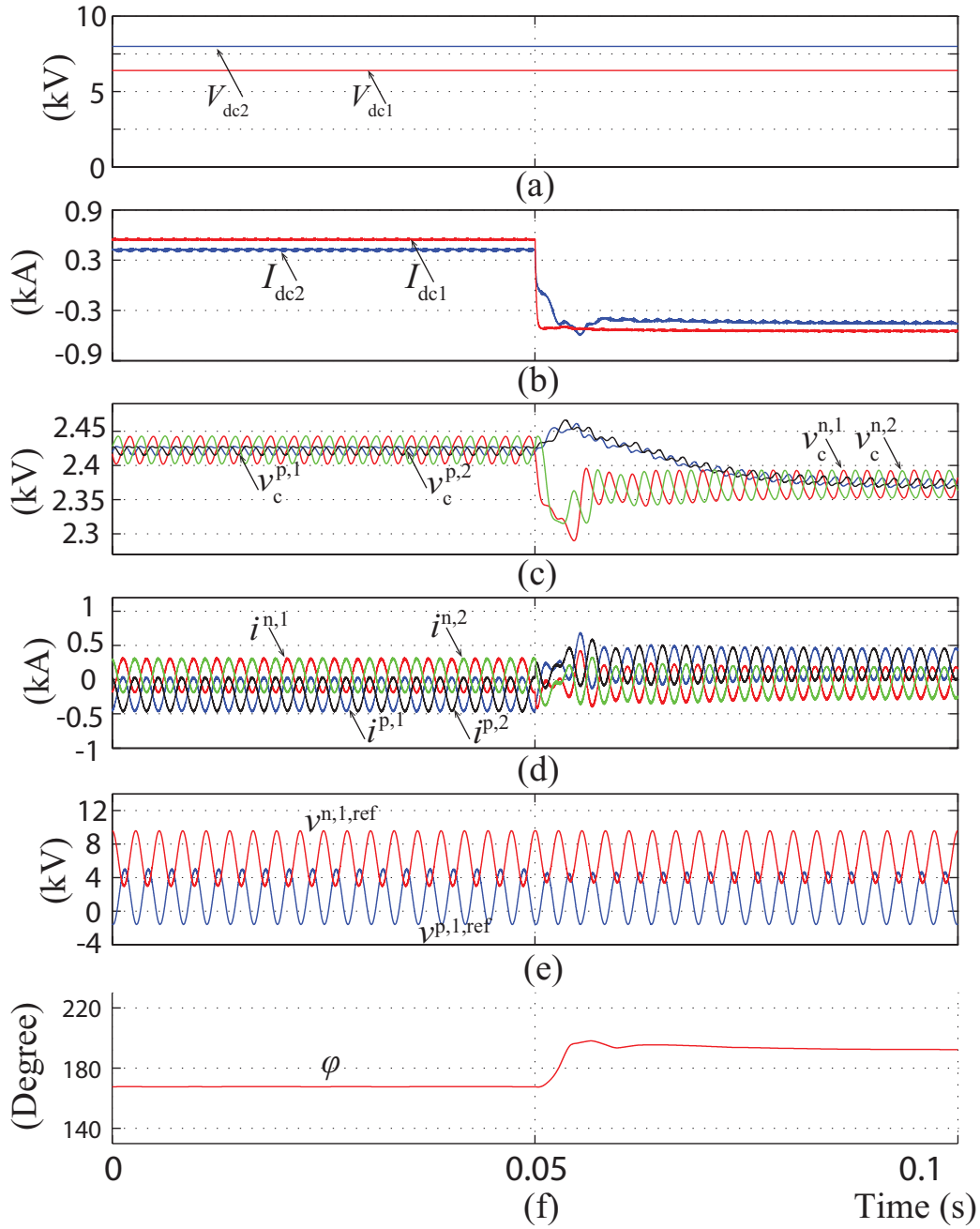


Figure 4.12: Simulated converter waveforms using the proposed control strategy with the full-bridge SMs at $D = 0.8$: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) phase shift angle between the upper and lower arms.

- The controller reduces ϕ to increase $P_{\text{ac}}^{p,n}$. ϕ reaches $\frac{\pi}{2}$ at $t = 0.035$, which indicates that $P = P_{\text{max}}$ is attained. Nevertheless, the controller fails to re-establish energy balance for the SM capacitors as $P^{\text{ref}} > P_{\text{max}}$.

It is obvious that the DC MMC is not able to deliver the commanded power. To increase P_{max} of the converter, ζ is set to 1.2 at $t = 0.08$ s. Subsequent to the step change of ζ, the following events occur:

- The maximum value of $v^{p,\text{ref}}$ is raised above 8 kV whereas the minimum value of $v^{p,\text{ref}}$ is decreased below zero.
- ϕ is increased to accommodate the higher P_{max} due to the elevated $V_C^{p,n}$.
- Energy balance is re-established for the SM capacitors as the converter is able to deliver the commanded power with the elevated SM capacitor voltages. Consequently, the new operating points of the elevated SM capacitor voltage is maintained at 2.4 kV in steady state.

Furthermore, the AC circulating current is reduced with the SM capacitor voltage elevation though a greater amount of power is transfered. The simulation study demonstrates that the proposed control strategy is able to increase P_{max} of the DC MMC while maintaining the SM capacitor voltage balanced.

4.5 Chapter Summary

This chapter proposes a enhanced closed-loop control strategy for the full-bridge SM based DC MMC. The proposed control strategy offers two major advantages over the conventional control strategies: (i) the converter power transfer capability is extended; and (ii) the AC current component of each arm is reduced significantly. Comparative evaluations are provided to illustrate the salient features of the proposed control strategy. Case studies are presented to validate the dynamic response of the proposed control strategy.

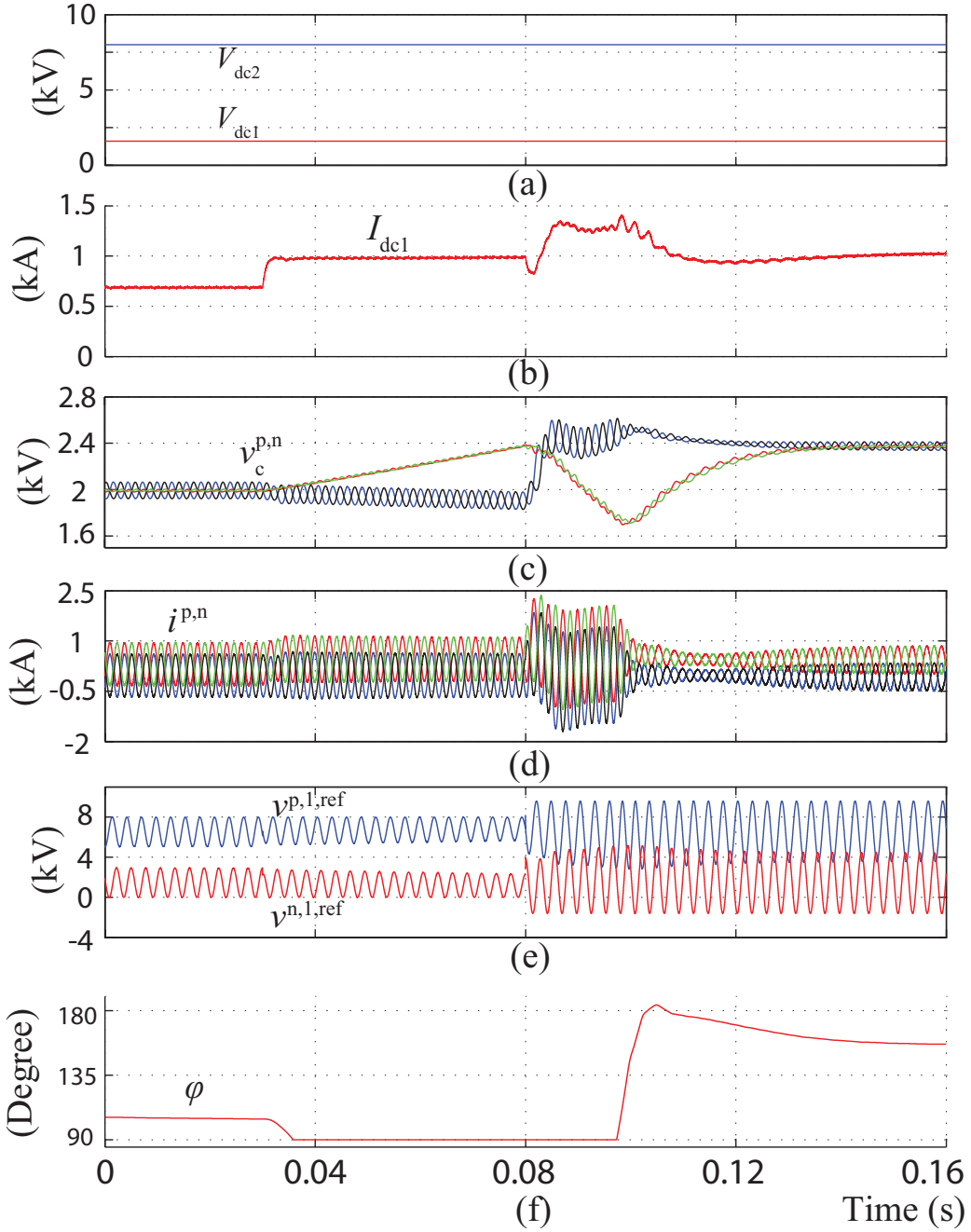


Figure 4.13: Simulated converter waveforms using the proposed control strategy with the full-bridge SMs at $D = 0.2$: (a) DC links 1 and 2 voltages, (b) DC links 1 and 2 currents, (c) SM capacitor voltages of the upper and lower arms of phase legs 1 and 2, (d) arm currents of phase legs 1 and 2, (e) arm voltage reference of phase-leg 1, and (f) phase shift angle between the upper and lower arms.

CHAPTER 5

CONSTRAINTS-ORIENTED DESIGN OF THE DC MMC

This chapter presents a constraints-oriented design approach for the DC MMC to achieve high efficiency while satisfying a set of design constraints. In the DC MMC, the operating frequency can be chosen arbitrarily. Although a higher operating frequency reduces the size of passive components, it increases the power losses of the converter. Furthermore, the DC MMC topology inherently requires a large phase filtering inductor to remove the AC component presented in the phase current. However, an over-sized inductor will add to the system cost and size/volume. In this chapter, a systematic approach is developed, such that based on certain given design constraints, the size of passive components as well as the operating frequency of the converter can be determined. In this way, it is ensured that the converter meets the design specifications. Accuracy of the design approach is validated based on simulation studies in the PSCAD/EMTDC software environment.

5.1 Converter Design and Component Sizing

The objective of the component sizing is to meet the specifications of the converter while satisfying a set of given design constraints. The first step of designing a DC MMC is to define its specifications based on the application. The following electrical specifications are identified as the key parameters of the power stage of the converter:

- The nominal converter power throughput, P_{nominal}.
- The minimum converter efficiency, η_{min}.
- The nominal DC-link 2 voltage, $V_{\text{dc2,nominal}}$.
- The rated voltage conversion ratio, D_{nominal}.

- The number of phase legs, M.
- The number of SMs per arm, N.

Once the electrical specifications are given, design constraints need to be determined to ensure proper operation of the DC MMC. The following constraints are identified:

- The energy flow in the SM capacitors results in voltage ripple. The voltage ripple is inversely proportional to the SM capacitance. Large SM capacitor voltage ripple may compromise the stability of the converter. Consequently, the SM capacitance must be sized properly such that the voltage ripple is less than a pre-specified value, which is usually between 5% to 10% of the nominal average SM capacitor voltage.
- The DC MMC utilizes inductive filters to prevent the AC circulating current from leaking to the DC link. An undersized inductive filter may result in large DC-link current ripple, which subsequently causes the AC circulating current to increase and the converter power transfer capability to decrease. Therefore, the inductive filter must be sized sufficiently large such that the phase current ripple is less than a rated value, which is usually set to 5% of the rated phase DC current.
- To meet the converter efficiency requirement, the total converter losses that includes semiconductor losses and passive components losses must be less than a rated value determined based on the converter specifications.

Based on the identified design specifications and constraints, the following inequalities are derived:

$$P_{\text{max}} \geq P_{\text{nominal}} \tag{5.1a}$$

$$\max(\Delta v_C^p, \Delta v_C^n) \leq \Delta v_{C,\text{max}}, \tag{5.1b}$$

$$I_{\text{o,ac}} \leq I_{\text{o,ac,max}}, \tag{5.1c}$$

$$P_{\text{loss}} \leq P_{\text{loss,max}}, \tag{5.1d}$$

where P_{max} represents the maximum converter power, $\Delta v_{C,\text{max}}$ represents the maximum SM capacitor voltage ripple, $I_{\text{o,ac,max}}$ represents the maximum amplitude of the phase current AC component, and $P_{\text{loss,max}}$ represents the maximum converter power losses.

In the following sections, a systematic design procedure is developed for the DC MMC such that (5.1a)-(5.1d) are satisfied at the rated operating condition. Sizing of the arm and phase filtering inductors as well as the SM capacitor are discussed in this chapter. In addition to the component sizing, selection of the operating frequency of the converter is also explained. The design approach proposed in this chapter is equally applicable to the DC MMC with either the half-bridge or the full-bridge SMs based DC MMC in which the capacitor voltage elevation is disabled ($\zeta = 1$).

5.1.1 Arm Inductive Reactance

A simplified model of the DC MMC is employed to size X_L. The simplified model is derived by assuming that $X_{L_o} >> X_L$. Consequently, (2.13), (2.14), and (2.18) are simplified to:

$$I^p_{\text{ac}} = I^n_{\text{ac}} = | - \frac{1}{2jX_L}(\tilde{v}^p_{\text{arm,ac}} + \tilde{v}^n_{\text{arm,ac}})|, \tag{5.2}$$

$$(\frac{V_{\text{dc1}}}{V_{\text{dc2}}} - 1)\frac{P}{M} = -\frac{1}{2X_L}V^p_{\text{ac}}V^n_{\text{ac}}sin(\phi). \tag{5.3}$$

In the conventional DC-AC MMC used for HVDC applications, the arm reactance serves two main functions:

- Attenuating the magnitude of circulating currents.
- Limiting the DC-side short-circuit fault current.

In contrast, in the DC MMC, the AC circulating current is required to exchange active power between the upper and lower arms of each phase-leg, whereby power balance can be maintained within each phase-leg. As a result, the magnitude of the circulating current at the fundamental frequency is controlled to maintain the SM capacitor power balance

and it does not need to be suppressed by passive components. In the DC MMC, the arm inductor acts as a line impedance such that the voltage across the inductor generates an AC component for the arm current. It should be noted that since the AC circulating current in the DC MMC may contain high-frequency harmonics, the arm inductor is utilized to attenuate the high-frequency harmonics of the AC circulating current.

The maximum converter power is tightly coupled with X_L. Consequently, it is essential to size X_L such that (5.1a) is satisfied. To determined $P_{\max}$ for a given conversion ratio, $\phi = \pi/2$ and the maximum attainable amplitude of arm AC voltages from (4.15) are substituted into (5.3). Fig. 5.1 presents the impact of X_L on $P_{\max}$ for various voltage conversion ratios and X_L. As shown in Fig. 5.1, $P_{\max}$ reduces as X_L increases. In addition, as the conversion ratio deviates from 0.5, $P_{\max}$ deceases at fixed X_L. Consequently, the maximum X_L can be determined to ensure $P_{\max} > P_{\text{nominal}}$ at the rated voltage conversion ratio:

$$X_{L,max} = \begin{cases} \frac{M}{P(1-D)}(\min[(\zeta^n N V_{C,nomial} - v^n_{\text{dc}}), (v^p_{\text{dc}} + \zeta^p N^p_{\text{FB}} V_{C,nomial})])^2; D \geq 0.5 \\ \frac{M}{P(1-D)}(\min[(\zeta^p N V_{C,nomial} - v^p_{\text{dc}}), (v^n_{\text{dc}} + \zeta^n N^n_{\text{FB}} V_{C,nomial})])^2; D \leq 0.5 \end{cases} \tag{5.4}$$

It should be noted that (5.4) is valid for both half-bridge and full-bridge SM based DC MMCs with or without SM capacitor voltage elevation. For the half-bridge SM based DC MMC, ζ is set to one and $N^{p,n}_{\text{FB}}$ is set to zero. For full-bridge SM based DC MMC without SM capacitor voltage elevation, ζ is set to one.

Furthermore, it is desired to size X_L such that the AC circulating current is minimized. Once the DC-link 1 and 2 voltages along with the rated power are given, the amplitude of the arm current AC component, $I^{p,n}_{\text{ac}}$, can be solved for various ϕ based on (5.2) and (5.3), $I^{p,n}_{\text{ac}}$ versus ϕ for various X_L is plotted in Fig. 5.2 in which $D = 0.5$ is assumed. For a constant X_L, as ϕ increases, $I^{p,n}_{\text{ac}}$ moves along a distinct curve. As ϕ approaches π, $I^{p,n}_{\text{ac}}$ reaches a minimum. As shown in Fig. 5.2, size of X_L does not affect the minimum achievable $I^{p,n}_{\text{ac}}$. Nevertheless, based on Fig. 5.2, as X_L decreases, the rate of change of $I^{p,n}_{\text{ac}}$ with respect to ϕ increases at the vicinity of the achievable minimum $I^{p,n}_{\text{ac}}$. As a result, a sufficiently large X_L

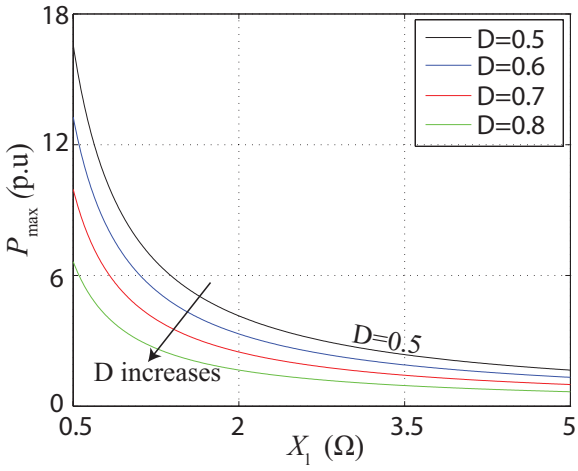


Figure 5.1: The maximum attainable converter output power versus arm inductive reactance.

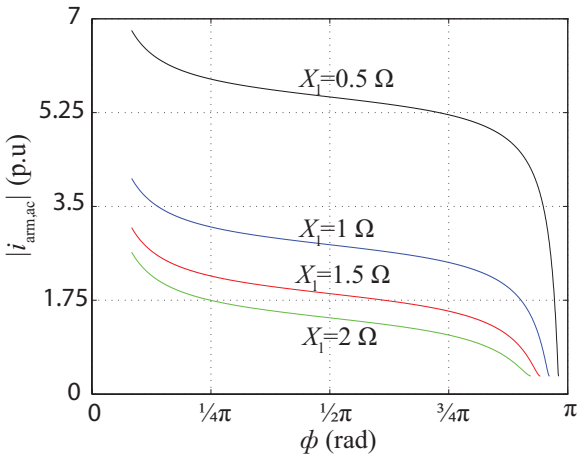


Figure 5.2: Arm AC current amplitude versus the arm voltage phase shifting angle.

should be selected to ensure that the controller is able to converge to the minimum attainable $I_{\text{ac}}^{p,n}$. In addition, a large X_L is also helpful in filtering the high-frequency harmonics of the AC circulating current and limiting DC-link fault current. Consequently, the maximum X_L determined by (5.5) should be selected, i.e.,

$$X_L = X_{L,max} \tag{5.5}$$

5.1.2 Phase Filtering Inductive Reactance

For proper operation and minimized power losses of the DC MMC, the amplitude of the AC component of the output phase current, $I_{\text{o,ac}}$, should be negligible. This necessitates a large X_{L_o}, which for high power/voltage applications, adds to the system cost and volume/size. Therefore, it is essential to determine the minimum X_{L_o} that satisfies (5.1c). $I_{\text{o,ac}}$ can be determined by solving (2.15) for various X_{L_o}. Fig. 5.3 presents $I_{\text{o,ac}}$ versus X_{L_o} at various voltage conversion ratios. In Fig. 5.3, it is assumed that the maximum attainable amplitude of the arm AC voltage and its corresponding angle ϕ are applied such that the amplitude of the arm AC current is minimized and the power balance is maintained for each arm. Assuming $X_{L_o} \gg X_L$, X_{L_o} that satisfy (5.1c) can be determined by:

$$X_{L_o} = \frac{\sqrt{(V_{\text{ac}}^p)^2(V_{\text{ac}}^n)^2 - 2V_{\text{ac}}^p V_{\text{ac}}^n cos(\phi)}}{2I_{o,\text{ac,max}}}, \tag{5.6}$$

where $V_{\text{ac}}^p = V_{\text{ac}}^p = V_{\text{ac,max}}^{p,n}$ determined by (4.15) is assumed for circulating current minimization. The phase-shift angle can be determined by:

$$\phi = sin^{-1}[\frac{4(1-D)PX_L}{M(V_{\text{max}}^{p,n})^2}]. \tag{5.7}$$

As shown in Fig. 5.3, as X_{L_o} increases, $I_{\text{o,ac}}$ decreases. However, the rate of change of $I_{\text{o,ac}}$ is reduced as X_{L_o} increases, which implies the marginal cost of reducing $I_{\text{o,ac}}$ is increased. In addition, as the voltage conversion ratio deviates from 0.5, $I_{\text{o,ac}}$ decreases for the same X_{L_o}. The minimum X_{L_o} that ensures the $I_{\text{o,ac}}$ meets the design constraint is selected as the best value for X_L.

5.1.3 SM Capacitive Reactance

As shown in (2.25) and (2.26), the ripple components of the SM capacitor voltages of the upper and lower arms include one fundamental component term as well as a second-order harmonic term. The amplitude of the fundamental term depends upon the ratio of the input and output DC-link voltages. The magnitude of the SM capacitor voltage ripple in the upper

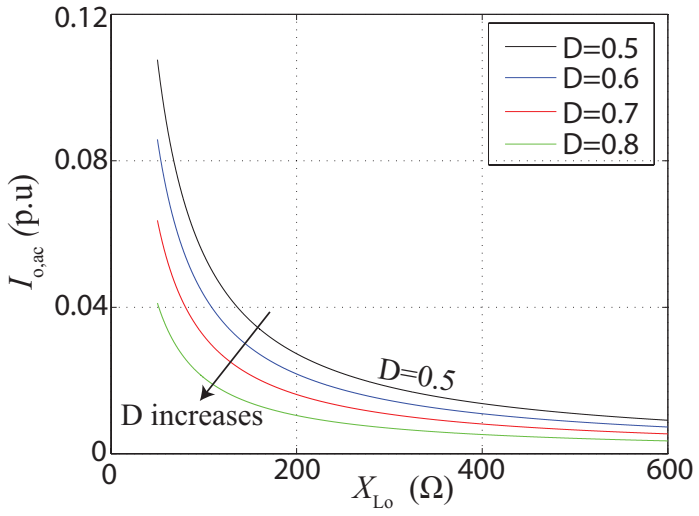


Figure 5.3: Phase AC current amplitude versus phase filtering inductive reactance.

and lower arms is a function of the voltage conversion ratio. As the voltage conversion ratio deviates from 0.5, the magnitudes of the SM capacitor voltage ripple of the upper and lower arms become different. Therefore, it is important to size X_C to ensure the magnitudes of the SM capacitor voltage ripple in both arms stay below the design constraint.

X_C is determined by solving (2.25) and (2.26) using numerical method. The normalized magnitude of the SM capacitor voltage ripple versus the SM capacitive reactance is shown in Fig. 5.4, when $D = 0.7$. As shown in Fig. 5.4, the normalized magnitude of the voltage ripple of the SMs in the lower arm is greater than the upper arm. As X_C decreases, the normalized magnitude of the voltage ripple of the SMs in both arms decrease. Based on Fig. 5.4, the best value of X_C is selected as its maximum value so that the magnitudes of SM capacitor voltage ripple in both arms satisfy (5.1b).

5.1.4 Operating Frequency

Unlike the DC-AC MMC used in HVDC applications in which the operating frequency is imposed by the converter AC-side frequency, the operating frequency of the DC MMC is a free design parameter. The operating frequency is determined based on a trade-off between the component size/cost and the converter efficiency. To choose a proper AC operating

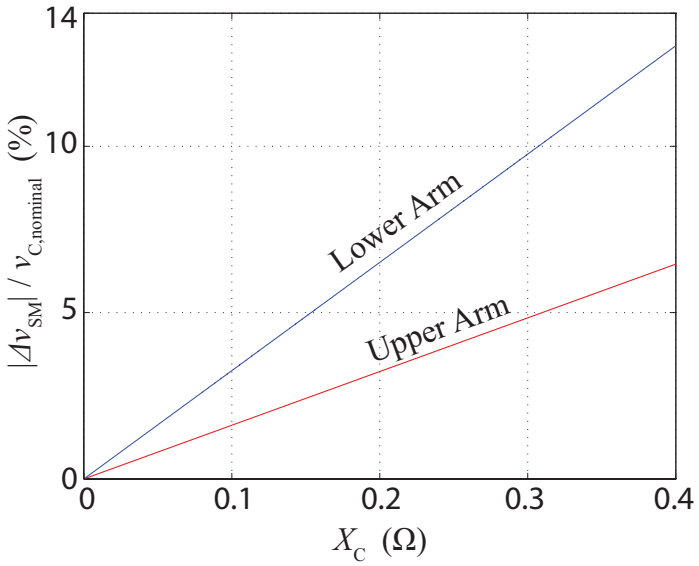


Figure 5.4: The normalized magnitude of the SM capacitor voltage ripple versus the SM capacitive reactance at D=0.7.

frequency, the power losses of the converter are evaluated at various operating frequencies. Since a higher operating frequency leads to smaller passive component size/cost, the maximum AC operating frequency that satisfies the power loss constraint is identified as the best operating frequency. Since the semiconductor devices are the major contributors to the converter total power losses [98], in this chapter, the power losses due to the passive components are ignored. To calculate the power losses of the active switches, a power loss estimation method based on semiconductor behavior model is adopted from [99]. By applying this method, the total conduction and switching losses of the DC MMC at the given operating conditions are evaluated for various operating frequencies using numerical method. The converter semiconductor power losses versus the converter operating frequency are shown in Fig. 5.5. As shown, as the operating frequency increases, the switching losses increase whereas the conduction losses are independent of the operating frequency. Once the operating frequency is chosen, the arm and phase filtering inductances as well as the SM capacitance can be determined based on the operating frequency and their corresponding reactances that are determined in the previous steps.

The overall design procedure of the DC MMC is illustrated in the flowchart of Fig. 5.6.

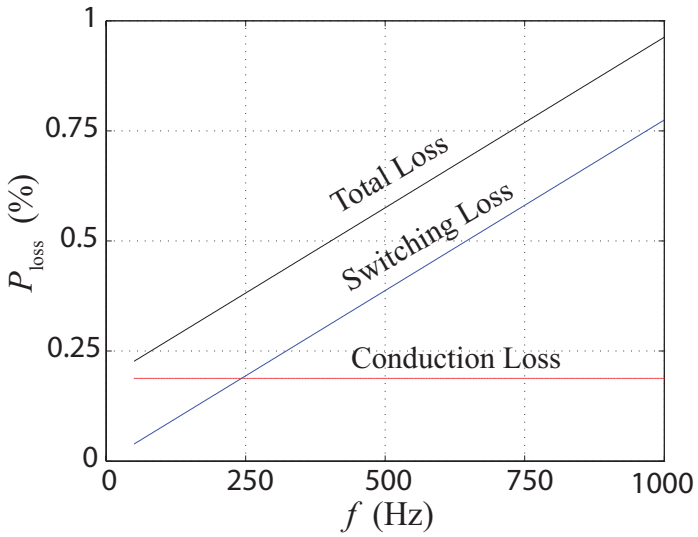


Figure 5.5: Converter semiconductor power losses versus the operating frequency.

Given the nominal operating conditions and the design constraints, first, X_L is selected based on the converter nominal power and the controller convergence test. X_L should be sized to guarantee that the controller converges to the achievable minimum arm AC current. As shown in Fig. 5.6, several iterations might be required to find the best set of components that satisfy the design constraints. Once X_L is selected, the amplitude of the AC component of the phase current is calculated for various X_{L_o}. X_{L_o} that satisfies (5.1c) is determined by applying (5.6) in this step. The magnitude of the SM capacitor voltage ripple will then be calculated for different X_{C}. The maximum X_{C} that satisfies the constraint on the SM voltage ripple magnitude is identified as the best value of X_{C}. In the next step, semiconductor power losses are estimated at various operating frequencies and the maximum frequency that satisfies the power loss constraint can be identified as the best value. After this step, the controller performance will be evaluated by simulation studies. If the controller fails to converge to the minimum achievable amplitude of AC circulating current, X_L will be resized. Finally, the arm and output inductors as well as the SM capacitor can be sized.

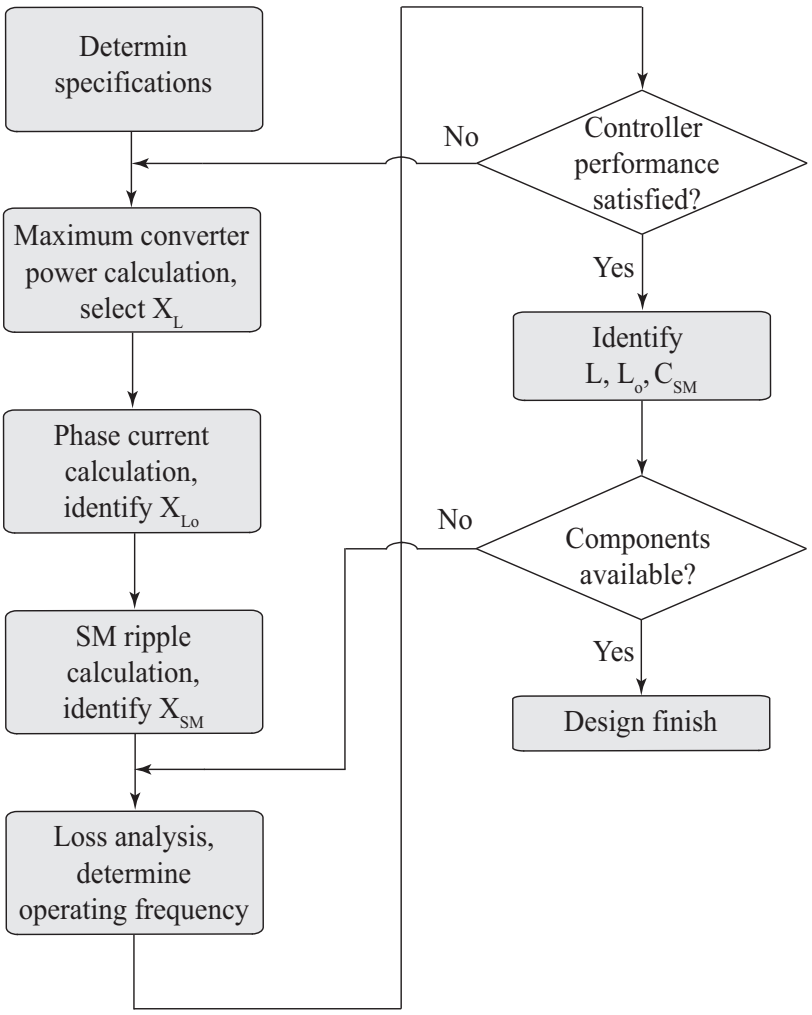


Figure 5.6: Flowchart of the component sizing procedure of the DC MMC.

5.2 Simulation Results

Two case studies are presented in this section on a 3 phase-leg DC MMC of Fig. 2.1, using parameters and corresponding constraints listed in Tables 5.1 and 5.2. The studies are conducted to demonstrate the accuracy of the converter design process. The size of the passive components is determined based on the design procedure in Fig. 5.6. Two modes of operations are simulated to mimic the bidirectional power flow: the buck mode of operation, which is defined as DC power flowing from DC-link 2 to DC-link 1 and the boost mode of operation, which is defined as DC power flowing from DC-link 1 to DC-link 2. The designed converters are simulated in the PSCAD/EMTDC software environment.

The control strategy proposed in [49] is used in the simulation. The control strategy consists of an open-loop output voltage controller combined with a closed-loop circulating current controller. The sinusoidal pulse width modulation strategy is used to generate the gating signals.

Table 5.1: Nominal Conditions and Design Constraints for D=0.5

Nominal Conditions	**Value**
Output power, P	7 MW
DC-link 1 voltage, V_{dc1}	4.4 kV
DC-link 2 voltage, V_{dc2}	8.8 kV
Design Constraints	**Value**
Phase current ripple, $I_{o,\text{ac,p-p}}/i_{o,dc}$	5%
SM voltage ripple, $\lvert\Delta v_{\text{SM}}\rvert/v_{C,nominal}$	4%
Converter power losses	1%
Converter Parameters	**Value**
Number of phase-legs, M	3
Number of SMs per arm, N	4
SM capacitor, C	2 mF
Arm inductor, L	0.89 mH
Phase filtering inductor, L_o	132 mH
Operating frequency, f	360 Hz
Performance Parameters	**Analytical Results**
Phase current ripple, $I_{o,\text{ac,p-p}}$	19.6 A
SM capacitor voltage ripple $\lvert\Delta v_{\text{SM}}\rvert$	81.6 V
Converter power losses	0.5%

5.2.1 Case I: Steady-state Operation at $D = 0.5$

The steady-state converter waveforms for buck and boost modes of operation of the DC MMC are provided in Figs. 5.7 and 5.8, respectively, where $D = 0.5$. In both figures, the SM capacitor voltages and arm currents of only the phase-*a* are shown. The nominal conditions, design constraints, converter parameters, and analytical results are shown in Table 5.1. By following the described design procedure, an X_L of 2 Ω is selected to ensure the power transfer capability is greater than the nominal power. An X_{L_o} of 450 Ω is chosen, which results in 19.6 A phase current ripple. X_{C} is selected as 0.2 Ω, which results in 3.8%

Table 5.2: Nominal Conditions and Design Constraints for D=0.7

Nominal Conditions	**Value**
Output power, P	7 MW
DC-link1 voltage, V_{dc1}	6.16 kV
DC-link2 voltage, V_{dc2}	8.8 kV
Design Constraints	**Value**
Phase current ripple, $I_{o,\text{ac,p-p}}/i_{o,dc}$	5%
SM voltage ripple, $\lvert\Delta v_{\text{SM}}\rvert/v_{C,nominal}$	4%
Converter power losses	1%
Converter Parameters	**Value**
Number of phase-legs, M	3
Number of SMs per arm, N	4
SM capacitor, C	4.1 mF
Arm inductor, L	0.89 mH
Phase filtering inductor, L_o	97.3 mH
Operating frequency, f	360 Hz
Performance Parameters	**Analytical Results**
Phase current ripple, $I_{o,\text{ac,p-p}}$	19 A
SM capacitor voltage ripple $\lvert\Delta v_{\text{SM}}\rvert$	86 V
Converter power losses	0.5%

(81.6 V) SM capacitor voltage ripple. An AC operating frequency of 360 Hz is chosen, leading to 0.5% semiconductor power losses.

Since $D = 0.5$, the DC components of i^p and i^n have the same magnitude as shown in Figs. 5.7(c) and 5.8(c). The magnitudes of the SM capacitor voltage ripple in the upper and lower arms are the same, i.e., 74 V for buck mode of operation and 78 V for boost mode of operation. The peak to peak magnitude of the phase current ripple is equal to 18 A for both modes of operation. As confirmed by the waveforms of Figs. 5.7 and 5.8, the magnitudes of the SM capacitor voltages ripple and AC component of the phase current are below the design constraints for both modes of operation.

5.2.2 Case II: Steady-state Operation at $D = 0.7$

The corresponding simulation results at $D = 0.7$ for buck and boost modes of operation are provided in Figs. 5.9 and 5.10, respectively. For both modes of operation, the converter

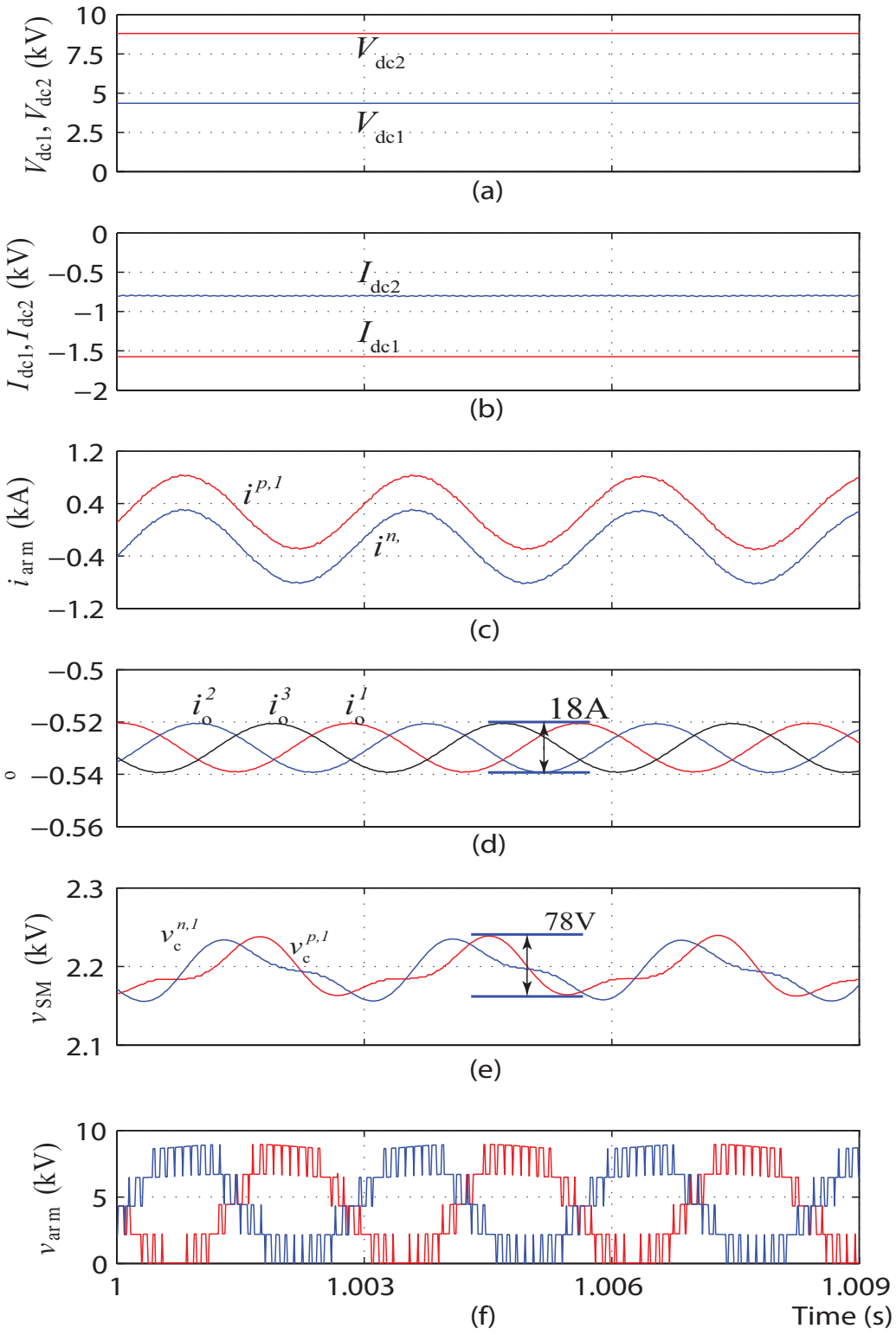


Figure 5.7: Steady-state converter waveforms for buck mode of operation when $D = 0.5$: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-leg 1, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-leg 1 and (f) upper and lower arm voltages of phase-leg 1.

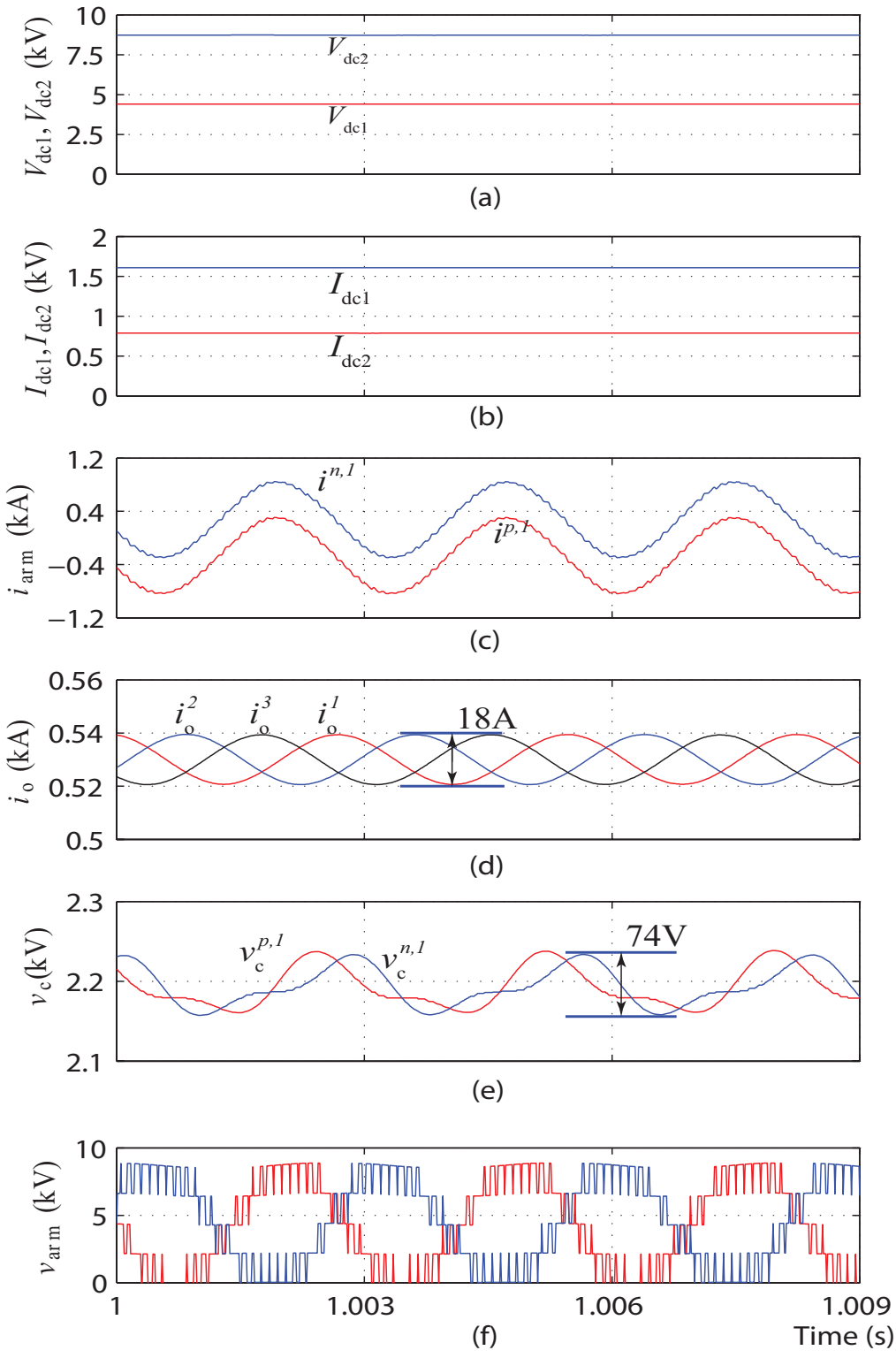


Figure 5.8: Steady-state converter waveforms for boost mode of operation when $D = 0.5$: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-leg 1, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-leg 1 and (f) upper and lower arm voltages of phase-leg 1.

transfers 7 MW power. The nominal conditions, design constraints, converter parameters, and analytical results are shown in Table 5.2. An X_{L_o} of 120 Ω is chosen, which results in a phase AC current with a ripple of 19 A. X_{C} is selected as 0.11 Ω, which leads to 3.9% (86V) SM capacitor voltage ripple. An AC operating frequency of 360 Hz is used, resulting in 0.5% semiconductor power losses. Since the current sharing between the upper and lower arm pairs changes with the conversion ratio, when $D = 0.7$, the upper and lower arms unequally contribute to the DC current shown in Figs. 5.9(c) and 5.10(c). This, consequently, leads to unequal magnitudes of the SM capacitor voltage ripple in the upper and lower arms, as shown in Figs. 5.9(e) and 5.10(e). To accommodate the change in the SM capacitor voltage ripple, the SM capacitor is sized larger than Case A. In this case, X_{C} is sized based on the magnitude of the SM capacitor voltage ripple of the lower arm, which is larger than that of the upper arm.

The magnitude of the SM capacitor voltage ripple of the lower arm is 80 V in the buck mode operation and 83 V in the boost mode operation. As shown in Figs. 5.9(d) and 5.10(d), the peak to peak magnitude of the phase current ripple is equal to 18 A for both modes of operation. As confirmed by the waveforms of Figs. 5.9 and 5.10, in both modes of operation, the magnitudes of the SM capacitor voltage ripple and AC component of the phase current are below their per-specified constraints. As shown in Figs. 5.9(c) and (f) to 5.10(c) and (f), in both cases, the power factor of each arm is near unity so that the arm AC current component is minimized for the given simulation conditions.

5.3 Chapter Summary

In this chapter, a systematic procedure for sizing the converter components and selecting of the operating frequency is developed based on the phasor-domain model of the DC MMC in Chapter 2. Proper sizing of the components ensures the converter achieves high efficiency while satisfying a set of given design requirements. Simulation results are presented to demonstrate the accuracy of the proposed method.

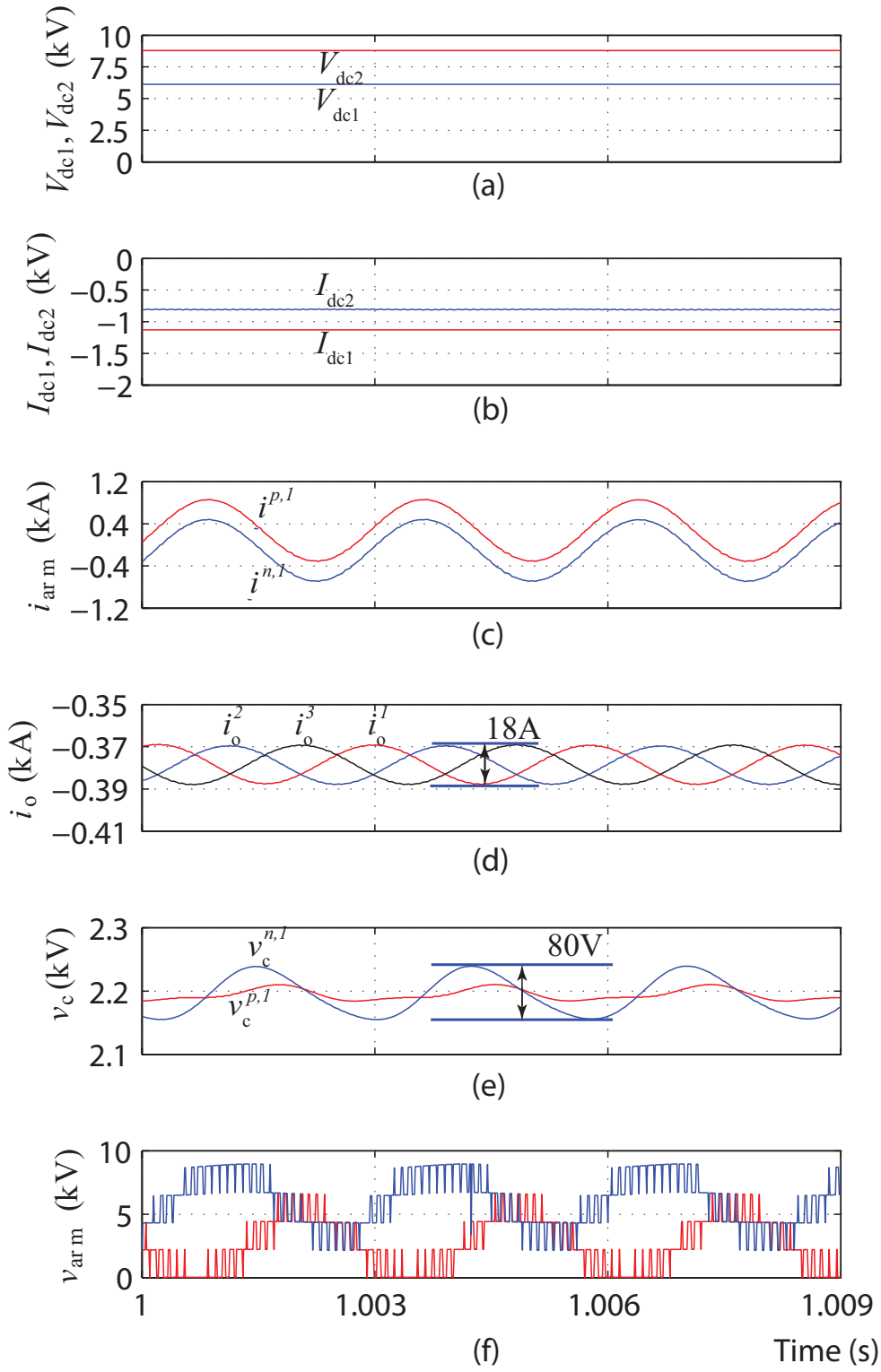


Figure 5.9: Steady-state converter waveforms for buck mode of operation when $D = 0.7$: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-leg 1, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-leg 1, and (f) upper and lower arm voltages of phase-*a*.

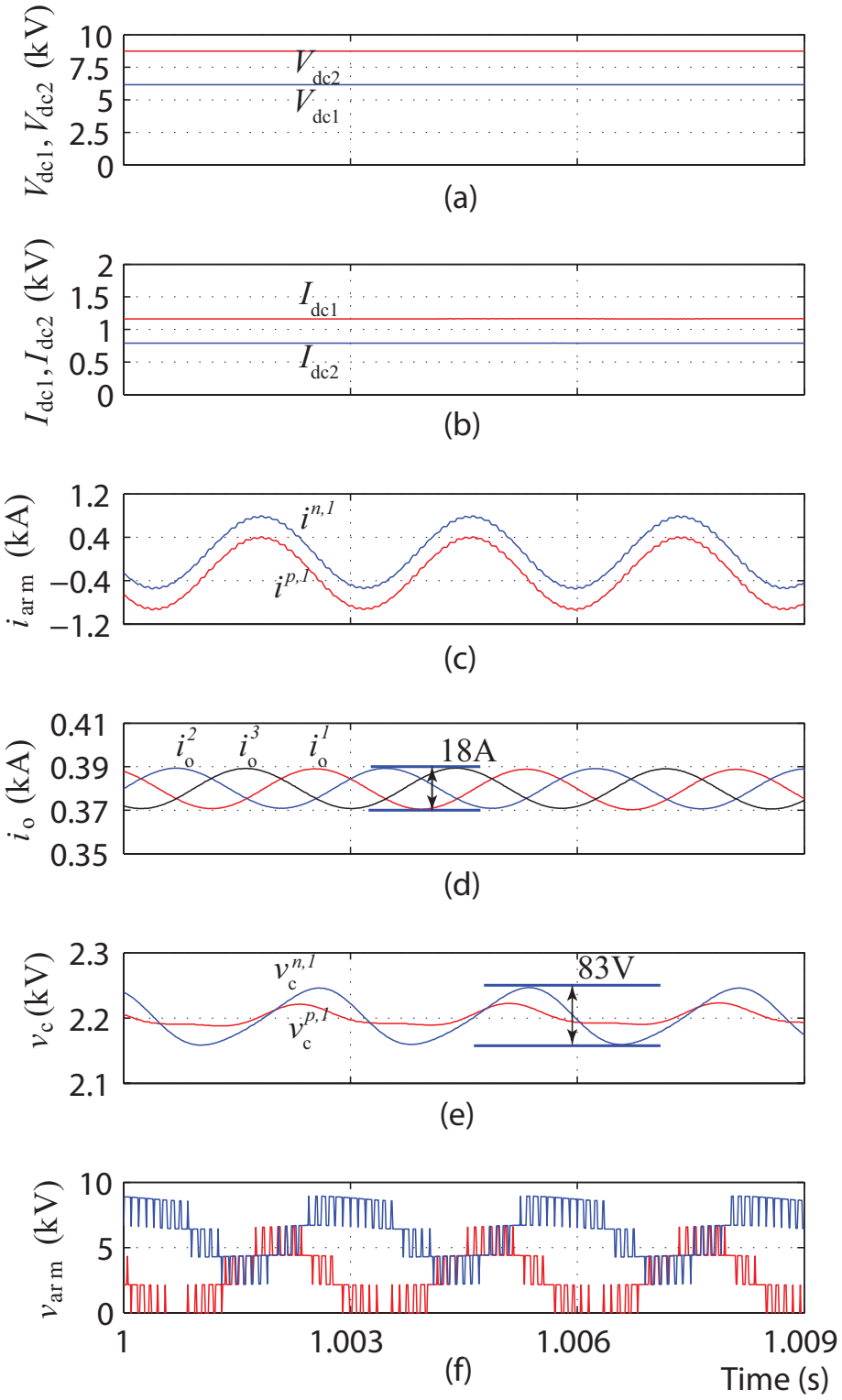


Figure 5.10: Steady-state converter waveforms for boost mode of operation when $D = 0.7$: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-leg 1, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-leg 1, and (f) upper and lower arm voltages of phase-leg 1.

CHAPTER 6

EXPERIMENTAL VALIDATION

In this chapter, the development of a 3.5-kW DC MMC prototype is presented. Experimental results are provided to:

- Validate the developed mathematical model of the DC MMC.
- Validate the developed design approach.
- Evaluate the proposed control strategy for the half-bridge based DC MMC.
- Evaluate the proposed control strategy for the full-bridge based DC MMC.

6.1 Development of the DC MMC Prototype

The design of the DC MMC prototype is provided in this section, which includes components sizing and implementation of the control strategy in Opal-RT rapid prototyping system. The developed DC MMC system is shown in Fig. 6.1

6.1.1 Hardware Design

The hardware of the DC MMC system involves power stage and sensing/driving circuits. The design of the power stage includes determination of the following parameters:

- The number of phase legs.
- The number of SMs in each arms.
- The size of arm inductor.
- The size of phase filtering inductor.

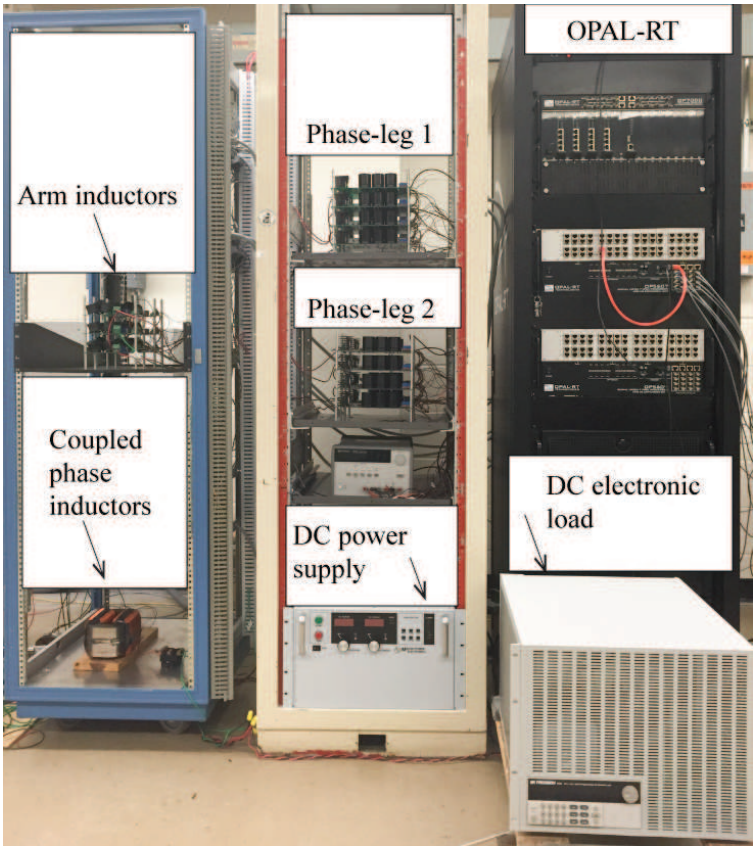


Figure 6.1: Experimental setup.

- The operating frequency.
- The voltage/current rating of the active switches.

The number of phase legs is determined based on the power rating and cost/loss optimization of the converter. In the developed prototype, two phase legs are used. In contrast to the conventional DC-AC MMC, in which the number of SMs also depends on the total harmonic distortion requirements, the number of SMs in a DC MMC is determined solely based on IGBT voltage rating and DC-link voltages. Selection of the number of SMs usually involves design iterations for sequential-based design approach as the device rating is tightly coupled with cost and conduction/switching losses. In the prototype, the number of SMs is set to four. Half-bridge SMs are employed in the lower arms and full-bridge SMs are employed in the upper arms. It should be noted that the full-bridge SMs can be operated in the half-bridge mode by disabling one pair of half-bridge switch module. Three design constraints are identified. The maximum SM capacitor voltage ripple is set to 10% of its nominal average voltage. The maximum phase current ripple is set to 5% of its rated DC value. The minimum converter efficiency is set to 90%. The specifications and design constraints of the DC MMC is summarized in Table 6.1.

Table 6.1: Converter Specifications

Quantity	**Value**
Nominal power, P	3.5 kW
DC-link 2 voltage, V_{dc2}	300 V
Nominal voltage conversion ratio, D	0.7
Number of phase legs, M	2
Number of SMs per arm, N	4
SM capacitor voltage ripple	10%
Phase current ripple	5%
Converter efficiency η	90%

Based on the identified specifications, the components sizes as well as the operating frequency are determined by following the design procedure proposed in Chapter 5. The maximum AC voltage component of each arm are determined by (4.15) as 90 V at nominal

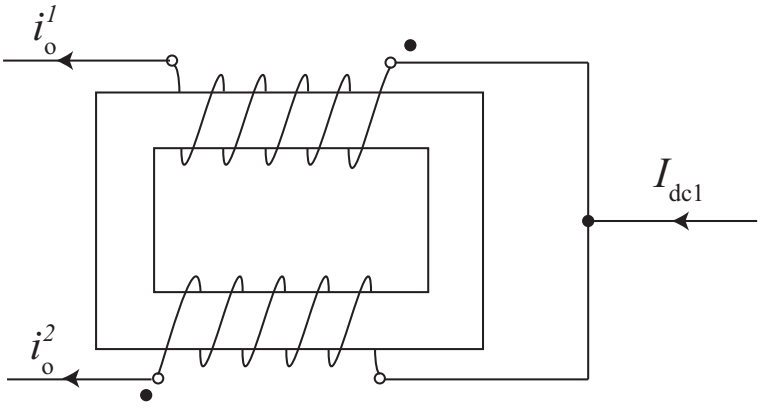
condition. $X_L = 3.77\ \Omega$ is determined by applying (5.5). $X_{L_o} = 391\ \Omega$ is determined by solving (5.6). $X_C = 0.45\ \Omega$ is determined using numerical method to solve for (2.25) and (2.26). For the laboratory prototype design, an extra voltage/current rating margin is allowed on the active switches to ensure safety operation. The half-bridge IGBT module IXYS FII40-06D is chosen to implement the active switches in the SM. By examining the semiconductor losses of the IGBT module, an operating frequency of 250 Hz is selected. The DC MMC parameters are summarized in Table 6.2.

Table 6.2: Parameters of the DC MMC Prototype

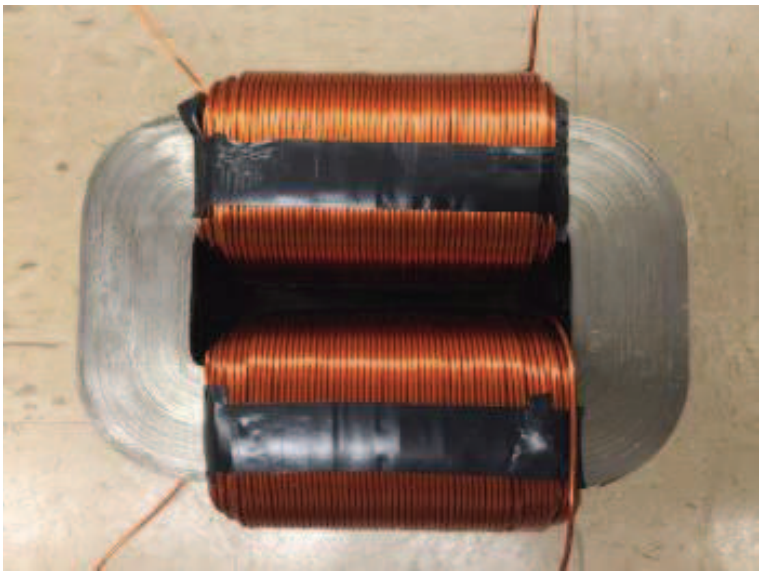
Converter Parameters	**Value**
SM capacitor, C_{SM}	1.41 mF
Arm inductor, L	2.5 mH
Phase filtering inductor, L_{o}	400 mH
Operating frequency, ω	250 Hz
Switch IGBT Model	IXYS FII40-06D

The arm inductors and SM electrolytic capacitors are implemented using commercially available products in the market. The design and fabrication of the phase filtering inductor is carried out in-house since the coupled inductor requires a special design. The coupled inductor is designed by following the design procedure of reference [100]. Amorphous alloy core is chosen for the coupled inductor due to its high saturation flux density (at 1.56 T) and low core losses. The schematic of the coupled inductor is shown in Fig. 6.2. The induced DC flux is canceled in the core due to the dot convention of the primary and secondary winding. Therefore, energy storage is not required in the core. The coupled inductor utilizes magnetizing inductance, and a large magnetizing inductance is required (0.4 H). Therefore, a small air-gap is designed in the core to minimize the size of the coupled inductor. Two U-shape cores are clamped together with a plastic insert between them creating air-gap in the core.

The SMs of the DC MMC are implemented using 16 PCBs, each consists of the power stage half-bridge/full-bridge circuit, gate driver, and capacitor voltage sensing circuit. The



(a)



(b)

Figure 6.2: (a) The schmematic and (b) photo of the coupled inductor.

input digital signal from the controller controls the state of each half-bridge module. This signal is inverted by using a logic gate to generate a pair of complementary gating signals. For a half-bridge SM, two sets of identical gate driver circuits are implemented on each PCB to drive the two switches in the half-bridge. Similarly, four sets of gate driver circuits are implemented for the full-bridge SMs. The driving circuit includes a dead-time delay circuit, an open-collector buffer, and an optical coupled gate driver. A dead-time period during which both switches in the half-bridge are in block state is required to prevent current shoot-through during commutation. The dead time can be implemented in software

and/or hardware. Since the software generated dead time is vulnerable to noise in a laboratory environment, it is generated using an RC circuit in each SM PCB. This dead time should be chosen carefully. A shorter than required dead-time may cause both IGBTs conducting at the same time. A longer than required one, however, leads to discontinued arm current and spike on arm voltages. The dead time can be determined by:

$$t_{\text{delay}} = [(t_{\text{off,max}} - t_{\text{on,min}}) + (t_{\text{pg,max}} - t_{\text{pg,min}})](1 + \text{m}\%), \tag{6.1}$$

where $t_{\text{off,max}}$ represents the maximum turn-off delay, $t_{\text{on,min}}$ represents the minimum turn-on delay, $t_{\text{pg,max}}$ and $t_{\text{pg,min}}$ represent the maximum and minimum propagation delay of the driver, respectively, and m represent the safety margin, which is usually set to 20%.

The capacitor voltage sensing circuit is implemented in each SM using LEM hall-effect voltage sensor LV-25. A low-pass filter is used to remove high-frequency noise from the output signal of the voltage sensor.

6.1.2 Controller Implementation

The control strategy is implemented through using Opal-RT rapid control prototyping system. The Opal-RT system consists of a real-time simulator running real-time operating system (RTOS) and two Vertex 7 FPGA and I/O expansion units. A host computer is interfaced with the simulator to monitor real-time signals of the control system and adjust controller parameters. The schematic of the control system is shown in Fig. 6.3. The main control system is divided into three components: controller, modulator, and SM capacitor voltage sorting balancing algorithm. The control system is implemented in three processing cores to maximum the speed. The power balance controller and DC-link current regulator generate the reference arm voltage, which is modulated by using the phase disposition pulse width modulation (PDPWM) technique. The generated modulation indices are fed to the capacitor voltage sorting algorithm, which sorts the capacitor voltages based on the arm current direction and set the switching state of each individual SM (insert or bypass). The

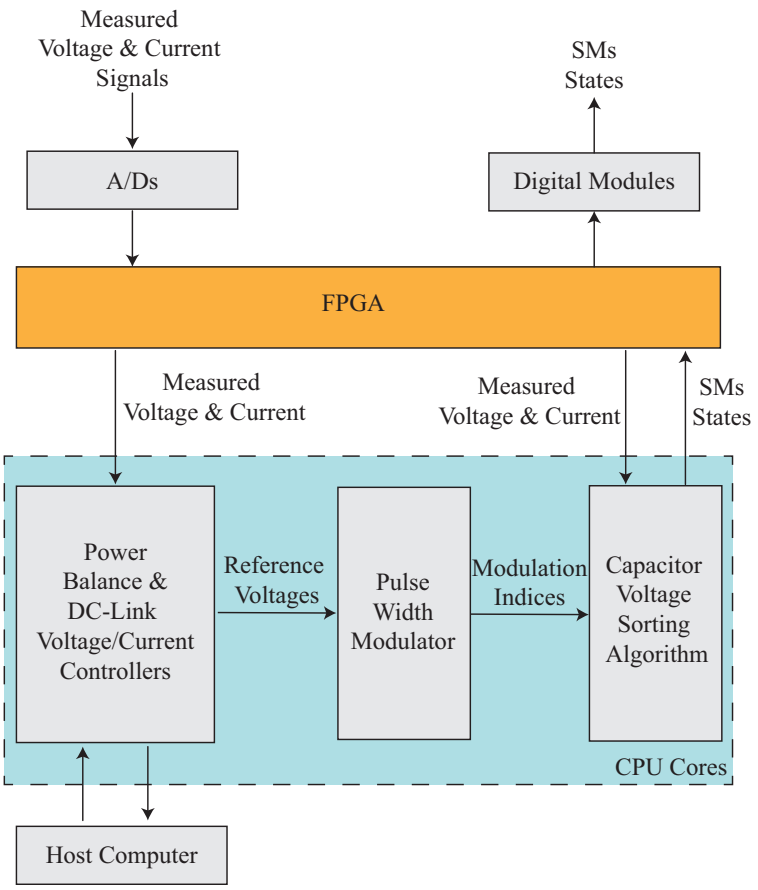


Figure 6.3: Control system architecture of the DC MMC prototype.

interface between the real-time controller and the hardware prototype is made through the FPGA and I/O expansion units. The measured analog input signals from the DC MMC are interfaced to the CPU cores through the analog-to-digital converter (A/D) that is controlled by the FPGA. The processed measured signals are fed into the CPU cores. The generated SM state signals are send to the hardware through digital modules.

6.2 Control Strategy Validation for the Half-bridge Based DC MMC

The capability of the proposed closed-loop control strategy to regulate the DC-link power, maintain energy balance of the SM capacitors, and minimize AC circulating current of the half-bridge based DC MMC is experimentally verified. In this section, the full-bridge SMs in the upper arms operate in the half-bridge mode as one half-bridge switch module in each

full-bridge SM is disabled. A programmable DC electronic load that operates in constant voltage mode is used to mimic a DC power grid with a constant voltage. A programmable DC power supply is used to provide input power to the converter. The proposed closed-loop control strategy in current regulation mode is adopted. The experimental results for both steady-state operation and dynamic response are presented.

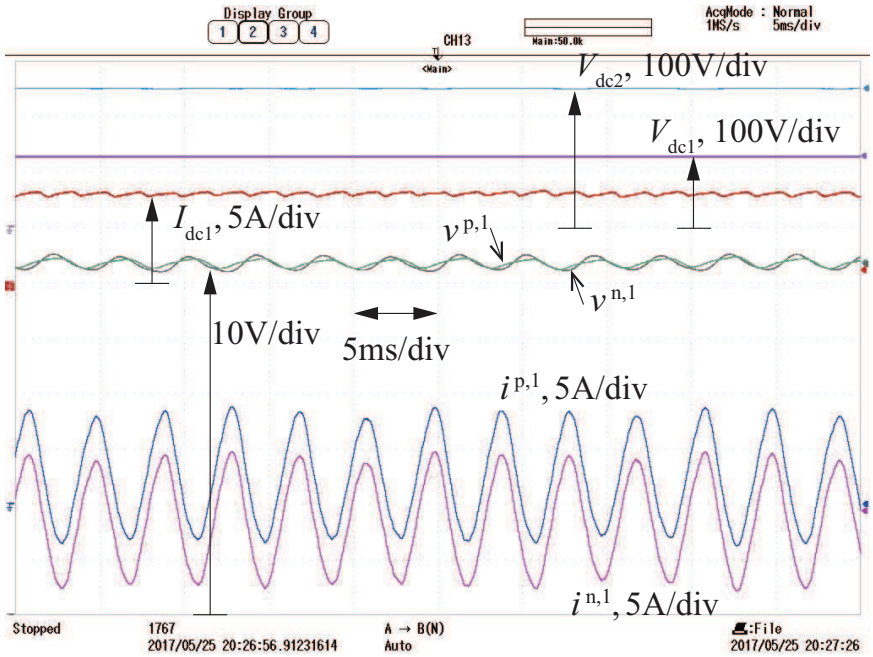
6.2.1 Steady-state Operation

Two case studies are presented in this section for $D = 0.52$ and $D = 0.7$. The experimental waveforms of the DC MMC in steady state at $D = 0.52$ where $P = -1$ kW, are presented in Fig. 6.4. The operating condition is summarized in Table 6.3. As shown in Fig. 6.4, the average SM capacitor voltages of the upper and lower arms are maintained at 62.5 V. The divergence between the SM capacitor voltages of the upper and lower arms are minimized by the controller. Fig. 6.4(b) shows the reference signal of the arm voltages of the phase-leg-1. The AC voltage components of the upper and lower arms are maintained equal in amplitude. The maximum value of the upper arm voltage is maintained at 250 V while the minimum value of the lower arm voltage is maintained at 0 V as the controller applies the maximum attainable amplitudes of the upper and lower arms voltages to minimize the AC circulating current.

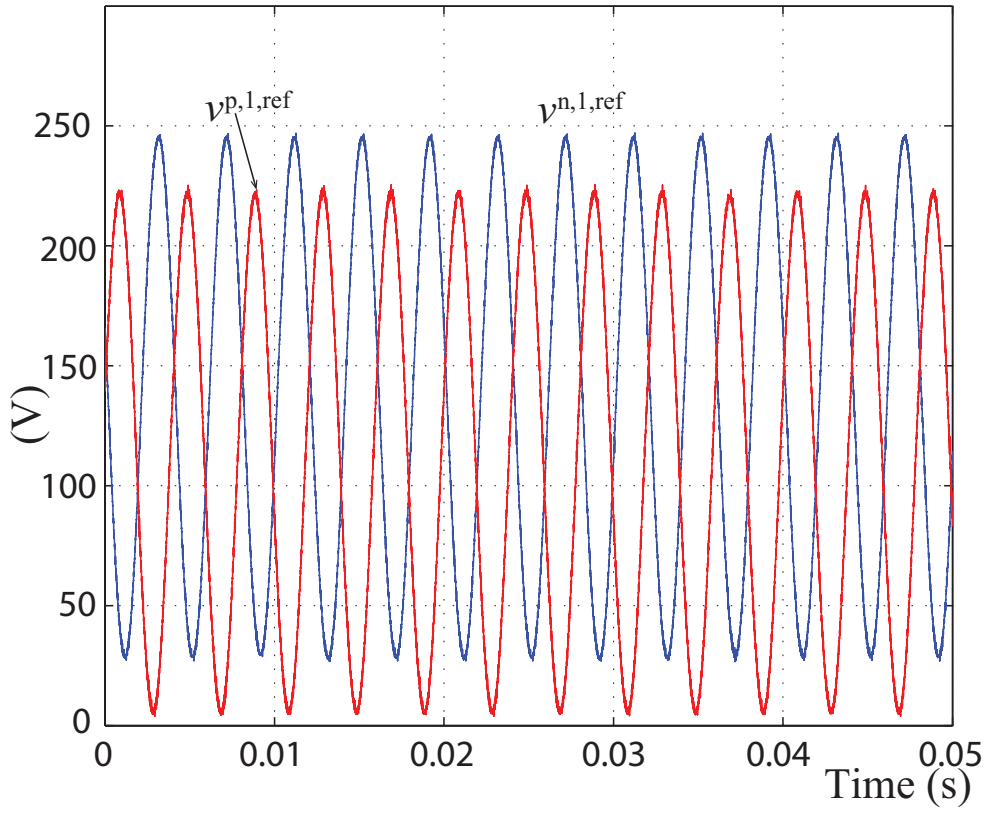
Table 6.3: Operating Condition for $D = 0.52$

Parameters	**Value**
DC-link 1 voltage, V_{dc1}	130 V
DC-link 2 voltage, V_{dc2}	250 V
DC-link 1 current , I_{dc1}	8 A

The experimental waveforms of the DC MMC in steady state at $D = 0.7$ where $P = -1.4$ kW are presented in Fig. 6.4. The operating condition is summarized in Table 6.4. As shown in Fig. 6.5(a), the SM capacitors experience an increased voltage ripple due to the increased DC power. Fig. 6.5(b) shows the reference signal of the arm voltages of the phase-leg-1. The controller is able to adjust the AC and DC components of the reference



(a)



(b)

Figure 6.4: Experimental results at $D = 0.52$.

voltage to accommodate the voltage conversion ratio change and control the phase-shift angle to maintain the energy balance of the SM capacitors.

Table 6.4: Operating Condition for $D = 0.7$

Parameters	**Value**
DC-link 1 voltage, V_{dc1}	176 V
DC-link 2 voltage, V_{dc2}	250 V
DC-link 1 current , I_{dc1}	8 A

6.2.2 Dynamic Response

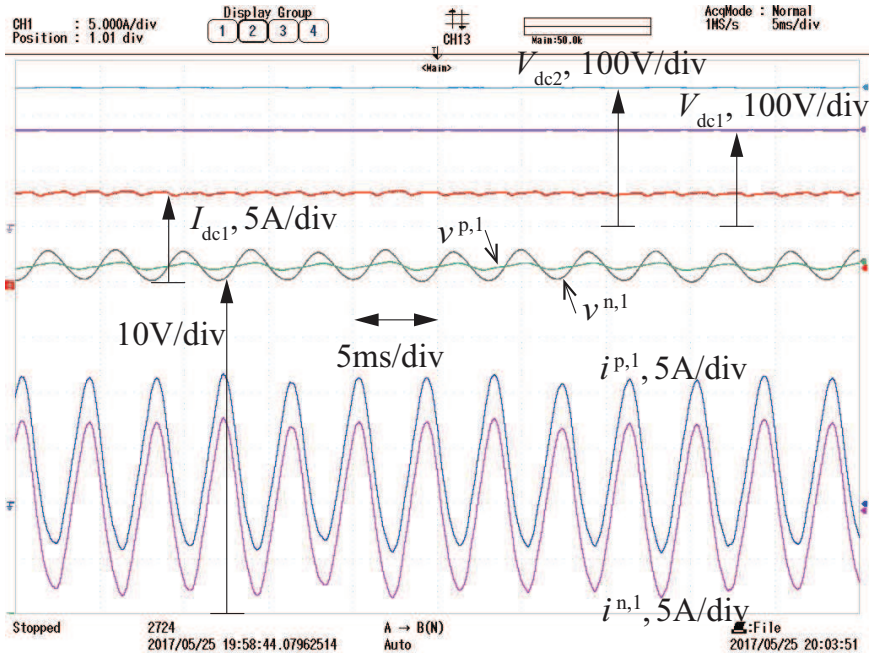
The dynamic response of the DC MMC to a power step change is provided in this section. The operating conditions of the prototype are provided in Table 6.5. The experiments include both buck and boost modes of operation to validate bidirectional operation of the DC MMC. In both modes of operation, the voltages of DC links 1 and 2 are maintained at 180 V and 240 V, respectively.

Table 6.5: Operating Condition for the Dynamic Response

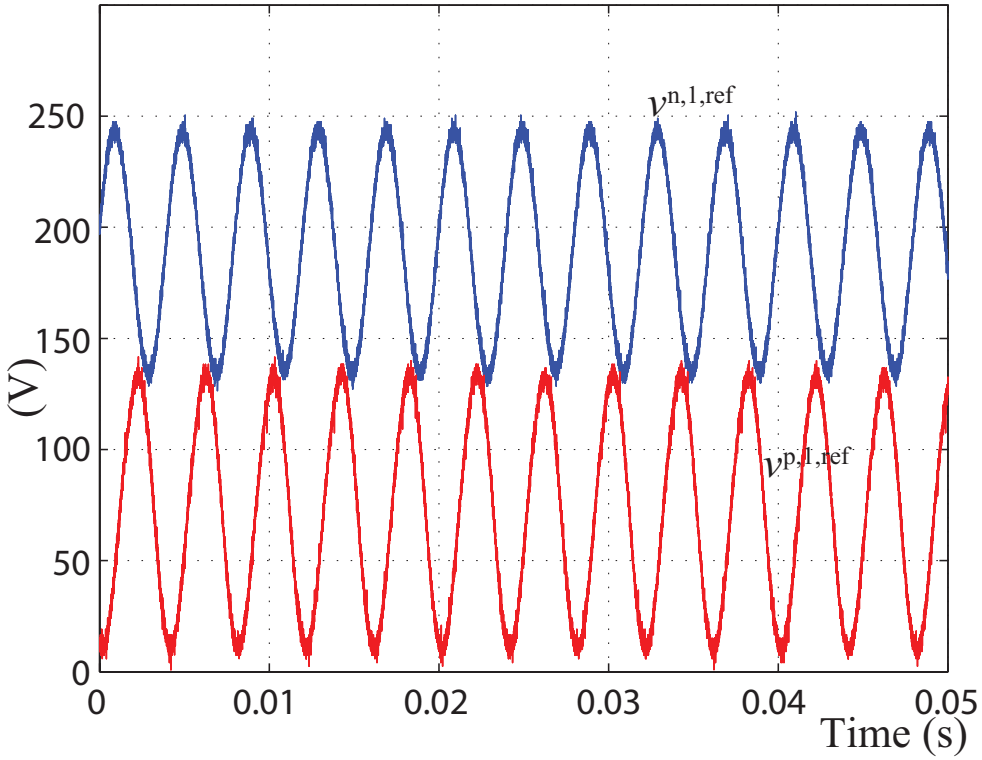
Parameters	**Value**
DC-link 1 voltage, V_{dc1}	180 V
DC-link 2 voltage, V_{dc2}	240 V

The experimental waveforms for boost mode of operation are shown in Fig. 6.6, in which the nominal SM capacitor voltage is 60 V. Under boost mode of operation, the DC power supply is connected to DC-link 1 to provide a constant voltage. The DC electronic load is connected to DC-link 2 to sink power while maintaining a constant bus voltage.

The experimental waveforms for power step-up and step-down scenarios are shown in Figs. 6.6(a) and (b), respectively. As shown in Fig. 6.6(a), initially, the DC MMC system is in steady state and I_{dc1}^{ref} is set to 3 A while $P = 540$ W is transferred from DC-link 1 to DC-link 2. At $t = 100$ ms, I_{dc1}^{ref} is changed to 5.5 A corresponding to 1 kW power throughput. To accommodate the step-up change of the DC-link 1 current, the DC component of the lower arm voltage is reduced. As discussed in Chapter 3, the peak values



(a)



(b)

Figure 6.5: Experimental results at $D = 0.7$.

of voltage references of both arms are maintained at their maximums to minimize the AC circulating current. The SM capacitor voltages in the upper and lower arms are maintained balanced by the closed-loop control strategy. It should be noted that under boost mode of operation, ϕ is limited within the range of $[\frac{\pi}{2}, \pi)$. Similarly, the experimental waveforms of the power step-down test shown in Fig. 6.6(b) confirm that the proposed control strategy is capable of controlling the converter power throughput, maintaining the SM capacitor voltages balanced, and minimizing the AC circulating current.

The experimental waveforms of buck mode of operation that include both power step-up and step-down scenarios are shown in Figs. 6.7(a) and (b), respectively. In the power step-up scenario, initially, $I_{\text{dc1}}^{\text{ref}}$ is set at -3 A to transfer -540 W power. At $t = 100$ ms, $I_{\text{dc1}}^{\text{ref}}$ is changed to -5.5 A to facilitate the power transfer of -1 kW as shown in Fig. 6.7(a). Similarly, in the power step-down scenario, a power step-down occurs at $t = 100$ ms from -1 kW to -540 W. As demonstrated in Fig. 6.7, in both scenarios, the capacitor voltages of the SMs of the upper and lower arms are maintained balanced. The AC circulating current is minimized by maintaining the AC component of the arm voltages at its maximum. The converter operates in the region of $\phi \in (\pi, \frac{3\pi}{2}]$ in buck mode of operation.

6.3 Control Strategy Validation for the Full-bridge SM Based DC MMC

In this section, the proposed enhanced control strategy in Chapter 4 is experimentally validated. Specifically, the capability of the proposed control strategy to reduce AC circulating current and SM capacitor voltage ripple, extend power transfer capability, and maintain SM capacitor voltage balance is evaluated experimentally. The experimental results for both steady-state operation and dynamic response are presented. Comparative evaluations of the enhanced control strategy with difference elevation coefficients are demonstrated in steady state.

6.3.1 Steady-state Operation

Two case studies are presented in this section for $D = 0.7$ and $D = 0.8$. In each case, experimental results are obtained for both $\zeta = 1$ and $\zeta = 1.2$. The experimental waveforms of the DC MMC in steady state at $D = 0.7$ where $\zeta = 1$ and $\zeta = 1.2$, are presented in Figs. 6.8(a) and (b), respectively. The operating condition of $D = 0.7$ is provided in Table 6.6. In both scenarios, $P = -1.6$ kW is transfered. As shown in Fig. 6.8(a), the average SM capacitor voltages of the upper and lower arms are maintained at 75 V at $\zeta = 1$. $\phi = 224°$ is generated by the controller to maintain energy balance of the SMs. The AC voltage components of the upper and lower arms are maintained equal in amplitude. The maximum value of the upper arm voltage is maintained at 300 V while the minimum value of the lower arm voltage is maintained at 0 V. In Fig. 6.8(b), 20% SM capacitor voltage elevation is enabled. Consequently, the average SM capacitor voltages are increased to 90 V. Due to the elevation of the SM capacitor voltages, the maximum voltage of the lower arm is increased to 360 V and the minimum voltage of the upper arm is reduced to -60 V as shown in Fig. 6.8(b). Compared to the experimental result at $\zeta = 1$, the AC circulating current and SM capacitor voltage ripple at $\zeta = 1.2$ are reduced significantly. The peak-to-peak amplitude of the AC circulating current at $\zeta = 1$ and $\zeta = 1.2$ are measured as 13.85 A and 8.32 A, respectively. The maximum peak-to-peak SM capacitor voltage ripple at $\zeta = 1$ and $\zeta = 1.2$ are measured as 5.83 V and 3.6 V, respectively. A 40% reduction in the AC circulating current and 38% reduction in the SM capacitor voltage ripple are achieved by 20% SM capacitor voltage elevation. Moreover, $\phi = 195°$ is generated by the controller at $\zeta = 1.2$. A 29° reduction is achieved compared to the case of $\zeta = 1$ for the same power level. The reduction in ϕ signifies an increase of the maximum converter power.

The experimental waveforms of the DC MMC in steady state at $D = 0.8$ where $\zeta = 1$ and $\zeta = 1.2$, are presented in Figs. 6.9(a) and (b), respectively. The operating condition is listed in Table 6.7. In both scenarios, $P = -1.8$ kW is transfered. As shown in Fig. 6.9, the average SM capacitor voltages of the upper and lower arms are maintained at 75

Table 6.6: Operating Condition for $D = 0.7$

Parameters	Value
DC-link 1 voltage, V_{dc1}	210 V
DC-link 2 voltage, V_{dc2}	300 V
DC-link 1 current , I_{dc1}	7.7 A

V and 90 V for $\zeta = 1$ and $\zeta = 1.2$, respectively. The peak-to-peak amplitude of the AC circulating current at $\zeta = 1$ and $\zeta = 1.2$ are measured as 16.23 A and 7.36 A, respectively. The maximum peak-to-peak SM capacitor voltage ripple at $\zeta = 1$ and $\zeta = 1.2$ are measured as 7.4 V and 3.3 V, respectively. A 54% reduction in the AC circulating current and 55% reduction in the SM capacitor voltage ripple are achieved by 20% SM capacitor voltage elevation. As shown in Fig. 6.9(a), the phase shift angle is maintained at 266° at $\zeta = 1$, which indicates that the converter operates near its maximum power transfer capability at $\phi = 270°$. By setting ζ to 1.2, A 70° reduction in ϕ is achieved, which translates to a significant increase of power transfer capability of the converter compared to the case of $\zeta = 1$.

Table 6.7: Operating Condition for $D = 0.8$

Parameters	Value
DC-link 1 voltage, V_{dc1}	240 V
DC-link 2 voltage, V_{dc2}	300 V
DC-link 1 current , I_{dc1}	7.7 A

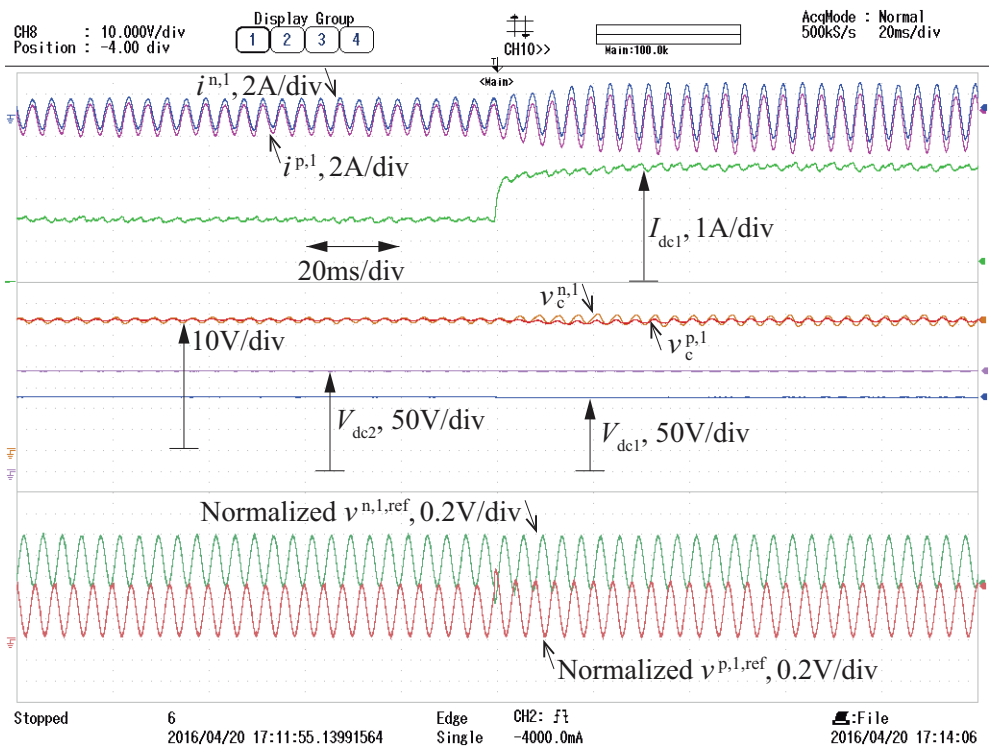
6.3.2 Dynamic Response

Dynamic response of the proposed control strategy is evaluated at $\zeta = 1.2$. The experimental waveforms for power step-up and step-down scenarios at $D = 0.8$ are shown in Figs. 6.10(a) and (b), respectively. In both scenarios, the DC-link 1 and DC-link 2 voltages are 240 V and 300 V, respectively. The SM capacitor voltages are maintained at 90 V. As shown in Fig. 6.10(a), initially, the DC MMC system is in steady state and I_{dc1}^{ref} is set to 4 A while $P = -1$ kW is transferred from DC-link 1 to DC-link 2. At $t = 100$ ms, I_{dc1}^{ref} is

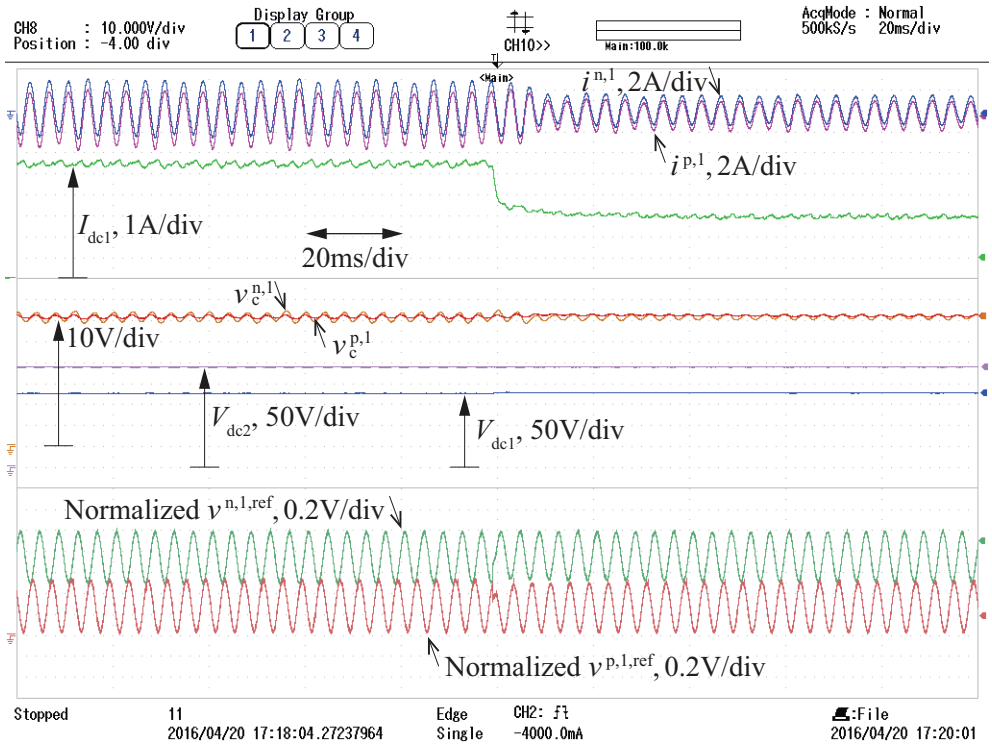
changed to 7 A corresponding to 1.7 kW power throughput. To accommodate the step-up change of the DC-link 1 current, the DC component of the lower arm voltage and ϕ are increased. The SM capacitor voltages in the upper and lower arms are maintained balanced by the closed-loop control strategy. In addition, the maximum voltage of the lower arm is maintained at 360 V and the minimum voltage of the upper arm is maintained at -60 V for AC circulating current minimization. Similarly, the experimental waveforms of the power step-down test shown in Fig. 6.10(b) confirm that the proposed control strategy is capable of controlling the converter power throughput, maintaining the SM capacitor voltages balanced, and minimizing the AC circulating current.

6.4 Chapter Summary

This chapter presents the development of a DC MMC prototype. The hardware design and control system implementation are presented. Experimental results are provided to validate the proposed control strategies.

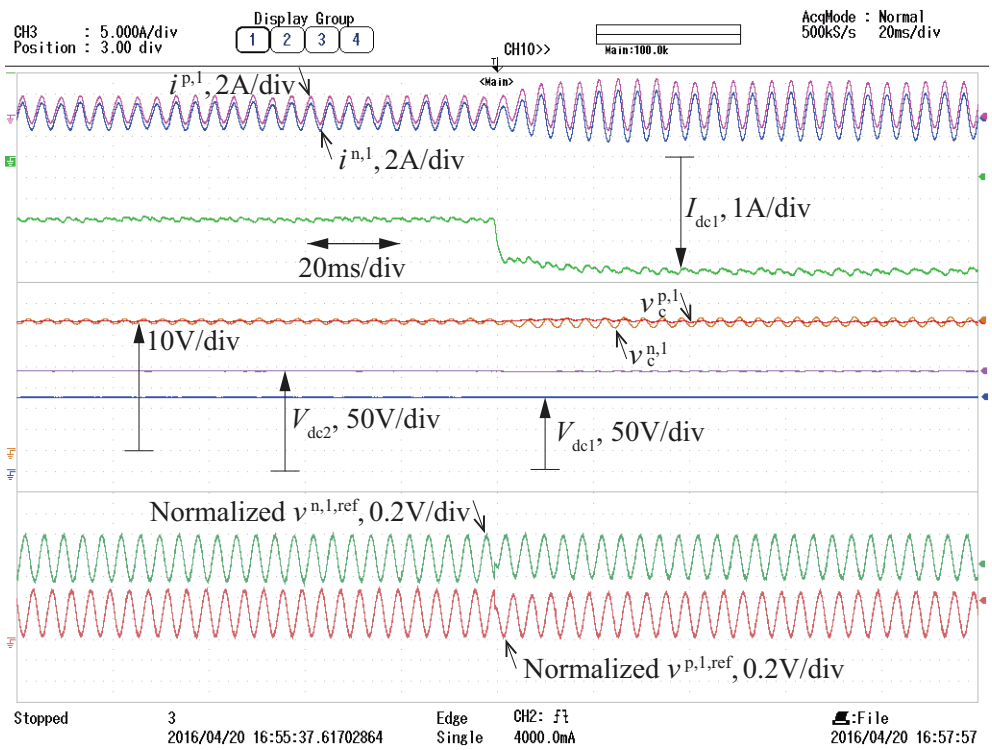


(a)

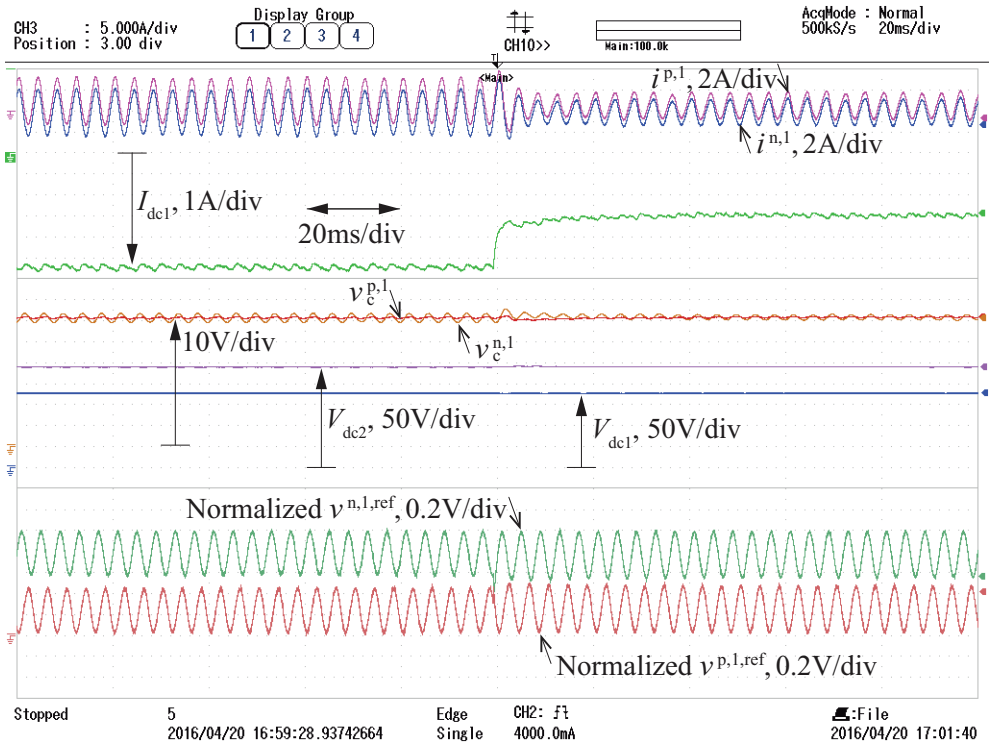


(b)

Figure 6.6: Experimental waveforms of the DC MMC in boost mode of operation for (a) power step-up and (b) power step-down scenarios.

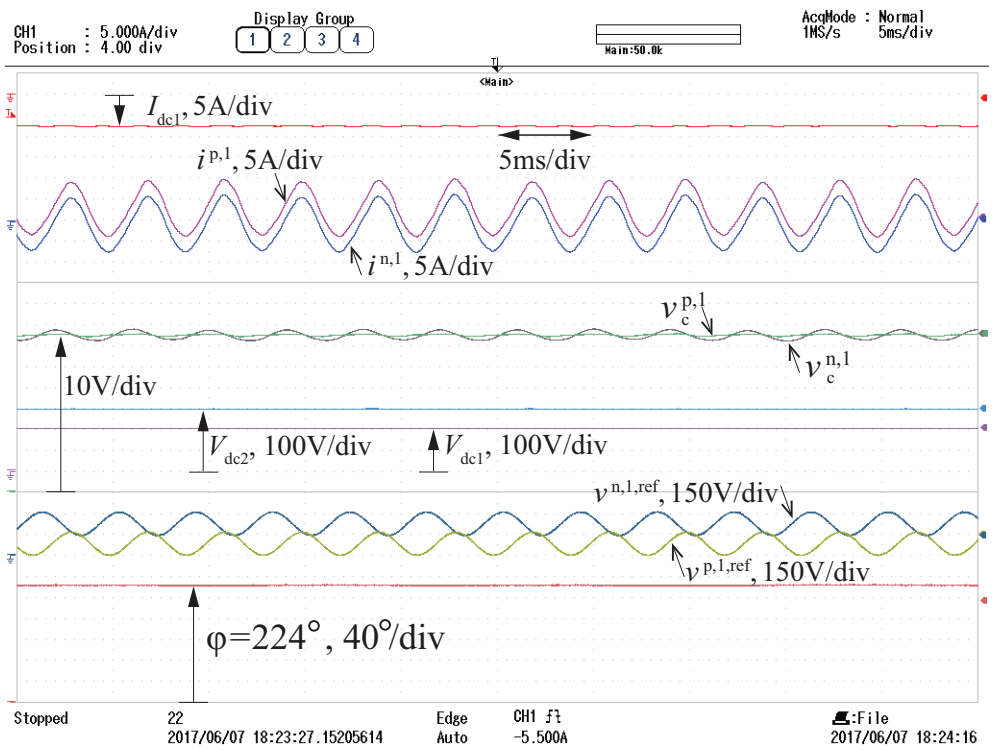


(a)

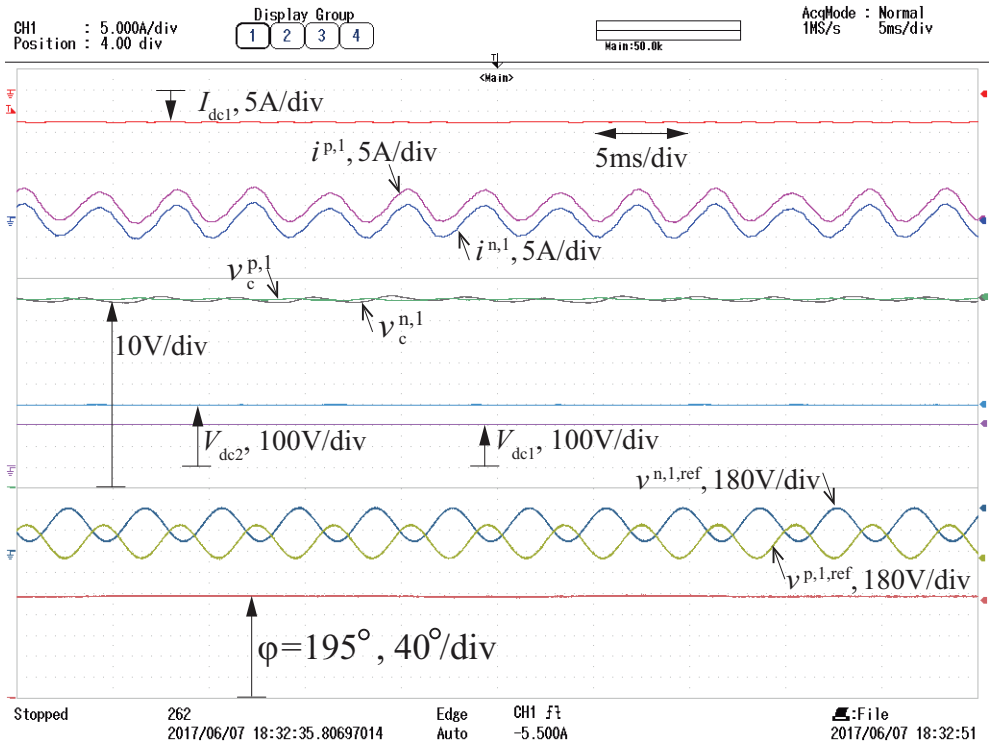


(b)

Figure 6.7: Experimental waveforms of the DC MMC in buck mode of operation for (a) power step-up and (b) power step-down scenarios.

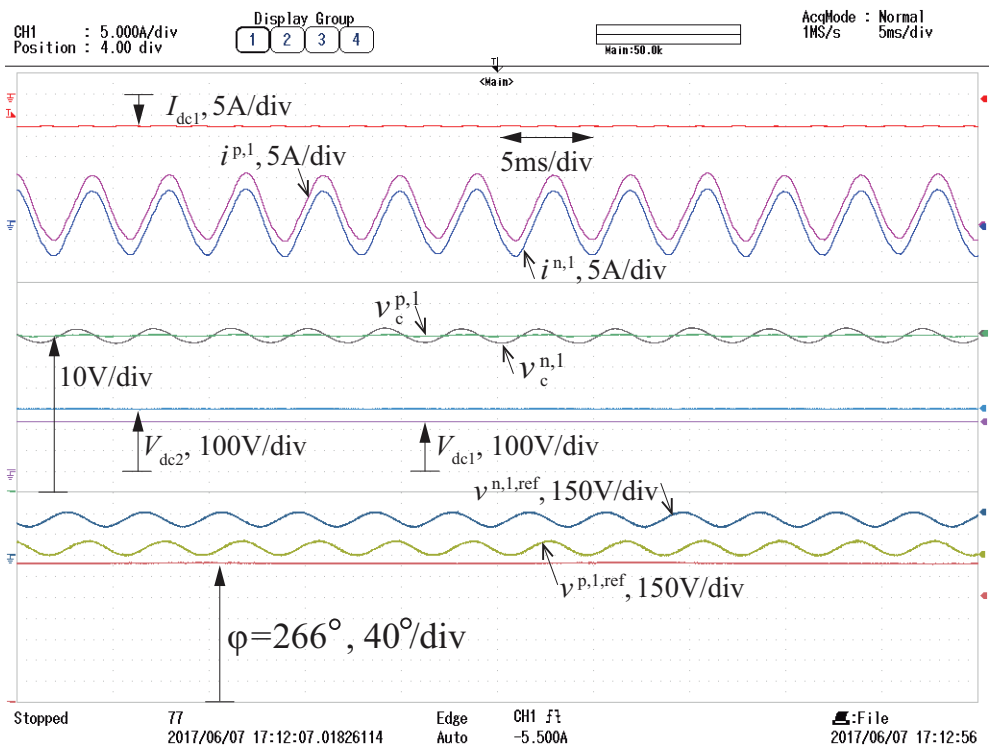


(a)

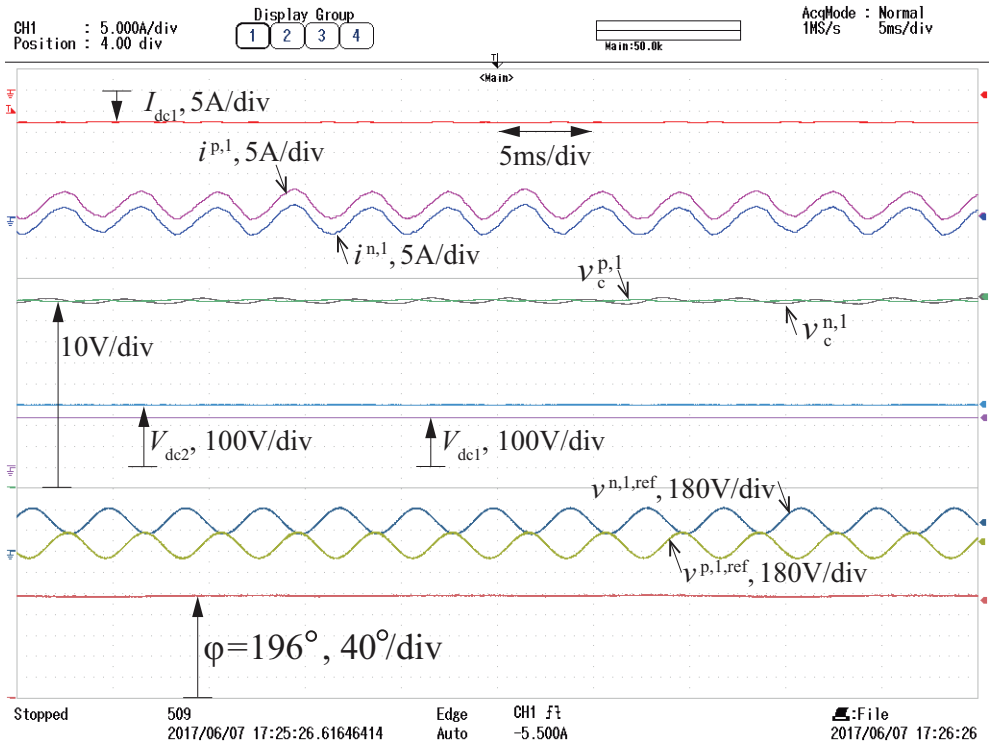


(b)

Figure 6.8: Experimental waveforms of the DC MMC at $D = 0.7$ with (a) $\zeta = 1$ and (b) $\zeta = 1.2$

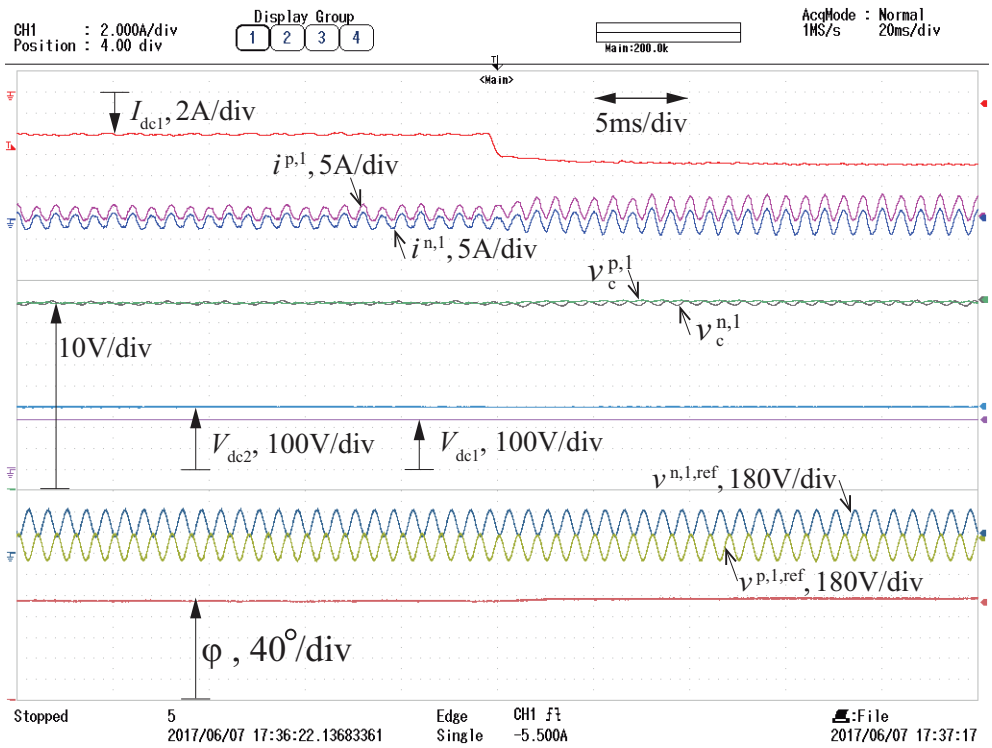


(a)

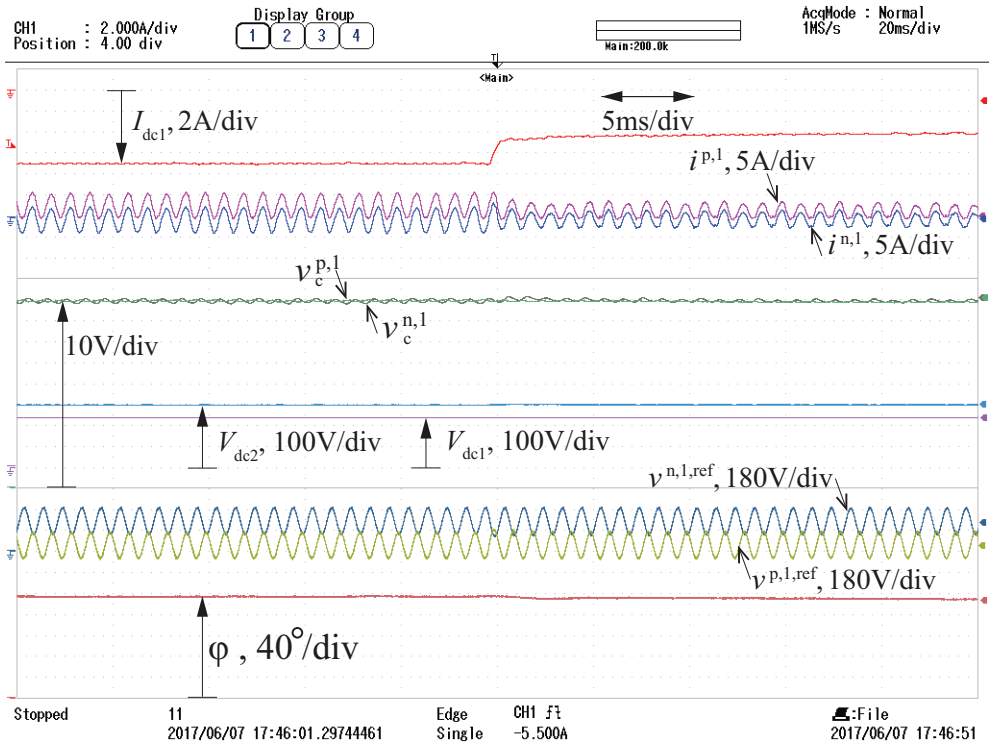


(b)

Figure 6.9: Experimental waveforms of the DC MMC at $D = 0.8$ with (a) $\zeta = 1$ and (b) $\zeta = 1.2$.



(a)



(b)

Figure 6.10: Experimental waveforms of the DC MMC at $D = 0.8$ for (a) power step-up and (b) power step-down scenarios.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

In this chapter, the contributions of this research and future work are discussed.

7.1 Contributions

The main contributions of this work are:

- A large-signal model of the DC MMC is developed in the phasor domain. The proposed analytical model captures key parameters of the converter in steady state. Furthermore, a dynamic model is developed for the SM capacitor voltages. The proposed dynamic model enables calculation of the SM capacitor voltage ripple in the time domain.

- A closed-loop control strategy is developed for the half-bridge SM based DC MMC. The DC MMC requires accurate control of the AC circulating current to maintain the energy balance of its SM capacitors. A detailed analysis is carried out to reveal the necessary conditions for minimization of the AC circulating current. The developed dynamic control strategy regulates the DC-link voltage/current while maintaining the SM capacitor voltage balance of the DC MMC over a wide range of voltage conversion ratios. The key advantage of the proposed control strategy is that minimum AC circulating current is attained for the half-bridge SM based DC MMC under arbitrary operating condition.

- A control strategy is developed to extend the power transfer capability and reduce AC circulating current of the DC MMC exploiting full-bridge SMs. The DC MMC suffers poor active switch utilization ratio and reduced power transfer capability at

voltage conversion ratios close to unity or zero. The developed control strategy allows the converter to operate with elevated SM capacitor voltage while maintaining the energy balance of its SM capacitors. The salient benefits of the proposed control strategy includes extended power transfer capability, reduced SM capacitor voltage ripple and AC circulating current, and improved active switch utilization.

- A constraints-oriented design approach is proposed for the DC MMC based on the developed analytical model. This design approach is the first systematic procedure for the new class of DC MMC. Design equations are derived for the arm inductor, inductive filter, and SM capacitor. A set of design constraints are identified that guarantees the proper operation of the converter. By following the proposed design procedure, sizes of all passive components are determined and the operating frequency is selected. The design process ensures that the converter meet its electrical specifications.

- A DC MMC prototype is developed. The effectiveness and abilities of the proposed control strategy is verified experimentally in terms of regulating DC-link voltage/current, maintaining energy balance of the SM capacitors, and minimizing the AC circulating current.

7.2 Future Work

The future work in the following areas include:

- Develop an optimization-oriented design approach for the DC MMC. The control strategy developed in Chapter 4 requires full-bridge SMs. The number of full-bridge SMs and elevation coefficient need to be selected based on a trade-off between the converter efficiency and cost. A large number of full-bridge SMs and elevation coefficient lead to further extended power transfer capability and reduced AC circulating current. However, more switches, capacitors, and driving circuitry are required,

which leads to increased cost. Furthermore, the number of SMs per arm and number of phase legs are also coupled with the converter cost. A optimization-oriented design approach that accounts for the SM capacitor voltage elevation should be developed to achieve optimized performance for the DC MMC.

- Experimentally validate the developed closed-loop control strategy for the full-bridge SM based DC MMC. In particular, the ability of the control strategy to extend the converter power transfer capability and reduce the AC circulating current need to be validated

- Develop a method to design the compensators used in the closed-loop control strategy. The parameters of the compensators should be selected such that the transient response of the DC MMC meet a given set of specifications.

- The DC MMC experiences unequal peak currents in the upper and lower arms. This translates to uneven power loss distribution among the semiconductor devices. The unequal temperature variations among the semiconductor devices in the upper and lower arms may compromise the reliability of the DC MMC. A control strategy/topology modification should be developed to balance the thermal stress of the semiconductor devices in the DC MMC.

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