RADIO FREQUENCY CIRCUIT DESIGN AND PACKAGING FOR SILICON-GERMANIUM HETROJUNCTION BIPOLAR TECHNOLOGY

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RADIO FREQUENCY CIRCUIT DESIGN AND PACKAGING FOR SILICON-GERMANIUM HETROJUNCTION BIPOLAR TECHNOLOGY

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In memory of my loved one, my dad:
Eng Hock Poh

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SUMMARY

The objective of this thesis is to design RF circuits using silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) for communication system. The packaging effect for the SiGe chip using liquid crystal polymer (LCP) is presented and methodology to derive the model for the package is discussed.

Chapter 1, we discuss the overview and benefits of SiGe HBT technology in high frequency circuit design.

Chapter 2 presents the methodology of the low noise amplifier (LNA) design and discusses the trade-off between the noise and gain matching. The technique for achieving simultaneous noise and gain matching for the LNA is also presented.

Chapter 3 presents an L-band cascaded feedback SiGe low noise amplifier (LNA) design for use in Global Position System (GPS) receivers. Implemented in a 200 GHz SiGe BiCMOS technology, the LNA occupies 1 x 1 mm^2 (including the bondpads). The SiGe LNA exhibits a gain greater than 23 dB from 1.1 to 2.0 GHz, and a noise figure of 2.7 to 3.3 dB from 1.2 to 2.4 GHz. At 1.575 GHz, the 1-dB compression point (P_{1dB}) is 1.73 dBm, with an input third-order intercept point (IIP3) of -3.98 dBm.

Lastly, Chapter 4 covers the packaging techniques for the SiGe monolithic integrated circuit (MMIC). We present the modeling of a liquid crystal polymer (LCP) package for use with an X-band SiGe HBT Low Noise Amplifier (LNA). The package consists of a 2 mil LCP laminated over an embedded SiGe LNA, with vias in the LCP serving as interconnects to the LNA bondpads. An accurate model for the packaging interconnects has been developed and verified by comparing to measurement results, and can be used in chip/package co-design.

Publications generated from this thesis are as follow:

1. J. C. H. Poh, P. Cheng, T. K. Thrivikraman, and J. D. Cressler, "A high gain, high linearity, L-band SiGe low noise amplifier with fully-integrated matching network," *IEEE Tropical Meeting on Silicon Monolithic Integrated Circuits in RF systems*, Jan 2010 (to appear).
2. C. H. J. Poh, T. K. Thrivikraman, S. K. Bhattacharya, C. E. Patterson, J. D. Cressler, and J. Papapolymerou, "An LCP package model for use in chip/packaging co-design of an X-band SiGe low noise amplifier," *IEEE Tropical Meeting on Electrical Performance of Electrical Packaging*, pp. 203-206, Oct 2009.
3. C. E. Patterson, T. K. Thrivikraman, S. Bhattacharya, C. H. J. Poh, J. D. Cressler, and J. Papapolymerou, Organic wafer-scale packaging for X-band SiGe low noise amplifier, *European Microwave Conference*, Oct 2009.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Modern wireless communication systems require higher broadband performance, high speed data transmission rate, low power consumption, low cost and multifunctional properties for a compact transceiver front ends in hand held set [1]. To meet the demand, low power and high efficient integrated circuits (IC) are being designed into wireless communication products.

Silicon-Germanium (SiGe) heterojunction bipolar transistor (HBT) has become a leading technology for radio frequency (RF) circuit design in recent years. SiGe ICs can be found in many communication applications such as the cellular handsets, wireless local area networks (WLAN) building blocks, from components to fully integrated systems ranging from 2.4 to 60 GHz, global position system (GPS), radar systems ranging from 3 to 77 GHz and etc. Figure 1 show the application of SiGe ICs at various frequencies. [2]

The recent development of SiGe HBT offers low-cost, high speed, and multifunctional solution for such system because of its potential for integrating RF microwave circuits and CMOS base-band circuits into a single chip. SiGe HBT has created opportunities leading to better performance, cost reduction of existing wireless communication systems, and providing opportunities for many applications towards higher frequencies and faster data rates.

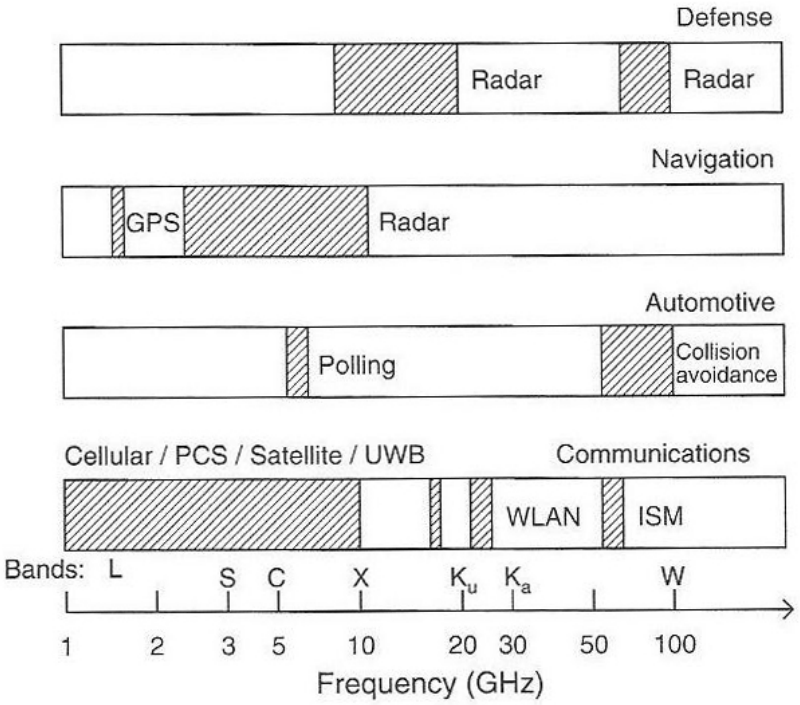


Figure 1. Application frequency bands for SiGe integrated circuit. [2]

1.2 Silicon-Germanium Heterojunction Bipolar Transitor Technology

For the past, III-V materials [3] such as Gallium Arsenide (GaAs) and Indium Phosphide (InP) have always been the core technology platform for monolithic microwave integrated circuit (MMIC) because of their higher electron mobility and electron velocity, allowing the transistors to operate at high frequency. However, it is difficult to integrate GaAs or InP with CMOS on a single wafer because there is no decent grown oxide for GaAs or InP and this makes fabrication process very complex and higher cost. Since the GaAs or InP does not provide a system-on-chip (SOC) solution and if the performance is acceptable, the use of silicon-base processing technology may be preferred to lower the cost. In fact, over the year, there have been many research activities to improve the performance of SiGe HBT to be on par with III-V devices for many RF and microwave applications and on top of that, the yield, the cost and the manufacturing advantages associated with conventional Si fabrication are still preserved.

There is always been a growing demand for lower power consumption in communication system because of the widely spread mobile communication system. SiGe HBT on the other hand, can operate at a higher f_T [3] with a lower collector current density (J_c) than other conventional silicon-based products as shown in Figure 2.

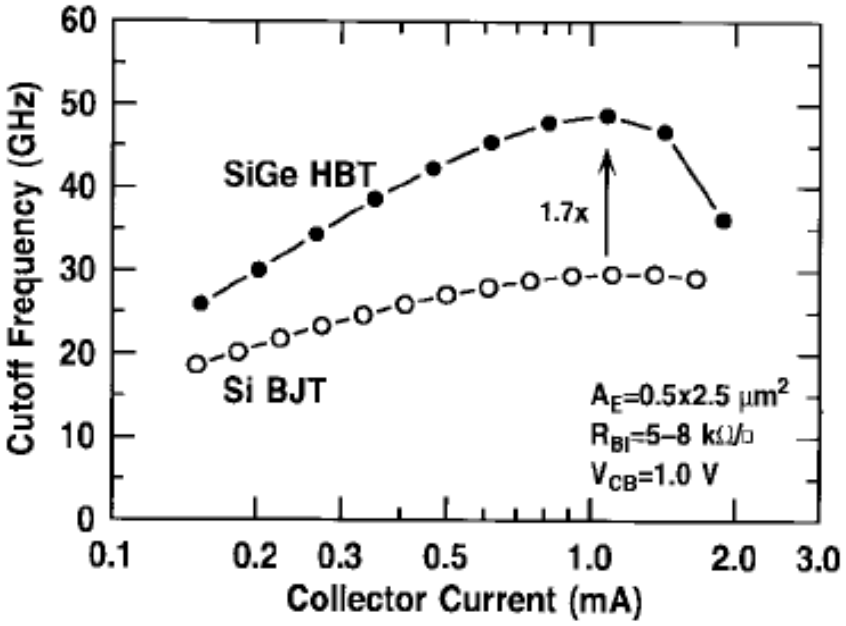


Figure 2. Comparision of the cutoff frequency as a function of bias current for a SiGe HBT and a Si BJT of comparable doping profile. [3]

Noise performance of SiGe HBT is an advantage over CMOS for RF circuit designs. The 1/f noise due to carrier trapping-detrapping at interface states and thermal noise due to gate and channel resistances are both significantly higher in CMOS than in SiGe HBTs. Very often, very large CMOS devices and large operating current are required to reduce the noise.

Therefore, it can be shown that the SiGe is a promising candidate for many RF and microwave circuit applications. In this thesis, an L-band low-noise amplifier (LNA) designed based on SiGe HBT will be covered. Towards the end of the thesis, the packaging issues of a SiGe LNA at X band will be covered.

Over the year, SiGe HBT has been distinguished between different technology generations according to their ac performance, such as unity gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) [4].

1. First Generation – SiGe HBT with a peak f_T in the range of 50 GHz.
2. Second Generation – SiGe HBT with a peak f_T in the range of 100 GHz.
3. Third Generation - SiGe HBT with a peak f_T in the range of 200 GHz.
4. Fourth Generation – SiGe HBT with a peak f_T in the range of 300 GHz.

Figure 3 shows the measured fmax versus f_T for a variety of generation of SiGe HBT BiCMOS technology.

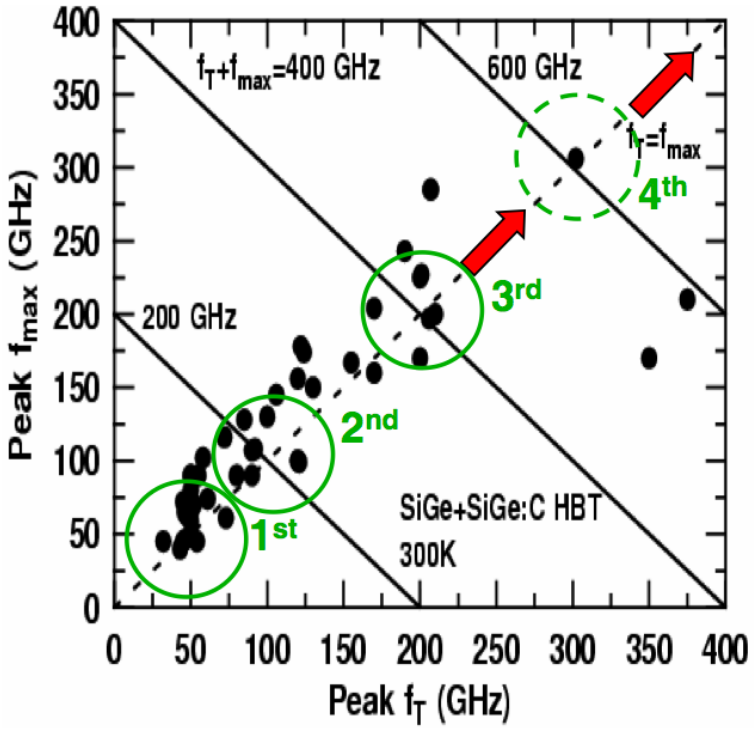


Figure 3. Measured f_{max} verus f_T for a variety of generation of SiGe HBT BiCMOS Technology. [4]

The SiGe HBT technology used in this thesis is based on the third generation, IBM SiGe 8HP.

1.3 Organization of Thesis

This thesis explores the use of SiGe HBT for RF applications. The subsequent chapters will cover on the LNA design using SiGe HBT and also packaging of SiGe LNA using LCP. Chapter 2 of the thesis will cover the basic idea of designing a low-noise amplifier (LNA) using SiGe HBT BiCMOS technology. The LNA consists of a single-end cascoded structure and how both gain and noise matching can be achieved simultaneously. Chapter 3 of the thesis will talk about an L-band LNA with feedback network and measurement result. Chapter 4 will discuss on SiGe packaging issues such as wire bonds and embedded SiGe chip in liquid crystal polymer (LCP) substrate. Chapter 5 will summarize the results of all the works and discuss future research direction.

CHAPTER 2

LNA DESIGN IN SiGe HBT BICMOS TECHNOLOGY

2.1 Introduction

In a wireless communication system, the LNA is one of the most important circuit blocks in the receiver. The role of the LNA is to amplify the signal received at the antenna while adding as little noise as possible to the receiver so that the retrieval of the received signal is possible in the later stages in the receivers [5]. The sensitivity of the receiver is determined by the noise figure and power gain of the LNA. The noise figure has an impact on the overall noise performance of the receiver. On the other hand, the power gain significantly suppresses noise contributions from the subsequent stages. All these can be observed in the Friis equation in (1).

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \quad (1)$$

F_i represents the noise factor of the i^{th} component in a receiver chain while Gi is the gain of the i^{th} components. From the equation, it can be shown that the noise figure of the first stage which is usually the LNA, dominants the total noise figure in the receivers, assuming the LNA has a large gain G_1. Therefore, the receiver noise figure performance depends primarily on the LNA.

There are several works on LNA designs over the years. The DC power supply has becomes smaller in RF designs and hence the power consumption of the LNA has to be as small as possible and yet the performance has to be maintained at the same time. LNA design has always been challenging and tradeoffs are to be made between the sizes, the cost and the performance.

2.2 Single-ended Cascode Low Noise Amplifier Design

The LNA in this thesis is implemented as a single-ended cascode amplifier [6].

The first stage is a common-emitter (CE) configuration and the second stage is a common-base (CB) configuration. The cascode transistor Q2 prevents the Miller effect from degrading the power gain and also improves the reverse isolation, and improves stability of the LNA. Figure 4 shows the small-signal equivalent circuit for the transistors Q_1 and Q_2 in a cascode configuration.

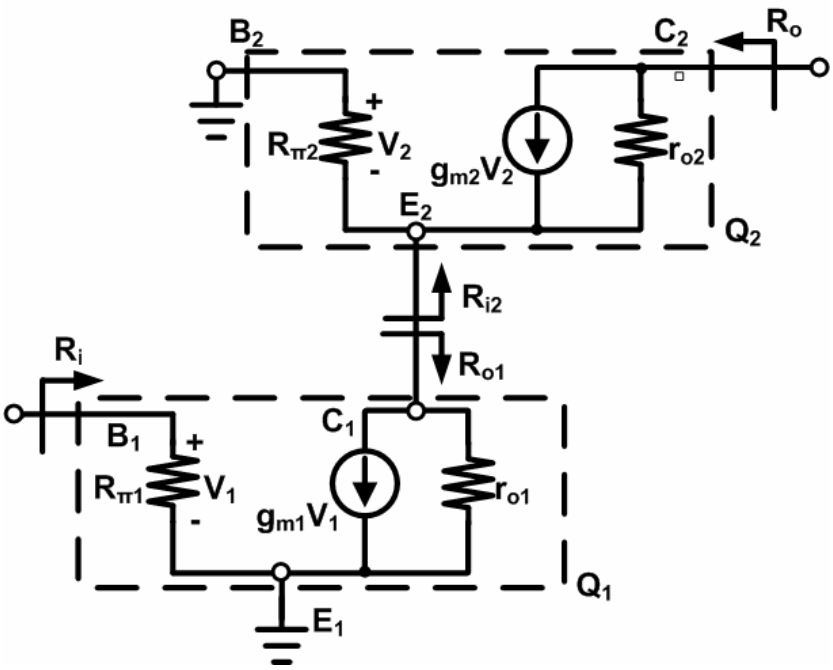


Figure 4. Small-signal equivalent circuit for the transistors Q_1 and Q_2 in a cascode configuration.

The output resistance [6] looking into the collector of Q_1 is given by

$$R_{o1} = r_{o1} \tag{2}$$

and the input resistance looking into the emitter of Q_2 is

$$R_{i2} = r_{e2} = \frac{1}{1+\beta_2} r_{\pi 2} \approx \frac{r_{\pi 2}}{\beta_2} \tag{3}$$

The voltage gain for the first stage, assuming transistor Q_1 and Q_2 are equally sized, is

$$A_{v1} = -g_{m1} r_{o1} // R_{i2} \approx -1 \tag{4}$$

The total output resistance of the cascode structure is given by

$$R_o \approx r_{o2} \left(1 + \frac{g_{m2} r_{o1}}{1 + \frac{g_{m2} r_{o1}}{\beta_o}} \right) \tag{5}$$

Since $g_{m2}r_{o1} >> \beta_o$ and $\beta_o >> 1$, (5) can be simplified to

$$R_o \approx r_{o2} \beta_o \tag{6}$$

The total transconductance of the cascode structure is given by

$$G_m = g_{m1} \tag{7}$$

From (6) and (7), the total voltage gain A_v for the cascode structure is thus

$$A_v \approx G_m R_o \approx g_{m1} r_{o2} \beta_2 \tag{8}$$

From (8), it can be shown that the magnitude of the maximum available voltage gain of a cascode pair is higher by a factor β_2 than for the case of a single transistor.

2.3 Noise and Gain Matching of the Low Noise Amplifier

The noise figure [7] of a noisy block can be expressed by

$$NF = NF_{\min} + \frac{R_n}{G_s} \left[\left(Y_s - Y_{s,opt} \right) \right] \tag{9}$$

where R_n is the equivalent noise resistance, G_s is the conductance of the input source, Y_s is the admittance of the input source and $Y_{s,opt}$ is the optimum admittance of input source. The noise two ports block can reach a minimum noise figure if

$$NF = NF_{\min} \tag{10}$$

when

$$Y_s = Y_{s,opt} \tag{11}$$

and

$$\Gamma_s = \Gamma_{s,opt} \tag{12}$$

where Γ_s is the source reflection coefficient and $\Gamma_{s,opt}$ is optimum the source reflection coefficient.

However in most situations, an LNA with maximum gain may not be in the state of minimum noise, or vice versa and therefore, trade-off has to be made between the maximum gain and minimum noise figure [8]. In the past, much effort has been made to design the LNA to reach both maximum gain and minimum noise figure simultaneously, and this poses a huge challenge for designing a good LNA.

The basic principle of designing the LNA is which both the maximum gain and the minimum noise can come together at one point one on the smith chart such that

$$\Gamma_{s,opt} = S11^* \tag{13}$$

where $\Gamma_{s,opt}$ is the optimum source reflection coefficient, looking from the transistor toward the source at which the noise figure is the minimum and $S11^*$ is the conjugate of S11 which is the input port voltage reflection coefficient as shown in Figure 5.

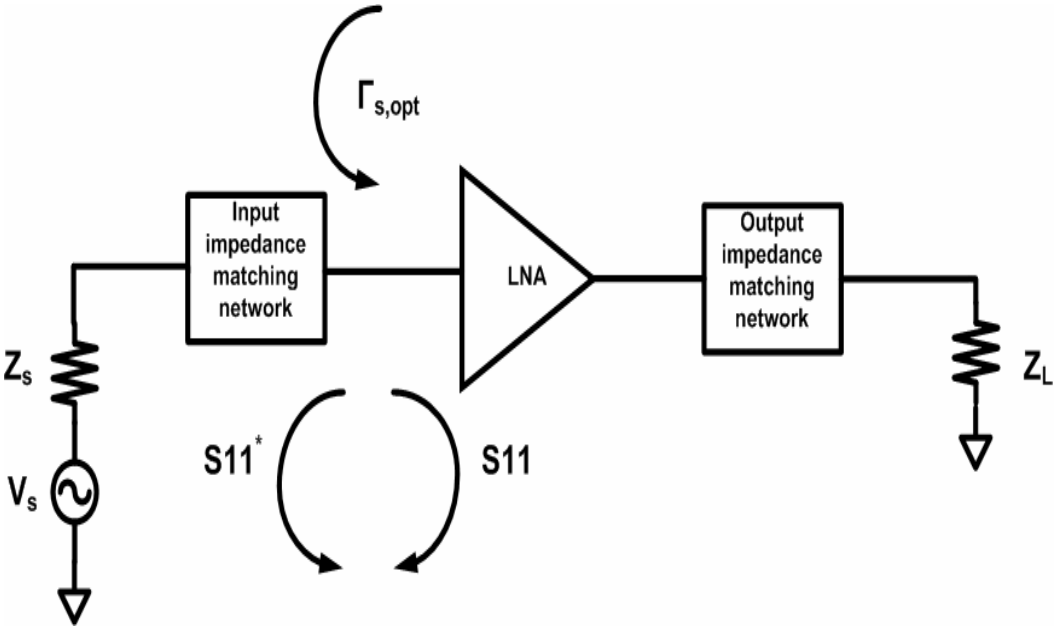


Figure 5. Direction of $\Gamma_{s,opt}$, S_{11} and S_{11}^* in the LNA schematic

Generally, three approaches [8] can be used in order to achieve (13).

1. Increasing or decreasing the collector current, I_c. The S parameter as well as the values of $\Gamma_{s,opt}$ changes as the I_c is varied, and hence the condition in (13) could be achieved with the appropriate amount of I_c.
2. Changing the emitter length. Again, the condition in (13) could be achieved with the appropriate device size.
3. Emitter degeneration. By adding the degenerate inductance to the emitter of the transistor, the input impedance of the transistor changes and this could also lead to the condition in (13).

The equation (13) represents the conditions by which the LNA with minimum noise figure and maximum gain can be simultaneously approached after the input and output impedance matching networks are implements.

The basic idea is to bring the minimum noise circle and maximum gain circle together at the same point on the smith chart.

2.4 Low Noise Amplifier Design Procedure

This section will cover the steps to design an inductively degenerated cascode LNA [9]. Firstly, the collector current density (J_c) of the transistor has to be determined.

$$J_c = \frac{I_c}{L_e W_e} \tag{14}$$

where I_c is the collector current, L_e is the emitter length and W_e is the emitter width.

As shown in Figure 6, by sweeping the collector current and keeping L_e and W_e constant, the current gain H_{21} and the NF_{min} of the transistor vary and the optimum collector current density is then selected [10].

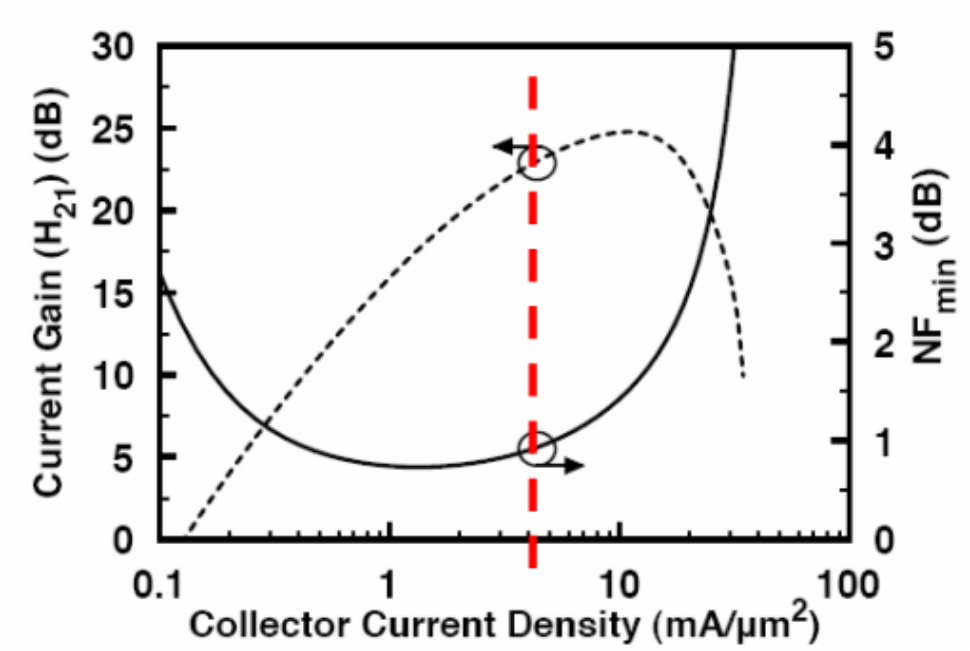


Figure 6. Current gain (H_{21}) and NF_{min} as a function of collector current density [10].

After the J_c is determined, the L_e of the transistor is tuned such that condition in (13) can be met. If the condition in (13) is not achievable after tuning L_e, a degenerated-inductance can be added to the emitter of the transistor and this will change the input impedance of the transistor so that condition in (13) can be achieved.

Once the condition in (13) is met, the input and output impedance matching networks can be added to bring the LNA to 50Ω match.

Figure 7 show the design flow chart of the LNA [8].

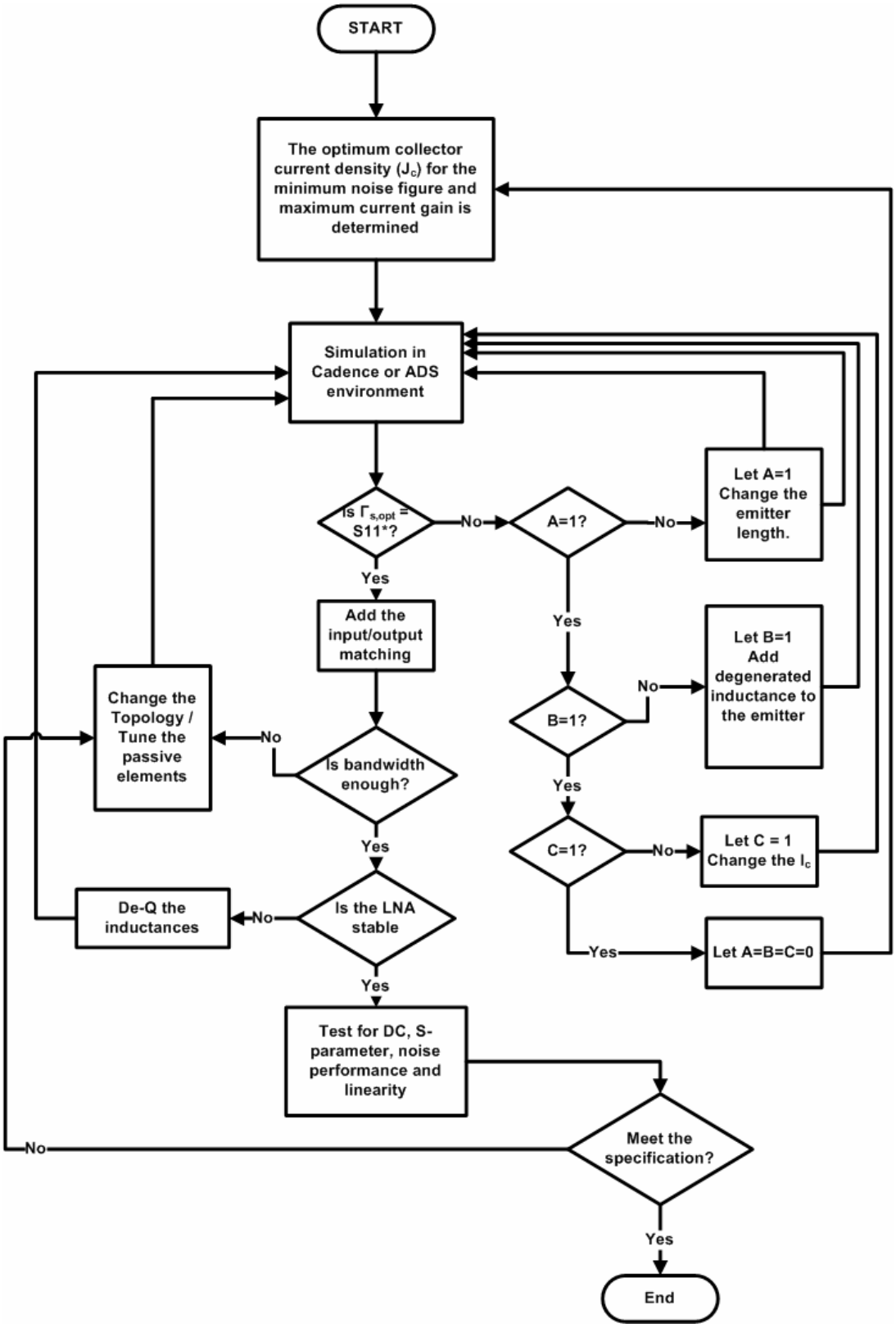


Figure 7. Flowchart of the LNA design [8].

CHAPTER 3

L-BAND LNA

3.1 Introduction

Built-in Global Positioning System (GPS) capability is increasingly becoming a standard feature for cellular handset and other low-cost embedded applications. The requirements for these systems provide a strong motivation for developing highly integrated and low-cost GPS receivers. Low-noise amplifiers (LNAs) in GPS receivers are often the most challenging block to implement, given the difficulty of simultaneously achieving sufficient gain, low noise figure, and low power consumption.

Typically, GPS receivers operate in the L-band frequency range (1575.42 MHz (L1), 1227.60 MHz (L2), 1381.05 MHz (L3) and 1176.45 MHz (L5)). Designing a monolithic LNA at L-band poses significant challenges due to the large size of the passive components, making it difficult to implement the LNA with its requisite matching networks on-die.

Silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) [11] are attractive for analog, mixed-signal and RF applications because they exhibit very low noise figure and very high power gain, at modest power dissipation levels, which can be leveraged to improve the sensitivity of receiver front-ends. SiGe HBT technology utilizes bandgap engineering to improve transistor performance, and at present peak cutoff frequency (fT) and peak maximum oscillation frequency (fmax) greater than 300 GHz have been achieved at modest lithographic feature size (130 nm), while maintaining compatibility with the traditional CMOS processes

In this thesis, a high gain, L-band SiGe LNA with fully-integrated on-chip matching networks is presented. At 1.575 GHz, the LNA achieves a gain of 26 dB, a NF of 3.2 dB, while dissipating 17.89 mW of dc power.

3.2 Single-ended Cascoded LNA with Feedback Network Design

In Figure 8, the schematic of an L-band LNA is shown. The optimum collector current density (J_c) at minimum noise figure (NF_{min}) was first determined with equally sized transistors Q_1 and Q_2 [9]. By maintaining a constant J_C, the emitter lengths of Q_1 and Q_2 were then scaled so that $\Gamma_{s,opt}$ is closer to the conjugate of S_{11}, which leads to simultaneous impedance matching for both NF_{min} and maximum gain (G_{max}). The capacitances C_{in} and C_{out} act as DC blocks, and the inductances L_b and L_c act as RF chokes, and are used as part of the matching network to match the LNA to 50 Ω at 1.575 GHz. Tables I shows the device sizes for the LNA.

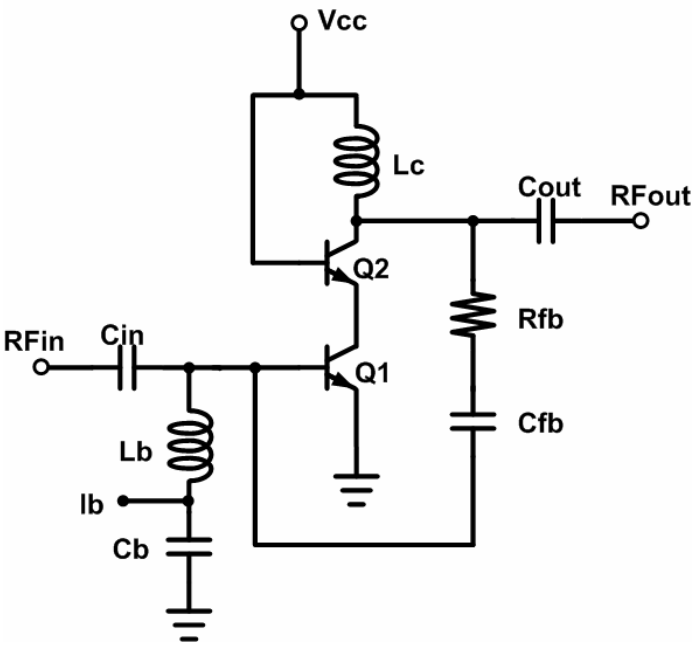


Figure 8. Schematic of the L-band SiGe LNA.

TABLE 1

DEVICE SIZES FOR THE L-BAND SiGe LNA

Parameter	Device Sizes
$\mathbf{C_{in}}$	2 pF
$\mathbf{L_b}$	7.3 nH
$\mathbf{C_b}$	10 pF
$\mathbf{L_c}$	13.5 nH
$\mathbf{R_{fb}}$	4.8 kΩ
$\mathbf{C_{fb}}$	11.5 pF
$\mathbf{C_{out}}$	976.8 fF
$\mathbf{Q_1}$	0.12 x 10 μm^2
$\mathbf{Q_2}$	0.12 x 10 μm^2

The feedback topology [12] for the LNA uses a shunt-shunt configuration with both the resistance R_{fb} and the capacitance C_{fb} connected in series. Adding the feedback network to the LNA improves stability, eases the match, and broadens the bandwidth of the LNA.

For the shunt-shunt feedback amplifier, the open-loop gain or transresistance gain is given by

$$A = \frac{V_{out}}{I_{in}} \tag{15}$$

The feedback factor B_f is given by

$$B_f \approx \frac{1}{R_{fb}} \tag{16}$$

where Rfb >> $\frac{1}{j\omega C_{fb}}$

With the feedback network, the closed-loop gain of the amplifier is given by

$$A_{close} = \frac{A}{1 + AB_f} \tag{17}$$

and if $AB_f >> 1$, (17) can be simplified to

$$A_{close} \approx \frac{1}{B_f} = R_{fb} \tag{18}$$

The closed-loop input impedance of the feedback amplifier is given by

$$Z_{if} = \frac{R_i(R_{fb})}{R_{fb} + A} \tag{19}$$

The closed-loop output impedance of the feedback amplifier is given by

$$Z_{of} \approx \frac{R_o(R_{fb})}{R_{fb} + A} \tag{20}$$

Hence, from (18), (19) and (20), R_{fb} can be optimized for maximum gain, and at the same time, brings the input and output impedance closer to 50 Ω.

This feedback network improves the linearity of the amplifier [13]. From (17), for a small deviation, ΔA, in the signal, the closed-loop gain is given by

$$A_{close} = \frac{A + \Delta A}{1 + (A + \Delta A)B_f} \approx \frac{A}{1 + AB_f} + \frac{\Delta A}{1 + AB_f} \tag{21}$$

Hence, from (21), it can be shown with the feedback network the deviation ΔA from linearity is reduced by a factor of

$$\frac{1}{1 + AB_f} \tag{22}$$

However, the feedback network may also adversely affect the noise figure performance of the LNA. When the resistance R_{fb} is added, there is a resistive loading effect at the LNA input, as shown in Figure 9. Assuming that the gain at Q_1 is greater Q_2, the equivalent noise input current, I_{ni} for a shunt-shunt feedback amplifier [14] is given as

$$I_{ni} = \left[\frac{4kT\Delta f}{R_s // R_{fb}} \left(1 + \frac{r_x}{R_s // R_{fb}}\right) + 2qI_B\Delta f \left(1 + \frac{r_x}{R_s // R_{fb}}\right)^2 + 2qI_c\Delta f \left[\frac{1}{\beta} + \frac{1}{R_s // R_{fb}} \left(\frac{r_x}{\beta} + \frac{V_T}{I_c} \right) \right]^2 \right]^{\frac{1}{2}} \tag{23}$$

Hence from (23), in order to minimize the effects of the feedback network on the noise figure performance, R_{fb} needs to be made large compared to the source impedance R_s at the LNA input.

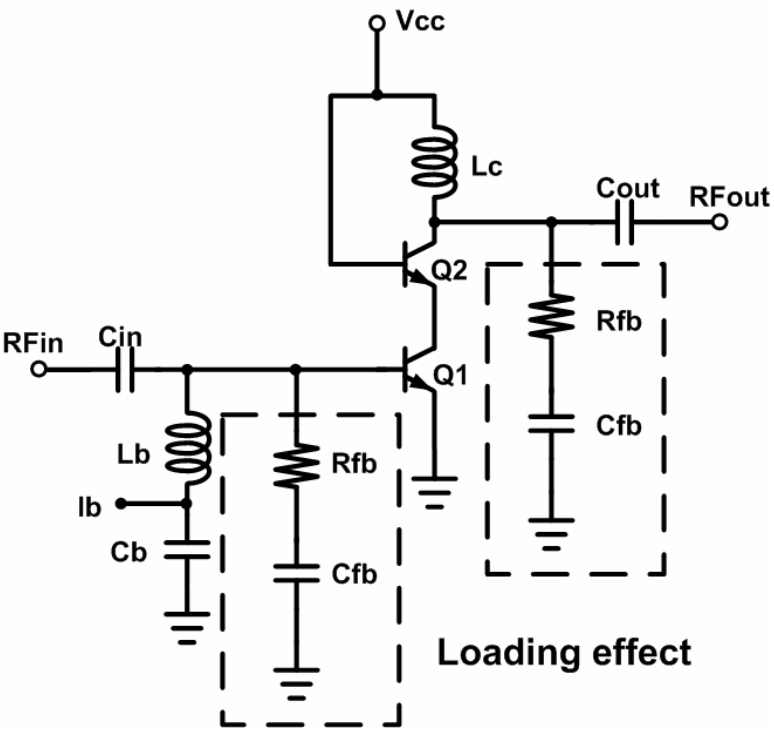


Figure 9. Schematic of the L-band SiGe LNA with loading effect due to the feedback network.

3.3 L-Band Measurement Result

The LNA was designed to operate off of a supply voltage as low as V_{cc}=1.5 V and I_c=11.9 mA, yielding a total power dissipation of 17.89 mW. The LNA was measured on-wafer using ground-signal-ground (GSG) coplanar microwave probes, with probe-level calibration used to account for cable losses. Figure 10 shows the photomicrograph of the fabricated LNA die, and the total die area including the bond pads is 1 x 1 mm^2.

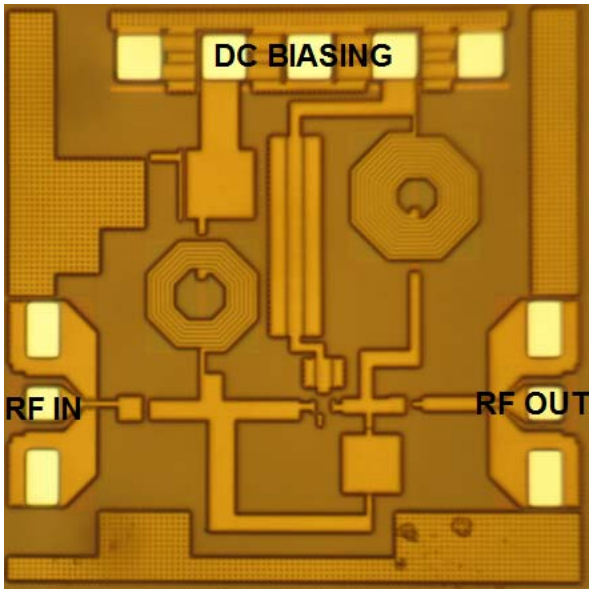


Figure 10. Photograph of the fabricated L-band SiGe LNA.

The S-parameters of the LNA were measured on-wafer using an Agilent E8361C Network Analyzer. Figure 11 shows the measured and simulated gain and the isolation of the LNA. The LNA achieves a peak gain of 26 dB at 1.575 GHz, and from 1.1-4.0 GHz, it maintains a gain above 22 dB. The reverse isolation of the LNA is more than 35 dB from 1 to 4 GHz indicating good stability.

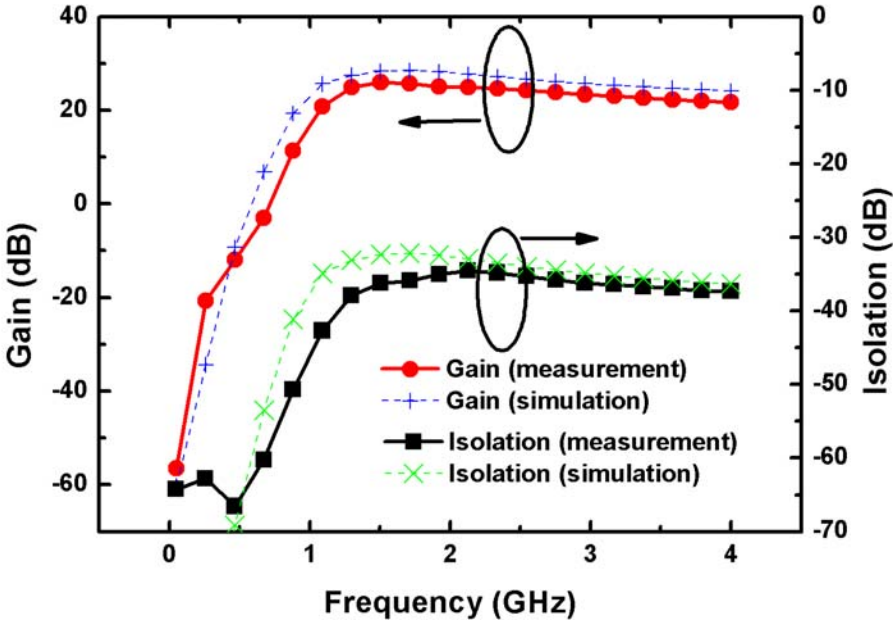


Figure 11. Measured and simulated gain and isolation (S_{21} and S_{12}).

The LNA exhibits a good 50 Ω match and Figure 12 shows that the measured and simulated input return loss (S_{11}) and the output return loss (S_{22}) are less than -10 dB from 1.1-1.9 GHz.

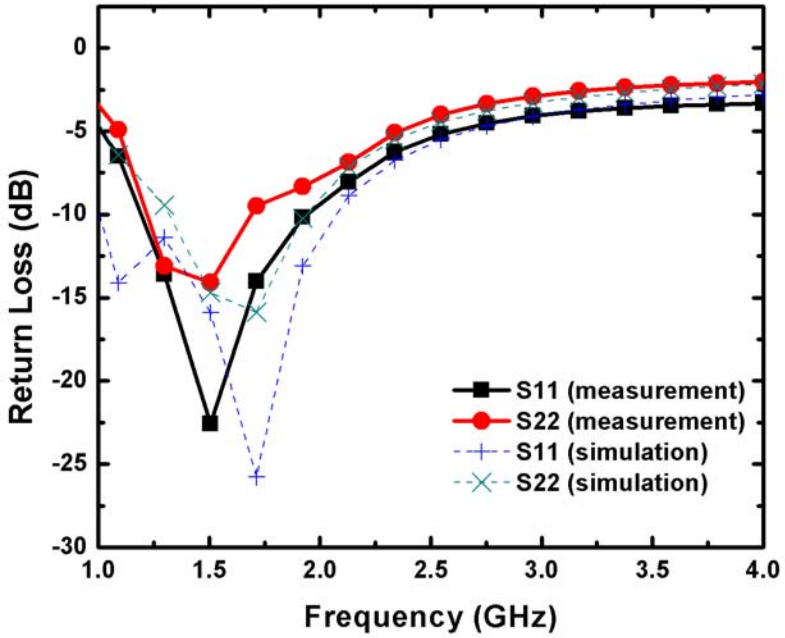


Figure 12. Measured and simulated input and output return loss (S_{11} and S_{22}).

Noise figure (NF) was measured using the noise figure option of the Agilent E4446A spectrum analyzer. As shown in Figure 13, the LNA achieves a NF of 2.7-3.3 dB from 1.2 to 2.4 GHz.

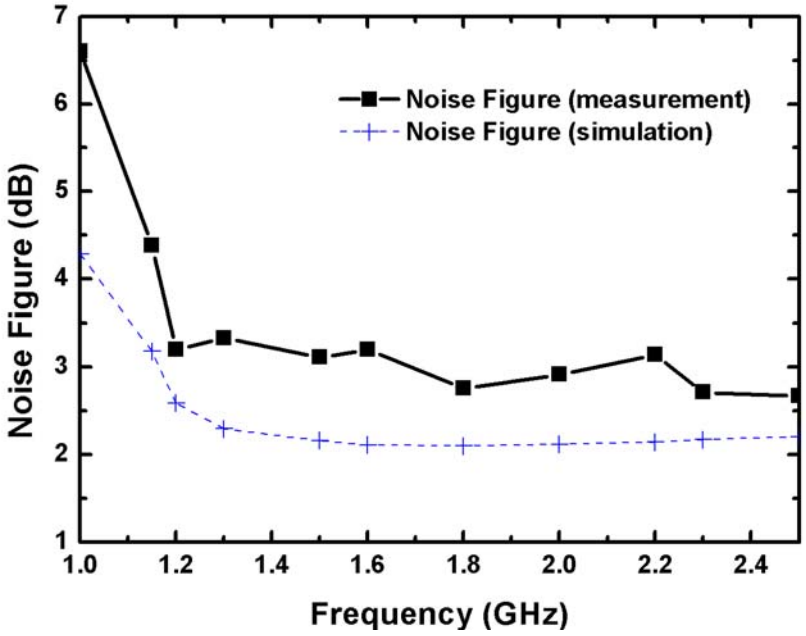


Figure 13. Measured and simulated noise figure of the LNA.

The third-order intercept point (IIP_3) and the output 1-dB gain compression point (P_{1dB}) were measured to evaluate the linearity of the LNA. Figure 14 plots the measured and simulated IIP_3 for a two-tone test using Agilent E8316C Network Analyzer. The extrapolated input third-order intercept point IIP_3 is -3.98 dBm, with the fundamental frequency at 1.575 GHz, with the second tone at 1.567 GHz. Figure 15 shows that the measured and simulated output P_{1dB} is 1.73 dBm at 1.575 GHz.

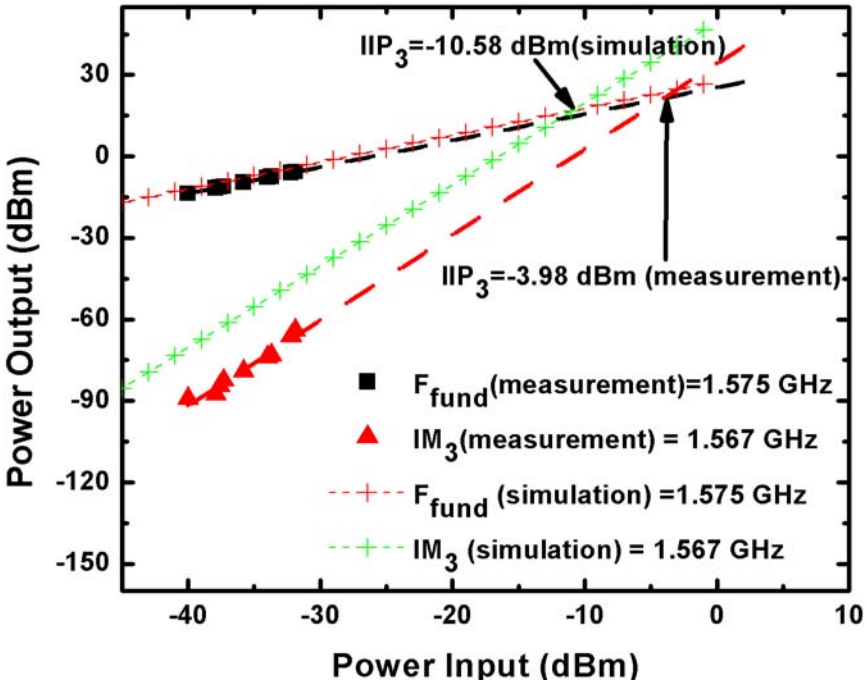


Figure 14. Measured and simulated third-order intercept point.

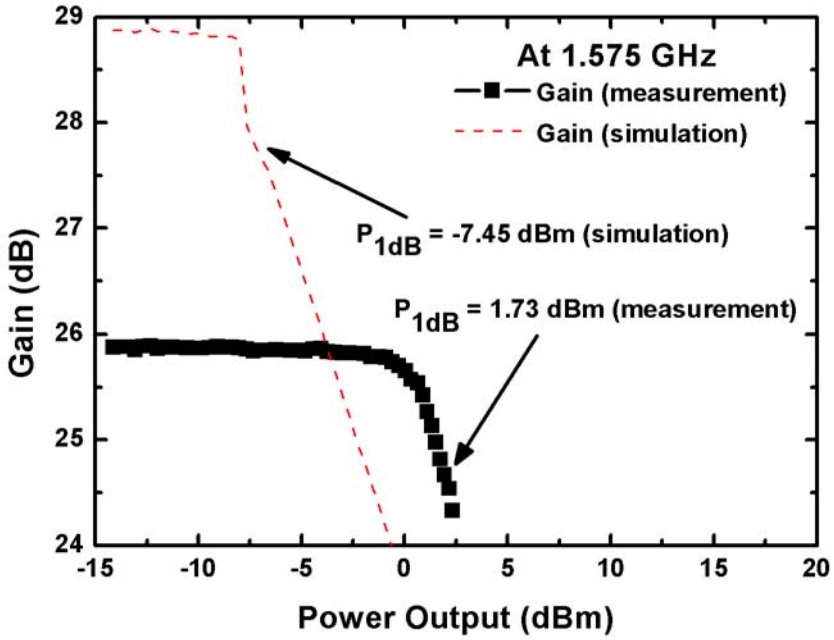


Figure 15. Measured and simulated output 1-dB gain compression.

A comparison of the present work with other LNAs operating in the L-band is summarized in Table I. An LNA figure-of-merit (FOM) [15] was calculated to

benchmark the LNAs listed in Table I. The FOM in (24) takes into account the gain, linearity, noise figure, and dissipated power. For the defined FOM, a higher number represents better LNA performance.

$$FOM = \frac{S_{21}(mag).IIP3(mW)}{[NF(mag)-1].P_{diss}(mW)} \tag{24}$$

Table II shows that the present LNA has the highest FOM when compared against other L-band LNAs.

TABLE II

PERFORMANCE COMPARSION BETWEEN OTHER L-BAND LOW NOISE AMPLIFIERS

Reference	This Work	[16]	[17]	[18]	[19]	[20]	[21]
Frequency (GHz)	1.575	1.5	1.9	2	1.2276	1.575	1.575
Gain (dB)	26	22	10	11.1	20	16.5	18
S11 (dB)	-20	-15.5	-5	-13.7	-11	-13	-16.9
S22 (dB)	-13	NA	-16	-14.7	-11	-14	-11.4
NF (dB)	3.2	3.5	2.7	2	0.8	1.3	3.3
Pdiss (mW)	17.89	30	4	4	9	9	24
Vcc (V)	1.5	1.5	2	2	1.5	1.5	3
IIP3 (dBm)	-3.98	-9.3	-12.5	-0.1	-11	-5	-11
OIP3 (dBm)	21.59	12.7	-2.1	11	9	11.5	7
IP1dB (dBm)	-23	-21	NA	-9	-24	NA	NA
OP1dB(dBm)	1.73	0	NA	0	-5	NA	NA
FOM	7.400	0.501	0.178	5.381	4.363	4.497	0.183
Technology	0.13 µm SiGe BiCMOS	0.6 µm CMOS	0.8 µm Si BiCMOS	GaAs HBT	0.25 µm CMOS	0.25 µm CMOS	0.35 µm SiGe BiCMOS

A high gain, monolithic L-band SiGe LNA with integrated matching networks has been designed and fabricated in a 200 GHz SiGe BiCMOS technology. The LNA exhibits a gain of over 23 dB across the entire L-band from 1.1 to 2 GHz, with a peak gain of 26 dB, and an IIP_3 of -3.98 dBm at 1.575 GHz. The LNA achieves a NF of 2.7 to 3.3 dB from 1.2 to 2.4 GHz. This LNA exhibits the potential of SiGe BiCMOS technology to be used for low-cost, highly-integrated GPS applications.

CHAPTER 4

PACKAGING OF SIGE MMIC

4.1 Introduction

Understanding the electrical characteristics of a high-frequency package and its interconnects is important in order to optimize circuit performance. At X-band (8 – 12 GHz), the parasitics due to the package and interconnects are no longer transparent to electrical performance and hence they need to be explicitly taken into consideration during the design stage. One way to model the parasitics of the interconnections is to perform a full electromagnetic (EM) simulation for the package; however, this is time consuming and increases the complexity for circuit designers. Therefore, it is highly desirable to implement an equivalent circuit model for the package that can be used in circuit design kits for circuit optimization in order to achieve better overall system performance.

In a packaged monolithic microwave integrated circuits (MMIC), the interconnections are usually made using wire bonding [22] which tends to add large impedances [23], degrading circuit performance.

4.2 Effect of Wire Bondings on LNA Performance

In this section, the degradation of the LNA performance due to bond wires is been studies. Firstly, the LNAs were integrated into the package using bond wires. The length of the bondwire introduces significant parasitics which could degrade the performance of the LNA. Figure 16 and 17 shows the simulated performance of the LNA with and without bond wires. The S-Parameters had shown general degradation in the RF performance with the presence of bond wires.

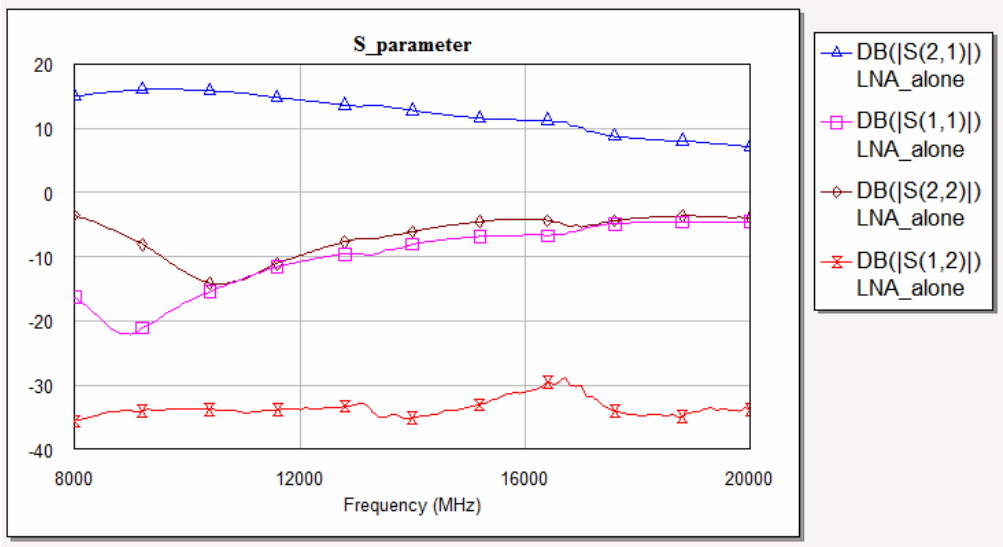


Figure 16. LNA without bond wires.

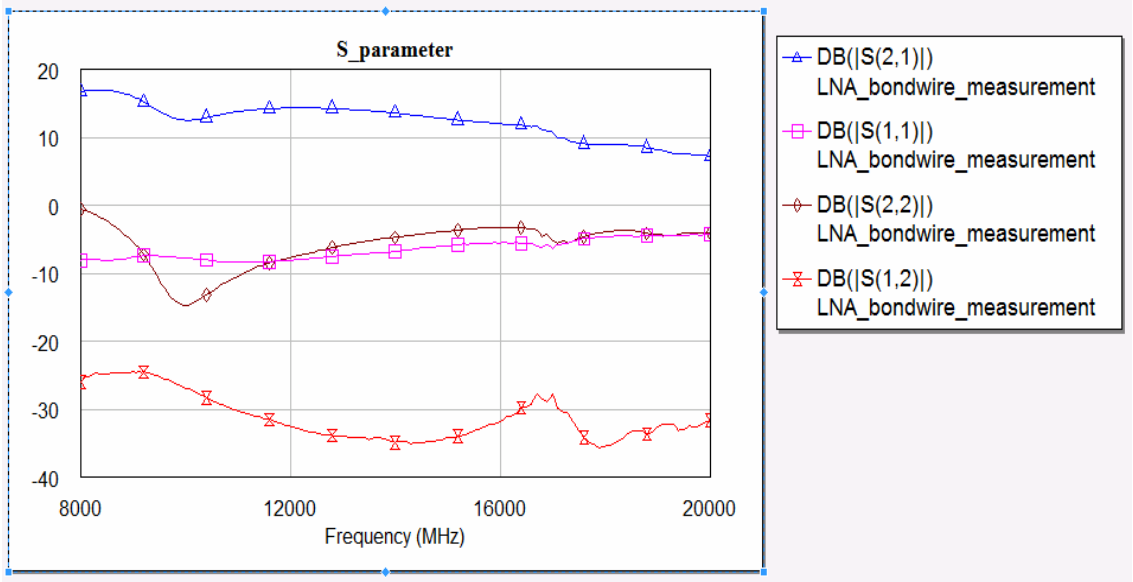


Figure 17. LNA with bond wires.

4.3 Effect of Bond Wire Length

The results of the LNA performance with different lengths of the bond wire are present in this section. In the circuit simulation, the bond wires were added at the input and output of the amplifier (bare die) as shown in Figure 18. The length of the bond wire was swept from 0.127 mm to 1 mm). Figure 19-22 shows the performance of the LNA

when 10, 20, 30, and 40 mil of wire bonding lengths. The diameter of the bondwire is 1 mil.

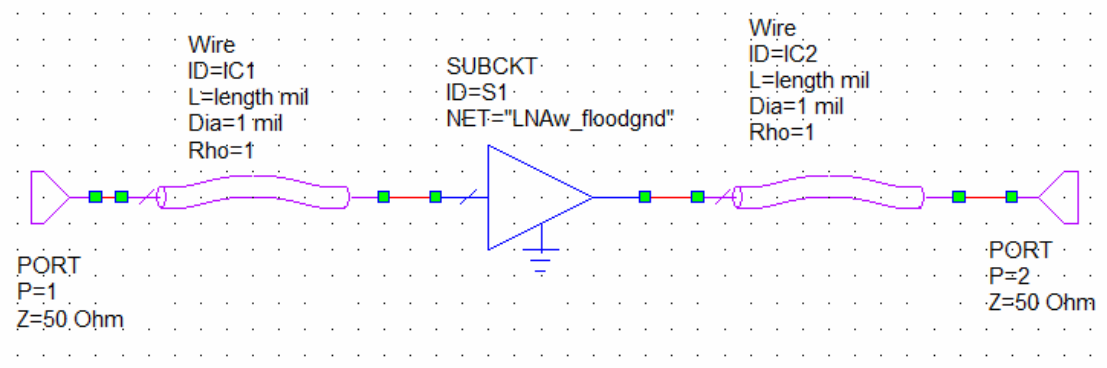


Figure 18. Schematic of the wire bonds at the input and the output of the LNA.

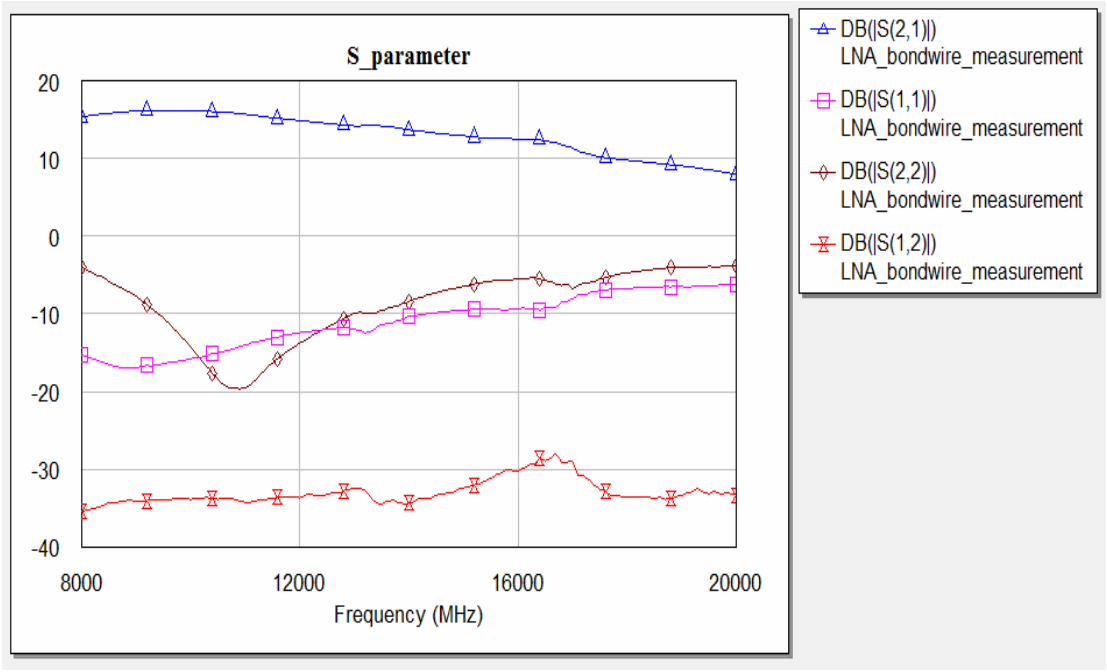


Figure 19. Simulated result of LNA with 10 mil bond wires

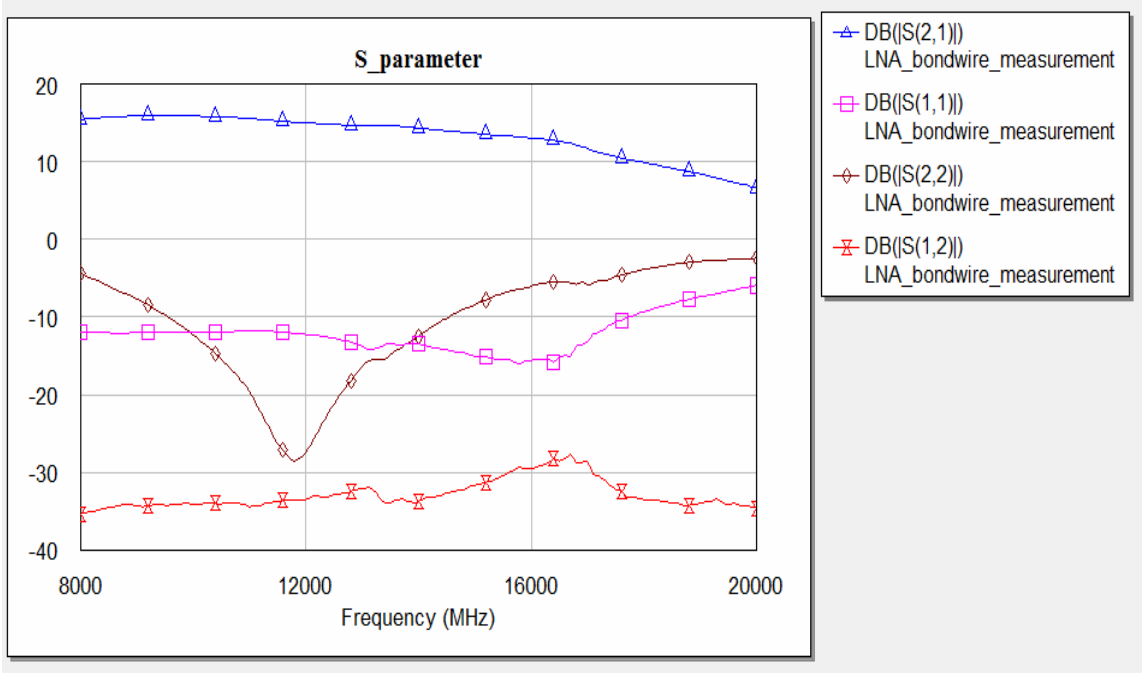


Figure 20. Simulated result of LNA with 20 mil bond wires

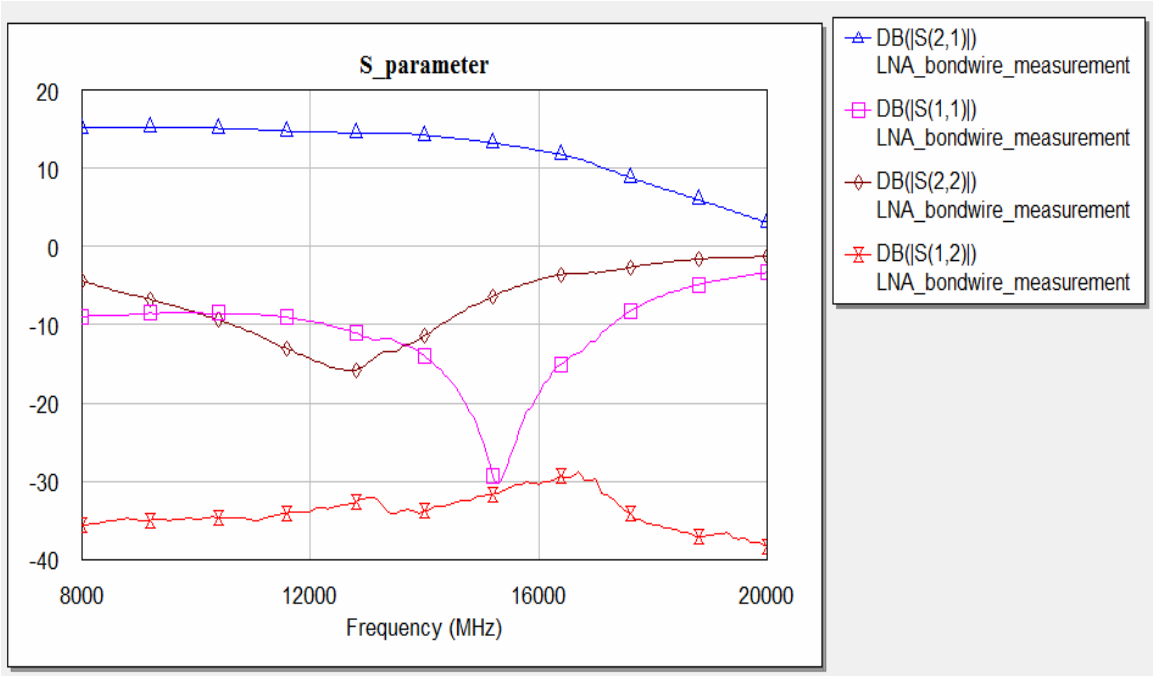


Figure 21. Simulated result of LNA with 30 mil bond wires

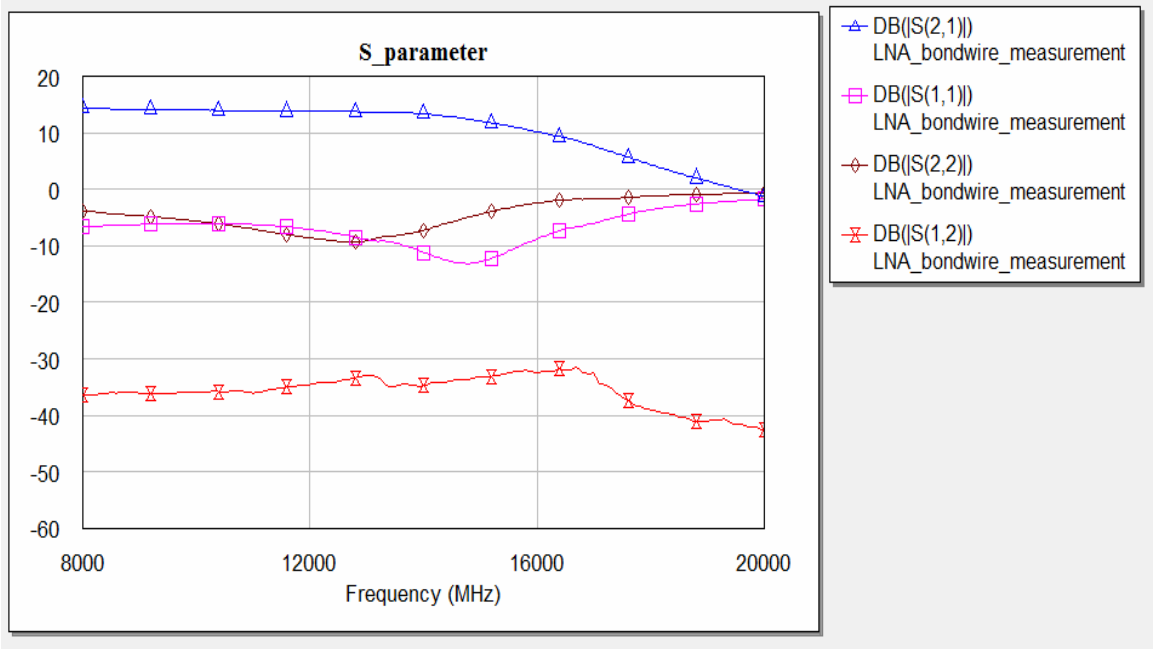


Figure 22. Simulated result of LNA with 40 mil bond wires

Figure 23 shows effect of inductance as the length of the wire bonding increased from 10 mil to 40 mil.

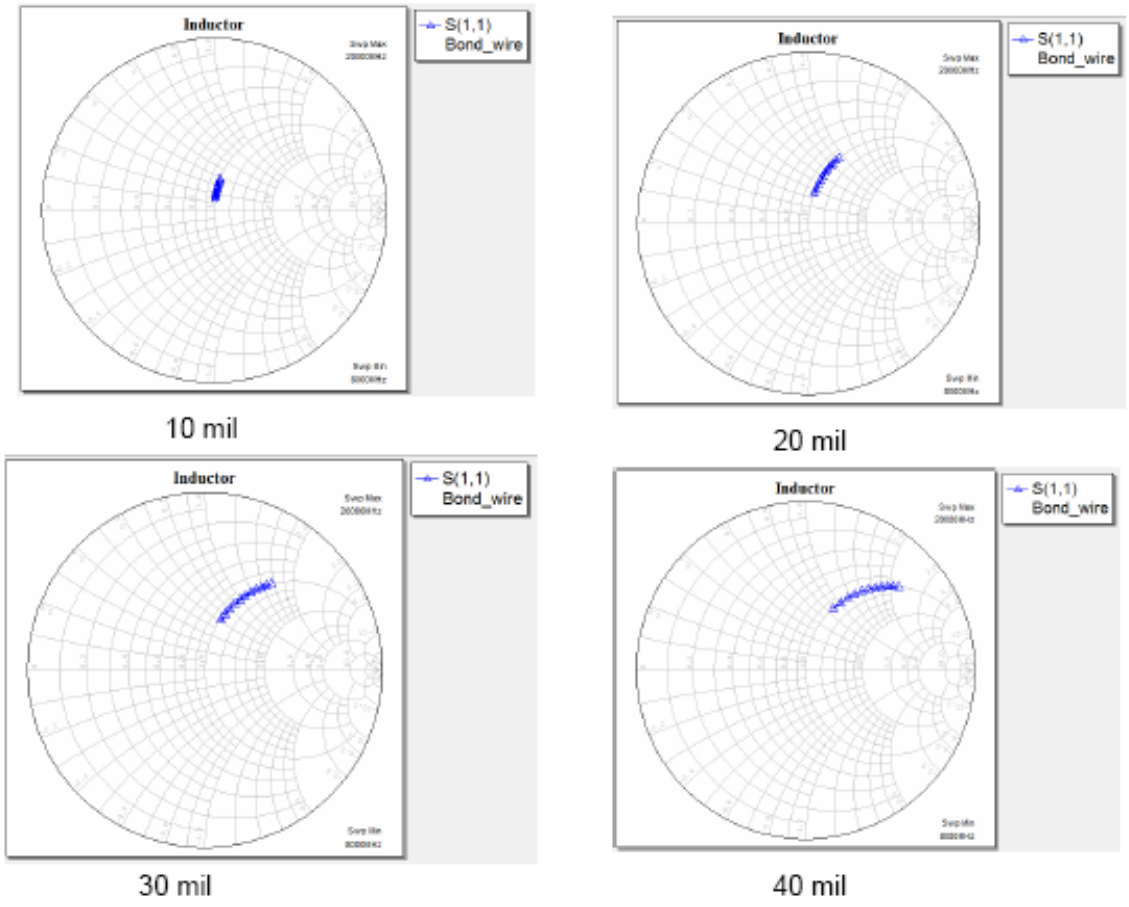


Figure 23. Inductance of the bondwires at different lengths.

From the simulation result, the bond wires were affecting both the input and output matching of the LNA and hence its performance. As the wire lengths get longer, the performance of the LNA got degraded and when the frequency gets higher, the circuit will be even more sensitive towards the change of the bond wire length. Compensation structure/tunable matching network on the package could be added to counter the effect of the bond wire.

4.4 LCP Package on SiGe LNA

Liquid crystal polymer (LCP) has been used for the MMIC packaging because of its excellent high frequency electrical properties, such as low dielectric constant and low loss tangent [24]-[26]. The package design here consists of a 2 mil LCP which is been

laminated onto the top surface of a SiGe HBT LNA die. The CPW lines of the LCP are connected directly to the pads of the SiGe die through 50 μm via interconnections. The details of the LCP fabrication are discussed in [27]. Using this approach, the large parasitics usually introduced by the bondwires interconnects in a conventional package are greatly reduced.

The SiGe LNA is shown in Figure 24 was fabricated in a commercially-available 200GHz, 0.13 μm BiCMOS SiGe technology and the measured on-wafer results of the LNA is shown in Table III. The details of the LNA design and measured results are discussed in [28].

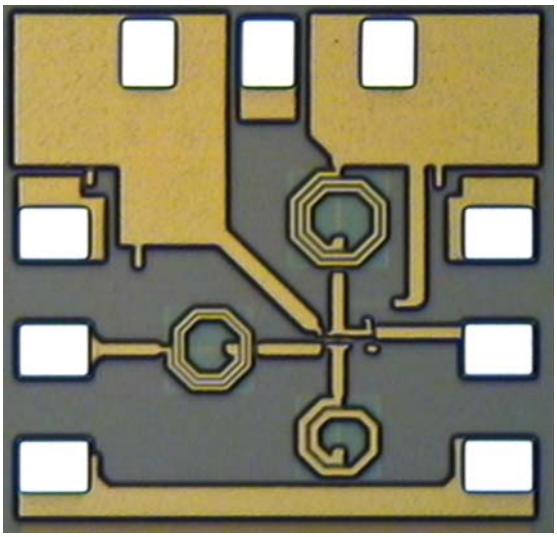


Figure 24. Photograph of the X-band SiGe LNA die.

TABLE III

SiGe LNA SPECIFICATIONS

Frequency (GHz)	9.5 – 10.5
Vcc (V)	1.5
Gain (dB)	10
Return loss (dB)	>10
Noise Figure (dB)	2
Power dissipation (mW)	< 2

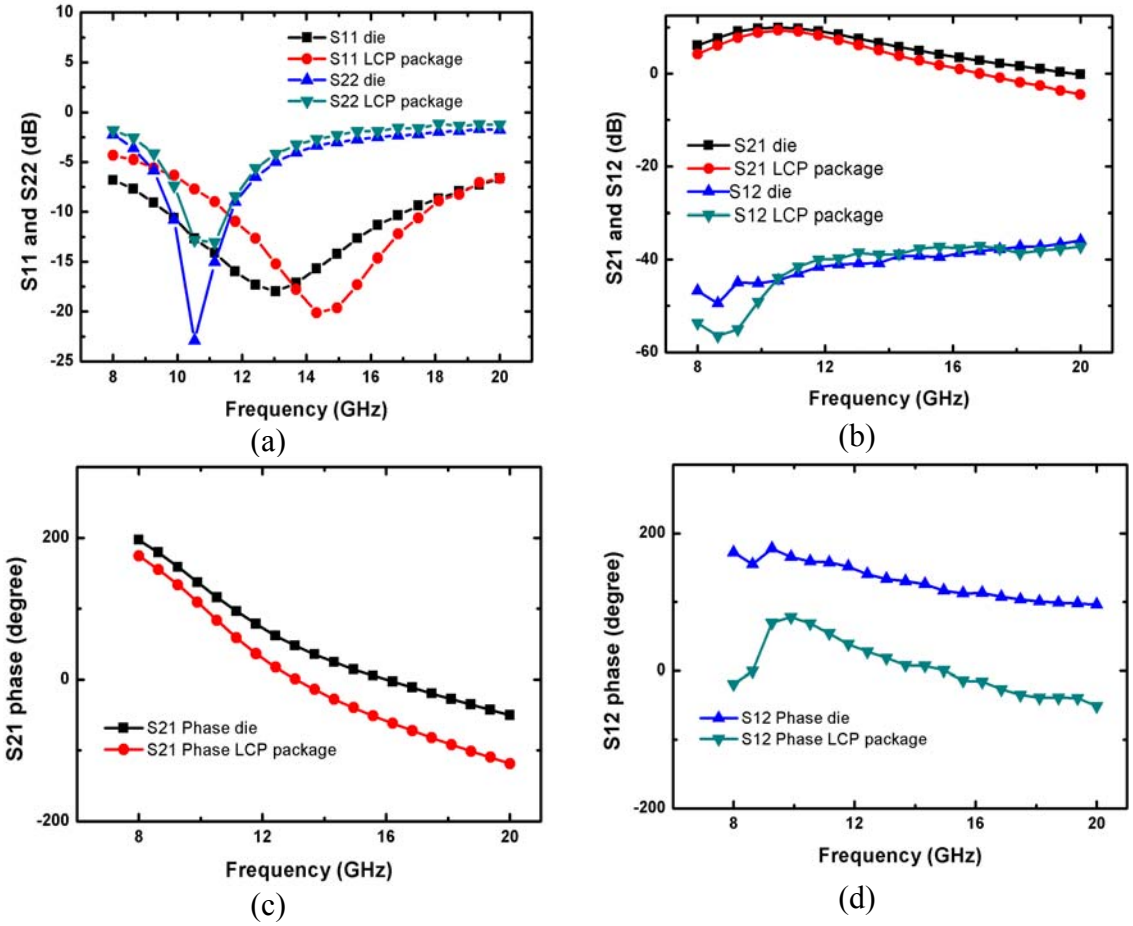


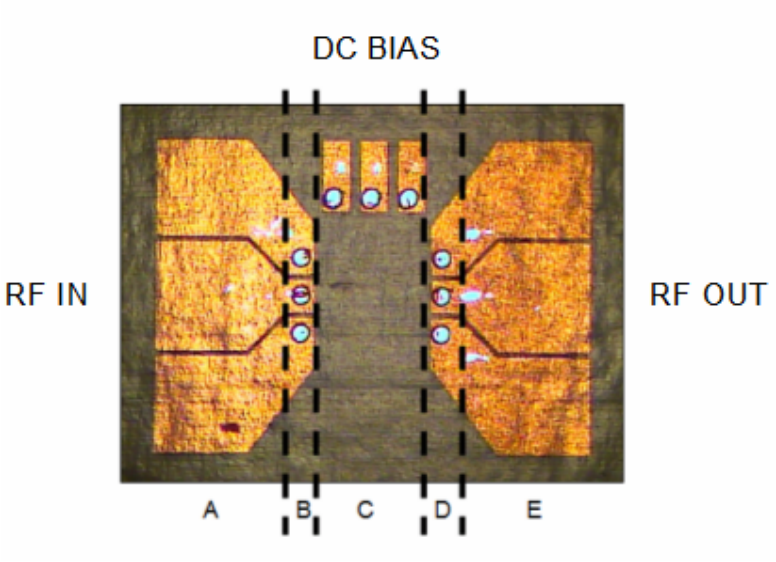
Figure 25. Measured S-parameter results, both before and after LCP packaging: (a) S_{11} and S_{22}, (b) S_{21} and S_{12}, (c) S_{21} phase and (d) S_{12} phase.

In Figure 25, the LCP-packaged SiGe LNA was measured and was compared with the on-wafer measurement result.

It can be seen that after the SiGe LNA had been packaged, there is a shift in the input matching and a slight degradation of less than 1 dB in the magnitude of S_{21}. All these changes are due to the mismatch introduced by the package parasitics. In the next section, the effects of the LCP package on the LNA performance is studied and modeled.

4.5 Modeling the Package Parastics

The package was divided into five components, as shown in Figure 26 as in [29].



A – CPW line in
B – Via in
C – LCP on top of the LNA
D- Via out
E – CPW out

Figure 26. Top view of the LCP packaged SiGe LNA.

Each of the components was simulated in Ansoft HFSS and the equivalent circuit models were derived based on the simulated S-parameter results from HFSS. Agilent's Advanced Design System (ADS) was then used to optimize the lump elements in the equivalent circuit model to correlate the HFSS simulation results and the models. The CPW line of the LCP package shown in Figure 27 was represented by the circuit topology shown in Figure 28. In Figure 28, the L_{cpw} represents the self-inductance of the CPW line, while C_{cpw} represents the coupling between the signal and the ground pad in the CPW transmission line.

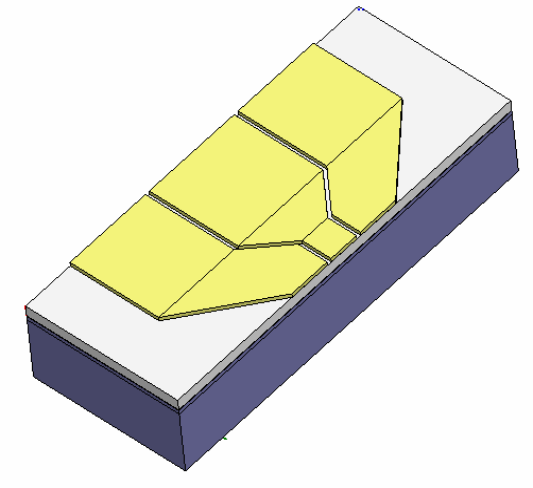


Figure 27. CPW line of the LCP package.

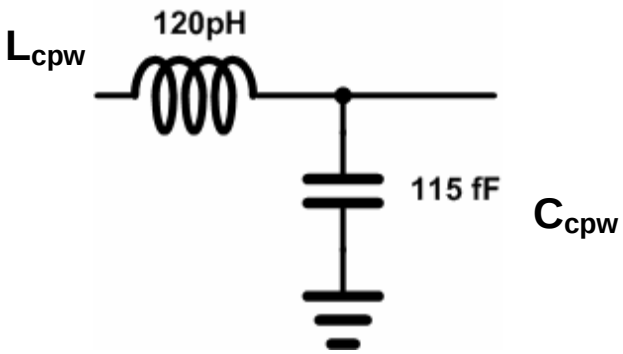


Figure 28. Equivalent circuit model for the CPW line.

As shown in Figure 29, the package consists of vias and LCP on the top surface of the SiGe LNA die. The equivalent circuit model for the vias [30] and the LCP are shown in Figure 30 and Figure 31, respectively. In Figure 31, the resistance R1 models the dielectric loss in the LCP material, both C1 and C2 model the coupling to the ground vias and, C3 models the coupling between the input and output vias.

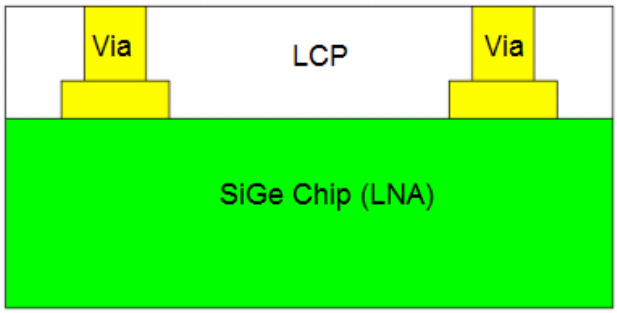


Figure 29. Cross-sectional view of the vias in the LCP package.

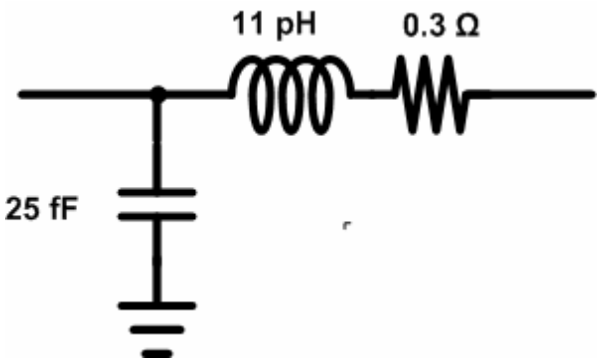


Figure 30. Equivalent circuit model for the interconnection via.

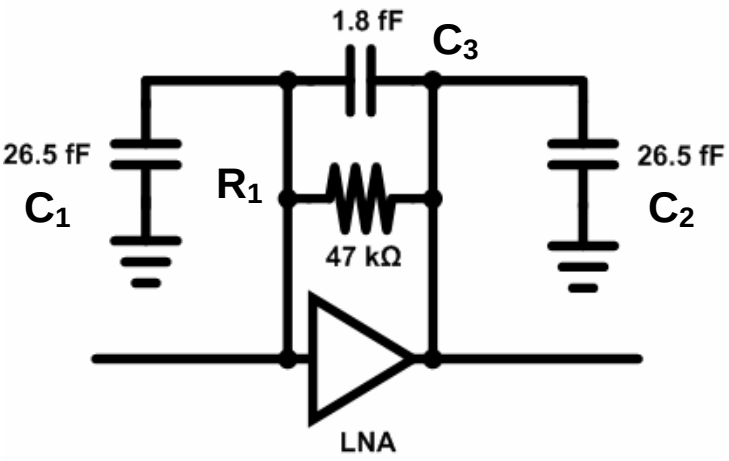


Figure 31. Equivalent circuit model for the LCP on top of the SiGe LNA die.

4.6 Comparison between the Measured and Modeled

The equivalent circuit models for the individual components in the LCP package in Figure 32 were extracted and then added to the SiGe LNA for re-simulation (Figure 33) to verify the model and to compare with measured results.

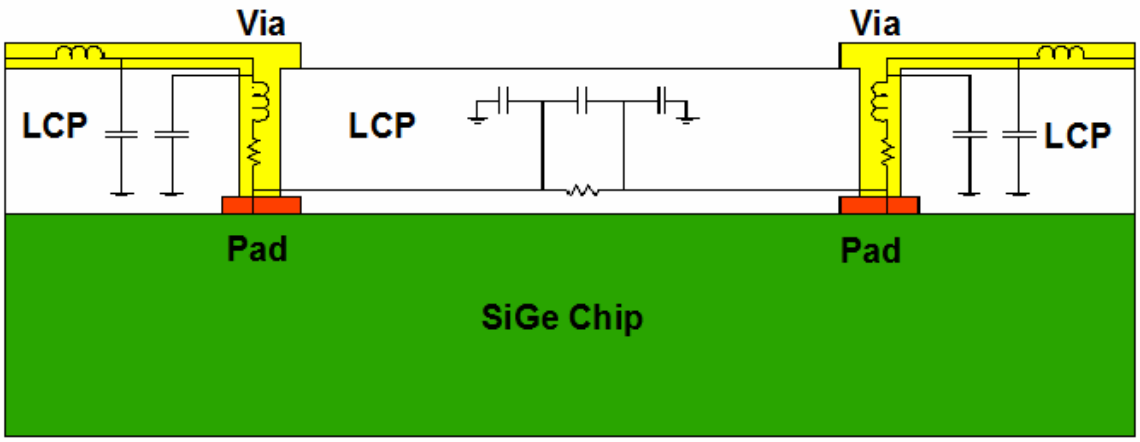


Figure 32. Cross-sectional view of the packaged SiGe LNA with the parasitic models.

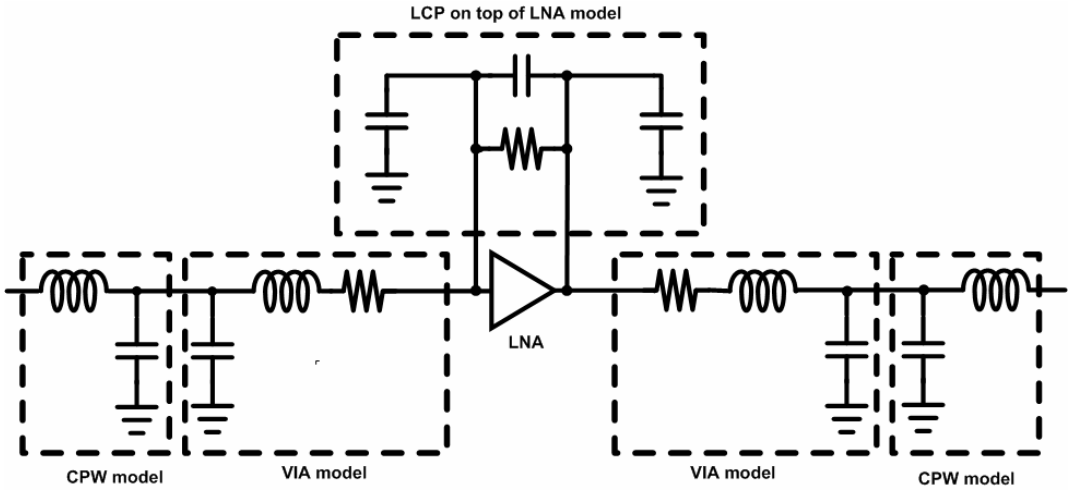


Figure 33. Schematic view of the packaged SiGe LNA with the parasitic models used for circuit simulation.

Figure 34 shows the measured results of the packaged LNA, together with the simulation results of the LNA with the LCP model included. It can be seen from the

comparison that the simulations of the LNA which include the package model give good agreement with measured data.

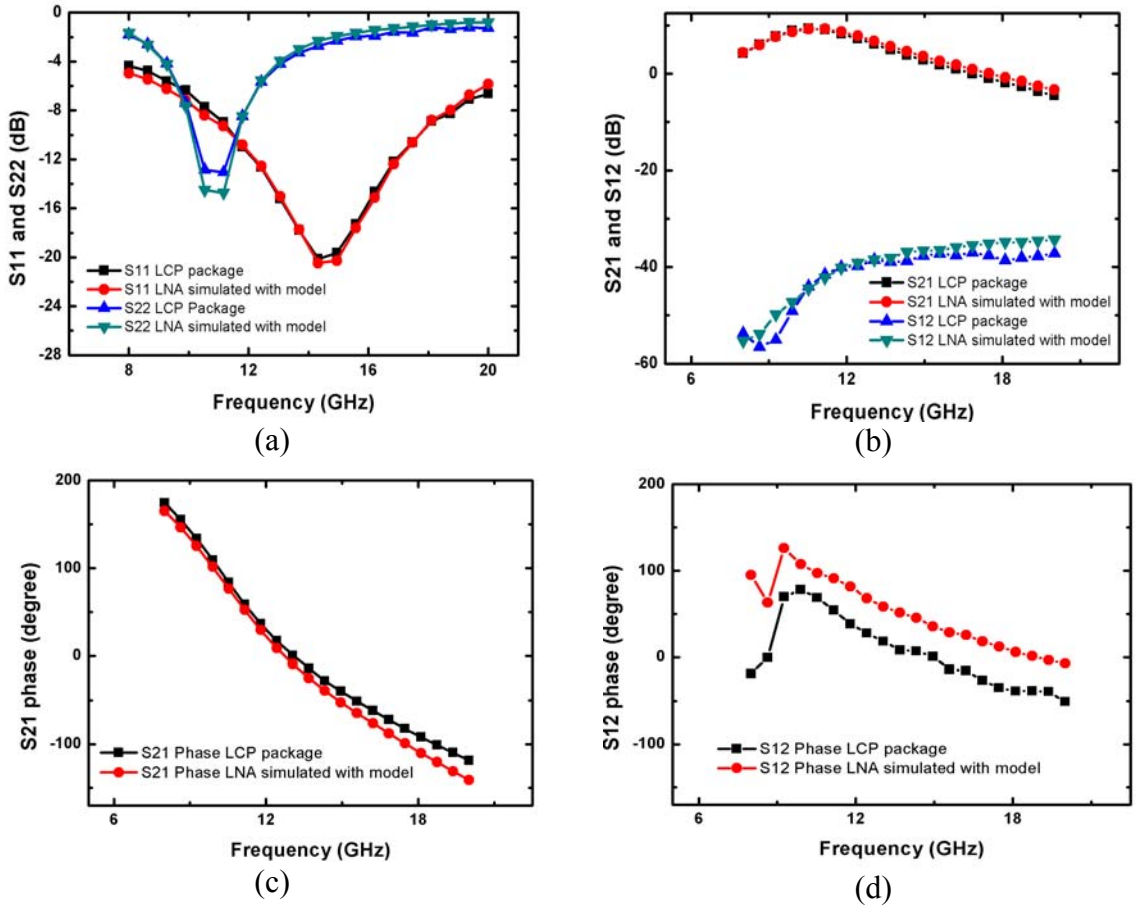


Figure 34. Measured and modeled S-parameters of the packaged LNA. (a) S_{11} and S_{22}, (b) S_{21} and S_{12}, (c) S_{21} phase and (d) S_{12} phase.

This thesis has presented a model for an LCP packaged SiGe HBT LNA, and simulation results match closely with measurements. These results imply that the LCP package has a significant impact on the LNA performance due to its parasitics, and therefore it is important that all these parasitics be considered during the circuit design stage. With this LCP package model, circuit designers will be able to performance more accurate optimization for envisioned MMIC applications which require the use of embedded SiGe die in a LCP package matrix.

CHAPTER 5

CONCLUSION

5.1 Conclusions

In this thesis, SiGe HBT has demonstrated its potential to meet the demand for the new generation wireless communication systems. The SiGe HBT has many advantages over III-V devices in many RF and microwave applications due to the high F_T, F_{max} and most importantly, its ability to integrate with CMOS circuits into a single chip leading towards the system-on-chip (SOC) approach.

In chapter 1, the overview and benefits of SiGe HBT technology were discussed and it can be shown that the SiGe HBT is a promising candidate for many RF and microwave circuit applications.

In Chapter 2, the role of the low noise amplifier in a wireless communication system had been discussed and the basic concept of a single-ended cascode low noise amplifier (LNA) had been introduced. The technique to achieve simultaneous noise and gain matching for the LNA had been discussed and the methodology in designing the LNA had been shown.

In Chapter 3, the design of a single-ended cascode L-band LNA with feedback network was demonstrated. The feedback network helped to improve the matching and the linearity of the LNA. The measurement result was presented as the end of Chapter 3.

In Chapter 4, the package considerations for the SiGe HBT were discussed. The simulation results of SiGe chips with bond wires had proven that the length of the bond wires had a significant impact on its RF performance. It can be shown that the result degraded was due to the parasitic inductances introduced by the bond wires. Liquid crystal polymer (LCP) substrate was used as a packaging material to embed the whole SiGe and by using this approach; it reduces the parasitics inductances and leading to a more compact package than the conventional bond wire package. An X-band LNA was

laminated with LCP and the model for the LCP package had been derived so that the model can be included in circuit simulation for optimization leading to better performance and reliability.

In conclusion, both the RF circuit design and packaging for SiGe HBT technology had been covered in the thesis and the SiGe HBT had demonstrated as a core technology to develop the next generation of communication system such as TR module for radar system.

5.2 Future Research

This thesis covers an overview of using SiGe HBT technology for RF and microwave circuit applications and the use of LCP substrate to package the SiGe integrated circuits. There are many opportunities to extend the research of SiGe HBT as core technology to develop RF and microwave circuits that require good noise performance, high linearity, radiation hardening, higher frequency and low power consumption. With the advancing process technology, SiGe transistor can operate at up to 200 GHz, its noise and power performance is comparable to III-V devices such as GaAs, with the CMOS option, it enable mixed-signal design which compare both RF and digital functions on a single chip, and hence it leads to system integration and reduce the cost of the complete system. However in reality, a circuit performance depends also on the packaging and hence, packaging is one of the important factors for circuit designer to be considered.

In this thesis, the use of LCP substrate to package the SiGe HBT LNA is shown. The LCP substrate is a potential candidate for RF packaging and this thesis has shown that the LCP substrate can be used as a backplane to connect different RF chips and MEMS devices together to form a complete system. However, in order to incorporate the LCP package into the circuit design, a good model for the LCP package is important so that circuit designer can use the model for circuit simulation and optimization. Further

research works are needed to model the effect of the LCP packages on the circuit performance, such as the diameter and the height of the LCP via, and how are these parameters going to affect the RF performance. Understanding the via interconnections in the LCP package will help to improve and optimize the circuit performance.

To summarize, a low cost high performance communication system can be realized using the SiGe HBT as the core technology for the circuits and the LCP as the core packaging material. Further research works will be done on both the SiGe HBT and LCP package to bring on the communication system to the next level.

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