Design and Test Methodologies with Statistical Analysis for Reliable Memory and Processor Implementations

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123 Pages

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The object of the proposed research is to develop comprehensive methodologies, including circuit design, new test methodologies, and statistical failure analysis, to implement reliable microprocessor and main memory systems. For a microprocessor, we have focused on the reliability issues in the embedded cache, since SRAMs are designed with the tightest design rules, and high performance processors are expected to consist of a large embedded memory. Also, to solve the scaling challenges for the main memory system, we have studied optimized design schemes for the 3D DRAM system, to achieve better performance, reliability, cost, and power.

To implement a reliable microprocessor, this research has focused on wearout mechanisms, namely BTI, GTDDB, EM, SIV and BTDDB, in the embedded cache systems. The research has presented built-in self-test and statistical analysis methodologies for electrical detection and diagnosis of wearout mechanisms in an SRAM to improve the manufacturing process. Also, based on the diagnosis result, this research work has proposed to use the ECC failure bits as the mileage monitor for the remaining lifetime of the processor.

For the main memory system, we have studied design methodologies for an emerging main memory to overcome the limitations of device scaling. Especially, we present a design solution for 3D DRAM to optimize reliability, power, cost, and performance, given emerging reliability issues induced by through silicon vias (TSVs).