US006785458B2

(12) **United States Patent**
Mule'et al.

(10) **Patent No.: US 6,785,458 B2**
(45) **Date of Patent: Aug. 31, 2004**

(54) **GUIDED-WAVE OPTICAL INTERCONNECTIONS EMBEDDED WITHIN A MICROELECTRONIC WAFER-LEVEL BATCH PACKAGE**

(75) Inventors: **Tony Mule'**, Atlanta, GA (US); **Chirag Patel**, College Park, GA (US); **James D. Meindl**, Marietta, GA (US); **Thomas K. Gaylord**, Atlanta, GA (US); **Elias N. Glytsis**, Dunwoody, GA (US); **Kevin P. Martin**, Atlanta, GA (US); **Stephen M. Schultz**, Tucson, AZ (US); **Muhannad Bakir**, Atlanta, GA (US); **Hollie Reed**, Smyrna, GA (US); **Paul Kohl**, Atlanta, GA (US)

(73) Assignee: **Georgia Tech Research Corporation**, Atlanta, GA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/074,420**

(22) Filed: **Feb. 11, 2002**

(65) **Prior Publication Data**

US 2002/0136481 A1 Sep. 26, 2002

Related U.S. Application Data

(60) Provisional application No. 60/268,142, filed on Feb. 11, 2001.

(51) **Int. Cl.**^{7} **G02B 6/10**
(52) **U.S. Cl.** **385/131**; 385/132
(58) **Field of Search** 385/14, 15, 37, 385/39, 125, 129–132

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,950,073 A * 4/1976 Horiguchi et al. 385/123
4,959,540 A 9/1990 Fan et al. 250/227.12
5,054,872 A * 10/1991 Fan et al. 385/130
5,250,816 A 10/1993 Kitamura 257/81
5,253,319 A * 10/1993 Bhagavatula 385/129
5,278,925 A * 1/1994 Boysel et al. 385/14

(List continued on next page.)

OTHER PUBLICATIONS

Anthony R. Blythe and John R. Vinson; Polymeric Materials for Devices in Optical Fibre Systems; Sep. 1, 1999; Polym. Adv. Technol. 11, 601–611 (2000).

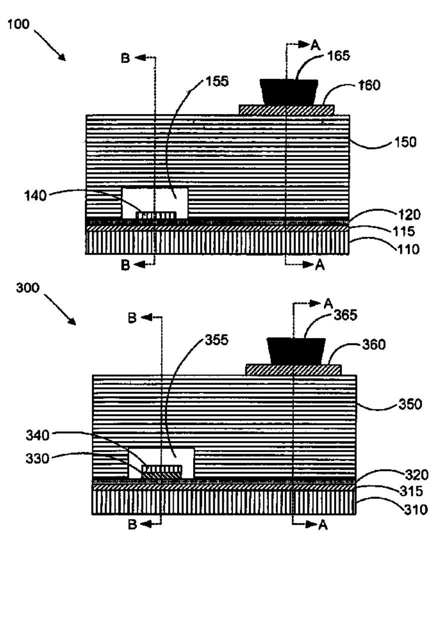
Thomas K. Gaylord and M. G. Moharam; Analysis and Applications of Optical Diffraction by Gratings; May, 1985; Proceedings of the IEEE, vol. 3, No. 5, May 1985; pp. 894–937.

Primary Examiner—Edward J. Glick
Assistant Examiner—Thomas R Artman
(74) *Attorney, Agent, or Firm*—Thomas, Kayden, Horstemeyer & Risley, LLP

(57) **ABSTRACT**

Wafer-level electronic packages having waveguides and methods of fabricating chip-level electronic packages having waveguides are disclosed. A representative chip-level electronic package includes at least one waveguide having a waveguide core. In addition, another representative chip-level electronic package includes a waveguide having an air-gap cladding layer around a portion of the waveguide core. A representative method for fabricating a chip-level electronic package includes: providing a substrate having a passivation layer disposed on the substrate; disposing a waveguide core on a portion of the passivation layer; disposing a first sacrificial layer onto at least one portion of the passivation layer and the waveguide core; disposing an overcoat layer onto the passivation layer and the first sacrificial layer; and removing the first sacrificial layer to define an air-gap cladding layer within the overcoat polymer layer and around a portion of the waveguide core.

13 Claims, 40 Drawing Sheets



U.S. PATENT DOCUMENTS

5,293,626	A		3/1994	Priest et al.	713/401
5,416,861	A	*	5/1995	Koh et al.	385/14
5,430,567	A		7/1995	Shaw et al.	359/107
5,434,524	A		7/1995	Shaw et al.	327/187
5,434,935	A	*	7/1995	Kragl	385/14
5,508,835	A		4/1996	Takahashi et al.	359/140
5,515,194	A		5/1996	Kanterakis et al.	359/127
5,526,838	A	*	6/1996	Robert	137/12
5,677,778	A		10/1997	Kanterakis et al.	359/127
5,708,671	A		1/1998	Siao et al.	372/20
5,812,708	A		9/1998	Rao	385/14
5,889,903	A		3/1999	Rao	385/14
6,008,918	A		12/1999	Kanterakis et al.	359/117
6,125,217	A		9/2000	Paniccia et al.	385/14
6,285,813	B1	*	9/2001	Schultz et al.	385/37
6,493,497	B1	*	12/2002	Ramdani et al.	385/131
6,621,972	B2	*	9/2003	Kimerling et al.	385/132
2002/0076188	A1	*	6/2002	Kimerling et al.	385/132
2002/0122648	A1	*	9/2002	Mule' et al.	385/129

* cited by examiner

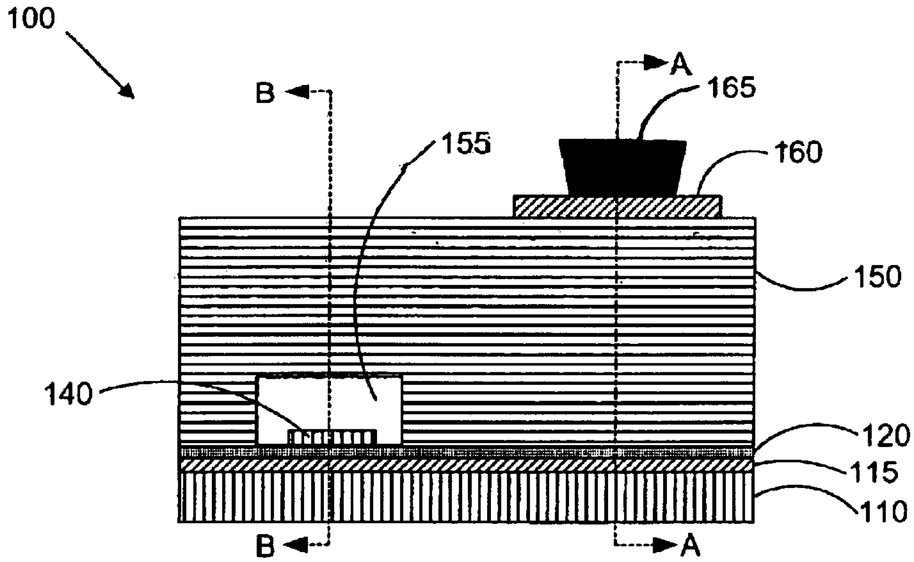


FIG. 1A

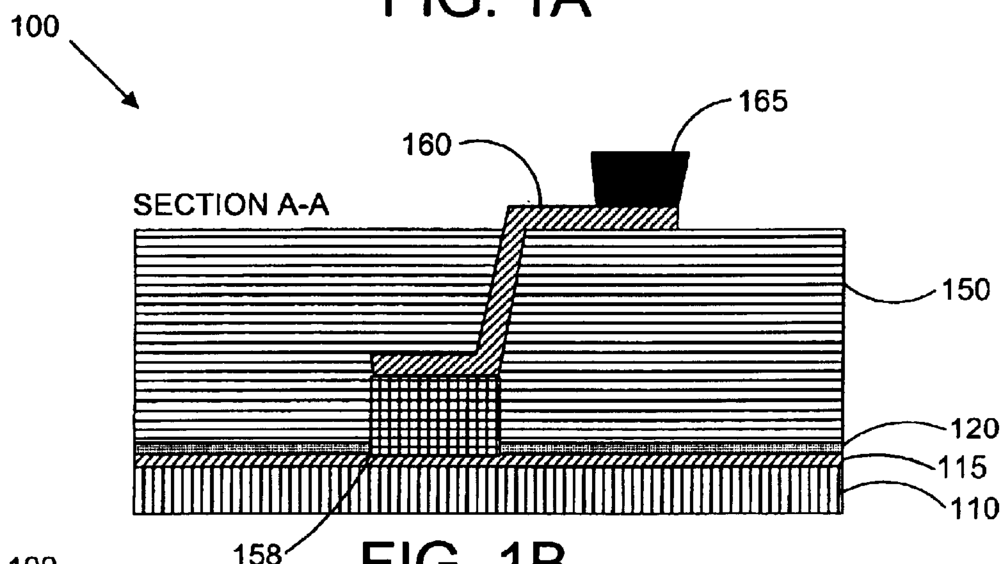


FIG. 1B

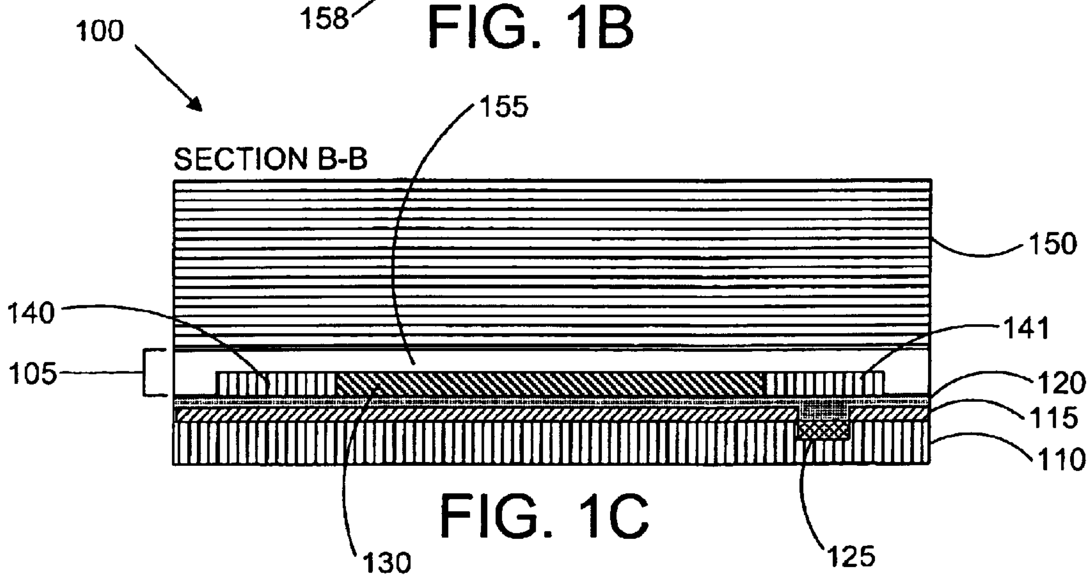


FIG. 1C

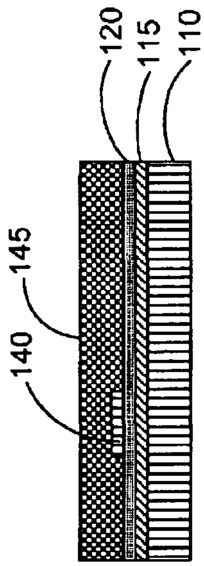


FIG. 2E

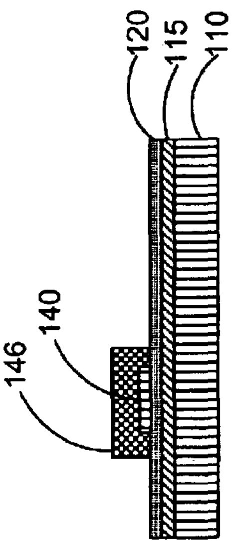


FIG. 2F

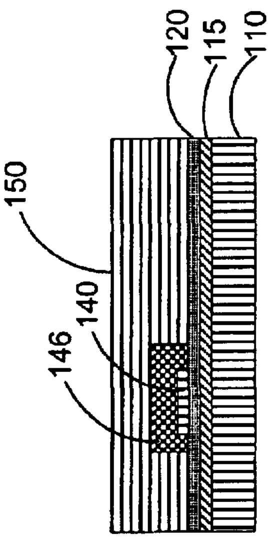


FIG. 2G

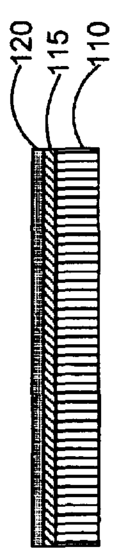


FIG. 2A

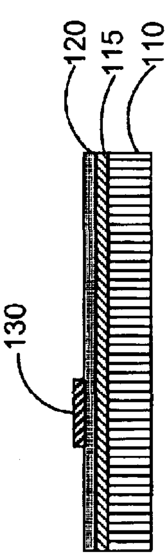


FIG. 2B

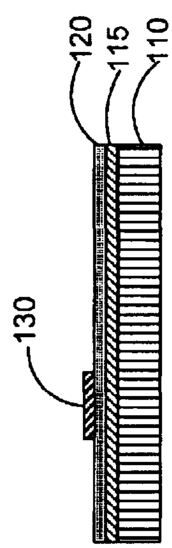


FIG. 2C

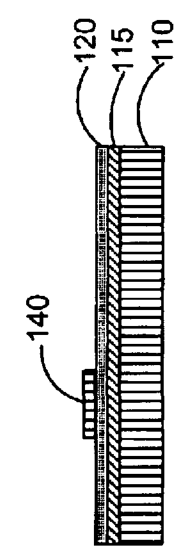


FIG. 2D

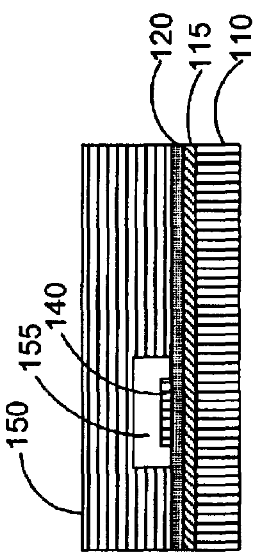


FIG. 2H

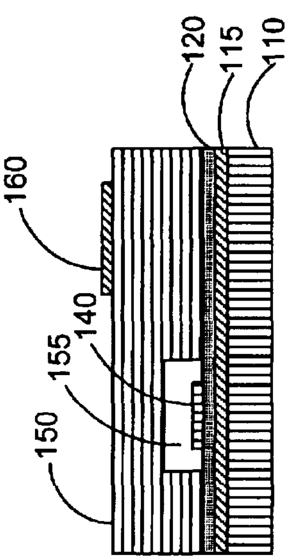


FIG. 2I

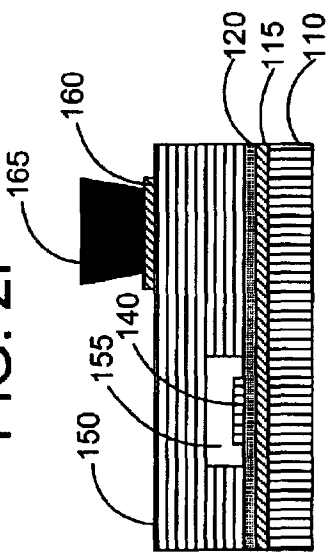


FIG. 2J

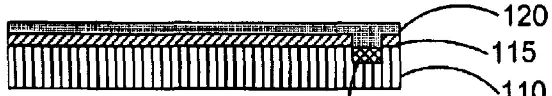


FIG. 3A
SECTION B-B

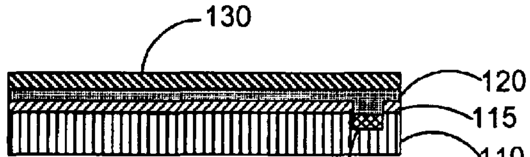


FIG. 3B
SECTION B-B

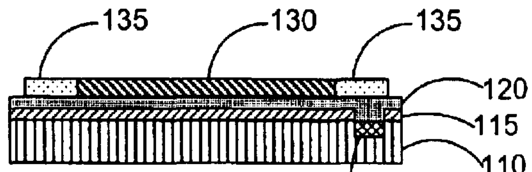


FIG. 3C
SECTION B-B

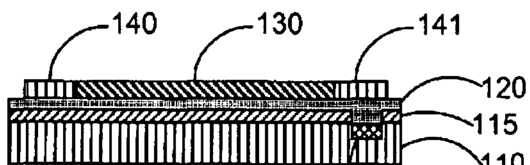


FIG. 3D
SECTION B-B

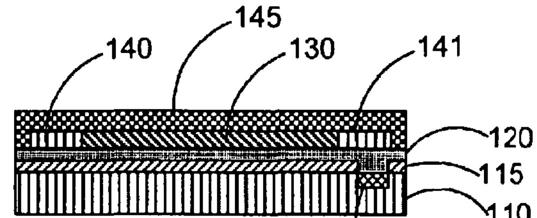


FIG. 3E
SECTION B-B

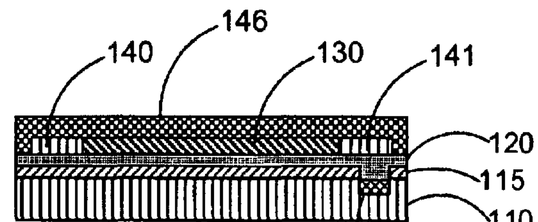


FIG. 3F
SECTION B-B

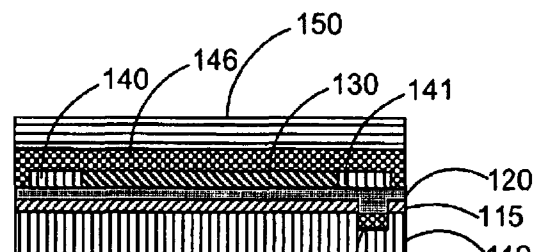


FIG. 3G
SECTION B-B

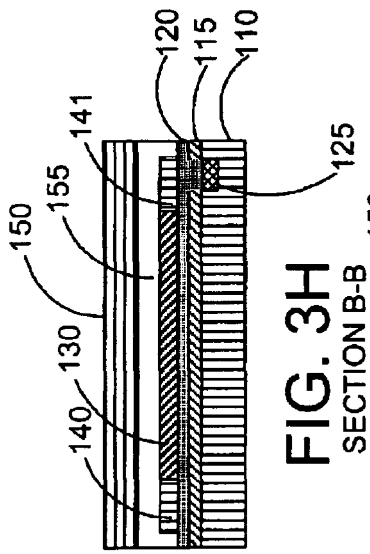


FIG. 3H
SECTION B-B

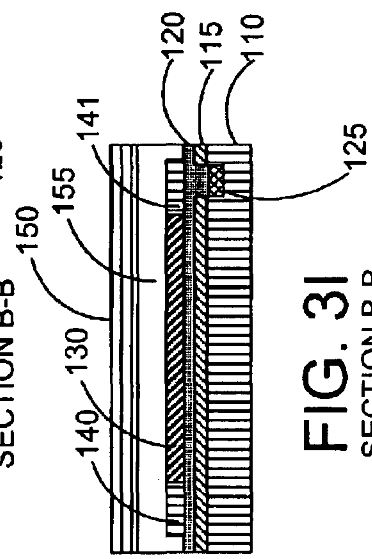


FIG. 3I
SECTION B-B

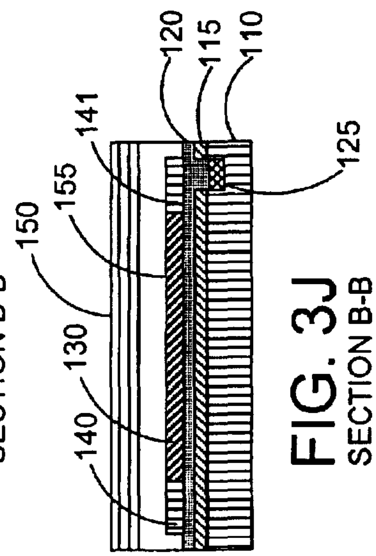


FIG. 3J
SECTION B-B

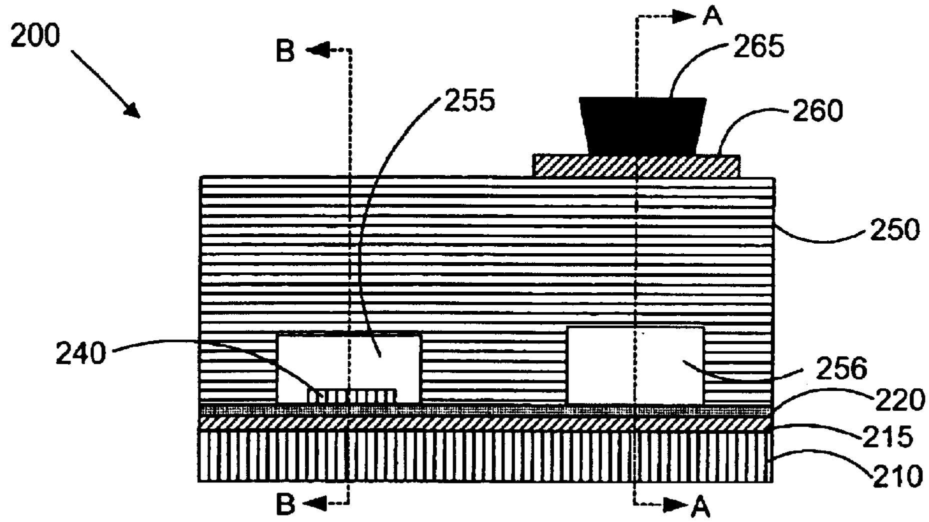


FIG. 4A

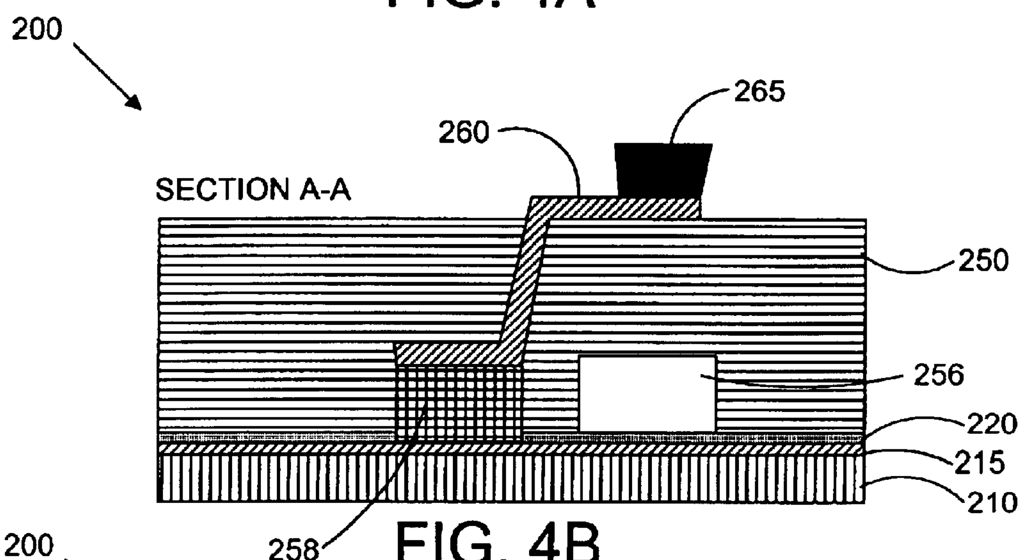


FIG. 4B

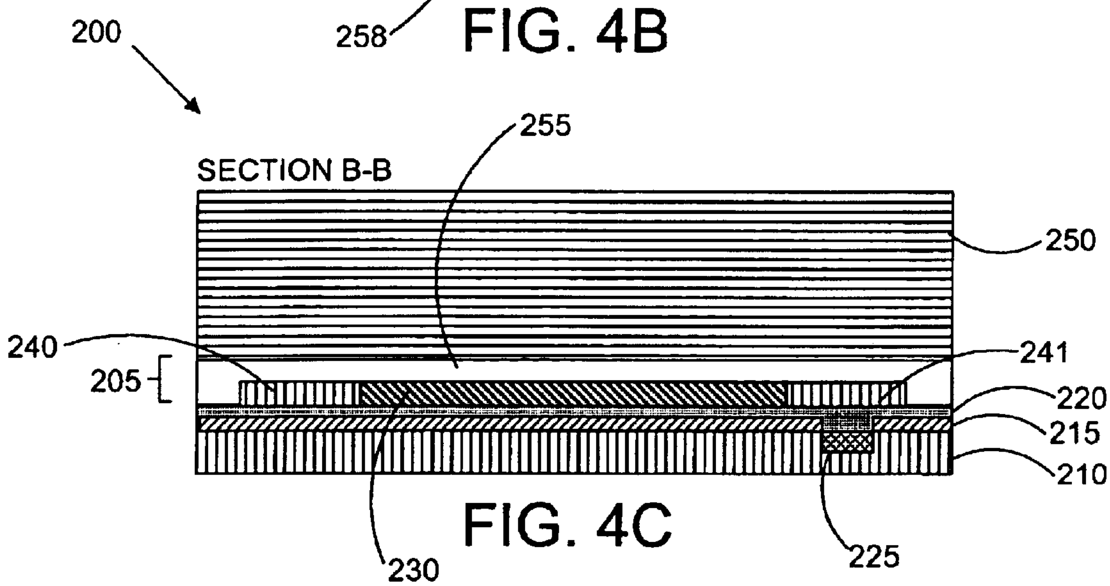


FIG. 4C

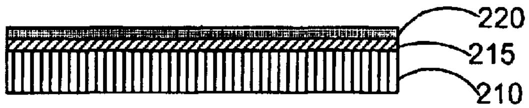


FIG. 5A

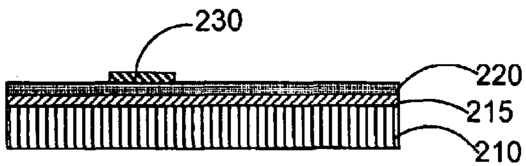


FIG. 5B

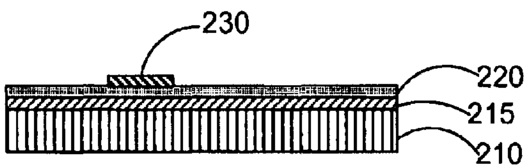


FIG. 5C

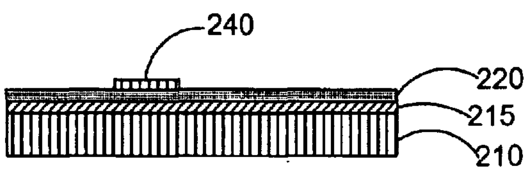


FIG. 5D

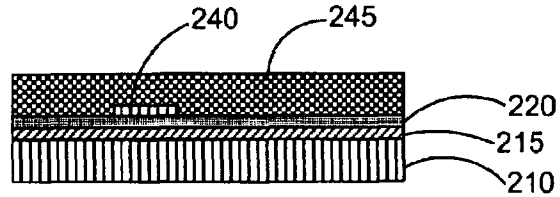


FIG. 5E

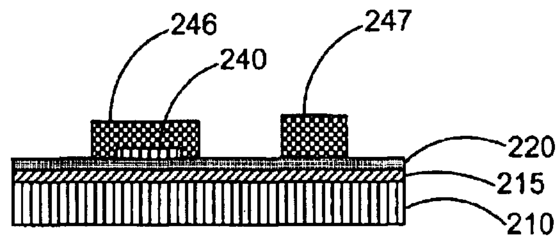


FIG. 5F

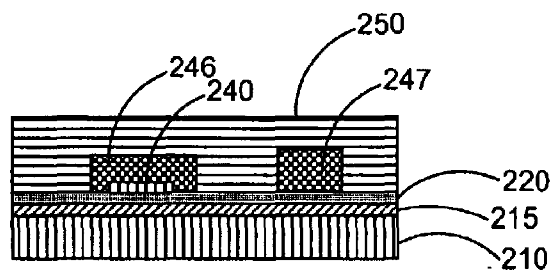


FIG. 5G

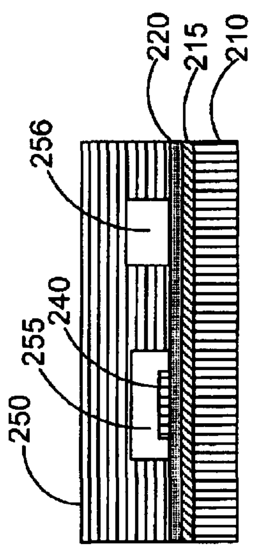


FIG. 5H

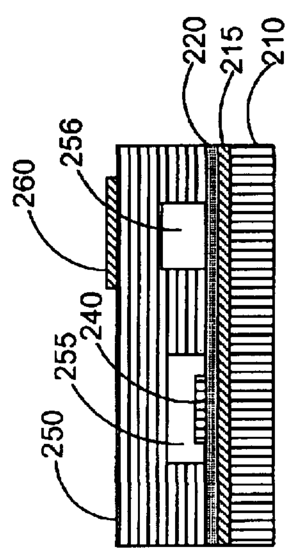


FIG. 5I

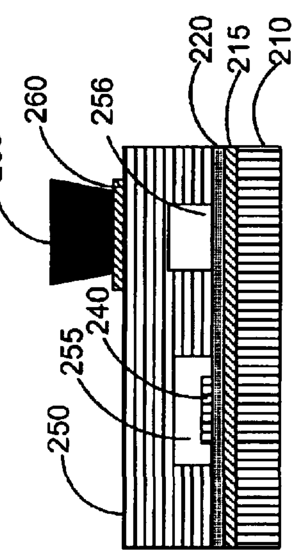


FIG. 5J

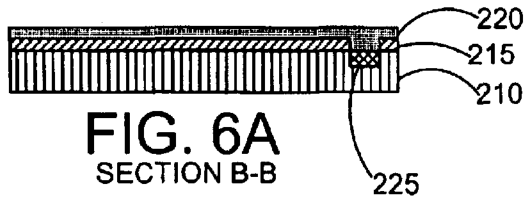


FIG. 6A
SECTION B-B

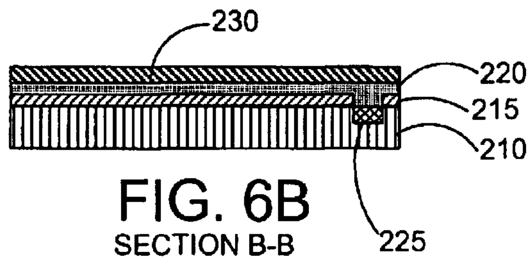


FIG. 6B
SECTION B-B

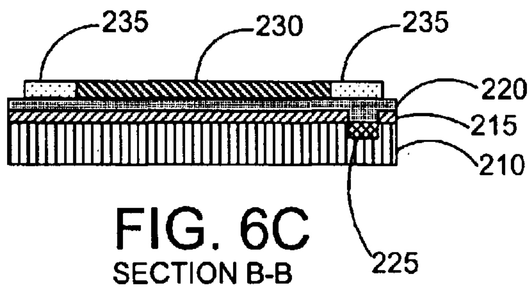


FIG. 6C
SECTION B-B

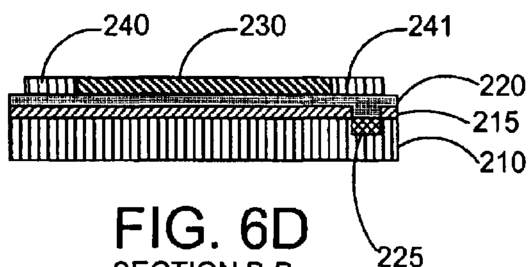


FIG. 6D
SECTION B-B

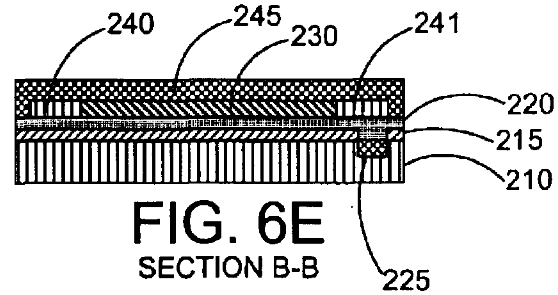


FIG. 6E
SECTION B-B

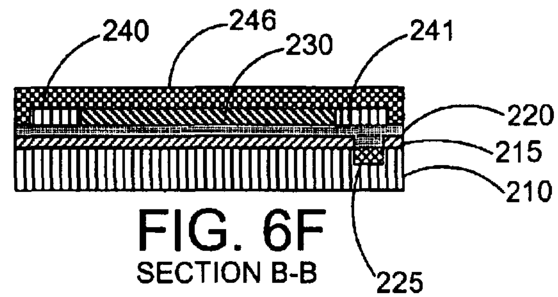


FIG. 6F
SECTION B-B

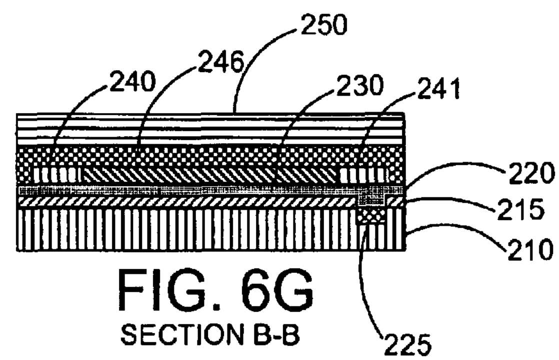


FIG. 6G
SECTION B-B

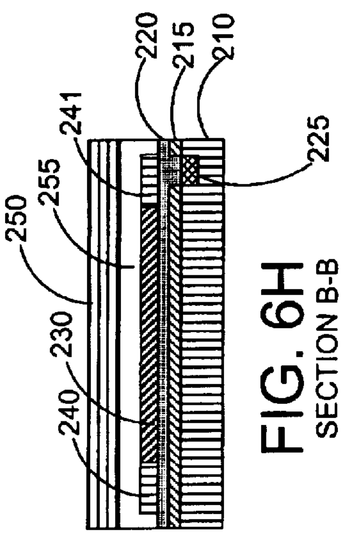


FIG. 6H
SECTION B-B

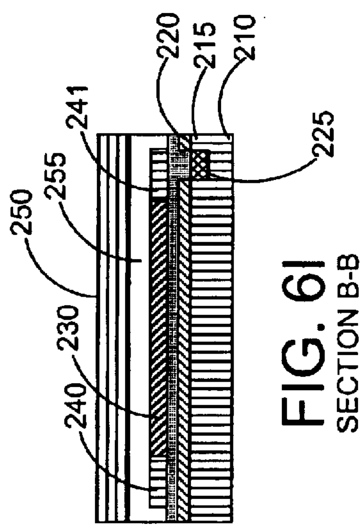


FIG. 6I
SECTION B-B

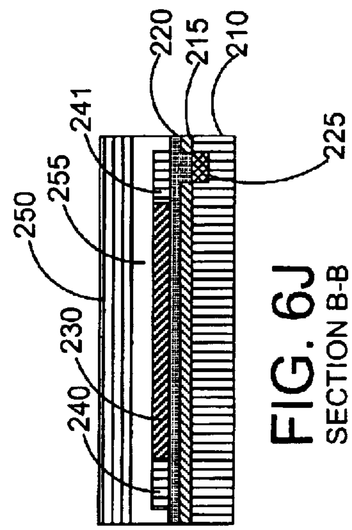


FIG. 6J
SECTION B-B

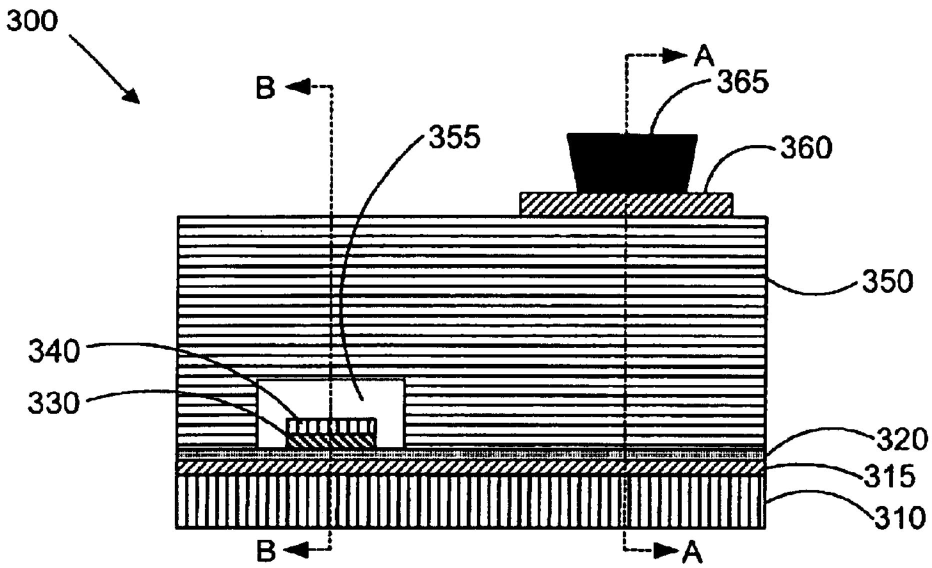


FIG. 7A

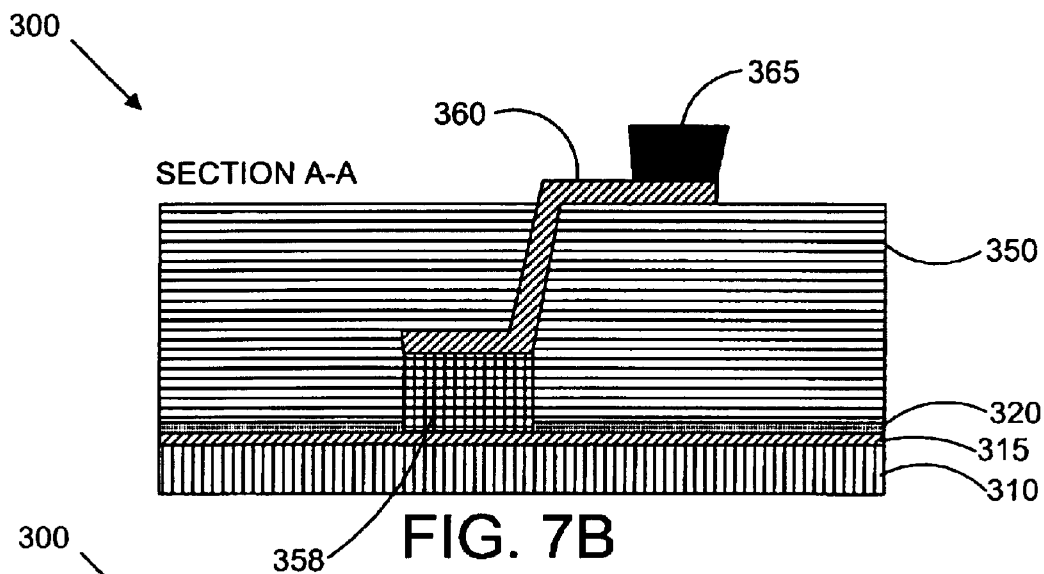


FIG. 7B

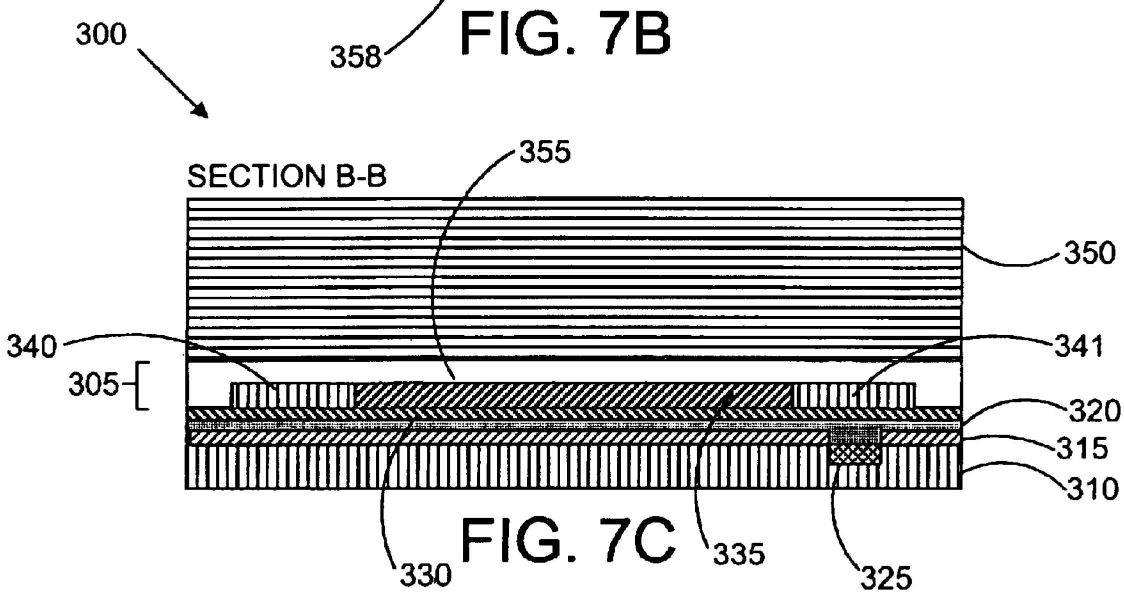


FIG. 7C

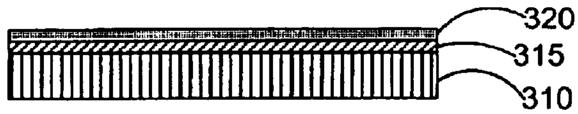


FIG. 8A

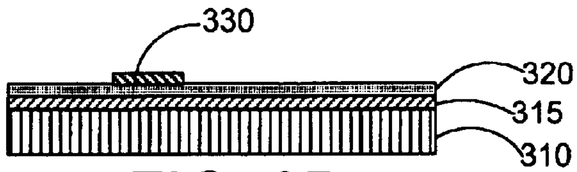


FIG. 8B

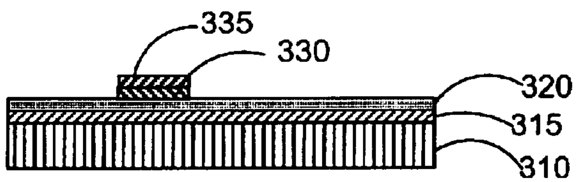


FIG. 8C

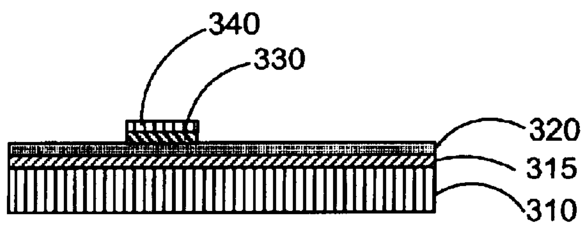


FIG. 8D

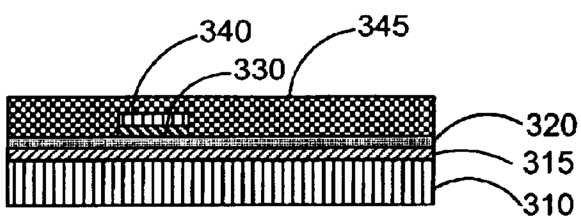


FIG. 8E

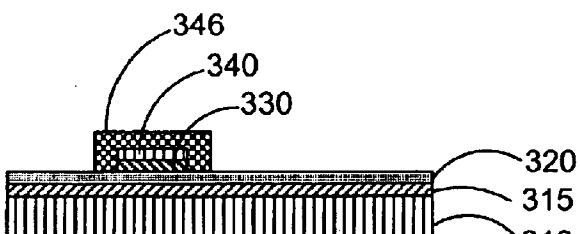


FIG. 8F

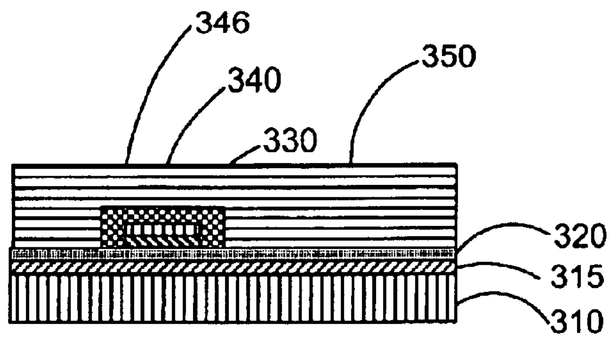


FIG. 8G

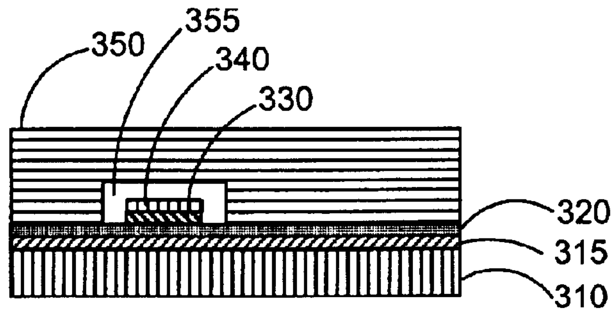


FIG. 8H

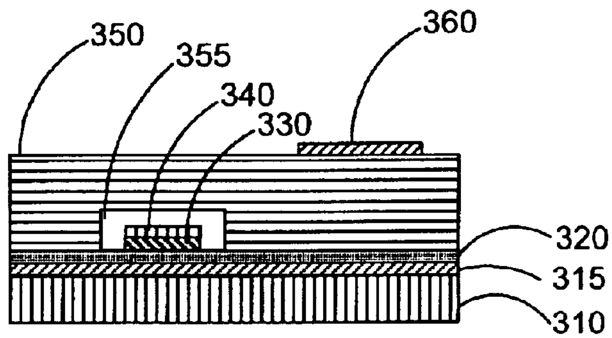


FIG. 8I

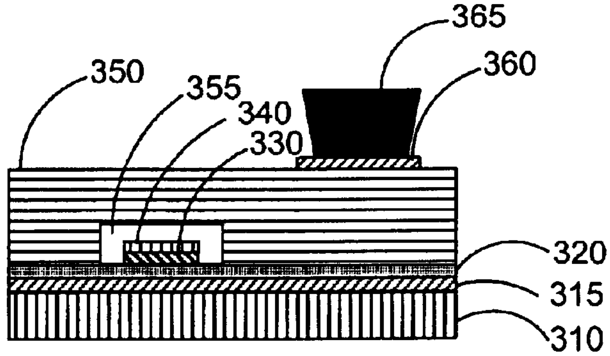


FIG. 8J

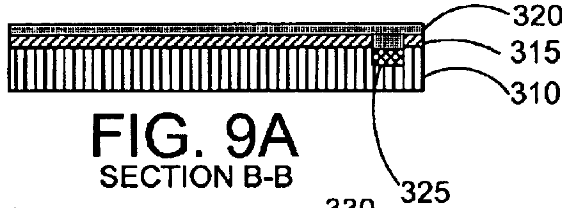


FIG. 9A
SECTION B-B

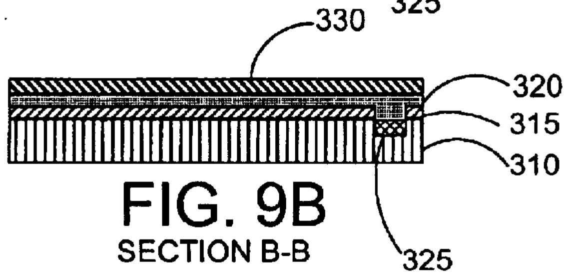


FIG. 9B
SECTION B-B

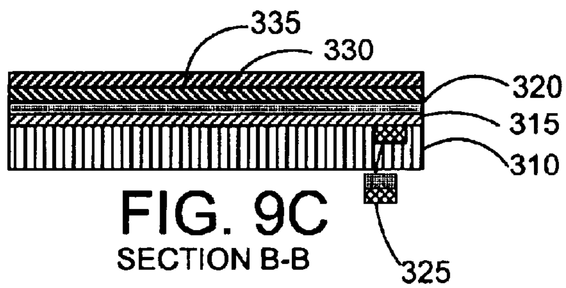


FIG. 9C
SECTION B-B

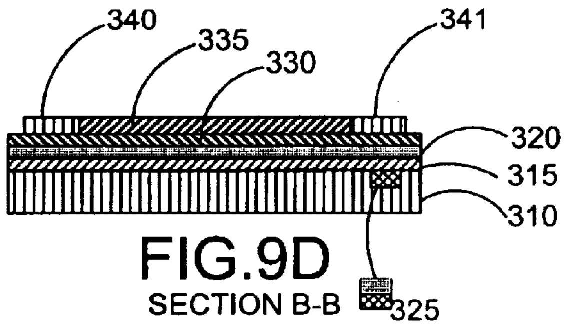


FIG.9D
SECTION B-B

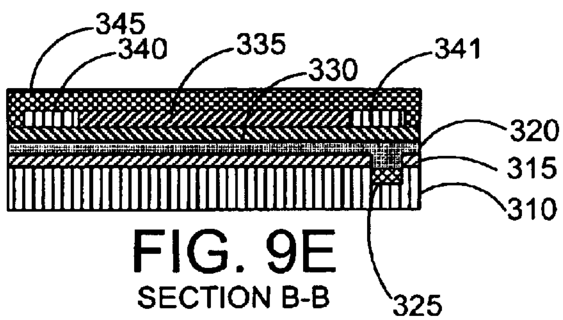


FIG. 9E
SECTION B-B

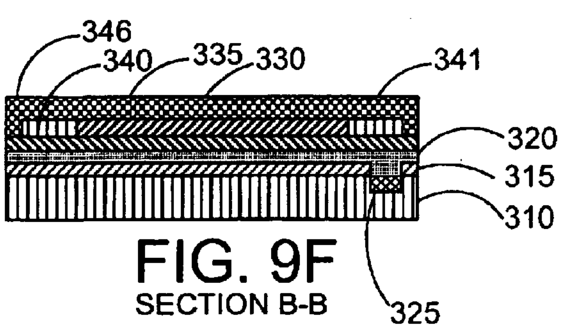


FIG. 9F
SECTION B-B

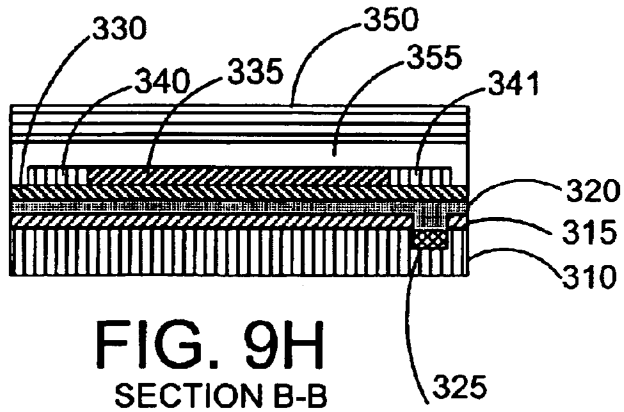


FIG. 9H
SECTION B-B

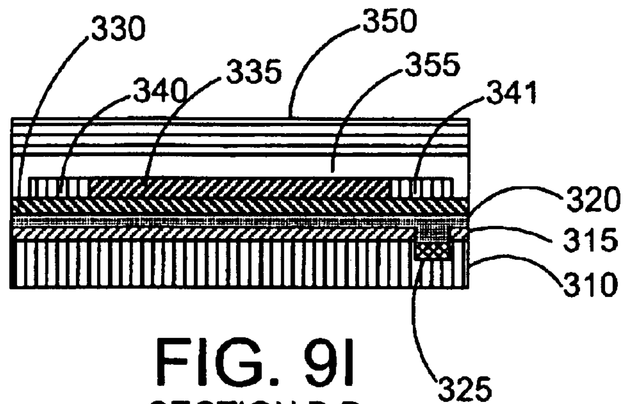


FIG. 9I
SECTION B-B

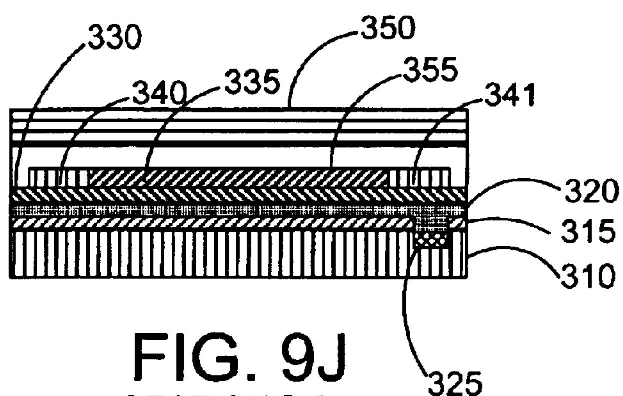


FIG. 9J
SECTION B-B

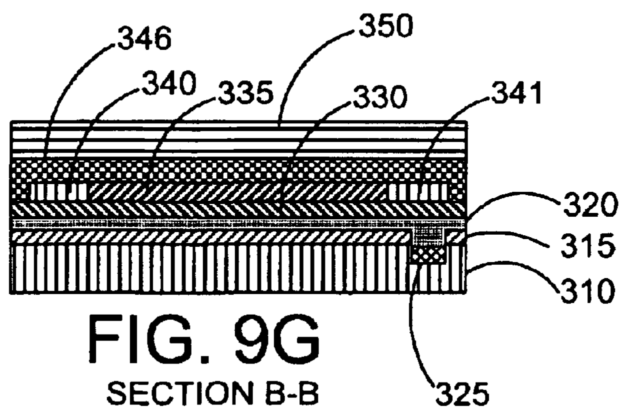


FIG. 9G
SECTION B-B

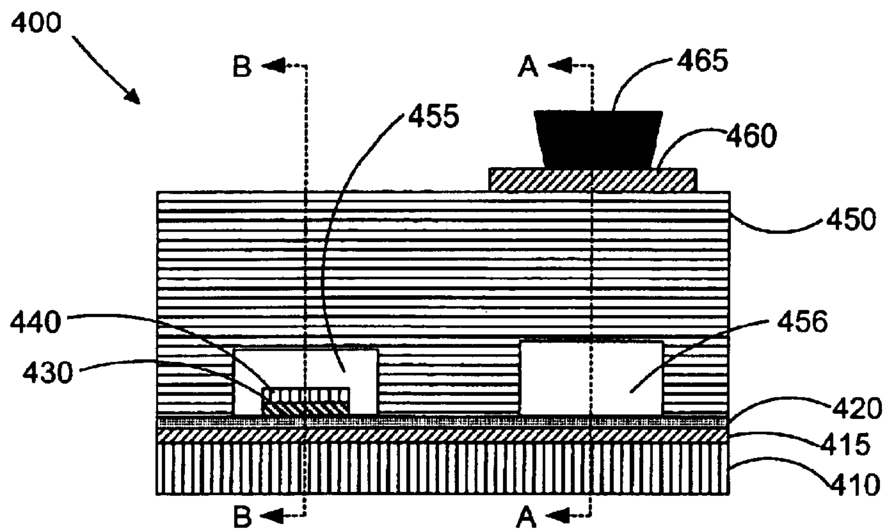


FIG. 10A

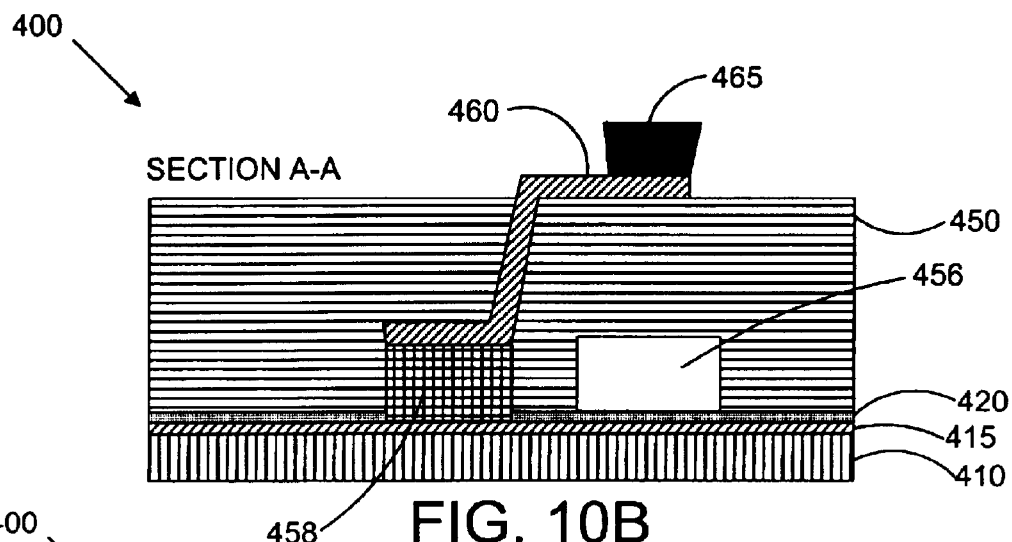


FIG. 10B

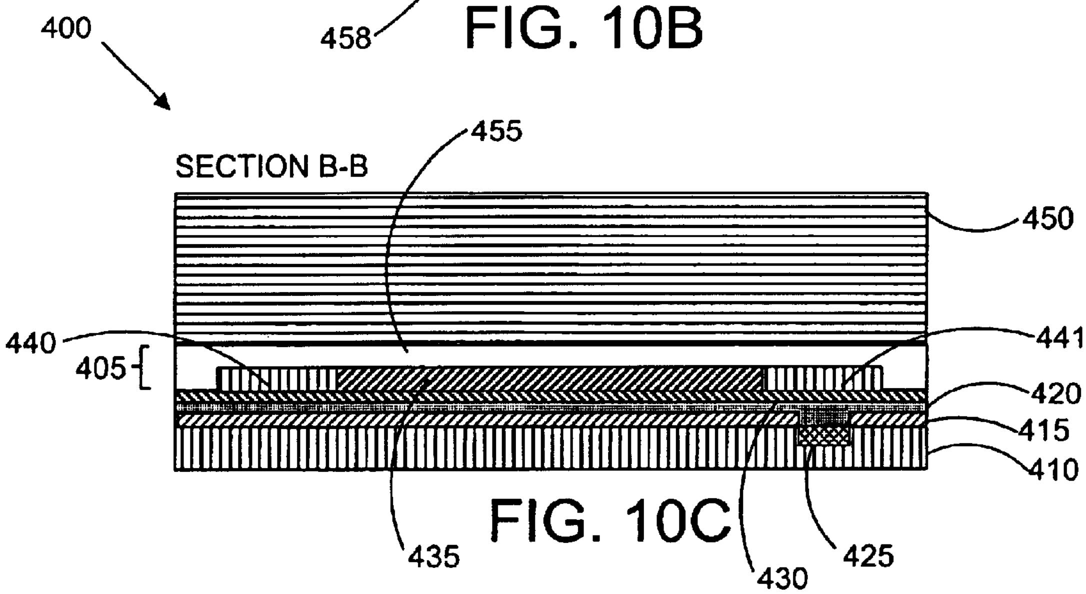


FIG. 10C

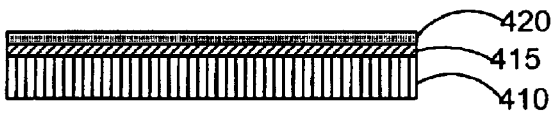


FIG. 11A

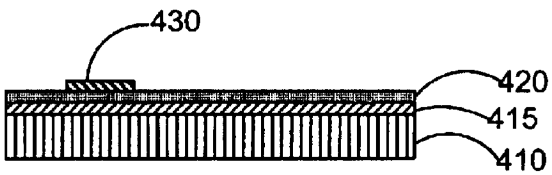


FIG. 11B

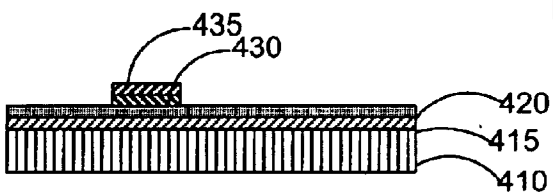


FIG. 11C

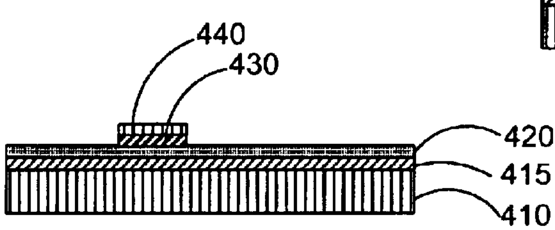


FIG. 11D

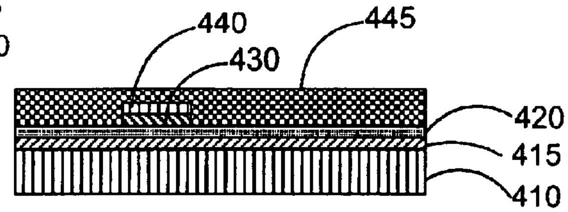


FIG. 11E

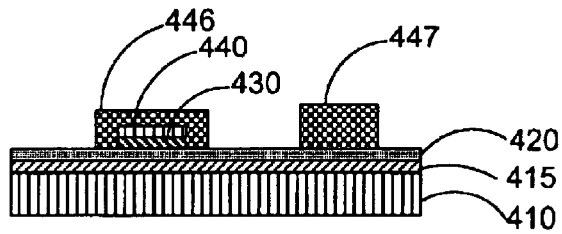


FIG. 11F

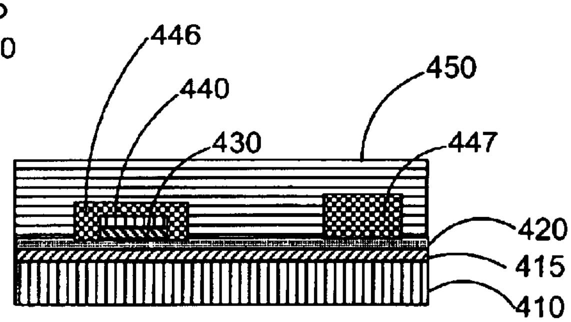


FIG. 11G

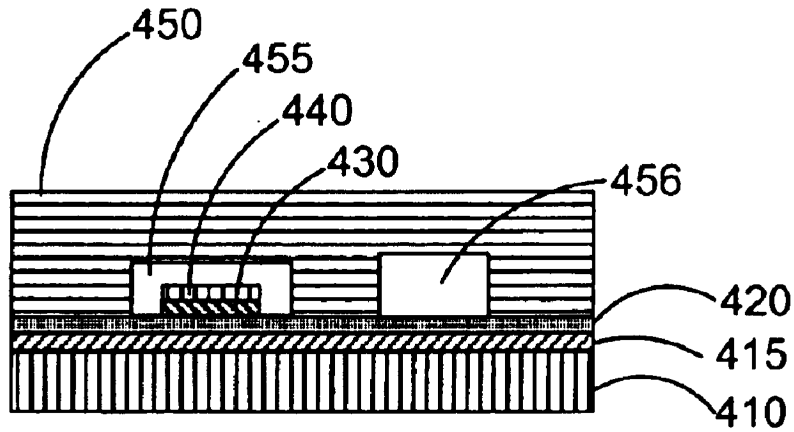


FIG. 11H

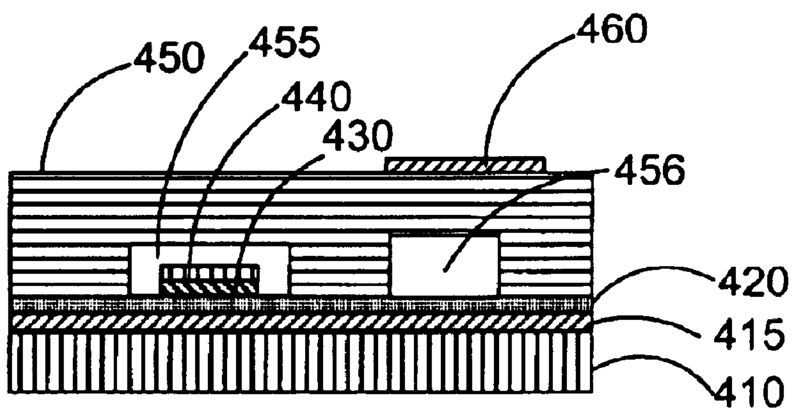


FIG. 11I

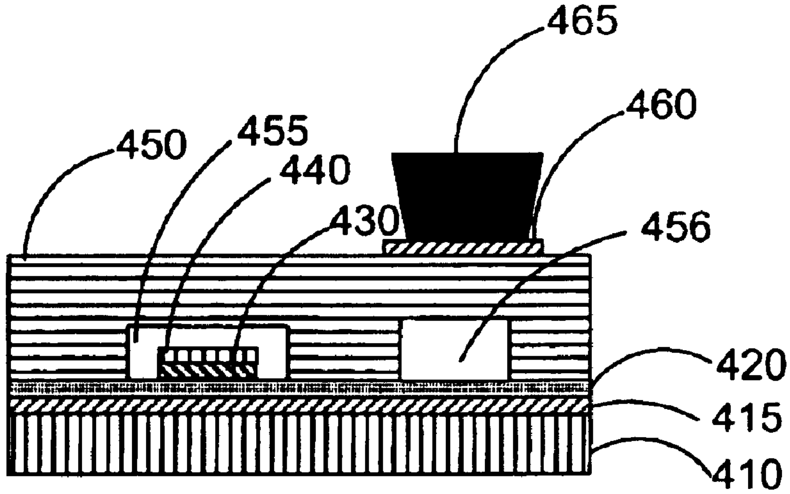


FIG. 11J

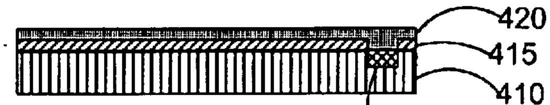


FIG. 12A
SECTION B-B

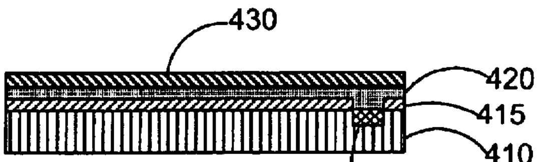


FIG. 12B
SECTION B-B

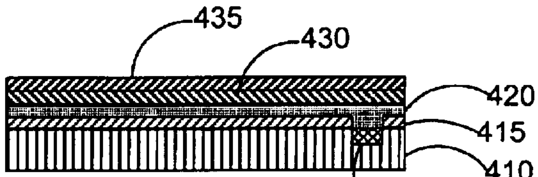


FIG. 12C

SECTION B-B

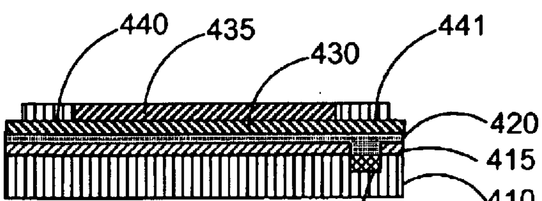


FIG. 12D
SECTION B-B

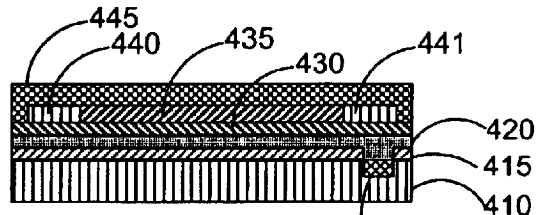


FIG. 12E
SECTION B-B

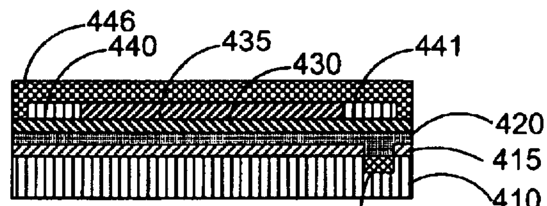


FIG. 12F
SECTION B-B

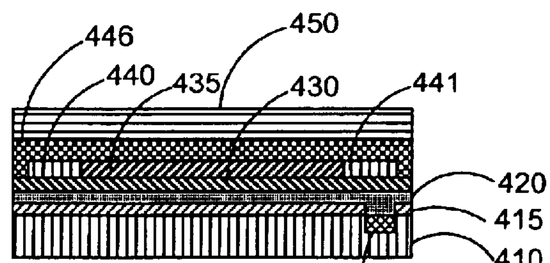


FIG. 12 G
SECTION B-B

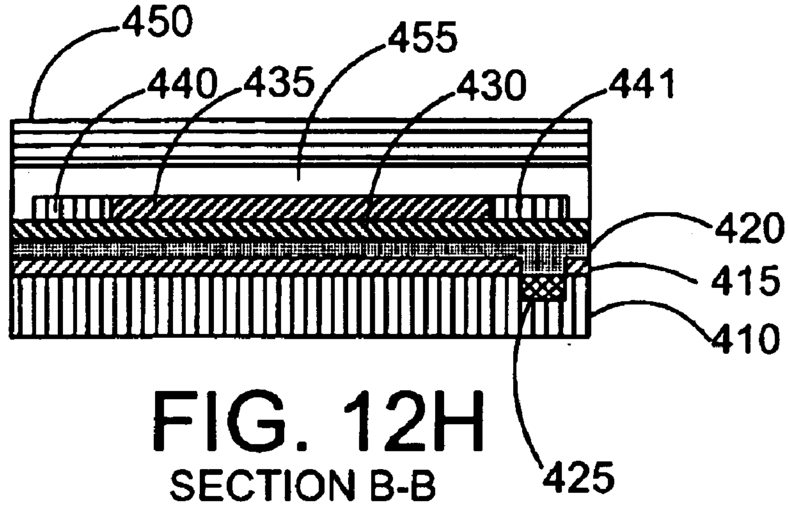


FIG. 12H
SECTION B-B

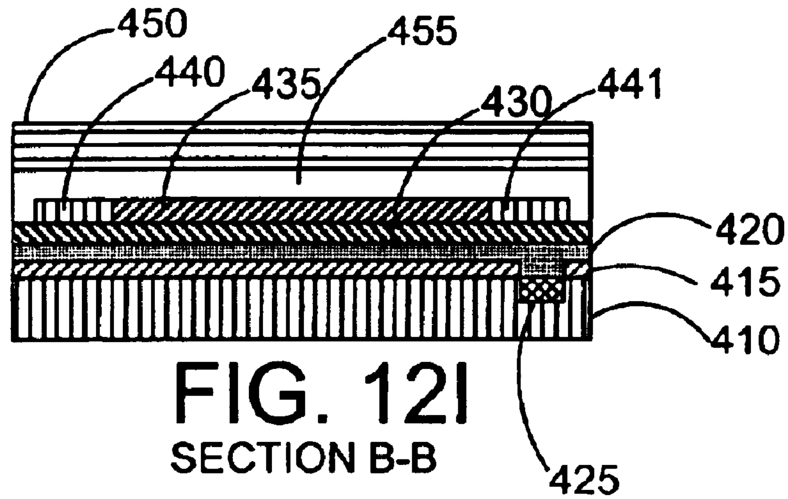


FIG. 12I
SECTION B-B

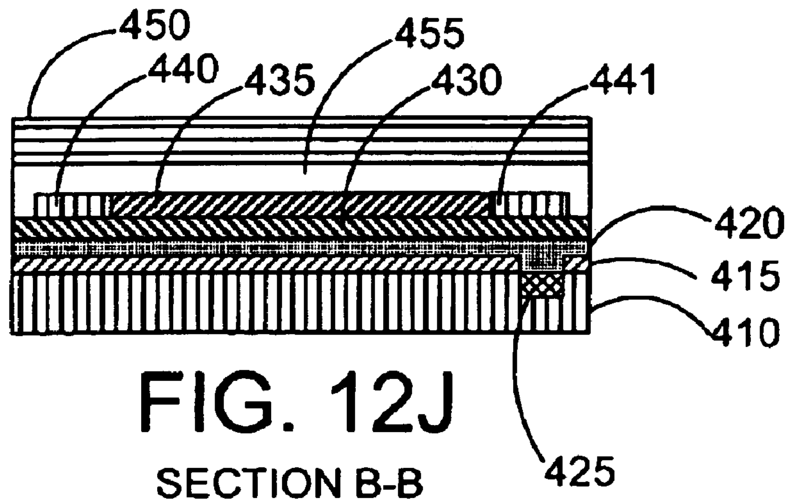


FIG. 12J
SECTION B-B

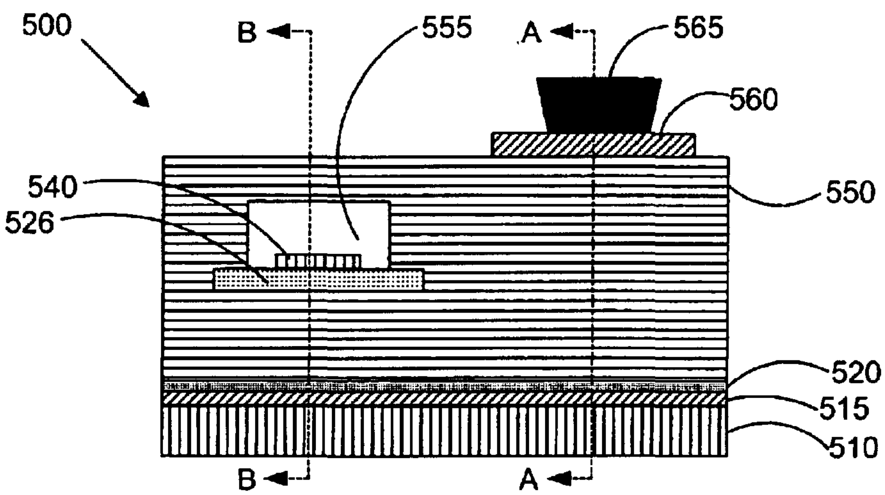


FIG. 13A

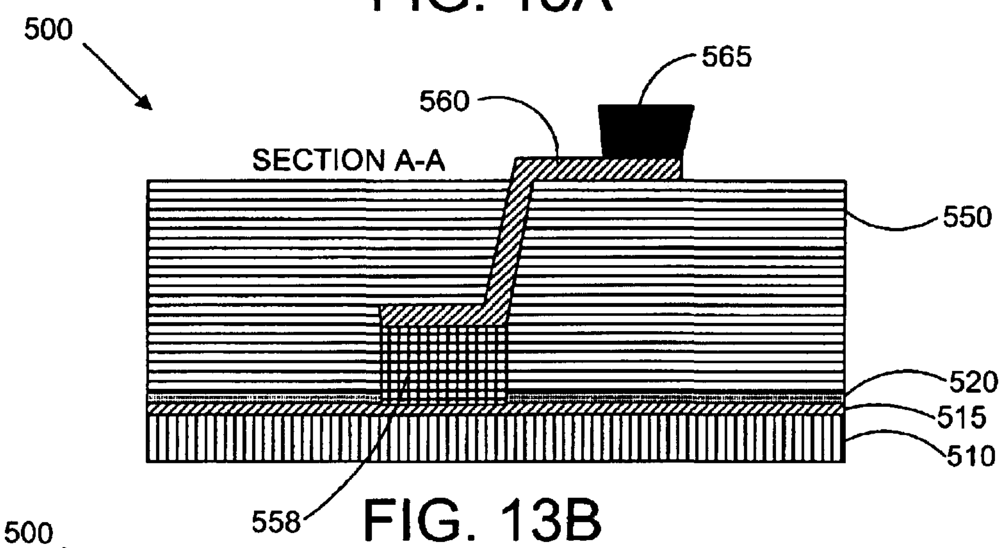


FIG. 13B

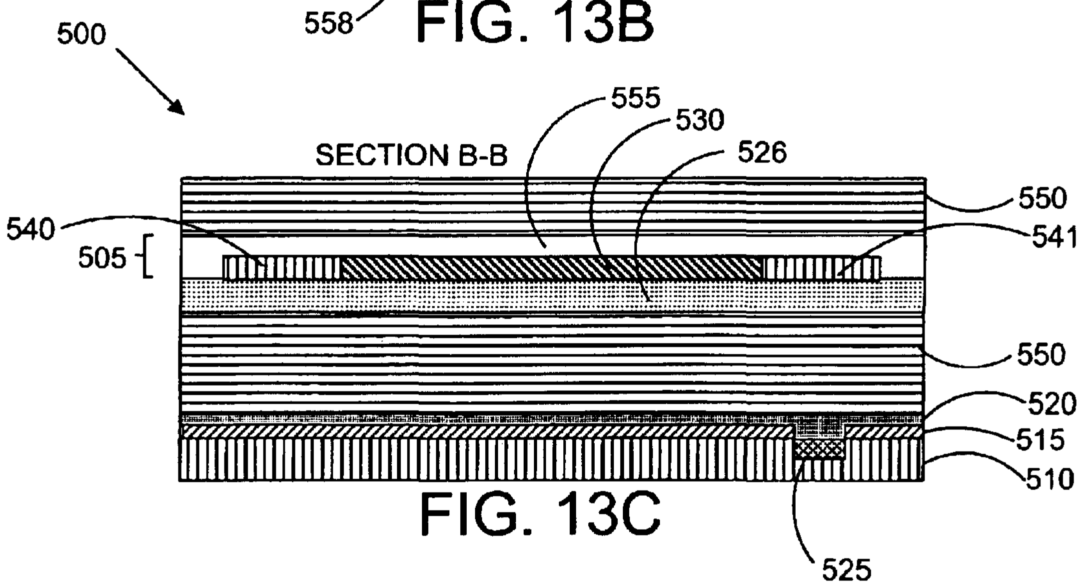


FIG. 13C

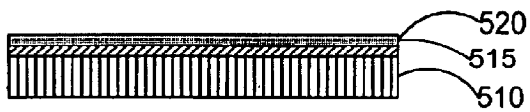


FIG. 14A

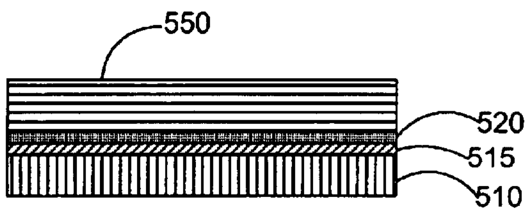


FIG. 14B

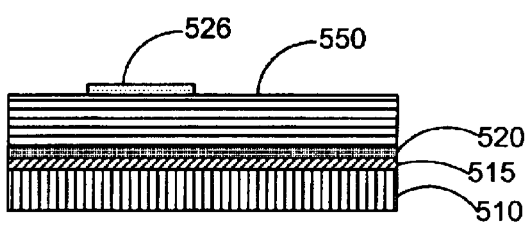


FIG. 14C

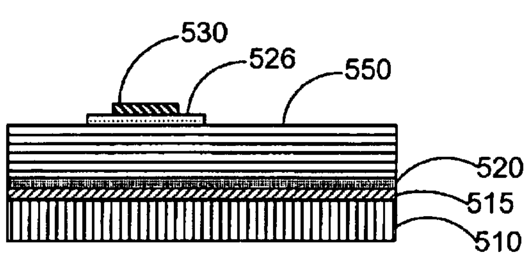


FIG. 14D

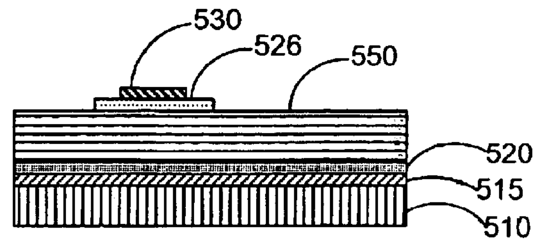


FIG. 14E

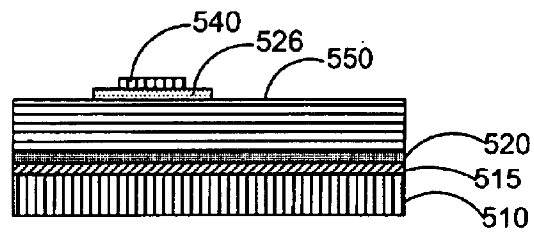


FIG. 14F

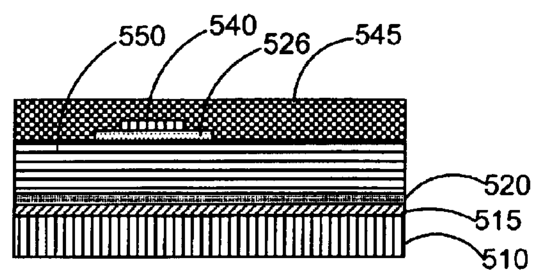


FIG. 14G

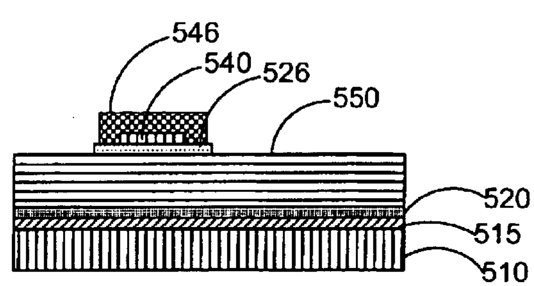


FIG. 14H

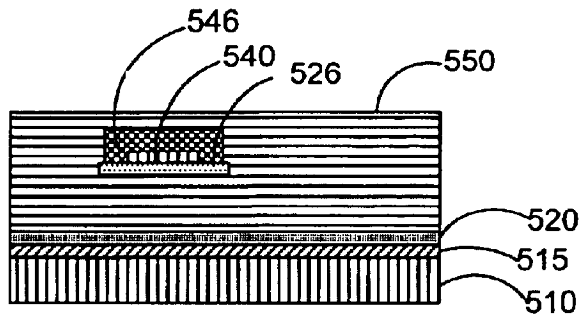


FIG. 14I

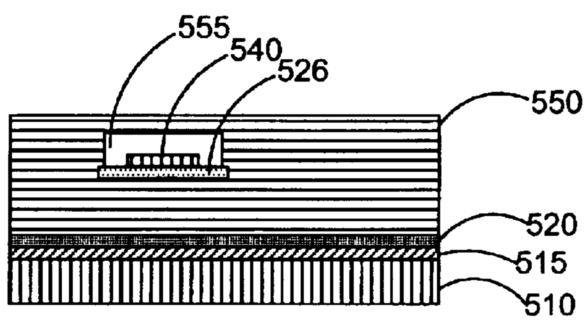


FIG. 14J

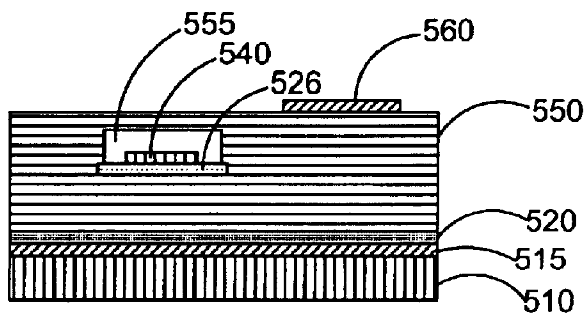


FIG. 14K

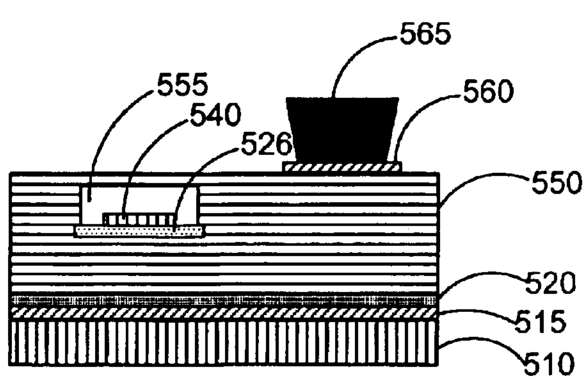


FIG. 14L

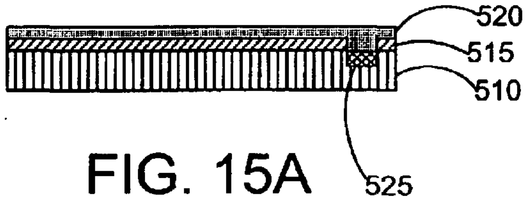


FIG. 15A
SECTION B-B

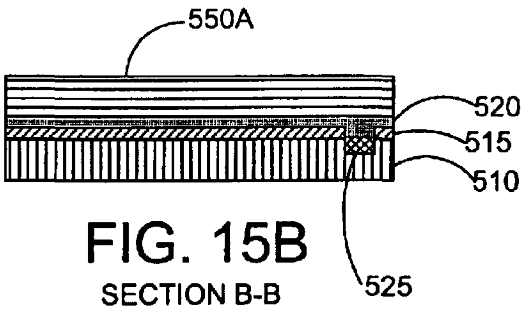


FIG. 15B
SECTION B-B

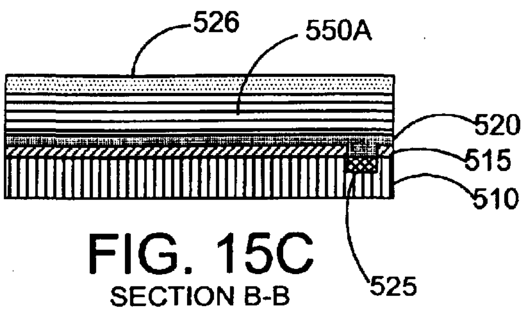


FIG. 15C
SECTION B-B

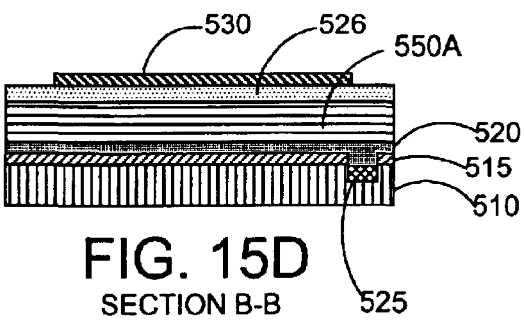


FIG. 15D
SECTION B-B

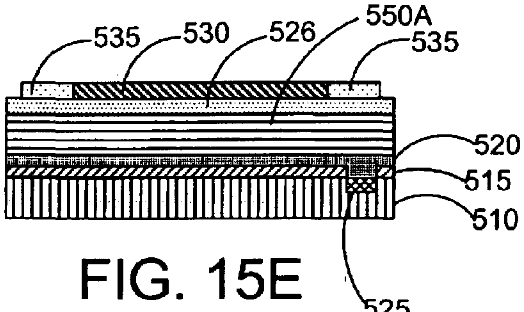


FIG. 15E
SECTION B-B

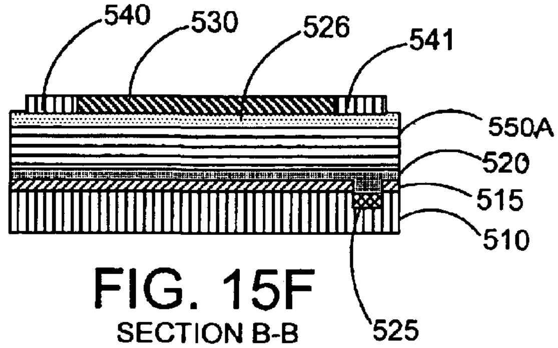


FIG. 15F
SECTION B-B

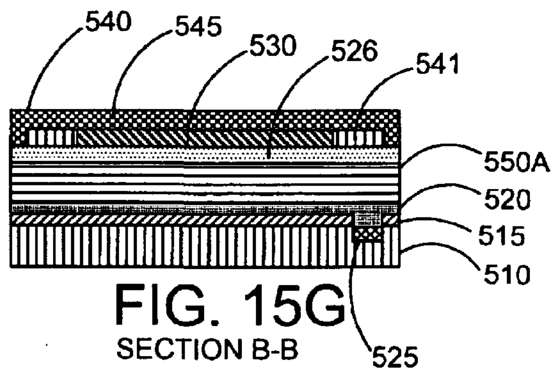


FIG. 15G
SECTION B-B

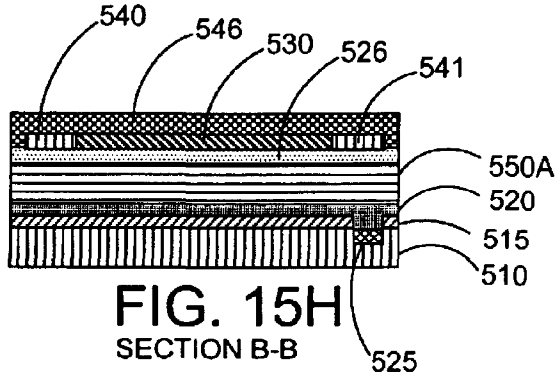


FIG. 15H
SECTION B-B

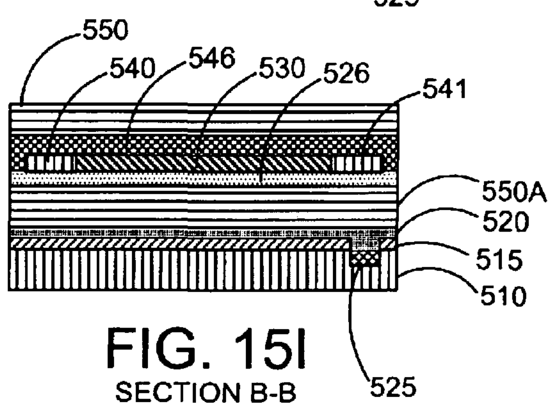


FIG. 15I
SECTION B-B

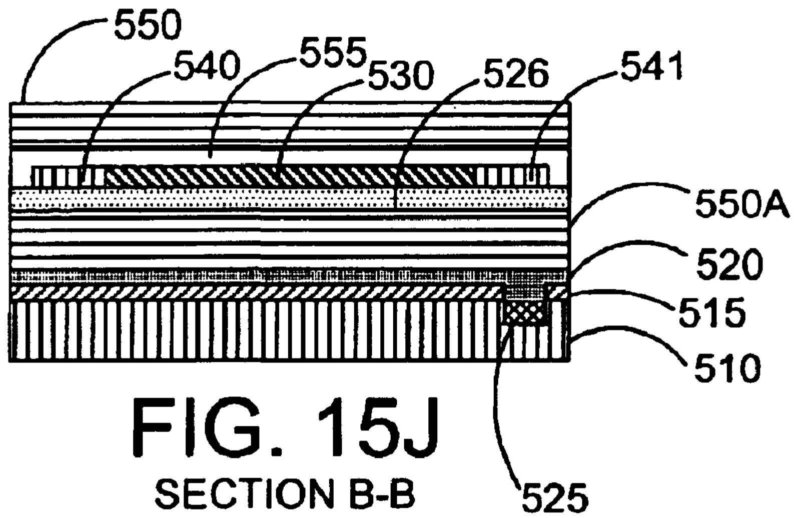


FIG. 15J
SECTION B-B

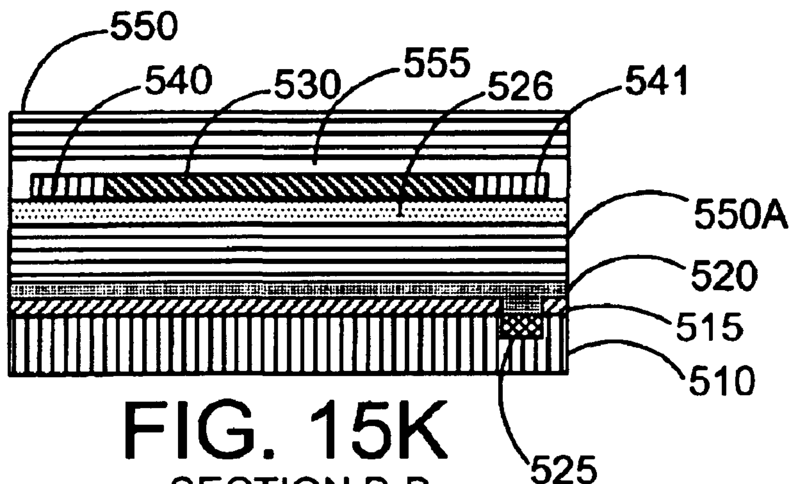


FIG. 15K
SECTION B-B

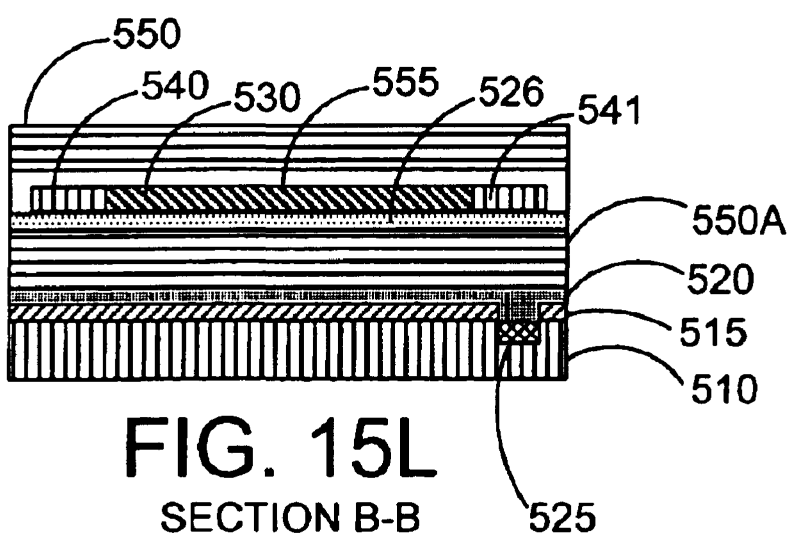


FIG. 15L
SECTION B-B

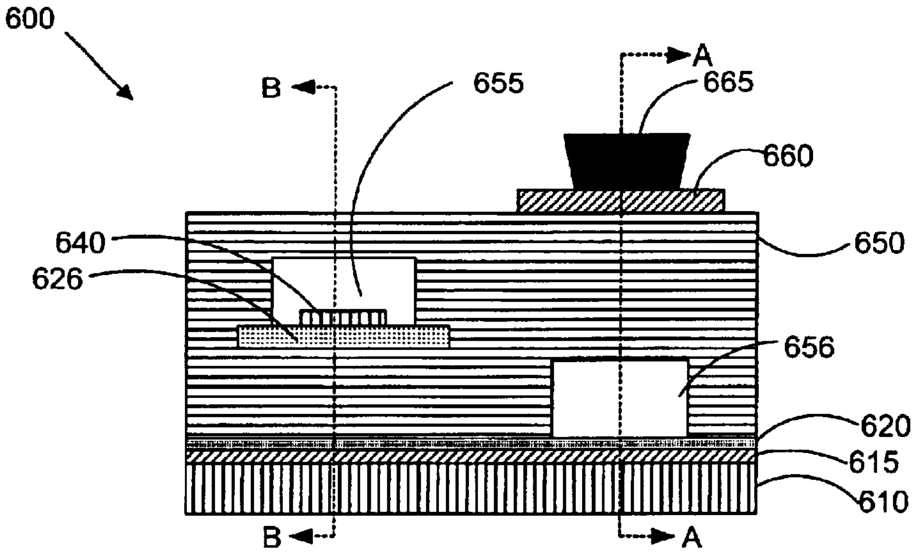


FIG. 16A

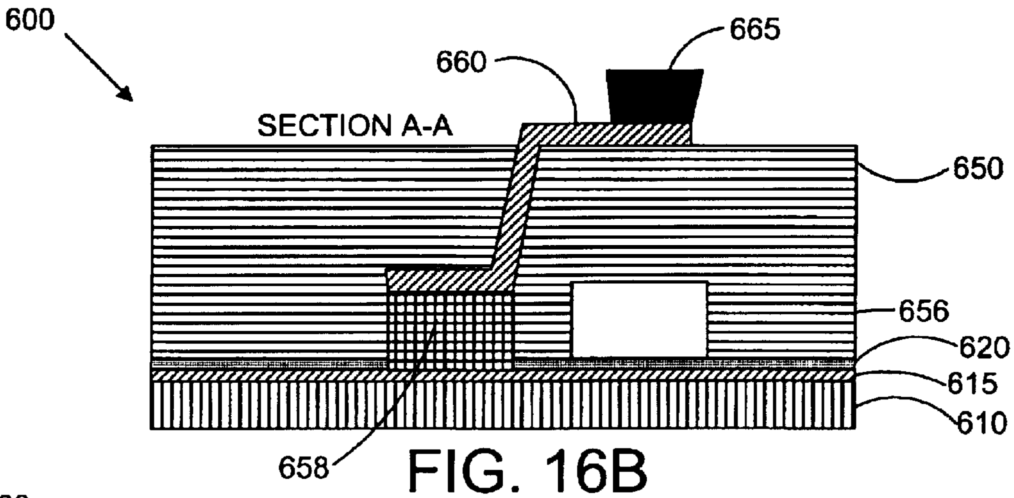


FIG. 16B

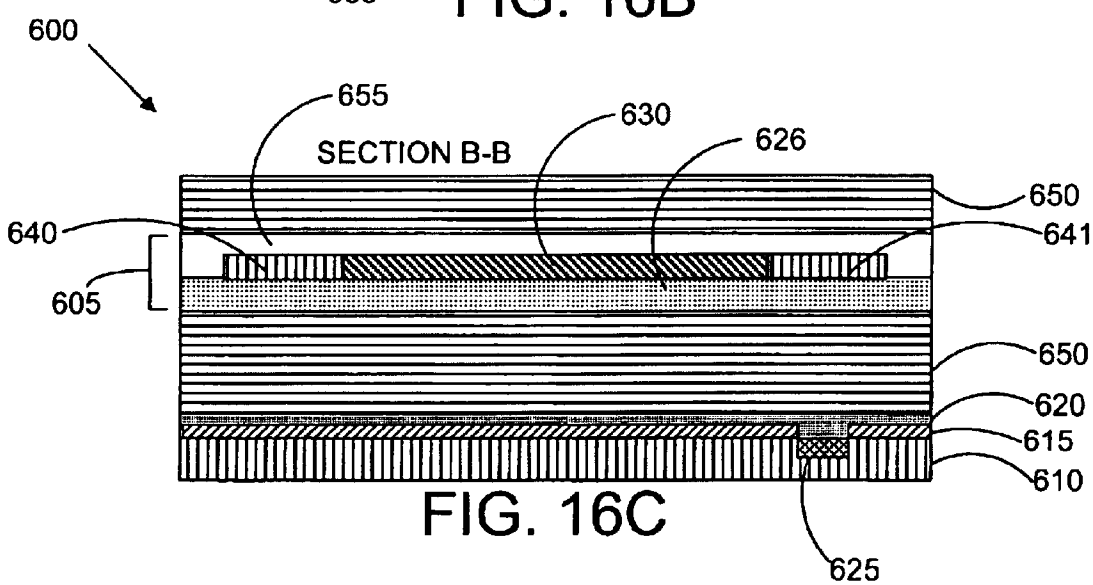


FIG. 16C

FIG. 17A

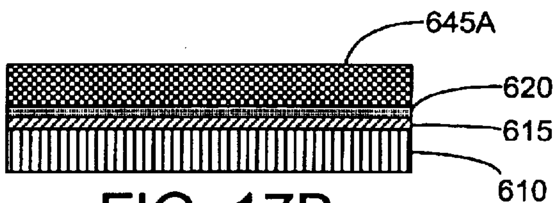


FIG. 17B

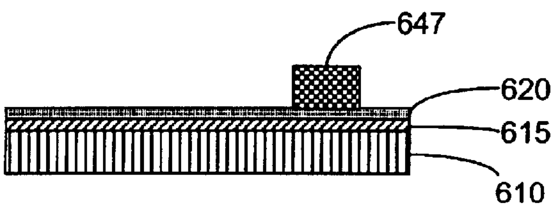


FIG. 17C

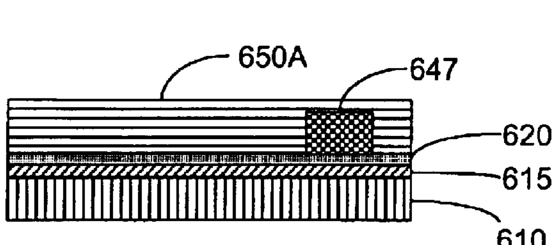


FIG. 17D

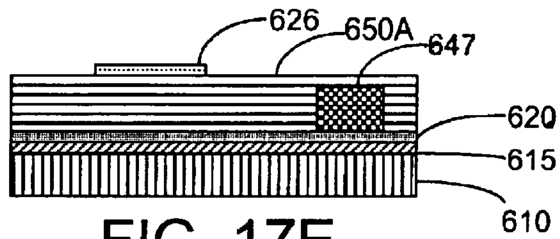


FIG. 17E

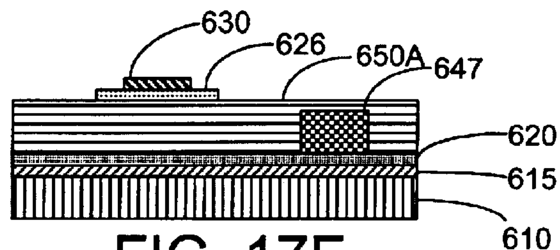


FIG. 17F

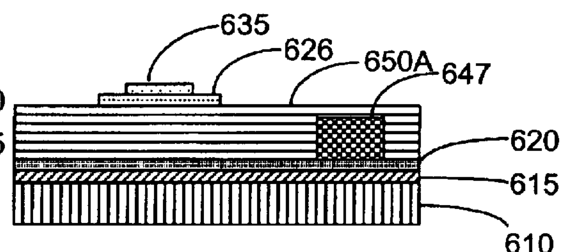


FIG. 17G

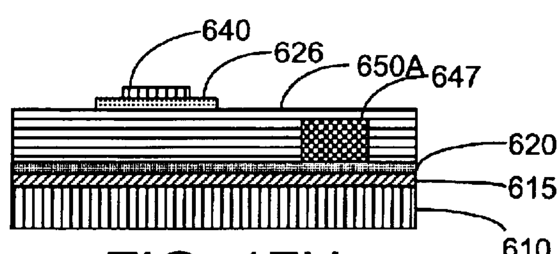


FIG. 17H

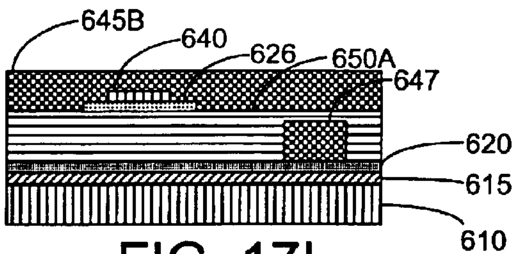


FIG. 17I

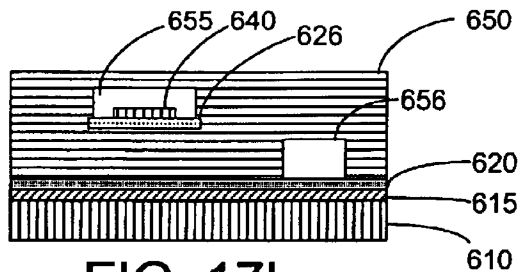


FIG. 17L

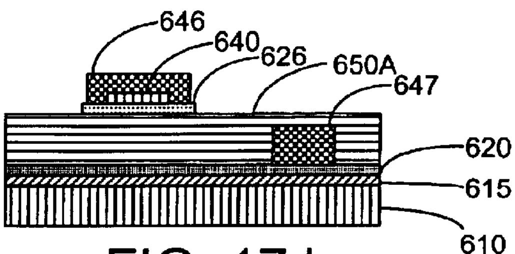


FIG. 17J

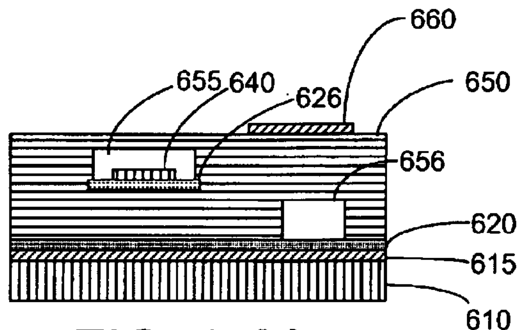


FIG. 17M

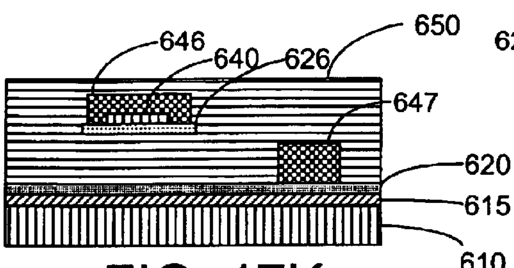


FIG. 17K

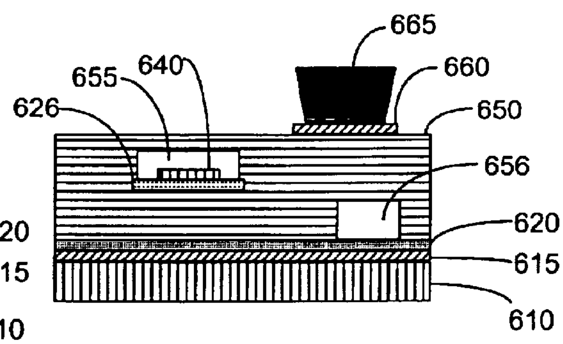


FIG. 17N

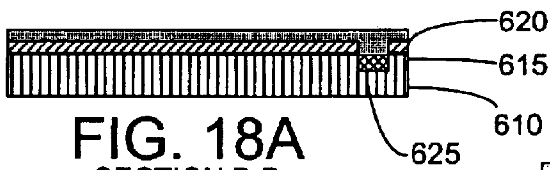


FIG. 18A
SECTION B-B

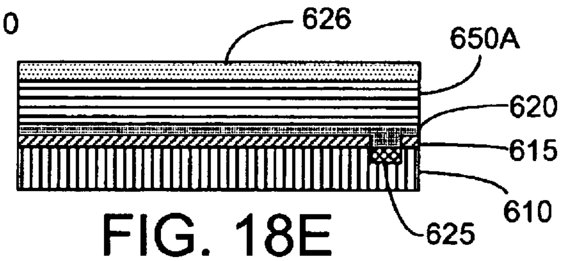


FIG. 18E
SECTION B-B

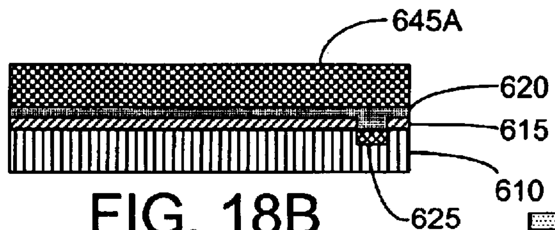


FIG. 18B
SECTION B-B

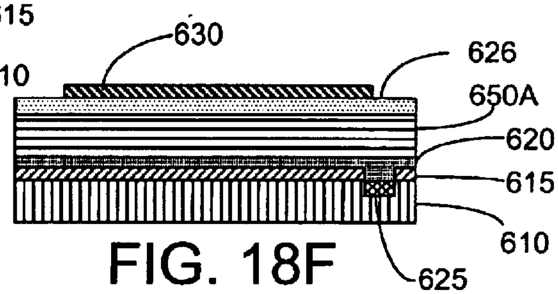


FIG. 18F
SECTION B-B

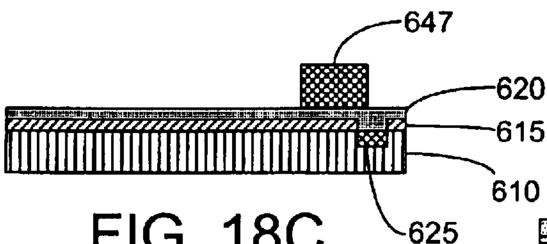


FIG. 18C
SECTION B-B

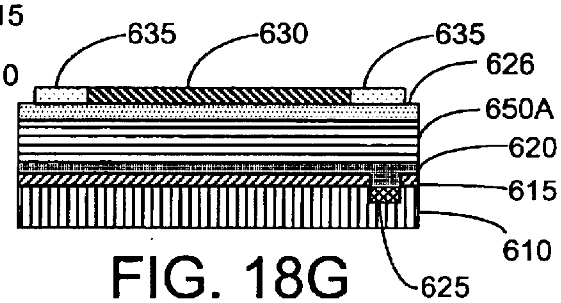


FIG. 18G
SECTION B-B

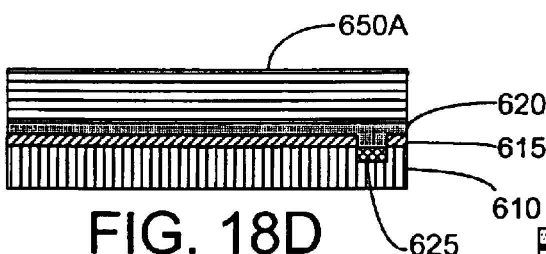


FIG. 18D
SECTION B-B

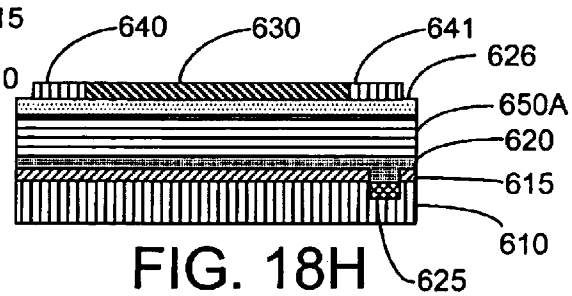


FIG. 18H
SECTION B-B

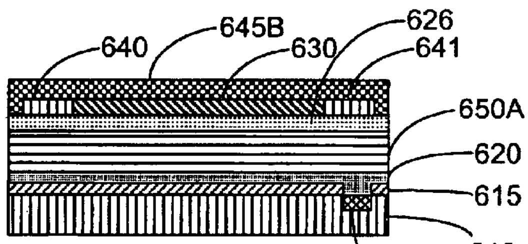


FIG. 18I
SECTION B-B

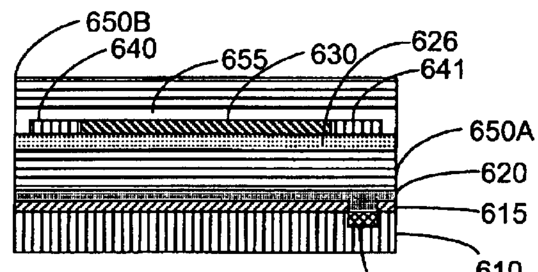


FIG. 18L
SECTION B-B

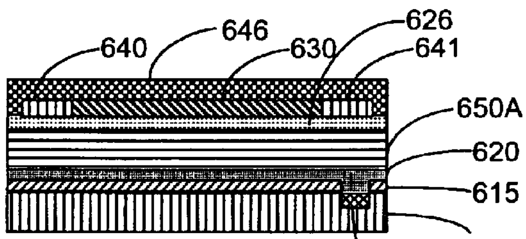


FIG. 18J
SECTION B-B

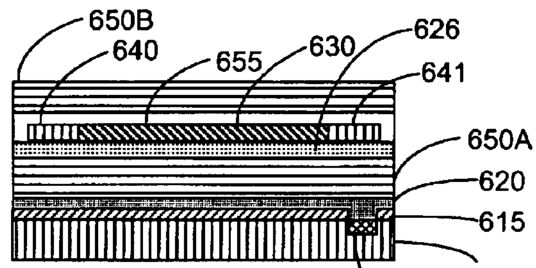


FIG. 18M
SECTION B-B

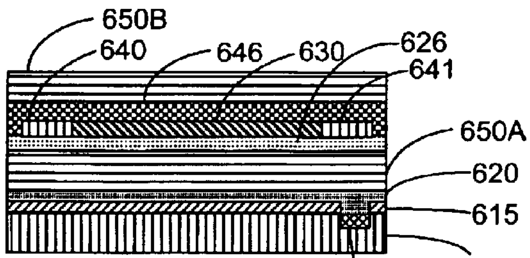


FIG. 18K
SECTION B-B

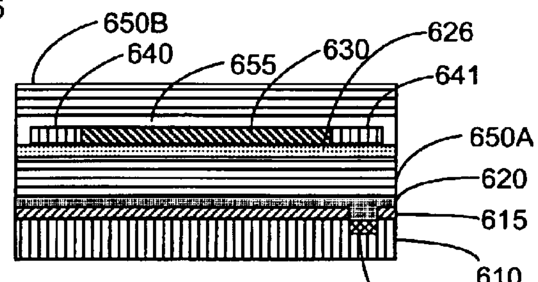


FIG. 18N
SECTION B-B

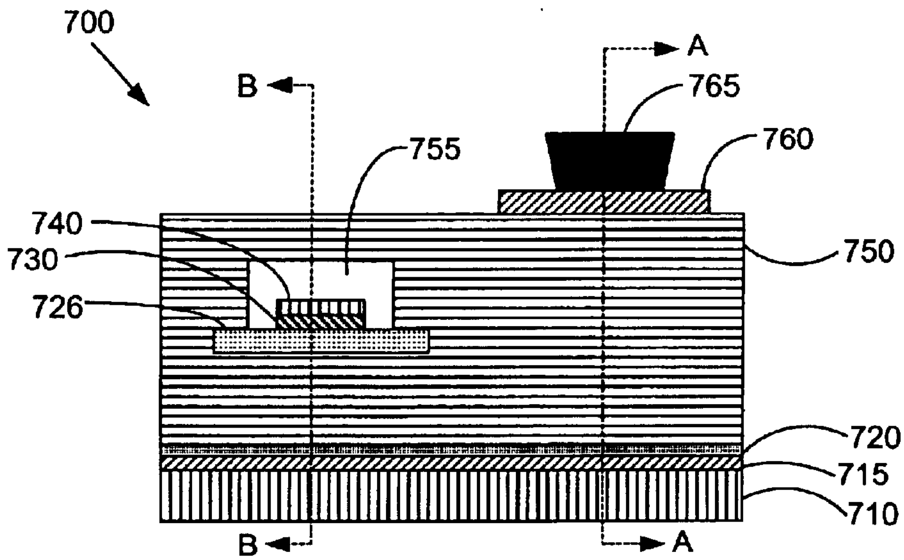


FIG. 19A

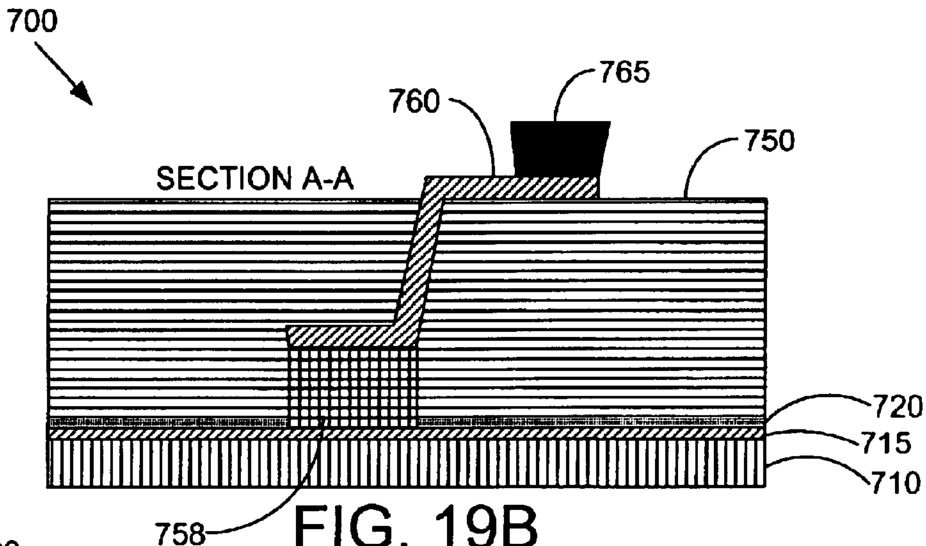


FIG. 19B

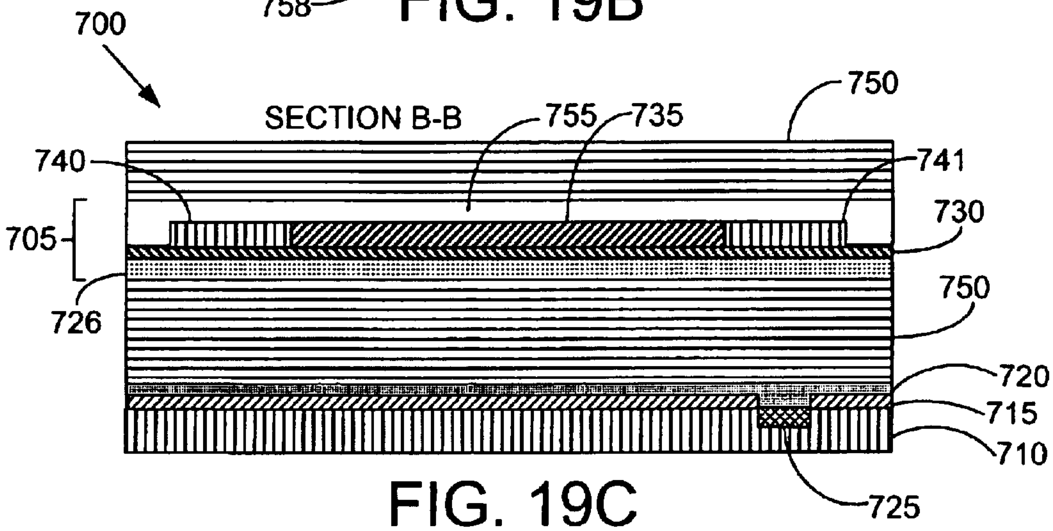


FIG. 19C

FIG. 20A

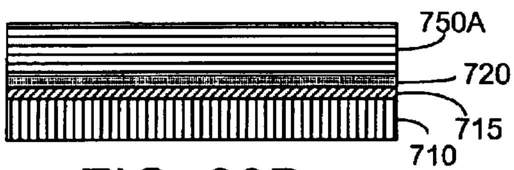


FIG. 20B

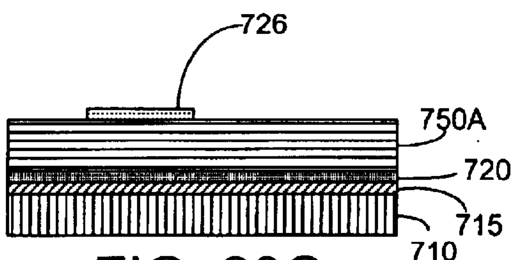


FIG. 20C

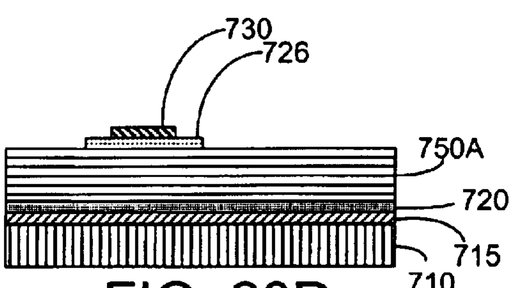


FIG. 20D

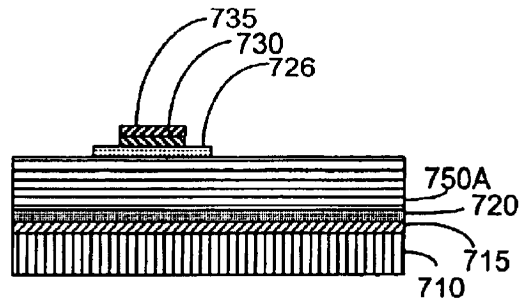


FIG. 20E

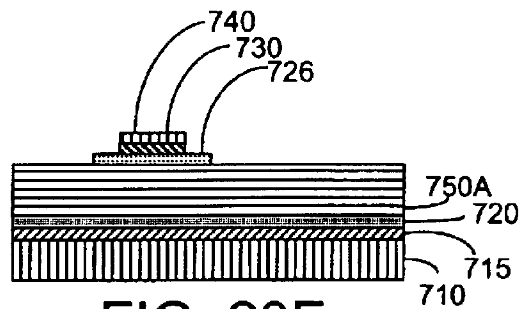


FIG. 20F

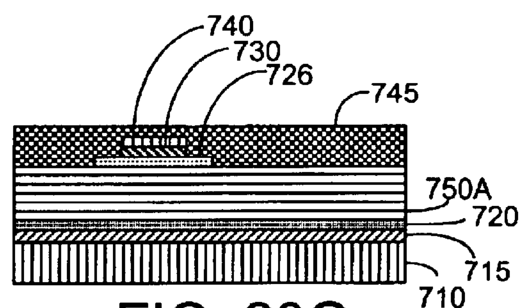


FIG. 20G

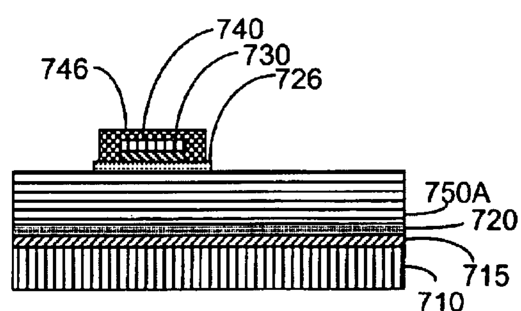


FIG. 20H

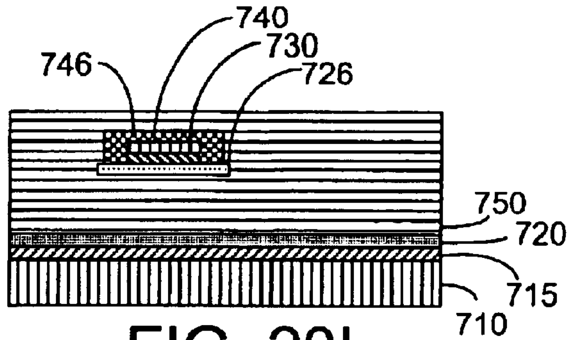


FIG. 20I

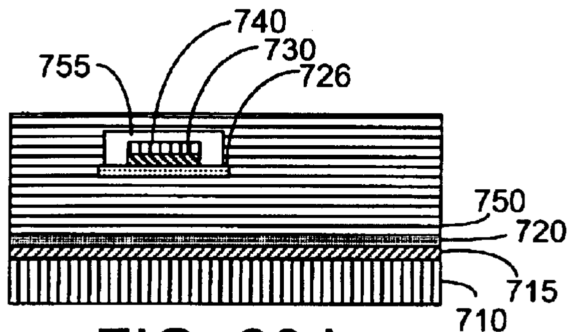


FIG. 20J

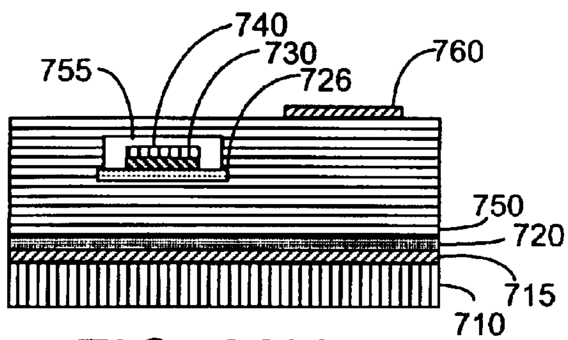


FIG. 20K

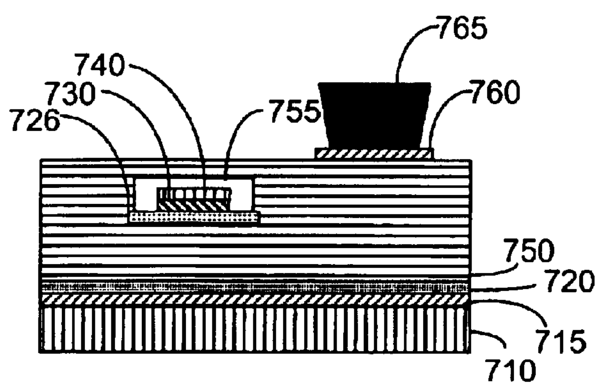


FIG. 20L

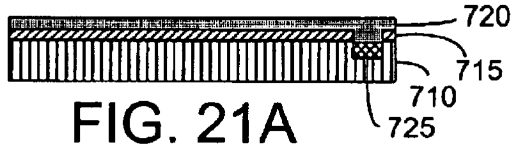


FIG. 21A
SECTION B-B

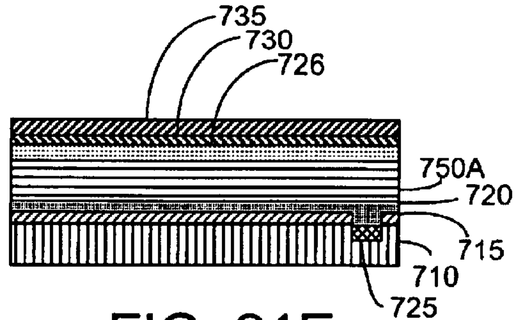


FIG. 21E
SECTION B-B

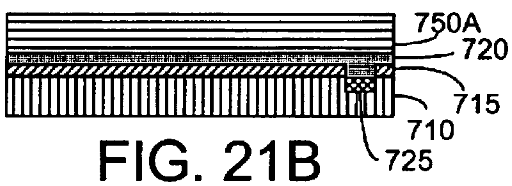


FIG. 21B
SECTION B-B

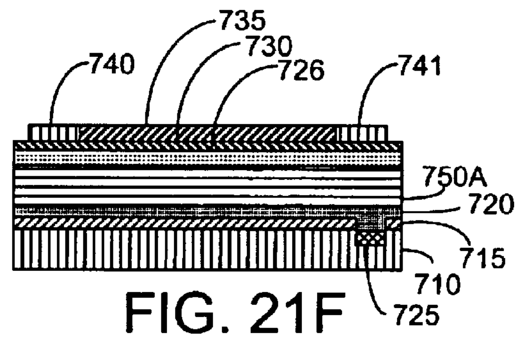


FIG. 21F
SECTION B-B

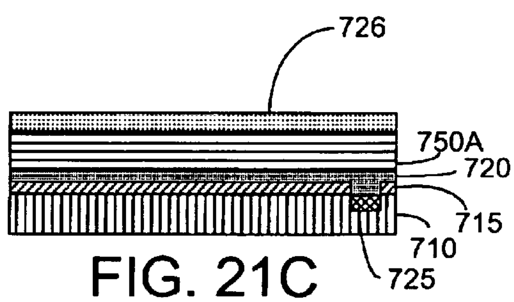


FIG. 21C
SECTION B-B

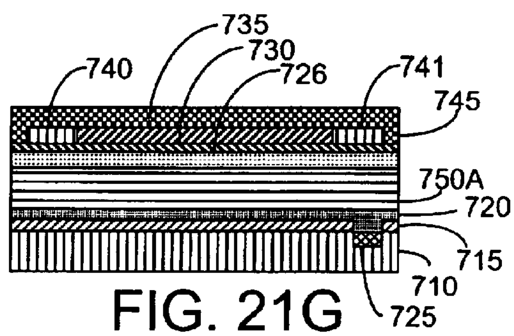


FIG. 21G
SECTION B-B

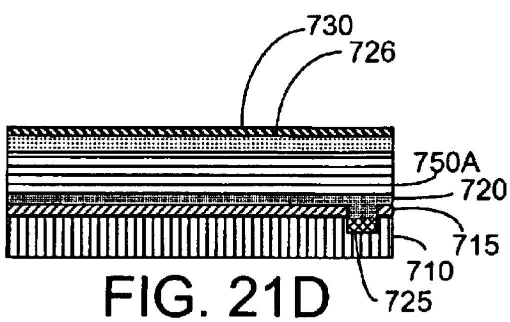


FIG. 21D
SECTION B-B

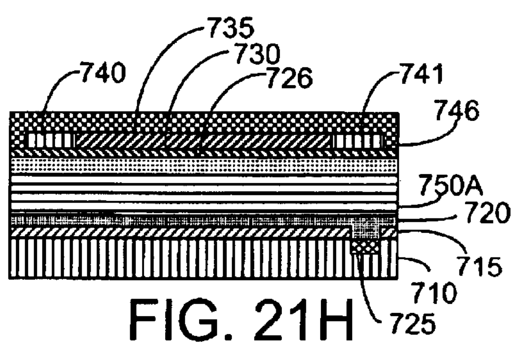


FIG. 21H
SECTION B-B

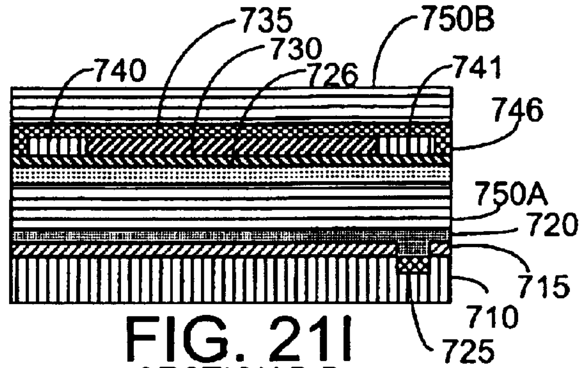


FIG. 21I
SECTION B-B

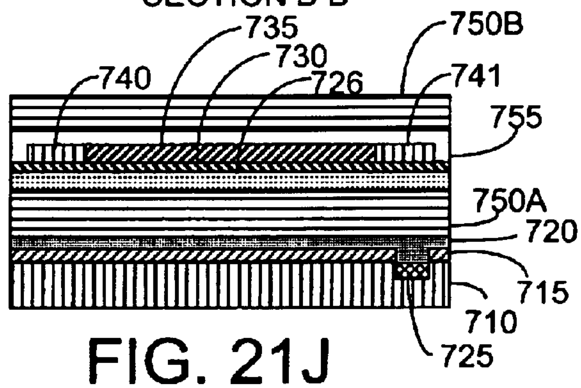


FIG. 21J
SECTION B-B

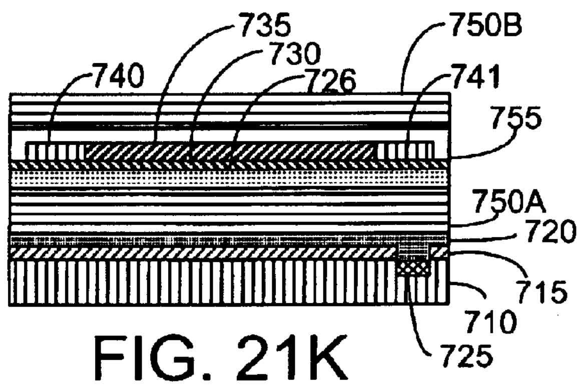


FIG. 21K
SECTION B-B

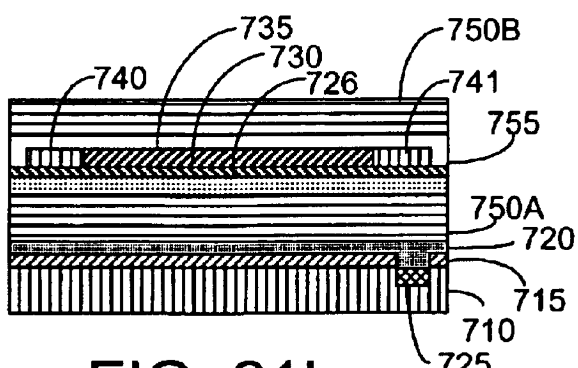


FIG. 21L
SECTION B-B

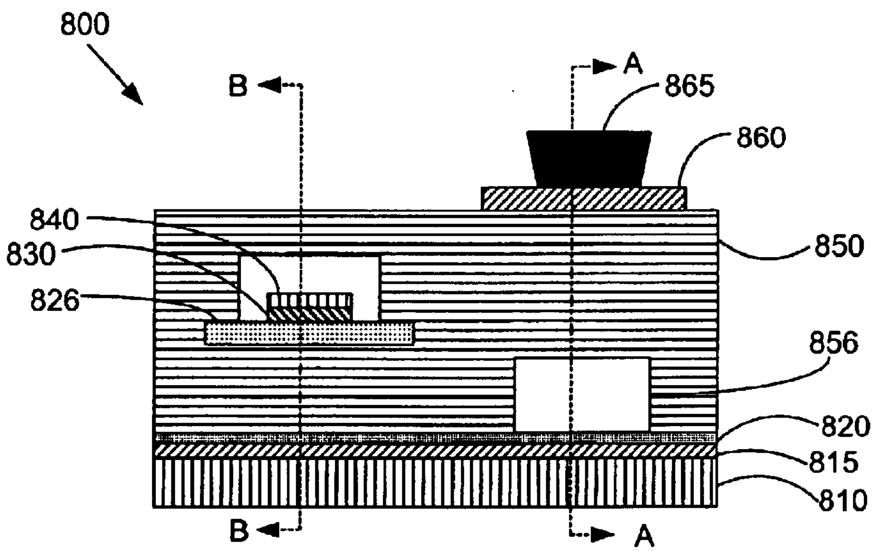


FIG. 22A

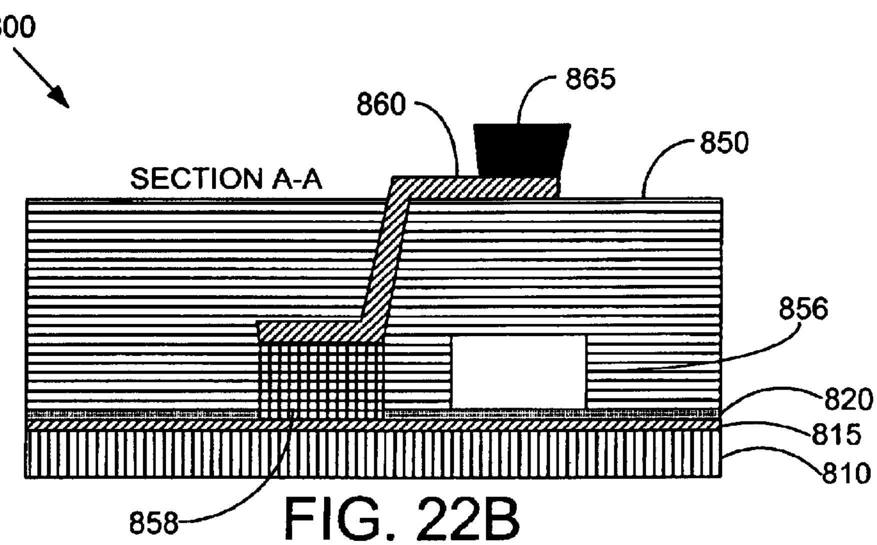


FIG. 22B

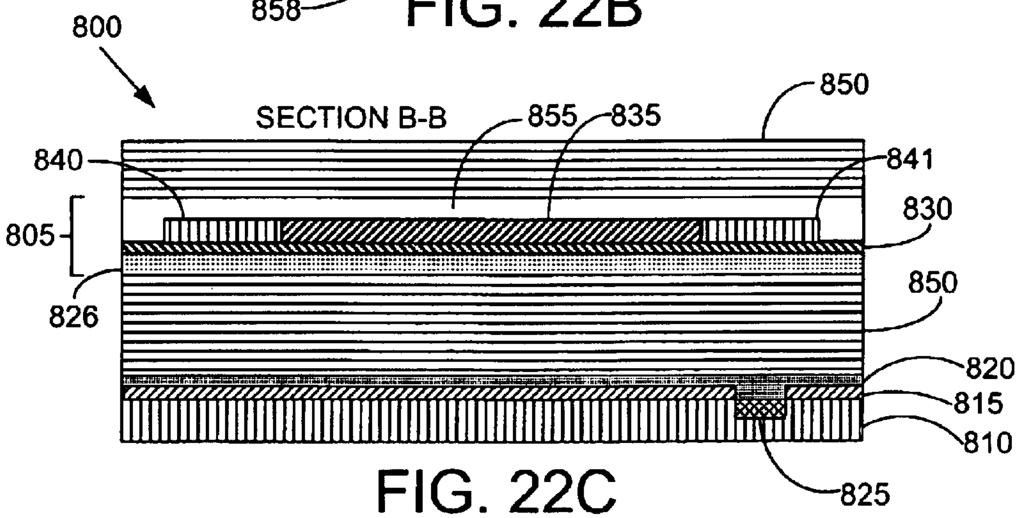


FIG. 22C

FIG. 23A

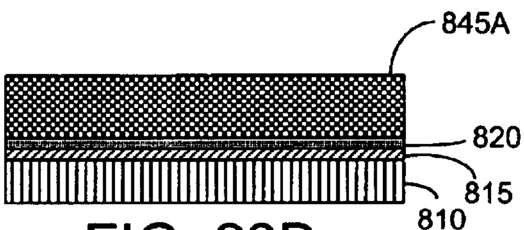


FIG. 23B

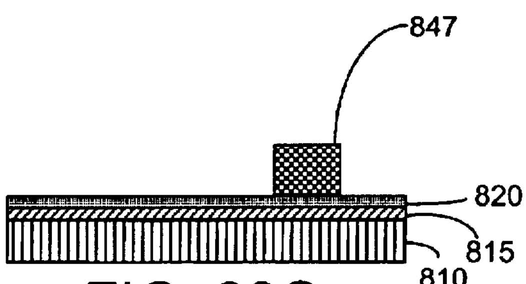


FIG. 23C

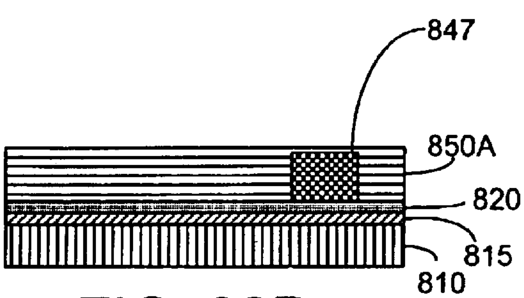


FIG. 23D

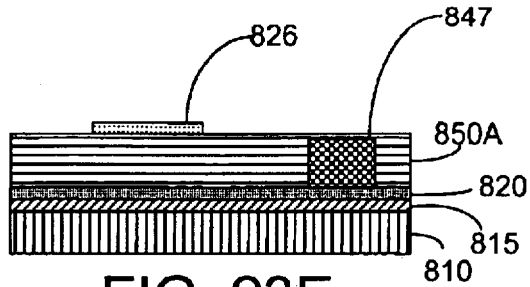


FIG. 23E

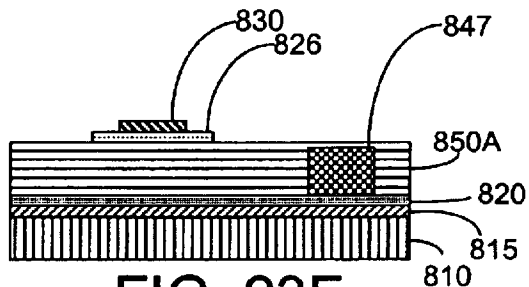


FIG. 23F

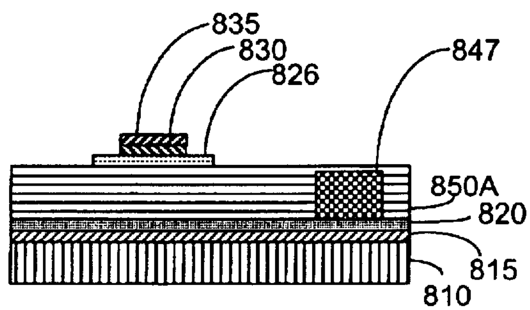


FIG. 23G

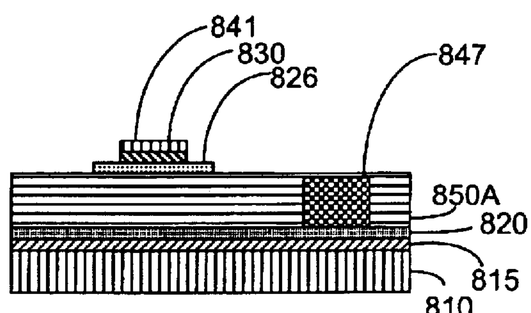


FIG. 23H

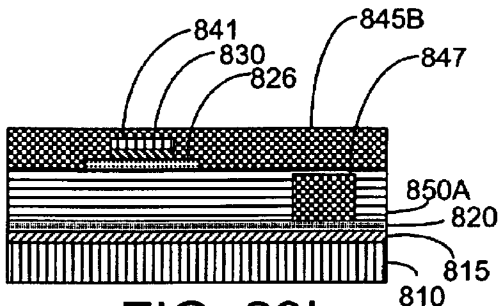


FIG. 23I

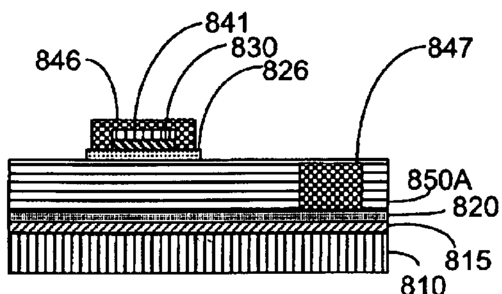


FIG. 23J

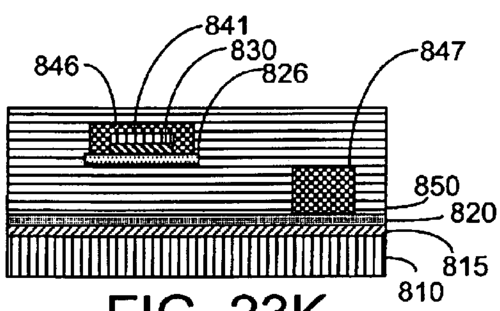


FIG. 23K

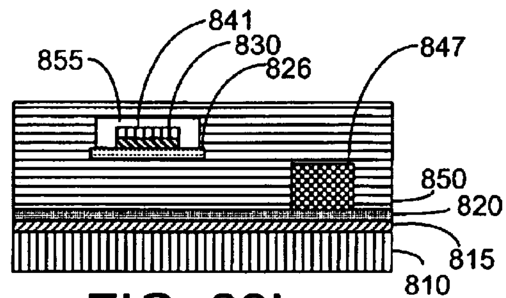


FIG. 23L

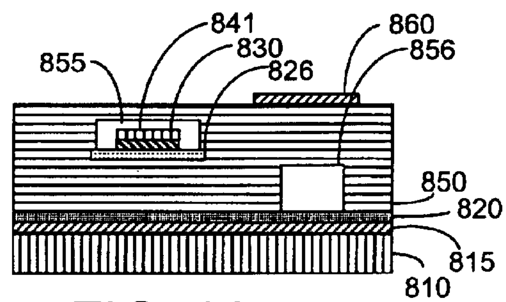


FIG. 23M

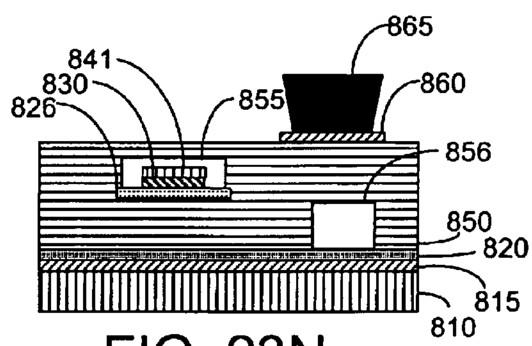


FIG. 23N

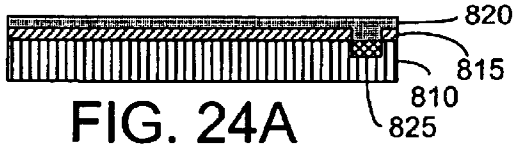


FIG. 24A
SECTION B-B

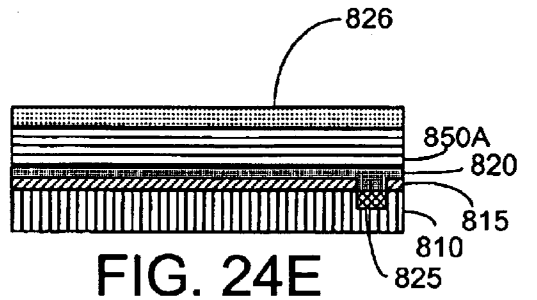


FIG. 24E
SECTION B-B

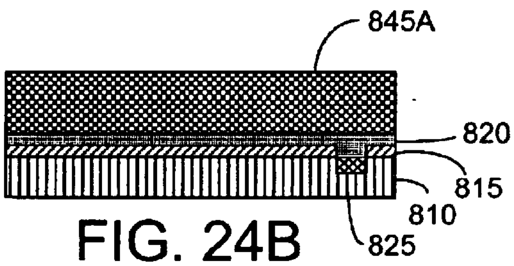


FIG. 24B
SECTION B-B

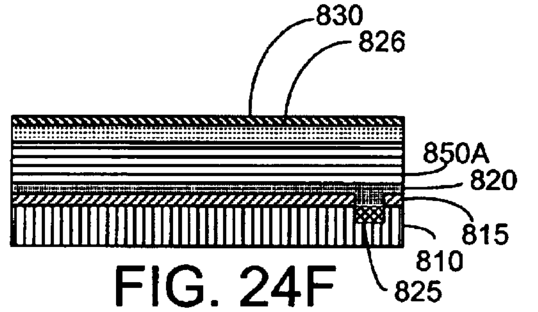


FIG. 24F
SECTION B-B

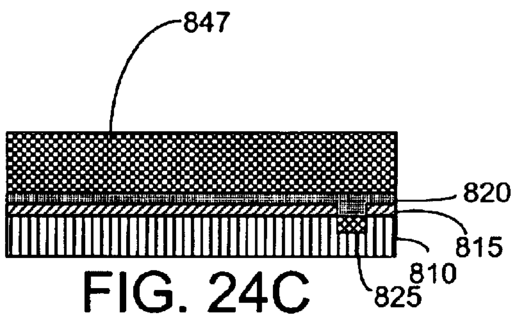


FIG. 24C
SECTION B-B

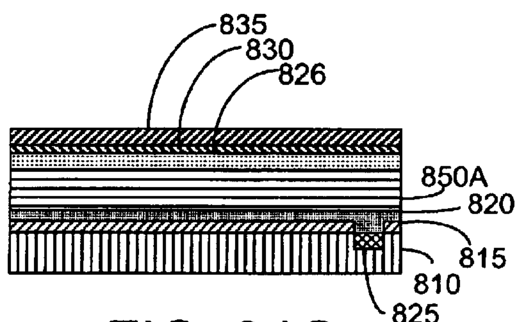


FIG. 24G
SECTION B-B

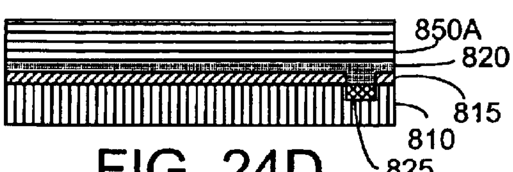


FIG. 24D
SECTION B-B

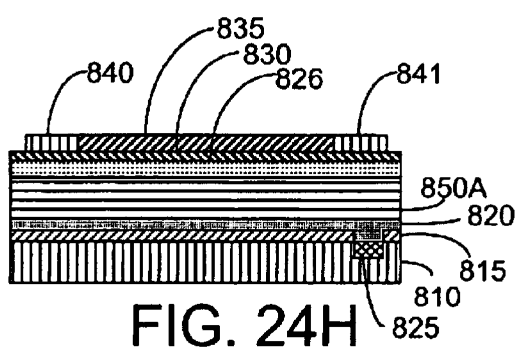


FIG. 24H
SECTION B-B

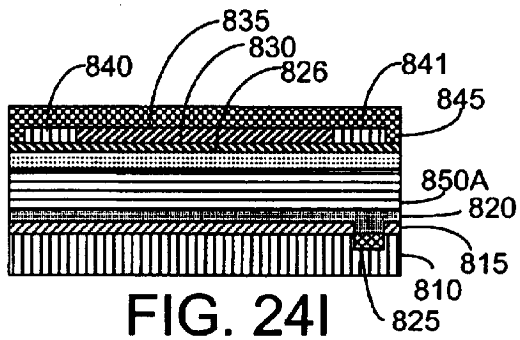


FIG. 24I
SECTION B-B

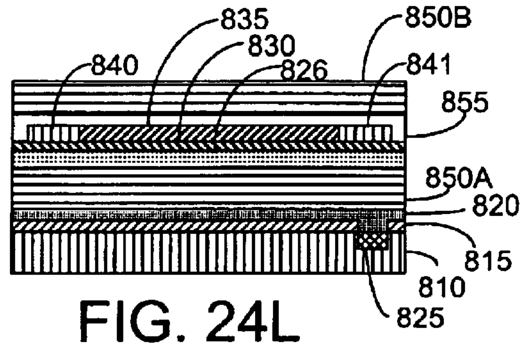


FIG. 24L
SECTION B-B

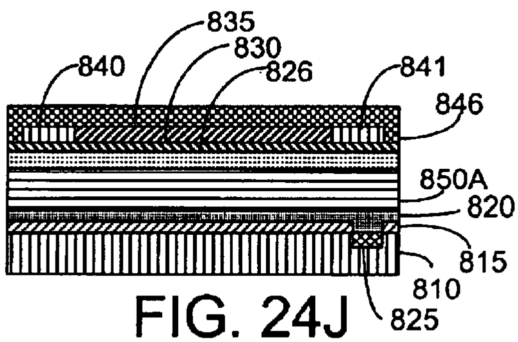


FIG. 24J
SECTION B-B

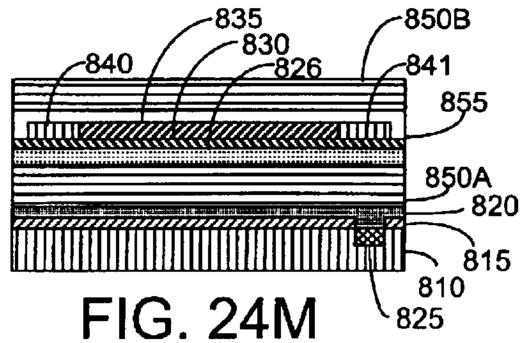


FIG. 24M
SECTION B-B

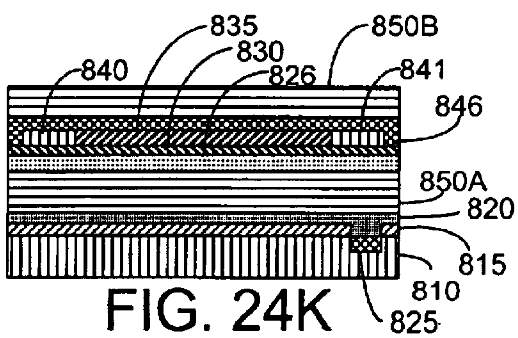


FIG. 24K
SECTION B-B

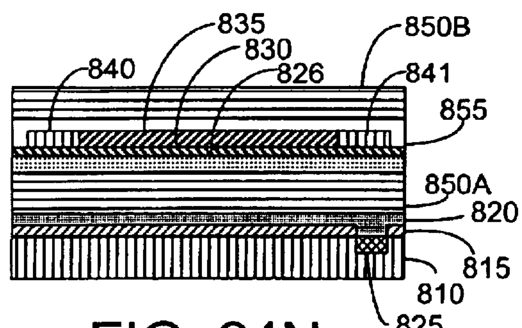


FIG. 24N
SECTION B-B

GUIDED-WAVE OPTICAL INTERCONNECTIONS EMBEDDED WITHIN A MICROELECTRONIC WAFER-LEVEL BATCH PACKAGE

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to co-pending U.S. provisional application entitled, "Guided-wave Optical Interconnection Using Volume Grating Coupler and Air Gap Technologies Embedded Within A Microelectronic Package," having ser. No. 60/268,142, filed Feb. 11, 2001, which is entirely incorporated herein by reference.

This application is related to co-pending U.S. utility patent application entitled "Waveguides," filed on Feb. 11, 2002, which is entirely incorporated herein by reference.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

The U.S. government has a paid-up license in this invention and the right in limited circumstances to require the patent owner to license others on reasonable terms as provided for by the terms of MDA972-99-1-0002 awarded by the DARPA of the U.S. Government.

TECHNICAL FIELD

The present invention is generally related to guided-wave interconnections and, more particularly, is related to guided-wave interconnections within a microelectronic package.

BACKGROUND OF THE INVENTION

High performance microprocessors with heat sink capabilities will likely be required to dissipate hundreds of watts from sub-volt power supplies in near and long-term microelectronic technology generations. A need exists for low cost and high pin count microelectronic package technology that can satisfy power supply and heat removal requirements within such chips.

The mechanical performance of a microelectronic package is important for wafer-level testing, protection, and reliability. Wafer-level testing requires simultaneous reliable contact to all die across a non-planar wafer surface. In-plane (i. e., x-y axis) compliance is generally required to account for thermal expansion between the chip and printed wiring board (or other attachment substrate). Wafer-level testing and burn-in demands significant out-of-plane (i.e., z-axis) compliance in order to establish reliable electrical contact between wafer-level pads and test-card or printed wiring board probes due to the non-planarity of each surface.

Unlike conventional packaging, wafer-level packaging (WLP) is a continuation of integrated circuit manufacturing. In WLP, additional masking steps can be used after fabricating die pads to simultaneously package all die across a wafer. A unique class of WLP is called "compliant wafer-level packaging" (CWLP). In CWLP, additional masking steps can be used after fabricating die pads to batch fabricate compliant x-y-z axis I/O leads between the die pads and the board pads. The use of compliant leads allows for the elimination of underfill between chip and substrate, and hence improves manufacturability and cost. A mechanically x-y-z flexible lead is formed between the die pad and the bump interconnection that would be joined with the board. Accordingly, there is a need in the industry for x-y-z compliant leads that provide high density, high electrical performance, low cost, and ability of batch fabrication.

Thus, a heretofore unaddressed need exists in the microelectronics industry to address the aforementioned deficiencies and/or inadequacies.

SUMMARY OF THE INVENTION

Briefly described, the present invention provides for chip-level electronic packages. A representative chip-level electronic package includes at least one waveguide having a waveguide core. In addition, another representative wafer-level electronic package includes a waveguide having an air-gap cladding layer around a portion of the waveguide core.

The present invention also involves a method of fabricating chip-level electronic packages. A representative method includes the following steps: providing a substrate having a passivation layer disposed on the substrate; disposing a waveguide core on a portion of the passivation layer; disposing a first sacrificial layer onto at least one portion of the passivation layer and the waveguide core; disposing an overcoat layer onto the passivation layer and the first sacrificial layer; and removing the first sacrificial layer to define an air-gap cladding layer within the overcoat polymer layer and around a portion of the waveguide core.

Other systems, methods, features, and advantages of the present invention will be or become apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional systems, methods, features, and advantages be included within this description, be within the scope of the present invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Many aspects of the invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present invention. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

FIGS. **1A–1C** are schematics that illustrate three cross-sectional views of microelectronic package **100**. FIGS. **1B** and **1C** are cross-sectional views of FIG. **1A** in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **1A**.

FIGS. **2A–2J** are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **1A**, while FIGS. **3A–3J** are cross-sectional views of the fabrication process relative to the view in FIG. **1C**, section B—B of FIG. **1A**.

FIGS. **4A–4C** are schematics that illustrate three cross-sectional views of microelectronic package **200**. FIGS. **4B** and **4C** are cross-sectional views of FIG. **4A** in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **4A**.

FIGS. **5A–5J** are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **4A**, while FIGS. **6A–6J** are cross-sectional views of the fabrication process relative to the view in FIG. **4C**, section B—B of FIG. **4A**.

FIGS. **7A–7C** are schematics that illustrate three cross-sectional views of microelectronic package **300**. FIGS. **7B** and **7C** are cross-sectional views of FIG. **7A** in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **7A**.

FIGS. **8**A–**8**J are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **7**A, while FIGS. **9**A–**9**J are cross-sectional views of the fabrication process relative to the view in FIG. **7**C, section B—B of FIG. **7**A.

FIGS. **10**A–**10**C are schematics that illustrate three cross-sectional views of microelectronic package **400**. FIGS. **10**B and **10**C are cross-sectional views of FIG. **10**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **10**A.

FIGS. **11**A–**11**J are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **10**A, while FIGS. **12**A–**12**J are cross-sectional views of the fabrication process relative to the view in FIG. **10**C, section B—B of FIG. **10**A.

FIGS. **13**A–**13**C are schematics that illustrate three cross-sectional views of microelectronic package **500**. FIGS. **13**B and **13**C are cross-sectional views of FIG. **13**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **13**A.

FIGS. **14**A–**14**L are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **13**A, while FIGS. **15**A–**15**L are cross-sectional views of the fabrication process relative to the view in FIG. **13**C, section B—B of FIG. **13**A.

FIGS. **16**A–**16**C are schematics that illustrate three cross-sectional views of microelectronic package **600**. FIGS. **16**B and **16**C are cross-sectional views of FIG. **16**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **16**A.

FIGS. **17**A–**17**N are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **16**A, while FIGS. **18**A–**18**N are cross-sectional views of the fabrication process relative to the view in FIG. **16**C, section B—B of FIG. **16**A.

FIGS. **19**A–**19**C are schematics that illustrate three cross-sectional views of microelectronic package **700**. FIGS. **19**B and **19**C are cross-sectional views of FIG. **19**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **19**A.

FIGS. **20**A–**20**L are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **19**A, while FIGS. **21**A–**21**L are cross-sectional views of the fabrication process relative to the view in FIG. **19**C, section B—B of FIG. **19**A.

FIGS. **22**A–**22**C are schematics that illustrate three cross-sectional views of microelectronic package **800**. FIGS. **22**B and **22**C are cross-sectional views of FIG. **22**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **22**A.

FIGS. **23**A–**23**N are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **22**A, while FIGS. **24**A–**24**N are cross-sectional views of the fabrication process relative to the view in FIG. **22**C, section B—B of FIG. **22**A.

DETAILED DESCRIPTION

In general, microelectronic packages (e.g., wafer-level or chip-level packages) of the present invention include embedded waveguides (e.g., optical dielectric or photonic crystal waveguides). Microelectronic packages with embedded waveguides allow for time-of-flight (ToF) propagation delay along global data interconnects and gate-delay limited frequencies of modulation along global clock interconnects. Microelectronic packages having waveguide interconnects allow for compact packaging of a hybrid electrical/optical system in a manner conducive to power supply and heat removal requirements of future technology generations.

In addition, the microelectronic packages of the present invention can include waveguides having either a dielectric or air-gap cladding engaging (e.g., surrounding the waveguide core of the waveguide) a portion of the waveguide core. The presence of an air-gap cladding allows for a maximization in refractive index contrast between waveguide core and cladding regions, which in turn permits tighter bends and increased waveguide density through enhanced confinement of optical power within the waveguide core region.

Further, the microelectronic packages of the present invention can include a waveguide having a coupling element disposed within and/or adjacent to the waveguide core in order to couple optical power both into and out of waveguide regions. The coupling element can be in the form of a grating coupler, total internal reflection mirror, or be represented simply by bringing the waveguide region to within close proximity of the detector region without the express definition of a specific coupling structure (i.e., evanescent coupling).

Also, hybrid-attached optoelectronic devices such as emitters or detectors could be situated within or adjacent to the package such that butt-coupling of optical power into and out of the waveguide core region(s) is allowed, thus negating the specific need for a coupling structure to be incorporated.

Furthermore, the microelectronic package can include embedded air-gap regions to a) enhance z-compliance of compliant leads when disposed substantially under a portion of each lead, b) permit the integration of micro-fluidic channels for thermal cooling, and c) provide electrical isolation between neighboring electrical interconnections.

Microelectronic packages can find application within high-performance or cost-performance microprocessors, Application Specific Integrated Circuits (ASICs), System-on-a-Chip (SoC) architectures that incorporate multiple technologies (such as RF, optical and MEMs structures), optoelectronic chips for telecommunications, or any other microelectronic device that requires or can benefit from a low-cost wafer-level batch package incorporating optical interconnect technology.

Now having described microelectronic packages in general, examples 1–8 will describe some embodiments of the microelectronic package. While embodiments of the microelectronic package are described in connection with examples 1–8 and the corresponding text and figures, there is no intent to limit embodiments of the microelectronic package to these descriptions. On the contrary, the intent is to cover all alternatives, modifications, and equivalents included within the spirit and scope of embodiments of the present invention.

EXAMPLE 1

FIGS. **1**A–**1**C are schematics that illustrate three cross-sectional views of microelectronic package **100** having a waveguide **105**. FIGS. **1**B and **1**C are cross-sectional views of FIG. **1**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **1**A.

Microelectronic package **100** includes a waveguide **105**, a substrate **110**, a multi-level interconnect layer **115**, a passivation layer **120**, a detector **125**, an overcoat layer **150**, a die pad **158**, a lead **160**, and a contact **165**. The multi-level interconnect layer **115** is disposed on the substrate **110**, while the passivation layer **120** is disposed on the multi-level interconnect layer **115**. In this embodiment the waveguide **105** is disposed on the passivation layer **120**, where the passivation layer **120** acts as the lower cladding of the waveguide **105**. In addition, the die pad **158** is disposed on the multi interconnect layer **115**. The overcoat layer **150** is disposed over the waveguide **105** and the passivation layer **120**. The lead **160** is disposed on the die pad **158** and a portion of the overcoat layer **150**. Additional details regarding the spatial relationship of the components of microelectronic package **100** depicted in FIGS. **1A–1C** are discussed in FIGS. **2A–2J** and **3A–3J**, which illustrate an exemplary fabrication process of microelectronic package **100**.

The substrate **110** can be any of a variety of substrates that can be used to support microelectronic package **100**. The substrate **110** can include materials such as, for example, silicon, silicon compounds, germanium, germanium compounds, gallium, gallium compounds, indium, indium compounds, or other semiconductor materials/compounds. In addition, the substrate **110** can include non-semiconductor substrate materials such as ceramics and organic boards.

The multi-level interconnect layer **115** can be any of a variety of materials and these include copper, low-k dielectric materials, aluminum, and/or polysilicon, for example. The multi-level interconnect layer **115** functions to connect individual or groups of transistors located within different sections of the die.

The passivation layer **120** can be any of a variety of materials that, when serving as the lower cladding region, have a lower index of refraction than the waveguide core **130**. The passivation layer **120** includes materials such as silicon dioxide and silicon nitride. The passivation layer serves to protect the underlying metallization and CMOS circuitry from corrosion or corruption by external elements.

The die pads **158** can be deposited upon the surface of the substrate **110**, the multi-level interconnect layer **115**, or the passivation layer **120** using techniques such as, for example, sputtering, evaporation, electron-beam systems, electroplating, electro-less plating, and displacement reactions.

The lead **160** can be fabricated of any single layer or layers of different metals, metal composites, dielectrics, superconductors, organic conductors, or light emitting organic materials, for example, appropriate for microelectronic package **100**. The metals and metal composites include gold, gold alloys, copper, and copper alloys. The lead **160** can be fabricated by monolithically electroplating the selected metal or metal composite onto the compliant wafer device.

The lead **160** can range from about 1 to about 100 micrometers in thickness and preferably from about 4 to about 40 micrometers. The preferred embodiment has a thickness of about 15 micrometers. The lead **160** length can range from about 2 and about 400 micrometers, preferably from about 40 to about 120 micrometers. The lead **20** width can range from about 1 to about 100 micrometers, preferably from about 2 to about 40 micrometers. The preferred embodiment has a width in the range of about 15 to about 25 micrometers.

The lead **160** can be compliant in-plane and out-of-plane. The shape of the lead along with the overcoat layer **150** provides compliance in-plane. The lead **160** is compliant in-plane in the range of about 1 to about 100 micrometers, preferably from about 1 to about 50 micrometers.

Optionally, the contact **165** can be disposed on the lead **160**, which can include a variety of contacts designed to make contact or attach to a pad or point on another device such as a microelectronic device, for example. The contact **165** can be, for example, a solder bump (as shown in FIG. **1A–1C**), a conductive adhesive or filled polymer, or a contact probe. The contact **165** can be formed with methods such as electroplating, electroless plating, screen or stencil printing.

The waveguide **105** can be defined through multiple fabrication processes such as, but not limited to, photo-definition, wet chemical etching, thermally-induced refractive index gradients, and ion implantation. In addition, the waveguide **105** can have geometries such as, for example, raised strip geometry, buried geometry, and rib geometry.

The waveguide **105** can include a waveguide core **130** having coupling elements **140** and **141** disposed at each end of the waveguide core **130**. Typically, one of the coupling elements **141** is disposed above the detector **125**. In this manner, optical energy (e.g., light) can enter one coupling element **140**, travel down the waveguide core **130**, and exit another coupling element **141** to be detected by the detector **125**. The detector **125** can include any device capable of providing optical-to-electrical conversion of optical energy incident from the waveguide **105** onto the detector region. In addition, the detector can be monolithically incorporated within the semiconductor die, or hybridly incorporated within or adjacent to the package itself.

The waveguide core **130** functions as a medium for optical energy to travel through. Therefore, waveguide **105** can communicate optical energy through the microelectronic package **100**. The waveguide core **130** can be fabricated from materials such as, for example, polynorbornenes, polyimides, epoxies, or other polymer materials, low-k dielectric materials such as silicon dioxide, silicon nitride, or porous low-k dielectrics, or semiconductor or other crystalline materials. In general, any material that exhibits a) transparency to a particular optical wavelength of light, b) process compatibility with other materials such that a contrast in refractive index is achieved, c) process compatibility with standard microelectronic fabrication processes, d) suitable mechanical strength, flexibility, and durability, and e) sufficient lifetime and/or reliability characteristics can serve as a waveguide material. A reference describing polymer materials suitable for optical waveguide applications can be found in A. R. Blythe and J. R. Vinson, Proc. 5th *International Symposium on Polymers for Advanced Technologies*. Tokyo, Japan: pp. 601–11, August–December 2000, which is incorporated herein by reference.

The coupling elements **140** and **141** can include planar (or volume) grating couplers (as shown in FIGS. **1A–1C**, **2A–2J**, and **3A–3J**), evanescent couplers, surface-relief grating couplers, and total internal reflection couplers. More specifically, when the couplers **140** and **141** are volume grating couplers, the volume grating coupler material can be laminated or spin-coated onto the appropriate surface. In particular, laminated volume grating couplers can be formed by holographic exposure of the grating region following lamination of the grating material. Alternatively, the laminated volume grating couplers can be formed by holographic exposure prior to lamination of the grating material. Additional details regarding grating couplers can be found in U.S. Pat. No. 6,285,813, which is herein incorporated by reference.

The grating coupler material includes materials such as, for example, polymer materials, silver halide photographic emulsions, photoresists such as dichromated gelatin, photopolymers such as polymethyl methacrylate (PMMA) or

Dupont HRF photopolymer films, thermoplastic materials, photochromic materials such as crystals, glasses or organic substrates, photodichroic materials, and photorefractive crystals such as lithium niobate, for example. These materials have the characteristics of creating a refractive index modulation through a variety of mechanisms, all of which result in the creation of a phase or absorption or mixed grating. Other suitable materials are described in T. K. Gaylord and M. G. Moharam, *Proc. IEEE,* vol. 73, pp. 894–937, May 1985, which is herein incorporated by reference.

As depicted in FIGS. **1**A–**1**C, the waveguide **105** includes an air-gap cladding layer **155** surrounding a portion of the waveguide core **130** and coupling elements **140** and **141**. The air-gap cladding layer **155** has a lower index of refraction (e.g., index of refraction of **1**) than the waveguide core **130**. However, other types of cladding layers (e.g., dielectric cladding) can be used to surround the waveguide core **130** and coupling elements **140**, so long as the refractive index of the dielectric cladding material is lower than that of the core material.

The air-gap cladding layer **155** can be formed by the removal (e.g., decomposition) of a sacrificial layer (as shown in FIGS. **2**A–**2**J and **3**A–**3**J and depicted as sacrificial layer **145**) from the area in which the air-gap cladding layer **155** is to be located, as illustrated in FIGS. **1**A–**1**C. The air-gap cladding layer **155** occupies a space bounded by the passivation layer **120**, the waveguide core **130**, the coupling elements **140** and **141**, and the overcoat layer **150**.

Generally, during the fabrication process of the microelectronic package **100**, a a sacrificial layer (illustrated in FIGS. **2**A–**2**J and **3**A–EJ) is deposited onto the passivation layer **120**, the waveguide core **130**, and the coupling elements **140** and **141** and patterned. Thereafter, the overcoat layer **150** is deposited around the sacrificial layer and on the passivation layer **120**. Subsequently, the sacrificial layer is removed forming the air-gap cladding layer **155**. The processes for depositing and removing the sacrificial layer are discussed in more detail hereinafter.

The sacrificial layer can be a polymer that slowly decomposes at a known temperature without leaving undesirable residue. The polymer should have a rate of decomposition so as to not create too great of a pressure while forming the air-gap cladding layer **155**. In addition, the decomposition of the sacrificial layer produces gas molecules small enough to permeate the overcoat layer **150**. Further, the sacrificial layer has a decomposition temperature less than the decomposition or degradation temperature of the overcoat layer **150**.

Examples of compounds that can be used to form the the sacrificial layer include polynorbornenes, polyformaldehyde, polycarbonates, polyethers, and polyesters. More specifically, the compounds of the preferred embodiments are Promerus L. L. C. Unity™ 400, polypropylene carbonate, polyethylene carbonate, polynorborene carbonate, or combinations thereof. The sacrificial layer may also be constructed of photosensitive compounds, which are additives for patterning or decomposition.

The sacrificial layer can be deposited using any suitable technique, for example, but not limited to, spin coating, doctor-blading, spray-coating, sputtering, lamination, screen or stencil-printing, melt dispensing, chemical vapor deposition (CVD), and plasma based deposition systems.

The height of the air-gap cladding layer **155** can range from about 0.5 to about 300 micrometers, preferably in the range of about 1 to about 15 micrometers. The radius of the air-gap cladding layer **155** can range from about 1 to about 300 micrometers, and more particularly can range from about 50 to about 250 micrometers. In general, the height of the air-gap cladding layer **155** is controlled by both the weight fraction of the sacrificial polymer in solution as well as the deposition technique.

The sacrificial layer can be removed by thermal decomposition, ultra violet irradiation, for example, or patterned directly during application, (i.e. screen-printing or selective etching). The thermal decomposition of the sacrificial layer can be performed by heating electronic package **100** to the decomposition temperature of the sacrificial layer and holding at that temperature for a certain time period (e.g., 1–4 hours). Thereafter, the decomposition products diffuse through the overcoat layer **150** leaving a virtually residue-free hollow structure (air-gap cladding layer **155**).

Although only one waveguide **105** is depicted in FIGS. **1**A–**1**C, one or more waveguides **105** can be included in microelectronic package **100**. In addition, one or more waveguide cores/couplers can be included in the air-gap cladding layer **155**. Although only one layer of optical waveguides **105** is depicted, multiple layers can also be incorporated.

In the case where buried air-gap cladding layers **155** are incorporated, the overcoat layer **150** can be any modular polymer that includes the characteristic of being permeable or semi-permeable to the decomposition gases produced by the decomposition of the sacrificial layer while forming the air-gap cladding layer **155**. In addition, the overcoat layer **150** has elastic properties so as to not rupture or collapse under fabrication and use conditions. Further, the overcoat layer **150** is stable in the temperature range in which the sacrificial layer decomposes. Furthermore, the overcoat layer **150** enables the lead **160** to be compliant in-plane (i.e., the x-y axis direction) when the lead **160** is adhered to the polymer surface.

Examples of the overcoat layer **150** include compounds such as, for example, silicon dioxide, silicon nitride, polyimides, polynorbornenes, epoxides, polyarylenes ethers, and parylenes. More specifically, the overcoat layer **150** of the preferred embodiment is Amoco Ultradel™ 7501, BF Goodrich Avatrel™ Dielectric Polymer, DuPont™ 2611, DuPont™ 2734, DuPont™ 2771, DuPont™ 2555, or combinations thereof.

The overcoat layer **150** can be deposited using any suitable technique, for example, spin coating, doctor-blading, sputtering, lamination, screen or stencil-printing, chemical vapor deposition (CVD), or through the use of plasma based deposition systems.

For the purposes of illustration only, microelectronic package **100** of the present invention is described with particular reference to the below-described fabrication method. For clarity, some portions of the fabrication process are not included in FIGS. **2**A–**2**J and **3**A–**3**J. For example, photolithography or similar techniques can be used to define the overcoat layer **150**, the sacrificial layer, waveguide **105**, and/or lead **160** pattern. In this regard, the pattern can be defined by depositing material onto the surface of the substrate **110**, multi-level interconnect **115**, and/or the passivation layer **120** using techniques such as, for example, sputtering, chemical vapor deposition (CVD), plasma based deposition systems, evaporation, and electron-beam systems. Furthermore, the pattern can then be removed using reactive ion etching techniques (RIE), for example.

The following fabrication process is not intended to be an exhaustive list that includes every step required for fabricating microelectronic package **100**. In addition, the fabrication process is flexible because the process steps may be performed in a different order than the order illustrated in FIGS. **2A–2J** and **3A–3J**.

FIGS. **2A–2J** are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **1A**, while FIGS. **3A–3J** are cross-sectional views of the fabrication process relative to the view in FIG. **1C**, section B—B of FIG. **1A**. Therefore, FIGS. **2A–2J** and **3A–3J** illustrate corresponding views in the fabrication process from different cross-sectional views. The varying views of the fabrication process shown in FIGS. **2A–2J** and **3A–3J** have been provided to illustrate aspects of the fabrication process that are not necessarily observable using only FIGS. **2A–2J** or FIGS. **3A–3J**. In this regard, FIGS. **2A** and **3A**, **2B** and **3B**, **2C** and **3C**, and so on, are discussed in tandem to illustrate various aspects of the representative fabrication process.

FIGS. **2A** and **3A** illustrate the multi-level interconnect layer **115** disposed on the substrate **110**, while the passivation layer **120** is disposed on the multi-level interconnect layer **115**. In addition, the detector **125** is embedded in the substrate layer **110**.

FIGS. **2B** and **3B** illustrate the waveguide core **130** disposed on a portion of the passivation layer **120** after having been etched and photodefined. In this embodiment, the passivation layer **120** acts as the lower cladding of the waveguide **105**.

FIGS. **2C** and **3C** illustrate a portion of the waveguide core **130** that has been removed and replaced with the grating material **135**. FIGS. **2D** and **3D** illustrate the defining of the grating material **135** into grating couplers **140** and **141**. In an alternate embodiment, the waveguide core **130** and grating material **135** are the same material, in which case no material is removed, and the grating couplers **140** and **141** are defined only within the labeled areas.

FIGS. **2E** and **3E** illustrate the sacrificial layer **145** disposed over the passivation layer **120**, waveguide core **130**, and the grating couplers **140** and **141**.

FIGS. **2F** and **3F** illustrate the formation of sacrificial layer section **146** by etching or UV exposure/thermal decomposition, for example, of the sacrificial layer **145**. The sacrificial layer section **146** defines the area where the air-gap cladding layer **155** will subsequently be located once the sacrificial layer section **146** is removed.

FIGS. **2G** and **3G** illustrate the overcoat layer **150** disposed on the passivation layer **120** and the sacrificial layer section **146**.

FIGS. **2H** and **3H** illustrate the removal of the sacrificial layer section **146** to form the air-gap cladding layer **155** of the waveguide **105**. In this embodiment, the waveguide **105** includes the passivation layer **120** (lower cladding), the waveguide core **130**, the couplers **140** and **141**, and the air-gap cladding layer **155** (upper and side cladding).

FIGS. **2I** and **3I** illustrate the lead **160** disposed upon the die pad **158** (not shown) after a via (not shown) is etched in the overcoat layer **150** in the area substantially over the die pad **158**. It should be noted that the formation of the die pad **158** was omitted from earlier process steps for clarity. Alternatively, the sacrificial layer section **146** could be removed at this point in the fabrication rather than in the previous step.

FIGS. **2J** and **3J** illustrate the contact **165** disposed on the lead **160**, thereby forming microelectronic package **100**, as depicted in FIGS. **1A–1C**. It should be noted that formation of the contact **165** is optional.

EXAMPLE 2

FIGS. **4A–4C** are schematics that illustrate three cross-sectional views of microelectronic package **200** having a waveguide **205** and an air-gap layer **256**. FIGS. **4B** and **4C** are cross-sectional views of FIG. **4A** in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **4A**.

Microelectronic package **200** includes the waveguide **205**, a substrate **210**, a multi-level interconnect layer **215**, a passivation layer **220**, a detector **225**, the air-gap layer **256**, a overcoat layer **250**, a die pad **258**, a lead **260**, and a contact **265**. The multi-level interconnect layer **215** is disposed on the substrate **210**, while the passivation layer **220** is disposed on the multi-level interconnect layer **215**. In this embodiment the waveguide **205** is disposed on the passivation layer **220**, where the passivation layer **220** acts as the lower cladding of the waveguide **205**. In addition, the die pad **258** is disposed on the multi-level interconnect layer **215**. Further, the air-gap layer **256** is disposed on the passivation layer **220**. The overcoat layer **250** is disposed over the waveguide **205**, the passivation layer **220** and the air-gap layer **256**. The lead **260** is disposed on the die pad **258** and a portion of the overcoat layer **250**. A portion of the lead **260** is disposed above the air-gap layer **256**. Additional details regarding the spatial relationship of the components of microelectronic package **200** depicted in FIGS. **4A–4C** are discussed in FIGS. **5A–5J** and **6A–6J**.

The waveguide **205**, the substrate **210**, the multi-interconnect layer **215**, the passivation layer **220**, the overcoat layer **250**, the air-gap cladding layer **255**, the die pad **258**, the lead **260**, and the contact **265**, discussed in relation to FIGS. **4A–4C**, are analogous or similar to the waveguide **105**, the substrate **110**, the multi-interconnect layer **115**, the passivation layer **120**, the overcoat layer **150**, the air-gap cladding layer **155**, the die pad **158**, the lead **160**, and the contact **165**, discussed in reference to FIGS. **1A–1C**, **2A–2J**, and **3A–3J** above. Therefore, additional discussion of these components will not be presented in relation to microelectronic package **200**. The reader is directed to the discussion above for further explanation of these components.

In contrast to microelectronic package **100**, microelectronic package **200** includes the air-gap layer **256**, which can be formed by the removal (e.g., decomposition) of a sacrificial layer (as shown in FIGS. **5A–5J** and **6A–6J** and depicted as sacrificial layer **240**) from the area in which the air-gap layer **256** is subsequently located, as illustrated in FIGS. **4A–4C**. The air-gap layer **256** occupies a space bounded by the passivation layer **220** and the overcoat layer **150**. The, waveguide **205** can communicate optical energy through the microelectronic package **200**.

Generally, during the fabrication process of microelectronic package **200**, a sacrificial layer is deposited onto the passivation layer **220** and patterned i. e., forming both the first sacrificial layer section, which corresponds to the air-gap cladding layer **255**, and the second sacrificial layer section, which corresponds to the air-gap layer **256**. Thereafter, the overcoat layer **250** is disposed around the first sacrificial layer section, the second sacrificial layer section, and on the passivation layer **220**. Subsequently, the second sacrificial layer section is removed (e.g., decomposed) forming the air-gap layer **256**. The air-gap layer **256** enables the lead **260** to be compliant out-of-plane (z axis). The processes for depositing and removing the second sacrificial layer are discussed in more detail hereinafter.

Like the sacrificial layer discussed in reference to FIG. **1A–1C**, the second sacrificial layer can be virtually any polymer that slowly decomposes so as to not create too great of a pressure while forming the air-gap layer **256**. In addition, the decomposition of the second sacrificial layer produces gas molecules small enough to permeate the overcoat layer **250**. Further, the second sacrificial layer has a decomposition temperature less than the decomposition or degradation temperature of the overcoat layer **250**.

Examples of the second sacrificial layer include compounds such as polynorbornenes, polyformaldehyde, polycarbonates, polyethers, and polyesters. More specifically, the sacrificial polymer of the preferred embodiment is Promerus L. L. C. Unity™ 400, polypropylene carbonate, polyethylene carbonate, polynorborene carbonate, or combinations thereof. The second sacrificial layer may also contain photosensitive compounds, which are additives for patterning or decomposition.

The second sacrificial layer can be deposited onto the substrate **210** using techniques such as, for example, spray coating, spin coating, doctor-blading, sputtering, lamination, screen or stencil-printing, melt dispensing, chemical vapor deposition (CVD), and plasma based deposition systems.

The height of the air-gap layer **256** can range from about 0.5 to about 300 micrometers, preferably in the range of about 5 to about 50 micrometers. The radius of the air-gap layer **256** can range from about 1 to about 300 micrometers, and more particularly can range from about 50 to about 250 micrometers. In general, the thickness of the air-gap layer **256** (i.e., ultimately the height of the air-gap layer **256**) is controlled by both the weight fraction of the sacrificial polymer in solution as well as the deposition technique.

The second sacrificial layer can be removed by thermal decomposition, ultraviolet irradiation, etc., or patterned directly during application, i.e., by screen-printing. The thermal decomposition of the second sacrificial layer can be performed by heating electronic package **200** to the decomposition temperature of the second sacrificial layer and holding at that temperature for a certain time period (e.g., 1–2 hours). Thereafter, the decomposition products diffuse through the overcoat layer **250** leaving a virtually residue-free hollow structure (air-gap).

The air-gap layer **256** can provide compliance out-of-plane for the lead **260** in the range of about 1 to about 100 micrometers, preferably from about 1 to about 50 micrometers.

Typically, the first sacrificial layer and second sacrificial layer are formed of the same material. However, the first and second sacrificial layers can be formed of different materials, which may require additional fabrication steps.

For the purposes of illustration only, microelectronic package **200** of the present invention is described with particular reference to the below-described fabrication method. For clarity, some portions of the fabrication process are not included in FIGS. **5A–5J** and **6A–6J**. For example, photolithography or similar techniques can be used to define the overcoat layer **250**, the sacrificial layer, the waveguide **205**, and/or the lead **260** pattern. In this regard, the pattern can be defined by depositing material onto the surface of the substrate **210**, multi-level interconnect **215**, and/or the passivation layer **220** using techniques such as, for example, sputtering, chemical vapor deposition (CVD), plasma based deposition systems, evaporation, electron-beam systems. Furthermore, the pattern can then be removed using reactive ion etching techniques (RIE), for example.

The following fabrication processes are not intended to be an exhaustive list that includes every step required for fabricating microelectronic package **200**. In addition, the fabrication process is flexible because the process steps can be performed in a different order than the order illustrated in FIGS. **5A–5J** and **6A–6J**.

FIGS. **5A–5J** are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **4A**, while FIGS. **6A–6J** are cross-sectional views of the fabrication process relative to the view in FIG. **4C**, section B—B of FIG. **4A**. Therefore, FIGS. **5A–5J** and **6A–6J** illustrate corresponding views in the fabrication process from different cross-sectional views. The varying views of the fabrication process shown in FIGS. **5A–5J** and **6A–6J** have been provided to illustrate aspects of the fabrication process that are not necessarily observable using only FIGS. **5A–5J** or FIGS. **6A–6J**. In this regard, FIGS. **5A** and **6A**, **5B** and **6B**, **5C** and **6C**, and so on, are discussed in tandem to illustrate various aspects of the fabrication process.

FIGS. **5A** and **6A** illustrate the multi-level interconnect layer **215** disposed on the substrate **210**, while the passivation layer **220** disposed on the multi-level interconnect layer **215**. In addition, the detector **225** is embedded in the substrate layer **215**.

FIGS. **5B** and **6B** illustrate the waveguide core **230** disposed on a portion of the passivation layer **220** after having been etched or photodefined, for example. In this embodiment the passivation layer **220** is the lower cladding of the waveguide **205**.

FIGS. **5C** and **6C** illustrate a portion of the waveguide core **230** that has been removed and replaced with grating material **235**.

FIG. **5D** and **6D** illustrate the defining and forming of the grating material **235** into grating couplers **240** and **241**. In an alternate embodiment, the waveguide core and grating material are the same layer, in which case no material is removed, and the grating couplers are defined only within the labeled areas.

FIGS. **5E** and **6E** illustrate the sacrificial layer **245** deposited over the passivation layer **220**, the waveguide core **230**, and the grating couplers **240** and **241**.

FIGS. **5F** and **6F** illustrate the formation of first sacrificial layer section **246**, which defines the area where the air-gap cladding layer **255** will subsequently be located once the sacrificial layer **246** is removed. In addition, FIGS. **5F** and **6F** illustrate the formation of the second sacrificial layer section **247**, which defines the area where the air-gap layer **256** will subsequently be located once the second sacrificial layer section **247** is removed. It should be noted that the first and second sacrificial layer sections **246** and **247** do not have to be made from the same sacrificial layer. In this regard, appropriate fabrication steps could be included to form the sacrificial layer sections from different sacrificial materials.

FIGS. **5G** and **6G** illustrate the formation of the overcoat layer **250** on the passivation layer **220**, the first sacrificial layer section **246**, and second sacrificial layer section **247**.

FIGS. **5H** and **6H** illustrate the removal of the first sacrificial layer section **246** to form the air-gap cladding layer **255** of the waveguide **205**. In this embodiment, the waveguide **205** includes the passivation layer **220** (lower cladding), waveguide core **230**, couplers **240** and **241**, and air-gap cladding layer **255** (upper and side cladding). In addition, the second sacrificial layer section **247** is removed to form air-gap layer **256**.

FIGS. **5I** and **6I** illustrate the formation of the lead **260** upon the die pad **258** (not shown) after a via (not shown) is etched in the overcoat layer **250** in the area over the die pad **258**. It should be noted that the formation of the die pad **258** was omitted from earlier process steps for clarity. Alternatively, the first sacrificial layer section **246** and the second sacrificial layer section **247** could be removed at this point in the fabrication rather than in a previous step.

FIGS. **5**J and **6**J illustrate the formation of a contact **265** on the lead **260**, thereby forming microelectronic package **200** as depicted in FIGS. **4**A–**4**C. It should be noted that formation of the contact **265** is optional.

EXAMPLE 3

FIGS. **7**A–**7**C are schematics that illustrate three cross-sectional views of microelectronic package **300** having a waveguide **305** with surface-mounted couplers **340** and **341**. FIGS. **7**B and **7**C are cross-sectional views of FIG. **7**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **7**A.

Microelectronic package **300** includes the waveguide **305**, a substrate **310**, a multi-level interconnect layer **315**, a passivation layer **320**, a detector **325**, an overcoat layer **350**, a die pad **358**, a lead **360**, and a contact **365**. The multi-level interconnect layer **315** is disposed on the substrate **310**. The passivation layer **320** is disposed on the multi-level interconnect layer **315**. In this embodiment the waveguide **305** is disposed on the passivation layer **320**, where the passivation layer **320** acts as the lower cladding of the waveguide **305**. In addition, the die pad **358** is disposed on the multi-level interconnect layer **315**. The overcoat layer **350** is disposed over the waveguide **305** and the passivation layer **320**. The lead **360** is disposed on the die pad **358** and a portion of the overcoat layer **350**. Additional details regarding the spatial relationship of the components of the microelectronic package **300** depicted in FIGS. **7**A–**7**C are discussed in FIGS. **8**A–**8**J and **9**A–**9**J.

The substrate **310**, the multi-interconnect layer **315**, the passivation layer **320**, the overcoat layer **350**, the air-gap cladding layer **355**, the die pad **358**, the lead **360**, and the contact **365**, discussed in relation to FIGS. **7**A–**7**C, are analogous or similar to the waveguide **205**, the substrate **210**, the multi-interconnect layer **215**, the passivation layer **220**, the overcoat layer **250**, the air-gap cladding layer **255**, the die pad **258**, the lead **260**, and the contact **265**, discussed in reference to FIGS. **4**A–**4**C and **5**A–**5**J above. Therefore, additional discussion of these components will not be presented in relation to microelectronic package **300**. The reader is directed to the discussion presented above for further explanation of these components.

The waveguide **305** includes a waveguide core **330**, a grating coupler layer **335**, and couplers **340** and **341**. In this embodiment the couplers **340** and **341** are located above the waveguide core **330** in a surface-mount fashion. Surface-mounted coupler operates differently than the waveguide-embedded coupler system described in FIGS. **4**A–**4**C. The surface-mounted couplers **340** and **341** operate based on evanescent interaction between the grating coupler layer **335** and waveguide core layer **330**. The, waveguide **305** can communicate optical energy through the microelectronic package **300**.

For the purposes of illustration only, microelectronic package **300** of the present invention is described with particular reference to the below-described fabrication method. For clarity, some portions of the fabrication process are not included in FIGS. **8**A–**8**L and **9**A–**9**L. For example, photolithography or similar techniques can be used to define the overcoat layer **350**, the sacrificial layer, the waveguide **305**, and/or the lead **360** pattern. In this regard, the pattern can be defined by depositing material onto the surface of the substrate **310**, multi-level interconnect **315**, and/or the passivation layer **320** using techniques such as, for example, sputtering, chemical vapor deposition (CVD), plasma based deposition systems, evaporation, electron-beam systems. Furthermore, the pattern can then be removed using reactive ion etching techniques (RIE), for example.

The following fabrication processes are not intended to be an exhaustive list that includes every step required for fabricating microelectronic package **300**. In addition, the fabrication process is flexible because the process steps can be performed in a different order than the order illustrated in FIGS. **8**A–**8**L and **9**A–**9**L.

FIGS. **8**A–**8**L are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **7**A, while FIGS. **9**A–**9**L are cross-sectional views of the fabrication process relative to the view in FIG. **7**C, section B—B of FIG. **7**A. Therefore, FIGS. **8**A–**8**L and **9**A–**9**L illustrate corresponding views in the fabrication process from different cross-sectional views. The varying views of the fabrication process shown in FIGS. **8**A–**8**L and **9**A–**9**L have been provided to illustrate aspects of the fabrication process that are not necessarily observable using only FIGS. **8**A–**8**L or FIGS. **9**A–**9**L. In this regard, FIGS. **8**A and **9**A, **8**B and **9**B, **8**C and **9**C, and so on, are discussed in tandem to illustrate various aspects of the fabrication process.

FIGS. **8**A and **9**A illustrate the multi-level interconnect layer **315** disposed on the substrate **310**, while the passivation layer **320** is disposed on the multi-level interconnect layer **315**. In addition, the detector **325** is embedded in the substrate layer **310**.

FIGS. **8**B and **9**B illustrate the waveguide core **330** disposed on a portion of the passivation layer **320** after having been etched or photodefined, for example. In this embodiment the passivation layer **320** is the lower cladding of the waveguide **305**.

FIGS. **8**C and **9**C illustrate the coupler material **335** deposited on the waveguide core **330**. FIGS. **8**D and **9**D illustrate the defining and forming of the grating material **335** into grating couplers **340** and **341**.

FIGS. **8**E and **9**E illustrate the sacrificial layer **345** deposited over the passivation layer **320**, the waveguide core **330**, the grating layer **335**, and the grating couplers **340** and **341**.

FIGS. **8**F and **9**F illustrate the formation of the sacrificial layer section **346**, which defines the area where the air-gap cladding layer **355** will subsequently be located once the sacrificial layer section **346** is removed. FIGS. **8**G and **9**G illustrate the formation of the overcoat layer **350** on the passivation layer **320** and first sacrificial layer section **346**.

FIGS. **8**H and **9**H illustrate the removal of the sacrificial layer section **346** to form the air-gap cladding layer **355** and thereby forming the waveguide **305**. In this embodiment, the waveguide **305** includes the passivation layer **320** (lower cladding), the waveguide core **330**, the couplers **340** and **341**, and the air-gap cladding layer **355** (upper and side cladding).

FIGS. **8**I and **9**I illustrate the formation of the lead **360** upon the die pad **358** (not shown) after a via (not shown) is etched in the overcoat layer **350** in the area over the die pad **358**. It should be noted that the formation of the die pad **358** was omitted for clarity from earlier process steps. Alternatively, the sacrificial layer section **346** could be removed at this point in the fabrication.

FIGS. **8**J and **9**J illustrate the formation of a contact **365** on the lead **360**, thereby forming microelectronic package **300** depicted in FIGS. **7**A–**7**C. It should be noted that formation of the contact **365** is optional.

EXAMPLE 4

FIGS. **10**A–**10**C are schematics that illustrate three cross-sectional views of microelectronic package **400** having a waveguide **405** with couplers **440** and **441** surface-mounted and an air-gap layer **456**. FIGS. **10**B and **10**C are cross-sectional views of FIG. **10**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **10**A.

Microelectronic package **400** includes the waveguide **405**, a substrate **410**, a multi-level interconnect layer **415**, a passivation layer **420**, a detector **425**, an overcoat layer **450**, the air-gap layer **456**, a die pad **458**, a lead **460**, and a contact **465**. The multi-level interconnect layer **415** is disposed on the substrate **410**. The passivation layer **420** is disposed on the multi-level interconnect layer **415**. In this embodiment the waveguide **405** is disposed on the passivation layer **420**, where the passivation layer **420** acts as the lower cladding of the waveguide **405**. In addition, the die pad **458** is disposed on the multi-level interconnect layer **415**. The air-gap layer **458** is disposed on the passivation layer **420**. The overcoat layer **450** is disposed over the waveguide **405**, the passivation layer **420**, and the air-gap layer **456**. The lead **460** is disposed on the die pad **460** and a portion of the overcoat layer **450**. A portion of the lead **460** is disposed above the air-gap **456**. Additional details regarding the spatial relationship of the components of the microelectronic package **400** depicted in FIGS. **10**A–**10**C are discussed in FIGS. **11**A–**11**J and **12**A–**12**J. The, waveguide **405** can communicate optical energy through the microelectronic package **400**.

The waveguide **405**, the substrate **410**, the multi-interconnect layer **415**, the passivation layer **420**, the overcoat layer **450**, the air-gap cladding layer **455**, the die pad **458**, the lead **460**, and the contact **465**, discussed in relation to FIGS. **10**A=14 **10**C, are analogous or similar to the substrate **310**, the multi-interconnect layer **315**, the passivation layer **320**, the overcoat layer **350**, the air-gap cladding layer **355**, the die pad **358**, the lead **360**, and the contact **365**, discussed in reference to FIGS. **7**A–**7**C above. In addition, the air-gap layer **256** described in relation to FIGS. **4**A–**4**C is analogous or similar to the air-gap layer **456** described in relation to FIGS. **10**A–**10**C. Consequently, the second sacrificial layer described in relation to FIGS. **4**A–**4**C corresponds to the second sacrificial layer used to form the area where the air-gap layer **456** is formed upon removal of the second sacrificial layer (FIGS. **11**A–**11**J and **12**A–**12**J). Therefore, additional discussion of these components will not be presented in relation to microelectronic package **400**. The reader is directed to the discussion presented above for further explanation of these components.

For the purposes of illustration only, microelectronic package **400** of the present invention is described with particular reference to the below-described fabrication method. For clarity, some portions of the fabrication process are not included in FIGS. **11**A–**11**J and **12**A–**12**J. For example, photolithography or similar techniques can be used to define the overcoat layer **450**, the sacrificial layer, the waveguide **405**, and/or the lead **460** pattern. In this regard, the pattern can be defined by depositing material onto the surface of the substrate **410**, multi-level interconnect **415**, and/or the passivation layer **420** using techniques such as, for example, sputtering, chemical vapor deposition (CVD), plasma based deposition systems, evaporation, electron-beam systems. Furthermore, the pattern can then be removed using reactive ion etching techniques (RIE), for example.

The following fabrication processes are not intended to be an exhaustive list that includes every step required for fabricating microelectronic package **400**. In addition, the fabrication process is flexible because the process steps can be performed in a different order than the order illustrated in FIGS. **11**A–**11**J and **12**A–**12**J.

FIGS. **11**A–**11**J are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **1**A, while FIGS. **12**A–**12**J are cross-sectional views of the fabrication process relative to the view in FIG. **10**C, section B—B of FIG. **10**A. Therefore, FIGS. **11**A–**11**J and **12**A–**12**J illustrate corresponding views in the fabrication process from different cross-sectional views. The varying views of the fabrication process shown in FIGS. **11**A–**11**J and **12**A–**12**J have been provided to illustrate aspects of the fabrication process that are not necessarily observable using only FIGS. **11**A–**11**J or FIGS. **12**A–**12**J. In this regard, FIGS. **11**A and **12**A, **11**B and **12**B, **11**C and **12**C, and so on, are discussed in tandem to illustrate various aspects of the fabrication process.

FIGS. **11**A and **12**A illustrate the multi-level interconnect layer **415** disposed on the substrate **410**, while the passivation layer **420** is disposed on the multi-level interconnect layer **415**. In addition, the detector **425** is embedded in the substrate layer **410**.

FIGS. **11**B and **12**B illustrate the waveguide core **430** disposed on a portion of the passivation layer **420** after having been etched or photodefined, for example. In this embodiment the passivation layer **420** is the lower cladding of the waveguide **405**.

FIGS. **11**C and **12**C illustrate the coupler material **435** deposited on the waveguide core **430**. FIGS. **11**D and **12**D illustrate the defining and forming the grating material **435** into grating couplers **440** and **441**.

FIGS. **11**E and **12**E illustrate the sacrificial layer **445** deposited over the passivation layer **420**, the waveguide core **430**, the grating layer **435**, and the grating couplers **440** and **441**.

FIGS. **11**F and **12**F illustrate the formation of the first sacrificial layer section **446**, which defines the area where the air-gap cladding layer **455** will subsequently be located once the sacrificial layer section **446** is removed. In addition, FIG. **11**F and **12**F illustrate the formation of the second sacrificial layer section **447**, which defines the area where the air-gap layer **456** will subsequently be located once the second sacrificial layer section **447** is removed. It should be noted that the first and second sacrificial layer sections **446** and **447** do not have to be made from the same sacrificial layer. In this regard, appropriate fabrication steps could be included to form the sacrificial layer sections having different sacrificial layers.

FIGS. **11**G and **12**G illustrate the formation of the overcoat layer **450** on the passivation layer **420**, first sacrificial layer section **446**, and the second sacrificial layer section **447**.

FIGS. **11**H and **12**H illustrate the removal of the first sacrificial layer section **446** to form the air-gap cladding layer **455** and thereby forming the waveguide **405**. In this embodiment, the waveguide **405** includes the passivation layer **420** (lower cladding), the waveguide core **430**, the couplers **440** and **441**, and the air-gap cladding layer **455** (upper and side cladding). In addition, the second sacrificial layer section **447** is removed to form air-gap layer **456**.

FIGS. **11**I and **12**I illustrate the formation of the lead **460** upon the die pad **458** (not shown) after a via (not shown) is etched in the overcoat layer **450** in the area over the die pad **458**. It should be noted that the formation of the die pad **458** was omitted from earlier process steps for clarity. Alternatively, the sacrificial layer section **446** could be removed at this point in the fabrication.

FIGS. **11**J and **12**J illustrate the formation of a contact **465** on the lead **460**, thereby forming microelectronic package

400 depicted in FIGS. **10**A–**10**C. It should be noted that formation of the contact **465** is optional.

EXAMPLE 5

FIGS. **13**A–**13**C are schematics that illustrate three cross-sectional views of microelectronic package **500** having a suspended waveguide layer **505**. FIGS. **13**B and **13**C are cross-sectional views of FIG. **13**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **13**A.

Microelectronic package **500** includes the waveguide **505**, a substrate **510**, a multi-level interconnect layer **515**, a passivation layer **520**, a detector **525**, a lower cladding layer **526**, an overcoat layer **550**, a die pad **558**, a lead **560**, and a contact **565**. The multi-level interconnect layer **515** is disposed on the substrate **510** while the passivation layer **520** is disposed on the multi-level interconnect layer **515**. In addition, the die pad **558** is disposed on the multi-level interconnect layer **515**. The overcoat layer **550** is disposed on the passivation layer **520**. The lower cladding **526** is disposed upon the overcoat layer **550**. In this embodiment the waveguide **505** is disposed on the lower cladding **526**. Another overcoat layer **550** is disposed on the waveguide **505** and the lower cladding **526**. The lead **560** is disposed on the die pad **558** and a portion of the overcoat layer **550**. Additional details regarding the spatial relationship of the components of microelectronic package **500** depicted in FIGS. **13**A–**13**C are discussed in FIGS. **14**A–**14**L and **15**A–**15**L, which illustrate an exemplary fabrication process of microelectronic package **500**. The, waveguide **505** can communicate optical energy through the microelectronic package **500**.

The substrate **510**, the multi-interconnect layer **515**, the passivation layer **520**, the air-gap cladding layer **555**, the die pad **558**, the lead **560**, and the contact **565**, discussed in relation to FIGS. **13**A–**13**C, are analogous or similar to the substrate **410**, the multi-interconnect layer **415**, the passivation layer **420**, the overcoat layer **450**, the air-gap cladding layer **455**, the die pad **458**, the lead **460**, and the contact **465**, discussed in relation to FIGS. **13**A–**13**C above. Therefore, additional discussion of these components will not be presented in relation to microelectronic package **500**. The reader is directed to the discussion presented above for further explanation of these components.

In this embodiment, the overcoat layer **550** is deposited in two fabrication steps. Although additional fabrication steps are used to deposit the overcoat layer **550**, the overcoat layer **550** is analogous or similar to the overcoat layer **450** described in FIGS. **13**A–**13**C. Alternatively, the overcoat layer **550** can be composed of two different overcoat layer materials.

The lower cladding layer **526** includes materials having a lower index of refraction than the waveguide core **530** (FIGS. **14**A–**14**L and **15**A–**15**L). The lower cladding layer **526** can be fabricated from materials the same as or similar in nature to those materials employed for the waveguide core **530**. Consequently, the passivation layer **520** does not have to have a lower index of refraction than the waveguide core **530** (FIGS. **14**A–**14**L and **15**A–**15**L).

For the purposes of illustration only, microelectronic package **500** of the present invention is described with particular reference to the below-described fabrication method. For clarity, some portions of the fabrication process are not included in FIGS. **14**A–**14**L and **15**A–**15**L. For example, photolithography or similar techniques can be used to define the overcoat layer **550**, the sacrificial layer, the waveguide **505**, and/or the lead **560** pattern. In this regard, the pattern can be defined by depositing material onto the surface of the substrate **510**, multi-level interconnect **515**, and/or the passivation layer **520** using techniques such as, for example, sputtering, chemical vapor deposition (CVD), plasma based deposition systems, evaporation, electron-beam systems. Furthermore, the pattern can then be removed using reactive ion etching techniques (RIE), for example.

The following fabrication processes are not intended to be an exhaustive list that includes every step required for fabricating microelectronic package **500**. In addition, the fabrication process is flexible because the process steps may be performed in a different order than the order illustrated in FIGS. **14**A–**14**L and **15**A–**15**L.

FIGS. **14**A–**14**L are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **13**A, while FIGS. **15**A–**15**L are cross-sectional views of the fabrication process relative to the view in FIG. **13**C, section B—B of FIG. **13**A. Therefore, FIGS. **14**A–**14**L and **15**A–**15**L illustrate corresponding views in the fabrication process from different cross-sectional views. The varying views of the fabrication process shown in FIGS. **14**A–**14**L and **15**A–**15**L have been provided to illustrate aspects of the fabrication process that are not necessarily observable using only FIGS. **14**A–**14**L or FIGS. **15**A–**15**L. In this regard, FIGS. **14**A and **15**A, **14**B and **15**B, **14**C and **15**C, and so on are discussed in tandem to illustrate various aspects of the representative fabrication process.

FIGS. **14**A and **15**A illustrate the multi-level interconnect layer **515** disposed on the substrate **510**, while the passivation layer **520** is disposed on the multi-level interconnect layer **515**. In addition, the detector **525** is embedded in the substrate layer **510**.

FIGS. **14**B and **15**B illustrate the formation of the overcoat layer **550**A on the passivation layer **520**. FIGS. **14**C and **15**C illustrate the lower cladding **526** disposed on a portion of the overcoat **550**A. FIGS. **14**D and **15**D illustrate the waveguide core **530** disposed on a portion of the lower cladding **526**.

FIGS. **14**E and **15**E illustrate a portion of the waveguide core **530** that has been removed and replaced with grating material **535**. In an alternate embodiment, the waveguide core layer and grating material are the same layer, in which case no material is removed, and the grating couplers are defined only within the labeled areas.

FIGS. **14**F and **15**F illustrate the defining and forming of the grating material **535** into grating couplers **540** and **541**. FIGS. **14**G and **15**G illustrate the sacrificial layer **545** disposed over the overcoat layer **550**A, the lower cladding **526**, the waveguide core **530**, and the grating couplers **540** and **541**.

FIGS. **14**H and **15**H illustrate the formation of sacrificial layer section **546** by etching the sacrificial layer **545**, for example. The sacrificial layer section **546** defines the area where the air-gap cladding layer **555** will subsequently be located once the sacrificial layer section **546** is removed.

FIGS. **14**I and **15**I illustrate the overcoat layer **550**B disposed on the overcoat layer **550**A and the sacrificial layer section **546**. Overcoat layers **550**A and **550**B form overcoat layer **550**.

FIGS. **14**J and **15**J illustrate the removal of the sacrificial layer section **546** to form the air-gap cladding layer **555** and thereby forming the waveguide **505**. In this embodiment, the waveguide **505** includes the lower cladding layer **526**, the waveguide core **530**, the couplers **540** and **541**, and the air-gap cladding layer **555** (upper and side cladding).

FIGS. **14**K and **15**K illustrate the formation of the lead **560** upon the die pad **558** (not shown) after a via (not shown) is etched in the overcoat layer **550** in the area substantially over the die pad **558**. It should be noted that the formation of the die pad **558** was omitted from earlier process steps for clarity. Alternatively, the sacrificial layer section **546** could be removed at this point in the fabrication rather than in the previous step.

FIGS. **14**L and **15**L illustrate the formation of a contact **565** on the lead **560**, thereby forming microelectronic package **500**, as depicted in FIGS. **13**A–**13**C. It should be noted that formation of the contact **565** is optional.

EXAMPLE 6

FIGS. **16**A–**16**C are schematics that illustrate three cross-sectional views of microelectronic package **600** having a raised waveguide **605** and an air-gap layer **656**. FIGS. **16**B and **16**C are cross-sectional views of FIG. **16**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **16**A.

Microelectronic package **600** includes the waveguide **605**, a substrate **610**, a multi-level interconnect layer **615**, a passivation layer **620**, a detector **625**, a lower cladding layer **626**, a overcoat layer **650**, the air-gap layer **656**, a die pad **658**, a lead **660**, and a contact **665**. The multi-level interconnect layer **615** is disposed on the substrate **610**, while the passivation layer **620** is disposed on the multi-level interconnect layer **615**. In addition, air-gap layer **656** is disposed on the passivation layer **620**. The die pad **658** is disposed on the multi-level interconnect layer **615**. The overcoat layer **650** is disposed on the passivation layer **620**. The lower cladding **626** is disposed upon the overcoat layer **650**. In this embodiment the waveguide **605** is disposed on the lower cladding **626**. Another overcoat layer **650** is disposed on the waveguide **605** and the lower cladding **626**. The lead **660** is disposed on the die pad **658** and a portion of the overcoat layer **650**. Additional details regarding the relationship of the components of microelectronic package **600** depicted in FIGS. **16**A-**16**C are discussed in FIGS. **17**A–**17**N and **18**A–**18**N, which illustrate an exemplary fabrication process of microelectronic package **600**. The, waveguide **605** can communicate optical energy through the microelectronic package **600**.

The waveguide **605**, substrate **610**, the multi-interconnect layer **615**, the passivation layer **620**, the lower cladding **626**, the air-gap cladding layer **655**, the die pad **658**, the lead **660**, and the contact **665**, discussed in relation to FIGS. **16**A–**16**C, are analogous or similar to the substrate **510**, the multi-interconnect layer **515**, the passivation layer **520**, the overcoat layer **550**, the air-gap cladding layer **555**, the die pad **558**, the lead **560**, and the contact **565**, discussed in relation to FIGS. **13**A–**13**C above.

In addition, the air-gap layer **656** described in relation to FIGS. **16**A–**16**C is analogous or similar to the air-gap layer **456** described in relation to FIGS. **10**A–**10**C. Consequently, the second sacrificial layer described in relation to FIGS. **10**A–**10**C corresponds to the second sacrificial layer used to form the area where the air-gap layer **656** is formed upon removal of the second sacrificial layer (FIGS. **17**A–**17**N and **18**A–**18**N). Therefore, additional discussion of these components will not be presented in relation to microelectronic package **600**. The reader is directed to the discussion presented above for further explanation of these components.

In contrast to FIGS. **10**A–**10**C, the air-gap cladding layer **655** and the air-gap layer **656** are formed in different fabrication steps. The fabrication process is described below in relation to FIGS. **17**A–**17**N and **18**A and **18**N.

For the purposes of illustration only, microelectronic package **600** of the present invention is described with

particular reference to the below-described fabrication method. For clarity, some portions of the fabrication process are not included in FIGS. **14**A–**14**L and **15**A–**15**L. For example, photolithography or similar techniques can be used to define the overcoat layer **650**, the sacrificial layer, the waveguide **605**, and/or the lead **660** pattern. In this regard, the pattern can be defined by depositing material onto the surface of the substrate **610**, the multi-level interconnect **615**, and/or the passivation layer **620** using techniques such as, for example, sputtering, chemical vapor deposition (CVD), plasma based deposition systems, evaporation, electron-beam systems. Furthermore, the pattern can then be removed using reactive ion etching techniques (RIE), for example.

The following fabrication processes are not intended to be an exhaustive list that includes every step required for fabricating microelectronic package **600**. In addition, the fabrication process is flexible because the process steps may be performed in a different order than the order illustrated in FIGS. **14**A–**14**L and **15**A–**15**L.

FIGS. **17**A–**17**N are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **16**A, while FIGS. **18**A–**18**N are cross-sectional views of the fabrication process relative to the view in FIG. **16**C, section B—B of FIG. **16**A. Therefore, FIGS. **17**A–**17**N and **18**A–**18**N illustrate corresponding views in the fabrication process from different cross-sectional views. The varying views of the fabrication process shown in FIGS. **17**A–**17**N and **18**A–**18**N have been provided to illustrate aspects of the fabrication process that are not necessarily observable using only FIGS. **17**A–**17**N or FIGS. **18**A–**18**N. In this regard, FIGS. **17**A and **18**A, **17**B and **18**B, **17**C and **18**C, and so on, are discussed in tandem to illustrate various aspects of the representative fabrication process.

FIGS. **17**A and **18**A illustrate the multi-level interconnect layer **615** disposed on the substrate **610**, while the passivation layer **620** is disposed on the multi-level interconnect layer **615**. In addition, the detector **625** is embedded in the substrate layer **610**. FIGS. **17**B and **18**B illustrate the sacrificial layer **645**A deposited over the passivation layer **620**.

FIGS. **17**C and **18**C illustrate the formation of the second sacrificial layer section **647** by etching the sacrificial layer **645**A, for example. The second sacrificial layer section **646** defines the area where the air-gap layer **655** will subsequently be located once the sacrificial layer section **647** is removed.

FIGS. **17**D and **18**D illustrate the formation of the overcoat layer **650**A on the passivation layer **620** and second sacrificial layer section **647**. FIGS. **17**E and **18**E illustrate the lower cladding **626** disposed on a portion of the overcoat **650**A. FIGS. **17**F and **18**F illustrate the waveguide core **630** disposed on a portion of the lower cladding **626**.

FIGS. **17**G and **18**G illustrate a portion of the waveguide core **630** that has been removed and replaced with grating material **635**. In an alternate embodiment, the waveguide core layer and grating material are the same layer, in which case no material is removed, and the grating couplers are defined only within the labeled areas.

FIGS. **17**H and **18**H illustrate the defining and forming of the grating material **635** into grating couplers **640** and **641**. FIGS. **17**I and **18**I illustrate the sacrificial layer **645**B deposited over the overcoat layer **650**A, the lower cladding **626**, the waveguide core **630**, and the grating couplers **640** and **641**.

FIGS. **17**J and **18**J illustrate the formation of a first sacrificial layer section **646** by etching the sacrificial layer

645B, for example. The first sacrificial layer section **646** defines the area where the air-gap cladding layer **655** will subsequently be located once the sacrificial layer section **646** is removed.

FIGS. **17**K and **18**K illustrate the formation of the overcoat layer **650**B on the overcoat layer **650**A, the first sacrificial layer section **647**, and the second sacrificial layer section **647**. Overcoat layers **650**A and **650**B form entire overcoat layer **650**.

FIGS. **17**L and **18**L illustrate the removal of the first sacrificial layer section **646** to form the air-gap cladding layer **655** and thereby forming the waveguide **605**. In this embodiment, the waveguide **605** includes the lower cladding layer **626**, the waveguide core **630**, the couplers **640** and **641**, and the air-gap cladding layer **655** (upper and side cladding). In addition, the second sacrificial layer **647** is removed to form the air-gap layer **656**.

FIGS. **17**M and **18**M illustrate the formation of the lead **660** upon the die pad **658** (not shown) after a via (not shown) is etched in the overcoat layer **650** in the area substantially over the die pad **658**. It should be noted that the formation of the die pad **658** was omitted from earlier process steps for clarity. Alternatively, the first sacrificial layer section **646** and second sacrificial layer section **647** could be removed at this point in the fabrication rather than in the previous step.

FIGS. **17**N and **18**N illustrate the formation of a contact **665** on the lead **660**, thereby forming microelectronic package **600**, as depicted in FIGS. **16**A–**16**C. It should be noted that formation of the contact **665** is optional.

EXAMPLE 7

FIGS. **19**A–**19**C are schematics that illustrate three cross-sectional views of microelectronic package **700** having a raised waveguide **705** with surface-mounted couplers **740** and **741**. FIGS. **19**B and **19**C are cross-sectional views of FIG. **19**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **19**A.

Microelectronic package **700** includes the waveguide **705**, a substrate **710**, a multi-level interconnect layer **715**, a passivation layer **720**, a detector **725**, a lower cladding layer **726**, a overcoat layer **750**, a die pad **758**, a lead **760**, and a contact **765**. The multi-level interconnect layer **715** is disposed on the substrate **710**, while the passivation layer **720** is disposed on the multi-level interconnect layer **715**. In addition, the die pad **758** is disposed on the multi-level interconnect layer **715**. The overcoat layer **750** is disposed on the passivation layer **720**. The lower cladding **726** is disposed upon the overcoat layer **750**. In this embodiment the waveguide **705** is disposed on the lower cladding **726**. Another overcoat layer **750** is disposed on the waveguide **705** and the lower cladding **726**. The lead **760** is disposed on the die pad **758** and a portion of the overcoat layer **750**. Additional details regarding the spatial relationship of the components of microelectronic package **700** depicted in FIGS. **19**A–**19**C are discussed in FIGS. **20**A–**20**N and **21**A–**21**N, which illustrate an exemplary fabrication process of microelectronic package **700**. The, waveguide **705** can communicate optical energy through the microelectronic package **700**.

The waveguide **705**, substrate **710**, the multi-interconnect layer **715**, the passivation layer **720**, the air-gap cladding layer **755**, the die pad **758**, the lead **760**, and the contact **765**, discussed in relation to FIGS. **19**A–**19**C, are analogous or similar to the waveguide **405**, substrate **410**, the multi-interconnect layer **415**, the passivation layer **420**, the overcoat layer **450**, the air-gap cladding layer **455**, the die pad **458**, the lead **460**, and the contact **465**, discussed in relation to FIGS. **10**A–**10**C above. Therefore, additional discussion of these components will not be presented in relation to microelectronic package **700**. The reader is directed to the discussion presented above for further explanation of these components.

For the purposes of illustration only, microelectronic package **700** of the present invention is described with particular reference to the below-described fabrication method. For clarity, some portions of the fabrication process are not included in FIGS. **20**A–**20**N and **21**A–**21**N. For example, photolithography or similar techniques can be used to define the overcoat layer **750**, the sacrificial layer, the waveguide **705**, and/or the lead **760** pattern. In this regard, the pattern can be defined by depositing material onto the surface of the substrate **710**, the multi-level interconnect **715**, and/or the passivation layer **720** using techniques such as, for example, sputtering, chemical vapor deposition (CVD), plasma based deposition systems, evaporation, electron-beam systems. Furthermore, the pattern can then be removed using reactive ion etching techniques (RIE), for example.

The following fabrication processes are not intended to be an exhaustive list that includes every step required for fabricating microelectronic package **700**. In addition, the fabrication process is flexible because the process steps may be performed in a different order than the order illustrated in FIGS. **20**A–**20**N and **21**A–**21**N.

FIGS. **20**A–**20**N are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **19**A, while FIGS. **21**A–**21**N are cross-sectional views of the fabrication process relative to the view in FIG. **19**C, section B—B of FIG. **19**A. Therefore, FIGS. **20**A–**20**N and **21**A–**21**N illustrate corresponding views in the fabrication process from different cross-sectional views. The varying views of the fabrication process shown in FIGS. **20**A–**20**N and **21**A–**21**N have been provided to illustrate aspects of the fabrication process that are not necessarily observable using only FIGS. **20**A–**20**N or FIGS. **21**A–**21**N. In this regard, FIGS. **20**A and **21**A, **20**B and **21**B, **20**C and **21**C, and so on, are discussed in tandem to illustrate various aspects of the representative fabrication process.

FIGS. **20**A and **21**A illustrate the multi-level interconnect layer **715** disposed on the substrate **710**, while the passivation layer **720** is disposed on the multi-level interconnect layer **715**. In addition, the detector **725** is embedded in the substrate layer **710**.

FIGS. **20**B and **21**B illustrate the formation of the overcoat layer **750A** on the passivation layer **720**. FIGS. **20**C and **21**C illustrate the lower cladding **726** disposed on a portion of the overcoat **750**A. FIGS. **20**D and **21**D illustrate the waveguide core **730** disposed on a portion of the lower cladding **726**. FIGS. **20**E and **21**E illustrate the coupler material **735** deposited on the waveguide core **730**.

FIGS. **20**F and **21**F illustrate the defining and forming the grating material **735** into grating couplers **740** and **741**. FIGS. **20**G and **21**G illustrate the sacrificial layer **745** deposited over the overcoat layer **750A**, the lower cladding **726**, the waveguide core **730**, and the grating couplers **740** and **741**.

FIGS. **20**H and **21**H illustrate the formation of sacrificial layer section **746** by etching the sacrificial layer **745**, for example. The sacrificial layer section **746** defines the area where the air-gap cladding layer **755** will subsequently be located once the sacrificial layer section **746** is removed.

FIGS. **20**I and **21**I illustrate the formation of the overcoat layer **750B** on the overcoat layer **750A** and the sacrificial layer section **746**. Overcoat layers **750**A and **750**B form overcoat layer **750**.

FIGS. **20**J and **21**J illustrate the removal of the sacrificial layer section **746** to form the air-gap cladding layer **755** and thereby forming the waveguide **705**. In this embodiment, the waveguide **705** includes the lower cladding layer **526**, the waveguide core **730**, the couplers **740** and **741**, and the air-gap cladding layer **755** (upper and side cladding).

FIGS. **20**K and **21**K illustrate the formation of the lead **760** upon the die pad **758** (not shown) after a via (not shown) is etched in the overcoat layer **750** in the area substantially over the die pad **758**. It should be noted that the formation of the die pad **758** was omitted from earlier process steps for clarity. Alternatively, the sacrificial layer section **746** could be removed at this point in the fabrication rather than in the previous step.

FIGS. **20**L and **21**L illustrate the formation of a contact **765** on the lead **760**, thereby forming microelectronic package **700**, as depicted in FIGS. **19**A–**19**C. It should be noted that formation of the contact **765** is optional.

EXAMPLE 8

FIGS. **22**A–**22**C are schematics that illustrate three cross-sectional views of microelectronic package **800** having a raised waveguide **805** with surface-mounted couplers **840** and **841** and an air-gap layer **856**. FIGS. **22**B and **22**C are cross-sectional views of FIG. **22**A in the A—A and B—B direction, respectively, as shown by the arrows in FIG. **22**A.

Microelectronic package **800** includes the waveguide **805**, a substrate **810**, a multi-level interconnect layer **815**, a passivation layer **820**, a detector **825**, a lower cladding layer **826**, a overcoat layer **850**, the air-gap layer **856**, a die pad **858**, a lead **860**, and a contact **865**. The multi-level interconnect layer **815** is disposed on the substrate **810**, while the passivation layer **820** is disposed on the multi-level interconnect layer **815**. In addition, the air-gap layer **856** is disposed on the passivation layer **820**. The die pad **858** is disposed on the multi-level interconnect layer **815**. The overcoat layer **850** is disposed on the passivation layer **820**. The lower cladding **826** is disposed upon the overcoat layer **850**. In this embodiment the waveguide **805** is disposed on the lower cladding **826**. Another overcoat layer **850** is disposed on the waveguide **805** and the lower cladding **826**. The lead **860** is disposed on the die pad **858** and a portion of the overcoat layer **850**. In addition, the lead **860** is disposed over a portion of the air-gap layer **856**. Additional details regarding the spatial relationship of the components of microelectronic package **800** depicted in FIGS. **22**A–**22**C are discussed in FIGS. **23**A–**23**N and **24**A–**24**N, which illustrate an exemplary fabrication process of microelectronic package **800**. The, waveguide **805** can communicate optical energy through the microelectronic package **800**.

The waveguide **805**, substrate **810**, the multi-interconnect layer **815**, the passivation layer **820**, the air-gap cladding layer **855**, the air-gap layer **856**, the die pad **858**, the lead **860**, and the contact **865**, discussed in relation to FIGS. **22**A–**22**C, are analogous or similar to the waveguide **405**, substrate **410**, the multi-interconnect layer **415**, the passivation layer **420**, the overcoat layer **450**, the air-gap cladding layer **455**, the air-cladding layer **456**, the die pad **458**, the lead **460**, and the contact **465**, discussed in relation to FIGS. **10**A–**10**C above. In addition, the lower cladding **726** discussed in reference to FIGS. **19**A–**19**C is the same or similar to the lower cladding **826** discussed in reference to FIGS. **22**A–**22**C. Therefore, additional discussion of these components will not be presented in relation to microelectronic package **800**. The reader is directed to the discussion presented above for further explanation of these components.

For the purposes of illustration only, microelectronic package **800** of the present invention is described with particular reference to the below-described fabrication method. For clarity, some portions of the fabrication process are not included in FIGS. **23**A–**23**N and **24**A–**24**N. For example, photolithography or similar techniques can be used to define the overcoat layer **850**, the sacrificial layer, the waveguide **805**, and/or the lead **860** pattern. In this regard, the pattern can be defined by depositing material onto the surface of the substrate **810**, the multi-level interconnect **815**, and/or the passivation layer **820** using techniques such as, for example, sputtering, chemical vapor deposition (CVD), plasma based deposition systems, evaporation, electron-beam systems. Furthermore, the pattern can then be removed using reactive ion etching techniques (RIE), for example.

The following fabrication processes are not intended to be an exhaustive list that includes every step required for fabricating microelectronic package **800**. In addition, the fabrication process is flexible because the process steps may be performed in a different order than the order illustrated in FIGS. **23**A–**23**N and **24**A–**24**N.

FIGS. **23**A–**23**N are cross-sectional views of the fabrication process relative to the view illustrated in FIG. **22**A, while FIGS. **24**A–**24**N are cross-sectional views of the fabrication process relative to the view in FIG. **22**C, section B—B of FIG. **22**A. Therefore, FIGS. **23**A–**23**N and **24**A–**24**N illustrate corresponding views in the fabrication process from different cross-sectional views. The varying views of the fabrication process shown in FIGS. **23**A–**23**N and **24**A–**24**N have been provided to illustrate aspects of the fabrication process that are not necessarily observable using only FIGS. **23**A–**23**N or FIGS. **24**A–**24**N. In this regard, FIGS. **23**A and **24**A, **23**B and **24**B, **23**C and **24**C, and so on, are discussed in tandem to illustrate various aspects of the representative fabrication process.

FIGS. **23**A and **24**A illustrate the multi-level interconnect layer **815** disposed on the substrate **810**, while the passivation layer **820** is disposed on the multi-level interconnect layer **815**. In addition, the detector **825** is embedded in the multi-level interconnect layer **815**. FIGS. **23**B and **24**B illustrate the sacrificial layer **845**A deposited over the passivation layer **820**.

FIGS. **23**C and **24**C illustrate the formation of the second sacrificial layer section **847** by etching the sacrificial layer **845**A, for example. The second sacrificial layer section **846** defines the area where the air-gap layer **855** will subsequently be located once the sacrificial layer section **846** is removed.

FIGS. **23**D and **24**D illustrate the formation of the overcoat layer **850**A on the passivation layer **820**. FIGS. **23**E and **24**E illustrate the lower cladding **826** disposed on a portion of the overcoat **850**A. FIGS. **23**F and **24**F illustrate the waveguide core **830** disposed on a portion of the lower cladding **826**.

FIGS. **23**G and **24**G illustrate the coupler material **835** deposited on the waveguide core **830**. FIGS. **23**H and **24**H illustrate the defining and forming the grating material **835** into grating couplers **840** and **841**.

FIGS. **23**I and **24**I illustrate the second sacrificial layer **845**B deposited over the overcoat layer **850**A, the lower cladding **826**, the waveguide core **830**, and the grating couplers **840** and **841**.

FIGS. **23**J and **24**J illustrate the formation of first sacrificial layer section **846** by etching the second sacrificial layer

845B, for example. The sacrificial layer section **846** defines the area where the air-gap cladding layer **855** will subsequently be located once the sacrificial layer section **846** is removed.

FIGS. **23**K and **24**K illustrate the formation of the overcoat layer **850**B on the overcoat layer **850**A and the first sacrificial layer section **846**. Overcoat layers **850**A and **850**B form overcoat layer **850**.

FIGS. **23**L and **24**L illustrate the removal of the first sacrificial layer section **846** to form the air-gap cladding layer **855** and thereby forming the waveguide **805**. In this embodiment, the waveguide **805** includes the lower cladding layer **826**, the waveguide core **830**, the couplers **840** and **841**, and the air-gap cladding layer **855** (upper and side cladding). In addition, the second sacrificial layer section **847** is removed to form the air-gap layer **856**.

FIGS. **23**M and **24**M illustrate the formation of the lead **860** upon the die pad **858** (not shown) after a via (not shown) is etched in the overcoat layer **850** in the area substantially over the die pad **858**. It should be noted that the formation of the die pad **858** was omitted from earlier process steps for clarity. Alternatively, the first sacrificial layer section **846** and the second sacrificial layer **847** could be removed at this point in the fabrication rather than in the previous step.

FIGS. **23**N and **24**N illustrate the formation of a contact **865** on the lead **860**, thereby forming microelectronic package **800**, as depicted in FIGS. **22**A–**22**C. It should be noted that formation of the contact **865** is optional.

It should be emphasized that the above-described embodiments of the present invention are merely possible examples of implementations, merely set forth for a clear understanding of the principles of the invention. Many variations and modifications may be made to the above-described embodiments. For example, a plurality of air-gap layers can be included in the microelectronic package. In addition, the air-gap layer can occupy space only bound by the overcoat layer (i.e. suspended above the passivation layer). Further, an additional air-gap can be located between the lead and the compliant layer. Furthermore, the detector can be embedded (i.e., suspended above the substrate) within the electronic package and connected to the multi-level interconnect layer. All such modifications and variations are intended to be included herein within the scope of this disclosure and protected by the following claims.

Therefore, having thus described the invention, at least the following is claimed:

1. A chip-level electronic package comprising:

at least one monolithic waveguide having;

a waveguide core disposed in a fixed position on a lower cladding,

an air-gap cladding around a portion of the waveguide core, and

an overcoat layer engaging a portion of the air-gap cladding and engaging the lower cladding, wherein the air-gap cladding is completely bound on all sides by the overcoat layer, the lower cladding and the waveguide core.

2. The chip-level electronic package of claim **1**, further comprising:

a lead, and

at least one air-gap layer disposed substantially under a portion of the lead and wherein the at least one waveguide is adjacent the air-gap layer.

3. The chip-level electronic package of claim **1**, further comprising:

a coupling element adjacent to the waveguide core and engaging the air-gap cladding.

4. The chip-level electronic package of claim **1**, wherein the waveguide core includes at least one coupling element.

5. The chip-level electronic package of claim **4**, wherein the at least one coupling element is a volume grating coupling element.

6. The chip-level electronic package of claim **4**, wherein the air-gap cladding is disposed around a portion of one of the at least one coupling element.

7. The chip-level electronic package of claim **1**, wherein the waveguide core is adjacent to a lower waveguide cladding.

8. The chip-level electronic package of claim **1**, wherein the overcoat layer is selected from silicon dioxide, silicon nitride, polyimides, polynorbornenes, epoxides, polyarylenes ethers and parylenes.

9. The chip-level electronic package of claim **1**, wherein the overcoat layer is selected from polyimides, polynorbornenes, epoxides, polyarylenes ethers, and parylenes.

10. The chip-level electronic package of claim **1**, wherein the overcoat layer is selected from polymides and polynorbornenes.

11. A method of operating a chip-level electronic package comprising:

coupling an optical signal to a one monolithic waveguide in the wafer-level electronic package, and

communicating the optical signal through the waveguide, the waveguide having a waveguide core disposed in a fixed position on a lower cladding, an air-gap cladding around a portion of the waveguide core, and an overcoat layer engaging a portion of the air-gap cladding and engaging the lower cladding, wherein the air-gap cladding is completely bound on all sides by the overcoat layer, the lower cladding and the waveguide core.

12. A chip-level electronic package comprising:

at least one monolithic waveguide having,

a waveguide core disposed in a fixed position on a lower cladding

an air-gap cladding around a portion of the waveguide core, and

and overcoat layer engaging a portion of the air-gap cladding and engaging the lower cladding, wherein the air-gap cladding is bound by the overcoat layer, the lower cladding, and the waveguide core.

13. A method of operating a chip-level electronic package comprising:

coupling an optical signal to a one monolithic waveguide in the wafer-level electronic package, and communicating the optical signal through the waveguide, the waveguide having a waveguide core disposed in a fixed position on a lower cladding, and air-gap cladding around a portion of the waveguide core, and an overcoat layer engaging a portion of the air-gap cladding and engaging the lower cladding, wherein the air-gap cladding is bound by the overcoat layer, the lower cladding and the waveguide core.

* * * * *