A Floating-Gate Δ-Σ Modulator

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A Floating-Gate Δ-Σ Modulator

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To Allen, Eveline and Angeline for their selfless love and support throughout.

To Pinar Sayin JaJa for bringing joy and laughter into my life...

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ix

SUMMARY

Δ-Σ Analog to Digital Converters are well-known for their high dynamic range (bit resolution) and robustness to circuit imperfections. Conventional Δ-Σ ADCs are designed around switched capacitor circuits using some form of distributed feedback or feedforward or both in the modulator loop. The loop coefficients are realized using capacitors. Passive components like capacitors in an integrated circuit have associated limitations–value spread, matching and limited programmability. This thesis proposes the application of floating-gate techniques to address these issues. Electronic potentiometers(e-pots) are floating-gate elements which can provide accurate and programmable on-chip reference voltages. These voltages determine the feedback coefficients of the modulator. With e-pots, the modulator can be optimized while in operation to correct for fabrication mismatches, or to realize various noise shaping functions. The e-pots can be re-programmed in the event of any environmental deterioration to retrieve desired response. An experimental chip that can implement second through fourth order modulators has been fabricated in a 0.5μm CMOS process. Simulation and experimental results for a second order modulator on this prototype are presented. Preliminary experimental results of a third modulator are also shown. The prototype is used as a proof of concept device to explore the limitations of the proposed technique. Circuit level optimizations to improve performance are considered.

CHAPTER I

OVERSAMPLING ANALOG TO DIGITAL

CONVERTERS

The features of oversampling data converters are reviewed. The advantages of over-sampling converters are considered with particular emphasis on Δ-Σ noise shaping converters. Typical performance metrics and their definitions are discussed.

1.1 *Overview of Oversampling ADCs*

Data converters are divided into two categories–*Nyquist rate* converters and *oversampling* converters, according to the ratio of the sampling rate to the Nyquist rate. The ratio is referred to as the *oversampling ratio–M*. Typical values of M for oversampling converters found in prior literature are from 16 to 256 [2, 4, 7, 21, 8]. Δ-Σ ADCs belong to the class of oversampling data converters.

Over-sampling ADCs are based on trading off accuracy in amplitude for accuracy in time [2]. The final digital output is obtained from several coarsely quantized, generally 2-level encoded samples. Oversampling affords the following advantages:

1. Relaxed anti-aliasing filter requirements at the input.

2. Dedicated Sample and Hold circuits are not necessary.

3. Relatively high tolerance to circuit imperfections such as comparator offsets and

integrator gain variations.

Under certain assumptions [21], the error introduced by quantization can be shown to have the characteristics of white noise, uncorrelated with the input signal. Oversampling spreads the quantization noise over a wider frequency range, thereby reducing the fraction of noise power in the bandwidth of interest. To make the process more efficient and obtain higher resolution, noise-shaping converters place the quantizer in a feedback loop. Such a system selectively attenuates the in-band noise, while leaving the signal spectrum unaltered. A noise shaping converter employing a coarse quantizer, goes by the name of Δ-Σ *modulator*. The order of a modulator refers to the number of integrator elements in the forward path of the loop.

1.2 Δ-Σ *Analog-to-Digital Converters*

Δ-Σ Analog to Digital converters are well-known for their high dynamic range and robustness to circuit imperfections such as variations in integrator gains [1, 6, 10, 16, 26].

1.2.1   Principles

The converter works by shaping the quantization noise spectrum of an over-sampled low-resolution signal, to push most of the noise power into frequencies far beyond the band of interest. Thereafter, a decimation filter removes the out of band quantization error from the output, giving a high-resolution digital signal. The converter consists of two building blocks–the modulator which shapes the noise and the decimation filter. A first-order modulator is shown in figure 1. It consists of an integrator and a
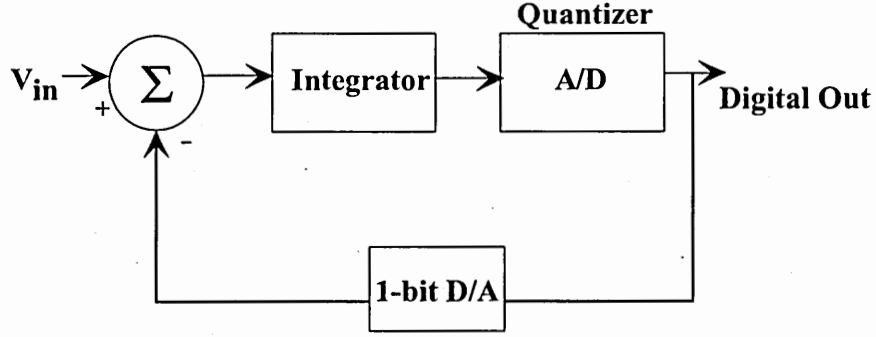
Figure 1: Block diagram of a first order Δ-Σ modulator.

1-bit quantizer in a feedback loop. The integrator is typically realized using switched capacitor circuits, while the 1-bit quantizer is a comparator. The DAC output could be a scaled version of the quantizer output.

When the integrator output has positive(negative) polarity, the quantizer feeds back a positive(negative) reference voltage that is subtracted(added) from(to) the input. The integrator accumulates the error between the input and the quantized output, and the comparator forces this error value towards zero. Thus the local time average of the output tracks the local time average of the input. This is true provided the integrator does not saturate. The decimation filter computes the local average and uses the number so obtained as a digital representation of the analog input signal.

1.2.2 Performance Metrics

Δ-Σ modulator performance is measured using the following metrics [17, 18]. All spectral computations are performed in the bandwidth of interest.

1. **Signal-to-Noise Ratio [SNR]:** SNR is defined to be the ratio in decibels of the signal power to the noise power at the modulator output. It is measured

using a spectral analysis (FFT) of the output. An FFT by itself introduces spectral power leakage between adjoining frequency bins [8]. Windowing functions are used to minimize spectral leakage and improve the SNR estimate. In practice, SNR is computed by taking the ratio of the rms signal to the rms noise, which includes all spectral components minus the fundamental, the first four harmonics and the DC offset.

2. **Signal-to-Noise and Distortion Ratio** [SINAD]: SINAD is evaluated as the ratio in decibels of signal power to the power of all spectral components minus the fundamental and the DC offset. For sinusoidal input signals, the first N harmonics of THD, usually the 2nd through 5th harmonics are included. SINAD is specified for a given input frequency and sampling rate.

3. **Total Harmonic Distortion** [THD]: Harmonic distortion is produced by ADC non-linearities. For pure sine-wave inputs, the harmonic distortion components in the output spectrum are at frequencies which are integer multiples of the applied sinusoidal frequency. The output THD is computed as the ratio in decibels, of the rms sum of the amplitudes of the first four harmonics of the input signal frequency to the amplitude of the fundamental.

$$THD = 20 log_{10}\left(\frac{\sqrt{A_{HD2,rms}^2 + A_{HD3,rms}^2 + A_{HD4,rms}^2 + A_{HD5,rms}^2}}{A_{fin,rms}}\right) \quad (1)$$

4. **Spurious-Free Dynamic Range** [SFDR]: SFDR is the ratio in decibels of the rms amplitude of the fundamental to the rms value of the next-largest spurious/harmonic component, excluding DC offset in a specified frequency

4

range. SFDR is specified when harmonic distortion and spurious signals are considered undesirable in the ADC output spectrum, for a pure sinusoidal input. SFDR is measured usually by applying a near full-scale sinusoidal input such as -1dBFS (dB full-scale) and plotting the FFT of the output.

$$SFDR_{dB} = 20log_{10}\left(\frac{A_{fin,rms}}{A_{HDmax,rms}}\right) \tag{2}$$

or

$$SFDR_{dB} = 20log_{10}\left(\frac{A_{fin,rms}}{A_{SPURmax,rms}}\right) \tag{3}$$

Complete specification of SFDR requires specifying the sampling frequency as well as input frequency and amplitude at which the measurement was made.

5. **Dynamic Range** [DR]: The dynamic range of a data converter is the input signal amplitude range it can handle. DR is defined to be the ratio in decibels, of the power of a full-scale sinusoidal input for undistorted output to the power of a sinusoidal input for which the SNR is 1. It is shown [21] that for a single-bit quantizer with modulator order L, and oversampling ratio M,

$$DR = \frac{3\left(2L+1\right)M^{2L+1}}{2\left(\pi^{2L}\right)} \tag{4}$$

6. **Effective Number of Bits** [ENOB]: ENOB expresses the resolution of the ADC in terms of effective number of bits in its digital representation. ENOB is specified at a particular input frequency, amplitude and sampling rate. ENOB is directly related to SINAD and is expressed as,

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02} \tag{5}$$

1.3 Research Outline

This research focuses on building single loop, 1-bit Δ-Σ modulators, using switched capacitor techniques, to address the following issues.

1. **Lack of Programmability:** The modulator parameters, such as integrator gains and feedback coefficients cannot be modified or optimized after fabrication.

2. **Capacitor Spread:** Capacitor ratios are set to achieve particular coefficient values. A large capacitance spread results in an increased overall area, which could be a bottleneck for multichannel ADCs on a single die.

Specifically, the goals of this thesis are to demonstrate the feasibility of using floating-gate voltage references in a Δ-Σ modulator. Results from current literature [5, 19] are used to model system behavior at a higher level of abstraction, incorporating as much circuit information as possible. Behavioral simulations are used to design modulator elements. Circuit performance is evaluated using SPICE simulations and experiments on a silicon prototype. The implementation of the decimation filter is not considered in this work. Rather, an ideal decimation is assumed and post-processing of modulator output is carried out in software.

These goals are part of a collaborative effort in the Integrated Computational Electronics Lab to apply floating-gate techniques to the space of various A–to–D and D–to–A converters.

The rest of this work is organized as follows. In chapter 2, the architecture of the proposed modulator incorporating floating-gate elements is described. Chapter 3

6

details the high-level models used to describe the modulator and determine optimum coefficients. In chapter 4 the circuit implementation and simulation results are presented. The experimental measurement setup and results are dealt with in chapter 5. Chapter 6 concludes by stating how limitations of the current prototype are being addressed.

CHAPTER II

PROGRAMMABLE DISCRETE-TIME

FLOATING-GATE Δ-Σ MODULATOR

This chapter describes the proposed programmable Δ-Σ modulator with floating-gate elements. This architecture was discussed in [22] and refined in [23]. Floating-gate elements called e-pots [11] are used to provide programmability to the modulator. The structure and programming of of e-pots is reviewed. This is followed by details of how e-pots are incorporated into the modulator as programmable reference voltages.

Figure 2 shows a conventional n^{th} order modulator. The proposed alternate implementation incorporating e-pots is shown in figure 3. The modulator architecture is a Distributed Feedback (DFB) with Cascade of Integrators (COI) in the forward path [3]. The integrator gains are kept constant to reduce the degrees of freedom of the circuit. The feedback coefficients are programmed using e-pots. The use of e-pots provides the following advantages–No dependence on capacitor ratios; Capacitance spread may be reduced; Circuit is programmable while in operation; Multiple transfer functions can be realized for a given modulator order.

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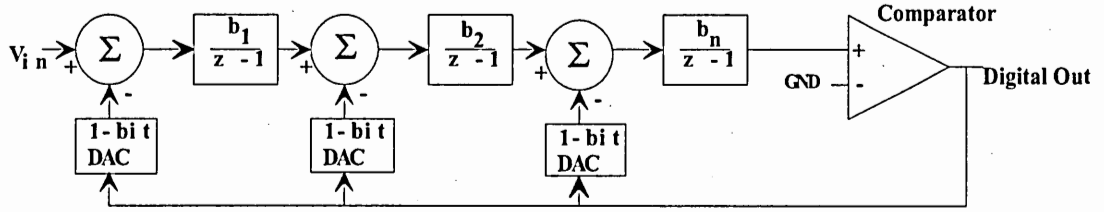
Figure 2: Cascade of integrators n^{th} order modulator with distributed feedback.
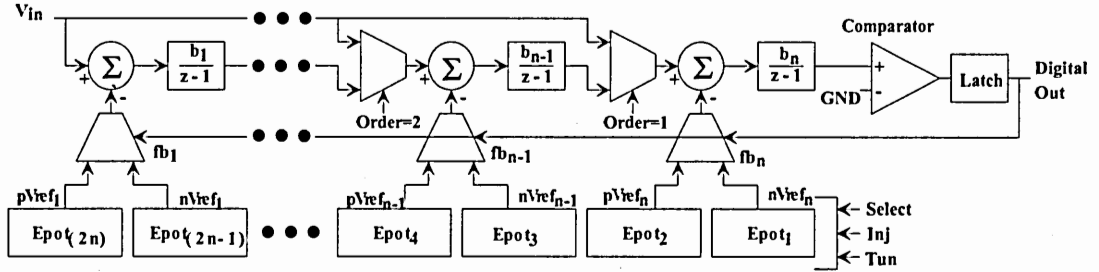
Figure 3: Schematic of the nth order modulator with the 1-bit DACs in the feedback loop replaced by e-pots and associated circuitry. The order of the modulator can be chosen using digital select pins. The digital output determines which e-pot element is in the feedback loop. This approach, currently restricted to tuning the feedback path, can be extended to include variable integrator gains in the forward path.

2.1 *Electronic Potentiometers(e-pots)*

Figure 4 shows the structure of a basic e-pot. E-pots are on-chip, non-volatile analog memory cells with voltage outputs, that can be individually addressed and programmed. The stored voltages can be programmed and held for extended periods of time with low noise and drift. They also have good power supply noise rejection [9, 11]. An e-pot uses the floating-gate of a MOS transistor as a charge storage element. Programming the memory element is done using controlled quantum mechanical phenomena–Fowler-Nordheim tunneling [15] and hot-electron injection through thin SiO_2 [9, 11].

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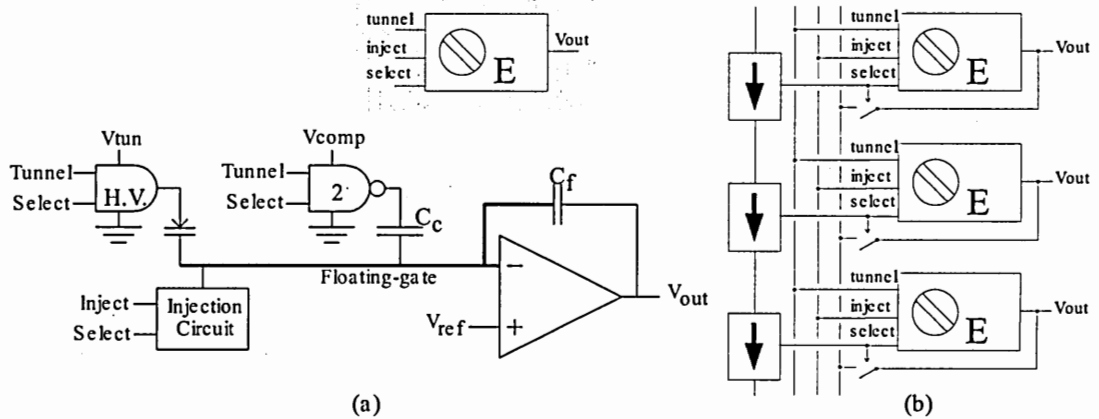
Figure 4: (a) Simplified e-pot structure. (b) Shift register to address each e-pot in an array(Adapted from [9]). The e-pots are fabricated as a regular array structure with additional control circuitry to address and program each of them separately. Each integrator feedback stage requires two e-pots. During programming, the e-pot output voltages are multiplexed onto a single pin to minimize pin count.(Adapted from [11])

Referring to figure 4, the amplifier has its positive terminal connected to an external reference voltage. The negative terminal is a floating-node. Connected to the negative terminal is a pFET transistor for injection, a tunneling capacitor, and a feedback capacitor.

To lower an e-pot's output voltage, electrons are removed from its floating gate by the process of Fowler–Nordheim tunneling. A high voltage V_{tun} is applied to one end of the tunneling capacitor. The other end of the tunneling capacitor is connected to the floating node. The effective energy barrier is lowered so that electrons can tunnel through the gate oxide. To raise the e-pot output voltage, electrons are added to the floating gate using hot-electron injection. A method for pFET injection [11] is shown in figure 5. A high voltage V_{inj} is placed across the source and drain of the injection pFET when the current e-pot is selected with $SELECT$=1 and injection is enabled with $INJECT$=1. The NAND gate is implemented using pseudo-NMOS logic so that

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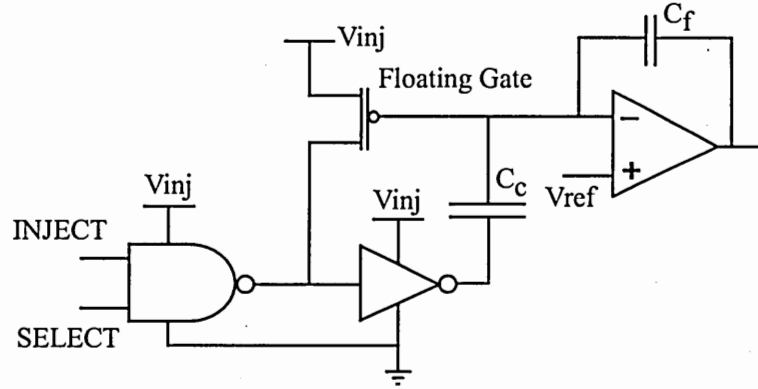
Figure 5: A method for pFET injection. The inverter and capacitor C_c are used to compensate for the capacitive coupling into the floating–gate node through the drain–gate overlap capacitance.

the digital control signals–*INJECT* and *SELECT* do not have to operate at the high V_{inj} voltage level. The gate-source voltage of the pFET is controlled by setting V_{ref} so as to place the pFET in the subthreshold regime. Some of the holes that have diffused across the channel, on entering the high electric field region at the drain are accelerated enough, to launch an impact ionization event. This creates a hole-electron pair. If the kinetic energy of the electron exceeds 3.1eV, the silicon-silicon dioxide energy barrier potential, the electron is injected into the oxide and onto the floating-node [14].

Figure 6 shows the tunneling and injection processes as a function of time. The output falls and rises linearly. V_{comp} is the compensation voltage source. Its function is similar to that of the inverter shown in figure 5. In both tunneling and injection processes, switching on tunneling or injection results in a step change in voltage which capacitively couples onto the floating-gate node and causes an offset in the floating-gate voltage. For tunneling, the tunneling capacitor is itself the coupling mechanism.

11
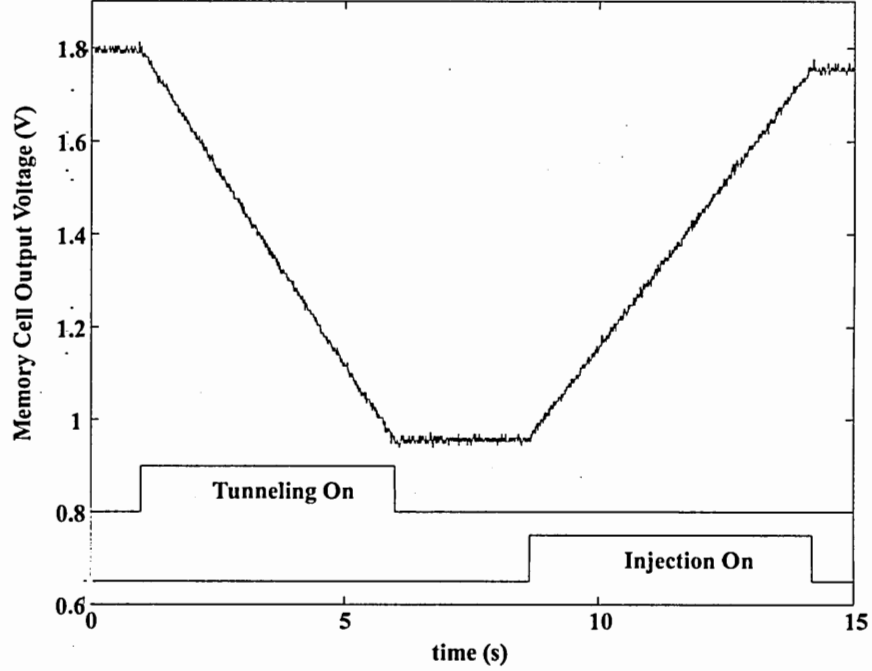
Figure 6: Tunneling and injection processes in an e-pot. Note the linear relation between voltage and time.(Adapted from [11])

For injection, it is a combination of the channel–gate capacitance as well as the drain–gate overlap capacitance. V_{comp} and the compensation capacitors C_c can be chosen to reject the tunneling or injection induced offset for a narrow range of V_{tun} and V_{inj} voltages.

E-pots have been characterized for their noise properties, dynamic range and Power Supply Rejection Ratio(PSRR) [9, 11]. The rms noise voltage at the e-pot output voltage is on the order of 1-2 mV, this number being very similar to other floating-gate amplifiers [12, 13]. It has also been found that tunneling and injection do not contribute significantly to the noise [12]. The dynamic range has been found to be approximately 84 dB (14 bits), using a 5V supply with 4V linear range, and typical C_f capacitors of 2pF at room temperature (T=300K). The PSRR of the e-pots is 39 dB.

12

Table 1: EPOT parameters in a $0.5\mu m$ CMOS process.(Adapted from [11])

Parameter	Value
1/fnoise	$3.6\mu V/fsqrtHz$
Thermal noise	$2.2\mu V/\sqrt{Hz}$
α	$0.034V/°C$
Injection rate	150mV/s
Tunneling rate	410mV/s
DR(5V supply)	84 dB(14 bits)
PSRR	39 dB

The primary contribution to the PSRR degradation is from the amplifier [9, 11].

E-pot voltage references exhibit temperature dependence [9](see Table 1). The temperature coefficient α is significant. From a performance perspective a 10°C temperature change could result in nearly 340mV change in each e-pot and hence nearly 680mV of mismatch for a pair of e-pots used in the same modulator stage. This could be a serious drawback of this architecture, since the modulator does not have compensation (such as that used in bandgap references). However, direct SNR measurements on the modulator at room temperatures indicate much better stability of e-pot outputs than predicted by prior measured data. One possible explanation could be that the prior data [9] was obtained by setting the bias voltages of the device under test using potentiometers. General purpose potentiometers typically do not have very good temperature stability. The overall temperature variation of the e-pot voltages in these experiments could have been influenced by the potentiometers. In the present test setup all bias voltages are set by commercially available IC Digital-to-Analog converters such as the 10-bit MAX5250 and the 12-bit MAX536 from MAXIM Semiconductor, followed by low-pass filters. Nevertheless, for high performance data

converters, the temperature stability of floating-gate elements is a critical requirement and needs further investigation.

2.2 E-pots in a Programmable Δ-Σ Modulator

The e-pots used in the modulator are fabricated as a linear array. The *Select* digital input shown in figure 4(a), is used to turn the tunneling or injection process on/off on an addressed e-pot. The addressing mechanism for the e-pot array consists of a shift register and a synchronization output. A logic '1' is shifted through the register, on the rising edge of a clock signal. Tunneling/Injection are enabled only on the e-pot in whose position the '1' currently resides. The sync output goes high whenever the '1' is scanned past the last e-pot of the array. The *Tunnel* input starts/stops the tunneling operation on the currently addressed e-pot. Similarly, the *Inject* input starts/stops the injection operation.

As seen in figure 3, each integrator stage has two e-pot outputs connected to the feedback path through a two-input analog multiplexor. When the modulator operates, depending on the instantaneous polarity of the latched digital output, one of the e-pot outputs is switched into the feedback path.

CHAPTER III

SYSTEM MODELS

Transistor level analysis of Δ-Σ modulators is tedious and time consuming. Several methods have been advocated to capture the performance of $\Delta - \Sigma$ modulators at a higher level of abstraction [5, 19, 21]. The transform domain approach on a linearized modulator system is the simplest. A linear model of a second-order modulator is shown in figure 7. The quantization noise is modelled as an additive white gaussian noise source, uncorrelated with the input signal and placed before the quantizer. A 1-bit quantizer is essentially a comparator and therefore responds to the sign of its input alone. In the linearized system, it is abstracted as a variable gain block, the gain k varying as a function of the amplitude of the quantizer input. Two independent input variables can be identified – the quantization noise source (N) and the input signal source (X). Therefore two transfer functions can be computed in the z-domain, the *Noise Transfer Function* (NTF) and the *Signal Transfer Function* (STF) respectively.
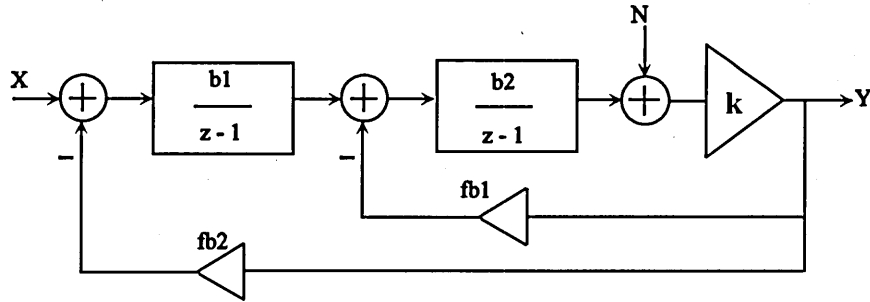
Figure 7: Transform domain model of a second order modulator.
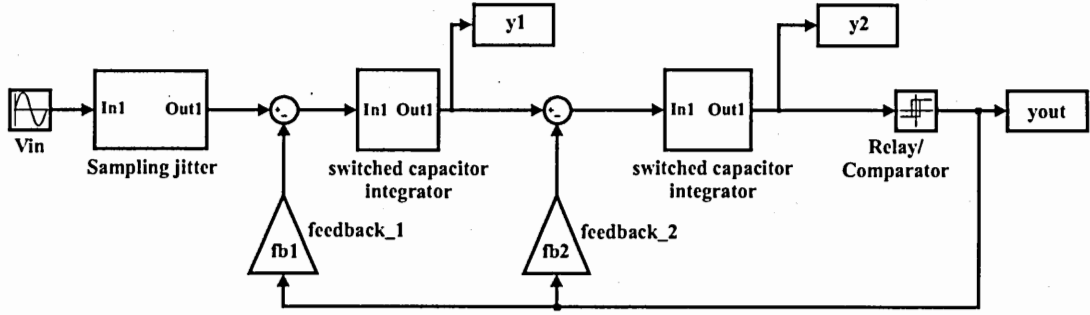
Figure 8: Schematic of a typical second order modulator system model implemented in SIMULINK. The model can be run directly or invoked using MATLAB commands. Results are available as variables in the MATLAB workspace and can be post-processed using built-in functions.

For a second order modulator the two transfer functions can be computed in terms of gain k, integrator gains b_1 and b_2 and feedback coefficients fb_1 and fb_2 as below.

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{k \cdot b_1 \cdot b_2}{(z-1)^2 + (z-1) \cdot k \cdot b_2 \cdot fb_2 + k \cdot b_2 \cdot b_1 \cdot fb_1} \quad (6)$$

$$NTF(z) = \frac{Y(z)}{N(z)} = \frac{k \cdot (z-1)^2}{(z-1)^2 + (z-1) \cdot k \cdot b_2 \cdot fb_2 + k \cdot b_2 \cdot b_1 \cdot fb_1} \quad (7)$$

It is desired that the STF pass signals in the bandwidth of interest unaltered, and the NTF attenuate quantization noise in the same frequency range. The design variables are the integrator gains $- b_i$ and the feedback coefficients $- fb_i$. The design variables can be used to place the poles appropriately (Note that the location of zeroes in the chosen topology is fixed at z=1). It must be appreciated that the pole locations are a function of the quantizer gain k. Hence to maintain stability it must be ensured that the poles lie within the unit circle over all values of k. In practice however, it is more difficult to keep the modulator stable at small values of k. This situation corresponds to a large amplitude integrator output causing overload.

The transform approach is primarily a frequency domain tool. It is not amenable

to including circuit level information such as the non-ideal behavior of op-amp integrators. Simulation of initial conditions and observation of the evolution of the output over time is not possible either. Another major drawback is the inability to predict stability of higher-order modulators.

Therefore, for fast design, but with better reliability than transform approach, time domain behavioral models have been proposed in [5, 19]. In this work, a SIMULINK model based on equations describes various modulator blocks as well as their non-ideal behavior and calculates the optimal feedforward and feedback coefficients. The following effects are considered – finite gain, gain-bandwidth, slew rate, saturation voltage and input referred noise V_{ni} of op-amps, clock jitter, clock and channel charge feed-through and the $\frac{kT}{C}$ noise due to switches. For simplicity, e-pots are modelled as ideal sources. A more accurate model would account for circuit behavior of e-pots (such as noise). The system model implementation of a second-order modulator in SIMULINK is illustrated in figure 8. This model can be extended to higher order modulators by adding integrators and feedback coefficients. However analysis and optimization for higher order modulators could be complicated by the large number of permutations of the design variables that are possible.

3.1 Clock Jitter

The sampling precision is degraded by the clock jitter, clock feed-through, channel charge feed-through and thermal noise voltage due to switches. Sampling clock jitter results in the input signal not being sampled at regular intervals. For sinusoidal

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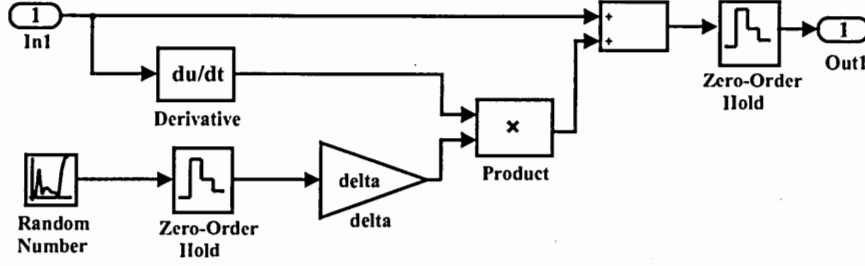
Figure 9: Clock jitter model implemented using SIMULINK constructs. Zero order hold block is an abstraction for an ideal sample-and-hold circuit.

inputs $Asin(\omega t)$, the error $e(t)$ introduced can be estimated as in [5] as

$$e(t) = x(t + \delta) - x(t) = A[sin(\omega t + \delta) - sin(\omega t)] \approx A\delta \omega cos(\omega t) \tag{8}$$

which can be rewritten as

$$e(t) = \delta \frac{d}{dt}[Asin(\omega t)] \tag{9}$$

where δ represents the uncertainty in sampling instant, A the amplitude of the input signal and ω the angular frequency. δ is modelled as a Gaussian random variable. The sampled value at an instant $t = nT$ may be written as

$$\hat{x}(nT) = x(nT) + e(nT) \tag{10}$$

The SIMULINK model of the clock jitter is shown in figure 9. It can be shown that if $\sigma(\delta)$ is the standard deviation of the sampling uncertainty, BW is signal bandwidth, and M is the oversampling ratio, then the modulator sensitivity to the clock jitter [8] is expressed as

$$SNR = -20log_{10}\left[\frac{2\pi BW\sigma(\delta)}{\sqrt{(M)}}\right] \tag{11}$$

18
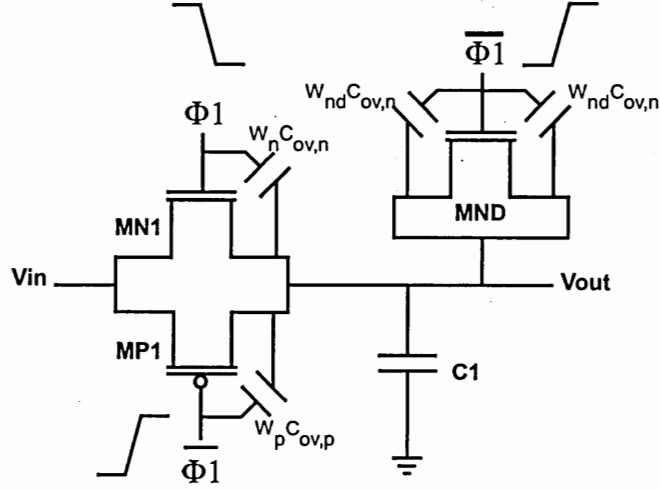
Figure 10: Switch circuit used in SC integrator (sampling phase).

3.2 Clock Feedthrough and Channel Charge Injection

Two effects are considered in this section–clock feedthrough and channel charge injection, both of which result in an error voltage imposed on the sampling capacitor. Before describing the models, it is critical to remind the reader that modelling these effects precisely in an analytic manner is an intractable problem [1]. The models presented here are simplistic and only represent the qualitative information about the underlying processes at work. At the time of writing this document it was brought to the attention of the author that a more rigorous treatment of these effects is found in [1].

The clock transitions are coupled to the sampling capacitor through the parasitic overlap capacitances of the transistor switches. As a result, an offset error voltage is stored on the sampling capacitor. Consider the error voltage magnitude imposed on the sampling capacitor C_1, when switches of widths W_n and W_p are used as in

figure 10.

$$\Delta V = V_{clk} \left[\frac{W_n C_{ov,n}}{C_T} - \frac{W_p C_{ov,p}}{C_T} \right] \qquad (12)$$

where $C_T = W_n C_{ov,n} + W_p C_{ov,p} + C_1$ is the total capacitance at the sampling node, V_{clk} is the magnitude of the clock pulse and $C_{ov,n}$ and $C_{ov,p}$ represent the overlap capacitance per unit length associated with nFET and pFET transistors respectively. This error can be reduced using a series connected dummy switch, with source and drain short-circuited [25] and fed by a clock phase of opposite polarity to the main sampling switches. When *MN1* and *MP1* turn off, *MND* turns on and induces a voltage change of opposite polarity on C_1 through its coupling capacitance $2W_{nd}C_{ov,n}$. This concept is illustrated in figure 10.

The choice of width of W_{nd} to cancel out clock feedthrough effect can be determined as follows. Assume lengths of all switches to be identical. For convenience assume $C_{ov,n}=C_{ov,p}$. From linearity considerations it is practical to choose the aspect ratios of the input switches MN1 and MN2 as,

$$\frac{W_n}{W_p} = \frac{\mu_p}{\mu_n} \qquad (13)$$

From the analysis in [25] we have for $\Delta V=0$

$$2C_{ov,n}W_{nd} = W_n C_{ov,n} - W_p C_{ov,p}$$
$$W_{nd}C_{ov,n} = 0.5 W_n C_{ov,n} \left(\frac{W_p}{W_n} - 1 \right)$$
$$W_{nd} = 0.5 \left(\frac{\mu_n}{\mu_p} - 1 \right) W_n \qquad (14)$$

When a switch (nFET or pFET) is turned off, the channel charge redistributes itself towards the input source or towards the sampling capacitor in a non-deterministic

20

manner. This phenomenon of charge injection may be mitigated by using complementary MOS switches (as shown in figure 10). The principle used is that when the switches turn off, opposite charge packets injected by the nFET and pFET devices cancel each other. However, since the charge injection has an input signal dependence as shown in (15), the cancellation is effective for only one input level. The signal dependent error is included via (15) in the model. The switches are sized such that $W_pL_p=W_nL_n$.

$$\Delta V = \frac{W_pL_pC_{ox}(V_{in} - V_{Tp}) - W_nL_nC_{ox}(V_{DD} - V_{in} - V_{Tn})}{C_1} \tag{15}$$

3.3   Thermal Noise

Consider the stray insensitive SC integrator shown in figure 11. There are four switches corresponding to the two non-overlapping clocks phases Φ_1 and Φ_2. Non-ideal switches cause a thermal noise voltage to be sampled in addition to the input signal. If $R_{on,eq}$ is the non-linear resistance of the switches in series with the sampling capacitor C_1, then the mean-square noise voltage $4kTR_{on,eq}\Delta f$ due to the switches is band-limited by C_1 to $\overline{v_n^2} = \frac{kT}{C_1}$. If the noise is assumed to be white, and spread over the frequency range 0–$\frac{f_s}{2}$, then over-sampling by a factor M would reduce the baseband noise to $\frac{kT}{MC_1}$ [5], since the signal bandwidth is now restricted to $\frac{f_s}{2M}$. If the effect of the integrating capacitor C_2 is included, then the total mean-square noise voltage is $\overline{v_n^2} = \frac{kT}{MC_1}(1+b)$, where b $= \frac{C_1}{C_2}$.
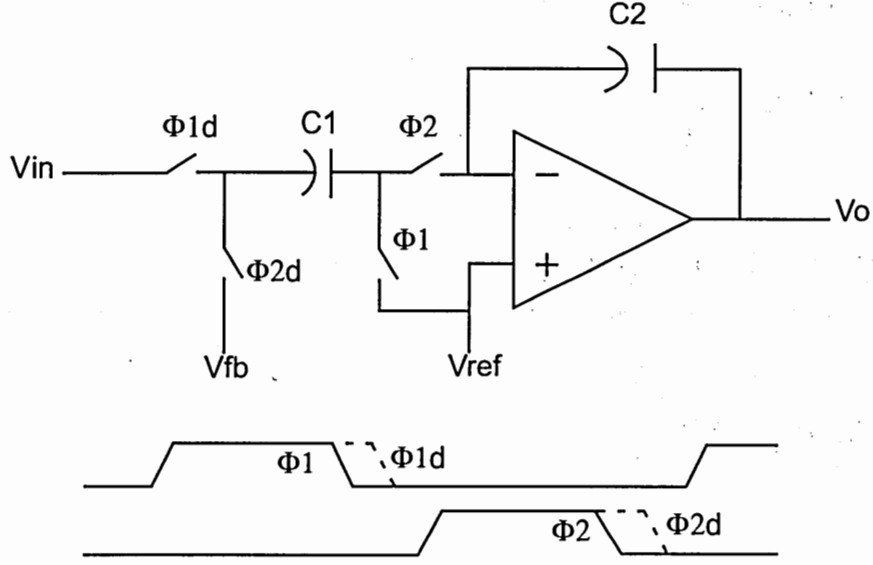
Figure 11: Schematic of stray-insensitive SC integrator with sampling-ϕ_1 and integrating-ϕ_2 clock phases indicated. The delayed clock phases ϕ_{1d} and ϕ_{2d} are used to reduce charge feed-through errors.

3.4 Integrator Op-amp Parameters

The open-loop gain, slew rate, bandwidth and equivalent input noise of the integrator op-amp can be obtained from SPICE simulations. The rms output noise of an op-amp over a given bandwidth can be referred back to its input as a noise source–V_{ni}, in series with the input. Since the ADC is a sampled data system, the total noise estimate must include the contribution from the high-frequency op-amp noise folding into the baseband due to sampling.

The output stage of the op-amp places limits on the signal swing. A saturation block in the integrator model restricts the output to $\pm V_{sat}$ around the mid-supply voltage, where $V_{sat} = kV_{DD}, (k < 1)$.

The finite gain of the op-amp affects integrator performance. The transfer function

of an ideal integrator with gain b can be expressed as

$$H(z) = \frac{bz^{-1}}{1 - z^{-1}} \qquad (16)$$

In the SC integrator shown in figure 11 the finite gain$-A_v$ of the op-amp modifies (16) in two ways. First, the ideal transfer function is modified to

$$H(z) = \frac{bz^{-1}}{1 - \alpha z^{-1}} \qquad (17)$$

To obtain α,

$$H(z = 1) = \frac{b}{1 - \alpha} = A_{v,opamp}(\omega = 0) \qquad (18)$$

The time-domain equation modelling this behavior is

$$y[n] = bx[n-1] + \alpha y[n-1] \qquad (19)$$

Second, during the integrating phase, the SC integrator behaves like a charge amplifier with a nominal gain of $b = C_1/C_2$. It can be shown that b is modified to

$$b' = \left| \frac{V_o}{V_i} \right| \approx \left[\frac{C_1}{C_2} \right] \left[1 - \frac{C_1 + C_2}{C_2 A_v} \right] = b \left[1 - \frac{1+b}{A_v} \right] \qquad (20)$$

The above equations are included in the integrator model shown in figure 12.

3.5 Time-Domain Response of SC Integrator

An important consideration in the behavioral model is the evolution of the integrator output. The analysis presented in [19] is modified to include the finite gain parameter α. The integrator response depends on the bandwidth and slew rate of the op-amp. For convenience a 50% duty cycle for the sampling and integrating phases is assumed. Let the nth integration phase stretch over $(nT - \frac{T}{2} < t < nT)$. Let the input sample

23
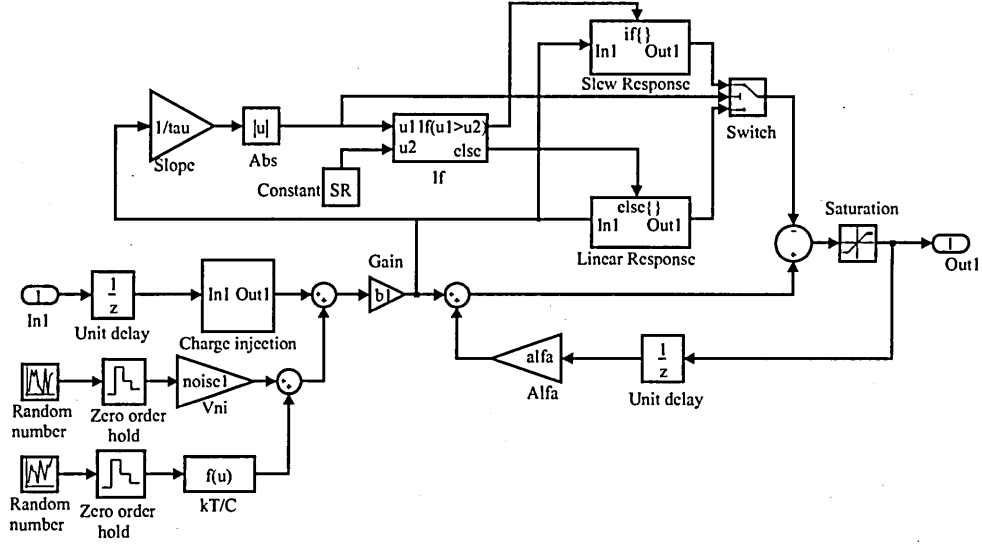
Figure 12: Integrator model representation in SIMULINK.

just prior to the start of this phase be denoted by V_{is}, i.e. $V_{is} = V_{in}(nT - T/2)$.

Assume the op-amp has a single dominant pole. Then output in the nth integration

phase is of the form,

$$v_o(t) = \underbrace{\alpha v_o(nT - T)}_{\text{previous cycle output after leakage}} + \underbrace{bV_{is}(1 - e^{\frac{-t}{\tau}})}_{\text{linear response term}} \tag{21}$$

where the time constant τ is $\frac{1}{2\pi UGBW}$. UGBW denotes the unity-gain bandwidth of

the integrator op-amp, α is defined in (18) and $b = C_1/C_2$. $v_o(t)$ has maximum slope

at $t = 0$,

$$m = \frac{d}{dt} v_o(t)|_{t=0} = b \frac{V_{is} e^{\frac{-t}{\tau}}}{\tau}|_{t=0} = b \frac{V_{is}}{\tau} \tag{22}$$

If the op-amp slew rate $SR \leq m$, then the output slews initially and then acquires a

linear response. The duration $t = t_0$ of slew can be computed as the time at which

the output slope equals SR.

$$\frac{bV_{is}}{\tau} e^{\frac{-t_0}{\tau}} = SR \Rightarrow \frac{bV_{is}}{SR} = \tau e^{\frac{t_0}{\tau}} = \tau \left[1 + \frac{t_0}{\tau}\right] \Rightarrow t_0 = b \left[\frac{V_{is}}{SR}\right] - \tau \tag{23}$$

24

The output at the end of the slewing period maybe written as,

$$v_o(t_0) = \alpha v_o(nT - T) + SRt_0 \tag{24}$$

Combining the slewing response term (24) with the linear response term in (21) the total response is given by

$$v_o(t) = \alpha v_o(nT - T) + bV_{is} + (SRt_0 - bV_{is})e^{-\frac{t-t_0}{\tau}} \tag{25}$$

Substituting for t_0, we get

$$v_o(nT) = \alpha v_o(nT - T) + bV_{is} - sgn(V_{is})SR\tau e^{-\left(-\frac{T}{2\tau} - \frac{bV_{is}}{SR\tau} + 1\right)} \tag{26}$$

In the above derivation, the positive and negative slew rates of the op-amp, SR^+ and SR^- are assumed identical. In a real op-amp the positive and negative slew rates may be asymmetrical, but a good design can keep this asymmetry small.

Figure 12 shows the SIMULINK implementation of the integrator model discussed. Note the use of a time domain construct implementing an *if-then* clause to realize a linear or slewing response. Also note the implementation of integrator gain leakage, saturation and input referred noise terms.

3.6   System Modeling Results

Table 2 shows specific values for various circuit and process level parameters in the model. The parameters used in the integrator model are indicated Table 3. These values are deliberately pessimistic as compared to results from circuit level simulations shown in chapter 4, so as to provide sufficient design margin. Optimal coefficients for a second order modulator are obtained by iterative search and listed in Table 4. The

Table 2: General parameters for a second order modulator system model. Process parameters are specified for $0.5\mu m$ CMOS. L_{mos} is the gate length for switches.

Parameter	Value	Parameter	Value
V_{DD}	± 2.5 V	L_{mos}	$0.6\mu m$
C_{ox}	$2.45fF/\mu m^2$	Bandwidth	4kHz
V_{Tn}	0.7 V	$|V_{Tp}|$	0.91 V
F_s	2.048 MHz	OSR	256

Table 3: Integrator model parameters for a second order modulator. SR, UGBW, V_{ni} are op-amp slew-rate, gain-bandwidth and noise parameters.

Parameter	Value	Parameter	Value
b_1	0.4	b_2	0.8
α_1	0.9996	α_2	0.9992
V_{sat}	$0.9\ V_{DD}$	$A_v(0)$	60 dB
$UGBW = 1/2\pi\tau$	30 MHz	$\sqrt[2]{v_{ni}^2}$	$10\mu V$ (rms)
SR	20 V/μs	C_{sample}	1pF

loop coefficients obtained by iterative search, satisfy $fb_2 \geq 1.25fb_1$, $0.1 \leq b_1 < 0.8$ for stable operation, as described in [8]. The iterative search procedure used to find the optimal coefficients is described below.

1. Initialize process and circuit parameters for the model.

2. Define a suitable amplitude level, frequency for the analog input.

Table 4: SIMULINK model results for a second order modulator.

b1– First Integrator Gain	0.4
b2– Second Integrator Gain	$0.1 - 0.8$
fb1– First Integrator Feedback	0.4
fb2– Second Integrator Feedback	0.5
SNR [dB]– Signal to Noise Ratio	98.45
OL [V]– Input Overload Level	0.6551
DR [dB]– Dynamic Range	100.82
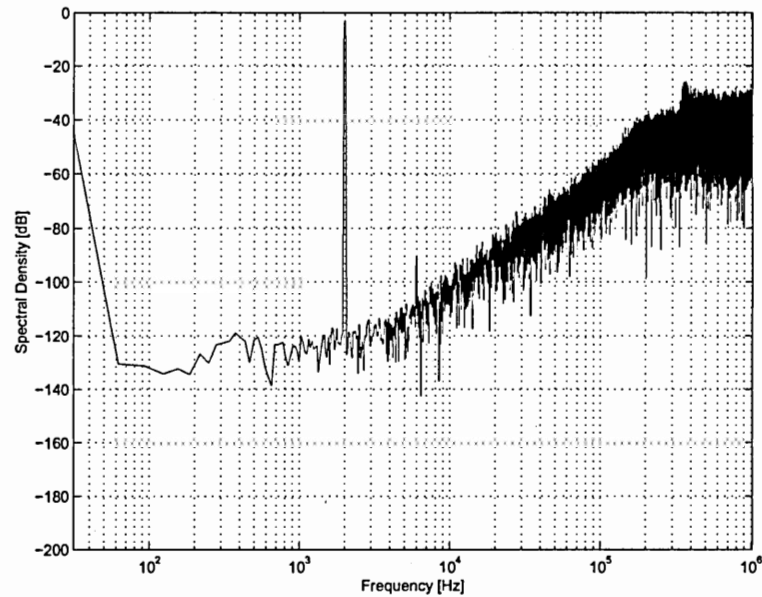
Figure 13: Full spectrum plot of second order modulator output.

3. Constrain all coefficients to lie in the range 0.1 to 0.9. Constrain the step in every coefficient value to be 0.1.

4. Use a nested loop structure to execute the model for all combinations of the coefficient values.

5. Determine the best 20 coefficient vectors (b_1, b_2, fb_1, fb_2) using SNR as the criterion.

6. For each of the chosen 20 vectors re-run the model varying the input amplitude to measure dynamic range and overload level (The overload level is the input amplitude at which the SNR starts drooping after reaching a peak).

7. Choose the vector(s) that give highest SNR, widest dynamic range and highest overload level.
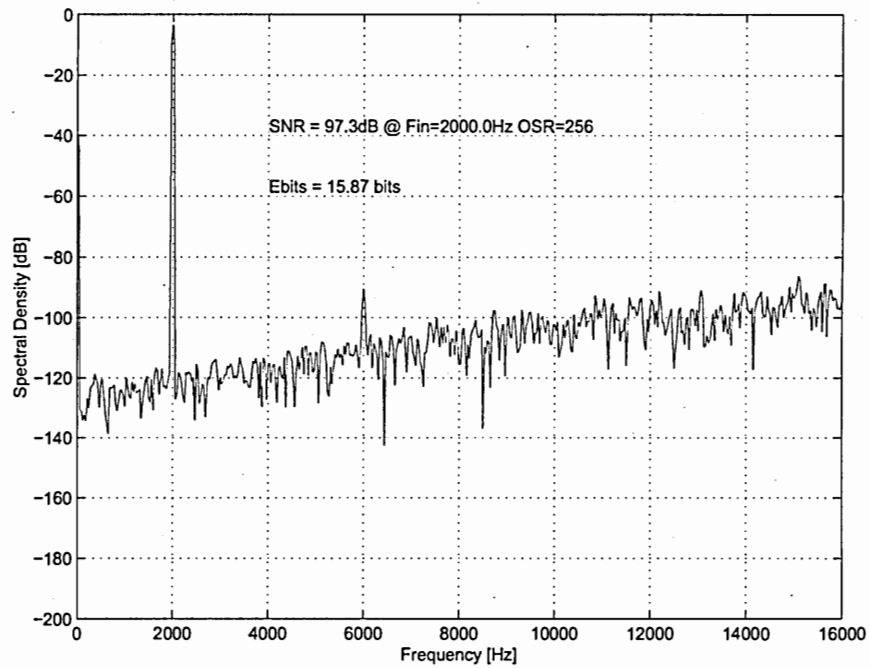
Figure 14: Magnified view of the bandwidth of interest from figure 13
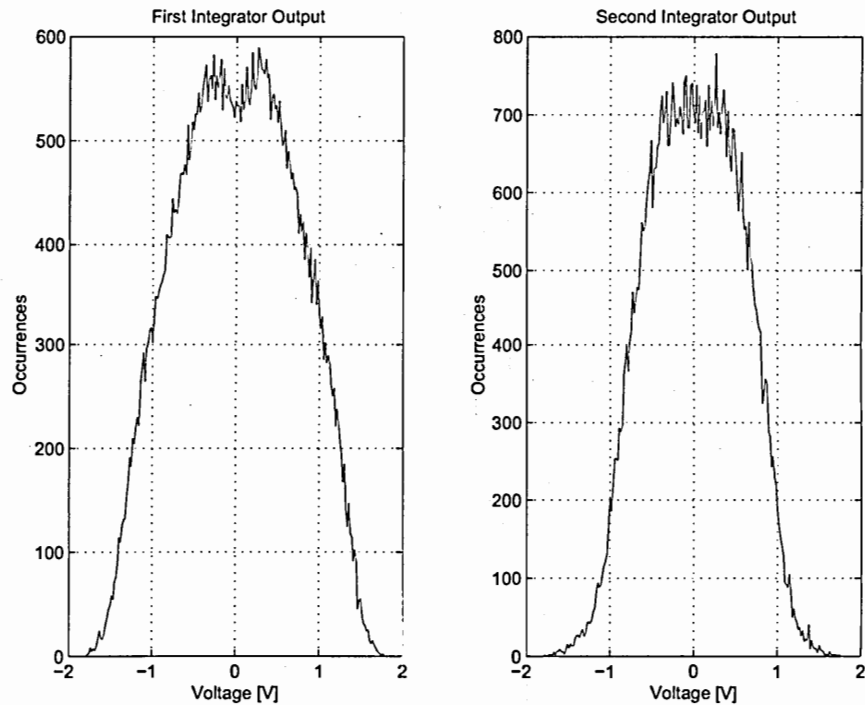
Figure 15: Second order modulator, integrator output histogram.

Table 5: Measured time complexity of behavioral model routines

Operation	Average time(MEX)	Average time(w/o MEX)
SNR	0.044 min	0.24 min
SNR & Spectrum Plot	0.12 min	0.35 min
DR (100 points)	4.75 min	24.25 min

8. Coefficient values are refined further by repeating above steps with coefficient vectors around the coarse optimum and reducing the step size.

An interesting observation made during the course of the behavioral model development effort, was the speed-up given by converting most of the optimization code from MATLAB M-file format to a C-like compiled form called the MEX format. This observation is documented in this work in Table 5. The table lists the average time required for performing an operation for a given coefficient vector. The ability to predict the performance of the modulator for a given set of coefficients as well as the ability to do it quickly is a definite advantage to any designer.

Figures 13 and 14 show example plots of the SNR obtained in behavioral simulation. Peak SNR obtained in figure 14 is $\approx$97 dB. The zoomed-in view in figure 14 indicates the presence of the third harmonic in the output spectrum. The integrator histograms are shown in figure 15. The integrators do not get overloaded for the optimal coefficients chosen.

CHAPTER IV

CIRCUIT DESIGN AND SIMULATIONS

This chapter discusses the design of the modulator as well as its sub-circuits. The top level circuit schematic for a second order modulator is shown in figure 16. The circuit consists of two switched–capacitor integrators, comparator, latch and two analog multiplexors.

4.1 Integrator and Switch Design

The SC integrators are the critical blocks of the modulator. It is well-known that the linearity and noise of the integrator closest to the input determines overall performance to a large extent. A balanced-cascode op-amp (see figure 17) with load compensation, is used for all integrators. The input differential pair aspect ratio is
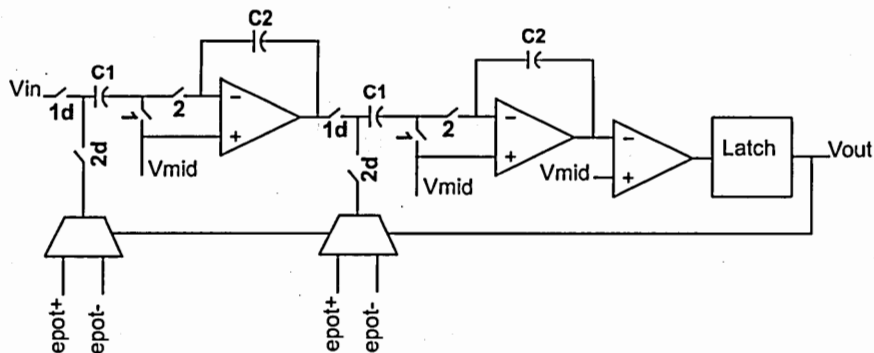
Figure 16: Circuit schematic of second order modulator.

Figure 17: Op-amp used in SC integrator. Circuit schematic of balanced-cascode topology.

Table 6: Aspect ratios of integrator op-amp transistors.

Device	W	L
M0	117	1.2
M1, M2	40.8	1.2
M3, M4, M5, M6, M7, M8	33.6	1.5
M9, M10, M11, M12	8.40	1.2

made large to reduce the input-referred noise. The transonductance of the load transistors is lowered by using longer devices for the same purpose. The symmetry of this topology is expected to reduce the systematic offsets. The first stage gain is low due to the low output impedance of the diode connected load transistors. The gain can be improved by increasing the length of the load devices. The gain is recovered by using cascodes in the output stage. The op-amp has a class-AB output stage giving it symmetric slewing properties. The designed aspect ratios for the op-amp are shown

Figure 18: Bias circuit for the integrator op-amp. Current reference IREF is external to the chip.

Table 7: Aspect ratios of bias circuit transistors.

Device	W	L
MN1, MN2, MN3, MN4	117	1.2
MN5, MN6	2.4	1.2
MP1, MP2, MP3, MP4	33.6	1.5
MP5	8.1	1.5

in Table 6. The bias circuit to set V_{pc}, V_{nc} and *Biasop* is shown in figure 18. The aspect ratios of the bias circuit devices are indicated in Table 7. Figure 11 in chapter 3 shows the block diagram of the stray-insensitive integrator built using the op-amp above. The SPICE simulation results for the op-amp are summarized in Table 8.

Switch design is governed by sizing for linearity, charge-injection and speed considerations. The SC integrator employs the bottom-plate sampling technique to minimize signal dependent charge injection. This is achieved through delayed clock phases Φ_{1d} and Φ_{2d}. In figure 16 when the switches labelled **1** are turned off, the charge injection from these switches remains to a first order approximation, signal independent.

Table 8: Post layout simulation results of integrator op-amp. $I_{tail} = 40\mu A$. All parameters measured with $C_L = 1.5pF$. Noise is computed over $0 - 10$ kHz with folding noise contribution included.

Parameter	Value	Parameter	Value
Gain	85.59 dB	UGBW	41.55 MHz
SR^+	47.0 V/μs	SR^-	38.9 V/μs
PM	53.85°	$\sqrt[2]{v_{ni}^2}(rms)$	1.0518 μV

Now with one plate floating, turning off the switches labelled 1d a little later does not introduce any signal dependent charge-injection errors.

CMOS switches are used in the SC integrator. The switches labelled 1d are connected directly to the input and are sized for linearity, i.e. equal R_{on} for the pFET and nFET. Hence the pFET aspect ratio is made larger than that of the nFET by a factor μ_N/μ_P. The bottom-plate switches labelled **1** are sized for partial cancellation of charge-injection errors as $W_N L_N = W_P L_P$. This choice of aspect ratios also serves to cancel clock feedthrough errors due to gate-drain overlap capacitances.

It has been shown that for best speed-precision tradeoff [25] minimum L switches are to be used. With L fixed, increasing the width decreases the resistance but increases the parasitic capacitance of the sampling network. An optimum width is to be found that satisfies linearity and speed considerations.

From the above criteria the designed values for input and bottom-plate switches are listed in figure 19.

4.2   Comparator and Latch Design

The design constraints for the comparator in a $\Delta - \Sigma$ modulator are relaxed, since the non-idealities undergo noise-shaping. Hence there is no need for a pre-amplifier or
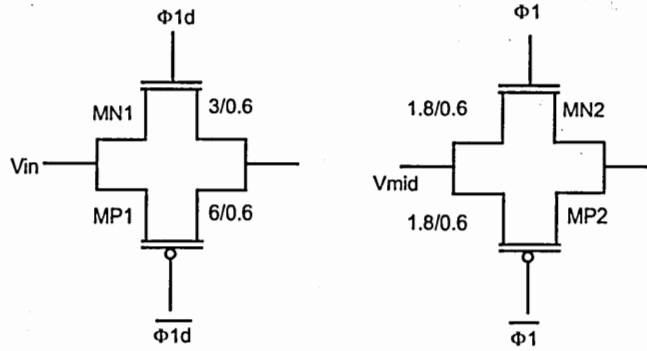
Figure 19: Aspect ratios of sampling switches.
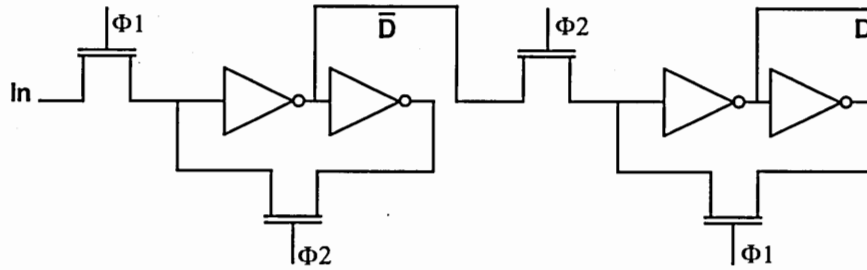
Figure 20: Master-Slave flip-flop realized using pseudo-static latch.

offset cancellation circuit. In this work we use an open-loop op-amp that is designed for use in the integrators.

A master-slave flip-flop, implemented using pseudo-static latch [24] is used to clock the modulator bit stream for external measurements as well as internal feedback. Figure 20 shows the schematic of the flip-flop. The flip-flop was chosen because of its simplicity as well as its requirement of non-overlapping clocks, which are already available in this circuit. The analog multiplexors in figure 16 are implemented using transmission gates.
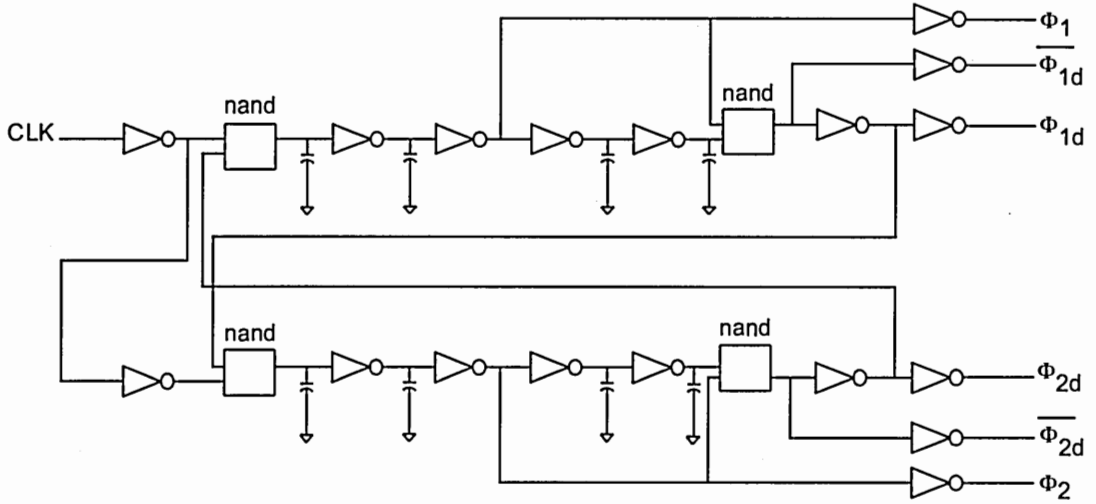
Figure 21: Schematic of the clock generator that generates the non-overlapping clock phases. The capacitors (500fF) are used to increase the non-overlap period.
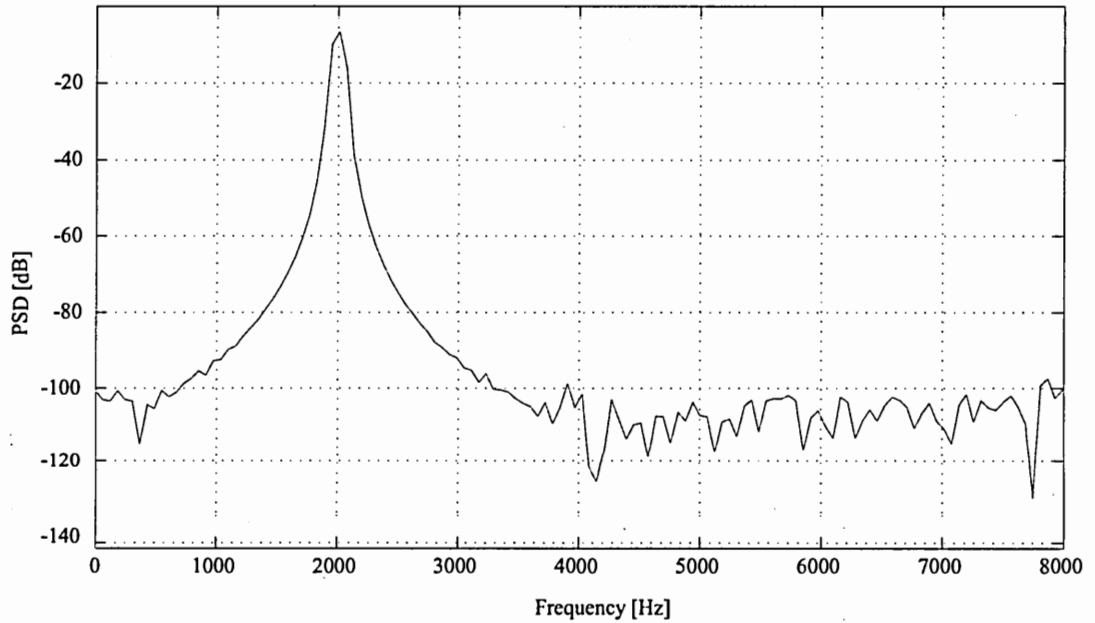
Figure 22: Second order modulator baseband spectrum plot. SNR=85.9 dB at OSR=256 BW=4kHz(SPICE).

4.3   Clocking Scheme Design

An on-chip circuit [6] generates the clock phases shown in figure 11 and figure 16. The circuit generates the non-overlapping clock phases Φ_1 and Φ_2 as well as the delayed

35

clock phases Φ_{1d} and Φ_{2d} used to reduce charge injection errors.

The schematic is shown in figure 21. The capacitors shown in the schematic, increase the load on the gates and thereby the propagation delay. This helps to increase the non-overlap period between the phases.

4.4 *Simulation Results*

SPICE simulations for input sinusoid at -1dB below overload level of 0.65V obtained in SIMULINK, gave SNR=85.9dB for a BW=4kHz and over-sampling ratio(OSR)=256. For an input signal of amplitude -1dB below the overload level computed by the behavioral model, a plot of the FFT spectrum is shown in figure 22.

CHAPTER V

EXPERIMENTAL MEASUREMENTS ON

SECOND AND THIRD ORDER MODULATORS

The IC prototype is fabricated in a 0.5μm CMOS process with a scalable architecture up-to 4th order. Experimental results are shown for a second-order modulator.

5.1 Experimental Setup

The custom test setup is shown in figure 23. The Stratix FPGA from Altera and the Nios development board form the core of the setup. The FPGA is loaded with VHDL modules including a 32-bit Nios processor, PLL, SPI interface, TRIMATRIX on-chip memory and custom data sampler block. C functions have been written for the Nios processor to handle tasks such as transferring data and commands between the host PC and the FPGA board, initializing the modulator test board, navigating and monitoring e-pot outputs and controlling tunneling and injection processes. The compiled and linked C code is downloaded onto static RAM (SRAM) blocks on the Nios development board. MATLAB 6.5 has built-in support for the ethernet protocol. Hence the C functions resident on the SRAM can be invoked using a MATLAB interface via ethernet.

The FPGA I/Os operate at 3.3V rails. The low-jitter PLL output of the FPGA provides the external clock input to the modulator. The PLL frequency is chosen to
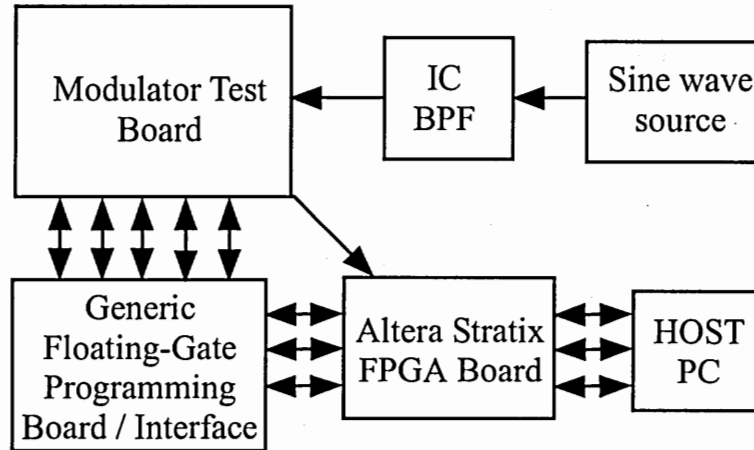
```
┌─────────────────┐      ┌──────────┐    ┌────────────┐
│ Modulator Test  │◄─────│   IC     │◄───│ Sine wave  │
│     Board       │      │   BPF    │    │  source    │
└─────────────────┘      └──────────┘    └────────────┘
   ▲ ▲ ▲ ▲ ▲  \
   ▼ ▼ ▼ ▼ ▼   \
┌─────────────────┐  ┌──────────────┐   ┌──────────┐
│    Generic      │◄►│              │◄► │          │
│ Floating-Gate   │◄►│Altera Stratix│◄► │  HOST    │
│  Programming    │◄►│  FPGA Board  │◄► │   PC     │
│Board / Interface│  └──────────────┘   └──────────┘
└─────────────────┘
```

Figure 23: Custom test setup to evaluate modulator performance-an Altera Stratix FPGA development board that executes e-pot programming and data sampling routines. The modulator prototype is located on a custom 4 layer PCB with separate analog and digital ground planes. The FPGA interfaces with the PC using a ethernet link. The FPGA controls the generic board and also sets up external bias voltages to the prototype.

be 2 MHz. The clock is level-shifted to 5V rails using a 74ACT541 IC level shifter. Ringing on the clock line at transitions, caused by trace inductance and capacitance is damped by adding a small series resistance (100 ohm).

A copy of the PLL clock that feeds the modulator is internally provided to the custom data sampling block on the FPGA. The sampler reads in 1-bit data on the falling edge of the clock. The falling edge is chosen for sampling because (1) The modulator output is produced at the rising edge of the clock. It has nearly half a clock period to settle. (2) Clock skew on the board does not affect the sampling.

A 512k long stream of modulator 1-bit samples is stored on the FPGA on-chip TRIMATRIX memory in the form of 8-bit words. Sampled output data is transferred to the PC via ethernet. To minimize spectral leakage, the data is sampled coherently [18] and a four term Blackman–Harris window function [8] is employed on the sampled data before generating an FFT in MATLAB. The B–H window is chosen
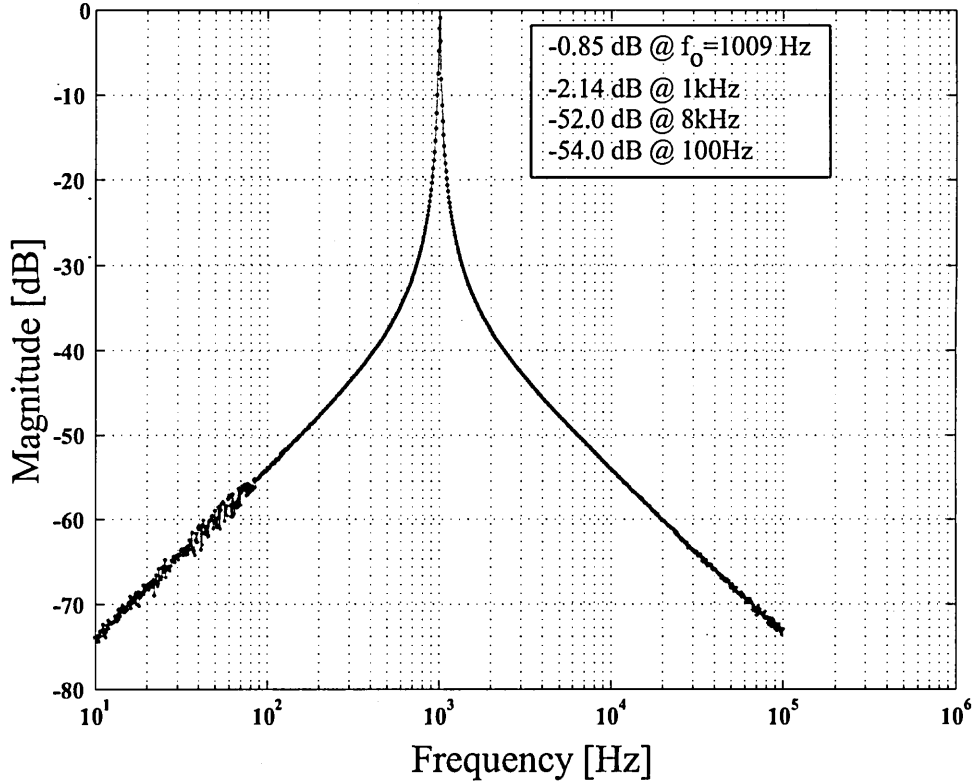
Figure 24: Measured magnitude response of IC input bandpass filter.

because the largest leakage component is below -92 dB and the SNR degradation due to the window is less than 3.8 dB [8].

All measurements are made using a 1kHz sinusoidal input. To improve the frequency selectivity of the input signal, an IC second-order bandpass filter(Q=50) MAX274 from MAXIM Semiconductor is employed after the function generator. This filter is tuned to 1kHz with near 0 dB attenuation at the resonant frequency. The measured response of the filter is shown in figure 24. Actual center frequency is 1009 Hz, with attenuation of −0.85 dB. Attenuation at 1kHz is −2.14 dB. Attenuation at the band edges is ≈−52 dB.

The minimum amplitude of the function generator output is only 10mV$_{pp}$. To
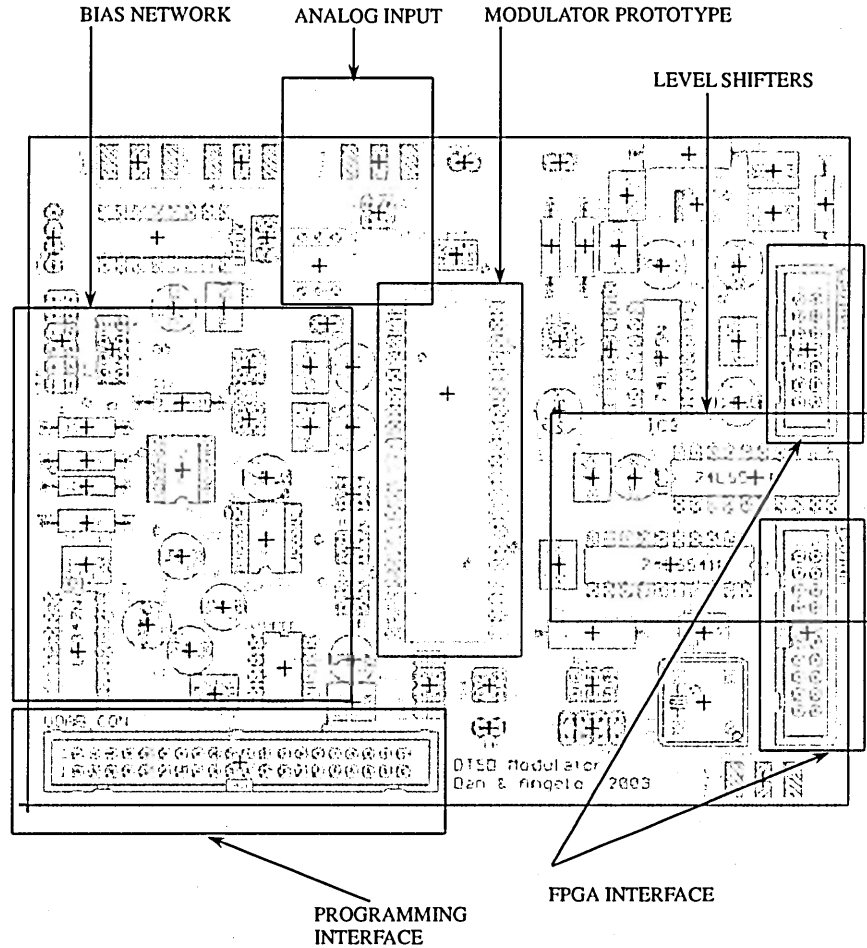
Figure 25: Modulator test board layout showing key functions. Bias network consists of buffer amplifiers and passive low pass filters. Analog input is given through an RF-SMA socket and a 5:1 transformer. The FPGA interface provides the sampling clock to the modulator and reads in the digital bit stream. The programming interface controls the tunneling and injection operations.

enable better dynamic range measurements, a high-quality audio transformer SP-21 with turns ratio 5:1 is interposed between the filter and the chip input. The secondary advantage of using this transformer is that the output is center-tapped, and hence, the input common-mode voltage can be applied to the center-tap. The sinusoidal test signal at the transformer output swings symmetrically above and below this DC voltage. In the experimental setup, the input common-mode is set to 1.850.

5.2 PCB Design for the Modulator Test Board

Design guidelines for mixed-signal circuits are adopted to minimize degradation of modulator performance due to board layout as well as provide visibility for debug purposes [20]. Figure 25 shows the functional layout of the modulator test board. The 4-layer modulator test board is designed with a split ground plane. The analog and digital portions of the circuit are located as far away from each other as possible. Separate analog and digital grounds are used, and are star connected at the point where the board gets its power input. Clock trace is kept short and away from sensitive analog circuitry. Sensitive analog inputs and outputs use RF-SMA sockets for better isolation.

The power supply pins of every IC on the test board are decoupled by a parallel combination of two capacitors ($10\mu F$, $0.1\mu F$) to reject noise effectively as well as to ensure stable DC power supply. The decoupling capacitors are placed very close to the IC power supply pins for effective operation. Bias voltages to the test prototype are also decoupled similarly. Sufficient number of test points are provided to monitor DC voltages on the board and modulator test outputs using either a multi-meter or an oscilloscope. Figure 26 shows a partial view of the routing layers and the split ground planes. The analog blocks are to the left side while the digital blocks are to the right. In figure 27 the soldered test board is shown while in operation. The decoupling capacitors that obscure the modulator prototype from view, were added to filter out noise on bias voltages effectively.
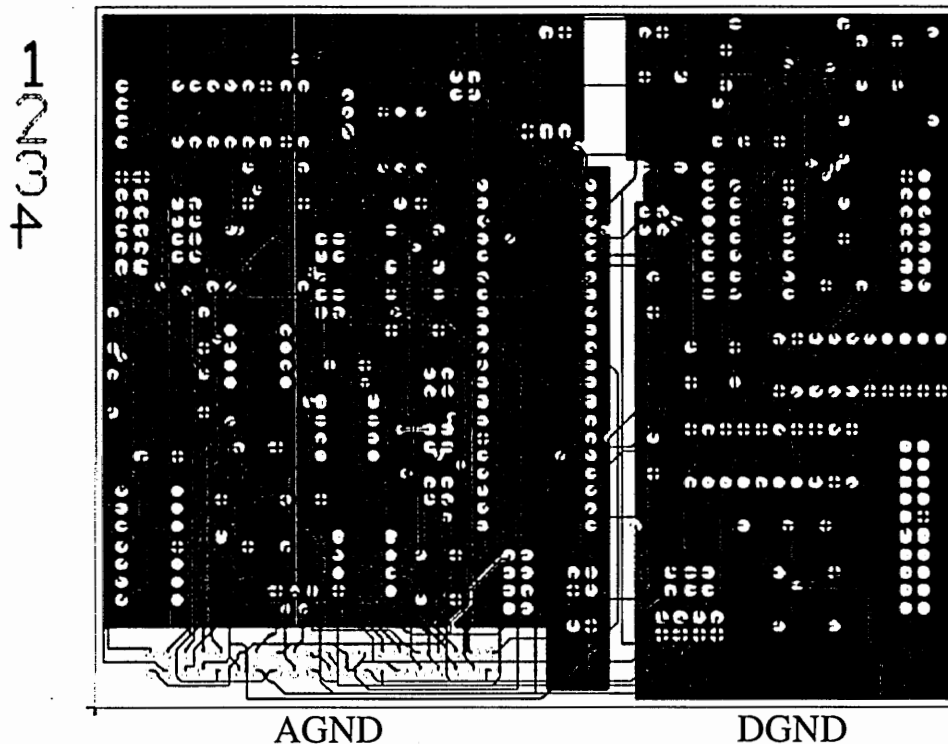
Figure 26: Partial view of the routing layers of the modulator test board as well as the separate ground planes. Note that the analog circuits are mounted on the AGND side while the digital circuits are over the DGND side.

5.3 Coefficient Programming and Measurements

The pin-out of the modulator is shown in figure 28. The die is packaged in a 40-pin ceramic DIP. While programming the device, *CLOCK* and *SYNC* are used to navigate the e-pot array. *DIGINJECT* and *DIGTUNNEL* are select inputs that turn on/off the injection and tunneling operation respectively. The e-pot currently being programmed or read is monitored at the pin *CHIPVOUT*. The remainder of the programming interface consists of bias voltages.

When the modulator is in operation (achieved by bringing reset to inactive and turning on the modulator clock), the three signals of interest are *VIN*-the analog
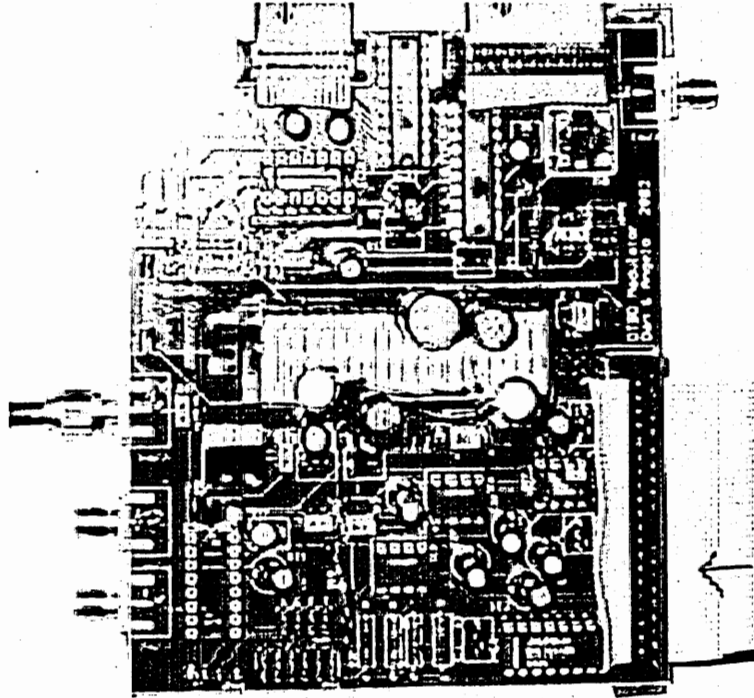
Figure 27: Soldered test board in operation.

input signal, CLK-the modulator clock at 2 MHz and the modulator output $DOUT$. The order of the modulator is selected using the pins $ORDERSEL1$ and $ORDERSEL2$. Visibility into the internal nodes is provided in several ways. The $CURRMEAS$ pin is normally connected to ground. However, for debug, an ammeter can be inserted between the pin and ground to sense the bias current of the integrator op-amps. The operation of the decoders that select the modulator order can be verified by observing $ORDER1$ through $ORDER4$. For correct operation only one of these outputs should be at logic high. Pins $INTOUT1$ through $INTOUT4$ are buffered integrator outputs. They can be used to indicate if the integrators are stable or overloaded. $VMID$ is the input common-mode voltage. It can be set either with an external 2.5V voltage

DUT PIN DIAGRAM

1	INTOUT2	INTOUT3	40
2	INTOUT1	INTOUT4	39
3	CHIPVOUT	LAT1OUT	38
4	DVDD	COMPOUT	37
5	FOLBIAS	CLKOUT	36
6	VREF	AVDD	35
7	OUTBIAS	ORDER4	34
8	VTUN	ORDER3	33
9	DIGINJECT	ORDER2	32
10	CLOCK	RESET	31
11	VCOMP	VPC	30
12	VINJ	ORDER1	29
13	PDBIAS	ORDERSEL2	28
14	DIGTUNNEL	ORDERSEL1	27
15	GND	VNC	26
16	SYNC	AVDD	25
17	VIN	NC	24
18	BIASOUT	DOUT	23
19	BIASIN	CURRMEAS	22
20	VMID	CLK	21

LEGEND:	
MODULATOR OUTPUT	
EPOT OUTPUT	
PROGRAMMING INTERFACE	
POWER SUPPLY	
MODULATOR CLOCK	
ANALOG INPUT	

Figure 28: Chip prototype pin-out diagram. The die size is 1.5mm x 1.5mm and is packaged in a 40-pin ceramic DIP.

reference or by a DAC. The DAC option is provided to allow an adjustable common-mode voltage. *AVDD* and *DVDD* can be set at any level between 3.3V and 5V through LM317 adjustable voltage regulators. The current setup sets *AVDD* and *DVDD* to 5V. The *RESET* pulse is used before every data sampling run, to start the modulator in a known state.

The die photograph of the complete modulator is shown in figure 29. At the top are the e-pot array elements as well as the navigation circuits. The bottom left portion of the die contains the clock phase generator. The forward path of the modulator,
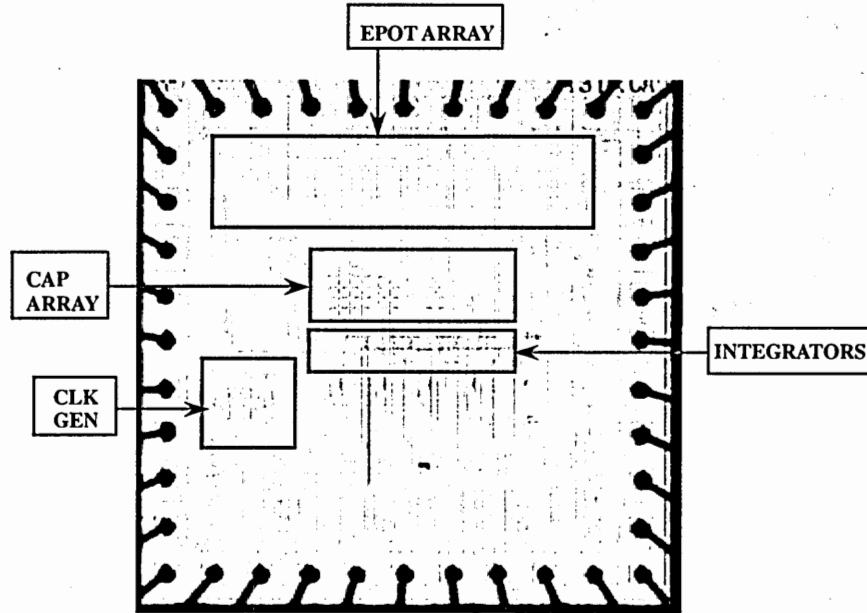
Figure 29: Modulator die photograph.

consisting of integrators, comparator and latch is located in the center. The unused sections of the die are covered by metal fill layers required by the fab.

5.4 Second Order Modulator Results

On the IC prototype, a second order modulator is programmed at run-time with the following coefficients - $f_{b1} = 0.8$, $f_{b2} = 0.6$ to give the best performance. $b_1 = 0.4$ and $b_2 = 0.8$ are the fixed integrator gains. By run-time programming we imply that the e-pots are programmed while the input and sampling clock are active. In other words the modulator is actually producing a digital bit stream. From a survey of current literature, this is the first time such an initialization of the modulator has been attempted. The programming is carried out in two passes sequentially starting from the integrator closest to the input. The first pass is used to place the e-pots
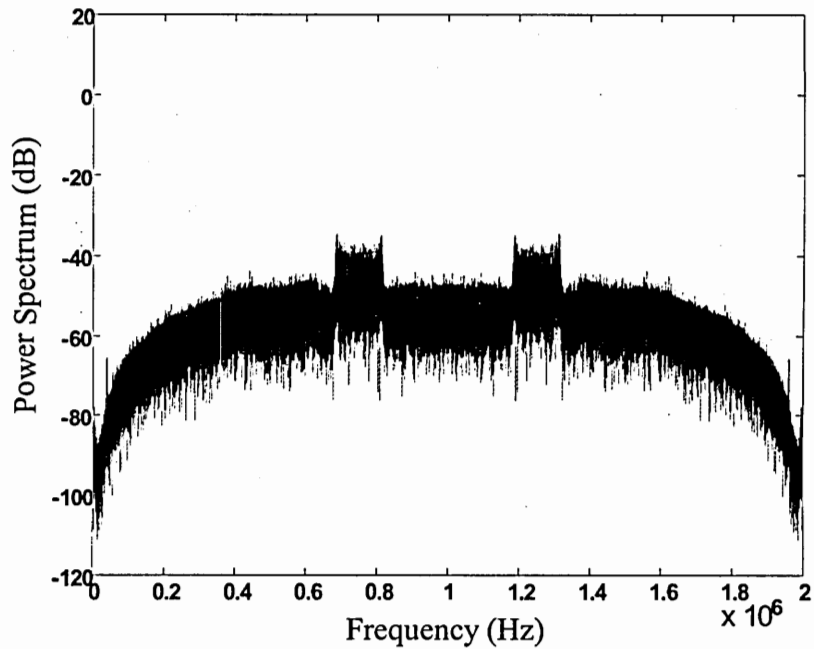
45

Figure 30: Illustration of typical second order modulator noise shaping. At high frequencies the shape of the curve departs from a smooth high pass transfer function. This is not catastrophic as these frequencies are well beyond the range of interest.

in a coarse range around the true target value. The second pass is used to get the precision.

In the second order modulator experiments the coefficient f_{b2} is increased over the value predicted by SIMULINK to provide for increased stability margin. The increase in f_{b1}, however is empirical and needs to be correlated with the model. The voltages corresponding to the coefficients as well as other pins of the modulator are listed in Table 9. Figure 30 shows a sample two-sided spectrum illustrating the noise shaping performed by the modulator.

Figure 31 shows the idle channel noise spectrum. The idle channel noise spectrum can be used to determine if the modulator suffers from unwanted tones in the output
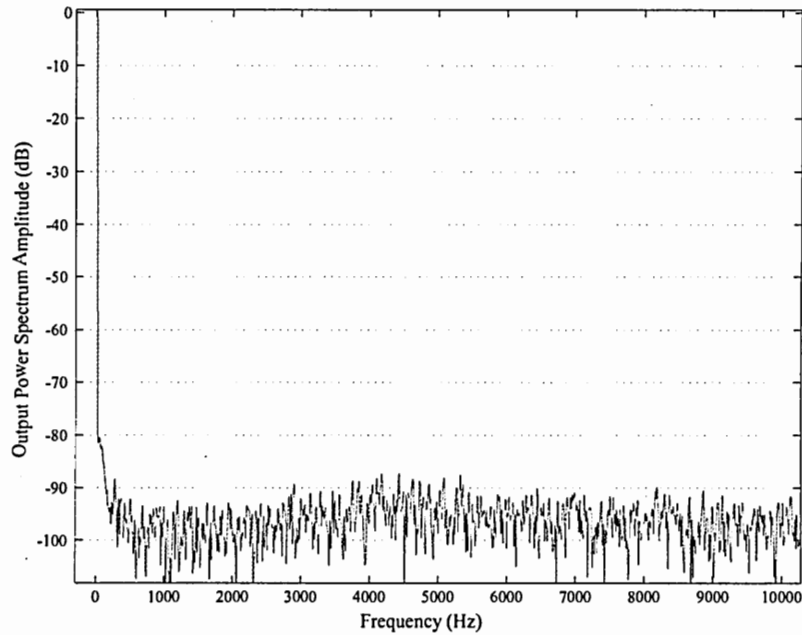
Figure 31: Output spectrum of second order modulator for zero signal amplitude. Idle channel noise indicates the performance of the modulator during periods of signal silence. Noise floor=-95 dB.
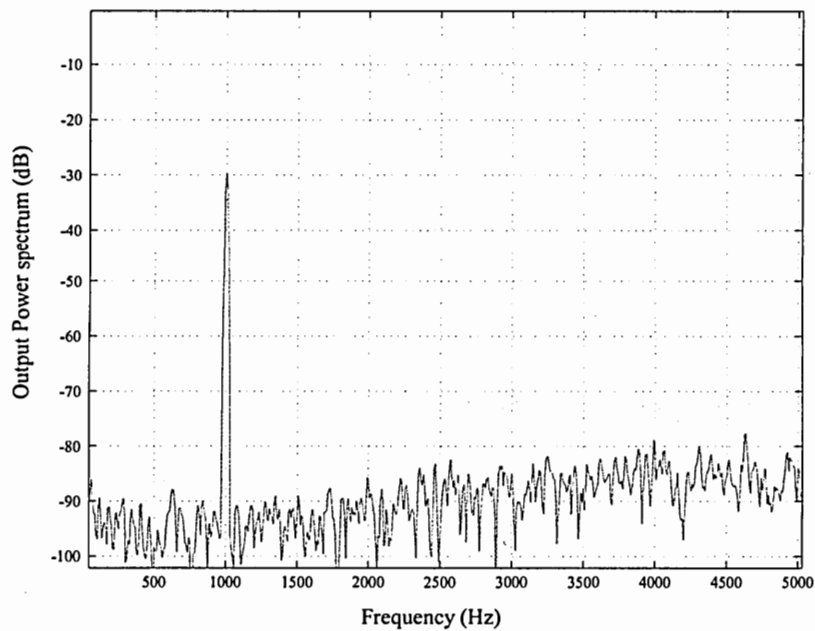

Figure 32: Output spectrum of second order modulator for 360mV$_{pp}$ input sinusoid at 1 kHz. SINAD=51.23 dB, SNR=51.69 dB, Fin=1 kHz, Fs=2 MHz, BW=8 kHz.

Table 9: Key voltage values for a second order modulator. Refer figure 28 for pin level details.

Pin/Signal	Voltage [V]
V_{mid}	1.850
$V_{outbias}$	1.800
V_{ref}	2.500
V_{comp}	2.650
V_{tun}	14.00
V_{inj}	6.500
$V_{fb1,plus}$	3.330
$V_{fb1,minus}$	0.370
$V_{fb2,plus}$	3.000
$V_{fb2,minus}$	0.700

spectrum when the input is absent. Figures 32 and 33 show experimental power spectrum and DR respectively for the tuned modulator. The input frequency is 1 kHz. The signal bandwidth for computing SNR and SINAD (Signal-to-noise and distortion) is chosen to be 8 kHz. Dynamic range is computed by plotting SINAD versus input amplitude, normalized to the input value that gives peak SNR. SINAD includes contributions from noise as well as 2nd through 5th harmonics. The peak SINAD is used to calculate the ENOB using (5) in chapter 1. The noise floor is around −95 dB. Figure 34 shows how run-time tuning out of the e-pot output mismatch can help to reduce harmonic distortion significantly. The experimental measurements are summarized in Table 10.

Several valuable observations resulted from the prototype testing. The noise floor was higher than expected. Possible causes could be the noise on the external bias voltages as well as power supply and digital noise coupled into the substrate. Experimental observation of noise on the power supply pins showed values of about $40mV_{pp}$.
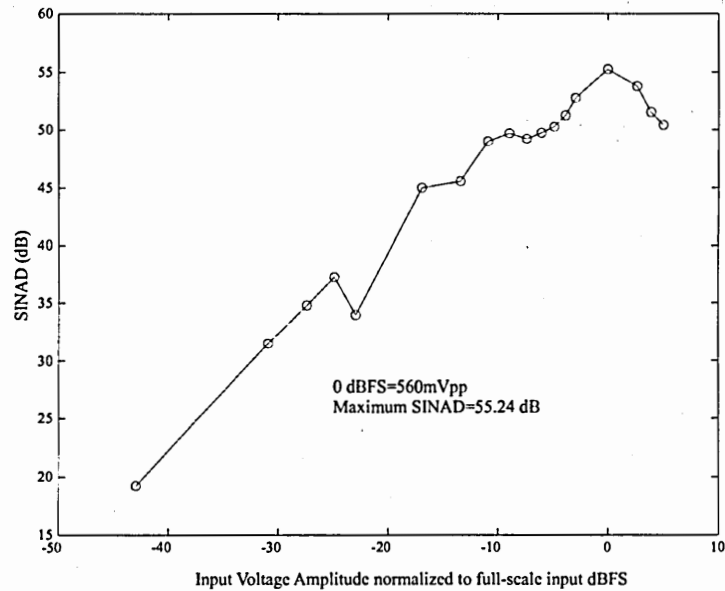
48

Figure 33: Dynamic range plot for the second order modulator. Maximum SINAD is obtained as 55.3 dB for an input amplitude of 560mVpp at 1 kHz, BW=8 kHz.
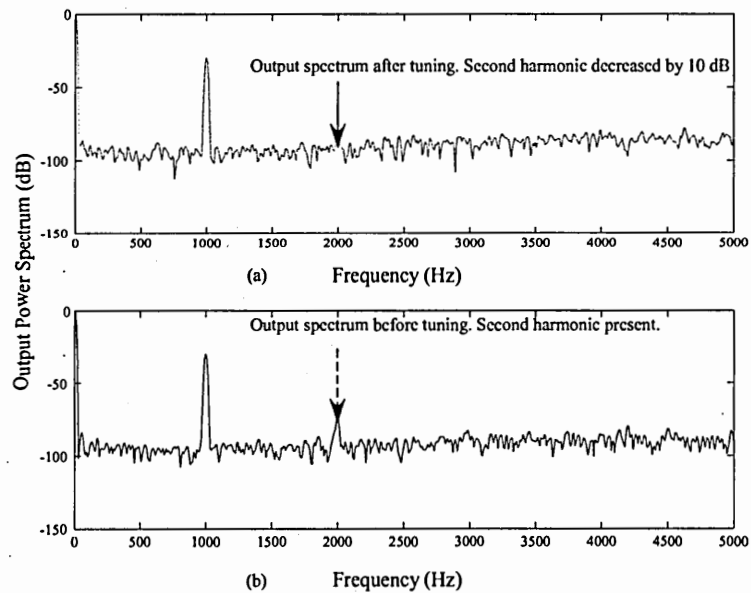

Figure 34: E-pot output mismatch induced second harmonic distortion. Better matching by run-time programming can reduce such distortion. (a) After tuning, (b) Before tuning. Second harmonic reduced by 10 dB for input signal amplitude of 360mVpp at 1 kHz.

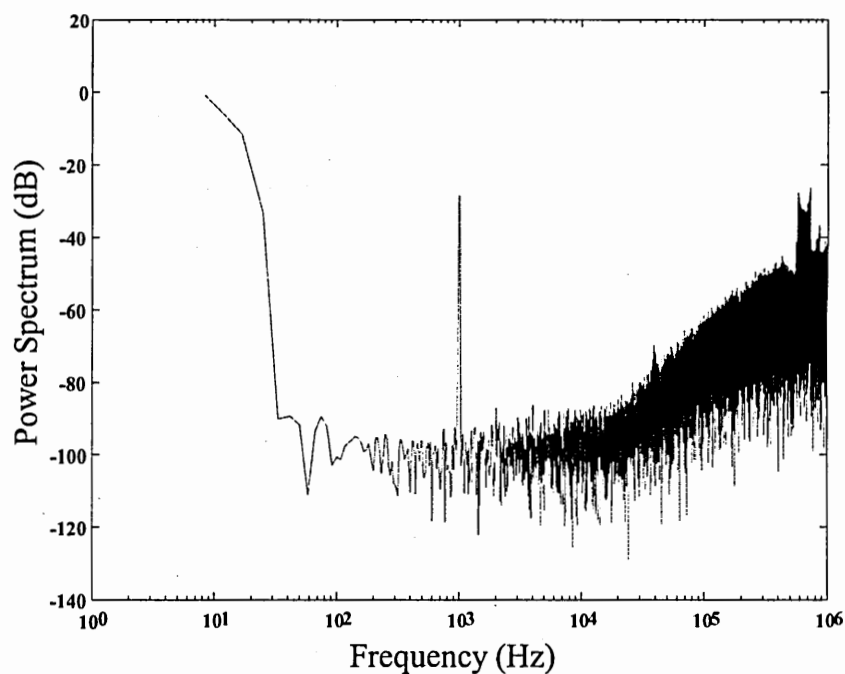**Figure 35:** Spectral plot showing improved noise floor due to precise matching of e-pot coefficients.
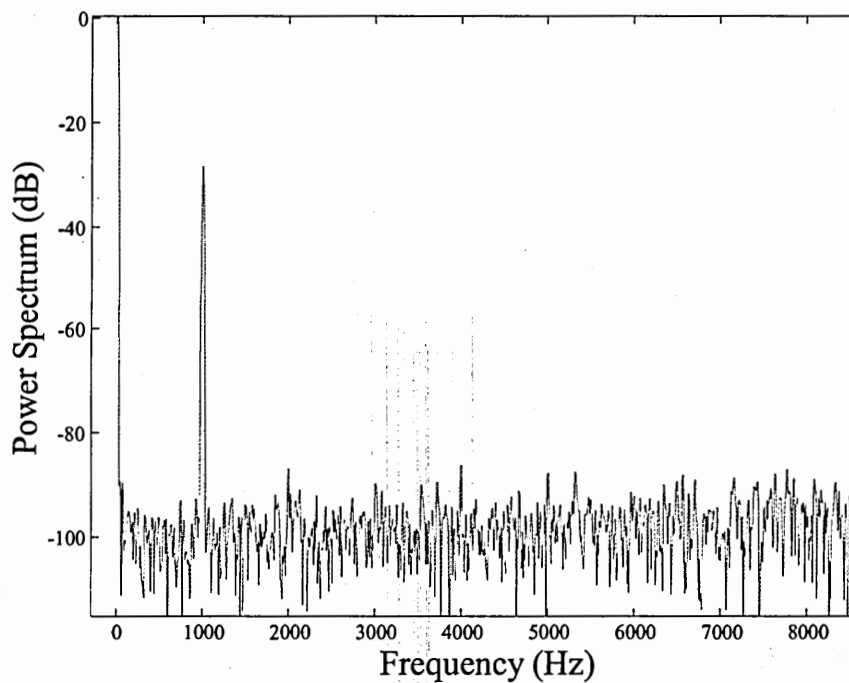

Figure 36: Magnified view of the baseband spectrum of figure 35. Note the low amplitudes of harmonics and the near -100 dB noise floor.

Table 10: Summary of experimental results for a second order modulator.

Parameter	Value
F_{sample}	2 MHz
OSR	125
Bandwidth	8 kHz
F_{input}	1 kHz
$V_{in,pp}$	560 mV_{pp}
SNR_{max}	56.80 dB
$SINAD_{max}$	55.24 dB
ENOB	≈ 9
Dynamic range	55 dB
Noise Floor	-95 dB

The deviation of the noise floor from the simulated values could also be the attributed to the fact that the transient analysis in SPICE does not simulate thermal or 1/f noise. Hence simulations indicate the effect of quantization noise only. An educated guess would be that the modulator performance in the baseband is dominated by thermal and 1/f noise rather than the quantization noise. The noise shaping is on expected lines. However a peaking is noticed in the 700 kHz-800 kHz frequency range. It could be the result of a peaking in the noise transfer function at these frequencies. However its dependence on coefficient values that set the transfer function poles needs to be quantified.

Second harmonic distortion was noticed. The dominant cause is experimentally determined to be the e-pot output voltage mismatch for a given stage. It was found empirically that the distortion was reduced considerably by programming e-pots such that the feedback coefficients for each stage were matched to within a 1–2 mV. However, during run-time measurements of the e-pot values, deviations of the order of 7-10mV were noticed from the programmed values. The transients at clock edges
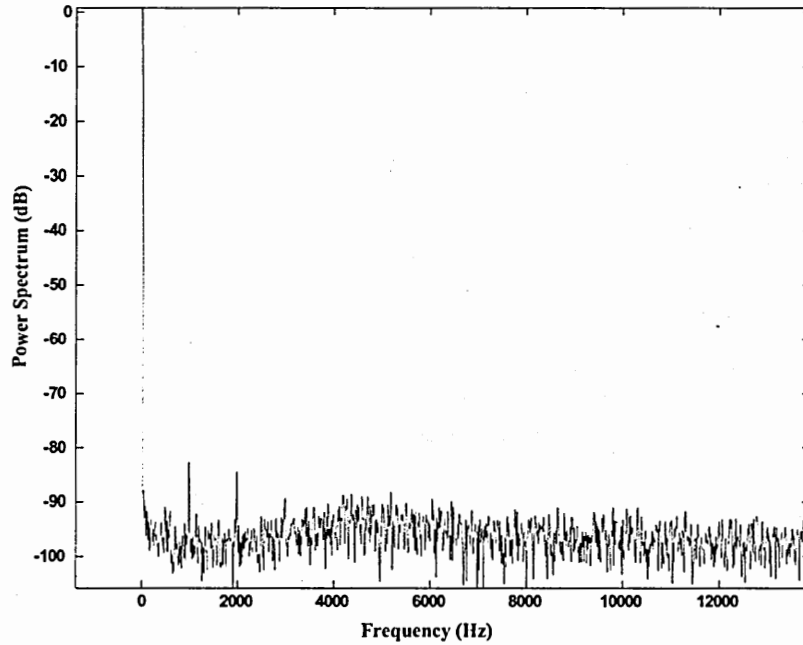
Figure 37: Idle tones in the output spectrum. Tone frequencies are 1 kHz, 2 kHz and 3kHz. Tone amplitude is below -83 dB.

could be responsible for these temporal changes. The magnitude of the change was reduced by increasing the tail current of the e-pot amplifier ostensibly to enable the e-pots to drive the capacitive load.

The matching seems to have an impact on the noise floor too. Figure 35 shows a spectral plot for a 200mV_{pp} input where the e-pots have been matched to 0.05%. The noise floor is improved by about 5 dB as compared to figure 31 and is close to -100 dB. Figure 36 shows a magnified view of the baseband spectrum for the same experiment. This is to be compared with the results obtained in figure 32. However in this prototype, It was not possible to sustain the accurate matching of the e-pots over an extended time duration. At high input amplitudes where the integrators saturate, matching of e-pots has little impact on distortion.
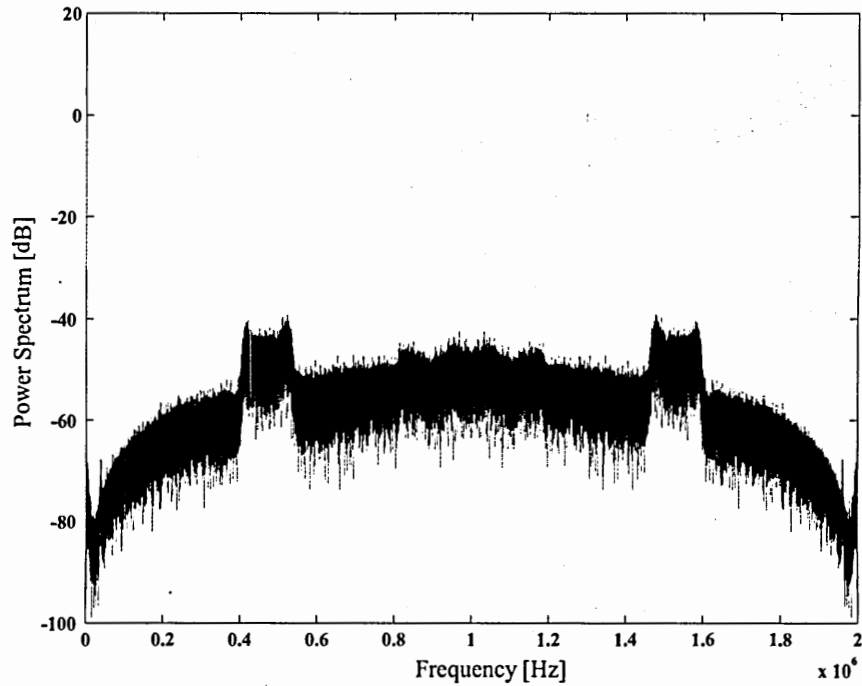
Figure 38: Third order modulator noise shaping.

During idle channel noise measurements, occasional tones were observed in the output spectrum. Tones are a known phenomenon in second-order modulators not employing dithering [21]. When the channel is idle, the gaussian white noise approximation for the quantization noise and consequently the noise shaping concept are not valid. Figure 37 shows a snapshot of tones in the output. Observed tonal amplitude was below -83dB.

5.5 Preliminary Third Order Modulator Results

At this time a third order modulator is being programmed in a similar manner as a second order modulator described in the previous section. The following coefficients are being used - $f_{b1} = 0.3$, $f_{b2} = 0.8$, $f_{b3} = 0.9$. $b_1 = 0.3$, $b_2 = 0.4$ and $b_3 = 0.8$ are
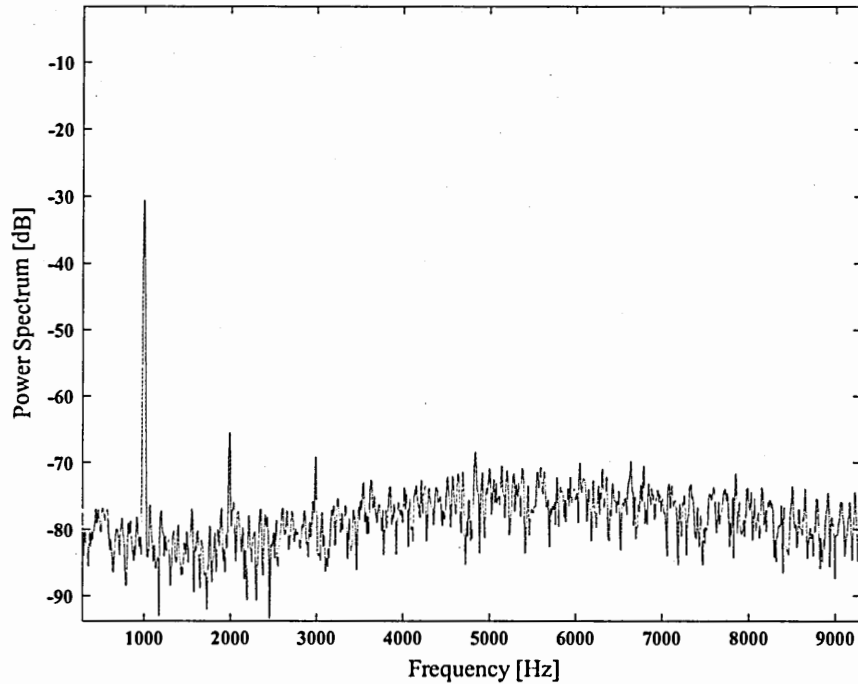
Figure 39: Baseband spectrum of a third order modulator for a 40mV_{pp} sine input.

the fixed integrator gains. The modulator is stable for input voltage amplitudes less than 120mV_{pp}. Figure 38 shows a sample two-sided spectrum illustrating the noise shaping performed by the third order modulator. The peaking at high frequencies is noticed here too, as in the case of the second order modulator. The shaping is less steeper than expected for a classical third order modulator. At this time an explanation is being sought for this behavior. Figure 39 shows the baseband spectrum for a 20mV_{pp} sinusoidal input. Comparison with the second order modulator spectra indicate a higher noise floor as well as the presence of increased harmonic distortion contributing to a lower signal-to-noise ratio. Efforts are on to investigate how the spectral quality of the output can be improved.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

This work represents the first experimental foray into using floating-gate circuits in discrete–time Δ-Σ modulators. It has been shown here that floating gates can be used in Δ-Σ modulators achieving close to 9 bits of resolution. Experimental results show a maximum SNR of 57 dB and a DR of 55 dB. Currently third and fourth order modulators are being tested using the experimental setup described in chapter 5. A simple topology has been used for the modulator. With better topologies, improved performance can be expected.

Experimental investigations also revealed limitations of the integrator and e-pot amplifier circuit blocks. The integrator op-amp is load stabilized. This is a problem since the op-amp sees a varying load in different clock phases. The e-pot amplifier is being redesigned to be low noise as well as to be able to drive large capacitive loads. A further PSRR optimization of e-pots is also being carried out. Better layout design to minimize injected substrate noise due to sampling clock and other digital signals is in progress. The current integrator topology uses single-ended amplifiers. Hence common-mode rejection is poorer. The redesigned chip will use fully differential circuits to achieve better linearity and common-mode noise rejection.

An evolution of this work to target continuous-time modulators is being pursued concurrently. The Δ-Σ continuous-time modulator uses a Cascade-Of-Integrators
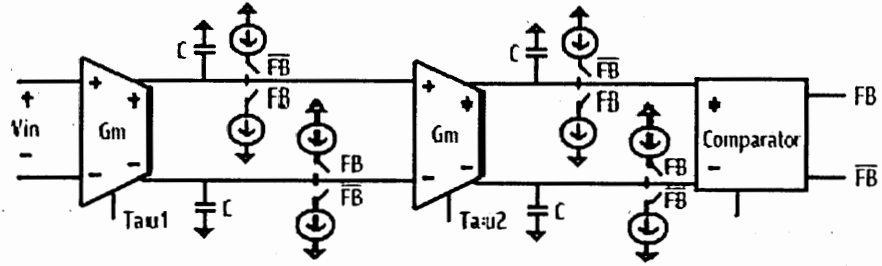
Figure 40: Continuous-time Δ-Σ modulator architecture. Floating-gate transistors set the G_m of the integrator and the current of the modulator feedback. The forward path is implemented as a Cascade Of Integrators topology.
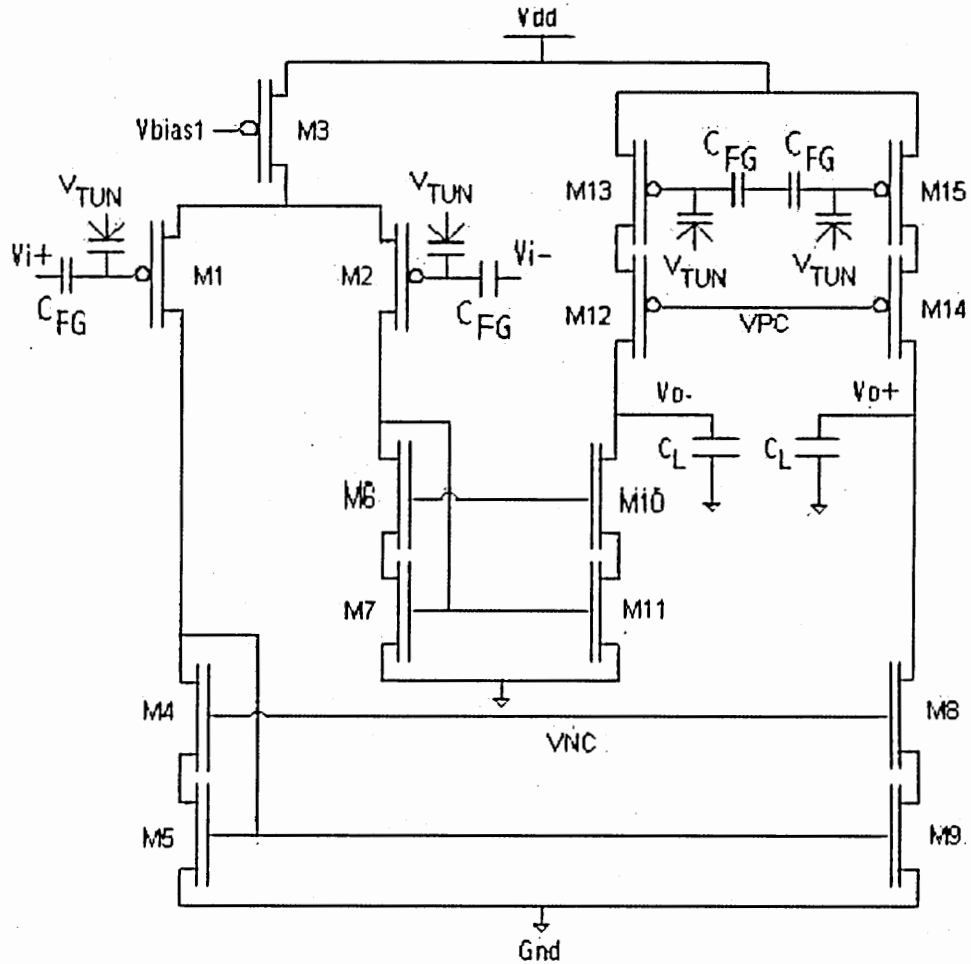

Figure 41: G_m-C integrator circuit schematic used in the continuous-time modulator.

56

structure consisting of a tunable subthreshold G_m-C integrators and a tunable 1-bit current DAC for negative feedback. The architecture can be seen in figure 40. The G_m-C integrator is designed to run at subthreshold current levels and to take advantage of floating gate programming techniques. The proposed architecture can be seen in figure 41. The differential pair, M1 and M2 are attached to floating gate inputs which allow for improved linearity and an ability to program out offset due to threshold voltage V_{TH} mismatch. Bias transistor M3 is set by a CMFB circuit (not shown). Transistors M13 and M15 are also programmable by floating-gates and allow for the removal of current mismatch in the output leg. For a given SNR, the modulator has lower power consumption than the discrete time realization because of the use of subthreshold currents.

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