THERMAL TRANSPORT IN III-V SEMICONDUCTORS AND DEVICES

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THERMAL TRANSPORT IN III-V SEMICONDUCTORS AND DEVICES

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SUMMARY

Research and development of wide bandgap semiconductors has showed that there is an amazing potential to affect the lives of everyday people. Improvements in widely available products like cell phones and light sources will be realized with the introduction of higher performance and more efficient devices. It is no surprise that the huge potential market has made wide bandgap semiconductors, specifically gallium nitride (GaN) the second most researched semiconductor. However there are still technical challenges that need to be addressed and overcome.

It is the objective of this work to focus on heat dissipation in gallium nitride based solid-state logic devices as well as optoelectronic devices, a major technical challenge. With a direct band gap that is tunable through alloying between 0.7-3.8 eV, this material provides an enabling technology for power generation, telecommunications, power electronics, and advanced lighting sources. Previously, advances in these areas were limited by the availability of high quality material and growth methods, resulting in high dislocation densities and impurities. Within the last 40 years improvements in epitaxial growth methods such as lateral epitaxial overgrowth (LEO), hydride vapor phase epitaxy (HVPE), molecular beam epitaxy (MBE), and metal organic chemical vapor deposition (MOCVD), has enabled electron mobilities greater than 1600 cm^2V/s, with dislocation densities less than $10^9/ cm^2$. Increases in device performance with improved materials have now been associated with an increase in power dissipation ($>1kW/cm^2$) that is limiting further development.

With this increase in power dissipation there exists a need for a cooling methodology that at the chip level requires a purely conductive path for heat removal. The fact that conduction plays a critical role in the heat removal process has driven research to accurately characterize the key thermophysical parameters in the active layers as well as the substrates that are used to grow the semiconducting thin films. Determining these material parameters will aid in the development of more representative models of device behavior that will allow for higher reliabilities to be demonstrated. Characterization of semiconducting thin films (as well as related substrates) is a non-trivial task due to the low dimensionality of heterostructure layers and often very high material thermal conductivity. As a result of the epitaxial growth of the thin films there is a significant coupling between thickness and the thermal conductivity. Lattice mismatches lead to dislocation growth that allow for a higher rate of phonon scattering; phonons are the major heat carrier in semiconductors. In addition to dislocations, potentially high levels of impurities can cause a significant decrease in the thermal conductivity. To investigate these effects on the thermal conductivity, experiments were performed using the 3ω method within a cryostat in order to find trends as a function of temperature.

In addition to determining the thermal conductivity of various III-V semiconductors, temperature mapping must be performed to study the heat flow within a device. Both micro infrared imaging and Raman spectroscopy have the ability to provide absolute temperature measurements with high spatial resolution, which is sufficient for most power electronic devices. Temperature mapping was performed on a dual multi-quantum well light emitting diode as well as an $Al_{0.3}Ga_{0.7}N/GaN$ heterostructure high

electron mobility transistor. Comparisons were made between experimental results and device level-finite element modeling which provided the building blocks needed to perform a study of current electronic packaging technologies. High heat flux package geometries and materials were investigated as possible solutions to the heat generation problem within the devices. Among possible solutions were both passive and active technologies. Passive cooling must be achieved with advances in material properties, most notably, the thermal conductivity. A wide range of composites including diamond impregnated silicon carbide and carbon nanotube/copper alloys were introduced as next generation package materials. More aggressive active cooling strategies were considered for very high heat flux devices; these included spray cooling, thin film evaporation, and dielectric fluid boiling.

In the following work thermophysical material of III-V semiconducting thin films and associated substrates are presented. Numerical modeling coupled with optical methods was utilized in order to study the heat carrier motion and the temperature distribution in an operating device. Results from temperature mapping experiments led to a discussion of next generation advancements in electronics packaging.

CHAPTER I

INTRODUCTION

1.1 Motivation for Research

There has been notable interest in the use of wide bandgap (WBG) semiconductors for consumer as well as defense applications. This driving force led to Defense Advanced Research Projects Agency (DARPA), Office of Naval Research (ONR), Air Force Office of Scientific Research (AFOSR), and the Army Research Laboratory (ARL) to identify several specific technological initiatives that drive interest in WBG devices. Specifically, DARPA and the ONR are developing high power radio frequency (RF) circuitry for radar, satellite communications, smart weapons, and other air defense and signal jamming applications. With the rapid development in the performance of WBG devices comes a significant amount of power dissipation, on the order of 1000W/cm^2, with can lead to high temperatures and premature failure. This concern has caused the Navy Manufacturing Technology Program (MANTECH) to categorize issues in thermal management of power devices as "most critical" due to the large range of applications in X-band radar, S-band radar, and the Link 16 (pictured below), just to name a few [1].

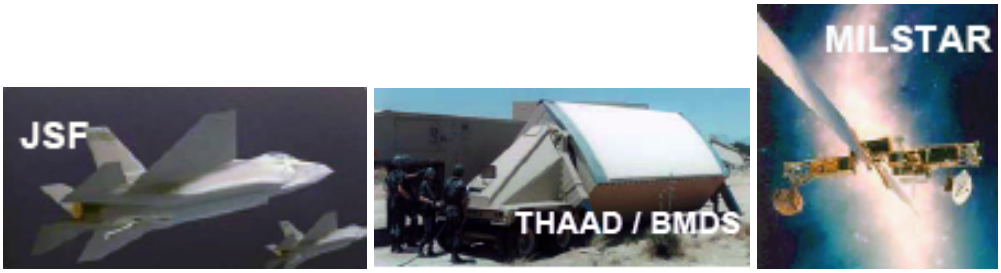


Figure 1. Joint Strike Fighter (JSF), Theater High-Altitude Area Defense (THAAD), and MILSTAR (advanced satellite communications) are all examples of various military programs that rely on the development of wide bandgap semiconductors [2].

Figure 2. The Link 16, developed by Rockwell Collins is a Tactical Digital Information Link (TADIL). The primary function of the Link 16 are to exchange friendly unit positions, status data, and control/manage air, surface and subsurface units [3]. Average power dissipated from this enclosure can be up to 750W for a 12.5 x 10 x 7.5 inch unit.

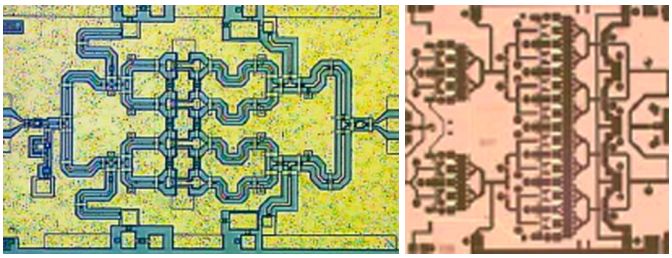


Figure 3. Wide bandgap semiconductors can be used to build a variety of electron devices. An example of a Q-band integrated circuit (>40Ghz) (left) and a X-band IC (8-12 Ghz) (right) that make programs like the ones mentioned above possible [4].

Beyond defense applications WBG devices can have a huge impact in commercial areas such as traffic control, large area displays, automotive, general illumination, mass data storage, and advanced wireless communications. Having WBG semiconductors penetrate these markets will result in transportation lighting with is brighter, more energy efficient, and reliable, stronger wireless communications signals with increased area coverage, and high efficiency small form factor lighting for buildings and flat panel displays. The significant potential for everyday uses will make the GaN market a >$5 billion/year arena by 2010 [2].

The development of group III-nitride semiconductors, including GaN, AlN, and InN, have long been recognized for their potential in optoelectronic and microelectronic device applications. While much effort over the last 40 years has been invested in their development major challenges to their realization have been the lack of suitable growth substrates contributing to films with poor electronic properties [5-8]. However, continued advancements in growth technologies (MBE and MOCVD) for Si and GaAs devices have benefited the fabrication of III-nitride devices. These techniques are now commonly used to produce high quality GaN layers on a variety of substrates including sapphire, GaN, SiC, ZnO, and lithium gallate ($LiGaO_2$). While improvements in material fabrication continue to be a key area of research, a second limiting factor to the successful development of GaN devices has emerged. The increase in performance of power electronic devices has been associated with considerable heat generation, which presents major challenges in the area of thermal management and reliability. Even with the ability to operate at temperatures in access of 200°C, challenges still arise in maintaining this maximum junction temperature and are critical to first order [5].

Methods used to dissipate this heat and reduce device temperatures have included traditional thermal management solutions taken from Si microelectronics in addition to the use of high thermal conductivity substrates like SiC and single crystal GaN. In practical applications, heat dissipation through high conductivity substrates has seen some improvements in thermal behavior of devices, but fails to provide an adequate solution for ultra high power devices. This issue of heat dissipation and controlling device temperature has now become paramount to the realization of modern GaN based microelectronics.

To address the heat dissipation problem several system-level cooling schemes have been investigated for efficient thermal management, such as flip-chip bonding, two-phase spray cooling, and mounting devices onto advanced metal matrix composites with ultra high thermal conductivity values [9-15]. In many of the thermal management strategies presented, a significant portion of the heat removal occurs from dissipation of thermal energy through the substrate of the GaN device. Thus the contributions of the substrate to the device thermal resistance must be understood. In general, this contribution is more complicated than the substrate simply adding its own thermal resistance to the heat dissipation path. While GaN can be grown on a number of high thermal conductivity substrates, passive heat dissipation into these materials can be adversely affected the by dislocation densities induced in the GaN from lattice mismatch during epitaxial growth and the interface resistance with the substrate material. In order to dissipate thermal energy under a minimal temperature rise, an accurate understanding of the thermal behavior of the materials used in construction of the device must be obtained.

Currently GaN-based devices are grown on a limited number of substrates, most popular being sapphire due to its low cost. However, sapphire's lattice mismatch with GaN along the *a*-axis is –13.62% [16]. This mismatch results in difficulties when trying to grow high quality thin-films because of large dislocation densities that are inherent in an epitaxial process (>10^9 cm^{-2}) [17, 18].

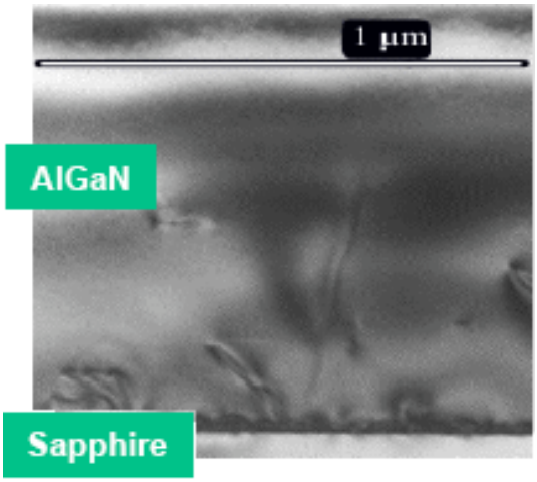


Figure 4. Cross-section TEM image of threading dislocation formation in an AlGaN layer grown on sapphire. Despite the alloying of GaN and AlN the lattice constant is still largely mismatched to the sapphire [2].

Low temperature deposited GaN buffer layers and lateral epitaxy overgrowth can help to reduce the dislocation density in the active region of the device but induces layers of much lower thermal conductivity material near the substrate interface. To alleviate this issue, a substrate that has a closer lattice match would help to simplify the growth and heat dissipation processes by simultaneously reducing dislocation formation and the interfacial resistance caused by the material dissimilarity [19]. Of the available substrates which are closely matched with GaN, lithium gallate ($LiGaO_2$) possesses a lattice mismatch of only 0.19% and would therefore be a strong candidate for growing high

quality GaN films without the need for buffer layers [16]. The disadvantage to these substrate materials is that they are poor thermal conductors, usually having a thermal conductivity of ~30W/mK at room temperature. Techniques such as "epitaxial lift-off" and "bonded substrate removal" allow for a high quality GaN layer to be grown and then bonded to a higher thermal conductivity substrate [20]. Currently, the growth of GaN on substrates that have very close lattice matches, such as $LiGaO_2$, has been demonstrated and is being considered for applications involving LEDs, laser diodes and metal-semiconductor-metal (MSM) photodetectors. Other substrate materials, such as SiC, are still in initial research phases but results have showed promise in the areas of GaN MESFETs, MISFETs, AlGaN/GaN/SiC HFETs, GaN/SiC HBTs, piezoelectric and pyroelectic sensors. High temperature application areas are particularly suited for these GaN/SiC devices; pressure sensors, temperature sensors, high power microwave switches, and non-volatile memories are just a few areas of interest [21].

Alternatives to passive cooling techniques were briefly mentioned previously; those being variations on 2-phase spray cooling. Two-phase cooling can be highly efficient at removing heat from a device due to the latent heat of the working fluid that is absorbed during vaporization phase. However there are several problems with hermetic sealing of the devices, large packaging enclosures, and high costs. Even with these roadblocks device enhancements have been realized with some novel packaging ideas that try and minimize the effect of these three problems. Recently parylene, a cheap and easy polymer to apply in nanometer thick films was deposited onto a 500Mhz RF power LD-MOSFET and water sprayed through silicon micromachined nozzles directly onto the

surface of the device as seen in Figure 5 [22]. An increase of 8% in power output was observed which was attributed to the reduction in the junction temperature.

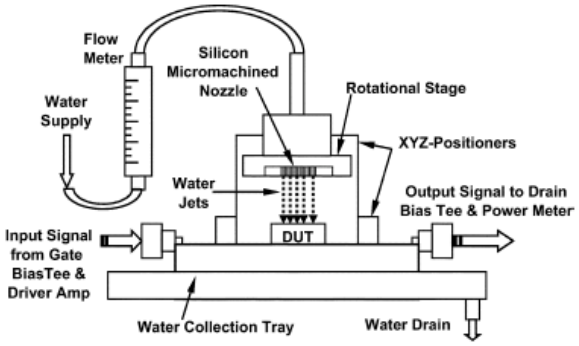


Figure 5. Schematic of water spray cooling experimental arrangement [22].

Solid-state lighting could be one of the most important developments of this century. If LEDs can reach a target efficiency of 50% (200lm/W) a 50% decrease in the 600TW-hr/year or almost $25B/yr can be saved [23]. In addition a 50% decrease in the 50Mtons/yr of carbon emissions created during generation of electricity for lighting will occur [23]. As is the case with high power electronics the heat generation within the device is one of the major limiting factors in the performance. In the case of optical devices many of the active packaging schemes are not feasible, as they do not allow for efficient extraction of the emitted light or are not suitable for the application environment. To further complicate the heat removal process the most common packaging materials for the LED housing tend to be polymer-based composites, notorious for low thermal conductivities. Therefore the surrounding package adds a large thermal resistance that will cause the device to operate at higher temperatures. Hot spots in deep UV emitting LEDs have been reported to reach temperatures of >150^{o}C at only moderate

power levels around 1W [24, 25]. While the mechanism of heat generation is primarily due to Joule heating a high heat flux package could help to reduce the temperature for the same loadings.

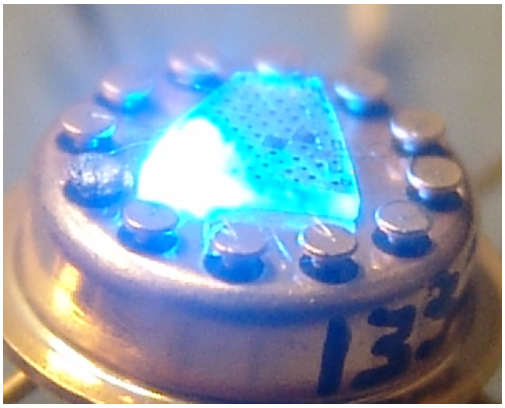


Figure 6. Dual InGaN/GaN multi quantum well light emitting diode under operation.

Elevated operational temperatures have been linked to lower quantum efficiencies, shorter lifetimes, emission wavelength shifts and catastrophic device failure [26-28]. For these reasons it is imperative that an LED package be designed considering electrical, optical and thermal issues in parallel.

Research advancements in the fields of high power electronics and optoelectronics have led to results that promise huge impacts on the environment and the way that we live. However, in order to push the technology from the research arena into the mainstream critical issues in thermal management must still be addressed. Accurate thermometry and materials' characterization of the building blocks will lead to improved output and efficiency.

1.2 Thesis Overview

The purpose of this research is to investigate the performance of power electronic devices from the nanometer lengths scales up to macro-sized packaging technologies. Power electronic systems must be analyzed as a whole in order to maximize the efficiency of the devices. The characterization of key thermophysical parameters of the semiconducting thin film building blocks was performed with the 3ω method, a resistance thermometry tool, as a function of temperature. Phonon transport models were developed for the material layers in order to better verify and understand the behavior of these relatively new materials under different growth conditions. Results of these experiments were implemented in nonlinear numerical models, performed with FEMLAB, to solve for the temperature distribution within a device. Temperature distribution was investigated utilizing different heat removal technologies. In addition to simulations, surface temperature mapping was achieved with using two techniques, micro-Raman Spectroscopy and micro infrared imaging. Both technologies have the ability to give high spatial as well as temporal resolutions. These tools allow "hot spotting" to be identified and in conjunction with material parameters could lead to an optimized electronic structure. Moving up from the device level, attention was focused on how the packaging affected the temperature of the devices contained within. Parametric studies were performed in order to identify key areas of thermal resistance in the system. Advancements in packaging technology were then suggested.

Chapter 2 is an introduction to high power electronics and includes fundamentals of how heat is generated in a structure, detailed overview of current electronic devices and cooling technologies, as well as a discussion of various growth methods. Chapter 3

focuses on different characterization methods for thermal conductivity, temperature and crystal quality. Techniques discussed in detail include the 3ω method, scanning joule expansion microscopy, x-ray diffraction, atomic force microscopy, micro-Raman spectroscopy, and micro infrared imaging. Chapter 4 outlines, in detail, the experimental methods used in all testing of materials and simulation running. Chapter 5 explains the phonon modeling methods including the relaxation time approximation to the Boltzmann transport equation. In addition to the phonon transport-modeling chapter 5 also discusses the developed thermal resistor network that was used for the parametric study of the packing density of high power LEDs. In chapter 6 future work will be outlined which leads into chapter 7 where final conclusions will be stated.

CHAPTER II

HIGH POWER ELECTRONICS

The following chapter introduces and reviews major technological advances in the field of high power electronics. Subsections include information on how heat is generated in semiconductor crystals, reviews of the state of the art devices, current cooling technologies, information on future cooling needs, and methods of semiconductor thin film growth. This review aims to give the reader a general knowledge of the field, its challenges, some solutions, and future needs.

2.1 Heat Generation in Semiconductor Devices

Heat generation in semiconductor materials has been well studied and therefore only major topics will be discussed in this subsection [29-33]. Although an overview is presented, having a solid qualitative understanding of the transport phenomena can be helpful in predicting trends and understanding complicated device structures. Major heat carriers must first be identified before proceeding.

There are three major classifications of materials: insulators, conductors, and semiconductors; the physical properties of these materials are directly related to their electronic band structure. Insulators exhibit a full valence band and as a result the electrons are tightly bound to each ion core. Energy, and therefore heat, is transferred by phonons (quantized lattice vibrations). However, phonon motion is inhibited due to the disordered nature of most insulators, with exceptions, on the molecular level. Therefore

most insulators are also poor heat conductors. Electronic conductors (metals) due to their weakly bound valence electrons form what is usually referred to as a "sea" of electrons that are not bound to any particular nuclei, therefore they easily move throughout the system. In this case the major heat carrier can be identified as the electron due to the large numbers that are allowed to move and interact with neighboring atoms. The large number of free energy carriers usually means that electrical conductors are also good heat conductors. Materials that are classified as semiconductors theoretically exhibit full valence bands at 0^{o}K. As a result of a finite operational temperature electrons will be excited into the conduction band producing a hole in the valence band; a Coulomb force weakly binds the hole and electron and this excited state is often called an exciton. An exciton can also be created if an electron in the valence band absorbs a photon of the proper wavelength (and therefore energy) from some outside source. Once in the conduction band the excited electron and corresponding hole are free to move throughout the lattice and can therefore transfer energy to its neighbors. While energy can be transported in semiconductors by electrons, their highly ordered structure allows phonons to also carry heat efficiently. When studying energy transfer in semiconductors all generation and recombination effects between excitons, photons, and phonons must be taken into account. This is not a trivial task as it involves aspects of quantum mechanics and the fact that many materials used have been artificially doped to enhance their properties [34].

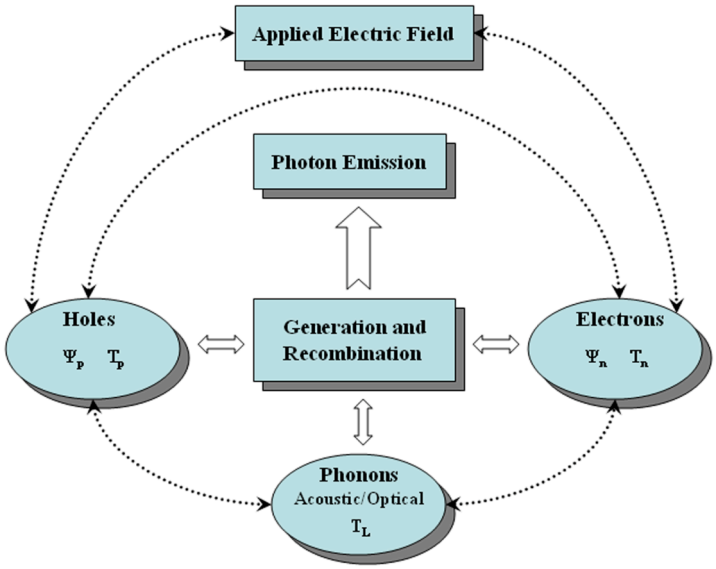


Figure 7. Above is an energy flow diagram that describes the relationship between the elementary particles found in semiconductors. The dotted lines describe paths where energy can be transferred where as the block arrows relate the particles to a general generation and recombination box. Here any number of particle combinations can interact to release any number of new particles. Ψ is the electric potential and T is the temperature that is associated with each particular system component. Adopted from [30].

As a result there have been many attempts at simplifying the problem by classifying major transport regimes. If a mean free path is defined as $\ell = v\tau$ where v is the energy carrier velocity and τ is the mean time between collisions two regimes can be identified. The so-called quantum ballistic (also called "ballistic") regime occurs when a characteristic length, $L << \ell$. At these scales the energy carriers behave in a purely quantum mechanical manner, it is necessary to solve the Schrödinger equation to understand the wave nature of the system. Devices such as light emitting diodes and other heterostructres tune the bandgap energies of the materials in order to trap electrons in desired regions of the device. Confinement of this type relies on quantum mechanical phenomena and therefore requires a study of the electron waves. At the opposite end of

the length scales is the classical diffusive regime where $L >> \ell$. The mean free path ℓ can be visualized a distance over which there is no scattering of the wave whether they be electron or phonon waves. More traditional types of semiconductor devices such as field effect transistors (FETs) behave in this regime as a result of their larger dimensions. Modeled devices in this study use classically diffusive model with additional phonon transport phenomena included, more details about the modeling of devices will be included in Chapter 5.

Under the assumption of a classically diffusive system the heat generation term Q can be defined as:

$$\begin{aligned} Q = {} & \vec{E}\cdot\vec{J} + \left(E_g + 3k_BT\right)R - \vec{J}_n\cdot\nabla\left(\chi - \frac{3}{2}\frac{k_BT}{q}\right) - \vec{J}_p\cdot\nabla\left(\chi + \frac{1}{q}E_g + \frac{3}{2}\frac{k_BT}{q}\right) \\ & + \nabla\cdot\left\{\pi_n^o\vec{J}_n - \pi_p^o\vec{J}_p\right\} - \frac{3}{2}k_B T\frac{\partial \ln m_c}{\partial \ln T}\cdot\frac{\partial n}{\partial t} - \left\{\frac{3}{2}k_B T\frac{\partial \ln m_v}{\partial \ln T} - T\left(\frac{\partial E_g}{\partial T}\right)_{n,p}\right\}\frac{\partial p}{\partial t} \end{aligned} \tag{2.1}$$

Looking at each one of these terms separately reveals their physical significance. The first term, $\vec{E}\cdot\vec{J}$ represents the Joule heating (resistive heating) component of the heat generation. The second term in the definition, $\left(E_g + 3k_BT\right)R$, is the heat generated when an electron and a hole recombine. Heat from this type of process can be transferred directly to the lattice (produces a phonon) or another charge carrier can be created (known as Auger recombination). In this equation E_g is the bandgap, $3k_BT$ represents the average kinetic energy of both the electron and hole, and R represents the rate of recombination. The term R has its roots in the Boltzmann transport equation and is usually approximated by the use of relaxation times. Analytic expressions for relaxation

times for various recombination mechanisms can be found in [34]. The third and fourth terms describes energy that is released/absorbed from an electron/hole that transitions from one minimum in the conduction band to another minimum; in the hole sense from one valence band maximum to another maximum. These types of transitions arise from variations in material composition where the bandgap differs. The $\vec{J}_{n,p}$ term represents the electron/hole current density, χ is the band energy offset, and the $3k_BT/2q$ term accounts for a type of convection. The term convection is used to describe the process of moving energy from a hot region to a cold region in the device by electron/hole motion. The fifth term of the heat generation arises directly from Peltier effects of the material; this type of heating is also called Thompson Heating. The last two terms can often be neglected since most studies are under steady-state conditions.

While the heat generation can be cumbersome to obtain, significant simplifications can be made for most types of devices. The magnitude of Joule heating dominates over the other steady state effects. Models based on Joule heating alone are acceptable as long as the working material does not posses any large Peltier (thermoelectric) effects. The effects of the transient terms have been estimated to be up to ~25% of the Joule heating magnitude for the turn off cycle of a bipolar power transistor [29]. However the time scales are <1μs which allows the use of purely Joule heating based models, at least as a first order approximation. Other simplifications might be made to the generation term but they would depend strongly on the structure of the electron bands, and thus the material chosen.

2.2 Current Cooling Technologies

2.2.1 Cooling of High Power Electronics

Many common cooling technologies rely on heat removal through the substrate that the device is built on because of the ease with which heat sinks can be implemented. The thermal resistance in this direction is a strong function of the substrate thermal conductivity and crystal quality (i.e. dislocation density). The large thermal resistance of the substrate and the lattice strained interfaces inherently impedes this method of heat dissipation as opposed to heat removal from the front of a device. Thus, methods of heat dissipation that can utilize the surface area on top of the devices may be more advantageous to thermal management of some GaN power devices.

Heat removal technologies including two-phase convection from boiling and thin-film evaporation are expected to provide the highest heat flux removal rates. This two-phase cooling may be facilitated through recently developed technologies such as spray cooling from synthetic microjets, droplet atomization, mist flow or immersion [12, 13, 35, 36]. Two-phase cooling is effective because of the large latent heat of vaporization that most liquids posses, however it is desirable to use inert fluids so as not to cause electrical problems. Dielectric fluids do not pose a short circuit threat and fluorochemical liquids such as FC-87, PF-5052 and FC-72 have saturation temperatures of 32.0, 50.0, and 56.6^{o}C (at 1atm) respectively which allow for reasonable device temperatures to be maintained [37]. Even though these fluids show promise for cooling applications their low latent heat values, up to 25 times smaller than water, makes them somewhat less effective. Typical convection coefficients that are obtainable with fluorochemicals are in

the 1-10 W/cm^{2}K range, whereas convection coefficients for water can reach up to 100W/cm^{2}K. In Figure 8 a schematic of a pool boiling cooling situation for a multichip module in a dielectric fluid is shown. Pool boiling dielectric fluids enables higher convection rates when compared to forced air convection but ultrahigh convection rates are hampered by surface bubble formation. By utilizing a micro-boiling package there is a rapid energy extraction due to the small amount of fluid that is being evaporated at any given moment. In addition there is also a "sweeping" phenomenon that is associated with many spray-boiling techniques. The impinged jets of liquid tend to remove the nucleate bubbles and provide a constant supply of liquid to the surface in order to ensure a continuous evaporation regime. In Figure 9 a microjet array cross-section is shown. Microjet arrays have been shown to theoretically dissipate powers of up to 500W with water as the working fluid [35].

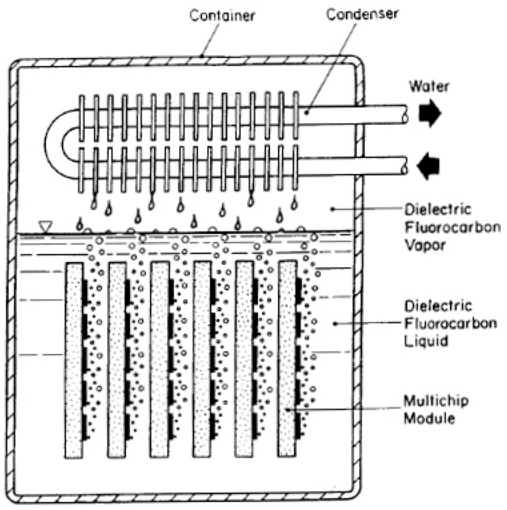


Figure 8. A schematic of a dielectric fluid-cooling module for an avionics application. Notice that the multichip boards are simply submerged into the fluid and allowed to boil the surrounding liquid; a closed fluid loop is used as the condenser. From [37].

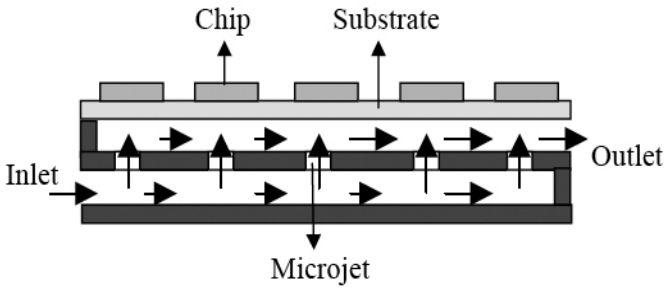


Figure 9. Diagram outlining the theoretical model of a microjet array package for high heat flux removal from power electronics. Jets can be made with standard silicon microfabrication techniques. Note that water is an option for the working fluid since it is possible to isolate the electronics from the stream. From [35].

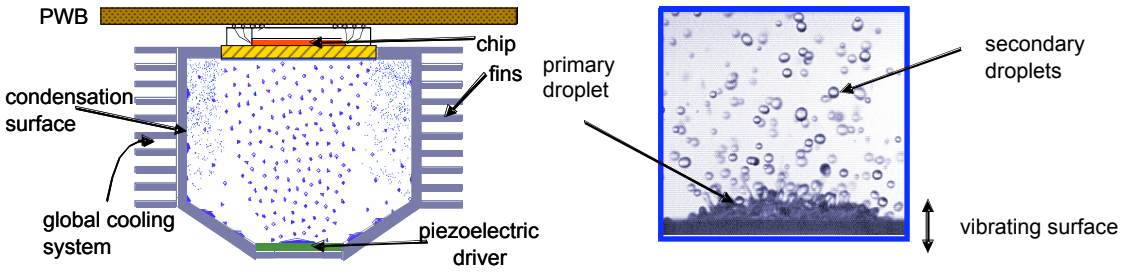


Figure 10. Vibration Induced Droplet Atomization (VIDA) cooling package. Here a piezoelectric driver vibrates at a high frequency and causes the working fluid to atomize and spray over the heat generation region of the chip. From [13].

Similar to the microjet cooling technique is a spray-cooling module shown in Figure 10; the difference is that the spray can be localized on to the top of the chip where there is a smaller thermal resistance from the active area. Heat fluxes over 100W/cm^2 have been realized while keeping the chip temperature below 100^{o}C with this technique [13].

In addition to open two-phase cooling configurations advancements in closed loop heat pipe design also make them an effective heat removal tool. Principles of heat pipe operation are similar to other two-phase systems where a working fluid is evaporated and then condenses elsewhere in the system resulting in a removal of heat from the source.

The difference is that a wicking mechanism is present in a heat pipe in order to draw the liquid phase back towards the heat source to be re-evaporated instead of having active components delivering the fluid. A schematic is shown in Figure 11.

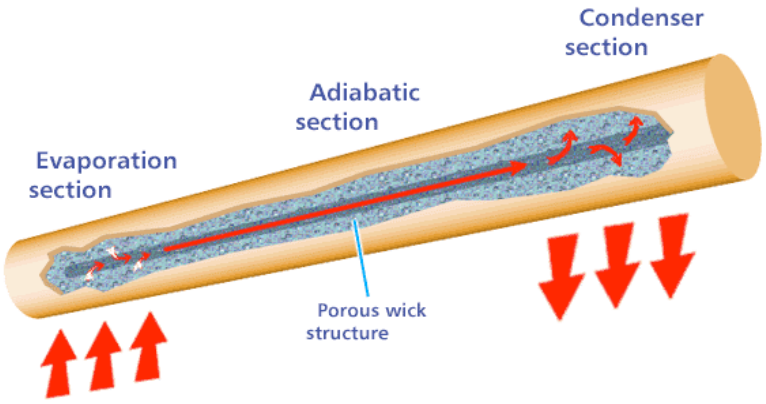


Figure 11. Cross section view of a heat pipe exposing the wicking material along the sidewalls of the pipe. From [38].

Pulsed heat pipes have been designed in order to dissipate up to 250W/cm^2 from a source, making them an attractive option for cooling schemes where space is limited or where liquid spraying is not an option [39]. Heat pipes are especially popular in notebook computers [40].

2.2.2 Cooling of Optoelectronics

The advantages of these technologies are that high heat flux removal with localized control is possible while maintaining reduced device temperatures. Topside convection cooling schemes also allow low cost substrates like sapphire to remain viable for advanced GaN devices. However there are inherent problems with topside cooling configurations when working with optoelectronics; efficient light extraction is usually

inhibited by the extensive packaging requirements for spray-type systems. This problem will be addressed in paragraphs to follow.

Recent trends in optoelectronics' packaging have been towards the development of advanced devices on SiC and GaN substrates due in part to their high thermal conductivity. High thermal conductivity substrates are attractive for device growth because there is a significant thermal resistance as a result of the more common low thermal conductivity substrates (sapphire, lithium gallate, and zinc oxide). Being able to extract light dictates that heat be removed from the backside of the device and as a result there is a push for novel packaging methodologies. Flip chip bonding is a popular method of chip attachment that allows for heat removal by conduction through the topside of the optoelectronic device; the transparent nature of the sapphire substrate makes it possible to emit light. Below is a diagram of a typical flip chip bonded device.

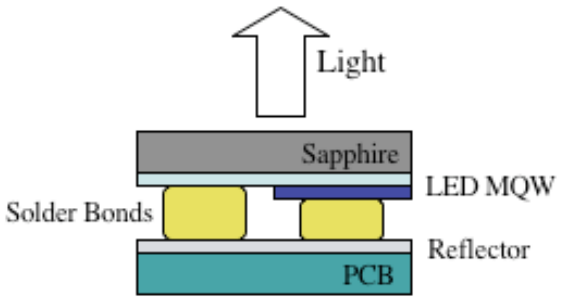


Figure 12. A simplified view of a flip chip bonded device. The main advantage is that heat can be removed from the active layers through the solder bonds without worrying about the added thermal resistance of the sapphire substrate.

Incorporating high thermal conductivity composite materials into the design of the package also helps reduce the overall thermal resistance. Metal matrix composites that

have ultrahigh thermal conductivities (>400W/mK) due to mixing of the component materials are being introduced into high power LED packages, although they are still not widely used. Current materials include copper impregnated with chemical vapor deposited (CVD) diamond particles, aluminum with graphite flakes and more recently carbon nanotubes are being incorporated into copper [15].

All of these cooling methods show great potential for the continued development of high power electronics. However each method needs design attention in order to optimize the system as a whole.

2.3 Roadmap for Cooling in High Power Electronics

The 2005 International Technology Roadmap for Semiconductors (ITRS) on assembly and packaging calls for a maximum power dissipation of 0.98W/mm^2 for a single chip by 2013 [41]. This level of power dissipation demands an aggressive cooling scheme, like those discussed in the previous section. Outlined in Table 1 are the equivalent thermal resistances that are required in order to achieve the maximum junction temperatures that have been specified by the ITRS. The values that are specified are from the junction of the device to the ambient.

Table 1. An outline of the ITRS roadmap and the thermal requirements for the chip system. For comparison a desktop computer would correspond to a "cost-performance" system, a high-end server would correspond to a "high performance" system and a power electronics module would correspond to a "harsh" system.

Year of Production	2006	2007	2008	2009	2010	2011	2012	2013
Maximum Power (W/mm^2)								
Cost-Performace	0.7	0.74	0.79	0.83	0.85	0.85	0.89	0.98
High Performance	0.58	0.61	0.64	0.64	0.64	0.64	0.64	0.64
Harsh	0.18	0.18	0.2	0.2	0.22	0.22	0.24	0.25
Maximum Junction Temperature (°C)								
Cost-Performace	100	95	95	90	90	90	90	90
High Performance	100	95	95	90	90	90	90	90
Harsh	175	175	175	200	220	220	220	220
Maximum Ambient Temperature (°C)								
Cost-Performace	45	45	45	45	45	45	45	45
High Performance	55	55	55	55	55	55	55	55
Harsh	150	150	150	150	200	200	200	200
Chip Size (mm^2)								
Cost-Performace	140	140	140	140	140	140	140	140
High Performance	630	662	695	729	766	804	750	750
Harsh	100	100	100	100	100	100	100	100
Required Thermal Resistance (K/W)								
Cost-Performace	0.56	0.48	0.45	0.39	0.38	0.38	0.36	0.33
High Performance	0.12	0.10	0.09	0.08	0.07	0.07	0.07	0.07
Harsh	1.39	1.39	1.25	2.50	0.91	0.91	0.83	0.80

It can be seen from Table 1 that all levels of the power electronics packaging are significant. As a parallel to the power electronics industry the solid-state lighting industry also suffers from heat removal issues. Outlined in Table 2 are roadmap values for power dissipation and thermal resistances needed in order to achieve reliable devices.

Table 2. Solid state lighting roadmap as proposed by the 2002 Optoelectronics Industry Development Association (OIDA) [23]. For comparison purposes typical values for incandescent and fluorescent light sources are provided. **As specified by a 2005 Lumileds Luxeon Emitter lamp.

Year of Production	2002	2007	2012	2020	Incandescent	Fluorescent
Luminous Efficacy (lm/W)	25	75	150	200	16	85
Lifetime (khr)	20	>20	>100	>100	1	10
Flux (lm/lamp)	25	200	1000	1500	1200	3400
Lumens Cost ($/klm)	200	20	<5	<3	0.4	1.5
Lamp Cost ($/lamp)	5	4	<5	<3	0.5	5
Color Rendering Index (CRI)	75	80	>80	>80	95	75
Maximum Power (W/lamp)	1	2.7	6.7	7.5	75	40
Maximum Junction Temperature (^oC)**	120	120	120	120	N/A	N/A
Maximum Ambient Temperature (^oC)**	85	85	85	85	N/A	N/A
Chip Size (mm^2)**	4	4	4	4	N/A	N/A
Required Thermal Resistance (K/W)	8.75	3.24	1.31	1.17	N/A	N/A

Chapter 5 will discuss in more detail how to design a low thermal resistance package.

2.4 Growth Methods of Semiconducting Thin Films

Demands for more advanced devices has required that growth methods also be refined in order to achieve high levels of material quality and atomic layer deposition control. Outlined here are several popular growth methods, their advantages and disadvantages, that illustrate the evolution of this technology starting with CVD leading to molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD).

A conventional CVD system is shown in Figure 13. Hydrogen gas is bubbled into an $AsCl_3$ bath and the vapor mixture flows over a gallium bath where gallium in the vapor phase travels to the GaAs substrate and condenses onto the surface. Adding

additional solid sources to the flow chamber makes it easy to incorporate dopants and other alloying materials such as aluminum. However controlling the deposition rate onto the substrate is difficult as it depends strongly on the flow kinetics in the system as well as the substrate temperature. Another disadvantage of CVD is a result of the high growth temperatures; the interdiffusion of materials makes it difficult to grow multilayer structures. There have been improvements on the reactor design, one of which is shown in Figure 14 that includes a rotating substrate holder that results in greater uniformity over the substrate. Chemical vapor deposition is also known as vapor phase epitaxy (VPE).

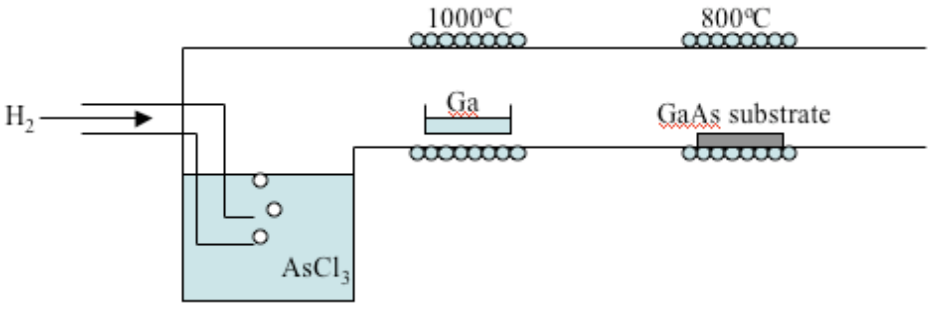


Figure 13. A schematic of a chemical vapor deposition system for deposition of GaAs thin films onto a GaAs substrate.

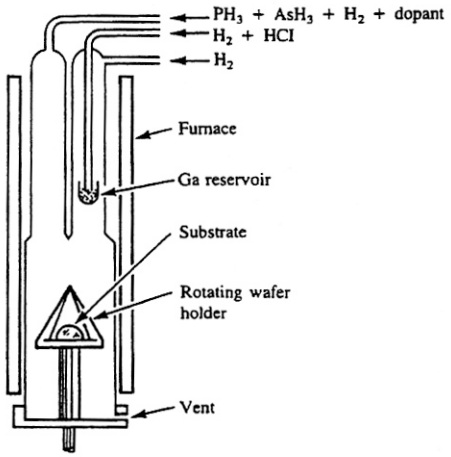


Figure 14. Schematic of a CVD/VPE chamber with a rotating wafer holder that allows for more uniform depositions across the substrate. From [42].

One of the most promising technologies for high volume production of current device fabrication is metal-organic chemical vapor deposition (MOCVD). To avoid some possible confusion, MOCVD is also known as organometallic vapor phase epitaxy (OMVPE), organometallic chemical vapor deposition (OMCVD), and metal-organic vapor phase epitaxy (MOVPE). MOCVD is similar to the conventional CVD system discussed previously but there are important reactor design considerations that make MOCVD superior. The metal-organic materials are the sources for the growth and similarly they are bubbled with hydrogen gas and passed into a reactor chamber. The metal-organics are liquid at room temperature and therefore the flow of reactants can be easily controlled with mass flow controllers. The reacting chamber also maintains a lower temperature that minimizes the diffusion of doping/alloying materials. The combination of these design changes allows for compositionally abrupt surfaces within the device and has resulted in state of the art devices. A typical schematic of an MOCVD system is shown in Figure 15.

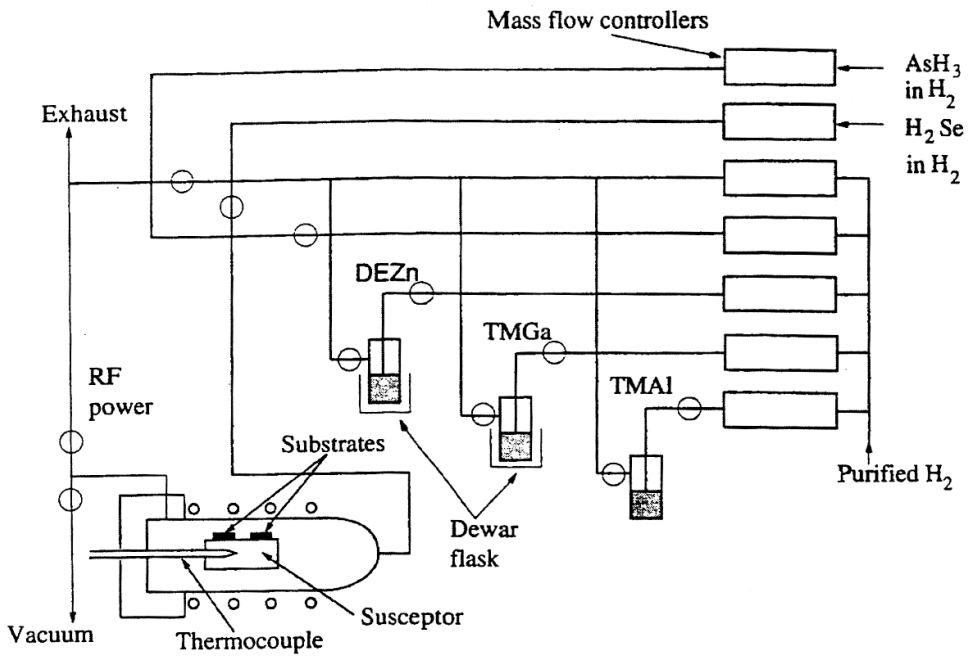


Figure 15. MOCVD schematic. It is easy to incorporate new metal sources by changing the metal-organic bubbler. DEZn, TMGa, and TMAl are diethylzinc, trimethylgallium, and trimethylaluminum respectively. From [43].

While MOCVD reactor systems can achieve atomic layer deposition it is still difficult to control due to residual gases in the line post mass flow controller. Characterization techniques such as pyrometry and deposition monitoring have been incorporated into the reactor chamber it is difficult to obtain information about the quality of the growth in situ.

With a MBE type system it is possible to obtain monolayer deposition due to the incorporation of shutters near the effusion sources, which allow for abrupt changes in the deposition composition. The MBE chamber must be kept under ultra-high vacuum ($<10^{-9}$ Torr) to allow for a long enough mean free path of the thermally evaporated materials to reach the substrate. This leads to an extensive pumping system and often the sidewalls are cooled with liquid nitrogen to condense any extra materials. The main advantage that

MBE has over MOCVD is that a Reflection High Energy Electron Diffraction (RHEED) characterization tool can also be incorporated into the chamber. With RHEED it is possible to monitor single island-type nucleation sites on the substrate and therefore one can resolve monolayer growth; this in situ type characterization has made MBE a key research tool for state of the art devices. A typical MBE system is shown in Figure 16.

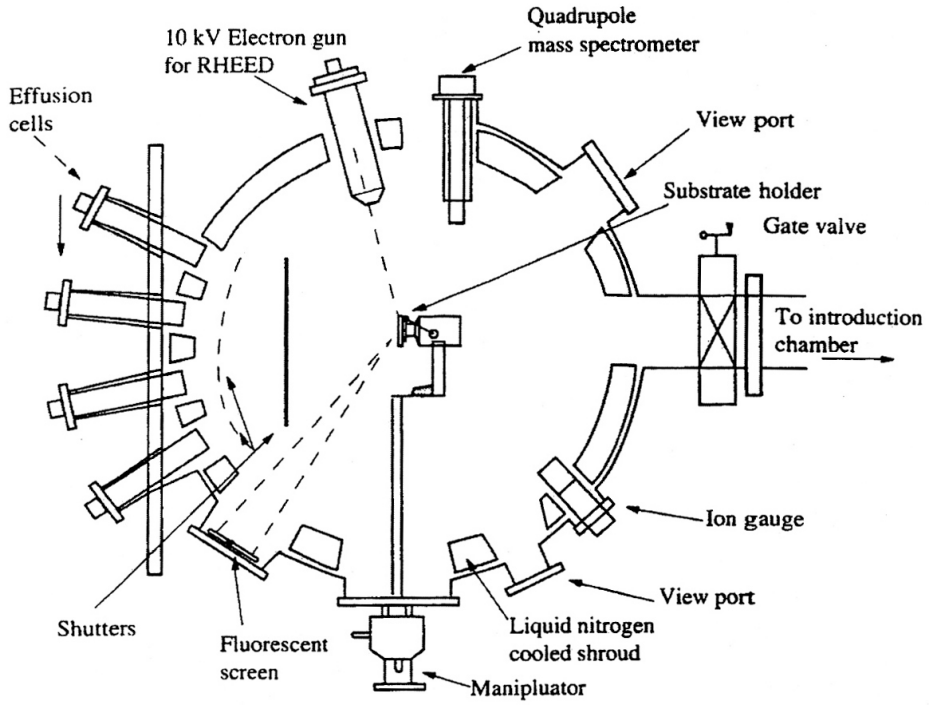


Figure 16. A MBE growth chamber incorporated with RHEED and a mass spectrometer for growth characterization. Notice that only one substrate at a time can be loaded at a time; MBE suffers from low throughput and therefore is not used on production lines. From [44].

2.5 Dislocation Formation

It was previously mentioned that the thermal conductivity of thin film materials is a strong function of the dislocation density. In addition to the thermophysical properties, electronic and optical properties can degrade quickly with the introduction of dislocations. Dislocations are areas within the crystal where the atomic periodicity is broken due to bonds no longer lining up in a regular manner. Threading, screw and edge dislocations are all specific types of dislocations and are illustrated in Figure 17.

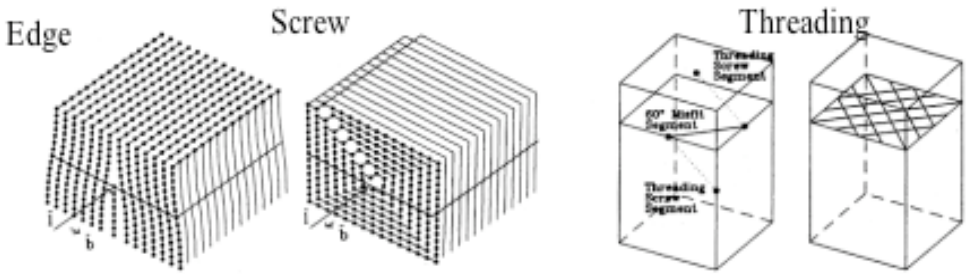


Figure 17. The three types of dislocations encountered when growing thin films epitaxially. Edge dislocations can be designed into a device as a way to introduce stress that would change the electronic band structure in a way that could enhance the performance. From [45].

Introducing edge dislocations can actually improve the electronic properties at a heterojunction by causing the band structure to change in that localized area, but most dislocations are detrimental to high performance device operation. As a result of the shift in periodicity of the lattice there are usually dangling bonds within the material. These free bonds act as charge carrier traps for non-radiative electron-hole recombination, which is exactly the opposite of what is desired in optoelectronic devices. Instead of a photon being emitted during the electron recombination, heat is released in the form of a

phonon. This trapping of charge carriers and self-heating is responsible for many problems in high power electronics as well as optoelectronics. The heat that is generated in the device must migrate towards lower temperatures, but dislocations also act as scattering site for phonons and result in a lower material thermal conductivity. In Figure 18 it is possible to see threading dislocations that form from a rough surface, in this case $LiGaO_2$.

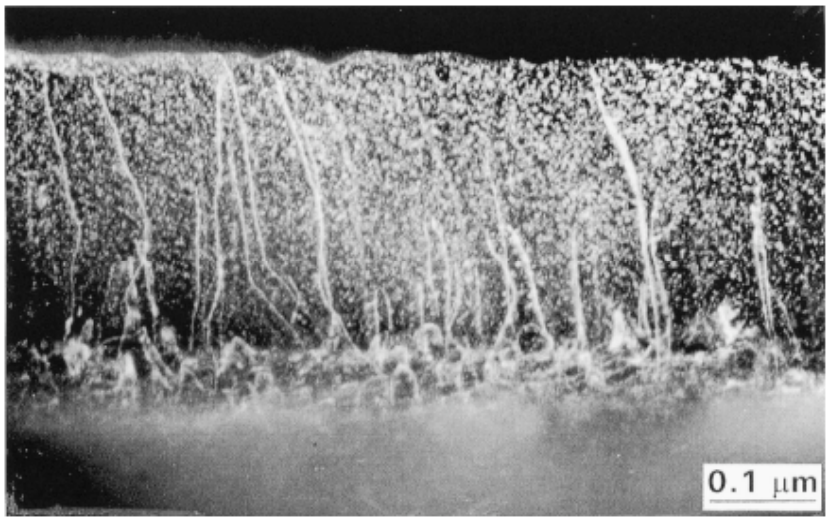


Figure 18. A cross-section TEM image of threading dislocations in GaN that has been grown by MBE on $LiGaO_2$. From [16].

This circular feedback has motivated research to improve the material quality of these thin films. Techniques such as growing strained buffer layers, laser liftoff transferring, or bonded substrate removal can all lead to high quality GaN films.

CHAPTER III

CHARACTERIZATION OF THIN FILM MATERIALS

The following chapter introduces several technologies that are used in order to characterize crystalline thin films. Techniques that are introduced will allow qualitative information to be gained about the crystal quality, thermal conductivity, and temperature. This review aims to give the reader a general knowledge of how to characterize thin films and the challenges that are faced when performing these experiments.

3.1 Crystal Quality

Crystal quality is of primary importance for development of high performance devices. In §2.5 the effect of dislocations as charge trapping and phonon scattering sites was discussed. It will be reiterated that high quality crystalline materials are needed for predictable and efficient behavior of both high power electronics as well as optoelectronics. There are several very common methods of characterizing crystalline materials that allow for the determination of lattice constants, crystal shape, surface roughness, and many other properties. Of the most widely used are Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), X-Ray Diffraction, Atomic Force Microscopy, Cathodoluminescence, and Scanning Tunneling Microscopy for probing the physical parameters of the material. In this work the primary concern was directed towards methods that would be able to render information about the dislocation density and relative crystal quality within the thin film. Methods available that were utilized were X-Ray Diffraction (XRD) and a wet etching technique coupled with Atomic

Force Microscopy (AFM); these will be discussed in more detail in the following sections.

3.1.1 X-Ray Diffraction

X-ray diffraction is one of the most widely used techniques to gain information about materials whether in bulk crystalline form or as thin films, as in the case of this work. In this technique high energy x-rays that correspond to wavelengths in the 0.06nm to 10nm range bombard the surface of the sample. Due to the small wavelengths most of the x-rays can penetrate through the sample without interference from the crystal lattice. There are, however, some x-rays that will encounter an obstacle (an atomic position) where they will be scattered back towards the source as in Figure 19.

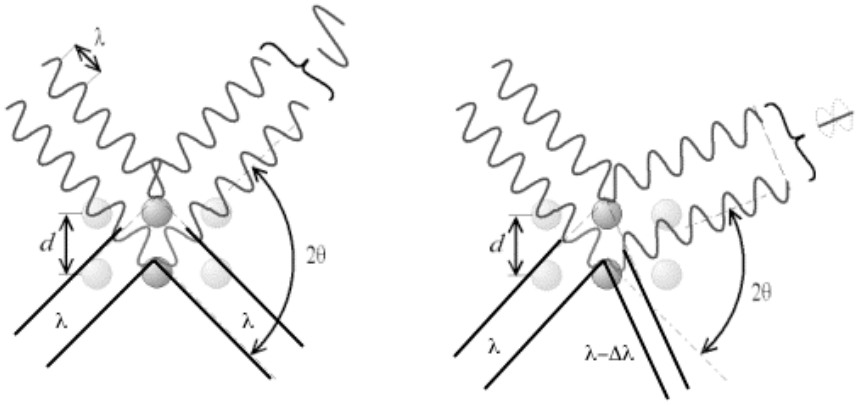


Figure 19. X-ray scattering from two different atomic planes. The marked wavelength sections indicate the path difference between the two scattered waves giving rise to an interference pattern to be observed.

The backscattered x-ray interference (diffraction) pattern that is observed gives information about the atomic spacing in the lattice from Bragg's Law (2).

$$n\lambda = 2d\sin\theta \tag{2}$$

During data collection the x-ray source rotates around the sample in order to obtain a full spectrum through the rocking angle, θ. The resulting diffraction pattern due to a generalized crystal structure shows many peaks in the reflected intensity as the detector encounters new crystallographic planes. In the case of a perfect crystal where the order is infinite the x-ray diffraction pattern would show peaks at discrete angles as shown in Figure 20

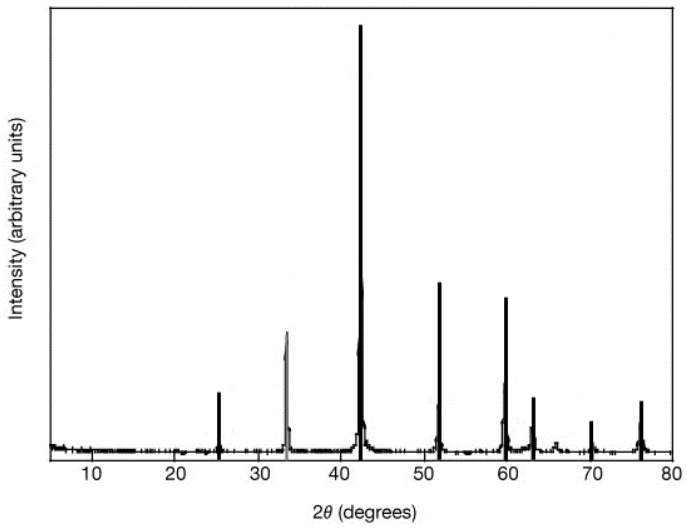


Figure 20. A real XRD spectrum as a function of angle. An ideal crystal diffraction spectrum from a perfect crystal (spikes).

The broadening in the in peak width arises from small variations in the crystal dimensions throughout the sample. This broadening can be measured as a full width half

maximum value (FWHM) and can be used to make comparisons about the crystal quality; the more broadening the more variations in the crystal which implies lesser quality.

The GaN that was obtained for study was grown on (0001) sapphire wafers that cause the c-axis to grow vertically. Since the preferred growth direction was along the c-axis the (0002) direction in the GaN was used for comparison among samples. In Figure 21, Figure 22, and Figure 23 are XRD rocking curves that show the width of the (0002) peak.

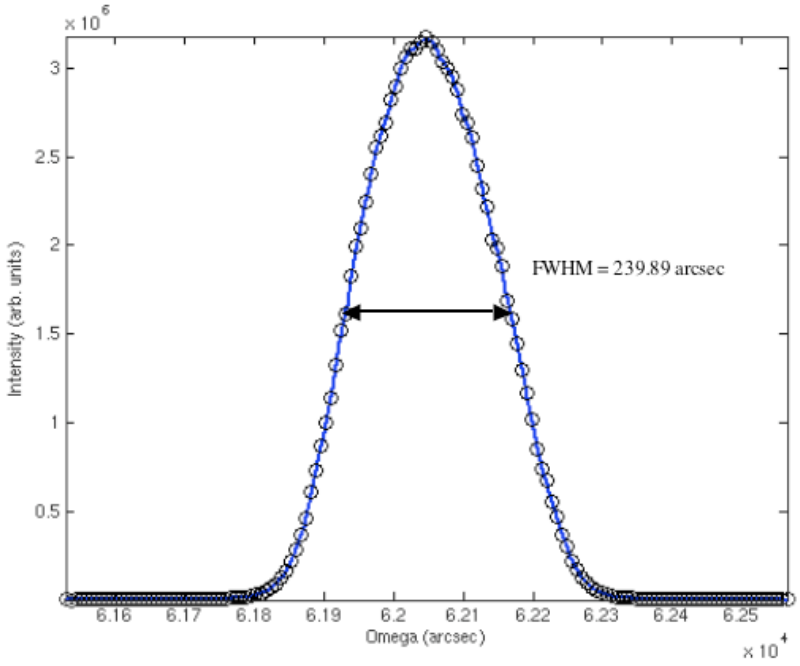


Figure 21. Undoped GaN x-ray rocking curve along the (0002) direction showing a FWHM of 239 arcsec.

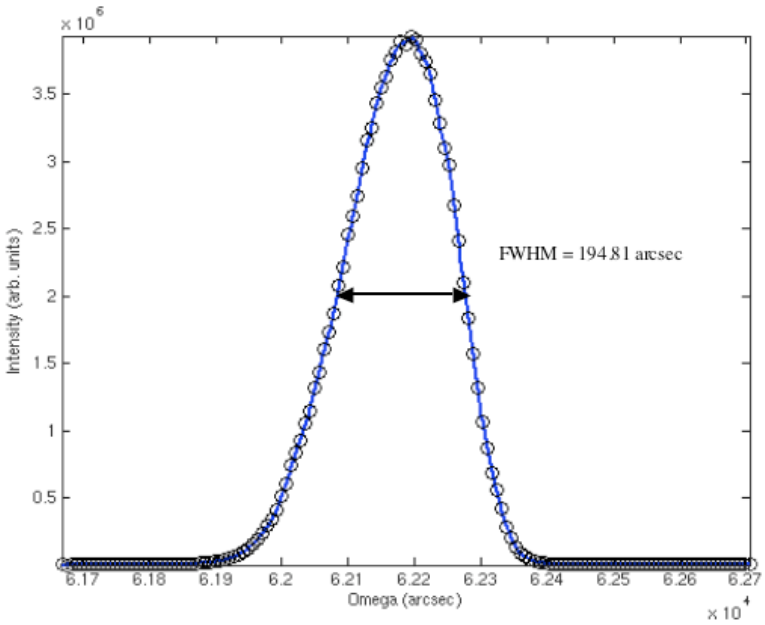


Figure 22. P-doped (Mg is the substitutional atom) GaN x-ray rocking curve along the (0002) direction showing a FWHM of 194 arcsec.

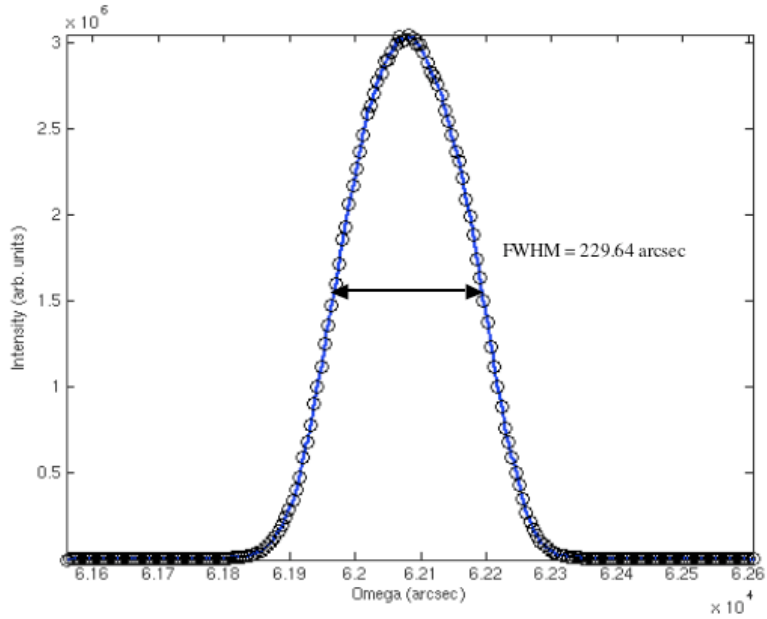


Figure 23. N-doped (Si is the substitutional atom) GaN/Undoped GaN two-layer structure x-ray rocking curve along the (0002) direction showing a FWHM of 229 arcsec.

In addition to observing samples of GaN with XRD a sample of zinc oxide (ZnO), a new substrate material for c-axis GaN growth was observed. In shows the rocking curve of the single crystal sample has been grown by using a pressurized melt process.

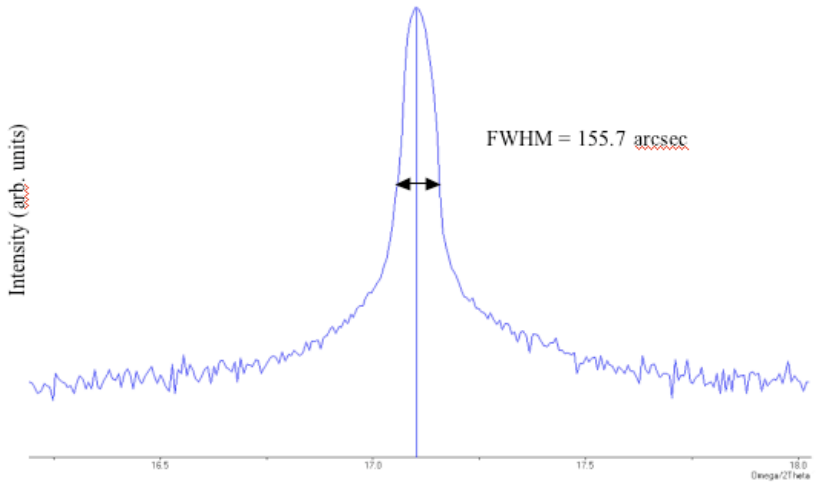


Figure 24. Single crystal ZnO sample x-ray rocking curve measured along the (0002) direction showing a FWHM of 155.7 arcsec.

In Table 3 a summary of the results is made. Since the FWHM does not give exact measures of disorder in the crystal only comparisons can be made. Previously reported that GaN grown by the MOCVD process on (0001) sapphire had typical FWHM values of the (0002) peak around 1000-1250 arcsec [46]. These results were reported in 1996 and since then there have been improvements in the growth methods which have produced typical FWHM values around 250-350 arcsec, which reveals that the obtained GaN samples were of high quality [47, 48]. The variation in the Mg and Si doped samples from the pure GaN sample could be due to other growth parameters that affected the crystal quality favorably.

Table 3. Summary of results from XRD of GaN and ZnO samples.

Sample	FWHM (arcsec)	Notes
Undoped GaN	239.89	MOCVD grown on sapphire (~1μm thick)
P-type GaN	194.81	MOCVD grown on sapphire with Mg doping
N-type/Undoped GaN 2 Layer Structure	229.64	MOCVD grown on sapphire with Si doping
ZnO	155.7	Pressurized melt growth

3.1.2 Wet Etching/Atomic Force Microscopy

Atomic Force Microscopy is another common characterization technique that can be used in order to gain information about the grown crystal. Surface roughness and approximations of the dislocation density can be obtained by performing a wet etch of the surface. In this technique a silicon cantilever probe with a tip radius on the order of 20nm is scanned across the surface with constant force while a photodetector tracks the deflections of the beam caused by variations in the topography. Using an AFM system allows height variations on the order of angstroms to be resolved. This resolution allows for visualization of growth planes and any islands that might have formed that would lead to dislocation formation.

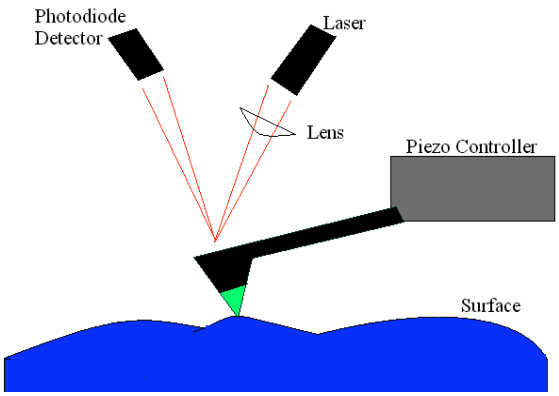


Figure 25. AFM operating in constant force contact mode while scanning the surface of a MOCVD grown GaN thin film. Adapted from [49].

In keeping with the same notation used previously for the samples Table 4 is provided which outlines the results of roughness scans. The roughness results from the formation of steps that occur during the kinetics of the growth process. This is an undesirable phenomenon as it can cause irregular growth that leads to dislocation formation.

Table 4. Surface roughness measurements on MOCVD grown GaN on a (0001) sapphire wafer. The data shows the largest roughness in the undoped GaN sample.

Sample	Max (nm)	Min (nm)	RMS Roughness (pm)	σ (pm)
Undoped GaN	2.892	-5.105	332.296	332.299
N-type/Undoped GaN 2 Layer Structure	0.625092	-0.5949	176.565	175.817

In addition to observing the crystal growth planes with an atomic force microscope it is also possible to gain information about the dislocation density of the material. Multiple studies have shown that performing a wet acid etch prior to AFM

scanning can reveal locations of dislocations due to the difference in the etch rate between the bulk material and the area in the vicinity of the dislocation; by counting the etched feature it is possible to obtain the density of defects [50-56]. Different types of defects appear as different features when wet etched; the polarity of the terminating surface also plays a vital role in the shape of the etching [53]. Youtsey showed that both mixed and edge type dislocations could form whiskers when etched in a photochemically enhanced 0.02M KOH solution. Ng showed that etching in a 2M solution of KOH with a Ga-polar material can form pyramids; if the surface was N-polar then hexagonal pits were observed (Figure 26). Further features show up as micropipes, hillocks, and protrusions as seen in Figure 27 [57-66]

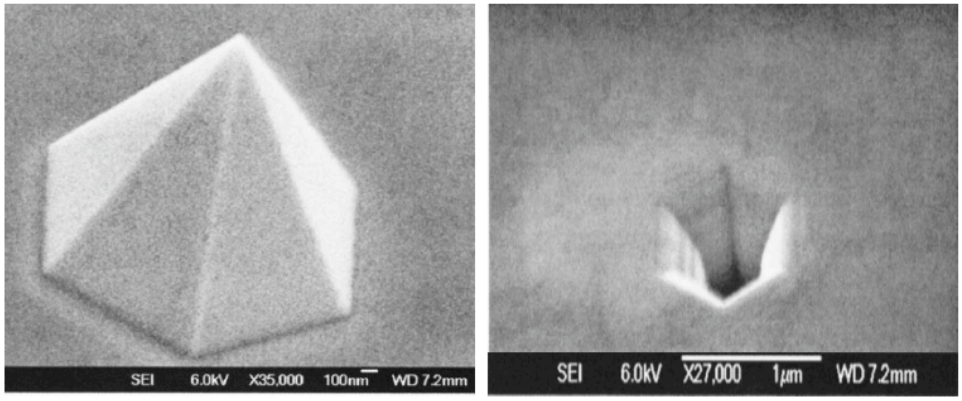


Figure 26. KOH Wet etched features at dislocation sites of Ga-polar (left) and N-polar (right) GaN. From [53].

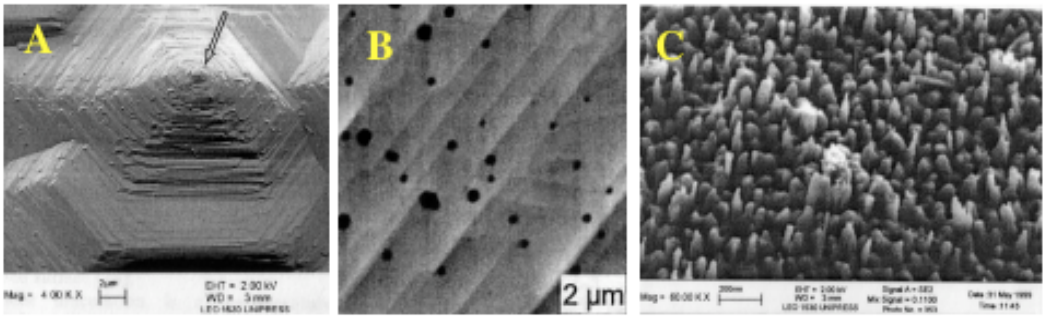


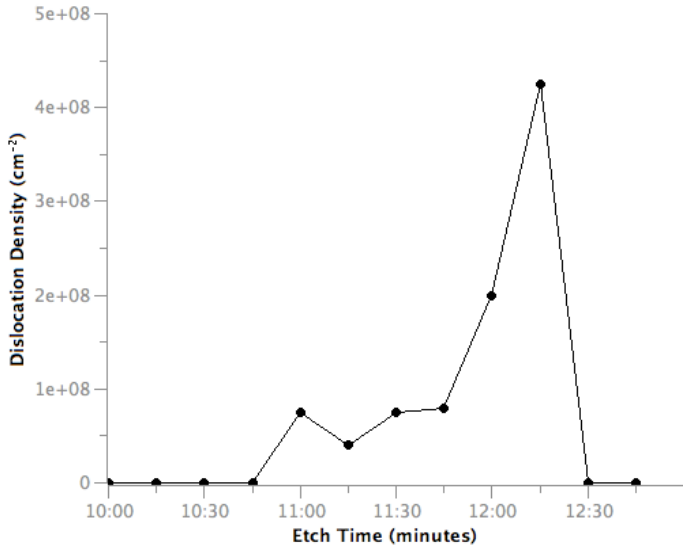
Figure 27. (A) Hillock formed by wet etch in a 3:1 H_2SO_4/H_3PO_4 solution at 60°C for 2 minutes. From [57]. (B) Micropipe formation after a molten KOH etch at 210°C for 2 minutes. From [58]. (C) Protrusions formed by a 0.02M KOH solution for 10 minutes. From [57].

A sample of MOCVD grown GaN on a (0001) sapphire wafer was wet etched using an 180°C bath of H_3PO_4 at 30-second intervals. In between each etch several AFM scans were taken at different areas of the sample in order to observe the dislocation density. It was found that a dislocation density of ~4.25×10^8 cm^{-2} existed in this sample of GaN, making it of high quality. A summary of the findings is presented in Table 5.

While the wet etching method is convenient to use it is subject to errors due to the randomness of the dislocation growth. The nature of the technique allows the characterization of surface defects or ones that penetrate through the sample. However the true dislocation density (found with Transmission Electron Microscopy) can be up to 10^4 times larger due to defects that do not terminate at the surface [59]. Even with its deficiencies the wet etching method is still utilized because of the ease with which it can be performed.

Table 5. A graph of the MOCVD GaN sample wet etched in hot (180°C) H_3PO_4 for the specified times. All etch features were ~100nm in diameter and up to 50nm in height and

were quickly etched once observed at 11:30. As a consequence of the features being raised it is deduced that this GaN sample had a N-polar terminating surface.



3.2 Thermal Conductivity

There is an intimate link between the microstructure of a crystal and the thermal conductivity. The previous analysis of the crystal quality and the dislocation density can now be used in order to more fully understand the values for thermal conductivity. The thermal conductivity of thin films can be found by several techniques, which include modulated thermoreflectance, scanning thermal microscopy, the 3ω method, among others. In this work the 3ω method was used in order to determine the material properties of the thin films. The 3ω method was chosen due to its ability to test materials in a wide range of temperatures, which is important to consider when designing high power device packaging. A detailed derivation and explanation is provided in §3.2.1.

3.2.1 3ω Method and Extensions

The concept of the 3ω method was originally proposed by Cahill and then further developed by many other groups to make it a very powerful testing tool [67]. Testing methods prior to the 3ω method relied on macroscopic measurements of a temperature gradient in a material that resulted from a steady heat source. This type of testing, sometimes called the guarded-hot plate method, is prone to heat losses by convection and radiation and therefore requires careful test design to prevent over prediction. Another method called flash diffusivity relies on the a transient measurement of a heat spot size. Direct measurement of the thermal conductivity is not possible other tests to determine the thermal capacity must be performed. A method that accommodates the low dimensionality of the thin film system and is able to extract the thermal conductivity directly is the 3ω method.

The 3ω method relies heavily on the ability to pattern a micro-heater onto the surface of the material to be tested. This metal wire is usually on the order of 100 nm thick, 20 μm wide, and 3 mm long, which allows for the simplifying 2D assumption to be made. This metal wire, when an AC voltage is applied, acts as both the heater and the thermometer (Figure 28). The AC voltage at ω causes heat to be dissipated at 2ω due to periodic Joule heating within the wire diffuses through the sample and causes the wire to cool down in a periodic fashion. In turn, this causes a resistance change and an artifact at 3ω in the voltage signal can be detected and later correlated to the material properties of the sample.

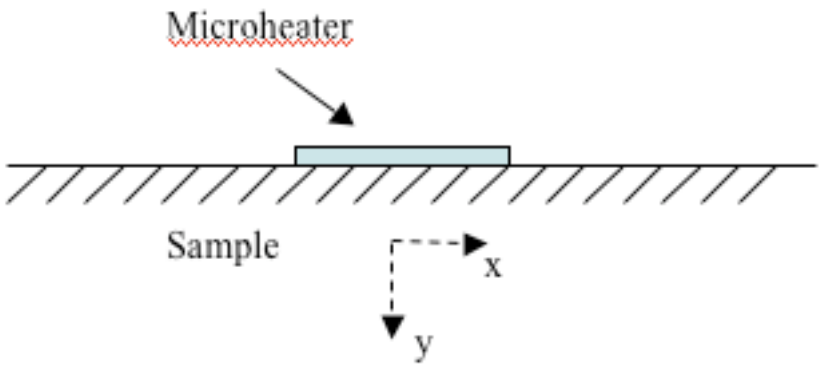


Figure 28. 2D cross-section of the microheater used in 3w testing. Adopted from [67].

When Cahill first introduced the 3ω solution to the temperature distribution in terms of a single radial coordinate, *r*, this limited the types of samples that could be tested to single bulk material. This solution was then modified to account for a thin film of a low thermal conductivity material (usually SiO_2). The modified solution assumed a 1D thermal resistance of the thin film and therefore restricted the material system to low thermal conductivity materials on a substrate [68]. The development of multilayer microelectronic structures led to the development of a generalized 3ω solution that accounted for the 2D nature of the heat flow in an N layer system [69, 70]. The solution also lifted the restrictions of having isotropic low thermal conductivity thin films so that anisotropic high thermal conductivity thin films could now be measured [69, 70]. Thermal conductivity measurements of materials that are not planar have also been performed with success [71]. The details of this derivation are outlined in the following section.

3.2.1.1 Generalized 3ω Solution

The geometry of the micro heater allows for a 2D approximation of the heat flow to be made and making an argument about the symmetry of the heater simplifies the boundary value problem to a quarter plane. The temperature distribution is defined by solution of the time dependent 2D heat equation for the n^{th} layer.

$$k_x \frac{\partial^2 T_n}{\partial x^2} + k_y \frac{\partial^2 T_n}{\partial y^2} = \rho c_p \frac{\partial T_n}{\partial t} \qquad n = 1,2,...N \tag{3.1}$$

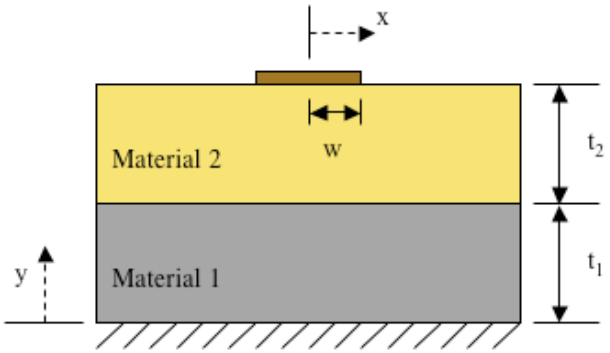


Figure 29. Diagram of the generalized 3ω material system with coordinate and symmetry system that was used for the analytical solution. Adopted from [72].

The driving frequency ω will cause Joule heating in the wire at a frequency of 2ω and would therefore expect to see a periodic temperature fluctuation in the form of (3.2).

$$T_n = \mathrm{T}_n e^{i2\omega t} \qquad n = 1,2,...N \tag{3.2}$$

That then, upon substitution, transforms the heat equation into (3.3).

$$\alpha_{x_n}\frac{\partial^2 \mathrm{T}_n}{\partial x^2}+\alpha_{y_n}\frac{\partial^2 \mathrm{T}_n}{\partial y^2}=i2\omega \mathrm{T}_n \qquad n=1,2,...N \tag{3.3}$$

It is now possible to solve this problem with separation of variables approach however this leads to a complicated solution so a Fourier Transform approach can be used in order to simplify the solution [70, 72]. Recalling that the Fourier Transform and Inverse Transform are

$$\hat{f}(\lambda)=\int_{-\infty}^{\infty} f(x)e^{-i\lambda x}dx \tag{3.4}$$

$$f(x)=\frac{1}{2\pi}\int_{-\infty}^{\infty} \hat{f}(\lambda)e^{-i\lambda x}d\lambda \tag{3.5}$$

By applying the forward transform to equation (3.3) and defining a new quantity Φ yields an ordinary differential equation.

$$\frac{d^2\hat{\mathrm{T}}_n}{dy^2}-\Phi^2\hat{\mathrm{T}}_n=0 \qquad n=1,2,...N \tag{3.6}$$

$$\Phi_n=\sqrt{\frac{\alpha_{x_n}}{\alpha_{y_n}}\lambda^2+\frac{i2\omega}{\alpha_{y_n}}} \qquad n=1,2,...N \tag{3.7}$$

$$\hat{\mathrm{T}}_n=A\sinh(\Phi y)+B\cosh(\Phi y) \qquad n=1,2,...N \tag{3.8}$$

A complex valued thermal resistance (impedance) can be defined with the use of Fourier's Law.

$$R \Rightarrow z = \frac{\hat{\mathrm{T}}}{\hat{q}} \tag{3.9}$$

The transformed heat flux can be also be defined by Fourier's Law and the solution in (3.10) can be substituted in to find an expression for the impedance for each layer in the system.

$$\hat{q} = -k_y \frac{\partial \hat{\mathrm{T}}}{\partial y} \tag{3.10}$$

$$\hat{z}_n = \frac{1}{k_{y_n}\Phi_n} \frac{k_{y_n}\Phi_n z_{n-1} - \tanh(\Phi_n t_n)}{1 - k_{y_n}\Phi_n z_{n-1}\tanh(\Phi_n t_n)} \qquad n = 1,2,...N \tag{3.11}$$

In the definition of the impedance from each layer $\hat{z}_o$ is the base layer impedance. Condition at the upper surface can be determined by applying the Fourier Transform to the heat flux from the heater and recognizing that as a result of symmetry the transform is an even function over the total width of the heater.

$$\hat{q}_N = \int_{-w}^{w} q_N \cos(\lambda x) dx \tag{3.12}$$

Upon substitution of $\hat{q}_N$ into equation (3.9) and recognizing the symmetry condition about $x = 0$ an expression for the surface temperature can be found.

$$\hat{\mathrm{T}}_N = 2q_N \frac{\sin(\lambda w)}{\lambda} z_N \tag{3.13}$$

Now that a transformed surface temperature has been found a reverse transform can be applied to find the true temperature at the surface. The expression below has also been averaged spatially over the width of the heater to accurately reflect the temperature that is sensed in experimentation.

$$\left\langle \mathrm{T}_N \right\rangle = \frac{1}{2w}\int_{-w}^{w}\left[\frac{1}{2\pi}\int_{-\infty}^{\infty}\hat{\mathrm{T}}_N \cos(\lambda x)d\lambda\right]dx = \frac{q_N}{\pi w}\int_{-\infty}^{\infty}\frac{\sin^2(\lambda w)}{\lambda^2}\hat{z}_N d\lambda \tag{3.14}$$

The impedance at the surface of the material system must be recursively solved for starting at the base of the sample ($y = 0$, Figure 29). Depending on the sample configuration in the experimental setup different boundary conditions might be more appropriate; equations (3.15) through (3.17) apply to the semi-infinite, fixed temperature, and adiabatic cases respectively at the base layer.

$$\hat{z}_o = \frac{-1}{k_{y_o}\Phi_o} \tag{3.15}$$

$$\hat{z}_o = \frac{-1}{k_{y_o}\Phi_o}\tanh(\Phi_o t_o) \tag{3.16}$$

$$\hat{z}_o = \frac{-1}{k_{y_o}\Phi_o}\frac{1}{\tanh(\Phi_o t_o)} \tag{3.17}$$

Now that the temperature fluctuations at the surface have been solved for a relationship between the temperature and the applied voltage signal is needed. Noting that the change in resistance of the heater can be expressed as equation (3.18).

$$\Delta R = \langle \Delta \mathrm{T} \rangle \frac{dR}{d\mathrm{T}} \tag{3.18}$$

The current is going to be exactly in phase with the driving voltage at frequency ω. The resistance will be changing at a frequency of 2ω due to the Joule heating but in phase with the temperature fluctuations.

$$I = I\cos(\omega t) = \frac{V}{R}\cos(wt) \tag{3.19}$$

$$\Delta R = \left|\langle \mathrm{T}_N \rangle\right| \frac{dR}{d\mathrm{T}} \cos(2\omega t + \phi) \tag{3.20}$$

Ohm's law can then describe the voltage fluctuations.

$$\begin{aligned} \Delta V &= \frac{V}{R}\cos(\omega t)\left|\langle \mathrm{T}_N \rangle\right| \frac{dR}{d\mathrm{T}} \cos(2\omega t + \phi) \\ &= \frac{V}{2R}\left|\langle \mathrm{T}_N \rangle\right| \frac{dR}{d\mathrm{T}} \left[\cos(3\omega t + \phi) + \cos(\omega t + \phi)\right] \end{aligned} \tag{3.21}$$

The 3ω portion of the applied voltage can now be identified as being proportional to the temperature fluctuations at the heater interface. The third harmonic voltage signal can be measured with a lock-in amplifier and then a data reduction scheme can be applied in order to solve for the material properties. More details about the experimental techniques will be discussed in §4.1. The following section describes the data reduction technique in more detail.

Figure 30. The 3w experimental setup. Stanford Research Systems SR-830 Lock In Amplifier along with Aglient multimeters and a Lakeshore temperature controller (left). The computer that controls the data collection and the cryostat and the cold finger (right).

3.2.1.2 Data Reduction in the 3ω Technique

Inverse problems like the 3ω method require an error minimization routine between the experimental data and the developed model. This is why an accurate representation of the experimental system must be represented in the analytical model, or else severe errors can result. There are many curve fitting routines available that fit a curve in the least squares sense. Olson outlines one method based on a the gradient method that has been developed for four degrees of freedom per material layer [72]. This method proved to be an efficient method for finding multiple material properties during a single experiment. However there are cases that suffer from numerical instabilities of the gradient based method and can therefore result in physically impossible solutions. When materials of similar thermal conductivity or very high thermal conductivity are present in the system problems with convergence can occur. As a result a more robust optimization algorithm was desired, even at the expense of computational time. A medium-scale optimization algorithm was used as a replacement for the gradient based method. A

method referred to as sequential quadratic programming (SQP) was implemented with the MATLAB function fmincon. This solves the problem outlined in equation (3.22).

$$\min_x f(x) \text{ subject to} \tag{3.22}$$

$$\begin{aligned} c(x) &\le 0 \\ c_{eq}(x) &= 0 \\ A \cdot x &\le b \\ A_{eq} \cdot x &= b_{eq} \\ lb &\le x \le ub \end{aligned}$$

Where x, b, b_{eq}, lb, and ub are vectors, A and A_{eq} are matrices, $c(x)$ and $c_{eq}(x)$ are functions that output vectors, and $f(x)$ is a function that returns a scalar and is a measure of the error in the experiment. In this case it was taken that $A_{eq} = 0$, $b_{eq} = 0$, $A = 0$, and $b = 0$ leaving only vectors lb and ub to be defined as the upper bound (ub) and lower bound (lb) to the material properties. In this case the vector x serves the purpose of a generalized vector of properties that can be searched for. Equation (3.23) shows the general case for a vector construction.

$$x = \begin{bmatrix} k^T \\ \rho c_p{}^T \\ \psi^T \\ R_c{}^T \end{bmatrix} \tag{3.23}$$

Here k is the thermal conductivity, ρc_p is the thermal capacity, ψ is the thermal conductivity ratio k_x/k_y, and R_c is the interface contact resistance. Each one of these properties is a vector that is $1xN$ so that x is a column vector. The minimization function $f(x)$ is the same as outlined in [72]. The main advantage over the gradient method is the

ability to set bounds to the solutions for each one of the material properties that is being searched for. This allows for physically impossible solutions to be rejected prior to computation.

3.2.1.3 Systematic Error Analysis

Error in the thermal conductivity measurement arises from the uncertainties in the microheater dimensions, film thicknesses, film thermal capacity, voltage sensing capabilities, variations in the applied voltage signal, thermal coefficient of resistance calibration, resistance measurements, and the fitting error in the extraction routine.

The microheater was defined using a microlithography process that has a resolution of <1μm. The oxide layer was grown using a PECVD method with a growth rate of 60Å/min. Due to the complicated layer structure the deposition rate was calibrated on a reference Si sample and the thickness was determined with a profilometer; the growth rate was assumed to be the same on the GaN structure. This growth rate allowed the layers to be controlled to 0.1nm/s, which results in an uncertainty of 0.1nm in the total layer thickness. The GaN growth was performed in a MOCVD reactor as the thickness in the error was assumed to be similar to that of the PECVD method (0.1nm). Using an Agilent 34401A multimeter the resistance of the potentiometer can be resolved to within 0.003%. The Stanford Research System's SR830 Lock-In Amplifier is accurate to within 1% of the stated applied voltage. Due to the additional annealing step before 3ω testing the thermal coefficient of resistance was found to be linear with a R^2 of 1 and therefore it does not contribute to the uncertainty in the thermal conductivity. The fitting error was performed assuming a *t*-distribution due to the small number of frequency

points taken; this accounts for the random error in the experiment and was simply added to the systematic error found from a sensitivity analysis. Table 6 summarizes the uncertainty values for each parameter that was varied in the analysis.

Table 6. Summary of typical uncertainty values for various system parameters.

Error Source	Typical Uncertainty
Width of Heater	1mm
Length of Heater	1mm
Oxide Thickness	3nm
GaN Thickness	0.1nm
TCR	0 Ω/K
Test Voltage Measurement	0.05V
Resistance Measurement	0.00048Ω
Thermal Capacity of Oxide	5%
Thermal Capacity of GaN	5%
Thermal Capacity of Sapphire	5%

Using the formulation in equation (3.24) the uncertainty in the thermal conductivity can be determined based on all system parameters outline in Table 6, P_n. To obtain the derivative terms the parameters were systematically perturbed and a numerical approximation was made; all perturbations were linear in nature and therefore the derivatives are assumed constant.

$$\delta k_{total} = \left[\sqrt{\left(\frac{\partial k}{\partial P_1} \delta P_1 \right)^2 + \left(\frac{\partial k}{\partial P_2} \delta P_2 \right)^2 + \left(\frac{\partial k}{\partial P_3} \delta P_3 \right)^2 + \left(\frac{\partial k}{\partial P_4} \delta P_4 \right)^2 + \ldots} \right] + \delta k_{fit} \qquad (3.24)$$

The uncertainty was found to be 17.21%, 8.40%, and 7.21% for the GaN, SiO_2, and sapphire layers respectively. The majority of the error is from the curve fitting routine, but other significant portions of the error were found in the ability to sense the correct

voltage drop across the test element and in the thermal capacity of the thin films. This highlights the importance of knowing material properties accurately as well as having capable equipment.

3.3 Temperature

The operational temperature of a device is a direct consequence of the ability to dissipate heat in the material system. When the dominant mode of heat removal is by conduction the operational temperature is related directly to the thermal conductivity. However thermal conductivity itself does not cause failure, ultimately it is the excessive temperatures that will cause a device to degrade in performance then fail [26]. It is therefore critical to study both the thermal conductivity and the temperature distributions within operating devices in order to design better construction techniques to improve performance. In this work two techniques were utilized in order to measure the local temperature on operating devices, micro infrared imaging and micro Raman Spectroscopy. Both of these techniques will be outlined in the following sections in order to provide the reader with some knowledge of the abilities of these methods as well as some of the operational theory.

3.3.1 Micro Infrared Imaging

Infrared (IR) imaging makes use of the fact that energy in the form of infrared radiation is emitted from a surface; this energy is proportional to T^4. The reason that radiation is emitted in within the infrared region can be explained by Planck's law of black body radiation (equation (3.25)).

$$I(\omega,T) = \frac{2h\omega^3}{c^2}\frac{1}{e^{h\omega/k_BT}-1} \tag{3.25}$$

Here I is the spectral radiance, T is the temperature of the emitter, h is Planck's constant, c is the speed of light, k_B is Boltzmann's constant, and ω is the frequency of the emitted radiation. As the emitting body gets cooler the peak emission shifts to longer wavelengths; for most objects between 300-500K, 95% of the energy is emitted between 3.5-58μm. In Figure 31 a picture of the Quantum Focus Infrascope II infrared microscope (QFI) is shown. This microscope has temperature mapping abilities down to 0.1°C and spatial resolution of ~2.8μm which is operating in a diffraction limited mode. The QFI has an indium antimonide (InSb) p-n junction based detector, which has a bandgap of 0.17eV. This bandgap corresponds to a photon wavelength of 7.29μm, well into the IR region of the spectrum. Electrons in the valence band can be thermally excited across this narrow bandgap resulting in a large source of noise in the p-n junctions. In order to decrease the effect of this thermal noise the detector is held at liquid nitrogen (77K) temperatures.

It is critical when performing IR based experiments that the surface emissivity of the sample be calibrated. In order to perform this calibration the QFI is outfitted with a thermoelectric stage that allows for emissivity maps to be made at various known temperatures. This observed emissivity map is assumed to be constant between temperature intervals, which allows for a corrected temperature map to be made based on the material properties.

Figure 31. Quantum Focus Instruments' Infrascope II infrared microscope used in temperature mapping of a multi quantum well (MQW) based LED and an AlGaN/GaN based power HFET device.

The results of the experiments that were performed were later used as inputs to finite element models that allowed for a full mapping of the temperature within the device structure. Details on the results of the numerical models and the correlation between the IR experiments will be discussed in Chapter 5.

3.3.2 Micro Raman Spectroscopy

Raman Spectroscopy relies on the ability to analyze a broad spectrum of light that has been inelastically scattered (Raman scattering) from a sample due to the incident photons interacting with phonons present in the sample. Typically the quantum yield of the Raman scattered light is on the order of 1 in 10^6 photons smaller than elastically, and therefore a notch filter is needed in order to remove the Rayleigh scattered light

(elastically scattered). The spectrometer used in this work was a Renishaw inVia Raman Microscope (Figure 32).

Figure 32. A Renishaw Raman spectrometer coupled with a Leica microscope. The microscope allows a laser spot size to be focused to <1μm, providing high spatial resolution capabilities.

The incoming radiation in the form of photons interacts with the electron cloud of the atoms. The amount of induced deformation in the electron cloud is called the polarizability of the material. This polariziablity leads to shift in the dipole moment of the atom that then causes a shift in the phonon frequency. Since the frequency shift centers on that of the incident photon, only low frequency optical phonons near the dispersion zone center take part in the Raman scattering. Thus, any effect that alters the lattice spacing (e.g., expansion or contraction due to stress and/or temperature changes) will result in changes of the frequency where the first Raman phonon mode occurs. A Raman active material is one in which dipole moments can be induced, thus Raman scattering has been used in the diagnostics of solids, liquids and gases. Metals are not measurable using Raman spectroscopy due to their free electrons which prevent induced dipole moments [49].

The coefficient of Raman shift with stress is approximately an order of magnitude lower than the Raman shift with temperature; therefore stress changes in the film due to temperature changes can be neglected [49]. In GaN one of the dominant resonant modes is located at 568cm^{-1}, it was this peak that was tracked for the temperature calibration and temperature mapping experiments [25, 73, 74]; a sample scan is shown in Figure 33. Studies have been performed on epitaxial grown layers of α-GaN and the E_2 Raman peak shift with stress was found to be 0.00417cm^{-1}/MPa [75]. In contrast the E_2 Raman peak shift with temperature was found to be 0.017188cm^{-1}/K. While there is a coupled thermomechanical response, the dominant cause of peak shifting is generally due to temperature and stress effects can be ignored, to first order. In order to calibrate the material as a function of temperature a Linkam TS1500 temperature stage was mounted under the microscope (Figure 34) and displacements of the 568 cm^{-1} peak were recorded. A sample calibration curve is show in Figure 35.

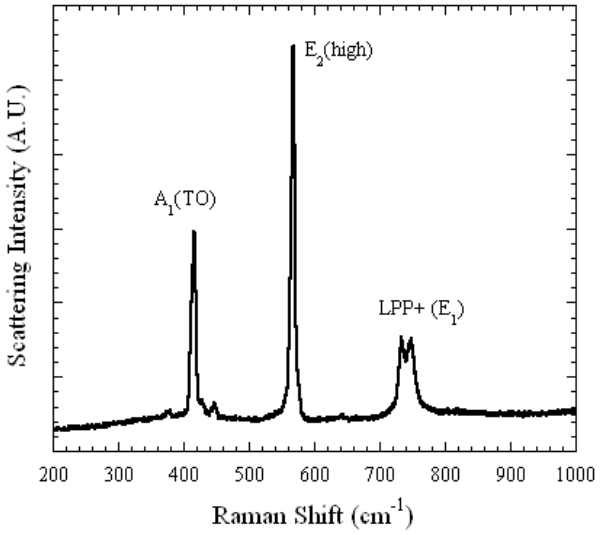


Figure 33. A broad band scan of the Raman signature of a single crystal GaN sample showing the A_1, E_2 and E_1 peaks. The intensity of scattering events is much higher at the E_2 peak (568 cm^{-1}) and therefore this peak was tracked during all experiments.

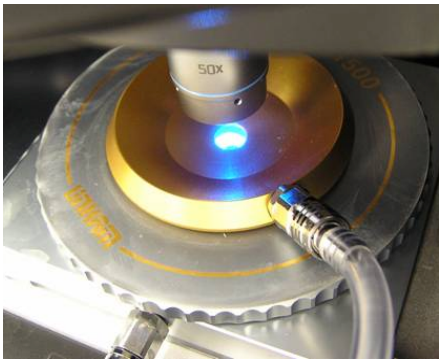


Figure 34. The Linkam TS1500 mounted under the Renishaw inVia Raman microscope.

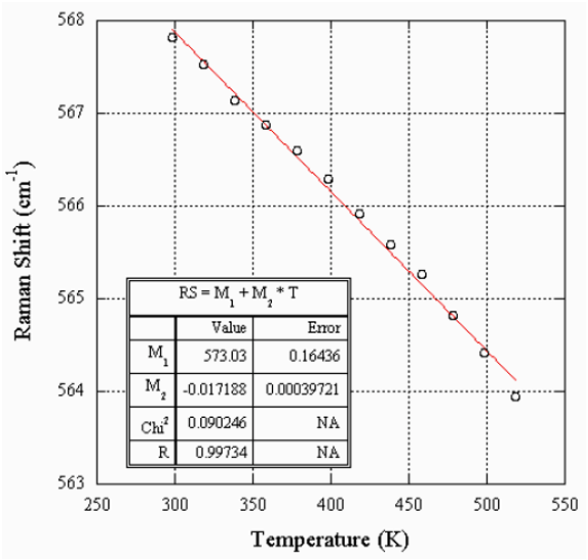


Figure 35. A graph showing the E_2 peak position in GaN as a function of temperature. The linearity of the the position (R^2=0.997) shows that stresses the film does not effect the temperature calibration.

It is important to note that the incident laser power could result in additional sample heating. Therefore it is critical to investigate this possibility in order to eliminate any effects that laser heating could cause on the temperature calibration. Classes of semiconductors known as direct bandgap semiconductors are less prone to laser heating due to their electron band structure. In this case the conduction band minimum and the valence band maximum lie at the Brillouin zone center. This allows low momentum photons to be the primary means of valence band electron excitation. Gallium nitride as well as the other materials tested in this work fall under this classification. Silicon, a very common material for MEMS and other electronics, is an indirect bandgap material; the conduction band minimum and valence band maximum lie at different wavevectors. Therefore a high momentum phonon is needed to assist the photon in electron excitation and relaxation. As a result silicon suffers from laser heating problems during

experimentation. It should also be noted that the energy of the incident photons is well below the bandgap of GaN (~3.5eV correlates to a laser wavelength of 354nm); thus they will not excite any electrons into the conduction band, which can lead to phonon release due to electron relaxation. The Renishaw system that was used operated at a laser wavelength of 488nm. The coefficients that are obtained from the temperature calibration are not widely published. However groups have used this calibration technique in order to analyze AlGaN/GaN HFETs with an accuracy of ±10°C [73, 74]. This level of accuracy enables Raman spectroscopy to be a valuable tool in order to study the temperature distribution of operational devices.

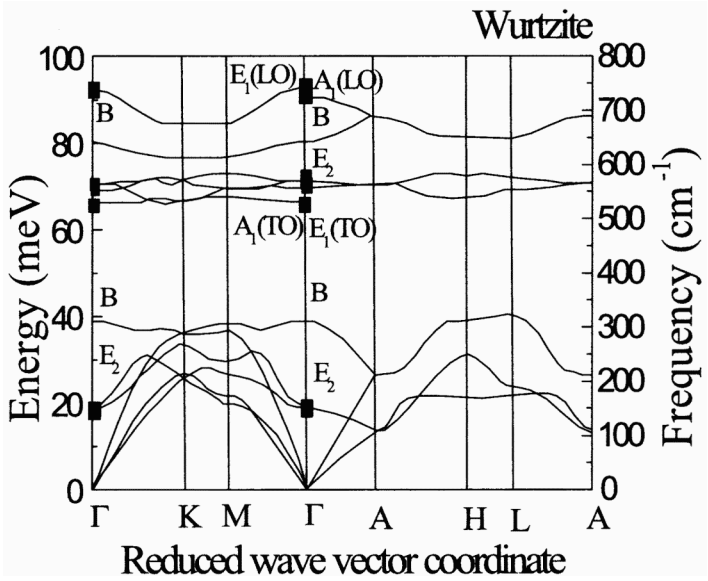


Figure 36. Phonon dispersion curve in wurtzite GaN. Optical phonon modes that are Raman active are labeled. From [76].

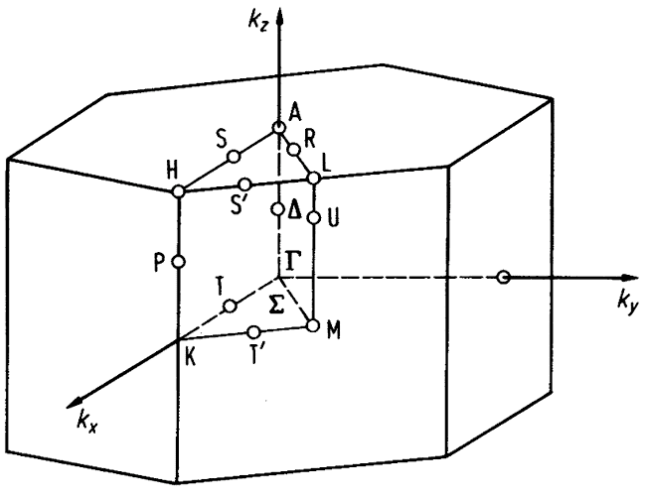


Figure 37. The first Brillouin zone in the hexagonal crystal structure. Major symmetry points have been labeled that correspond to the reduced wavevector coordinates shown in Figure 36. From [77].

CHAPTER IV

EXPERIMENTAL METHODS

Experimental methods and results are discussed in this chapter. The chapter begins with a discussion of the lithographic process in order to fabricate the microheaters discussed in §3.2.1. Results of the 3ω method are then presented for each of the materials tested and comparisons between fitting routines are made. Thermal conductivity is then compared to previous characterization methods to observe the effect that microstructre has. The chapter progresses with the details of the experiemental methods used in order calculate the temperature of operating devices. Material properties from this chapter as well as temperature distributions are used in order to model devices. The methods of device modeling are located in chapter 5.

4.1 Thermal Conductivity

4.1.1 Microheater Fabrication

The microheater that was used in the 3ω measurements was fabricated with a standard lithography process in the Microelectronics Research Center's cleanroom. Before starting the lithography process there was some sample preparation that was needed. The materials under investigation were semiconductors and therefore electrically conductive. A dielectric layer had to be deposited over the material in order to prevent current leakage from the microheater during operation. A layer of silicon oxide (SiO_2)

was deposited using a plasma enhanced chemical vapor deposition (PECVD) system by flowing 400 sccm of SiH_4 and 900 sccm of N_2O at 900 mTorr and 250^oC and a RF power of 30W into the reacting chamber. This recipe allowed for a deposition rate of 600 Å/min (Figure 38 step (B)). Due to the amorphous nature of the deposited material a layer that was 500 nm was needed in order to provide total insulation, otherwise defects formed that allow current to leak into the GaN layer. After deposition of the dielectric the lithography process was performed. Hexamethyldisilazane (HMDS), an adhesion promoter, was spun onto the sample first followed by a layer of Shipley 1813 positive photoresist. Each of these chemicals were spun onto the small samples at 3000 rpm for 30 s and an acceleration of 1500 rpm/s. This spinning recipe resulted in a photoresist layer that was ~1-2 μm thick (Figure 38 step (C)). The samples were then softbaked at 90^oC for 5 min in order to set the photoresist. After cooling the samples they were aligned in a Karl Suss MA6 mask aligner and exposed under a 405 nm UV light source with an intensity of 6 mW/cm^2 for 30 s. This provided a dosage of .18 Joules to the photoresist, which was sufficient to define features down to 3 μm. The exposed sample was then developed in Microposit 319 developer for ~30 sec or until the features were observable (Figure 38 step (D)). A 20 nm thick layer of titanium was used as a metal adhesion layer for 50 nm thick layer of gold that defined the microheater. The metal was deposited using a metal evaporator, which results in high quality heaters (Figure 38 step (E)). It should be noted that a sputtering technique was originally used but inconsistencies in the device resistance were observed; evaporation provided much more predictable results and was used exclusively afterwards. Extra photoresist was removed

by placing the sample into an acetone bath to define the final structure (Figure 38 step (F)).

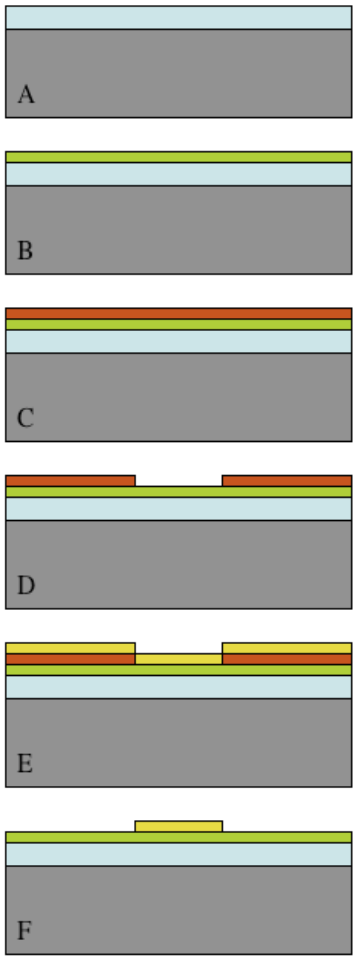


Figure 38. (A) Substrate with GaN layer. (B) GaN after SiO_2 dielectric layer deposition. (C) Photoresist layer spun onto surface. (D) Developed photoresist layer after UV exposure. (E) Evaporative Ti/Au deposition. (F) Lift-off of photoresist and extra metal.

Once the microheater fabrication was complete the process of mounting the sample into the cryostat could begin. In order to make electrical connections to the device a probe card that was compatible to 300^{o}C was manufactured by Alpha Probes, Inc. was used. The probes on the ceramic mounting plate are made of a BeCu alloy to

provide the lowest contact resistance possible. The probe card is mounted on to the copper sample holder as shown in Figure 39. Additionally the sample was mounted to the copper cold finger with high temperature heat sink grease manufactured by AOS Thermal Compounds. Once the electrical connections had been made and verified the testing process can begin following the testing flow chart shown in Figure 40. The data reduction process outlined is then implemented in order to extract the thermal conductivity.

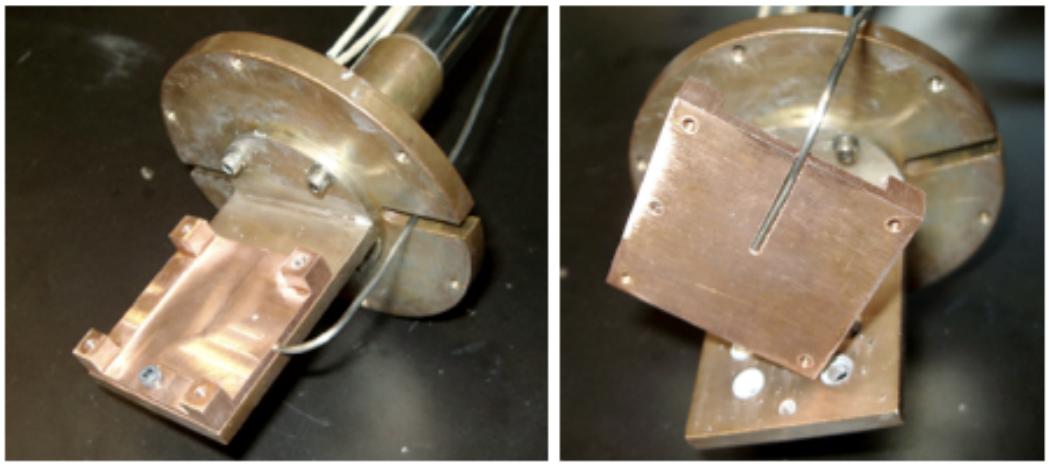


Figure 39. A picture of the cold finger of the cryostat and the thermocouple placement. The sample is mounted to the center of the copper block with the four posts. The probe card is then bolted on top of the sample to make the electrical connections and provide additional mechanical connection to the cold finger.

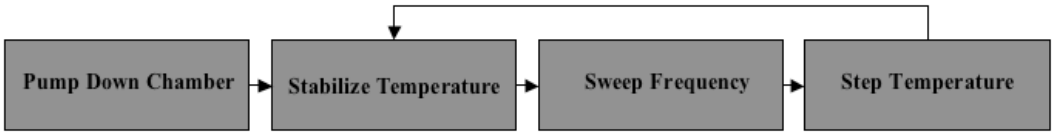


Figure 40. 3ω process flow chart to test a material thermal conductivity as a function of temperature.

Results from the data analysis are now presented for sapphire, $LiGaO_2$, ZnO, GaN, P-Type GaN, SiN, SiO_2, Si doped/Undoped GaN, and an InGaN MQW LED structure. The 3ω method has the capability of characterizing several layers at once; this was explored in this work by comparing a layered structure to a control sample. A bare sapphire wafer, being the most popular substrate choice for GaN growth, was used as the control sample. Other samples are outlined in Table 7.

Table 7. Samples that were tested with the 3ω method. Samples with more than one material present were characterized simultaneously and then compared to the control sample (Sample 1)

Sample Number	Materials Present
1	Sapphire
2	ZnO
3	$LiGaO_2$
4	Sapphire/Undoped GaN/SiN
5	Sapphire/Undoped GaN/SiO_2
6	Sapphire/Si doped Gan/Undoped GaN/SiO_2
7	Sapphire/P-Type GaN/SiO_2
8	Sapphire/InGaN MQW/SiO_2

4.1.2 Sample 1 Results

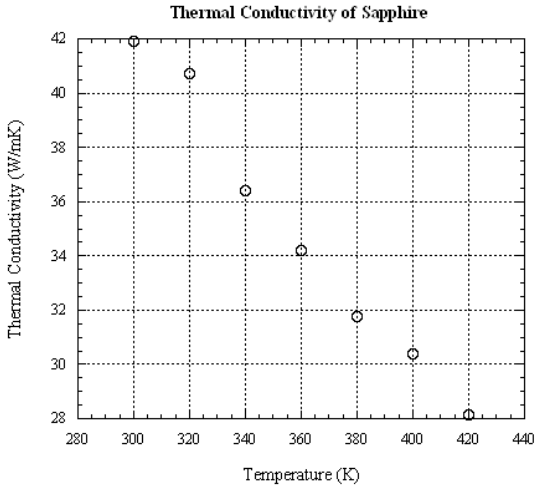


Figure 41. Results from the 3ω method of a bare sapphire wafer as a function of temperature. The results show that sapphire has only a moderate thermal conductivity.

4.1.3 Sample 2 Results

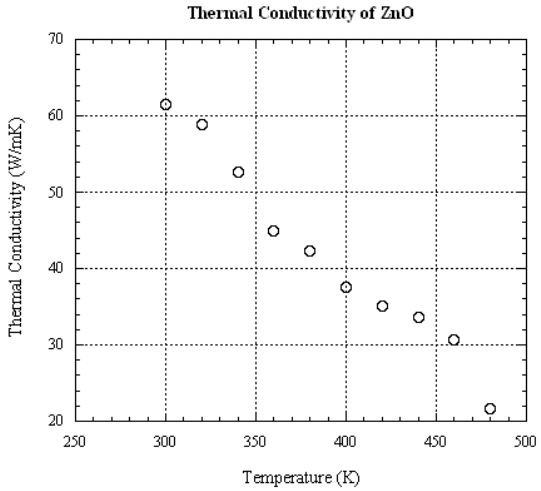


Figure 42. Results from the 3ω method of ZnO shows a factor of 1.5x higher thermal conductivity than sapphire.

4.1.4 Sample 3 Results

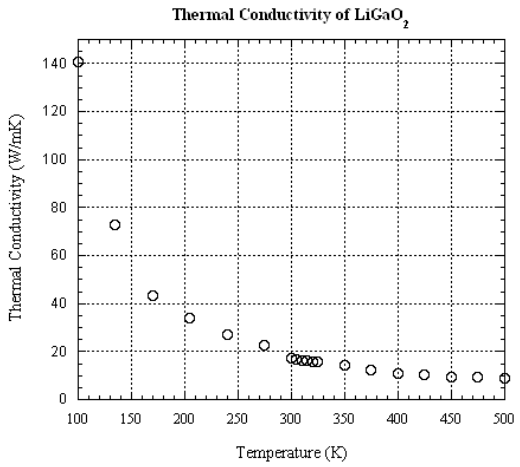


Figure 43. Results from the 3ω method of $LiGaO_2$ as a function of temperature. The tests show that $LiGaO_2$ is a low conductivity material.

4.1.5 Sample 4 Results

The following material system was multilayered and contained sapphire, undoped GaN, and SiN as the dielectric layer. All of these layers were characterized simultaneously.

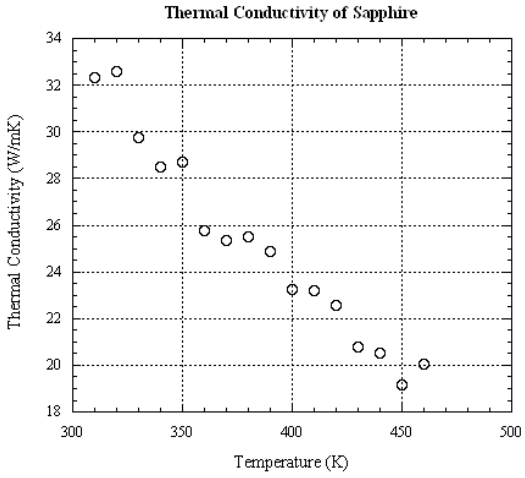


Figure 44. Thermal conductivity of sapphire from a multilayer structure. Results show good agreement when compared to the control sample.

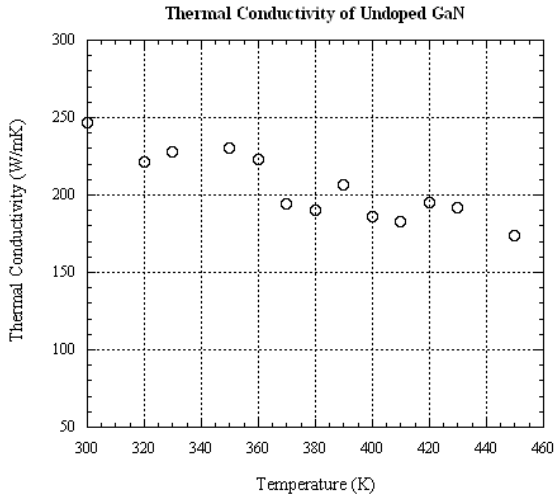


Figure 45. Thermal conductivity of an undoped GaN layer 2μm thick grown on sapphire by MOCVD. The results show that GaN is a high thermal conductivity material.

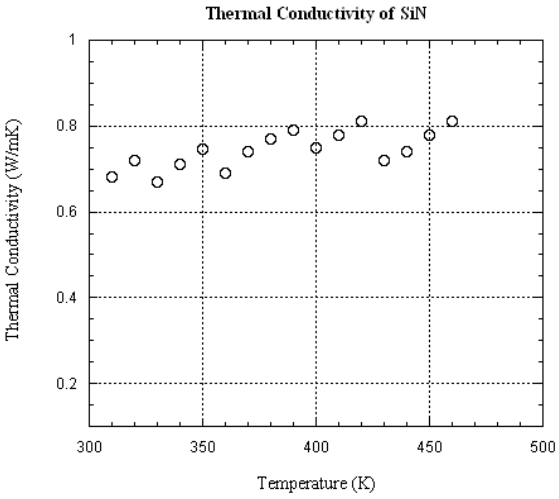


Figure 46. Thermal conductivity of the 500nm thick SiN dielectric layer deposited by PECVD. The results show reasonable values for an amorphous material.

4.1.6 Sample 5 Results

The following material system was also multilayered and contained sapphire, undoped GaN, and SiO_2 as the dielectric layer. In this sample only the GaN layer was

characterized. The SiO_2 and sapphire thermal conductivities were used from previous tests. Sample 5 was used as a test in order to examine the repeatability of the 3ω method when a multi layer system is being tested. The GaN layer in Sample 5 was also grown by MOCVD however in a different reactor than Sample 4. As expected the thermal conductivity of GaN was almost 1.5x higher than silicon as also reported in [17, 78-83].

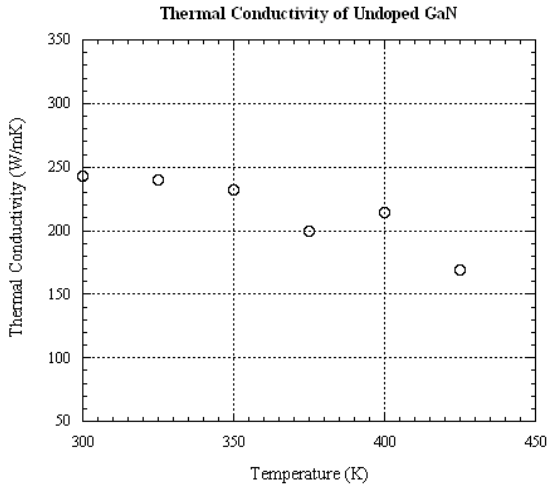


Figure 47. Thermal conductivity of an undoped Gan sample 2μm thick grown by MOCVD on sapphire. The results show good agreement between this result and the previous test with Sample 4.

4.1.7 Sample 6 Results

As with previous samples, Sample 6 is also multilayered. The structure of Sample 6 is sapphire/Undoped Gan/Si doped GaN/SiO_2. Due to noise in the system it was not possible to extract all four layers simultaneously. Instead an averaged thermal conductivity of the two GaN layers was found as a function of temperature; it was still possible to search for the SiO_2 and sapphire layers along with this averaged thermal conductivity. The searching algorithm used on this sample was the medium-scale

optimization routine outlined in §3.2.1.2. This method had to be used since the gradient based method tended to diverge or converge to physically impossible solutions. The optimization based method allowed the solution to be constrained to physically possible regions, this aided in proper convergence.

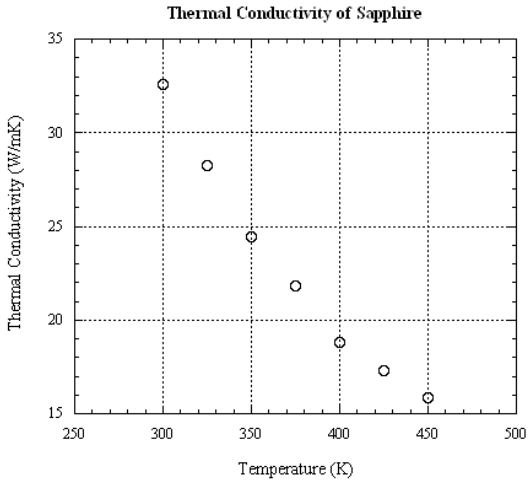


Figure 48. Thermal conductivity of sapphire in Sample 6. The results show reasonable agreement when compared to the control sample.

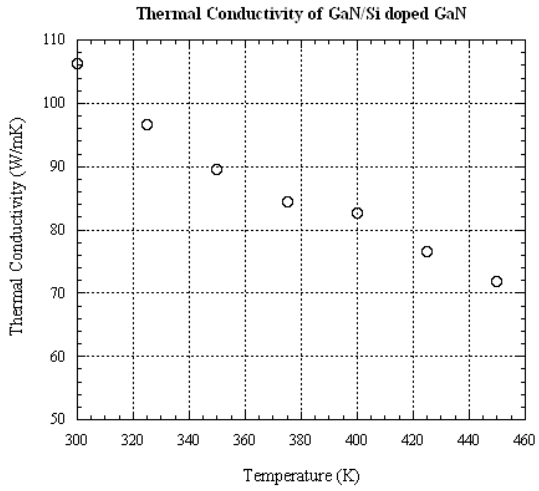


Figure 49. Effective thermal conductivity of the undoped GaN/Si -doped GaN bi-layers. As expected, Sample 6 has a lower thermal conductivity than the undoped GaN in Sample 4.

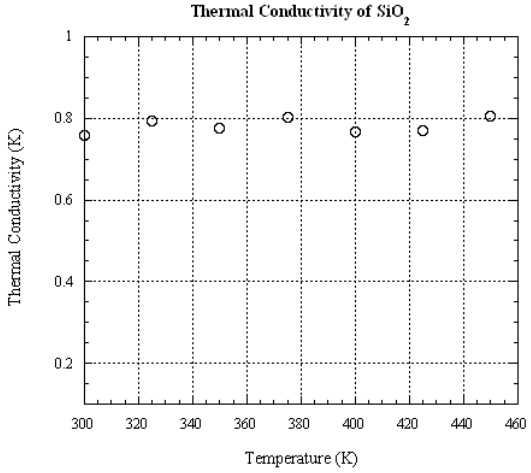


Figure 50. Thermal conductivity of the PECVD SiO_2 dielectric layer. Data agrees well with other amorphous materials discussed in [84].

4.1.8 Sample 7 Results

The following material system was multilayered and contained sapphire, P-Type GaN, and SiO_2 as the dielectric layer. All of these layers were characterized simultaneously using the gradient-based method [72].

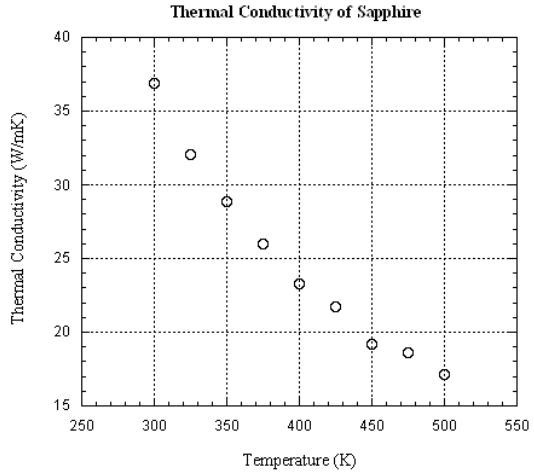


Figure 51. Thermal conductivity of sapphire as a function of temperature. The data shows good agreement between the multilayer structure and the control structure.

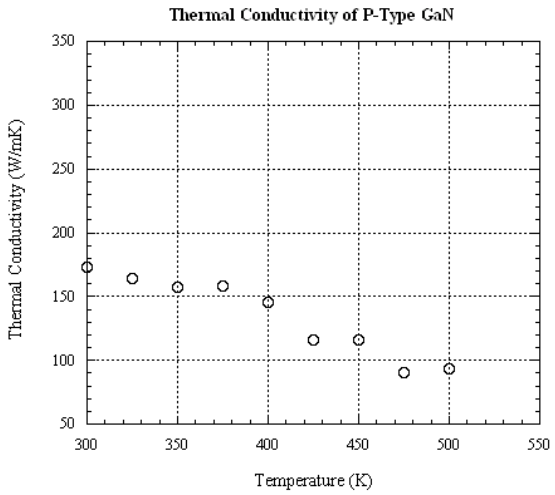


Figure 52. Thermal conductivity of P-Type GaN as a function of temperature. The data shows that, due to the Mg doping, the thermal conductivity decreases because of increased phonon scattering sites.

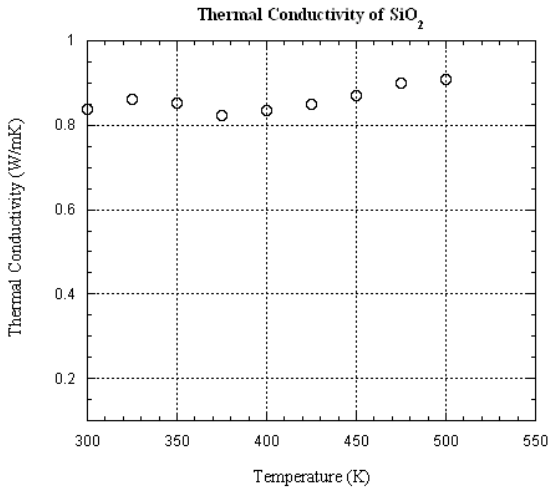


Figure 53. Thermal conductivity of the 500nm thick SiO_2 dielectric layer. The data agrees well with previous experiments as well as literature [84].

4.1.9 Sample 8 Results

The following material system was multilayered as it consisted of two decoupled MQWs as well as GaN electrical contact layers. The layered structure is shown in Figure 54. In addition to the LED structure a 500nm thick dielectric layer of SiO_2 was deposited on the wafer. The sapphire and the SiO_2 material properties were used from previous tests in order to aid in proper convergence.

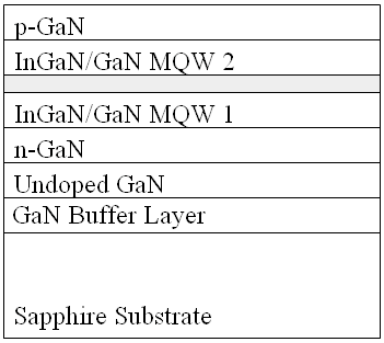


Figure 54. InGaN/GaN LED structure tested for an average thermal conductivity of all the layers.

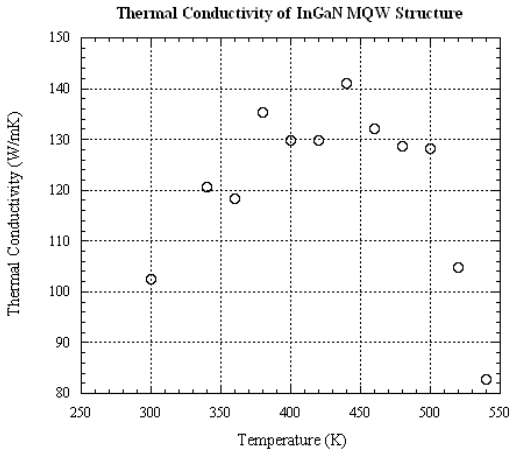


Figure 55. Effective thermal conductivity of the LED structure. Notice that the peak conductivity is above room temperature.

In Figure 55 the effective thermal conductivity of the material peaks well above room temperature, which is not a common behavior. This behavior can be explained by the increased boundary scattering in the MQW layers, which are on the order of 2 nm thick. Attempts to capture this behavior using the relaxation time approximation have been made however this modeling technique is not without its deficiencies and as a result will be left for future work.

4.2 Temperature

4.2.1 InGaN/GaN LED Results

The device under study is a dual emitting MQW light emitting diode that has been optimized for peak emission wavelengths at 460nm and 400-420nm. The LEDs were grown using a Veeco Discovery series D-125 GaN MOCVD tool with a vertical injection, confined inlet design. Trimethyl-gallium, triethyl-gallium, thrimethyl-indium, and thrimethyl-aluminum were used for group III metals and ammonia for group V. P-type doping was achieved with magnesium incorporation from biscyclopentyldienyl magnesium (Cp_2Mg), and n-type doping with silicon incorporation from silane (SiH_4). The advantage that a dual emitting MQW structure has over a single wavelength emitter is that greater efficiency and a broader spectrum can be obtained when using a phosphor converter to more accurately render white light.

In all tests the LED was pumped using a DC current and a turn-on voltage of 4.2V was observed from the I-V curve shown in Figure 56. The temperature of the operating device was first characterized with the Quantum Focus Microscope shown in Figure 31. It was important to first obtain an emissivity map in order to account for the small variations material composition that could distort the temperature measurements. The device was held at a known temperature and the emissivity map was obtained. From the calibration an average emissivity of ~0.8 resulted, meaning that a black body approximation would have resulted in a significant under prediction of the temperature.

An example of the device dissipating 0.5W is shown in Figure 57. It can be seen from this image that large temperatures within the active area of the device are possible.

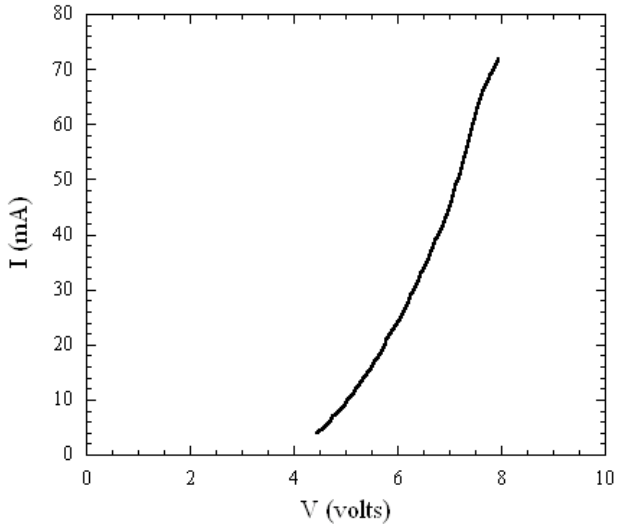


Figure 56. I-V curve for the InGaN/GaN MQW LED structure.

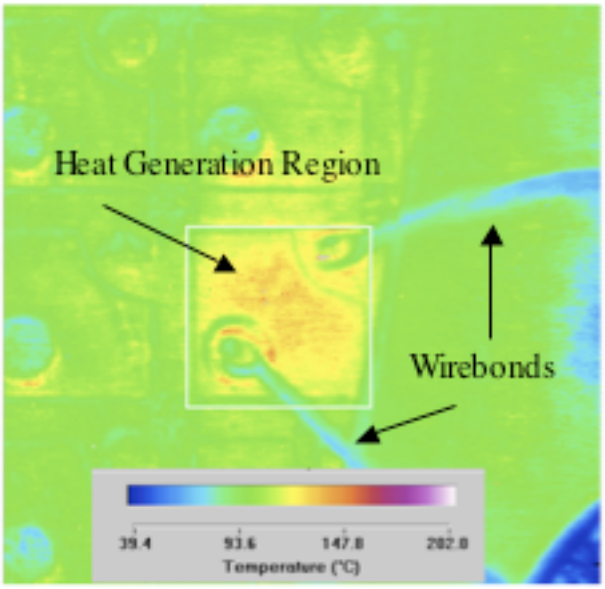


Figure 57. An infrared image of the MQW under investigation. The power dissipated in this test was 0.5W and resulted in a mean temperature of 115°C within the box. A maximum temperature of 149°C was also observed.

In addition to the temperature mapping of the LED with IR, average device temperatures were calculated with micro-Raman spectroscopy. When observing the Raman signal of the active LED the excitation laser had to be exchanged for a wavelength that would not interfere with the LED emission; instead of the 488nm laser an excitation laser that operated at 765nm was used. When observing the Raman spectrum of MQW structures using a 765nm source laser there were issues with material fluorescence that resulted in a high level of background counts on the CCD. In order to increase the signal-to-noise ratio more Raman active modes needed to be excited; this was accomplished by switching from a point focused laser mode to a line-focused mode. This effectively increased the sample area to a 1μm x 35μm size and therefore the number of Raman scattered events increased.

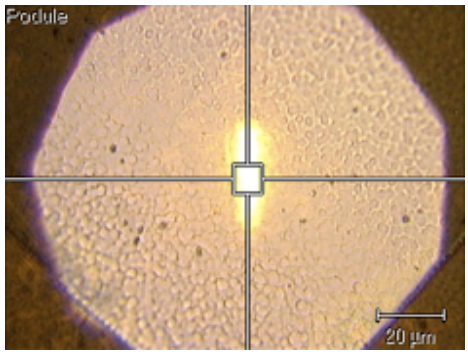


Figure 58. Line-focused mode on the MQW structure. In this particular picture the LED is not operating in order to show the details of the laser spot size.

A material calibration was performed as outlined in §3.3.2 and the average device temperature has been plotted along with data from the IR experiments, shown in Figure 59. The FEMLAB results that are also plotted will be discussed more in §5.2.1. While there is some deviation from the modeled trend all results fall within the error limits of

the experiments. All Raman peak locations were taken ten times per power setting and the standard deviation, σ, was calculated; uncertainty in the measurements are presented within a 2σ window of the mean.

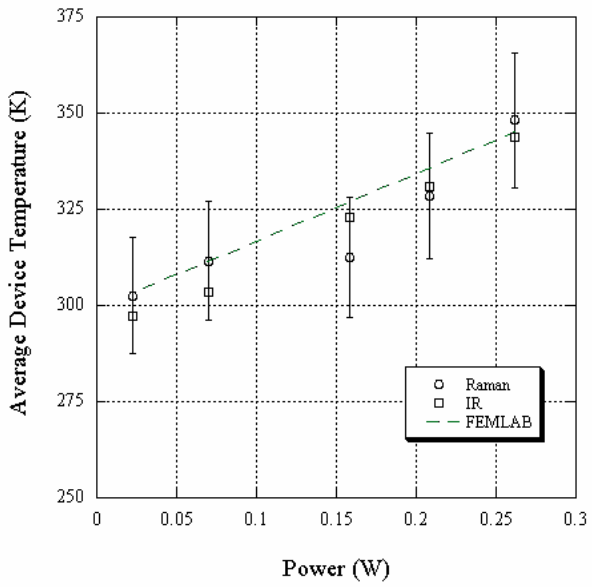


Figure 59. A comparison graph between Raman Spectroscopy, infrared imaging, and FEMLAB results. A trend with input power is observed, however large error bars show the negative effects of a line focused excitation laser as well as material fluorescence.

4.2.2 HFET Results

An $Al_{0.3}Ga_{0.7}N/GaN$ HFET was also examined with the IR microscope. This HFET is a symmetric dual gate device, and as a result of the symmetry only half of the device was operated at a time. A cross-section of the different layers of the device is shown in Figure 60. The heterostructure interface ($Al_{0.3}Ga_{0.7}N/GaN$) in this device allows for electrons to be confined in a shallow region within the undoped GaN layer due to the difference in the conduction band levels. Electrons in this region have very high

mobilities since impurity/doping concentrations are very low; this makes the devices very fast even with wide gates (9μm in this device).

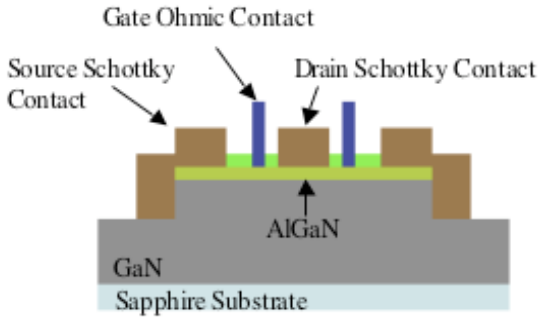


Figure 60. Symmetric dual gate AlGaN/GaN HFET. The ohmic contacts are Ti/Al/Ti/Au; the Schottky contacts are Ni/Au. Flanking the gate is a layer of SiN that behaves as an isolation layer.

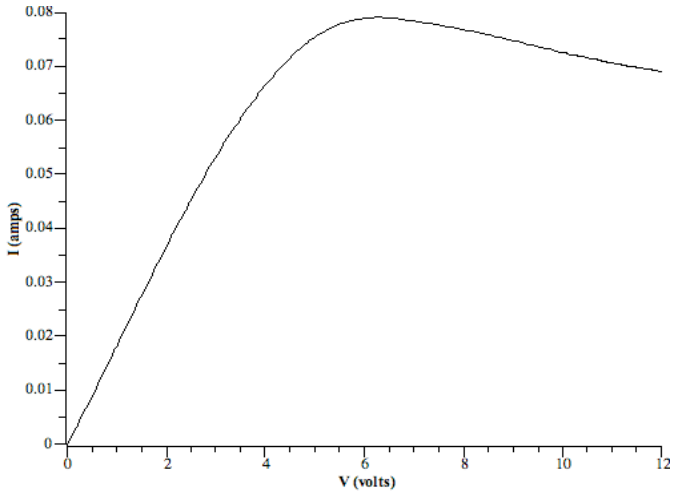


Figure 61. I-V curve of the AlGaN/GaN HFET at zero gate bias voltage. The graph shows that the saturation current is 80mA. The graph also shows the effect of high temperatures on performance as the saturation current begins to decrease with increasing voltage.

After obtaining the I-V characteristics of the zero-bias voltage case several power levels were chosen to investigate the temperatures that the device reaches (Figure 62).

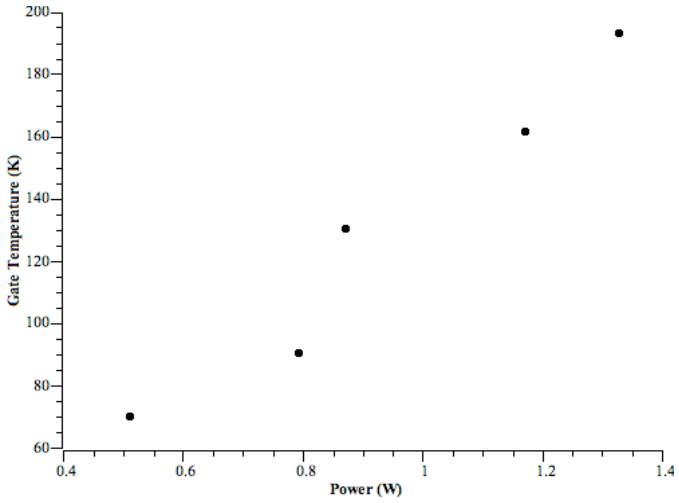


Figure 62. The temperature response of the HFET under investigation. The gate of the device was followed because the largest temperature rise was observed there. The nearly linear nature of the data points suggests that Joule heating generates the majority of the heat.

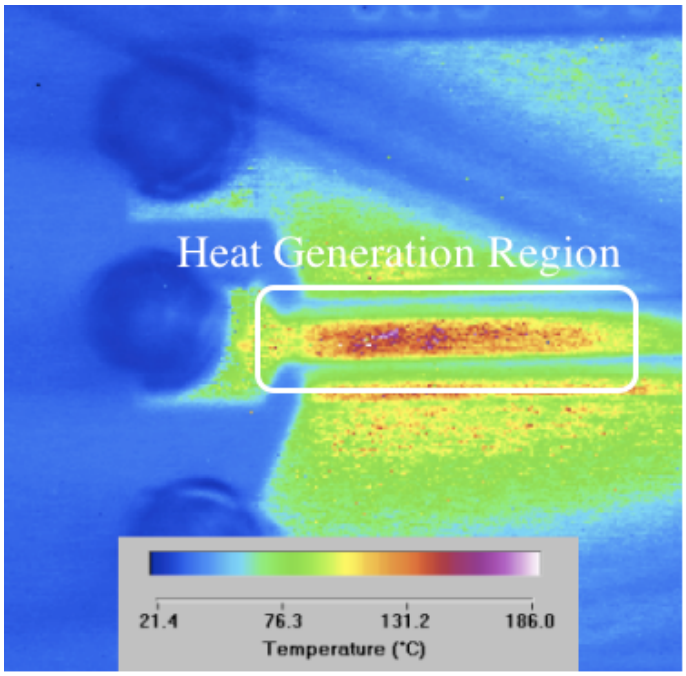


Figure 63. IR image of an AlGaN/GaN HFET. A power of 0.87W was applied to this device. The high temperatures can be clearly seen in the region of the gate connection.

With information about the temperature response it is possible to develop numerical models in order to conduct further analyses on the packaging of such devices. Further discussion will be made in Chapter 5.

CHAPTER V

MODELING

This chapter is a discussion of the phonon transport modeling techniques that are used in order to predict material behavior, specifically the thermal conductivity. It begins with a high level overview of phonons in materials and some of the foundations needed in order to continue with phonon analysis. Included will also be a discussion of the commonly used relaxation time approximation. Further refinements to the thermal conductivity solution have been made by Callaway, which will also be discussed. Results from all calculations are shown in comparison to experimental data presented in Chapter 4.

In addition to the phonon modeling techniques an investigation of the materials used in electronics packaging was conducted. Finite element models were built in FEMLAB to simulate an operating HFET and LED. To validate the models the results were compared to IR and Raman temperature distributions for several power levels. As well as solving for the temperature distribution within the packages a system level parametric study was performed to provide some insight into key design parameters. The focus in the parametric study was on heat sink materials, thermal interface materials, modes of convection, and LED slug materials.

This chapter combines many ideas and aims to give the reader a sense for what parameters are important in design of high power electronics packaging.

5.1 Phonon Modeling

5.1.1 Phonon Transport Theory

Phonons have been described as energy packets that travel through a material by lattice vibrations. The amplitude, velocity, frequency and time between scattering events all contribute to the amount of energy that is transported and therefore the final value of the thermal conductivity. In considering a crystal lattice it is possible to develop theoretical models for phonon transport that can provide insight into the physical phenomena that are occurring when heat travels.

In envisioning a crystal structure the energy of all phonons at a specific temperature can be written as equation (5.1).

$$U = \sum_{k} \sum_{p} \left\langle n_{k,p} \right\rangle \hbar \omega_{k,p} \tag{5.1}$$

Here k is the wavevector and p is the polarization index; there are two possible transverse modes as well as one longitudinal mode. Phonons have zero spin and therefore the average number of phonons in an energy state is given by the Planck distribution, $\left\langle n_{k,p} \right\rangle$.

$$\left\langle n_{k,p} \right\rangle = \frac{1}{e^{\hbar\omega/k_B T} - 1} \tag{5.2}$$

The expression for the internal energy given is difficult to work with since all polarizations for all wavevectors must be known, therefore several simplifying

assumptions can be made. It is usual convention to replace the summation of all wavevectors with an integral. In order to accomplish this the density of states must be defined, $D(\omega)d\omega$. Upon substitution the internal energy expression transforms into equation (5.3).

$$U = \sum_{p} \int \frac{D(\omega)\hbar\omega}{e^{\hbar\omega/k_B T}-1} d\omega \tag{5.3}$$

There exist several models for the density of states expression however the most popular was developed by Debye [85]. Under the Debye approximation the relationship between the frequency and wavevector is assumed to be linear by $\omega = vk$, where v is the phase velocity. The density of states can therefore be expressed as equation (5.4) [85].

$$D(\omega) = \frac{dN}{d\omega} = \frac{V\omega^2}{2\pi^2 v^3} \tag{5.4}$$

Here V is the volume of the sample and N is the number of vibrational modes present. If there are N number of cells in a crystal the total number of modes is also represented by N. Therefore there exists a cutoff point at the wavevector (equation (5.5)); this wavevector is located at the edge of the so-called Brillouin zone. In considering a general three-dimensional case the Debye approximation assumes a spherical Brillouin zone in frequency space, which in most cases is not accurate. However, despite this inaccuracy the Debye approximation has been able to reproduce experimental data with acceptable results.

$$k_D = \frac{\omega_D}{v} = \left(\frac{6\pi^2 N}{V}\right)^{\frac{1}{3}} \tag{5.5}$$

In applying the Debye approximation the internal energy of the crystal can be simplified down to equation (30).

$$U = \sum_p \int_0^{\omega_D} \frac{V}{2\pi^3 v_p{}^3} \frac{\hbar\omega^3}{e^{\hbar\omega/k_B T - 1}} d\omega \tag{5.6}$$

Now that an expression has been developed for the internal energy of a lattice movements toward a theoretical thermal conductivity expression can be made. From the kinetic theory of gases an expression for the thermal conductivity can be realized with the familiar form of equation (5.7).

$$\kappa = \frac{1}{3} c_v l \tag{5.7}$$

Here c_v is the specific heat and l is the mean free path, which can also be represented by the expression $l = v\tau$. The time between collisions, also known as the relaxation time, has now been introduced as τ. Recalling the thermodynamic definition of the specific heat, c_v can then be expressed as equation (5.8).

$$c_v = \left(\frac{\partial U}{\partial T}\right)_v = \sum_p \frac{V\hbar^2}{2\pi^2 v_p{}^3 k_B T^2} \int_0^{\omega_D} \frac{\omega^4 e^{\hbar\omega/T}}{\left(e^{\hbar\omega/k_B T} - 1\right)^2} d\omega \tag{5.8}$$

By combining equations (5.7) and (5.8) an expression for the thermal conductivity of the lattice results as equation (5.9).

$$\kappa = \frac{1}{3}\sum_{p}\frac{V\hbar^2}{2\pi^2 v_p{}^2 k_B T^2}\int_0^{\omega_D}\tau_p(\omega,T)\frac{\omega^4 e^{\hbar\omega/T}}{\left(e^{\hbar\omega/k_B T}-1\right)^2}d\omega \tag{5.9}$$

From this point there are still many problems in solving for an accurate value of the thermal conductivity. The most significant problem occurs when trying to approximate the relaxation time since it can be temperature and frequency dependent. Many methodologies have been developed in order to simplify the solution to the phonon transport model of thermal conductivity, each one with their advantages and disadvantages. In this work one major type of modeling methodology was used which was developed by Callaway. This will be discussed in detail in the following section. In addition, modeling results will be presented and compared to experimental data

5.1.3 Callaway Type Phonon Modeling

The Callaway model for thermal conductivity accounts for thermal transport by acoustic phonons only [86]. Figure 36 shows the phonon dispersion curve for wurtzite GaN in several of the major symmetry directions in the Brillouin zone. Noting that the group velocity of the phonons is defined as $v_g = d\omega/dk$ it is possible to see that only acoustic phonons move energy; optical phonons have a near zero group velocity and therefore represent a standing lattice wave. Callaway also makes some simplifying

assumptions of the phonon velocity. An averaged single branch phonon velocity over all three modes is calculated by using equation (34) [87].

$$v_{ave} = \left[\frac{1}{3}\left(\frac{1}{v_l} + \frac{1}{v_{t1}} + \frac{1}{v_{t2}}\right)\right]^{-1} \tag{5.10}$$

Using this velocity averaging scheme and by defining a non-dimensional phonon frequency, $x = \hbar\omega/k_B T$, the thermal conductivity expression previously developed can be represented in the more standard form in equation 5.11 [87].

$$\kappa = \left(\frac{k_B}{\hbar}\right)^3 \frac{k_B T^3}{2\pi^2 v_{ave}} \int_0^{\theta_D/T} \tau_c(x,T) \frac{x^4 e^x}{\left(e^x - 1\right)^2} dx \tag{5.11}$$

In the above equation θ_D is the Debye temperature and τ_c is the combined relaxation time due to all phonon processes. This combined relaxation time is found by using Mattheissen's rule.

$$\frac{1}{\tau_c} = \sum_i \frac{1}{\tau_i} \tag{5.12}$$

Relaxation time expressions have been developed for three phonon umklapp processes, boundary, point defect, screw dislocations, edge dislocations, mixed dislocations, and dislocation core scattering [78, 86-97]. These relaxation times have been used in order to predict the behavior of the thermal conductivity of several of the materials that were tested with the 3ω method in §4.1. Specifically samples of sapphire, $LiGaO_2$, ZnO, and

undoped GaN, and the InGaN LED structure were investigated; the analysis of each material follows.

5.1.4 Sapphire Thermal Conductivity Model

The sapphire wafers that are commonly used to grown GaN films are (0001) oriented. This means that the c-axis is perpendicular to the grown direction. For this reason the thermal conductivity along the c-axis was examined in the model. Upon inspection of the phonon dispersion curves (Figure 64) it can be seen that the typical Callaway approximations are valid. The Debye approximation to the density of states as well as the relaxation time approximation was also employed in this analysis.

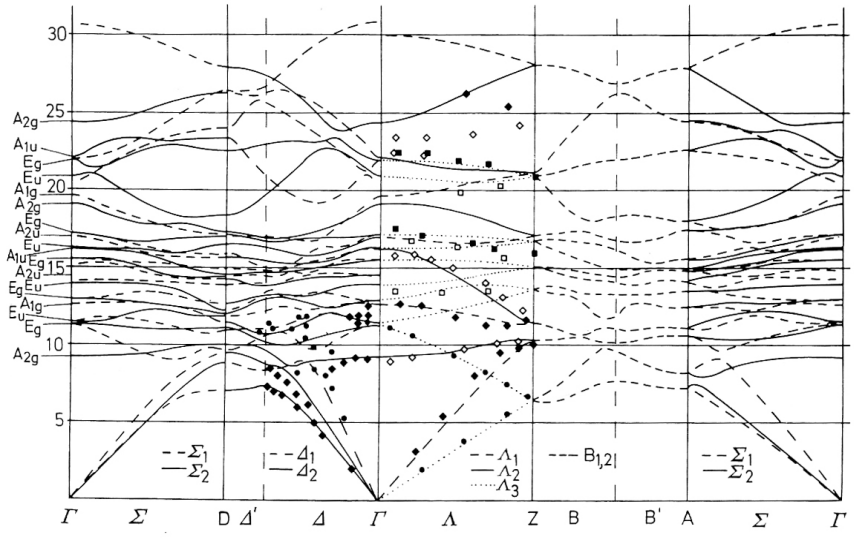


Figure 64. Phonon dispersion curves for sapphire for various directions through the Brillouin zone. The direction considered in this model (along the c-axis) corresponds to the Γ-Z direction due to the rhombohedral crystal structure. From [98].

It is possible to calculate the velocities of each phonon polarization from the dispersion curves, however they can also be estimated from the elastic constant tensor

[99]. This way the single phonon branch can be characterized as outlined previously. The following relationships hold for all hexagonal type crystal structures along the (001) direction [100]. Table 8 provides a summary of other material properties used in the calculation of the thermal conductivity.

$$v_l = \sqrt{\frac{C_{33}}{\rho}} \tag{5.13}$$

$$v_t = \sqrt{\frac{C_{44}}{\rho}} \tag{5.14}$$

While sapphire is a common material for epitaxial growth, relatively little research has been directed toward characterization of the thermal properties. Therefore it was impossible to develop a phonon transport model without the aid of fitting parameters. Difficulties in developing accurate relaxation time expressions also led to the use of fitting parameters. The phonon scattering events that were considered were due to defects, normal processes, and umklapp processes. Expressions for each process are shown below and are based off the work of Holland and Klemens.

$$\tau_d^{-1} = A\omega^4 \tag{5.15}$$

$$\tau_n^{-1} = B_1 T\omega^2 \tag{5.16}$$

$$\tau_u^{-1} = B_2 T^3 \omega^2 \exp\left(\frac{-\theta_D}{\gamma T}\right) \tag{5.17}$$

The coefficients A, B_1, and B_2 were determined by minimizing the error between the experimental data and the model prediction by using the Nelder-Mead simplex method; Figure 65 shows the results of the modeling.

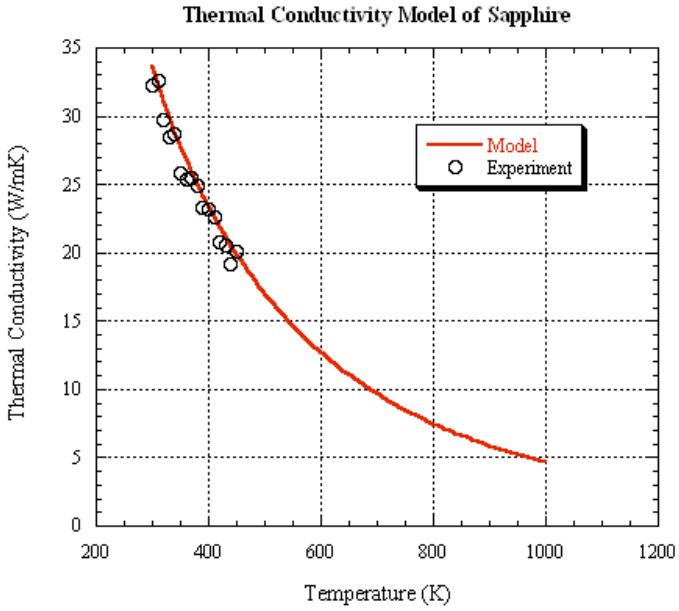


Figure 65. Thermal conductivity of a (0001) sapphire wafer used to grow GaN. The model was based on a modified Callaway approach. The model has been extrapolated out to predict the high temperature response of the wafer.

Table 8. Outline of the material properties of sapphire used in the model. The sound speeds were calculated from the elastic constants from [99]. The coefficients found when performing the error minimization routine are also shown. The values here are assumed to be independent of frequency and temperature and have therefore been used to extrapolate out to high temperatures.

Density	3980 kg/m^3
Molecular Weight	110.962 kg/mol
Gruneisen Parameter	0.74
Transverse Acoustic Speed	6081.52 m/s
Longitunidal Acoustic Speed	11181.46 m/s
A (sec^3)	3.5822x10^{-43}
B1 (sec deg)	1.7301x10^{-19}
B2 (sec deg^{-3})	1.2746x10^{-23}
θ_D (Debye Temperature)	961 K
ω_D (cut off frequency)	1.2593x10^{14} s^{-1}

5.1.6 ZnO Thermal Conductivity Model

The model for the ZnO sample was very similar to the model discussed for sapphire. Before proceeding the phonon dispersion curves must be examined to make sure that the Callaway approximations were valid. Figure 66 shows the theoretical dispersion curves as well as some experimental data. Unlike sapphire, ZnO has a wurtzite crystal structure and therefore the direction under investigation is the Γ-A direction (along the c-axis).

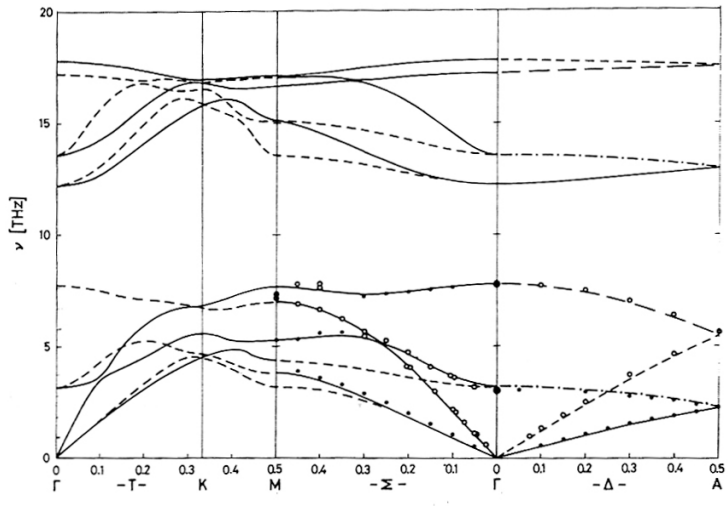


Figure 66. Phonon dispersion curves for the ZnO wurtzite crystal structure. The curves show that the optical modes are nearly stationary, which validates the use of the Callaway model. From [101-103].

The only difference between the two runs was the material specific properties, which have been outline in Table 9. The results of the modeling are shown in Figure 67.

Table 9. Outline of the material properties of ZnO used in the model. The sound speeds were determined from the elastic constants from [104]. The coefficients found when performing the error minimization routine are also shown. The values here are assumed to be independent of frequency and temperature and have therefore been used to extrapolate out to high temperatures.

Density	5675 kg/m^3
Molecular Weight	81.408 kg/mol
Gruneisen Parameter	0.74
Transverse Acoustic Speed	2736.6 m/s
Longitunidal Acoustic Speed	6077.32 m/s
A (sec^3)	9.0325x10^{-42}
B1 (sec deg)	5.6452x10^{-21}
B2 (sec deg^{-3})	4.0098x10^{-25}
θ_D (Debye Temperature)	402 K
ω_D (cut off frequency)	5.2677x10^{13} s^{-1}

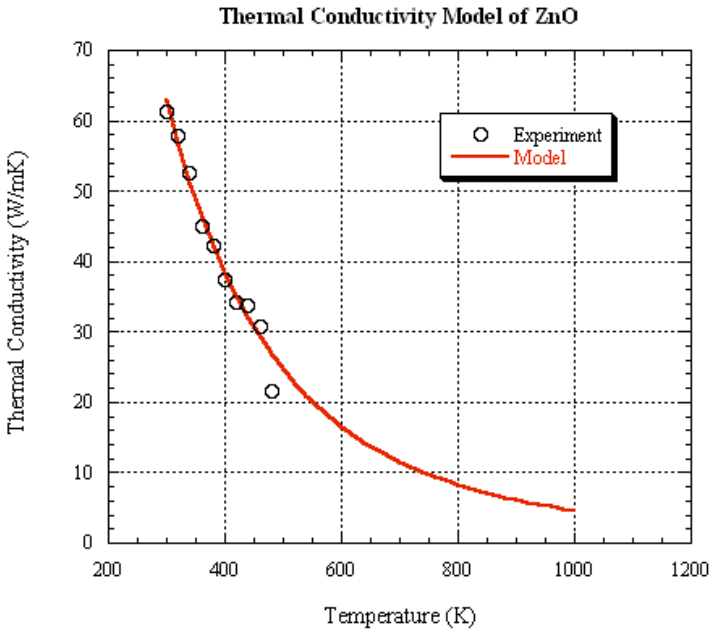


Figure 67. Thermal conductivity of a ZnO wafer used to grow GaN. The model was based on a modified Callaway approach. Calculations have been extrapolated out to predict the high temperature response of the wafer.

5.1.7 $LiGaO_2$ Thermal Conductivity Model

The model for the $LiGaO_2$ sample was very similar to the model discussed for sapphire. Due to a lack of research on $LiGaO_2$ the phonon dispersion curves were not available to verify the assumptions made in the Callaway model. Experimental data was gathered from 80K up to 500K, which allows for both a high temperature and low temperature approximation. The difference in the two models was the weighting of the N-phonon process relaxation times; "high" temperature is considered to be above 240 K. Relaxation times that were used are shown in.

Table 10. The relaxation time expressions used in the modeling of $LiGaO_2$. All expressions are taken from Holland [91].

Scattering Process	Inverse Relaxation Time
Impurities (mass difference)	$\tau_I^{-1} = A\omega^4$
Three Phonon Scattering:	
N Process	
Low Temperature	$\tau_N^{-1} = B_1 T^3 \omega^2$
High Temperature	$\tau_N^{-1} = B_1 T \omega^2$
U Process	$\tau_U^{-1} = B_2 T^3 \omega^2$

Table 11. Outline of the material properties of $LiGaO_2$ used in the model. The sound speeds were calculated using the elastic constants taken from [105].

Density	4170 kg/m^3
Molecular Weight	108.6628 kg/mol
Transverse Acoustic Speed	3700 m/s
Longitunidal Acoustic Speed	5794.23 m/s
θ_D (Debye Temperature)	547.39 K
ω_D (cut off frequency)	7.1661×10^{13} s^{-1}

Table 12. The coefficients found when performing the error minimization routine are also shown. The values here are assumed to be independent of frequency and temperature and have therefore been used to extrapolate out to both high and low temperatures. Values found are similar in magnitude to those found in [91].

Coefficient	High Temperature	Low Temperature
A (sec^3)	2.3283×10^{-42}	7.246×10^{-45}
B1 (sec deg^3)	1.0688×10^{-24}	1.8836×10^{-23}
B2 (sec deg^3)	2.9939×10^{-24}	2.4177×10^{-23}

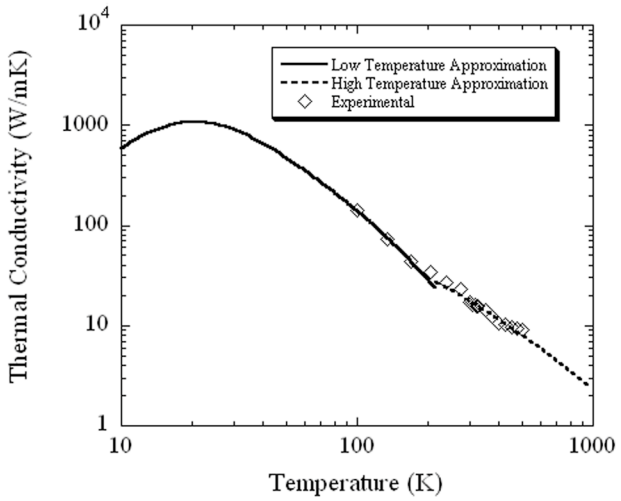


Figure 68. Thermal conductivity of a $LiGaO_2$ wafer used to grow GaN. The model was based on a modified Callaway approach.

The model shows good agreement with the experimental data with the largest deviation at room temperature where the transition from the high temperature to the low temperature model occurs. Based on this model, a peak thermal conductivity of 1081 W/mK is expected to occur near 21K

5.1.8 GaN Thermal Conductivity Model

The approach with GaN differs slightly from the analysis performed on the three previous materials. Gallium nitride is widely studied and as a result there exists relaxation time expressions that do not depend on any fitting parameters [78, 87-90]. This allows a study of the effects of different crystal imperfections to be performed by changing key physical parameters like the dislocation density or impurity concentration both of which can be experimentally determined. While the relaxation time expressions differ the combined time is still found with Mattheissen's rule.

The temperature dependent thermal conductivity of an undoped GaN sample was initially studied with the 3ω method and the results of the test were presented in Figure 47. Using the relaxation time expressions presented in [87] the thermal conductivity was calculated. The result of the analysis is presented in Figure 69. As inputs to the model various impurity concentration profiles can be selected. Due to the thermally induced dissociation of the metal-organic carrier gases hydrogen, carbon, oxygen, and silicon are the major impurities found in MOCVD grown GaN films. Table 13 shows four common impurity profiles that were studied; other material parameters are located in Table 14.

Table 13. Common impurity concentrations found in GaN. (a) From [88]. (b) From [87].

Atom	I (cm^{-3})[a]	II (cm^{-3})[b]	III (cm^{-3})[b]	IV (cm^{-3})[b]
Hydrogen	$4x10^{18}$	$2x10^{17}$	$3x10^{18}$	$1.4x10^{20}$
Carbon	$1.5x10^{18}$	$3x10^{16}$	$6x10^{15}$	$2x10^{17}$
Oxygen	$2x10^{18}$	$1x10^{17}$	$6x10^{16}$	$3x10^{16}$
Silicon	$8x10^{17}$	$3x10^{16}$	$1.5x10^{18}$	$1.4x10^{20}$

Table 14. Properties of GaN used in the thermal conductivity model. The sound speeds were calculated from the elastic constants from [106].

Density	6150 kg/m^3
Molecular Weight	83.7236 kg/mol
Transverse Acoustic Speed	4130 m/s
Longitunidal Acoustic Speed	8040 m/s
θ_D (Debye Temperature)	613.64 K
ω_D (cut off frequency)	$8.0335x10^{13}$ s^{-1}

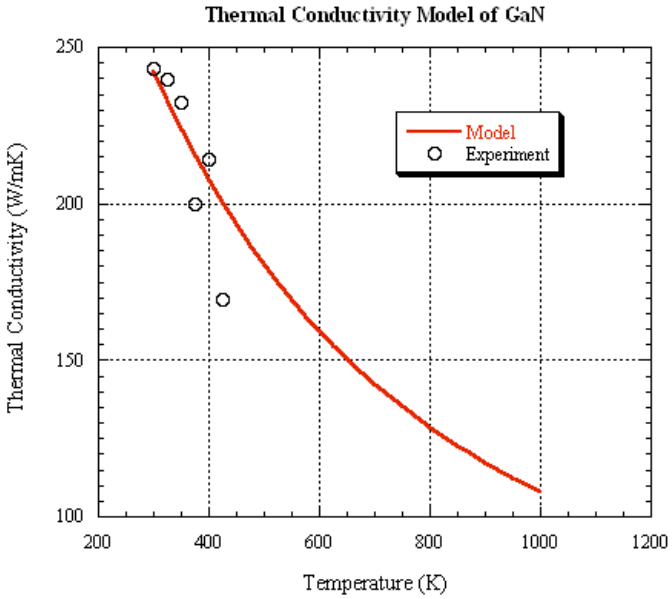


Figure 69. Thermal conductivity model of undoped GaN as a function of temperature. The model shows relatively good agreement with the experimental data. The dislocation density for this model was $2x10^{12}$ cm^{-2}; the impurity concentrations are given by profile II in Table 13.

The effects of dislocations and temperature on the thermal conductivity of the GaN layer were also estimated. The results of integrating equation (5.11) are shown in Figure 70. It should be noted that the results in Figure 70 were calculated using a Debye temperature of 613K for GaN. This value varies significantly from the results in [87] and [88] however it is supported by [107]. Variation in the Debye temperature will alter the upper limit of integration in (5.11). In all the cases that are plotted, the effect of dislocation densities below 10^{13} cm^{-2} plays a minor role in thermal conductivity of GaN.

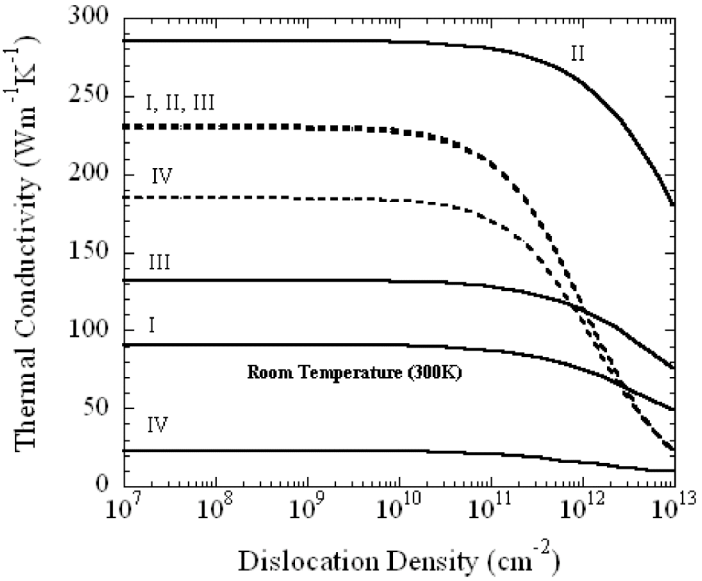


Figure 70. Thermal conductivity of GaN for various impurity concentrations shown in Table 13. The dashed lines represent solutions found by the method of Kotchetkov. The solid lines represent solution found by the method of Zou. Note the negligible difference in I, II, and III using the method of Kotchetkov [88].

5.2 Electronics Packaging

Temperature data of a MQW LED and a HFET was gathered and presented in §4.2. This data along with information about the material properties found with the 3ω method has been used in order to develop FEA models to predict the packaging requirements of high power devices. Presented in this section will be details of the numerical models used and the results that were obtained.

5.2.1 Multi-Quantum Well Light Emitting Diode

Several analytical tools were used in order to characterize the thermal performance of a LED structure. Analytical solutions to the heat equation along with

FEA models built in FEMLAB were employed in order to investigate the effect of the substrate material, package design, thermal interface material, heat spreader, and convection conditions.

With temperature data gathered from infrared imaging and micro-Raman a compact numerical model was developed in the commercially available FEMLAB modeling software in order to predict the effect of different packaging schemes on device temperatures. The system was modeled in three dimensions and included temperature dependent material properties. The equation that was solved is the familiar three-dimensional energy equation. Heat generation in the device was considered to be a surface heat flux directly on the substrate that was uniformly distributed over an area the shape of the light pumping region of the LED as seen in Figure 71.

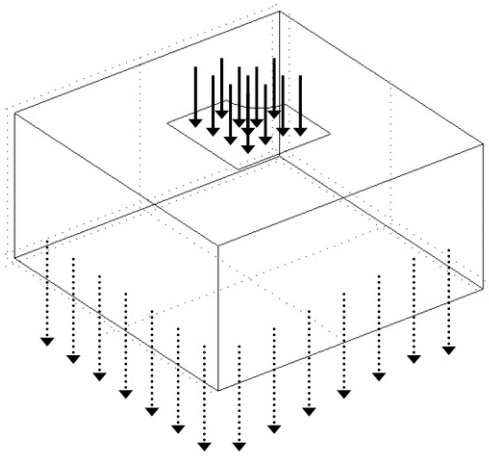


Figure 71. Heat flux boundary conditions on the numerical model. Dashed arrows on bottom surface indicate a uniform heat flux condition across the entire surface. All other surfaces are considered adiabatic. From [108]

By choosing the boundary condition this way the complications in meshing the extremely high aspect ratios of the actual MQW stack are avoided. Furthermore, this assumption leads to an upper bound on the temperature of the device and will not jeopardize the device during actual operation. Effects of the package on the device temperature were modeled as a heat flux boundary condition on the opposite side of the substrate. Typical thermal resistances of packages can range from 3-240K/W depending on the manufacturing method [109]. Good agreement between experimental and numerical models occurred with a total package resistance of 140K/W which is reasonable considering the device was mounted in a simple TO-can with the use of a non-thermally conductive epoxy. All other boundary conditions in the model were considered to be adiabatic. The results of the model are presented in Figure 59. With the developed numerical model the effect of different packaging technologies was investigated. Also varied in this study was the effect of the substrate material used for the epitaxy of the LED device (sapphire, ZnO, single crystal GaN, and SiC). These materials offer superior epitaxial growth possibilities due to similar lattice parameters with the GaN active layers, higher thermal conductivity and good optical properties. The following graphs are presented which show the effects of packaging and growth substrate.

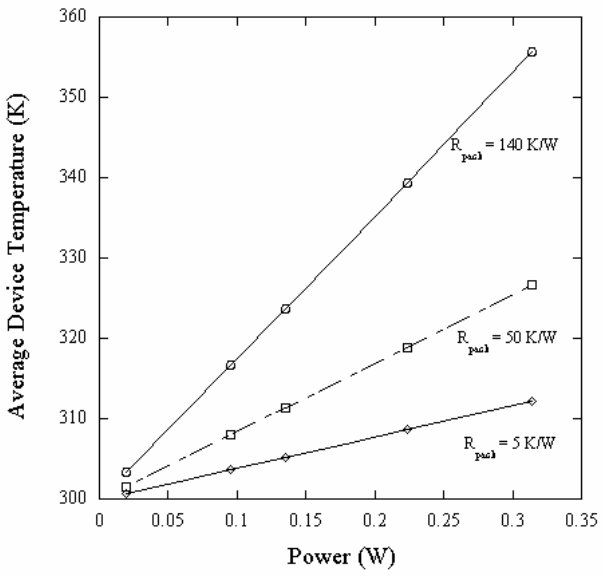


Figure 72. LED package design parameters' effect on device temperature for a device grown on a sapphire substrate.

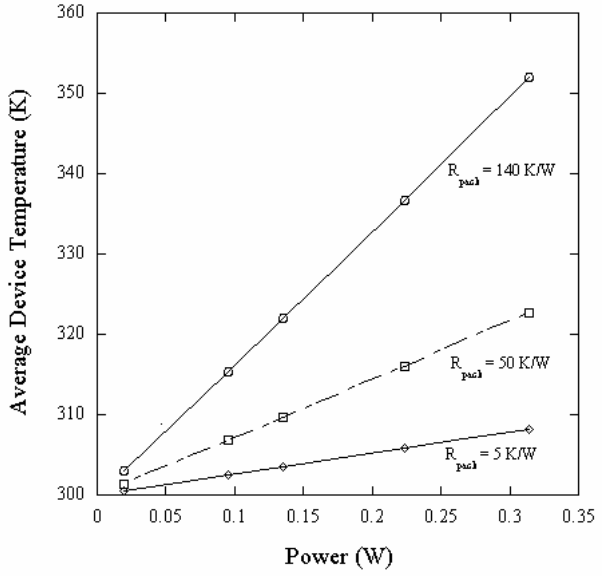


Figure 73. LED package design parameters' effect on device temperature for a device grown on a ZnO substrate.

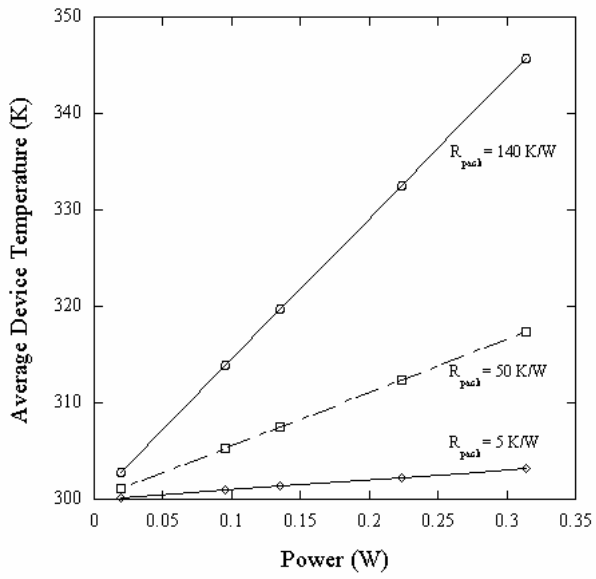


Figure 74. LED package design parameters' effect on device temperature for a device grown on a single crystal GaN substrate

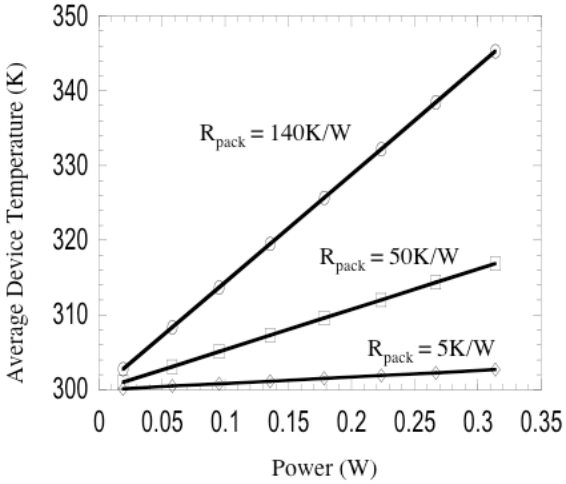


Figure 75. LED package design parameters' effect on device temperature for a device grown on a SiC substrate. Note that there is not much change in device temperature from that mounted on single crystal GaN.

Figure 72, Figure 73, Figure 74, and Figure 75 illustrate how the thermal resistance of the package can dominate over the resistance of the substrate that the device is grown on, making an efficient design of the package a priority in reducing the overall temperature of the device. Furthermore the thermal conductivity of the MQW stack is only important in obtaining detailed measurements of the temperature distribution within the device

itself. As can be seen from the above graphs the focus should be drawn to packages that achieve thermal resistances of ~5K/W since they offer a substantial decrease in average device temperature. In fact there is only a 3% decrease in average device temperature when comparing a sapphire substrate device to a GaN substrate device with a package thermal resistance of 140K/W. By comparison there can be as much as a 12% decrease by moving to a package thermal resistance of 5K/W. Currently there are a number of different materials that are used for thermal issues encountered in high power electronics. Most advanced materials can be classified into six categories; monolithic carbonaceous materials (MCMs), metal matrix composites (MMCs), carbon/carbon composites (CCCs), ceramic matrix composites (CMCs), polymer matrix composites (PMCs), and advanced metallic alloys (AMAs) [15]. Typical thermal conductivities have been reported in [15] and summarized in
Table 15.

Table 15. Advanced packaging material properties given in [15].

Material	Thermal Conductivity (W/mK)
Copper/Molybdenum/Copper	182
Epoxy Resin	1.7
Al Matrix w/ Continuous Carbon Fibers	218
Epoxy Matrix w/ Graphite Fibers	370
Copper Matrix w/ Diamond Particles	600

With the aid of these advanced materials a design for high power LEDs was developed based on the Lumileds Luxeon III package. The overall package thermal resistance includes several system parameters that contribute in different ways. In development of the thermal design the relative contribution of each thermal resistor to the network was investigated. By studying individual resistors it is possible to suggest improvements that greatly enhance the overall ability of the package to dissipate heat. As suggested by the roadmap outlined in Table 2 the overall thermal resistance should be <5K/W for high power operation. The system that is under investigation is diagramed in Figure 76.

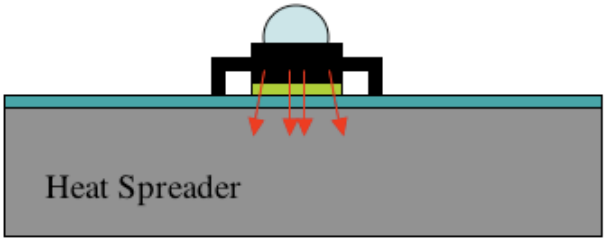


Figure 76. The LED mounting system. A thermal interface material is shown directly under the LED. The LED needs to be mounted on a dielectric epoxy layer in order to construct the electrical traces.

The representative resistance network that was developed is shown in Figure 77 and shows contributions from the package, thermal interface material, dielectric epoxy layer, heat spreader, and convection from the backside of the board.

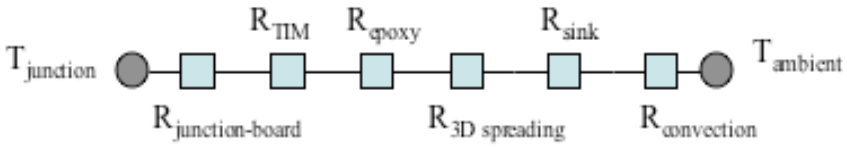


Figure 77. Resistor network model of the LED packaging system. All resistors have degrees of freedom in their design however the epoxy dielectric layer was fixed to be 1.24K/W, which represents a 100μm thick layer of epoxy (k=1.4W/mK).

To investigate the junction-board thermal resistance a 3D model was developed in order to investigate the junction to board thermal resistance; this resistor represents the resistance from the chip attachment area to the board attachment points including all 3D effects. An exploded view of the package is shown in Figure 78.

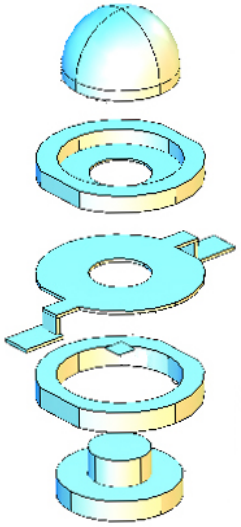


Figure 78. Exploded view of the LED package. The components from the top down are the lens, upper plastic housing, copper electrical leads, bottom plastic housing, and metal slug. The LED chip is flip-chip bonded to the metal slug in order to provide an efficient heat removal path.

Currently the metal slug that the LED chip is mounted to is made from a copper alloy with a relatively high thermal conductivity when compared to traditional packaging materials. However several of the advanced metal matrix composites suggested in [15] have a thermal conductivity of 2-3 times that of copper. In order to improve the performance of the LED package the slug material was varied and the overall thermal resistance of the package was calculated using the FEA model; the maximum temperature difference was fixed at 125°. A sample temperature distribution slice is shown in Figure 79 with k_{slug}=500W/mK and a convection coefficient of 5W/m^{2}K over the lens. By imposing the temperature difference at the junction and base of the package the total heat flux can be found by integrating the gradient of the temperature over the base area. The thermal resistance can then be found by $R = \Delta T / Q$; the results from calculations are shown in Figure 80.

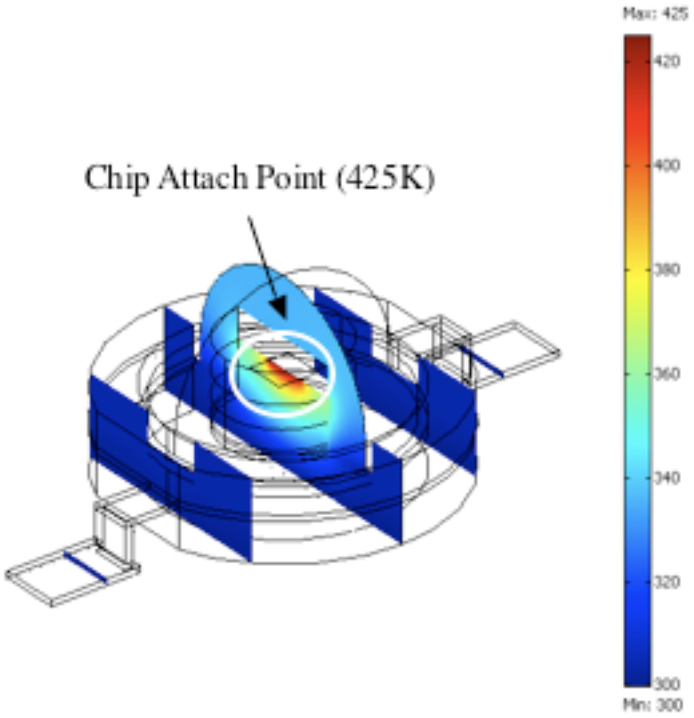


Figure 79. Sample temperature distribution within the LED package. The graph only shows slices of the total solution in order to reveal the temperature distribution under the chip.

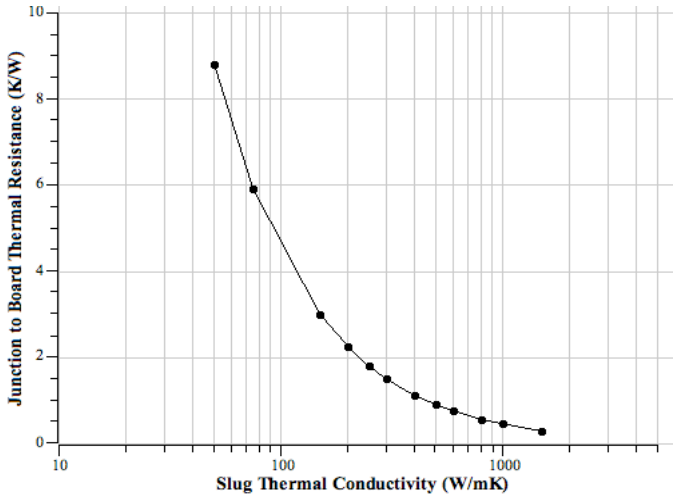


Figure 80. Junction to board thermal resistance as a function of slug material. As expected the thermal resistance of the package can decrease significantly with the use of advanced materials.

While cost is certainly an issue with advanced metal matrix composites the small volume of material needed to construct the slug could offset the cost.

The next thermal resistor in the network represents the thermal interface material (TIM). This material is usually a thin layer of low conductivity grease that helps reduce the contact resistance between the two materials. While this material is usually a very thin layer, on the order of 100μm thick, it can contribute significantly to the overall resistance due to the relatively low thermal conductivity. Several commercially available TIMs were investigated as possible choices; a table of materials is shown in Table 16 along with their thermal resistances (based on an area of 1 LED, 0.57cm^2).

Table 16. Various thermal interface materials and their thermal resistances. The CNT based materials are from [110]. Other materials are commercially available from their respective manufacturers (Amicon, Epotek, Bergquist, eGraf, Loctite). The materials in bold are those that are possible choices for high power LED packaging.

Material	R (m^2K/W)	R (K/W)
Amicon E3503-1	2.548E-04	4.46
Epotek T7109	3.612E-04	6.32
Bond Ply 105	3.920E-04	6.86
Kapton	2.660E-04	4.65
Graphite Sheet (100psi) eGraf 1205	**1.000E-05**	**0.1749309**
Graphite Sheet (15psi) eGraf 1205	**3.200E-05**	**0.5597788**
Pure S160 (1e-4m thick)	2.500E-04	4.3732717
S160 .4% random CNTs (1e-4m thick)	2.000E-04	3.4986173
S160 .4% aligned CNTs (1e-4m thick)	**1.20E-04**	**2.0991704**
Loctite PCM Powerstrate Xtreme (80psi)	**2.20E-06**	**0.0384848**

While several of these materials have been identified as potential TIMs they usually require high pressures in order to obtain low resistances. This is not desirable for electronics as it introduces stress into the system that can cause premature failure due to the difference in thermal expansions when thermally cycled. It is therefore preferred to have a compliant material at the interface to eliminate any stresses that form. Carbon nanotube based materials have been introduced in [110] and [111] show promise to enhance the effective thermal conductivity of more compliant greases like those made by Amicon, Epotek, and Bergquist. Phase change materials like those made by Loctite also can benefit from an increased effective thermal conductivity. However in this study the focus will be on traditional greases not phase change materials. Following the modeling methods of Xue the effective thermal conductivity of a carbon nanotube composite can be calculated [112]. Xue's model includes percolation effects as well as dimensional effects of the nanotubes. In this work the nanotubes were assumed to be 50,000nm long and 25nm in diameter and have a thermal conductivity of 3000W/mK.

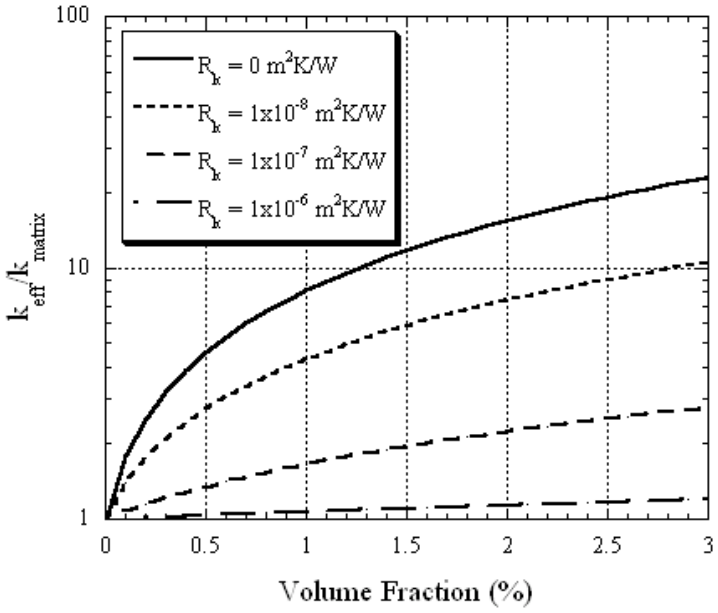


Figure 81. Thermal conductivity enhancement of a thermal interface material. R_K is considered to be the thermal resistance at the interface of the nanotube and the matrix. A large increase in the effective thermal conductivity can be seen at relatively low volume fractions.

It can be seen from Figure 81 that a large increase in the thermal conductivity of the TIM can be possible with relatively low volume fractions of nanotubes. For further investigation a matrix with a thermal conductivity of 1W/mK was simulated and the thermal resistance of a 100μm thick layer was calculated, the results are shown in Figure 82.

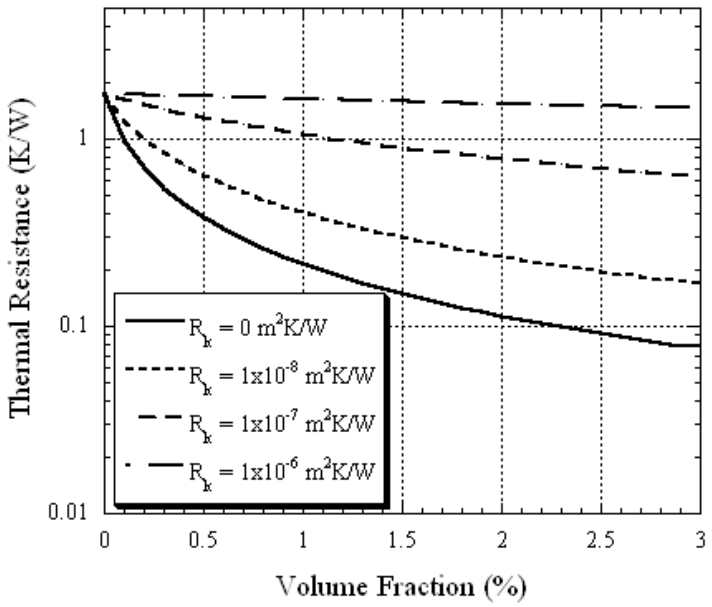


Figure 82. Thermal resistance of a thermal interface material with carbon nanotube loading. The steep decrease in the resistance is due to percolation effects of the nanotubes. This effect relies on a low Kapitza resistance at the interface of the nanotube and the matrix.

From this analysis it is theoretically possible to drastically decrease in the thermal resistance of the TIM by incorporating high thermal conductivity carbon nanotubes. Further work is still needed in order to reduce the cost of manufacturing large quantities of nanotubes in order to make high performance TIMs a reality.

Another key component in the LED package resistor network is the heat spreader that the LED is mounted to. A balance of geometry, convection conditions, and materials selection for this component is critical for maximum power dissipation by the LEDs. In order to model the thermal resistance of the heat spreader the 3D heat equation was solved, details of which are found in [113]. The boundary conditions were chosen to be adiabatic on all surfaces of the cube except for the heat flux input from the LED and then

a convective boundary on the backside of the spreader. These conditions model a LED in the middle of an array of similar devices as depicted in Figure 83.

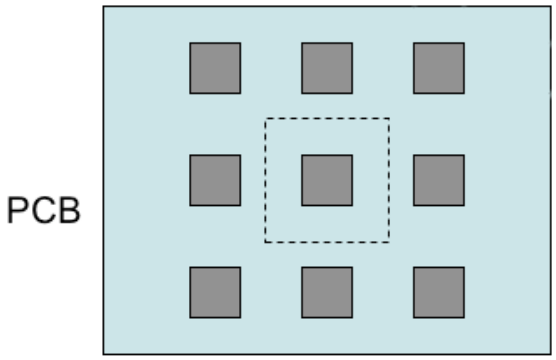


Figure 83. A top view of the LED contact points (grey squares). The dotted line is the domain that is being simulated in the resistor network. Due to symmetry conditions imposed in the analysis the LED being simulated is surrounded by other LEDs in a rectangular array.

The thermal resistance was calculated by using the solution developed in [113] and plotted as a function of geometry, convection coefficient, and material thermal conductivity. The results are shown in Figure 84. This graph shows that the thermal resistance is only a weak function of the convection coefficient on the backside. It also shows that once the thermal conductivity of the spreader is >300W/mK there is not much change in the thermal resistance. As a result of this a material such as aluminum with a moderate thermal conductivity (218W/mK [114]) can be used in place of much more expensive metal matrix composites.

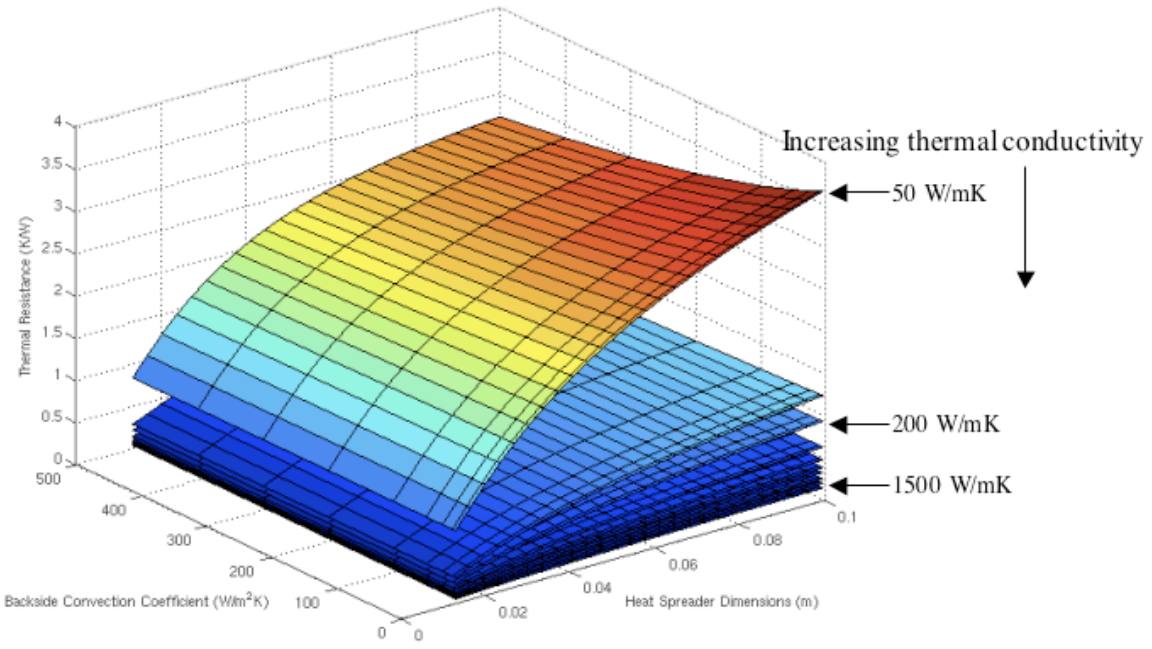


Figure 84. Thermal resistance of a flat plat (2mm thick) heat spreader as a function of geometry, convection condition, and material.

As an aid to designing an array of LEDs the dimension of the heat sink has been converted to a packing density of LEDs per 10cm x 10cm area and the maximum power dissipated by the LED has been calculated. For this particular run the convection coefficient was varied from 5W/m^{2}K to 500W/m^{2}K, the heat spreader was built from aluminum, and the TIM material was the Loctite phase change material (PCM) outlined in Table 16. Knowing that the LED's maximum temperature was 125^o above room temperature the maximum power dissipated by the device can be calculated from the results of the resistor network. The packing density of LEDs and the maximum power dissipated has been plotted in Figure 85.

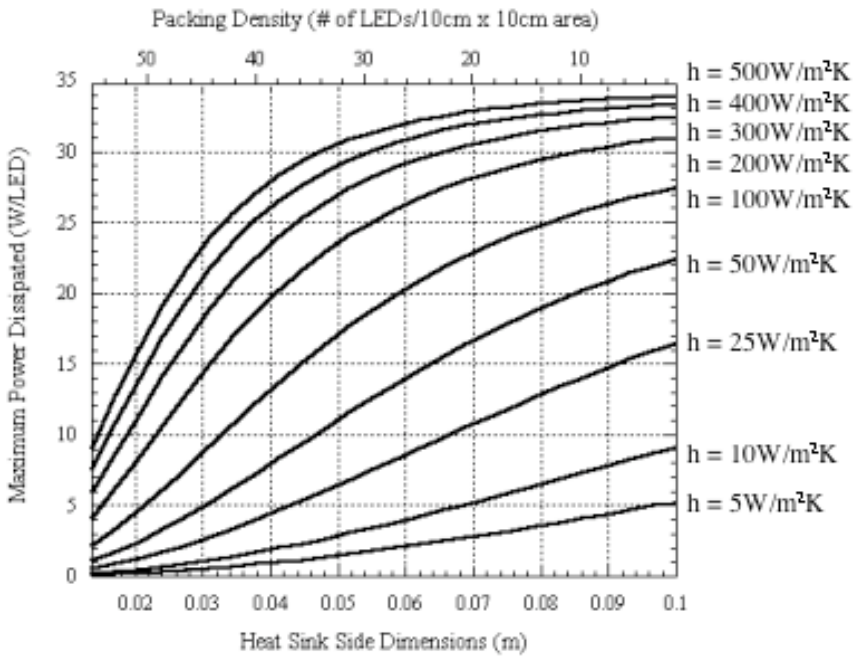


Figure 85. Maximum power dissipated for a ΔT of 125° for various packing densities of high power LED components on a square flat plate heat sink under different convection conditions.

It can be seen from this graph that for very high power devices (>5W/LED) it is necessary to reduce the convection coefficient resistance by utilizing forced air convection or other high heat flux removal technologies. . To further understand the relationship between all of the resistors several cases were investigated to studied. In many cases the last resistor in the network $R_{convection}$ represents up to 99% of the total package resistance. For the following runs the $R_{junction\text{-}to\text{-}board}$ was calculated from a slug material with k=500W/mK, the resistance from the Loctite PCM TIM material was used, and an aluminum heat sink was chosen with an area of 3cm^2. The detailed breakdown of the value of the resistors for convection coefficients of 500W/m^{2}K, 100W/m^{2}K, and 10W/m^{2}K is shown in Figure 86.

A

Resistor	Magnitude (K/W)	Percent of Total (%)
R (junction to board)	0.91788	9.32
R (TIM)	0.5597	5.68
R (epoxy)	1.2495	12.68
R (spread)	0.2103	2.13
R (sink)	0.0316	0.32
R (convection)	6.8829	69.86
Total	9.85188	
Power Dissipated	11.8376	W

B

Resistor	Magnitude (K/W)	Percent of Total (%)
R (junction to board)	0.91788	2.46
R (TIM)	0.5597	1.50
R (epoxy)	1.2495	3.34
R (spread)	0.211	0.56
R (sink)	0.0316	0.08
R (convection)	34.41	92.06
Total	37.37968	
Power Dissipated	3.2816	W

C

Resistor	Magnitude (K/W)	Percent of Total (%)
R (junction to board)	0.91788	0.26
R (TIM)	0.5597	0.16
R (epoxy)	1.2495	0.36
R (spread)	0.2103	0.06
R (sink)	0.0316	0.01
R (convection)	344.14	99.14
Total	347.10898	
Power Dissipated	0.3601	W

Figure 86. Thermal resistor breakdown for a high power LED packaging situation under different backside convection conditions. (A) 500W/m^{2}K. (B) 100W/m^{2}K. (C) 10W/m^{2}K. Notice the large increase in the possible power dissipated for a set ΔT of 125^o for case A.

Current technology limits the temperature rise of the LED junction to ~125^o, however there are devices that are currently being made that can withstand temperatures rises up to 180^o. Under the same conditions that the results in Figure 86 were created a high temperature device was simulated which led to power dissipations of 18.27W, 4.8148W, and .5186W for the previously mentioned convection conditions.

5.2.2 High Field Effect Transistor (HFET)

A finite element model of the HFET was built in FEMLAB in order to study the effects of different packaging schemes on the temperature of the device. Difficulty in developing a fully coupled electro-thermal model led to solving the heat equation only. Due to the geometry of the HFET it was found that a 2D solution was adequate in order to capture the thermal response of the device. Material properties that were needed for

the model were found from the 3ω experiments outlined in §4.1. Boundary conditions that were used included effects from radiation, convection and conduction. The black body radiation assumption was not used since emissivity data was available from the calibration during the IR experiments; an adjusted emissivity of 0.8 was used. Convection conditions were considered to be in the natural flow regimes with a convection coefficient of $10 W/m^2K$, although Rayleigh numbers make convection heat losses nearly negligible [114]. Heat from the generating region was also allowed to flow into the substrate as well as into the air mass above the device. Other analyses have shown that the heat generation in FET-type devices has been located near the gate, the area of peak electric field [115-118]. The IR experiments performed support this idea as well as other temperature measuring techniques [73, 74]. It has been assumed that the electron channel at the interface of the AlGaN/GaN is also the major site of heat generation; the channel extends approximately 150Å below the interface [119]. In Figure 87 a detailed picture of the mesh that was constructed in FEMLAB is shown; the total mesh has 60,428 elements.

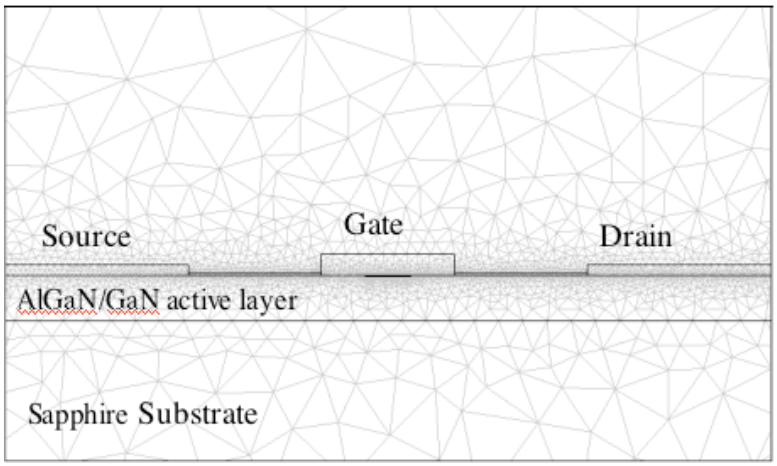


Figure 87. Detailed view of the mesh that was constructed in FEMLAB of one half of the HFET. The heat generation region is located directly below the gate.

Simulations were run at the same power levels shown in Figure 62 and then compared to experiments. In order to achieve good agreement an assumed package resistance of 30K/W was used. The HFET wafer was bonded to a standard ceramic package and therefore a thermal resistance of 30K/W is reasonable. The comparison between the IR results and the FEMLAB model is made in Figure 88.

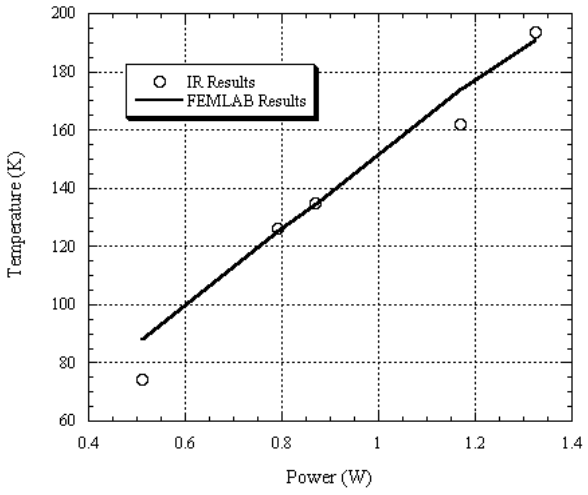


Figure 88. FEMLAB model results plotted with the IR microscope results.

As a first order analysis of the packaging requirements for high power HFET devices the package resistance in the FEMLAB model was allow to vary and the maximum device temperature was observed. For a power dissipation of 1.3W the model shows only a slight dependence on the maximum device temperature. This is primarily due to the already large thermal resistance contribution of the sapphire substrate. Future work will focus on a more detailed analysis of the thermal path and concentrate on major areas of resistance.

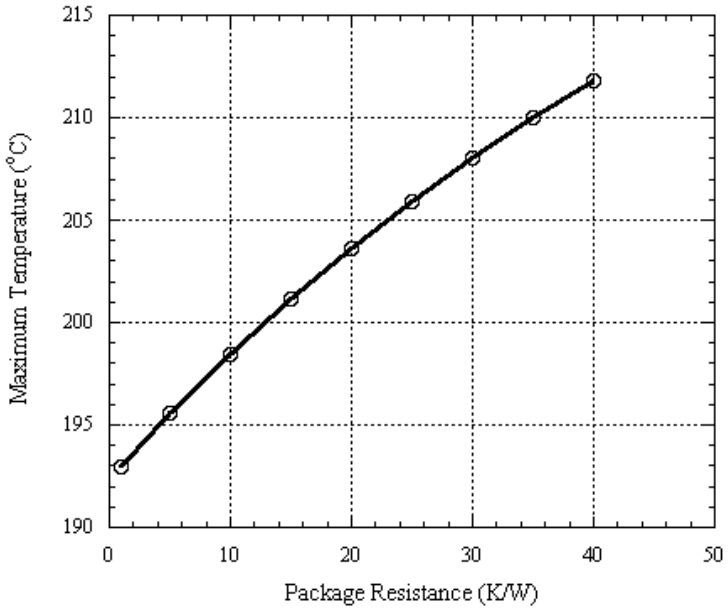


Figure 89. The effect of the package thermal resistance on the maximum device temperature for a power dissipation of 1.3W. The temperature is only a weak function of the package resistance due to the highly resistive sapphire substrate. This result has led to advancements in flip chip attachment to high thermal conductivity circuit boards.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this study, the main objective was to study the thermal properties of III-V semiconductors, in particular GaN thin films and the substrate materials used to grow them. The primary thermal property that this study focuses on was the thermal conductivity, a key parameter for accurate thermal modeling of an active device. Thermal conductivity tests were performed with the 2D generalized 3ω solution method, which is critical when analyzing high thermal conductivity materials for accurate determination of properties. The GaN films were also tested in an environmental chamber in order to observe the behavior as a function of temperature. In addition to several differently doped GaN thin films, samples of sapphire, SiO_2, SiN, $LiGaO_2$, and ZnO were analyzed. Many of these material properties were found simultaneously while testing the GaN, the first time that this has been performed with repeatable results. Upon inspection of the data it has been determined that undoped GaN thin films, grown by MOCVD, have a high thermal conductivity of ~250W/mK at room temperature. Also observed was a decrease in thermal conductivity when dopant materials were introduced. As much as a 55% decrease in the thermal conductivity can be seen when doped with Si atoms (n-type doping). The additional phonon scattering sites that the doping atoms offer can severely affect the material properties.

With the use of phonon modeling techniques developed by Callaway this decrease in thermal conductivity has been verified by using the relaxation time approximation. It is also possible to extrapolate estimates as to the behavior of materials at temperatures that exceed the limits of the test equipment with these same models. This has been done for the substrate materials under investigation as well as undoped samples of GaN. Using Callawy's simplifications and relaxation time expressions available in the literature, the effect of dislocations on the thermal conductivity of GaN was studied as well. Both X-ray diffraction as well as chemical etching/AFM surface scans has verified the quality of the GaN films. These experiments show that the GaN was of very high quality. This explains how the GaN tested in this work has had one of the highest thermal conductivities reported to date.

Knowing the thermal conductivity of the GaN/substrate material system allowed a study of the heat removal from an active device to be performed. Finite element models of both a LED package and a HFET were constructed with FEMLAB in order to aid in the design of efficient packaging designs. For high power applications advanced materials such as metal matrix composites and carbon nanotube based thermal interface materials were investigated in order to improve the passive cooling potential of the packages. It was found that for very high power devices (>5W/LED), like those that will be needed in order to replace conventional lighting, active cooling such as forced air convection or heatpipes will be needed. In order to validate these models temperature maps using micro-IR imaging and micro Raman Spectroscopy were created. Agreement between the models and the experiments was acceptable and therefore the temperature distribution within the active device can be determined.

6.2 Future Work

This research has been focused on several aspects of electronics packaging. Attention has been given to several of the length scales involved in electronics, from the single device level to the system level. Phonon modeling, at the microscale, has been performed using several common assumptions and simplifying conditions, however models can be made that reflect the true shape of the Brillouin zone and would not ignore the energy transfer by high frequency optical phonons. Solving the 3D harmonic oscillator problem using a program such as GULP (General Utility Lattice Program) the full dispersion curve for a crystal can be generated. The need for more accurate phonon transport models to be made also calls for more accurate knowledge of the material under investigation. Utilizing experimental methods such as SIMS (Secondary Ion Mass Spectrometry) or Auger Spectrometry the composition of thin films can be determined. An accurate assessment of the impurities within the GaN films would help to increase the accuracy of phonon based models.

In addition to pure phonon based models of materials attention should turn to a more complete understanding of the behavior of devices. Assumptions made in this work have allowed for the heat equation to be solved uncoupled to other effects. However the physics of devices respond to electric fields generated at the contact as well as stresses in the films. A more accurate model of a device is one that solves the heat equation along with the Poisson equation in order to capture the effects that diffusion of carriers (both electronic and heat) cause. This problem is further complicated by the complexity of current technologies such as HEMTs (High Electron Mobility Transistors) and LEDs, which operate on principles of quantum confinement. The Schrödinger equation must

then be incorporated into the analysis in order to capture the location of electronic carriers. Effort has focused on solving the purely electronic problem in quantum devices in order to determine areas of highest electron concentration under bias. However little has been done in order to incorporate the effects of temperature on device behavior.

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