PART 1

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RESEARCH REPORT APPROVAL SHEET

Project No.__E-21-6MW____
Lab/School/Center:__ECE_____

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A. Report Title___A Switching Noise Analysis Tool for ASICs _____
B. Author(s) and/or PD/PI__ M Swaminathan _____Phone___404-894-3340_____
C. Period Covered:_____Due Date_____

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B. Division Chief or Branch Head _____ Date _____
C. Lab/School/Department/Center Head_____ Date_____
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Georgia Tech Research Corporation

Georgia Institute of Technology
Office of Sponsored Programs
Atlanta, Georgia 30332-0420 U.S.A.

February 17, 2004
In reply refer to: E-21-6MW

Dr. Harold H. Hosack
Semiconductor Research Corp.
1101 Slater Road
Brighton Hall
Durham, NC 27703

Subject: Annual Review Presentation
Project Director(s): Dr. M. Swaminathan
Telephone No.: (404) 894-3340
Contract No.: 2003-NJ-1063
Prime No: N/A
"A Switching Noise Analysis Tool for ASICs""
Period Covered: N/A

The subject report is forwarded in conformance with the contract/grant specifications.

Should you have any questions or comments regarding this report(s), please contact the Project Director or the undersigned at 404-894-4763.

Sincerely,

Thelma Woods
Customer Service Representative

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E-21-6MW
#1

Switch
A Switching Noise Analysis Tool for ASICs

Madhavan Swaminathan
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Task ID:986.001
IBM Custom Funding

Start Date: Jan 1, 2002

Technical Thrust: Packaging and Interconnect Systems

Task Leader: Madhavan Swaminathan

Students: Di Qian

Industrial Liaisons: James P. Libous, IBM, Endicott, New York
Daniel P. O' Connor, IBM, E. Fishkill, New York

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Anticipated Result

Integrated tool for the analysis of power supply noise in packaged ASICs

Task Description

- Integration of the tools and algorithms developed under Task ID: 735.001 and 1063.001 into a single design environment
- Development of a Graphical User Interface
- Development and incorporation of statistical modeling and analysis capability. Variation of power supply noise as a function of package tolerances can be estimated using this feature.

Task Deliverables

- Report on the architecture for the GUI will be defined along with the preliminary development of a prototype tool. The tool will be applied to a specific package and will contain interfaces to APD
  Planned: Dec 31, 2002

Task Outcome

- Tool architecture – completed.
- Report on architecture – completed.
- Change in direction
  Mentors have suggested that manual entry is preferable initially
  Interfaces to APD will be developed as part of Year 2
- Switch – Ver 1.0 Release Date – Mar. '03

Task Deliverables

- The prototype tool will be modified by providing interfaces to extraction tools such as Fast Henry and Maxwell. The tool will be made generic to support different kinds of ASICs
  Planned: Dec 31, 2003

- Report on the features such as hierarchical modeling will be added to the tool. The code will be tested and made available to the SRC companies along with a user manual
  Planned: Dec 31, 2004

Executive Summary
Feedback from Last Review

Importance = 7.9
Satisfaction = 7.7

Strengths:
- Very good start on this program
- Plan to integrate several engines commended
- Sensitivity analysis commended

Opportunities for improvement:
- Need for rapid incorporation of student involvement into program
- Meetings with member company representatives to identify mutual needs

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Executive Summary

Accomplishments

- Completed definition of design environment for Switch
- Integrated Cavity Resonator and Transmission Matrix Method into Switch
- Developed generic statistical modeling and diagnosis methodology for systems
- Released Switch Ver 1.0

Future Direction (past year 3)

- Integration of features from RID 1063.001

Technology Transfer & Industrial Interactions

- Visit to Georgia Tech by mentors James Libous and Dan O' Connor in 2002
- Summer internship for graduate student Di Qian in 2003

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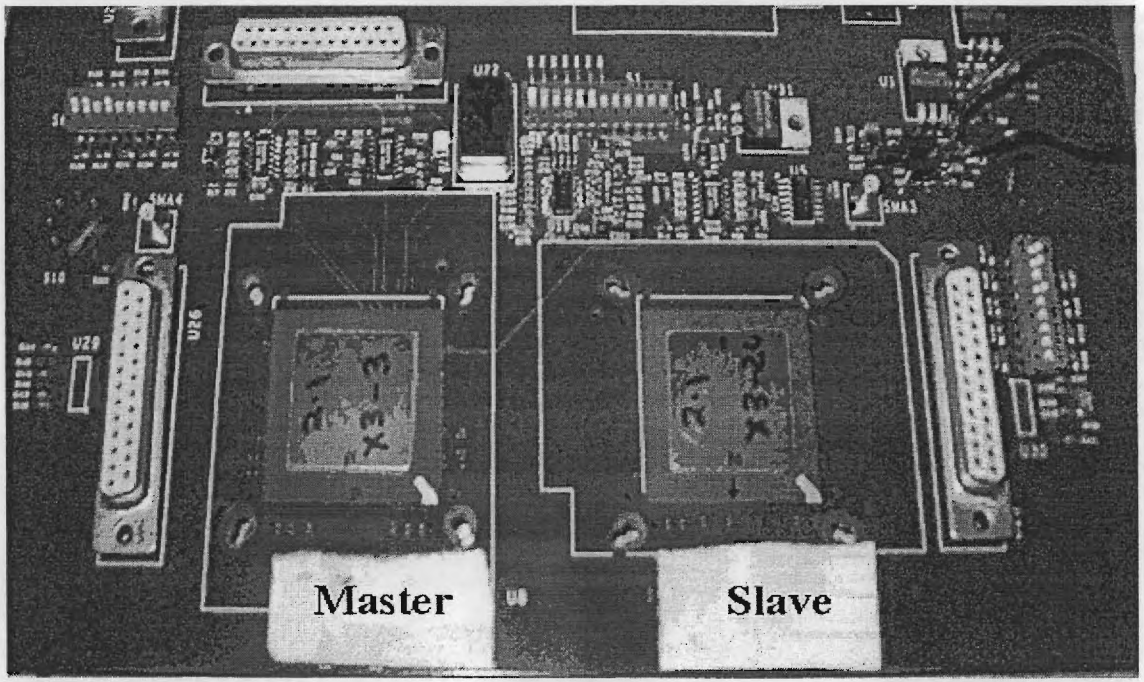
What is Switch ?



Only Statistical System Level tool that combines Chip, Package and Board Power distribution networks for power supply noise analysis

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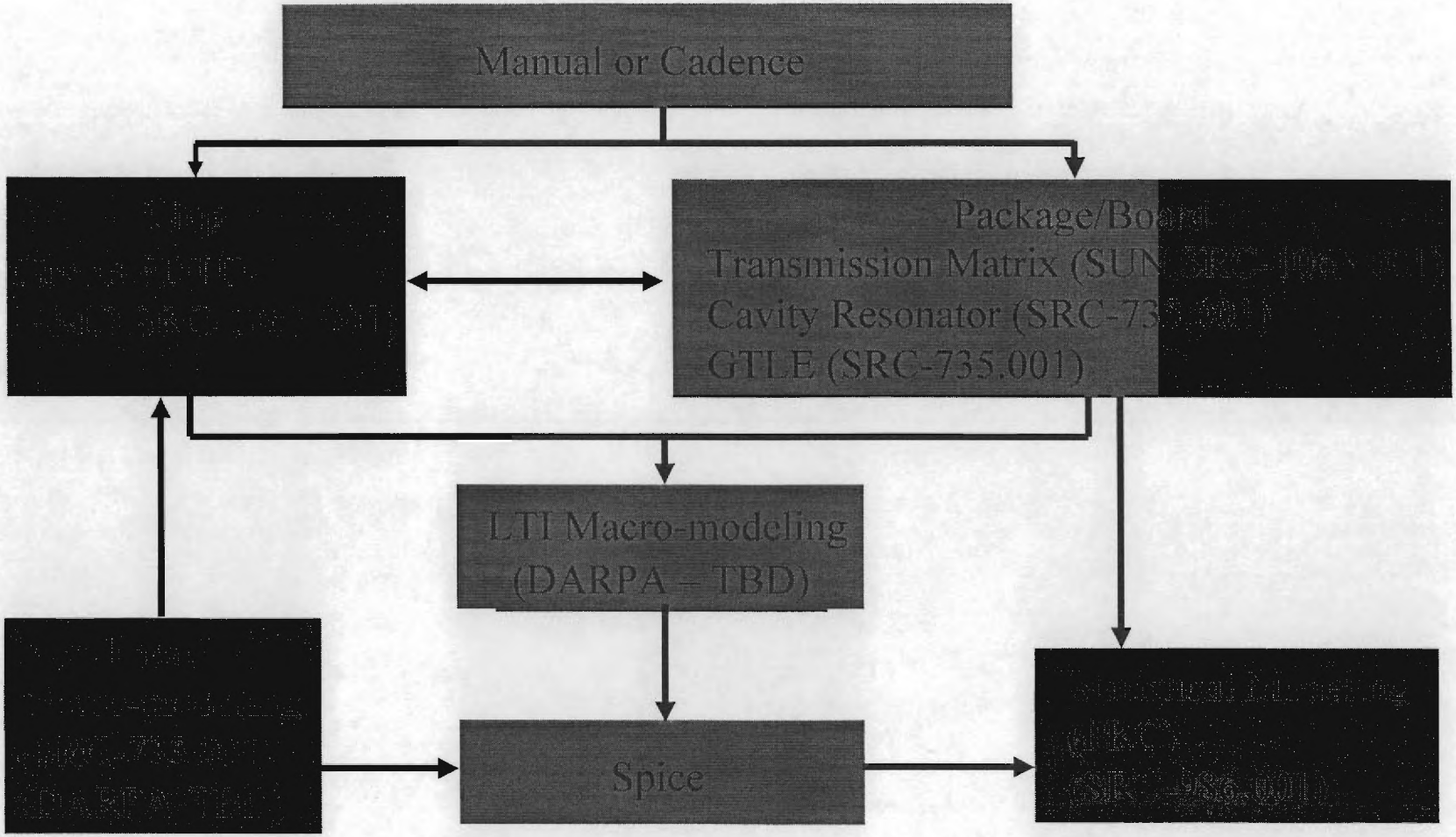
Architecture for SWITCH



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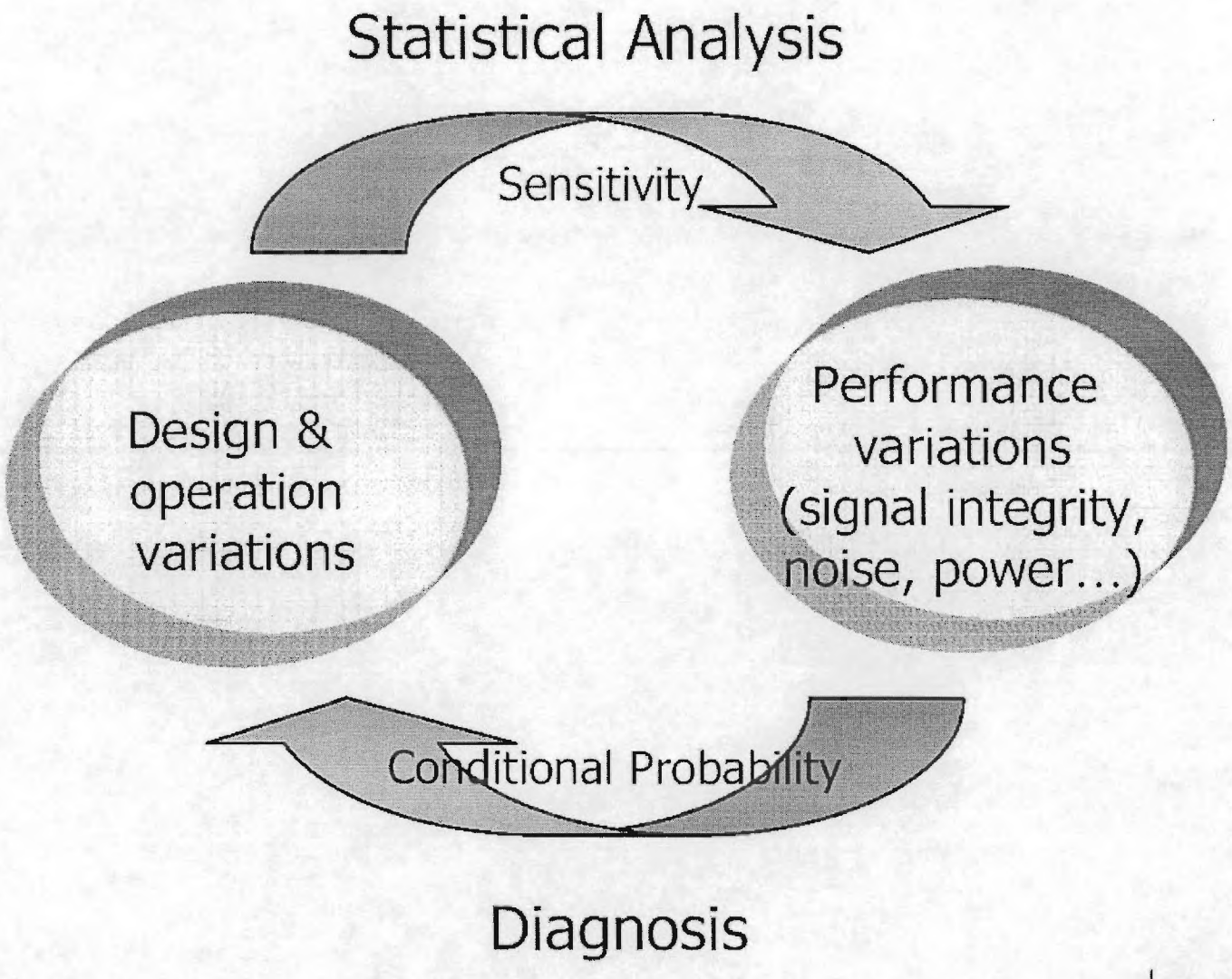
Statistical Analysis and Diagnosis Methodology for High Speed Systems

Student: Erdem Matoglu
Advisor: Madhavan Swaminathan
Partially funded by SRC

Variations in Manufacturing Environment



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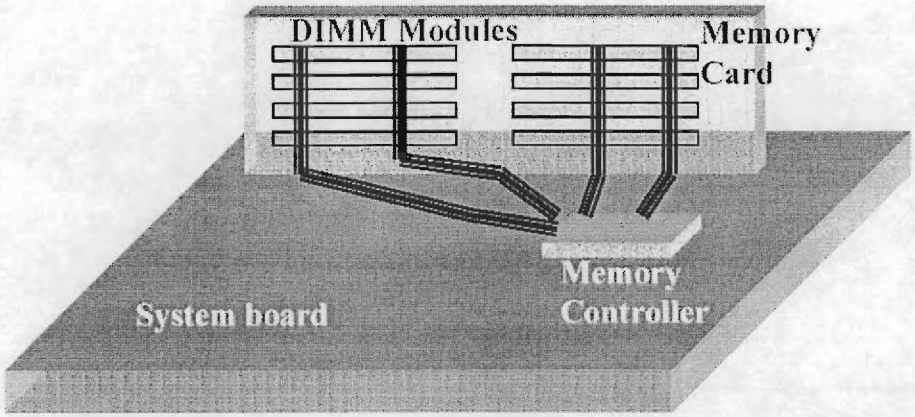
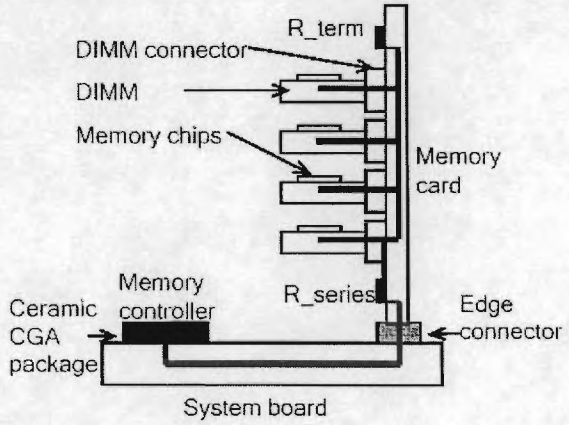
Test System

DDR SDRAM System



- Routed to the edge connector and the card
- Longest memory trace: 14.5 inches
- 16 GBytes capacity
- 184 pin SDRAM DIMM Modules
- 128 bit wide, 200MHz memory bus (3.2GBytes/s)



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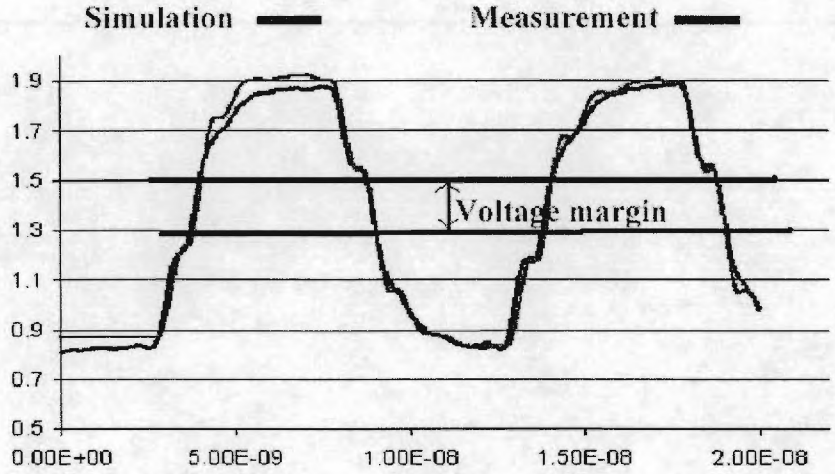
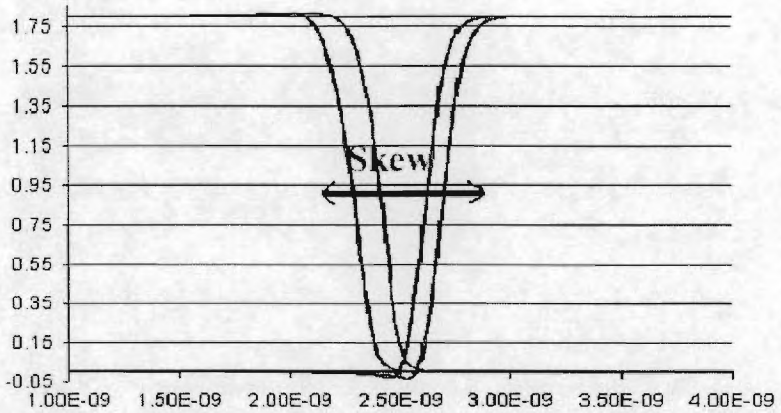
Performance Measures

- Data transmission is relative to strobe (DQS) signal
- Switching occurs when DQS crosses a reference voltage
- During switching, DQS signal must be free of any plateaus or slope reversals
- DQS voltage margin must be ensured at the rising and falling edges
- Data skew must be analyzed to satisfy timing



Strobe (DQS)



Data (DQ)

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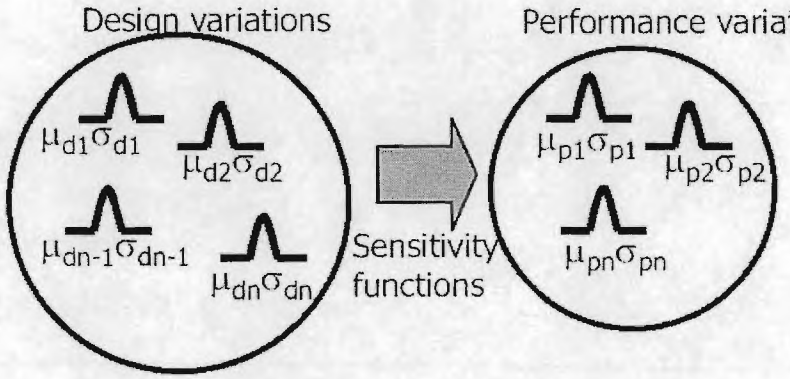
Design Parameters

- Data skew and DQS voltage margin, are related to various design and operation parameters
- The parameters under investigation can be considered as random variables
- Their impact on the operation can be modeled, and statistical distribution of the performance can be computed

Parameter	Mean (μ)	Sigma (σ)
Process parameter (s1)	1	0.33
SDRAM dv/dt (s2)	4.5V/ns	0.167
Supply voltage (V)	2.6V	66.67e-3
Temperature (T)	50 C	8.33
System board dielectric thickness (b1)	9.5 mils	0.5
System board trace width (w1)	3.5 mils	0.33
Memory card dielectric thickness (b2)	10.9 mils	0.6
Memory card trace width (w2)	4 mils	0.33

Statistical Analysis

- **Sensitivity functions vs Monte Carlo**



- **Taguchi array technique minimizes the number of experiments (27 simulations)**

- **Each row represents a different simulation condition where 1's are the mean (μ), 0 and 2 are μ-3σ and μ+3σ respectively**

Taguchi array ($L_{27}(3^8)$) with 8 variables at 3 levels

	Parameters s1 s2 V b1 w1 b2 w2 T	DQ Skew (ps)	DQS Margin (mV)
1	0 0 0 0 0 0 0 0	293	229
2	0 0 0 0 1 1 1 1	226	256
3	0 0 0 0 2 2 2 2	151	267
4	0 1 1 1 0 0 0 1	362	217
5	0 1 1 1 1 1 1 2	362	274
6	0 1 1 1 2 2 2 0	406	289
7	0 2 2 2 0 0 0 2	416	252
8	0 2 2 2 1 1 1 0	537	293
9	0 2 2 2 2 2 2 1	483	309
10	1 0 1 2 0 1 2 0	457	328
11	1 0 1 2 1 2 0 1	461	133
12	1 0 1 2 2 0 1 2	324	397
13	1 1 2 0 0 1 2 1	512	350
14	1 1 2 0 1 2 0 2	512	141
15	1 1 2 0 2 0 1 0	600	406
16	1 2 0 1 0 1 2 2	207	260
17	1 2 0 1 1 2 0 0	383	81
18	1 2 0 1 2 0 1 1	262	336
19	2 0 2 1 0 2 1 0	726	200
20	2 0 2 1 1 0 2 1	544	498
21	2 0 2 1 2 1 0 2	600	244
22	2 1 0 2 0 2 1 1	408	146
23	2 1 0 2 1 0 2 2	232	402
24	2 1 0 2 2 1 0 0	479	176
25	2 2 1 0 0 2 1 2	465	174
26	2 2 1 0 1 0 2 0	586	431
27	2 2 1 0 2 1 0 1	555	190

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Sensitivity Analysis

Data skew (Sk) and DQS voltage margin (Vm) are represented as;

$$Sk = \beta_{10} + \beta_{11}s_1 + \beta_{12}s_2 + \beta_{13}V + \beta_{14}b_1 + \beta_{15}w_1 + \beta_{16}b_2 + \beta_{17}w_2 + \beta_{18}T + \varepsilon_1$$

$$Vm = \beta_{20} + \beta_{21}s_1 + \beta_{22}s_2 + \beta_{23}V + \beta_{24}b_1 + \beta_{25}w_1 + \beta_{26}b_2 + \beta_{27}w_2 + \beta_{28}T + \varepsilon_2$$

Probability density functions of data skew and DQS voltage margin can be computed with convolution as;

$$f_{Sk}(Sk) = \delta(\beta_{10} - \beta_{10}) * f_1(\beta_{11}s_1) * f_2(\beta_{12}s_2) * f_3(\beta_{13}V) * f_4(\beta_{14}b_1) * f_5(\beta_{15}w_1) * f_6(\beta_{16}b_2) * f_7(\beta_{17}w_2) * f_8(\beta_{18}T) * f_{\varepsilon_1}(\varepsilon_1)$$

$$f_{Vm}(Vm) = \delta(\beta_{20} - \beta_{20}) * f_1(\beta_{21}s_1) * f_2(\beta_{22}s_2) * f_3(\beta_{23}V) * f_4(\beta_{24}b_1) * f_5(\beta_{25}w_1) * f_6(\beta_{26}b_2) * f_7(\beta_{27}w_2) * f_8(\beta_{28}T) * f_{\varepsilon_2}(\varepsilon_2)$$

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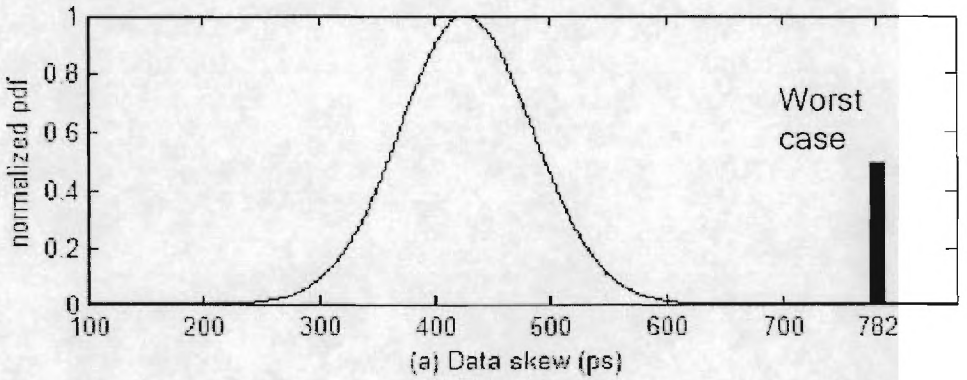
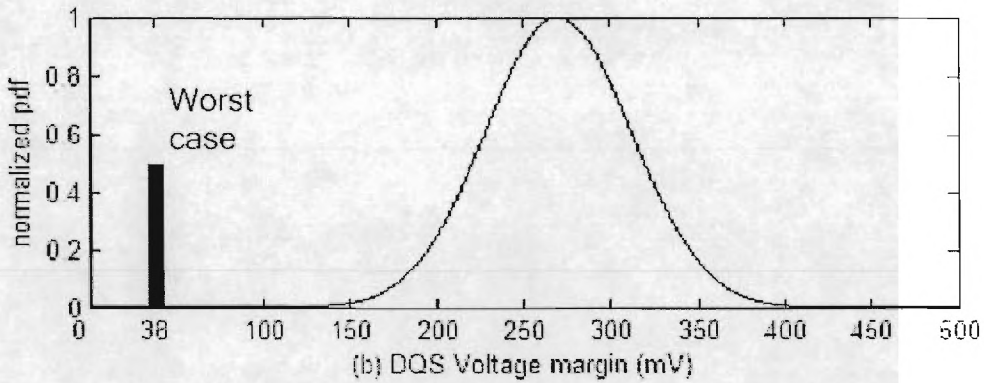
Probability Density Functions

Data skew
(μ_{Sk}=427ps,
σ_{Sk}=60ps)



DQS voltage margin
(μ_{Vm}=270mV,
σ_{Vm}=42mV)



✓ **Statistical distributions can be optimized to assure a larger percentage of the products meet the intended performance**

✓ **Yields more information than the worst case analysis**

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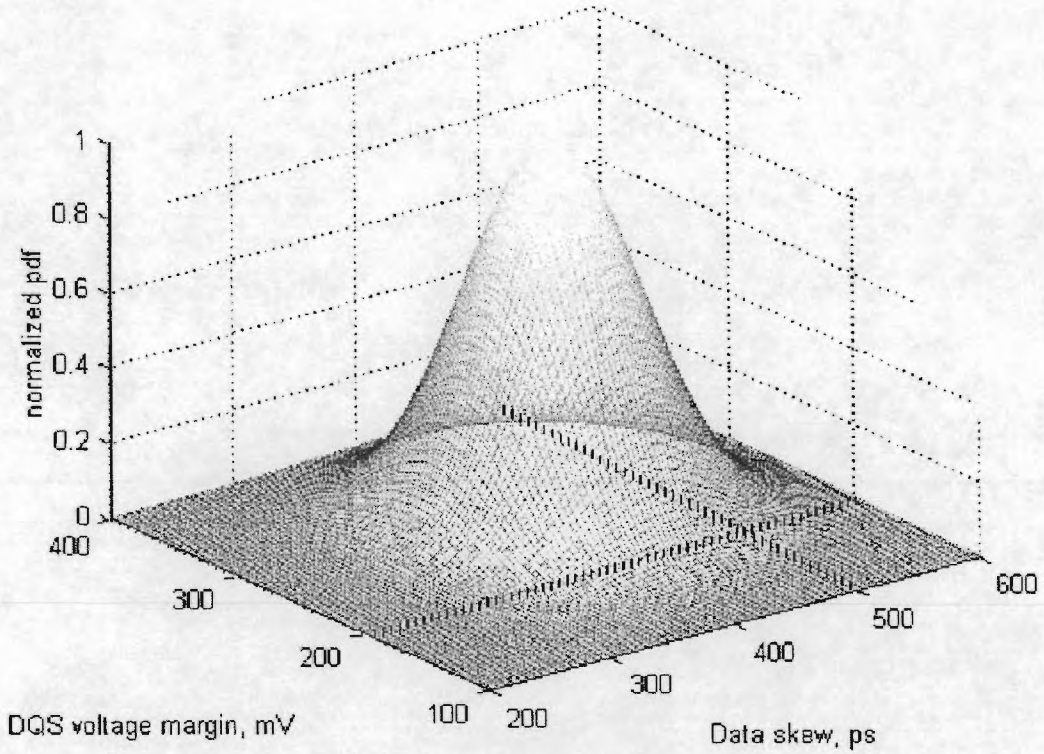
Probability Density Functions



Joint probability density function of data skew and DQS voltage margin.

Ideal for predicting the yield of a product

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Diagnosis Method

- **DQS voltage margin and data skew are related to design parameters**

$$Sk = \beta_{10} + \beta_{11}s_1 + \beta_{12}s_2 + \beta_{13}V + \beta_{14}b_1 + \beta_{15}w_1 + \beta_{16}b_2 + \beta_{17}w_2 + \beta_{18}T + \varepsilon_1$$

$$Vm = \beta_{20} + \beta_{21}s_1 + \beta_{22}s_2 + \beta_{23}V + \beta_{24}b_1 + \beta_{25}w_1 + \beta_{26}b_2 + \beta_{27}w_2 + \beta_{28}T + \varepsilon_2$$

- **For a measured pair of DQS voltage margin and data skew, the most probable design parameter set can be computed**

$$Y = \beta X + \varepsilon \qquad Y = \begin{bmatrix} Sk - \beta_{10} \\ Vm - \beta_{20} \end{bmatrix} \qquad \beta = \begin{bmatrix} \beta_{11} \cdots & \beta_{18} \\ \beta_{21} \cdots & \beta_{28} \end{bmatrix} \qquad \varepsilon = \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \end{bmatrix}$$

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Diagnosis Method

Example:

- A random set of parameters have been modeled and simulated

- Resulting data jitter and strobe voltage margin (559ps, 163mV) has been applied to diagnosis equation

- Parameters s1, V, T, b2, and w2 are estimated close to the actual values

- Parameters s2, b1, and w1 could not be estimated due to their insignificant effects on the performance measures

- The estimated parameter vector can be verified or tuned by measuring some of the easily accessible parameters

Param.	Estimated vector	Input vector
s1	$\mu + 0.90\sigma$	$\mu + 1.18\sigma$
s2	$\mu + 0.35\sigma$	$\mu + 0.85\sigma$
V	$\mu + 0.90\sigma$	$\mu + 1.29\sigma$
T	$\mu + 0.89\sigma$	$\mu + 1.10\sigma$
b1	μ	$\mu - 1.59\sigma$
w1	$\mu - 0.50\sigma$	$\mu - 1.44\sigma$
b2	$\mu + 1.82\sigma$	$\mu + 2.08\sigma$
w2	$\mu - 1.93\sigma$	$\mu - 2.25\sigma$

Future Work

- Release new version of Switch every 6 months

- Release Switch Ver 2.0
  - Release Date: Sept '03
  - TMM extended to multiple planes
  - Fine tuning of Cavity Resonator Method
  - Interface to APD

- Non-linear sensitivity analysis capability for Statistical Modeling

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Demo – Switch Ver 1.0

Student: Di Qian
Advisor: Madhavan Swaminathan

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SWITCH

Switching Noise Analysis Tool for ASICs

Di Qian

MS Student

Advisor: Madhavan Swaminathan

School of Electrical and Computer Engineering

Georgia Institute of Technology

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Overview

Objective:

Development of software tools that combine the various power distribution analysis algorithms for the modeling and simulation of power supply noises.

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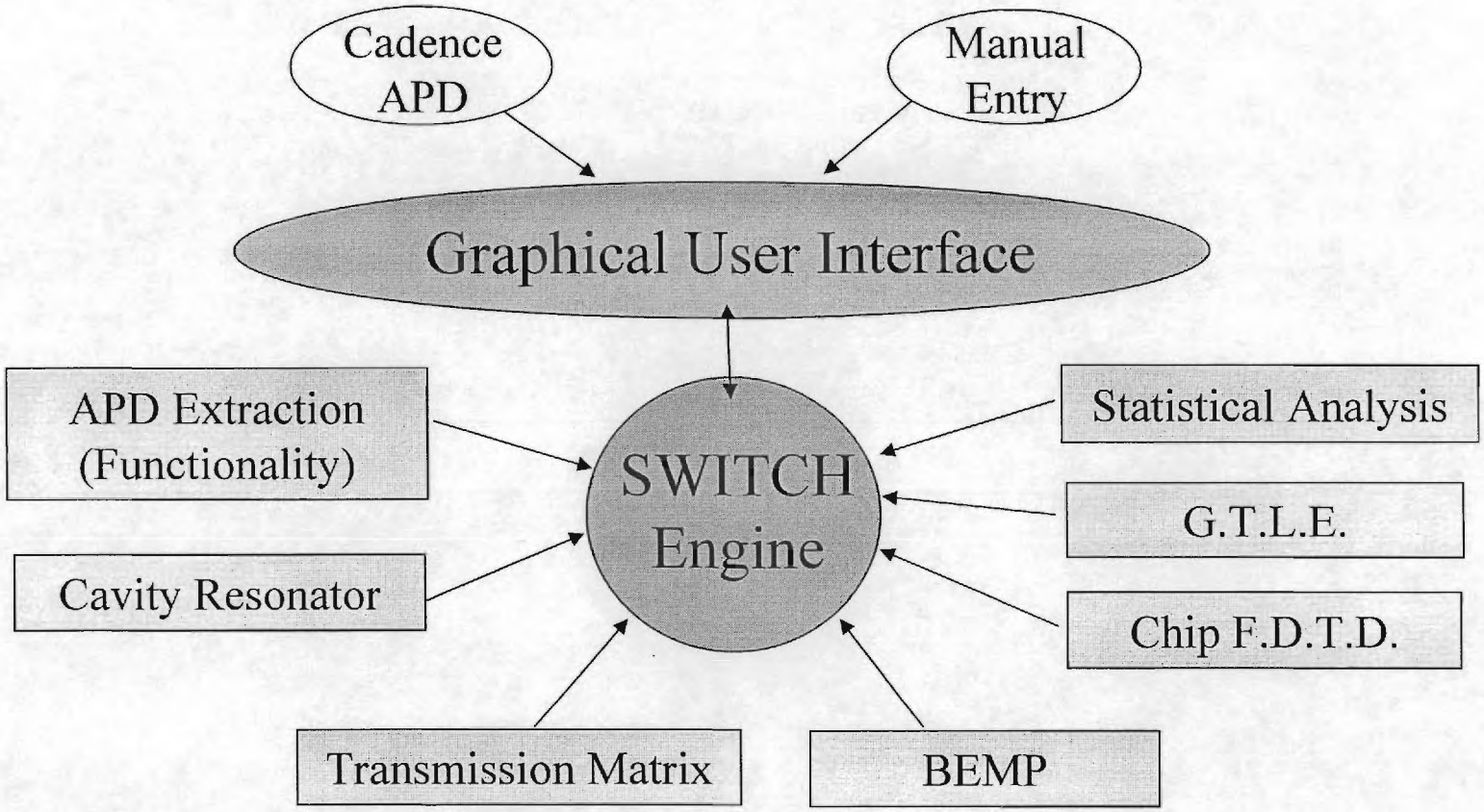
Modeling Techniques & Functionalities



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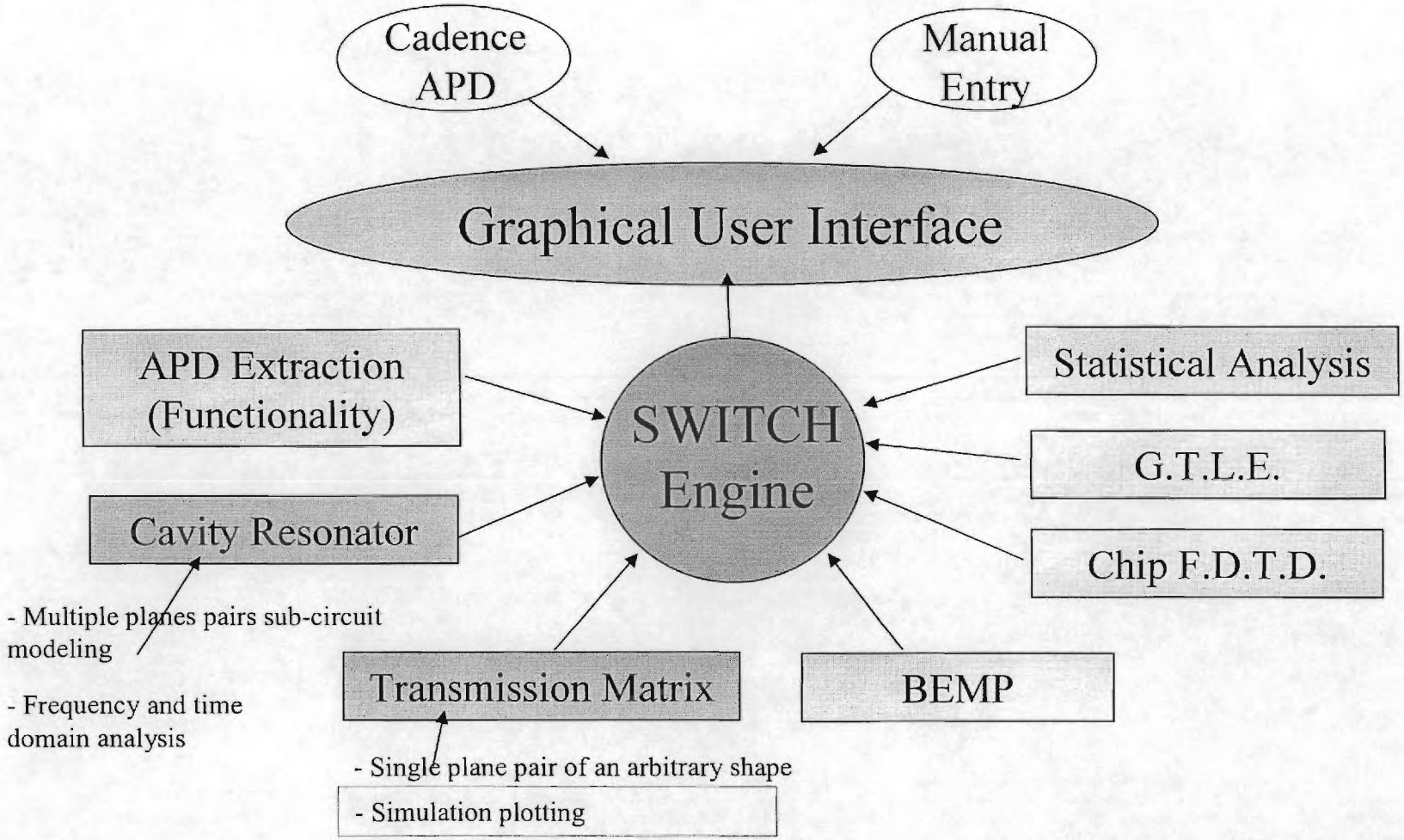
SWITCH Version 1.0



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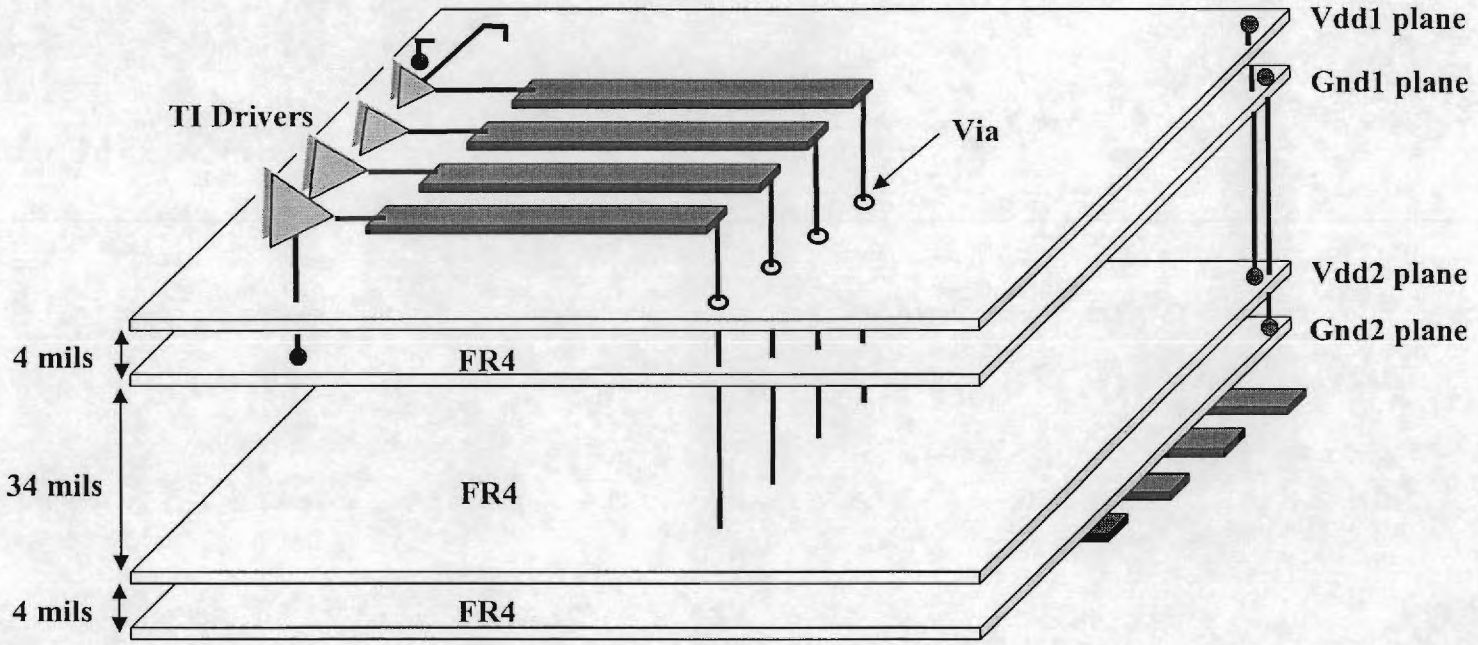
Demo I: Cavity Resonator Method

Example: Plane bound effect caused by via transition.

(Reference: Sungjun Chun, "Methodologies for Modeling Simultaneous Switching Noise in Multi-Layered Packages and Boards", Defense Thesis, pp62-68, April 2002.)



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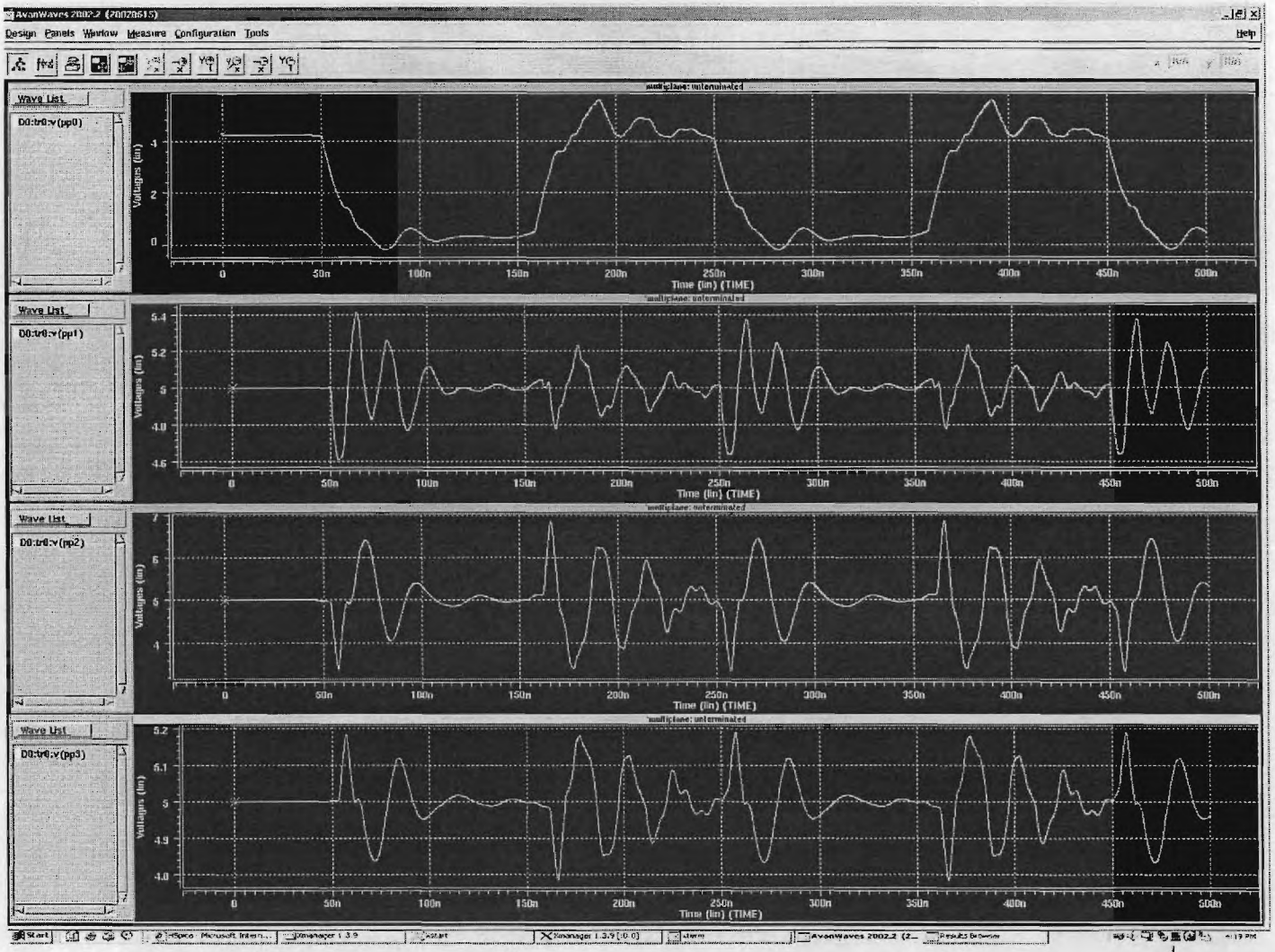
Demo I: Cavity Resonator Method



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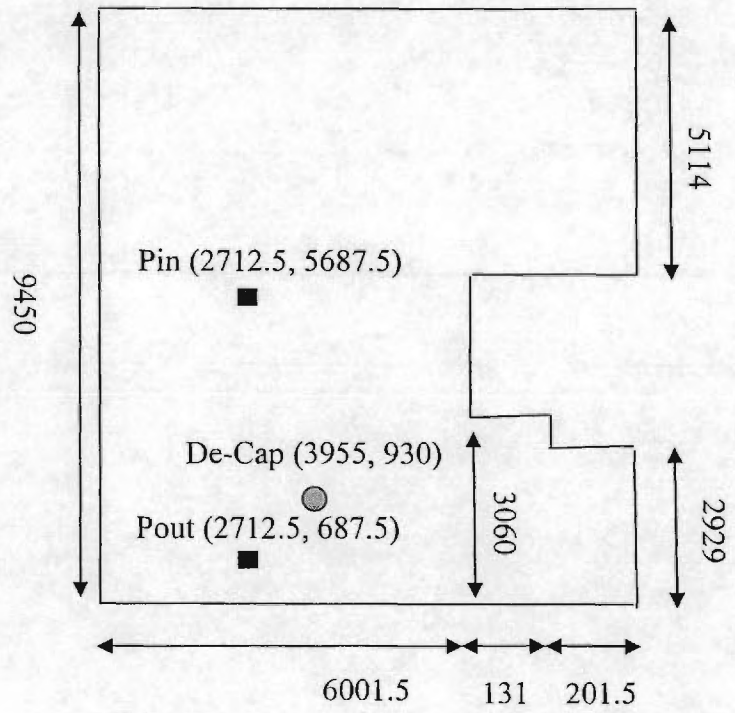
Demo II: Transmission Matrix Method

Example: Single plane pair of arbitrary shape



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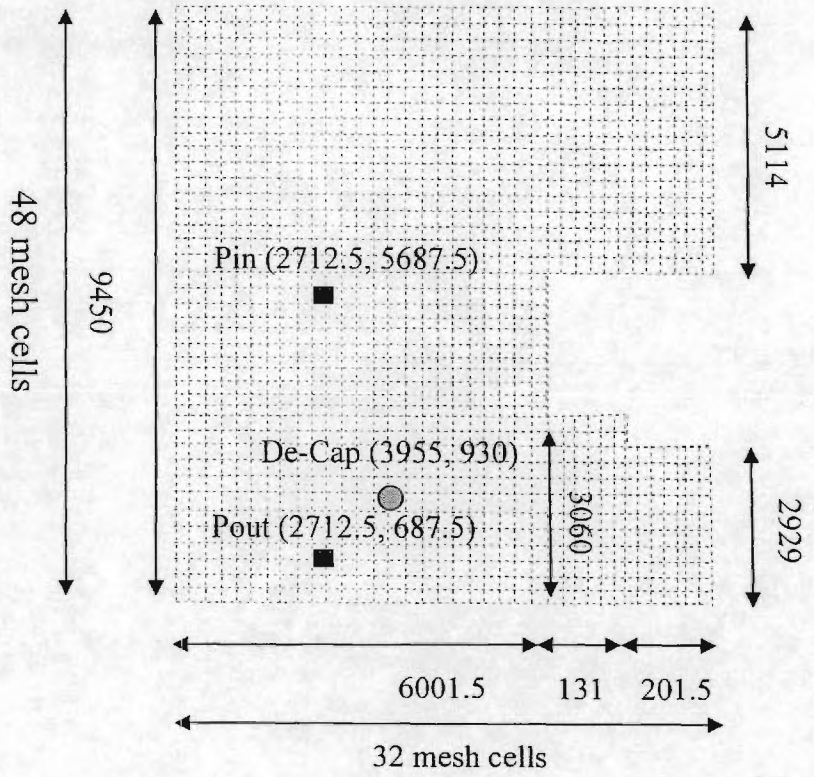
Demo II: Transmission Matrix Method

Example: Single plane pair of arbitrary shape



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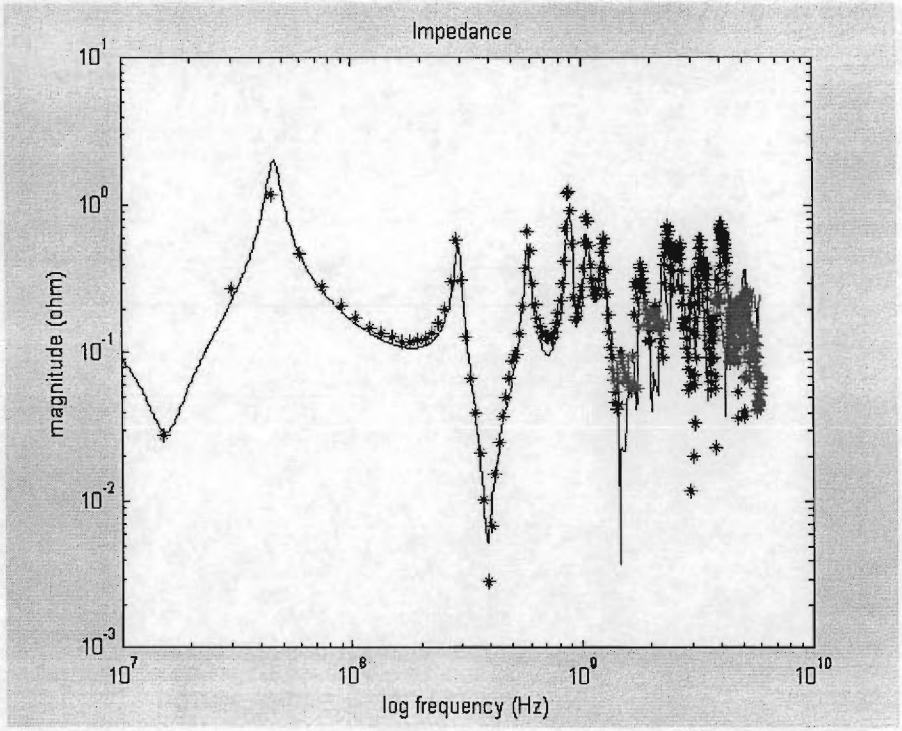
Demo II: Transmission Matrix Method

Plot for the transient impedance Z12:



Modeling Results

Measurement Results

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Future Work Plan

- May, 2003
  - Start Transmission Matrix multi-level simulation and Cavity Resonator fine tuning
  - GUI debugging; more work on graphical scaling; more user friendly component manipulation
- September, 2003
  - Cavity Resonator Method (Multiple power plane simulation) Incorporated
  - Transmission Matrix Method (Multiple power plane simulation) Incorporated
  - APD Extraction Incorporated
- March, 2004
  - Incorporation of two more modeling methods: FDTD, BEMP (Subject to change)

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Power Distribution Networks in Digital and Mixed Signal Systems

Madhavan Swaminathan
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Email: madhavan.swaminathan@ece.gatech.edu

Acknowledgement

James Libous – Project Mentor for RID 735.001, 1063.001, 986.001

SRC 2002 Mehboob Khan Award
for Outstanding Mentorship

Overview

- Why research in power distribution ?
- International Technology Roadmap on Semiconductors
- Integration issues in mixed signal systems
- SRC RID: 735.001
  - Macro-modeling of Non-linear drivers
- Summary for Task RID: 735.001
- Modeling and Co-Simulation of Power Distribution Networks (RID: 1063.001)
  - Chip-Package Interaction
  - Switch
  - Student Presentation – Jinwoo Choi
  - Student Presentation – Jifeng Mao
- Summary for Task RID: 1063.001

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Importance of Power Supply Noise In High Speed Systems

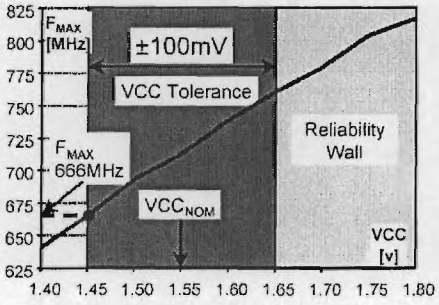

Figure 1: FMAX vs. VCC (TOL = 100mV)

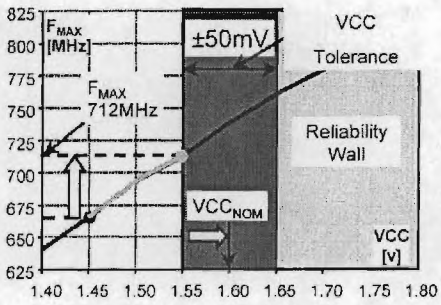

Figure 2: FMAX vs. VCC (TOL = 80mV)

- Reduction in Power Supply Tolerance increases operating frequency
- This effect is pronounced for sub-micron CMOS with low voltage levels and high operating frequencies (ITRS)
- Effect of package and board on power supply noise can be large
- Chip – Package Co-design techniques are therefore required to limit noise in future systems

Ref: A. Waizman and C. Y. Chung, "Package Capacitors Impact on Microprocessor Maximum Operating Frequency", ECTC, Orlando, Florida, May 2001

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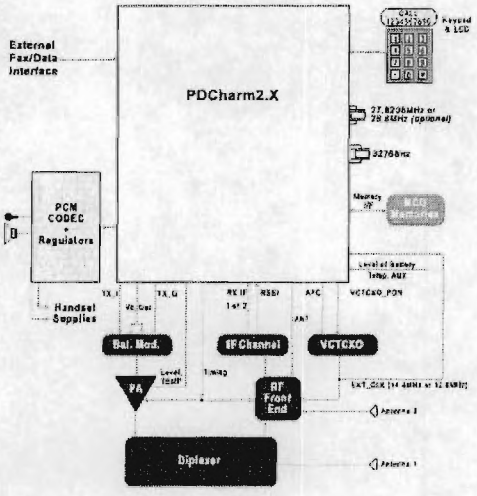
2001 ITRS – High Performance

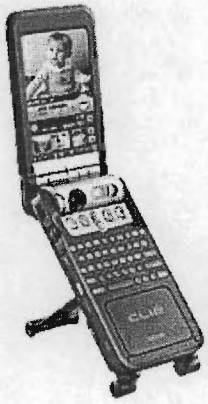
Year	Feature (nm)	Power (W)	Vdd (V)	Current (A)	Frequency (MHz)	Power Imp. (mOhm)
2001	150	130	1.1	118	1684	**0.93**
2003	107	150	1.0	150	3088	**0.67**
2005	80	170	0.9	189	5173	**0.48**
2007	65	190	0.7	271	6739	**0.26**
2010	45	218	0.6	363	11,511	**0.17**
2013	32	251	0.5	502	19,348	**0.1**
2016	22	288	0.4	720	28,751	**0.06**

Georgia Tech

Integrated Mixed Signal Systems



Radio Free Intel (SOC)

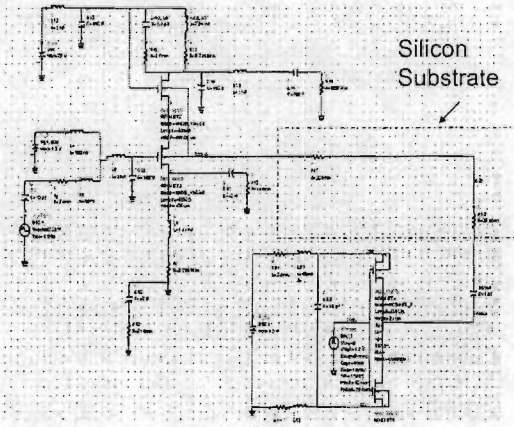


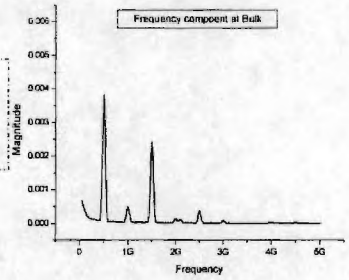
Sony Clie (SOP)

Georgia Tech

Inverter – LNA Substrate Coupling

2.1GHz LNA





Bulk noise

500MHz Inverter

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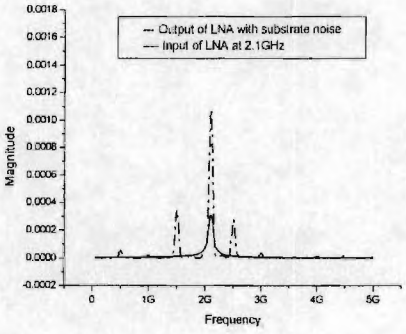
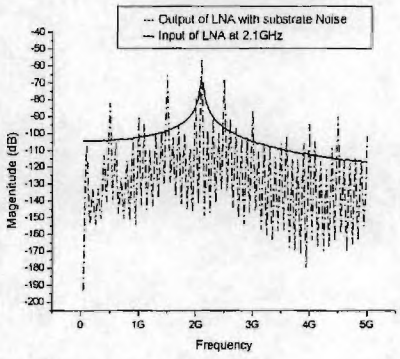
Multi-tone Signals at LNA Output

I/O Magnitude in linear scale



I/O Magnitude in log scale



High degree of isolation required between digital and RF circuits
Major source of coupling is through power distribution

Georgia Institute of Technology

Design of the Power Delivery System for Next Generation Gigahertz Packages

Georgia Tech

Task ID: 735.001

Technical Thrust: Packaging and Interconnect Systems

Task Leader: Madhavan Swaminathan

Students: Jifeng Mao (Graduation Date: Fall 2004)
Jinwoo Choi (Graduation Date: Fall 2004)
Nanju Na (Graduation Date: May 2001; Employer: IBM)

Industrial Liaisons: James P. Libous, IBM, Endicott, New York
Daniel P. O' Connor, IBM, E. Fishkill, New York
Shyamala Chickmenahalli, Intel, Arizona

Georgia Tech

Anticipated Result

Methods for the computation of simultaneous switching noise that enables the pre-layout analysis and post layout verification of packages and boards

This will enable:

- A better understanding of power supply noise in high speed systems
- Analysis of the package/board power distribution network operating at gigahertz frequencies
- Package grading in an ASIC foundry

Georgia Tech

Task Description

- Develop efficient methods for computing core and I/O noise in high speed systems
- Apply the method for computing noise in systems containing chips, packages and boards
- Validate through measurements on active test vehicles supplied by SRC and non-SRC member companies
- Develop a path towards integration for supporting the design of ASICs (Through Research Customization RID – 986.001)

Georgia Tech

Task Deliverables

- Algorithms for simulating I/O noise in multi-layered packages for uncoupled transmission lines in the presence of bouncing planes and decoupling capacitors
  Completion Date: Oct 1, 2000

- Inclusion of inductance and methods to reduce simulation time. Correlation with Test Vehicle Measurements
  Completion Date: Oct 1, 2001

- Algorithms for simulating I/O noise in multi-layered packages for coupled transmission lines in the presence of bouncing planes and decoupling capacitors. Inclusion of non-linear drivers.
  Completion Date: Jan 31, 2003

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Executive Summary
Feedback from Last Review

Importance = 8.2
Satisfaction = 8.3

Strengths:
- Excellent system level approach to modeling of realistic industry problems
- Approach is very pragmatic
- Good experimental validation of analytical results
- High level view of noise vs speed was very appropriate information
- Good mentor interaction and response to mentor needs
- Excellent student presentation

Opportunities for improvement:
- Presentation materials have improved considerably, but still need work
- Can you come up with a way to deconvolve the requirements for different system components

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Executive Summary For Past Contract Year

Accomplishments

- Model to hardware correlation for IBM's HyperBGA Test Vehicle and Rambus Test Vehicle
- Macro-modeling of non-linear drivers

Future Direction (past year 3)

- Modeling of on-chip power distribution network
- Co-simulation of on-chip and package power distribution networks
- Noise interference for mixed signal circuits (Digital and RF)
- Near field coupling

Technology Transfer & Industrial Interactions

- Summer internship for Jifeng Mao
- Measurements by Madhavan Swaminathan at Rambus
- Biweekly conference calls with IBM
- Nanju Na hired by IBM (after a brief stint at Agilent)

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Executive Summary Publications

- Annual Report: 1
- Annual Review Presentations: 2
- Deliverable Reports: 3
- Technical Reports: 1
- Conference Presentations: 4
- Journal papers: 4 (including 1 submitted)
- Invited Seminar: 1
- Thesis: 1

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Macro-modeling of Non-Linear Drivers

Student: Bhyrav Mutnury
Advisor: Madhavan Swaminathan

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Objective

- Develop methods for the macro-modeling of non-linear drivers
- Easy extension to multi-port drivers
- Fast simulation time compared to transistor level models
- Good accuracy compared to transistor level models
- Compatible with Spice and other circuit simulators
- Load independence
- Input independence

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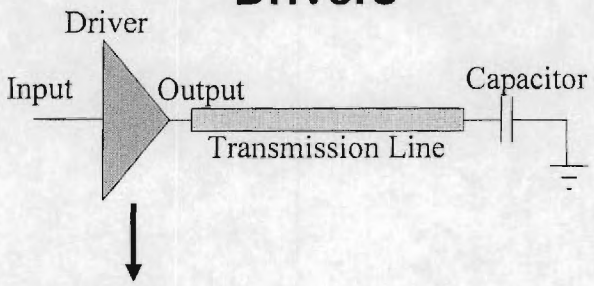
Macro-modeling of Non-linear Digital Drivers



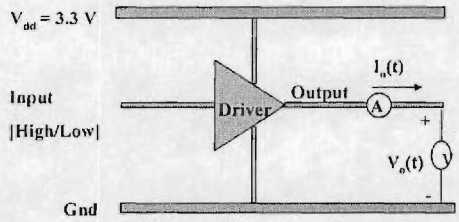
Weakly Non-linear Circuits
Linear models

Georgia Tech – Prof. M. Swaminathan

Highly Non-linear Circuits
RBF models

Univ. of Torino – Prof. F. Canavero

Macro-modeling of Non-Linear Digital I/O Buffers (Linear)



$$I_o(t) = w_1(t)\, F_1(V_o) + w_2(t) F_2(V_o)$$

$$F_1(Vo) = A.Vo + B$$

$$F_2(Vo) = C.Vo + D$$

Calculation of Weighting Functions

The driver output is terminated with two different loads (Example: 50 ohms and 50 ohms + 3.3 Volts) .

The Weighting functions w_1 and w_2 are evaluated as:

$$\begin{bmatrix} w1 \\ w_2 \end{bmatrix} = \begin{bmatrix} F_{1a} & F_{2a} \\ F_{1b} & F_{2b} \end{bmatrix}^{-1} \begin{bmatrix} I_a \\ I_b \end{bmatrix}$$

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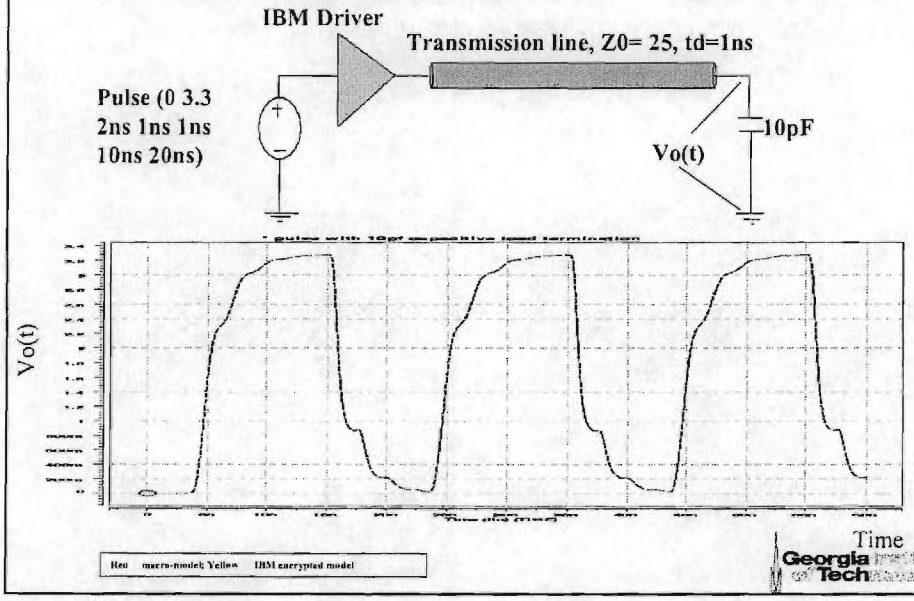
Transistor Level Model and Macro-model – Comparison (Active Line)



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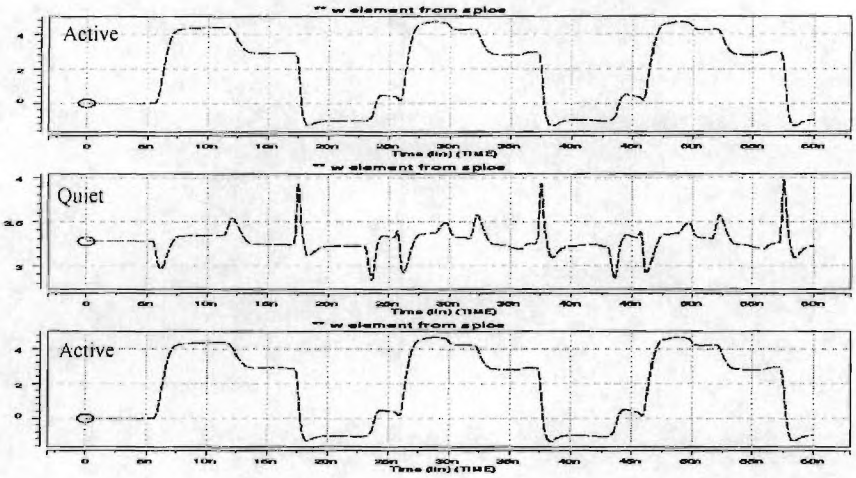
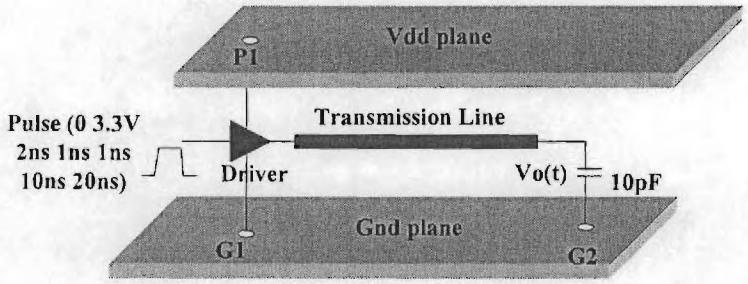
Transistor Level Model and Macro-model Comparison (Quiet Line – Cross Talk)



Macro-modeling for Multi-port Digital I/O Circuits

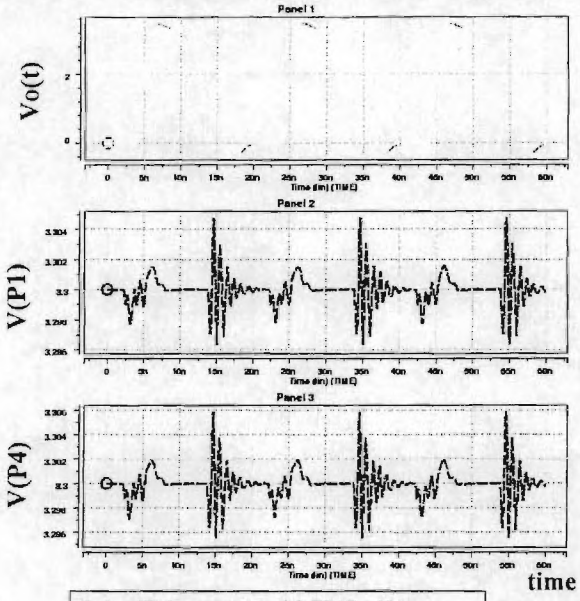
For a ***n-port*** network functions F_1 and F_2 become

$F_1(port1, port2, ..., portn)$ and $F_2(port1, port2, ..., portn)$



$$I_o(t) = w_1(t).\ F_1(V_o, V_{dd}) + w_2(t).F_2(V_o, V_{dd})$$

Macro-modeling for Multi-port Digital I/O Circuits



Red IBM encrypted model: TIME = 122ns

Yellow macro-model: TIME = 6ns

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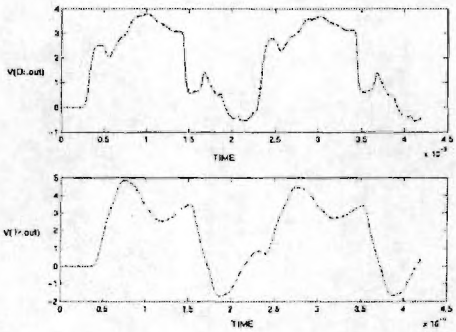
Macro-modeling of Non-Linear Digital I/O Buffers (RBF)

$$I_o(t) = w_1(t)\, F_1(V_o) + w_2(t) F_2(V_o)$$

Functions F_1 and F_2 are replaced with RBF to capture the relationship between present output, present input, previous outputs and previous inputs



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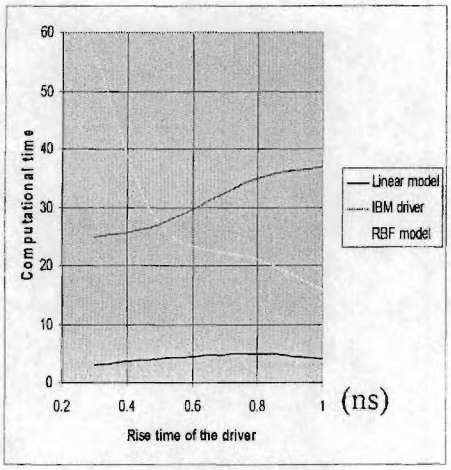
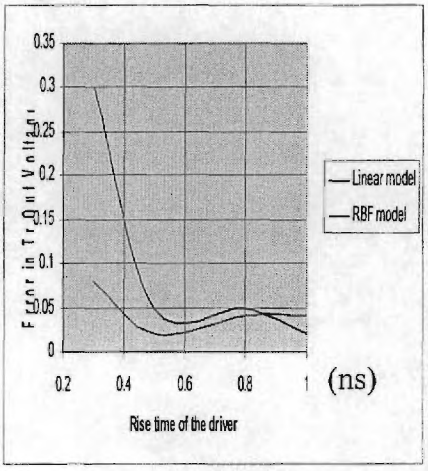
Comparison between Linear and RBF Models



CPU Time



Accuracy

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Summary
Modeling of Non-linear Digital Drivers

- Linear Model is 12 to 40 times faster
- RBF model is 4 times faster
- Both models are load insensitive
- Linear model is made input dependent using post processing
- Linear model can be easily extended to multi-ports
- RBF models are a good choice for highly non-linear circuits

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Significant Accomplishments for

Task ID: 735.001

- Development of the Cavity Resonator Method for analyzing power/ground planes
- Inclusion of Magnetic Field Penetration into Cavity Resonator Method
- SSN Measurements on HyperBGA Test Vehicle from IBM
- Development of methodology for SSN Measurements
- Model to hardware correlation
- Development of Generalized Transmission Line Equation Method
- Effect of Chip, Package and Board on Core Noise quantified
- Development of methods for macro-modeling non-linear drivers
- Development of software and algorithms for modeling and simulating power power supply noise developed
- Software to be integrated into SWITCH under SRC Research Customization RID: 986.001

Georgia Institute of Technology

Modeling and Co-Simulation of Power Distribution Networks in Digital and Mixed Signal Systems

Georgia Institute of Technology

Task ID:1063.001

Start Date: Feb 1, 2003 (1 month into project)

Technical Thrust: Packaging and Interconnect Systems

Task Leader: Madhavan Swaminathan

Students: Jifeng Mao (Graduation Date: Fall 2004)
Jinwoo Choi (Graduation Date: Fall 2004)

Industrial Liaisons: James P. Libous, IBM, Endicott, New York
Daniel P. O' Connor, IBM, E. Fishkill, New York
Shyamala Chickmenahalli, Intel, Arizona

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Anticipated Result

System level modeling and simulation tools that will enable the following:

- Modeling of on-chip power distribution networks for digital circuits
- Integration of on-chip, package and board power distribution modeling tools for enabling the co-design of chip, package and board
- Modeling of power distribution networks for mixed signal circuits that combine digital and RF circuits
- Quantification of near field coupling effects from power distribution on mixed signal circuits

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Task Description

- Inclusion of substrate losses and leakage currents into FDTD based on-chip power distribution analysis tool
- Extension of Transmission Matrix Method (TMM) for analyzing on-chip power distribution networks
- Development of optimum methods that combine FDTD and TMM for modeling and simulating system power distribution networks
- Quantification of power supply noise and electro-migration effects in large packaged chips on boards
- Quantification of noise coupling between digital and RF circuits
- Quantification of near field coupling mechanisms for mixed signal circuits
- Develop a path towards integration for analyzing systems (Through Research Customization RID – 986.001)

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Task Deliverables

- Finite Difference Time Domain (FDTD) Method for analyzing on-chip power distribution networks with substrate losses
  Preliminary results for the use of Transmission Matrix Method for analyzing on-chip power distribution
  Comparison of the two methods
  Completion Date: Dec 31, 2003

- Development of hybrid method that combines FDTD and TMM
  Co-simulation of chip and package power distribution network
  Quantification of EM coupling between digital and RF circuits
  Preliminary integration
  Completion Date: Dec 31, 2004

- Design of Test Vehicles for quantifying near field coupling
  Measurement of Near Field Coupling
  Complete integration
  Completion Date:Dec 31, 2005

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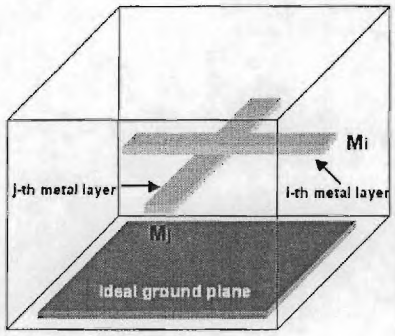
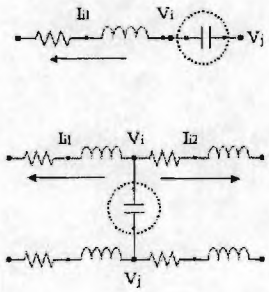
Circuit Finite Difference Time Domain Method For On-chip Power Distribution Networks





- Physical structure replaced with RLGC circuit components
- Simulated using FDTD

Ref: Modeling of Power Supply Noise in Large Chips using the Finite Difference Time Domain Method, Jinseong Choi, PhD Thesis, Georgia Tech, 2002

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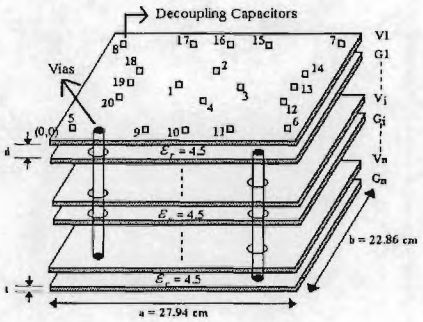
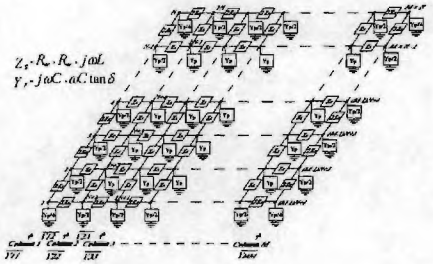
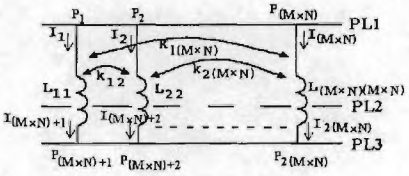
Transmission Matrix Method







Can analyze up to 20 power/ground layers with relative ease

Ref: Modeling of Package and Board Power Distribution Networks using Transmission Matrix and Macro-modeling Methods, Joong-Ho Kim, PhD Thesis, 2002

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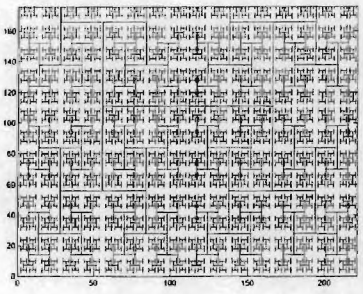
On-Chip Power Distribution Network

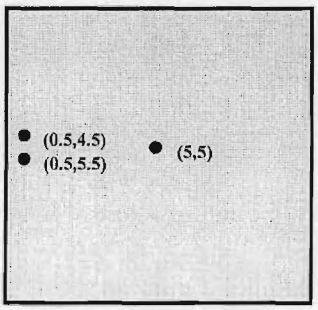


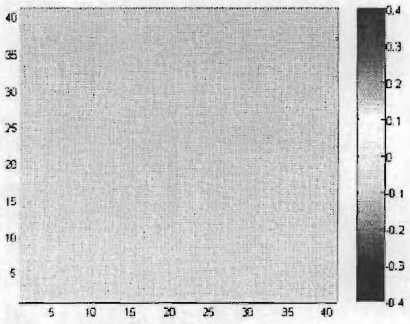
Clock Distribution

Top View of PDN

- Produces a cylindrical/elliptical electromagnetic wave
- Attenuated Wave – Low Q Circuit
- 90% of energy diminished within 1.2mm
- Simulation based on Circuit FDTD with > 2 million nodes

Package Power Planes

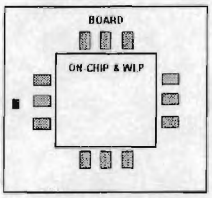




- Produces a cylindrical electromagnetic wave
- Low Attenuation – High Q Circuit
- 99% of energy reaches the edge, reflects and produces standing waves
- Two unloaded power planes

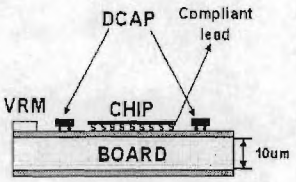
Ref: Modeling of Power Supply Noise in Large Chips using the Finite Difference Time Domain Method, Jinseong Choi, PhD Thesis, 2002

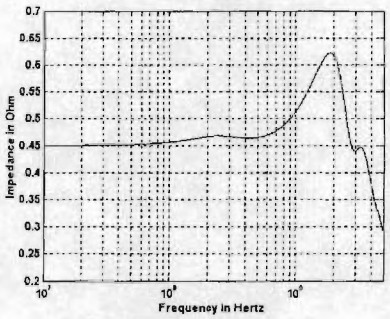
Chip – Package Interaction



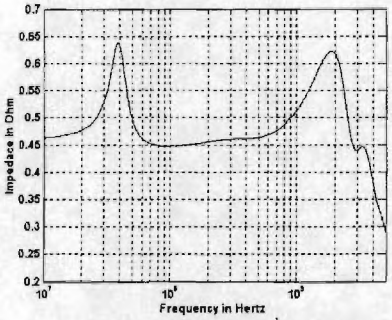
: DCAP (1.5uF each) in total, 4were used.

: Location of VRM





Chip Only



Chip + Board

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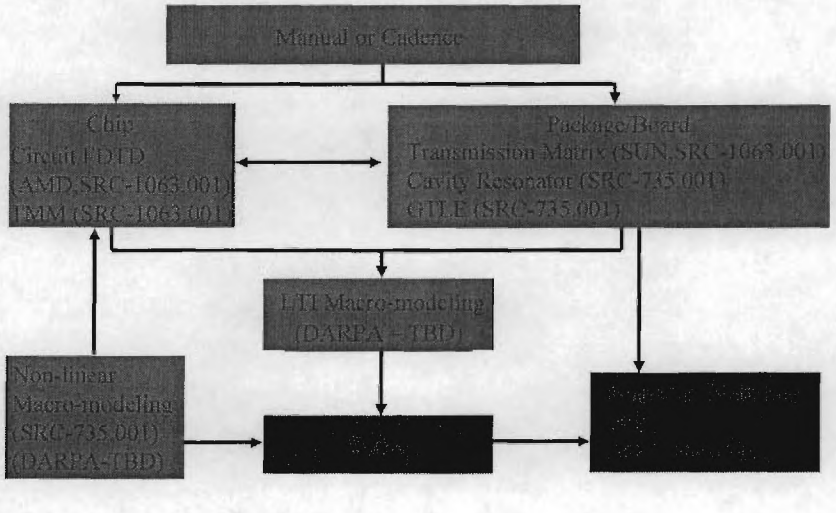
Architecture for SWITCH (RID 986.001)



Georgia Institute of Technology

Modeling and Analysis of Power Distribution Networks for Gigabit Applications

Student : Jinwoo Choi

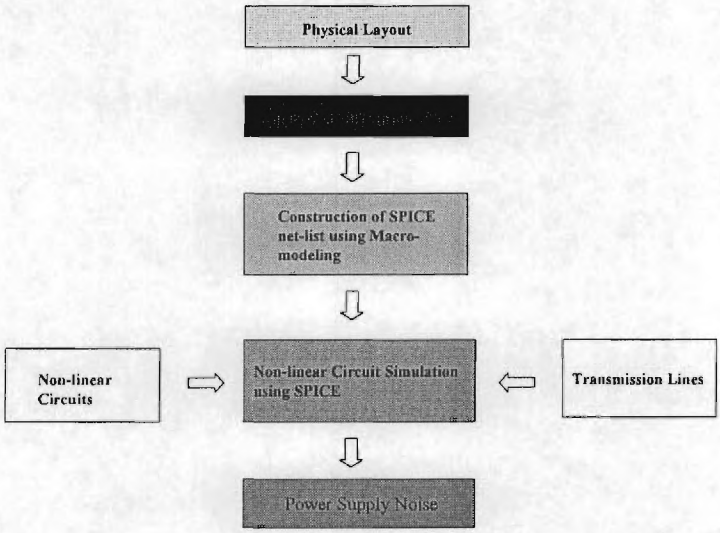
Advisor : Prof. Madhavan Swaminathan

School of Electrical and Computer Engineering
Georgia Institute of Technology

Outline

- Modeling and Simulation Methodology.
- Test Vehicle Description.
- Model to Hardware Correlation.
- Modeling and Analysis of Master-Slave Power Distribution Network.
- Power Supply Noise Simulation.
- Summary.

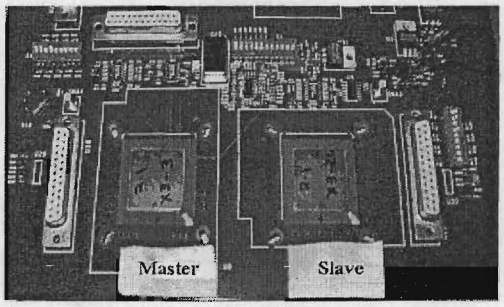
Modeling and Simulation Methodology



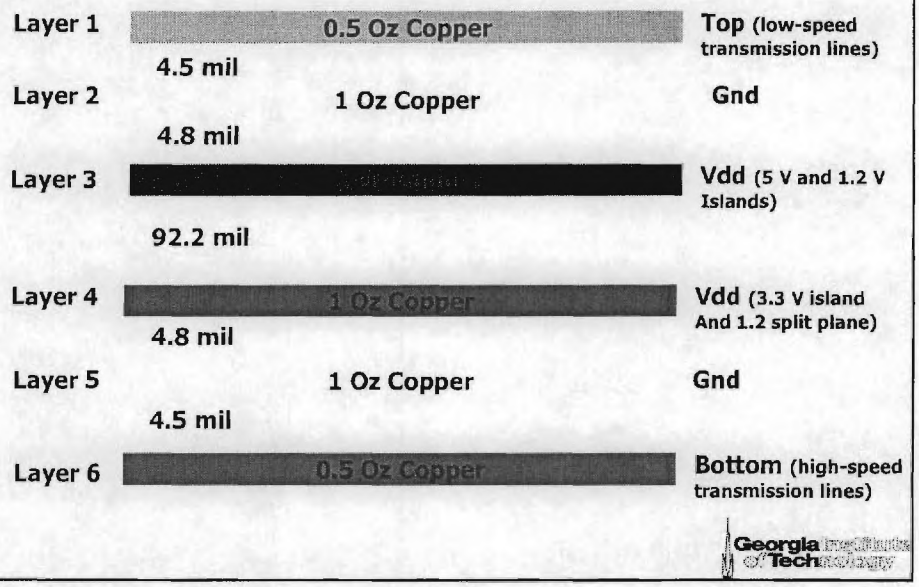
Rambus Test Vehicle

- Designed for chip-to-chip communication at a data rate of 3.2 Gbps.

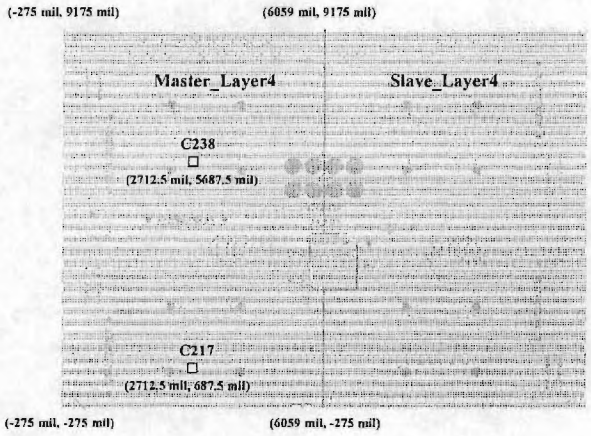
- Consists of transmitter and receiver chips mounted on wirebond PBGA packages on a PCB.



Cross Section of PCB

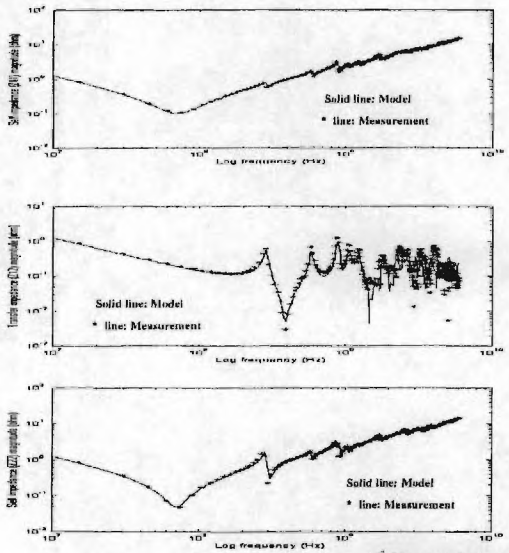


Modeling and Measurement of Layers 4 and 5



Model to Hardware Correlation for Bare Board with Pad Parasitics

- Good model to hardware correlation
- verified TMM modeling method through measurements



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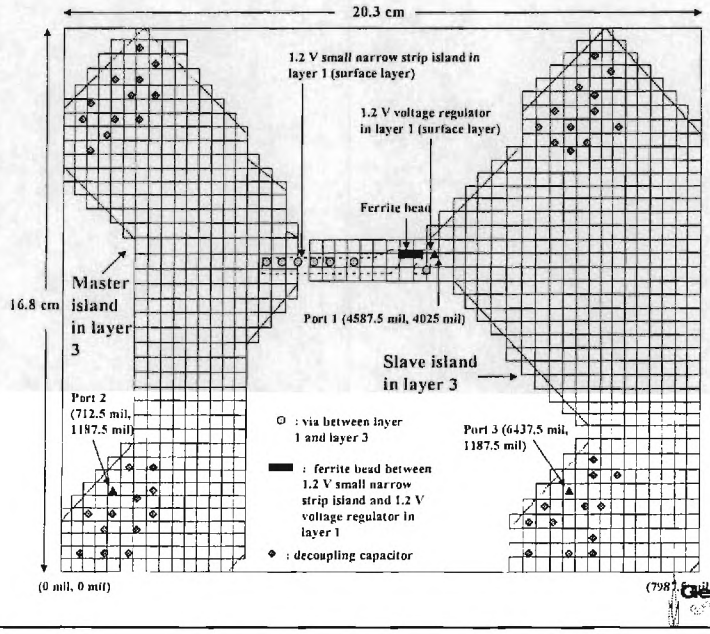
Modeling of Master-Slave Islands



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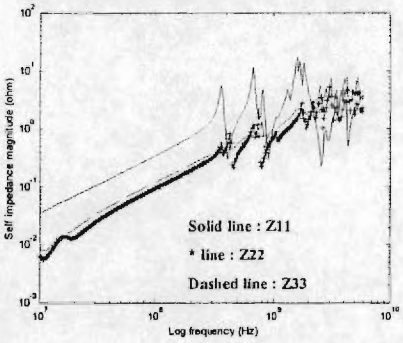
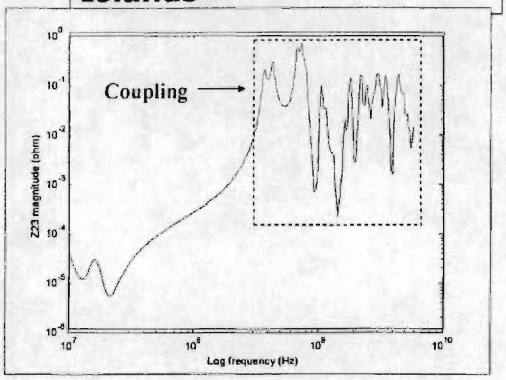
Self Impedances at Ports within Master & Slave Islands



Transfer Impedance between Master & Slave Islands



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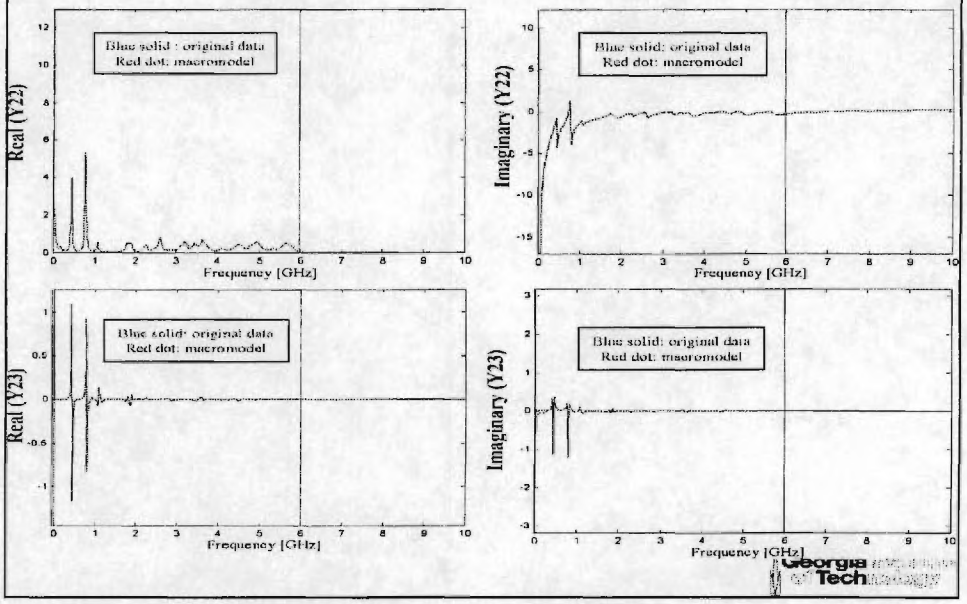
Macro-modeling Results



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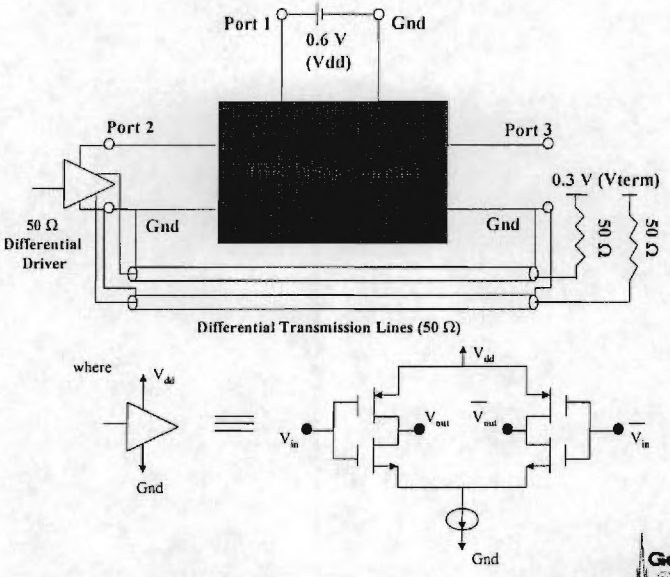
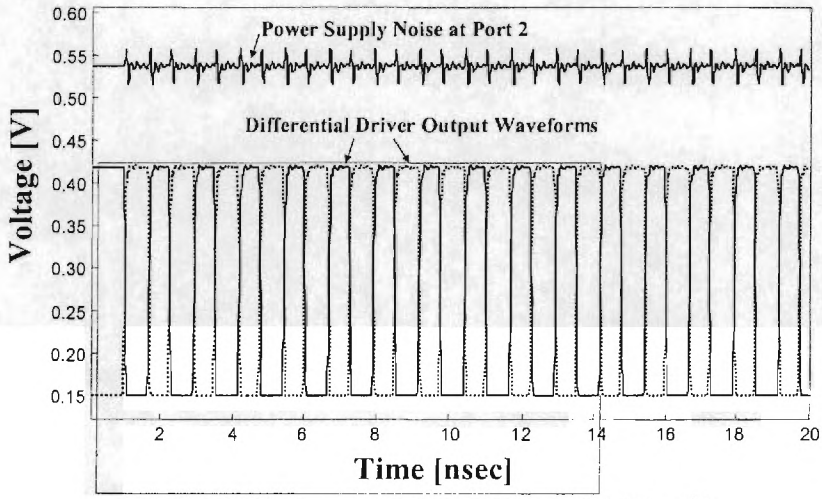
Modeling of Power Supply Noise



Differential Drivers – Yellowstone Channel

Data (Period=1.25ns, tr=0.05ns, tf=0.05ns, Tline = 50 ohms; 1ns)
Data Pattern: 0000111100001111....



Power Supply Noise = 40mV (4 Differential Drivers)

Summary

- Presented a methodology for analyzing a high-speed test vehicle
  - method accurately and efficiently analyzes PDN of test vehicle
- Showed good model to hardware correlation
  - verified TMM modeling method through measurements
- Analyzed behavior of split power planes
- Showed power supply noise
  - got power supply noise using macro-modeling successfully
  - time signature of power supply noise is largely dependent on the driver models
  - good driver models therefore need to be developed to obtain a good estimation on power supply noise

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Effect of Silicon Substrate on Switching Noise in Onchip Power Distribution Network

Jifeng Mao
Advisor: Madhavan Swaminathan
Mentor: James P. Libous & Daniel O'Connor

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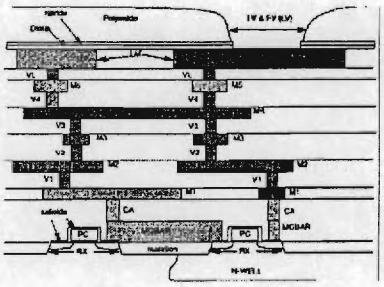
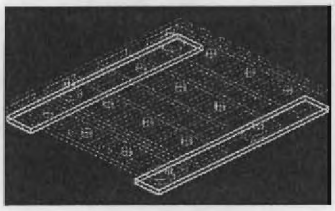
Physical Structure of Onchip Power Distribution(PD)

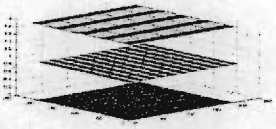


Cross section of ASIC*

* James Libous, IBM ASIC group

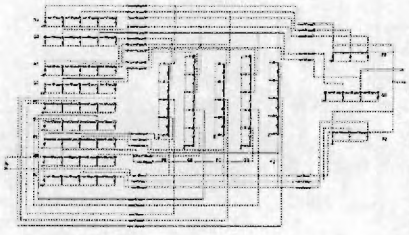


3D view of onchip PD



DC voltage of onchip PD

Modeling & Simulation Approach



Simple circuit representation of onchip power bus

- ◆ HFSS
- ◆ Maxwell 3D/2D
- ◆ Measurement -- NA/TDR

Modeling tools

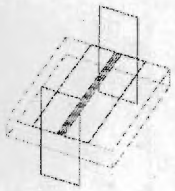
- ➢ **Hspice**
  - •Time consuming
  - • No spatial information
- ➢ **Circuit-based FDTD***
  - •Computational efficient
  - •Easy to get spatial information

Simulation tools

* J.Choi, L. Wan, M.Swaminathan, B. Beker and R. Master " Modeling of a Realistic Power Grid using FDTD", Symposium on EMC, pp.236-243, Aug. 2002

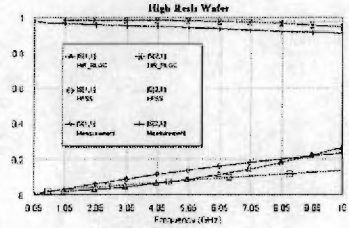
Model to Hardware Correlation of CPW Structures on Silicon

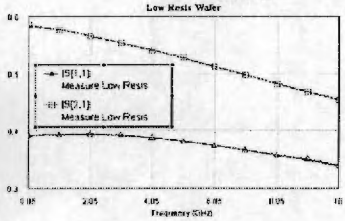
CPW on wafer



HFSS setup**

Cross section of CPW onchip**





Measurement vs. Modeling

**Woopoung. Kim & Suna. Choi, Gatech Epsilon group

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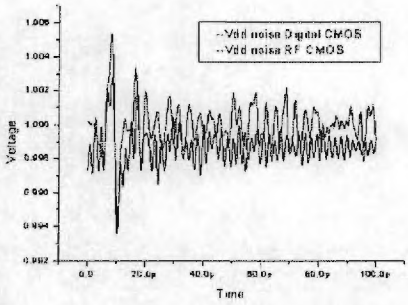
Effect of Substrate Resistivity on SSN

Layer M1	Digital CMOS 1	Digital CMOS 2	RF CMOS	GaAs
Resis(Ωcm)	5	100	1,000	1,000,000
L (pH)	40.626	40.696	40.696	40.696
R (Ω)	0.17326	0.17317	0.17317	0.17317
C (fF)	2.5597	2.1097	2.1016	2.1014
G (s)	2.972e-4	1.4843e-5	1.491e-6	1.4912e-9

Tab.1 RLGC of various substrate



Noise waveform at same Vdd Node

Effect: Lossy substrate helps attenuate switching noise.

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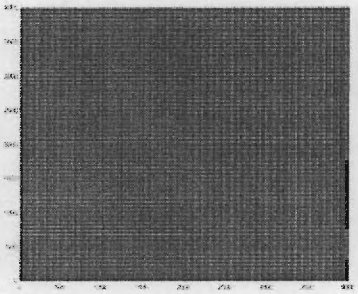
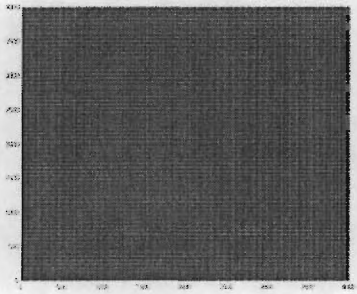
Comparison of Propagation

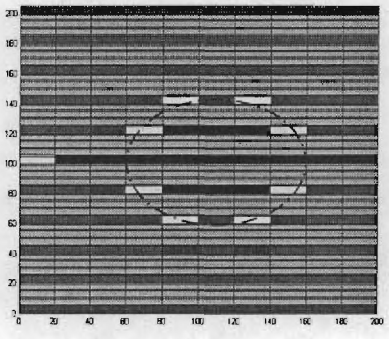


Low Resistivity Substrate

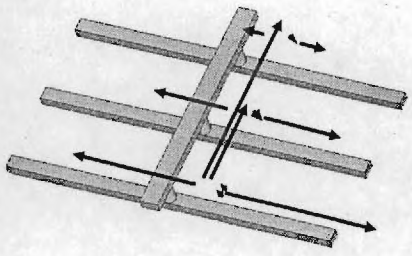


High Resistivity Substrate

Elliptical Pattern and Physical Explanation



Elliptical pattern on M1 metal Layer



Noise propagation along Vdd buses

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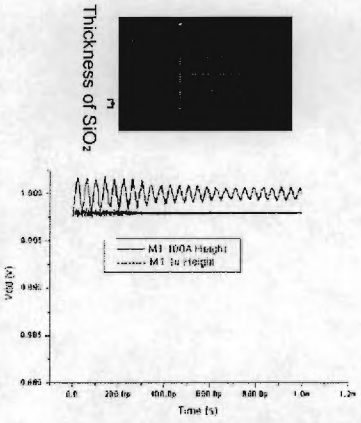
Different Thickness Between M1 and Si

M1 Resis.= 5 (Ωcm)	Thickness of SiO_2 between M1 and wafer		
	1u	300A	100A
L(pH)	76.513	76.483	76.467
R(ohm)	0.20949	0.20949	0.20948
C(fF)	23.752	23.778	23.795
G(ms)	0.00992	0.55903	0.61786

Tab.2 RLGC of M1 bus with different height



Noise waveform at same Vdd Node

Effect: thin SiO_2 helps attenuate switching noise.

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Future Work

- Modeling methods for low resistivity silicon
- Modeling of CMOS inverters and RF circuits
- Effect of onchip decoupling capacitor on simultaneous switching noise
- Substrate noise coupling between digital and RF circuits
- Chip package co-simulation
- Noise coupled through package among mixed-signal circuits

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Summary for Task RID: 1063.001

- Good start to a very aggressive program
- Preliminary results indicate that the TMM can be applied to complex package and board power distribution networks
  (Ex: Rambus Test Vehicle)
- Preliminary results show importance of Silicon Substrate loss on power supply noise propagation
- Preliminary integration of TMM into Switch completed
- Need access to layout of chip power distribution network for analysis

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PART 2

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Office of Research Administration, Compliance, Training & Technologies (ReACTT)
RESEARCH REPORT APPROVAL SHEET

Project No. E-21-6MW
Lab/School/Center: ECE

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A. Report Title Use of Transmission Matrix Method and its Comparison to Finite difference Time Domain
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Georgia Tech Research Corporation

Georgia Institute of Technology
Office of Sponsored Programs
Atlanta, Georgia 30332-0420 U.S.A.

February 17, 2004
In reply refer to: E-21-6MW

Dr. Harold H. Hosack
Semiconductor Research Corp.
1101 Slater Road
Brighton Hall
Durham, NC 27703

Subject: Transmission Matrix Method report
Project Director(s): Dr. M. Swaminathan
Telephone No.: (404) 894-3340
Contract No.: 2003-NJ-1063
Prime No: N/A
"Use of Transmission Matrix Method and its Comparison to Finite difference Time Domain"
Period Covered: N/A

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Thelma Woods
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E-21-6 MW #2

Use of Transmission Matrix Method and its Comparison to Finite Difference Time Domain Method for Modeling Power Distribution Networks

Abstract: Power distribution networks can be broadly classified into on-chip and package power distribution. For computing the dynamic electromagnetic response of these networks, Maxwell's equations need to be numerically solved. These equations can be solved either in the time or frequency domain using an integral equation or differential equation based approach. Both the Transmission Matrix Method (TMM) and Finite Difference Time Domain (FDTD) methods are differential equation based solvers with the primary difference that TMM is a frequency domain based method [1] while FDTD is a time domain based method [2].

On-chip power distribution is a highly dissipative network as compared to the package power distribution. However, on-chip power distribution networks are more complex, requiring more unknowns for representing them. These two properties require different methods for analyzing the on-chip and package power distribution networks. Since the package power distribution is a high Q passive circuit, use of FDTD could create two problems namely, i) result in erroneous frequency domain response if the waveform hasn't reached the steady state and ii) take a long time to converge due to the time step dictated by the Courant condition. On the other hand, FDTD can produce a robust solution for on-chip power distribution due to its dissipative characteristics, resulting in the waveform reaching the steady state in a few time steps.

In this report, the TMM and FDTD methods have been applied for analyzing a package power distribution structure. As a comparison, the results in the frequency domain have been compared along with the time required for the solution. A commercial tool was used for the FDTD method.

Technical Results and Data: The structure of the power plane is shown in Fig. 1. It consists of an irregularly shaped power and ground plane populated with decoupling capacitors and ferrite bead. The structure also contains numerous vias, as shown in the figure. The port locations at which the frequency response was computed are as follows: Port 1: (0.677,3.7268); Port 2:(1.058,1.3138); Port 3:(3.471, 1.6948) and Port 4:(3.09, 4.1078). All dimensions are in cms. The input impedance of the ferrite bead that was used is shown in Fig. 2. The frequency response of the bare board was measured at port 1 using a network analyzer, converted to impedance parameter and compared with the results from the TMM method and FDTD method. Fig. 3 shows good comparison between measurements and the TMM method. However, Fig. 4 shows erroneous results from the FDTD method, causing a shift in the resonant frequencies. In addition, at high frequencies, FDTD shows a capacitive behavior as opposed to an inductive behavior that was measured. In Table 1, the CPU time for analyzing the structure has been compared using the TMM and FDTD method. As shown in the figure, a speed-up of 670 – 800X has been achieved using TMM method as compared to the FDTD method.

The inaccuracy in the results can be attributed to the lack of convergence. In other words, the waveform hasn't reached the steady state before conversion to the frequency domain. The large CPU time for the FDTD method can be attributed to the small time step (dictated by the Courant condition) and the high Q characteristics of the structure, which requires numerous time steps for reaching the steady state.

However, as shown in [2], the FDTD method is suitable for on-chip power distribution networks, which are dissipative in nature. Hence, the steady state solution does not require a large number of time steps.

As an example, consider the on-chip power grid structure shown in Fig. 5. One current source was placed at the center of the on-chip power grid to study the characteristics of the power grid using FDTD. The current source has a rise time of 100 ps, a fall time of 200 ps and peak current of 1 A. A total of 38896 on-chip decoupling capacitors were uniformly distributed over the on-chip power grid. Each decoupling capacitor has 1.5 pF of capacitance, 1 pH of ESL (Equivalent Series Inductance) and 0.001 ohm of ESR (Equivalent Series Resistance). Fig 6. (a)-(f) show the snapshots of the transient voltage response with one current source at different times. Fig. 6. (a) shows the differential noise due to the single source excitation at t=110ps, propagating outwards as shown in Fig. 6. (b)-(e). Finally, at time t=1160 ps, the radial wave propagation is totally attenuated, as shown in Fig 6. (f). Based on the transient response, the propagation length is 3660um. At this distance, the energy in the radial wave is completely attenuated. This noise localization effect can be attributed to the low Q characteristics of the on-chip power grid.

Conclusion: Based on the many test cases that have been considered (one that has been provided in this report), the TMM method seems well suited for modeling power distribution in the package. However, FDTD method is more appropriate for modeling on-chip power distribution. In both cases, Maxwell's Equations are analytically solved to extract the transmission line parameters before applying the two methods, as part of the SRC project.

References:

[1] J. Choi, S. Min, J. Kim, M. Swaminathan, W. Beyene and X. Yuan, "Modeling and Analysis of Power Distribution Networks for Gigabit Applications", *IEEE Transactions on Mobile Computing*, vol. 2, no. 4, pp.299-313, October-December 2003.

[2] J. Mao, W. Kim, S. Choi, M. Swaminathan, J. Libous and D. O' Connor, "Electromagnetic Modeling of Switching Noise in On-Chip Power Distribution Networks", *Proceedings of the International Conference on Electromagnetic Interference and Compatibility (INCEMIC)*, pp. 47-52, Chennai, India, Dec. 2003.

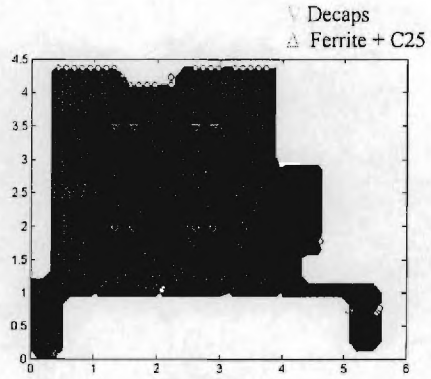


Fig. 1. Irregular Power Plane Structure

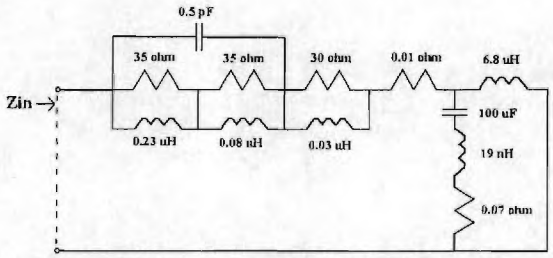


Fig. 2. Ferrite Bead with 100uF Capacitor

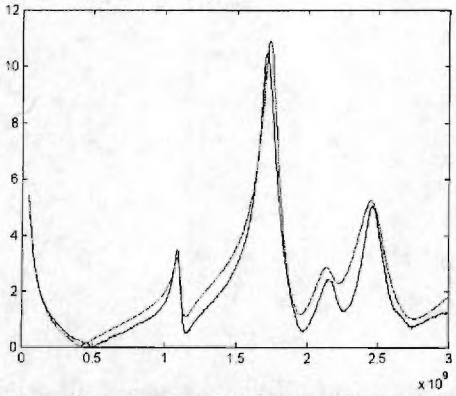


Fig. 3. Z11 Vs Frequency: Comparison between TMM Method (Blue) and Measurements (Red)

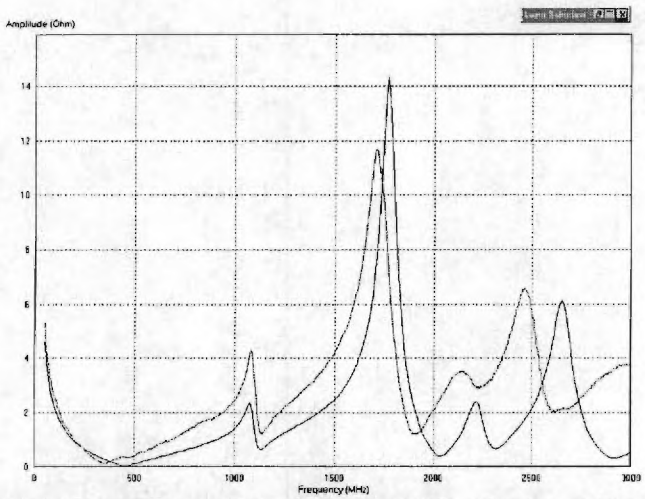
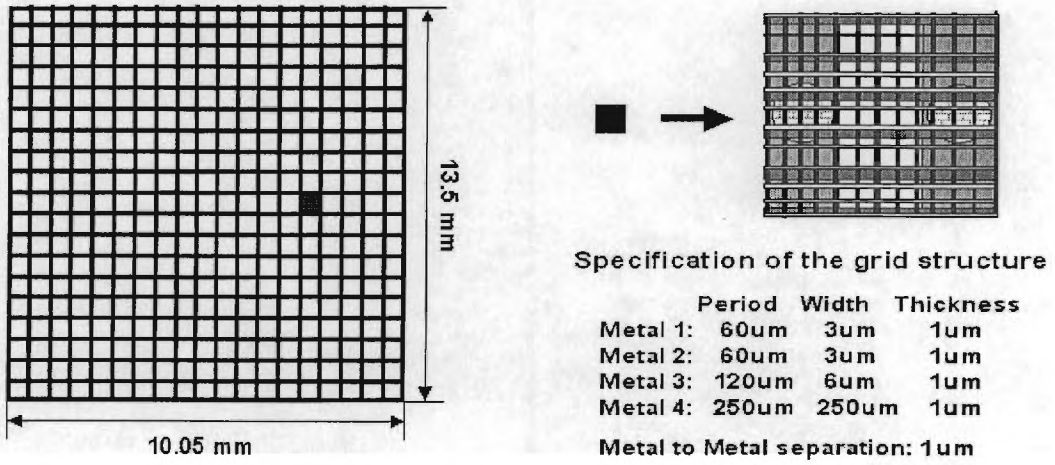


Fig. 4. Z11 Vs Frequency; Comparison between FDTD (Blue) and Measurement (Red)

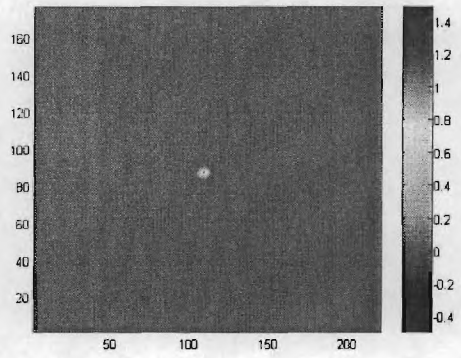
Test Case	TMM	FDTD	Speed-up
Plane (without Decaps)	213 s	40 hrs	~ 670
Plane (with Decaps)	220 s	50 hrs	~ 800

Table 1. Comparison between TMM and FDTD for Package Planes

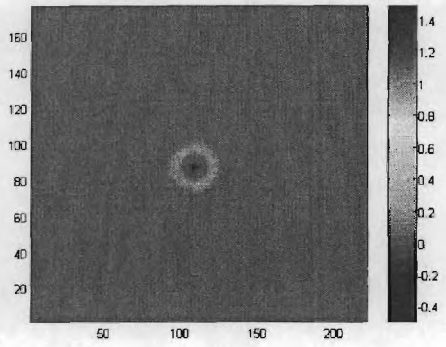


(a) (b)

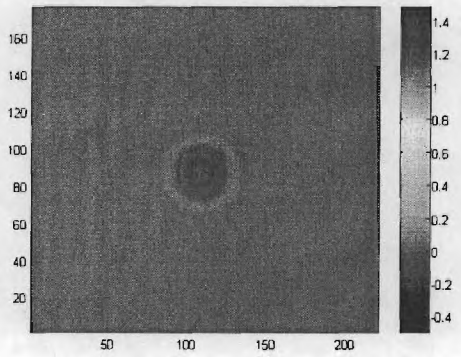
Fig. 5. (a) On-chip power grid structure. (b) Detailed description of a unit cell.



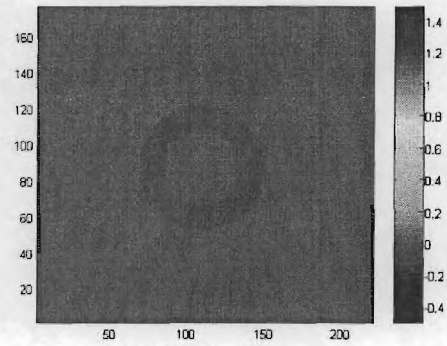
(a) At t=110ps



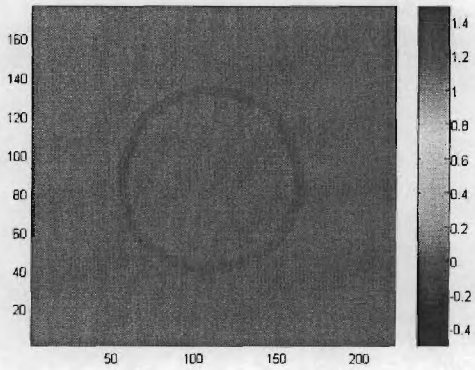
(b) At t=310ps



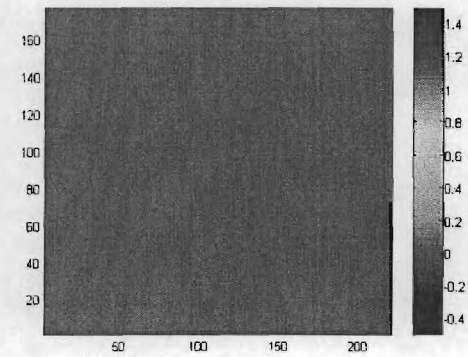
(c) At t=450ps



(d) At t=750ps



(e) At t=1000ps



(f) At t=1160ps

Fig. 6. Snap shots of the radial wave propagation due to single source excitation at the center of the on-chip power grid.

PART 3

GEORGIA INSTITUTE OF TECHNOLOGY OFFICE OF SPONSORED PROGRAMS
Office of Research Administration, Compliance, Training & Technologies (ReACTT)
RESEARCH REPORT APPROVAL SHEET

Project No.__E-21-6MW____
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1. GENERAL
A. Report Title___Electronic Modeling of Power supply Noise in On_Chip Power Distribution Networks_____
B. Author(s) and/or PD/PI__ M Swaminathan _____Phone___404-894-3340_____
C. Period Covered:_____Due Date_____

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In reply refer to: E-21-6MW

Dr. Harold H. Hosack
Semiconductor Research Corp.
1101 Slater Road
Brighton Hall
Durham, NC 27703

Subject: On-Chip Power Distribution Preliminary Report
Silicon Substrate Losses Report
Project Director(s): Dr. M. Swaminathan
Telephone No.: (404) 894-3340
Contract No.: 2003-NJ-1063
Prime No: N/A
"Electronic Modeling of Power Supply Noise in On-Chip Power Distribution Network"
Period Covered: N/A

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3+4

Electromagnetic Modeling of Power Supply Noise in On-Chip Power Distribution Networks

Abstract: This report summarizes recent results for the modeling of simultaneous switching noise in on-chip power distribution networks. The circuit models of orthogonal multi-conductor buses are first derived as frequency dependent RLGC parameters using conformal mapping and complex image theory. The analytical expressions accurately characterize the dispersive nature of interconnects over finite-resistivity substrates. Debye rational functions are then adopted to represent the frequency dependent impedance/admittance parameters. Finally, the waveform and propagation pattern of the noise are simulated using Finite Difference Time Domain (FDTD) method. The power distribution analysis including substrate effects can prevent the over-designed of power distribution networks, since the finite resistivity of the substrate help attenuate simultaneous switching noise.

Technical Results and Data: Complex image theory has been used for modeling the on-chip interconnects for extracting the frequency dependent transmission line parameters. This method takes into account the loss due to eddy currents in the silicon substrate by replacing the substrate with a conducting image plane located at a complex distance from the metal-SiO_2 interface as shown in Fig. 1. The numerical results show good agreement with measurement from Vector Network Analyzer for Coplanar Waveguide (CPW) on wafers with high resistivity (2000Ω-cm) and low resisitivyt (100Ω-cm), as shown in Fig. 2. The parameters of the CPW transmission lines were as follows: W_{vdd}=25μm, W_{gnd}=300μm, h_{ox}=1μm and h_{Si}=500μm.

Due to its periodicity topology and symmetric field distribution, the capacitance of coplanar multi-conductor (CMC) structure in on-chip power distribution networks can be derived using conformal mapping as show in Fig. 3-5, using which the RLGC transmission line parameters can be extracted. The differences between RLGC parameters of a CPW and CMC structure with similar geometry, namely w=25μm, h_{ox}=1μm, h_{si} =500μm as defined in Fig. 1 with width of Vdd the same as Gnd for the CMC structure, is shown in Fig.6.

For simulating the very large equivalent circuit representing the power grid in the time domain, FDTD has been used. First order Debye approximation has been used for approximating the frequency dependent power grid, as shown in Fig. 7. Computational efficiency of FDTD is maintained since it only takes a slight modification in the algorithm to include the first-order Debye circuit model.

A software program has been developed in C++ language to construct the on-chip power grid model automatically, which takes the power grid geometry data as input and the outputs of the program are a group of text files, which are either in the format of SPICE netlist or in a format readable by parameter extraction tools. The effect of substrate resistivity on SSN has been demonstrated through a simple test vehicle, which is a 4mm×4mm chip with a three-layer power supply consisting of pitch in each layer of 20μm, 40μm, and 80μm. Two simulations have been done for the chip with the same physical setup but different substrates with high and low resistivity. The voltage at a node 1mm away from the chip center at the bottom layer has been recorded. The waveforms for the two substrate have been compared in Fig. 8. It can be clearly seen that lossy substrate helps attenuate the on-chip simultaneous switching noise by reducing the peak-to-peak value and accelerating the damping of the voltage swing.

The detailed technical results and data can be obtained in SRC publication P007759, P007760 and P007761.

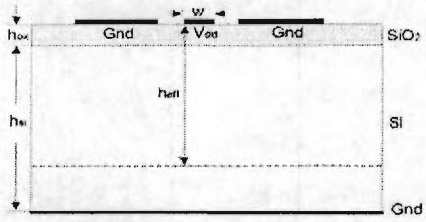
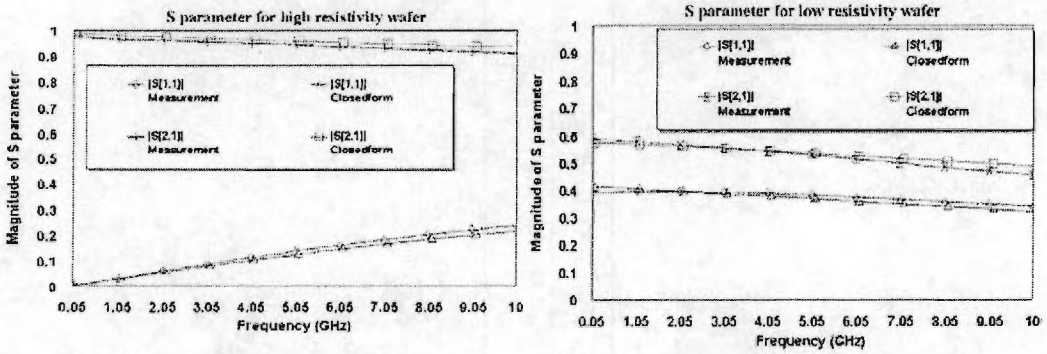


Fig.1. On-chip coplanar waveguide.



a) CPW on high resistivity wafer

b) CPW on low resistivity wafer

Fig.2. S parameter of CPW on wafer with different resistivity

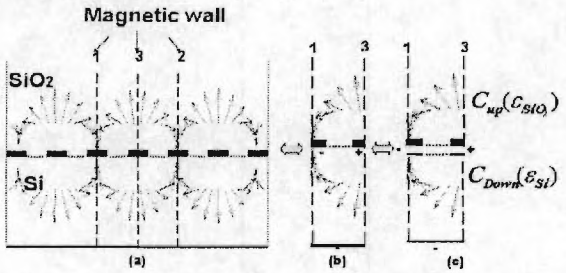


Fig.3. Electric field of CMC and capacitance calculation

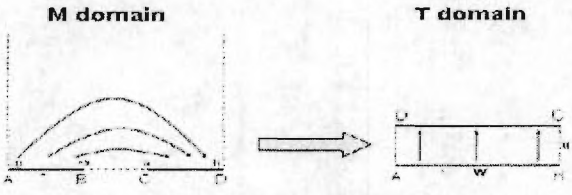


Fig. 4. Conformal mapping of C_{up}

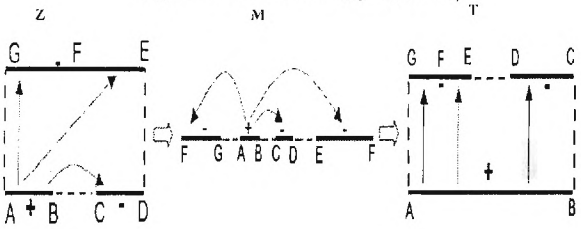


Fig. 5. Conformal mapping of C_{down}

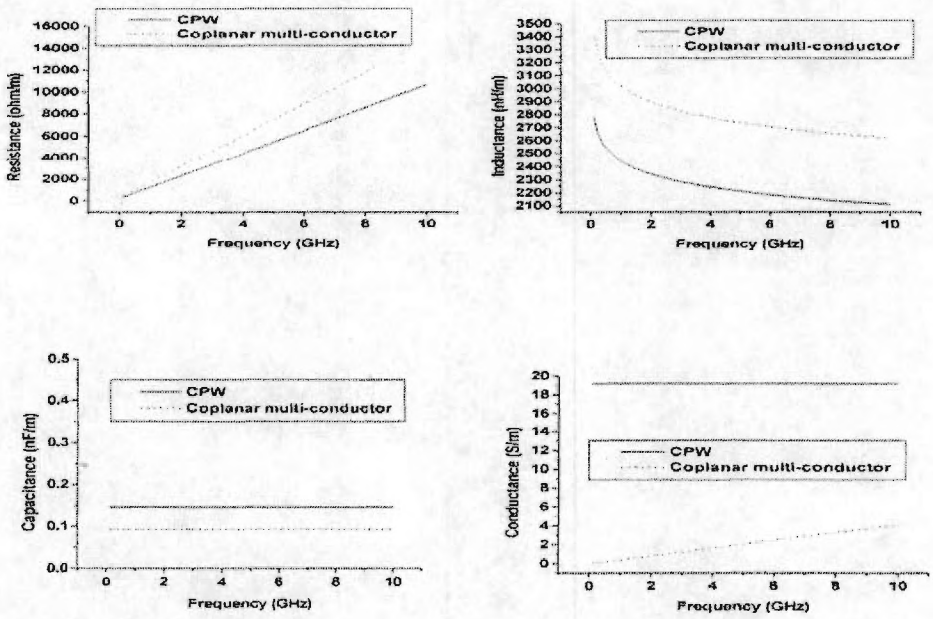


Fig. 6. RLGC parameter of CPW and coplanar multi-conductor

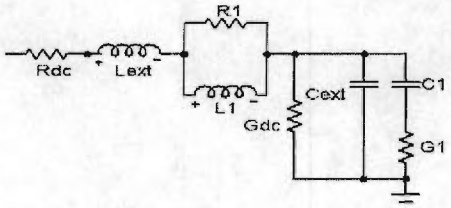


Fig. 7. Implementation of first order Debye approximation

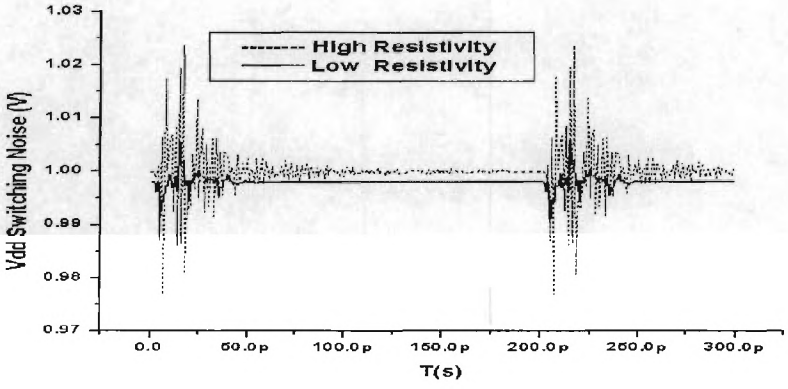


Fig. 8. Switching noise on wafers with different resistivity

[P007759] J. Mao, M. Swaminathan,, J. Libous and D. O'Connor, "Effect of Substrate Resistivity on Switching Noise in On-chip Power Distribution Networks", 12th Electrical Performance of Electronic Packaging, pp. 33-36, Oct.2003.

[P007760] J. Mao, W. Kim, S. Choi, M. Swaminathan, J. Libous and D. O'Connor, "Electromagnetic Modeling of Switching Noise in On-Chip Power Distribution Networks", 8th International Conference and Workshop on Electromagnetic Interference and Compatibility, Dec. 2003.

[P007761] J. Mao, M. Swaminathan, J. Libous and D. O'Connor, "Electromagnetic Modeling of On-chip Power Distribution Networks", 20th Annual Review of Progress in Applied Computational Electromagnetics, April, 2004.