An Inductively Powered Multichannel Wireless Implantable Neural Recording System (WINeR)

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An Inductively Powered Multichannel Wireless Implantable Neural Recording System (WINeR)

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To my family

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SUMMARY

The objective of this research is to advance a multi-channel wireless implantable neural recording (WINeR) system for electrophysiology and behavioral neuroscience research applications. The system is composed of two units: a system-on-a-chip (SoC) transmitter (Tx) unit and a receiver (Rx) unit. In the Tx unit, the outputs are combined with marker signals and modulated into pulse widths after the neural signals are amplified and filtered by an array of low-noise amplifiers (LNA). The next step involves time-division multiplexing (TDM) of pulse-width modulation (PWM) signals. The TDM-PWM signal drives RF transmitter block and is transmitted by an antenna. To satisfy the needs of neuroscientists during animal experiments, the proposed WINeR system provides long-term recording with inductive powering and stimulus-artifact rejection for closed-loop operations, which requires simultaneous stimulation and recording.

The Rx is another critical unit for wireless-link communication. To increase the area of wireless coverage, multiple antennas are used for the Rx. In addition, the automatic frequency-tracking method is used to track free-running Tx frequencies, and a smart time-to-digital conversion method is used to reduce noise and interference. A high-throughput computer interface and software are also developed to continuously receive and store neural data. The WINeR system is a potential tool for neuroscientists due to several advantages, such as a reliable wireless link with large coverage and no blind spots, low power consumption, an unlimited power source, and a stimulation function.

The contributions from this research are summarized as follows:

1. Development of a low-power and low-noise neural recording amplifier
2. Development of a power scheduling mechanism for a multi-channel analog front-end (AFE) to conserve power consumption
3. Development of a dual-slope charge sampling AFE, which can simultaneously amplify and filter neural signals and easily modulate them into PWM signals

4. Development of a wideband multi-antenna receiver for the wireless recording of animals in large arenas
5. Development of a real-time data acquisition system for multi-channel neural recordings
6. Development of a pulse-width-modulation impulse-radio ultra-wideband (PWM-IR-UWB) receiver for a low-power wireless neural recording system
7. Development of a robust closed-loop power transmission system based on RF back telemetry
8. Demonstration of a battery-powered WINeR system tested in scientifically meaningful *in vivo* experiments in large arenas
9. Demonstration of data acquired from an inductively powered WINeR system from an animal in a home cage

CHAPTER I

INTRODUCTION

1.1. Motivation

The multisite monitoring of brain activities is essential to the ongoing development of effective therapies for neurological diseases, such as epilepsy, dementia, and Alzheimer's disease. Over the past few years, researchers have attempted to engineer multichannel neural recording systems with minimum disturbance to the animal subject. Wireless operations possess several distinct advantages compared with wired operations, including the elimination of tethering effects, minimal irritation, a low risk of infection, smaller size, and simplicity. However, hardwired systems remain more popular than their wireless counterparts in the majority of neurophysiology laboratories. Wireless systems continue to experience a variety of problems, such as limited battery lifetime, limited wireless coverage area, and poor connectivity, which render them unreliable for state-of-the-art behavioral neuroscience studies.

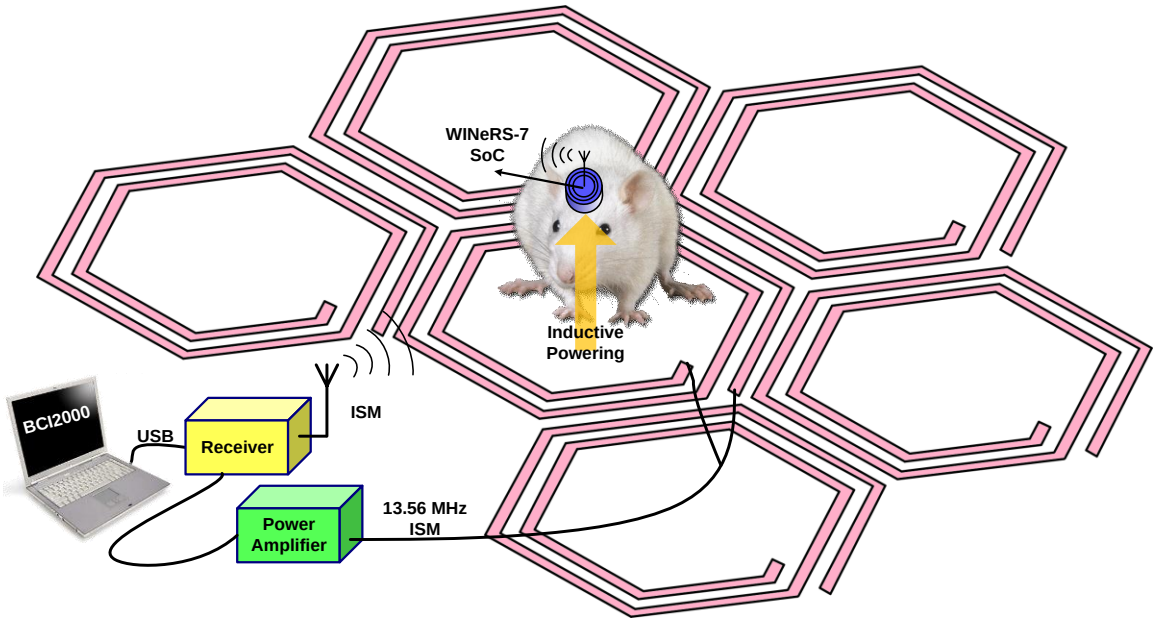


Fig. 1.1. A conceptual view of the inductively powered wireless implantable neural recording system-on-a-chip with for long-term neural recording from small freely behaving animals.

The objective of this research is to develop a multi-channel wireless implantable neural recording (WINeR) system that outperforms existing systems. A WINeR system can provide a reliable wireless link with large coverage without blind spots, low power consumption, an unlimited power source, and a stimulation function with stimulus-artifact rejection. Thus, the developed system enables neuroscientists to eliminate cables from their experimental setups and detect high-density and meaningful neural signals.

A conceptual view of the WINeR system is provided in Fig. 1.1, which employs two independent wireless links in the industrial-scientific-medical (ISM) band at 433/915 MHz and 13.56 MHz for wireless neural recording and inductive powering, respectively.

1.2. Background

1.2.1. Neural-Recording Applications

Neural recording technology has become significant in the medical treatment of neurological diseases and neuroscience research [1]-[4]. Devices that target neurological diseases, known as neuroprostheses, replace sensory or motor functions that may become lost as a result of injury or disease. These devices must be chronically implantable, safe, and highly reliable for use in humans as part of a therapeutic paradigm. Size, power consumption, and carrier frequency are highly constrained in these devices due to implantation requirements. Cochlear implants and deep brain stimulation (DBS) are examples of neuroprostheses that produce undeniably positive outcomes [5].

Devices that target neuroscience research applications are frequently used on animal subjects and do not always have to be implantable. They are frequently used to monitor interactions among large populations of neurons because animals perform specific tasks that involve processing sensory inputs, generating motor control outputs, or performing specific cognitive functions, such as learning and memory [6]. However, these devices must compete with sophisticated instruments that are employed by the

neuroscience community [7]. These devices should provide the same quality and quantity of information as their previous counterparts while resolving some of their limitations, such as hardwired interconnects. The tethering effect produced by wires attached to small animals may affect animal behavior. These devices deteriorate rapidly, increase noise and motion artifacts, and require costly motorized commutators as part of the recording setup.

1.2.2. Neural-Recording Amplifier Design

The depolarization of the membrane of a neuron generates extracellular action potentials (AP) that are waveforms in the range of 100 Hz to 10 kHz with amplitudes ranging from 50 μVpp to 1 mVpp. Another important neural signal is the local field potential (LFP) that consists of lower-frequency neural waveforms ranging from mHz to 200 Hz with amplitudes ranging from 500 μVpp to 5 mVpp [8]. It is very important to have a low-noise neural amplifier design to record both neural signals. Indeed, achieving a low-cutoff frequency in the sub-hertz range with a small footprint and low-power consumption on the chip is a challenge for LNA designers. Among them, Harrison et al. have reported a remarkable study [9], in which they presented a topology for a metal-oxide-semiconductor (MOS) and bipolar pseudo-resistor with a capacitor feedback amplifier. This topology has been used by many other groups [10], [11]. In addition, Harrison et al. resurrected a figure-of-merit for noise performance known as the noise efficiency factor (NEF), which is defined as

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}},$$

where $V_{ni,rms}$ is the input-referred rms noise voltage, I_{tot} is the total amplifier supply current, and BW is the amplifier bandwidth in hertz. U_T is the thermal voltage kq/T, k is the Boltzmann constant, and T is the absolute temperature. An amplifier using a single bipolar transistor (with no 1/f noise) has an NEF of one; all practical circuits have

higher values. Using NEF has encouraged designers to invent topologies and techniques with successively lower and improved NEFs.

However, in these designs, the MOS resistance highly depends on the input and output voltages, causing distortion when large signals appear at the output. This is not uncommon, particularly at the output of the second OTA in the presence of local field potentials (LFPs) that are in-band neural signals from large populations of neurons firing in sync and creating low-frequency signals with relatively large amplitudes. To solve this problem, Zou et al. developed a balanced tunable pseudo-resistor to minimize the resistance distortion depending on the output voltage [12]. In addition, although 895 nA of low-power consumption was remarkable, the bandwidth was low for neural-recording applications.

Several interesting LNA architectures have been proposed after Harrison. One of the most interesting circuit configurations that has been developed to improve the NEF is that of the source degeneration resistor, which is proposed in [13]. The noise contribution from a source-degenerated load is mainly from degeneration resistors, whose noise is essentially thermal, whereas MOSFETs in a regular active load contribute a large amount of 1/f noise. Otis et al. proposed a complementary input stage to double the effective transconductance with a given bias current [14]. Muller et al. used a digitally intensive architecture to reduce system area and enable operation from a 0.5 V supply. The architecture replaced AC coupling capacitors and analog filters with a dual mixed-signal servo loop, which allows for the simultaneous digitization of the action and local field potentials. A noise-efficient DAC topology and a compact, boxcar sampling ADC are used to cancel input offset. The prototype occupies 0.013 mm^2 while consuming 5 μW and achieving 4.9 μVrms of input-referred noise over a 10 kHz bandwidth [15]. Finally, Gao et al. used switched-capacitor filtering to provide a well-controlled frequency response, and utilized windowed integrator sampling to mitigate noise aliasing, enhancing noise/power efficiency [16].

1.2.3. Wireless Neural Recording Microsystems

Over the past few years, researchers have been trying to engineer multichannel neural-recording systems with minimum disturbance to animal subjects. To this end, wireless operation has several clear advantages in comparison to wired operation, such as not having tethering effects, exhibiting less irritation or a lower risk of infection, being smaller in size, and being easy to use. However, hardwired systems are still far more popular than their wireless counterparts in the majority of neurophysiology labs. Wireless systems still suffer from problems such as limited battery lifetime, limited wireless coverage area, and poor connectivity, which render them unreliable for state-of-the-art behavioral neuroscience studies.

The majority of ongoing wireless neural interfacing research has been focused on transferring some sort of limited processing capability to the implantable front-end to limit the required wireless bandwidth at the cost of losing some neural information and complicating the implantable unit [2], [17], [18]. However, these data reduction methods are employed only for spike detection. This is not possible for LFP recording, although LFPs are becoming increasingly important in neurophysiological investigations [19]. Moreover, the majority of the research on wireless neural recording performed to date has been focused on the high-density recording front-ends and the transmitting (Tx) side of the system, where the main challenges are miniaturization, low-power consumption, and low noise to the extent that the Tx side could eventually be implanted in the animal or human body. However, in a complete wireless data acquisition system, the wireless link, external receiving (Rx) side, computer interface, data storage, and user interface should be able to support the Tx unit for the entire system to operate smoothly without losing information that is important for the further processing of the recorded signals.

The most challenging problems to address in designing the Rx side are bandwidth, sensitivity, coverage of the experimental arena without leaving blind spots, and continuous streaming of the acquired data to the computer without any losses. In

some early designs, analog samples were amplified, filtered, and directly fed into a voltage-controlled oscillator (VCO) on the Tx side to be frequency modulated (FM) after time-division multiplexing (TDM). On the Rx side, commercial FM receivers, such as the WinRadio (Melbourne, Australia) were employed [20]. However, because of the bandwidth limitation (~150 kHz) on the Rx side, such systems suffered considerable crosstalk between channels, which also limited the number of channels to fewer than 10. Increasing the Rx bandwidth can alleviate these problems, as demonstrated in a 32-channel wireless neural-recording system by Triangle Bio-Systems (Durham, NC), which operates at 3.2 GHz using a custom-designed Rx with a bandwidth of 300 MHz [21]. Another advantage of increasing the carrier frequency is reducing the size of the optimal antennas. However, such frequencies are not useful for implantable devices because of the significant absorption of high-frequency electromagnetic fields in the tissue [22].

As a result of the above-mentioned limitations, most recent wireless neural-recording systems have on-chip analog-to-digital converters on the Tx side followed by amplitude, on/off, frequency, or phase-shift keying (ASK/OOK/FSK/PSK) to transmit digital samples in the industrial, scientific and medical (ISM) band. The HermesD system, for instance, utilized an FSK scheme along with a 24 Mbps custom-designed transceiver [4]. Rizk et al. used a commercial ASK/OOK transceiver at 1 Mbps from RF Monolithics (Dallas, TX) for their 96-ch system [23]. Cheney et al. used a commercial 2.4 GHz FSK transceiver at 1 Mbps from Nordic Semiconductor (Trondheim, Norway) for their 16-ch system [24]. High-data-rate digital systems require frequency-stabilization components, such as crystals and phase locked loops (PLL), to reduce the phase noise and ensure proper synchronization between Tx and Rx, which can increase the size and power consumption of the Tx. Those with lower data rates either have a limited number of channels, low sampling rate per channel (not suitable for single-unit recording), or require an extensive data reduction strategy on the Tx side [25].

Using ultra wideband (UWB) transceivers is quite attractive because of their high data rate, low multipath interference, low-power consumption, and relatively simple circuitry on the Tx side. Chae et al. developed a 128-ch neural-recording system operating over the 3-5 GHz band [17]. They reported a maximum data rate of 90 Mbps; however, neither separation between Tx-Rx nor coverage of the experimental space was reported. Greenwald et al. also developed a 16-ch neural monitoring system with a controllable pulse rate between 90 and 270 MHz [26]. They verified the functionality of the system *in vivo*. However, a data rate of 1 Mbps was insufficient for neural-recording systems with high channel count. A UWB transceiver is commercially available from Neuralynx (Bozeman, MT) for another 128-ch system, which offers a data rate of 100 Mbps and supports up to 18-bit resolution and 32 kSps for all channels [27]. However, the architecture of the Rx has not been disclosed. Although the UWB offers many advantages, it is prone to interference from other RF sources. In addition, because of the wide spectrum of the device's carrier-less short pulses, a long synchronization time is required to achieve lossless signal acquisition and tracking on the Rx side with complex signal processing methods to recover data in noisy environments [28].

1.2.4. Inductive Powering

A key limitation of common wireless neural recording systems is that the animal subject must carry a large payload of batteries. This requirement may not be an issue in recording from costly primates [3], [29]. However, the majority of laboratories use small animals, such as rats and mice, for which a compromise must be reached between the size and the weight of the headstage and the uninterrupted duration of the experiments. The ability to conduct long-term uninterrupted recording is attractive to neuroscientists because the neural population under analysis frequently changes over time. Therefore, overnight recording is required to track neurons for an extended period of time for learning studies or to combine experimental trials across consecutive days [4].

Cong et al. designed a blood-pressure-monitoring microsystem that was powered by an external RF power source. The received RF power level and blood pressure signals can be sensed and wirelessly transmitted for feedback control of the external RF power [30]. Xiao et al. designed a 20-μW neural-recording tag for extremely small implants; the tag can be either remotely powered using a transponder-reader link or operated from a small battery to expand the communication range [31]; however, they did not apply their system to *in vivo* experiments. Sodagar et al. proposed an implantable microsystem that was capable of simultaneously recording neural activity on 64 channels and wirelessly transmitting spike occurrences to an external interface. Although the system is powered and programmed through an inductive RF link, the distance is limited [18].

1.2.5. Recording and Stimulation

Some applications require a system that interacts with the central and peripheral nervous system in a bidirectional manner. For example, DBS which is an effective neuromodulation therapy for Parkinson's disease (PD), requires neural recording for a closed-loop operation. Shahrokhi et al. developed a 128-channel neural recording and stimulation interface [32] that did not operate with a wireless system, featured no stimulus-artifact rejection, and was not used to perform *in vivo* experiments. Lee el al. introduced 64-channel stimulators and an 8-channel neural-recording system [33] with an external wireless micro controller. Azin et al used two identical 4-channel modules in a single SoC [34].

When recording and stimulation are performed simultaneously, a large amount of stimulation current can force the saturation of adjacent recording electrodes and recording amplifiers. Due to the large time constant, the recovery may be time consuming but can prevent immediate neural recording after stimulation, which is referred to as a stimulation artifact [35], [36]. In the case of arrays of chronic microelectrodes, this problem is exacerbated by the close spacing between the electrodes and their mutual

coupling. Although the reduction of artifacts using software is feasible [37], software techniques are not capable of recovering the period during which the amplifiers are saturated, which is frequently longer than 5 ms. Previously reported hardware-based techniques use a low-slew-rate initial amplifier [38] or actively discharge the electrodes immediately after stimulation [39]. These solutions require that electronics be placed on the animal next to the electrodes. To reduce the complexity of hardware-based techniques, Venkatraman et al. used an array of switches between the first and second amplifier stages to disconnect the second stage from the first stage for a short period after the stimulation [40].

As previously discussed, several issues for wireless neural-recording systems remain unresolved. Important specifications for the state-of-the-art wireless neural recording systems are summarized and compared in Table 1.1. Photographs of recently developed miniaturized wireless neural-recording systems are provided in Fig. 1.2.

Table 1.1: State-of-the-art wireless neural-recording systems.

	Sodagar [18]	**Harrison [42]**	**Chae [17]**	**Miranda [4]**	**Azin [41]**	**TBSI [21]**	**Mitra [43]**	**Muller [44]**
Year of Publication	2009	2011	2009	2010	2011	2011	2013	2014
Total # of Channels	64	100	128	32	8	64	24	64
Simultaneous Channels	2	1	128	32	4	64	24	64
LNA Gain (dB)	60	60	60	46	32	58	35.6-75.6	-
Power Source	Inductively powered	Inductively powered	Battery powered	Battery powered	Battery powered	Battery powered	Battery powered	Inductively powered
Modulation	OOK	FSK	UWB	FSK	FSK	FM	-	Back-scattery
Data Carrier Frequency	174 ~ 216 MHz	915 MHz	4 GHz	3.7 ~ 4.1 GHz	433 MHz	3.2 GHz	·	N/A
Power Carrier Frequency	4 MHz / 8 MHz	2.765 MHz	N/A	N/A	N/A	N/A	N/A	300 MHz
Data Acquisition	Spike data reduction	Spike data reduction	data reduction / raw	Raw data	Spike data reduction	Raw data	Raw data	Raw data
Data rate	2 Mbps	157 kbps	90 Mbps	24 Mbps	500 kbps	3200 kSps	1 kSps For LFP	1 Mbps
Resolution (bits)	8	10	9	12	10	·	10	15
Data link Energy per bit	·	3185 pJ/b	17.78 pJ/b	1250 pJ/b	·	·	·	·
Power supply (V)	1.8	3.3	3.3	5	1.5 / 5	2.95	1.8 / 3.3	·
Process	0.5-µm CMOS	0.6-µm BiCMOS	0.35-µm CMOS	Discrete	0.35-µm CMOS	·	0.18-µm CMOS	65-nm CMOS
Power consumption (mW)	14.4	8	6	142	0.42	·	Activity-dependent	0.225

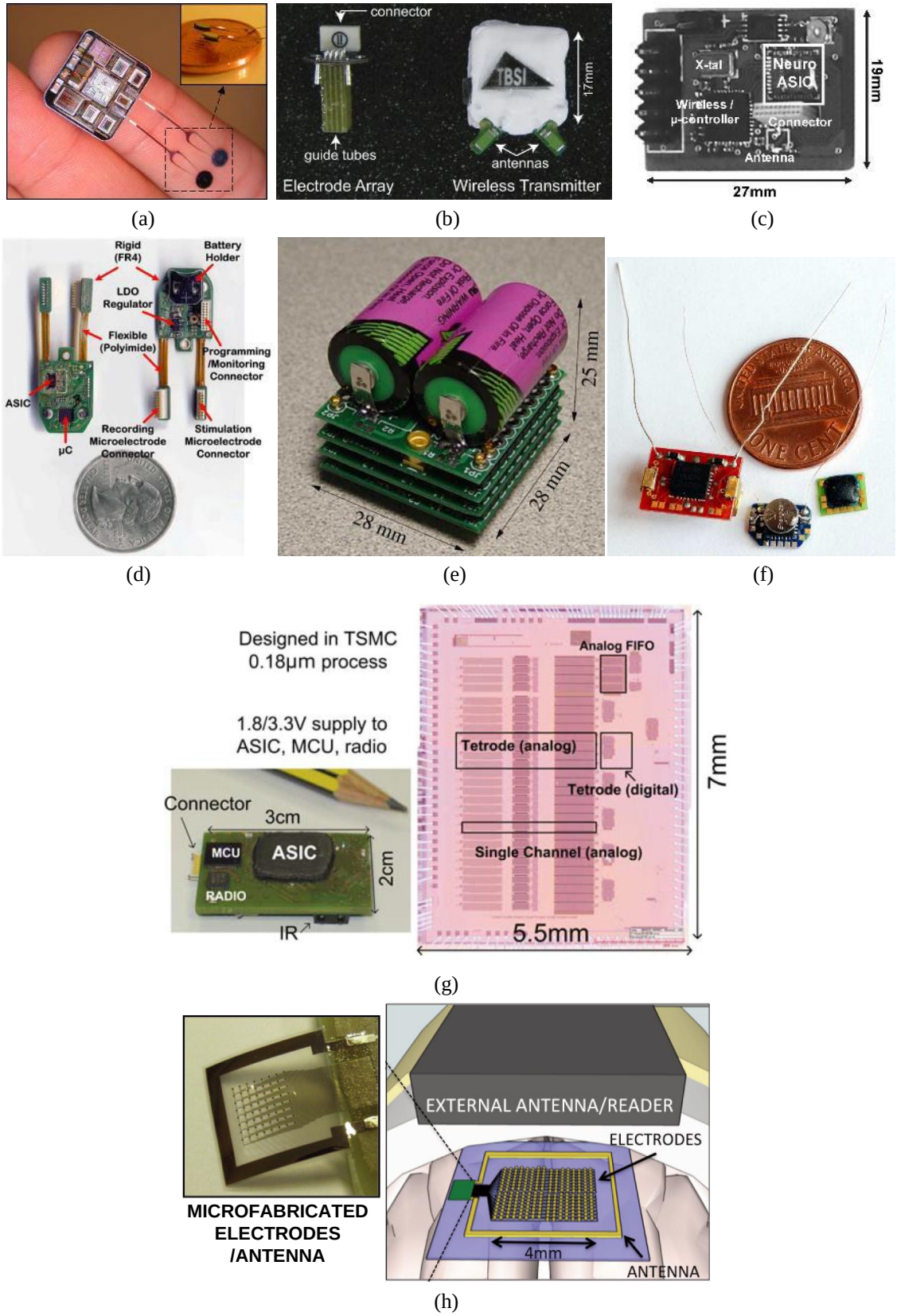


Fig. 1.1. State-of-the-art miniaturized wireless neural recording systems (a) [18], (b) [21], (c) [33], (d) [41], (e) [4], (f) [42], (g) [43], (h) [44].

1.3. Dissertation Outline

The remainder of this dissertation is organized as follows. Chapter 2 presents the preliminary wireless neural recording system WINeR-6, in which neural signals are amplified, filtered, converted to pulse width signals, and transmitted wirelessly through a FSK transmitter. After describing the Tx headstage, the wideband dual-antenna receiver, which demodulates the transmitted neural signals, is described. The results of a biologically meaningful animal experiment are also presented in this chapter. Chapter 3 proposes a dual-slope charge sampling analog front-end, which can simultaneously amplify and filter neural signals and easily modulate them into PWM signals. Chapter 4 describes a WINeR-7 system with a novel dual-slope charge sampling AFE. In this chapter, pulse-width-modulation impulse-radio ultra-wideband (PWM-IR-UWB) communication with a WINeR-7 system is also described for a low-power wireless neural recording system. Chapter 5 presents *in vivo* animal experiments performed with the WINeR-7 system, which is powered by battery source and near-field wireless power transmission. A robust closed-loop power transmission system based on RF back telemetry was developed for inductively powered freely moving animal experiments. Chapter 6 presents the conclusions of this work and proposes future studies.

CHAPTER II

WIRELESS NEURAL RECORDING SYSTEM

2.1. WINeR-6 SoC Design

Yin and Ghovanloo presented the WINeR-5 [45], which was a battery-powered 32-channel wireless neural-recording system. The next revision of the SoC, which is called the WINeR-6 was developed. Because the WINeR-6 uses a closed-loop inductive power system, it can simultaneously record from 32 channels for an unlimited period of time without losing any piece of information.

2.1.1. System Architecture

The current WINeR-6 system prototype consists of three key components: (1) a 32-channel transmitter application-specific integrated circuit (ASIC) that is integrated on a chip, (2) a custom-designed wideband receiver unit (Rx), and (3) a wireless power transmitter unit (Reader). The complete WINeR-6 system block diagram is shown in Fig. 2.1. Extracellular neural activity is picked up by a microelectrode array (MEA), which can either be micromachined or operated as an equally spaced bundle of sharpened microwires. An array of two-stage, low-noise amplifiers (LNA) magnifies the neural signals by a gain of up to 8000. An array of high-speed comparators compares the amplified neural signals with a precision triangular waveform to sample and convert the amplitudes of the neural signals to time segments in a step well known as pulse-width modulation (PWM) or analog-to-time conversion (ATC) [46]. The next stage of the WINeR-6 structure involves a time-division multiplexer (TDM), which serializes the PWM samples and combines them with four monitoring signals: half of the rectifier output ($V_{REC}/2$), the bandgap reference voltage (V_G), a temperature dependent voltage (V_T), and the negative supply rail (V_{SS}).

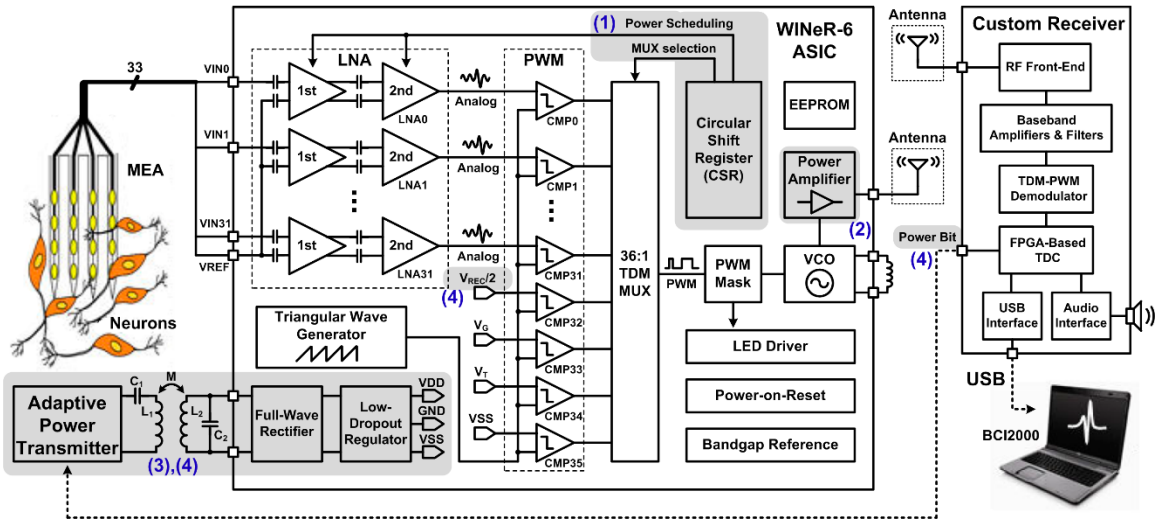


Fig. 2.1. WINeR-6 system block diagram with its key new features highlighted: (1) LNA power scheduling, (2) improved RF transmitter, (3) inductive powering, and (4) closed-loop power control.

Therefore, every frame of the PWM signal at the output of the TDM block consists of 36 pulses, which pass through a PWM mask to improve their timing accuracy and drive a tunable voltage-controlled oscillator (VCO) that operates at about 915 MHz. The VCO up-converts the baseband PWM-TDM signal by frequency-shift keying (FSK), and finally, the PWM-TDM-FSK signal at the output of the VCO is amplified and transmitted through a miniature wideband monopole antenna.

The WINeR-6 system has four important new features compared to its predecessor (WINeR-5): (1) LNA power scheduling, (2) an improved RF transmitter, (3) inductive powering, and (4) closed-loop power control, which are highlighted in Fig. 2.1 and explained in more detail in the following sections.

The prior experience with the WINeR-5 indicated that although each LNA consumes a small current, because there are 32 of them on-chip, the LNA block quickly becomes one of the major power consumers of the WINeR SoC. To address this issue, a power-scheduling mechanism places most of the LNAs that are not being sampled in sleep mode, which affords very low-power consumption. The power-scheduling mechanism is explained in greater detail in Section 3.1.2.4. In the WINeR-6, a class-AB RF power amplifier (PA) has been added after the VCO to extend the transmission range,

improve the signal to noise ratio (SNR) at the receiver input, and stabilize the operation of the VCO by blocking reflections and back scattering from the antenna. The external adaptive power transmitter, which is shown on the lower left corner of Fig. 2.1, drives a geometrically optimized hexagonal coil that induces power at 13.56 MHz in a receiver LC-tank circuit that is embedded in the animal headstage [47]. The induced power is sent to an on-chip active full-wave rectifier that is followed by a low-dropout regulator. Because of the closed-loop power control mechanism, the WINeR-6 is expected to maintain the power delivered to the headstage at a constant level even when the distance or alignment between the transmitter and receiver coils changes due to animal movements [30], [48].

2.1.2. Neural Signal Flow

2.1.2.1. Low-noise amplifiers (LNA)

The WINeR-6 analog front-end has been designed using two-stage capacitively coupled LNAs with built-in tunable band-pass filtering. A schematic diagram of the LNA is shown in Fig. 2.2. The first stage of the LNA is a fully differential operational transconductance amplifier (OTA1), shown in Fig. 2.2a and Fig. 2.2b, with a midlands gain of $C_1/C_2 = 100$. V_{CM} is the common mode voltage, which is usually grounded, and V_{REF} is the reference voltage from the animal reference electrode. Turning OTA1 completely off when it is not in use to reduce power consumption results in a long transient to allow charge to build up in its capacitors before it resumes normal operation. To reduce this transient time, the OTA1 bandwidth is changed from its nominal value of 10 kHz when the current consumption is 16 μA (En1 = VSS) and the LNA is in the active mode to 200 Hz when the current consumption is ~0.5 μA (En1 = VDD) and the LNA is in sleep mode. The second stage of the LNA (OTA2), shown in Fig. 2.2c, has an adjustable gain of either $C_3/C_4 = 20$ or $C_3(C_4+C_5)/(C_4C_5) = 80$ for a total LNA gain of

2000 or 8000 (66/78 dB). The current in OTA2 also changes from 8.6 μA to 2.8 μA when the LNA is switched from active to sleep mode and vice versa (controlled by En2).

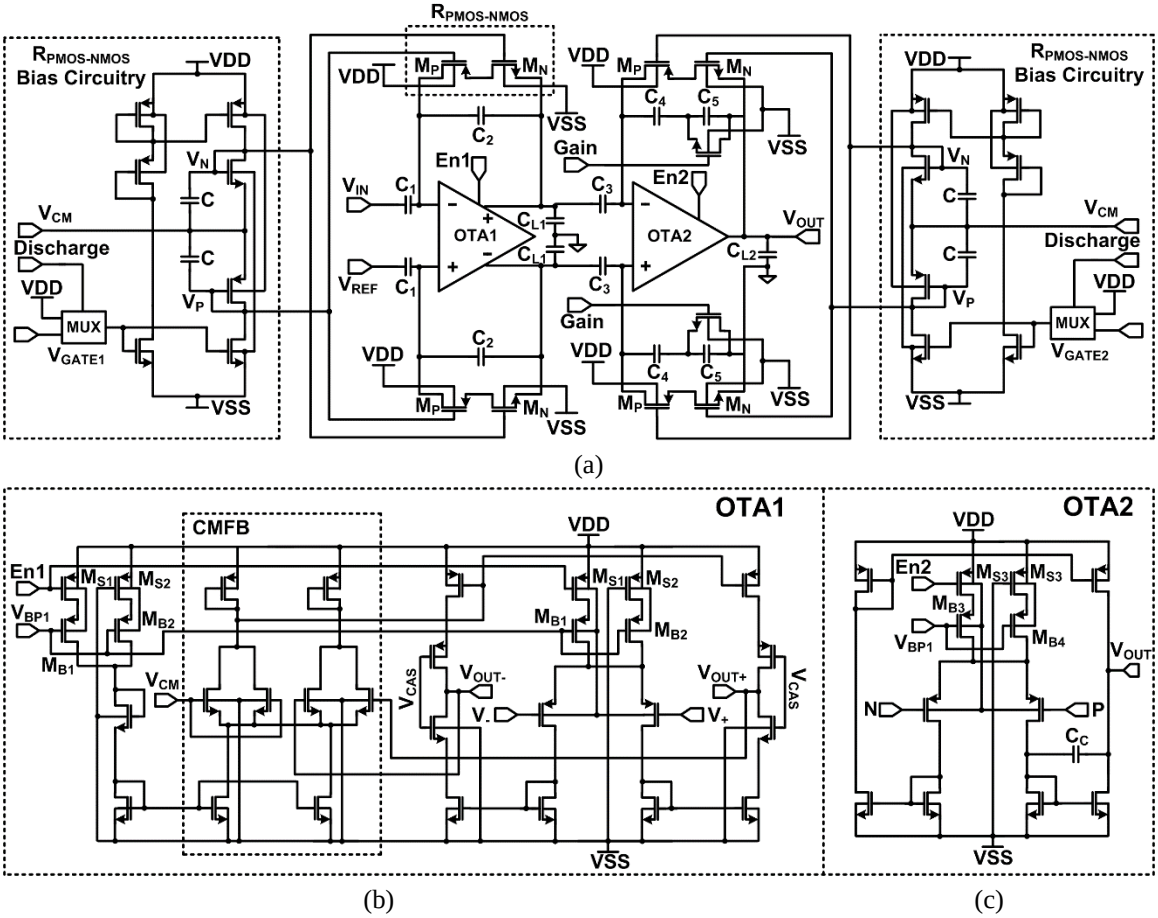


Fig. 2.2. Schematic diagram of the WINeR-6 analog front-end: (a) two stage LNA, (b) OTA1, and (c) OTA2.

To achieve high resistance($>10^{11}$ Ω) and ultra low cutoff frequencies, both stages of the LNA in Fig. 2.2a are equipped with voltage-controlled PMOS-NMOS pseudo resistors, $R_{PMOS\text{-}NMOS}$, to create a low-cutoff frequency that can be continuously tuned by V_{GATE1} and V_{GATE2}, as presented in [45]. $R_{PMOS\text{-}NMOS}$ transistors are biased with a floating bias circuitry such that they can operate as a bidirectional current source. Hence, the impedance seen from either end of the $R_{PMOS\text{-}NMOS}$ remains constant and almost independent of the OTA input and output voltages, causing less distortion.

2.1.2.2. Pulse-width modulator and 36:1 time-division multiplexer

As shown in Fig. 2.1, conditioned neural signals at the 32 LNA outputs join four monitoring signals, $V_{REC}/2$, V_{BG}, V_T, and V_{SS}, at the input of the PWM-TDM block. These 36 analog signals are fed into the PWM block, which consists of 36 rail-to-rail high-speed comparators, enabled one at a time over one sampling period to convert the analog signals from each channel into a sequence of pulses by comparing them with a precision triangular waveform (TW). To reduce noise and dynamic power dissipation, WINeR-6 does not use any high-frequency clock signal. Instead it uses a low-frequency clock at the sampling rate for TDM, which is generated locally by the triangular waveform generator (TWG) block. As a result during each comparison, the substrate is completely quiet, and there is no digital transition anywhere on the chip. Monitoring signals also play a secondary role by providing a unique pattern that is used for synchronization between the WINeR-6 transmitter and external receiver by marking the beginning of each TDM-PWM 36-pulse frame to be easily detected on the receiver side.

The TDM block consists of a 36-bit circular-shift register (CSR) and a 36:1 multiplexer (MUX) as shown in Fig. 2.3a. The CSR receives a buffered time-base signal at the sampling rate from the TWG block, shown in Fig. 2.3b, for its clock. At the global reset, the CSR is loaded with a 36-bit binary code, "1…10…00", in which the number of "1s" is programmable (N). When the system is running, the string of "1s" circulates in the CSR and connects one out of 36 comparator PWM pulses (the last "1") to the MUX output. The resulting signal will be a 36-pulse TDM-PWM frame, which is buffered and trimmed before being fed into the VCO.

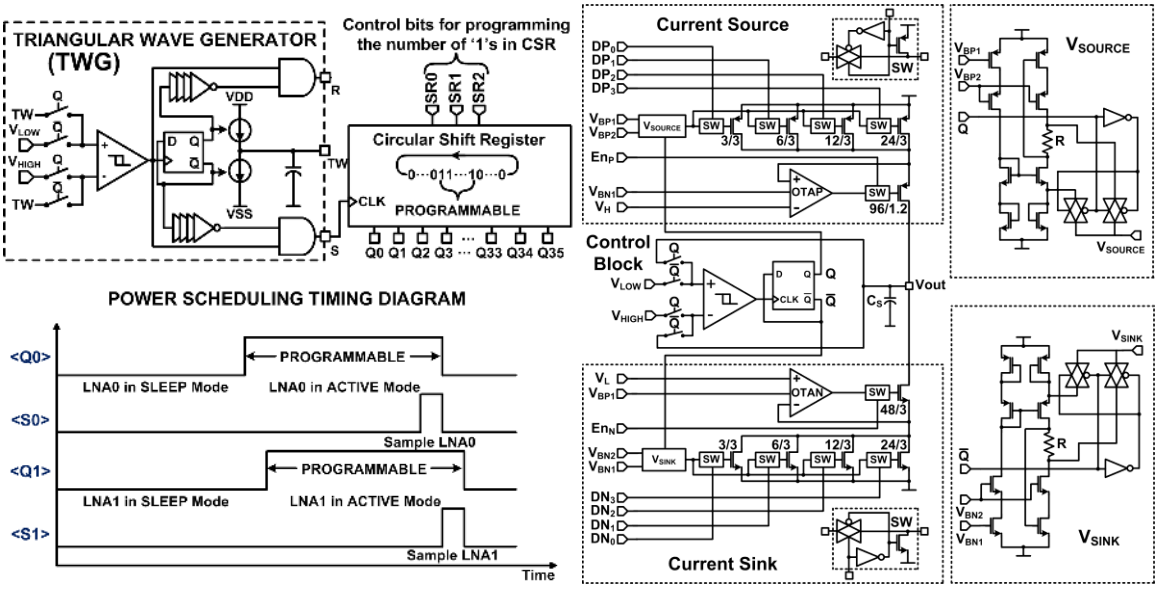


Fig. 2.3. (a) Block diagram and timing diagram of the power scheduling mechanism. The OTAs in the LNA block are switched between active (BW = 10 kHz) and sleep (BW = 200 Hz) modes by changing their bias currents, (b) schematic diagram of triangular waveform generator (TWG) block.

2.1.2.3. Triangular waveform generator (TWG)

A precision TWG, shown in Fig. 2.3b, is a key building block in accurate amplitude-to-time conversion (ATC). Its performance affects the noise, accuracy, and resolution of the system, as described in [46]. A TWG features binary weighting ($DP_{0\sim3}$ and $DN_{0\sim3}$), high voltage compliance (-1.4 ~ 1.4 V), large output impedance, and a complementary current source/sink (CCSS) pair, which linearly charges/discharges C_S (6 pF) to generate the triangular wave [45], [49]. Unlike common designs that require at least two comparators, the new TWG design utilizes only one comparator to reduce power consumption and the negative effects of offset mismatch. V_{Source} and V_{Sink} are dynamic, current-limited, bias generator blocks. They provide fast switching waveforms at specific DC biasing nodes to turn the CCSS on and off, while consuming negligible static power.

2.1.2.4. Power scheduling

Although each individual LNA consumes only ~25 μA, the 32-channel LNA block is responsible for 42% of the total WINeR-6 power consumption when all channels are active. Unfortunately, this situation is only exacerbated when the number of channels is increased. On the other hand, the TDM-PWM block, only samples one LNA at a time. To address this issue, a power-scheduling mechanism has been employed, depicted in Fig. 2.3b, which places most of the LNAs that are not being sampled in the sleep mode, reducing their power consumption by 86% to ~3.5 μA.

The LNAs are not completely turned off to reduce the transient time, t_T, for a dormant LNA to reach its active state well ahead of the sampling time and thereby be able to track neural signals with high bandwidth and low distortion (10 kHz). Because t_T cannot be reduced to zero, the number of LNAs that should be activated ahead of sampling, N, depends on the overall sampling rate, f_S, which in turn depends on the desired neural signal bandwidth, i.e.) $N > f_S t_T$. In the power-scheduling schematic, N is programmable by SR0:2, which can change the number of consecutive "1s" in the CSR from 4 to 32. For example, when N = 12, twelve consecutive "1s"circulate in the CSR and each LNA is switched to the active mode 11 times during the sampling period, $11/f_s$, before being sampled. In this case, the LNAs remain in the sleep mode during the rest of the sampling periods ($24/f_s$) and reduce the power consumption of the LNA block by 51%.

2.1.2.5. Voltage-controlled oscillator and power amplifier

The WINeR-6 RF transmitter consists of a VCO with an off-chip inductor followed by a PA, as shown in Fig. 2.4. As a result of changes in the antenna loading and reflected RF signal, animal movements in the shielded Faraday cage result in undesired VCO frequency shifts in WINeR-5. To prevent the undesired VCO frequency shifts, a

nonlinear class-AB PA is used not only to reduce the frequency shift problem but also to facilitate transmitter output matching with miniature 50 Ω antennas and extend the transmission range. A complementary negative-Gm structure is used for the VCO core because of its low power and superior phase-noise performance [50]. Coarse and fine VCO tunings are performed using an off-chip inductor and a 4-bit on-chip varactor bank (VC0:3), respectively. VCO varactors are PMOS transistors whose gates are connected to the VCO outputs, bulks are tied to V_{DD}, and sources and drains are tied together and connected to either the varactor bank control signals (VC0:3) for center frequency tuning or TDM-PWM signal to generate the FSK signal. To finely tune the transmitter frequency, VC0:3 is accessible to the user. Once the VCO frequency is adjusted to the desired band, the external receiver can be tuned to the transmitter frequency.

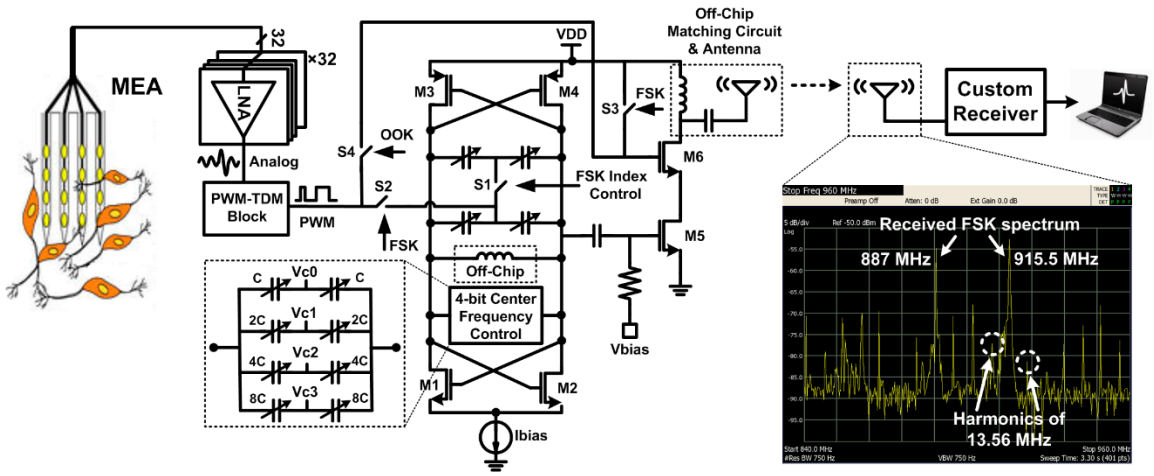


Fig. 2.4. WINeR-6 neural signal flow diagram with emphasis on the transmitter SoC.

2.1.3. Simulation and Measurement Results

The WINeR-6 SoC was fabricated using the ON Semiconductor 0.5-µm 3-metal 2-poly standard CMOS process. A micrograph and floorplan of the chip, which occupies 4.9 × 3.3 mm^2 of silicon area including the padframe, are shown in Fig. 2.5.

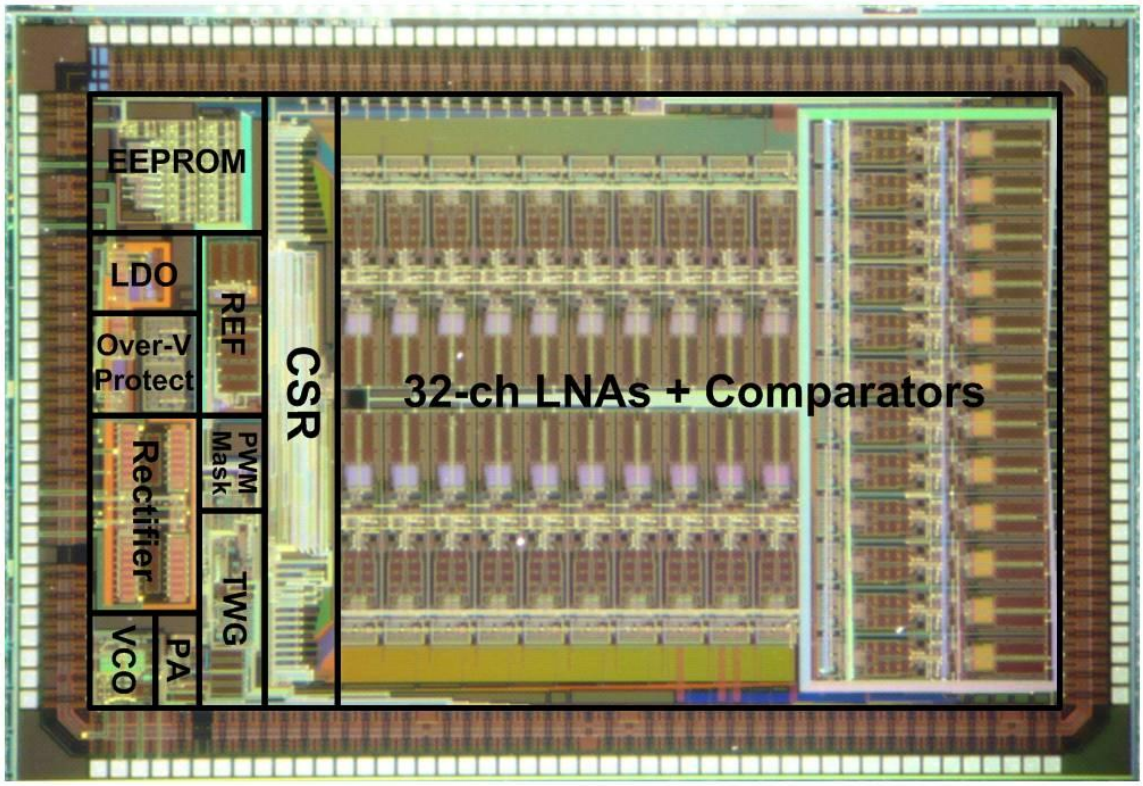
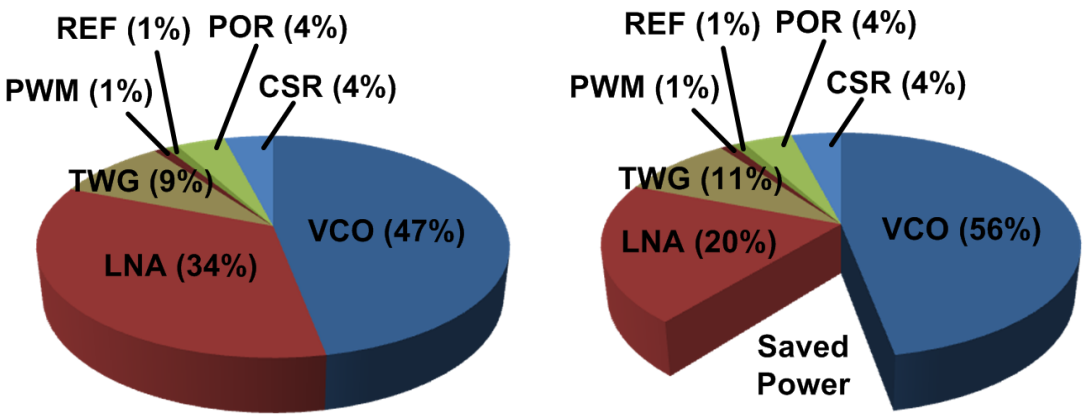


Fig. 2.5. Die photomicrograph of the 32-ch WINeR-6 SoC fabricated using the ON semiconductor 0.5-µm 3M2P std. CMOS process (size: 4.9 × 3.3 mm^2).

2.1.3.1. Power-scheduling measurements

The power consumption of the WINeR-6 with and without power scheduling are compared in Fig. 2.6. When all LNAs are active, the WINeR-6 consumes 7.05 mW from ±1.5 V supplies. On the other hand, when 12 LNAs (N = 12) are on at a time and the other 20 are in the sleep mode under power scheduling, the power consumption drops by 17% to 5.85 mW. From a different perspective, as depicted in Fig. 2.6, with power scheduling, the share of the LNA block power consumption in the total power consumption decreases from 34% to 20%. Obviously this power saving become even more significant by decreasing N. However, if $N < f_S t_T$, the LNA outputs will be sampled before they reach their operational values, which may cause distortion.



(a) (b)

Fig. 2.6. Comparison between the power consumption of each block in the WINeR-6 SoC as the percentage of the total power with and without power scheduling, which results in a 17% reduction in the total power consumption: (a) without power scheduling 7.05 mW and (b) with power scheduling 5.85 mW.

To evaluate the effect of power scheduling on the quality of the recorded signals, artificial spikes were applied with a 0.5 mV amplitude and 1 ms pulse width to the LNAs inputs and compared the recorded signals with and without power scheduling. The measured waveforms are shown in Fig. 2.7, in which the sampling rate is set to 18 kSps per channel and N = 12. The upper two waveforms show the LNA inputs. In the 3rd row, the black trace shows the output signal without using power scheduling, and the blue trace shows the output signal with power scheduling. Even though the LNA output seems to be noisy with power scheduling, because the LNA output reaches its operational value by the time each sample is taken, the effect of this noise on the digitized signal will be negligible. The last row shows the reconstructed signals from the digitized samples. The correlation coefficient between the two reconstructed signals was measured to be 0.97, which demonstrates almost a perfect match between the two conditions.

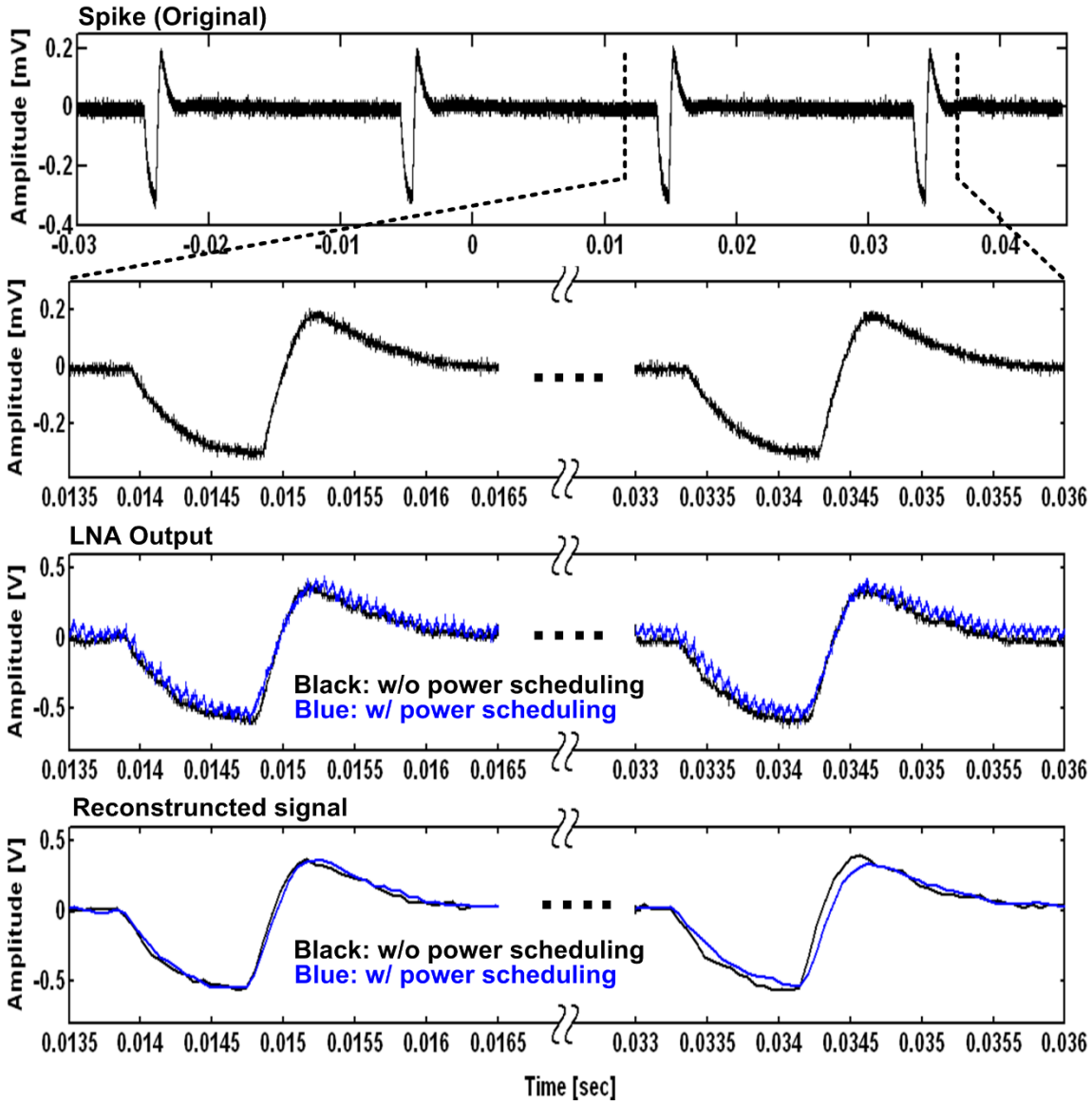


Fig. 2.7. Measured waveforms from top: original artificial spike waveform, magnified spike waveform, waveforms recorded at the LNA output with (blue) and without (black) power scheduling, reconstructed signal in the PC.

2.2. Receiver and Computer Interface

2.2.1. Rx Design

Resolution of the TDM-PWM based WINeR-6 system is determined by the accuracy of the recovered pulse width. Higher Rx bandwidth corresponds with sharper pulse edges and lower pulse width error [46]. Thus, the WINeR-6 Rx needs high enough bandwidth to receive the FSK-TDM-PWM signal while providing an adequate resolution

of more than 8 bits. Most commercially available ISM-band FSK receivers only provide up to 600 kHz bandwidth [51], which is far below what is required for a neural recording system with data volume in the order of 10 Mbps. Hence, a custom-designed Rx with 18 MHz bandwidth using commercially available off-the-shelf (COTS) components was implemented.

The WINeR-6 Rx block diagram, shown in Fig. 2.8, has four major modules in addition to the antennas: RF front end, analog signal conditioning, FPGA including USB 2.0 interface, and digital- to-analog converter (DAC).

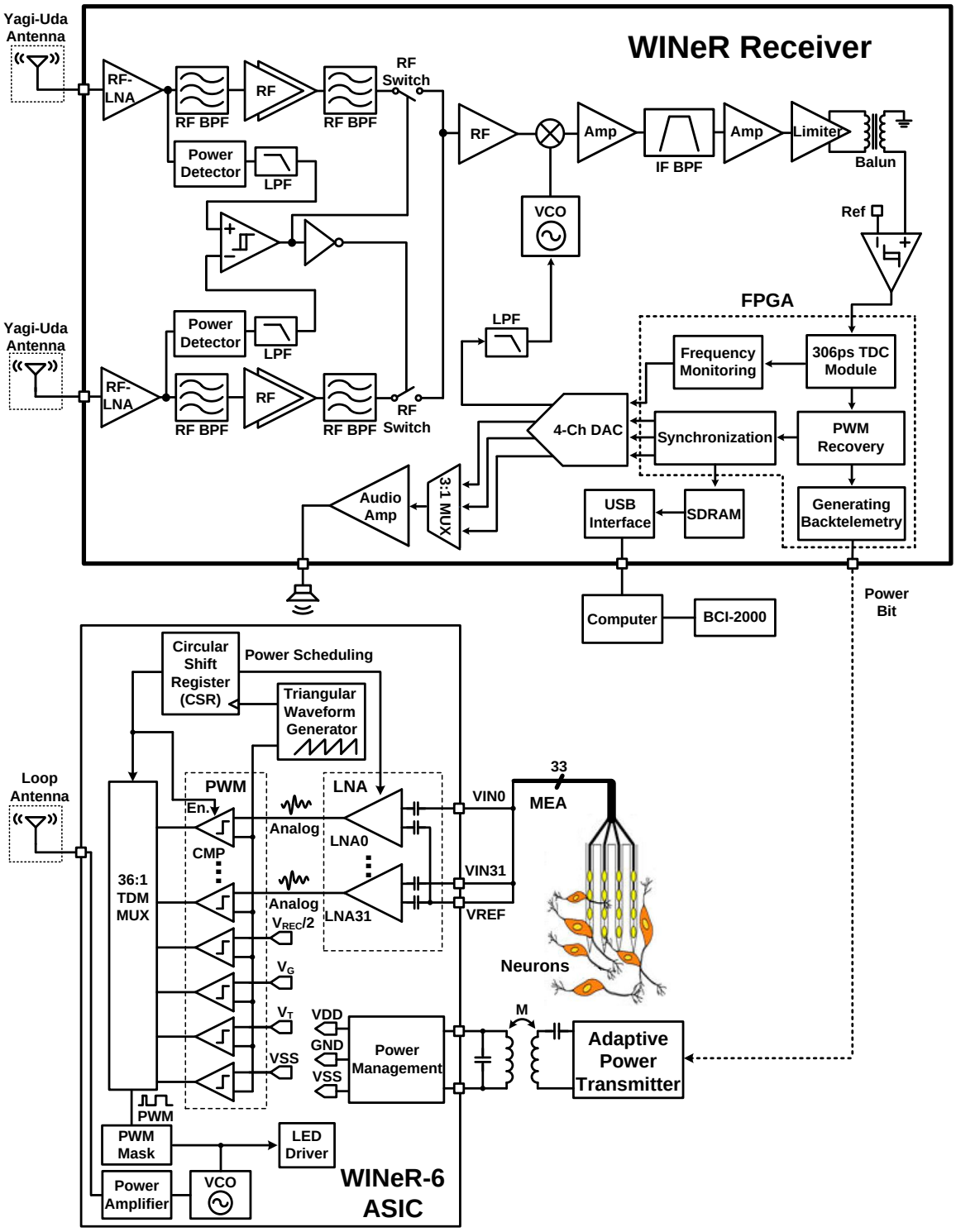


Fig. 2.8. Block diagram of the entire wireless implantable neural recording (WINeR-6) system: Rx (top) and Tx (bottom).

2.2.1.1. Yagi-Uda antenna

Like other implantable medical devices (IMD), WINeR-6 Tx has a limited power budget for RF transmission to keep its overall power consumption down. At the same time, it was desired to provide coverage over large experimental arenas in the order of 2 × 2 m^2 without any blind spots. This specification required high Rx front-end sensitivity and high-gain Rx antennas. A Yagi-Uda antenna satisfies these requirements while offering wide bandwidth. Relatively high directivity of the Yagi-Uda antenna was mitigated by the inclusion of two antennas in each WINeR-6 Rx. A 3-element Yagi-Uda antenna was designed based on [52], as shown in Fig. 2.9.

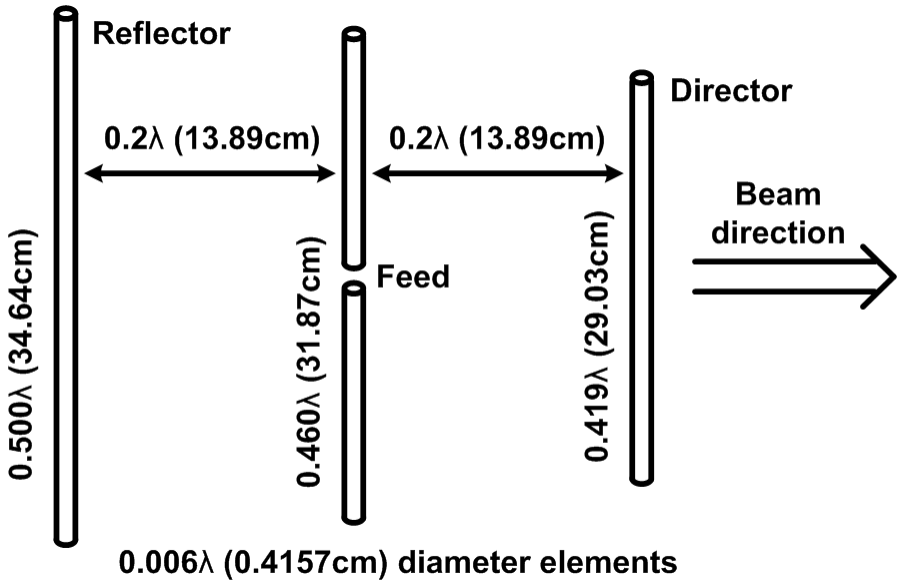


Fig. 2.9. Three-element Yagi-Uda dipole antenna designed for 433 MHz carrier.

2.2.1.2. RF front-end

In order to increase the wireless coverage of the experimental arena and eliminate blind spots, the Rx was equipped with two identical RF front-ends, each with its own antenna. As shown in Fig. 2.8, the FSK-TDM-PWM signal from the Tx was picked up by each antenna, and amplified/filtered independently through its parallel RF front-end.

Each path has an RF power detector (ADL5513), and depending on the strength of the received RF signal from each path, an RF switch connects the stronger one to the mixer. Depending on the size of the experimental arena, the wireless coverage can potentially be extended even further by increasing the number of antennas and parallel RF front-end paths.

Each RF front-end consists of an RF-LNA (MAX2640) with a gain and noise figure of 15.1 dB and 0.7 dB at 400 MHz, respectively, followed by a gain stage (BGA2712) that provides an additional 24 dB amplification. The RF front-end can provide up to 1.5 GHz bandwidth, while two passive third-order Chebyshev band-pass filters with 403-490 MHz bandwidth are placed before and after the gain stage to provide selectivity around the Tx signal and limit the out-of-band noise. The RF front-end thus provides 45 dB gain and 87 MHz bandwidth.

2.2.1.3. Analog signal conditioning

The amplified and filtered FSK signal is fed into a mixer, which is a 50 MHz to 1 GHz quadrature demodulator with 75 MHz bandwidth (AD8348). The mixer has a built-in variable gain amplifier (VGA) that provides −18.5 to +25.5 dB programmable gain. The VGA output drives two (I and Q) double-balanced Gilbert cell down-conversion mixers, which down-convert the RF signal to 43.5/56.5 MHz IF band. The IF-TDM-PWM signal is then further filtered and amplified in the baseband. To create a tunable local oscillator (LO) for the down-converter, a 720-1750 MHz VCO (V585ME41-LF) from Z-Comm (San Diego, CA) has been utilized. The LO frequency is divided by two inside the mixer, resulting in its ability to receive RF frequencies in 360-875 MHz range.

IF amplifiers and filters improve the SNR by eliminating the out-of-band interference. AD4899-1 amplifier was chosen for this block because of its 300 MHz unity gain bandwidth, ultra low distortion, and low noise. Three instances of this amplifier have been implemented with a total IF gain of 46 dB. In order to reject all adjacent channels'

interference, a band-pass filter (KR2850) from KR Electronics (Avenel, NJ, USA) has been included between the second and the third amplifiers. The filter has an 18 MHz bandwidth from 41-59 MHz and a 1 dB pass-band ripple.

The amplified and filtered IF-FSK signal is fed into a logarithmic limiting IF amplifier (AD8309) and a high speed comparator (TLV3501) with 4.5 ns delay. This stage recovers the rail-to-rail baseband FSK-TDM-PWM signal, which is then fed into an FPGA to be FM-demodulated in the digital domain to recover the TDM-PWM signal.

2.2.1.4. FPGA module

A COTS FPGA module, called Xylo-EM [53], was used, which includes an Altera FPGA (EP2C5T144C8), 2 MB of synchronous dynamic random access memory (SDRAM) for data buffering, and the USB interface circuitry.

2.2.1.4.1. FSK demodulation via TDC

A TDC in the FPGA demodulates the down-converted IF-FSK signal in the digital domain. The FPGA-based TDC block diagram is shown in Fig. 2.10. The IF-FSK signal is used as the clock signal for the 8-bit encoder and D-type flip-flops in the delay chain. A unit gate delay, τ, is the average time required for a rising or falling edge to propagate through a four-input AND gate. As a falling edge of the IF-FSK propagates through the chain of AND gates, the following rising edge saves a snapshot of the AND gate outputs in the rising edge-trigged D flip-flop register. Since the duration of a logic low is different in two FSK cycles at two different frequencies, the contents of the D flip-flop register at every rising edge of the IF-FSK can determine the period of that FSK half-cycle, ΔT. The 8-bit encoder then converts the contents of the D flip-flop register to an 8-bit value, C1[7:0] = $\Delta T/\tau$. The measured FSK pulse widths are accumulated in two separate registers, PWH and PWL, after comparing C1 with a programmable threshold value that discriminates between the two periods in the IF-FSK. The two frequencies in

the IF-FSK are 43.5 and 56.5 MHz, which correspond to ΔT of 11.5 ns and 8.8 ns, respectively. Considering τ = 304 ps in this FPGA, $\Delta T/\tau$ yields 38 and 29 delay cells for the low and high frequency half-cycles, respectively. To distinguish between these values, their average, 34, was used for as the FSK period threshold.

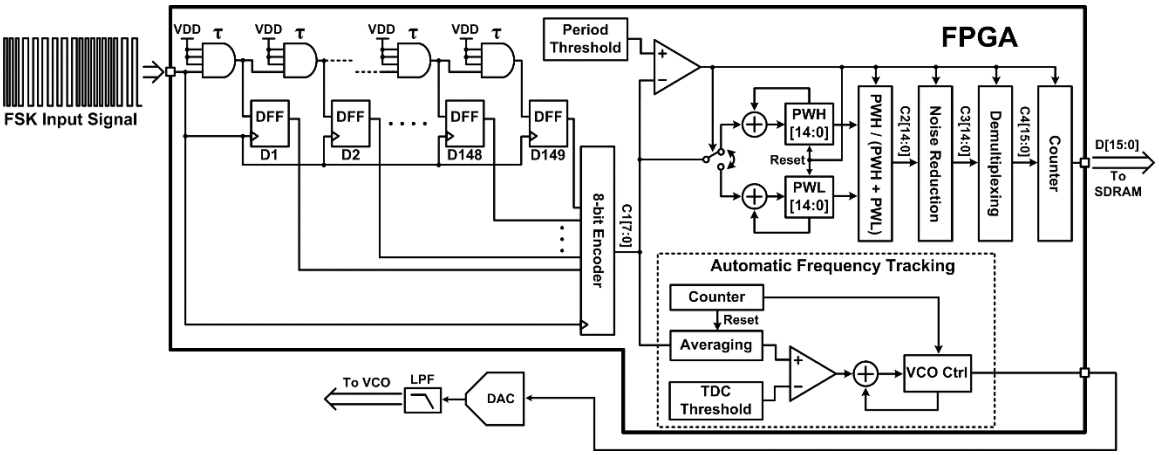


Fig. 2.10. The FPGA-based high resolution TDC, using a delay cell chain with τ = 304 ps and an automatic frequency tracking (AFT) block.

Although the absolute values of PWH and PWL vary with the instantaneous changes in the triangular waveform, the TDM- PWM duty cycle is relatively more stable and changes mainly with amplitude of the analog sample [46]. Thus C2[14:0] was calculated inside the FPGA from PWH/(PWH + PWL) of the recovered TDM-PWM signal as a normalized value within 0 and 1 that is proportional to the analog sample. C2 passes through a noise filtering block, which removes the pulse widths that are too small or too large to eliminate sharp glitches. The demultiplexing block that follows is designed to detect the marker created from four monitoring signals ($V_{REC}/2$, V_{BG}, V_T, and V_{SS}), which indicates the beginning of each TDM-PWM pulse frame. The pulse width following the monitoring signals is the sample taken from the first neural recording channel. In order to mark this channel for the BCI-2000, running on the computer, the demultiplexing block adds a flag to C3[14:0] as its most significant bit (MSB) such that

the MSB of the 16 bits digitized output, C4[15:0], would be "1" for the 1st channel and "0" for all other channels.

2.2.1.4.2. Automatic frequency tracking (AFT)

Frequency stabilization components, such as phase-locked loops (PLL) or crystals, were not used in the WINeR-6 Tx to reduce its size and power consumption [61]. As a result, the Tx carrier frequency varies with temperature, supply voltage, and to a lesser extent antenna loading variations. To compensate for these variations, digital automatic frequency tracking (AFT) function was implemented in the Rx. Following TDC, the AFT block averages 500 IF-FSK periods, which are available from C1[7:0]. The AFT tries to match the low-pass filtered carrier period from TDC with a programmable reference period by changing the local oscillator (LO) control voltage via a DAC. The AFT changes the LO frequency until the down converted IF-FSK spectrum is centered at 50 MHz.

2.2.1.4.3. Continuous high throughput USB interface

A USB 2.0 interface delivers a continuous stream of digitized neural data from WINeR-6 Rx to the computer in real time. A high speed EZ-USB chip (Cy7C68013A) was chosen for its high throughput, programmability, reliability, and ease of use. The data rate in the 32-ch WINeR-6 system is in the order of 10 Mbps for 640 kSps. When USB operates in the burst mode, the delays between successive USB data packets in the computer are quite unpredictable, varying from 100 µs to a few ms. To ensure continuous real time recording without data loss, a 2 MB SDRAM has been used between the TDC and the USB interface blocks to buffer the incoming data. The EZ-USB chip is set to operate in the slave-FIFO mode, controlled by a master module implemented in the Altera FPGA. The USB control module in the FPGA manages data transfers between the SDRAM and USB. It writes the 16-bit data created in the TDC module into the SDRAM

at the falling edge of every TDM-PWM pulse. In this module, the EZ-USB reads a 16-bit sample from the SDRAM into its internal 2056 Byte FIFO. Meanwhile, the EZ-USB chip continuously checks its own FIFO state, and when it is full, commits the data to the computer.

2.2.1.5. DAC module

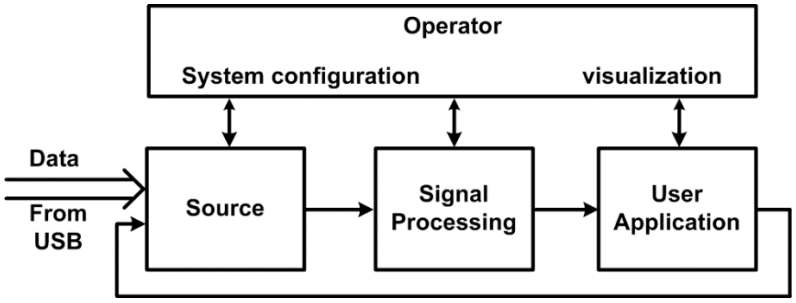
To assist users with visualizing and determining the quality of the incoming neural signals and to be compatible with some commercial hardwired neural recording back-ends, WINeR-6 Rx includes a 4-channel 16-bit DAC (AD5664R), which operates at 71.1 kSps. The clock, data, and enable signals for the DAC are generated by the same FPGA, which also allows users to select 3 out of 32 digitized and demultiplexed neural recording channels as inputs to the DAC. The DAC converts them into 3 analog signals that can be accessed independently through SMA connectors. In addition, one of these three analog signals can be selected and used to drive a 1 W audio amplifier with DC volume control (TDA7052A). The output of the audio amplifier drives an 8 Ω speaker, allowing users to identify the spike activity by how tit sounds. The first channel of the DAC is used in the AFC block, described in section 2.2.1.4.3.

2.2.1.6. Graphical user interface

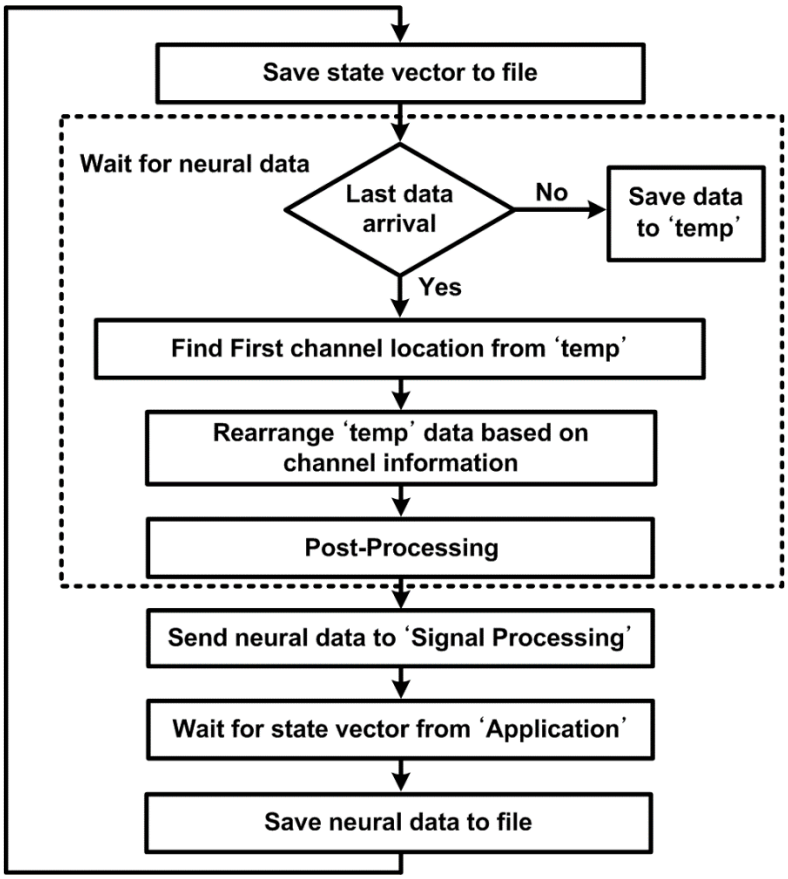
BCI-2000, an open-source piece of software for BCI research applications, displays the received neural signals on the GUI and saves them on the computer hard disk in real time [54]. It consists of four modules that communicate within each other, as shown in Fig. 2.11a. The “source” module receives data from the data acquisition device (WINeR-6 Rx), saves it, and sends it to the signal processing module. The “application” module is responsible for visualization on the computer screen. The source module has

been modified to continuously receive the neural data from WINeR-6 Rx through the USB port.

Fig. 2.11b shows the flowchart for data acquisition algorithm in the source module, which performs two important tasks. First, it detects the marker that indicates sampled data for the first channel and time division demultiplexes the rest of the incoming data accordingly. While the program is running, the module waits for a predefined amount of data to arrive by saving it in a temporary memory space before arranging the samples. Second, the source module applies a simple post-processing algorithm to compensate for some of the nonlinear characteristics of the ATC process on the Tx side. The TWG block in particular has nonlinear characteristics that can degrade the quality of the TDM-PWM signal. In a one-time calibration process, the nonlinear characteristics of the TWG block in each WINeR-6 ASIC can be measured and stored in the BCI-2000 to be applied to the incoming data from that ASIC before further signal processing.



(a)



(b)

Fig. 2.11. (a) The core modules and their interactions in the BCI-2000, (b) Data acquisition flowchart of the "Source" module.

2.2.2. Bench-Top Measurement Results

The RF, analog, and DAC modules of WINeR-6 Rx were implemented on separate custom-designed printed circuit boards (PCBs) for electromagnetic isolation and shielding, as shown in Fig. 2.12. They are carefully fitted in a 17.9 × 17.5 × 7.6 cm^3 aluminum enclosure along with the COTS FPGA module and SMA interconnects. The

WINeR-6 Rx consumes 80 mA and 290 mA from -5 V and 5 V supplies, respectively. The FPGA module is powered from the USB port. It has on-board 3.3 V and 5 V regulators, which also power the DAC module.

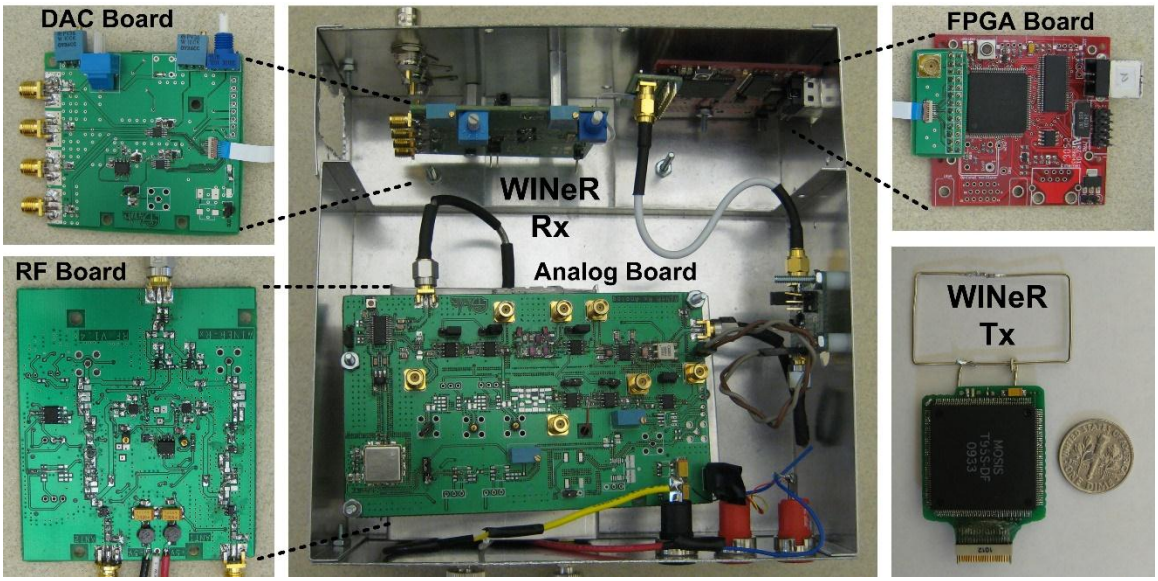


Fig. 2.12. WINeR-6 Rx and Tx hardware components.

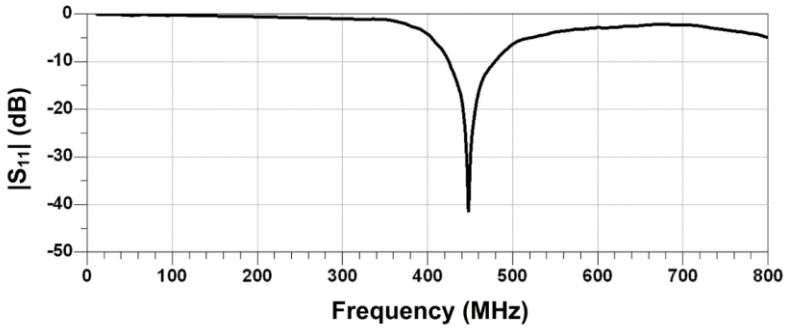
The delays measured at different taps along the 4-input AND gate delay chain indicate that $\tau \approx 304$ ps. Thus, $K = 66$ gates were needed for $1/\Delta T = 50$ MHz. Hence, a chain of delay cells with $N = 100$ elements was implemented, as shown in Fig. 2.9, to make sure that the total delay time was longer than the clock period.

2.2.2.1. Antennas

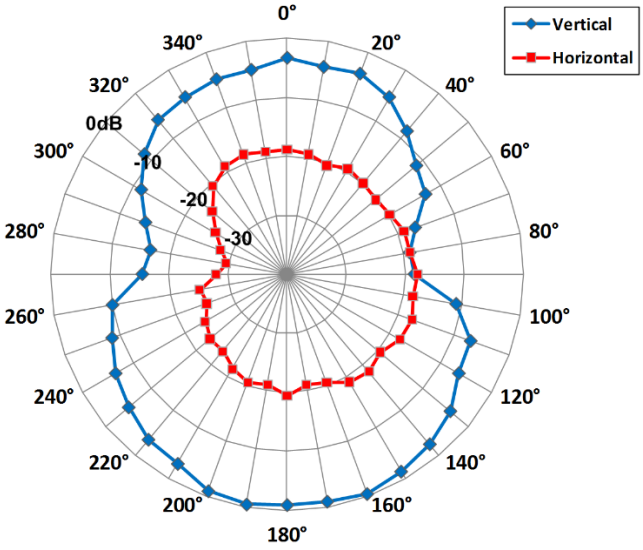
The WINeR-6 Rx was bench-top tested along with the three- element Yagi-Uda antennas, designed based on specifications in Fig. 2.9. Fig. 2.13a shows the measured return loss of the antennas. Considering the effect of baluns, the 10 dB return loss of the fabricated antennas shows 54 MHz bandwidth, over the 424-478 MHz frequency range.

A loop antenna (3.5×2 cm^2) was designed for the WINeR-6 Tx, as shown in the lower right panel in Fig. 2.12 [55]. The vertical and horizontal radiation patterns of the WINeR-6 Tx are shown in Fig. 2.13b, which were measured in an outdoor open space to

minimize external interference. The WINeR-6 Tx was placed in the center of the measurement area, and the received signal strength from the Yagi-Uda Rx antenna was measured at 1 m distance from the Tx. The Tx was manually rotated clockwise from 0° to 360° with 10° increments. Fig. 2.13b shows that the WINeR-6 Tx antenna has maximum signal variation of 25 dB.



(a)



(b)

Fig. 2.13. (a) Measured return loss of the Rx Yagi-Uda antenna. The -10 dB bandwidth was 54 MHz from 424 to 478 MHz frequency range. (b) Relative radiation patterns of WINeR-6 Tx at 433 MHz measured by the Rx antenna.

2.2.2.2. RF front-end

The S_{11} and S_{21} of the RF front-end have been measured and depicted in Fig. 2.14. The total RF gain for this block was 45 dB over 403-490 MHz range, which is matching in the center and slightly wider than the Yagi-Uda Rx antenna bandwidth.

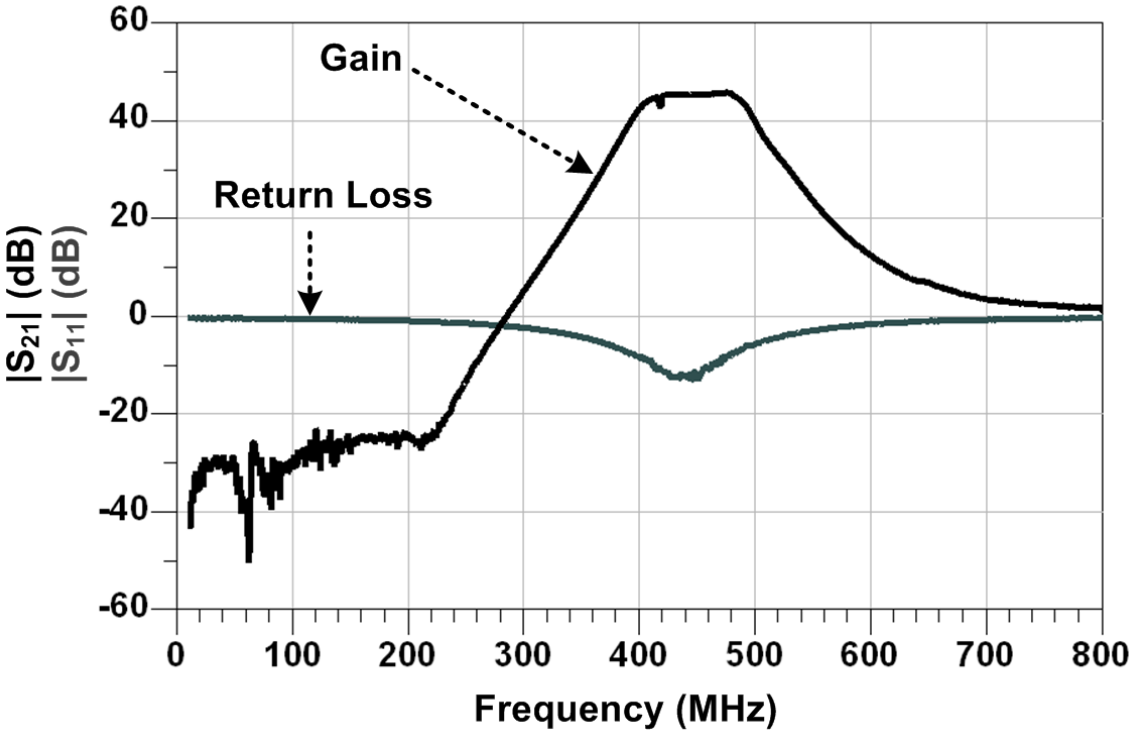


Fig. 2.14. Measured return loss and gain of the RF front-end (RF module).

2.2.2.3. Complete WINeR-6 Tx-Rx operation

To test the operation of the complete WINeR-6 system (Fig. 2.8) operation in a bench-top setting, an artificial spike waveform was played from a DAC (mp3 player), attenuated to 1 mV peak amplitude, and applied to all 32 input channels. The input signal was then amplified and filtered by the LNA block with 67.8 dB gain and 1 Hz - 8 kHz bandwidth. The triangular waveform generator (TWG) output signal was adjusted at ±1.4 V and 640 kHz, setting the overall sampling rate of the WINeR-6 system. The TDM-PWM block compared the 32 LNA outputs and 4 monitoring signals with the TWG

output, and the MUX organized the resulting PWM samples into frames of 36 pulses. In order to make sure the TDM-PWM pulses were detectable on the Rx side, i.e. they were neither too narrow nor too wide, when the input was below -1.1 V or above 1.3 V, the ATC pulse width was kept constant by the PWM mask. This signal drove the on-chip MOS varactor of the hybrid LC-VCO, running at 428/441 MHz in the FSK mode.

The transmitted FSK-TDM-PWM carrier was picked up 1.5 m away from the WINeR-6 Tx by the Rx antenna. In the FPGA, the down-converted signal was FSK demodulated and digitized via TDC to 16-bit samples, which were buffered in the SDRAM and delivered to a computer through its USB port. Three out of the 36 channels were further converted to analog signals in the DAC module. The upper and lower traces in Fig. 2.15 are the LNA output on the Tx side and the corresponding DAC output on the Rx side for the same channel, respectively. The measured WINeR-6 latency from the LNA output of the Tx to the Rx DAC output was ~1 µs.

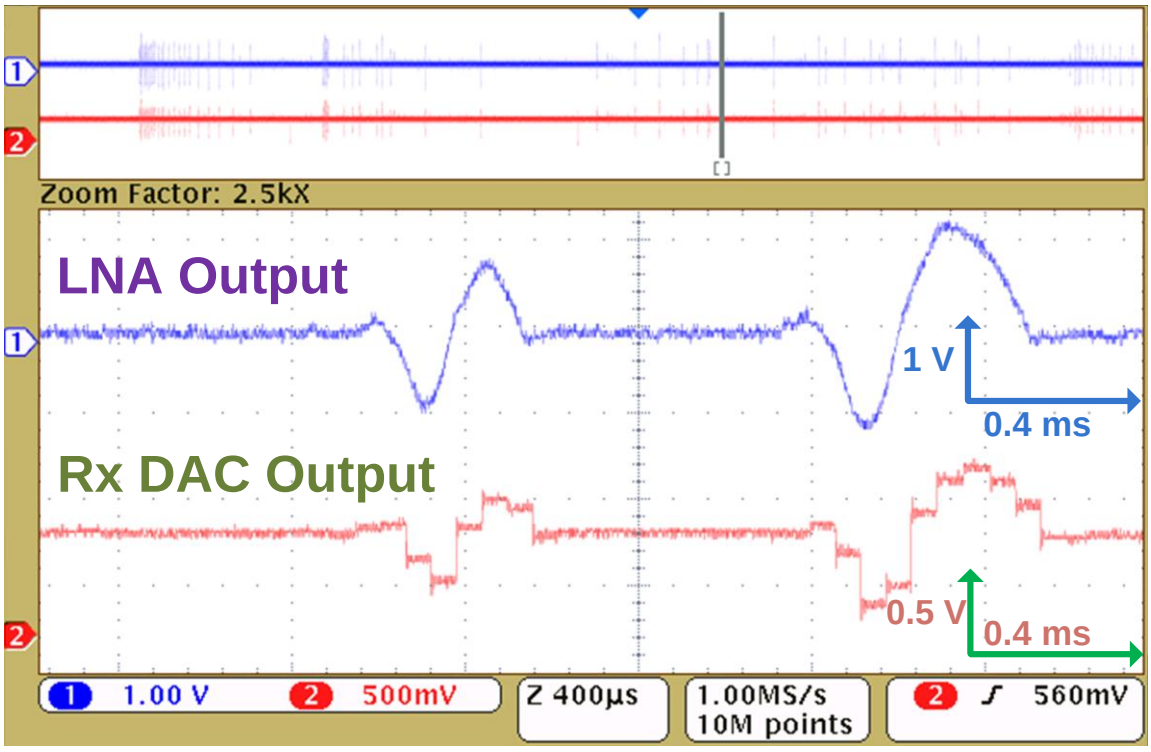


Fig. 2.15. Top trace: One of the LNA outputs on the WINeR-6 Tx when a pre- recorded neural signal with 1 mV spikes was applied to the input. Bottom trace: DAC output on the WINeR-6 Rx for the same channel at 1.5 m away.

Using the above setup and bypassing the LNA block, the integral nonlinearity (INL) and differential nonlinearity (DNL) of the rest of WINeR-6 were measured as a wireless data acquisition system, combining ATC and TDC on the Tx and Rx sides, respectively. In this measurement, a constant voltage, generated by an Agilent 33250A function generator with 12-bit resolution was applied to the LNA output of ch-12. By varying the DC input from rail to rail, ±1.5 V, the increments in the 16-bit digitized value from the same channel were recorded on the Rx side, which was located 1.5 m from the Tx. Considering the PWM mask, a window between -1.1 V and 1.3 V was selected to measure the DNL and INL, and the LSB size was set to 9.4 mV for 8 bit resolution. Fig. 2.16 shows the measured DNL and INL for the WINeR-6 prototype, which were within (-0.364, +0.444) LSB and (-0.468, +0.226) LSB, respectively.

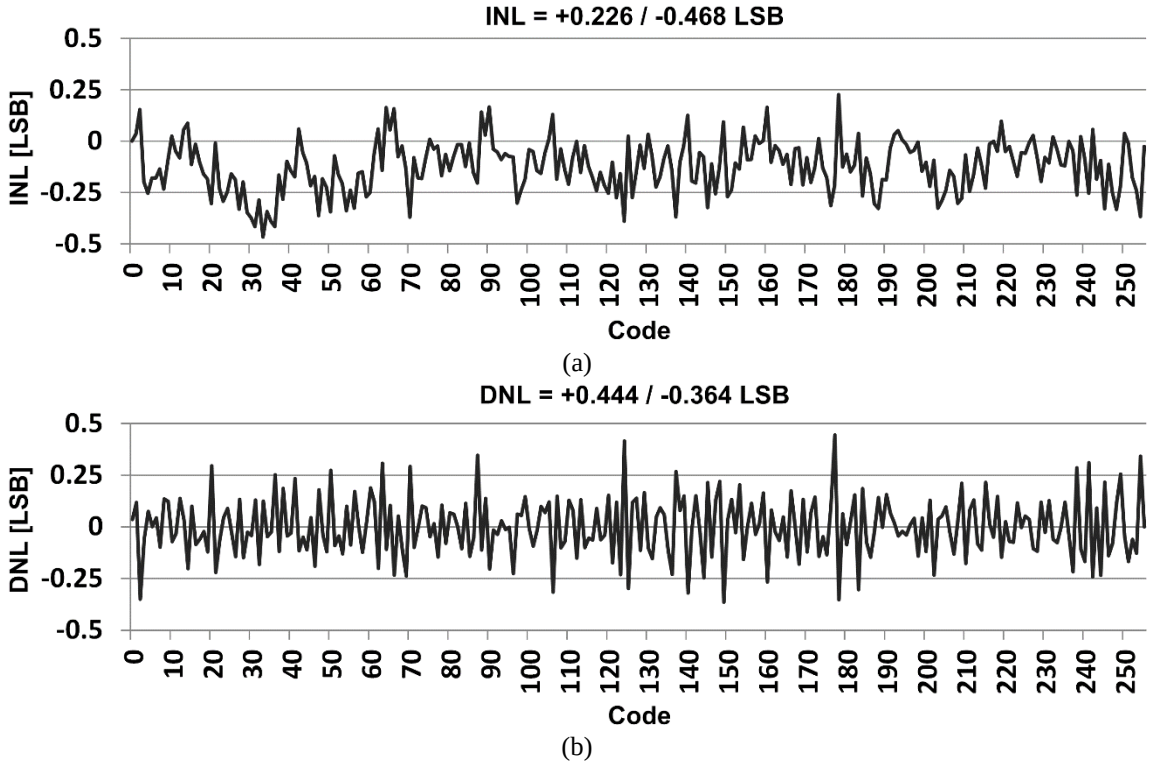
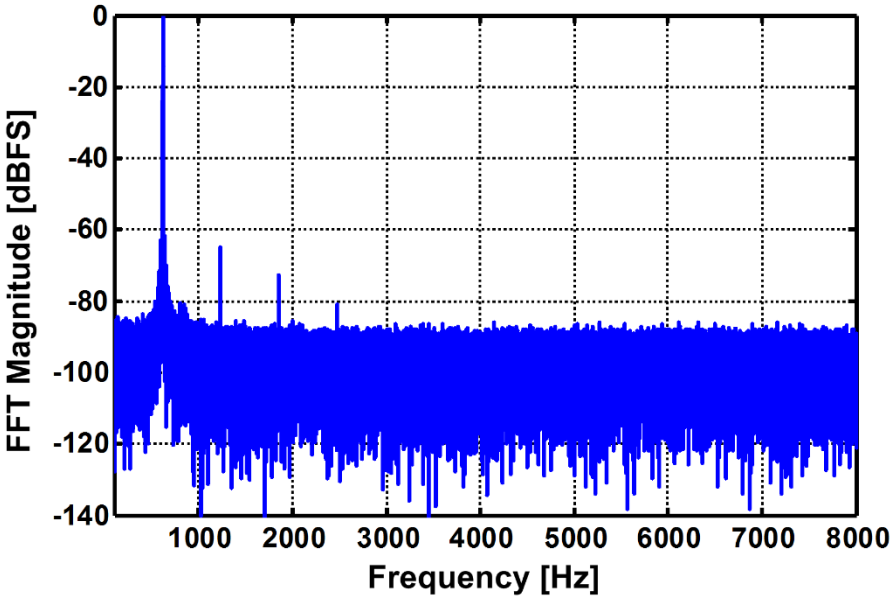
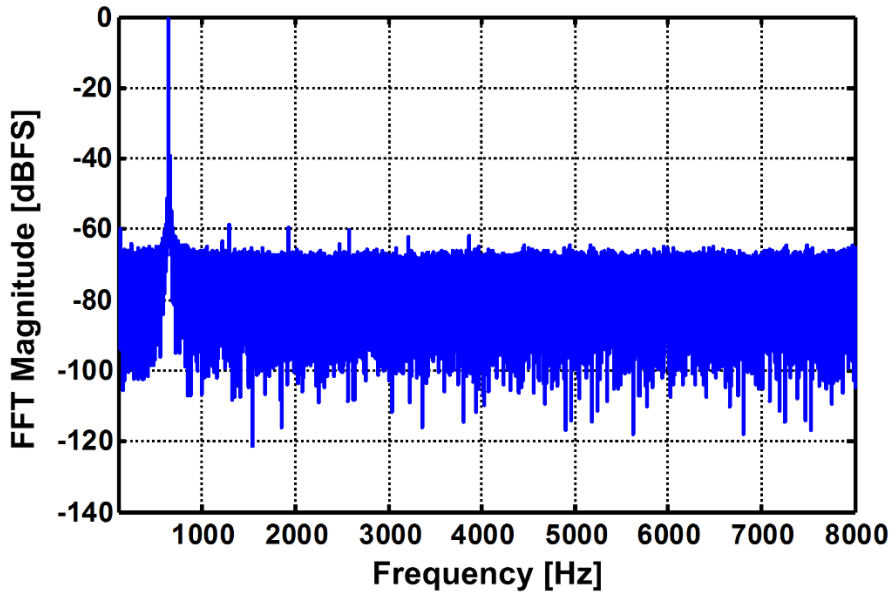


Fig. 2.16. (a) INL and (b) DNL measurements for the entire WINeR-6 system at the Tx-Rx distance of 150 cm.

In addition to the INL and DNL, a tone test was conducted by applying a 600 Hz sinusoidal waveform to ch-12 LNA output. The test results in Fig. 2.17 show a spurious-free dynamic range (SFDR) of 64.95 dB with a hardwired link. With a wireless link at 150 cm Tx-Rx separation, the SFDR was 58.86 dB. This measurement indicates that linearity performance of WINeR-6 has decreased by 6.1 dB because of the 150 cm wireless link.



(a)



(b)

Fig. 2.17. Tone test measurements of the WINeR-6 system (a) without wireless link, (b) at the Tx-Rx distance of 150 cm.

2.2.2.4. WINeR-6 noise performance

To analyze the noise contribution from different WINeR-6 blocks, noise measurement was performed in an unshielded laboratory environment in several

configurations shown in Fig. 2.18. In each case, a fast Fourier transform was applied on 20 s of the recorded signal in the computer to derive its spectrum and refer it back to the input. Fig. 2.18a shows the TDC noise measurement setup. Here a series of pulses with 50% duty cycle were generated by a function generator and fed into the TDC block in the FPGA. It was expected that the TDC noise is very small, but it should be noted that the measurement included the function generator phase noise as well, which was considered negligible. In Fig. 2.18b the LNA outputs are forced to ground to cancel the LNA noise. Noise of the wireless link has also been bypassed by directly connecting the TDM-PWM signal from Tx to the TDC input on the Rx side through a high-speed digital isolator (ISO721). The setup in Fig. 2.18c is similar to the one in Fig. 2.18b except for the fact that the LNA noise has been included by grounding the LNA inputs. Finally, Fig. 2.18d shows the noise measurement setup for the entire WINeR-6 system. In all noise measurements, the LNA bandwidth was set to 200 Hz to 8 kHz, while the input referred noise was integrated over a wider range from 1 Hz to 10 kHz.

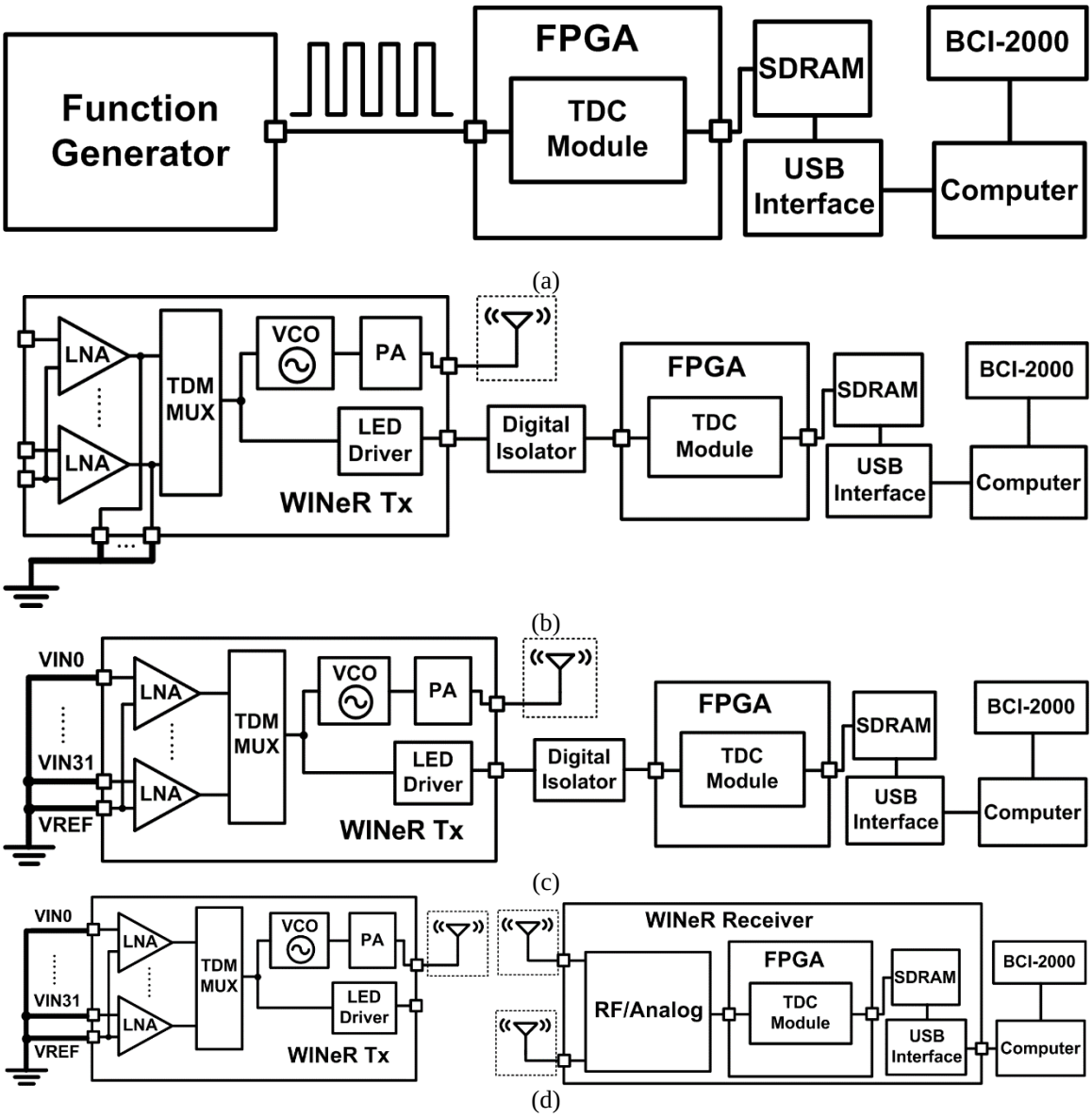


Fig. 2.18. Various noise measurement configurations to find out the contribution of each major WINeR-6 component: (a) TDC noise, (b) ATC + TDC noise without wireless link, (c) LNA + ATC + TDC noise without wireless link, (d) Noise of the entire system.

Using the setup in Fig. 2.18d (i.e. the entire system), the Tx-Rx distance was swept from 30 cm to 210 cm to observe the effect of Tx-Rx separation on the noise of the wireless link without shielding. The input referred noise amplitudes for these measurements are shown in Figs. 2.19 and 2.20. According to these graphs and our theoretical analysis in [46], the noise from the wireless Rx is obviously the dominant noise source for the current 32-ch WINeR-6 system prototype, especially at large Tx-Rx

separation. At the nominal Tx-Rx distance of 1.5 m, the effective number of bits (ENOB) is 8 bits considering the INL and DNL measurements in Fig. 2.16. In addition, the measured Rx sensitivity was -65 dBm. Table 2.1 summarizes the key measured specifications of the entire WINeR-6 system.

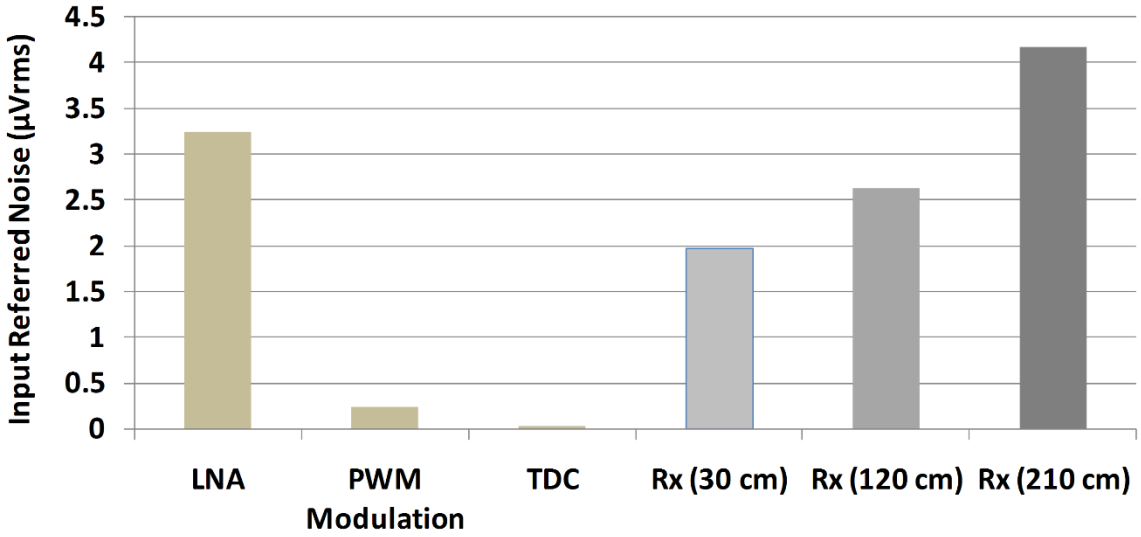


Fig. 2.19. Noise contributions of different WINeR-6 blocks at 640 kSps.

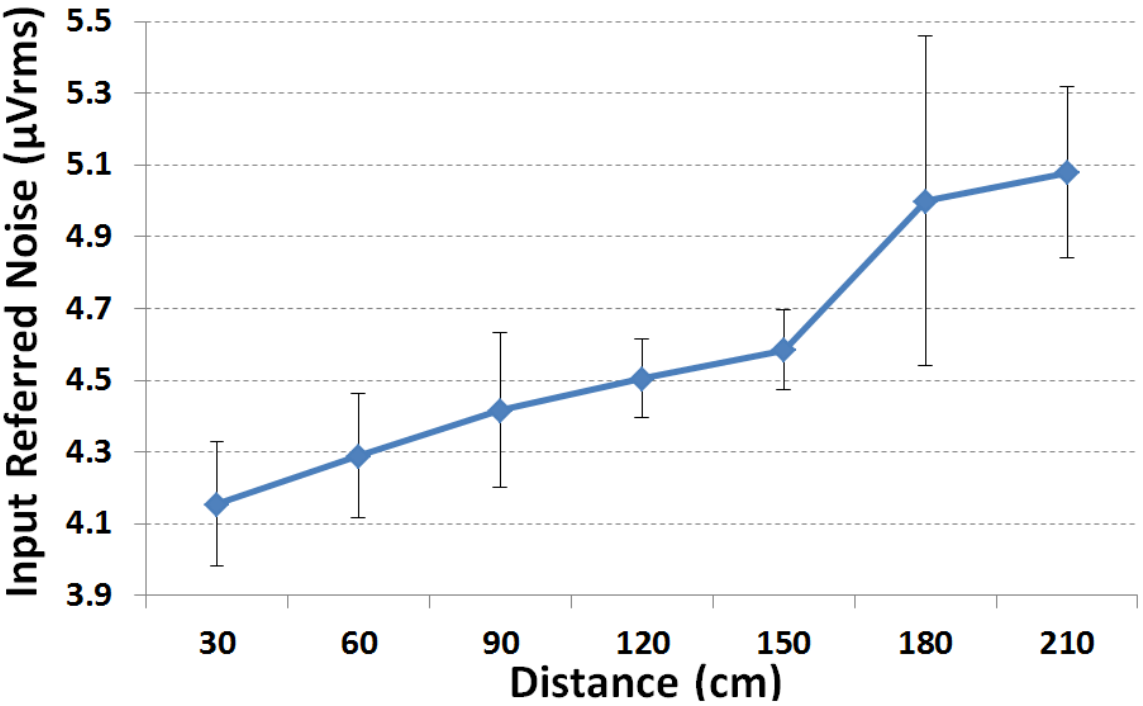


Fig. 2.20. Noise measurement of the entire WINeR-6 vs. Tx-Rx distance.

Table 2.1: Summary of the WINeR-6 system specifications.

WINeR-6 Tx ASIC	
Fabrication technology	0.5-µm Std. CMOS
Number of channels	32 + 4 feedback
Die size (mm^2)	4.93 × 3.33
Supply voltage (V)	±1.5
Total power consumption at -14 dBm RF output power (mW)	15
Sampling rate from all channels (kSps)	58 - 709
FSK carrier frequency (MHz)	428/441
WINeR Rx	
Supply voltage (V)	±5
Current consumption (mA)	290 (+5 V), 80 (-5 V)
Size (cm^3)	17.9 × 17.5 × 7.6
Bandwidth (MHz)	18
Center frequency (MHz)	433 MHz
Sensitivity (dBm)	-65
Tuning range (MHz)	28 (419 - 447)
Nominal Tx-Rx antenna distance (m)	1.5
Max. Tx-Rx antenna distance (m)	4.2
Neural Recording	
Sampling rate/ch (kSps)	1.6 - 19.7
LNA gain (dB)	67.8 / 78
LNA input referred noise (μV_{rms}) (BW: 200 Hz - 8 kHz)	3.25
System input referred noise (μV_{rms}) (BW: 200 Hz - 8 kHz, Distance: 1.5 m)	4.58
System resolution (ENOB)	8
PC Interface	USB 2.0 (480 Mbps Max)
Graphical user interface	BCI 2000 (Open source)

2.3. Animal Experiments

2.3.1. Wideband Neural Recording for Seizure Detection

The WINeR-6 system was used with the AFE bandwidth adjusted to 1 Hz - 8 kHz to record the neural activity of a male Sprague-Dawley rat whose dorsal hippocampus was injected with tetanus toxin (TT). A 16-channel (2×8) multi electrode array (MEA) was also implanted with one row in the CA3 and the other in CA1. High frequency oscillations (HFO), which are considered emerging biomarkers for epileptic seizures, were recorded with the WINeR-6 system and compared with recordings from a custom

hardwired system with commercial components, as described in [56]. The hard-wired system bandwidth was set to 1 - 500 Hz for local field potentials (LFP). The recorded neural waveforms at different times are compared in Fig. 2.21. Because of its wide bandwidth, the WINeR recording shows both HFO and LFP recordings.

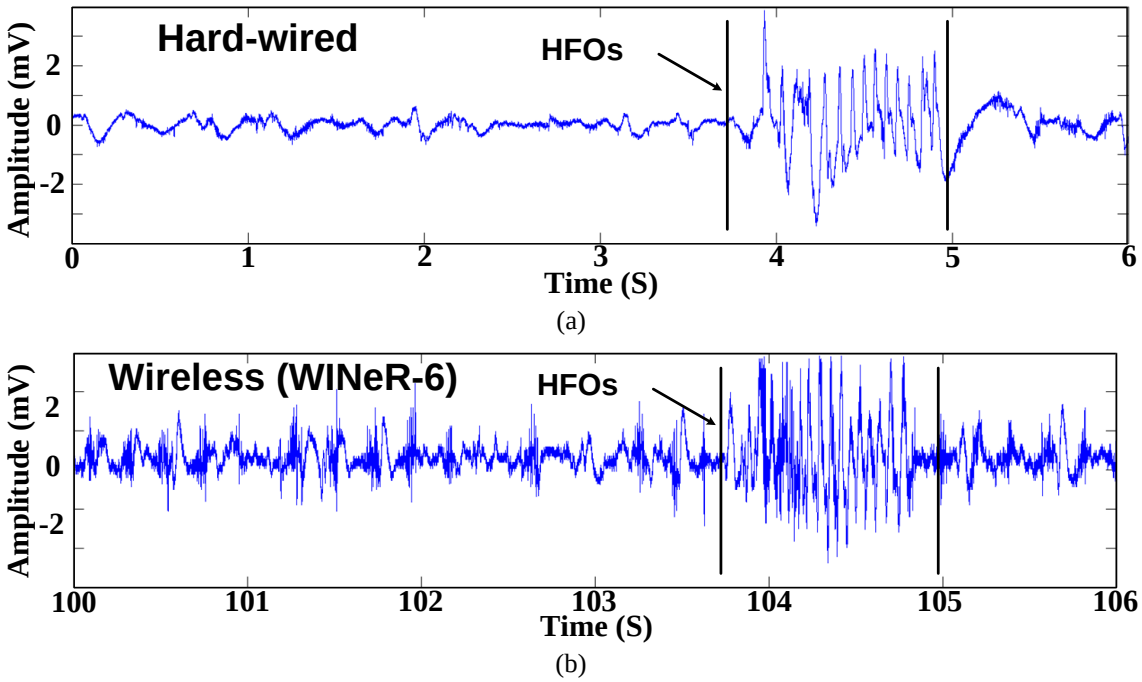


Fig. 2.21. Epilepsy detection by LFP recording from (a) hard-wired system and (b) the WINeR-6 (The author thanks Dr. S. Desai for helping this animal experiment).

2.3.2. Single Unit Recording for Behavioral Experiments

To further evaluate the performance of the WINeR-6 system, its overall performance was compared to that of a commercial hardwired system, based on NSpike [57], in a meaningful behavioral neuroscience experiment, in which action potentials were recorded from hippocampal pyramidal neurons of a rat as it completed laps on a relatively large circular track (~1 m^2). The subject was a 15-month-old male Long-Evans rat, weighing approximately 550 g. This set of experiments was conducted with approvals from the Institutional Animal Care and Use Committees (IACUC) at the Georgia Institute of Technology and Emory University.

The rat was implanted with a chronic recording assembly that contained 32 tetrodes (bundle of four electrodes) targeted at the dorsal hippocampus. Further details can be found in [58], [59]. The electrodes were connected to four 36-pin male Nano connectors from Omnetics (Minneapolis, MN). In each of the four connectors, 4 lateral pins were used for grounding and reference, and the other 32 were connected to 8 out of 32 tetrodes. The WINeR-6 analog front-end (AFE) bandwidth for this experiment was set to 400 Hz-8 kHz with a total gain of 8000 for recording single-neuron action potentials, similar to the settings for the NSpike system. The experiment was carried out in a circular track with an outer diameter of 91.4 cm and width of 7.6 cm, as shown in Fig. 2.22, which was setup in a small shielded cubicle. During the test, the rat completed two sessions of 40 laps each, in which video and neural data were recorded with both systems. The rat was rewarded for completing each lap with a small piece of chocolate.

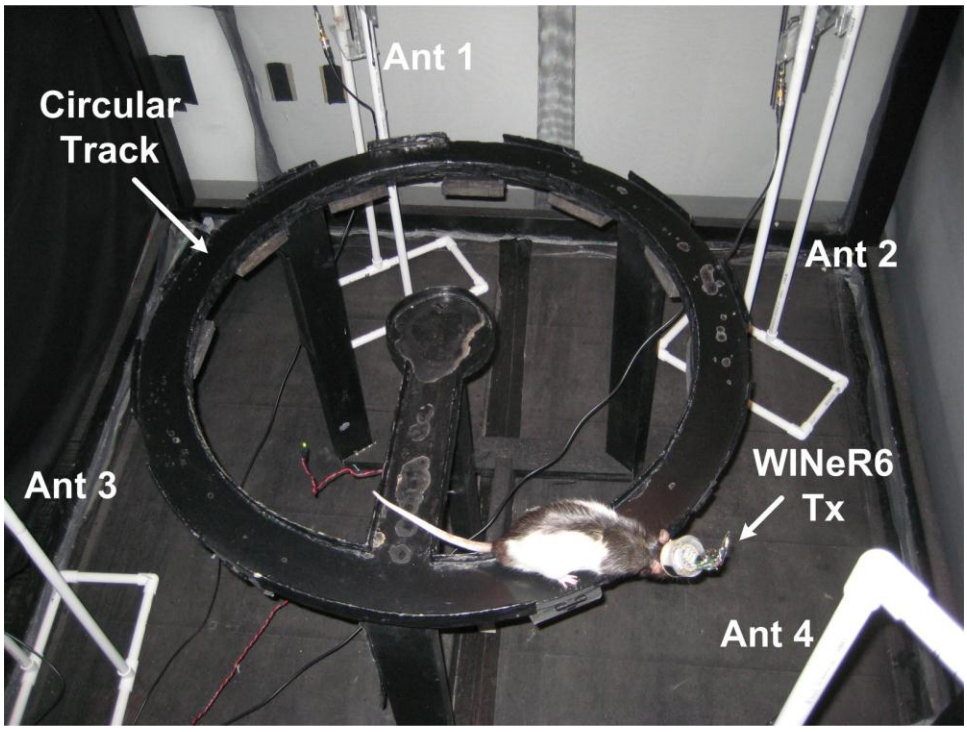


Fig. 2.22. Awake freely behaving animal experimental setup. The rat completed two sets of 40 laps on a circular track with an outer diameter of ~1 m, while neural signals were recorded simultaneously from 32 channels using the WINeR-6 and a hardwired setup. The quality of the recorded neural signals was observed in real time, but single-unit activities were classified offline and used to construct the place fields in each case after synchronizing and combining the neural activity with the animal position from the recorded video (The author acknowledges F. Getaneh in the Manns lab for helping this animal experiment).

To provide sufficient wireless coverage, four antennas from two WINeR-6 receivers were mounted on stands made of PVC pipes, and positioned roughly at 3, 6, 9, and 12 o'clock slightly above the circular track in order not to miss any neural signal during the experiment due to fading. The two WINeR-6 Rxs and associated computers were placed outside the cubicle.

Fig. 2.23 shows the operating diagram of the dual-Rx solution. When two receivers record the same neural signals from a single WINeR-6 Tx, the data needs to be synchronized by indicating the same marker signals in both recorded data streams. For this purpose, a predefined marker was generated in the master FPGA when a push button was pressed. This marker signal was then transferred to the master BCI-2000, and easily distinguished from the digitized neural signals. A similar marker signal was generated in the slave FPGA at the same time and sent to the slave BCI-2000. Fig. 2.24 shows a snapshot of 32 neural recording channels that was shown in real time on one of the two BCI-2000 GUIs. A similar WINeR-6 configuration could be used to simultaneously record neural signals from multiple animal subjects in the same experimental arena in a socially-relevant context, provided that their Tx-Rx pairs were tuned at different center frequencies.

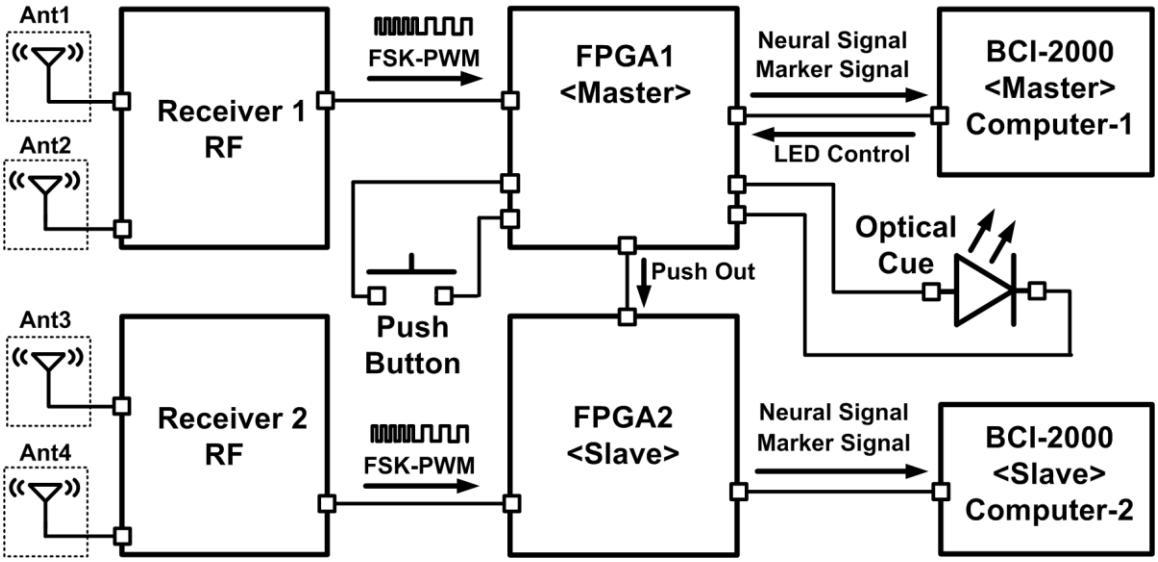


Fig. 2.23. Synchronization between two WINeR-6 Rxs, each of which has two antennas, with a push button as well as a video stream, using an optical cue.

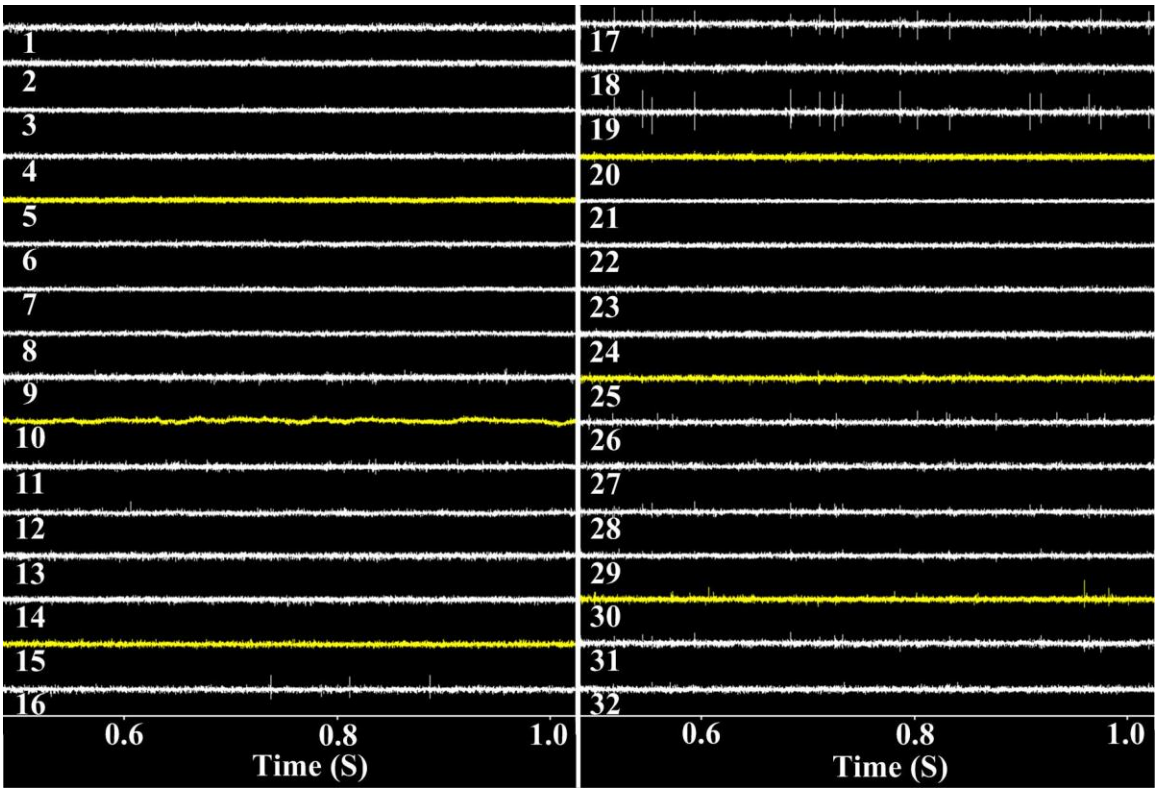
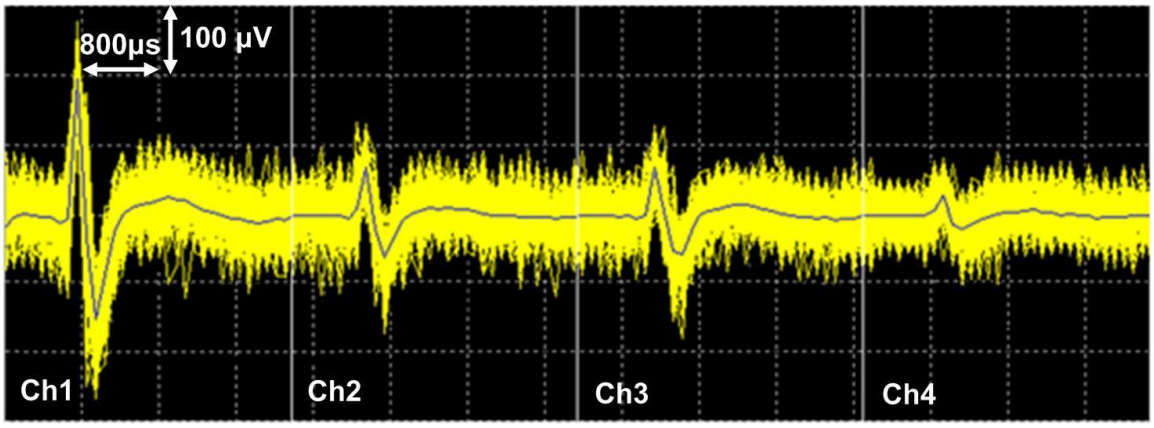


Fig. 2.24. Time domain representation of 32-ch recorded signals in real time using the BCI2000 GUI.

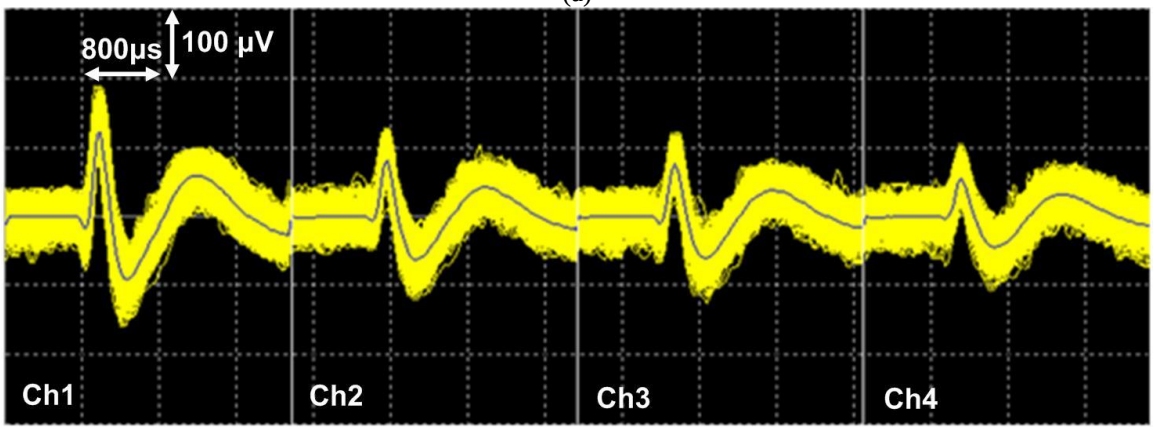
The exact same experiment was repeated with the same animal and the same electrode positions using the hardwired NSpike system, which sampling rate, gain, and

bandwidth were adjusted to be very close to that of the WINeR-6 system. A video camera was mounted above the track to record the rat position in synchrony with the neural recording. The video frames were synchronized with the neural data from WINeR-6 by flashing the LED, shown in Fig. 2.23, as an optical cue.

After completion of the data recording phase, spike classification was conducted on both wireless and hardwired datasets using the Offline Sorter software from Plexon (Dallas, TX) in order to isolate activity from individual neurons. Figs. 2.25a and 2.25b show spike waveforms across four channels (wires) of the same tetrode, activity from what was thought to be the same pyramidal neuron recorded during the WINeR-6 (wireless) and NSpike (hardwired) sessions, respectively. After classifying putative single neurons, the spike firing location for the best-isolated units were marked on the circular track by synchronizing the timing of the spiking activity with the rat location on the recorded video data.



(a)

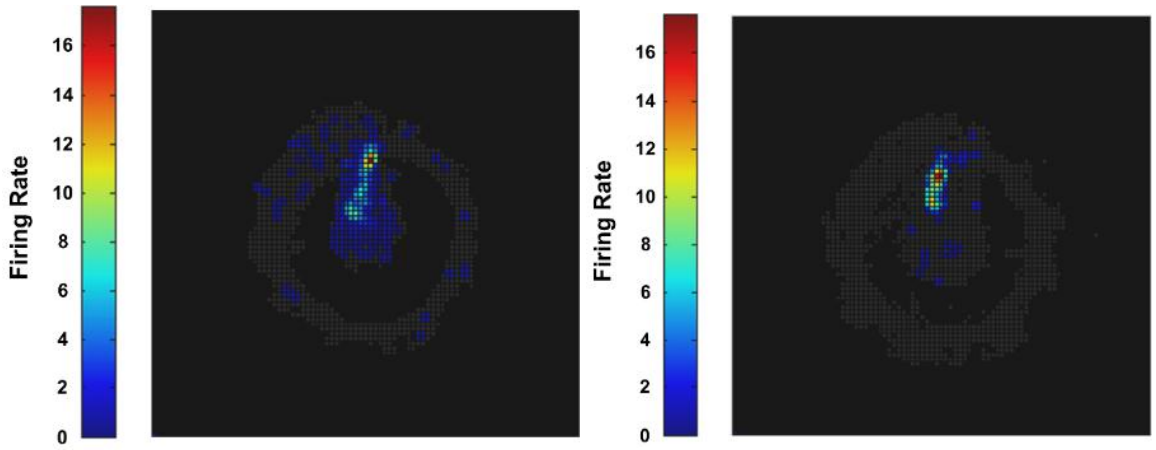


(b)

Fig. 2.25. Spike classification of 4 individual channels in Tetrode 5 from (a) WINeR-6 and (b) NSpike systems using Plexon's Offline Sorter.

Many pyramidal neurons in the dorsal rat hippocampus, termed place-cells, show location-specific activity, and the location at which the greatest firing rate of an individual neuron occurs is often referred to as its place field [60]. Fig. 2.26 shows a place field plot for a place-cell recorded during both recording sessions. Brighter colors indicate a higher firing rate, and grey colors show the overlapping trajectories of the rat as it completed laps on the circular track. Based on the similar spatial selectivity of the place fields in both plots and similar firing rates, the results suggest that the WINeR-6 wirelessly recorded data is similar to that of the hardwired recording setup (gold standard) in an experiment with a rat freely behaving in a 1 m^2 arena. The results illustrate the feasibility of the WINeR-6 system as a substitute for hardwired systems in behavioral neuroscience experiments. The lower SNR of the WINeR-6 system, which is also

noticeable in Fig. 2.25 classified single- neuron waveforms, has resulted in lower concentration of the place-cell firing around the peak in Fig. 2.26.



(a) (b)

Fig. 2.26. Comparison between place fields resulted from (a) WINeR-6 wireless and (b) NSpike hardwired recordings.

CHAPTER III

DUAL-SLOPE CHARGE SAMPLING ANALOG FRONT-END

3.1. Introduction

A conventional AFE architecture consists of several voltage gain stages and filters. The signal is buffered and multiplexed before a sample-and-hold (SHA) and digitized using a low-power, medium-resolution analog-to-digital converter (ADC). According to the analysis in [62], conventional AFEs consume an increasing amount of power in the buffer and ADC blocks as the number of channels increase because the conversion per channel must be completed in a short period of time.

A dual-slope charge sampling (DSCS) architecture is presented to improve the power efficiency of the AFE for multichannel neural recording systems. A charge sampling mechanism was recently employed in neural recording interfaces because it is stronger than voltage sampling in terms of wideband operation and provides an inherent pre-filtering function by integration [16],[63],[64]. The proposed DSCS-AFE architecture exploits the benefits of charge sampling while converting input signals to PWM pulses, which eliminates the need for high-speed ADCs on the transmitter unit (Fig. 3.1). These features make the proposed DSCS-AFE architecture a suitable choice for large channel count systems with limited available power and channel bandwidth.

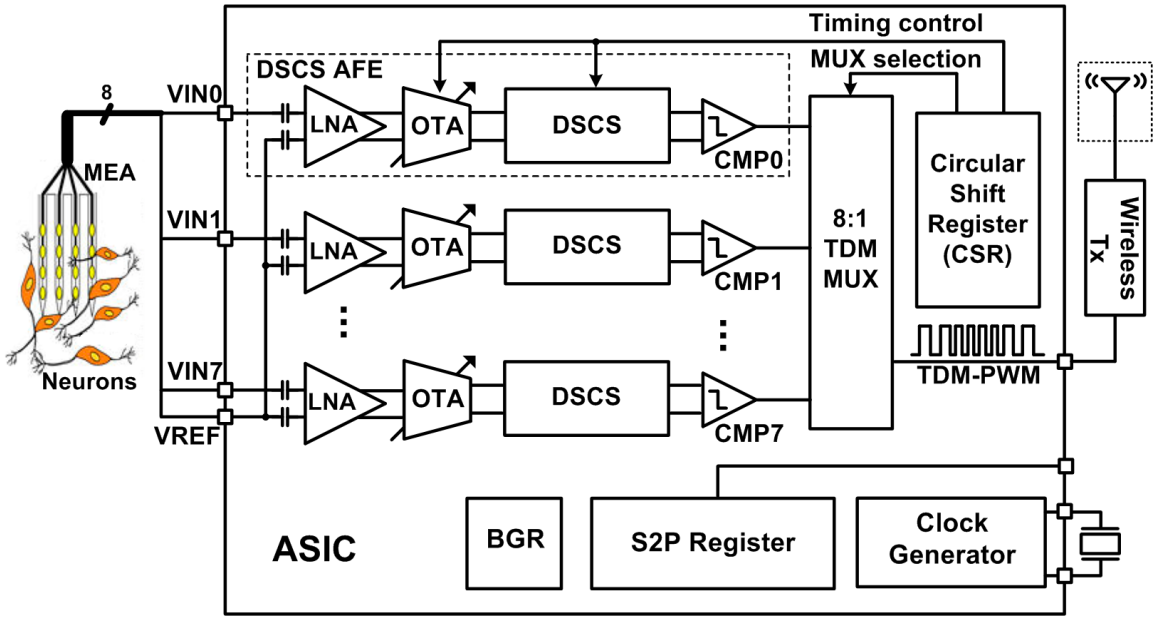
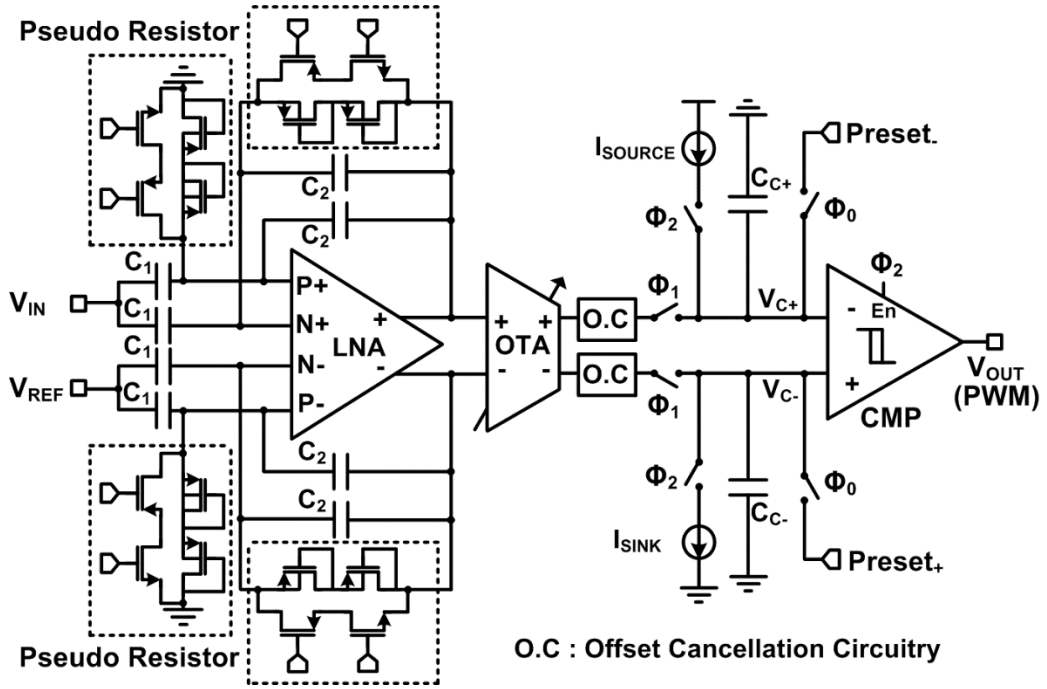


Fig. 3.1. Block diagram of an 8-ch DSCS-based wireless implantable neural recording (WINeR-6.5) system.

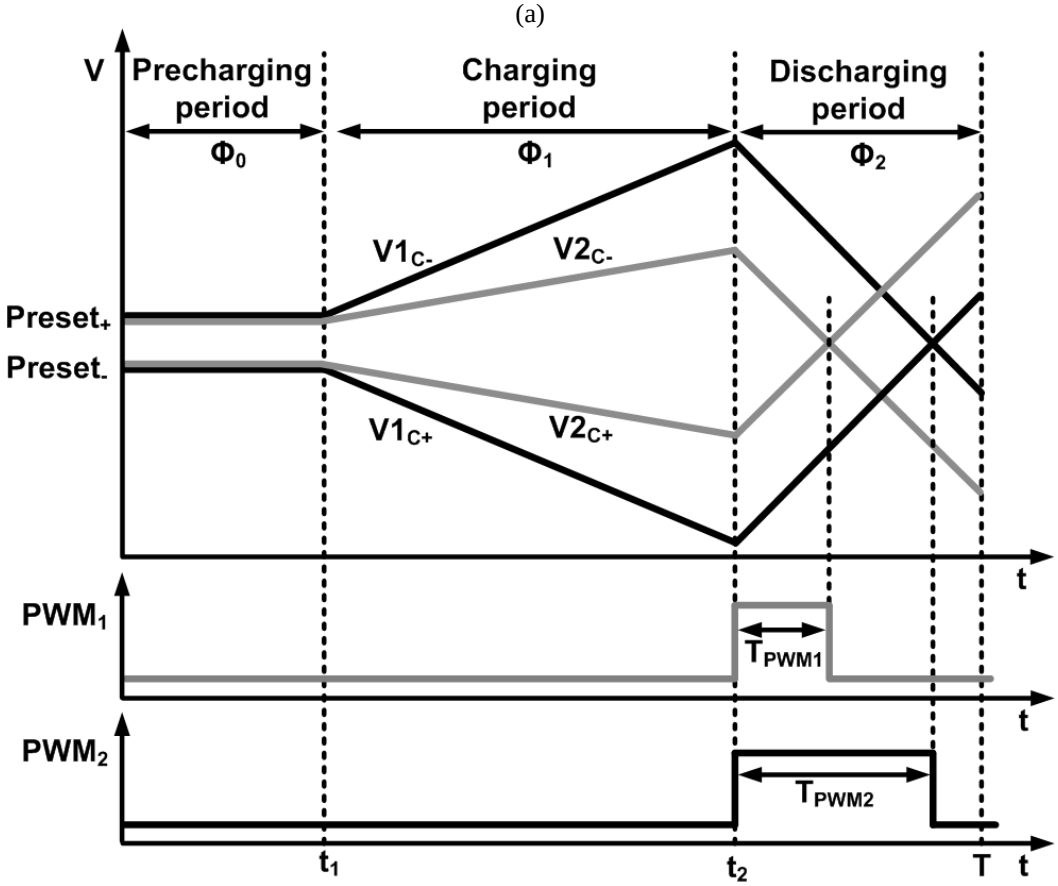
The prototype presented here is an 8-channels DSCS AFE with additional control circuitry. However, it can be easily extended to higher channel counts. The next section describes the entire WINeR system, and Section 3.3 presents the measurement results followed by discussion.

3.2. DSCS-AFE Architecture

A schematic of the proposed DSCS-AFE is shown in Fig. 3.2a. The neural signal is amplified in a fully differential LNA. The LNA also serves as a bandpass filter, which is composed of feedback capacitors and pseudo-resistors that are located on the front end and feedback loop [9]. The variable-g_m OTA converts the amplified neural signal into a differential pair of currents, which are integrated into capacitors C_{C+} and C_{C-} for the fixed time period Φ_1, which is labeled as the "charging" period in Fig. 3.2b. The slopes of capacitor voltages V_{C+} and V_{C-} during the charging period are dependent on the amplitude of the neural signal within that period. A "precharging" period Φ_0, during which the capacitor voltages are set to the pair of well-defined preset values Preset_+ and Preset_-, occurs prior to the charging period.



(a)



(b)

Fig. 3.2. DSCS-AFE for a single channel: (a) Block diagram, (b) Operating waveforms of the dual-slope integration for two different input voltages.

After the charging period, a constant current source and a constant current sink discharge the accumulated charges on C_{C+} the C_{C-} during another constant period Φ_2, which is labeled in Fig. 3.2b as the "discharging" period. V_{C+} and V_{C-} are compared by the fast hysteresis comparator, which is only enabled during Φ_2 to conserve power. The resulting comparator output is a PWM signal, in which the duty cycle T_{PWM}/Φ_2 is proportional to the amplitude of the differential LNA input voltage V_{IN}-V_{REF} from the DSCS mechanism.

Dual-slope integration has several advantages compared with the previously employed single-slope integration [61]. First, the accuracy of the amplitude-to-time conversion (ATC) is independent of both the capacitance values and clock frequency because they affect both the charging slope and discharging slope by the same ratio. Second, the fixed input signal integration period results in the attenuation of the background and LNA noise components in the analog input. Third, there is no need for a separate high-precision triangular wave generator, which further reduces the power requirements.

3.2.1. LNA

The proposed LNA uses a complementary input stage to increase the effective transconductance with a given bias current by two-fold [66]. A detailed schematic of the LNA and its common-mode feedback (CMFB) is provided in Fig. 3.3.

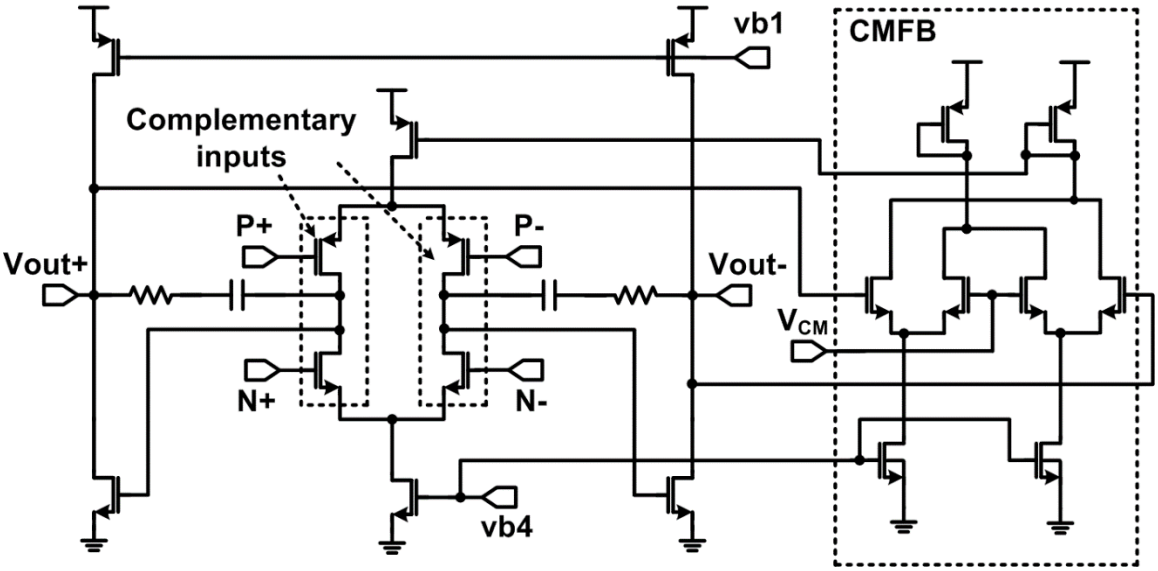


Fig. 3.3. Schematic diagram of the fully-differential LNA with CMFB.

3.2.2. OTA

A schematic of the OTA is provided in Fig. 3.4. It converts the amplified differential voltage at the LNA output to differential current at the input of the DSCS stage. Following a simple differential pair, differential currents are fed into a variable-gain fully differential current amplifier stage. The total g_m of the OTA can be adjusted by controlling the current mirror ratios of the current amplifier stage by 3 bits. The cascode mirror structure in the output stage reduces the nonlinearity in the charging and discharging output currents due to variations in the output voltages, V_{C+} and V_{C-}.

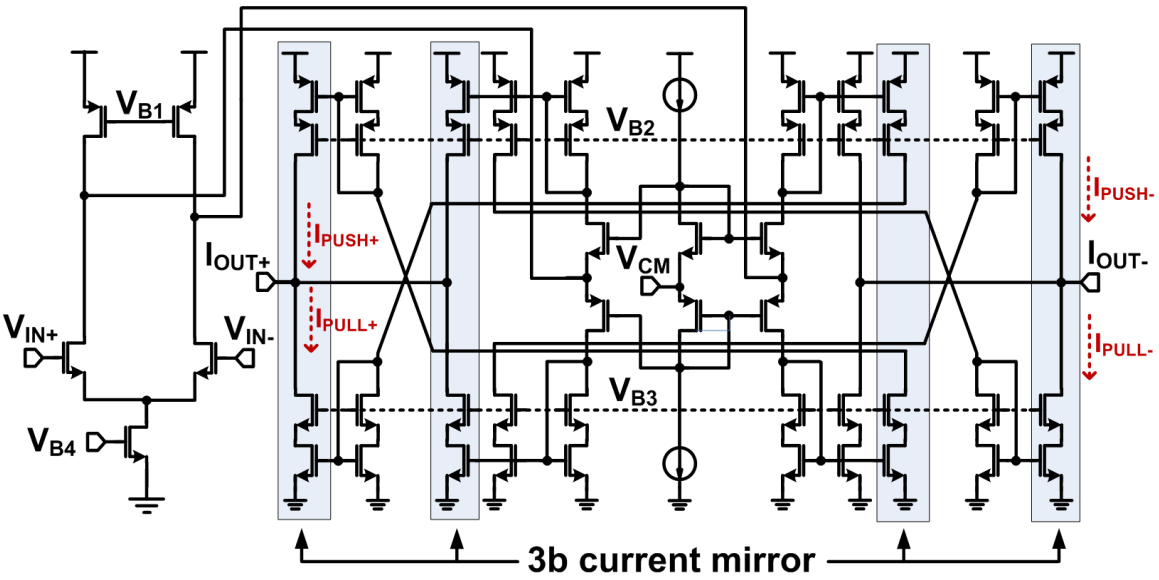


Fig. 3.4. Schematic diagram of the fully diff. OTA with 3-bit adjustable g_m.

3.2.3. DSCS and OTA Offset Cancellation

When the OTA outputs are connected to C_{C+} and C_{C-} at the end of Φ_0, the voltage difference between the floating OTA outputs and capacitors, which are precharged at $Preset_-$ and $Preset_+$, creates undesirable instantaneous currents that can distort the current integration during Φ_1. When its inputs are shorted, the OTA's offset currents can add offset to the charge being sampled during Φ_1. The offset cancellation (OC) circuit in Fig. 5 is employed to prevent these effects.

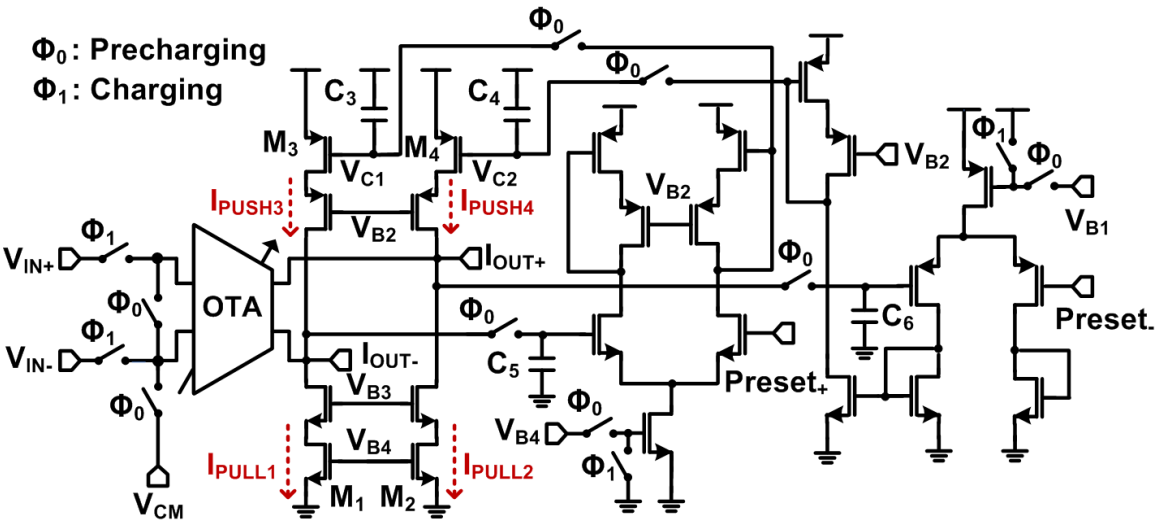


Fig. 3.5. Schematic diagram of the DSCS block including OTA offset cancellation circuitry.

During Φ_0, the OTA inputs are shorted to the common mode voltage V_{CM}; as a result, the OTA current outputs during this phase comprise its offset current. The OC circuit adds I_{PULL1} and I_{PULL2} to the OTA output pull currents, I_{PULL+} and I_{PULL-} in Fig. 3.4 and adds I_{PUSH3} and I_{PUSH4} to the OTA output push currents I_{PUSH+} and I_{PUSH-}. The resulting currents are connected to the pair of dummy capacitors C_5 and C_6 during Φ_0, in which the voltages are compared to $Preset_+$ and $Preset_-$, respectively, via a feedback loop and the resulting error voltages V_{C1} and V_{C2} are used to calibrate I_{PUSH3} and I_{PUSH4} until I_{OUT-} and I_{OUT+} node voltages become equivalent to $Preset_+$ and $Preset_-$, respectively, prior to the end of Φ_0. The two feedback voltages are simultaneously sampled in C_3 and C_4 and maintained during Φ_1, in which the OC currents cancel the OTA output currents while charging C_{C+} and C_{C-}. The OC feedback loop is only turned on during Φ_0 to conserve power.

3.3. Measurement Results

An 8-channel prototype ASIC was fabricated using the TSMC 0.35-µm 4-metal 2-poly CMOS process. Fig. 3.6 displays the chip micrograph and floor planning, which occupies 2.4 × 2.1 mm^2, including the padframe. In this implementation, a single DSCS-based AFE channel occupies 872 × 331 μm^2.

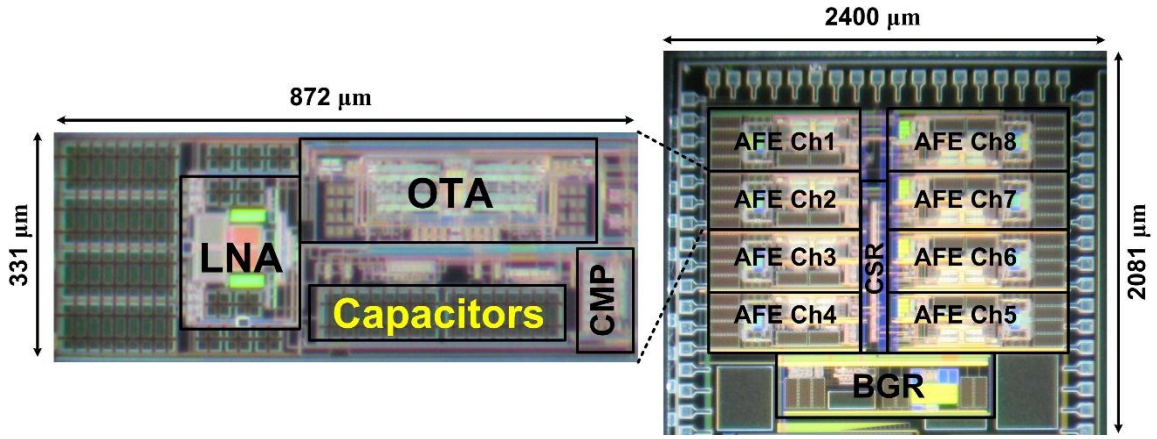


Fig. 3.6. Die photomicrograph of the 8-channel neural recording SoC with DSCS-AFE, implemented in the TSMC 0.35-µm CMOS (size: 2.4 × 2.1 mm^2).

C_1 was 10 pF, C_2 was 100 fF, $C_{3,4}$ were 200 fF, $C_{5,6}$ were 400 fF, and $Cc+/-$ were 10 pF. The LNA specifications were measured when the gain was set at 40 dB. The lower cutoff frequency was tunable from 288 Hz to 1 kHz by voltage-controlled pseudo resistors, and the higher cutoff frequency was ~10 kHz. The fully differential design of the LNA caused a 65.5 dB power supply rejection ratio (PSRR) and a 56.4 dB common mode rejection ratio (CMRR), with an input referred noise of 2.77 μV_{rms} in the range of 288 Hz to 10 kHz. The g_m of the OTA was programmable from 7.43 to 52 µS in 8 steps. The discharge current was also programmable from 332 nA to 2.3 µA in 8 steps. The sampling frequency f_S for each channel was set to 31.25 kHz. The charging time Φ_1 was adjustable in 6 steps from 2.7 to 15.0 µs by programming the S2P register.

Fig. 3.7 presents some of the main waveforms in the DSCS-AFE. $\Phi_{1,Ch1}$ is the charging clock signal for the 1st channel, and $V_{C+,Ch1}$ and $V_{C-,Ch1}$ are the differential output voltages of the charge sampling capacitors of that channel. The bottom trace is the time-division multiplexing (TDM)-pulse-width modulation (PWM) output signal, which combines the PWM signals from all 8 channels. The three phases of the DSCS operation are displayed in the enlarged segment. During Φ_0, $V_{C-,Ch1}$ and $V_{C+,Ch1}$ are precharged to $Preset_+$ and $Preset_-$, respectively. They are differentially charged during Φ_1 with the offset-calibrated OTA output currents, which are proportional to the differential input

signal. During Φ_2, the capacitors are discharged by the programmable current sources, while their voltages are compared. PWM_{Ch1} becomes high at the beginning of Φ_2, and goes low when $V_{C+,Ch1} \geq V_{C-,Ch1}$. The pulse width T_{PWM} is proportional to the input signal. Table 2.2 lists the specifications of the new WINeR-6.5 system with DSCS-based AFE and compares them with other recent studies.

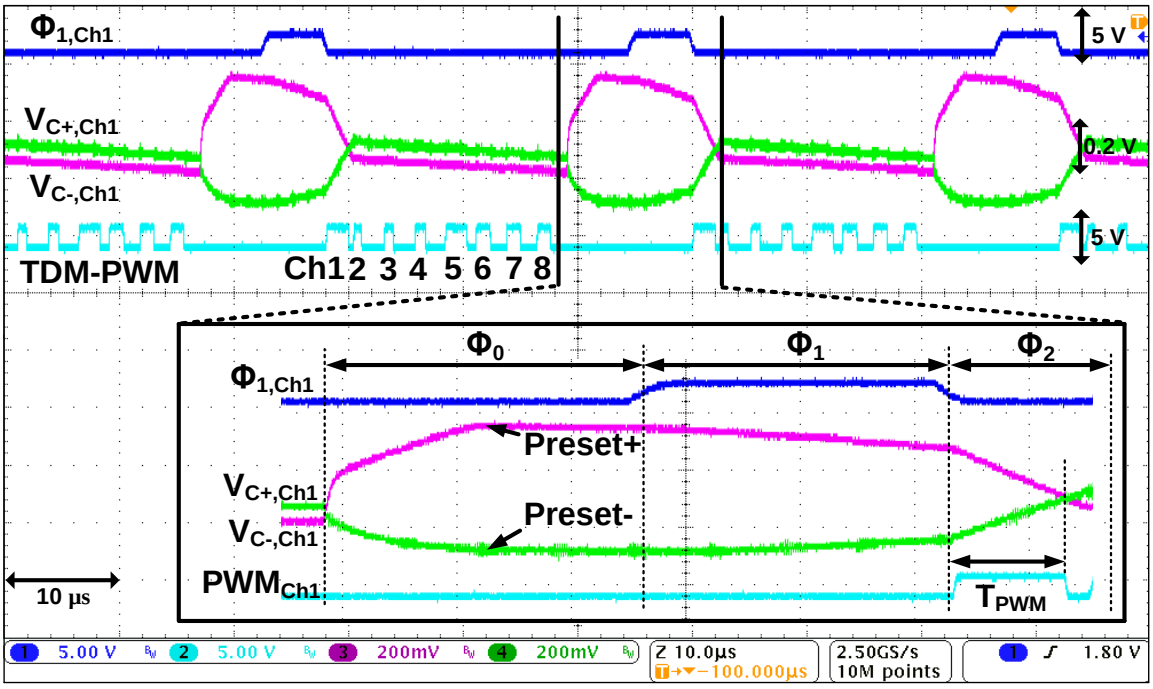


Fig. 3.7. DSCS-AFE measured waveforms at 250 ksps from 8 channels.

Table 2.2: WINeR-6.5 specifications and benchmarking.

Publication	This work	[16] 2012	[15] 2012	[67] 2014
Technology	0.35µm CMOS	0.13µm CMOS	65nm CMOS	0.5µm CMOS
V_{DD} (V)	1.8	1.2	0.5	1.5, 3
Die size (mm^2)	2.4 × 2.1	5 × 5	0.13	2.85 × 3.84
No. of channels	8	96	1	9
Total power (mW)	0.255	6.5	0.005	5
Power/ch. (µW)	31.8	68	5.04	55.68
Area/ch. (mm^2)	0.29	0.26	0.13	-
Sampling rate (kSps/ch)	31.25	31.25	20	200
LNA gain (dB)	40	-	> 32	39.35
LNA input ref. noise (μV_{rms})	2.77	2.2	4.9	4.58
LNA HPF (Hz)	288 to 1000	<1, 280	300	178 - 302
LNA LPF (kHz)	10	10	10	6.92 - 8.13
Resolution (bit)	-	10	8	-
System input ref. noise (μV_{rms})	6.50	-	-	4.58

The basic functionality of the entire system was verified by playing attenuated artificial spike waveforms. The original signal with an amplitude of ~40 mV_{p-p} was connected to the LNA through a 100:1 resistive attenuator. The resulting PWM signal from the DSCS-AFE was transmitted to an FPGA-based TDC for digitization. In addition, 16-bit digitized samples were buffered, packetized, and sent to a PC through its USB port as a serial data bit stream, which was demultiplexed using BCI2000 open-source software, displayed on the screen, and stored on the hard disk. Fig. 3.8 compares the original neural signal with the recovered waveform in the BCI2000.

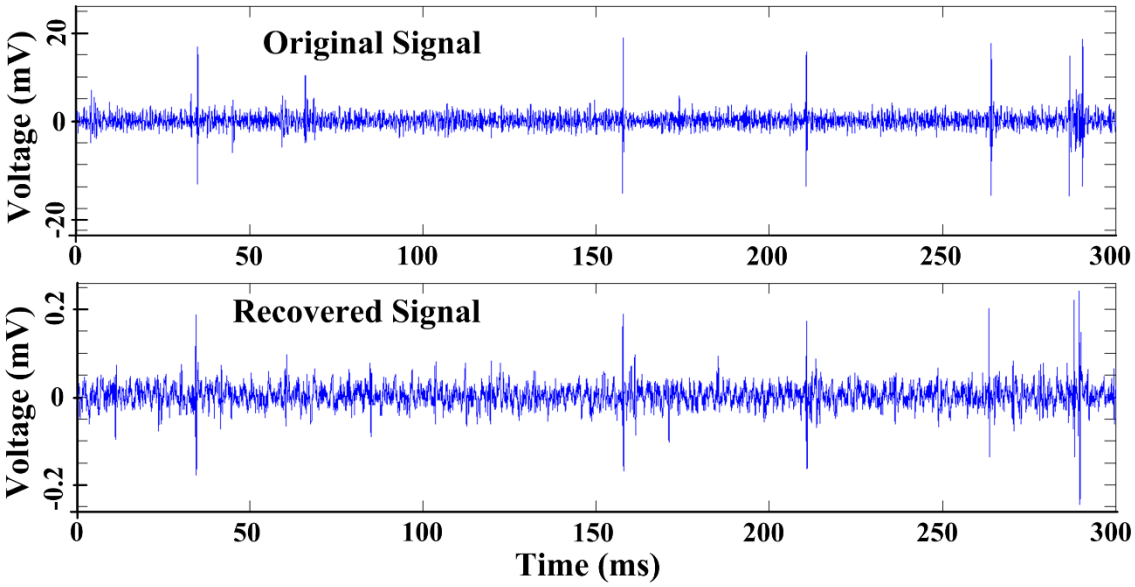


Fig. 3.8. The original and recovered pre-recorded spike signals, sampled at 31.25 kHz.

The input referred noise of the DSCS-AFE was measured by grounding the OTA inputs and conducting a fast Fourier transform (FFT) on the recorded signal for 10 s. The resulting input referred noise spectral densities are shown in Fig. 3.9. Integration of these curves from 288 Hz to 10 kHz yielded an input referred noise of 5.88 μV_{rms}. Including the LNA noise, the noise of the entire system became 6.5 μV_{rms}.

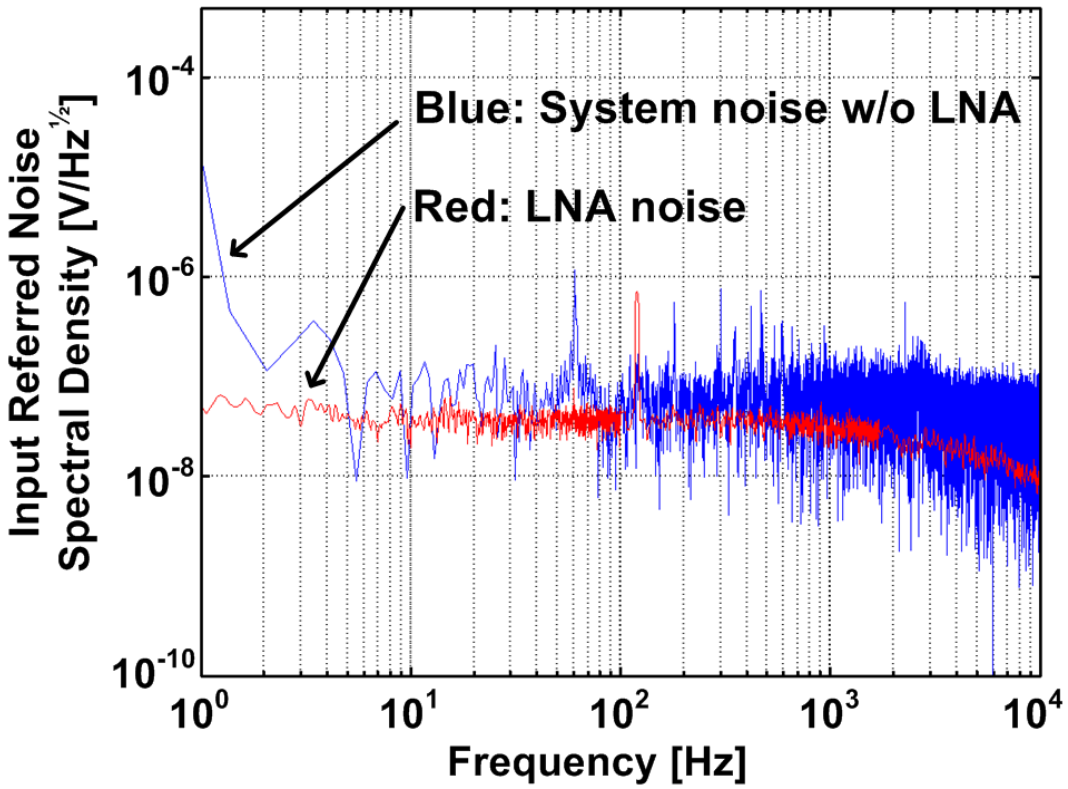


Fig. 3.9. Input referred noise of the LNA and the entire system without the LNA.

3.4. Discussion

A new DSCS-based AFE architecture for use in multi-channel wireless bio-signal recording systems has been presented. The DSCS architecture enables low noise and low power amplification, filtering, and ATC with robust pseudo-digital PWM-TDM output, which does not require sophisticated synchronization between the Tx and Rx in systems with a large number of channels that utilize high speed ADCs in the Tx unit.

CHAPTER IV

WINER-7 SYSTEM WITH A DUAL-SLOPE CHARGE SAMPLING ANALOG FRONT-END

In this chapter, a wireless integrated neural recording system (WINeR-7) is presented with a novel-dual slope charge sampling (DSCS) analog front-end (AFE) architecture, which amplifies neural signals by utilizing the charge sampling concept for analog signal conditioning, such as amplification and filtering. The presented DSCS-AFE simultaneously achieves amplification, filtering, and sampling while consuming a small amount of power. The output of the DSCS-AFE produces a PWM signal that is proportional to the input voltage amplitude. A circular shift register (CSR) utilizes time division multiplexing (TDM) of the PWM pulses to create a pseudo-digital TDM-PWM signal that can feed a wireless transmitter. The 8-channel SoC was fabricated in a 0.35-μm CMOS process, occupied 5.0 × 2.5 mm^2 and consumed 51.4 mW from a 1.8 V/4.2 V supply. The measured input-referred noise for the entire system, including the receiver located at 1.2 m, is 5.38 μV_{rms} in the range of 1 Hz to 10 kHz when the system is inductively powered. For each channel, the sampling rate is 21.701 kHz and the power consumption is 19.3 μW.

4.1. Introduction

The proposed DSCS- AFE architecture utilizes charge sampling benefits while converting input signals to PWM pulses, which eliminates the need for high-speed ADCs on the transmitter unit, as shown in Fig. 4.1. These features render the proposed DSCS-AFE architecture a suitable choice for large channel count systems with limited available power and channel bandwidth. The system presented here has an 8-channel DSCS AFE with additional control circuitry. However, it can be easily extended to higher channel counts.

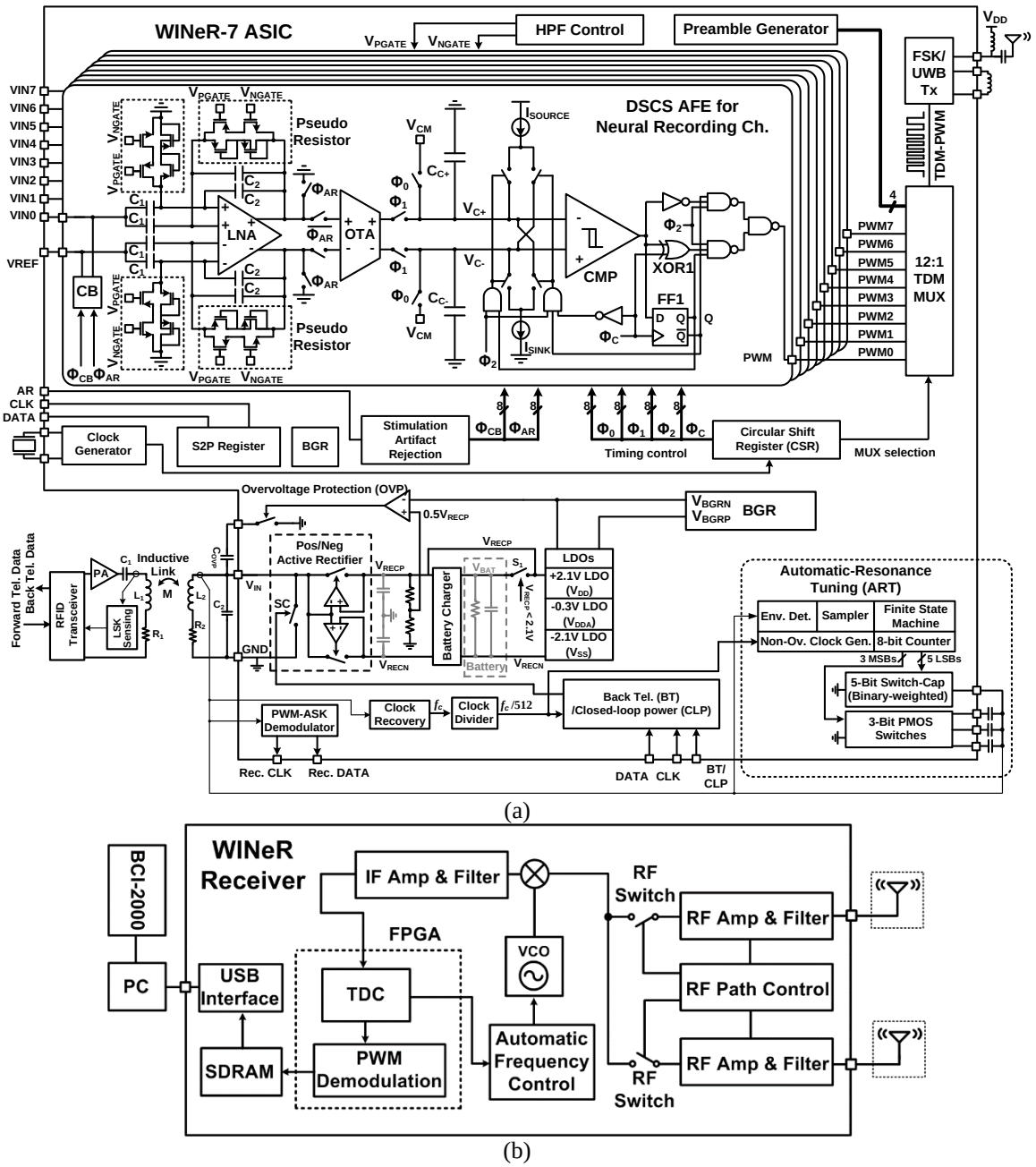


Fig. 4.1. Block diagram of an 8-channel DSCS-based wireless implantable neural recording (WINeR-7) system, (a) Transmitter unit, (b) Receiver unit.

4.2. System Architecture

4.2.1. Transmitter Unit

A simplified block diagram of the WINeR-7 ASIC is shown in Fig. 4.1a. Fully differential low-noise amplifiers (LNAs) amplify and filter neural signals with a gain of 100 V/V and an adjustable bandwidth. A variable-g_m operational transconductance amplifier (OTA) converts the amplified signal to a current with 3-bit binary control over g_m. The DSCS block pulse width modulates the neural signal by comparing differentially charged and discharged capacitors via a rapid hysteresis comparator. A TDM combines the eight PWM outputs of the DSCS blocks and generates the TDM-PWM signal. A circular shift register (CSR) controls the AFE timing. The pseudo-digital TDM-PWM signal can be directly fed into a wireless Tx to be transmitted using a frequency-shift keying (FSK) modulation scheme. The PWM-TDM-FSK signal at the output of the VCO is amplified and transmitted through a miniature wideband monopole antenna. A serial-to-parallel (S2P) 32-bit register is used to control various adjustable parameters among the 8 channels.

4.2.2. Receiver Unit

A WINeR-7 wideband Rx unit is similar to the WINeR-6 Rx described in Section 2.2. Its block diagram, which is depicted in Fig. 4.1b [65], has been designed to demodulate and digitize the incoming FSK-TDM-PWM signal (909/921 MHz) in the ISM band from 902 to 927 MHz. The RF signal is detected by two individual antennas to increase the wireless coverage over the experimental space and amplified and filtered by a pair of identical RF front-ends. A control circuit subsequently connects the RF path with a stronger signal to a mixer, which down-converts the received RF signal to a baseband (44/56 MHz) before demodulating the FSK signal in an FPGA. The resulting TDM-PWM signal is fed into a time-to-digital converter (TDC) in the same FPGA to generate the

digitized samples, which are demultiplexed and buffered in a 1-Mbit SDRAM to handle data transfer delays and transferred to a PC through a USB port. The general-purpose open-source platform BCI2000, which is frequently used with EEG signals for brain-computer interfacing (BCI) applications, runs on the PC to display the received neural signals on the screen and store them on a hard disk in real time [54]. The entire Rx without an FPGA board is compactly integrated in a single PCB, as shown in Fig. 4.2. The size shrinks compared with the WINeR-6 Rx. The size of the WINeR-7 PCB is 10.1 × 4.5 cm.

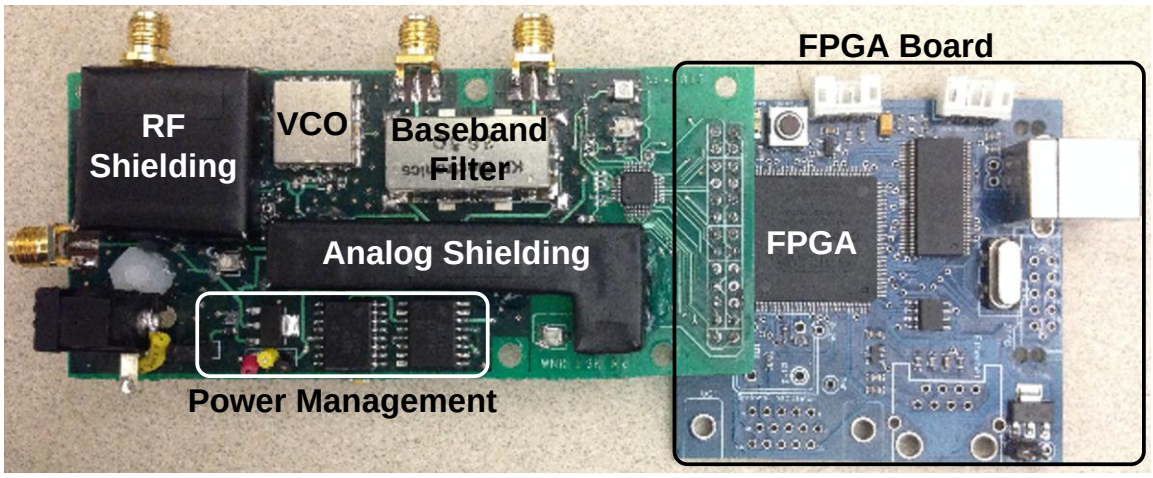


Fig. 4.2. WINeR-7 FSK Rx PCB.

The total structure of the WINeR-7 FSK Rx is similar to the total structure of the WINeR-6 Rx, with the exception that the frequency range changes from 433 to 915 MHz. In the RF front-end, a commercial surface acoustic wave (SAW) filter is employed for a bandpass filter with a bandwidth that ranges from 902 to 928 MHz. Thus, the channel selectivity increases compared with the WINeR-6 Rx with a passive bandpass filter. The RF front-end provides 45 dB gain and 26 MHz bandwidths.

To handle +/- 5 V of dual power supplies in the WINeR-6 Rx, a computer power supply was required. The volume and size of the power supply was also a hindrance. The WINeR-7 Rx requires +12 V of the single power supply because power management chips can generate +/-5 V from a +12 V input supply. The current consumption of the WINeR-7 receiver is 380 mA. In addition, RF shielding and analog shielding improves

RF noise interference shielding, as shown in Fig. 4.2. Ground shielding becomes important in an inductively powered experiment because strong RF harmonic interferences are generated from the power carrier frequency.

4.2.3. Power Management Data Transceiver (PMDT) Unit

Fig. 4.3 presents the block diagram of a PMDT, which includes an active positive/negative rectifier, a battery charger, three regulators (LDOs) at 2.1, -0.3, and -2.1 V, an automatic-resonance tuning (ART), a low-power PWM-IR-UWB Tx, a 915-MHz FSK Tx, PWM-ASK demodulator and a PDM transceiver. A power amplifier (PA) drives the Tx coil L_2 at the designated carrier frequency, f_c, which can be either 13.56 or 2 MHz in this design by controlling the rectifier. The AC signal across the Rx L_3C_3-tank, which is tuned at f_c, is rectified by the positive/negative rectifier. The rectifier outputs V_{RECP} = 2.3 V and V_{RECN} = -2.3 V are applied to the battery charger. A decision circuit connects the battery output (V_{BAT}) to the LDO input if $V_{RECP} < 2.1$ V. Three LDOs create a constant V_{DD} = 2.1 V, V_{DDA} = -0.3 V and V_{SS} = -2.1 V, in which V_{DD} and V_{SS} are used for stimulation and FSK Tx whereas V_{DDA} and V_{SS} provide a 1.8 V supply for the recording blocks, UWB Tx, and PDM transceiver. The ART ensures that L_3C_3-tank is always tuned at f_c by sweeping a 5-bit binary-weighted on-chip (3, 6, 12, 24, and 48 pF) and a 3-bit binary-weighted off-chip (100, 200, and 400 pF) capacitor bank, which results in a 0-800 pF capacitance change across the L_3C_3-tank with a 3-pF resolution. A hysteresis comparator detunes L_3C_3-tank by a C_{ovp} of 1 nF when $V_{RECP} > 2.4$ V to protect the PMDT from large input voltages. The circuit-level implementation and measurements are explained in [70].

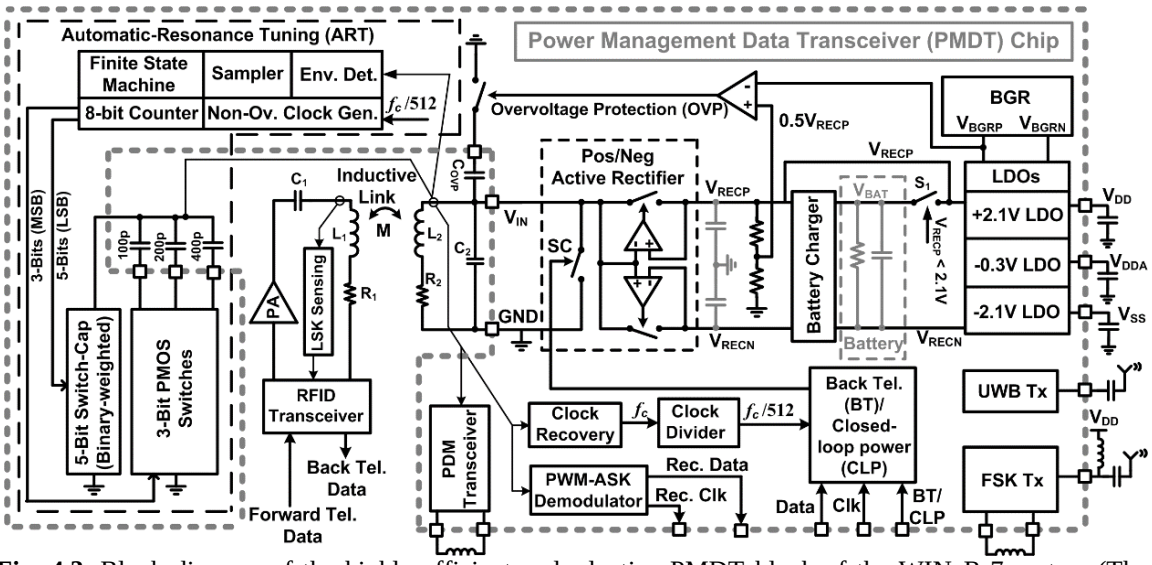


Fig. 4.3. Block diagram of the highly efficient and adaptive PMDT block of the WINeR-7 system (The author acknowledges Dr. M. Kiani for designing this block).

4.3. Wide-Swing DSCS-AFE Architecture

The prototype I of the DSCS-AFE schematic is shown in Fig. 4.4a to demonstrate the proposed DSCS-AFE architecture. The neural signal is amplified in a fully differential LNA. The LNA also functions as a bandpass filter composed of feedback capacitors and pseudo-resistors, which are located on the front end and in the feedback loop [9]. The variable-g_m OTA converts the amplified neural signal into a differential pair of currents, which are integrated the capacitors C_{C+} and C_{C-} for the fixed time period Φ_1, which is labeled as the "charging" period in Fig. 4.4b. The slopes of the capacitor voltages V_{C+} and V_{C-} during the charging period are dependent on the amplitude of the neural signal within that period. A "precharging" period Φ_0 occurs prior to the charging period, during which the capacitor voltages are set to the pair of well-defined preset values Preset$_+$ and Preset$_-$.

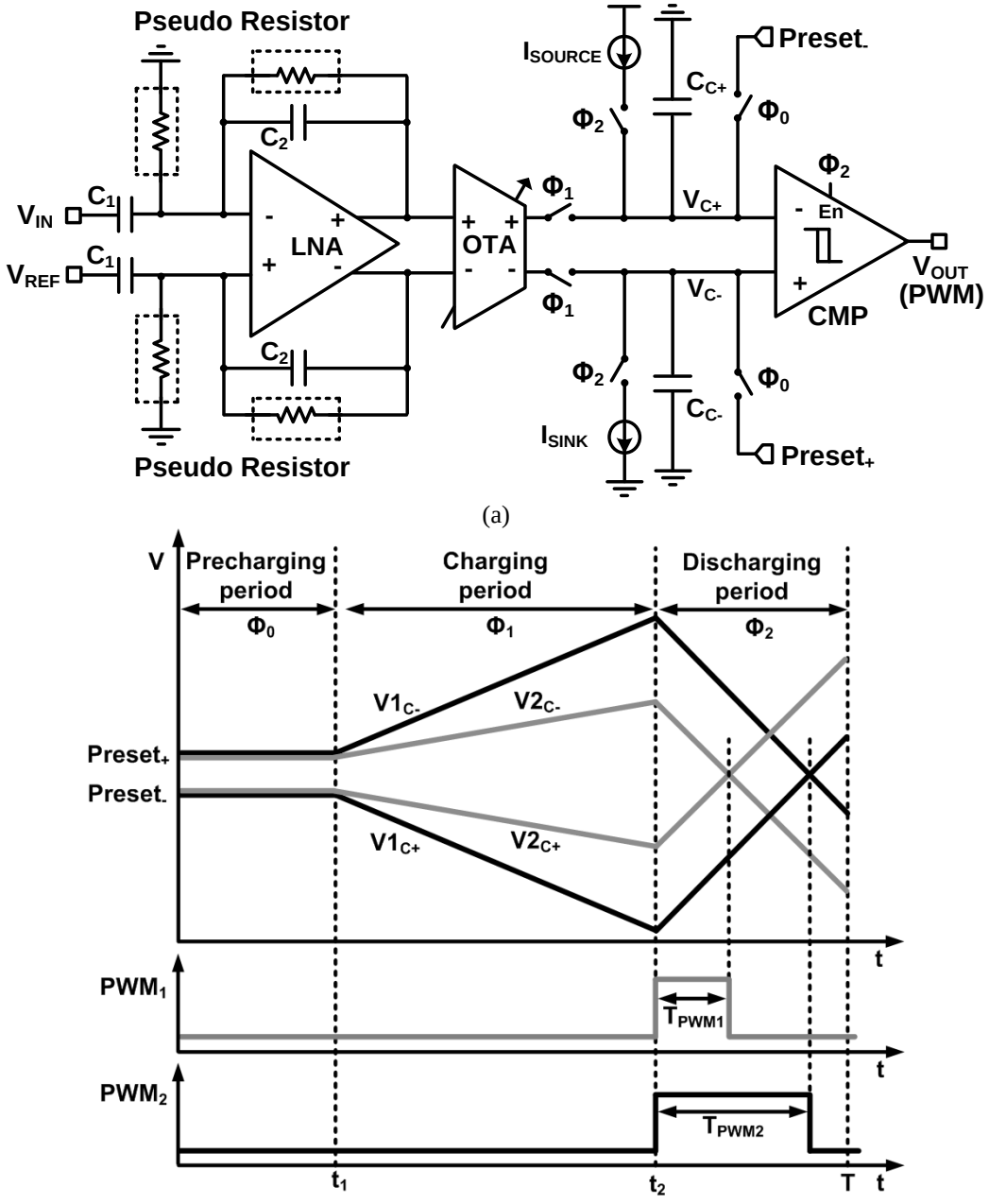


Fig. 4.4. DSCS-AFE prototype I for a single channel: (a) Block diagram, (b) Operating waveforms of the dual-slope integration for two different input voltages.

After the charging period, the constant current source and current sink discharge the stored charges on C_{C+} and C_{C-} during another constant period Φ_2, which is labeled in Fig. 4.4b as the "discharging" period. V_{C+} and V_{C-} are compared by the rapid hysteresis comparator, which is only enabled during Φ_2 to conserve power. The resulting comparator

output is a PWM signal, in which the duty cycle T_{PWM}/Φ_2 is proportional to the amplitude of the differential LNA input voltage V_{IN}-V_{REF} from the DSCS mechanism.

Although the fabricated prototype DSCS-AFE architecture exhibits low power consumption and low noise, the robustness of the system is limited because the negative capacitor voltage output V_{C-} should always be higher than the positive output V_{C+} at the end of Φ_1 to correctly generate the PWM pulse. Thus, the dynamic range of V_{C+} and V_{C-} is limited to half of the supply. In addition, two separate buffers are required to precharge V_{C+} and V_{C-} to $Preset_-$ and $Preset_+$, respectively.

After the fabrication of the prototype DSCS-AFE, the improved DSCS-AFE architecture was designed in the WINeR-7 system, as shown in Fig. 4.1a. The operating waveforms of the WINeR-7 DSCS-AFE are shown in Fig. 4.5. In the new architecture, half of the supply voltage V_{CM} is used to precharge V_{C+} and V_{C-}. In addition, both V_{C+} and V_{C-} can swing within the entire supply range. After Φ_1, the system verifies whether V_{C+} or V_{C-} is higher prior to Φ_2. Using this information, I_{SOURCE} is connected to the lower output and I_{SINK} is connected to the higher output during Φ_2. The PWM pulse width for $V_{C+} > V_{C-}$ should be longer than the PWM pulse width for $V_{C+} < V_{C-}$. The center reference clock signal Φ_C, whose period T_{Center} is half of the Φ_2 period, is used to distinguish the two cases. If $V_{C+} > V_{C-}$, discharging of the output capacitors begins after Φ_C changes from '1' to '0'. $V1_{C+}$, $V1_{C-}$, and the resulting PWM_1 in Fig. 4.5 demonstrate this case. Here, $T_{PWM} = T_{CENTER} + T_{COMP}$. If $V_{C+} = V_{C-}$, the resulting PWM pulse width T_{PWM2} is equivalent to T_{CENTER}. If $V_{C+} < V_{C-}$, the capacitors begin discharging immediately at Φ_2 and $T_{PWM} = T_{CENTER} - T_{COMP}$. When a minimum input is attained, $V3_{C+}$, $V3_{C-}$, and PWM_3 are generated. The pulse width output can be formulated as follows:

$$\begin{aligned} T_{PWM} &= T_{CENTER} + T_{COMP} \quad \text{for } V_{C+} > V_{C-} \\ &= T_{CENTER} - T_{COMP} \quad \text{for } V_{C+} < V_{C-} \end{aligned}$$

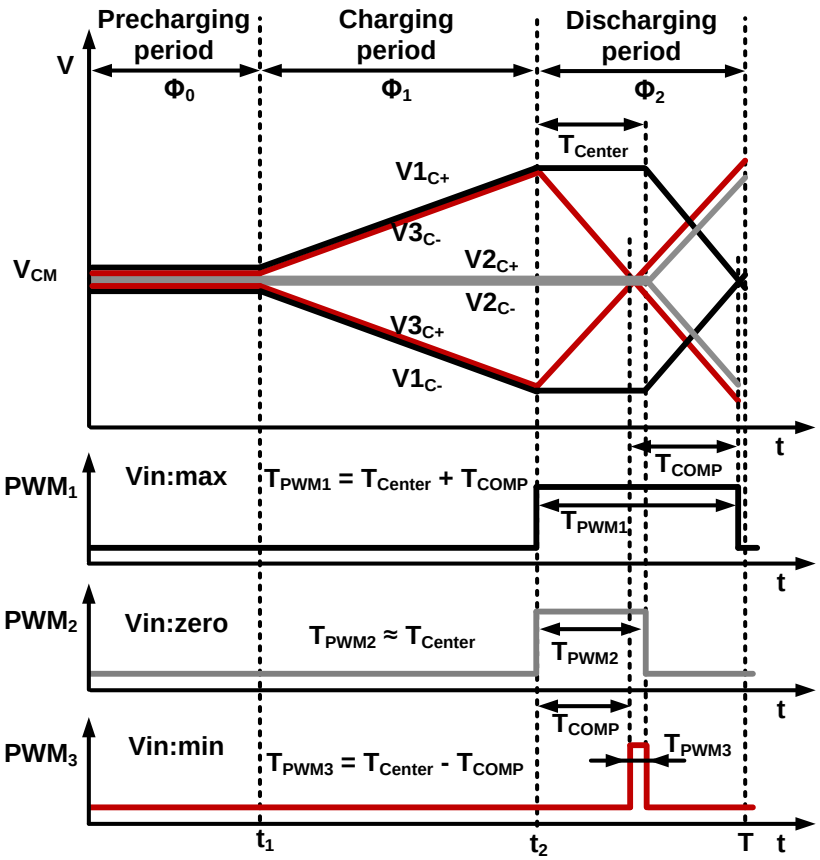


Fig. 4.5. WINeR-7 DSCS-AFE Operating waveforms of the dual-slope integration for two different input voltages.

Four clock signals for the system are shown in Fig. 4.6, in which Φ_C does not overlap Φ_1 and is faster than Φ_2. Therefore, the D flip-flop *FF1* in Fig. 4.1 can distinguish the two cases when it is triggered by Φ_C prior to Φ_2. If $V_{C+} > V_{C-}$, the *FF1* output Q is '0'; if $V_{C+} < V_{C-}$, Q is '1' during Φ_2.

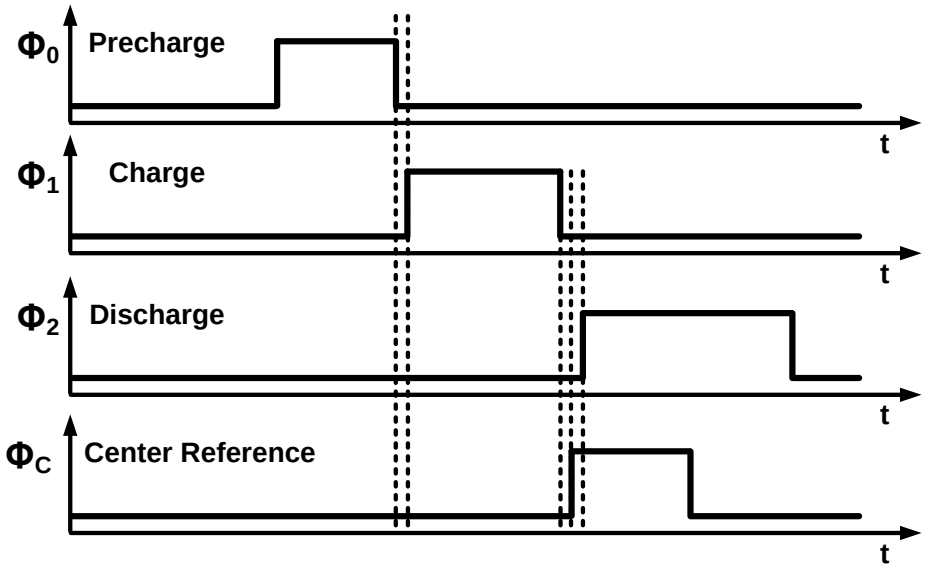


Fig. 4.6. Four clock signals for the WINeR-7 DSCS-AFE.

Two different operations of the system are shown in Fig. 4.7. First, the circuitry of Fig. 4.7a is activated when $V_{C+} > V_{C-}$ and $Q = 0$. Here, I_{SOURCE} and I_{SINK} are connected to V_{C-} and V_{C+}, respectively, after Φ_C changes from '1' to '0' during Φ_2. The PWM output is the inverted signal of the *CMP* output. Therefore, $T_{PWM} = T_{CENTER} + T_{COMP}$. Second, the circuitry of Fig. 4.7b is activated when $V_{C+} < V_{C-}$ and $Q = 1$. Here, I_{SOURCE} and I_{SINK} are connected to V_{C+} and V_{C-}, respectively, during Φ_2. The PWM output is the exclusive 'OR' operation of the *CMP* output and Φ_C. Therefore, $T_{PWM} = T_{CENTER} - T_{COMP}$.

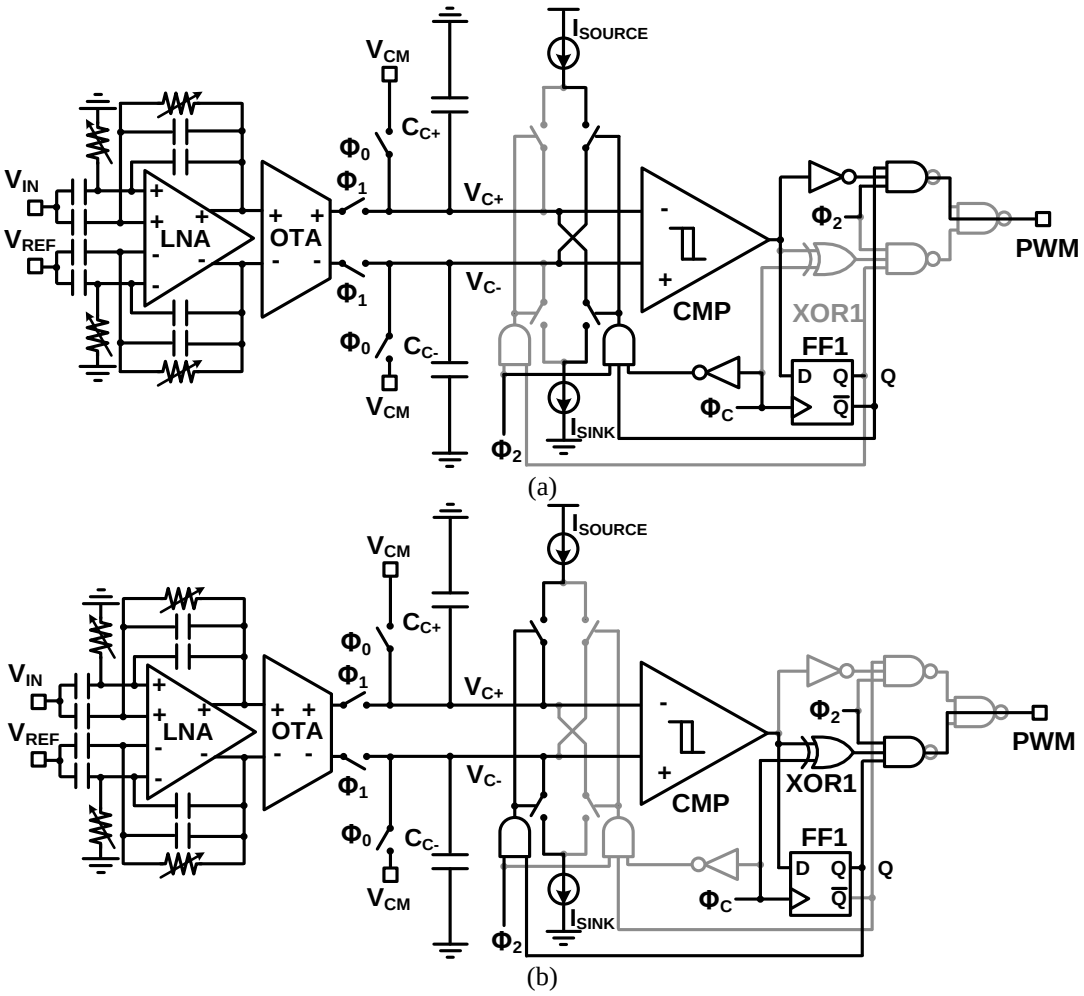


Fig. 4.7. WINeR-7 DSCS-AFE operating block diagrams when (a) $V_{C+} > V_{C-}$ and $Q = 0$, (b) $V_{C+} < V_{C-}$ and $Q = 1$.

Dual-slope integration exhibits several advantages compared with the previously used single-slope integration [61]. First, the accuracy of the ATC is independent of both the capacitance values and clock frequency because they affect the charging and discharging slopes by the same ratio. Second, the fixed input signal integration period results in attenuation of the background and LNA noise components on the analog input. Third, a separate high-precision triangular wave generator, which results in additional power consumption, is not needed.

4.3.1. LNA for Power Scheduling Operations

The proposed LNA uses a complementary input stage to increase the effective transconductance with a given by two-fold [14]. A schematic of the LNA and its common-mode feedback (CMFB) is shown in Fig. 4.8. Two-bit digital control over bias currents offers a programmable low-pass cutoff frequency, which is realized by gate-enabled bits B0 and B1 and change the tail currents of the main LNA and CMFB circuitries. These control bits are also employed for power-scheduling mechanism introduced in [61], which converts the majority of the LNAs that are not being sampled in sleep mode; their power consumption is reduced by disabling B0 and B1.

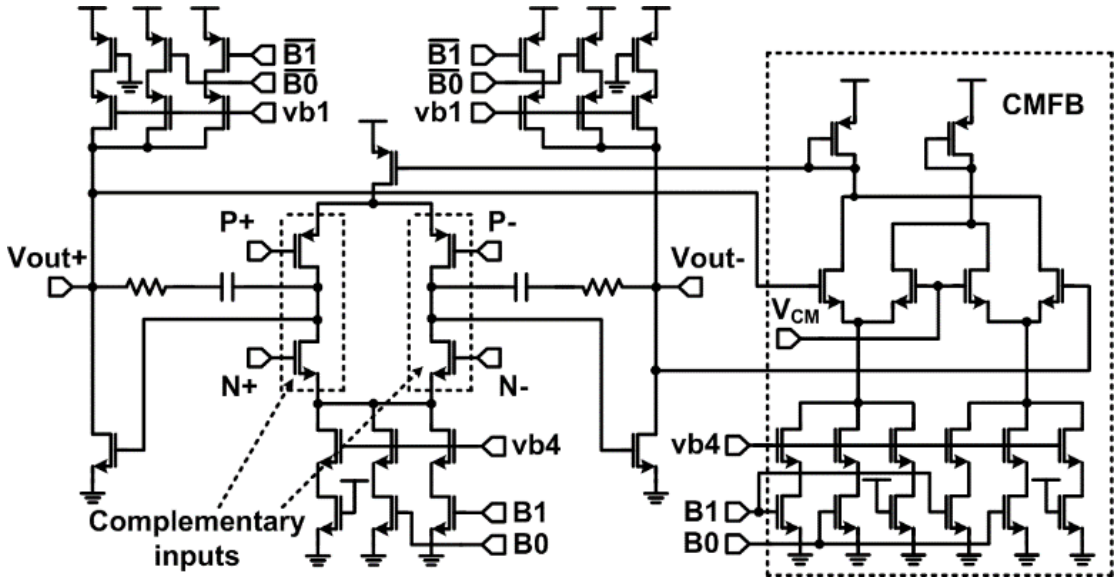


Fig. 4.8. Schematic of the fully differential LNA with the CMFB circuitry.

4.3.2. OTA

The OTA schematic of the WINeR-7 system is similar to the OTA schematic of the WINeR-6.5 in Fig. 3.4. It converts the amplified differential voltage at the LNA output to differential current at the input of the DSCS stage. Following a simple differential pair, differential currents are fed into a variable gain fully differential current

amplifier stage. The total g_m of the OTA can be adjusted by controlling the current mirror ratios of the current amplifier stage by 3 bits. These control bits can also turn off the OTA to limit power consumption. The presented LNA and OTA can function with duty cycle operation for the power scheduling mechanism. The power consumption can be decreased without reducing the quality of the recording capability.

4.3.3. DSCS and OTA Offset Cancellation

The WINeR-7 DSCS AFE has an OTA offset cancellation circuitry that is similar to that of the WINeR-6.5 DSCS AFE, as explained in Section 3.2.3. The difference is that the new offset cancellation circuitry has a V_{CM} for precharge voltages of the WINeR-6.5 DSCS offset cancellation circuitry. When the OTA outputs are connected to C_{C+} and C_{C-} at the end of Φ_0, the voltage difference between the floating OTA outputs and capacitors, which are precharged at V_{CM}, creates undesirable instantaneous currents that can distort the current integration during Φ_1. When its inputs are shorted, the OTA's offset currents can increase the offset to the charge being sampled during Φ_1. The offset cancellation (OC) circuit in Fig. 4.9 is used to prevent these effects.

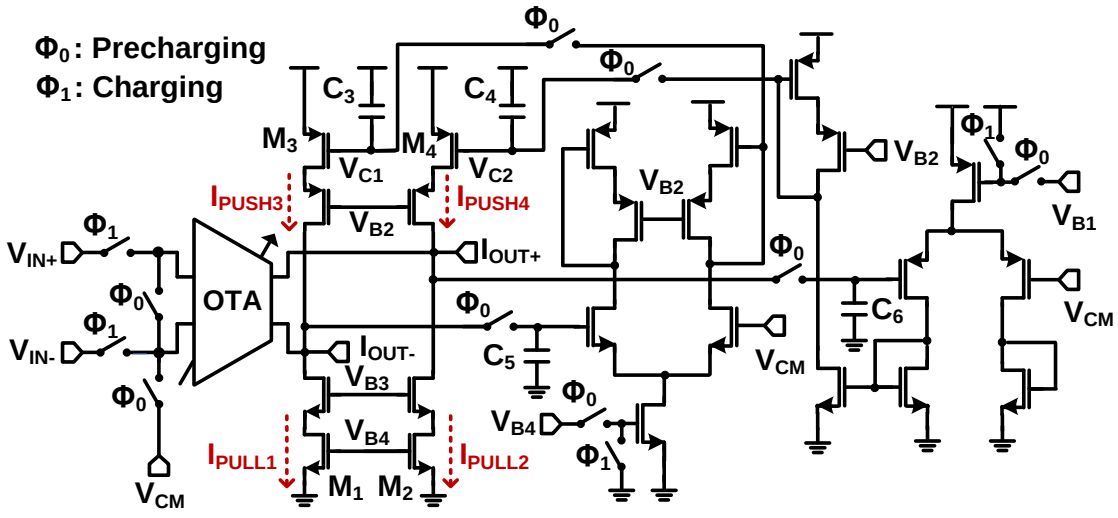


Fig. 4.9. Schematic of the DSCS block including the OTA offset cancellation circuitry.

During Φ_0, the OTA inputs are shorted to the common mode voltage V_{CM}; as a result, the OTA current outputs during this phase comprise its offset current. The OC circuit adds I_{PULL1} and I_{PULL2} to the OTA output pull currents, I_{PULL+} and I_{PULL-} in Fig. 4.9 and I_{PUSH3} and I_{PUSH4} to the OTA output push currents I_{PUSH+} and I_{PUSH-}. The resulting currents are connected to the pair of dummy capacitors C_5 and C_6 during Φ_0. The voltages are compared via a feedback loop to V_{CM}, and the resulting error voltages V_{C1} and V_{C2} are used to calibrate I_{PUSH3} and I_{PUSH4} until the I_{OUT-} and I_{OUT+} node voltages become equivalent to V_{CM} prior to the end of Φ_0. The two feedback voltages are sampled in C_3 and C_4 and maintained during Φ_1, in which the OC currents cancel the OTA output currents while charging C_{C+} and C_{C-}. The OC feedback loop is only turned on during Φ_0 to save power.

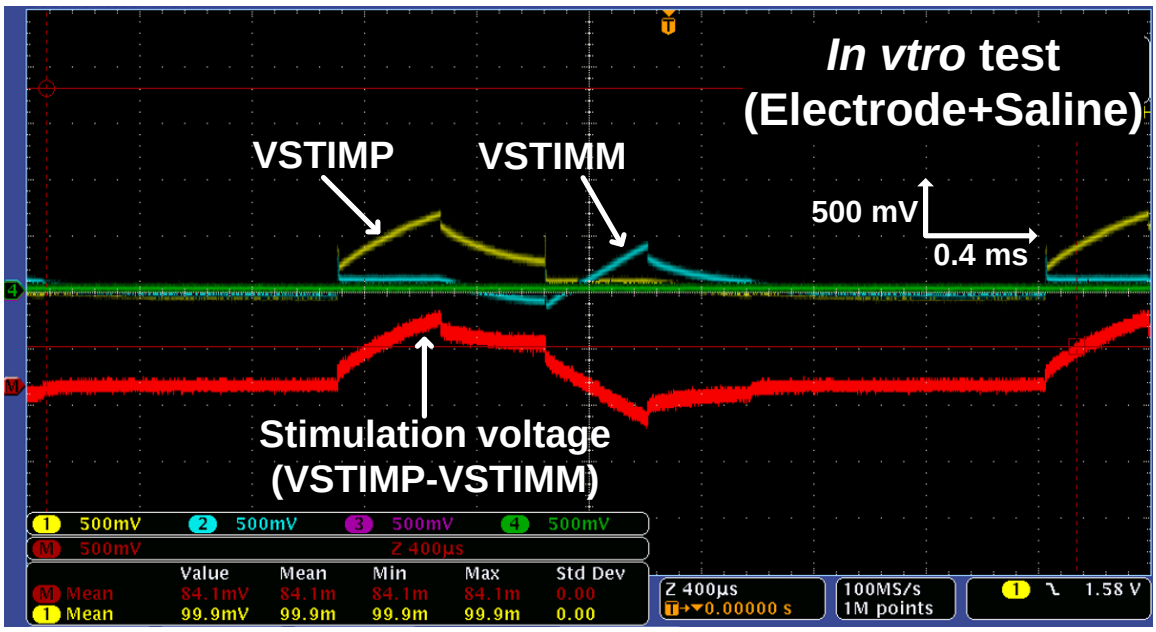
4.4. Stimulus Artifact Rejection

Some applications require a system that interacts with the central and peripheral nervous system in a bidirectional manner. DBS, which is an effective neuromodulation therapy for PD, requires neural recording for a closed-loop operation [69]. When recording and stimulation are performed concurrently, the large amount of stimulation current can force the saturation of adjacent recording electrodes and recording amplifiers. Due to the large time constant, the recovery may be time consuming but can prevent immediate neural recording after stimulation, which is referred to as a stimulation artifact [35],[36]. In the case of arrays of chronic microelectrodes, this problem is exacerbated by the close spacing of the electrodes and their mutual coupling. Although the reduction of artifacts using software is feasible [37], software techniques are not capable of recovering the period during which the amplifiers are saturated, which is frequently longer than 5 ms. Previously reported Hardware-based techniques use a low-slew-rate initial amplifier [38] or actively discharge the electrodes immediately after stimulation [39]. These solutions require that electronics be placed on the animal next to the electrodes. To reduce the

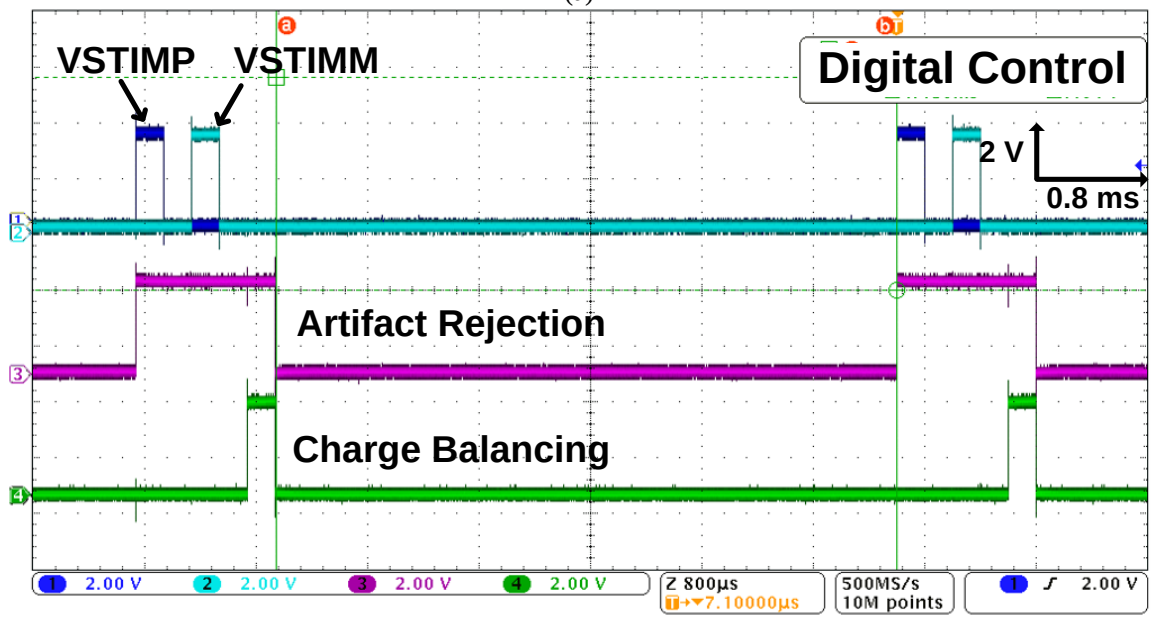
complexity of hardware-based techniques, Venkatraman et al. used an array of switches between the first and second amplifier stages to disconnect the second stage from the first stage for a short period after the stimulation [40].

The WINeR-7 system provides a stimulus artifact rejection block, as shown in Fig. 4.1a for a closed-loop operation, which requires simultaneous stimulation and recording. During stimulation, the LNA can be disconnected from the signal path by stimulus-artifact rejection (AR) switches. In addition, the charge balancing (CB) switch will connect the recording electrode to the reference electrode to ensure charge balancing between the two electrodes. This approach allows the potential charge accumulation to be minimized. These operations will rapidly recover the neural recording as soon as stimulation is terminated.

The explained stimulus artifact rejection function was tested in an *in vitro* set-up with the custom-designed biphasic current stimulator described in [71]. In Fig. 4.10a, a differential stimulation current of 840 µA was applied to a saline solution via electrodes. The stimulus-artifact rejection and charge balancing mechanisms, which simultaneously ensures that the residual charge is neutralized after biphasic stimulation, were triggered in WINeR-7 AFE units via digital control signals, as shown in Fig. 4.10b. In this test, the stimulation pulse duration was set to 600 µs, followed by an additional 400 µs of stimulus artifact rejection and 200 µs of charge balancing.



(a)

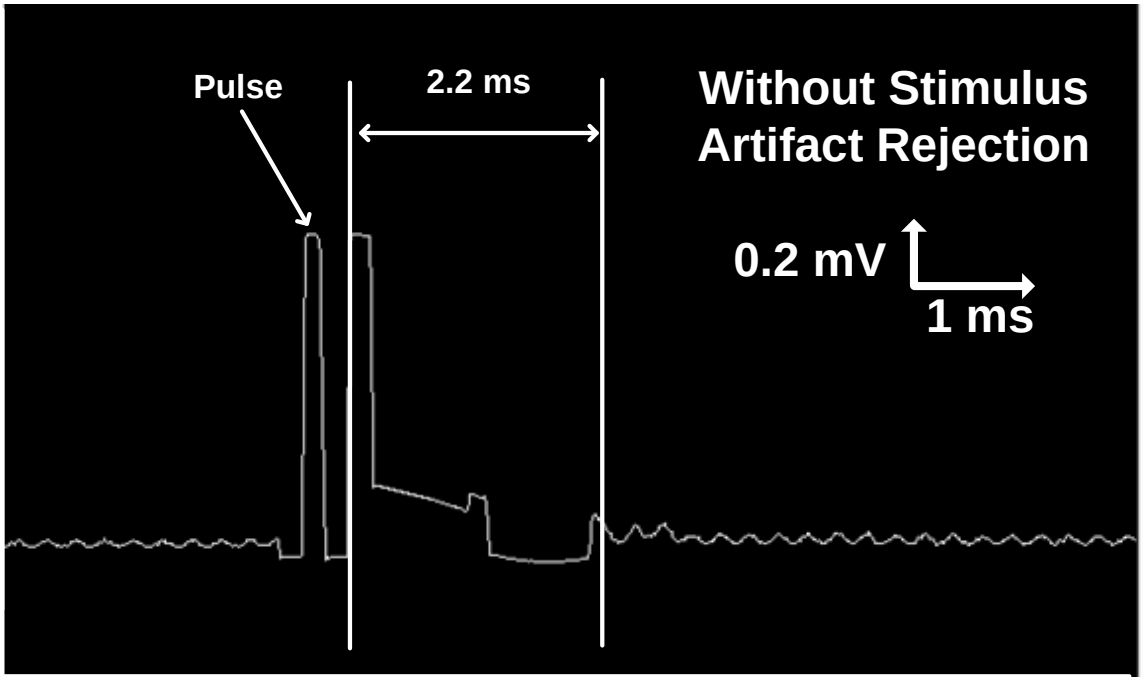


(b)

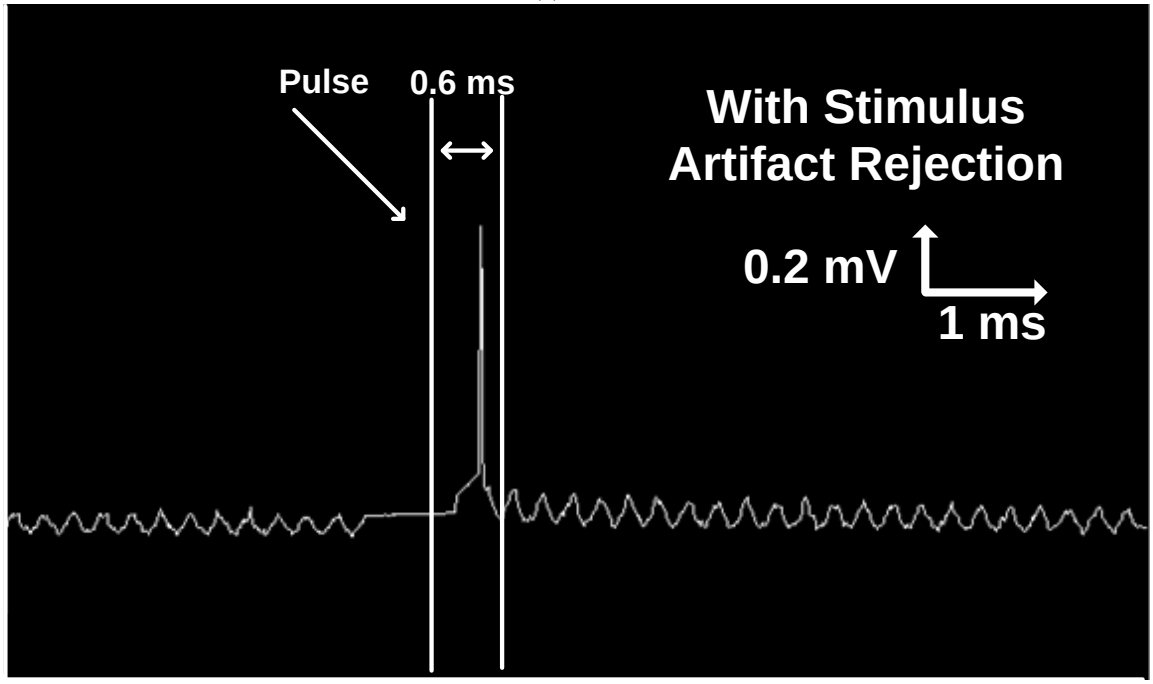
Fig. 4.10. (a) Measured stimulation waveforms from the *in vitro* experiments showing different stimulation currents, (b) Digital control signals: differential simulation signals, artifact rejection signal, and charge balancing signal.

To determine whether the AFE is saturated, 1 kHz of a reference sinusoidal signal was also applied in the saline. In this set-up, an AFE bandwidth that ranged from 400 Hz to 8 kHz was established. First, the set-up was tested without a stimulus artifact rejection function, the transmitter transmitted a recorded signal in the saline, and the Rx recovered and displayed in BCI2000, as shown in Fig. 4.11a. In this figure, the LNA saturation is

distinct and the LNA takes 2.2 ms to recover from saturation. When the same test was performed with stimulus artifact rejection, the recovery time decreased to less than 600 µs, as shown in Fig. 4.11b.



(a)



(b)

Fig. 4.11. Recorded waveforms in the BCI2000 (a) without stimulus artifact rejection, (b) with stimulus artifact rejection.

4.5. FSK RF Transmitter

The FSK Tx consists of a voltage controlled oscillator (VCO) with an off-chip inductor and power amplifier (PA), as shown in Fig. 4.12. Coarse and fine VCO tunings are performed with an off-chip inductor and 2-bit on-chip varactor bank, respectively. The PA can be configured in both single- and differential-mode operation. In differential-mode operation, two antennas with a 180^o orientation can be used to increase the coverage. In single mode, a gate of M_7 is connected to V_{SS} to turn off the left PA branch. The maximum single-tone output power of the PA is 0.4 dBm in single mode and 3.4 dBm in differential mode when the FSK Tx consumes a 12 mA current. Fig. 4.13 also presents the FSK spectrum at two frequencies, i.e., f_1 = 902 MHz and f_2 = 917 MHz, with an output power of -17 dBm. A detailed description of the Tx is provided in [70].

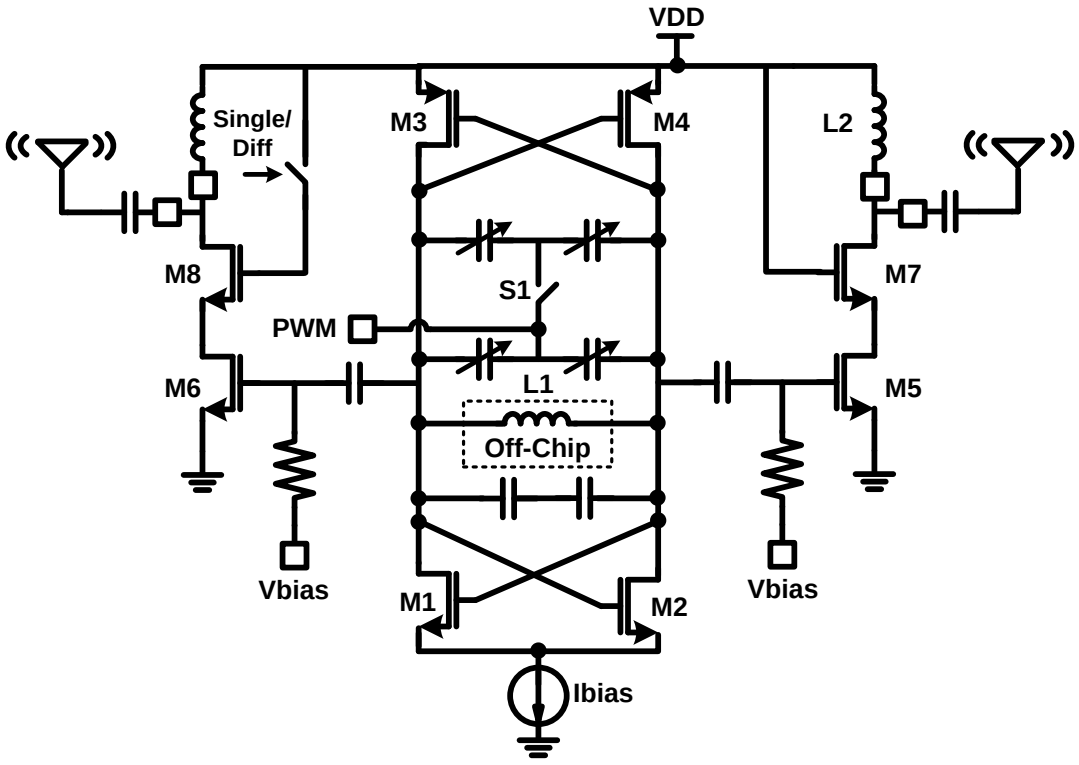


Fig. 4.12. Schematic of the FSK Tx.

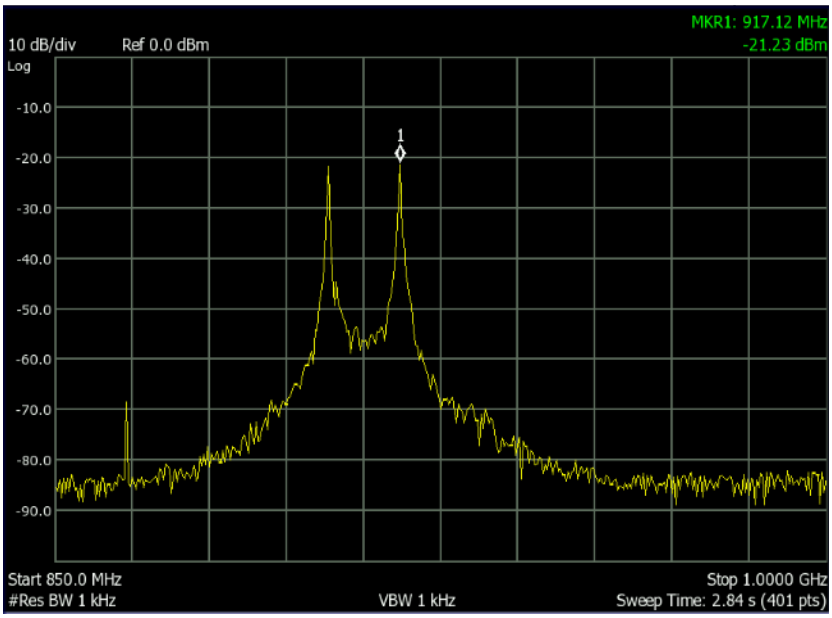


Fig. 4.13. FSK spectrum of the WINeR-7 Tx.

4.6. DSCS FPGA Demodulation for the WINeR-7 System

The WINeR-6 design required a PWM mask to separate each channel PWM pulse [61] because it did not have an accurate clock generator. The DSCS does not require a PWM mask because it functions with an accurate clock signal that is generated by a crystal oscillator. Without a PWM mask, the channel pulse may disappear when the input is not sufficiently large or two channel PWM pulses may be combined when the input is excessive. The elegant FPGA TDC demodulation method should be developed on the Rx side to correctly distinguish this special case. The time bin of the WINeR-7 system is accurately defined by a crystal oscillator. Therefore, once marker signals are detected similar to the WINeR-6 Rx, then the timing of following every channel can be determined in the Rx. This approach does not require the channel to contain a mask.

For synchronization, the preamble generator block in Fig. 4.1a generates four sequences, max pulse, zero pulse, half pulse, and zero pulse, followed by eight sequences from channels 1 to 8. The preamble bits will be detected by the TDC method used in the WINeR-6 Rx. After the detection of preamble bits, eight time bins can be established based on the location of the end point of preambles, as shown in Fig. 4.14. PWM signals

can be accurately detected without any mask function on the Tx side by comparing the channel PWM signals to the time bin.

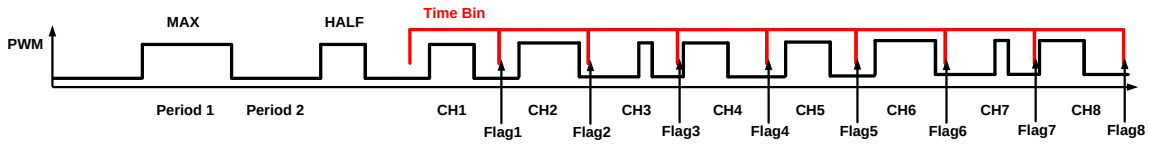


Fig. 4.14. WINeR-7 Rx TDC in the FPGA.

4.7. System Measurement Results

An 8-channel WINeR-7 ASIC was fabricated in the TSMC 0.35-μm 4-metal 2-poly CMOS process. Fig. 4.15 presents the chip micrograph and floor planning, which occupies 5.0 × 2.5 mm^2, including the padframe. In this implementation, a single DSCS-based AFE channel occupies 1,220 × 260 μm^2.

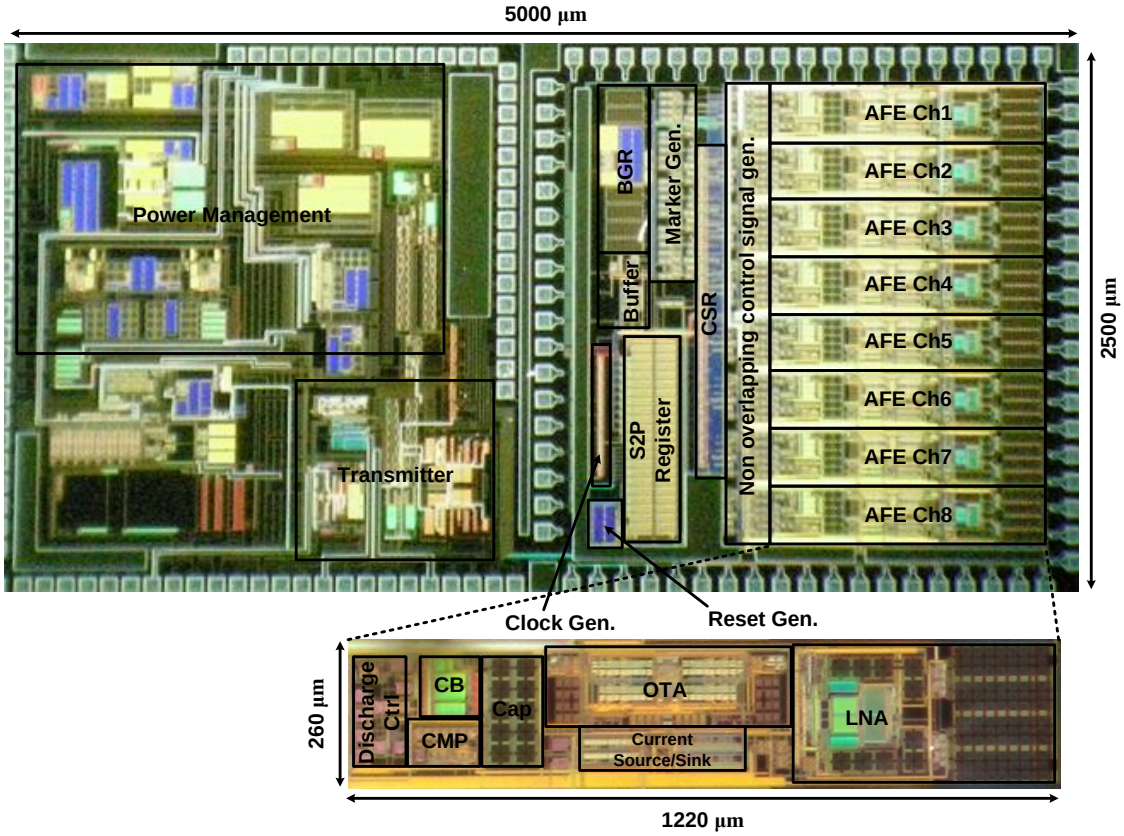
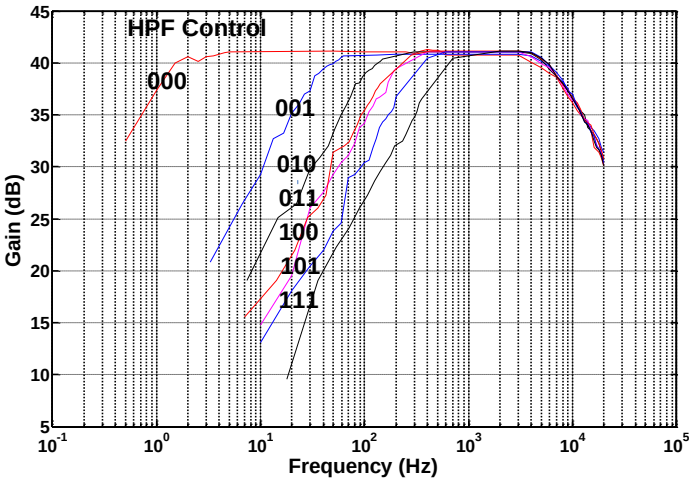


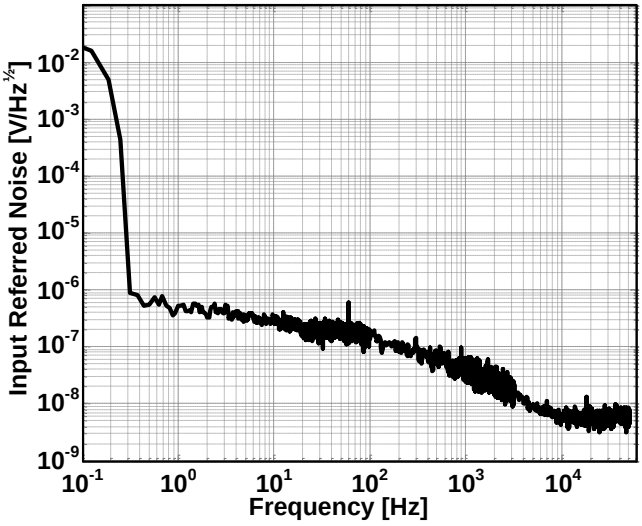
Fig. 4.15. Die photomicrograph of the 8-channel neural recording SoC with the DSCS-AFE, implemented in the TSMC 0.35-µm CMOS (size: 2.5 × 2.5 mm^2).

C_1 was 8 pF, C_2 was 80 fF, $C_{3,4}$ were 200 fF, $C_{5,6}$ were 400 fF, and Cc_+ and Cc_- were 10 pF. The LNA specifications were measured when the gain was set at 40 dB. The lower cutoff frequency could be tuned from 1 to 800 Hz in 8 steps, and the higher cutoff frequency was tunable from 3 to 8 kHz in 4 steps by voltage-controlled pseudo resistors. The fully differential design of the LNA yielded a power supply rejection ratio (PSRR) of 65.5 dB and a common mode rejection ratio (CMRR) of 56.4 dB, with an input referred noise of 2.9 μV_{rms} in the range of 1 Hz to 10 kHz for a LNA, of which a bandwidth was adjusted in the range of 10 Hz to 8 kHz. The g_m of the OTA could be programmed from 7.43 to 52 µS in 8 steps. The discharge current was also programmable from 332 nA to 2.3 µA in 8 steps. A sampling frequency f_S of 21.48 kHz was established for each channel. The charging time Φ_1 could be adjusted from 2.7 to 15.0 µs in 6 steps by

programming the S2P register. The gain and bandwidth and the input referred noise of the LNA were measured and are shown in Figs. 4.16a and 4.16b, respectively.



(a)

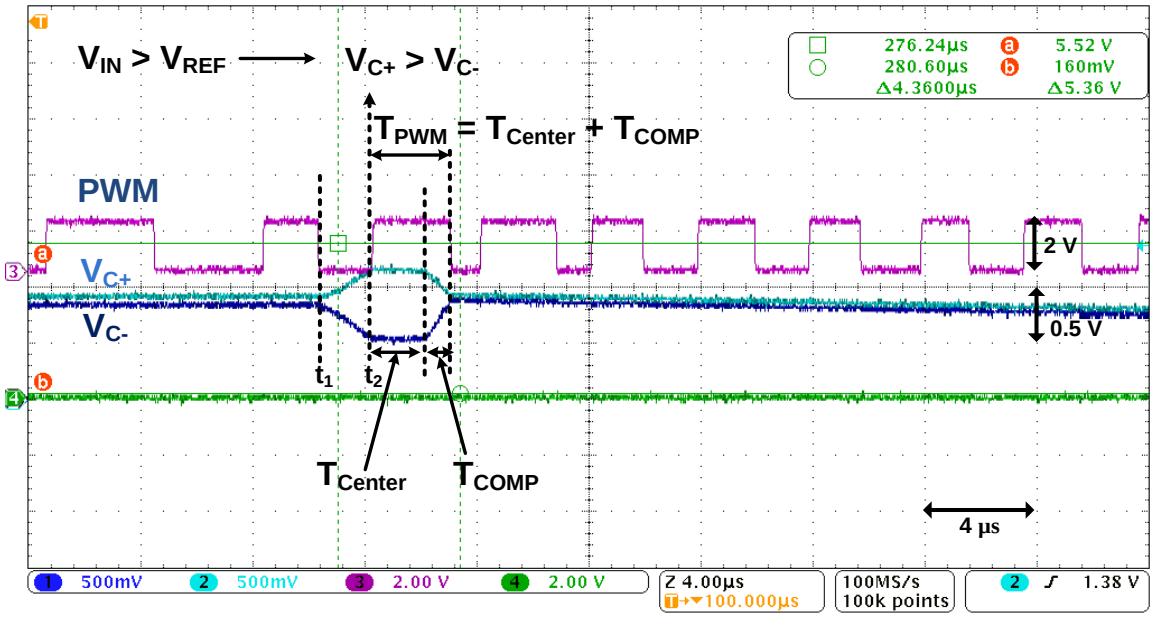


(b)

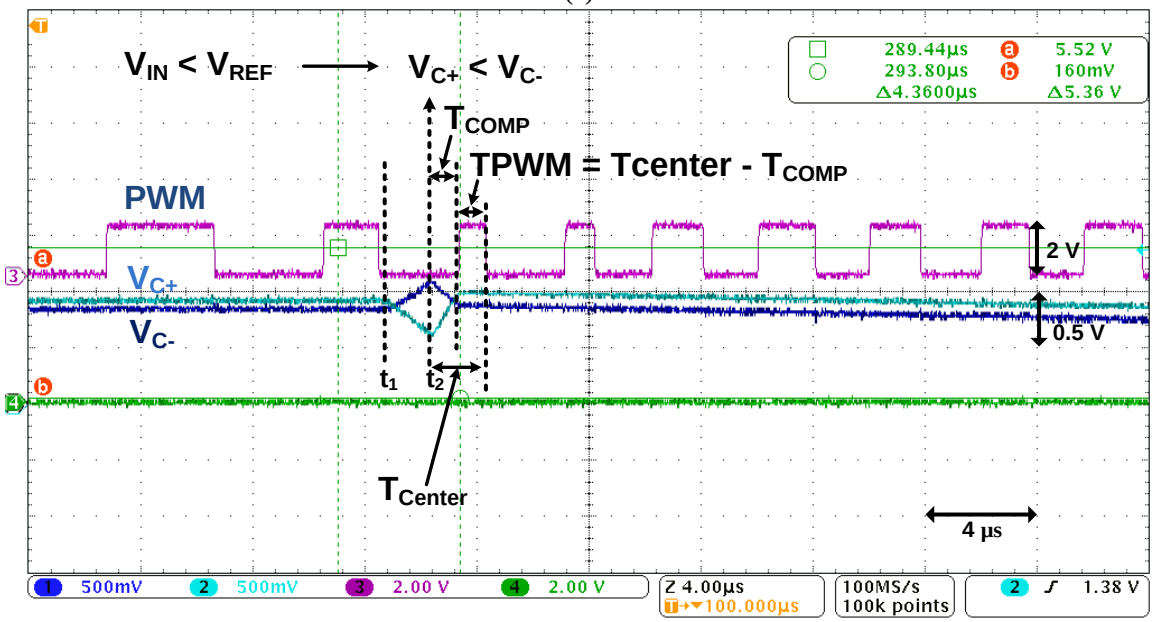
Fig. 4.16. LNA measurements of (a) the gain and bandwidth and (b) the input referred noise.

Fig. 4.17 presents some of the main operating waveforms in the DSCS-AFE for two different cases, as explained in Section III. The purple waveform is the TDM-PWM output signal, which combines the PWM signals from all 8 channels. In Fig. 4.17a, the input is higher than V_{Ref}; thus, $V_{C+} > V_{C-}$, and the measurement results of $T_{PWM} = T_{CENTER} + T_{COMP}$ are attained. In Fig. 4.17b, the input is lower than V_{Ref}; thus, $V_{C+} < V_{C-}$, and the

measurement results of $T_{PWM} = T_{CENTER} - T_{COMP}$ are attained. The pulse width T_{PWM} is proportional to the input signal.



(a)



(b)

Fig. 4.17. DSCS-AFE measurement waveforms from 8 channels.

4.7.1. Rx Antenna

The WINeR-7 Tx has a limited power budget for RF transmission to maintain a low total power consumption. At the same time, it is desired to provide coverage over the large experimental areas and reject the undesirable RF interferences including the harmonics of 13.56 MHz of wireless power transmission. This specification required high Rx front-end sensitivity and high-gain Rx antennas, and a bow tie antenna at 915 MHz (21×10 cm^2) was designed by the collaborator Aida Vera due to these requirements, as shown in Fig. 4.18. The return loss of this antenna was measured, as shown in Fig. 4.19, and the -10 dB bandwidth was 50 MHz in the 870–1,020 MHz frequency range.

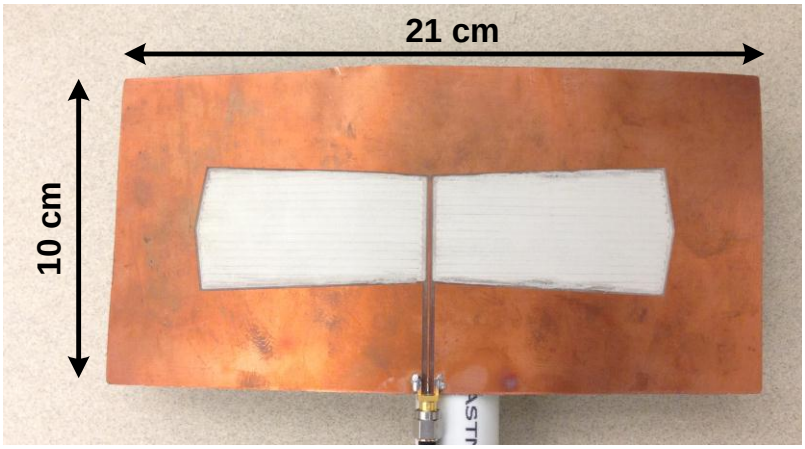


Fig. 4.18. Bow tie antenna for 915 MHz carrier (The author acknowledges Aida Vera for designing this antenna).

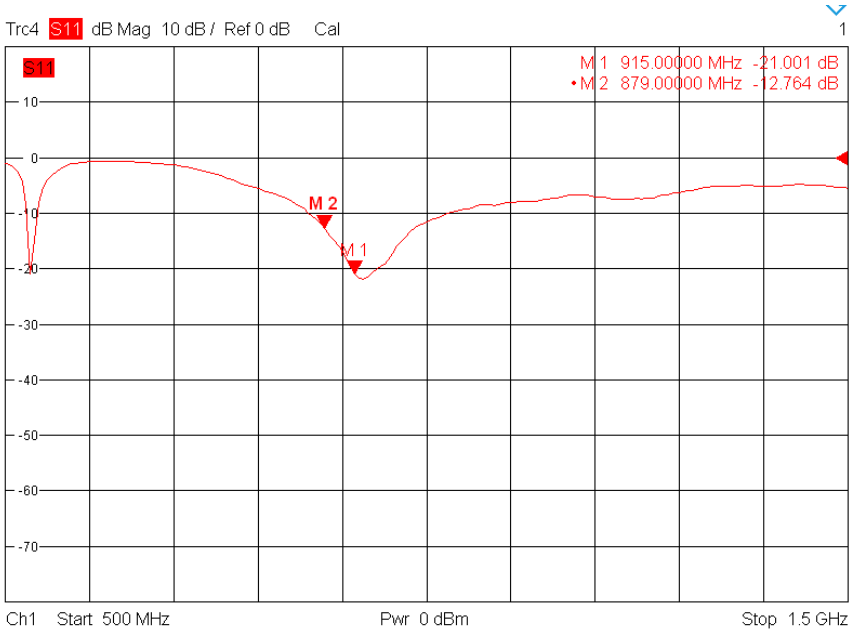
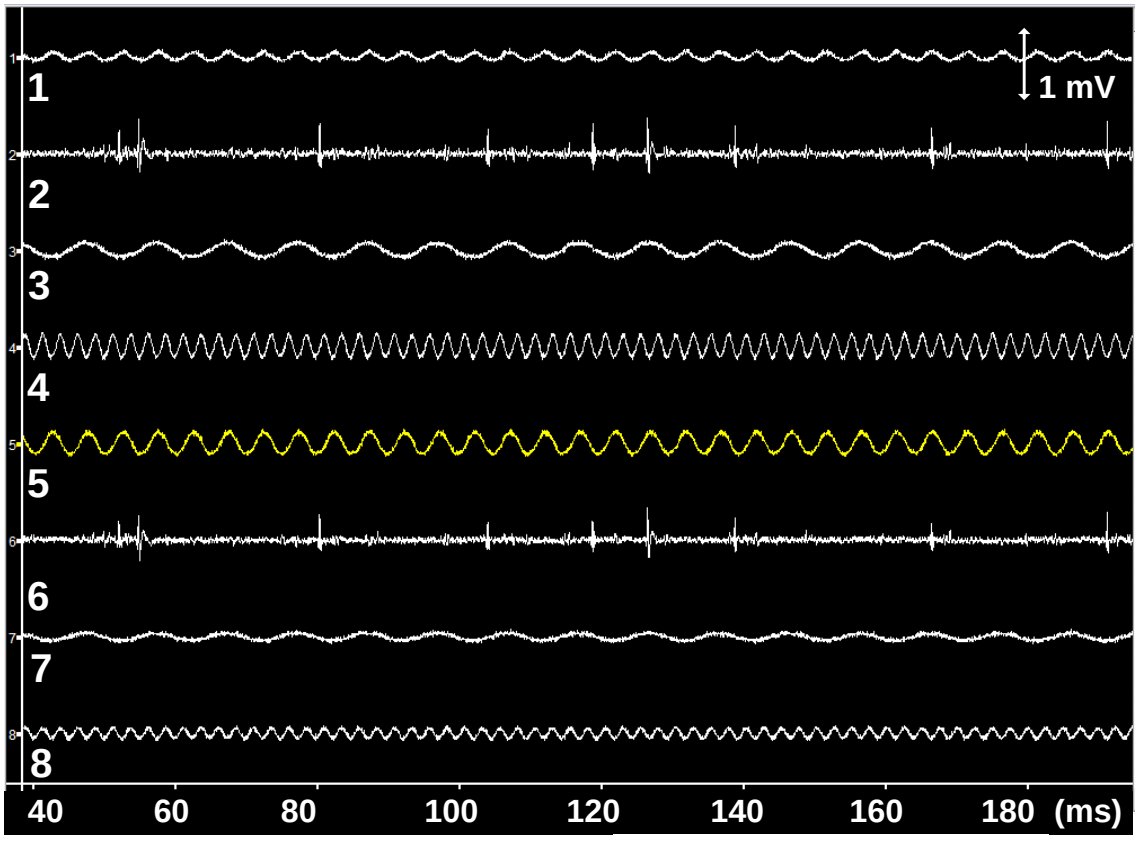


Fig. 4.19. Measured return loss of the Rx bow tie antenna.

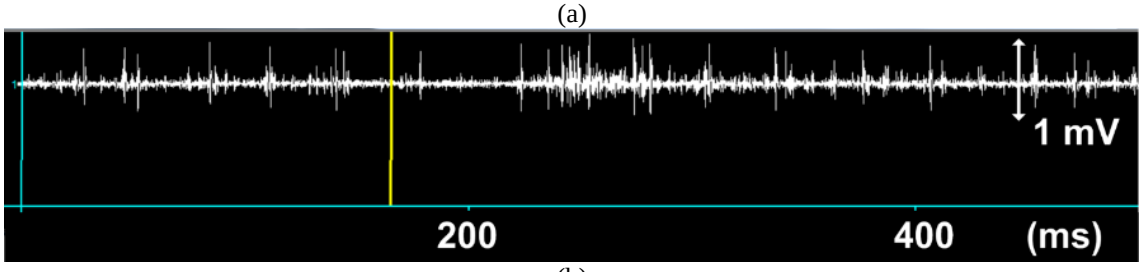
4.7.2. Complete WINeR-7 Tx-Rx Operation

The basic functionality of the entire system was verified by playing attenuated pre-recorded spike waveforms and sinusoidal waveforms. The original signals were connected to the LNA by a 10:1 resistive attenuator. The resulting PWM signals from the DSCS-AFE were transmitted to an FPGA-based TDC for digitization. In addition, 16-bit digitized samples were buffered, packetized, and transmitted to a PC via its USB port as a serial data bit stream, which was subsequently demultiplexed by the BCI2000 open-source software, displayed on the screen, and stored on the hard disk. Simultaneous 8-channel hard-wired recordings are shown in Fig. 4.20a. Channels 1 and 5 received sinusoidal waveforms of ~0.6 mVpp at 200 Hz, Channels 2 and 6 received the pre-recorded spike waveform with 0.8 mVpp, Channels 3 and 7 received sinusoidal waveforms of ~0.6 mVpp at 100 Hz, and Channels 4 and 8 received sinusoidal waveforms of ~0.6 mVpp at 400 Hz. Wireless recording was also tested. The FSK-TDM-PWM RF carrier signal was detected ~100 cm away from the WINeR-7 SoC by a dipole

receiver antenna with a bandwidth of 824–960 MHz. Fig. 4.20b presents the recovered pre-recorded neural signal with 1 mVpp at a Tx-Rx distance of 100 cm.



(a)



(b)

Fig. 4.20. Recovered signals in BCI2000 GUI from (a) simultaneous 8-channel bench-top hard-wired recording and (b) wireless recording at a Tx-Rx distance of 100 cm.

Using this setup and bypassing the LNA block, the integral nonlinearity (INL) and differential nonlinearity (DNL) of the remainder of the WINeR-7 system were measured as a wireless data acquisition system by combining ATC and TDC on the Tx and Rx sides, respectively. In this measurement, constant differential voltages were

generated by an Agilent 33250A function generator with a 12-bit resolution and applied to the LNA output of Channel 1. By varying the DC input from rail to rail, 0 to +1.8 V, the increments in the 16-bit digitized value from the same channel were recorded on the Rx side, which was located 1.5 m from the Tx. Considering a dynamic OTA range, a window between +0.4 and 1.4 V was selected to measure the DNL and INL, and the LSB size was set to 3.9 mV for an 8-bit resolution. Fig. 4.21 presents the measured DNL and INL for the WINeR-7 prototype, which fell within (+0.391, -0.254) LSB and (+0.353, -0.415) LSB, respectively.

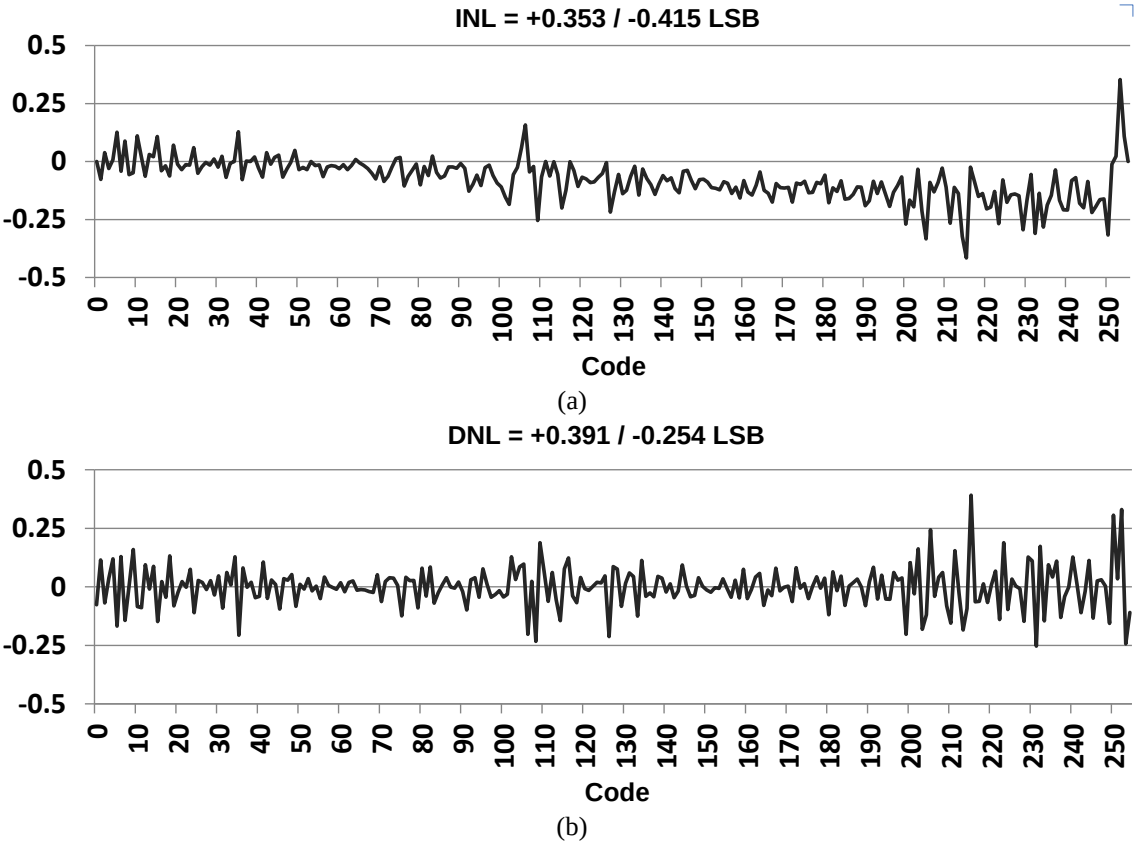


Fig. 4.21. (a) INL and (b) DNL measurements for the entire WINeR-7 system at a Tx-Rx distance of 200 cm.

In addition to the INL and DNL, a tone test was conducted by applying a 217-Hz sinusoidal waveform to the ch-5 LNA output. The test results indicate a spurious-free dynamic range (SFDR) of 64.95 dB with a hardwired link. The SFDR was 66.54 dB with

a wireless link at a Tx-Rx separation distance of 150 cm in Fig. 4.22, indicating that the linearity performance of the WINeR-7 system has increased by 8 dB compared with the WINeR-6 system shown in Fig. 2.17b.

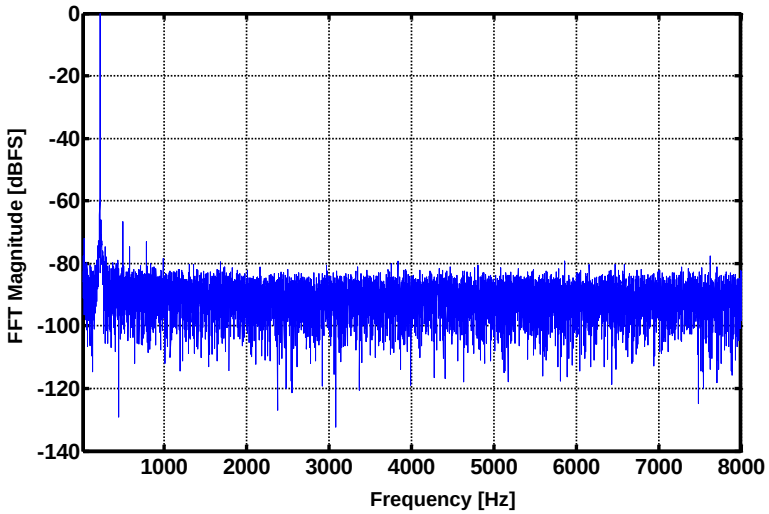


Fig. 4.22. Tone test measurements of the WINeR-7 system at a Tx-Rx distance of 150 cm.

4.7.3. WINeR-7 Noise Performance

To analyze the noise contribution from different WINeR-7 blocks, the noise measurements were performed in an unshielded laboratory environment in several configurations, as shown in Fig. 2.18. In each case, an FFT was applied to 20 s of the recorded signal on the computer to derive its spectrum and refer it back to the input. Fig. 2.18a presents the TDC noise measurement setup. Here, a series of pulses with a 50% duty cycle was generated by a function generator and fed into the TDC block in the FPGA. The TDC noise is expected to be small. The measurement also included the function generator phase noise, which was considered negligible. In Fig. 2.18b, the LNA outputs are forced to ground to cancel the LNA noise. Noise of the wireless link has also been bypassed by directly connecting the TDM-PWM signal from the Tx to the TDC input on the Rx side using a high-speed digital isolator (ISO721). The setup in Fig. 2.18c

is similar to the setup in Fig. 2.18b, with the exception that the LNA noise has been included by grounding the LNA inputs. Fig. 2.18d presents the noise measurement setup for the entire WINeR-7 system. In all noise measurements, the LNA bandwidth was set from 10 Hz to 8 kHz, whereas the input referred noise was integrated over the range of 1 Hz to 10 kHz.

Using the setup shown in Fig. 2.18d (i.e., the entire system), the Tx-Rx distance was swept from 30 to 360 cm to observe the effect of Tx-Rx separation on the noise of the wireless link without shielding. The input-referred noise amplitudes for these measurements are shown in Figs. 4.23 and 4.24. According to these graphs and our theoretical analysis in [46], the noise from the wireless Rx is the dominant noise source for the current 8-channel WINeR-7 system prototype, especially when the Tx-Rx separation is large. At the nominal Tx-Rx distance of 2.0 m, the effective number of bits (ENOB) is 8 bits considering the INL and DNL measurements in Fig. 4.21.

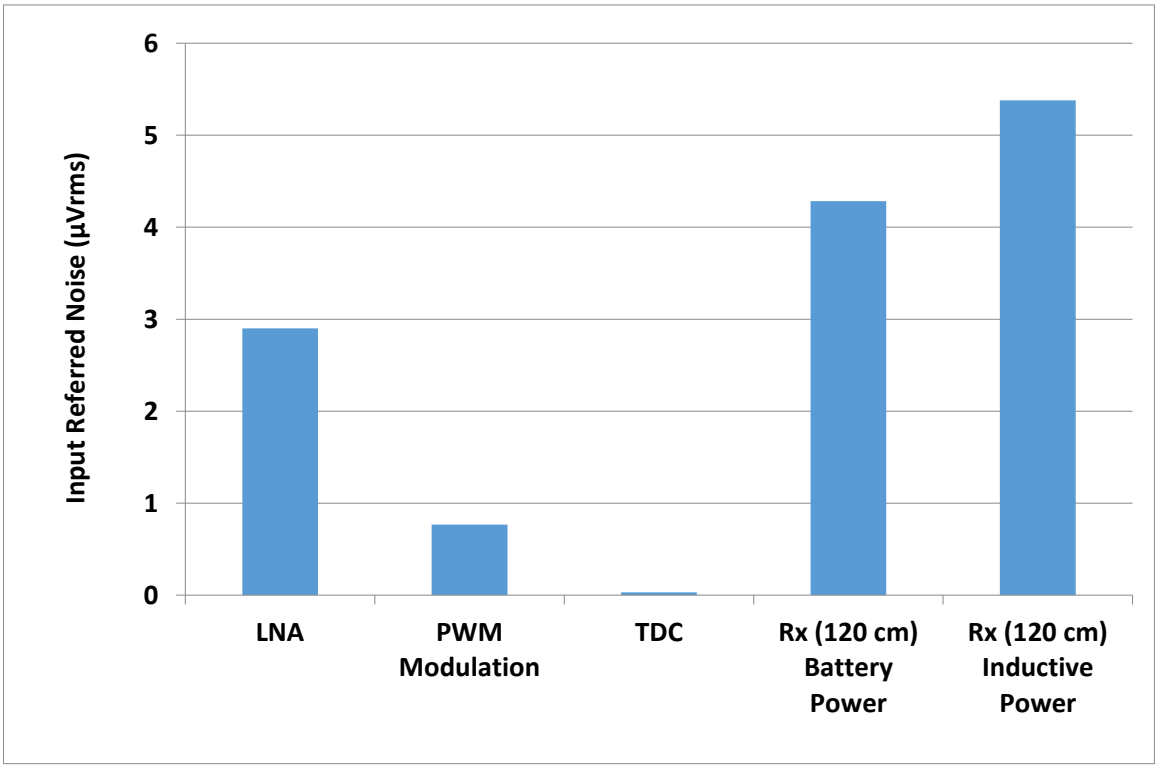


Fig. 4.23. Noise contributions of different WINeR-7 blocks at 21 kSps.

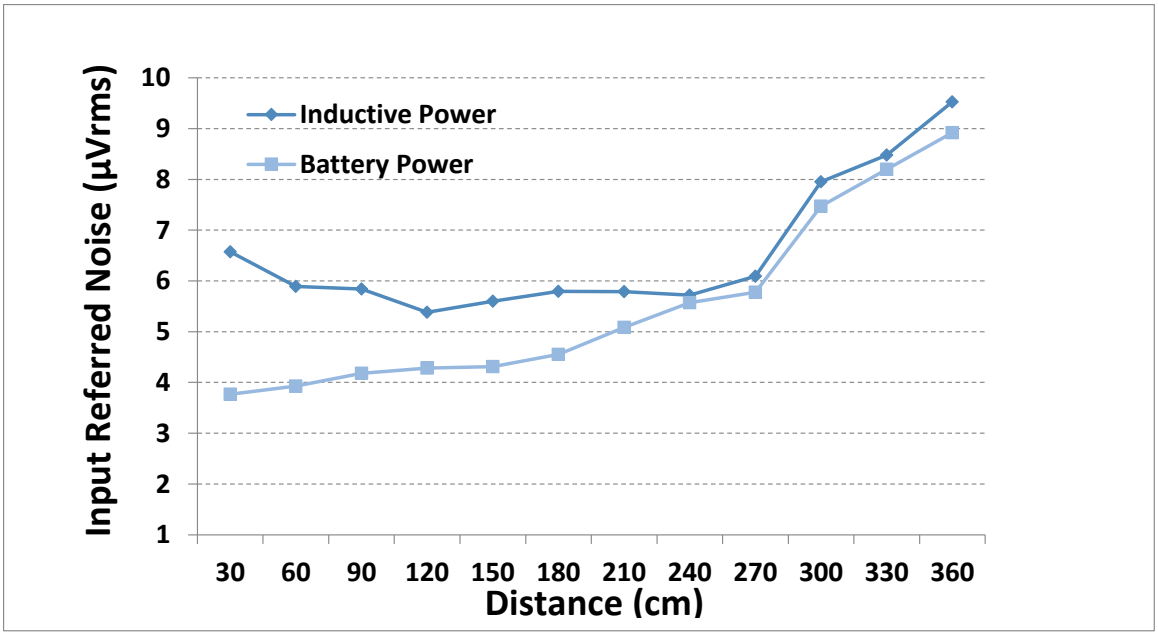


Fig. 4.24. Noise measurement of the entire WINeR-7 vs. Tx-Rx distance.

Fig. 4.24 illustrates that when the Tx-Rx separation is less than 120 cm in the inductive power operation, higher noise is measured within the shorter distance due to RF interference from a wireless power transmission system. If the Rx antenna is overly close to the Tx, the antenna can detect not only a desirable RF signal but also the harmonics of the power carrier signal at 13.56 MHz. Fig. 4.24 indicates that 120 cm is the optimal Rx antenna position.

Table 4.1 compares the specifications of the WINeR-7 system against other recent studies. The input referred noise of the WINeR-7 system was measured by grounding the LNA inputs and conducting an FFT on the recorded signal for 10 s. Integration of these curves from 1 Hz to 10 kHz resulted in an input-referred noise of 5.38 μV_{rms} for a Tx-Rx distance of 120 cm.

Table 4.1
WINeR-7 Specifications and Benchmarking

Publication	This work	[16] 2012	[15] 2012	[34] 2011	[67] 2014
Technology	0.35µm CMOS	0.13µm CMOS	65 nm CMOS	0.35µm CMOS	0.5µm CMOS
V_{DD} (V)	1.8 for AFE 4.2 for Tx	1.2	0.5	1.5	1.5, 3
Die size (mm^2)	5.0 × 2.5	5 × 5	0.13	3.3 × 3.3	2.85 × 3.84
No. of channels	8	96	1	4	9
Total power (mW)	51.4	6.5	0.005	0.42	5
Power/ch. (µW)	19.3	68	5.04	26.9	55.68
Area/ch. (mm^2)	0.29	0.26	0.13	-	-
Sampling rate (kSps/ch)	21.48	31.25	20	63 (Max.)	200
LNA gain (dB)	40	-	> 32	51.9 - 65.5	39.35
LNA input ref. noise (μV_{rms})	2.90	2.2	4.9	3.12	4.58
LNA HPF (Hz)	1 to 800	<1, 280	300	1.1 - 525	178 - 302
LNA LPF (kHz)	3 to 8	10	10	5.1 - 12	6.92 - 8.13
Resolution (bit)	8	10	8	10	-
System input ref. noise (μV_{rms})	5.38 (BW: 1 Hz-10 kHz, Distance: 120 cm)	-	-	-	4.58

4.8. UWB Communication with the WINeR-7 System

4.8.1. UWB Transmitter

Fig. 4.25 presents a schematic of the sub-GHz-range PWM-IR-UWB. Because the 0.35-µm process is not suitable to design a UWB Tx with a range of 3-5 GHz, the frequency has been reduced to < 1 GHz. In this Tx, the rising and falling edges of the PWM are detected and three pulses with a ns delay are created per edge, as shown as S_1 in the Fig. 4.25 inset. A simple all-digital pulse generator creates three sharp pulses. Three pulses are employed to increase the transmitted power for each edge to facilitate the detection of these small pulses by the receiver over long communication distances. Fig. 4.26 presents the measurement results of the UWB Tx when the output was connected to the oscilloscope that was terminated by 50 Ω. The input is the PWM signal that is directly fed by the recording chip on the same die. One pulse is generated per edge

of the PWM signal. Considering that the ENOB for the WINeR-7 system is ~8, the proposed PWM-IR-UWB reduces the power consumption by 4-fold compared with UWB digital communication using pulse-position modulation (PPM). Details of the UWB Tx are provided in [70].

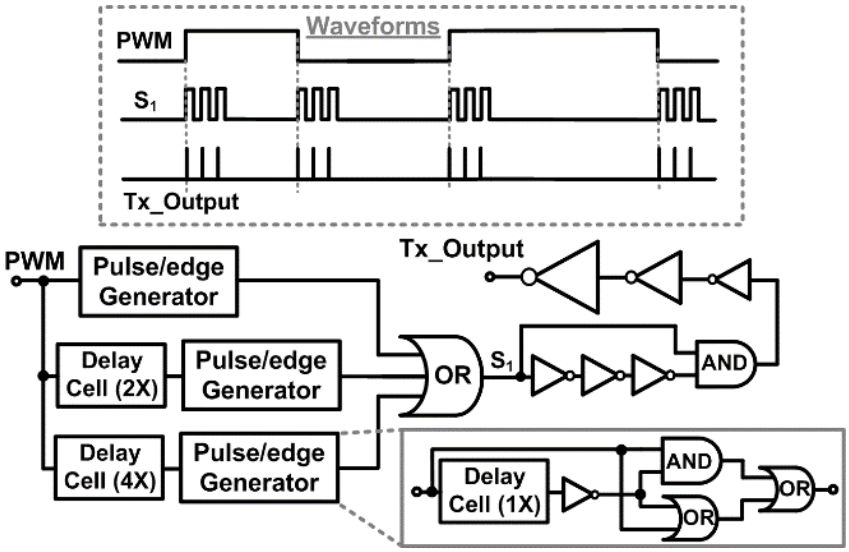


Fig. 4.25. Schematic of the sub-GHz-range PWM-IR-UWB (The author acknowledges Dr. M. Kiani for designing this block).

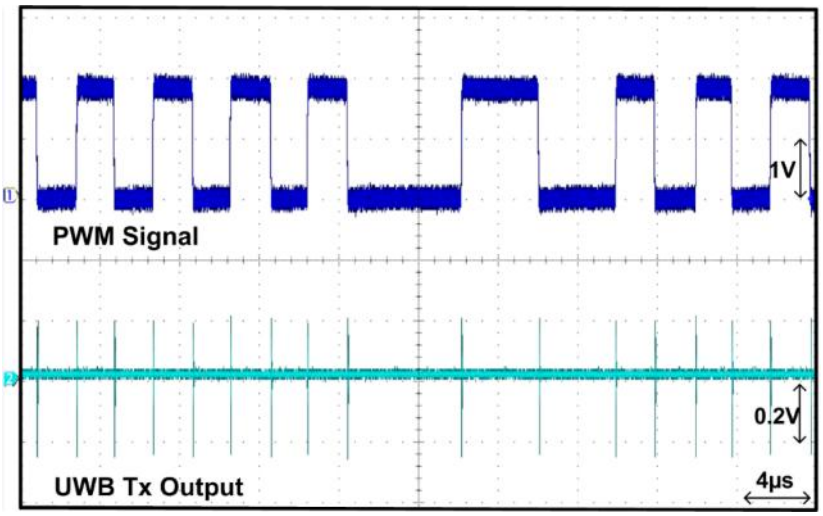


Fig. 4.26. Measurement results of the sub-GHz-range PWM-IR-UWB.

4.8.2. UWB Receiver

A custom-designed UWB Rx using commercially available off-the-shelf (COTS) components was designed, and a schematic is shown in Fig. 4.27. The received RF signal from the antenna is amplified and filtered through an RF LNA and band-pass filters. The amplified and filtered RF signal is downconverted to the baseband through an RF power detector. In the baseband, the downconverted signal is amplified, filtered, and converted to sharp pulses through a comparator. Similar to the WINeR-7 FSK receiver, an FPGA board will recover a PWM signal from the sharp pulses, digitize it, and transmit it to a computer. The size of the populated UWB receiver board, which is shown in Fig. 4.28, is 8.3 × 3.0 cm. The UWB Rx uses +12 V of a single power supply; its current consumption is 180 mA.

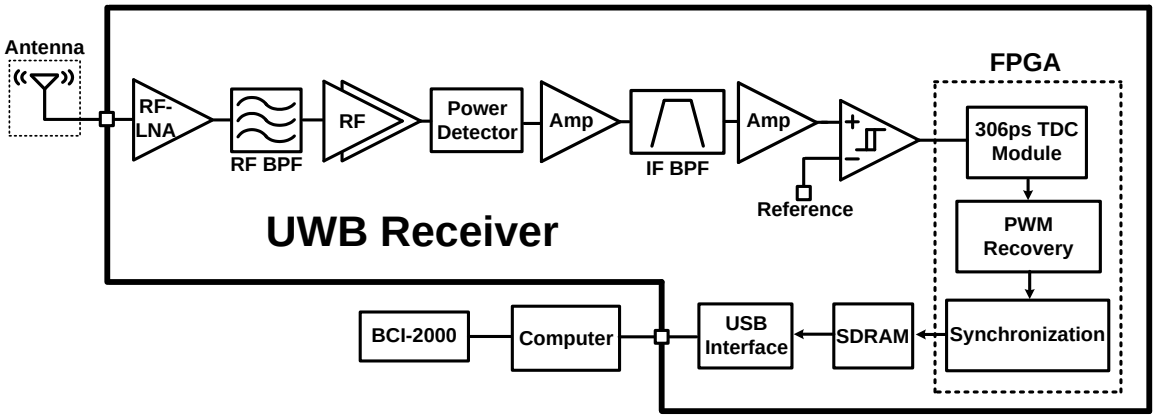


Fig. 4.27. Schematic of the UWB receiver.

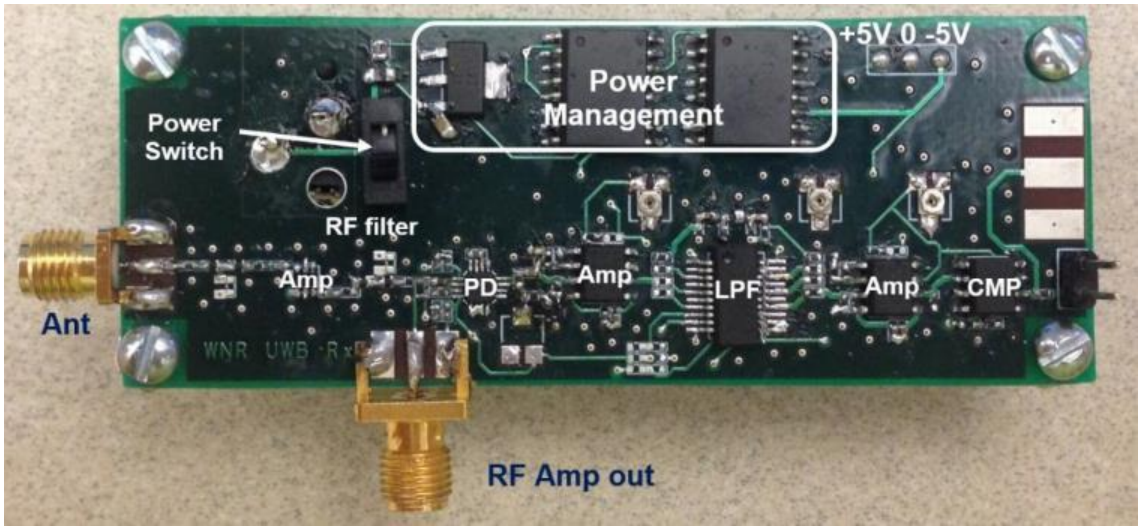


Fig. 4.28. UWB receiver board.

The UWB Tx and Rx were tested with a distance of 40 cm between the Tx and Rx antennas. For the Tx, a custom designed monopole antenna was used to verify the system function. For the Rx, a log periodic PCB directional antenna from Ettus Research (Santa Clara, CA, USA) with a range of 400 MHz to 1 GHz was used. In this set-up, the received signal spectrum after RF amplifiers is shown in Fig. 4.29. The UWB signal spectrum exhibits a peak at 470 MHz, and its bandwidth is approximately 600 MHz.

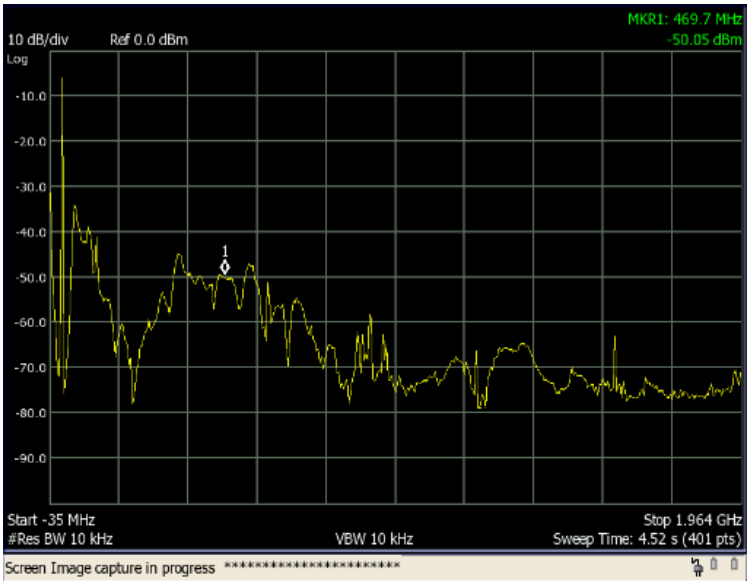


Fig. 4.29. Received RF spectrum output after the RF Amplifer.

The TDC algorithm in the FPGA for the UWB Rx is similar to the WINeR-7 FSK Rx in terms of gate delays. However, the algorithm should be modified because it is difficult to distinguish the start and end signals between adjacent pulses. The TDC method from the OOK Rx described in [45] is shown in Fig. 4.30a. Here, only the period in which the PWM signal is high is important. Thus, the PWM can be digitized by a combination of clock signal and gate delays, as described in Fig. 4.30a. However, the UWB pulses do not exhibit a period in which the PWM signal is high. Therefore, every period between adjacent periods should be digitized, as shown in Fig. 4.30b. The valuable alternate periods, which correspond to the high period of the PWM signal, can be distinguished during the channel synchronization period.

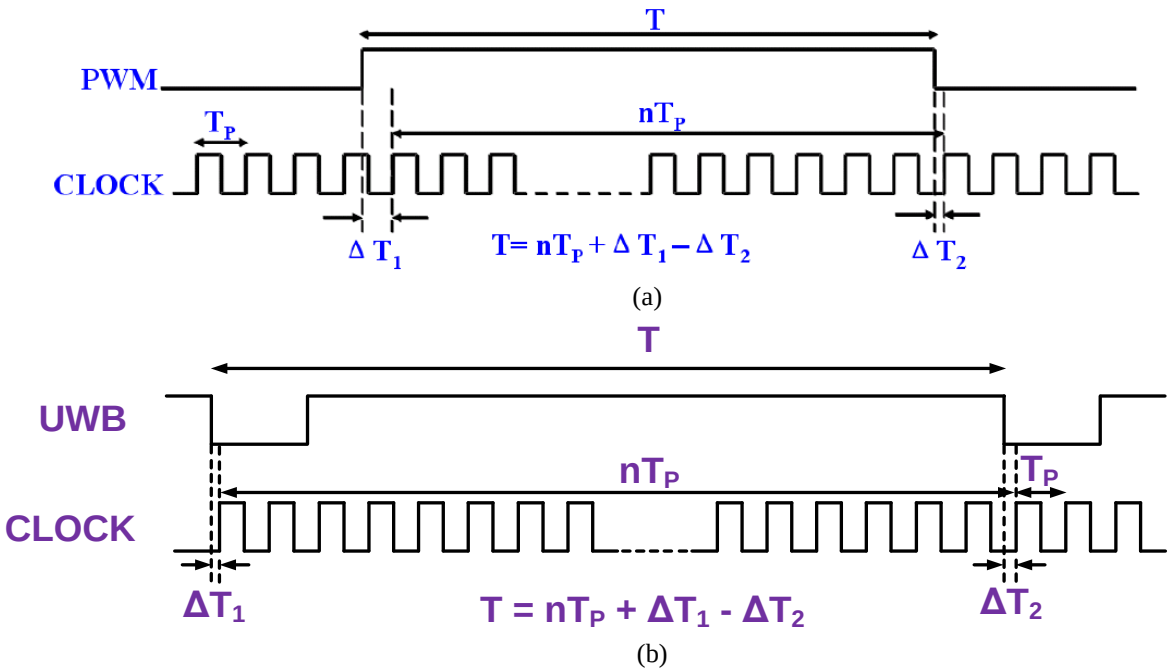


Fig. 4.30. Two different TDC methods from (a) OOK Rx and (b) UWB Rx.

The simultaneous eight-channel recorded signals shown in Fig. 4.31 were wirelessly recorded via UWB communication when Channel 1 received a sinusoidal waveform of 500 µVpp at 1 kHz and the remaining channels were grounded at a distance

of 40 cm between the Tx and Rx antennas. This measurement demonstrates PWM-UWB communication with a WINeR-7 system.

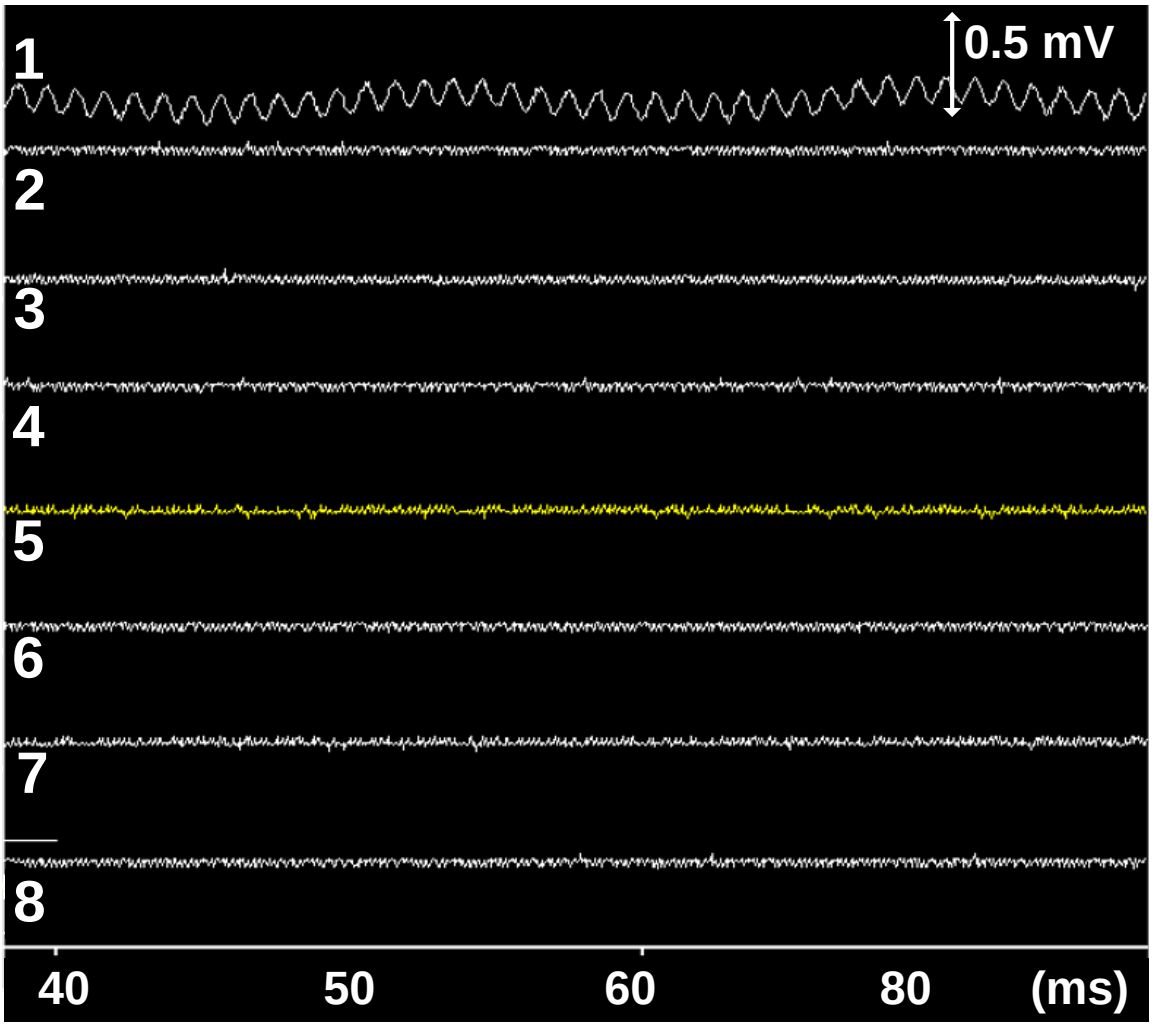


Fig. 4.31. Simultaneous eight-channel bench-top wireless recording with a WINeR-7 system with the UWB communication at a Tx-Rx distance of 40 cm (BCI2000 GUI).

CHAPTER V

ANIMAL EXPERIMENTS WITH THE WINER-7 SYSTEM

5.1. Battery-Powered Animal Experiments

A compact (3.2 × 3.0 cm^2) WINeR-7 mobile unit for battery-powered animal experiments was designed and is shown in Fig. 5.1; all experiments were conducted with prior approval from the Institutional Animal Care and Use Committee (IACUC) at the Georgia Institute of Technology and Emory University. In the *in vivo* experiment, 16 electrodes were implanted in the hippocampus of a Sprague-Dawley rat; eight of the electrodes were connected to the WINeR-7 system to record local field potentials (LFPs). The rat was anesthetized and carried the WINeR-7 headstage, for which the bandwidth was set to the range of 1 Hz to 10 kHz. Its recordings were compared with recordings from a custom hardwired system with commercial components, as described in [56]. The hard-wired system bandwidth was set to the range of 1–500 Hz for LFPs. The recorded neural waveforms at different times are compared in Fig. 5.2. Because of its wide bandwidth, the WINeR recording in Fig. 5.2a exhibits both high-frequency interference and LFP recordings. After the offline data of the WINeR recording were processed, the same bandwidth data were processed, as shown in Fig. 5.2c. The processed data became similar to the hard-wired recording in Fig. 5.2b demonstrating that the WINeR-7 system can replace the hard-wired recording system.

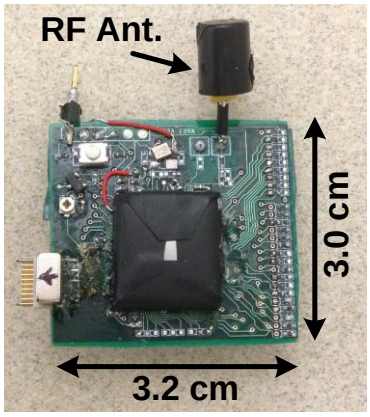
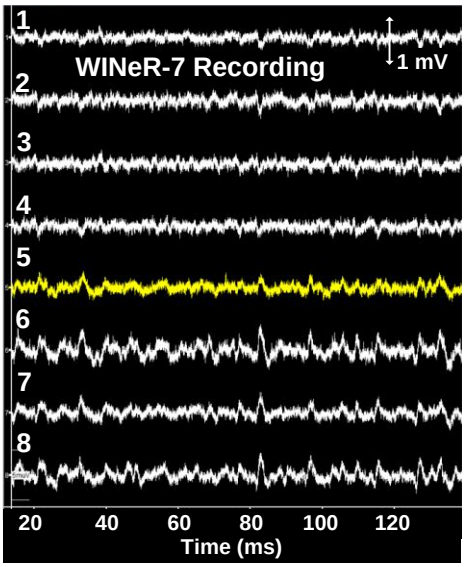
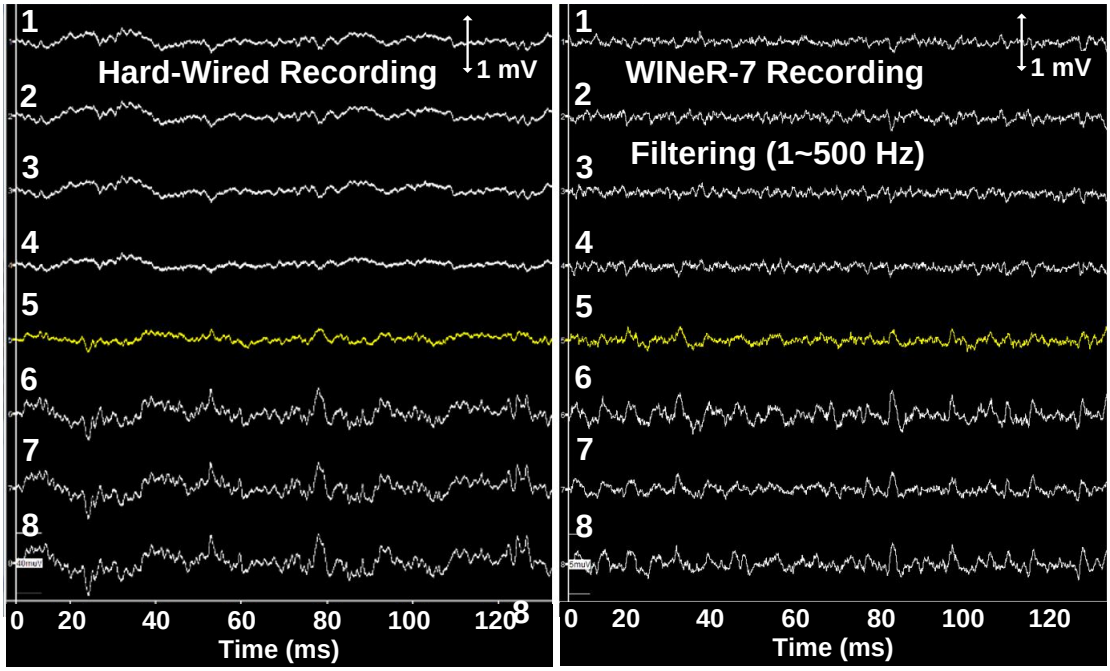


Fig. 5.1. WINeR-7 headstage for battery-powered animal experiments.



(a)



(b) (c)

Fig. 5.2. LFP recordings from (a) the WINeR-7 recording with a bandwidth from 1 Hz to 10 kHz, (b) the hard-wired system, and (c) the offline data process of the WINeR-7 recording with a bandwidth from 1 Hz to 10 kHz (The author acknowledges Dr. B. Mahmoudi for helping this animal experiment).

5.2. Closed-Loop Powering Implementation

When the WIneR-7 system is operated in the inductively powering mode, the most critical issue is the stabilization of received power. This issue is challenging when the distance between a power Tx and power Rx varies due to the movement of an animal

subject. To resolve this issue, the WINeR-6 system achieved the closed-loop powering operation through the RF link. In this approach, the attenuated rectifier output voltage was transferred to the Rx and used to control the wireless power transmission. However, a drawback for this approach is that the RF back telemetry does not work when the received power is either not sufficiently large or excessively high. To transmit the correct RF signal, the system should turn on correctly; however, this operation becomes difficult without the correct back telemetry signal. In addition, if the closed-loop link is broken during operation, it is difficult to recover due to the lack of a correct feedback signal. This situation can place the system and an animal at risk of danger from high power and generated heat.

The RF back telemetry method was improved in the WINeR-7 system. When the received power is out of the normal operation range, the output frequencies of the RF FSK Tx change due to a variation in the supply. In this case, the varying output frequencies can be used to indicate the rectifier output voltage because the WINeR-7 Rx can detect the RF frequencies by the TDC algorithm introduced in Section 2.2.1.4.2. The rectifier output voltage of the WINeR-7 headstage and the downconverted frequency of the WINeR-7 Rx under variations in the power amplifier voltage for inductive powering were measured and are presented in Fig. 5.3. When the PA voltage increases, the rectifier output voltage also increases; however, the downconverted frequency decreases until the rectifier output voltage reaches 4.5 V. The downconverted frequency does not decrease when the rectifier output voltage is higher than 4.5 V because the supply of the RF FSK Tx does not change; the supply remains constant because the LDO operates to stabilize the system power supply if the rectifier output voltage exceeds 4.5 V. Because the new RF closed-loop operation utilizes this phenomenon, the PA power can increase if the rectifier output voltage is less than 4.5 V by observing the downconverted frequency of the WINeR-7 Rx. When the rectifier output voltage exceeds 4.5 V, the PA voltage can decrease by observing the attenuated rectifier voltage transmitted from the RF link. In

this manner, automatic frequency tracking can also be implemented, which differs from the description in Section 2.2.1.4.2. The RF transmission frequency is fixed and the local oscillator frequency of the Rx varies in the Section 2.2.1.4.2, whereas the local oscillator frequency is fixed but the RF transmission frequency is varied by controlling the PA voltage in the new method. In this manner, the closed-loop operation stabilizes due to a corrected back telemetry signal when the received rectifier output voltage is small.

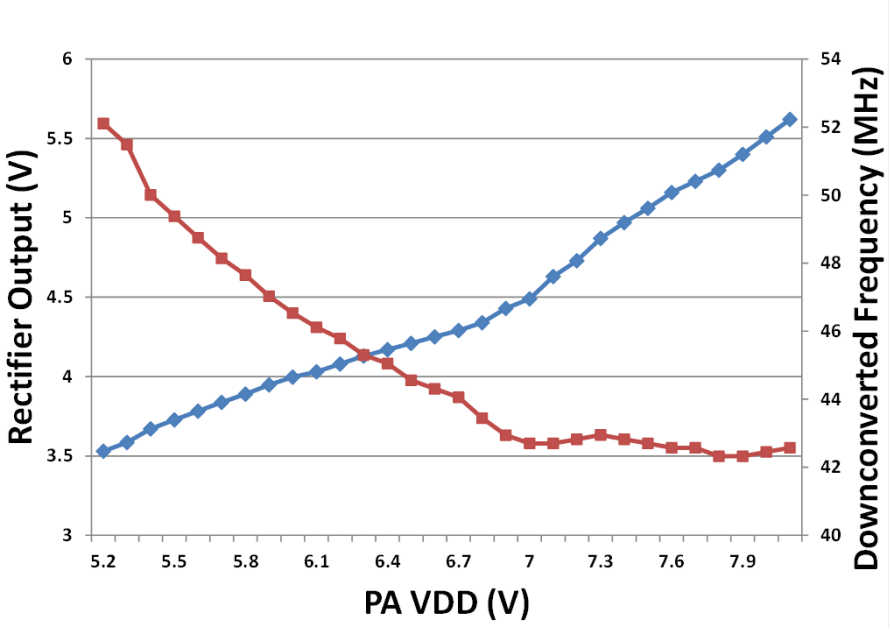


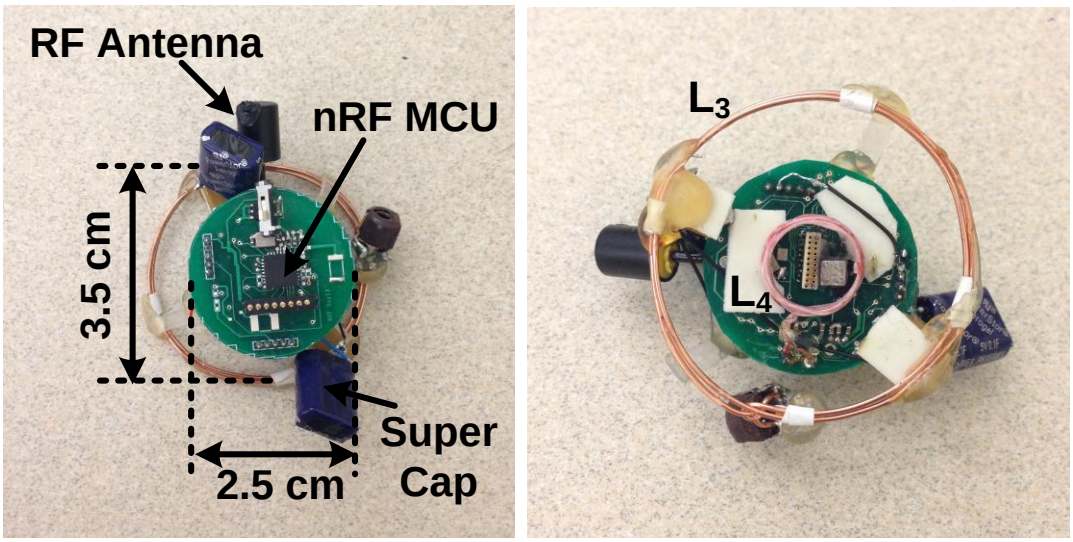
Fig. 5.3. Rectifier output voltage of the WINeR-7 headstage and the downconverted frequency of the WINeR-7 Rx when the power amplifier voltage for inductive powering varies.

5.3. Inductively Powered Freely Moving Animal Experiment

To demonstrate the functionality of the WINeR-7 system with an inductively powering system, the entire system was tested *in vivo* in a 30 × 28 × 18 cm^3 standard home cage. A Kinect from Microsoft (Redmond, WA) was installed above the cage to localize the animal position to turn on/off the Tx coils. The images, which were taken by the Kinect every 33 ms, were processed, and the position of the animal was determined by subtracting the images taken from the cage with the animal from the images taken

before the animal was placed in the cage. An IGLOO FPGA received the localization data via a WLAN link and controlled the switches in series with the coils based on the position of the animal. An nRF24LE1 microcontroller on the mobile unit was used to program S2P registers in the WINeR-7 SoC for initialization, and the RF back telemetry method described in the previous section was used to close the power loop. On the Tx side, a single bit that indicates whether the rectifier output voltage is higher or lower than 4.5 V was transmitted to the closed-loop power control unit (CLPC) via XPORT communication. In the CLPC unit, the data are received by an MSP430 microcontroller, and a digital potentiometer in the resistive feedback of a DC-DC converter controls the supply voltage of a class-C PA from 5 to 20 V. Two 200-mF supercapacitors were connected to the positive and negative rectifier outputs to supply the mobile unit when the inductive coupling is weak due to the large distance or rotation of the coil in the mobile unit. Additional details of the closed-loop external powering system are provided in [70] and [72].

The fabricated mobile unit and coils are shown in Fig. 5.4. The geometry of the coils in the mobile unit i.e., L_3 and L_4, were optimized based on the design procedure in [68] to maximize the PTE. The diameter of L3 is 3.5 cm, the diameter of L4 is 1 cm, and the diameter of the PCB is 2.5 cm.



(a) (b)

Fig. 5.4. WINeR-7 headstage for inductively-powered animal experiments, (a) top view, (b) bottom view.

The animal experiment set-up is shown in Fig. 5.5a, in which the *in vivo* results for the PA supply voltage after 40 s are displayed. The closed-loop system maintains the rectifier output voltage at 4.5 V by adaptively changing the PA supply with animal movements. In addition, the LFP recordings from the WINeR-7 system, which is operated by inductive powering with a bandwidth of 1 Hz to 10 kHz, is shown in Fig. 5.6.

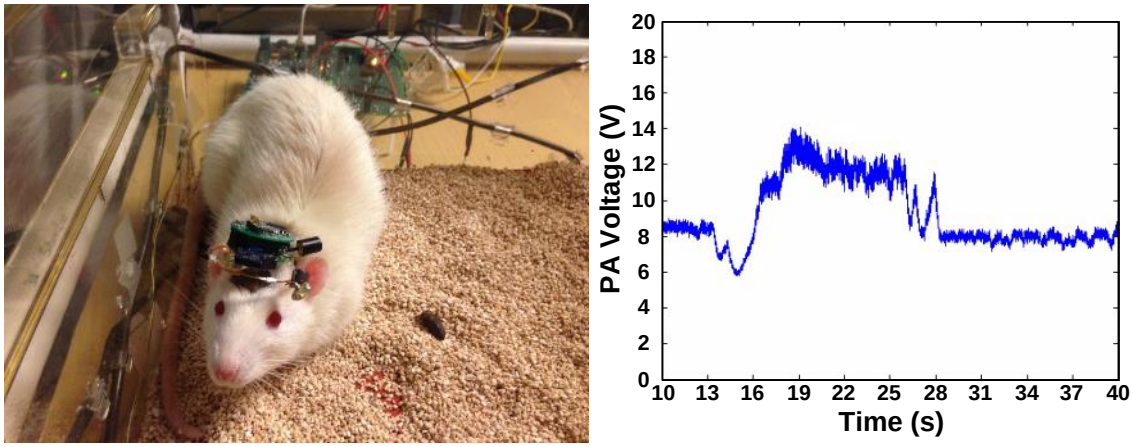


Fig. 5.5. (a) Animal experiment set-up, (b) The *in vivo* results for the PA supply voltage during 40 sec (The author acknowledges Byunghun Lee and Dr. Mahmoudi for helping this animal experiment).

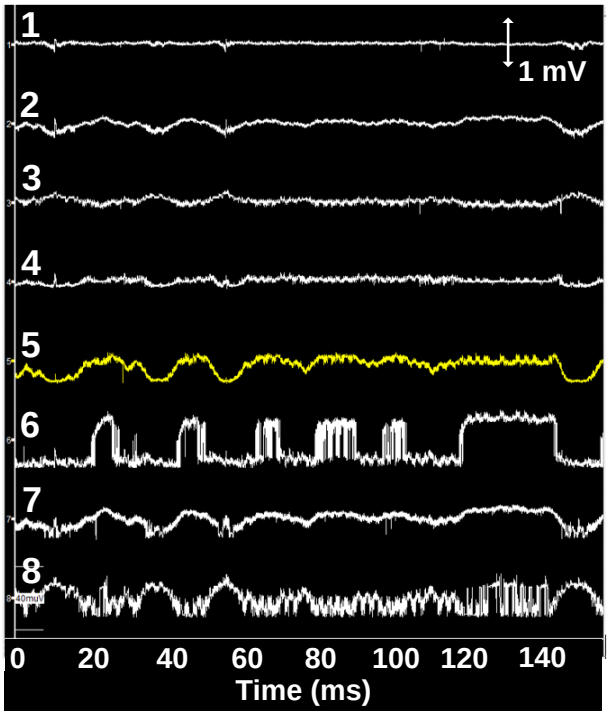


Fig. 5.6. LFP recordings from the WINeR-7 system operated by inductive powering with a bandwidth of 1 Hz to 10 kHz.

CHAPTER VI

CONCLUSIONS AND FUTURE STUDIES

This dissertation focuses on developing smart solutions by utilizing innovative system- and package-level designs with analog and digital circuit techniques for an inductively powered ultra-low-power and multi-channel wireless integrated neural recording system, which has resulted in several conference and journal publications [61], [65], [73]-[76]. A neural recording amplifier design with low power and low noise is critical to wireless neural recording systems. A power scheduling mechanism with a multi-channel analog front-end has been developed to improve the noise efficiency factor while not increasing the power consumption. The developed dual-slope charge-sampling AFE can simultaneously amplify and filter neural signals and easily modulate them into PWM signals with low power consumption. A wideband multi-antenna receiver with a real-time data acquisition system for multi-channel neural recordings enables wireless recording from animals in large arenas. In addition, a PWM-IR-UWB receiver was designed and tested with the WINeR-7 UWB Tx for an ultra-low-power wireless neural recording system. A robust closed-loop power transmission system based on RF back telemetry can manage wireless powering into the headstage of a freely moving animal subject without disrupting its neural recording function. This chapter summarizes the results and scientific contributions of this dissertation and proposes future studies.

6.1. Conclusions

Multi-channel electrophysiological neural recording is essential for developing effective therapies for neurological diseases, such as epilepsy, PD, and Alzheimer's disease. The wireless operation of these systems exhibit several clear advantages compared with wired operations, such as the elimination of tethering effects. However, hardwired systems remain more popular than their wireless counterparts in the majority of neurophysiology laboratories. Wireless systems are hindered by a variety of problems,

such as limited battery lifetime, limited wireless coverage area, and poor connectivity. As a result, wireless systems are considered unreliable for state-of-the-art behavioral neuroscience studies.

An 8-channel WINeR-7 system with a novel DSCS AFE architecture has been developed to address these challenges. The DSCS AFE converts neural signals into currents, and the currents charge capacitors that are connected to a comparator. In this manner, the neural signals are converted to PWM signals. The presented DSCS-AFE simultaneously achieves amplification, filtering, and sampling, while consuming a small amount of power. The output of the DSCS-AFE produces a PWM signal that is proportional to the input voltage amplitude. A CSR utilizes TDM of the PWM pulses to create a pseudo-digital TDM-PWM signal that can feed a FSK transmitter. The 8-channel system-on-a-chip was fabricated using a 0.35-μm CMOS process, occupying 5.0×2.5 mm^2 and consuming 51.4 mW of power from 1.8 V and 4.2 V supplies. The measured input-referred noise for the entire system, including the receiver located at 1.2 m, was 5.38 μV_{rms} in the 1 Hz–10 kHz range when the system is inductively powered. For each channel, the sampling rate is 21.701 kHz and the power consumption is 19.3 μW.

In an *in vivo* experiment, 16 electrodes were implanted in the hippocampus of a Sprague-Dawley rat, with 8 of the electrodes connected to the WINeR-7 to record LFPs. The rat carried the WINeR-7 headstage, which was inductively powered inside an EnerCage home cage (HC) system. In this system, the closed-loop inductive power control with optimal coil design provides high-power transfer efficiency while maintaining the received power at the headstage despite animal movements. The WINeR-7 system enables neuroscientists to eliminate cables from their electrophysiology experiments of freely behaving animal subjects, which are awake, while acquiring high-density and high-fidelity neural signals over extended periods of time.

6.2. Future Studies

6.2.1. Animal Experiments

The WINeR-7 headstage for the animal experiment is large and heavy for rats to carry. For successful animal experiments, a smaller and lighter headstage is desirable to prevent bias of an animal subject's behavior. First, the piggyback board with nRF MCU can be removed by designing new PCB and wirebondings. Initially, the current MCU only exists for S2P register programming. Therefore, its use is not efficient during the animal experiments. Instead of S2P register programming, the required digital pins can be directly wirebonded to the WINeR-7 SoC. In this manner, we can remove the piggyback board and reduce the system power consumption. To reduce the headstage size, the receiver coils L_3 and L_4 can also be reduced. The flip chip technique can be used to significantly shrink the headstage size.

6.2.2. UWB Communication

The most power-consuming block of the WINeR-7 system is the RF FSK transmitter block. If PWM-UWB communication is improved with compatible performance to the FSK communication, the power consumption of the system will be significantly reduced. Although the UWB communication was already demonstrated with the WINeR-7 system as described in Section 4.8, the performance can be increased by developing various components. First, optimum UWB antennas for the transmitter and the receiver should be designed. Second, the UWB Rx can be improved by increasing the RF gain. In addition, automatic gain control can be implemented to compensate for the variable distance between the Tx and Rx. Finally, a high-frequency UWB Tx with a deep submicron process should be designed. Because the 0.35-μm process is not suitable to design a UWB Tx with a range of 3–5 GHz, the frequency of the WINeR-7 system has been reduced to < 1 GHz. The low UWB frequency becomes problematic when the

system is inductively powered. Although the 13.56 MHz frequency of the inductive-powering RF signal is lower, the harmonics of 13.56 MHz can affect the low UWB in-band signal. To minimize the interference, a UWB Tx with a range of 3–5 GHz, which can be designed with the deep submicron process, is desirable.

6.2.3. WINeR-8 SoC Design

The proposed WINeR-7 SoC exhibits superior noise and power characteristics compared with the state-of-the-art neural recording systems, as shown in Table 4.1. However, the identified drawbacks should be improved in the next WINeR system, which is named WINeR-8. First, an unwanted reset signal for the S2P register was generated due to an abrupt power change because the system body voltage VBB differs from the system VSS voltage. In the WINeR-7 system, VBB is connected to the negative rectifier output voltage, and VSS is connected to the negative regulator output voltage. Thus, when the negative rectifier output voltage changes suddenly, the voltage between the VBB and VSS can change, which can generate unwanted digital signals, such as the S2P register reset signal. To resolve this issue, the triple-well process can be employed, or the VBB and VSS can be connected assuming single-supply operation of the WINeR-8 SoC.

A power management unit is critical for an inductive powering operation. The fabricated resistance value of the band gap reference (BGR) circuitry becomes three times larger than the designed value due to an inaccurate process design kit (PDK). External resistors were used in the WINeR-7 system to compensate for this mismatch. An accurate resistance value should be used in the WINeR-8 design. In the WINeR-7 measurement, the super-capacitors discharge faster than the simulation. The super-capacitors discharge from not only the load but also the rectifier output connection. To prevent this outcome, a separate super-capacitor charger control circuitry should be implemented in the WINeR-8 design. The load shift key (LSK) method can be implemented in the WINeR-8 for the closed-loop powering operation.

In the DSCS AFE, mismatches in the transconductance of the OTA, discharging currents, and capacitors may occur in each channel. These mismatches result in severe channel-to-channel gain and offset variations. To minimize the undesirable gain and offset variations, the WINeR-8 system can be designed with a DSCS auto-calibration feature. If the system operates in calibration mode, the LNA inputs will be shorted to the ground and the OTA gain and discharging currents of each channel will be calibrated. This calibration will be performed during the system initialization period when the system is turned on. Thus, the channel-to-channel gain and offset variations in multi-channel recording will be minimized. In addition, the WINeR-8 AFE will feature a higher-order bandpass filter, which is desirable for recording various signals. Multi-channel stimulators and robust stimulus-artifact rejection are also important features of the WINeR-8 for closed-loop operations. The Tx output power and frequency should be easily adjustable for a robust wireless link.

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