VERSATILE AUTONOMOUS SMARTGRID TESTBED (VAST)

Phase 1 Design Document

Revision: A

Date: 4/4/2011

Document Prepared for DRS-TEM

By: Nathan Ainsworth

Mitch Costley

Alyse Taylor

Prof. Santiago Grijalva

Advanced Computational Electricity Systems (ACES)

Table of Contents

1. Introduction

This document describes the requirements, design, and implementation of Phase I of the Versatile Autonomous Smartgrid Testbed (VAST). VAST is being developed by the Advanced Computational Electricity System (ACES) laboratory at Georgia Institute of Technology for use in testing and verifying autonomous Smartgrid, microgrid, and distributed generation algorithms.

In Phase I, the VAST will be developed primarily for the purpose of demonstrating a distributed control architecture for synchronization and power sharing of inverter-based sources on an autonomous AC electric microgrid, or "Smartgrid". However, VAST is envisioned as a flexible, modular system for rapid prototyping and testing of autonomous algorithms for control of Smartgrids. It is being designed with the intention of being expanded into testing of a large range of Smartgrid algorithms, including distributed device control, autonomous Smartgrid system control, protection, situational awareness, and market operations. When completed, VAST will be a significant tool for Smartgrid development and ultimately will serve as a demonstration of a flexible, robust, autonomous Smartgrid architecture.

VAST uses a modular design to allow for rapid reconfiguration to allow an easy approach to testing new algorithms, software, and hardware. It operates at low voltages and currents to enable easy approachability, low expense, safe operation in the ACES lab at Georgia Tech, and manageable transportation. This modular approach also allows it be easily expanded to an arbitrary number of sources, buses, or loads and allows new hardware or software to be easily added to the system. Moreover, the VAST is designed for scaling to higher voltages without changes to the architecture. Upgrading will require replacement of hardware with appropriately rated devices, but a lengthy redesign will not be needed.

2. Purpose and Design Principles

2.1. Desired Functionality

The VAST system will accomplish the following:

- Demonstrate, in hardware, synchronization and power sharing of inverter-based sources without need for communication
- Allow testing of parallel communication and power networks (networks of intelligent power devices)
- Allow for development and testing of system-level algorithms of the following types:
    - Centralized or decentralized device-level feedback control algorithms of inverter-interfaced or machine-interfaced sources
    - *Smartgrid Management and Automation*
        - *Parallel operation of inverters*
        - *Synchronization of arbitrary number of inverter-based sources*
        - *Synchronization of inverter-based generation, machine-based generation, and controllable loads*

  - *Power System-level optimization and control algorithms*
  - *Situational Awareness algorithms*
  - *Protection algorithms*
- Provide a platform for development of a software architecture for Smartgrid
- Provide a platform for hardware demonstration of the operation of Smartgrid algorithms
- Determine required capabilities of a communications architecture for Smartgrid applications
- Allow for rapid testing of communication architectures for Smartgrid applications
- Allow for rapid prototyping of new low-voltage inverter-interfaced devices and new inverter architectures
- Allow for rapid testing of the above under a variety of network structures and conditions
- Able to be safely operated in the ACES laboratory in the Van Leer building on Georgia Tech campus

2.2. Design Principles

- Scaled voltage and power to allow low cost, rapid development, ease of use, safety, and low profile
- Use generic (Commercial Off-the-Shelf) components and software wherever practical
- Use a well-developed, integrated software measurement and automation environment to allow for common interfaces and enable future expansion
- Use simple, common hardware interfaces to allow for interface flexibility and easy reconfigurability
- Virtualized separation between distributed components
- Virtualized communication architecture to allow for flexibility
- Modularity of components
- Incremental implementation (in hardware, in software, in capabilities, in voltage and number of components)
- Layered system architecture to allow for system to be viewed at different scales of time and space
- In Phase I, focus on capabilities required for demonstration of inverter synchronization and power sharing, but leave flexibility for development of additional capabilities in future phases

3. System Architecture

VAST is intended as a test and demonstration system for distributed Smartgrid architectures. This means that the architecture of the system itself is under test. Therefore, it is desirable that the system architecture, particularly the characteristics of less understood functional components, be flexible and easily reconfigurable. This will enable rapid prototyping and testing of new architectures and functional module implementations.

Operational AC Smartgrids may contain large numbers of devices. This necessitates the use of local distributed controllers, which interact with each other only through the power network and

communications network. This "separation" between distributed devices, along with the capabilities and limitations of both the power and communications network governing their interactions, are therefore the defining characteristics of the type of system that VAST is intended to simulate.

The physical characteristics of AC power networks are well understood, and they are relatively easy to implement in hardware. In addition, the VAST system is intended to serve as a platform for hardware testing and demonstration of Smartgrid architectures and algorithms. Therefore, in VAST, the power network will be implemented in low-voltage hardware.

However, communications architectures, along with their capabilities and limitations, are widely varying. The requirements of the communication architecture for management of an AC electric network are not well understood. Another major purpose of the VAST system is the determination of the requirements for such an architecture and how it might be built. This requires utmost flexibility in the implementation of the VAST communication network, up to and including the assumption of an "ideal" communication network, in which devices can transfer data to other devices as easily as they can transfer data internally.

In VAST, this is accomplished by the use of "virtual" separation between distributed software components and a virtual communications network. This means that all distributed software is run in a single integrated computational device, with separation and communication between devices occurring in software. A dedicated "communication network" software module, simulating the characteristics of any desired communication system, serves as the medium of data transfer between other modules, which represent other intelligent system entities like device controllers, measurement collectors, and system controllers. This allows for determination of requirements for the communication and rapid prototyping of any desired communication medium without significant reengineering.

3.1. Functional Architecture Description

The VAST system uses a modular, layered hardware/software architecture to allow for easy, flexible testing of Smartgrid software. Figure 1 below shows a functional diagram of the VAST. Functional modules are color-coded to indicate the layer to which they belong. Some layers are implemented in software, while others are implemented in hardware. Some of the components or layers (indicated in *italics*) will not be implemented in Phase I but are included in the diagram as planned extensions in future phases.

The layered architecture of VAST was chosen to allow for modularity, incremental implementation, and simplicity of individual functional components. Common, flexible interfaces are developed between modules, and each module is self-contained and easily separated from the others. This allows for modules to be developed and tested independently. Modules may be replaced with simpler or more complex models or, in some cases, may be removed if unneeded. These capabilities will be used to allow a straightforward demonstration of inverter synchronization and power sharing in Phase I while enabling additional capabilities and components to be integrated and tested in future phases.

The planned layers of the VAST system are the Power Network layer, the Device Layer, the Local Device Control layer, the Situational Awareness layer, the Communication Network layer, the System Control layer, and the Market layer. Of these, the Power Network layer, the Device Layer, the Local Device Control layer, and the Situational Awareness layer will be implemented in Phase I, while the Communication Network layer, the System Control layer, and the Market layer will be left for future phases.

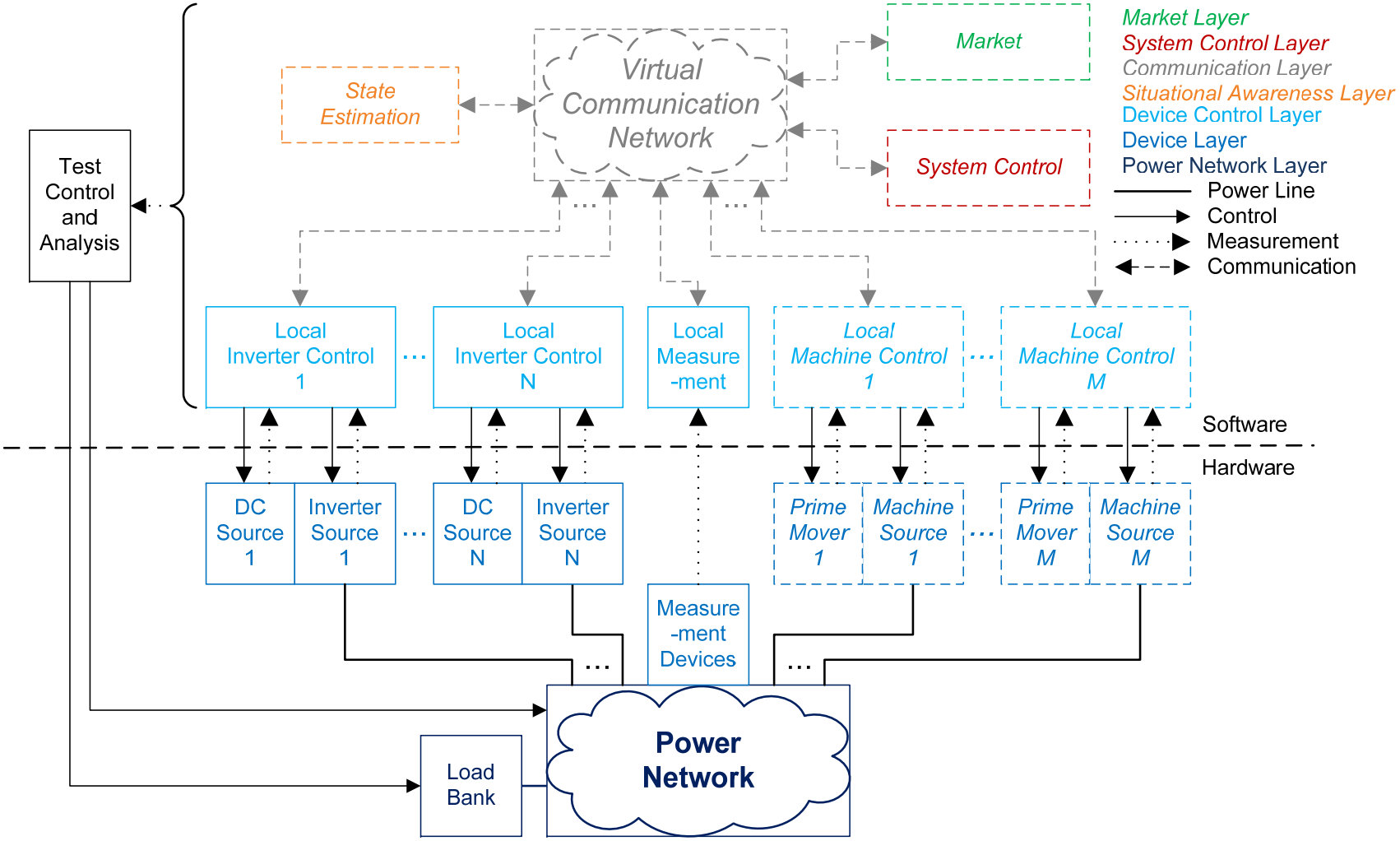


Figure 1 - VAST Functional Architecture

3.1.1. Power Network Layer

The Power Network layer contains the AC power network itself. It consists primarily of the physical wires, feeders, or transmission lines connecting sources to loads or other power devices. In an operational Smartgrid, this might include transmission lines, transformers, breakers, etc., which might span significant distances. In the VAST test system, the Power Network is represented by a 30 VRMS, easily reconfigurable network of wires, breakers, and static passive devices representing transmission models.

The Power Network layer also includes sensors which collect measurement data from throughout the network. These measurements are reported to the system control layer and test management layer.

In Phase I, all loads will be static and will be included in the Power Network layer. In future phases, controllable or dynamic loads will be integrated and may be considered devices on the Device layer.

Power networks can be structured in a wide variety of ways, including radial networks, meshed, star, etc. In Phase I, focus will be placed on the star network structure, in which all sources are connected to a common point, to which is directly connected all loads. Other network structures will be considered in future phases.

3.1.2. Device Layer

The Device layer consists of all controllable hardware devices that interact with the grid and are capable of generating, storing, using, or transferring power. Devices take local measurements, which are processed by their associated local controllers on the Device Control layer, and possibly reported to other functional modules through the Communication Network layer. They also accept controls from the same local controllers, allowing for fast local feedback control. This might include sources (inverters, generators, etc.), storage devices such as batteries, controllable loads, breakers, or even controllable transmission devices such as back-to-back converters, tapped transformers, phase-shifting transformers, etc. In Phase I of the VAST system, we will focus on inverter-interfaced sources.

The VAST system will eventually include an array of N inverter sources, an array of M machine sources, an array of measurement devices distributed through the power network, and possibly other power devices. In Phase I, there will be two inverters and no machines (N = 2, M = 0). It is planned to expand to six inverters and one machine in Phase 2 (N = 6, M = 1). While this is the limit of the presently used hardware, the VAST architecture allows for N and M to be expanded arbitrarily in software, and could also be expanded in hardware if desired.

The array of inverter sources (and the associated array of local controllers) is the primary focus of Phase I of the VAST system. Each inverter is a DC to AC converter. The DC sources are independent, and each inverter acts as the interface between a single DC source. On an operational Smartgrid and the AC microgrid, the DC source might be a photovoltaic panel, a diesel generator or wind turbine with a rectifier or AC-to-DC converter, a battery or ultracapacitor, etc. In Phase I of the VAST system, the DC

source is an isolating rectifier operating from 120 V utility. It is intended in future phases to replace this with more realistic sources, such as those from the above list.

In future phases, a machine generator will be added to the VAST system and will be included in the Devices layer. Each machine has an associated primary energy source called the prime mover. In an operational Smartgrid, this might be a diesel engine or natural gas turbine. In the VAST system, it will initially be a controlled DC motor.

A coupled DC source and inverter are assumed to be physically coupled and are therefore controlled by a single local controller. The same applies to a machine and its coupled prime mover.

The Devices layer also includes an array of measurement devices, distributed throughout the power network. In VAST, these measurements will be collected by a common multipurpose bus/line measurement device. This device measures four voltages (VAN, VBN, VCN, VNcmn) on a bus and four currents (IA, IB, IC, IN) on a line. Each measurement device is associated with a local control module on the Device Control layer, which processes its measurements and reports them to other functional modules via the Communication Network layer.

3.1.3. Device Control Layer

The Device Control layer consists of arrays of independent, distributed controller modules. Each module corresponds to and controls a device (or collection of physically coupled devices) on the Devices Layer. It receives measurement data only from its local device and sends control signals back to it. It interacts with other device control modules and other software layers only through the Communication Network layer.

The responsibility of each modules on the Device Control layer is to provide local control to its corresponding device on the device layer, which it can do using only local measurement data. Modules in this layer are capable of interaction with other modules through the Communication Network layer. However, since interaction on the Communication Network is high-latency (and possibly unreliable), it should not be required for stable operation. Stability through exclusively local observation and action is the unique and defining feature of distributed networks, and as a result, the Device Control layer is critically important to such networks.

In VAST, the modules of the Device Control layer are independent of each other in software but may be implemented in the same hardware device. This enables more flexible investigation of distributed architectures, as discussed in Section 2.2 above.

The primary functionality of Phase I of VAST, that is, synchronization and power sharing of inverter-based elements, is implemented mostly in the Local Inverter Control modules on this layer.

3.1.4. Communication Network Layer

The Communication Network layer implements a “virtualized” power system communication network, as discussed in Section 2.2 above. It simulates the capabilities and characteristics of any

desired communication medium. This enables exploration of the requirements of a communication network for Smartgrid applications, and experimentation in architectures for such a network.

In Phase I, no communication network is to be investigated, since all inverters will operate without communication with each other, and no system control, state estimation, or market layers exist. Therefore, a simplified Communication Network layer will be implemented to simply move measurement data from the Device Control Layer and Power Network Layer to the Situation Awareness module in the System Control layer for display to the user.

3.1.5. System Control Layer

The System Control layer is responsible for power system-level awareness, control, and optimization functions. These may include optimal power dispatch of sources, control of system-level devices such as a point-of-common coupling breaker, or high-latency coordination of response to events such as a fault or coupling or decoupling to an external grid. The System Control layer interfaces with other layers only through the Communication Network layer, and therefore it operates at a much lower update rate and much higher latency than the Device Control layer.

It is a design goal that transient stability and performance of the VAST Smartgrid does not require an operating System Controller. The System Control layer will not be designed or implemented in Phase I of the VAST system.

The Situational Awareness module exists at the system level, and is responsible for gathering and processing measurement data from throughout the power network. It performs state estimation or other measurement process to form a consistent understanding of the state of the power system. It then makes this understanding available to other layers through the Communication Network layer. It also reports the state to the Test Management and Analysis module to be recorded and displayed to the user.

In Phase I of the VAST program, a simplified Situational Awareness module will be implemented to collect the measurements from the power network (including both grid measurements and local device measurements) to report to the Test Management and Analysis module for display to the user. The System Control module will not be designed or implemented in Phase I.

3.1.6. Market Layer

The Market Layer of the VAST system is intended to simulate an electric energy market in a utility implementation of the VAST architecture. It is a placeholder intended for development in future phases, and will not be designed or implemented in Phase I.

3.2. Physical Implementation

Figure 2 below shows a diagram of the physical architecture of the VAST system for Phase I. The major components are the VAST Interface PC, the VAST National Instruments Control and Automation

System, the Inverter Source Array, and the Power Network. These components, along with the functional modules they implement, are described below.

The VAST Interface PC is a PC running Windows 7, which is located physically next to the VAST assembly. The VAST Interface PC implements the Test Management and Analysis functional module, and is therefore NOT part of the system under test. It is responsible for providing a user interface during testing, applies test vectors during testing, and assists with management and analysis of test results. It communicates with the VAST Integrated Control and Automation System via USB.

The VAST Integrated Control and Automation System (ICAS) is an integrated data acquisition, computation, and control system. It is based around a National Instruments PXIe system, which provides modular, expandable data acquisition and control capabilities, as well as an integrated software development and implementation environment, which will enable rapid development of software at all layers of the power system control.

The ICAS PXIe system has an NI PXIe-1062Q 8-slot PXI chassis. Modules installed in the chassis communicate with each other via PXIe real-time bus with 1GB/sec dedicated bandwidth per module. The bus master is an NI PXIe-8108 real-time controller, which contains an Intel Core 2 Duo T9400 (2.53GHz) processor with 1GB 800MHz DDR2 RAM running NI LabView Real-Time. In Phase I, installed modules on the PXIe bus are:

- 1 x NI PXIe-6363 M-Series DAQ (*Expand to 2 in Phase II*)
- 1x NI PXI-7842R FPGA Controller (*Expand to 4 in Phase II*)
    - 1x NI-9151 C-Series Expansion for R-Series
        - 4 x NI-9215 4 Channel Differential Simultaneous Analog Input
- 1 x NI PXI-2567 Relay Driver
- 2x Empty PXIe/PXI Slots
- 2x Empty PXI Only Slots

All of the system under test software in VAST is run in the ICAS, either on the real-time controller or one of the FPGAs.

The NI PXIe-8108 real-time controller communicates directly with the VAST Interface PC via USB. It is bus master of the PXIe bus, which gives it high-bandwidth, high-latency access to all other modules. Therefore, it runs software implementing all of the “centralized” power system functions, which are real-time in nature, but do not require low-latency feedback control. This includes the Communications Network, Grid Measurement, State Estimation, System Control, and Market software functional modules. Software running on the NI PXIe-8108 is implemented in NI LabView Real-Time.

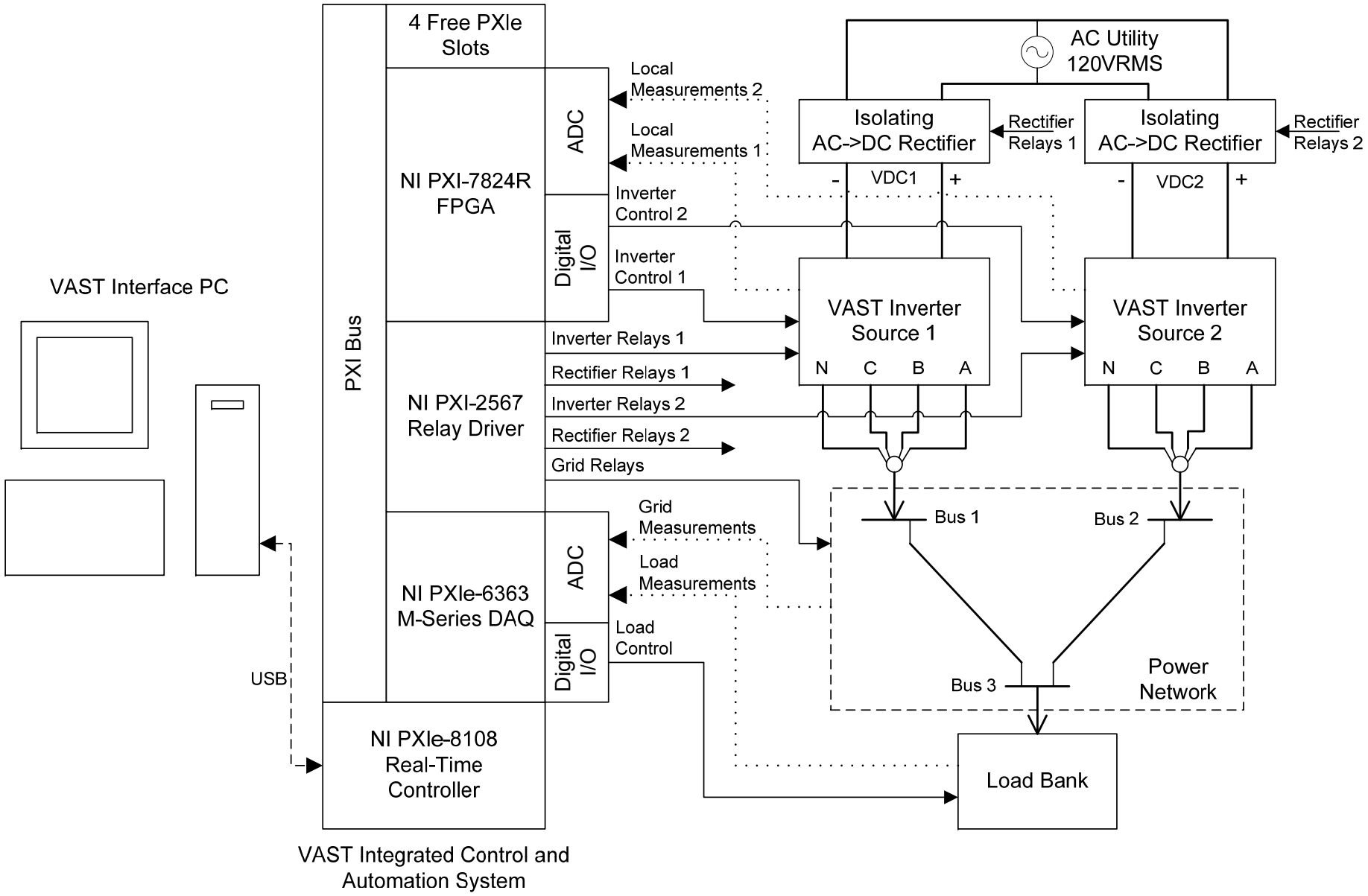


Figure 2 - VAST Physical Architecture: Phase 1

In Phase I, VAST contains one NI PXI-7824R FPGA Reconfigurable I/O Device. This module contains a Virtex-5 LX50 FPGA, to which are directly connected 8 differential simultaneously-sampled 16-bit analog inputs and 96 digital I/O. In the VAST system, the analog inputs are expanded by use of an NI-9151 with four attached NI-9215 4-Channel Analog Input devices. This uses up 40 of the available digital I/O on the NI PXI-7842R (brining total available digital I/O to 56), but provides 16 additional differential simultaneously-sampled 16-bit analog inputs (bringing the total to 24). These 24 analog inputs and 56 digital I/O can be accessed at very low latency (< 1 us) by the FPGA, enabling fast feedback control.

The software modules of the Local Device Control layer, including the Local Inverter Control modules, are implemented in FPGA firmware on NI PXI-7824R. Since there are an array of Local Device Control modules, there will also be an array of NI PXI-7824R modules sufficient to support all needed Local Device Control modules. Since each Local Inverter Control requires 12 analog inputs and 14 digital I/O (see Table 1 and Table 2 in Section 4.4), there is sufficient I/O for two Local Inverter Control modules per NI PXI-7824R (limited by analog inputs). In Phase I of VAST, there will be only one NI PXI-7824R (sufficient for two Local Inverter Control modules), which will expand to four NI PXI-7824R in Phase II (sufficient for six Local Inverter Control modules and one Local Machine Control module).

The NI PXIe-6363 M Series DAQ provides 16 differential, high-bandwidth, high-latency analog inputs to the ICAS. These analog inputs are used to collect the voltage and current measurements taken from the Power Network, and are read directly by the NI PXIe-8108 real-time controller. They are not used for low-latency feedback control (thus high latency is acceptable), but may be used for system control or test results.

The NI PXI-2567 Relay Driver drives all relays in the VAST system, including both relays controlled by local controllers, relays controlled by the system controller, and relays controlled by the test management system. Since relays are slow acting devices, the high latency of the PXIe bus is acceptable.

4. Functional Module Detail Design

Details of each block in the functional design are discussed here. Schematics referenced here are available in Appendix A.

4.1. Power Network

The power network module is the 3-phase AC grid connecting all the AC sources, loads, and devices. It includes the wires, transmission line models, measurements, breakers, and fault models. In Phase I, it will be operated at 30 VRMS and 60 Hz. However, it is designed to be capable of operating at up to 120 VRMS without significant redesign. Load currents are planned for up to 10 ARMS with fault currents up to 50 ARMS.

It is designed to be easily reconfigurable into any network topology. Hardware components will be connectorized to allow for offline restructuring, but relays, controllable from software, will allow for online grid actions to demonstrate behavior under a wide variety of scenarios. This flexibility in the network results in maximum potential for test cases.

4.2. Load Bank

The load bank is the main consumer of power connected to the power network. It is representative of any number of devices that require service from a Smartgrid power network. In Phase I, the load bank will consist of a Y-connected, balanced R-L load of 9.1 Ω in parallel with 32 mH on each phase. At 30 VRMS, the load will consume approximately 100 W and 75 VA (inductive) per phase, for a total of 300 W and 225 VA. Separate single-phase relays will connect each leg so that phase imbalances can be tested.

In future phases, more load banks will be connected to the expanded power network to allow for testing of more diverse scenarios. They will also incorporate a more dynamic range of control, allowing for shifts in load magnitude and power factor with respect to time.

4.3. DC Source

DC sources are the origin of the power that supplies the power network through the interface of an inverter. Phase I includes only DC sources supplied by the rectification of utility AC (120 VRMS). The resultant DC rails will operate approximately 170 VDC apart, a more-than-adequate range over which to synthesize the 30 VRMS power waveform. The DC link capacitance, which amounts to about 3000 μF, smoothes the output by reducing ripple to 5 V. Two relays allow for multiple rectifier states: charging through a 1 kΩ resistor, connected and operating in steady state (shorting the resistor), and discharging through the resistor (disconnected from utility). Charging and discharging states are necessary respectively to separate transients during turn-on from normal operation and to remove stored energy when the source is not in operation. The DC rails are protected against operating at voltages greater than 200 VDC.

4.4. VAST Inverter Source

The inverter-interfaced source is a custom inverter design, intended to be simple and easy to reconfigure and measure for testing purposes. Currently available inverter products do not offer the level of flexibility required, including direct access to transistor gating signals; thus, a custom design was necessary. A 3-phase, 4-wire architecture was used to allow for single-phase devices and imbalances in the system. Figure 3 shows a top-level view of the physical modules contained in each VAST Inverter Source. The following sections proceed step-by-step through these modules to describe the essentials of the design and functionality of each. Additionally, Table 1 and Table 2 describe the analog and digital signals that interface the inverter sources to the ICAS. All the digital signals reside on the inverter board, except for the relay signals that switch the grid tie relay.

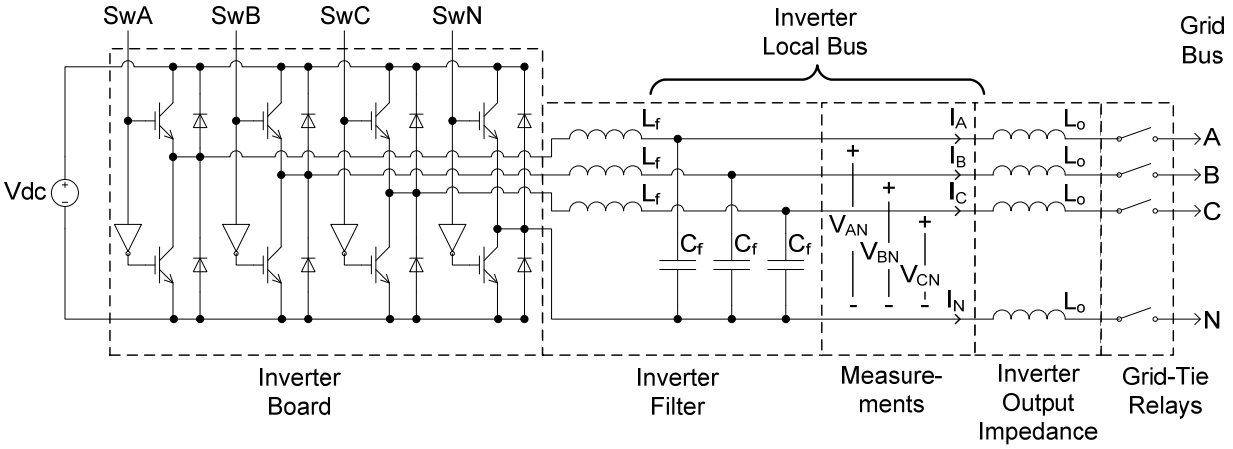


Figure 3 - Inverter Source Power Electronics Stage

Table 1 - Inverter Board Analog Interface Signals

Measurement	Type	Nominal Value	Min Value	Max Value	Update Frequency	Location	Device
VAN_Local	Voltage (Diff)	30 VRMS	-250 V	250 V	20 kHz	Measurement Board	NI-9215
VBN_Local	Voltage (Diff)	30 VRMS	-250 V	250 V	20 kHz	Measurement Board	NI-9215
VCN_Local	Voltage (Diff)	30 VRMS	-250 V	250 V	20 kHz	Measurement Board	NI-9215
VN_Local	Voltage (Diff)	60 VDC	0 V	250 V	20 kHz	Measurement Board	NI-9215
IA_1	Current	3.3 ARMS	-50 A	50 A	20 kHz	Measurement Board	NI-9215
IB_1	Current	3.3 ARMS	-50 A	50 A	20 kHz	Measurement Board	NI-9215
IC_1	Current	3.3 ARMS	-50 A	50 A	20 kHz	Measurement Board	NI-9215
IN_1	Current	3.3 ARMS	-50 A	50 A	20 kHz	Measurement Board	NI-9215
VDC_1	Voltage (Diff)	120 VDC	0 V	450 V		Inverter Board	NI PXI-7842R
IDC_1	Current	10 ADC	0 V	50 A		Inverter Board	NI PXI-7842R
Temp_ABC	Voltage (Diff)		0 V	5 V		Inverter Board	NI PXI-7842R
Temp_N	Voltage (Diff)		0 V	5 V		Inverter Board	NI PXI-7842R

Table 2 - Inveter Board Digital Interface Signals

Signal	Direction (NI)	Type	Voltage	Current (High)	Current(Low)	Frequency
Ap	Output	PWM	3.3 V	CMOS	CMOS	20 kHz
An	Output	PWM	3.3 V	CMOS	CMOS	20 kHz
Bp	Output	PWM	3.3 V	CMOS	CMOS	20 kHz
Bn	Output	PWM	3.3 V	CMOS	CMOS	20 kHz
Cp	Output	PWM	3.3 V	CMOS	CMOS	20 kHz
Cn	Output	PWM	3.3 V	CMOS	CMOS	20 kHz
Np	Output	PWM	3.3 V	CMOS	CMOS	20 kHz
Nn	Output	PWM	3.3 V	CMOS	CMOS	20 kHz
Gate_Enable	Output	GPIO	3.3 V	CMOS	CMOS	
Fault_Reset	Output	GPIO	3.3 V	CMOS	CMOS	
Fault_ABC	Input	GPIO	3.3 V	1 kΩ	30 mA	
Fault_N	Input	GPIO	3.3 V	1 kΩ	30 mA	
Relay_ABC	Output	Relay	24 V	286 mA	0 mA	
Relay_N	Output	Relay	24 V	83 mA	0 mA	
Relay_DC_On	Output	Relay	24 V	83 mA	0 mA	
Relay_Charge_Discharge	Output	Relay	24 V	83 mA	0 mA	

4.4.1. DC Link

The DC link for the inverter can potentially be provided by a number of sources. In Phase I, the DC link is supplied from rectified utility service through the DC source design described in section 4.3. However, any number of natively DC supplies, such as batteries or photovoltaic cell arrays, could be used. In future updates, these options will be considered and implemented to demonstrate operation under a wide variety of capabilities and constraints based on the nature of the power sources.

4.4.2. Inverter Board

Containing the actual switching elements and the majority of the hardware of the source, the inverter board (schematic “VAST DIPIPM Board”) is the most significant part of the source from a control perspective. The requirements of system operation, such as power balance, voltage stability, and frequency regulation ultimately influence and are influenced by the operations happening in this module. The schematic illustrates the division of the inverter board into five sections: analog control power, measurements, IPM, gate signal isolation, and fault isolation.

The analog control power module (schematic “Analog Control Power”) has a number of functions related to conditioning of power at the various voltages used on-board. Protection circuitry ensures fuse opening when the DC link rails exceed 200 V (expandable to 400 V) or they are connected in reverse (applying -200 V instead of +200 V). An LED indicates the presence of voltage greater than 60 V on the DC link. In addition to the DC link rails for grid power delivery, two more voltage levels are needed on-board for different purposes. To drive the gates of the IGBTs in the 3-leg bridges, 15 V was needed; to

power the electronics in the isolation and measurement modules and signal IGBT gates (but not actually drive them), 5 V was needed. These are required to be isolated from the transients in the power system, so they cannot be derived from the DC link rail. Thus, AC utility voltage is transformed and rectified to provide a source for two linear regulators, which provide the appropriate voltage levels. LEDs indicate the presence of voltage on each of the outputs.

The measurements module (schematic Inverter Board Measurements) provides circuitry for monitoring the DC link rails. Voltage and current measurements are obtained by using a voltage divider and current transducer, respectively. Also, temperature measurements from the two IPM devices are multiplexed due to I/O constraints.

The IPM module (schematic "IPM Circuit") contains the circuitry immediately surrounding the PS21A7A IPM (Intelligent Power Module) devices, each of which contains 3 half-bridges (6 IGBTs total) in a standard 3-phase inverter configuration. Since the neutral also required a half-bridge, two IPM modules were needed, with the result that one module had two half-bridges unused. For each IGBT, a gate-source voltage of 15 V was needed to modulate the channel. The bootstrap circuit (schematic "Bootstrap"), of a design provided by the manufacturer, ensures that the gate-source voltage for the upper IGBTs is the appropriate level given the dependence of the upper IGBT's source voltage on the switching state. These voltage levels provide the IGBT gate drives internally to the device, being modulated by the 5 V signals determined by the control software.

It should be noted here that the analog ground is tied to the lower DC link rail. This was required because many of the voltages on the PS21A7A device are referenced to this rail. Because the relationship between the DC link rails and earth ground are not defined, the analog ground net may float inside the range of the DC rail voltages and switch quickly with respect to earth ground. However, since the analog voltages are referenced to this net, the appropriate voltages are applied at all points. No inverter equipment is referenced to earth ground with the exception of a varistor that prevents analog ground from straying more than 200 V away from earth ground.

The gate signal isolation module (schematic "Gate Signal Isolation") provides optical isolation between digital signals from the NI system and the gate modulation signals to the IGBTs. This is necessary to decouple the test and measurement equipment from transients on the inverter board and the on-board analog and power voltage reference, which is floating with respect to earth ground. Pull-up and pull-down resistors ensure that IGBT gate modulation signals result in open channels until the buffer gate enable is activated from software, preventing a possible short between the DC rails. The emergency stop switch, through a hardware action, can also disable the buffer devices to produce the same result.

The fault signal isolation module (schematic "Fault Signal Isolation") provides optical isolation for three signals on the inverter board to output to the NI test and measurement system. Some signal conditioning is required in addition to the isolation, including latching of pulsed signals and buffering to provide appropriate current levels. LEDs indicate when each of the fault signals (from each of the two PS21A7A modules) or the emergency stop switch is activated.

4.4.3. Inverter Filter

A filter (schematic "Inverter Output Filter") is needed on the output of the inverter to remove the high frequency signals due to the switching actions, expected to have a fundamental frequency of 20 kHz. To provide high rejection of these components, an *LC* filter was designed with 3.9 mH and 2 µF to achieve a cutoff frequency of less than 2 kHz on the phase lines. The neutral also required some filtering, so a 3 mH series inductor was inserted. Also, two 1 MΩ resistors and two 150 µF capacitors were used to maintain the neutral voltage halfway in between the DC rails. This configuration also provided a low-pass cutoff of about 200 Hz, an appropriately low value since the neutral voltage should not have significant differential switching signals compared to the DC rails or the phase lines.

4.4.4. Measurement Device

The circuitry and measurements in this measurement module are identical to those in the grid measurement devices module (schematic "VAST Measurement Board"), described below. Measurements of inverter output at the local bus are taken upstream from the grid tie relay to observe inverter behavior when disconnected from the grid. These measurements are essential to predict behavior before and after grid connection and to observe behavior while isolated from other power equipment.

4.4.5. Inverter Output Impedance

An output impedance is needed downstream from the voltage regulated node of the inverter source. The point at which the inverter couples to the power network cannot be the same as the inverter local bus. It is conceivable and likely in many cases that two inverter sources may be tied together to the same bus through a very small impedance (perhaps to provide redundant service to a critical load). The two sources would then attempt to regulate the same voltage to control power output, resulting in instability. Output impedances prevent this situation. Although no output impedance is included in the present inverter source design, the requirements for this element will be a topic of ongoing investigation throughout work in Phase I. The exclusion of an output impedance is not seen as detrimental for the time being because of the nontrivial transmission line inductance connecting the three buses in the power network.

4.4.6. Grid Tie Relay

The grid tie relay (schematic "Grid Tie Relay") represents the point of common coupling between the inverter and the power network. It consists of a 3-phase SPST relay for the A, B, and C phase lines and a single-phase SPST relay for the neutral line.

4.5. Prime Mover

Any machine source connected to the VAST as a generator will require a prime mover as a source of mechanical energy. The source of the prime mover's energy will necessarily be external to the VAST power network to achieve a net positive power injection. However, its output will be controllable at the local and system levels as part of the generation dispatch procedure. Machine source integration is not

part of the VAST Phase I plan, but it will be a crucial element of future phases where interactions between inverter-interfaced sources and machine sources will be studied.

4.6. VAST Machine Source

Study of machine source behavior and its effects on a power network with inverter-interfaced sources will be a principal effort in research conducted using the VAST. It is expected that a microgrid (or, more generally, a power grid of any size) will include inverter-interfaced sources alongside synchronous generators to serve load. As stated above, machine sources are not planned for VAST Phase I but are being considered for future phases.

4.7. Local Inverter Control

<Preliminary Design on Local Inverter Control software is complete. A more detailed design will be presented at CDR – NGA>

The Local Inverter Control module is the local controller (on the Device Control layer) for an inverter source. Its primary purpose is to determine inverter duty cycle values to implement feedback control of the inverter output to balance real and reactive power (P_C and Q_C) with other inverters on the power network while maintaining a nominal voltage magnitude ($V_{DQ0,n}$) and frequency (ω_n). This requires a fast feedback control on the order of 20 kHz utilizing low-latency local measurements. Therefore, the Local Inverter Control modules (one per inverter) are implemented in the NI PXI-7842R FPGA I/O Devices (two Local Inverter Control modules per FPGA). The FPGA firmware is written in NI LabView FPGA development environment.

The Local Inverter Controller must balance the output power of its associated inverter with other inverters on the power network as well as regulate its own output voltage magnitude. This is achieved by a two-loop architecture, shown in Figure 4 below.

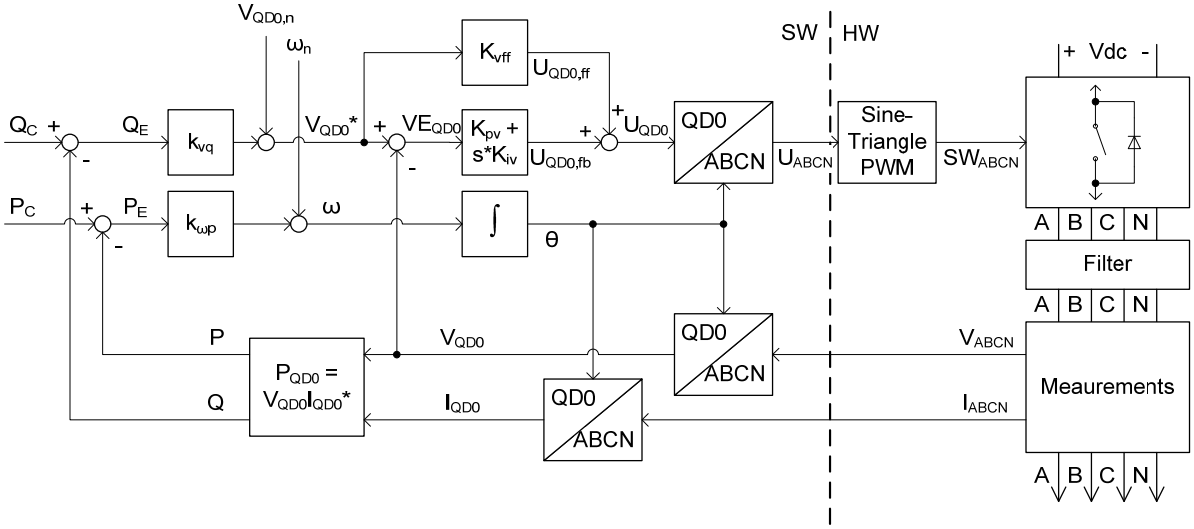


Figure 4 - Local Inverter Control Diagram

The outer loop is a consensus-based, frequency-real power droop and voltage-reactive power droop controller. This controller regulates real and reactive power (P and Q) as close to commanded values (P_C and Q_C) as possible. This is done by adjusting voltage magnitude (V_{DQ0}) and frequency (ω) away from their nominal values ($V_{DQ0,n}$ and ω_n respectively). The outer loop controller's outputs are the commanded voltage magnitude (V_{DQ0}*) and frequency (ω) to which the inner loop must regulate voltage. The outer loop is described in detail and simulated in the document "VAST Preliminary Software Simulation Report".

The inner loop is a PI voltage regulation loop operating in DQ0 space. Its purpose is to regulate voltage magnitude to the value commanded by the outer loop (V_{DQ0}*). It also creates a voltage waveform with the frequency commanded by the outer loop (ω). Because voltage time waveforms can be assumed to be approximately sinusoidal, voltage in DQ0 space is constant at steady state, even for an unbalanced system. This allows a PI controller to achieve zero steady state error in voltage regulation for any linear external system, even an unbalanced one. The inner loop controller is described in detail and simulated in the document "Design and Simulation of a Zero-Steady State Error Controller for Imbalanced 3-Phase 4-Wire Inverters", available in Appendix B.

4.8. Local Machine Control

Local machine control will be more deeply considered once machine sources are integrated into the VAST generation mix. Initially, machine control will likely simulate contemporary methods for automatic generation control (AGC). Further work will examine how these traditional control strategies compare when significant penetration of inverter-interfaced sources (employing their own control methods) occurs. Like the local inverter control, this software will be implemented in the NI PXI-7842R FPGA.

4.9. Measurement Devices

The grid measurement module (schematic "VAST Measurement Board") is deployed throughout the VAST power network through a standardized measurement board. Phase-to-neutral and neutral-to-earth voltages are observed through resistive dividers in a 1/25 ratio. Currents on phase and neutral lines are measured using current transducers, outputting a voltage signal. Measurements are appropriately scaled for the data acquisition equipment. Power for the on-board electronics is provided from the ICAS, providing independence of grid measurements from the power network state or power device behavior. The board includes overvoltage protection of 200 V phase-to-neutral and 200 neutral-to-earth as well as overcurrent protection of 10 A on phases and neutral. This standard design is installed at every power network bus and on every inverter upstream of the grid tie relay. Thus, symmetry in measurements can be achieved while minimizing possibilities for measurement error. Table 3 summarizes the measurements conducted by the measurement board. The update frequencies of these measurements is not fixed in Phase I since the communication network will be a driving influence on the rate that new measurements are needed and can be delivered.

Table 3 - Measurement Board Data Collection

Measurement	Type	Nominal Value	Min Value	Max Value	Device
VAN	Voltage (Diff)	30 VRMS	-250 V	250 V	NI-6363
VBN	Voltage (Diff)	30 VRMS	-250 V	250 V	NI-6363
VCN	Voltage (Diff)	30 VRMS	-250 V	250 V	NI-6363
IA_Load	Current	33.3 ARMS	-200 A	200 A	NI-6363
IB_Load	Current	33.3 ARMS	-200 A	200 A	NI-6363
IC_Load	Current	33.3 ARMS	-200 A	200 A	NI-6363
IN_Load	Current	33.3 ARMS	-200 A	200 A	NI-6363

4.10. Local Measurement

"Local measurement" refers to the software module responsible for collecting data from the measurement devices and sending it to the upper levels of the system control. It provides the interface between the signals from the actual measurement devices and the communication network. This may involve very basic analysis, data packaging, or timing to ensure synchronized measurements. The specific tasks it performs will be determined as software development progresses. This software will reside in the NI PXI-7842R FPGA.

4.11. Virtual Communication Network

Any Smartgrid with system-level control operations will require a communication network to deliver data to a computational center from distributed locations. A virtual communication network will be implemented in software on the NI PXIe-8108 real-time controller to simulate the latency in transferring data between all the local controllers and measurement devices and the system control. In Phase I, the virtual communication network is planned to be very simple, possibly consisting of straight-through connections that introduce very simplified or no latency behavior. In future phases, this module will be an essential component to study the requirements on power grid communication systems and will be a target of deeper development and evaluation.

4.12. Situational Awareness

The measurements collected from throughout the power network are used to create a refined description of the overall system state; this software module (also on the real-time controller) is called "Situational Awareness". For many system control applications, it is necessary to have a complete picture of the system state. However, it cannot be expected that measurements in a real system will always be complete or reliable. Situational Awareness encompasses state estimation techniques to identify bad or incomplete data and to use the available data to derive the actual system state with reasonable confidence. State estimation techniques under various data collection scenarios will be a topic of investigation primarily in future phases. Phase I will not include this layer of system analysis in real time.

4.13. System Control

Frequency regulation and load balancing and voltage/reactive power coordination are system level control issues. A significant portion of the analysis of VAST Phase I will be devoted to realizing effective autonomous controls for frequency and voltage.

The system control layer, intended as part of the software managed by the real-time controller, includes many possible applications related to the operation and optimization of the electric grid as a whole. Power flow computation, contingency analysis, and economic dispatch are some of the tools that are needed to maximize global satisfaction with electricity service supply and consumption. These applications, part of the system control layer, will not be a core topic of study or development in VAST Phase I.

4.14. Market

Electricity markets are yet another system-level influence on the electricity grid. The market software, another component of the real-time controller functions, will provide capabilities to simulate economic grid operation in response to arbitrary implementations of electricity industry policy. Many factors will be included, such as methods for establishing price-based power management in response to critical or emergency contingencies. Price-based control includes various pricing models, and distinctions of energy and ancillary services, such as frequency regulation or spinning reserve. This layer of software is not planned for implementation in VAST Phase I.

4.15. Test Management

Test management will be an essential part of the VAST software. It will handle test vector organization and input. In Phase I, test vectors will include the local device control algorithms of inverter sources, network topology (including source, load, and transmission line connections), and power network transient behavior. Test vectors will be designed around investigating and evaluation of local control strategies for inverter sources. Test management software will reside on the host PC and will serve as the interface between the system control and operation software and the user.

5. Assembly and Layout

<This section will be completed for CDR - NGA>

6. Specifications

<Specifications are a work in progress, and will include more detail at CDR - NGA>

Requirements for the VAST system are presented briefly below. Requirements which will be implemented in future phases of the VAST program (beyond Phase I) are presented in *italics*.

6.1. Power Network Specifications

- Provide a 3-phase AC network for connecting power devices
- Easily configurable into arbitrary network types (radial, meshed, etc.)

- Operate nominally at 30VRMS *(Capable of being extended to 120VRMS without significant redesign)*
- Balanced/Unbalanced or Single-Phase Operation
- Load currents up to 10ARMS/phase
- Load power up to 600W *(1.8kW)*
- Fault currents up to 50A

6.2. Load Bank Specifications

- Provide up to 2 *(10)* statically-configurable real loads up to 300W
- Provide up to 2 *(10)* statically-configurable reactive loads up to 225VAR
- *Provide up to 1 dynamically-configurable load*
    - *Up to 1.0kW*
    - *Power Factor 1.0-0.8 Lagging*
    - *Controllable by Test Management Suite*
- Provide up to 10 breakers
    - 1-pole 3-throw or 2-pole 3-throw
    - Capable of breaking up to 100A
    - Controllable by either Test Management Suite or System Under Test Software

6.3. Inverter Source Specifications

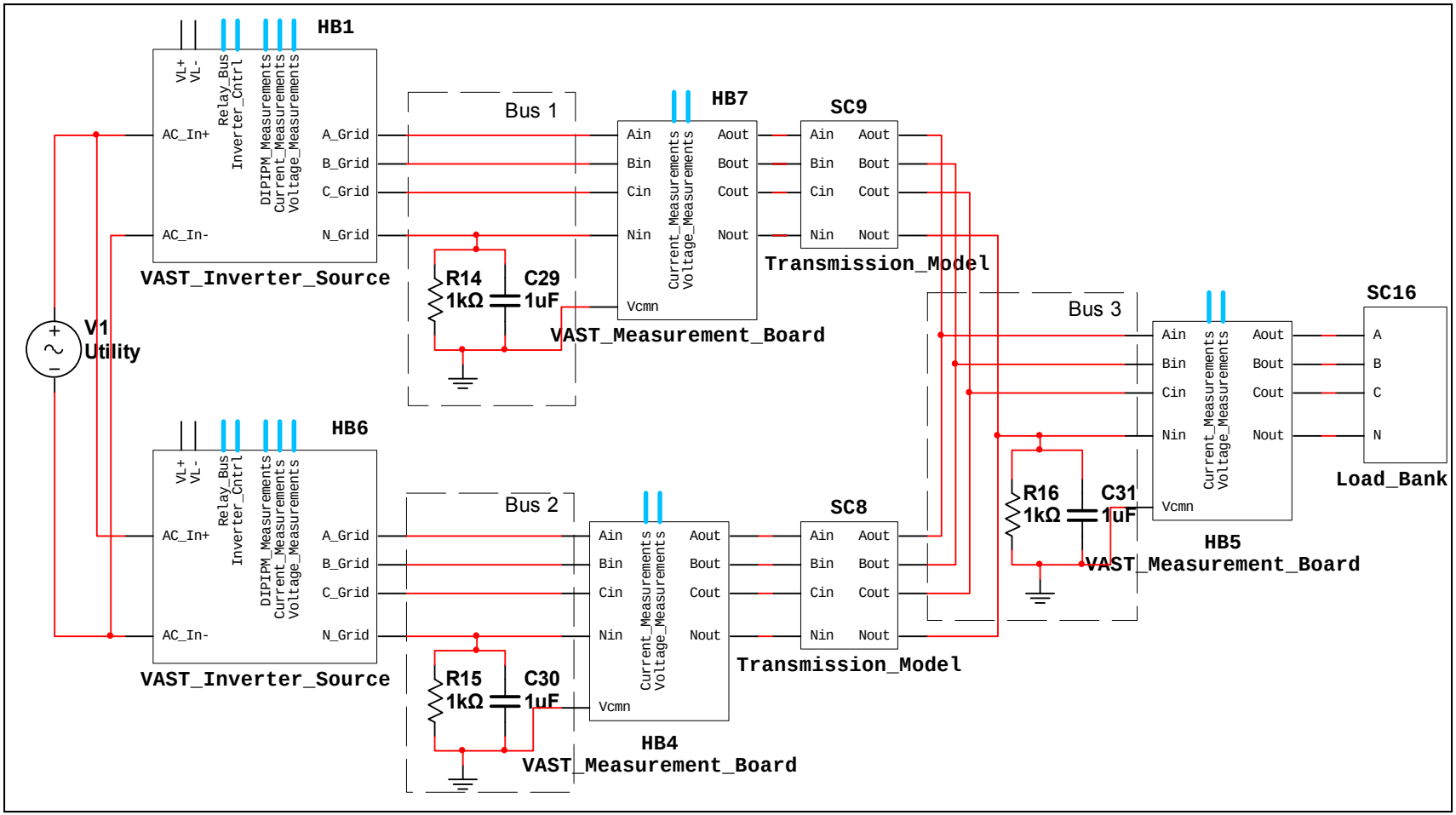
- DC Input Voltage of 150-200VDC, 170VDC nominal *(350-450VDC, 400VDC nominal)*
- DC Input Current up to 3A
- AC Output Voltage (line to neutral) of 30VRMS *(120VRMS)*
- AC Output Current up to 4.17ARMS/line
- AC Output Power up to 300W, 100W/line
- AC Output Power Factor 1.0-0.8 lagging
- Requires one 120VRMS AC utility connection for housekeeping power, up to 5W
- Green LEDs indicate when housekeeping power is present
- Yellow LED indicates when DC voltage greater than 60V is present (even if housekeeping is not present)
- Two inverter sources will be built in Phase I *(six in Phase II)*

6.4. Communication Specifications

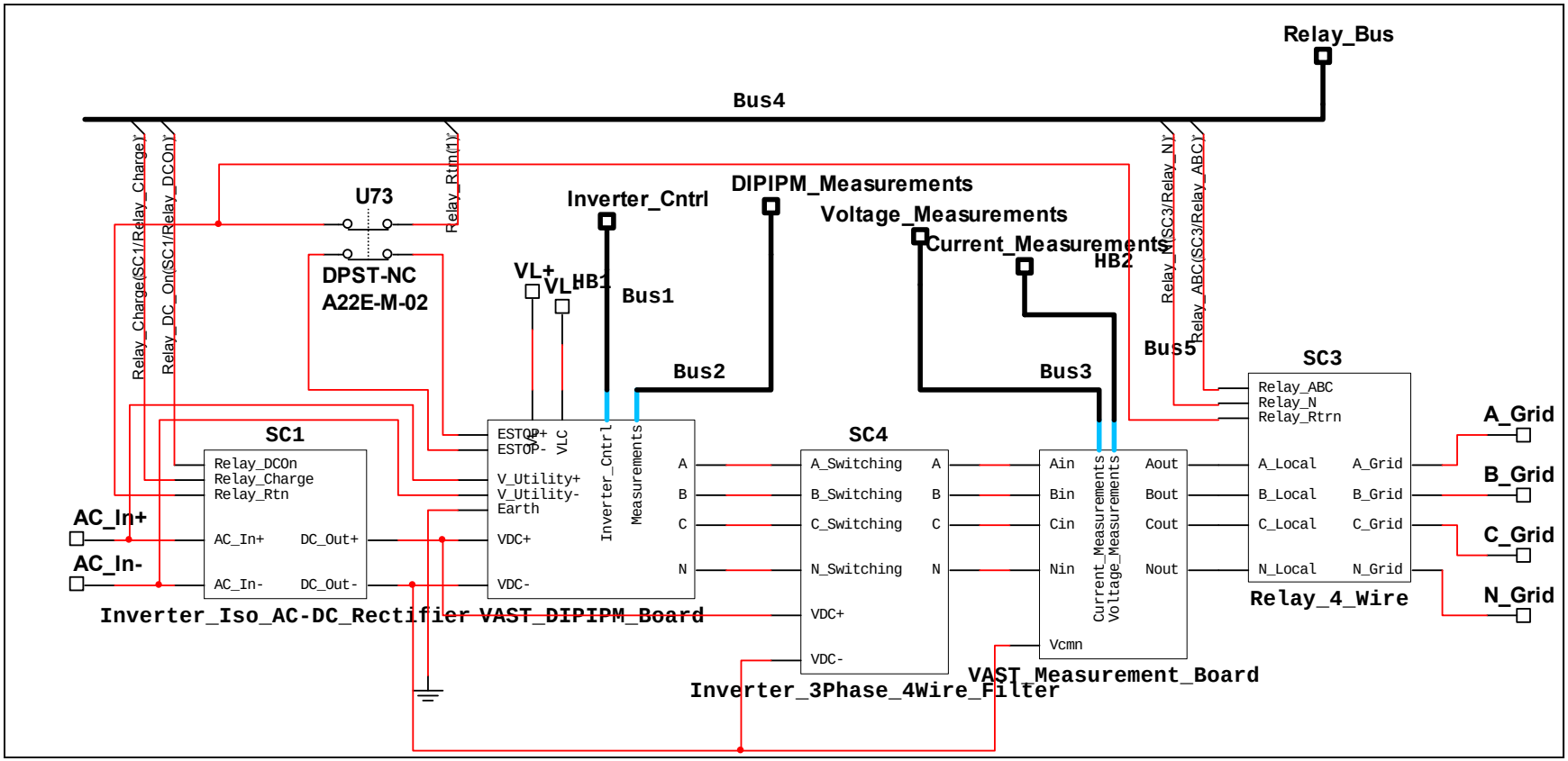
6.5. Inverter Control Software Specifications

6.6. Test Management Software Specifications

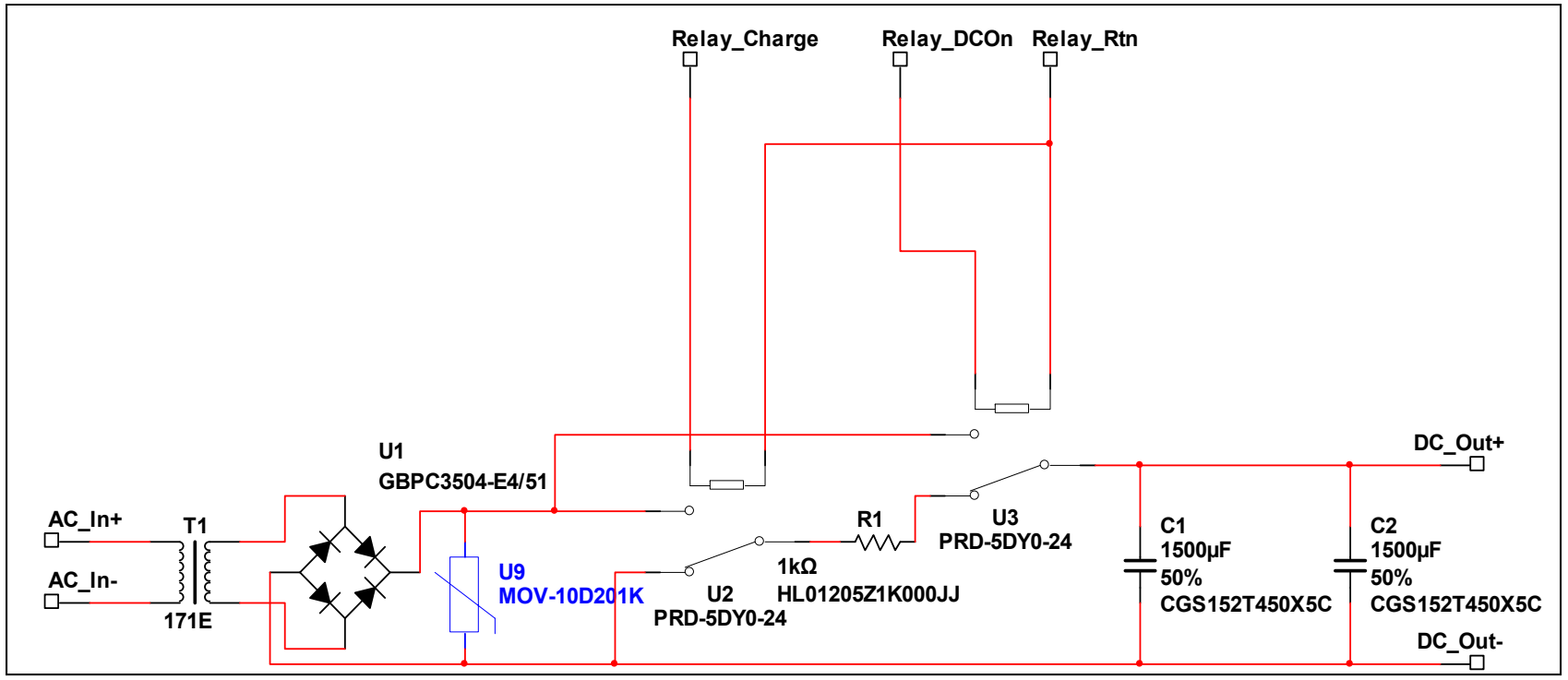
7. Appendix A: Schematics



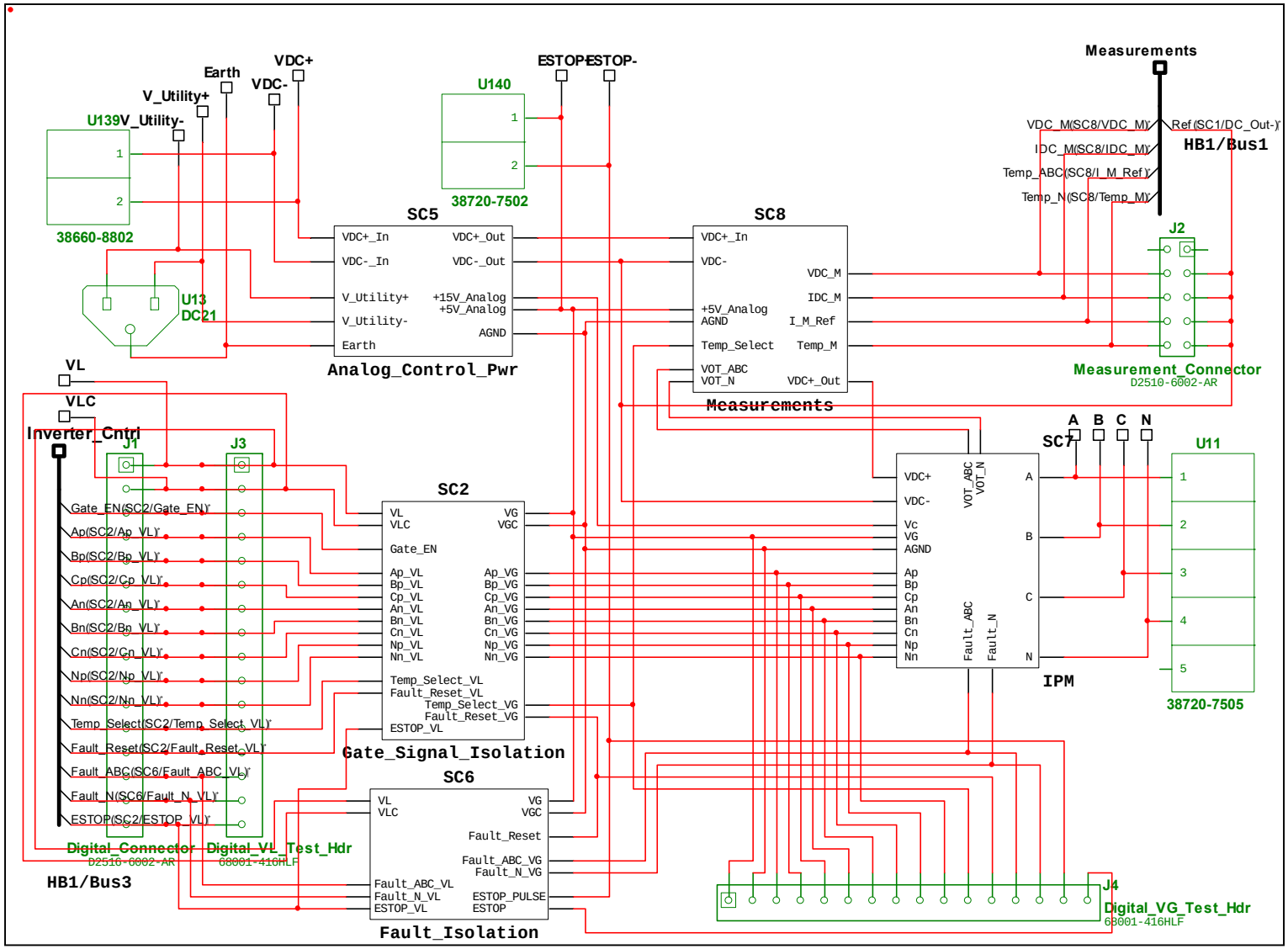
VAST Phase I Top-Level



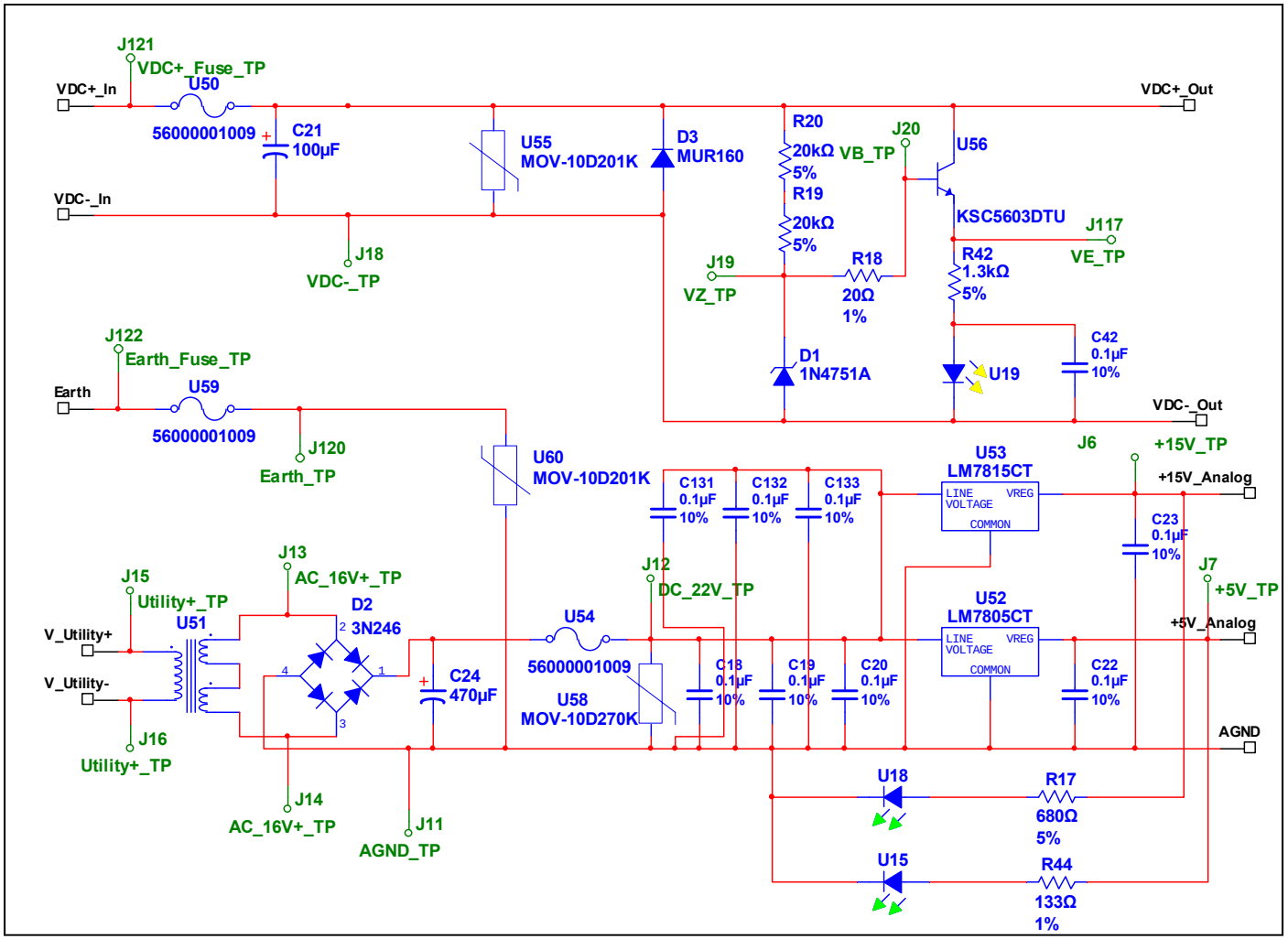
VAST Inverter Source



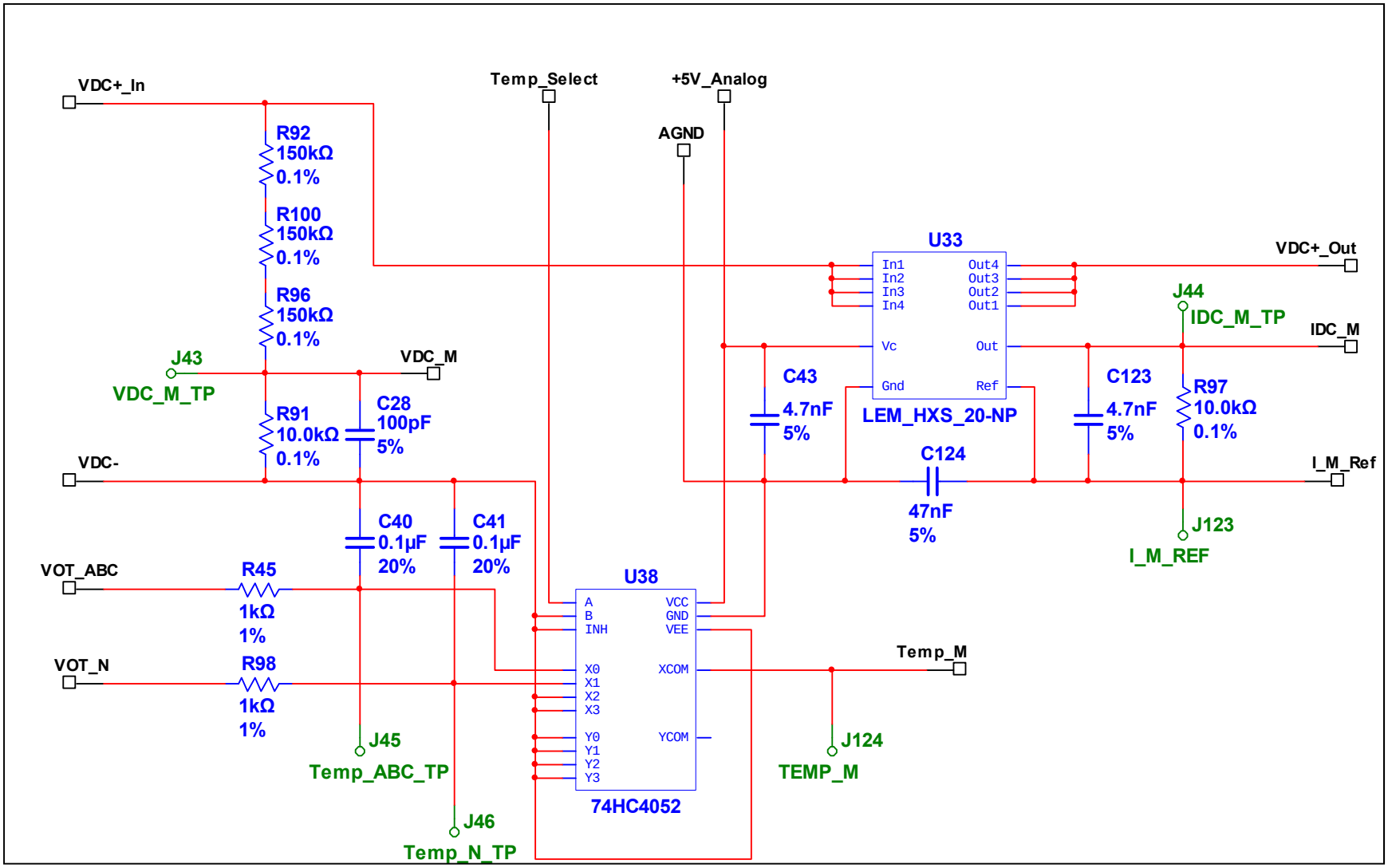
AC-DC Rectifier for DC Link



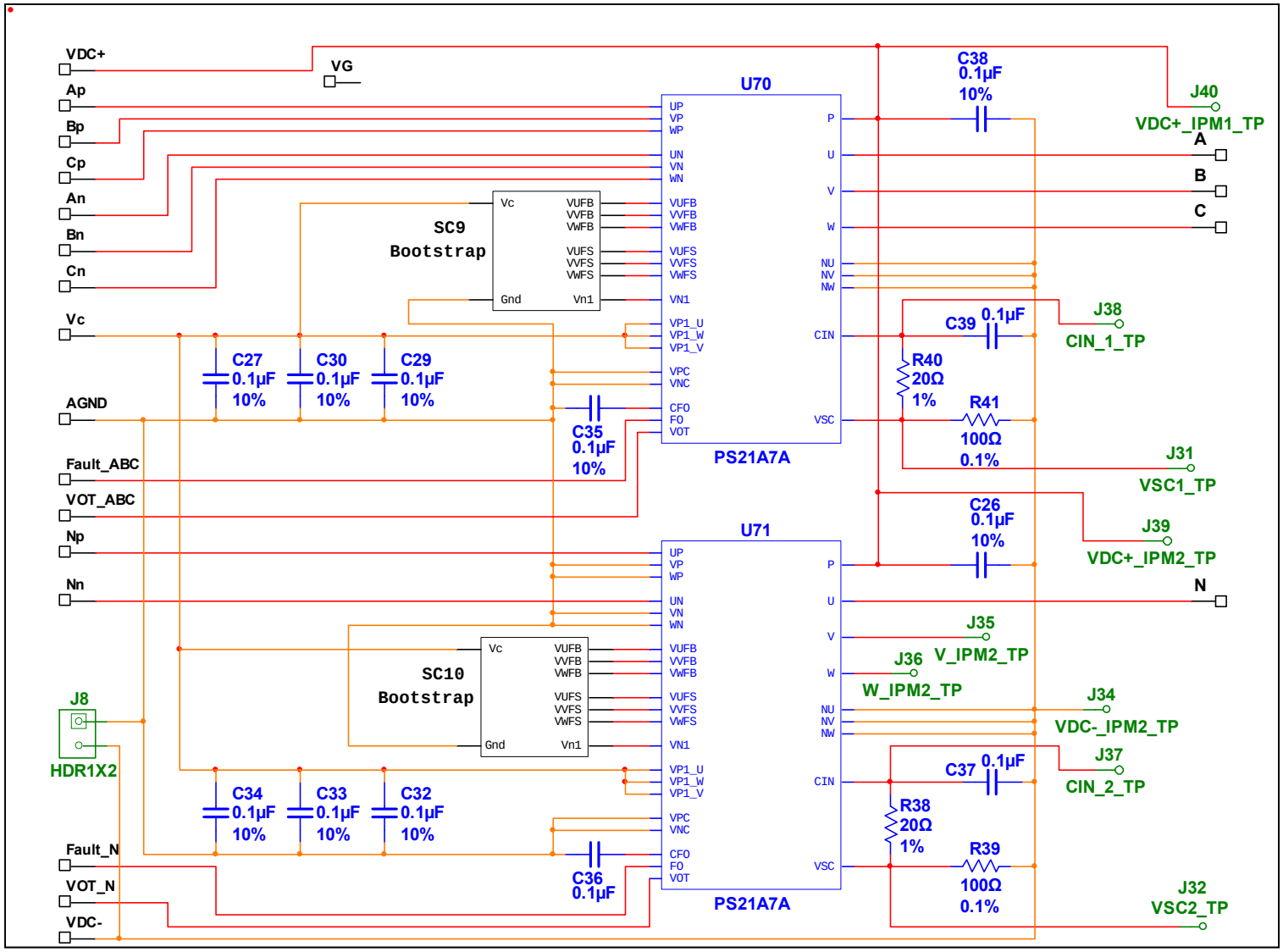
VAST DIPIPM Board



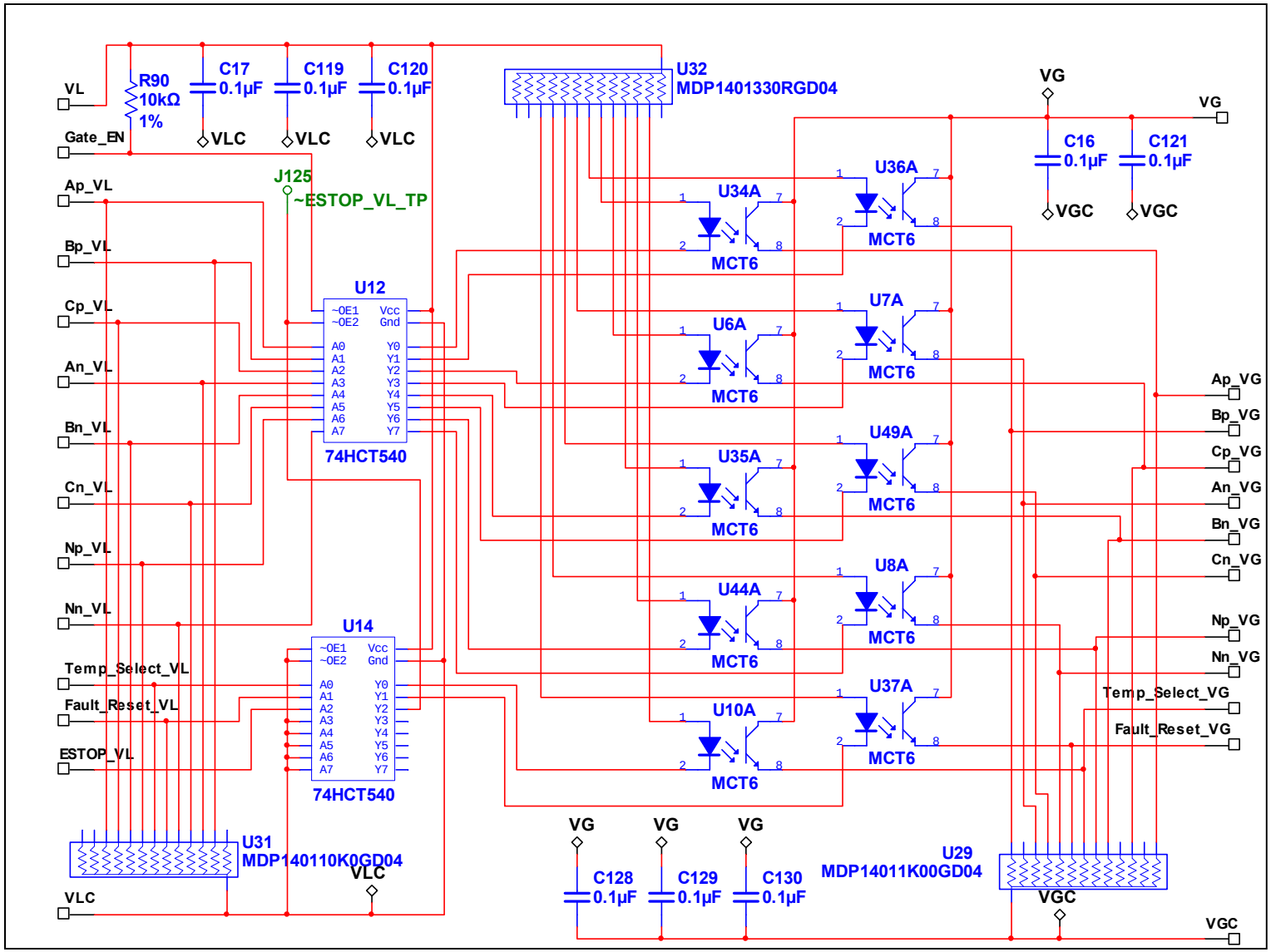
Analog Control Power



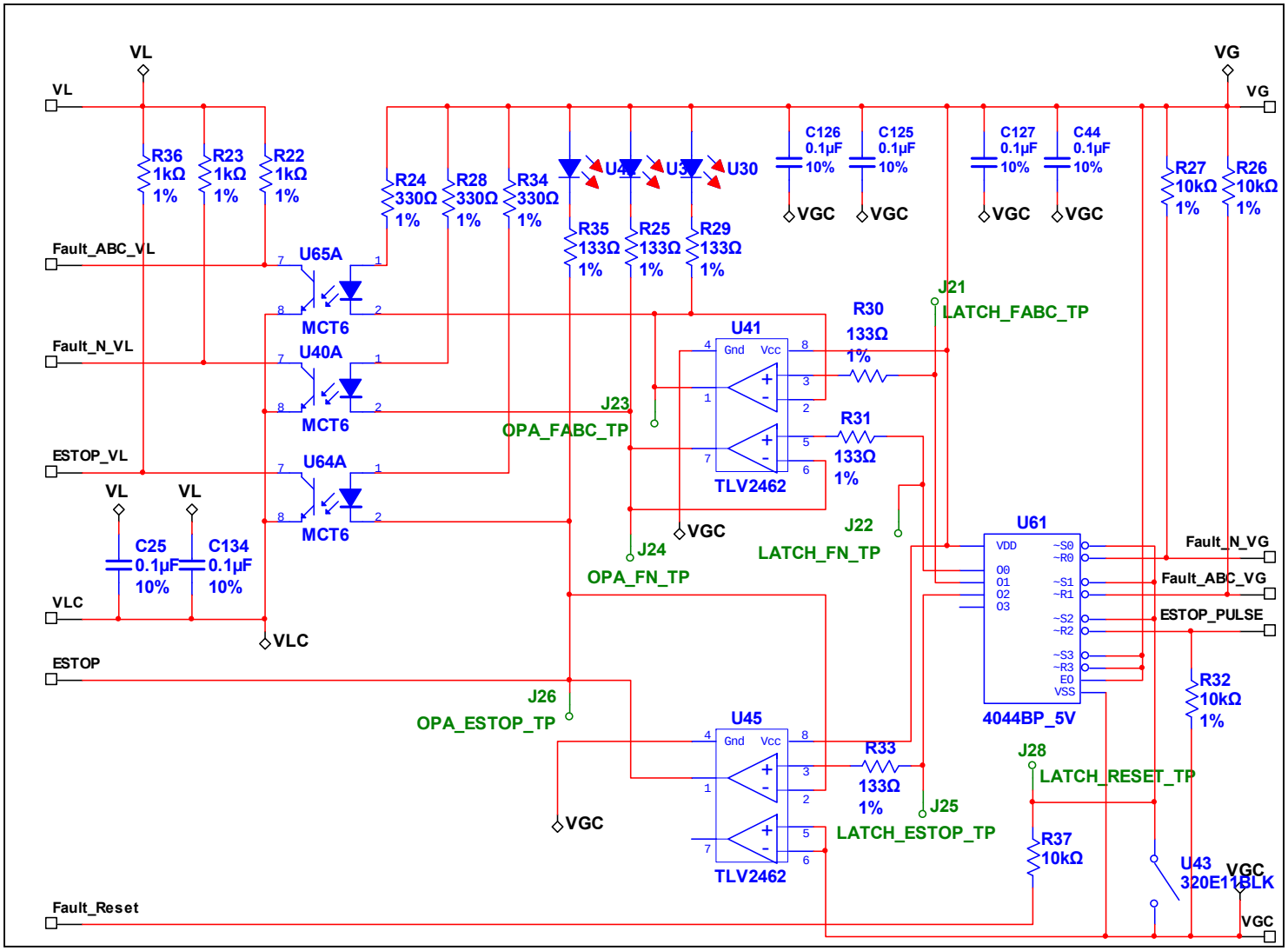
Inverter Board Measurements


VDC+
VG
Ap
Bp
Cp
An
Bn
Cn
Vc
AGND
Fault_ABC
VOT_ABC
Np
Nn
J8
HDR1X2
Fault_N
VOT_N
VDC-
U70
U71
PS21A7A
SC9
Bootstrap
SC10
Bootstrap
C38 0.1µF 10%
C39 0.1µF
C26 0.1µF 10%
C27 0.1µF 10%
C30 0.1µF 10%
C29 0.1µF 10%
C35 0.1µF 10%
C34 0.1µF 10%
C33 0.1µF 10%
C32 0.1µF 10%
C36 0.1µF
C37 0.1µF
R40 20Ω 1%
R41 100Ω 0.1%
R38 20Ω 1%
R39 100Ω 0.1%
J40 VDC+_IPM1_TP
J38 CIN_1_TP
J31 VSC1_TP
J39 VDC+_IPM2_TP
J35 V_IPM2_TP
J36 W_IPM2_TP
J34 VDC-_IPM2_TP
J37 CIN_2_TP
J32 VSC2_TP
A
B
C
N

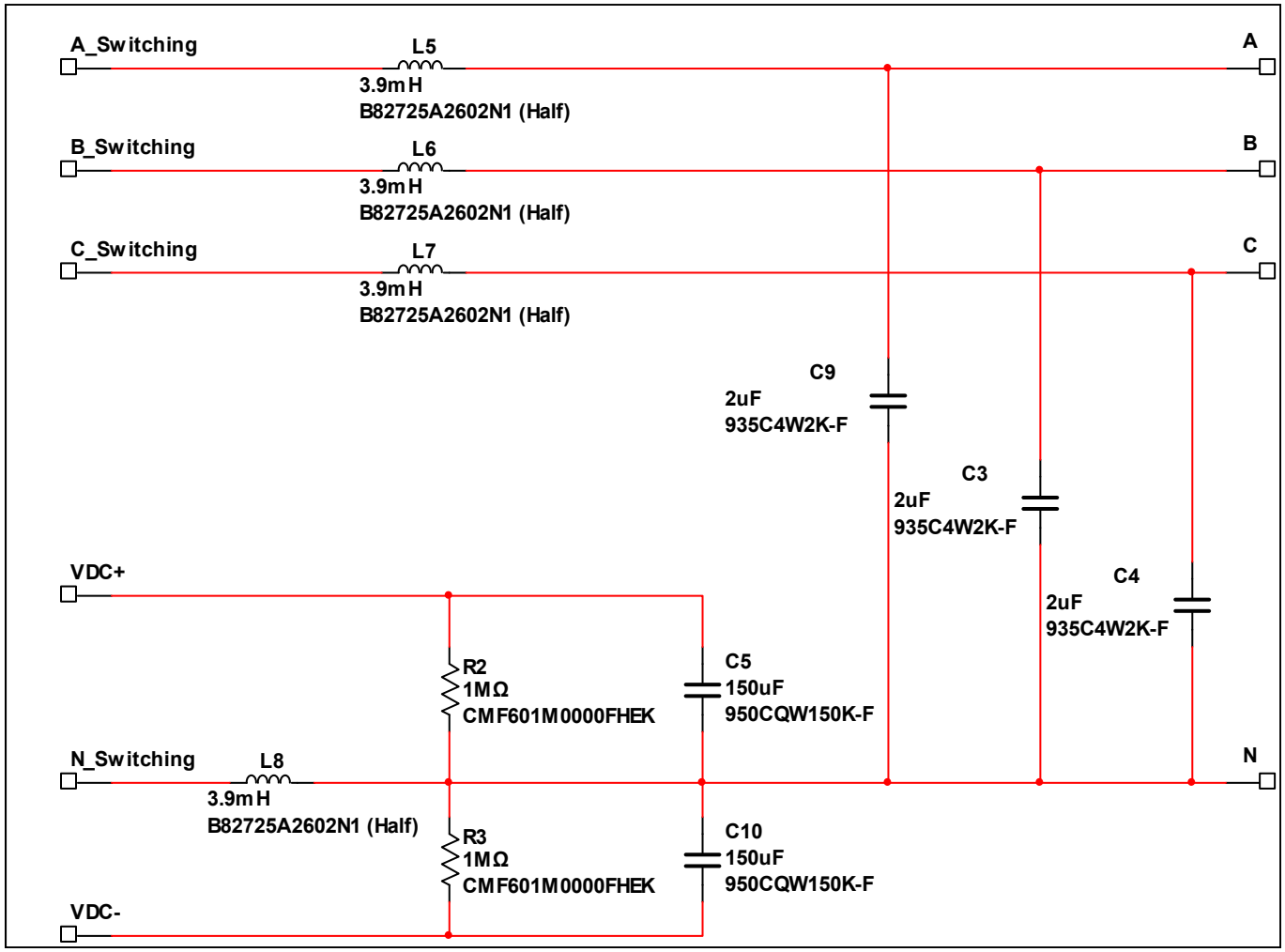
IPM Circuit



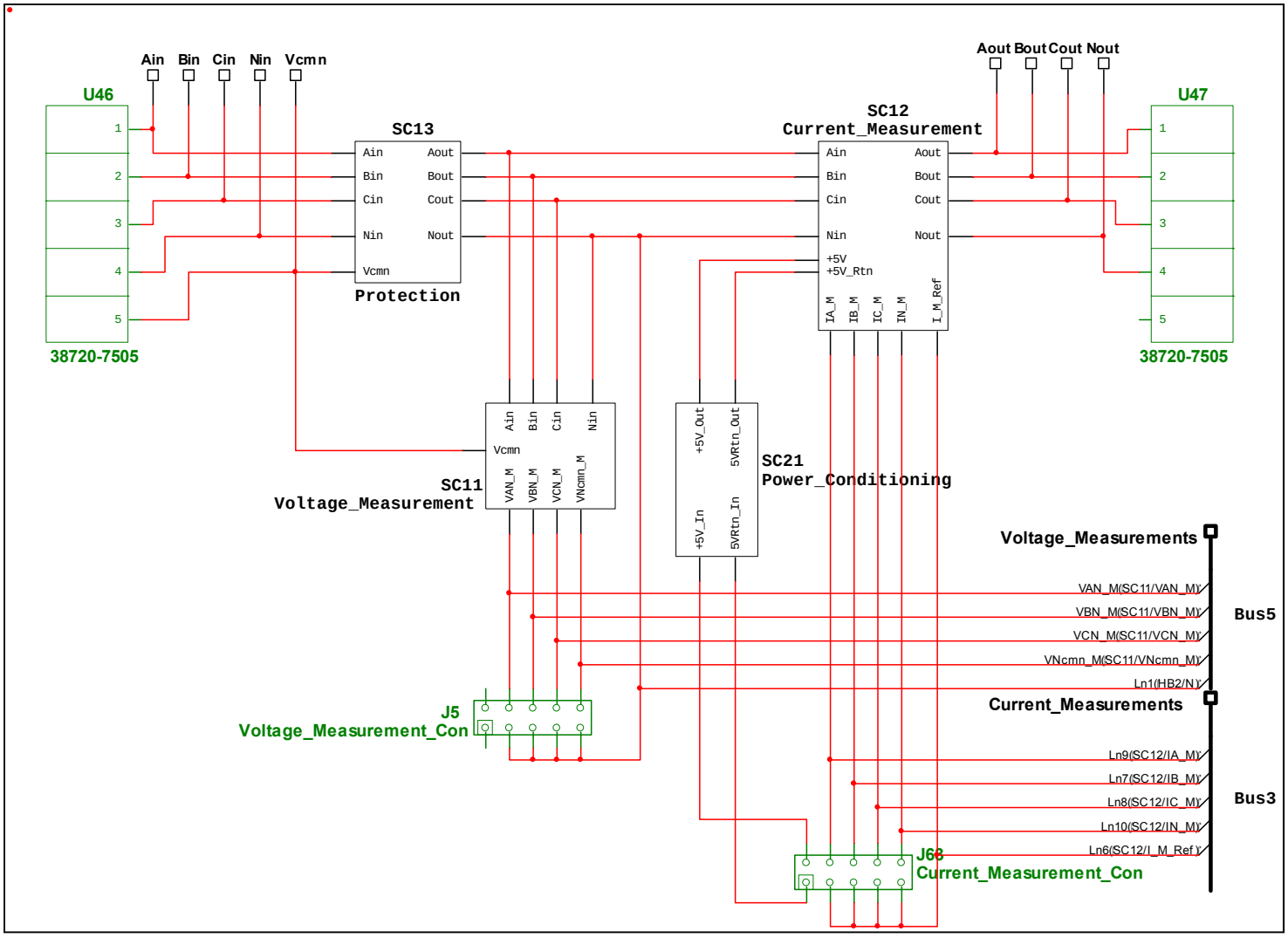
Gate Signal Isolation



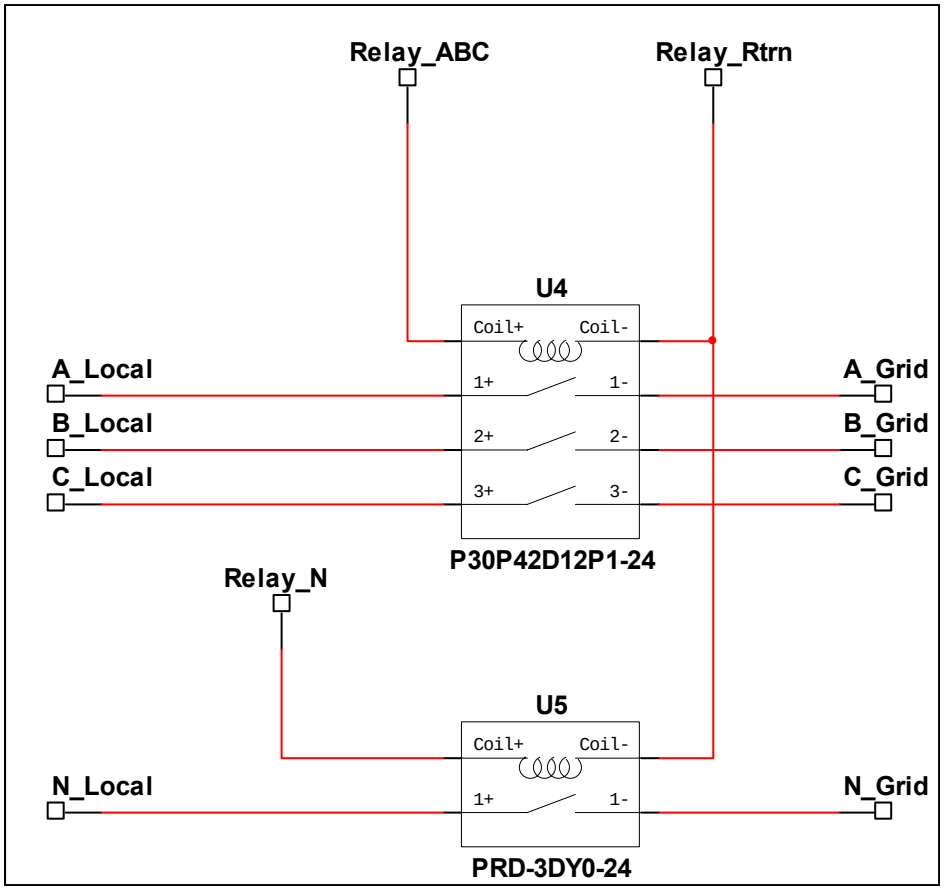
Fault Signal Isolation



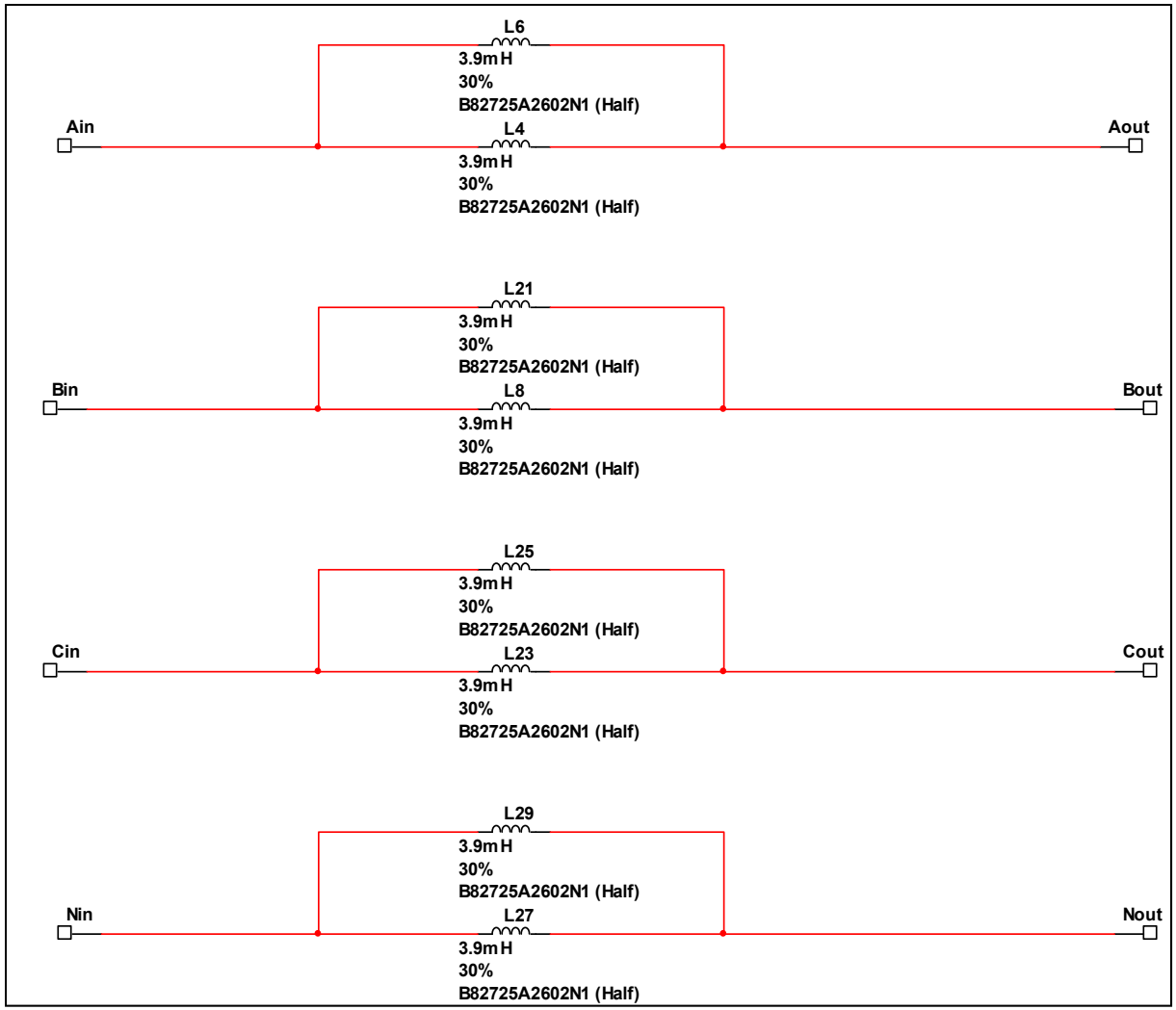
Inverter Output Filter



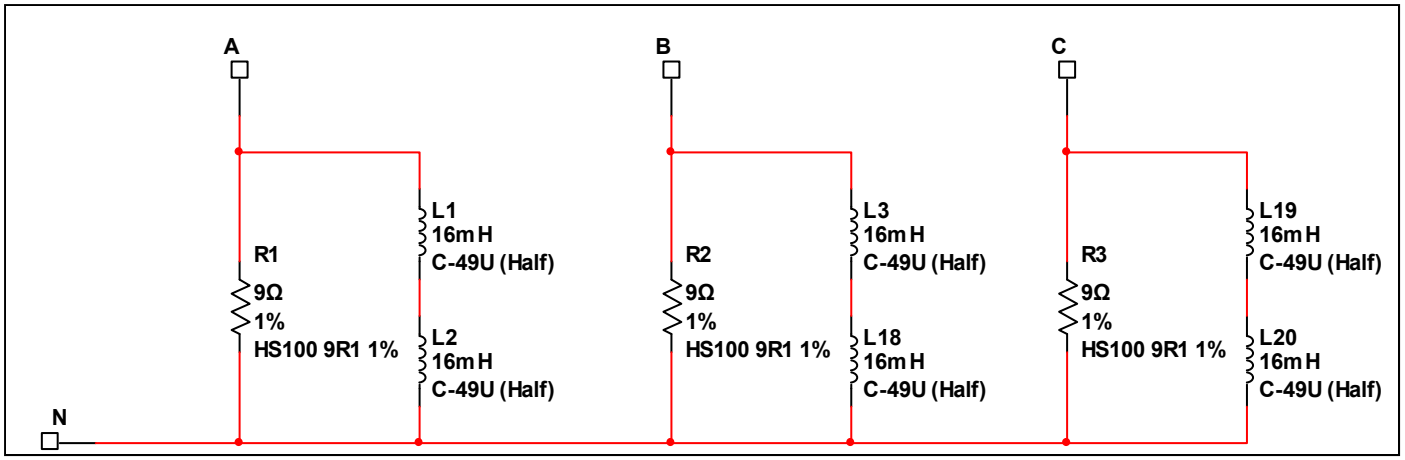
VAST Measurement Board



Grid Tie Relay



Transmission Line Model


A
B
C
N
R1
9Ω
1%
HS100 9R1 1%
R2
9Ω
1%
HS100 9R1 1%
R3
9Ω
1%
HS100 9R1 1%
L1
16m H
C-49U (Half)
L2
16m H
C-49U (Half)
L3
16m H
C-49U (Half)
L18
16m H
C-49U (Half)
L19
16m H
C-49U (Half)
L20
16m H
C-49U (Half)

Load Bank

8. Appendix B: Design and Simulation of a Zero-Steady State Error Controller for Imbalanced 3-Phase 4-Wire Inverters

Introduction

-Phase 3-Wire Voltage-Source DC to AC 3Inverters have long been used for motor drive or UPS applications. Such systems are typically intended for driving known loads, which can be assumed to be approximately balanced, and no neutral wire is required. Control methodologies for such have been extensively developed, and include such techniques as Space Vector, DQ-space transformation, or hysteresis methods.

Recently, increasing deployment of increasing numbers of renewable energy devices on the electric power grid, such as photovoltaics, wind turbines, and storage systems, have motivated the increasing use of voltage-source inverters for grid-tie applications, at both the transmission and distribution level. At present, such devices usually act as current-injection devices in support of larger traditional synchronous machine sources. However, it is highly desirable for such inverter-based sources to be able to provide voltage support, or even to perform voltage regulation and power balancing for the grid independently of machine based sources.

This motivates the development of control methodologies for inverters under grid conditions. Such inverters, particularly at the distribution level, are typically 4-wire rather than 3-wire systems, operate with unknown and often highly imbalanced or nonlinear loads, and must still be capable of a tight regulation and quick dynamic response. Existing control techniques for motor drive inverters are generally based on 3-wire balanced assumptions, which do not apply in such cases. New, high-performance, zero steady state error control techniques must be developed in order to meet the requirements of grid control inverters.

This paper will describe and investigate a proposed control architecture for 3-phase 4-wire inverters, which is claimed to regulate a commanded phasor sinusoidal voltage on a 3-wire 4-wire inverter with zero steady state error, even under unbalanced or non-linear conditions. This method, proposed by Ryan, De Doncker, and Lorenz in (1), is based on a new transformation which is analogous to DQ transformation in 3 wire systems. The proposed controller is described, implemented, and simulated under a variety of conditions to test its performance. Finally, its performance is analyzed and its usefulness for the above applications critiqued.

System Architecture

Figure 5 below shows a schematic of the 3-Phase 4-Wire inverter system to be control. The AC side of the inverter is coupled to a load of unknown characteristics, and the DC side is provided by an energy prime mover source. For the purposes of this paper, the DC source will be considered ideal.

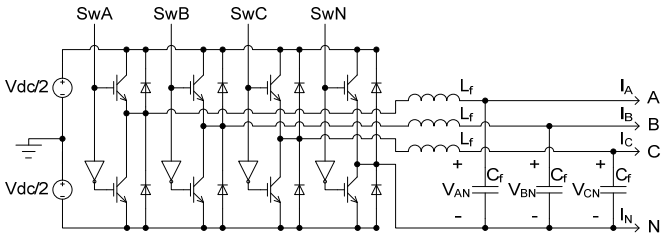


Figure 5. Schematic of the 3-Phase 4-Wire Inverter

It is desired to impose a set of sine voltage waves as follows on the phase-to-neutral outputs:

$$V_{AN}(t) = V_{AC}\sin(\omega t + \phi)$$

$$V_{BN}(t) = V_{AC}\sin\left(\omega t - {}^{2\pi}/_{3} + \phi\right)$$

$$V_{CN}(t) = V_{AC}\sin\left(\omega t - {}^{4\pi}/_{3} + \phi\right)$$

for specified constants $V_{AC}\angle\phi = V_D + jV_Q$. Because the load is unknown and not guaranteed to be balanced, the control law must be capable of regulating zero steady state voltage error even with significant load imbalance or neutral currents. It must also have quick transient response (settling time less than 1 cycle = 16.7 msec).

Proposed Control Architecture

In (1), Ryan, De Doncker, and Lorenz propose a 4x4 transform for the above system to convert the non-linear, time varying system above to a constant, linear system. They consider the following voltage vector:

$$V_{ABCN}(t) = \begin{bmatrix} V_{AN}(t) \\ V_{BN}(t) \\ V_{CN}(t) \\ V_N(t) \end{bmatrix}$$

This can be converted to a transformed space $V_{DQ0z}(t)$as follows:

$$V_{QD0z}(t) = \begin{bmatrix} V_Q(t) \\ V_D(t) \\ V_0(t) \\ V_z(t) \end{bmatrix} =$$

(1)

$$\frac{2}{3}\begin{bmatrix} \cos(\theta) & cos(\theta - \frac{2\pi}{3}) & cos(\theta - \frac{4\pi}{3}) & 0 \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{4\pi}{3}) & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}\begin{bmatrix} V_{AN}(t) \\ V_{BN}(t) \\ V_{CN}(t) \\ V_N(t) \end{bmatrix} =$$

(3)

$$T_{QD0z}(\theta) * V_{ABCN}(t)$$

This is similar to the well known Park transform, however, it is expanded to a 4-dimensional system, appropriate for the 4-wire system. Because it is a square matrix, it can be inverted, and its inverse is as follows:

$$V_{ABCN}(t) = \begin{bmatrix} V_{AN}(t) \\ V_{BN}(t) \\ V_{CN}(t) \\ V_N(t) \end{bmatrix} =$$

(2)

$$\begin{bmatrix} cos(\theta) & sin(\theta) & \frac{1}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \\ cos(\theta - \frac{2\pi}{3}) & sin(\theta - \frac{2\pi}{3}) & \frac{1}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \\ cos(\theta - \frac{4\pi}{3}) & sin(\theta - \frac{4\pi}{3}) & \frac{1}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \\ 0 & 0 & -\frac{3}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}\begin{bmatrix} V_Q(t) \\ V_D(t) \\ V_0(t) \\ V_z(t) \end{bmatrix} =$$

(4)

$$T_{QD0z}{}^{-1}(\theta) * V_{QD0z}(t)$$

The same matrices can be used to perform the transformation $I_{ABCN}(t) <=> I_{QD0z}(t)$. Since there are only 3 independent output voltages and currents, the z term of $V_{QD0z}(t)$ and $I_{QD0z}(t)$ can be dropped without loss of generality.

Because $V_{QD0}(t)$ is constant for steady state 3-phase 4-wire waveforms (even unbalanced ones), and because $T_{QD0z}(\theta)$is invertible, it is possible to regulate $V_{QD0}(t)$ with a Proportional-Integral (PI) controller to zero steady state error. The architecture of this control system is shown in Figure 6 below.

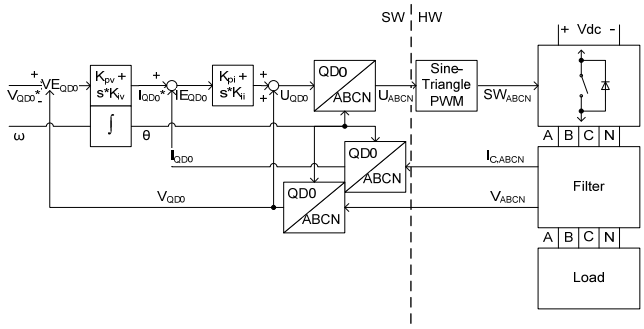


Figure 6. Proposed Control System Architecture

The control system above uses a current inner loop and voltage outer loop, both of which are regulated in the DQ0 space by a PI controller. The inner loop regulates filter capacitor current Ic, and the voltage outer loop regulates phase-to-neutral output voltage V.

Input commands to the controller are commanded voltage $V_{QD0}{}^{*}$, and the commanded frequency ω. Angle reference θ is generated in software by integration of the commanded frequency. Phase output voltage V_{ABCN} and filter capacitor current $I_{C,ABCN}$ are measured in the inverter output circuit. They are both converted to DQ0 space by $T_{QD0}(\theta)$ transform.

Voltage error $VE_{QD0}$is generated by subtraction of $V_{QD0}$from $V_{QD0}{}^{*}$, and regulation is performed by a PI compensator to produce commanded current $I_{QD0}{}^{*}$. Current error IE_{QD0} is then generated by subtration of I_{QD0}, and PI compensation performed to produce inverter commanded voltage U_{QD0}.

U_{QD0} is converted from DQ0 space back to ABCN space by $T_{QD0z}{}^{-1}(\theta)$. Inverter PWM switching signals are produced by Sine-Triangle PWM to produce inverter switching signals Sw_{ABCN}.

Simulation Results

Simulation was performed in MATLAB for the system shown in Figure 6 with several sets of system parameters and load characteristics.

Simulation 1: Reference System with Unbalanced Resistive Load

The first simulation performed attempts to recreate an example simulation in (1). This example shows a reference system with an unbalanced wye resistive load.

Table 4. Simulation 1 Parameters

Parameter	Value	Parameter	Value
V_{DC}	400 V_{DC}	$f_{sampling}$	20kHz
L_f	200µH	K_{pv}	0.12 Ω^{-1}
R_{Lf}	50mΩ	K_{iv}	1000 Ω^{-1}/sec
C_f	40µF	K_{pi}	3.5/(V_{DC}/2) Ω
V_D*	120√2 V_{AC}	K_{ii}	17900/(V_{DC}/2) Ω/sec
V_Q*	0 V_{AC}	$R_{Load,A}$	25.2 Ω

V_0*	0 V_{AC}	$R_{Load,B}$	5.2 Ω
ω	2π60 rad/sec	$R_{Load,C}$	4.8 Ω

The figures below show the simulation results for the above system. Figure 7 shows commanded and actual ABCN output voltages, Figure 8 shows commanded and actual output voltages in DQ0 space, and Figure 9 shows output currents.

The proposed control method shows zero steady state voltage regulation, even under a moderately imbalanced load. It shows an underdamped response with ringing that lasts until t=15.5 msec, just under the desired maximum settling time of 16.7 msec.

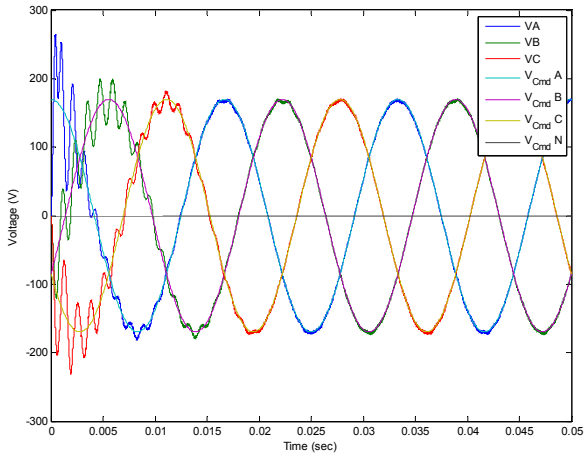


Figure 7. Simulation 1: Output Voltage ABCN Commanded vs. Actual

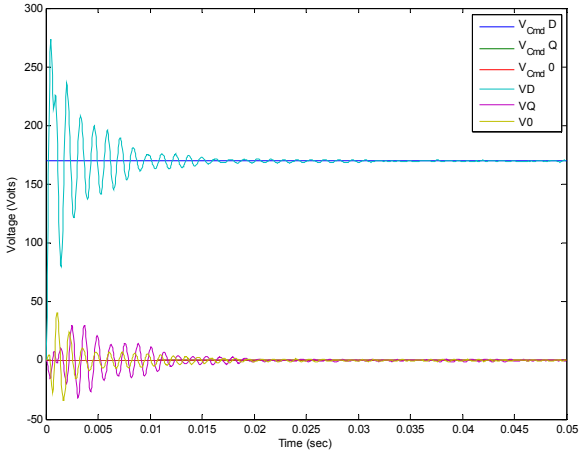


Figure 8. Simulation 1: Output Voltage DQ0 Commanded vs. Actual

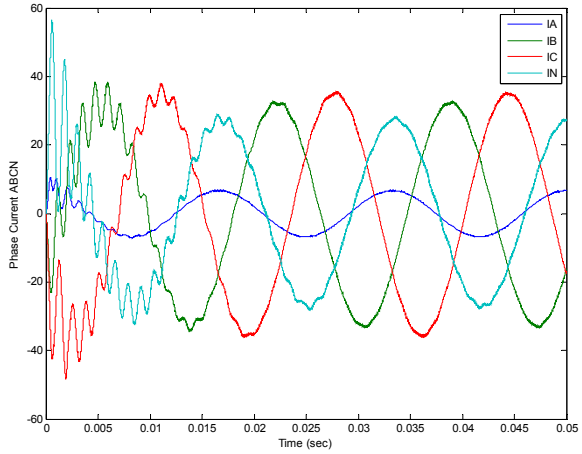


Figure 9: Simulation 1: Output Current

Simulation 2: Reference System with Imbalanced Inductive Load

The second simulation performed tests the performance of the proposed controller with the same system parameters as Simulation1, but driving a low power factor imbalanced inductive load.

Table 5. Simulation 2 Parameters

Parameter	Value	Parameter	Value
V_{DC}	400 V_{DC}	$f_{sampling}$	20kHz
L_f	200µH	K_{pv}	0.12 Ω^{-1}
R_{Lf}	50mΩ	K_{iv}	1000 Ω^{-1}/sec
C_f	40µF	K_{pi}	3.5/(V_{DC}/2) Ω
V_D*	120√2 V_{AC}	K_{ii}	17900/(V_{DC}/2) Ω/sec
V_Q*	0 V_{AC}	$R_{Load,A}$	0.1 Ω
V_0*	0 V_{AC}	$R_{Load,B}$	0.1 Ω
ω	2π60 rad/sec	$R_{Load,C}$	0.1 Ω
$L_{Load,A}$	3.1831 µH		
$L_{Load,B}$	15.9155 µH		
$L_{Load,C}$	31.8310 µH		

The proposed controller, once again, shows zero steady state error. The transient ringing settles much faster: 4.6msec. Notice the large Neutral current that is required due to the large load imbalance: this controller is capable of driving significant Neutral current while still maintaining zero steady state voltage error.

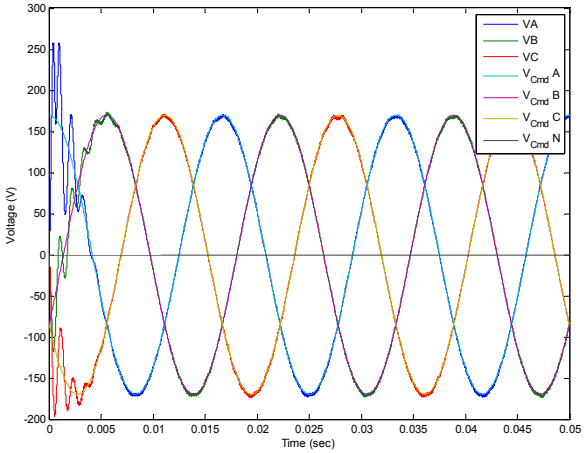


Figure 10. Simulation 2: Output Voltage ABCN Commanded vs. Actual

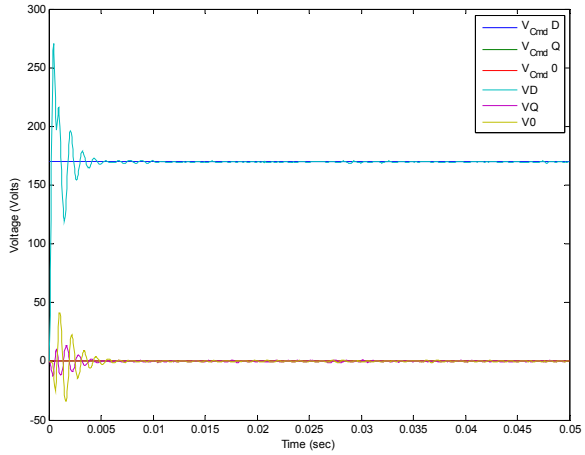


Figure 11. Simulation 2: Output Voltage DQ0 Commanded vs. Actual

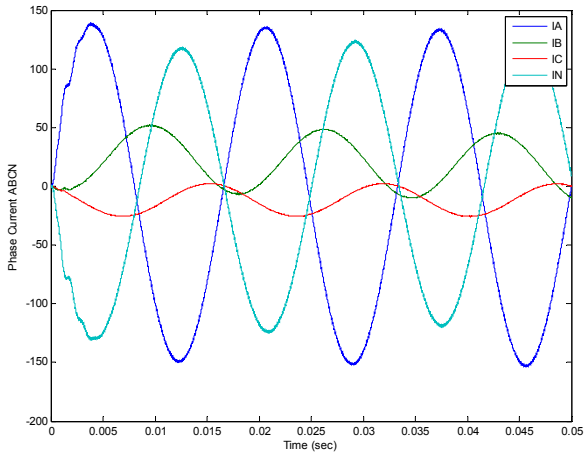


Figure 12. Simulation 2: Output Current

Simulation 3: Variable Frequency Voltage Command

The final simulation tests the controller's response to a variable frequency waveform. System and Load parameters are identical to the Simulation 1, except that a variable commanded frequency was applied, as shown in Figure 13.

Table 6. Simulation 3 Parameters

Parameter	Value	Parameter	Value
V_{DC}	400 V_{DC}	$f_{sampling}$	20kHz
L_f	200µH	K_{pv}	0.12 Ω^{-1}
R_{Lf}	50mΩ	K_{iv}	1000 Ω^{-1}/sec
C_f	40µF	K_{pi}	3.5/(V_{DC}/2) Ω
V_D*	120√2 V_{AC}	K_{ii}	17900/(V_{DC}/2) Ω/sec
V_Q*	0 V_{AC}	$R_{Load,A}$	25.2 Ω
V_0*	0 V_{AC}	$R_{Load,B}$	5.2 Ω
ω	Variable (See Figure 13)	$R_{Load,C}$	4.8 Ω

Figure 14 and Figure 15 show that, even with a variable commanded frequency, the proposed controller shows zero steady state error. Transient performance is similar to Simulation 1, with a notable underdamped ringing in voltage error, which has a settling time of approximately one cycle.

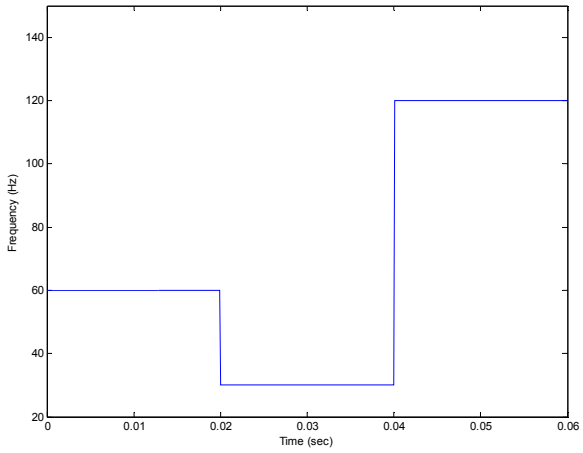


Figure 13. Simulation 3: Commanded Frequency

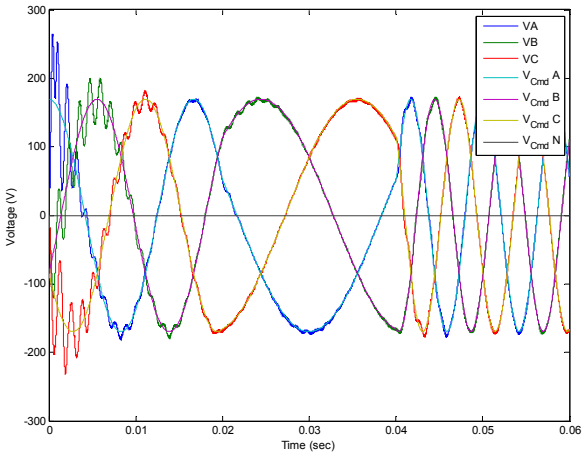


Figure 14. Simulation 3: Output Voltage ABCN Commanded vs. Actual

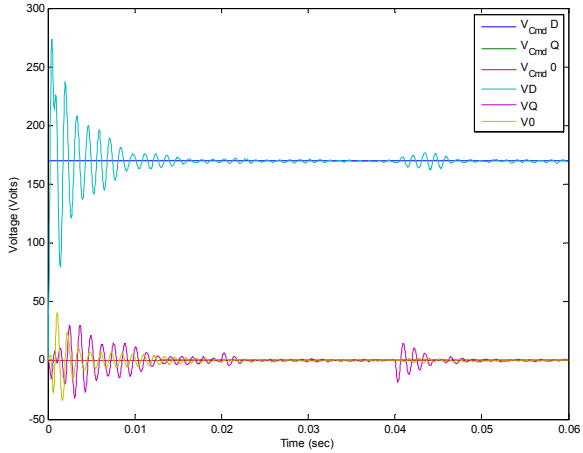


Figure 15. Simulation 3: Output Voltage DQ0 Commanded vs. Actual

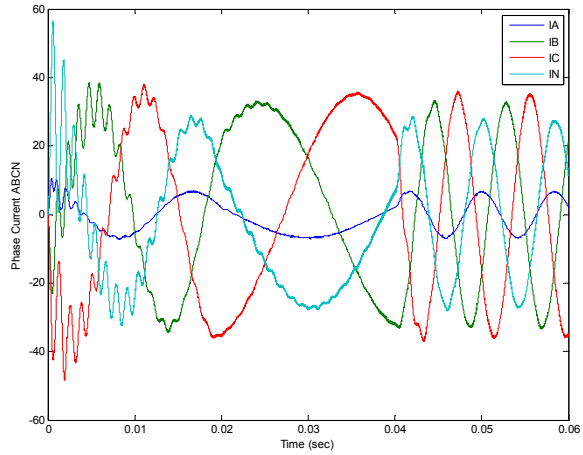


Figure 16. Simulation 3: Output Current

Conclusions

The above simulation results confirm that the proposed controller allows a voltage phasor at a specified frequency to be imposed on the phase-to-neutral voltage output. This commanded waveform has zero steady state error even for imbalanced loads, loads with a significant neutral current, or variable frequency command. The controller shows a significant ringing response, particularly to resistive loads, though this response (barely) meets the required max settling time of 1 cycle.

The controller tested in this paper used PI gains suggested by (1), with the addition of a small voltage integral term kiv to achieve zero steady state voltage error. It may be possible to improve transient performance by optimizing the selection of these gains. This would require a more detailed analysis of the dynamics of the inverter system in DQ0 space, for example, transfer functions or time-domain dynamic equations.

The controller simulated requires the measurement of filter capacitor current $I_{C,ABCN}$. This may present a problem in many implementations, since $I_{C,ABCN}$ contains a significant harmonic component at the switching frequency. This signal may have to be filtered to avoid aliasing, however, such filtration would introduce a phase shift that might cause stability issues or performance limitations.

The proposed controller functions quite well under a very wide variety of load conditions in a 3-phase 4-wire variable frequency inverter. More detailed design should allow the selection of PI gains to better optimize transient response. This controller should be capable of serving as the inner loop to more complex phasor-based algorithms for grid control.

References

1. *Decoupled control of a four-leg inverter via a new 4×4 transformation matrix.* **Ryan, M.J., De Doncker, R.W. and Lorenz, R.D.** vol.16, no.5, Sep 2001, Power Electronics, IEEE Transactions on, pp. 694-701.