SILICON-BASED TERAHERTZ SIGNAL GENERATION WITH MULTI-PHASE SUB-HARMONIC INJECTION LOCKING TECHNIQUE

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Taiyun Chi

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SILICON-BASED TERAHERTZ SIGNAL GENERATION WITH MULTI-PHASE SUB-HARMONIC INJECTION LOCKING TECHNIQUE

Approved by:

Dr. Hua Wang, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Muhannad S. Bakir
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. John Papapolymerou
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: 04/19/2016

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SUMMARY

This thesis presents a multi-phase injection locking (IL) technique and its application in the locking range extension in multi-phase injection locking oscillators (ILOs) for Terahertz (THz) signal generation. The proposed technique can significantly increase the frequency locking range of a multi-phase injection locking oscillator compared to the conventional single-phase injection locking scheme. Based on the multi-phase IL technique and sub-harmonic ILOs, an "active frequency multiplier chain" architecture and a multi-ring system layout topology are also proposed to achieve scalable THz signal generation. As proof of concept, a cascaded 3-stage 3-phase 2^{nd}-order sub-harmonic ILO chain is implemented in the IBM 9HP SiGe BiCMOS process. The design achieves a maximum output power of -16.6dBm at 498GHz, a phase noise of -87dBc/ Hz at 1MHz offset, and a total 5.1% frequency tuning range from 485.1GHz to 510.7GHz, which is the largest frequency tuning range among all the reported silicon-based THz oscillator sources in the 0.5THz band.

CHAPTER 1

INTRODUCTION

THz range, from 0.3THz to 3THz in the electromagnetic spectrum, has recently stimulated an increasing research interest with their unique applications, such as molecular spectroscopy, THz imaging, radar, and high-speed communication [1]–[3]. One of the major technology roadblocks of applying THz technologies lies in the lack of low-cost and compact THz sources. Most existing THz setups are based on discrete compound devices, bulky optics or quantum cascade lasers. Although these sources may support large output power at THz [4], [5], their low integration level, high-cost, and need for dedicated setups often limit their usage only in high-end research labs.

On the other hand, the continuous device scaling in silicon technologies (CMOS or SiGe BiCMOS) has shown tremendous promise to realize self-contained THz systems with low cost and compact form-factor [6]–[23]. However, there are several fundamental challenges for silicon technologies to generate large output power at THz range. First of all, according to the Johnson Limit [6], the product of the unity gain cutoff frequency f_T and the breakdown voltage V_m of a transistor is approximately a constant for a given semiconductor material, as

$$V_m \cdot f_T = \frac{E_m v_s}{2\pi}, \tag{1}$$

where E_m is the maximum electric field and v_s is the electron saturation velocity. As a result, although advanced silicon process nodes can provide higher f_T/f_{max}, the breakdown voltage also decreases, reducing the maximum allowed voltage swing and thus maximum output power delivered to the load. Secondly, the loss of the passive structures in standard silicon technologies does not decrease with device down-scaling either. This is because the thickness of top metal layers remains almost the same in scaled process nodes, which results in similar passive efficiency. The low-resistivity silicon substrate is another major loss factor for inductors, transformers and on-chip antennas in bulk silicon processes,

which again, does not improve in advanced process nodes except for special process, such as Silicon-on-Insulator (SOI) or Silicon-on-Sapphire (SoS). Vertical interconnects are getting more attractive at THz frequencies, but at the cost of post-processing and integration complexity. Therefore, there is an increasing need for design innovations on the circuit topologies and system architectures to improve the output power capability of silicon devices in the THz frequency range.

Besides sufficient output power, a broad bandwidth is equally important in many THz applications. For example, in an FMCW imaging radar, the range resolution of the radar is inversely proportional to its bandwidth [7]. Therefore, a higher range resolution can be achieved by increasing the system bandwidth. A large bandwidth is also critical in hyperspectral imaging systems, which measures the spectrum information of each pixel during the imaging to identify objects, characterize materials, and detect chemical processes [8], [9]. In addition, THz spectroscopy also prefers a large bandwidth to cover sufficient resonant peaks in the absorption spectrum [1]. Therefore, it is highly desirable for silicon-based THz sources to achieve both sufficient output power and bandwidth.

Figure 1 summarizes recently reported power generation designs in silicon. Below 150GHz, most designs are based on power amplifiers (PAs). This is because silicon transistors can provide sufficient power gain in this frequency range, which allows the implementation of PAs with both high output power and efficiency. Around 100GHz, power generation based on fundamental oscillators starts to become a viable design choice. These designs leverage the nature of oscillation to compensate the reduced transistor gain at these frequencies. However, the oscillation frequency of a fundamental oscillator is limited by the transistor f_{max}. Moreover, varactors commonly exhibit low quality factors (Q) in this frequency range, leading to a direct trade-off between frequency tuning range and output power. Above 150GHz, the intrinsic gain of silicon transistors starts to become inefficient to support power amplification. Therefore, passive frequency multipliers based on nonlinear passive devices, e.g., diodes and varators, become popular design choices to

generate harmonic signals from mm-wave pumping signals. Passive multipliers often offer broad bandwidths and consume low DC power. However, they also present substantial conversion loss during the passive harmonic generation, and therefore require inter-stage amplifiers to boost the signal level. The designs of these inter-stage amplifiers may become challenging to meet the high pumping signal power demands required by high-frequency passive multipliers. Another popular approach is to extract the harmonic signals from mm-wave oscillators. For example, the N-push oscillator (multi-phase oscillator) can naturally enable N^{th} harmonic extraction at its common node, while the fundamental tone, the 2^{nd} through $(N\text{-}1)^{th}$ order harmonics, are cancelled. In addition, there is no need for any high-power driving stages. Therefore, multi-phase oscillator has been a widely adopted technique to achieve THz power generation beyond f_{max} in silicon, although its frequency tuning range is often limited compared to passive multipliers.

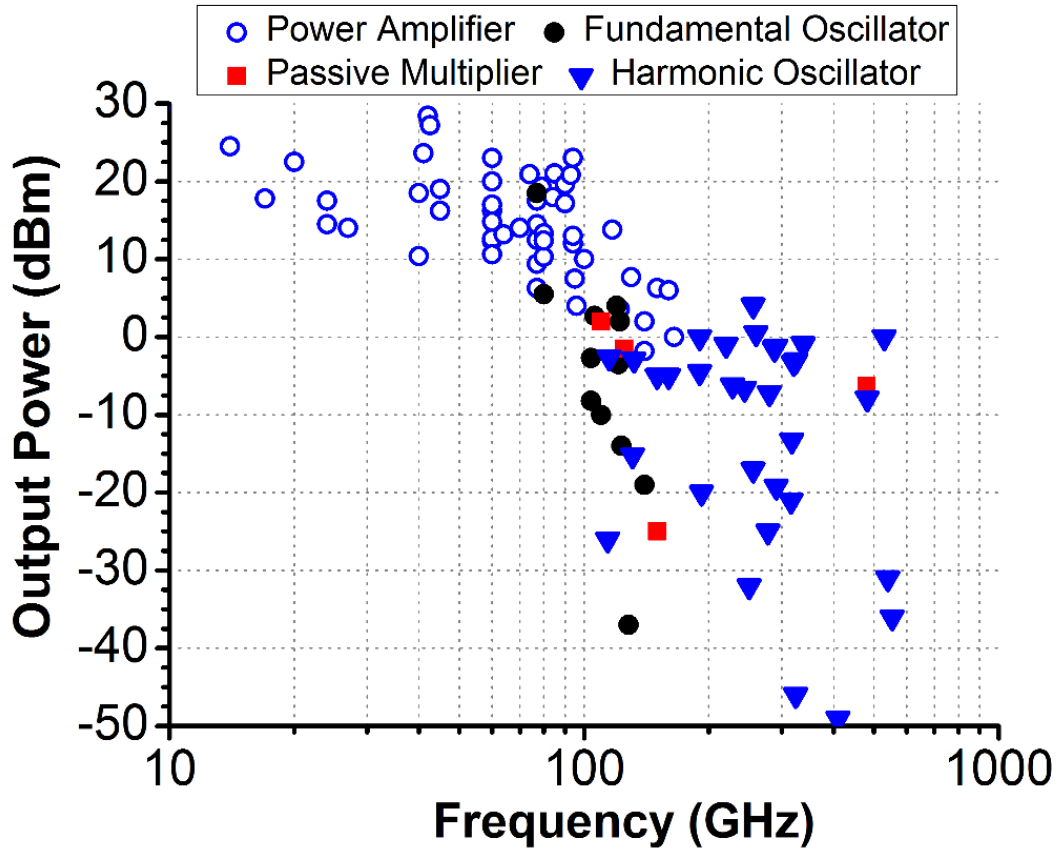

Figure 1. Recently reported power generation designs in silicon technologies (CMOS and SiGe BiCMOS).

In this thesis, a multi-phase injection locking (IL) technique is proposed, which can lock the N-push oscillator for coherent THz signal generation with both locking bandwidth extension and signal balancing for efficient harmonic extraction. Then, by employing multi-phase IL in sub-harmonic injection locking oscillators (ILOs), I also demonstrate an "active frequency multiplier" for frequency multiplication and signal restoration/amplification without any amplifiers. This enables a cascadable system architecture with several multi-phase sub-harmonic ILOs implemented in a chain to generate the THz signal from a reference source at a considerably lower frequency, e.g., tens of GHz. Such a low-frequency signal can be readily derived from a high-quality on-chip synthesizer for high spectral purity. Moreover, this cascadable topology opens the door for a scalable THz signal generation array, where each element can be locked to the common reference signal, and the THz signals from the array elements can be coherently combined to increase the output power. As proof of principle, a 3-stage 3-phase 2^{nd}-order sub-harmonic ILO chain is demonstrated in this thesis. It achieves a system tuning range of 5.1% (from 485.1GHz to 510.7GHz) with a phase noise of -87dBc/Hz at 1MHz offset, which is the largest frequency tuning range and best phase noise among all reported silicon-based THz oscillator sources in the 0.5THz band. Its maximum output power is -16.6dBm at 498GHz, and it achieves more than -20dBm across the system frequency tuning range.

This thesis is organized as follows. Chapter 2 presents the proposed multi-phase IL technique and demonstrates its benefits compared to the conventional single-phase IL approach. The scalable "active frequency multiplier" chain system topology and the design details of the 500GHz power generation system are presented in Chapter 3. The measurement results are shown in Chapter 4. Chapter 5 concludes this thesis with a performance comparison table.

CHAPTER 2

MULTI-PHASE INJECTION LOCKING TECHNIQUE

The multi-phase IL scheme was previously reported in the designs of RF frequency divider [24] and THz frequency divider [20]. We leverage the bandwidth extension nature of the multi-phase ILO to the THz signal generation. The following discussions will focus on an N-push oscillator operation, its harmonic extraction for THz signal generation, and its synchronization with multi-phase IL signals.

N-Push (Multi-Phase) LC Ring Oscillator

As an example, a 3-phase *LC* ring oscillator (120°-mode) is shown in Figure 2a. At the free-running frequency, the relative phases of the voltages V_1, V_2 and V_3 are 0°, 120° and 240° in the phasor analysis. Assume the transistors have negligible parasitic feed-through, the collector current (e.g., I_{osc1}) and the base voltage (e.g., V_1) of each transistor should be out of phase (180°). Thus, the *LC* tank provides -60° phase shift as its tank impedance to keep the 120° phase offset between the voltages of adjacent stages, e.g., V_1 and V_2 (Figure 2b). Assuming a constant quality factor Q around the natural resonance frequency ω_0 of the *LC* tank, the tank impedance is

$$Z(j\omega) = \frac{1}{\frac{1}{R} + \frac{1}{j\omega L} + j\omega C} = \frac{j\omega L}{\frac{j\omega L}{R} + (1 - \omega^2 LC)} = \frac{j\omega L}{\frac{j}{Q} + (1 - \frac{\omega^2}{\omega_0^2})}, \quad (2)$$

where R, L, and C are the parallel resistance, inductance, and capacitance of the tank. The quality factor and the resonant frequency are defined as

$$Q = \frac{R}{\omega L} \text{ and } \omega_0^2 = \frac{1}{LC}. \quad (3)$$

The phase of the tank impedance φ, i.e., the phase difference between tank current and voltage, is

$$\varphi = \frac{\pi}{2} - \arctan\left(\frac{1}{Q} \cdot \frac{\omega_0^2}{\omega_0^2 - \omega^2}\right) \text{for } \omega < \omega_0 \text{ , and} \quad (4)$$

$$\varphi = -\frac{\pi}{2} + \arctan\left(\frac{1}{Q} \cdot \frac{\omega_0^2}{\omega^2 - \omega_0^2}\right) \text{for } \omega > \omega_0 \,. \tag{5}$$

Note that with the definitions in (4) and (5), $0 < \varphi < \pi/2$ for $\omega < \omega_0$, and $-\pi/2 < \varphi < 0$ for $\omega > \omega_0$. Therefore, if the 3-phase ring oscillator oscillates in the 120°-mode, the oscillation frequency ω_{osc} should be higher than the resonant frequency ω_0 to provide the required -60° phase shift, as

$$\omega_{\text{osc}} = \sqrt{\frac{\sqrt{3}}{Q} + 1} \cdot \omega_0 \,. \tag{6}$$

The voltage phasors V_1, V_2 and V_3 at f_0, $2f_0$, and $3f_0$ are shown in Figure 2c. Assume there is no mismatch among all 3 stages, the 3rd harmonic signals from each stage are in-phase with the same amplitude and can be added constructively at the common node V_{out}. At the same time, all the harmonics which are not multiples of 3, e.g., f_0, $2f_0$, and $4f_0$, are naturally cancelled at V_{out} [11]. Therefore, this architecture allows the 3rd harmonic extraction for THz signal generation.

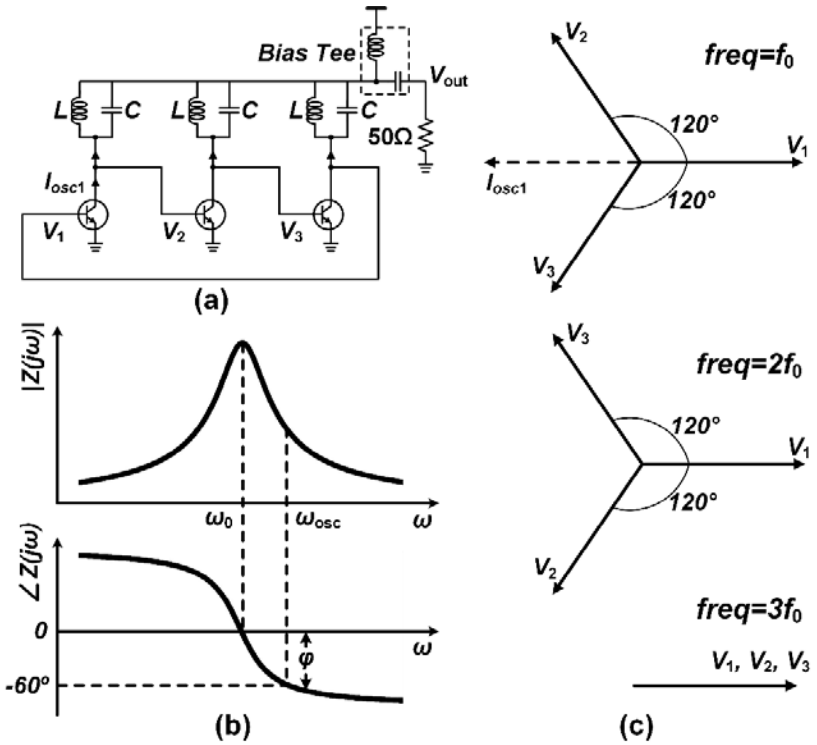

Figure 2. (a) A 3-phase *LC* ring oscillator in the 120°-mode. (b) The amplitude and phase of the *LC* tank impedance. (c) Voltage phasors at f_0, $2f_0$, and $3f_0$.

Multi-Phase Injection Locking Scheme

The simplified schematics of the single-phase and multi-phase IL schemes in a ring oscillator are shown in Figure 3. The conventional single-phase IL scheme feeds all the injection power into a single node. In contrast, in the proposed multi-phase IL scheme, the total injection power is split into N-ways and applied to each stage with the proper phase shifts to match the desired oscillation mode. To make a fair comparison on the resulting frequency locking range, the same total injection power is applied for the two schemes. Thus, the amplitude of the single-phase injection current is $\sqrt{N}$ larger than that in the multi-phase case, where N is the number of stages in the N-push oscillator.

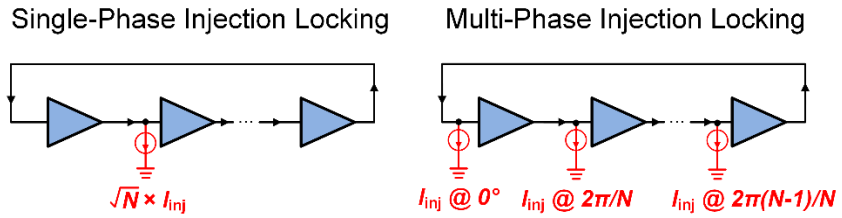

Figure 3. Single-phase vs. multi-phase injection locking scheme.

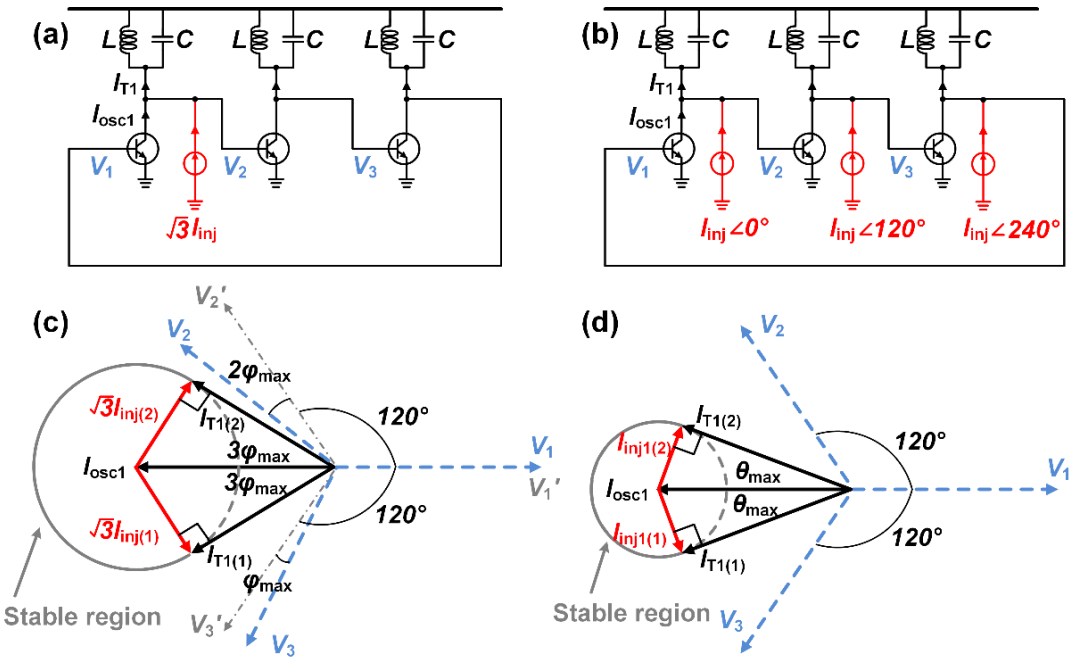

Figure 4. (a) A 3-phase *LC* ring oscillator with the single-phase injection locking (IL) scheme. (b) A 3-phase *LC* ring oscillator with the three-phase IL scheme. (c) The phasor diagram denoting the maximum phase shift in the single-phase IL scheme. (d) The phasor diagram denoting the maximum phase shift in the three-phase IL scheme.

The multi-phase IL scheme is analyzed first by using a 3-phase *LC* ring oscillator as an example (Figure 4b). The 3-phase IL scheme assumes that the 3 injection currents at ω_{inj} with 0°, 120°, and 240° phases are applied at the 3 transistor collectors. These injection currents are able to lock the oscillator from free-running frequency ω_{osc} to the injection frequency ω_{inj}. Due to the symmetry, the node voltages V_1, V_2, and V_3 automatically preserve the balanced amplitude and 120° phase difference (Figure 4d). Taking the first stage of the oscillator as an example, the *LC* tank current I_{T1} is a vector sum of the collector current I_{osc1} and the injection current I_{inj1}. The phase difference between the tank current I_{T1} and the tank voltage V_2 is due to the tank impedance function (2) with $\omega=\omega_{inj}$. Therefore, the frequency locking range of the oscillator can be determined by locating the maximum and minimum phase difference between I_{T1} and V_2 as a function of the I_{inj1}, whose possible vector values form a circle centered at I_{osc1}. On the phasor vector plot (Figure 4d), the maximum phase difference between I_{osc1} and I_{T1} can be found as,

$$\theta_{\max} = \arcsin\left(\frac{I_{\text{inj}}}{I_{\text{osc}}}\right), \tag{7}$$

$$-\left(\frac{\pi}{3} + \theta_{\max}\right) = -\frac{\pi}{2} + \arctan\left(\frac{1}{Q} \cdot \frac{\omega_0^2}{\omega_{\text{h}}^2 - \omega_0^2}\right), \text{and} \tag{8}$$

$$-\left(\frac{\pi}{3} - \theta_{\max}\right) = -\frac{\pi}{2} + \arctan\left(\frac{1}{Q} \cdot \frac{\omega_0^2}{\omega_{\text{l}}^2 - \omega_0^2}\right), \tag{9}$$

where θ_{max} represents the maximum phase difference between I_{osc1} and I_{T1}; ω_h is the higher frequency locking boundary; ω_l is the lower frequency locking boundary. From (8) and (9), the frequency locking boundaries can be determined as

$$\omega_{\text{h}} = \sqrt{\omega_0^2 + \frac{\omega_0^2}{Q \cdot \tan\left(\frac{\pi}{6} - \theta_{\max}\right)}} \quad \text{and} \quad \omega_{\text{l}} = \sqrt{\omega_0^2 + \frac{\omega_0^2}{Q \cdot \tan\left(\frac{\pi}{6} + \theta_{\max}\right)}}. \tag{10}$$

Therefore, the final normalized frequency locking range can be derived as

$$\frac{\omega_{\mathrm{h}}-\omega_{\mathrm{l}}}{\omega_{\mathrm{osc}}}=\frac{\sqrt{Q+\frac{1}{\tan\left(\frac{\pi}{6}-\theta_{\max}\right)}}-\sqrt{Q+\frac{1}{\tan\left(\frac{\pi}{6}+\theta_{\max}\right)}}}{\sqrt{Q+\sqrt{3}}}. \tag{11}$$

Next, the voltage and current phasor relationship for the single-phase IL scheme is analyzed (Figure 4a and 4c). In this case, the IL current $\sqrt{3}I_{\mathrm{inj}}$ acts only at a single node, resulting in two issues particularly relevant for harmonic-based THz signal generation. First, the single injection node now needs to provide all the additional phase shift between I_{osc} and I_{T} (previously distributed equally among all the 3 nodes in the three-phsae IL scheme) to ensure locking. Assume the maximum phase difference between I_{osc1} and I_{T1} is $3\varphi_{\max}$ with $\varphi_{\max}$ as

$$\varphi_{\max}=\frac{1}{3}\arcsin\left(\frac{\sqrt{3}I_{\mathrm{inj}}}{I_{\mathrm{osc}}}\right). \tag{12}$$

Thus, the minimum and maximum phase differences between I_{T1} and V_2 equal $-(\pi/3-\varphi_{\max})$ and $-(\pi/3+\varphi_{\max})$, respectively, and the locking range can be derived using (8)–(11).

To compare the frequency locking range of the three-phase IL scheme and the single-phase IL scheme, one can directly compare $\theta_{\max}$ and $\varphi_{\max}$, which are the maximum additional phases provided by the *LC* tank for the three-phase IL/single-phase IL scheme (Figure 4). Take the difference between $\theta_{\max}$ and $\varphi_{\max}$ as

$$\theta_{max}-\varphi_{max}=\arcsin\left(\frac{I_{inj}}{I_{osc}}\right)-\frac{1}{3}\arcsin\left(\frac{\sqrt{3}I_{inj}}{I_{osc}}\right). \tag{13}$$

The first derivative of (13) can be calculated as

$$\frac{d(\theta_{max}-\varphi_{max})}{d\left(\frac{I_{inj}}{I_{osc}}\right)}=\frac{1}{\sqrt{1-\left(\frac{I_{inj}}{I_{osc}}\right)^2}}-\frac{1}{\sqrt{3-9\left(\frac{I_{inj}}{I_{osc}}\right)^2}}. \tag{14}$$

Note that the phase provided by an *LC* tank should be between -π/2 and π/2. In addition, the phase of the *LC* tank equals π/3 at the free-running frequency (in the 120º-

mode). Therefore, an additional phase shift of the tank due to IL is within $\pi/6$, so I_{inj}/I_{osc} should be smaller than 0.5 to ensure $\theta_{max} < \pi/6$ based on (7).

From (13) one can get $\theta_{max} = \varphi_{max}$ only for $I_{inj}/I_{osc}=0$. Furthermore, from (14) one can get,

$$\frac{d(\theta_{max} - \varphi_{max})}{d\left(\frac{I_{inj}}{I_{osc}}\right)} > 0 \text{ for } \frac{I_{inj}}{I_{osc}} < 0.5\,, \tag{15}$$

meaning that $\theta_{max} > \varphi_{max}$ always holds for $I_{inj}/I_{osc} < 0.5$.

Therefore, the three-phase IL scheme provides larger additional phase shift of the *LC* tank compared to the single-phase IL scheme, meaning that the three-phase IL scheme can achieve larger frequency tuning range with the same total injection power. Similar analysis can be generalized to the N-phase IL scheme to show that it out-performs its single-phase IL counterpart.

The frequency locking ranges for these two schemes at different tank *Q*-factor are computed based on (7), (11) and (12), and are plotted in Figure 5a. For a given total IL power, the 3-phase IL scheme always offers a larger frequency locking range. Circuit simulations also confirm the superior locking range of the multi-phase IL scheme (Figure 5b) based on the schematics shown in Figure4. In this basic simulation demonstration, the injection currents are provided by ideal current sources and no device parasitics are included for simplicity. The HBTs are based on the IBM 9HP design kit model with 5μm×100nm as their emitter size and a supply voltage of 1.5V.

The other issue in the single-phase IL scheme is that the node voltages V_1, V_2, and V_3 will deviate from the desired symmetry. For example, if the IL current $\sqrt{3}I_{inj(1)}$ adds extra phase 3φ in the loop, the original voltage phasors V_2' and V_3' will rotate to V_2 and V_3, respectively. As a result, the phase difference between V_3 and V_1 (or V_2 and V_3) equals $120°-\varphi$ where the phase difference between V_1 and V_2 is $120°+2\varphi$ (Figure 4c). Note that this phase imbalance will be 2 times larger for the 2nd harmonic and 3 times larger for the

3rd harmonic signals. It compromises the fundamental and 2nd harmonic suppression and more importantly degrades the in-phase power combining and extraction of the 3rd harmonic signals at the common node. The simulation results from Figure 5b also shows that the simulated 3rd harmonic output power for three-phase IL is always higher than its single-phase IL counterpart.

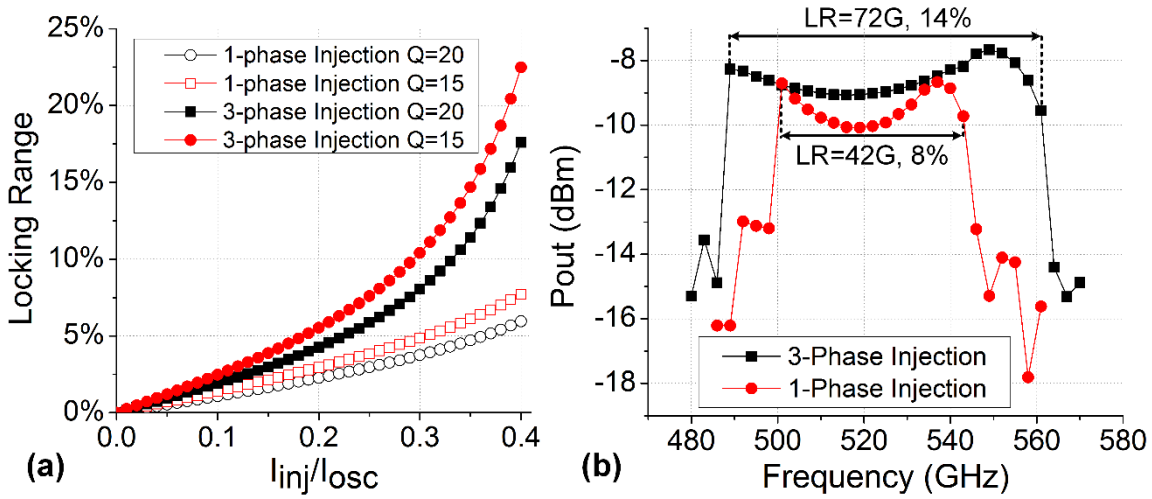

Figure 5. (a) Theoretically calculated locking ranges for the multi-phase and single-phase IL schemes on a 3-phase oscillator (Figure 4a and Figure 4b) at different tank Q (quality factor). (b) Schematic simulation of the locking range of a 3-phase 175GHz oscillator (I_{inj}/I_{osc}=0.33) with current source injection for producing its 3rd harmonic signal at 525GHz.

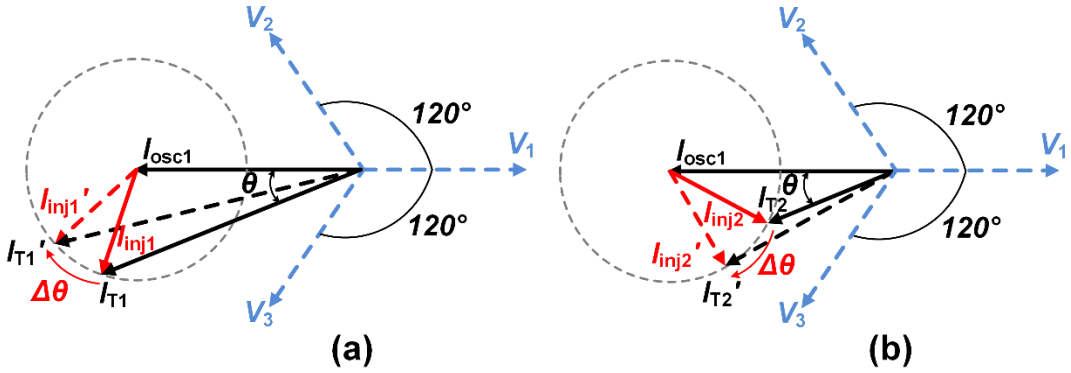

Figure 6. Perturbation analysis for two possible modes. (a) The stable mode. (b) The unstable mode.

In addition, for frequencies within this locking range, there are two possible phase solutions (Figure 6). The perturbation analysis [25] can be utilized to show that only the

mode in Figure 6a is stable. A graphical proof can be applied on the phasor diagram to demonstrate the mode stability. Assume ω_{inj} is larger than ω_0 for the mode in Figure6a. If the phase of V_1 experiences a small perturbation by a positive angle $\Delta\theta$, the phase of I_{inj1} lags by the same angle $\Delta\theta$, as shown in Figure 6a. Therefore, the phase difference between I_{T1} and I_{osc1} will decrease and result in a frequency decrease of the oscillator. This counteracts with the phase advance of V_1, meaning that the mode in Figure 6a is stable. Similarly, for the mode in Figure 6b, with a small perturbation by a positive angle $\Delta\theta$ in V_1, the oscillation frequency will increase, indicating the instability of this mode. To summarize this perturbation analysis, the stable regions are denoted in Figure 4c and Figure 4d.

CHAPTER 3

A SCALABLE AND CASCADABLE MULTI-PHASE SUB-HARMONIC INJECTION LOCKING ARCHITECTURE FOR THZ SIGNAL GENERATION

Based on the multi-phase IL technique, a scalable and cascadable "active frequency multiplier" architecture is proposed to achieve THz generation from a mm-wave tone. The system architecture and the detailed design considerations are presented below.

System Architecture

The multi-phase IL is combined with the sub-harmonic ILOs to realize an "active frequency multiplier" (Figure 7). First, the input of the system can be generated at f_0 by a mm-wave or RF signal source, e.g., a PLL or a free-running VCO. Then, the N_1^{th} harmonic signals of the input and extracted and injected to an oscillator operating at $N_1 \times f_0$. The ILO ensures the frequency/phase synchronization with the input tone at f_0. More importantly, it restores the signal amplitude at $N_1 \times f_0$ after the frequency multiplication to compensate the conversion loss in the harmonic generation. Next, the N_2^{th} harmonic signals from the first ILO and are injected to the next ILO at $N_1 \times N_2 \times f_0$ frequency. By cascading these sub-harmonic ILOs, an "active frequency multiplier" chain is created. Finally, the harmonic signal from the last stage ILO can be extracted as the desired THz output signal. Note that the system can be conveniently achieved if all the ILOs are implemented as multi-phase oscillators which provide bandwidth extension and signal balancing simultaneously.

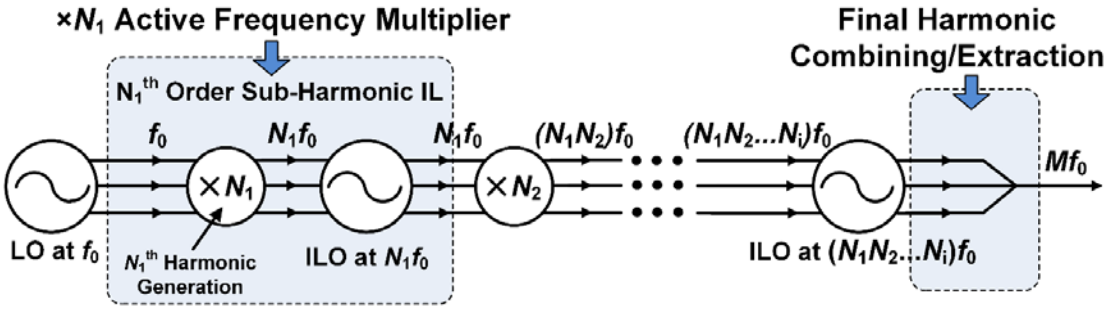

Figure 7. The proposed system architecture as an "active frequency multiplier" chain.

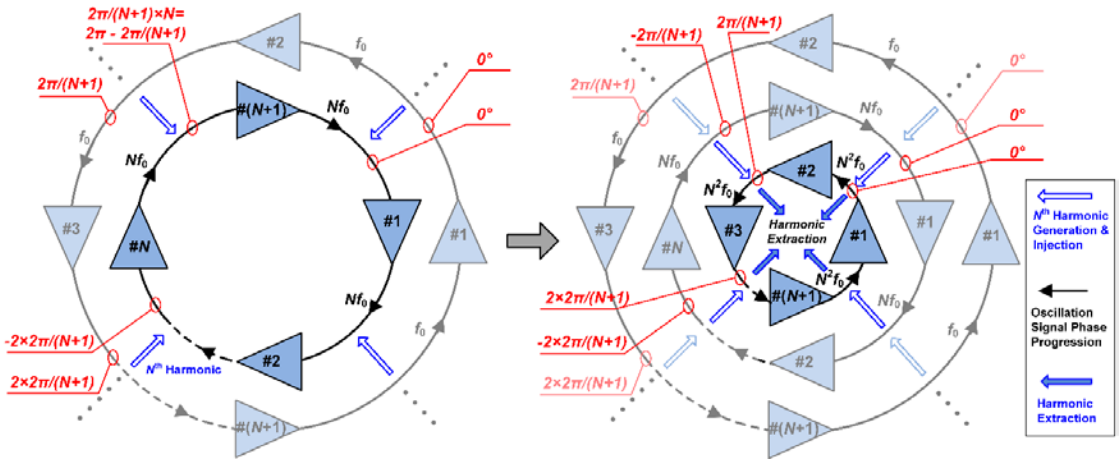

Figure 8. The proposed ring style system layout scheme.

Moreover, the proposed "active frequency multiplier" chain can be realized in a multi-ring topology if the sub-harmonic index and the multi-phase ILO stage number are co-prime. A special case for the N^{th} sub-harmonic IL and (N+1)-phase ILO is shown in Figure 8. Assume that the outermost ring is an (N+1)-stage ILO with its phase progression in the counter-clockwise direction at f_0 and the phase difference between each adjacent stage is $2\pi/(N+1)$. Thus, the phases at each stage are 0, $2\pi/(N+1)$, and $4\pi/(N+1)$, etc. If the N^{th} harmonic signals from each stage of this ILO are used to injection-lock the 2nd outermost ring ILO, the phases of these N^{th} harmonic signals are 0, $-2\pi/(N+1)$, and $-4\pi/(N+1)$, etc. Using these harmonic signals for locking, the 2nd outermost ring thus should oscillate with its phase progression in the clockwise direction, i.e., in the reversed direction compared to the outermost ring. Similarly, if the N^{th} harmonics of the (N+1) signals from the 2nd outermost ring ILO are used to lock the 3rd ring ILO, this will result in a counter-clockwise oscillation mode for the 3rd ring ILO. The signal frequency is gradually multiplied up from the outer rings to the inner rings, and all the rings can be mutually locked. Finally, the innermost ring ILO oscillates at the highest frequency, and its harmonic signal can be extracted as the desired THz output signal. This proposed ring style layout scheme provides the desired phase progression and significantly simplifies the high-

frequency signal routing, which are highly critical in the THz designs. Moreover, by employing more outer rings, the input frequency of the system can be further reduced.

This system architecture can also be scaled to an array where each element can be locked to a common reference at a considerably lower frequency, e.g., tens of GHz, by using the proposed sub-harmonic IL chain. Therefore, THz signals from the array elements can be coherently combined to further increase the output power. Note that the multi-phase outermost ring oscillator can be potentially included into an on-chip PLL. For example, one output from the multi-phase outermost ring can be connected to the frequency divider in the PLL, while the other outputs are connected to dummy loads to keep the balancing. Using this approach, the outermost ring oscillator can be locked to a MHz crystal reference signal, which will further facilitate the reference signal distribution among the array elements.

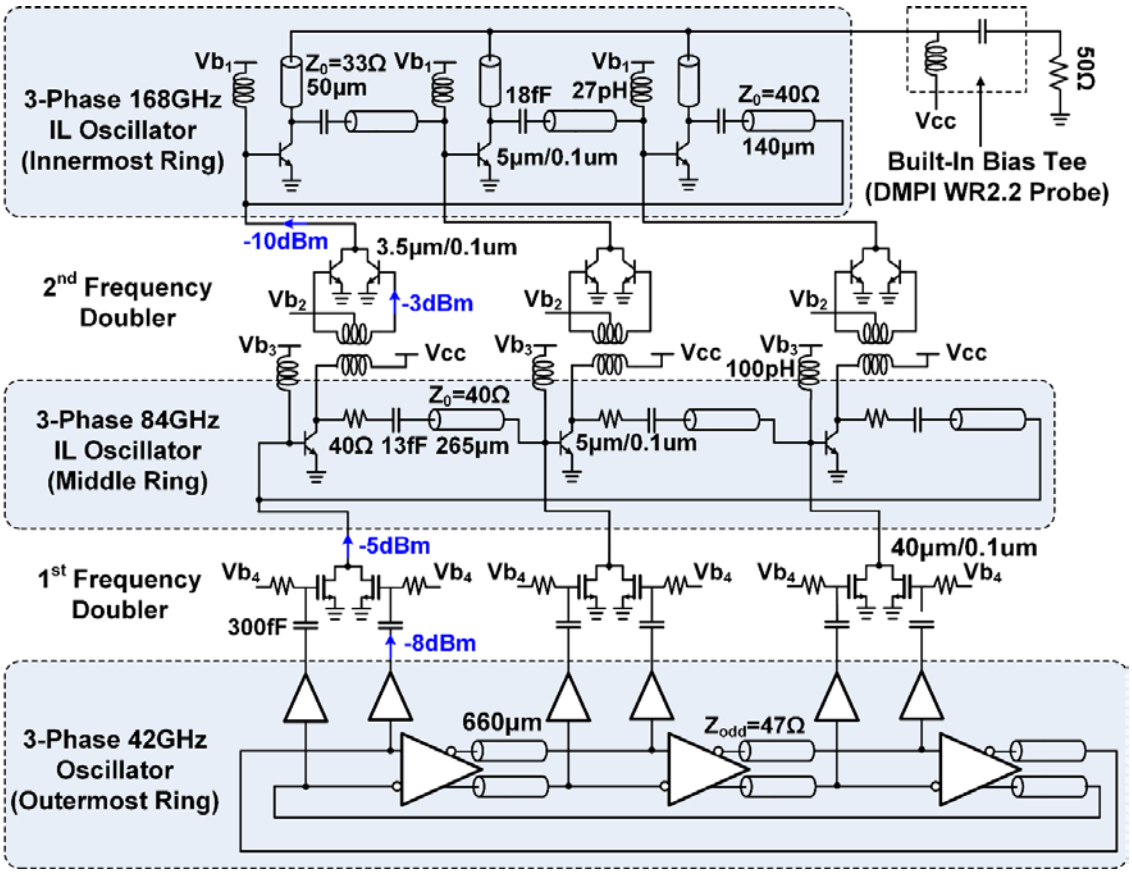

Figure 9. Circuit schematic of the THz signal generation system.

As proof of concept, a cascaded 3-stage 3-phase 2nd-order sub-harmonic ILO chain for 500GHz signal generation is implemented (Figure 9). The design details are shown below.

Process Technology

The THz signal generation circuit is implemented in the IBM 9HP SiGe BiCMOS process. It is a 90-nm process node which features high-speed SiGe HBTs with a maximum f_T/f_{max} of 300/350GHz. The BV_{CEO} of the high-speed HBT is 1.5V. This technology uses HiCUM model for the HBT devices. The design kit also provides MOSFETs with a drawn gate length of 100nm.

The 3-Phase 168GHz Oscillator (Innermost Ring ILO)

The innermost ring, i.e., the final stage of the system, is a 3-phase 168GHz ILO (120°-mode). The equivalent circuit for a single stage is shown in Figure 10. To generate the maximum output power for a transistor at a given fundamental frequency, there exists optimum conditions for the gain (A_{opt}) and phase difference (φ_{opt}) between the input and output of the transistor [11]. These optimum conditions are given as

$$A_{\text{opt}} = \sqrt{\frac{Re\{Y_{11}\}}{Re\{Y_{22}\}}}\,, \tag{16}$$

$$\varphi_{\text{opt}} = (2k+1)\pi - \angle(Y_{12} + Y_{21}^{*})\,. \tag{17}$$

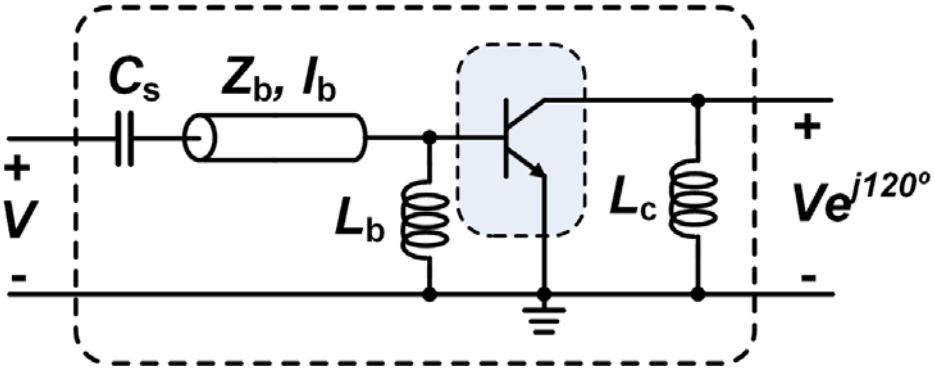

Figure 10. Equivalent circuit for a single stage ILO at fundamental frequency f_0.

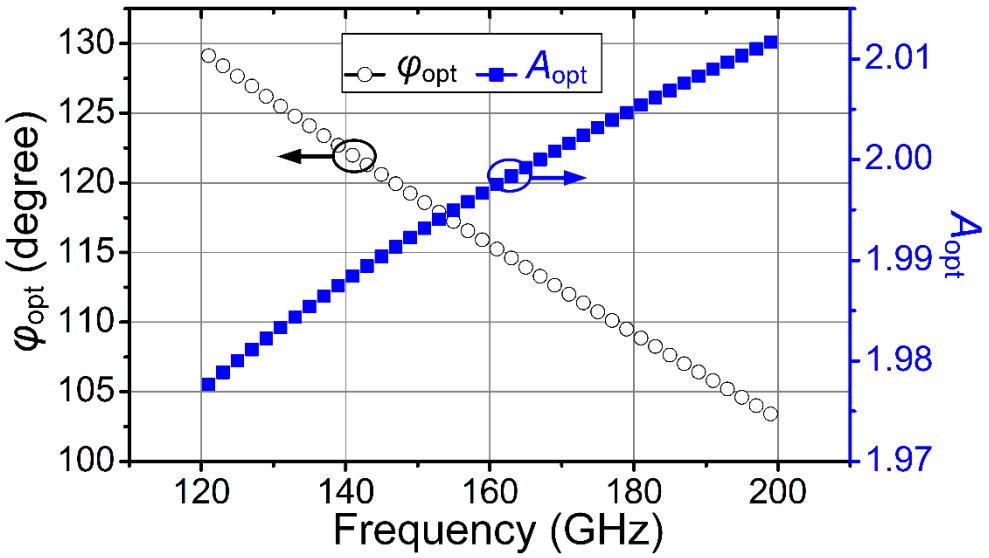

Figure 11. The optimum amplitude and phase conditions for a HBT with size of 5μm×100nm.

Figure 11 shows the simulated A_{opt} and φ_{opt} for a stand-alone HBT device (emitter size = 5μm×100nm). At 168GHz, the simulated A_{opt} is 2 and φ_{opt} is 113°. Since the simulated φ_{opt} is close to 120°, a 3-phase *LC* ring oscillator topology with a +120° phase progression becomes a natural choice. Improving the oscillator voltage swing at the fundamental frequency also makes the device more nonlinear and facilitates the 3rd harmonic current generation.

Shunt inductor L_b is added to resonate out the parasitic base capacitance of the HBT as well as provide DC bias for the base. L_b is realized by a short T-Line as 27pH at 168GHz. Series capacitor C_s of 18fF is used to block the DC between the adjacent stages. The T-line, with a characteristic impedance of Z_b=40Ω and length of l_b=140μm, together with C_s further helps the HBT to meet both optimum gain and phase difference conditions in (16) and (17).

At $3f_0$, the equivalent schematic of one stage is shown in Figure 12a. The nonlinearity of the HBT generates the 3rd harmonic current I_{3f0} at the collector. The currents (I_{3f0}) from each of the 3 branches are all in phase, each stage thus has an equivalent load of 150Ω. Moreover, in this equivalent circuit, the node connected to the collector of the

previous stage (to the left of C_s) can now be directly connected to the collector of the current stage to simplify the analysis with the loading effects. In order to deliver more power at $3f_0$ to the load, the impedance Z_1 should be boosted, so that more $3f_0$ harmonic current can sink into the load. As shown in Figure 12b, after the impedance transformation of the T-line and C_s, the low base impedance can be increased by a factor of 3.5 from 8.8Ω to 31Ω, as expressed by

$$Z_1 = \frac{1}{j\omega C_s} + Z_b \cdot \frac{Z_{base} + jZ_b \tan(\beta l_b)}{Z_b + jZ_{base} \tan(\beta l_b)}. \quad (18)$$

Based on the harmonic balance simulations, the base voltage swing at $3f_0$ is 13dB lower than the collector voltage swing. Although a shorter T-line will further increase Z_1 at $3f_0$ with better 3rd harmonic blocking, there exists a practical trade-off, since this T-line length is limited by the size of the innermost ring ILO to accommodate the output GSG pads and output combining network.

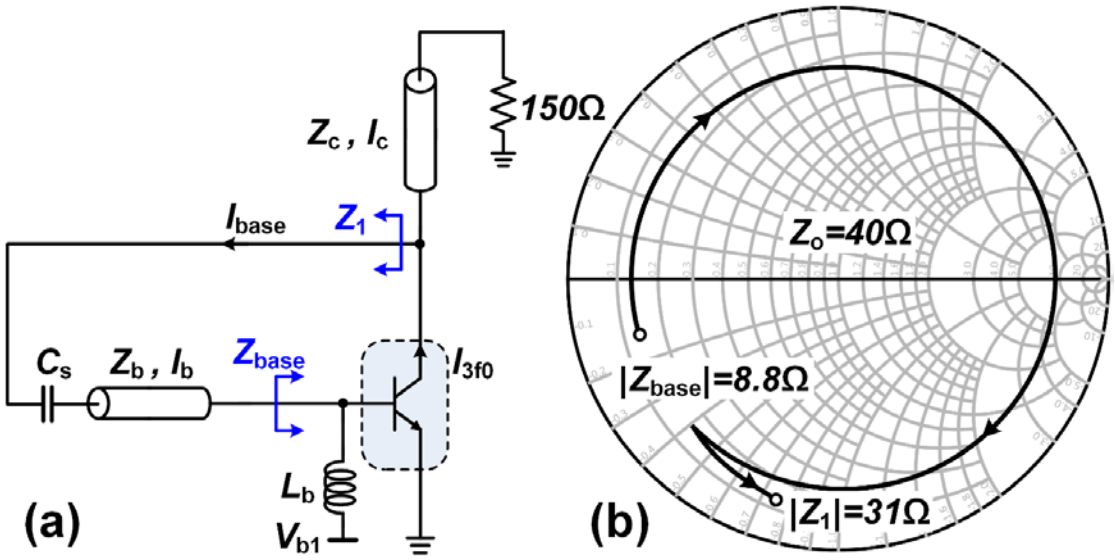

Figure 12. (a) Equivalent circuit for a single stage ILO at $3f_0$. (b) The low Z_{base} is transformed to a higher impedance at $3f_0$ through T-line and C_s.

Short T-lines serve as the peaking inductors at the collectors as well as the 3rd harmonic extraction network. Since it is critical to maintain the symmetry of the layout and account for any parasitic coupling, all T-lines, connections and output GSG pads are co-

designed using a 3D EM simulator HFSS (Figure 13a). The simulated transient oscillation waveforms based on the actual layout and the 3D EM modeling are shown in Figure 13b. Despite all the non-ideal effects of the practical layouts and routings, the oscillation waveforms still preserve good symmetry and balancing. The simulated frequency locking range of the innermost ring is shown in Figure 14a, which includes the loading of the 2nd-stage frequency doublers and assumes a total injection power of 4.8dBm at 84GHz. A simulated locking range of 6.8% and a maximum output power of -13dBm are achieved. Compared with Figure 5b, the frequency locking range is reduced and the peak output power also decreases because of the loading effect from the IL circuits, the limited available injection power from the previous stage, device layout parasitics, and the degraded routing symmetry in the EM structure. Figure 14b shows a typical output spectrum in this full extracted simulation with the fundamental, 2nd, 3rd, 4th, 5th, and 6th order harmonics. A P_{out} of -13dBm is achieved at the 3rd order harmonic. The fundamental leakage is 13dB lower than the 481.2GHz output signal while the 2nd harmonic is suppressed by 29dB. Without applying injection power, the simulated phase noise at the fundamental frequency is -85.2dBc/Hz at 1MHz offset and the simulated phase noise of the 3rd harmonic output signal is -75.7dBc/Hz at 1MHz offset.

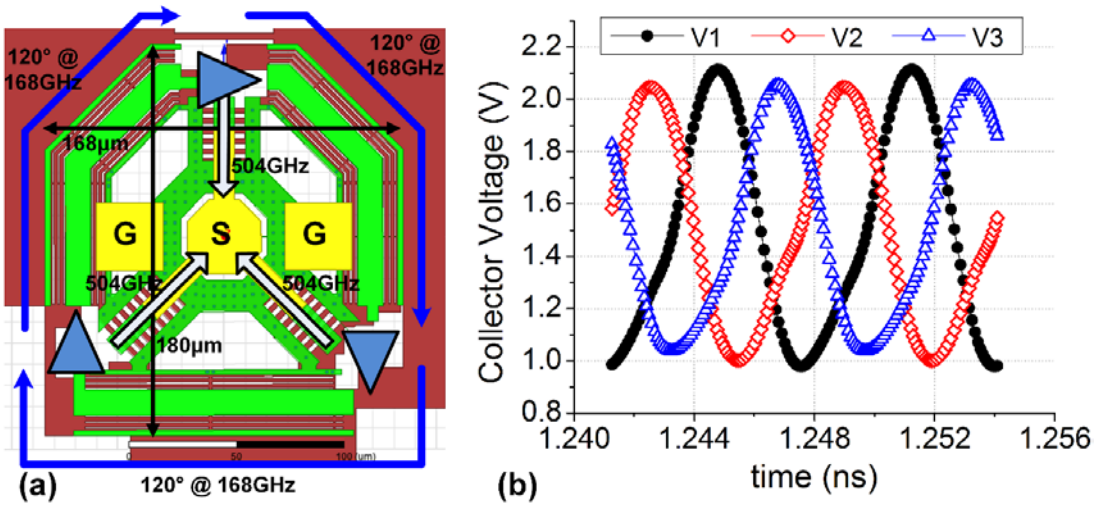

Figure 13. (a) The passive structure of the 3-phase 168GHz oscillator. (b) Transient simulation of the 3-phase 168GHz oscillation waveforms with the layout extraction and the 3D EM modeling.

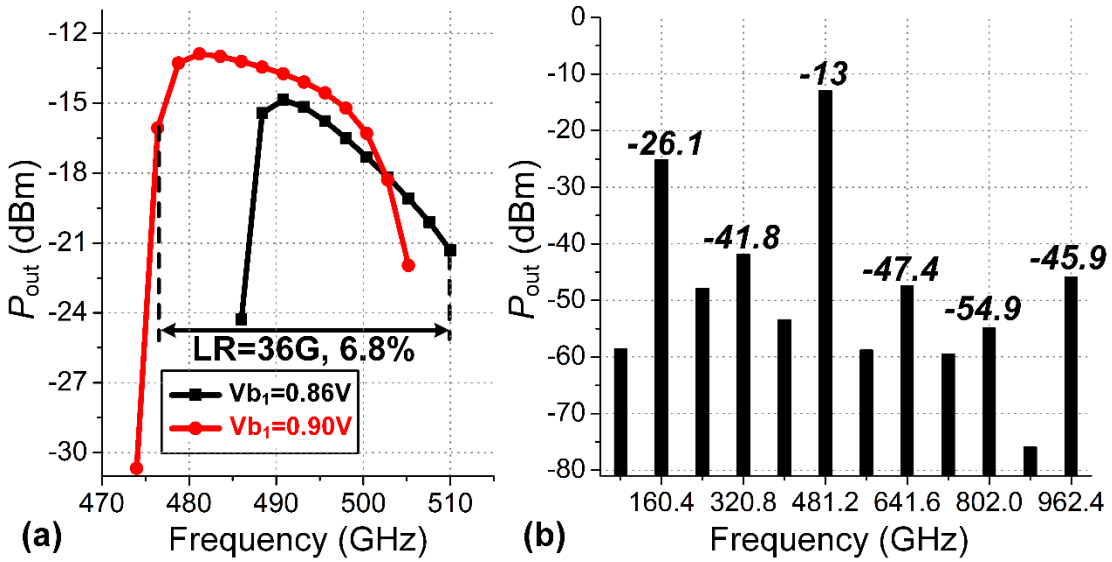

Figure 14. (a) Simulated locking range of the innermost ring ILO. (b) Simulated output spectrum with the fundamental and the 2nd, 3rd, 4th, 5th, and 6th order harmonics. A P_{out} of -13dBm is achieved at the 3rd order harmonic.

The 3-Phase 84GHz Oscillator (Middle Ring ILO)

Similar to the innermost ring ILO, the middle ring is a 3-phase *LC* ring oscillator at 84GHz, but oscillating in the 240°-mode. In order to ensure that the locking range of the middle ring can cover the locking range of the innermost ring under PVT variations, series resistors of 40Ω are added at each stage to boost the locking range by slightly sacrificing the loop gain (Figure 9). The simulated frequency locking range of the middle ring is 8.6%. A passive transformer-based balun is employed at each output to generate differential signals, which are then fed to a frequency doubler (push-push pair) to generate the injection currents at 168GHz for the innermost ring ILO.

The passive balun adopts a compact transformer-based design with its 3D EM model shown in the Figure 15a. Transformer-based baluns are widely used in RF applications since they can provide well-balanced outputs with a broad bandwidth, and achieve impedance transformation within a single inductor footprint [26]. However, a balancing issue may arise at high frequency because of the distributed capacitive coupling between the primary and secondary coils. In a transformer-based balun, the primary coil is

driven in a single-ended fashion with one terminal connected to the AC ground. Therefore, from the capacitive coupling perspective, the primary coil couples a strong signal to the secondary coil at its un-grounded terminal (i.e., input feed), but it only couples a weak signal at its grounded terminal. This is the fundamental reason of the unbalanced behavior of a transformer-based balun at high-frequency. Such unbalancing can be mitigated by using a multiple-turn structure at lower frequencies. However, due to the self-resonance-frequency (SRF) constraint, most of the transformers can only be implemented in a one-turn fashion at the mm-wave frequency.

To improve the signal balance in our design, the primary and secondary coils are offset to mitigate the capacitive coupling between the primary and secondary coils [27]. The primary coil is also rotated by 45° to further improve balance and more importantly facilitates the inter-stage routing. Figure 16a shows the simulated amplitude and phase mismatches versus different offset values at different transformer radiuses. It can be seen that there are multiple solutions which achieve good amplitude and phase balancing simultaneously. The final design parameters should be chosen together with the required coupling coefficient (k) and the primary self-inductance (L) which are plotted in Figure 16b. In this design, an offset distance of 8.5μm and a radius of 32μm are chosen (Figure 15). At 84GHz, this offset balun structure achieves an amplitude mismatch of only 0.3dB and a phase mismatch of 2.9° with an SRF of 140GHz.

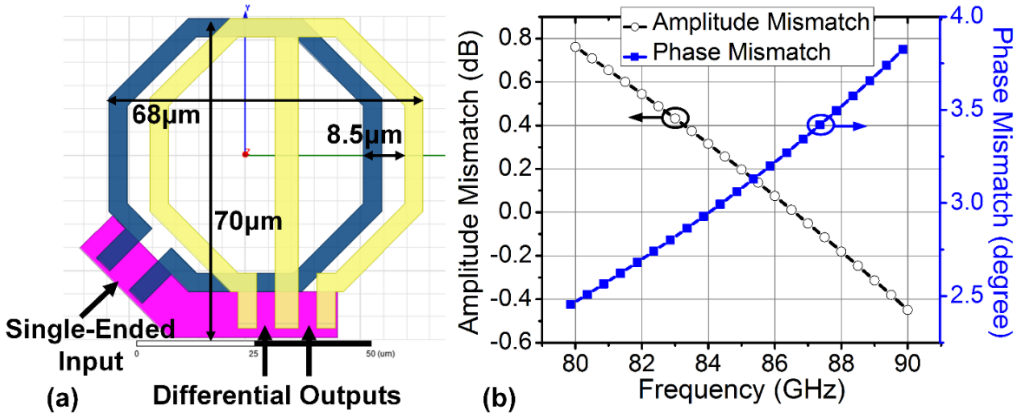

Figure 15. (a) The EM model of the proposed offset transformer-based balun. (b) Simulated amplitude mismatch and phase mismatch of the balun.

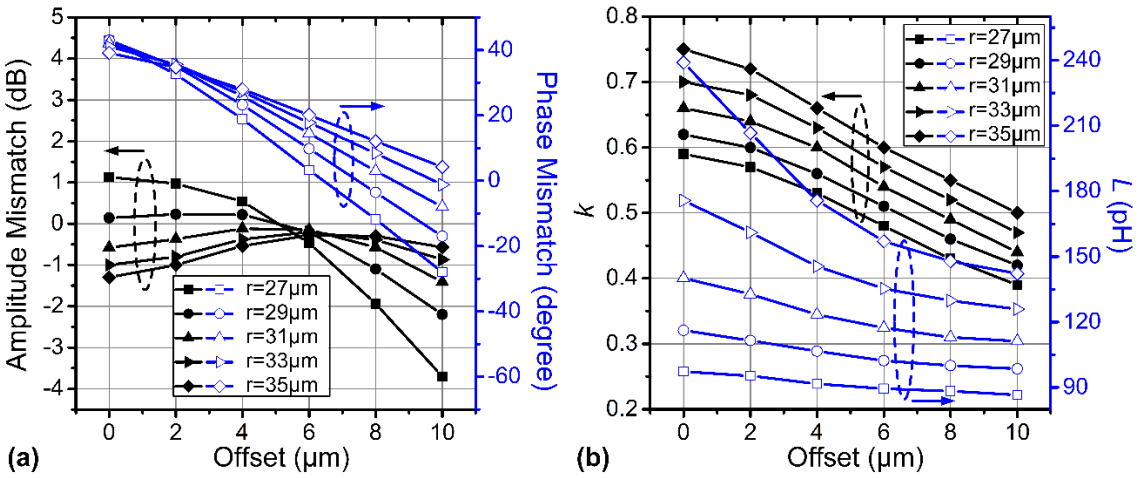

Figure 16. (a) Simulated amplitude mismatch and phase mismatch versus different offset values at different transformer radiuses. (b) Simulated coupling coefficient (*k*) and primary inductance value (*L*) versus different offset values at different transformer radiuses.

The single-ended input of the balun is used as part of the resonance tank in the middle ring oscillator, and the parallel inductance value should be around 140pH to achieve a free-running frequency of 84GHz. If the two differential outputs are well-balanced, the on-chip balun can be modeled using the simplified transformer model [28], [29] shown in Figure 17. The desired single-ended input impedance can be obtained by

$$Z_{\text{single}} = j\omega(1-k^2)L + r_{\text{p}} + \frac{k^2}{n^2}(r_{\text{s}} + Z_{\text{diff}})//j\omega k^2 L\,, \tag{19}$$

where k is the coupling coefficient, n is the turn ratio, L is the primary self-inductance, r_{p} and r_{s} are the loss resistances in the primary and secondary windings. The differential input impedance of the next stage frequency doubler is (32-j30) Ω, as an equivalent impedance based on a 60Ω resistor parallel with a 30fF capacitor at 84GHz. Figure 18a shows the EM-simulated Z_{single} and the modeled Z_{single} based on (19), demonstrating well-matched results. In addition, the EM-simulated and modeled passive losses of the balun are plotted in Figure 18b. When the balun is loaded by the next-stage doubler, its passive loss is 0.88dB at 84GHz.

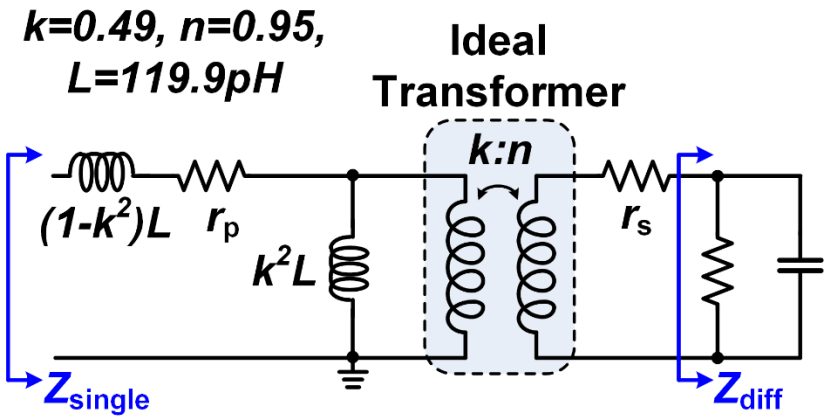

Figure 17. Simplified on-chip balun model.

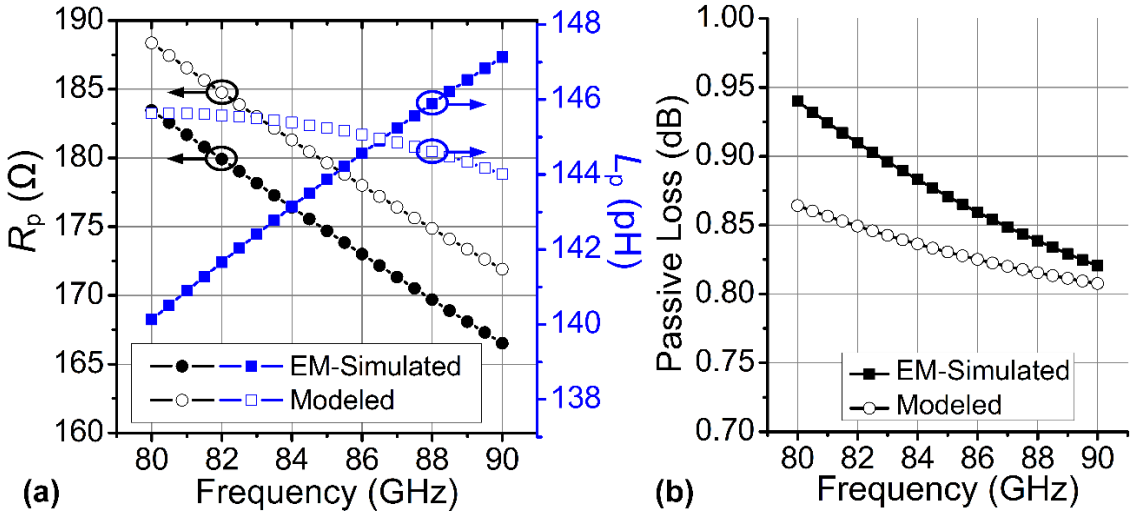

Figure 18. (a) EM-simulated and modeled parallel resistance (R_p) and inductance (L_p) of Z_{single}. (b) EM-simulated and modeled passive loss of the proposed offset balun.

The 3-Phase 42GHz Oscillator (Outermost Ring VCO)

The input stage of the system (the outermost ring), is a 3-phase 42GHz differential ring VCO (120°-mode) designed using the MOSFETs (Figure 19). Due to the long T-line routing (660µm), series capacitors are used to reduce the total capacitive loading at the drain nodes. The differential signals at each stage from the outermost ring are buffered and fed into the 1st stage frequency doubler (Figure 9). The doubler is also designed using MOSFETs and biased for optimum 2nd harmonic current generation with Vb_4 of 500mV.

At each stage of the 42GHz ring VCO, the tuning capacitor bank consists of 5-bit binary weighted digital controls (C_0 – C_4) for discrete tuning and 1 varactor for continuous tuning. The simulated tuning range of the VCO is plotted versus the bias voltage of the varactor (VCTRL) under different digital control settings in Figure 20a. A total frequency tuning range from 38.8GHz to 42.5GHz (9.1%) is achieved. The phase noise of the VCO is within -105dBc/Hz to -107dBc/Hz across the tuning range. Figure 20b shows a simulated phase noise plot for all the ILO stages when the system is locked to the outermost ring VCO. Since the frequency multiplication factor is 2 from the outermost ring to the middle ring and also 2 from the middle ring to the innermost ring, the phase noise is thus 6dB higher for the middle ring, and 12dB higher for the innermost ring compared with the outermost ring. The final THz output is the 3rd harmonic output of the innermost ring, which thus has 21.5dB (20×log12) phase noise degradation compared with the outermost ring VCO. At 1MHz frequency offset, the final output has a simulated phase noise of -85.1dBc/Hz, showing the expected phase noise degradation due to the cascaded frequency multiplication.

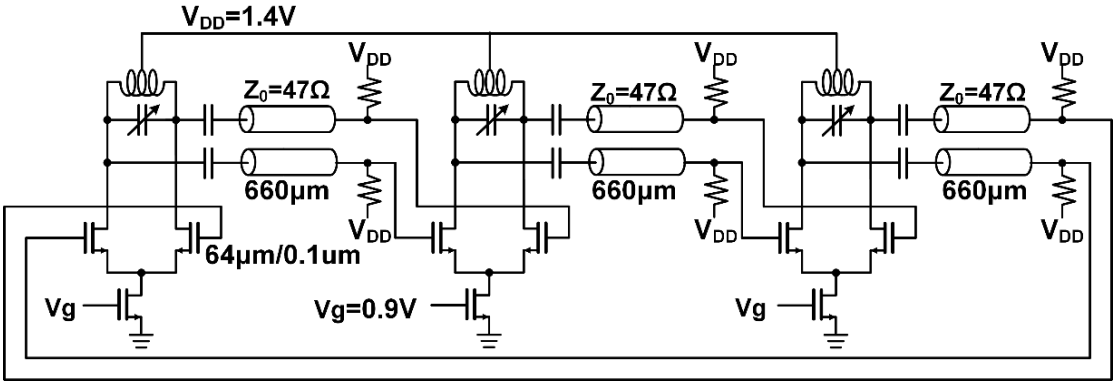

Figure 19. The schematic of the 3-phase 42GHz ring oscillator (outermost ring VCO).

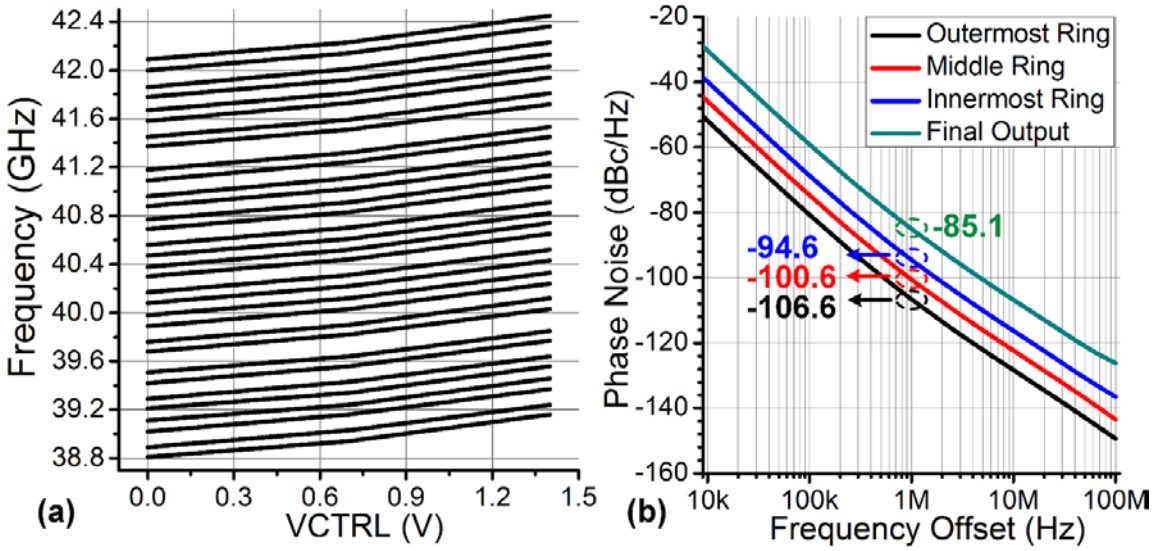

Figure 20. (a) The frequency tuning range of the outermost ring VCO. (b) Simulated phase noise of each ring oscillator and the final THz output when the system is locked to the outermost 42GHz ring VCO.

CHAPTER 4

EXPERIMENTAL RESULTS

The chip microphotograph and a photo of the measurement setup are shown in Figure 21. The DC pads and digital controls are directly wire-bonded to an open-top chip carrier mounted on an FR4 PCB. The core area of the chip is 720μm by 700μm. The 3-stage "active frequency multiplier" chain multiplies a 42GHz signal to generate the 504GHz output. The outermost ring VCO draws 122mA from 1.4V. The middle ring ILO draws 113-129mA from 1.6V, and the innermost ring ILO draws 24-32mA from 1.5V within the system frequency tuning range.

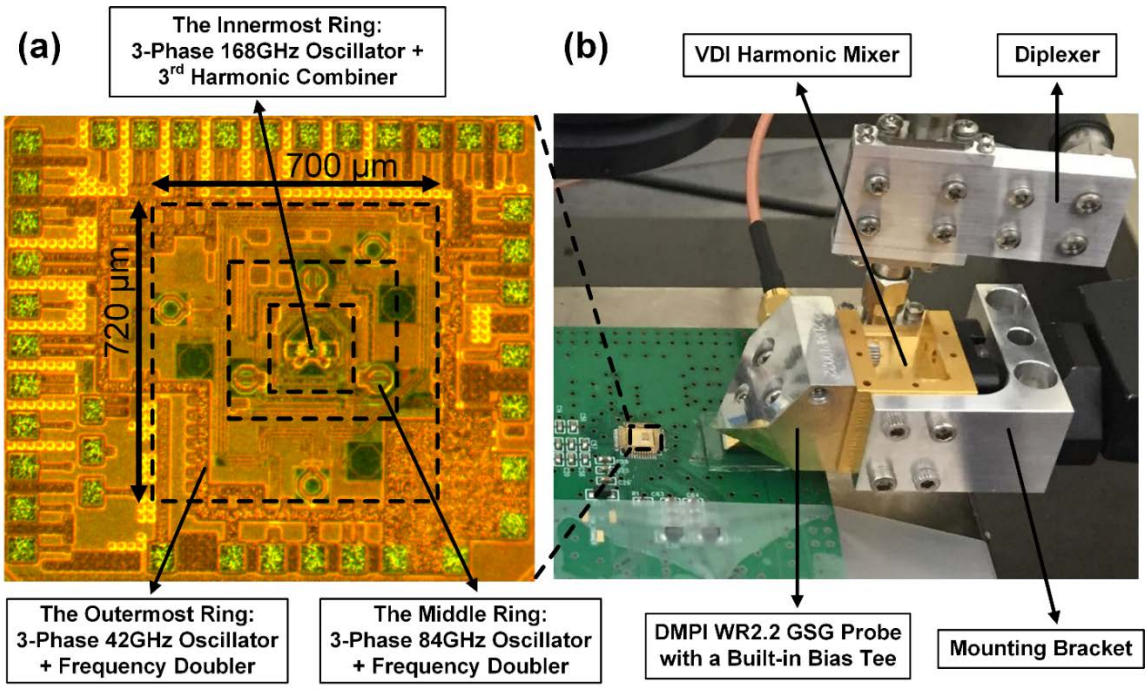

Figure 21. (a) Chip microphotograph. (b) Photograph of the spectrum measurement setup including the probe and the down-conversion harmonic mixer.

Since the output GSG pads are in the middle of the chip, the prototype is directly measured through wafer probing. In a practical application, the chip can be flip-chip packaged to connect to the antenna in package (AiP) [30], so that the signal can be radiated out. Alternatively, silicon-based micromachined waveguides [31], [32] can be used to

guide the THz signal from the chip. Figure 22 shows the simplified setups for the spectrum and the power measurements. The output 500GHz signal is probed by a DMPI WR2.2 GSG probe with a built-in bias tee [33]. First, the frequency measurement is performed by down-converting the 500GHz tone with a VDI WR2.2 EHM harmonic mixer. The harmonic mixer uses the 16^{th} harmonic of the LO signal which is provided from a Keysight signal generator. After the frequency down-conversion, the IF signal is amplified by an IF amplifier and captured with a spectrum analyzer. A typical IF spectrum is shown in Figure 23a with a clean spectrum when all the three oscillators are locked. The 500GHz signal tone is identified by sweeping the LO frequency and observing the corresponding change in the IF frequency. However, at the edge of the frequency locking range, 2 tones will arise at the output IF spectrum shown in Figure 23b, indicating an undesired quasi-locking behavior [35]. To demonstrate the total frequency tuning range, the measured output frequency is plotted in Figure 24 with the corresponding capacitor bank settings of the outermost ring VCO together with Vb_1 and Vb_2 (Figure 9). A frequency tuning from 485.1 to 510.7GHz is achieved (with a total 5.1% tuning range). This is the largest frequency tuning range among all the reported Si-based THz oscillator sources in the 500GHz band.

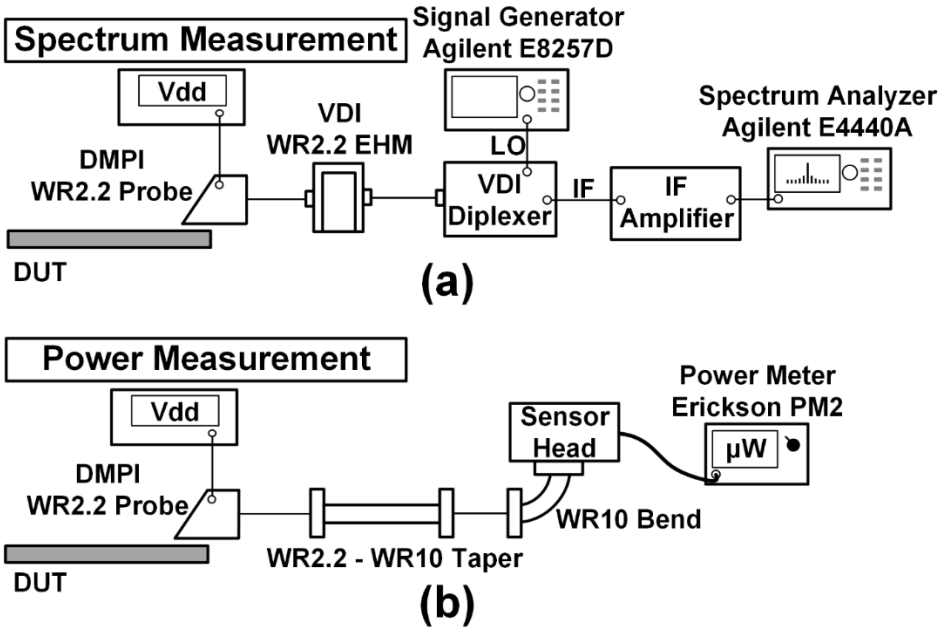

Figure 22. (a) Spectrum measurement setup. (b) Power measurement setup.

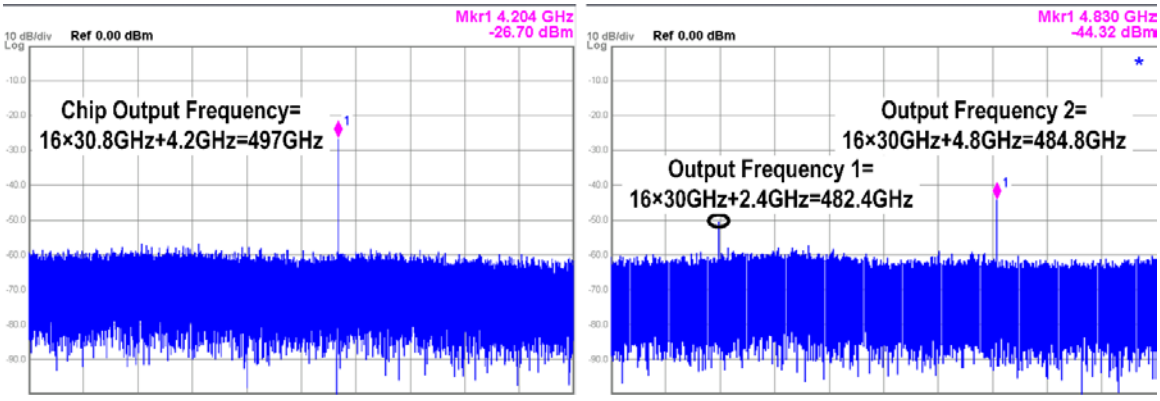

Figure 23. (a) A typical measured output spectrum (with IF amplifier) after down-conversion by the 16th harmonic of the LO (LO=30.8 GHz). (b) At the edge of locking range (LO=30GHz), it shows 2 tones on the spectrum analyzer, demonstrating an undesired quasi-locking behavior.

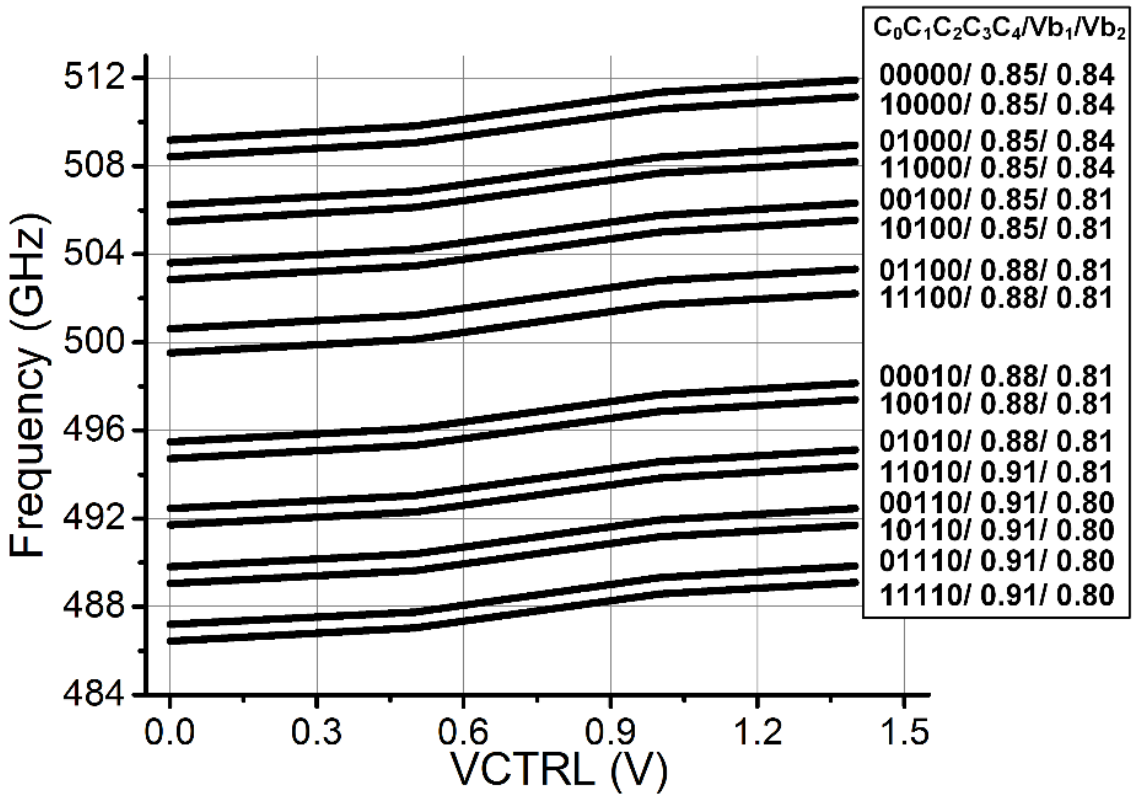

Figure 24. Measured output frequencies versus varactor's tuning voltage (VCTRL) under different digital control settings (C_0 – C_4) together with Vb_1, Vb_2 settings.

As mentioned previously, the frequency ranges of the three oscillators are designed to ensure their mutual locking. To verify the mutual locking of the three oscillators in the measurements, the following checking has been performed. First, from the output frequency perspective, the digital setting and the varactor's tuning voltage (VCTRL) of the outermost ring VCO are changed, and the corresponding frequency change of the final output is observed. However, if we only change the biasing voltages of the inner two ring ILOs (Vb_1 and Vb_2), the output frequency remains the same. This directly verifies that the 3 ring oscillators are locked together, and the final output frequency is determined only by the outermost ring VCO. Secondly, from the phase noise perspective, the phase noise of the final output is -87dBc/Hz at 1MHz offset at the output frequency of 501GHz (Figure 25a) when the 3 ring oscillators are mutually locked. The outermost ring VCO is then turned off and the phase noise is measured again. The output frequency shifts from 501GHz

to 497.8GHz and the phase noise degrades to -75.6dBc/Hz at 1MHz offset (Figure 25b), which is now limited by the innermost ring oscillator. Thirdly, the output phase noise is also measured and compared with the simulated phase noise of the outermost ring VCO (Figure 26) across the frequency tuning bandwidth. Theoretically, phase noise of the 504GHz tone should have a 21.5dB (20×log12) degradation compared with the 42GHz tone. The measured phase noise difference matches well with this theoretical prediction within a 5.1% locking range, indicating the proper injection locking of the 3-stage oscillators. Note that this 5.1% locking range is used to determine the system frequency turning range. On the other hand, the output phase noise degrades substantially when the oscillators are not locked, i.e., beyond the locking range.

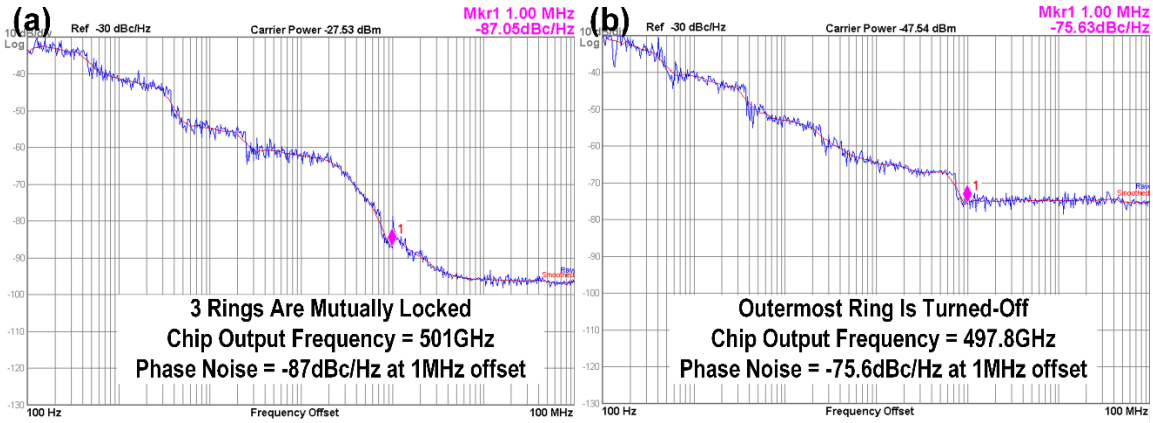

Figure 25. (a) Measured phase noise at chip output frequency of 501GHz when 3 rings are mutually locked. (b) Measured phase noise when the outermost ring is turned off. The final output frequency shifts from 501GHz to 497.8GHz, and its phase noise degrades to -75.6dBc/Hz at 1MHz offset.

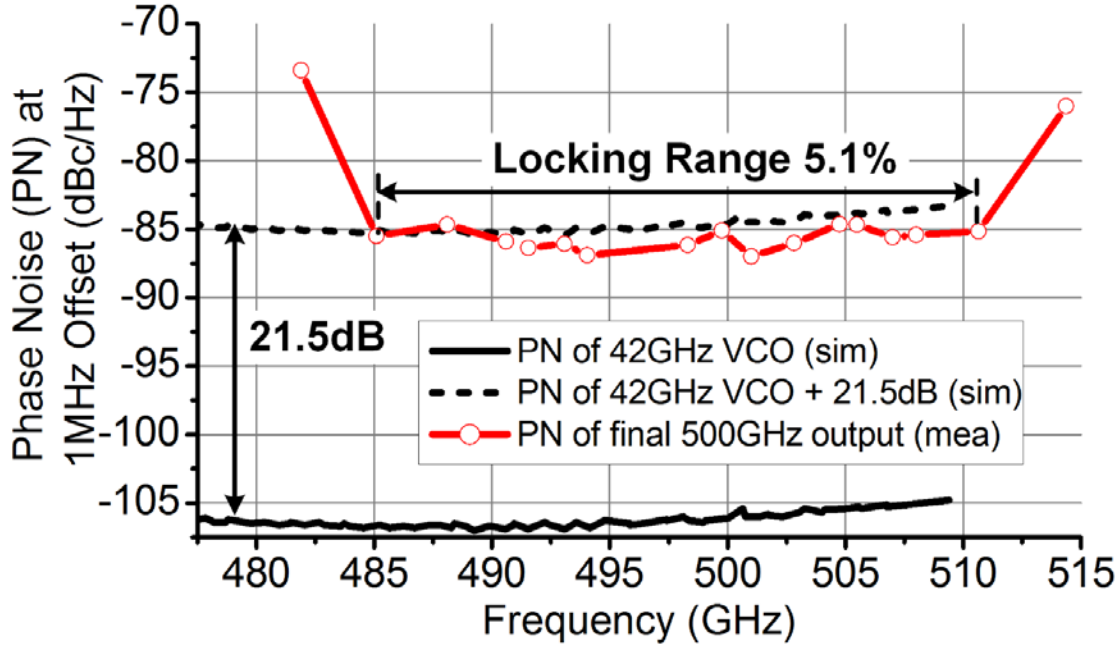

Figure 26. Simulated phase noise of the outermost ring (42GHz VCO), and measured phase noise of the final 500GHz output at 1MHz offset.

In the power measurement, the probed output signal is first filtered by a WR-2.2 waveguide. This suppresses any signal outside of 325-500GHz, e.g., the fundamental tone of the 168GHz oscillator. The signal is then detected by an Erickson PM2 power meter. The loss of the WR2.2 probe is 5dB at 500GHz [33], the loss of the taper is 0.6dB, and the loss of the waveguide bend is 0.4dB according to VDI application note [34]. The measured

output power versus frequency is shown in Figure 27, verifying the broadband performance at 500GHz. The peak output power drops 3.3dB compared with the simulation. The difference between the simulation and measurement may be due to the inaccuracy of transistor model at this frequency.

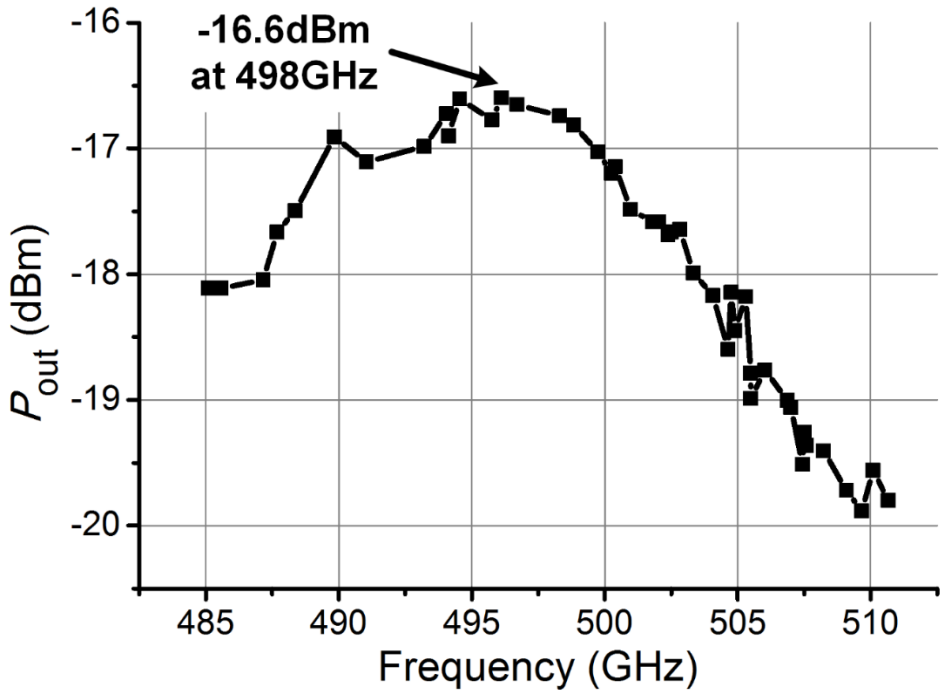

Figure 27. Measured output power versus frequency.

CHAPTER 5

CONCLUSIONS

This thesis presents a multi-phase injection locking (IL) technique and its application in the locking range extension in multi-phase ILOs for THz signal generation. Based on the multi-phsae IL technique and sub-harmonic ILOs, an "active frequency multiplier chain" architecture is proposed to achieve scalable THz signal generation. A cascaded 3-stage 3-phase 2nd-order sub-harmonic ILO chain is implemented in the IBM 9HP SiGe BiCMOS process to generate THz signal in the 500GHz band. A frequency tuning range of 5.1% and a phase noise of -87dBc/Hz at 1MHz offset are achieved, which are the largest frequency tuning range and the best phase noise among the reported silicon-based THz oscillator sources at 0.5THz. In addition, this design generates a maximum output power of -16.6dBm at 498GHz, and it achieves more than -20dBm across the entire system frequency tuning range. A performance comparison of silicon-based THz oscillator sources is summarized in Table I.

TABLE I COMPARISON OF STATE-OF-THE-ART SILICON-BASED THZ OSCILLATOR SOURCES

Reference	Center Frequency (GHz)	CW Tuning Range	P_{out} (dBm)	Phase Noise at 1MHz (dBc/Hz)	Technology
This work	**498**	**5.1%**	**-16.6**	**-87**	**90nm BiCMOS**
[11]	482	N/A	-7.9	-76	65nm CMOS
[12]	528	3.2%	-11.3†/0†,*	N/A	130nm BiCMOS
[13]	540	4.0%	-31/-33.1†	N/A	40nm CMOS
[14]	553	N/A	-36.5†	N/A	45nm CMOS
[15]	256	6.5%	4.1	-94	65nm CMOS
[16]	260	1.4%	0.5†	-78.3	65nm CMOS
[17]	280	3.2%	-7.2†,*	N/A	45nm SOI
[18]	288	1.4%	-1.5/-4.1†	-87	65nm CMOS
[19]	290	4.5%	-1.2	-78	65nm CMOS
[20]	290	7.9%	-14	-82.5	90nm BiCMOS
[21]	316	1.9%	-21	N/A	45nm SOI
[22]	317	5%	-13.3	-78	120nm BiCMOS
[19]	320	2.6%	-3.3	-77	65nm CMOS
[23]	338	2.1%	-0.9†	-93	65nm CMOS

† Radiated power from on-chip antennas. * P_{out} generated by 16-element array.

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