Correlation of Flip Chip Underfill Process Parameters and Material Properties with In-Process Stress Generation

Prema Palaniappan, Daniel F. Baldwin, Paul J. Selman, Jaili Wu, and C. P. Wong

***Abstract*— Electronic packaging designs are moving toward fewer levels of packaging to enable miniaturization and to increase performance of electronic products. One such package design is flip chip on board (FCOB). In this method, the chip is attached face down directly to a printed wiring board (PWB). Since the package is comprised of dissimilar materials, the mechanical integrity of the flip chip during assembly and operation becomes an issue due to the coefficient of thermal expansion (CTE) mismatch between the chip, PWB, and interconnect materials. To overcome this problem, a rigid encapsulant (underfill) is introduced between the chip and the substrate. This reduces the effective CTE mismatch and reduces the effective stresses experienced by the solder interconnects. The presence of the underfill significantly improves long term reliability. The underfill material, however, does introduce a high level of mechanical stress in the silicon die. The stress in the assembly is a function of the assembly process, the underfill material, and the underfill cure process. Therefore, selection and processing of underfill material is critical to achieving the desired performance and reliability. The effect of underfill material on the mechanical stress induced in a flip chip assembly during cure was presented in previous publications. This paper studies the effect of the cure parameters on a selected commercial underfill and correlates these properties with the stress induced in flip chip assemblies during processing.**

***Index Terms*— Direct chip attach, electronics manufacturing, electronics packaging, flip chip, microelectronics.**

I. Introduction

DEVELOPMENT of advanced electronic packages addresses the need for miniaturization, lower cost, and increased performance in emerging electronic products. Flip chip technology is a rapidly growing technique for achieving these needs via an area array interconnect. It also offers advantages of increased functionality, smaller circuit board footprint, smaller profiles, and superior electrical performance. Flip-chip on board (FCOB) processing involves interconnection of unpackaged integrated circuits directly to low cost organic substrates. A typical interconnection technique utilizes devices having solder bumps on the chip input/output (I/O) bond pads. The bumped devices are aligned to the substrate traces and attached using eutectic solder. Due to the thermal expansion coefficient mismatch between the organic substrate and the silicon device (which can differ by an order of magnitude), flip chip on board assemblies are encapsulated with filled epoxy resins called underfills. The rigid encapsulants mechanically couple the device and substrate reducing the effective stresses experienced by the solder interconnects and significantly improving long term reliability.

Since the physical properties of epoxies are highly dependent on the cure parameters, this study explores the fundamental effects of assembly process history on stresses generated in low cost flip chip assemblies. The long term goal being to link residual stresses to reliability performance. The objectives of this work are:

1) to characterize the material properties of underfills processed under varying assembly conditions;
2) to perform in situ stress measurements on flip chip test vehicle assemblies processed under the same conditions;
3) to characterize the stress distribution and maximum stress at the die/underfill interface;
4) to correlate material properties with the residual stresses as a function of assembly process parameters.

The encapsulation process induces thermomechanical stress in the assembly. Shrinkage of the underfill during cure and the CTE mismatch during cooling, results in relatively large stresses on the active surface of the die. In some instances, the stresses generated can be sufficiently large to cause die fracture. The stress tensor components σ_{xx} and σ_{yy} within the plane of the die depend strongly on the underfill material and cure schedule. In previous work, the effect of underfill material type on process induced stresses based on in situ measurements in flip chip test vehicle assemblies was presented [1], [2].

In order to quantitatively determine the relative stress magnitudes in flip chip assemblies, it is desirable to have a test device that can simulate the actual integrated circuit (IC) as close as possible. To achieve this, piezoresistive stress sensing IC devices are used in place of functional IC devices. These devices have stress sensitive piezoresistors implanted into the die surface and have interconnect metallization identical to typical IC's [3]. In this work, the Sandia National Laboratories' assembly test chip ATC04 is used for in situ stress measurements during flip chip underfill processing. The ATC04 is designed for measurement of mechanical stress and thermal resistance. It is a second generation CMOS assembly test chip that dissipates no power, except when the cell address is changed or when the heaters are activated.

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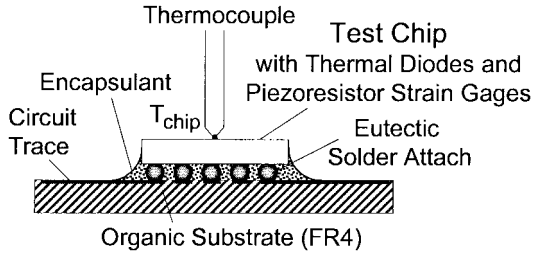


Fig. 1. Schematic of the test vehicle assemblies used for stress measurement during underfill processing.

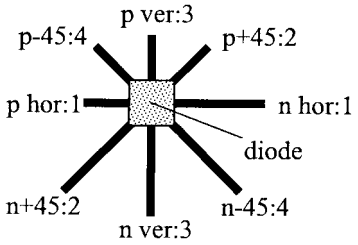


Fig. 2. Stress sensor rosette.

Piezoresistive stress sensors have been widely used for experimental stress analysis of electronic packages. The theory and application of piezoresistive sensors is discussed in detail by Sweet *et al.* [3], [4], Peterson *et al.* [5], Bittle *et al.* [6], Spencer *et al.* [7], Gee *et al.* [8], [9], and Nguyen *et al.* [10].

Described in this paper are the flip chip test vehicles used for stress measurements, a review of stress measurement theory using piezoresistors, the experimental methodology, the in situ stress measurement results during underfill processing of a commercial material under various assembly process parameters, and the correlation of residual stress generation with underfill glass transition temperature T_g, storage modulus G', and CTE.

II. Test Vehicle Description

The *in situ* stress measurement test vehicles are comprised of ATC04 test chips mounted on FR-4 substrates as shown schematically in Fig. 1. The device size is approximately 5.75 mm square with 35 redistributed solder bumped area array bondpads. Redistribution of the I/O is achieved using a proprietary polyimide thin film redistribution technology based on Sandia's mini-ball grid array (mBGA) technology. The chip is approximately 575 μm thick and has a polyimide passivation over the active surface. The ATC04 test chip contains 25 addressable test cells for sensing temperature and stress over the active surface of the die. Each cell contains two stress rosettes, one with four n-type piezoresistors, and the second with four p-type piezoresistors as shown in Fig. 2. The cells also contain a diode centered within the stress rosettes for measurement of relative temperature changes. The ATC04 is also equipped with four polysilicon resistive heaters for thermal resistance measurements, and two ring oscillators used for monitoring die functionality in accelerated life testing. A schematic of the ATC04 die layout is shown in Fig. 3 without the redistribution layer.

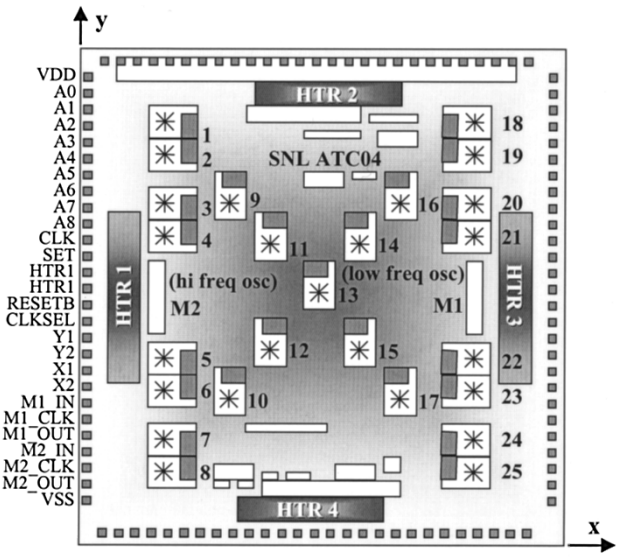


Fig. 3. Layout of the atc04 chip, with the 25 piezoresistive stress cells.

The test substrates are 50.8 $\times$ 50.8 mm double sided FR-4 PWB's, 625 μm thick, metallized with 17.8 μm copper, 2.54 μm nickel, and 0.2 μm gold.

III. Piezoresistive Stress Derivation from Test Data

Sweet *et al.* [3], [4] presents the derivation of the stress tensor for the ATC04 test chip piezoresistance data. The four n-type and four p-type resistors in each test cell are oriented at 0°, 45°, 90° and $-45°$ with respect to the (110) plane of the silicon. Each set of n-type and p-type piezoresistors within a rosette are numbered 1, 2, 3, and 4, respectively, as shown in Fig. 2 [3].

In principle, the ATC04 test chip can measure the σ_{xx}, σ_{yy}, σ_{zz} stress tensor components and the in-plane σ_{xy} shearing stress component relative to the coordinate system of Fig. 3. Equations (1) though (4) show the change in resistance ΔR_i of the ith piezoresistor as a function of the stress tensor components under isothermal conditions ($\Delta T = 0$) [3]–[5], [11]. The resistance change is relative to a baseline stress measurement at a temperature of T_0

$$\frac{\Delta R_{1n,p}}{R_{10n,p}} = \left(\frac{\pi_{11}^{n,p} + \pi_{12}^{n,p} + \pi_{44}^{n,p}}{2}\right)\sigma_{xx} + \left(\frac{\pi_{11}^{n,p} + \pi_{12}^{n,p} - \pi_{44}^{n,p}}{2}\right)\sigma_{yy} + \pi_{12}^{n,p}\sigma_{zz} \quad (1)$$

$$\frac{\Delta R_{2n,p}}{R_{20n,p}} = \left(\frac{\pi_{11}^{n,p} + \pi_{12}^{n,p}}{2}\right)\sigma_{xx} + \left(\frac{\pi_{11}^{n,p} + \pi_{12}^{n,p}}{2}\right)\sigma_{yy} + \pi_{12}^{n,p}\sigma_{zz} + \left(\pi_{11}^{n,p} - \pi_{12}^{n,p}\right)\sigma_{xy} \quad (2)$$

$$\frac{\Delta R_{3n,p}}{R_{30n,p}} = \left(\frac{\pi_{11}^{n,p} + \pi_{12}^{n,p} - \pi_{44}^{n,p}}{2}\right)\sigma_{xx} + \left(\frac{\pi_{11}^{n,p} + \pi_{12}^{n,p} + \pi_{44}^{n,p}}{2}\right)\sigma_{yy} + \pi_{12}^{n,p}\sigma_{zz} \quad (3)$$

$$\frac{\Delta R_{4n,p}}{R_{40n,p}} = \left(\frac{\pi_{11}^{n,p} + \pi_{12}^{n,p}}{2}\right)\sigma_{xx} + \left(\frac{\pi_{11}^{n,p} + \pi_{12}^{n,p}}{2}\right)\sigma_{yy} + \pi_{12}^{n,p}\sigma_{zz} - \left(\pi_{11}^{n,p} - \pi_{12}^{n,p}\right)\sigma_{xy} \quad (4)$$

where

$\Delta R_{1n,p}$ change in resistance of the ith n or p type resistor after stress application;

$\Delta R_{i0n,p}$ initial resistance before stress application or at a baseline stress state at T_0;

π_{ij} "pi" coefficient which is the fundamental coupling constant relating the stress field to the Si resistively;

superscript/subscript n and p refer to the n-type and p-type stress sensor rosettes, respectively, [3]–[5], and [11].

If there is a temperature change ΔT, the resistance change due to the temperature difference is subtracted from the measured ΔR. The stress data depends on the sum S and the difference D between the ith and jth resistors oriented at 90° as given by [4], [5], [11]

$$\delta R_{ijn,p}^{S,D} = \left[\frac{\Delta R_i}{R_{i0}} \pm \frac{\Delta R_j}{R_{j0}}\right]_{n,p}. \tag{5}$$

The superscript S corresponds to the $(+)$ and D to the $(-)$ of (5). The quantity ΔR_{ij} refers to a relative stress difference where i and j are given by 1 and 3 oriented at 0° and 90° or 2 and 4 oriented at 45° and $-45°$, respectively. Two temperature invariant stress tensor quantities derived from δR^D are given by [4], [5], [11]

$$\sigma_{xy} = \frac{\delta R_{24n}^D}{2\pi_D^n} \tag{6}$$

$$\sigma_{xx} - \sigma_{yy} = \frac{\delta R_{13p}^D}{\pi_{44}^p} \tag{7}$$

where $\pi_D^n = \pi_{11}^n - \pi_{12}^n$ [4], [5]. Due to the calibration accuracy of the π coefficients, the n-type resistors are used to determine σ_{xy} and the p-type resistors for $\sigma_{xx} - \sigma_{yy}$ [4], [5], [11]. Equations (1) and (3) or (2) and (4) are summed to give the result

$$\delta R_{13n}^S = \delta R_{24n}^S = \pi_S^n(\sigma_{xx} + \sigma_{yy}) + 2\pi_{12}^n \sigma_{zz} \tag{8}$$

where $\pi_S^n = \pi_{11}^n + \pi_{12}^n$ [4], [5]. Solving for σ_{yy} from (7) and substituting into (8) yields (9), [5], [11]

$$\sigma_{xx} + \frac{\pi_{12}^n}{\pi_S^n}\sigma_{zz} = \frac{\left(\delta R_{24n}^S - 2\alpha_n \Delta T\right)}{2\pi_S^n} + \frac{\delta R_{13p}^D}{2\pi_{44}^p}. \tag{9}$$

Substituting this equation into (7) generates σ_{yy} [5], [11]

$$\sigma_{yy} + \frac{\pi_{12}^n}{\pi_S^n}\sigma_{zz} = \frac{\left(\delta R_{24n}^S - 2\alpha_n \Delta T\right)}{2\pi_S^n} - \frac{\delta R_{13p}^D}{2\pi_{44}^p} \tag{10}$$

It has been shown that $\pi_{12}^n/\pi_S^n \approx -1$ [4], [5], [11] resulting in simplification of (9) and (10) to a stress difference. In the case of flip chip attachment to a substrate, the magnitude of σ_{zz} is very small relative to σ_{xx} and σ_{yy} at all sensor locations. This has been shown both theoretically and through finite element simulations [11]. Therefore, the left side of (9) and (10) becomes σ_{xx} and σ_{yy}, respectively yielding

$$\sigma_{xx} = \frac{\left(\delta R_{24n}^S - 2\alpha_n \Delta T\right)}{2\pi_S^n} + \frac{\delta R_{13p}^D}{2\pi_{44}^p} \tag{11}$$

$$\sigma_{yy} = \frac{\left(\delta R_{24n}^S - 2\alpha_n \Delta T\right)}{2\pi_S^n} - \frac{\delta R_{13p}^D}{2\pi_{44}^p}. \tag{12}$$

Equations (11) and (12) are equivalent to (9) and (10) in [2] and the original version of this paper presented at the 48th Electronics and Components Technology Conference, 1998, but the equations in the prior publications have an error in the last term on the right where a factor of 2 in the denominator was omitted. The spreadsheet analysis stress measurement data reported in all cases is based on the correct equation set and has been verified.

The π and α coefficients are given by Peterson *et al.* [5], [11]. The π_S^n, π_D^n, and π_{44}^p coefficients are generally accepted as temperature independent and have been well characterized showing relatively constant values from die to die and wafer to wafer. The α coefficients on the other hand are not as well characterized exhibiting variability from die to die and wafer to wafer.

IV. Experimental Methodology

An automated data acquisition system is used to monitor the in situ stresses in the flip chip assembly test vehicles. The automated testing system is based on a National Instruments Labview control architecture implementing a four-point measurement technique for resistance and diode voltage measurements on the ATC04 as shown in Fig. 4. Analysis of the stress and temperature data is accomplished using a spreadsheet template specially developed for analysis of the ATC04 data based on a commercial software package.

Stress data is collected post solder attach and during underfill processing. The raw data, consisting of four point resistance measurements, is then used to calculate the relative stresses on the die surface based on (6), (7), (9), and (10).

Test vehicle assembly involves using a typical flip chip on board assembly process. A 100 μm thick stainless steel stencil is used to print a Heraceus type 4, low solids, eutectic solder paste (-400 mesh) onto the PWB test coupon. Solder paste is printed using an MPM Corporation SPM Semiautomatic Screen Printer. Due to the relatively poor solder volume control in the thin film redistribution and bumping process used for the mBGA's, it is necessary to planarize the ATC04 test chip eutectic solder bumps prior to flip chip assembly. The bumps are planarized by placing a chip face down on a glass panel and applying flux to the perimeter of the die. The die is then reflowed in a Nitrogen convection reflow oven using a standard eutectic reflow profile. This allows for a uniform flattening of the solder bumps forming a planar surface. Prior to board assembly, the chips are ultrasonically cleaned to remove flux residues.

A Kulicke and Soffa Flip Chip Assembly System Model 6900 is used to align and place the die on the substrate. The bonding parameters include 200 g of load, 300 ms of applied bond load, and a stage temperature of 30 °C. Once tacked, the assembly is reflowed in a BTU International Paragon 98N nitrogen atmosphere reflow furnace. The oven forces recirculate hot nitrogen gas to create and maintain solder reflow temperatures within an inert atmosphere up to 325 °C. The Paragon 98N has a 98-in heated length containing seven top and bottom heating zones and closed loop feedback control of the plenum pressure and convection flow rate.

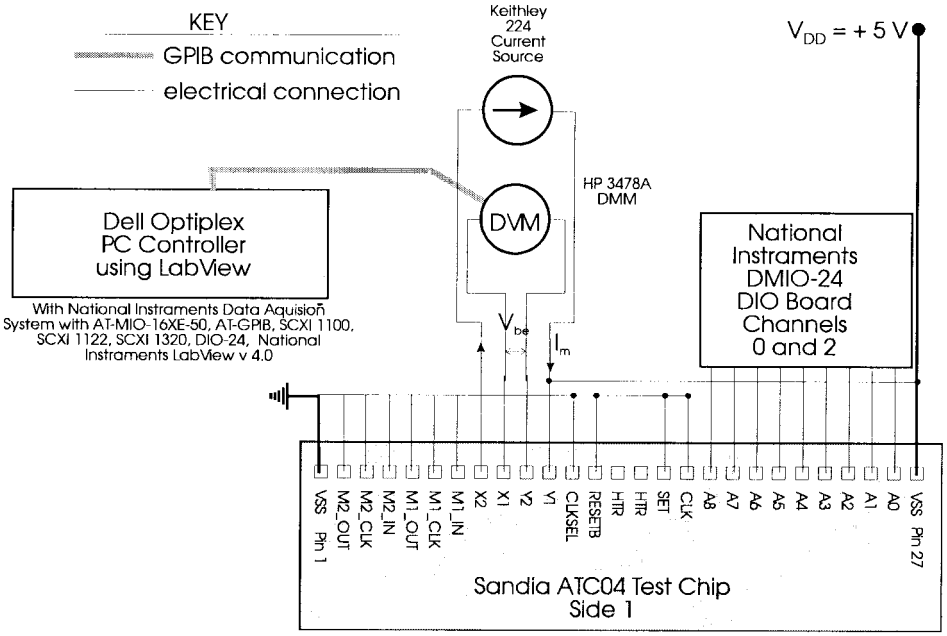


Fig. 4. Automated testing system for atc04 test chip.

The resulting controlled collapse interconnection yields robust self-aligned assemblies. Post reflow, the test vehicle is cleaned and baked out at 100 °C for 2 h. The cleaning operation consists of an ultrasonic scrub of the test vehicles in a proprietary solvent system. The bake out is required to evacuate the board of solvents and moisture which can lead to voiding during underfill cure. The assembly is then mounted in the test fixture and baseline stress measurements are taken at room temperature, 80 °C, and 120 °C. Next, the test vehicle is removed from the test fixture and underfilled. Underfill is applied using a CAM/ALOT 1818 Liquid Dispensing System with a 22 gauge dispense tip and a substrate temperature of 80 °C. Underfill is applied along the top edge of the die, and is allowed to flow between the chip and the substrate via capillary action. Once the underside of the chip is filled, fillets are dispensed along the perimeter of the die. Post reflow, the standoff gap height between the chip active surface and FR-4 substrate surface is 125 μm. The soldermask height for the FR-4 substrates varies between 20 and 30 μm over the ATC04 chip area.

The test vehicle is now mounted in the test fixture to enable in situ stress measurement during underfill cure processing. Curing is accomplished using a Despatch Industries convection oven. The underfill cure schedule is based on differential scanning calorimetry (DSC) analysis of the underfill material at select isothermal temperatures. The Labview data acquisition system determines when the steady state temperature of the test vehicle is reached and begins the specified cure time count down based on DSC analysis. Stress data is collected every 30 s during cure. Post cure, the test fixture with the test vehicle is removed from the oven and cooled. Stress measurements are conducted during a three hour cool cycle to room temperature.

Finally, the assembly is inspected using acoustic microscopy. A Sonoscan model D6000 C-SAM is used to inspect the assemblies for underfill void formation and delamination flaws within the interconnect layer. C-SAM images are used to correlate process defects and failures with the residual stress patterns measured on the flip chip test vehicles.

TABLE I
CRITICAL PROPERTIES OF SELECTED UNDERFILL CURED AT DIFFERENT CURE PARAMETERS

Cure Temp./Time (°C/min)	T_g (°C)	CTE (ppm/°C)	Storage Modulus G' (GPa)
135/80	138.37	22.6	5.74
145/40	137.39	21.7	5.841
165/60	139.83	20.5	6.868
180/15	135.35	18.9	4.937

Underfill samples prepared in a 1.5 in diameter aluminum pan and cured in situ during the test vehicle assembly process are analyzed to determine the glass transition temperature, T_g, the coefficient of thermal expansion CTE, and storage modules G'. The dynamic moduli of the samples are determined by dynamic mechanical analysis (DMA) using a TA Instrument, Model 2980. The samples are cut into strips and measured in a single cantilever mode under 1 Hz sinusoidal strain loading. The samples are heated from room temperature to 220 °C at a rate of 3 °C/min. The CTE of the samples is determined using thermal mechanical analysis (TMA) (TA Instrument, Model 2940). The specimen preparation is similar to the DMA testing except that the samples are cut into smaller sizes. The samples are heated from room temperature to 200 °C at a rate of 5 °C/min. The properties of the selected underfill cured at different conditions are listed in Table I. The storage modulus of the test vehicle printed wiring board is determined using the DMA, and the results are shown in Table II.

Some typical residual stress patterns in the x direction at room temperature post cure (28 °C) are shown in Figs. 5–8 for

TABLE II
STORAGE MODULUS OF THE FR-4 TEST VEHICLE PRINTED CIRCUIT BOARD

Direction	Storage Modulus G' (GPa)
X	1.172
Y	0.974

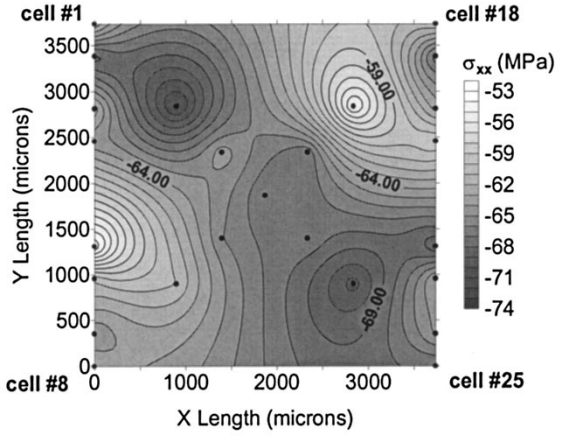


Fig. 5. Compressive stress distribution of σ_{xx} for cure temperature of 135 °C for 80 min.

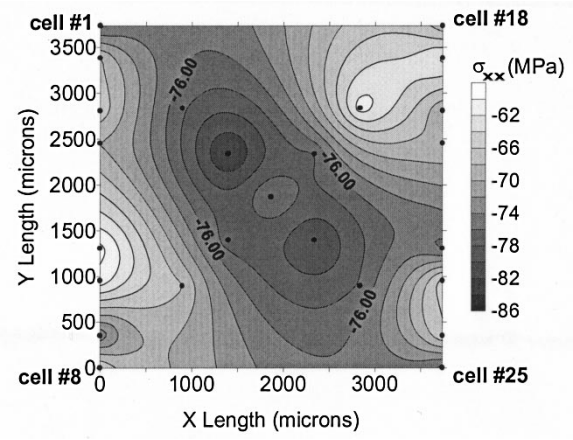


Fig. 6. Compressive stress distribution of σ_{xx} of cure temperature of 145 °C for 40 min.

the selected underfill. These stress maps are made using Surfer Version 6 software, which interpolates the stresses between the measurement cells shown in Fig. 3. Gridding for the contour and surface plots is based on interpolation techniques using the Kriging method and a linear variogram (12). The black circles on the stress maps denote the location of the stress sensing cells. It should be noted that the chip edge extends 1010 μm past the edge of Figs. 5–8 on each of the four sides.

V. RESULTS

Stress measurement data at the die/underfill interface was collected after solder joint attach, after underfill dispensing, during curing, and during the cool down process. In all test vehicles, a select commercial underfill was used, and four to seven test vehicles were manufactured under each set of conditions reported. Data presented reflects an average of test

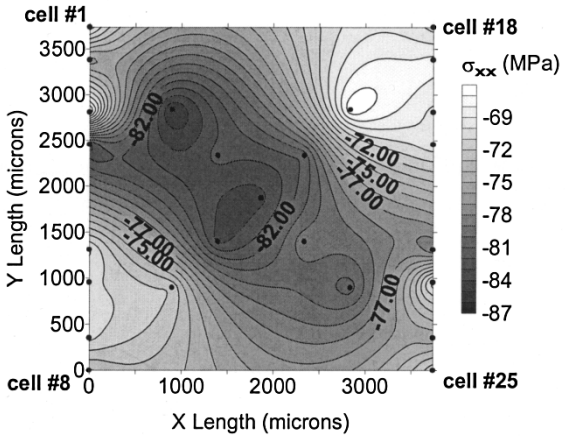


Fig. 7. Compressive stress distribution of σ_{xx} for cure temperature of 165 °C for 60 min.

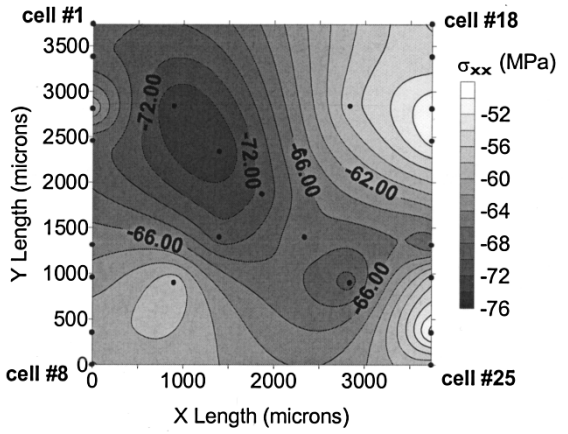


Fig. 8. Compressive stress distribution of σ_{xx} for cure temperature of 180 °C for 15 min.

vehicles produced under the same conditions. The experiments exhibit reasonable consistency from run to run especially at low temperature. All test vehicles processed under the same conditions exhibited similar residual stress distributions. In general, large compressive stresses were generated on the active die surface during cure and cool down indicating a complex state of convex chip bending relative to the active die surface. The compressive stress distribution seen by the chip surface in the x direction is shown in Figs. 5–8. On these figures, the solid points indicate the locations of the 25 test cells on the ATC04 where stress measurements are taken. The data are reported post cure at 28 °C. The maximum stress tends to be toward the center of the die. These plots show the variation in the stress distribution, minimum stress and maximum stress over the cure parameters studied.

Fig. 9 plots the compressive stress difference of a sample cured at 165 °C. The minimum value is near the center of the die. This pattern is consistent throughout all the samples subjected to different cure conditions. The results for σ_{xx}, σ_{yy}, σ_{xx}-σ_{yy}, and σ_{xy} at a constant temperature of 28 °C post underfill cure are shown in Figs. 10–13. The test vehicles with the underfill encapsulant cured at 180 °C for 15 min exhibit the lowest average σ_{xx} magnitude stress at −63 MPa, while the test vehicles cured at 165 °C for 60 min have the highest

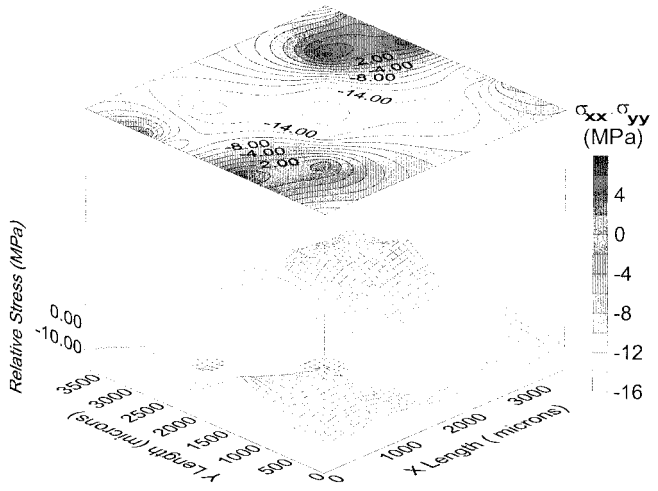


Fig. 9. In plane compressive stress difference σ_{xx}-σ_{yy} for underfill cured at 165 °C for 60 min.

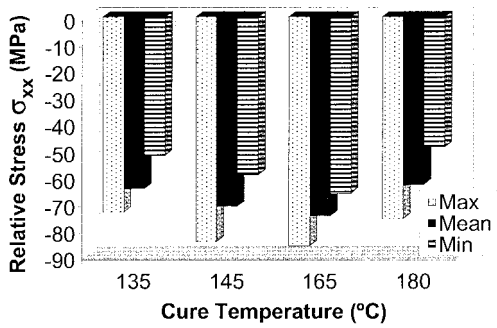


Fig. 10. Comparison of σ_{xx} for the four different cure parameters.

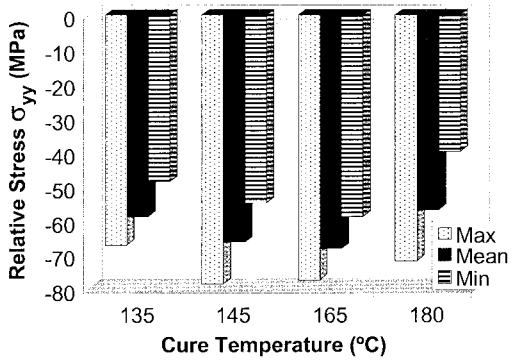


Fig. 11. Comparison of σ_{yy} for the four different cure parameters.

σ_{xx} magnitude at -74 MPa, an 18% increase. The average σ_{yy} stress for the test vehicles cured at 180 °C for 15 min was the lowest at -57 MPa, while those cured at 165 °C for 60 min have the highest σ_{yy} at -68 MPa, an 18% increase.

The average temperature invariant parameter σ_{xx}-σ_{yy} ranges from -5.5 MPa to -6.4 MPa over the cure temperatures studied. The average shear stress, σ_{xy}, over the die surface is very small and ranges from -0.90 to 0.11 MPa over the cure conditions studied. Since the average shear stress is small relative to the absolute accuracy of the stress measurement system, the global average shear stress is neglected in the calculation of the average Von Mises stress over the entire chip. However, as there is a variation in the

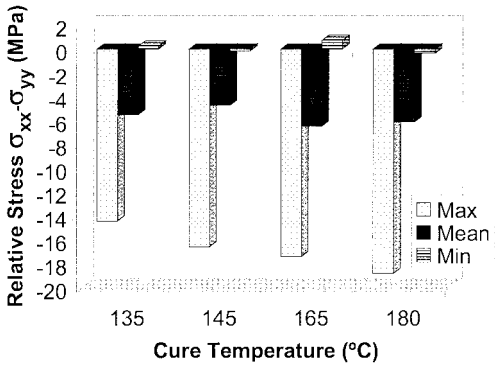


Fig. 12. Comparison of σ_{xx}-σ_{yy} for the four different cure parameters.

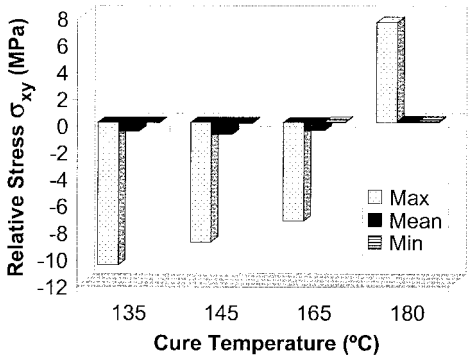


Fig. 13. Comparison of σ_{xy} for the four different cure parameters.

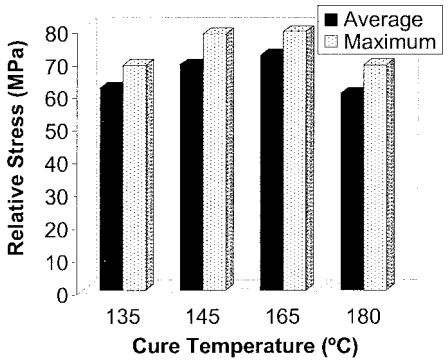


Fig. 14. Von Mises stress for the four different cure parameters.

local shear stress at each stress sensor cell, the local shear stress is accounted for in calculating the local Von Mises stress at each stress sensor cell. The values for σ_{xx}, σ_{yy}, and σ_{xy} are used to determine the maximum Von Mises stress given in Fig. 14. An assumption made in the calculation of the Von Mises stresses is that the out of plane shear stresses σ_{xz} and σ_{yz} are negligible. The assumption is based on the fact that the stress sensing cells are located well within the outer edges of the die. The die edges are regions where the out of plane shear stresses are large. This has been verified using Suhir's tri-layer composite model which predicts out of plane shear stresses ranging from 0.07 to 2.5 MPa over the regions where the stress sensing cells are located on the ATC04.

The average Von Mises stress and the maximum effective stress seen by the active die surface are plotted in Fig. 14. The cure parameter of 180 °C for 15 min exhibits the lowest average effective stress at 60 MPa, followed by the cure

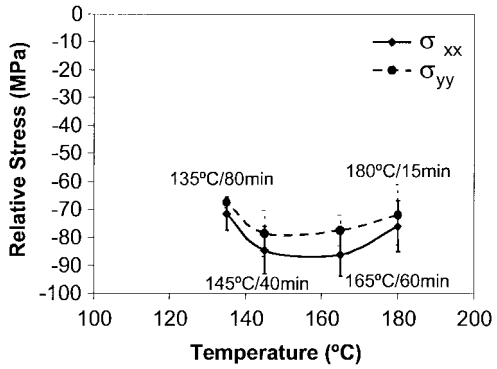


Fig. 15. Maximum stress at four different cure parameters.

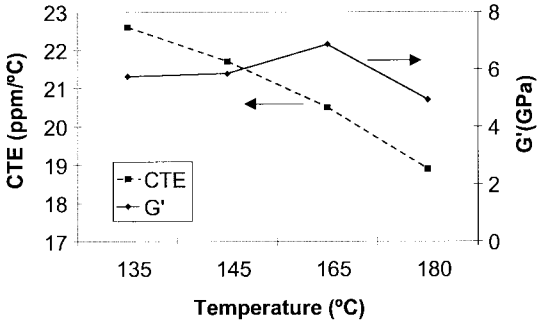
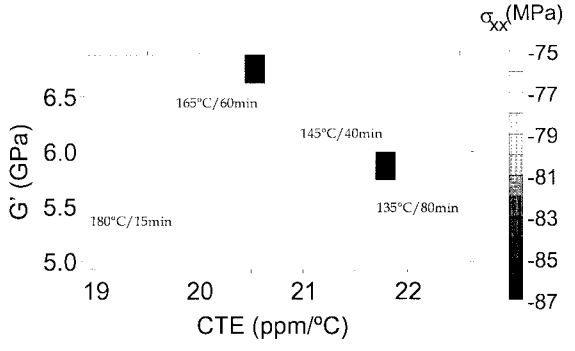


Fig. 16. Correlation between the cure temperature and the encapsulant CTE and storage modulus.

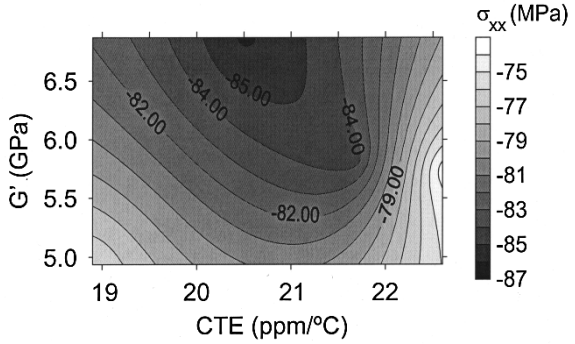
parameter of 135 °C for 80 min at 61 MPa, then 145 °C for 40 min at 69 MPa, and finally 165 °C for 60 min at 72 MPa. On average, the higher cure temperature of 180 °C for 15 min exhibited a 20% lower effective average stress. The local maximum Von Mises stress is also calculated for each stress sensor cell at the different cure temperatures and is shown in Fig. 14. The temperature of 180 °C for 15 min exhibits a 13% lower effective stress than the maximum of 79 MPa occurring at cure temperature of 165 °C for 60 min.

A comparison of the maximum residual σ_{xx} and σ_{yy} stress post cure at 28 °C is shown in Fig. 15 as a function of cure parameters. It is interesting to note that the maximum relative σ_{xx} and σ_{yy} stresses are significantly lower at the 180 °C cure temperature, representing a 12% reduction compared to the maximum at 165 °C. Fig. 15 also plots, as error bars, the standard deviation of the maximum relative σ_{xx} and σ_{yy} stresses. In each case, four to seven test vehicle assemblies were built and measured under the same cure parameters. The σ_{xx} standard deviation measurements ranges from 6 to 9 MPa. The σ_{yy} standard deviation ranges from 2 to 10 MPa.

In Fig. 17, the experimentally measured underfill encapsulant properties including the coefficient of thermal expansion and the storage modulus are correlated with the underfill cure parameters and with the resulting maximum die stress. Fig. 17(a) correlates the four maximum relative σ_{xx} stresses with the respective underfill CTE and the storage modulus. Fig. 17(b) expresses this correlation as a contour plot. Note that the underfill properties are measured on samples cured simultaneously with test vehicle assembly to ensure that the materials experience the same thermal history as the test vehicles used to measure stress.



(a)



(b)

Fig. 17. (a) Correlation between the maximum relative σ_{xx} stress and encapsulant CTE and G' properties. (b) Correlation between the maximum relative σ_{xx} stress and encapsulant CTE and G' properties plotted as contour map.

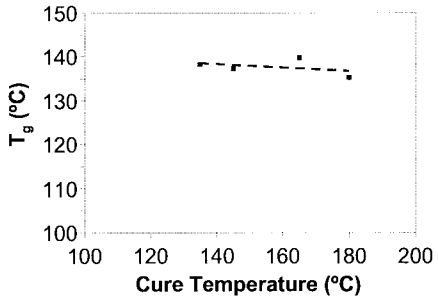
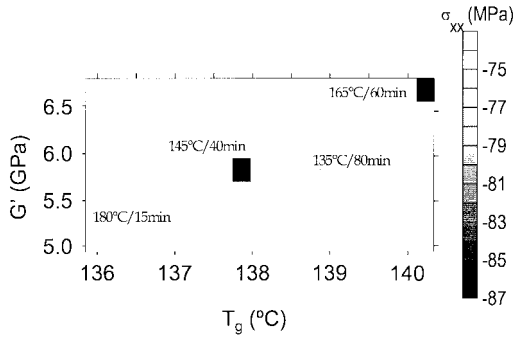


Fig. 18. Correlation between cure temperature and underfill T_g at various cure parameters.

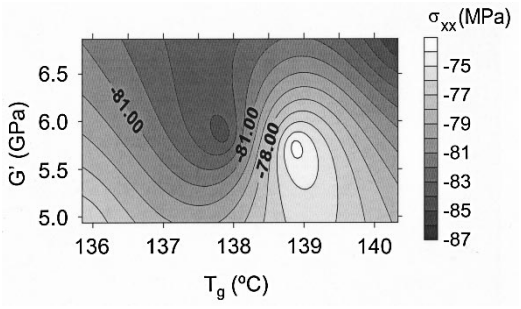
Fig. 18 plots the experimentally measured T_g with varying cure temperature. Notice that the T_g of the underfill post cure is nearly constant at approximately 137 °C. This tends to suggest that the underfill samples were fully cured or converted during processing. Fig. 19(a) and (b) show the variation in the relative residual stress as a function of T_g and G'. Fig. 19(a) exhibits the locations of the maximum relative σ_{xx} stresses as a function of T_g and G' while Fig. 19(b) displays the correlation as a contour map. Fig. 20(a) and (b) correlate the residual stress as a function of T_g and CTE.

VI. Discussion

The results in Figs. 5–20 correlate the residual stresses produced by a commercial underfill in flip chip on board assemblies for various underfill cure parameters. It should be noted that in all cases, the stresses reported are relative

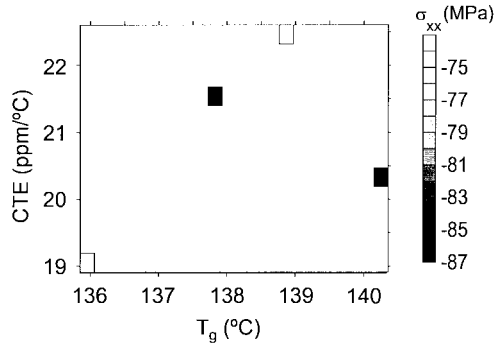


(a)

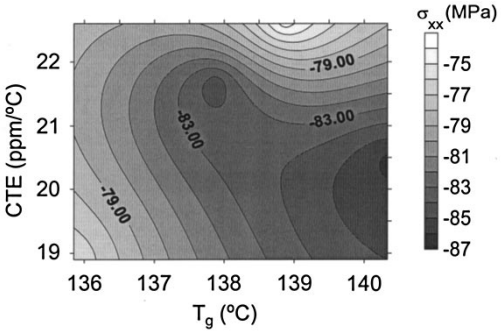


(b)

Fig. 19. (a) Correlation between the maximum relative σ_{xx} stress and encapsulant T_g and G' properties. (b) Correlation between the maximum relative σ_{xx} stress and encapsulant T_g and G' properties plotted as contour map.



(a)



(b)

Fig. 20. (a) Correlation between the maximum relative σ_{xx} stress and encapsulant T_g and CTE properties. (b) Correlation between the maximum relative σ_{xx} stress and encapsulant T_g and CTE properties plotted as contour map.

with respect to the post reflow stress state prior to underfill application. This is the reference or "zero" stress state for the stress measurements presented in Figs. 5 through 20.

Stress maps over the active die surface indicate a complex convex bending of the die reaching maximum negative values toward the die center. Though the average σ_{xx} and σ_{yy} values decrease by the same percentage, the resulting stresses are not symmetric in the x and y directions as would be predicted by simulations. This result is shown in Fig. 15. Also notice that the results for σ_{xx}-σ_{yy} are asymmetric indicating an anisotropy in the test vehicle assemblies. The most probable explanation for this anisotropy in the σ_{xx} and σ_{yy} stress values is due to the anisotropy in modulus of the PWB used for the test vehicles. Table II presents the storage modulus of the PWB showing the x direction modulus to be almost 200 MPa larger than the y direction. The higher modulus in the x direction correlates with the higher σ_{xx} values helping to explain the anisotropy in the stresses measured. Additional factors influencing the anisotropy in the results include the fact that the ATC04 test chip has a single missing solder bump toward the center of the chip negating symmetry conditions and inherent process defects within the flip chip assemblies. In many cases, the flip chip test vehicles had voids in the underfill ranging in size from small (10% of a solder ball) to very large (40% of the die area). In other cases, solder ball migration occurred and was verified by x-ray analysis. The solder interconnect volume varied considerably from bond site to bond site due to solder print variations and solder plating irregularities during bumping.

Underfill material cured at 180 °C for 15 min exhibits the lowest average relative compressive stress and lowest Von Mises or effective stress, approximately 20% lower than the maximum effective stress for test vehicles cured at 165 °C for 60 min. This is illustrated in Figs. 14 and 15. Of particular importance is the maximum effective stress seen by the die. This value is critical in determining the likelihood of die cracking and predicting the maximum interfacial stresses between the chip and underfill which ultimately govern interfacial crack propagation and delamination. Delamination is a common failure mode in flip chip assemblies. In general, the fracture strength of silicon is strongly dependent on surface characteristics of the wafer, dicing history, diced edge surface finish, etc. Fracture strengths of semiconductor silicon have been reported as low as 40 MPa [13], depending on the geometrical defects and microstructure defects. In that the effective residual stresses measured in this work are on the same order of magnitude as those that can induce die fracture, the importance of underfill process history, underfill geometry, and underfill selection take on a new level of importance in flip chip manufacturing.

Fig. 15 shows the maximum residual relative stress in the x and y directions to be at a cure temperature of 165 °C, while the minimum residual relative stress is at a cure temperature of 180 °C. This is contrary to the expected phenomena of residual stress increasing with cure temperature. In that the thermal expansion of the system is larger at higher temperature, it would be expected that the high cure temperatures would generate greater residual stress upon cooling. Interestingly, there are two low stress states based on the cure schedules studied. The first is at 135 °C for 80 min which is the lowest

cure temperature studied and is expected based on thermal expansion effects. The second is at 180 °C for 15 min which is the highest cure temperature studied.

Fig. 16 shows the trends between the cure temperature, the CTE, and the storage modulus of the underfill. The CTE decreases with increasing cure temperature showing a 20% lower CTE at 180 °C than at 135 °C. The highest storage modulus is 6.8 GPa at a cure temperature of 165 °C for 60 min—about 28% higher than the lowest value of 4.9 GPa at 180 °C for 15 min. It is interesting to note that the decrease in CTE with the increase in cure temperature is somewhat counter intuitive. The lower underfill CTE helps to explain the lower stress at the 180 °C cure temperature in that the lower CTE would naturally correlate with a lower strain due to the mismatch and ultimately to lower stress. Fig. 18 shows the effect of underfill cure parameters on the T_g of the underfill. In general, the T_g appears to be relatively constant over the 135 °C to 180 °C range in cure temperature, tending to indicate that the underfills have fully cured during processing.

To better understand how the T_g, CTE, storage modulus, and cure parameters correlate with the residual stress generated during cure, Figs. 17, 19, and 20 are developed. In these figures, the postcure residual stresses are plotted as contour maps as a function of G', CTE, and T_g. With such graphs, the impact of G', CTE, T_g, and cure parameters on residual stress generation can be more clearly illustrated. For the given test vehicle and underfill combination, the optimal cure parameter range to minimize residual stresses can be determined from Figs. 17, 19, and 20. Based on Fig. 17, the minimum residual stress occurs at a low CTE about 19 ppm and a low modulus about 5 GPa. Alternately, a higher CTE of about 23 ppm and moderate storage modulus of about 6 GPa also produces lower residual stresses. To achieve the lowest stress states, the optimal cure schedule would be 135 °C for 80 min or 180 °C for 15 min. In contrast, the maximum residual stress is seen at a CTE of 21 ppm and G' of 7 GPa, corresponding to a cure condition of 165 °C for 60 min.

From Fig. 19, the maximum stress is seen at a T_g of 138 °C and a storage modulus of 6.0 GPa. The minimum stress occurred at a T_g of 139 °C and a G' of 5.5 GPa. This implies an optimum cure condition for minimum residual stress generation of 135 °C for 80 min. The next lowest stress state occurs at a G' of 5 GPa and a T_g of 136 °C corresponding to a cure condition of 180 °C for 15 min.

Fig. 20 correlates T_g and the CTE of the encapsulant to the residual stress post underfill cure. The lowest stress is seen at a T_g of 139 °C and CTE of about 22.5 ppm/°C. This corresponds to the cure conditions of 135 °C for 80 min. Alternately, the next lowest stress state is at a CTE of 19 ppm and T_g of 136 °C corresponding to the cure condition of 180 °C for 15 min. In contrast, the maximum stress for the test vehicle studied is seen at a T_g of 140.5 °C and a CTE of 20.5 ppm. Based on these results and the requirement that the manufacturing cycle time be minimized, the best process conditions for the system studied to minimize residual stress generation corresponds to a cure temperature of 180 °C for 15 minutes.

Figs. 17, 19, and 20 illustrate some additional features worthy of discussion. Notice in these figures, particularly the (a) plots, that a minimum stress state occurs at the lowest G', CTE, and T_g. Based on the thermomechanical behavior of the system, it is expected that a low stress state would occur at these conditions. Interestingly, the cure schedule corresponding to the lowest G', CTE and T_g is 180 °C for 15 min. The other low stress state occurs for the underfill having moderate to high values for the G', CTE, and T_g which is contrary to what thermomechanical behavior would suggest. This corresponds to the 130 °C for 80 min cure schedule. In addition, one of the maximum residual stress states occurs for G', CTE, and T_g values very close to those of the 130 °C cure schedule. In particular, one of the maximum stress states occurred at the 145 °C for 40 min cure schedule having slightly different G', CTE, and T_g values than the 130 °C for 80 min cure schedule. This tends to suggest that the residual stress state resulting from underfill processing is more complex than basic thermomechanical behavior might suggest. Based on the results of Figs. 17, 19, and 20, it appears that more complex phenomena such as interfacial stress relief, underfill free volume effects, etc. can play a major role in determining the residual stress state of flip chip assemblies.

VII. Conclusion

The current results indicate that the underfill cure process produces relatively large compressive stresses on the active die surface. The stress state indicates a complex convex bending state in the flip chip relative to the active die surface. The resulting die stresses are within ranges reported for semiconductor silicon fracture indicating higher probabilities for die cracking. The residual die stresses are also found to be strongly dependent on underfill CTE, G', T_g, and ultimately the underfill cure process. To produce test vehicle assemblies with the lowest effective die stresses, the optimum cure schedule for the select underfill is a temperature of 180 °C for 15 min. The optimum post cure underfill properties are 19 ppm for CTE, 5 GPa for G', and 136 °C for T_g. The residual stresses are also very sensitive to changes in CTE, G', and T_g. In general, a 5–10% change in the underfill reported properties can result in stress differentials as large as 15 MPa. Based on first order calculations, the contribution to the overall stress state is dominated by the complex bending state of the device due to the interfacial stresses and, to a lesser extent, due to the pure shrinkage of underfill material.

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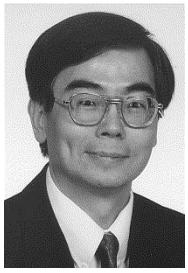

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