INTEGRATION OF OPTOELECTRONICS INTERCONNECTS ON GLASS INTERPOSERS FOR HIGH SPEED COMMUNICATIONS

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INTEGRATION OF OPTOELECTRONICS INTERCONNECTS ON GLASS INTERPOSERS FOR HIGH SPEED COMMUNICATIONS

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LIST OF ACRONYMS

3DGP	3D glass photonics
ABF	Ajinomoto buildup film
AI	artificial intelligence
BCB	benzocyclobutene
BEOL	back end of line
BSE	backscattered electron
CMOS	complementary metal–oxide–semiconductor
CTE	thermal expansion coefficient
DOF	depth of focus
EDS	energy–dispersive X–ray spectroscopy
EMIB	embedded multi–die interconnect bridge
i–THOP	integrated thin film high density organic package
I/O	inputs/outputs
IC	integrated circuit
ILD	interlayer dielectric
InFO	integrated fan–out
LPCVD	low pressure chemical vapor deposition
MMF	multimode fiber
MZM	Mach–Zehnder modulator
NA	numerical aperture
OOK	on–off keying
PAC	photoactive compound
PCB	printed circuit board
PECVD	plasma enhanced chemical vapor deposition
PET	polyethylene terephthalate
PID	photoimageable dielectric
PMMA	poly(methyl methacrylate)
PS	polystyrene
PU	polyurethane
PVD	physical vapor deposition
PZT	lead zirconate titanate
RCC	resin coated on copper
RDL	redistribution layer
RGB	red, green, and blue
RPM	round per minute
SAP	semi–additive process
SEM	scanning electron microscope
SiOB	silicon optical bench

SMF	single mode fiber
SMWG	single mode waveguide
SNR	signal–to–noise ratio
SOI	silicon–on–insulator
TMAH	tetramethylammonium hydroxide
UHD	ultra–high–definition
UI	unit interval
UV	ultraviolet
VR	virtual reality
WLP	wafer–level processing

SUMMARY

The development and application of artificial intelligence and augmented reality as well as billions of new devices connected to the network have resulted in unprecedented demands on high computing power and high speed communications. The focus has shifted from Moore's law on the transistor density of semiconductor chips to post–Moore's–law on the interconnect density of packages to continue improving the computing power and data rates. As the demand for data rates increases, electronic interconnects are limited to short–distance chip–to–chip communications by signal integrity issues at high frequency, which sheds a light on bringing optical interconnects onto the package for on–package long–distance communications.

The key technology to enhance electronic interconnect performance on a package is the redistribution layers, with the 2.5D interposer package with ultra–fine wiring to improve the density of interconnects. Challenges emerge as the density of lines increase with this approach such as poor adhesion due to small contacting areas. The density of microvias has not progressed as much to match the density of wires. On the other hand, silicon photonics and board–level optoelectronics have been studied and developed intensively to achieve high speed optical communications on chip. However, silicon photonics suffers from the high costs of silicon–on–insulator substrates and the back end of line fabrication processes, and the board–level optoelectronics is limited by the multimode operation and the mismatch on thermal expansion coefficients between different modules.

The objective of this research was to integrate high density electronic interconnects for chip–to–chip communications and low loss single mode optical interconnects for on–package communications, as well as fiber coupling and integration, on glass interposers. Glass as the substrate material offers a unique combination of superior properties compared to silicon and polymer substrates. It also has a low optical absorption at telecommunication wavelengths for optical applications. This research included the following topics:

1) development and optimization of ultraviolet laser ablation process for ultra–small microvia fabrication to match the density of ultra–fine routing wires; 2) modeling, design, processing, and characterization of high–quality low loss single mode waveguides on glass interposers; 3) high–precision passive fiber coupling and integration on glass interposers.

Laser ablation on polymer dielectrics was intensively studied for the fabrication of ultra–small microvias. A picosecond UV laser drilling system was used in this study, and microvias were scaled down to 5 μm in diameter from the state–of–the–art 20 μm microvias by laser ablation. By adding a nanometer metal barrier layer with a high ablation threshold, the fully opened microvias were scaled down to 1.3 μm in diameter, which is one fifteenth of the state of the art. Laser landing accuracy was also analyzed since the smaller microvias required multiple punches to fabricate. The average difference between the designed drilling spot and the actual landing spot was 0.24 μm.

Polymer–based single mode waveguides using glass as the bottom clad was modeled, fabricated and characterized. After process optimization, defects were eliminated, hence, the measured propagation loss of fabricated waveguides was around 0.6 dB/cm, half of the previously reported value. Data rates were also measured. However, the maximum data rate was limited by the electronic components in the measurement setup to be 21.3 Gbps. The potentially supported data rates could be much higher.

High accuracy passive fiber coupling and integration on glass were also investigated. A flip v–groove approach was proposed and developed to confine degrees of freedom of fibers. Using the surface of the glass substrate as a reference and the diameter of the fiber as the core height control brought the center of the fiber core to be 62.8 ± 0.1 μm, which is very close to the height of the fabricated waveguide cores which is 63 μm. Alignment in only one direction is needed.

CHAPTER 1
INTRODUCTION

As the emerging technologies like cloud computing, artificial intelligence (AI), virtual reality (VR), and ultra–high–definition (UHD), gaming and streaming are developed and applied, demands for higher computing power and higher data rates between chips keep increasing. The number of transistors on a semiconductor chip doubles every two years according to the famous observation, Moore's law [1], which increases the computing power of semiconductor chips dramatically. However, as the size of transistors is scaled down to 7 nm and even smaller, Moore's Law is beginning to hit the limit of physics, and slowing down in transistor performance. Continuous scaling of transistors on semiconductor chips is no longer economical to achieve the same level of improvement on performance as well.

The focus has shifted from Moore's law with semiconductor chips to post–Moore's–law with what Prof. Tummala calls Moore's law for Packaging or Interconnects [3, 4]. This resulted in integrating multiple chips on one package to increase computing power for many applications [2, 5], as shown in Figure 1.1, and such an architecture requires advanced packaging technologies to support high data rate chip–to–chip communications. The key technology to enhance interconnect performance on a package is the redistribution layer (RDL)s, with the 2.5D interposer package with ultra–fine RDL wiring to improve the density of interconnects and performance of a package. Challenges emerge as the density of lines and microvias increase with this approach. The semi–additive process (SAP) is currently the primary technique for copper trace fabrication in panel size RDL processing. When the line width of the copper trace is scaled down to less than 2 µm, poor adhesion due to small contacting area leads to reliability issues. Meanwhile, as the line width is scaled down to 5 µm and less, microvias connecting thin lines in different layers has not scaled down to support high density lines. Electronic interconnects with fine copper traces

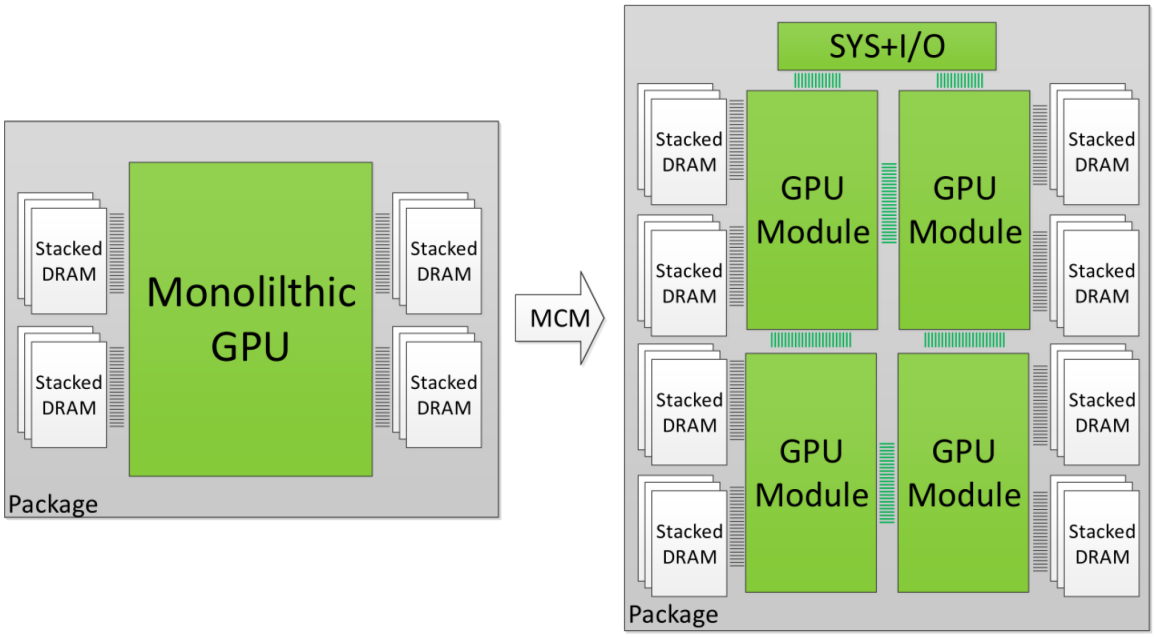


Figure 1.1: MCM-GPU: Aggregating GPU modules and DRAM on a single package [2].

and microvias are limited by signal integrity and interconnect delay issues caused by high frequency electromagnetic effects such as crosstalk, delay, resistance and capacitance when facing high data rate demands.

Fiber optics has advanced significantly over the past several decades due to the exceptional data transport ability of fibers over copper wires across long distances. Compared to copper wires, fibers have lower loss, immunity to electromagnetic interference, light weight, and they could provide extremely high data rates. Fibers are now the backbone of ever–increasing global internet traffic in modern communications. With the development and application of technologies like cloud computing and UHD streaming, as well as billions of new mobile devices that are interconnected every year, they have resulted in ever–increasing global internet traffic, which is projected to be 396 exabytes (10^{18} bytes) per month by 2022 [6, 7], as shown in Figure 1.2. Not only telecommunication demands higher data rates, but also other demands from on–device applications such as AI and VR. Traditionally, single mode optical components are placed on a silicon optical bench (SiOB) as individual chips, which requires a large substrate to integrate. As the single mode optics

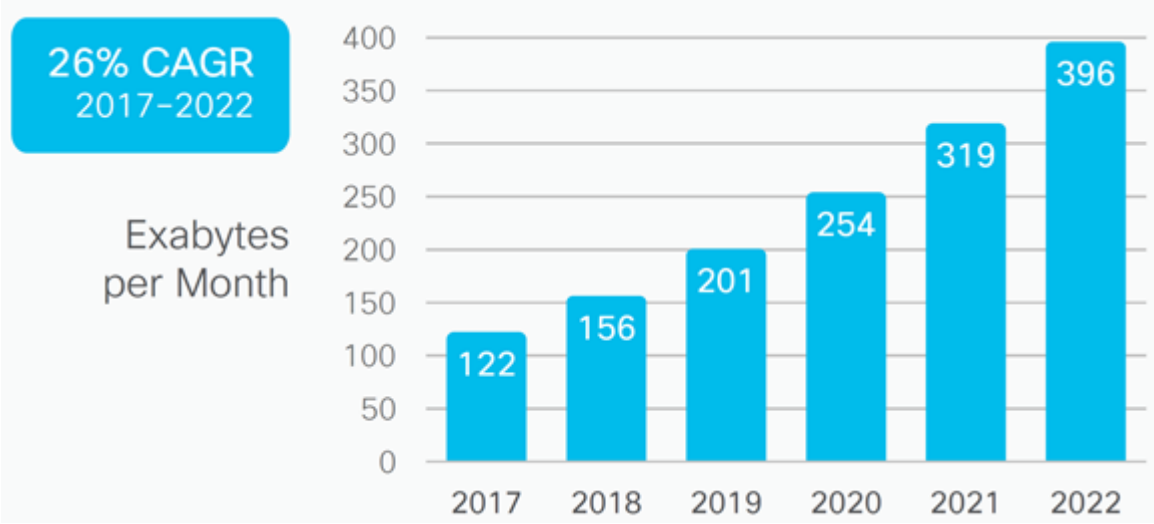


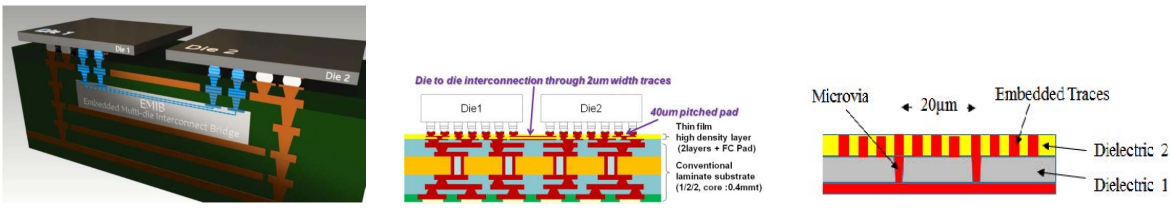
Figure 1.2: Cisco VNI forecasts 396 EB per month of IP traffic by 2022 [6].

is applied for shorter distances like chip–to–chip communications, packaging especially optical interconnects becomes the bottleneck. There are several factors contributing to this bottleneck; 1) Alignment requirement of fibers to waveguides at micron size level, and 2) optical structures fabricated on substrates to reduce coupling loss.

To address these issues for high data rate demands of on–package chip–to–chip communications, glass interposers with a combination of high–density electronic interconnects for chip–to–chip communications and single mode optical interconnects for on–package communications were proposed and developed in this work.

1.1 Current Trends on High Speed Interconnects

Several approaches have been investigated and developed to optimize the cost, performance, and integration density of high–speed interconnects at a system level. The current integration approaches are high density inputs/outputs (I/O) for electronics, silicon photonics, glass photonics, and board–level optoelectronics.



(a) **(b)** **(c)**

Figure 1.3: (a) Schematic showing the EMIB concept [8]. (b) Schematic cross sectional image of i–THOP [9]. (c) The schematic of novel ViT interconnect configuration for 20 µm bump pitch interposer and package application. The traces are embedded in the dielectric layer and surrounded by polymer [10].

1.1.1 High–Density I/O for Electronics

Increasing data traffic demands high bandwidth to transport data as well as high speed electronics to process data. Increasing I/O and component density in electronic systems requires higher density packaging and higher level of integration. Over the years, the wiring technologies for RDL have evolved from subtractive etching to SAP. Challenges emerge as the width of the copper trace is scaled down to less than 5 µm. Large areas of the sidewalls compared to the seed layer at the bottom will be etched away in the seed layer removal process, which leads to smaller contact area of copper to the substrate, and subsequent adhesion and reliability issues. The current trend is to push the line width down to submicron level with high aspect ratio to achieve high–density I/O with appropriate resistance, capacitance, and characteristic impedance.

There are three popular substrate materials used for high–density I/O in packaging: silicon, organic, and glass, as shown in Figure 1.3. Silicon interposers, led by Intel's embedded multi–die interconnect bridge (EMIB) [8], were developed using back end of line (BEOL) process. RDLs could be built directly on silicon wafers without a substrate as well, like the integrated fan–out (InFO) wafer–level processing (WLP) technology developed by TSMC [11]. The line width achieved is less than a micron, and the interconnect density is in the range of 500–1000 I/O/mm/layer. However, the cost of BEOL process is high due to primarily the small 300 mm wafer size. Organic interposers, such as integrated thin film

high density organic package (i–THOP) by Shinko [9], have a relatively low cost due to large panel processing, but the line width achieved is 2 µm. Glass interposers, developed by 3D Packaging Research Center at Georgia Tech [10], have achieved copper traces with 1 µm in line width with panel processing capability.

When copper traces are scaled down to increase I/O density, microvias to electrically connect copper traces in different layers must be scaled down as well to accommodate the smaller sizes of copper traces. Previously, laser drilling was widely used for microvia fabrication until the diameter of microvias was scaled down to 40 µm. Microvias by photolithography replaced laser ablation when the size of microvias was lowered to 8 µm, which hasn't matched the line width of copper traces developed in recent years.

1.1.2 Silicon Photonics

Silicon photonics is a promising candidate to realize high density on–chip integration of electronics and photonics. A photo of such a silicon photonic chip is shown in Figure 1.4. By adopting mature complementary metal–oxide–semiconductor (CMOS) technology for high–volume semiconductor manufacturing, silicon photonics could be a low–cost solution [13], and waveguides on silicon photonic chips could have an extremely low propagation loss at around 0.1 dB/m [14]. However, there are some drawbacks with silicon photonics.

First, the light sources are a huge challenge in silicon photonics. The integration of laser on silicon photonic chips could be monolithic or heterogeneous. For monolithic integration, silicon is an obvious choice, but silicon does not have a direct bandgap, which means photons generated from the combination of electrons and holes in silicon is too low in efficiency. Silicon is able to serve as a light source through Raman scattering, which is inelastic scattering of a photon upon interaction with matter. The first pulsed Rama laser was demonstrated in 2004 by a group in UCLA [15], and the first continuous–wave Raman laser was demonstrated in 2005 by Intel [16], but the efficiency was still low, approximately one in ten million photons. Erbium doped silicon materials and erbium compound materials

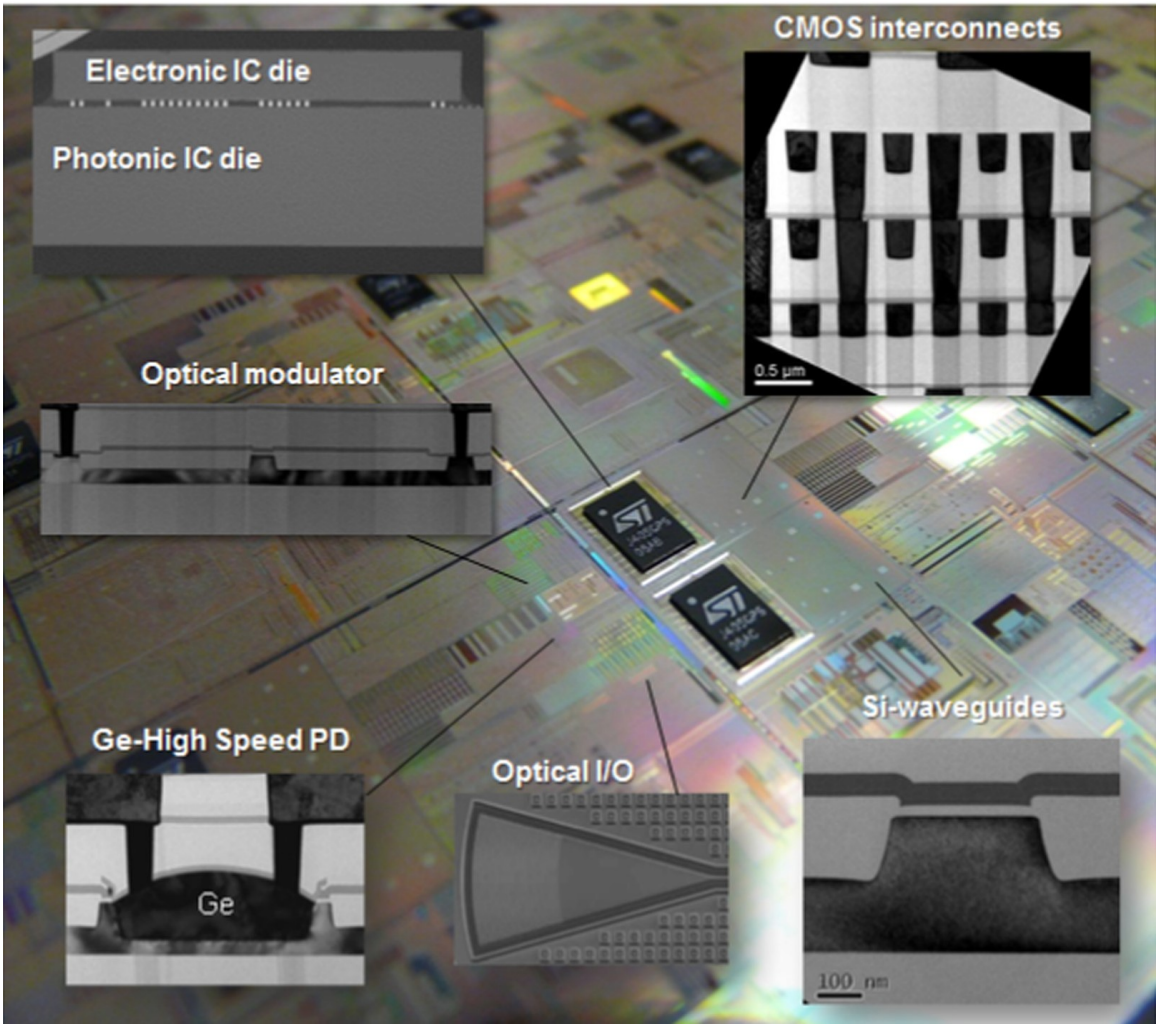


Figure 1.4: Overview of current fully integrated silicon photonics technology using a 3D electronic IC [12].

use erbium as an atomic emitting center for monolithic integration. Optical–pumped Er–doped lasers were demonstrated [17] but not electrical pumped lasers. Germanium exhibits a pseudo–direct gap behavior. The band gap could be engineered so that the direct recombination of electrons and holes could happen [18]. It could be a candidate for monolithic integration of laser source. Currently the most practical on–chip light source for silicon photonics is III–V–based lasers like InP. It could be monolithically integrated via epitaxial growth [19], but the high density dislocations from large differences in thermal expansion coefficients between III–V compounds and silicon may cause reliability issues. III–V compound lasers could also be directly mounted on silicon [20], which allows pre–testing

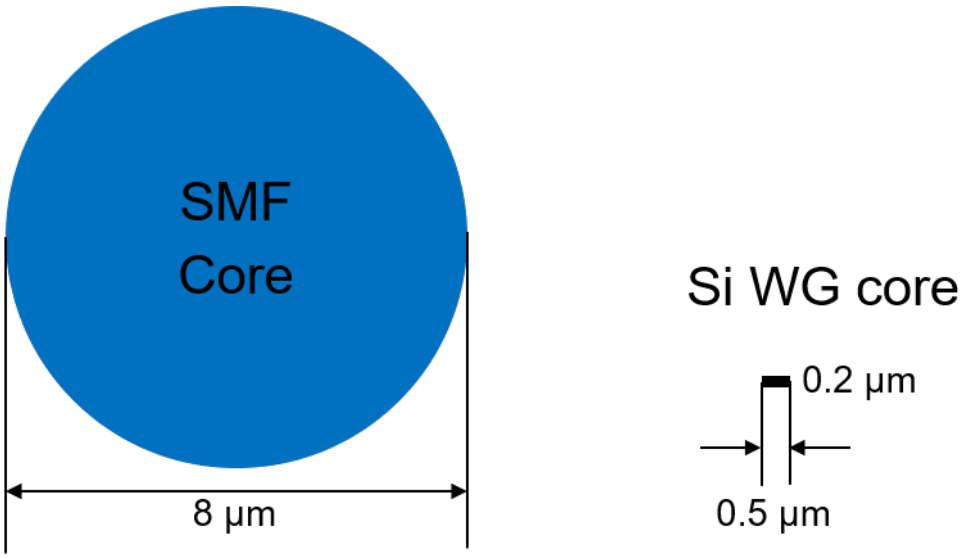


Figure 1.5: Schematics of (a) a SMF core and (b) a silicon waveguide core.

before integration to maintain superior characteristics of the laser chips.

The other issue with silicon photonics is silicon–based waveguides and their coupling. Due to the surface roughness (around 5 nm) of the side walls of silicon waveguide cores, the propagation loss of silicon was huge compared to polymer or glass waveguides. But as the fabrication process improved, the propagation loss of silicon waveguide has been lowered to less than 1 dB/cm [21]. Even though it's still large compared to polymer and glass waveguides, it's not an obstacle for application since the lengths of the silicon waveguides are generally short. Silicon also has a relatively large refractive index. The size of the silicon waveguide core is extremely small (around 0.5 μm by 0.2 μm) compared to the size of the fiber core (around 8.4 μm in diameter) as shown in Figure 1.5, so direct coupling from a fiber to a silicon–based waveguide would have a huge mode mismatch loss (20 dB). Additional couplers are needed to couple light from a fiber to a waveguide. For horizontal coupling, different spot size converters and couplers have been designed and tested for low coupling loss. For vertical coupling, grating couplers have been studied intensively for wide band low loss coupling.

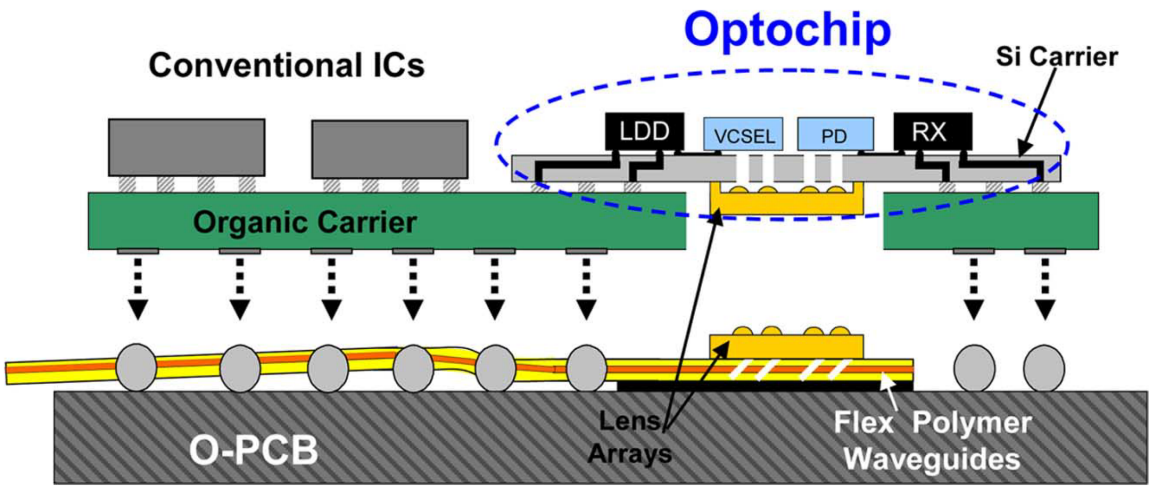


Figure 1.6: Schematic representation of the Terabus vision of an OE–MCM (or optomodule) incorporating an 850 nm transceiver optochip as well as conventional ICs [23].

1.1.3 Board–Level Optoelectronics

Traditional board–level optical systems use discrete integration of optical components and electronic chips. In a typical optical transceiver package, there are laser diodes, lenses, drivers, amplifiers, photodetectors, etc. These discrete components are placed on a SiOB [22]. Precise alignment structures for fiber positioning and coupling could be fabricated on SiOB due to its crystallinity.

The Terabus project, developed by IBM, focuses on highly integrated high density low–power and high speed optical interconnect technologies [23]. A schematic of Terabus project is shown in Figure 1.6. Optochips are mounted on a silicon carrier, and then assembled on an organic carrier with other conventional integrated circuit (IC)s. The organic carrier is then soldered to an optical printed circuit board (PCB). However, the system operates with multimode optics, and the mismatch in thermal expansion coefficient among silicon carriers, organic carriers, and optical PCBs might lead to reliability issues. Also, the silicon carrier for optochips might introduce high speed electrical losses, which leads to degradation of energy efficiency.

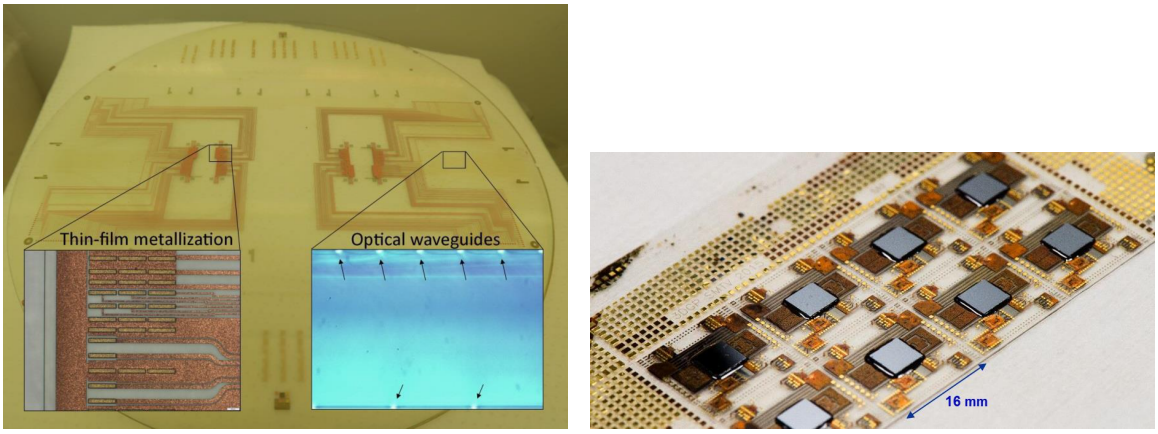
1.1.4 Glass Photonics

Glass photonics, which emerged in recent years as a superior option over organic and silicon interposers for microelectronics applications, has been drawing tremendous attention. Glass offers a unique combination of superior properties compared with traditional silicon and organic packaging for both electronics and photonics. Some of the properties of glass and silicon are listed in Table 1.1. For optical applications, the optical absorption of glass at telecommunication wavelengths is low, and the refractive index of glass matches that of SMFs, which enables glass to be integrated as part of waveguide structures. For electronic applications, the loss tangent of glass is relatively low compared to that of silicon. The thermal expansion coefficient (CTE) of glass could also be tailored to match either silicon– or III–V–based photonic chips.

Table 1.1: Properties of glass and silicon.

Material Properties	Glass	Silicon
Optical absorption α (cm^{-1}) @ 1550 nm	0.007	8.2
Refraxctive index n @ 1550 nm	1.49	3.48
Electrical loss $\tan\theta$ @ 10 GHz	0.006	0.015
Thermal expansion coefficient (CTE) (ppm/K)	3–8.5	3
Microscopic structure	Amorphous	Crystalline
Finest feature size (μm)	1	0.005
Processing capability	Panel–level	Wafer–level

The PhoxTroT project [24], developed by Fraunhofer IZM and TU Berlin, used ion exchange to modify refractive index of glass to create waveguides in the glass, with extremely low propagation losses (0.043 dB/cm at 1.31 μm and 0.059 dB/cm at 1.55 μm). It is shown in Figure 1.7(a). It also enables low loss coupling of glass waveguides to fiber. 3D glass photonics (3DGP) interposers, developed by Georgia Tech Packaging Research Center [25], is another candidate for glass photonics, as shown in Figure 1.7(b). Unlike



(a) **(b)**

Figure 1.7: (a) Optical dual–layer waveguide integration and thin–film metallization on a 200 mm wafer level [24], and (b) The top half of glass panel after ENIG and chip assembly [25].

PhoxTroT, 3DGP interposers enable light traveling in the horizontal direction, as well as vertical directions with turning structures, vertical optical vias through glass interposers, and optical lenses, by using low loss optical polymers with the glass interposer.

1.2 Unique Approach Proposed and Developed

Organic interposers do not address high–density integration need, and they are not compatible with optical interconnects on interposers. Although silicon interposers support high–density integration, and are transparent at telecommunication wavelengths, they are not able to address on–package communications, owning primarily to the huge electrical loss and the size of the chip.

In order to address the challenges of combining single mode optics with high speed electronics for high speed communications, the proposed research investigated integration of high density electronic interconnects and single mode optical interconnects, as well as fiber integration on glass interposers. A cross–sectional view of the proposed glass interposer with high density electronic interconnects and low loss single mode optical interconnects with fiber integration is shown in Figure 1.8.

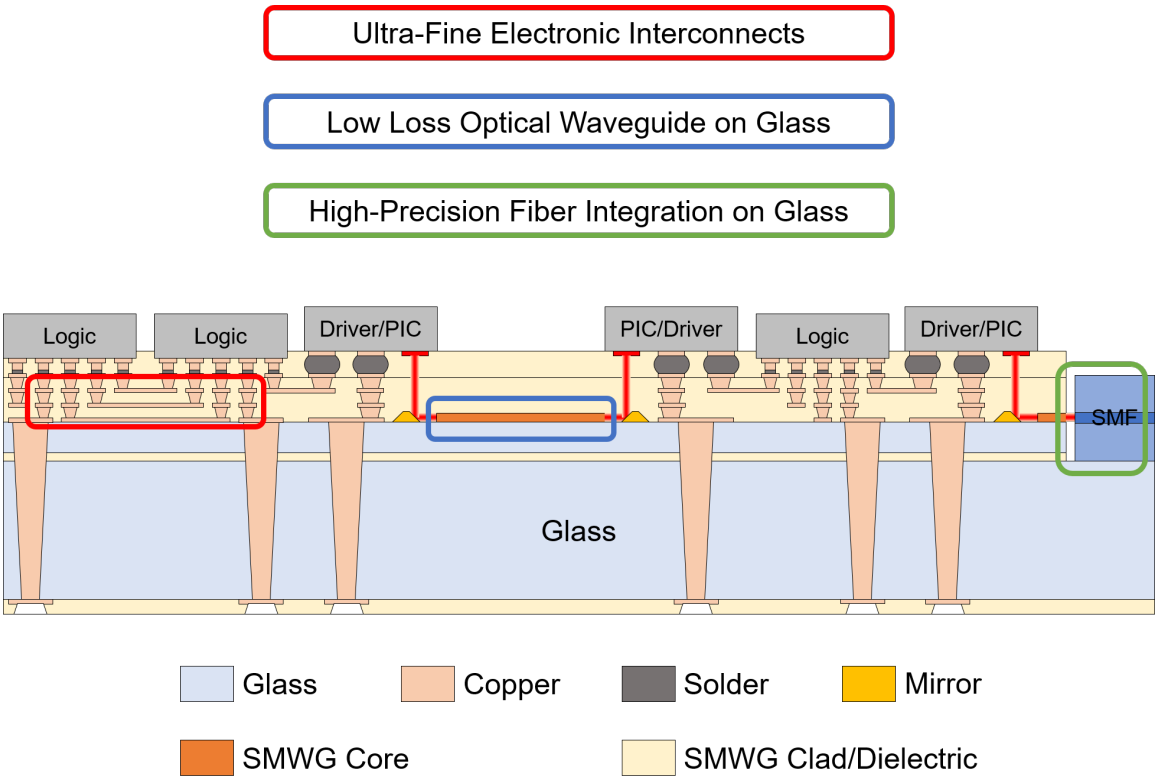


Figure 1.8: A schematic of glass interposers with high–density electronic interconnects and low loss single mode optical interconnects with fiber integration.

Glass as the substrate material offers a unique combination of superior properties compared to silicon and polymer substrates. The refractive index of glass matches that of SMFs, so optical polymer waveguides on glass substrates enable direct coupling without fabricating additional coupling structures. Low optical absorption and low loss polymers could also be used as high–performance dielectric for electrical interconnects. Glass's CTE could be tailored to match either silicon based chips or III–IV based compound photonic chips. Double side fabrication and panel–level processing also reduce costs. Thus, high bandwidth communications could be achieved by integrating single mode waveguide (SMWG)s on glass interposers and passive alignment of single mode fibers. Glass with its excellent surface finish also has a low surface roughness and high dimensional stability, which enables 1 µm features similar to silicon interposers for high density integration. With ultra–fine copper traces and microvias recently developed on glass substrates, high–density

electrical interconnects could be integrated on the same glass interposers.

1.3 Research Objectives, Challenges, and Tasks

The objective of the research is to integrate high–density electronic interconnects with low loss single mode optical interconnects along with fiber coupling and integration on glass interposers for high speed communications. The research can be broken into three aspects, electrical interconnects, optical interconnects, and fiber integration. Detailed research objectives are listed in Table 1.2.

Table 1.2: Research objectives, challenges, and tasks.

	Objective	**Prior Art**	**Challenges**	**Tasks**
Electronic interconnects	$\leq 5\,\mu m$ in diameter microvias and ultra–fine copper traces for RDL	$20\,\mu m$ in diameter	Development and optimization for smaller microvia fabrication	Embedded trenches for high–density RDLs Process optimization for smaller microvias
Optical interconnects	≤ 0.3 dB/cm SMWGs on glass interposers	Propagation loss of 0.3 dB/cm at 1310/1550 nm	High–quality polymer SMWG fabrication and characterization	Modeling, design, and process optimization Characterization on losses and data rates
Fiber coupling and integration	$\leq 1\,\mu m$ high accuracy positioning	Active alignment Passive alignment	Precise alignment structure fabrication on glass interposers	Glass–to–glass bonding Fibers in v–groove chips on glass

Electrical interconnects pose many issues: traditional SAP technology to fabricate copper traces scaling down to less than 5 µm creates adhesion challenges between copper traces and the substrate. New fabrication techniques need to be developed to address this issue. The other issue is to do with the size of microvias. Even though the width of copper traces is being scaled down to 5 µm and below, the currently available microvia technology connecting copper RDL traces is still at around $20\,\mu m$ in diameter (fabricated by laser ablation). Smaller microvias are needed to match the size of copper traces that are less than $5\,\mu m$. The research tasks to address the challenges to high density electronic interconnects are: 1) Development and optimization of embedded trenches for high density copper traces, and 2) Development and optimization of ultraviolet (UV) laser ablation process for ultra–small

microvia fabrication.

Optical interconnects have a set of their own challenges. One challenge is to do with low loss optical interconnects with single mode waveguide fabrication, and characterization. Optical polymers were studied and developed intensively 20 years ago by research groups and chemical companies, but the development of new and low loss optical polymers basically stopped due to lack of customers and applications. The main challenges for low loss optical interconnects on glass are identifying and developing optical polymers to be used with glass and silicon substrates as well as their fabrication and reliability of high–quality single mode waveguides. To address these challenges, the tasks include modeling, design, processing, and characterization of high–quality low loss single mode waveguides.

The other challenge in optical interconnects that needs to be addressed is precise fiber positioning. To minimize coupling loss, fiber alignment accuracy must be less than $\pm 2\,\mu m$ (more toward $\pm 1\,\mu m$). For traditional silicon optical benches, precise positioning of fiber could be achieved with the advanced etching technologies available such as polishing and creating tapered structures in silicon along with its inherent advantages from the crystallinity of silicon. However, with glass being an amorphous and brittle material, it is extremely challenging to fabricate structures for precise positioning either with chemical etching or physical machining. Additional structures must be introduced to achieve high accuracy alignment. So, the tasks include glass–to–glass bonding, and fibers in v–groove chips assembled on glass.

1.4 Dissertation Overview

The dissertation document is organized as follows. Chapter 1 provided the necessary background and strategic need for the research topic. It also defined the research objectives, identified three main challenges for integrating optical interconnects and electrical interconnects on a single package for high data rate communications. It also outlined the unique approach and research tasks to address the challenges. Chapter 2 summarizes the literature

describing the scaling down of microvias for high density electrical interconnects, the materials used for fabrication of single mode waveguides, board–level photonic and electronic integration, and fiber integration. Chapter 3 describes the modeling, process development, fabrication, and characterization of ultra–short (picosecond) pulsed laser ablation for ultra–small microvia fabrication. Chapter 4 describes the modeling, design, fabrication, and characterization of polymer SMWGs on glass. Chapter 5 describes the design and analysis of fiber integration on glass substrates. The research results and possible future work beyond the scope of this dissertation are summarized in Chapter 6.

CHAPTER 2
LITERATURE SURVEY

This chapter reviews the most recent work in three areas of research which are the focus of this thesis work. The first section discusses high-density I/O for electronics including ultra–fine routing wires and microvias, followed by the second section summarizing low loss optical interconnects including SMWGs fabricated using different types of materials. The last section covers fiber coupling techniques and methods.

2.1 High–Density I/O for Electronics

As the feature size of transistors is scaled down to 7 nm and below, Moore's law is approaching its limit, and the industry and the academia have shifted their focuses from shrinking the transistor sizes to increasing the packaging density. The key technology to improve electronic interconnect density is RDLs, and microvias are one of the crucial elements of RDLs. As a result, reducing the dimensions of routing lines and spaces in RDLs to increase I/O density has been widely recognized and studied. Interposer technologies to address this issue have been evolving, from high–cost but high–density silicon–based interposers, to organic and panel–glass–based interposers, whose densities have been developed to try to match silicon while the costs wouldn't be as high. As the sizes of routing wires and spaces on package RDLs are scaled down to 2–1 μm [26, 27], microvias to connect routing wires between layers haven't been progressed much to match the wiring density. To meet the requirement of the next generation packaging for high performance computing, the scaling of microvias plays the critical role.

There are two major technologies to fabricate microvias, photolithography (photovias), and laser ablation. Photolithography drew attention in fabricating microvias due to its ease to use and the ability to form small microvias. The dimension of microvias in polymer

has evolved from 10 µm in diameter in a 5 µm thick film with a 40 µm pitch [10], to 4 µm in diameter in a 3 µm thick film [28]. With the development of photoimageable dielectric (PID) materials, 2–3 µm microvias were also demonstrated [29, 30]. As the size of microvias is scaled down even further, new PIDs are needed to meet the critical dimension requirement. However, the availability of the suitable PID materials limits the development of even smaller microvias.

Laser ablation as a competing technology to fabricate microvias has been developed in parallel with photovias. It is the most economical method for mass production. Unlike photolithography, laser ablation is not limited to the substrate material to be drilled, which promotes the widespread use of laser ablation in packaging industry. The basic principle of laser ablation is to use high concentration photons in the laser beam to vaporize or ionize the material to be drilled. The intensity of the laser beam has to reach a certain level for the ablation to happen, which is called the ablation threshold of the material. If the intensity of the beam doesn't reach the threshold, the laser beam could only heat the material up or melt it, but it won't remove it away from the substrate.

Different laser systems have their own advantages and disadvantages for certain applications. Widely used lasers with regards to wavelengths are CO_2 lasers (infrared), UV lasers, and excimer lasers (deep–UV). In terms of the laser operation mode, lasers could also be categorized as continuous–wave lasers, and pulsed lasers, whose pulse width could be several nanoseconds, or on the picosecond level, or on the femtosecond level. CO_2 lasers have longer wavelengths among the aforementioned laser systems and they operate in a continuous wave mode, which limit CO_2 lasers to fabricate microvias with the diameter of 60–80 µm and above [31]. As the wavelength of the laser systems becomes shorter and into the UV range, it helps the laser system focus the beam into a smaller size. The state–of–the–art microvias fabricated by a nanosecond UV laser are 20 µm in diameter [32]. As the pulse width of the UV laser becomes shorter, photons in a laser beam could be more concentrated, which reduces the heat affected zone surrounding the drilling area.

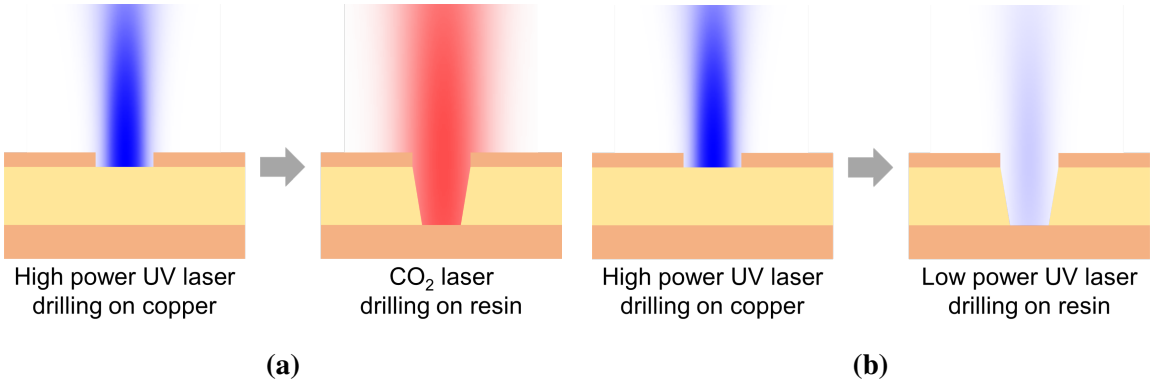


Figure 2.1: Schematics of laser drilling on RCC with (a) a hybrid laser system and (b) two—step UV laser drilling system. © 2020 IEEE

So picosecond and femtosecond UV lasers are favored over nanosecond UV lasers in terms of the micromachining quality and the cost of the lasers [33]. Excimer lasers have even shorter wavelengths compared to general UV lasers. Excimer laser ablation could achieve microvias of 5 µm in diameter [34]. However, excimer lasers suffer from high costs and high maintenance like femtosecond laser systems.

Using a single laser might not achieve microvias with the desired dimensions. Hybrid laser systems were also developed to create smaller microvias by using resin coated on copper (RCC) foil instead of bare polymer. One type of hybrid laser ablation includes a high–power UV laser drilling on the top copper layer, and subsequently a CO_2 laser drilling polymer through the opening in the copper layer, as shown in Figure 2.1(a). Copper has a high ablation threshold than polymer in general, so when the UV laser beam with the same power hit the copper, it will result in a smaller opening, which then serves as a mask for the following ablation in the polymer by CO_2 lasers. Since CO_2 lasers won't remove copper, the microvia would stay small after the ablation and copper removal. The other type of hybrid laser ablation is a two–step UV laser ablation [35, 36], as shown in Figure 2.1(b). Copper drilling is accomplished by the first step high–power UV laser ablation. The drilling time and drilling power are controlled in a way that it only ablates copper but not the resin underneath. The same laser is then adjusted to a lower power to drill through the resin without damaging the copper on top or underneath.

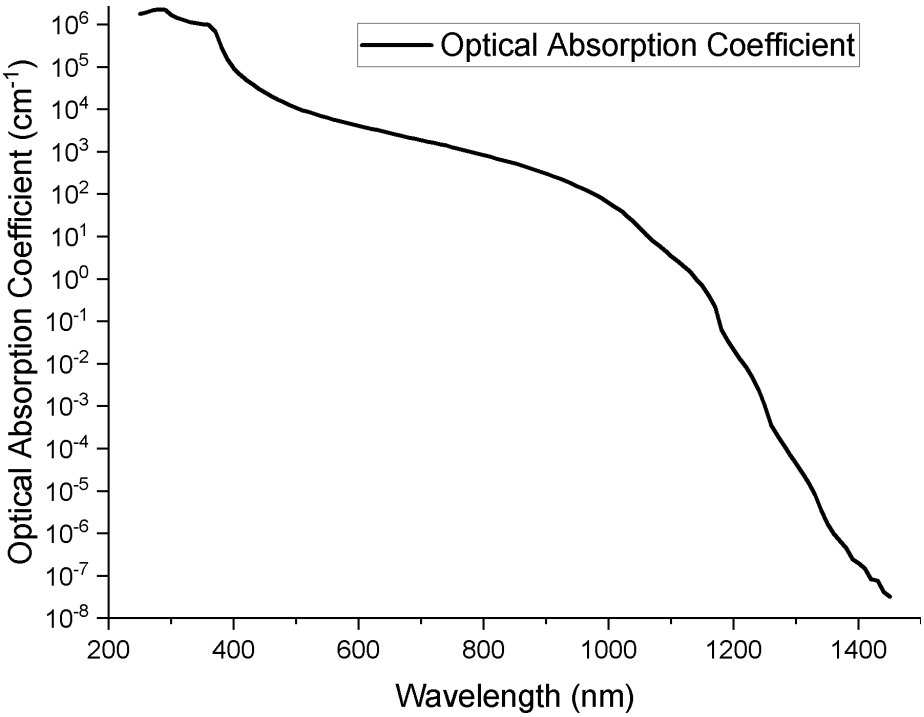


Figure 2.2: Optical absorption coefficient of silicon [37].

This thesis attempts to make contribution to fabricate ultra–small microvias for high density electronic interconnects using a picosecond UV laser in traditional and novel dielectric materials.

2.2 Low Loss Optical Interconnects

This section discusses selected publications in the area of SMWG materials, integration methods, and applications along with three categories of SMWG materials that are based on silicon, glass, and polymer.

2.2.1 Silicon–Based SMWGs

Silicon–based SMWGs are the key component of silicon photonics. The most commonly used material platform is silicon–on–insulator (SOI), which is a thin silicon layer on a buried oxide (SiO_2) layer on bulk silicon. There are three major silicon–based materials for waveguide cores, silicon, silicon nitride, and silicon germanium. Silicon is used as a

waveguide core material due to three reasons. First, the absorption of silicon at telecommunication wavelengths is low, as shown in Figure 2.2, as a result of which the propagation loss of silicon waveguides is tremendously reduced. The second reason is the electro–optical effects in silicon, which make it possible to modulate signals in silicon waveguides [38]. The third reason is that the large contrast between silicon and silicon dioxide makes the size of silicon waveguides small and compact which enables high density optical interconnects on chip.

The propagation loss of SOI waveguides was not great at the beginning of the development. Due to the traditional fabrication process, dry etching, the sidewalls of the silicon cores were extremely rough, around 7 nm, which contributes to the propagation loss as high as 5–12 dB/cm. Various techniques have been developed to address the roughness issue and then reduce the propagation loss. By using wet etching instead of dry etching, the sidewall roughness could be reduced down to 1.2 nm, and the propagation loss could be lowered to 0.85 dB/cm [39]. By adding a SiO_2 hard mask in the dry etching process, the propagation loss of silicon waveguide could also be reduced since the sidewall roughness was reduced to 0.7 nm, and the measured propagation loss was 0.89 dB/cm [40]. The performance of silicon waveguides were also improved by using CMOS platform and optimized etching process to lower the propagation loss down to 0.45 dB/cm [41].

Silicon nitride is a widely used material in CMOS fabrication. It is usually deposited by either low pressure chemical vapor deposition (LPCVD) at high temperature or plasma enhanced chemical vapor deposition (PECVD) at low temperature. Compared to silicon, silicon nitride has low optical absorptions including most of the visible spectral range. Silicon nitride as core material provides a low index contrast system compared to silicon cores, which makes the performance of silicon nitride waveguides not as sensitive to the roughness of the sidewall as silicon waveguides. By fabricating high aspect ratio silicon nitride cores, the scattering loss due to sidewall roughness could be greatly reduced compared to silicon core, which leaded to several orders of magnitude lower in propagation loss, as low

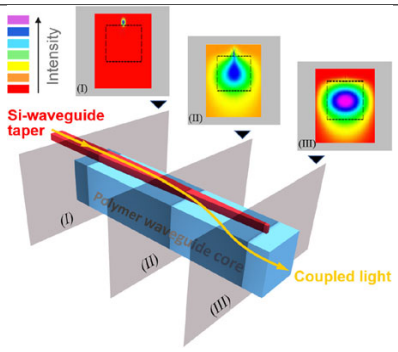
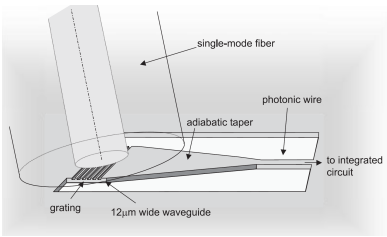
as 0.1 dB/m [14, 42]. Silicon nitride could be an alternative to silicon as the waveguide core material due to the extremely low propagation loss, but this is at the expense of lateral or vertical confinement owing to the low index contrast.

Silicon–germanium alloy has been drawing considerable attention in silicon photonics due to the capability of band gap engineering and lattice parameter engineering on the material. Germanium has a relatively high absorption at telecommunication wavelengths, and hence it is mostly used as a photodetector material but not a waveguide material. Germanium could enhance silicon's nonlinear response but it's at the expense of increasing propagation loss at telecommunication wavelengths. Silicon germanium as a waveguide core material does show low propagation loss at mid–infrared wavelength [43]. It could also be developed as modulators [44], photodetectors [45], and even on–chip light sources due to Raman scattering [18].

The propagation loss of waveguides in silicon photonics does not significantly impact the performance of the chip since the propagation length on a chip tends to be shorter compared to chip–to–chip or on–package interconnects. However, since the sizes of silicon–based cores are an order of magnitude smaller than the core sizes of SMFs or polymer–based SMWGs, direct coupling from silicon–based SMWGs to optical interconnects outside of the silicon photonic chip will cause up to 20 dB loss due to mode mismatch. Two major techniques to improve coupling efficiencies are spot size converters and grating couplers. A comparison table of these methods is shown in Table 2.1.

Spot size converters use adiabatic coupling to convert the spot size of the propagating mode confined in silicon to a relatively large mode comparable to SMF. Adiabatic coupling uses a tapered silicon waveguide to convert first–order mode propagating in the waveguide to higher–order modes or radiation modes, so when a polymer–based waveguide core is placed in close proximity of the tapered silicon core or in direct contact, light will be coupled into the polymer core, as shown in Table 2.1. The coupling loss between a silicon waveguide to a polymer waveguide could be less than 1 dB [46, 48]. Various designs for

Table 2.1: Comparison of two types of coupling for silicon–based SMWGs.

	Spot size converter	Grating coupler
Structure		
Couple to	SMWG	SMF
Coupling direction	Horizontal	Vertical
Coupling loss	0.5 dB	0.5 dB
Reference	[46]	[47]

spot size converters could reduce the coupling loss further down to 0.5 dB [49, 50]. Spot size converters could be then coupled to other SMWGs or SMFs.

Grating couplers are large periodic structures designed to couple waves or match phases in and out of the structure, as shown in Table 2.1. Grating couplers enable vertical coupling from silicon waveguides directly to SMFs unlike vertical coupling which requires couplers to be placed at the edge and polishing of facets. Vertical coupling is also beneficial to wafer–scale testing. However, grating couplers suffer from backscattering and enlarged mode compared to SMFs, which cause high coupling loss. Different designs and fabrication methods could lower the coupling loss down to 1–3 dB [51, 52]. By introducing metal mirrors in the structure, coupling loss could be significantly reduced to 0.5 dB [53].

2.2.2 Glass–Based SMWGs

Glass has been drawing attention as a promising candidate in optoelectronics packaging due to its low optical absorption coefficient at visible and telecommunication wavelengths, the composition of glass is similar to SMFs, and its panel–level processing capability. Chang-

ing refractive index of certain area of the glass could create index contrast between the area and its surroundings, which forms a waveguide in glass. Two popular techniques to modify refractive indices are laser writing and ion exchange. The former uses ultra–fast laser pulses to locally melt and recrystallize glass in a certain region so that the crystal structure and the concentration of glass components change in that area and its surrounding [54]. Laser–written glass waveguides could achieve extremely low propagation loss of 0.062 dB/cm [55].

Ion exchange to modify refractive index of a local area of glass has been studied for decades. The increase or decrease of refractive index is caused by two major effects, the size difference of the replacing and replaced ion, and the difference in electron polarizability of the two ions. Smaller ions replacing larger ions result in the collapsing of glass network, which in turn makes the area denser, and the refractive index larger. Ions with larger polarizability replacing ions with smaller polarizability increase the refractive index as well. Fraunhofer IZM developed a two–step high temperature ion exchange process to fabricate graded index SMWGs in glass, which has a low propagation loss of 0.059 dB/cm [24].

2.2.3 Polymer–Based SMWGs

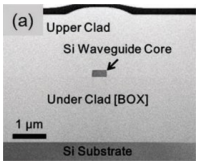
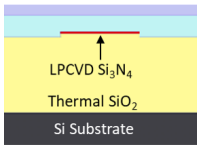
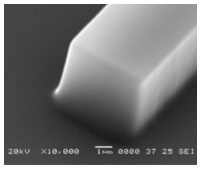
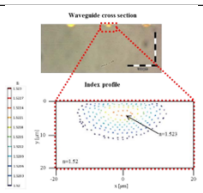
Conventional optical polymers like poly(methyl methacrylate) (PMMA), polystyrene (PS), polyurethane (PU), and epoxy resin have relatively low optical absorptions at visible wavelengths, but the loss at telecommunication wavelengths are not low enough for applications [56]. New polymer materials for SMWGs have been investigated and developed intensively but gradually slowed down a while ago due to various reasons. There are very few polymer materials available for SMWG fabrication nowadays. T. Ishigure [57] at Keio University developed a mosquito method to fabricate graded–index circular SMWGs with silicate–based organic–inorganic hybrid resins developed by Nissan Chemical. Graded–index single mode waveguides by mosquito method shows a relatively low propagation

loss of 0.29 dB/cm at 1310 nm and 0.45 dB/cm at 1550 nm. LFR series from ChemOptics show propagation loss of 0.1 dB/cm [58].

This thesis attempts to add knowledge in this area. The low loss waveguide materials used as cores and clads in this thesis are optical polymers from DuPont Electronics & Imaging, and glass will be used as bottom clad.

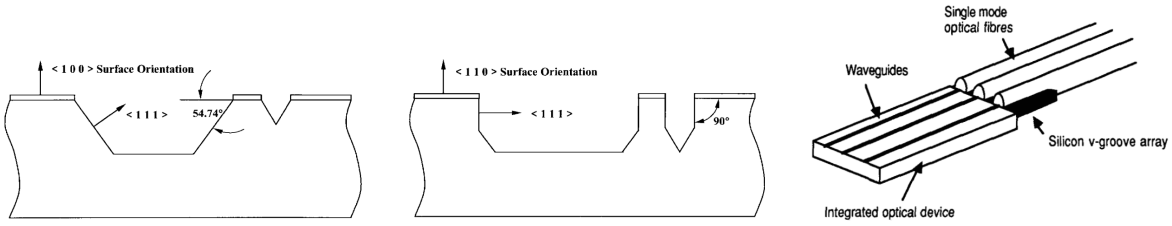
A comparison table of the different types of optical waveguide materials covered in this section is shown in Table 2.2.

Table 2.2: Comparison of different materials for SMWGs.

Material	Silicon	Silicon nitride	Glass	Polymer
Cross section				
R. I. @ 1550 nm	3.48	1.99	1.523 @ 678 nm	1.49–1.60
NA	3.15	1.35	0.1 @ 678 nm	0.1–0.6
Dimension	0.5 μm × 0.2 μm	3 μm × 0.05 μm	≥ 10 μm in diameter	4–8 μm square
Loss @ 1550 nm	0.5 dB/cm	0.05 dB/m	0.05 dB/cm	0.2–2 dB/cm
Process	SOI, RIE	LPCVD	Ion exchange	Photolithography
Coupling to fiber	Indirect	Indirect	Direct	Direct
Reference	[59, 60]	[61]	[62, 63]	[56]

2.3 High Precision Fiber Integration

Single–mode fiber–to–waveguide coupling has been challenging due to its small core size and tight alignment tolerance. Chou *et al.* simulated that in order to get less than 1 dB



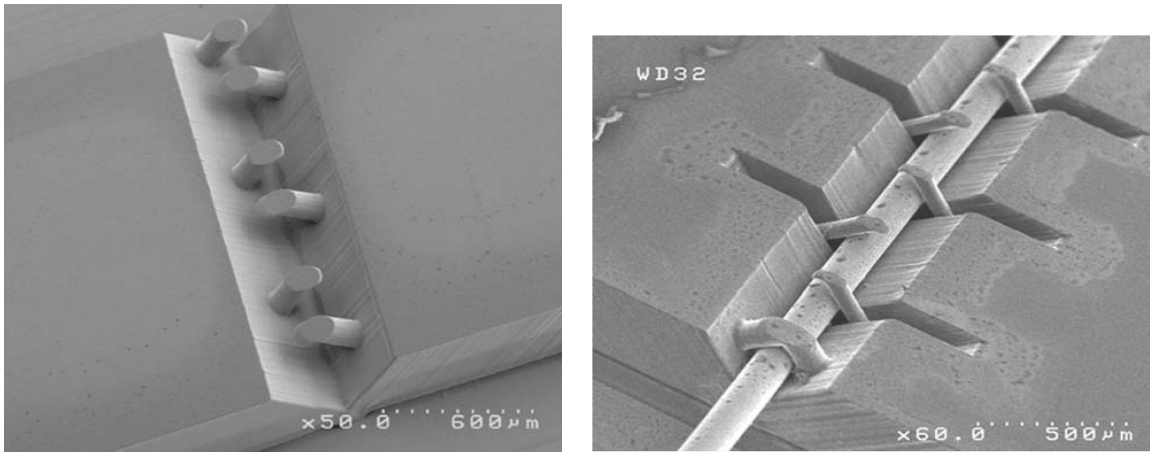
(a) **(b)** **(c)**

Figure 2.3: (a) Silicon v–groove on <100> wafer and (b) silicon v–groove on <110> wafer [64]. (c) Fibers in silicon v–grooves [65].

loss for fiber–to–waveguide coupling, there should be less than 1.5 µm offset in both x and y directions. In the z direction, the requirement is more relaxed, as in less than 30 µm, which is not a big challenge compared to other direction [25]. Many researchers have been working on fiber alignment techniques, but they are either high loss or high cost. There are two categories of fiber alignment techniques, passive alignment and active alignment. In passive alignment methods, alignment structures are fabricated so that once fibers are placed in the structure, the alignment will be achieved. However, in active alignment, a light source is launched into one side of the fiber, and a power meter is used to measure the coupling and the output of power from the coupled component, then a computer controlled micropositioner is used to adjust the position of the fiber until the lowest coupling loss is achieved. Passive alignment is low cost and fast, while active alignment is relatively slow but could achieve better coupling. Selected publications are summarized in this section.

2.3.1 Passive Alignment

The most implemented method to achieve fiber–to–waveguide coupling is to fabricated silicon v–grooves to confine the fiber in x and y directions due to the crystallinity of silicon. Strandman *et al.* [64] discussed the effect of different etchants on different types of silicon wafers. Due to the crystallinity of silicon and anisotropic etching, certain directions will be etched faster than others, which creates a v–groove shape, as shown in Figure 2.3. Wale *et al.* [65] fabricated silicon v–grooves to fix fibers in the trenches, and then used flip–



(a) **(b)**

Figure 2.4: (a) A polymer v-groove and (b) a polymer beam with fiber insertion [69].

chip assembly to integrate fibers and optical devices, and finally used melted solder balls to self–align the fibers to waveguides. Priyadarshi *et al.* [66] discussed the effects of attachment process parameters. After fibers are placed in the v–grooves, fiber location offsets will be affected by parameters like the amount of bulk adhesive, and symmetry of the adhesive layer. In order to achieve low cost and flexible fabrication, Lee *et al.* [67] developed a miniaturized machine tool with lead zirconate titanate (PZT) actuators for submicron resolution, three–axis positioning system using miniaturized stages for fiber holding. Moosburger *et al.* [68] took advantage of fabricating v–grooves and waveguides on the same silicon substrate where both of them being on the same substrate could be beneficial of the matching CTE.

Aside of silicon V–groove, researchers also used polymer to fabricate v–grooves. Kopp *et al.* [70] used SY–300 photoresist to form a dry film lamination, cured it with UV light, and developed it. Ling *et al.* [69] used SU–8 and inclined exposure to make a polymer v–groove, and they also made cantilever beams to confine location offset of fiber in x and y directions as shown in Figure 2.4.

V–grooves are an effective way to fix fibers within certain requirement. Other approaches were also investigated like modifying fibers in order to get a high accuracy align-

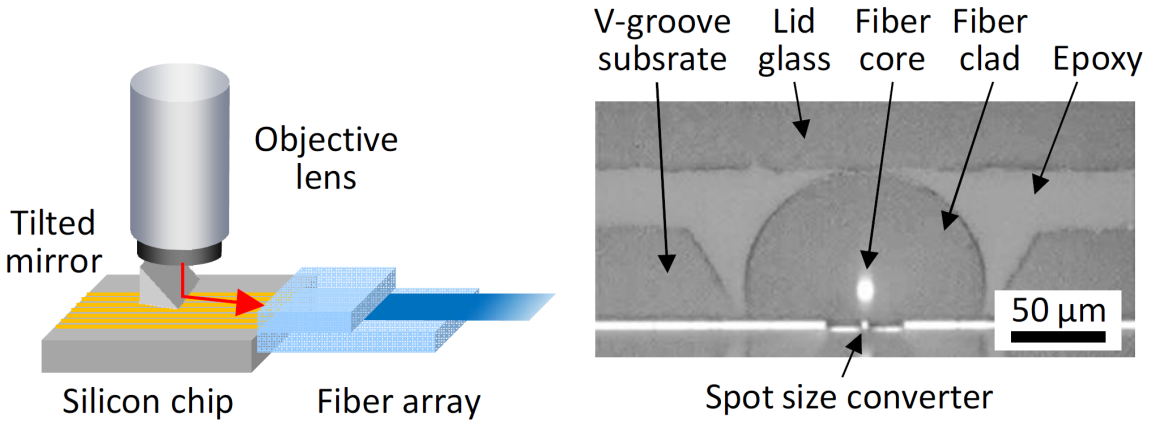


Figure 2.5: (a) Configuration diagram of core monitoring method and (b) an microscopic image of the alignment [73].

ment. Barry *et al.* [71] used a D–shaped fiber instead of a traditional cylindrical fiber, which makes alignment much easier when putting it in the alignment structure. D-shaped fibers were made by cleaving the lapped SMFs and polishing end faces. Rashidi *et al.* [72] also modified the fiber to get a better coupling efficiency. They cleaved the cladding part of the fiber butt into a cone shape, then polished the end face, and fixed it in a silicon v–groove. They achieved 1.1 dB loss using this technique.

Besides various methods to fabricate v–grooves, alternatives have also been developed for passive fiber alignment. Henzi *et al.* [74] developed a mold to achieve low cost fabrication and manufacturability, and used deep UV light to modify PMMA as the waveguide core and clad, so that the fiber alignment structure and a trench for the waveguide core were fabricated at the same time. Another method which falls between active alignment and passive alignment is called direct core monitoring [73]. This method, unlike active alignment which uses a photodetector or power meter, uses human eyes to monitor the alignment through microscope, as shown in Figure 2.5.

2.3.2 Active Alignment

Active alignment is a wildly used method to couple SMFs to waveguides or photonics integrated chips. Active alignment means transmitting a beam of light into the fiber and detecting the intensity of the beam at the other end. The fiber faces the waveguide, but it moves a small step in a certain time. When the maximum intensity is detected, the positions of the fiber and the waveguide are fixed with techniques like optical epoxy, or laser jointing. The issue with active alignment is that it's time consuming, and it's expensive, although scanning algorithms to speed up the process have been developed to lower the cost.

2.4 Summary

The first half of this chapter focused on the development and the most recent achievement in microvia fabrication. Microvia technologies have not been progressing as fast as scaling down the size of routing wires and spaces, but microvias are needed for high density electronic interconnects. Photolithography and laser ablation were compared for microvia fabrication.

SMWG materials for high density optical interconnects were reviewed and summarized in the second half of this chapter. Silicon–based SMWGs are compatible with the silicon photonic platform but they need to be coupled to other types of SMWGs on the package, and they are not suitable for on–package communications. Glass–based SMWGs and polymer–based SMWGs are both good candidates for on–package communications, and they are also capable of directly coupling to fiber. Fiber integration techniques were then covered in the next section. Despite the high cost the time–consuming process, active alignment is still prevalent for single mode optics.

CHAPTER 3

ULTRA–FINE ELECTRONIC INTERCONNECTS

This chapter describes the research on high density ultra–fine electronic interconnects for high data rate communications including routing wires in the horizontal direction and microvias in the vertical direction.

As the critical dimension of transistors moves towards 7 nm and below, chips with more computing power enable the development and application of AI, VR, and cloud computing, therefore the demand for high data rates continues to grow. However, such small features are reaching the physical limits, and as a result, the Moore's law hasn't progressed as predicted. The focus of the industry has shifted to the packaging side to continue driving the post–Moore's law on the system. As discussed before, even though optical interconnects are a good candidate for long–distance telecommunications, the high costs and additional system complexity prohibit the application of them for on–package or even chip–to–chip communications. Electronic interconnects via copper traces and vias still dominate communications between two chips in close proximity. RDLs which include fine copper traces and microvias are a key technology to increase packaging interconnect density. Increasing I/O density by shrinking the size of routing wires, spaces, and microvias for RDLs on a package has become the critical approach in academia and the industry.

A typical RDL configuration is shown in Figure 3.1. The pitch of vias is P, the landing pad or capture pad diameter is D, and the via size is d. The widths of routing lines and spaces are L and S, respectively, and n is the number of routing wires in a pitch.

Based on the configuration, we have

$$P = \frac{D}{2} + n \times (L + S) + S + \frac{D}{2} \tag{3.1}$$

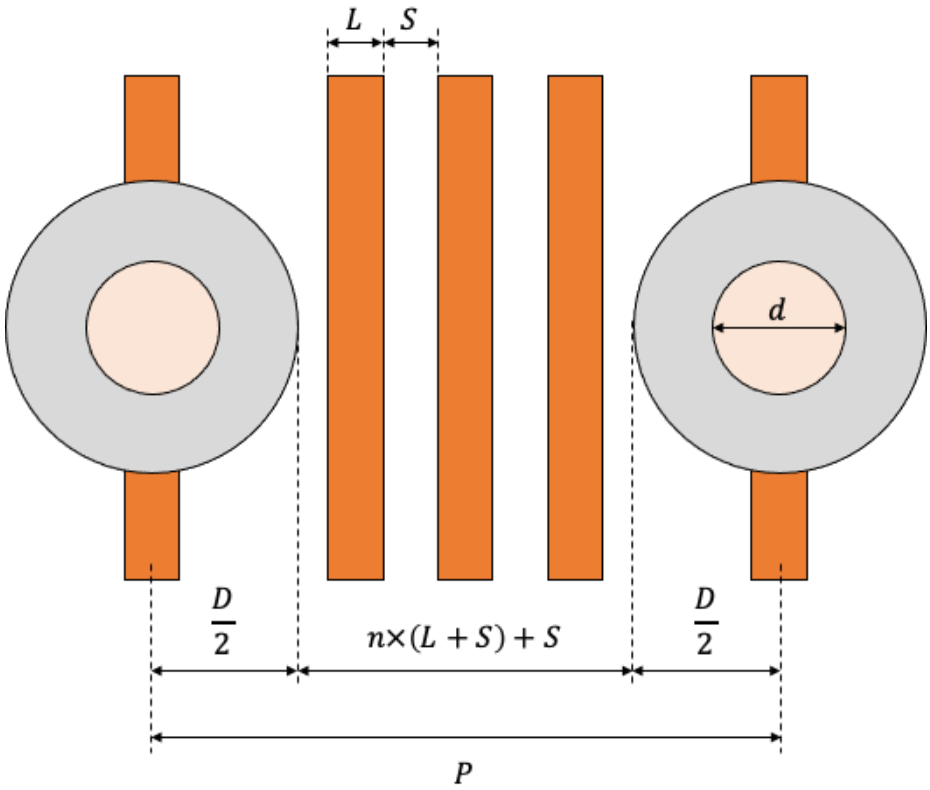


Figure 3.1: Electronic interconnect density parameters in a typical RDL configuration.

To pursue the maximum density with the current fabrication capacity, $L = S$ is usually assumed. Then we have

$$P = D + (2n + 1) \times L \tag{3.2}$$

$$n = \frac{1}{2}\left(\frac{P - D}{L} - 1\right) \tag{3.3}$$

The I/O density, in the unit of I/O/mm/layer, is defined as

$$\text{I/O density} = \frac{1000(n+1)}{P} = 1000 \times \frac{1}{2}\left[\left(1 - \frac{D}{P}\right) \times \frac{1}{L} + \frac{1}{P}\right] \tag{3.4}$$

where D, P, L are in microns. Since P is proportional to and always larger than D, it could be confirmed that to pursue higher I/O density, one can either reduce the size of the routing wires, or the size of the vias. The industry has been pursuing ultra-fine routing wires

intensively, but has not progressed on small microvia fabrication as much, so now microvias are the limiting factor of increasing I/O density. The current I/O density of the traditional multi–chip packaging is on the level of several tens of I/O/mm/layer and the minimum pitch is about 40–50 µm. With the development of high data rate demanding applications, the I/O density needed will be in the order of hundreds or thousands of I/O/mm/layer. In an extreme case where $L = S = d = D = 1\,\mu\mathrm{m}$ and $P = 20\,\mu\mathrm{m}$, we have

$$\text{I/O density} = \frac{1000(n+1)}{P} = 500 \tag{3.5}$$

This is the current goal of the industry, however, there are many challenges to achieve 1 µm lines or spaces, or microvias with 1 µm diameter.

For lines and spaces, 1 µm is achievable using BEOL technologies on silicon traditionally used in chip fabrication processes in wafer foundries. The I/O density of silicon interposers could be 1000 I/O/mm/layer and higher. The application of silicon interposers is limited mainly by the cost of the semiconductor BEOL process. On the other hand, organic interposers used in substrate foundries use SAP to form routing wires and microvias, but the I/O density on organic interposers is limited by seed layer etching, surface planarity, and other issues. There is a need to develop a new technology to close the gap between the organic interposers and silicon interposers at a reasonable cost, which is the work in this chapter. Both the development of ultra–fine routing wires and small microvias for high–density I/O will be presented in detail in this chapter.

3.1 Horizontal Interconnects: Routing Wires

Photolithography is widely used in packaging industry due its relatively low cost, simplicity of use, and effectiveness on precise patterning. It is also used in fabricating routing wires in RDLs.

3.1.1 Photolithography on Routing Wires

There are two types of photolithography tools used in the packaging industry: proximity or contact mode, and projection mode. In the proximity or contact mode exposure system, a collimated UV light usually generated by a mercury lamp with a broad spectrum, or filtered UV light at g–line (435 nm), h–line (405 nm), or i–line (365 nm), is used to expose the photosensitive material on the substrate. This type of exposure tools has been dominating in fabricating package substrates and printed wiring boards for a long time. The photomask is placed on top of the substrate being exposed, with a very small gap in the proximity mode, which in turn limits the resolution of the patterning due to the diffraction of the light in the gap after the photomask. Generally speaking, a pattern with a feature size of 10 µm could be resolved in a high–resolution dry film photoresist laminated on the substrate with a polyethylene terephthalate (PET) film on top and a gap less than 60 µm [75]. However, if 1–2 µm features are being pursued, the proximity mode photolithography tool is not sufficient and the photomask has to be in direct contact with the substrate, which is called the contact mode. In a contact mode exposure system, the photomask is placed on top of the sample with a vacuum system to help reduce the gap in between. Since the ultra–fine routing wire patterns are close–spaced periodical blocks which to the UV light serves as a diffraction grating, and the feature size (1 µm) is close to the wavelength of the light (365 nm), a Fresnel number is calculated to determine which type of the simulation suits the contact mode exposure to investigate the impact of the size of the gap on the diffracted UV light pattern. The Fresnel number is defined as

$$F = \frac{a^2}{L\lambda} \tag{3.6}$$

where a is the characteristic size of the aperture, which is 1 µm, L is the distance of the screen from the aperture, which is the gap between the mask and the substrate, and λ is the incident wavelength 365 nm. With the vacuum system in the contact mode exposure tool,

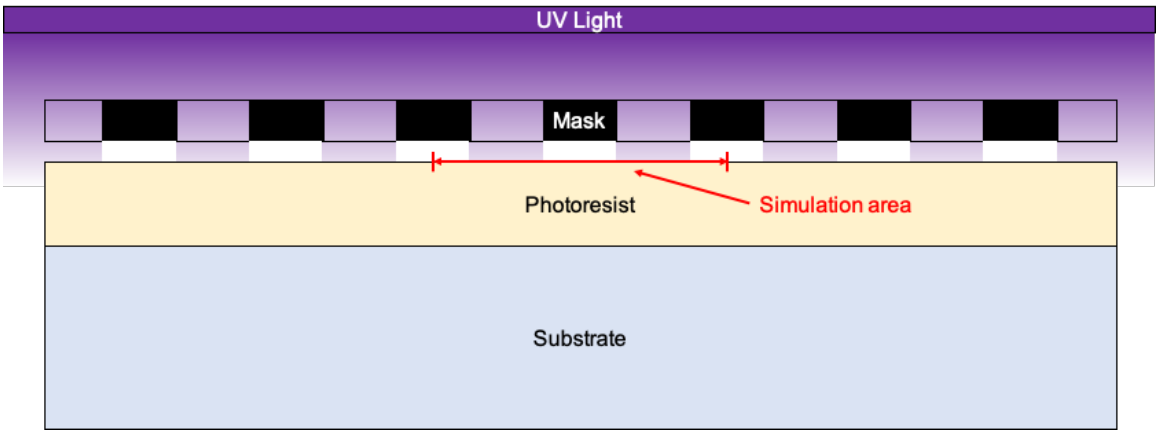


Figure 3.2: Schematic of a 2D diffraction grating in the contact mode exposure tool for near–field Fresnel diffraction simulation.

the gap is well below 10 µm, which brings the Fresnel number in Equation 3.6 to around 1 and beyond, so the near–field Fresnel diffraction could be used to estimate the impact of the gap on the patterning resolution.

To simplify the simulation, a 2D diffraction grating is used in the near–field Fresnel diffraction simulation in MATLAB, as shown in Figure 3.2. The electric field and the intensity pattern after the masks at the surface of the photoresist is calculated.

The electric field from light propagating through one aperture is given by

$$E(x) = \frac{E_0}{i\lambda} \int_{-\frac{1}{2}}^{\frac{1}{2}} \frac{e^{\frac{i\times 2\pi}{\lambda}\sqrt{(x-x')^2+h^2}}}{\sqrt{(x-x')^2+h^2}} \mathrm{d}x' \tag{3.7}$$

where E_0 is the electric field intensity in the mask, x' is the position of in the aperture, and h is the gap between the mask and the photoresist. Since the dimension of the mask is five orders of magnitude larger than the feature size and the flood exposure has same intensity in the mask area, the electric field calculated in Equation 3.7 could be applied to any aperture in the mask. The line width and the size of the space are both set to 1 µm, the gap is from 0.1 µm to 3 µm so that the near–field Fresnel diffraction is accurate for the simulation. By combining all the electric fields from 20 apertures in the mask, the normalized intensity of the 4 µm simulation area in the middle of the mask with different gap sizes were calculated

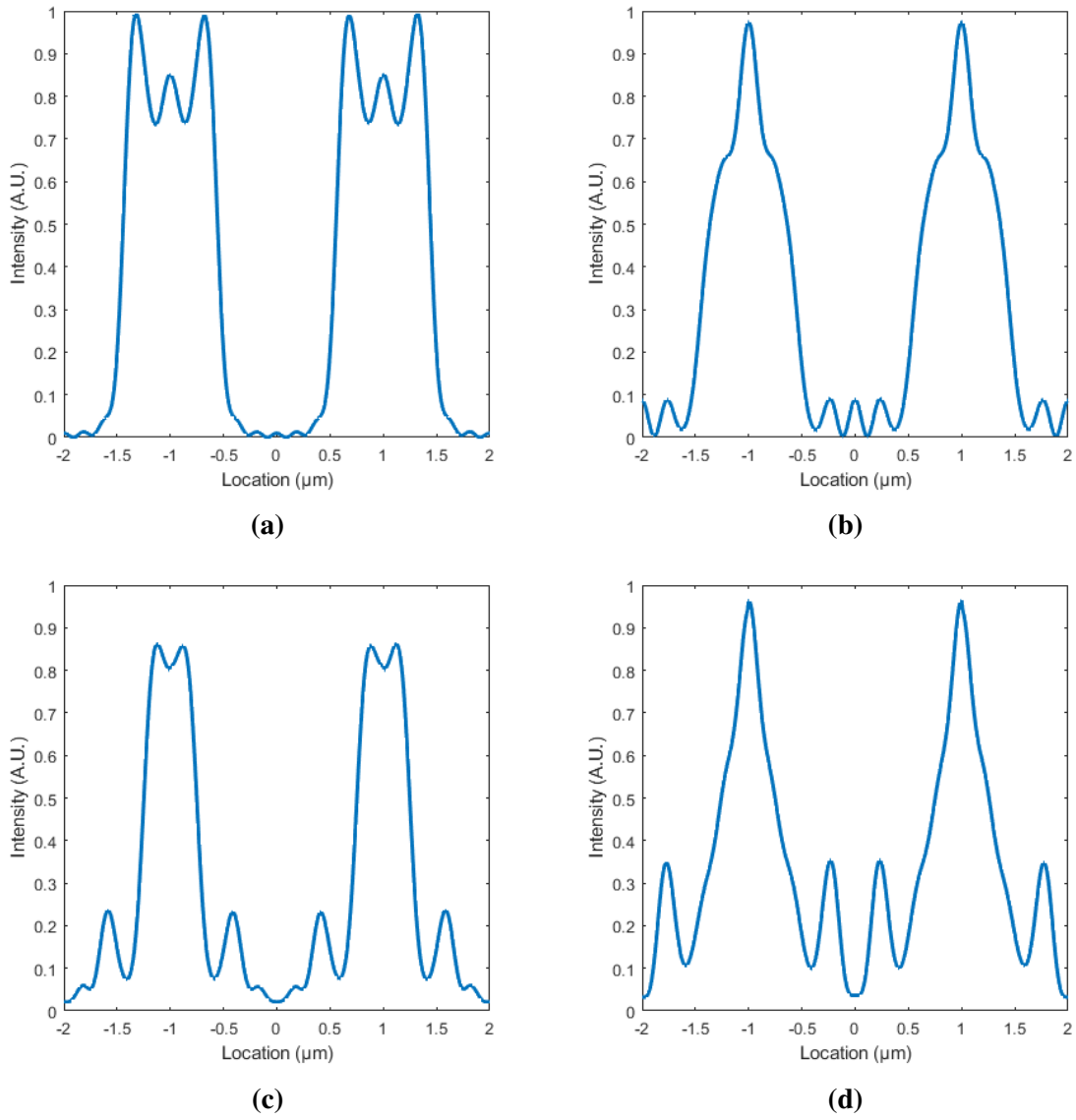


Figure 3.3: Diffraction patterns after the photomask with a gap of (a) 0.1 μm, (b) 0.5 μm, (c) 1.0 μm, and (d) 3.0 μm.

and presented in Figure 3.3.

When the gap between the mask and the photoresist is 0.1 μm, two exposure patterns are clearly separated as shown in Figure 3.3(a). When the gap is 0.5 μm as shown in Figure 3.3(b), by selecting proper exposure dose, two patterns could still be resolved. However, when the gap is 1.0 μm, it's challenging to resolve 1 μm features due to the intensity peaks on the side from diffraction as shown in Figure 3.3(c). When the gap is 3.0 μm, 1 μm

features could not be resolved based on the simulation result shown in Figure 3.3(d). When the gap is beyond 5.0 μm, near–field Fresnel diffraction is not suitable for the simulation anymore. It also could be concluded that the gap has a huge impact on the finest feature that could be resolved in a contact mode photolithography tool. It's very challenging to achieve 1 μm features in a proximity or contact mode exposure system.

Another type of the photolithography tools widely used in the industry is the projection mode exposure system. Unlike the proximity or contact mode, the mask is close to the light source and far away from the sample in a projection mode stepper. The advanced and complicated optical system in a projection stepper makes the tool superior in resolving finer features with a higher cost compared to the proximity or contact mode exposure system. However, resolution is not the only goal of high–density interconnects. Finer routing wires with the same height will result in a higher resistance, a higher inductance, a lower capacitance, a lower conductance, and a higher characteristic impedance. When the density per layer is increased by reducing the width of routing wires, the height needs to be simultaneously increased as well to match the impedance and other electronic characteristics, so high aspect ratio ultra–fine routing wires are desired for high–density interconnects. The two main criteria to pursue high–density interconnects with proper electrical performance include higher (or smaller) resolution and higher depth of focus (DOF).

In a photolithography system, the resolution is calculated by

$$R = \frac{k_1 \lambda}{NA} \tag{3.8}$$

and the DOF is defined by

$$DOF = \pm \frac{k_2 \lambda}{NA^2} \tag{3.9}$$

where k_1 and k_2 are constants related to the material and the process, λ is the wavelength of the light, and NA is the numerical aperture (NA) of the optical system. DOF is a concern since the light behaves like a Gaussian beam after complex optical system in the projection

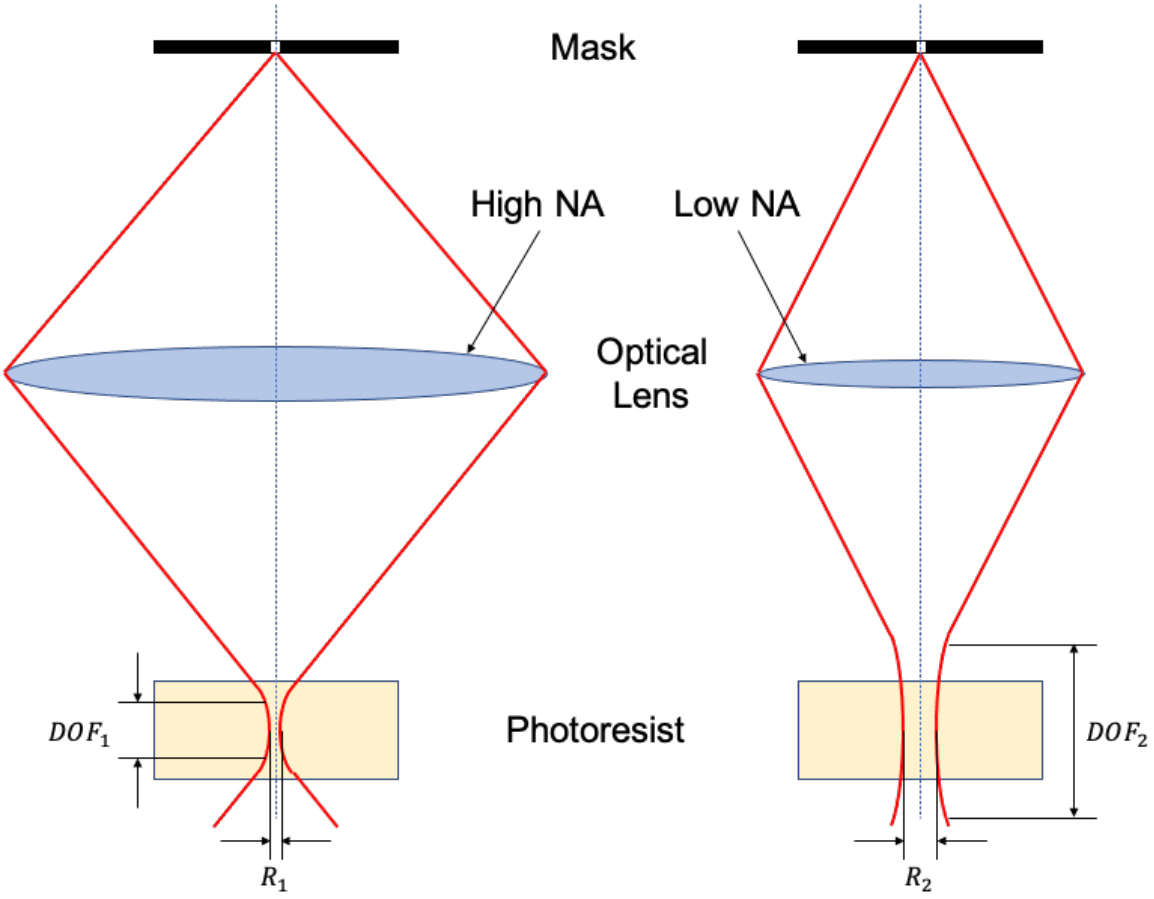


Figure 3.4: A schematic of the impact of NA on the resolution and DOF.

system. The density of interconnects in a layer has always been a priority over the density in the vertical direction due to two reasons. First, the size of the chips is limited, so the interconnect density has to match the pin density on a chip. Second, the DOF is never an issue for larger feature sizes. However, the density of interconnects required nowadays is higher, so the feature size on a package has to be smaller as well. Based on Equation 3.8, a higher resolution or a smaller feature size requires a shorter wavelength, and a higher NA. For smaller feature sizes, higher aspect ratio is required to meet the electrical design rules. However, shorter wavelengths and larger NAs will lead to smaller DOF, which is against the purpose to achieve higher DOF.

In advanced photolithography tools, a wavelength of 365 nm is commonly used in packaging applications. A numerical aperture from 0.1 to 0.6 is widely used but a NA on the

lower end is preferred due to its relatively low cost. The impact of NAs on the resolution and the DOF is shown in Figure 3.4. Since the light through an optical system behaves like a Gaussian beam, the small feature on the mask won't be exactly transferred to the photoresist. A higher NA can focus the beam with a smaller beam width, which is proportional to the resolution of the system, but the DOF becomes smaller as well. With a lower NA system, the resolution is bigger and the DOF follows the same trend. Since the system in a projection mode photolithography tool is fixed, changing the wavelength or the NA is not possible. Developing new materials with a lower k_1 and a higher k_2 is a viable approach for high resolution patterning in a relatively thick film. However, development of new materials is beyond the scope of this thesis, so it won't be discussed further.

3.1.2 SAP for Routing Wires

The SAP is the process of record for RDL fabrication. Photolithography is used in this process to define the opening of the photoresist and subsequently the width of the copper routing wires. A schematic of SAP is shown in Figure 3.5. The details of SAP are as follows.

1. **Seed layer deposition.** A thin layer of titanium and copper was deposited on top of the substrate as a conduction layer for the plating process later in the process.

2. **Photoresist application.** Either a dry film photoresist was laminated on the seed layer, or a liquid photoresist was spin coated on the seed layer.

3. **Photolithography.** Once the photoresist was applied on top of the seed layer, the sample underwent exposure and development so that the trenches in the photoresist were open for copper wire formation.

4. **Electrolytic plating.** After the photoresist was patterned and developed, the seed layer was exposed to the atmosphere. The substrate was then placed in a plating bath

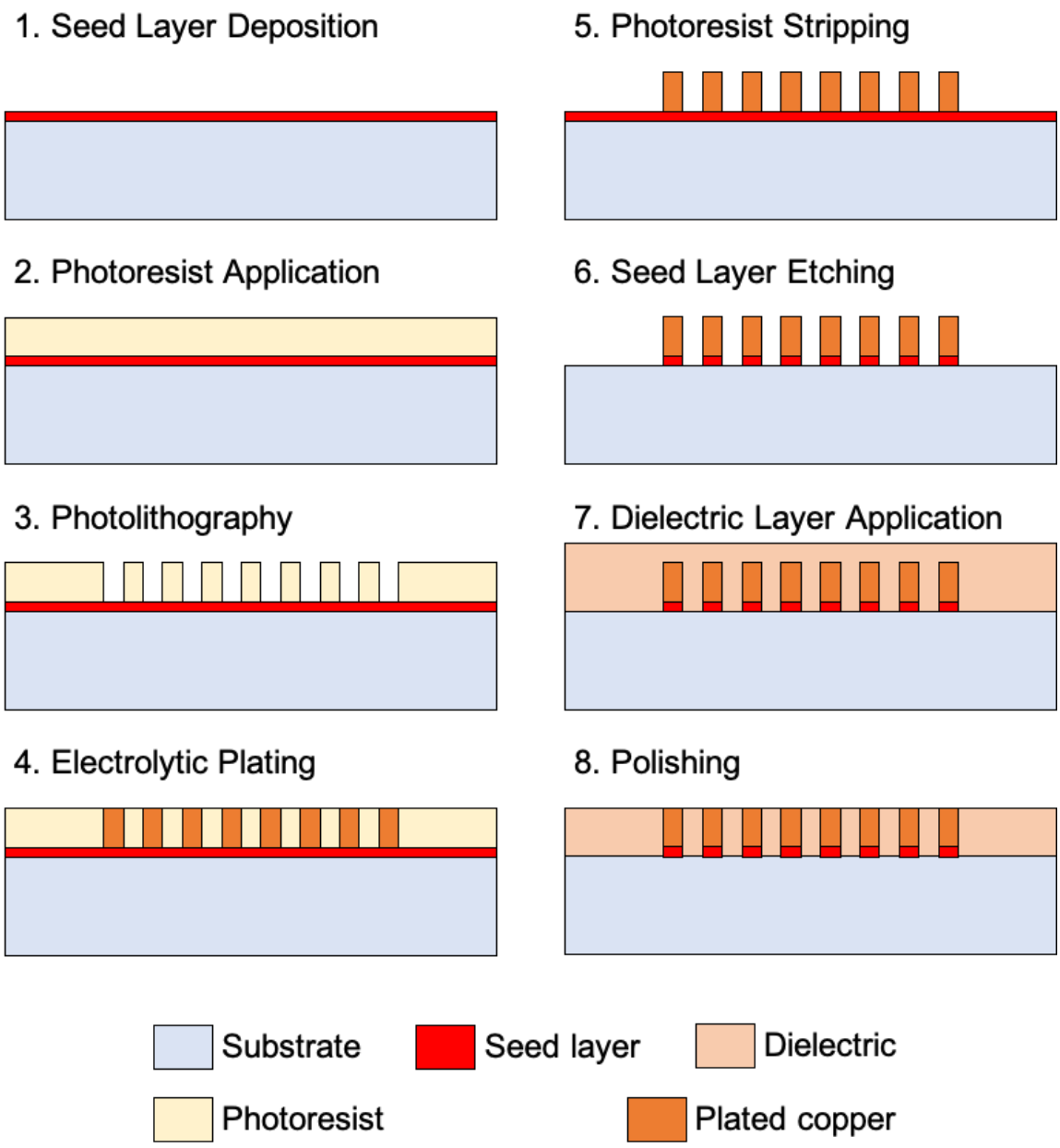


Figure 3.5: A schematic of SAP.

and the seed layer was connected to a cathode, so that the copper would be plated in the trenches in the photoresist to form routing wires.

5. **Photoresist stripping.** Once the electrolytic plating was done, the photoresist was removed, and the whole seed layer without the plated area was exposed to the atmosphere.

6. **Seed layer etching.** The seed layer was etched off to remove the short circuits between routing wires using either dry etching or wet etching. Surfaces of the routing wires would also be etched slightly in this process.

7. **Dielectric layer application.** After routing wires were formed and electrically isolated, the whole substrate was then covered by a dielectric film to meet the electrical and mechanical requirements for the RDL stack–ups.

8. **Polishing.** Since the dielectric layer was completely covering the routing wires, excessive polymer as removed so that the routing wires were exposed to the atmosphere. Then it was ready for the next set of processes.

In the seed layer etching process, both wet etching and dry etching would remove some of the copper on the sidewalls and the tops of the fabricated routing wires. Assuming the thickness of the seed layer is 200 nm, completely removing the seed layer will result in the reduction in the line width of fabricated routing wires by 0.4 µm. This is not an issue for the much wider routing wires, but it will be a huge challenge for ultra–fine wires since it is 20% of the line width for 2 µm wires, and even 40% reduction in 1 µm wires.

As the line width of routing wires is scaled down to 1 µm, the contact area of the wires to the substrate shrinks as well. Such a small contact area together with the high aspect ratio design will introduce mechanical issues due to low bonding strength. The thinning of the wires caused by seed layer etching worsens the situation as well. The subsequent processes like dielectric layer application might easily break the bonding between the routing wires to the substrate, which invalidates the sample. For small feature sizes, traditional SAP faces issues like sidewall etching and low bonding strength, so sidewall protection or a new fabrication process are needed.

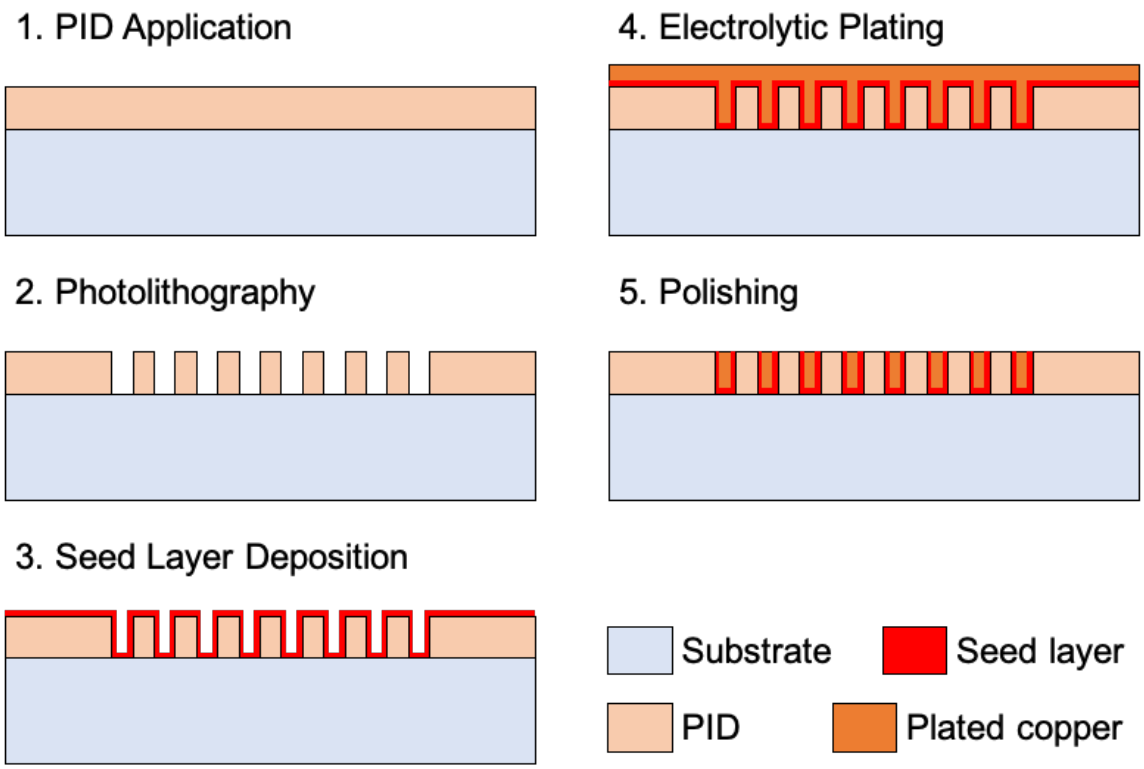


Figure 3.6: A schematic of the embedded trench method.

3.1.3 Embedded Trenches for Routing Wires

Embedded trenches are a newly developed technology to achieve ultra–fine routing wires without facing the issues from SAP. The process is shown in Figure 3.6, and the details are described as follows.

1. **PID application.** PIDs are a photosensitive dielectric liquid or dry films with low dielectric constant. The PID material was either laminated (for dry films) or spin coated (for liquids) on the substrate.

2. **Photolithography.** Like in SAP, the photosensitive material was exposed and developed to form trenches for routing wires.

3. **Seed layer deposition.** Instead of depositing the seed layer directly on top of the substrate, the seed layer in the embedded trench method was deposited on top of the

patterned PID. Since the physical vapor deposition (PVD) was used in this process, the coverage of the seed layer on the patterned features would be conformal.

4. **Electrolytic plating.** The seed layer was connected to the cathode in the plating bath, and copper was plated on top of the seed layer.

5. **Polishing.** Since the copper grew out of the trenches and completely covered the surface, excessive copper were removed by chemical mechanical polishing or fly cut until the plated copper on top of the dielectric surface was completely removed. Then the sample was ready for the next sets of processes.

Photoresists are not used in the embedded trench method, so photoresist application and photoresist stripping are removed from the process compared to SAP. It also completely resolves the issue of sidewall etching in SAP since the seed layer etching process is no longer needed in this method. By using PIDs instead of photoresists for fine feature patterning, the complexity of the process could be greatly reduced compared to SAP. However, the embedded trench method is limited by the resolution of the PIDs, and the availability of the PIDs.

CYCLOTENE^{TM} 6505 is used in the development of embedded trenches for ultra–fine routing wires. It has a good thermal stability without outgassing in the cure process which improves the photolithography performance. The process of using CYCLOTENE^{TM} 6505 is listed in Table 3.1. The detailed development and the optimization of the process will be discussed in Chapter 4.

Since the cured CYCLOTENE^{TM} 6505 ridges and trenches have a sidewall angle of 70°, the maximum aspect ratio of polymer lines by photo–patterning on this material is 1.5:1. To decrease the line width and increase I/O density, the spin speed of 2500 round per minute (RPM) is used instead of the regular 1250 RPM to reduce the thickness of the coated film. Cross sections of the patterned PID layer are shown in Figure 3.7.

Figure 3.7(a) is a top view of the patterned PID. The bright area is exposed and devel-

Table 3.1: Embedded trench fabrication process with CYCLOTENE™ 6505.

Process	Step	Condition
Glass substrate cleaning	Plasma clean	O_2, 100 W, 100 °C, 10 min
	Solvent clean	Acetone, methanol, IPA, DI water rinse, N_2 dry
	Drying	150 °C, 5 min
Surface activation	Adhesion promoter AP9000c application	2000 RPM, 45 s
	Bake	150 °C, 1 min
Waveguide core patterning	CYCLOTENE™ 6505 application	2500 RPM, 45 s
	Soft bake	90 °C, 90 s
	Post coat delay	15 min
	Exposure	400 mJ/cm^2
	Post exposure delay	15 min
	Development	0.14 N TMAH, immersion with gentle agitation, 60 s, immersion in DI water, 120 s
Cure	Thermal set	75 °C, 120 min
	Thermal cure	Soft cure: 200 °C, 100 min Hard cure: 250 °C, 10 min
	Descum	4:1 O_2:CF_4, 100 W, 100 °C, 10 min

oped trenches for the formation of copper routing wires, and the grey area is the dielectric remaining on the substrate. In this figure, the line width as small as 2 µm is opened. Then a 150 nm copper seed layer was deposited on top of the patterned PID. The cross–sectional images on the side are shown in Figure 3.7(b) and Figure 3.7(c) indicate that 3.0 µm and 3.5 µm features are fully resolved and isolated, however, the polymer ridges separating trenches of 2.0 µm and 2.5 µm become smaller, and gradually lose the top width due to

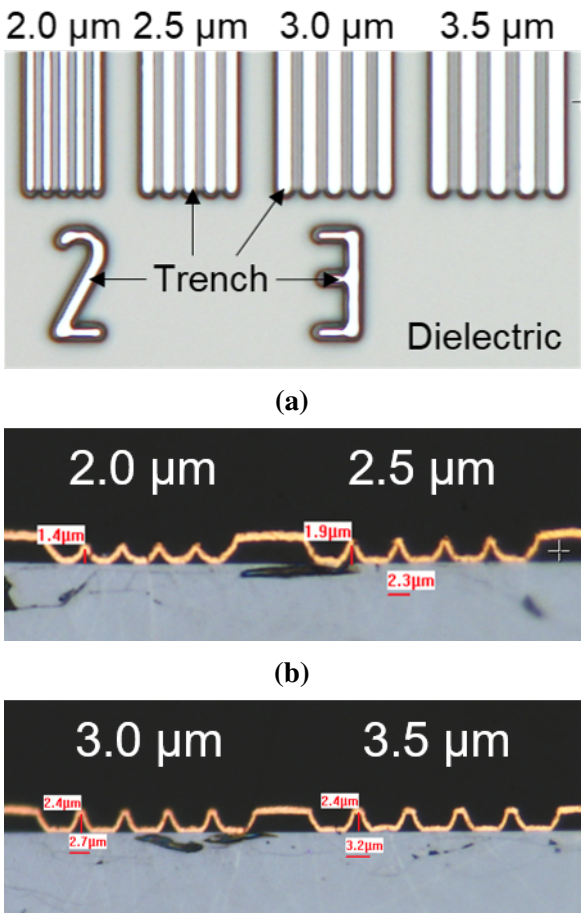


Figure 3.7: (a) Top view of dielectric lines and trenches. (b) Cross–sectional image of 2.0– and 2.5–µm 1:1 line and space structure after copper deposition. (c) Cross–sectional image of 3.0– and 3.5–µm 1:1 line and space after copper deposition. © 2020 IEEE

the side wall angle. In this sample, the thickness of the PID film is about 2.6 µm, and the smallest opening achieved in this film is 3.0 µm. The theoretical minimum opening based on calculation from the sidewall angle is 2.0 µm.

3.2 Vertical Interconnects: Microvias

The scaling down of routing wires has been pursued and developed well, however, the shrinking of microvias has not been progressed in the same way. A chart published by Intel [76] on the requirement of substrate features in terms of the size of lines, spaces, and mi-

crovias indicates the revolution from next–generation 2D packaging to the next generation 2.5D enterprise computing will be only on the via size from 8 µm down to 2 µm and the requirement for lines and spaces remain the same. Microvias are critical in the continuous scaling of the substrate package and the increasing of I/O density.

There are three methods to fabricate microvias, photolithography, plasma etch, and laser ablation. As described in the previous section, using photolithography to fabricate microvias is similar to using photolithography to fabricate routing wires. Photosensitive materials are exposed to UV lights and developed away to create cavities in the layer, which subsequently is plated with copper for form vertical interconnects. However, the fabrication of the microvias is more difficult than the fabrication of routing wires with a line width equal to the diameter of microvias since the feature size is getting close to the wavelength used in the photolithography exposure system, and the diffraction happens at the bottom surface of the mask. When the line width is the same as the diameter of the microvias on a photomask, the microvias required higher exposure dosage than the routing wires. The PID material used in ultra–fine feature patterning is usually a positive–tone material, which is the case in this study. If the pattern of routing wires is perfectly resolved, microvias might not be fully opened. If the microvias are fully resolved, trenches for routing wires might be too big. Photolithography is a great candidate for microvia fabrication together with other features, however the drawback of this method is the limited availability of the high resolution PID materials and their costs.

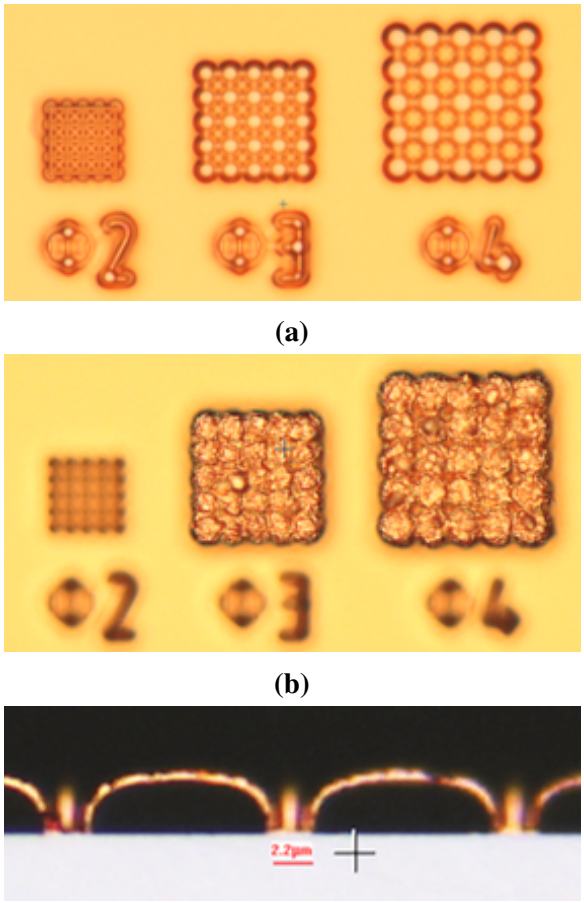
Plasma etch is another method to fabricate microvias. Similar to the process of photolithography, plasma etch is a parallel process in which all microvias are fabricated at the same time. A mask is required to fabricate microvias as well. However, due to the isotropic nature of the plasma etch process, the diameter of microvias fabricated using plasma etch could achieve as small as 40 µm. The capability of small microvia fabrication and the expense of the tool severely limit the wide application of plasma etch on microvia fabrication. This method will not be further discussed in this thesis.

Laser ablation is the third method to fabricate microvias. Lasers for ablation purpose usually have a small spot size, and an extremely high peak intensity, so they could potentially ablate any polymers. The abundance of the material suitable for laser ablation is its huge advantage over photolithography. Different types of lasers have been developed for via fabrication. CO_2 and UV lasers were rapidly developed in the late 1990s to ablate openings for microvias. CO_2 and UV laser work at different wavelengths. CO_2 lasers emit infrared beams of wavelengths in the range of 9.3 µm to 10.6 µm, and UV lasers typically use 355 nm light sources. Unlike plasma etch or photolithography, CO_2 and UV laser ablation is a serial process, which means the formation of microvias is one via at a time. However, the repetition rate of laser pulses and the fast movement of the galvo system for laser positioning have been greatly improved from 5–20 vias per second in 1995 to thousands of vias per second [32]. Excimer lasers have shorter wavelengths than UV lasers and microvia formation by excimer lasers is a parallel fabrication process like photolithography. A mask is required to protect the not–to–be–drilled area on the substrate. It has the capability to fabricate microvias as small as 5 µm, but the maintenance and the cost of the tool are huge concerns for mass production.

The progress on microvias fabricated using photolithography will be briefly discussed here and more detailed contents can be found in [77]. The rest of the chapter will focus on basics of laser ablation and microvias fabricated using laser ablation, which is an extended version of [32, 78].

3.2.1 Microvia Fabrication by Photolithography

CYCLOTENE^{TM} 6505 is used for microvia fabrication. First a seed layer of 50 nm titanium and 150 nm copper was sputtered on the glass substrate. Then the photosensitive dielectric liquid CYCLOTENE^{TM} 6505 was spin coated on a glass substrate at 2500 RPM, patterned and developed in tetramethylammonium hydroxide (TMAH), and cured in the nitrogen oven. By increasing the spin speed from 1250 RPM in the process of record to 2500 RPM,



(a)

(b)

(c)

Figure 3.8: 2–, 3–, and 4–µm microvias with 4–, 6–, and 8–µm pitch, respectively, (a) before and (b) after copper plating. (c) Cross–sectional image of 2–µm microvias with 12.5–µm pitch. © 2020 IEEE

the thickness of the film coated on the substrate were greatly reduced from 6 µm to 2.6 µm. Microscopic images of fabricated microvias are shown in Figure 3.8.

Figure 3.8(a) presents a top view of the sample after cure but before copper plating. The microscope used to capture the image was focused on the bottom opening of the microvias. It is clear that with this thickness, 3 and 4 µm microvias are fully opened, but the conclusion couldn't be drawn for 2 µm microvias. Figure 3.8(b) shows the top view of the sample after copper plating. Copper was fully plated from the seed layer in 3 µm and 4 µm microvias but there's no copper in 2 µm region, which indicates that 2 µm microvias were not open. Since the space between microvias in Figure 3.8(a) and Figure 3.8(b) are the same as the

diameter of the microvias in each region, 2 µm microvias were not open possibly due to the density of the microvias. By increasing the pitch of 2 µm microvias from 4 µm to 12.5 µm, microvias were fully opened as shown in Figure 3.8(c).

3.2.2 Fundamentals of Laser Ablation for Microvias

Ablation on polymer materials by UV lasers is usually achieved by photochemical and/or photothermal reactions. The photochemical reactions are chemical reactions caused by photons interacting with the material. The photon energy of UV lasers at 355 nm is given by

$$\epsilon = \frac{hc}{\lambda} \tag{3.10}$$

where h is the Planck constant, c is the speed of light in vacuum, and λ is the wavelength of the photon. The energy of a photon of 355 nm is 5.6×10^{-19} J corresponding to 3.49 eV, which is much higher than a photon from CO_2 laser, 0.21 eV. Such high energy photons could potentially break covalent bonds in the polymer chains so that the material will break down, which is the photochemical reaction. The photothermal reaction is the liquification or vaporization of the material due to thermal effects of the photon–material interactions. The UV laser tool used in this study has a maximum output power of 16 W, and the beam size is around 8 µm. So, the average beam intensity when the laser operates at the maximum output power is

$$I = \frac{P}{\pi D^2/4} = 3.18 \times 10^{11}\,\mathrm{W/m^2} \tag{3.11}$$

where P is the power of the laser, D is the diameter of the beam. Such high intensity in laser beam could potentially heat up the material very quickly to the point where the material is liquified or even vaporized in a short period of time, leading to a photothermal reaction. Photochemical and photothermal interactions are two possible explanations, but the fundamental mechanism of laser ablation is still being investigated and discussed, which is beyond the scope of this thesis.

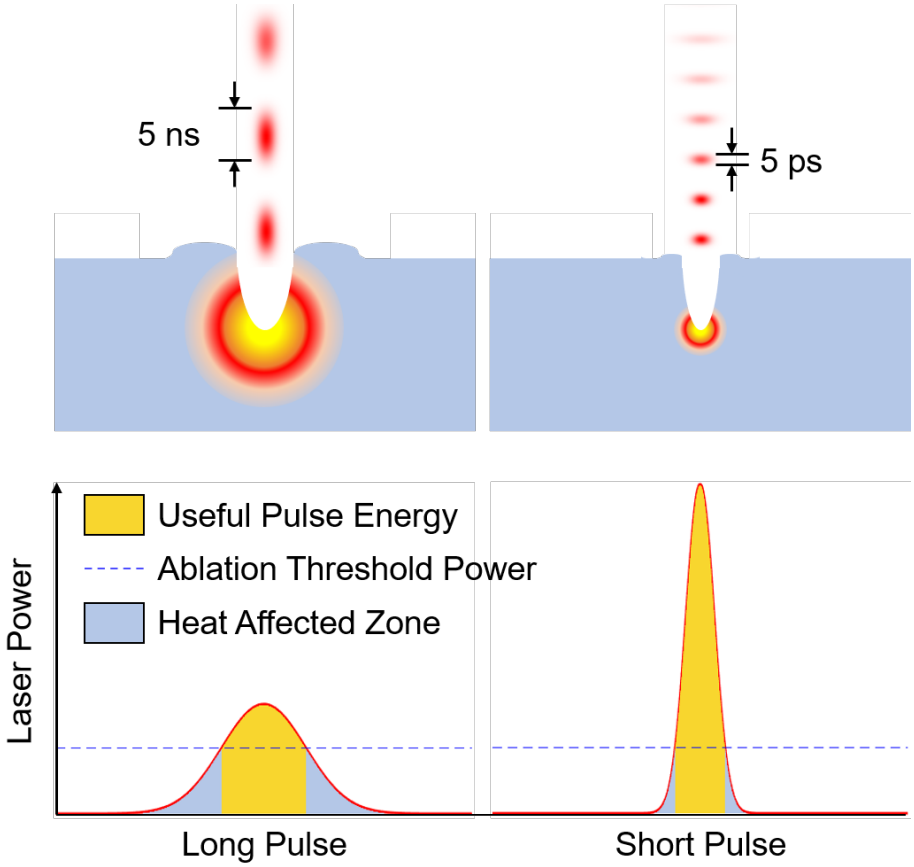


Figure 3.9: UV laser interaction with dielectric materials. Left: nanosecond pulse. Right: picosecond pulse. Peak power of a picosecond pulse is about 1000× of a nanosecond pulse. © 2019 IEEE

Lasers used in laser ablation are typically pulsed lasers. Compared to continuous wave lasers, pulsed lasers with the same power could have extremely high peak intensity, which is beneficial to the laser ablation process. The pulse width is a critical parameter of lasers. The pulse width of widely used UV lasers for ablation in industry is in the order of a few nanoseconds (10^{-9} s). More advanced laser ablation systems have shorter pulse width of a few picosecond (10^{-12} s) and even in the femtosecond (10^{-15} s) range. A comparison of laser–dielectric interaction between a nanosecond laser and a picosecond laser is shown in Figure 3.9.

Laser intensity on the surface of the substrate typically follows Gaussian distribution, and the intensity of the laser has to be larger than the ablation threshold for the ablation

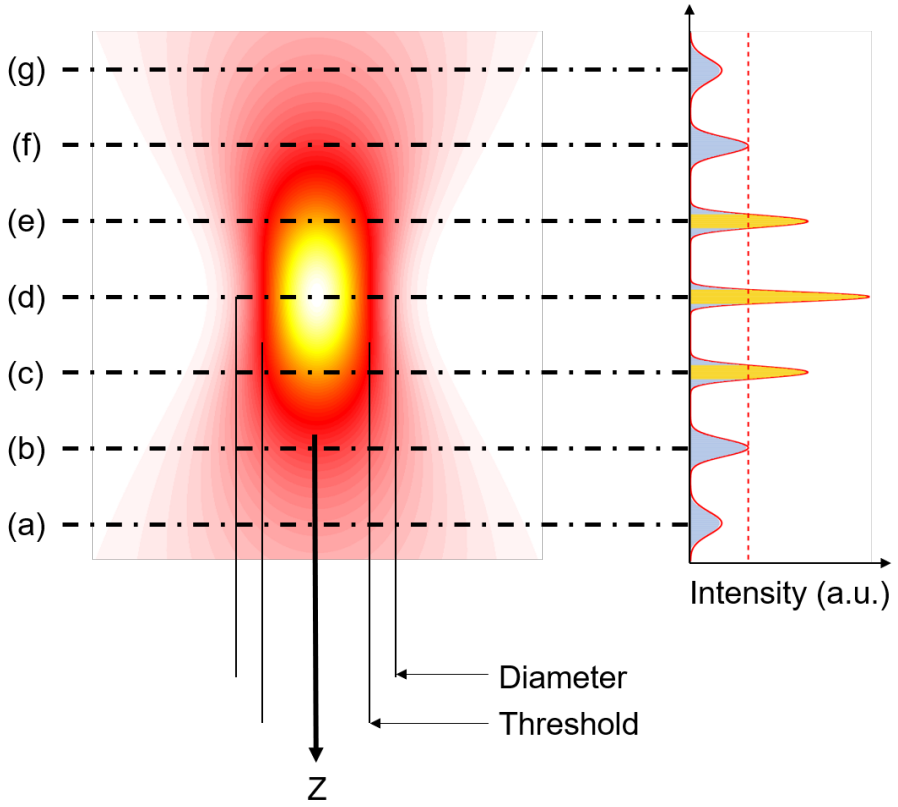


Figure 3.10: A schematic of the laser beam profile and the intensity distribution at different z locations around the focal plane.

to happen. Otherwise, photons in the laser beam will be absorbed and transformed into heat. When the laser has a 5 ps pulse width and the power of the laser is the same as the one with a 5 ns pulse with, less photons will be in the heat affected zone, so more power is used to drill the material deeper. Femtosecond lasers could open even smaller microvias compared to picosecond lasers, however, femtosecond lasers are much more expensive than picosecond lasers.

A schematic of a laser beam profile in shown in Figure 3.10. Seven different locations in the z direction around the focal plane are marked as (a) to (f) in the figure. At the focal plane, location (d), the beam has the highest peak intensity, and the material could be easily ablated since majority of the photons are used in the ablation area if the laser focal plane overlaps the surface of the material to be drilled. As the location along the laser beam moves from (d) to (c) or (e), the total power doesn't change but the peak intensity

drops, and the ablated regions become shallower. When the beam location overlapping the surface of the substrate moves from (c) or (e) to (b) or (f), the peak intensity decreases and becomes lower than the ablation threshold, so the laser ablation doesn't happen. The laser at this location could only heat the material up. So, the laser beam position has a huge impact on the ablation. Only when the laser focal plane is overlapping or parallel and close to the surface of the material to be drilled, the smallest microvia could be achieved.

Not only the beam location is important to laser ablation, the beam intensity at the focal plane also plays a crucial role. The laser beam intensity at the focal plane follows the Gaussian distribution described as

$$I(r) = \frac{P}{\pi r_0^2/2} e^{-2\frac{r^2}{r_0^2}} \tag{3.12}$$

where I is the beam intensity as a function of the distance from the center of the focal plane r, P is the average laser power, and r_0 is the beam radius. It could be inferred that the beam intensity is proportional to the power of the laser but inversely proportional to the size of the beam. The beam intensity also decreases as the observation point moves further away from the center. To simplify the discussion, assume the beam diameter $D_0 = 2r_0$, and the peak intensity at the center of the focal plane $I_{\mathrm{m}} = \dfrac{P}{\pi r_0^2/2}$, then Equation 3.12 could be rewritten as

$$I(D) = I_{\mathrm{m}} e^{-2\frac{D^2}{D_0^2}} \tag{3.13}$$

For a material to be drilled with an ablation threshold I_{th}, it could be derived from Equation 3.13 that

$$D = \sqrt{\frac{1}{2} \ln \frac{I_m}{I_{\mathrm{th}}}} D_0 \tag{3.14}$$

Based on Equation 3.14, it is straightforward that the theoretical microvia opening D is determined by the beam size D_0, the beam power in terms of the maximum beam intensity $I_m\mathrm{m}$, and the ablation threshold of the material I_{th}. In order to fabricate smaller microvias, there are three approaches Equation 3.14, reducing the beam size, lowering the laser power,

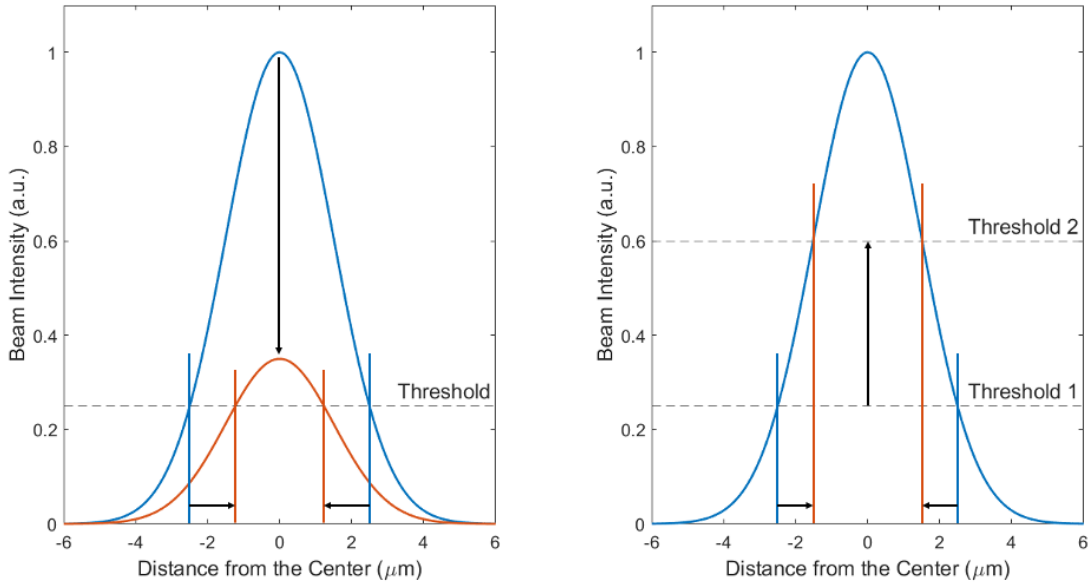


Figure 3.11: Reducing the size of microvias by (a) using lower laser power and (b) increasing the ablation threshold.

and increasing the ablation threshold. Typically for a laser ablation system, the beam size of the laser could not be changed. The beam size of the laser used in this thesis is around 8 µm. Besides adjusting the beam size, reducing the maximum beam intensity as shown in Figure 3.11(a) could also help decrease the size of microvias. It is the same as changing the output power of the laser, which is adjustable. Theoretically, the laser beam is capable of fabricating infinitely small microvias as long as the maximum beam intensity is larger than the ablation threshold of the material.

Adjusting the laser power down could potentially help achieve smaller microvias, but there are other concerns. When the maximum intensity is higher but very close to the ablation threshold of the material, the quality of microvia will be degraded due to the thermal effects generated by laser, and small fluctuation in the laser power affects the quality of

microvias as well. From Equation 3.14, it could be derived that

$$\frac{\mathrm{d}D}{\mathrm{d}I_{\mathrm{m}}} = \frac{D_0}{4\sqrt{\frac{1}{2}\ln\frac{I_{\mathrm{m}}}{I_{\mathrm{th}}}}}\frac{1}{I_{\mathrm{m}}} \tag{3.15}$$

Then we have

$$\frac{\mathrm{d}D}{D} = \frac{1}{2\ln\frac{I_{\mathrm{m}}}{I_{\mathrm{th}}}}\frac{\mathrm{d}I_{\mathrm{m}}}{I_{\mathrm{m}}} \tag{3.16}$$

Equation 3.16 indicates that both the power fluctuation $\frac{\mathrm{d}I_{\mathrm{m}}}{I_{\mathrm{m}}}$ and the relative position of the maximum intensity and the ablation threshold $\frac{I_{\mathrm{m}}}{I_{\mathrm{th}}}$ would have impacts on the stability of via size. Assuming that the laser drilling system has a power fluctuation of less than 5% at normal working power range (5% to 95% of the maximum power), if the acceptable fluctuation of the via size is within 10%, the maximum intensity should be larger than 1.28 times of the ablation threshold. When the laser power is adjusted down to reach the 1.28x limit, it might fall in the low power range (less than 5% of the maximum power), where the power fluctuation increases. This calculation indicates that there's a lower limit of the laser power to achieve smaller via size and simultaneously maintain the via size stability.

The last approach to achieve smaller microvia is to increase the ablation threshold as shown in Figure 3.11(b) instead of lowering the laser power. By increasing the ablation threshold, it means changing the material to be drilled. By using a material with a higher ablation threshold, the same laser power could open smaller microvias.

3.2.3 Laser Ablated Microvias on ABF–GX92P

The laser ablation system used in this study is CornerStone™ developed by Electro Science Industries. The UV laser source generates 355 nm laser pulses at 80 MHz with a maximum power of 16 W, and the pulse width is 5 ps. Since the repetition rate is 80 MHz, the interval between pulses is 12.5 ns. A schematic of the pulses at 80 MHz is shown in Figure 3.12(a). It's a fast repetition rate with narrow pulses. Figure 3.12(b) shows a close look of the first

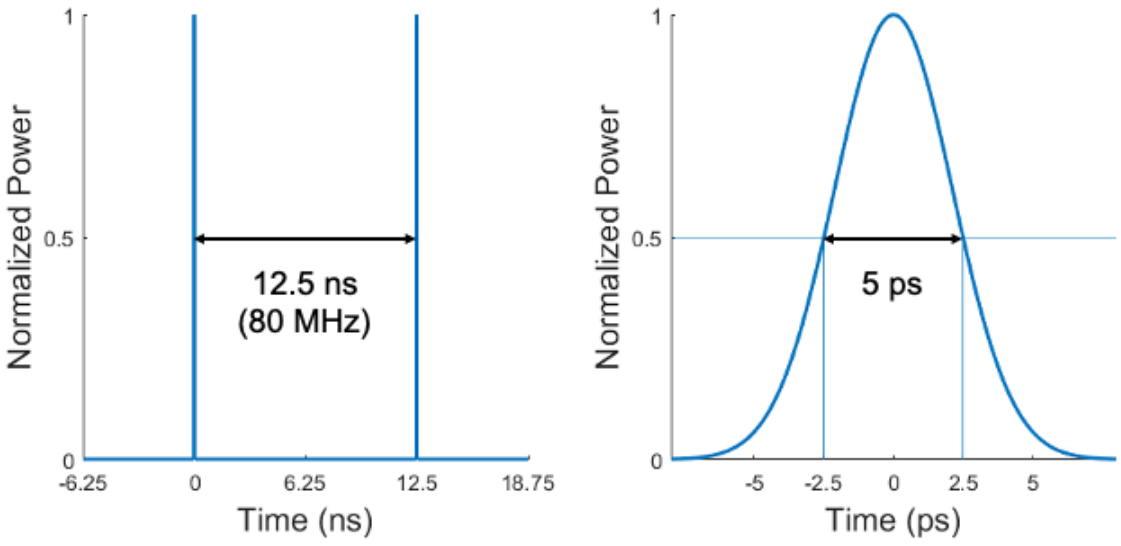


Figure 3.12: (a) Pulses at 80 MHz, and (b) a pulse with 5 ps pulse width.

pulse in Figure 3.12(a), the pulse width, along with the full width at half maximum, which is 5 ps. The units of the x axis in both figures are different.

There are several drilling methods available (pre–set) in the laser drilling tool, of which widely used methods are the spiral raster mode and the punch mode. In the spiral raster mode, the laser is first focused on the center of the drilling pattern, and then the focal point moves outward in a spiral path until the boundary of the drilling pattern is reached. The size of the drilled pattern is determined by the diameter of the outermost circle. The spiral raster mode exceeds in large area drilling, but it is not suitable for smaller microvia fabrication. In the punch mode, however, only one punch which consists of 400 pulses is performed on the substrate for microvia formation. Since there is only one punch in the punch mode, it can inherently be able to fabricate smaller openings than the spiral raster mode. The punch mode is used for smaller microvia fabrication study in this thesis.

The substrate used in this study is organic laminates. Glass panels and silicon wafers do have smoother surfaces, and the surface planarity is superior as well compared to organic laminates. However, organic laminates come with copper foils on both sides of the organic core, which helps reduce the fabrication complexity since seed layer deposition

is not needed. Organic laminates are also flexible and easy to handle, so dicing a small piece on organic laminates with drilled microvias for scanning electron microscope (SEM) characterization is easier compared to breaking a silicon wafer or a glass panel. Organic laminates used in this study has a 60 µm organic core, sandwiched by 3 µm thick low–profile copper foils on both sides. They are placed and taped on a silicon wafer to keep the surface flat and make the sample robust. The fabrication process developed for organic laminates could also be applied directly on glass panels or silicon wafers.

The dielectric material used for laser drilling is Ajinomoto buildup film (ABF–GX92P). ABF is widely used in the packaging industry due to its panel processing capability and high adhesion strength including low D_{f} and D_{k}. ABF–GX92P is a modified version of ABF–GX92, developed for ultra–fine RDLs. It has smaller fillers which result in low surface roughness, low CTE, and the thickness of the film is 5 µm. Properties of ABF–GX92P are listed in Table 3.2.

Table 3.2: Material properties of ABF–GX92P. © 2019 IEEE

Property	Conditions	Value
CTE / 10^{-6} m/(m·K)	TMA	39
T_{g} / °C	TMA	153
D_{k}	Cavity perturbation, 5.8 GHz	3.2
D_{f}	Cavity perturbation, 5.8 GHz	0.014
Young's modulus / GPa	23 °C	5.0

The process development of ultra-small microvia fabrication by laser ablation is illustrated in Figure 3.13, and details are described below.

1. **Ajinomoto buildup film (ABF) lamination.** After the organic laminate substrate was taped on the silicon wafer, ABF was laminated on the substrate using a vacuum laminator Meiki MVLP 300, and then cured in a conventional oven.

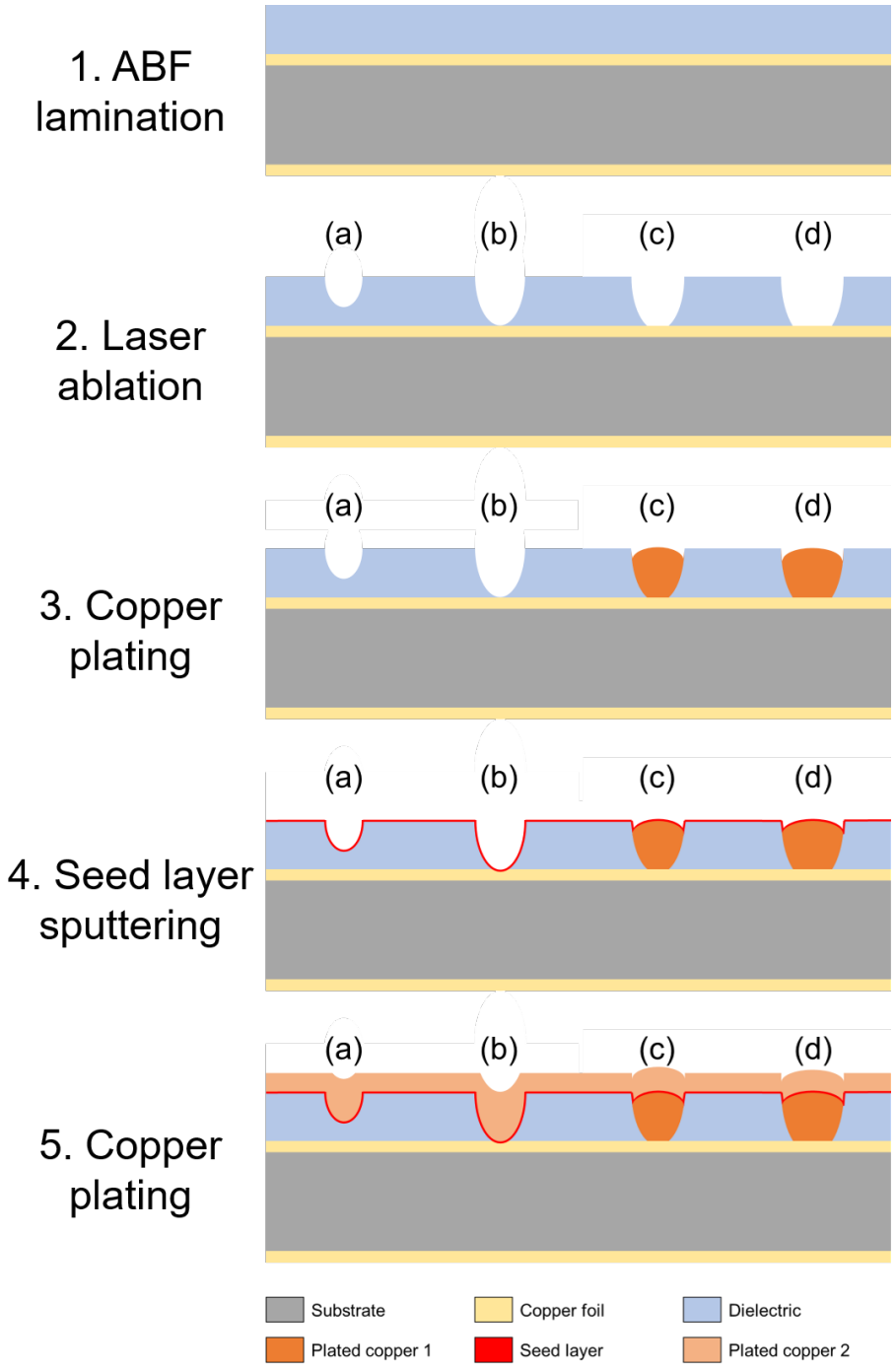


Figure 3.13: Process development flow of ultra-small microvia fabrication. © 2019 IEEE

2. **Laser ablation.** After ABF was laminated and cured, laser ablation was used for microvia fabrication in ABF. Four different results could emerge after laser ablation, which are marked (a) to (d) in Figure 3.13: (a) the microvia is not open, (b) the

microvia is barely open, (d) the microvia is open with a smaller opening, and (d) the microvia is fully opened with a larger opening. The location, power, and the number of punches of the laser was optimized in this step.

3. **Copper plating.** After laser ablation, plasma desmear was done on the sample to clean the debris and remove residues, followed by bottom–up electrolytic plating to fill microvias with copper. In case (b), plasma desmear might help open the microvia. In case (c), a smaller microvia with copper filled inside was achieved.

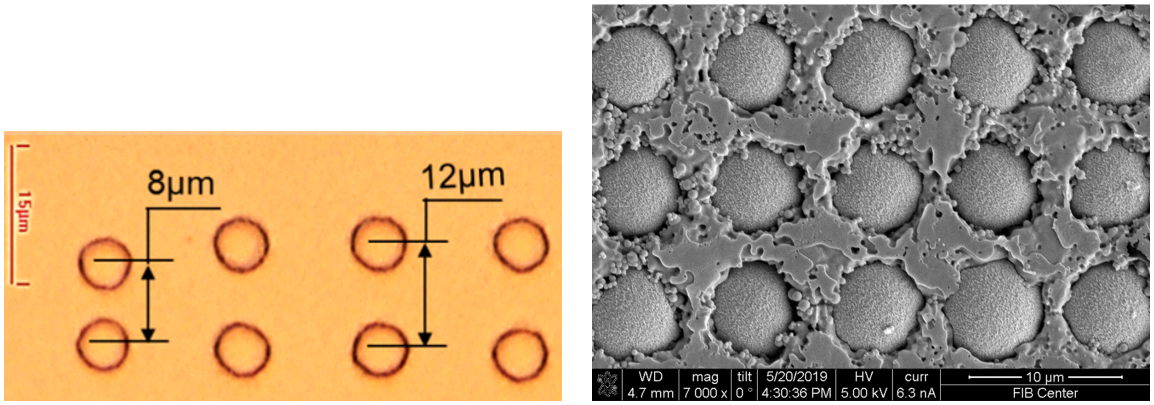
4. **Seed layer sputtering.** Fabrication of microvias in industry does not use copper plating directly after laser ablation since the substrate usually does not have fully covered copper on top as a conduction layer. Instead, a seed layer was sputtered on the drilled substrate.

5. **Copper plating.** After the seed layer was sputtered, copper of a few microns was plated on top of the seed layer.

Initial characterization on microvias was done using optical microscopes (optical imaging). However, as the size of microvias becomes smaller, the resolution and the DOF of optical microscopes might not be sufficient for microvia characterization. Cross–sectioning and/or SEM are needed to observe microvias with a diameter less than 5 µm.

In the laser ablation step, parameters in the laser setting need to be optimized to achieve the smallest microvias with the best quality. The optimization is detailed below.

1. **Laser beam location optimization.** As shown in Figure 3.10, the optimal beam location is achieved when the laser focal plane overlaps the surface of the material. Thus, beam location optimization was the first step of the whole optimization process. The first beam location scanning range was from −500 µm to 500 µm with a step of 50 µm. Then the range was narrowed down to −400 µm to 0 µm with a step of 20 µm. Eventually, it is confirmed that the beam location is not calibrated and there is



(a) **(b)**

Figure 3.14: (a) 5–µm microvias by ps UV laser with 8– and 12–µm pitches. (b) SEM image of microvias after copper plating. © 2019 IEEE

a systematic error of around −160 µm on this tool, so only when the laser focus is set to 160 µm below the sample, the laser focal plane overlaps the surface of the sample.

2. **Laser power optimization.** After the laser beam location was optimized, laser power optimization was the next step. The tool is capable of generating a laser power of 16 W, however, for small microvia fabrication, 16 W is extremely high. The power range was set from 0.1 W to 1 W with an increment of 0.1 W. As the laser power decreases, the maximum intensity decreases, so the area encircled by the ablation threshold becomes smaller as well. Laser beams of 0.1 W could still open microvia in ABF–GX92P, and a top view optical image is shown in Figure 3.14(a).

5 µm microvias opened by a laser beam of 0.1 W with 8– and 12–µm pitches are presented in Figure 3.14(a). A matrix of 5 µm microvias with 8 µm pitch after copper plating is shown in Figure 3.14(b). Since the copper was plated from the bottom to the top, it is evident that the microvias are fully open. The surface of the polymer is also flat, and the slag generated by heating and solidifying at the via edges is not observed.

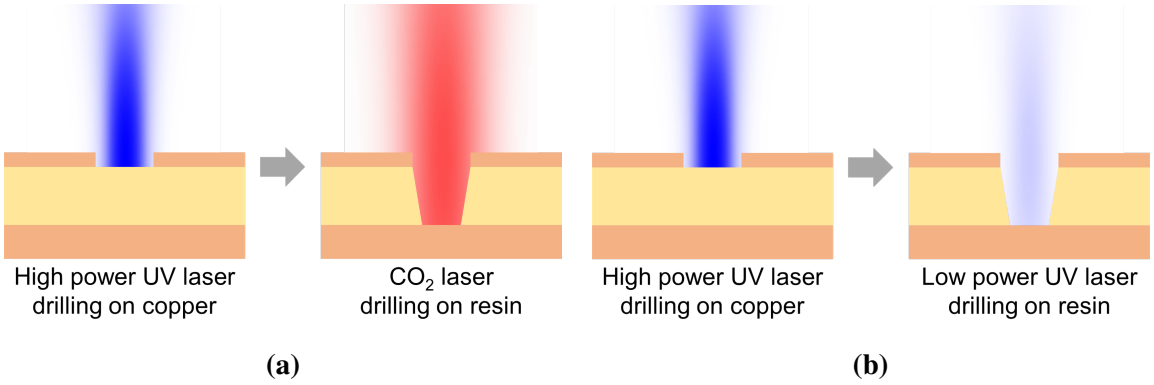


Figure 3.15: Schematics of laser drilling on RCC with (a) hybrid laser system and (b) two-step UV laser drilling system. © 2020 IEEE

3.2.4 Laser Ablated Microvias on ABF–GX92P with a Thin Metal Barrier Layer

Based on Equation 3.14, another approach to decrease the size of microvias besides reducing the laser power is to use a material with a higher ablation threshold. However, using a higher ablation threshold material will results in other issues like an increased heat affected zone, and a reduced drilling depth. The new material might not have the proper electrical properties required by the electrical design as well. Instead of using an entirely new dielectric material for microvia fabrication, a material with higher ablation threshold could be added on top of ABF, serving as a hard mask for the ABF layer beneath. This method was developed previously, and it is called the RCC foil approach. Two types of laser drilling were developed on RCC for microvia fabrication, hybrid laser drilling as shown in Figure 3.15(a), and a two–step UV laser drilling as shown in Figure 3.15(b).

In hybrid laser drilling, a high–power UV laser is first used to drill through the copper on top to form a hard mask, and then a CO_2 laser is used to open the resin layer. The CO_2 laser has a longer wavelength and lower intensity so it would not damage the copper. In two–step laser drilling, the first step is the same as in the hybrid laser drilling process. The second step is to use a low power UV laser to drill through the resin without damaging the copper underneath the resin.

The thickness of the top copper in the RCC approach is a few microns. However,

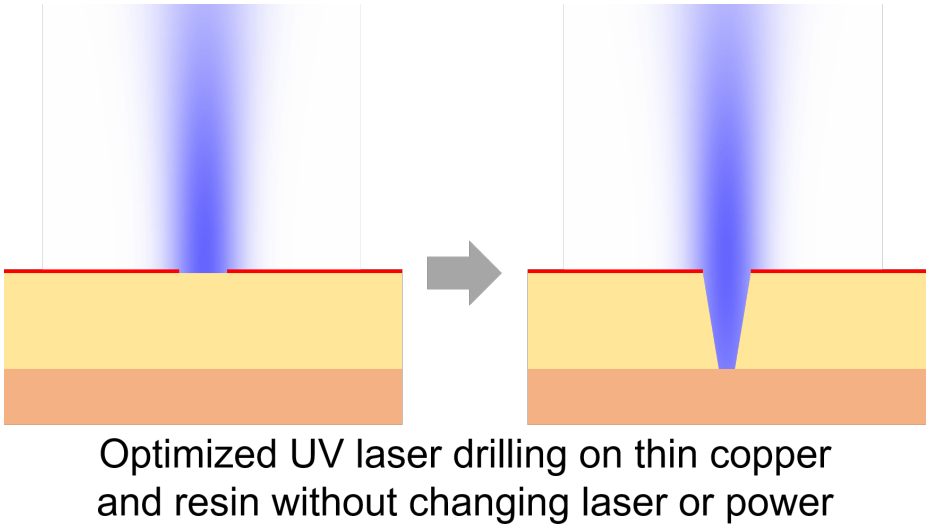


Figure 3.16: Smaller microvias fabricated in thin copper and resin by optimized UV laser drilling without changing laser or power. © 2019 IEEE

it's possible to reduce the thickness of this layer of copper and use a lower power to drill through the copper with a smaller opening, as shown in Figure 3.16. The copper layer sputtered on top of ABF in this study is only 80 nm thick.

Since copper is a good thermal conductor, the heat generated on the copper layer could be transported away from the drilling region soon. Hence, the impact of the heat generated in the copper layer on the layer beneath is minimal. The added thin copper layer could serve as protection not only from the heat affected zone but also the redeposition of the ablated material. During the laser ablation process, the ablated material is either vaporized or ionized, and then leaves the ablation region. Some ablated material could be redeposited back on the surface of the material. The redeposition adversely impacts the surface planarity of the sample. However, by adding a copper layer on top, it could potentially prohibit the redeposition of the ablated material directly on top of ABF as shown in Figure 3.17. The redeposition on top of the copper could be easily removed in the copper desmear process, which consequently improves surface planarity.

Once the copper was sputtered on top of ABF, the same laser optimization process discussed before was carried out on the sample. First locate the best beam position, and

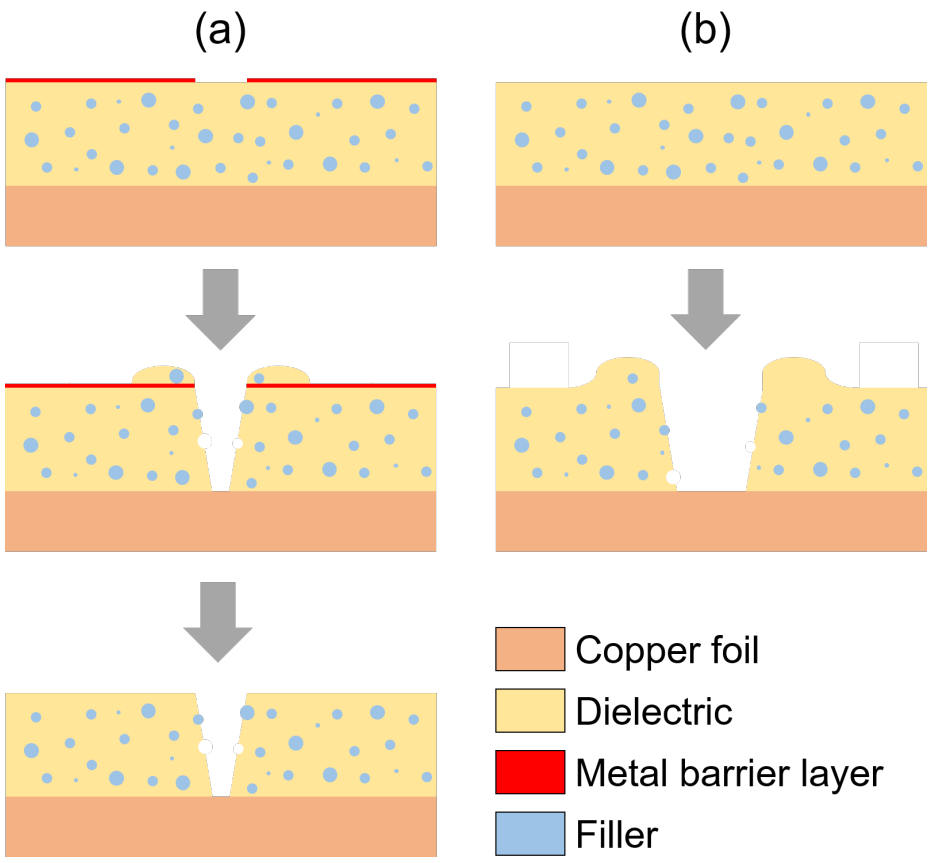
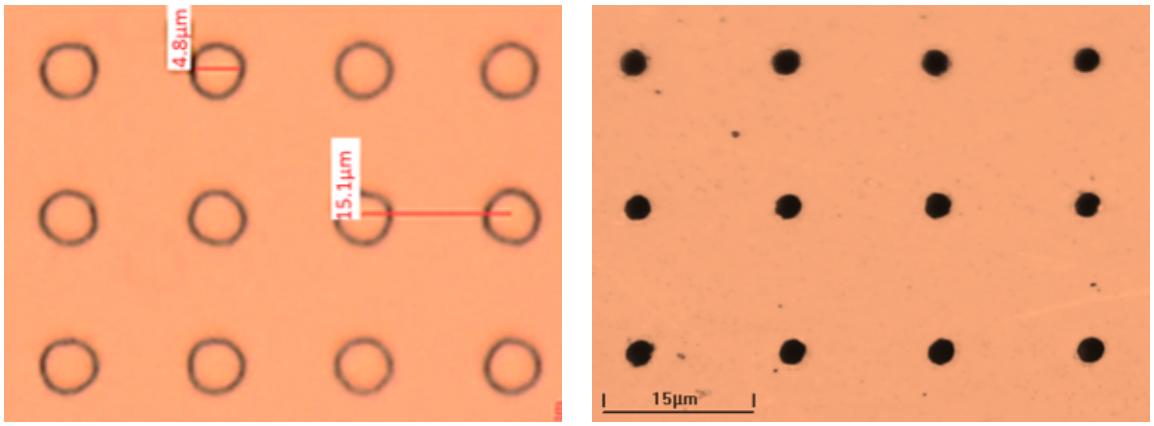


Figure 3.17: Schematics of redeposition on (a) ABF with a metal barrier layer and (b) bare ABF. © 2020 IEEE

then optimize the power and the number of punches. It must be noted that previously, one punch could fully open microvias in ABF, but the added copper layer requires an additional punch to open. One punch could only open the 80 nm copper layer, but it is not enough to drill through ABF. To achieve fully opened microvias using the thin metal barrier layer methods, at least two punches are needed.

As a comparison, 0.1 W laser power was used on bare ABF and a copper barrier layer on top of ABF, and the results are shown in Figure 3.19. Both figures have the same scale, and it is clear that 0.1 W laser opens smaller openings in copper than in ABF. From Figure 3.19(a) and Figure 3.19(b), 4 µm and 3 µm microvias could be open with the help of the nanometer metal barrier layer. Fillers on the edge are clear but they do not pose a risk for 3 µm microvia fabrication. However, when the opening becomes smaller, the fillers



(a) (b)

Figure 3.18: 0.1–W laser fabricates (a) 5–µm openings in ABF and (b) 2–µm openings in copper. © 2020 IEEE

in ABF could potentially block further ablation, as shown in Figure 3.19(c). Fillers are typically small silicon dioxide beads with a diameter of a few microns, which could not be vaporized by laser beam due to its high ablation threshold. When the microvias are large, laser ablation could remove the epoxy component in ABF and the fillers will follow the vaporized epoxy as the epoxy leaves the ablated region. When the opening in the copper layer is getting smaller, fillers could be large enough to prohibit anything from escaping from the microvia as shown in Figure 3.19(d).

3.2.5 Laser Ablated Microvias on JSR GT–N01 with a Thin Metal Barrier Layer

Fillers in ABF are the main issue for fabrication of less–than–3–µm microvias. ABF with smaller fillers could be used to study the feasibility, but the research on smaller microvia fabrication in this thesis proceeds by using other materials instead. Since the filler is the issue, an obvious choice is to use dielectrics with no fillers. The material used for the continuing smaller microvia fabrication is a liquid PID material GT–N01 from JSR Corporation. Two samples were prepared for the study. On one sample, the coated film has a thickness of 3 µm, and the other one is 2 µm. The ablation results are shown in Figure 3.20.

Figure 3.20(a) and Figure 3.20(b) are from a microvia fabricated on the sample with the

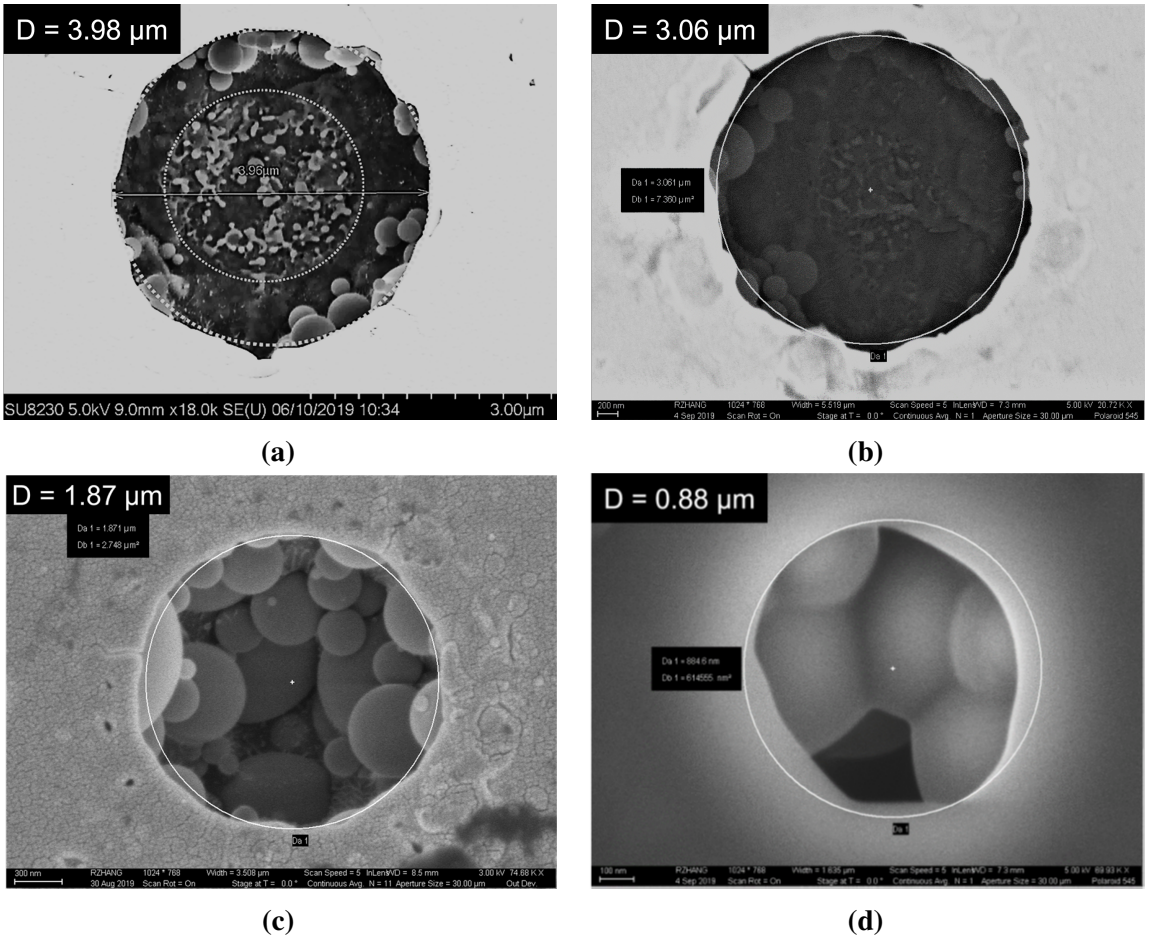


Figure 3.19: SEM images of microvias with a diameter of (a) 4 µm, (b) 3 µm. (c) 0.1–W laser ablates 2–µm opening with fillers inside. (d) A submicrometer opening and fillers trapped inside. © 2020 IEEE

3 µm film. When the SEM was focused on the top opening, the diameter of the microvia was measured to be around 1.5 µm. When the SEM was focused on the bottom opening, the residues indicate that the microvia was fully open and the copper beneath was exposed. In Figure 3.20(c), additional signals from backscattered electron (BSE) were added. The brightness of the BSE signals is a reflection of the atomic mass of the observed area. The white spot in the middle of the figure indicates that there was copper at the bottom of the microvia, which was confirmed by energy–dispersive X–ray spectroscopy (EDS). SEM typically has a relatively small DOF, it's very challenging to observe the full view of the microvia from the top to the bottom. Also, the microvia diameter is as small as 1 µm, so

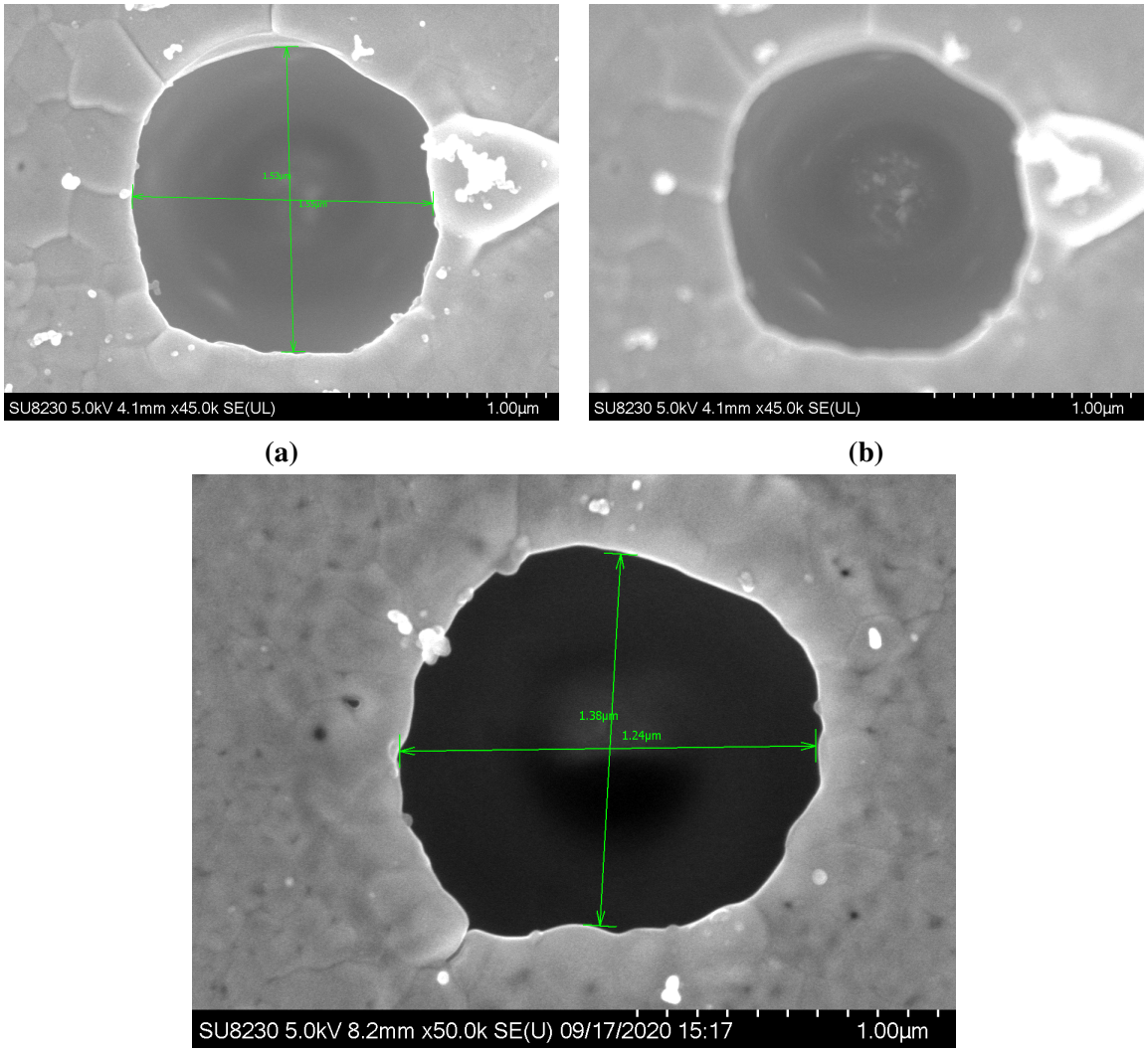


Figure 3.20: SEM images of a 1.5 µm microvia in a 3 µm film focused on (a) top opening and (b) bottom opening. (c) An SEM image of a 1.3 µm microvia in a 2 µm film

the electron detectors in SEM cannot get much signal from the inside of the microvia. To proceed further with the investigation of smaller microvias, other characterization methods are needed.

By adding a nanometer–thick metal barrier layer, multiple punches are needed to fully open microvias. When the size of microvias is approaching 1 µm, the landing accuracy of the laser beam could be a potential challenge. To characterize the landing accuracy, a matrix of openings by one punch in the copper layer is needed for statistical analysis.

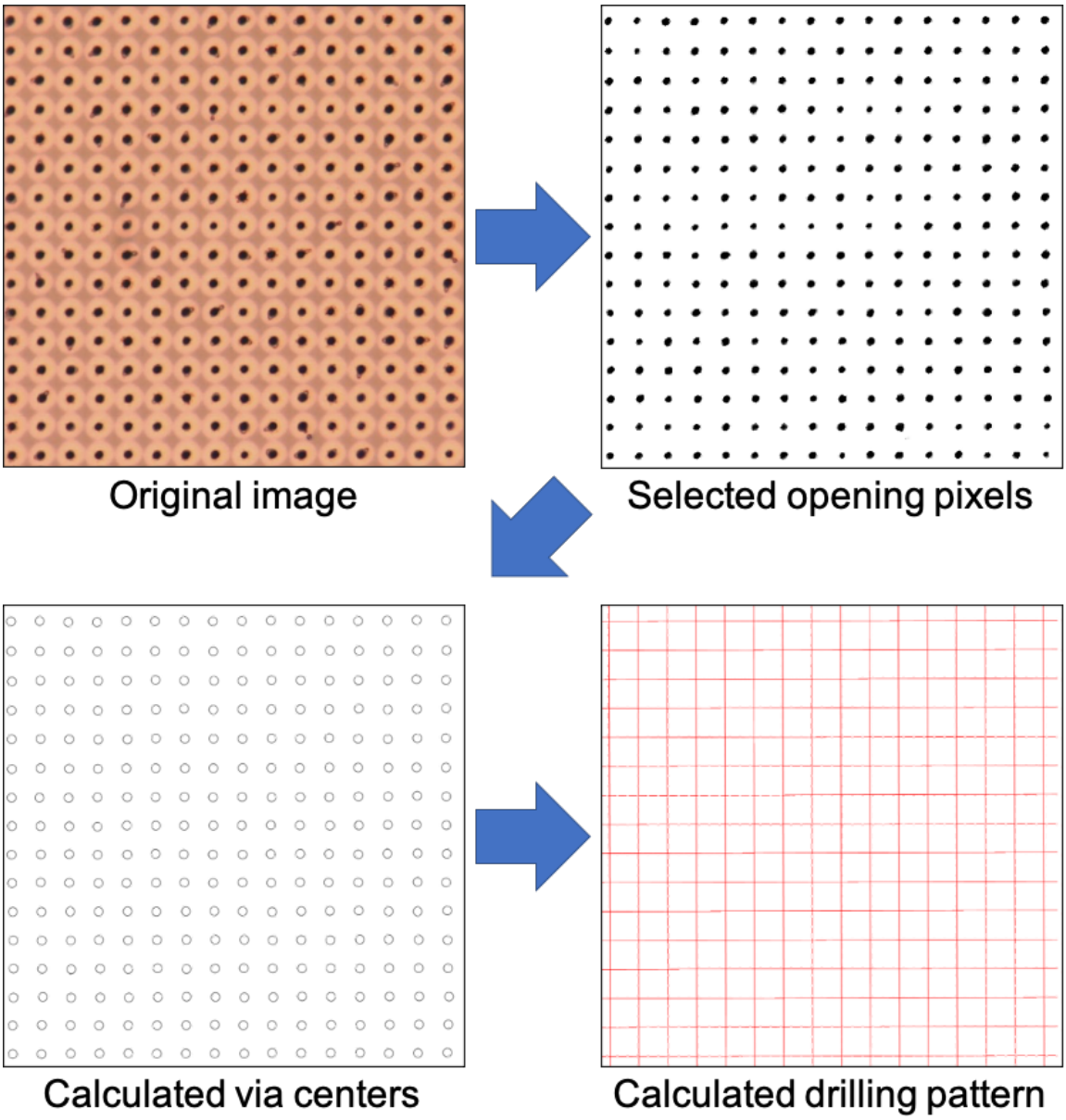
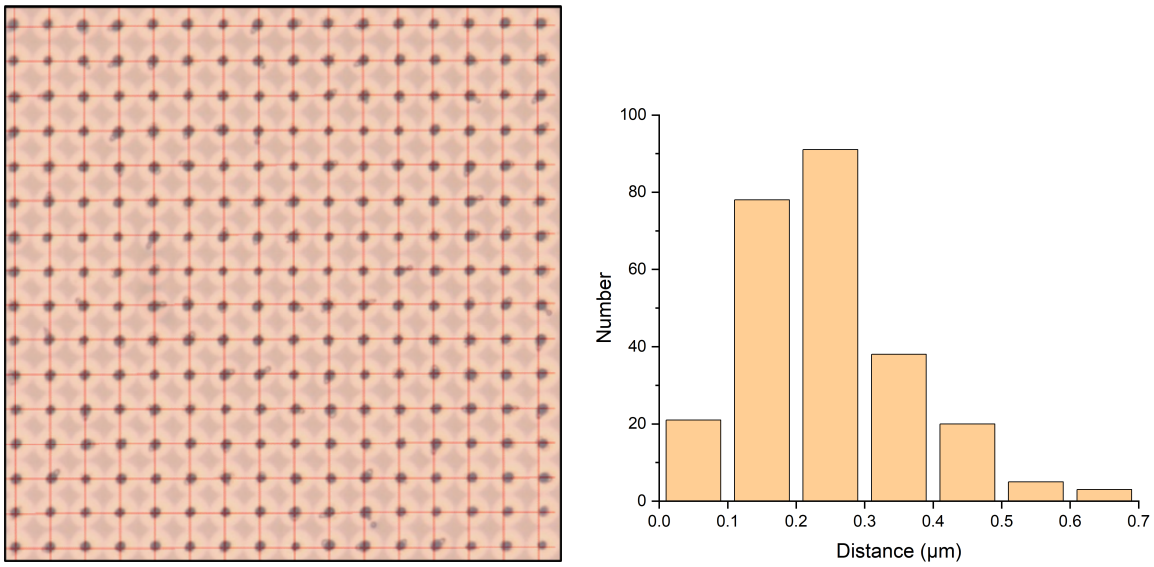


Figure 3.21: Drilling pattern calculation process.

However, the resolution of the optical microscope is not high enough to show the distance between the landing spot and the drilling spot, and SEM is extremely time consuming to do statistical analysis on the location of microvias in a matrix. An optical image with a matrix of 16 by 16 microvias was selected, and image processing by selecting red, green, and blue (RGB) channels to locate microvias was used to study the landing accuracy of the laser as shown in Figure 3.21, and the process is detailed below.



(a) **(b)**

Figure 3.22: (a) Drilling pattern combined with drilled microvias. (b) Landing accuracy distribution.

1. Select an in–focus area from an optical image of a matrix of microvias.

2. Select black pixels in the opening area as the microvia openings. Since there are dirt and redeposition on the surface which have black pixels in the image, pixel selection by tuning the threshold of RGB channels needs to be optimized.

3. Calculate the centers of openings by using the pixel locations and their average in both x and y directions. The calculated via centers are the laser drilling points.

4. Calculate drilling pattern. Since the vertical and horizontal drilling lines are perpendicular to each other but the image might not be perfectly aligned to the drilling lines, linear regression and iteration are used to find the minimum sum of the square of the distances between the landing spots and the drilling spots.

The calculated drilling pattern combined with the drilled microvias is shown in Figure 3.22(a). The landing spots are not on the exact locations of the drilling spots, but they are not far either. The landing accuracy distribution is shown in Figure 3.22(b) where out of the 256 microvias in the image, the average distance between the landing spot and the

corresponding drilling spot is 0.24 µm, and the maximum distance is 0.67 µm. For 1 µm microvia fabrication using two punches, the second punch is in average 0.24 µm away from the first punch, which might be a huge challenge for repeatability and yield. Further studies are needed to characterize the impact of the landing accuracy on smaller microvia fabrication.

3.3 Summary

This chapter described the research on high density electronic interconnects for high data rate communications including routing wires in the horizontal direction and microvias in the vertical direction.

As the I/O density demand increases, the width of routing wires is getting smaller. To meet the electrical design rules, high aspect ratio routing wires are desired. Analysis on photolithography for ultra–fine routing wires indicated that high resolutions and high aspect ratios are contradicting each other, so new type of materials or fabrication methods are needed. The embedded trench method was developed to address challenges faced by the traditional SAP and using this method, routing wires with 3 µm in line width were achieved. The same material was also used to fabricate smaller microvias following which 3 µm microvias with 6 µm pitch and 2 µm microvias with 12.5 µm pitch were demonstrated.

Picosecond UV laser was used to develop ultra–small microvias in vertical interconnects for high density I/O. Laser beams in the space domain and the time domain were analyzed for the optimal operation to fabricate microvias. The finest microvias by UV laser ablation were pushed from 20 µm down to 5 µm in diameter in ABF. By adding a 80–nm–thick copper layer on top of ABF due to its high ablation threshold, microvias as small as 3 µm in diameter could be achieved. However, fillers in ABF prohibit the further scaling of microvias in ABF so a no filler dielectric liquid was used instead. By spin coating the liquid on the substrate and sputtering copper on top, 1.5 µm microvias were achieved in a 3 µm film, which has an aspect ratio of 2:1. The finest microvias fabricated were 1.3 µm in

diameter in a 2 μm film. Since the additional copper layer requires an extra laser punch to open, landing accuracy of the laser beam was also studied. By fine–tuning the threshold of RGB channels on an optical image, the distance of the landing spot of the laser and the drilling spot is 0.24 μm in average and 0.67 μm at maximum. The 0.24 μm average landing distance is not an issue for microvias larger than 2 μm, but it's a serious challenge for less than 2 μm microvia fabrication using multiple punches.

CHAPTER 4

LOW LOSS OPTICAL INTERCONNECTS ON GLASS

Optical interconnects especially waveguides are essential building blocks in optical system packaging since they are the optical components to confine the light wave, guide the transmission, and preserve the power and signal integrity. The most common types of waveguides are based on total internal reflection, from geometrical optics point of view, and a side view of such a waveguide is shown in Figure 4.1.

Consider a light beam (red arrow) incident on the interface with an angle θ_1 between the outside and the waveguide. It propagates to the interface between two materials with refractive index of n_1 and n_2 , respectively. In this waveguide setup, the medium with a refractive index of n_1 is called the core, and the light will travel inside the core. The materials with refractive index of n_2 and n_3 are called clad. Based on Snell's law,

$$n_0 \sin\theta_1 = n_1 \sin\theta_2 = n_1 \cos\theta_3 \tag{4.1}$$

Assuming the total internal reflection happen at the interface of n_1 and n_2, the incident angle has to be larger than the critical angle

$$\theta_3 > \theta_{\mathrm{c}} \tag{4.2}$$

where

$$n_1 \sin\theta_{\mathrm{c}} = n_2 \tag{4.3}$$

Then we have

$$\sin\theta_{\mathrm{c}} = \frac{n_2}{n_1} \tag{4.4}$$

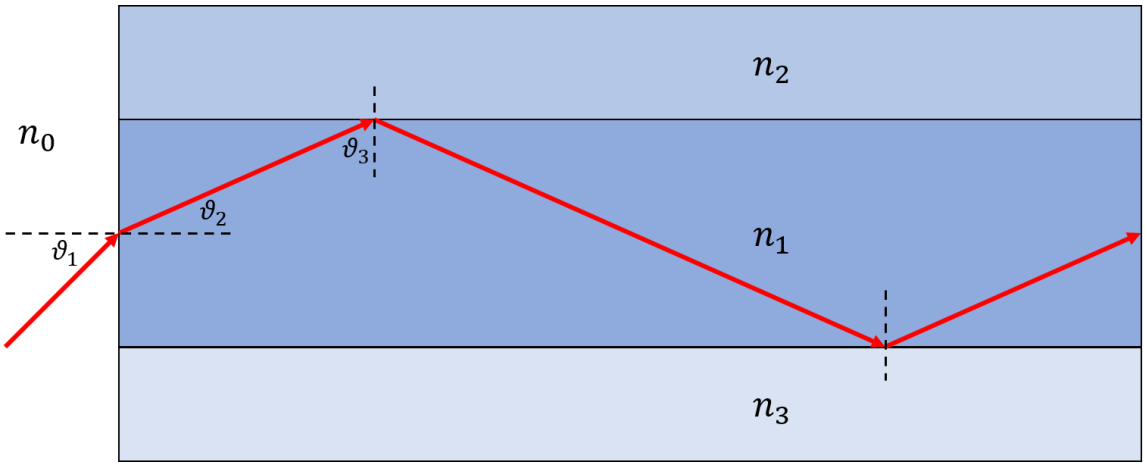


Figure 4.1: Total internal reflection in a waveguide.

$$\sin\theta_3 > \frac{n_2}{n_1} \tag{4.5}$$

$$\sin\theta_2 = \sqrt{1-\sin^2\theta_3} < \frac{\sqrt{n_1^2 - n_2^2}}{n_1} \tag{4.6}$$

In order for the total internal reflection at the interface of n_1 and n_2 to make sense in Equation 4.6, it's clear that $n_1 > n_2$, which means when a light travels from a high refractive index material (n_1) to a low refractive index material (n_2), and the incident angle is larger than θ_c, total internal reflection happens. All the light will be reflected back to material n_1 instead of getting refracted into material n_2. Total internal reflection in a waveguide would happen at the interface of n_1 and n_3, so the light will travel through the waveguide in the core without leaking into the clad.

Combining Equation 4.1 and Equation 4.6, we have

$$n_0 \sin\theta_1 = n_1 \sin\theta_2 < \sqrt{n_1^2 - n_2^2} \tag{4.7}$$

If the surrounding of the waveguide is air which has a refractive index of 1, we have

$$\sin\theta_1 < \sqrt{n_1^2 - n_2^2} \tag{4.8}$$

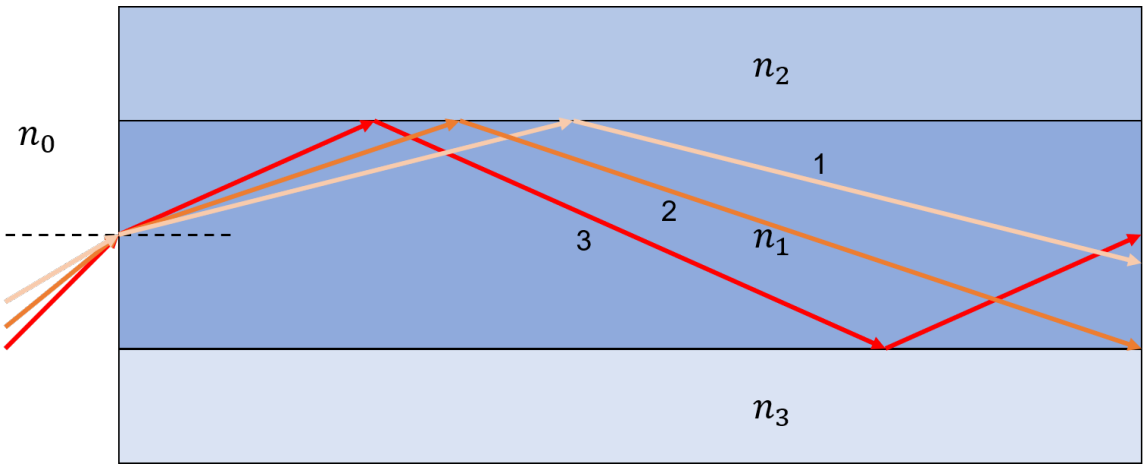


Figure 4.2: Guided modes in a waveguide.

If $\sqrt{n_1^2 - n_2^2} > 1$, total internal reflection happens for any incident angle θ_1. However, for most of the applications, $\sqrt{n_1^2 - n_2^2} \ll 1$, so the acceptance angle, which is the maximum acceptable incident angle, is described as

$$\sin\theta_{\text{ac}} = \sin\theta_1(\text{max}) = \sqrt{n_1^2 - n_2^2} \tag{4.9}$$

And the numerical aperture of a waveguide in defined as

$$NA = n_0 \sin\theta_{\text{ac}} = \sqrt{n_1^2 - n_2^2} \tag{4.10}$$

Light with any incident angle smaller than the acceptance angle will be totally reflected at the interface between the core and the clad. However, only a finite number of such angles exist for a given waveguide design due to restrictions based on electromagnetic wave characteristics from the wave optics perspective. Such discrete angles are called guided modes, and a schematic of guided mode is shown in Figure 4.2. Since a light beam with a larger incident angle (light beam 3 or the red beam) will have a longer optical path reaching the output side of the waveguide compared to a light beam with a smaller incident angle (light beam or the pink beam), the traveling times for different guided modes varies. When a pulse is launched into the waveguide, the pulse broadens when propagating down

along the waveguide, which is called intermodal dispersion. Such dispersion limits data rates a waveguide could support, however it could be addressed by waveguide design. As the numerical aperture becomes smaller or the core diameter becomes comparable to the wavelength of the incident light, the number of supported guided modes decreases. A waveguide could be designed to only support one guided mode, or one ray with a specific incident angle. Such a waveguide is called single mode waveguide.

SMWGs are crucial for high-speed communications. The most commonly used SMWGs are SMFs, especially for long haul communications. For on–package communications, fibers are very challenging to be integrated on a package due to the size and geometry of fibers. Instead, other waveguide materials are developed for chip–to–chip communications. However, for short distances, like two chips placed right next to each other, copper wires to connect them could match the performance and with lower costs compared to optical waveguides. As the size of the board and the number of the chips on board become larger, there's a need for on–package high–speed communications. In this chapter, the limit of electronic interconnects for on–package communications, the results of modeling, design, fabrication, and characterization of polymer–based SMWGs on glass will be reported.

4.1 The Limitation of Electronic Interconnects for On-Package Communications

For electronic interconnects, wider I/O have been the direction of research and application for high-speed electronic communications. As the size of copper wires is scaled down, the density of the wires increases, and the data rate could increase as well under the right circumstances. Compared to optical signals, high–speed electronic signals suffer from issues like crosstalk, electromagnetic interference, and signal integrity, especially over a relatively long distance on the package. Hence, a quantitative analysis of signal integrity on electronic interconnects is being conducted to determine the maximum length of copper wires for wide I/O interconnects.

The modeling and simulation of copper wires as electronic interconnects in a three–

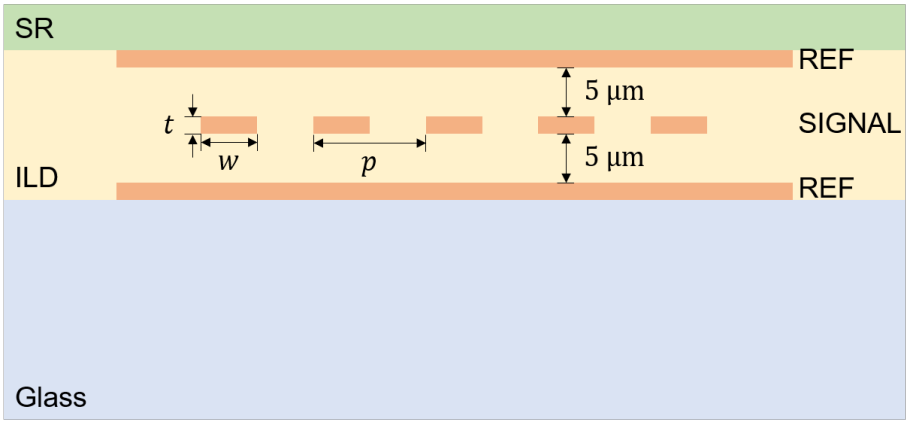


Figure 4.3: Three–metal layer stack RDL and signal layer assignment.

layer metal stack RDL on top of a glass substrate is illustrated in Figure 4.3. This simulation used a ground–signal–ground structure suitable for a stripline RDL geometry. The material properties used in this simulation are listed in Table 4.1. The glass properties were provided by Asahi Glass Company (AGC). Two thin film dielectric materials were used in the simulation. interlayer dielectric (ILD) materials serve the crucial role for the electronic performance of the transmission lines. The first material ILD–A is Ajinomoto buildup film, a widely used material in packaging industry. The second material ILD–B is a photoimageable benzocyclobutene (BCB) based dielectric film 14–P005 from DuPont Electronics & Imaging, with a lower dielectric constant and a lower loss tangent compared to ILD–A. The properties of the solder resist on top of the RDL layer is from the simulation software ANSYS™.

Table 4.1: Material properties of glass, ILDs, and the solder resist.

Material	D_f	D_k
Glass	5.3 @ 2.4 GHz	0.004 @ 2.4 GHz
ILD–A	3.2 @ 5.8 GHz	0.014 @ 5.8 GHz
ILD–B	2.59 @ 10 GHz	0.0065 @ 10 GHz
Solder Resist	3.1	0.035

ANSYS™ was used for the modeling and simulation. The module used in this work

was 2D Extractor to extract transmission line parameters resistance (r), inductance (l), capacitance (c), and conductance (g), per unit length, and characteristic impedance (Z_0) at 1 GHz. These parameters were extracted with either ILD–A or ILD–B in the stack–up. 3 variables representing the geometry were included for parametric sweep in the modeling and simulation. The variables are listed in Figure 4.3. The copper thickness (t) varies from $t = 1$ µm, 3 µm, 5 µm, 7 µm and 10 µm, and the line width (w) varies from $w = 1$ µm, 2 µm, 3 µm, 5 µm, 7 µm and 10 µm. The pitch of the copper wires are two times the linewidth. So, in all, there are 30 combinations of geometry designs. The results of the parametric study are listed in Table 4.2.

Transmission line parameters in Table 4.2 show that the resistance per unit length is dependent on the geometry of copper traces but independent of the dielectric materials. Inductance per unit length is independent of the dielectric materials since relative permeability $\mu_{\mathrm{r}} = 1$ is assumed for both dielectric materials. Capacitance per unit length is dependent on both line geometry and material dielectric properties. So is conductance since conductance is directly proportional to capacitance. The characteristic impedance decreases as the width or the thickness of copper traces increase. It is also understandable that the characteristic impedance increases with smaller dielectric constant as given by Equation 4.11 below

$$Z_{\mathrm{c}} = \sqrt{\frac{r + j\omega l}{g + j\omega c}} \tag{4.11}$$

Among all the line geometry, characteristic impedance of several designs is close to 50 Ω for satisfying the impedance matching requirements. Copper traces of 5 µm width and 5 µm thickness buried in ILD–B was selected for the next step of modeling and simulation, to calculate the maximum length of the transmission line which still preserve the signal integrity.

As the electronic signal propagates along the transmission line, the attenuation of the

Table 4.2: Transmission line parameters at 1 GHz.

		ILD–A					ILD–B				
t	w	r	l	c	g	Z_0	r	l	c	g	Z_0
µm	µm	Ω/mm	pH/mm	pF/mm	µS/mm	Ω	Ω/mm	pH/mm	pF/mm	µS/mm	Ω
1	1	18.0	567.6	77.7	6.8	181.6	18.0	567.6	62.6	2.6	202.6
	2	9.0	491.0	91.5	8.1	126.8	9.0	491.0	73.8	3.1	141.2
	3	6.1	442.2	103.1	9.1	101.5	6.1	442.2	83.0	3.5	113.1
	5	3.8	365.3	125.0	11.0	75.5	3.8	365.3	100.6	4.2	84.1
	7	2.9	311.0	147.5	13.0	61.1	2.9	311.0	118.7	5.0	68.1
	10	2.1	253.3	182.0	16.1	48.0	2.1	253.3	146.3	6.1	53.5
3	1	6.5	463.4	101.2	8.8	99.7	6.5	463.4	81.7	3.4	111.0
	2	3.3	415.4	116.3	10.3	75.2	3.3	415.4	93.7	3.9	83.8
	3	2.3	385.4	126.2	11.1	64.8	2.3	385.4	102.8	4.3	71.8
	5	1.5	331.1	146.1	12.9	53.0	1.5	331.1	117.8	4.9	59.1
	7	1.2	288.7	167.0	14.7	45.5	1.2	288.7	134.4	5.6	50.7
	10	0.9	240.4	200.5	17.7	37.6	0.9	240.4	161.1	6.8	41.9
5	1	4.2	412.1	115.9	10.0	78.5	4.2	412.1	93.8	3.9	87.4
	2	2.2	371.2	135.6	12.0	60.8	2.2	371.2	109.3	4.6	67.7
	3	1.5	348.7	145.0	12.8	54.2	1.5	348.7	118.0	5.0	60.0
	5	1.1	306.1	162.6	14.4	46.4	1.1	306.1	131.3	5.5	51.7
	7	0.9	271.4	182.9	16.1	40.8	0.9	271.4	147.5	6.2	45.4
	10	0.7	229.9	214.4	18.9	34.6	0.7	229.9	172.4	7.2	38.5
7	1	3.2	380.0	126.5	10.8	68.5	3.2	380.0	102.7	4.2	76.1
	2	1.7	341.0	151.1	13.3	53.5	1.7	341.0	121.7	5.1	59.6
	3	1.2	321.6	161.2	14.2	48.3	1.2	321.6	130.8	5.5	53.6
	5	0.9	285.7	177.8	15.7	42.3	0.9	285.7	143.4	6.0	47.1
	7	0.7	256.1	196.5	17.3	37.8	0.7	256.1	158.2	6.6	42.2
	10	0.6	219.9	226.8	20.0	32.6	0.6	219.9	182.1	7.6	36.3
10	1	2.5	348.2	137.5	11.6	60.5	2.5	348.2	112.0	4.5	67.1
	2	1.3	307.8	170.0	14.9	46.9	1.3	307.8	136.9	5.7	52.3
	3	1.0	290.3	182.1	16.1	42.6	1.0	290.3	147.7	6.2	47.3
	5	0.7	259.9	198.4	17.5	37.9	0.7	259.9	159.0	6.7	42.4
	7	0.6	235.3	214.2	18.9	34.5	0.6	235.3	171.8	7.2	38.6
	10	0.5	205.2	242.6	21.4	30.3	0.5	205.2	195.9	8.2	33.7

signal varies with frequency. For a sinusoidal signal of frequency $f = \dfrac{\omega}{2\pi}$,

$$a = \alpha + j\beta = \sqrt{(r + j\omega l)(g + j\omega c)} \tag{4.12}$$

where α is the real component of a and it represents the attenuation coefficient. To simplify the modeling and simulation, a square wave of 2 Gbps signaling was used for the calculation. A 2 Gbps square wave could be easily transformed into a sum of sinusoidal wave of 1 GHz, 2 GHz, $\cdots$, as described below

$$v(t) = \frac{4}{\pi}\left(\sin\omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t + \cdots\right) \tag{4.13}$$

The resistance (r), inductance (l), capacitance (c), and conductance (g), per unit length, of each frequency are simulated to calculate the attenuation at each frequency according to Equation 4.12 using ANSYS™. Then the amplitude of the sinusoidal signals at each frequency propagating down a certain length will be attenuated. At certain length, the sum of all the attenuated sinusoidal signals will be the distorted square wave with a significant increase in rise time. Signals at different frequencies have different propagating speed, which is described by Equation 4.14.

$$v_{\mathrm{p}} = \frac{\omega}{\beta} \tag{4.14}$$

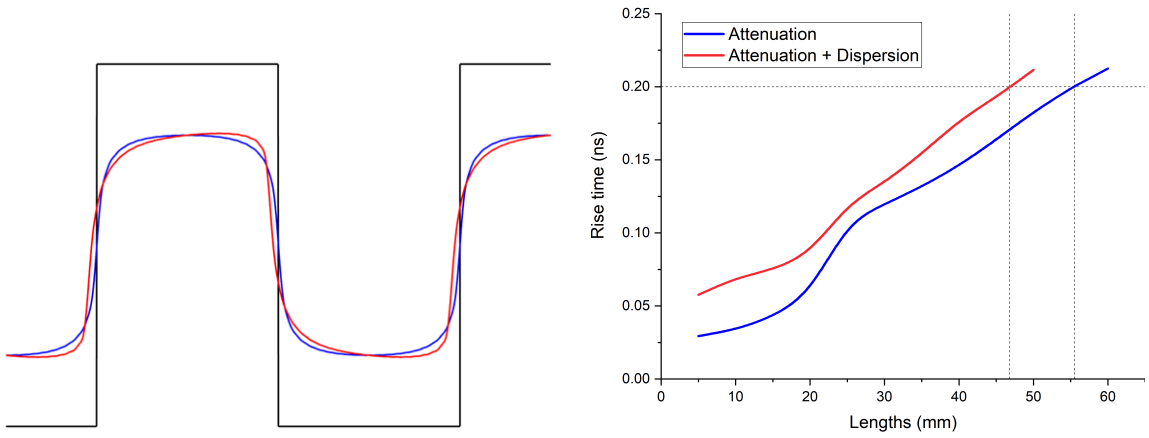
where β was defined in Equation 4.12 as the imaginary component of a. The dispersion property of transmission will distort the signal in addition to the signal degradation from attenuation. The calculation of attenuation and dispersion was done on MATLAB.

Typical timing budget for the signal rise time is 0.2 unit interval (UI), which is 0.2 ns in this situation. This will be the criteria for the maximum transmission line length analysis. The results of transmission line parameters and the calculated attenuation at each frequency are listed in Table 4.3.

Table 4.3: Transmission line parameters and attenuation coefficients from 1 GHz to 40 GHz.

f	r	l	c	g	α	f	r	l	c	g	α
GHz	Ω/mm	pH/mm	pF/mm	µS/mm	1/mm	GHz	Ω/mm	pH/mm	pF/mm	µS/mm	1/mm
1	1.1	306.1	131.3	5.5	0.0108	21	3.7	248.5	129.6	106.4	0.0446
2	1.3	290.7	130.9	11.0	0.0134	22	3.8	247.9	129.5	111.0	0.0460
3	1.4	282.2	130.6	16.4	0.0158	23	3.9	247.3	129.5	115.5	0.0474
4	1.6	276.0	130.5	21.8	0.0179	24	4.0	246.7	129.5	120.1	0.0488
5	1.8	271.4	130.4	27.1	0.0199	25	4.1	246.2	129.5	124.5	0.0501
6	1.9	267.8	130.3	32.4	0.0218	26	4.2	245.7	129.4	128.9	0.0515
7	2.1	265.0	130.2	37.6	0.0235	27	4.4	245.2	129.4	133.3	0.0528
8	2.2	262.7	130.1	42.8	0.0252	28	4.5	244.7	129.4	137.6	0.0541
9	2.3	260.8	130.0	48.0	0.0268	29	4.6	244.2	129.4	141.9	0.0555
10	2.4	259.1	130.0	53.1	0.0283	30	4.7	243.8	129.4	146.2	0.0568
11	2.6	257.7	129.9	58.1	0.0299	31	4.8	243.4	129.3	150.4	0.0581
12	2.7	256.4	129.9	63.2	0.0314	32	4.9	242.9	129.3	154.6	0.0593
13	2.8	255.2	129.8	68.1	0.0329	33	5.0	242.5	129.3	158.7	0.0606
14	2.9	254.2	129.8	73.1	0.0344	34	5.1	242.2	129.3	162.8	0.0619
15	3.0	253.2	129.7	78.0	0.0359	35	5.2	241.8	129.3	166.8	0.0631
16	3.1	252.3	129.7	82.8	0.0374	36	5.2	241.4	129.3	170.9	0.0644
17	3.3	251.4	129.7	87.6	0.0389	37	5.3	241.1	129.2	174.8	0.0656
18	3.4	250.6	129.6	92.4	0.0403	38	5.4	240.7	129.2	178.7	0.0668
19	3.5	249.9	129.6	97.1	0.0418	39	5.5	240.4	129.2	182.6	0.0680
20	3.6	249.2	129.6	101.8	0.0432	40	5.6	240.1	129.2	186.5	0.0692

The original signal, the signal after propagating 50 mm down the transmission line with the consideration of only attenuation, and the signal after propagating 50 mm with the consideration of both attenuation and dispersion are plotted in Figure 4.4. After propagating 50 mm along the designed transmission line, the voltage is only 60% percent of the original signal, and the rise time of the signal degrades significantly. Attenuation has a negative impact on the rise time, but the impact of dispersion is not clear from Figure 4.4(a). Rise times of the signal vs propagating lengths for both the attenuated signal, and the attenuated and dispersed signal are shown in Figure 4.4(b). Based on calculation and the 0.2 UI timing



(a) **(b)**

Figure 4.4: Original signal (black), attenuated signal (blue), and attenuated and dispersed signal (red).

budget, the maximum transmission line length for 2 Gbps square wave would be 55.5 mm for attenuated only signals, and 46.8 mm for attenuated and dispersed signals. Since there is no rise time for square wave in this simulation, it's safe to say, for signals in real life with a certain rise time, the maximum length of the transmission line which also meet the timing budget could only be shorter. So optical interconnects are a promising candidate for on–package communications.

4.2 Modeling and Design of Polymer–Based SMWGs on Glass

As mentioned at the beginning of this chapter, there is a need to integrate SMWGs on substrates for on–package high–speed communications. The waveguide materials along with the geometry of waveguides must be carefully designed in order to maintain single mode operation.

4.2.1 Material Selection

Glass has been drawing attention as the interposer or substrate material compared to silicon and polymer due to its low dielectric loss, tailored thermal expansion coefficient, mechanical stability, and panel processing capability. In addition, it's transparent at telecommu-

nication wavelengths 1.31 µm and 1.55 µm, which makes it a perfect candidate for optical applications as a part of optical waveguides. In this thesis, glass SGW3 from Corning Inc. is chosen as the bottom clad for SMWGs.

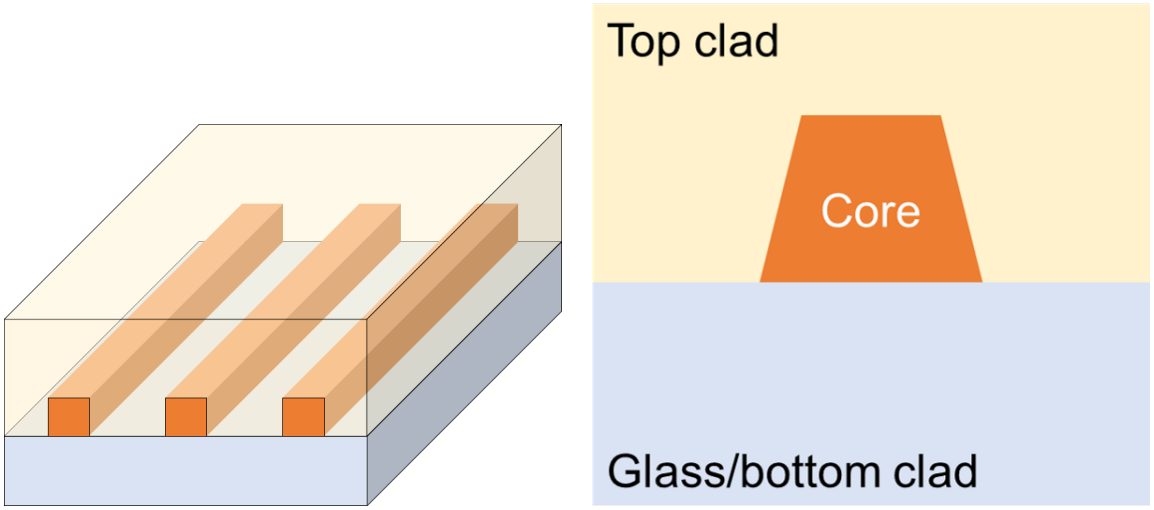


Figure 4.5: (a) A stack–up of waveguides on glass and (b) the cross section of a waveguide.

The polymer core material could be directly applied onto the glass interposer as the waveguide core with air as the top clad, but such a stack-up will lead to cores exposed to the environment so that it's susceptible of damage and accumulating dusts. So, in this thesis, the cores are buried under a layer of polymer dielectric material as the top clad and protection, as shown in Figure 4.5(a). The shape of the cross section of the core in Figure 4.5(b) is trapezoidal due to the fabrication process especially develop, which will be explored and discussed later in this chapter.

The polymer core and clad materials used in this research is CYCLOTENE^{TM} family BCB based dielectric polymer from DuPont Electronics & Imaging. BCB was chosen due to its reported low optical absorption, and high glass transition temperature. It also exhibits low dielectric constant, low dielectric loss, and high breakdown voltage for electronics application. The positive–tone high–resolution liquid PID CYCLOTENE^{TM} 6505 is used to fabricate waveguide cores, and negative–tone dry film CYCLOTENE^{TM} 14–P005 is used

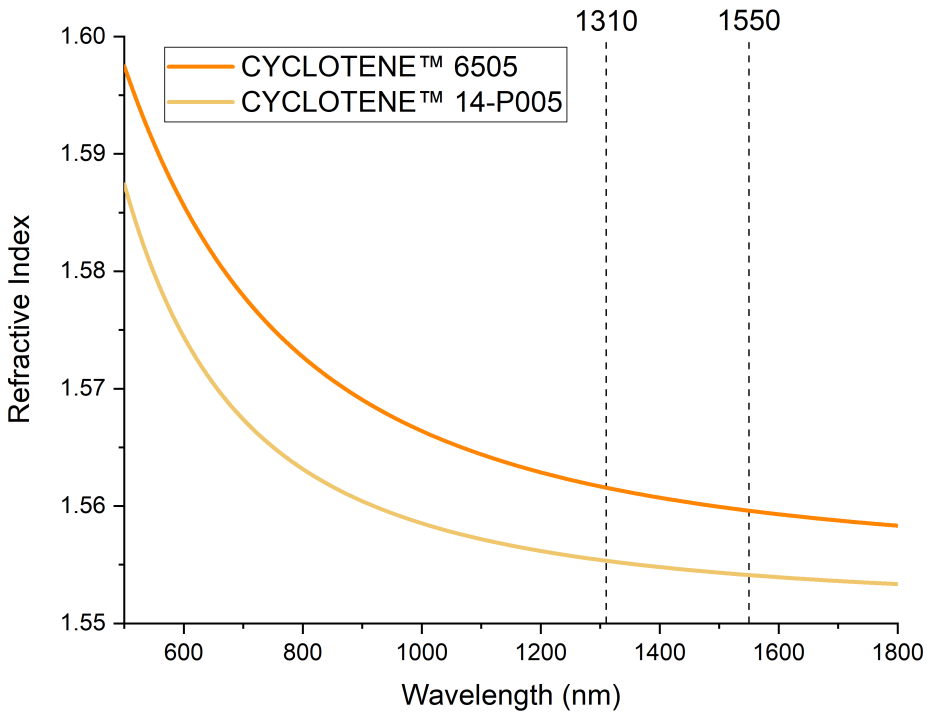


Figure 4.6: Refractive indices of the core and the clad materials.

for top clad.

Refractive indices of core and clad materials are crucial for the design and modeling of SMWGs. The refractive index of a material is wavelength dependent and it follow Cauchy's equation

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^2} + \cdots \tag{4.15}$$

where n is the refractive index, λ is the wavelength, A, B, C, etc., are coefficient that could be determined by fitting the equation to measured refractive indices at certain wavelengths. Cauchy's equation is an empirical equation, and usually it is sufficient to use two or three terms as shown below.

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^2} \tag{4.16}$$

For the optical materials used in this thesis, the coefficients were provided by the supplier DuPont Electronics & Imaging, and the data are plotted in Figure 4.6. According to the Cauchy coefficients provided by the supplier, refractive indices were calculated for two

materials at these wavelengths. However, the core material has a small absorption peak at around 1550 nm, so this thesis mainly focuses on optical measurement at 1310 nm. Some material properties for waveguides are listed in Table 4.4.

Table 4.4: Waveguide material properties.

Function	Core	Top Clad	Bottom Clad
Material	CYCLOTENE™ 6505	CYCLOTENE™ 14–P005	Corning SGW3
R. I. @ 1310 nm	1.5616	1.5553	1.4935
T_{g} / °C	$>$ 390	$>$ 350	670
CTE / ppm/°C	45	63	3
Thickness / μm	6	19	150

For optical waveguide materials, another important optical property is the birefringence. Based on information from DuPont Electronics & Imaging, CYCLOTENE™ family materials show a birefringence of less than 0.0001, which is considered negligible.

4.2.2 SMWG Geometry Design

Materials for waveguides chosen and their properties are listed in Table 4.4. Modeling and simulation were performed to design the waveguide geometry so that waveguides would be at single mode operation. The modeling and simulation were done using Electromagnetic Wave, Beam Envelope method in Wave Optics Module in COMSOL Multiphysics developed by COMSOL Inc.. The simulation setup is shown in Figure 4.7.

Due to the fabrication process, the side wall angle θ is always 70°, which indicates that the difference between the bottom width w and the top width is $2/3h$. In this setting, the height of the core is 6 μm, and the top width is 4 μm shorter than the bottom width. The modeling and simulation were focused on the impact of the bottom width on the number of guided modes supported in the design.

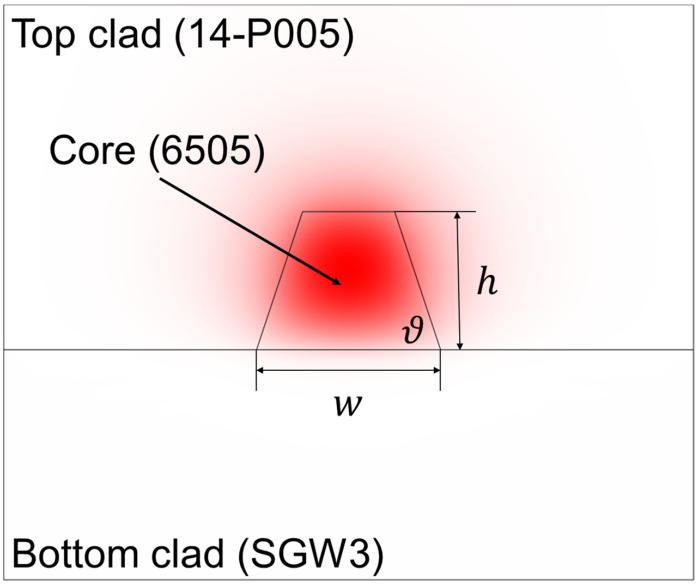


Figure 4.7: Simulation setup with the bottom width (w), height (h), and sidewall angle (θ).

There are two criteria for a waveguide to operate at single mode.

$$n_{\text{eff}} > n_{\text{clad}}, \qquad \text{for the fundamental mode} \tag{4.17}$$

$$n_{\text{eff}} < n_{\text{clad}}, \qquad \text{for all other modes} \tag{4.18}$$

where n_{eff} is the effective refractive index of a mode, which is determined by the optical properties of waveguide materials and the stack–up of the waveguide. The effective refractive index vs the bottom width for the lowest modes are plotted in Figure 4.8. And the electric fields of waveguide designs with different widths are shown in Figure 4.9.

When the bottom width is 6 µm, as shown in Figure 4.9(a), a significant portion of electromagnetic power of the fundamental mode is still outside the core. As the bottom width increase to 8 µm as shown in Figure 4.9(b) the electromagnetic wave is more confined inside the core. The waveguide operates at single mode up until the bottom width increases to 10 µm. As shown in Figure 4.9(c) and Figure 4.9(d), at 10 µm, the waveguide starts to support another mode. To avoid waveguides operating at multimode, and to avoid environmental factors attributed to the operation over the single mode threshold, 8 µm bottom

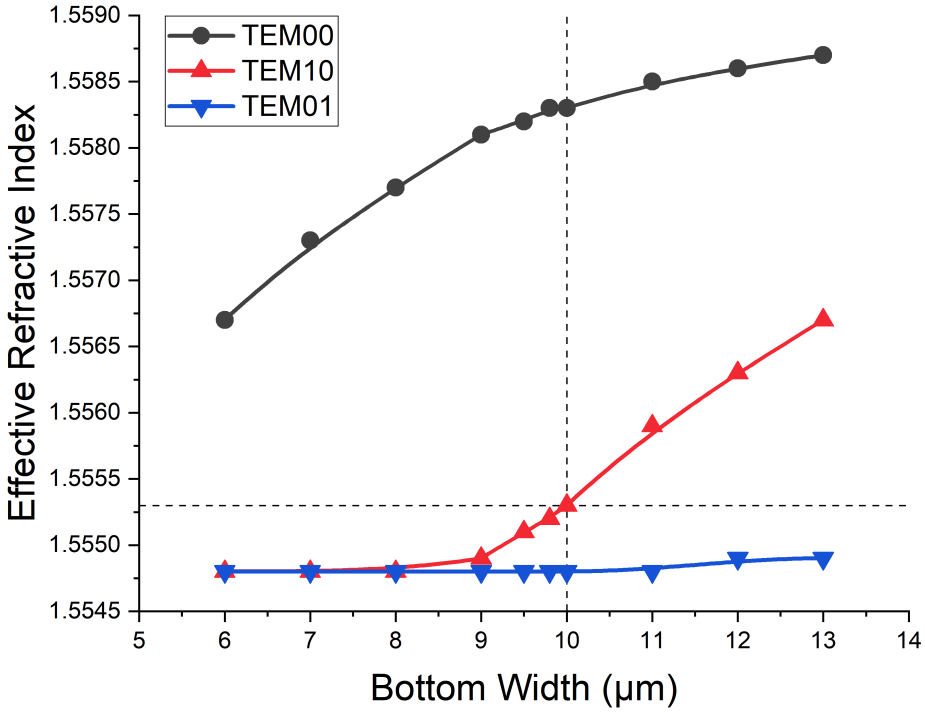


Figure 4.8: Effective refractive indices of the lowest three modes.

width is chosen as the waveguide bottom width design.

4.2.3 Coupling Analysis between Adjacent Waveguides

For high density interconnects, only one waveguide on a board is not enough. Multiple waveguides are usually designed in parallel with each other on a package to increase the number of channels for communication. However, since the electromagnetic wave is not totally confined inside the core, some of the power surrounding the core in the clad might be coupled into adjacent cores, which creates crosstalk between waveguide cores. If the electromagnetic wave propagates along one waveguide over a long distance, the full power could be coupled into the other waveguide as shown in Figure 4.10.

Waveguide cores in parallel need to be properly isolated to minimize crosstalk. There are usually two designs to minimize crosstalk, as shown in Figure 4.11. One way to isolate cores is to increase the distance between the cores as shown in Figure 4.11(a). By placing cores with a higher pitch could reduce the crosstalk but it's at the expense of interconnect

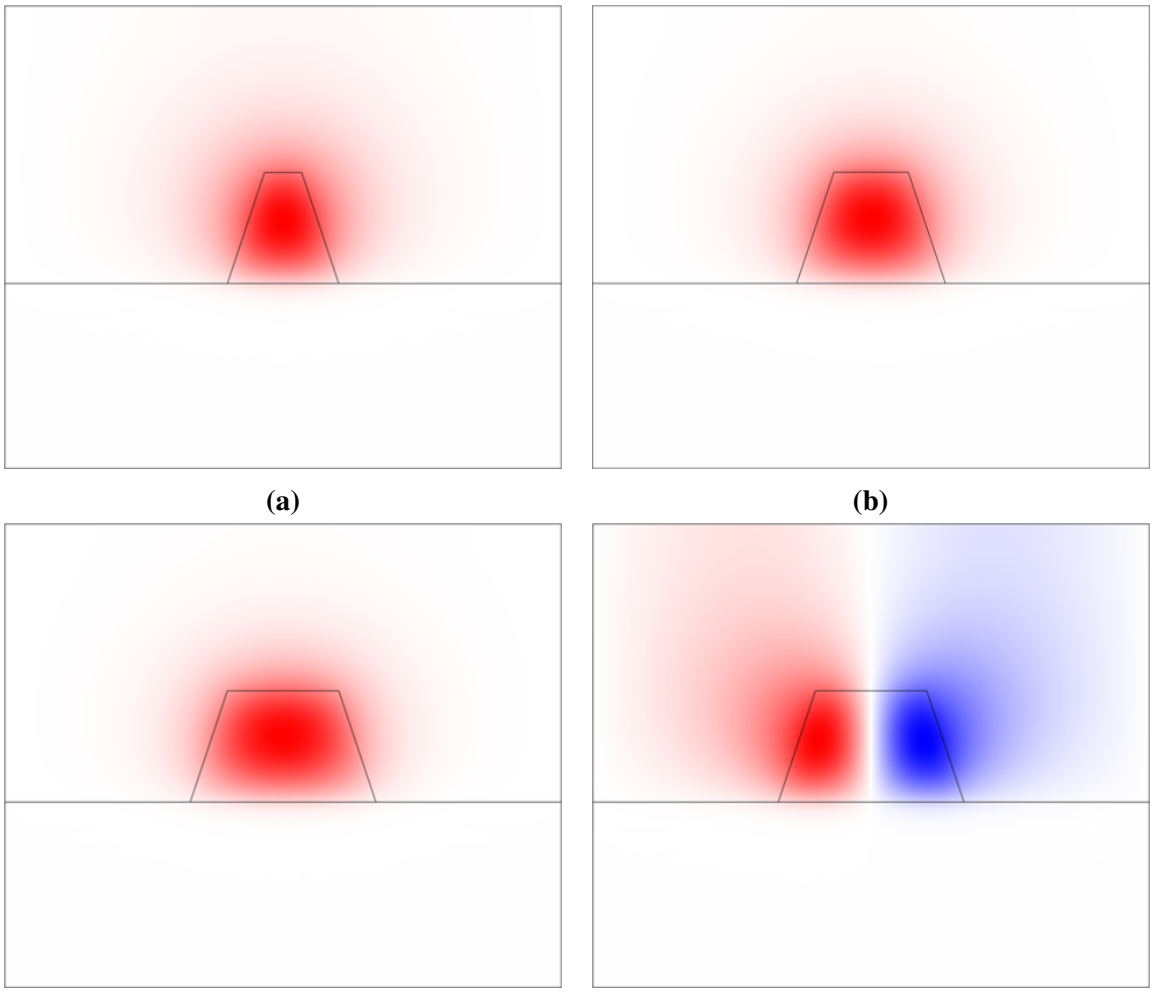


Figure 4.9: Electromagnetic fields of (a) the fundamental mode when $w = 6\,\mu m$, (b) the fundamental mode when $w = 8\,\mu m$, (c) the fundamental mode when $w = 10\,\mu m$, and (d) a higher mode when $w = 10\,\mu m$.

density. Another method to isolate cores is to introduce an air gap between clads surrounding each core. Since the refractive index of air is 1, which is very small compared to the refractive index of either the clad or the core, almost all the electromagnetic power will be confined inside the clad and the core, so power leaking from one waveguide to an adjacent one could be greatly reduced. The coupling between two cores were modeled using Beam Envelope Method in COMSOL.

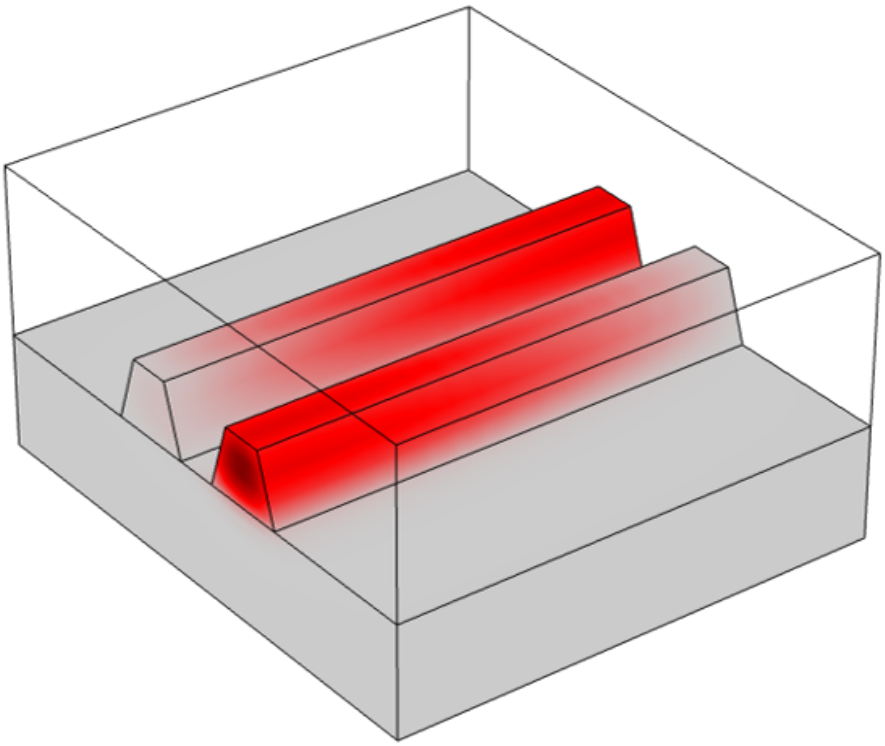
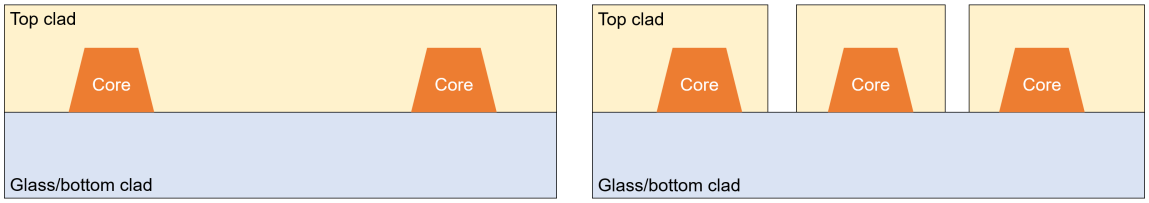


Figure 4.10: Coupling between adjacent waveguides.



(a) **(b)**

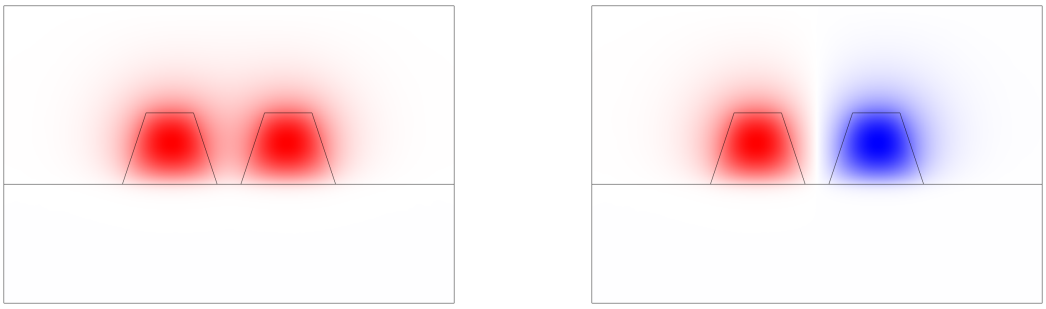
Figure 4.11: Isolate waveguide cores by (a) increasing the pitch between cores, and (b) introducing air gap between clad.

The coupling between two waveguides in close proximity could be calculated as

$$P_1 = \cos^2 \frac{\pi \Delta n L}{\lambda} \tag{4.19}$$

$$P_2 = \sin^2 \frac{\pi \Delta n L}{\lambda} \tag{4.20}$$

where P_1 is the power in the waveguide in which the electromagnetic wave is launched, P_2 is the power in the other waveguide, Δn is the difference between the effective refractive



(a) (b)

Figure 4.12: (a) Even mode and (b) odd mode propagating in two coupled waveguides with a distance of 2 µm.

index of two propagating modes, as shown in Figure 4.12, L is the coupling length, and λ is the wavelength of interest.

The even and odd modes propagate with different effective refractive indices. These could be calculated in COMSOL. In this simulation, the maximum power coupled to the other waveguide is set to be 10%. A parametric study was performed on the distance between two cores. The maximum coupling length was determined based on Equation 4.19. The results are listed in Table 4.5. It is intuitive that the coupling between waveguides becomes weaker as the distance between two cores increases, and the difference of two modes becomes smaller. So the calculated maximum coupling lengths based on data from Table 4.5 and Equation 4.19 are plotted in Figure 4.13.

The waveguide design with an air gap between clads as shown in Figure 4.11(b) isolates waveguides better than the design without air gaps in Figure 4.11(a). Based on simulation results, the coupling between two waveguides separated by an air gap is extremely low, so even a 1 µm air gap could significantly reduce the difference between the even mode and the odd mode, as shown in Figure 4.14. In this stack–up, the cores are fully encapsulated in the clads with 1 µm on each side at the bottom, and the air gap between two clads is 1 µm as well. Since the air is surrounding clads, Δn is three orders of magnitude smaller than the design without the air gap. The pitch between two cores is 11 µm in this configuration, so the density of a layer of parallel SMWG cores separated by 1 µm air gap is 90 per

Table 4.5: Refractive indices of the even mode and the odd mode for 1310 nm and 1550 nm.

Distance	1310 nm			1550 nm		
μm	n_1	n_2	Δn	n_1	n_2	Δn
0	1.557982	1.557404	0.000577	1.557660	1.554599	0.003061
1	1.557860	1.557517	0.000342	1.555387	1.554745	0.000642
2	1.557791	1.557587	0.000204	1.555303	1.554849	0.000454
3	1.557751	1.557628	0.000123	1.555245	1.554922	0.000323
4	1.557727	1.557653	7.41E-05	1.555205	1.554973	0.000232
5	1.557713	1.557668	4.49E-05	1.555176	1.555008	0.000168
6	1.557704	1.557677	2.74E-05	1.555155	1.555033	0.000122
7	1.557699	1.557682	1.68E-05	1.555140	1.555051	8.97E-05
8	1.557696	1.557686	1.03E-05	1.555129	1.555063	6.61E-05
9	1.557694	1.557688	6.35E-06	1.555121	1.555072	4.89E-05
10	1.557693	1.557689	3.93E-06	1.555115	1.555079	3.63E-05
12	1.557692	1.557690	1.52E-06	1.555107	1.555087	2.03E-05
14	1.557691	1.557691	5.91E-07	1.555103	1.555092	1.15E-05
16	1.557691	1.557691	2.33E-07	1.555101	1.555094	6.60E-06
18	1.557691	1.557691	9.22E-08	1.555099	1.555096	3.82E-06
20	1.557691	1.557691	3.68E-08	1.555099	1.555096	2.23E-06

millimeter.

However, the best resolution of the clad material reported is 3 μm, achieved by using an excimer laser which there is none in house. The best resolution of the clad material by photolithography is 20 μm by an i–line stepper, which brings the density of waveguides down to the same level of the design without air gaps. Therefore, from the perspective of in–house fabrication, the design without air gaps is chosen in this thesis, and the pitch between two cores is 250 μm, which is the same as the pitch of fiber arrays.

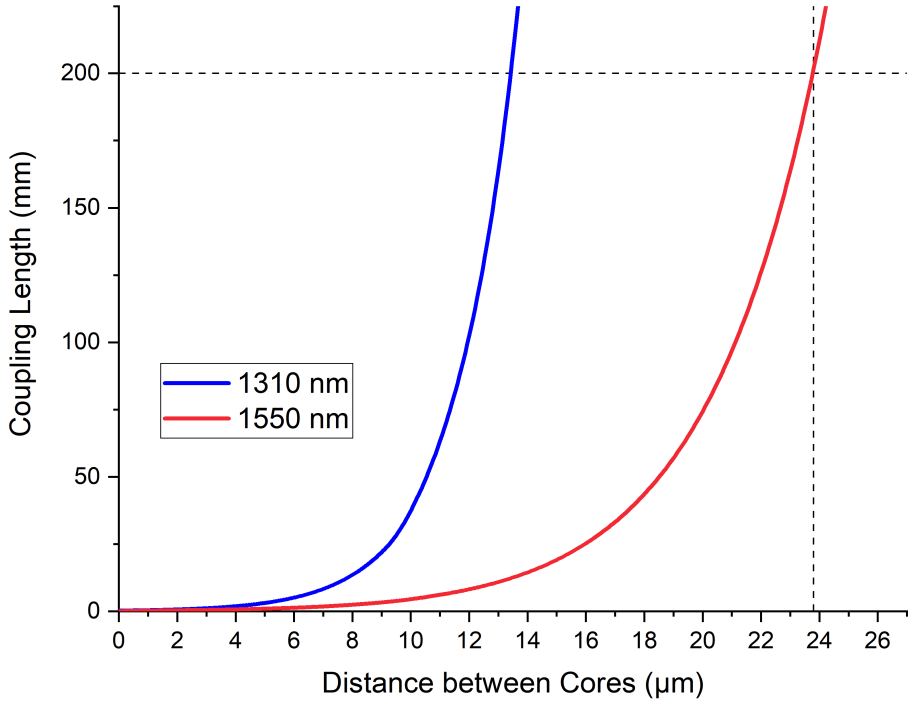
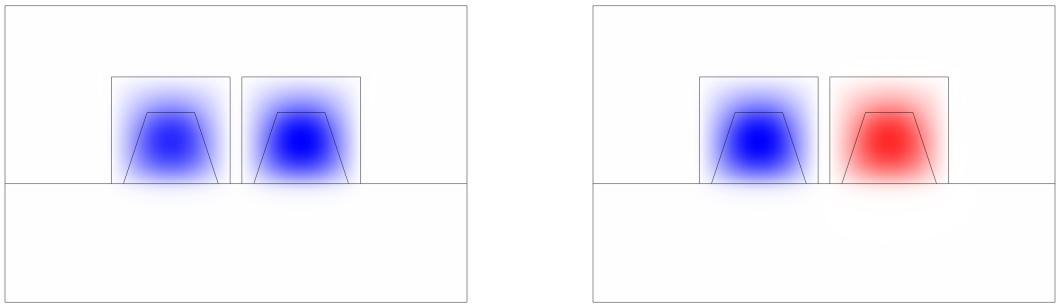


Figure 4.13: Maximum coupling lengths vs the distance between cores for 1310 nm and 1550 nm.

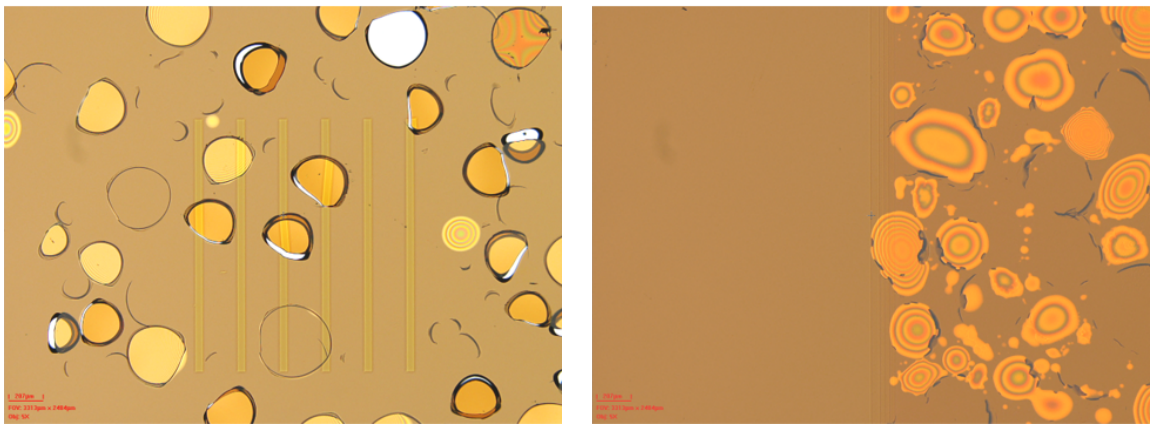


(a) **(b)**

Figure 4.14: (a) Even mode and (b) odd mode propagating in two coupled waveguides with an air gap of 1 μm.

4.3 Process Development and Fabrication

The waveguide involves three materials, a panel of glass as the bottom clad and the substrate, thin and long waveguide cores, and a layer of dielectric material as the top clad and protection layer, as shown in Figure 4.5(b). Glass panels are usually with high surface smoothness and flat. After a proper clean procedure, they are ready for the subsequent



(a) (b)

Figure 4.15: (a) Peeling after exposure. (b) Comparison of peeling on unexposed and exposed areas.

processes. The top clad is applied using a vacuum laminator. Under the already developed conditions, the clad material will be properly laminated and conformed on top of the glass panel without air bubble trapped inside. Even though the top surface might not be as flat, the top surface will be 4–13 µm away from the cores, which won't affect the performance of the cores. Fabrication of cores are very crucial for the waveguide performance since any imperfection on the cores will introduce extra loss. The fabrication of cores also involves many steps of processes, and each step need to be optimized.

4.3.1 Elimination of Defects

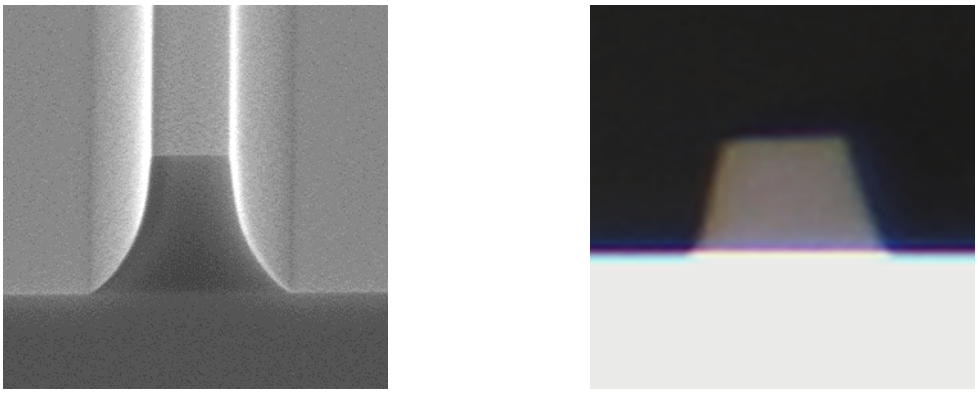
The waveguide fabrication process provided by DuPont Electronics & Imaging is shown in Table 4.6.

Several issues arose during the fabrication process while the recipe was followed, especially in the core patterning process. The first type of defects was peeling, which happened in the exposure step. An optical image of this defect is shown in Figure 4.15(a) and an optical image of the film with and without exposure for comparison is shown in Figure 4.15(b).

This type of defects was found after exposure where the exposure doses were studied. It only happened in areas with higher dosage ($> 500\,\mathrm{mJ/cm^2}$), which was higher than the

Table 4.6: The process of record on waveguide fabrication.

Process	Step	Condition
Glass substrate cleaning	Plasma clean	Plasma chamber, O_2, 100 W, 100 °C, 10 min
	Solvent clean	Acetone, methanol, IPA, DI water rinse, N_2 dry
	Drying	Hot plate, 100 °C, 2 min
Surface activation	Adhesion promoter AP9000c application	Spin coater, 2000 RPM, 45 s
	Bake	Hot plate, 150 °C, 1 min
Waveguide core patterning	CYCLOTENE™ 6505 application	Spin coater, 1250 RPM, 45 s
	Soft bake	Hot plate, 90 °C, 90 s
	Post coat delay	15 min
	Exposure	i–line stepper, 400 mJ/cm^2
	Post exposure delay	15 min
	Development	0.26 N TMAH, puddle, 60 s, DI water rinse
Cure	Thermal set	Nitrogen oven, 130 °C, 15 min
	Thermal cure	Soft cure: 200 °C, 100 min Hard cure: 250 °C, 10 min
	Descum	Plasma chamber, 4:1 O_2:CF_4, 100 W, 100 °C, 10 min
Surface activation	Adhesion promoter AP3000 application	Spin coater, 2000 RPM, 45 s
	Bake	150 °C, 1 min
Top clad lamination	Vacuum lamination	Vacuum laminator, 110 °C, 0.25 MPa, 30 s vacuum, 60 s pressure
	Exposure	i–line stepper or broadband, 100 mJ/cm^2
	Cure	Nitrogen oven, 250 °C, 100 min



(a) (b)

Figure 4.16: (a) An SEM image of a polymer line with curved sidewalls, courtesy of DuPont Electronics & Imaging, and (b) a cross-sectional optical image of a polymer line with straight sidewalls.

original recipe. After several discussions with scientists and engineers from DuPont Electronics & Imaging, it is believed that there might be some small water droplets trapped beneath the dielectric film, which were activated and vaporized under higher doses of exposure. By changing the hot plate baking condition for the glass substrate from 2 min at 100 °C to 5 min at 150 °C and optimizing the exposure dose, this type of defects was eliminated.

The second type of residues is the curved sidewalls after developing, and the top width is significantly smaller than the bottom width, as shown in Figure 4.16(a). Since there's a photoactive compound (PAC) in CYCLOTENE^{TM} 6505 and it is a positive–tone liquid material, the chemical reaction in the development process plays a significant role to understand these two phenomena, namely the curved sidewalls and the difference between the top width and the bottom width. A schematic of the development process is shown in Figure 4.17.

First the film is exposed under UV light. During this process, the UV light activates the PAC in the film, and then PAC decomposes into acidic molecules and nitrogen molecules. Then the soft bake process helps accelerate the reaction and subsequently promote the release of nitrogen. After the soft bake is done, the substrate is then cooled down and starts

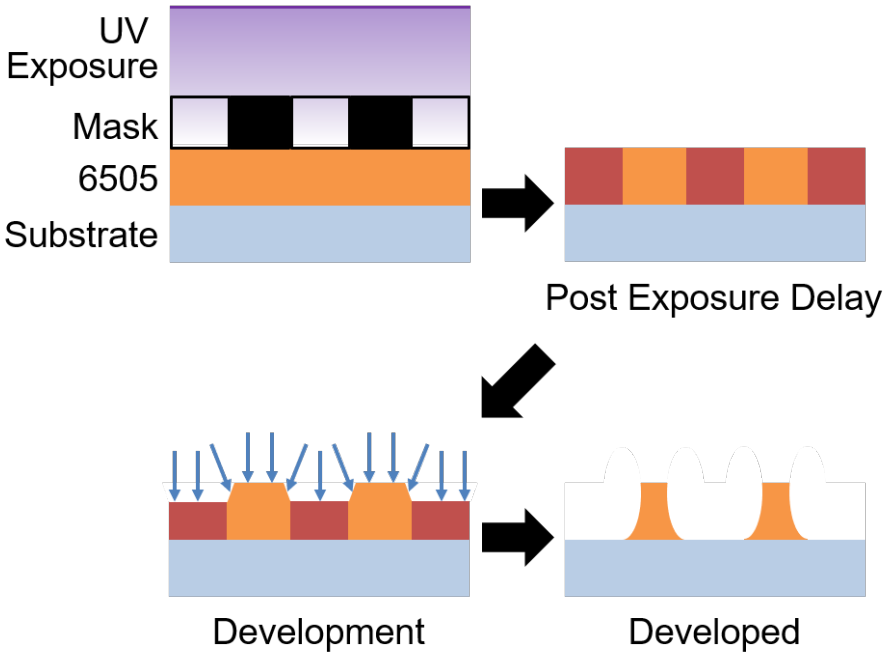
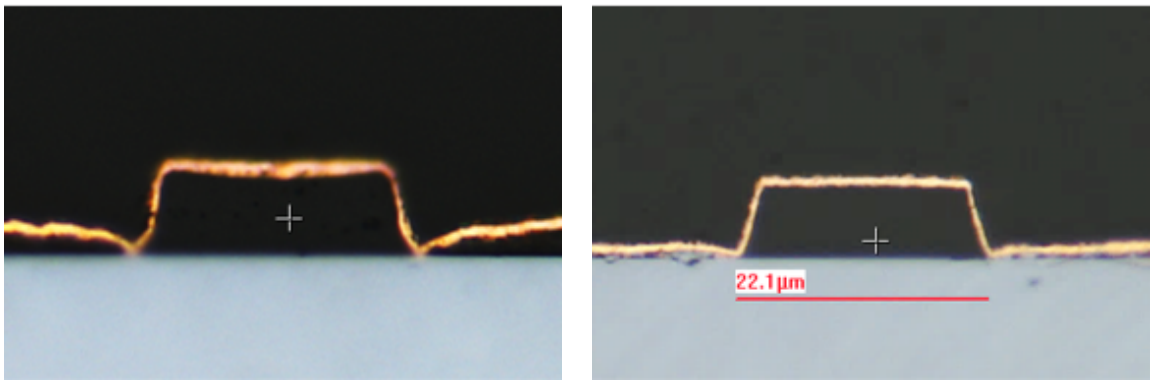


Figure 4.17: A schematic of the development process.

the puddle development process. The development of this material is essentially a neutralization of acid and base. As the developer neutralizes the acid in the exposed area, other components in the film will be dissolved into the solution. However, after the development process, the curved sidewalls emerge, and the top width is significantly shorter than the bottom width. It could be assumed that the developer is not only removing exposed areas, but also removing unexposed areas at a slower speed. However, this assumption could not fully explain the curve on the sidewall. If the developer concentration is constant, the sidewall should be straight with a sidewall angle. The curve indicates that the concentration of the developer is changing in the develop process. To keep the concentration of the developer same at all time, the puddle develop process has to be replaced with immersion with gentle agitation or spray develop. To reduce the etching on the top of the polymer lines, a less concentrated developer 0.14 N TMAH could be used instead of 0.26 N TMAH. After optimizing the develop process, the curved sidewalls become straight, and the top width increases simultaneously, as shown in Figure 4.16(b).

The third type of defects is the residue remained on the substrate after development.



(a) (b)

Figure 4.18: (a) A cross section of a developed pattern with residues, and (b) a cross section of a developed pattern without residues after optimization.

CYCLOTENE^{TM} 6505 is a positive–tone PID material, the exposed area should be etched off from the substrate in the development process. However, there were still residues after development on the substrate as shown in Figure 4.18(a).

The substrate was first sputtered with a thin layer of copper to show the shape of the pattern in a cross section. The bottom blue region in Figure 4.16 is the substrate, the orange line is the copper layer, and the black region in between is the dielectric layer. The trapezoidal shape is the designed pattern, and the dielectric residues on both side of the trapezoid need to be eliminated, otherwise when waveguide cores are fabricated, electromagnetic wave might be coupled into the residue which would impart a high propagation loss to the waveguide.

Residues emerge after development, so it could be inferred that the development time or the development method in our lab is not sufficient to remove all the exposed areas. A simple and efficient way to improve the develop process is to increase the develop time. By increasing develop time in the puddle develop process, residues could be properly removed, as shown in Figure 4.16(b). However, increasing the develop time could introduce another type of defects, which happens in the cure process. This type of defects emerges in the cure process, and could be observed by bare eyes, as shown in Figure 4.19.

As shown in the figure, patterns in certain region on the substrate exhibit diffuse re-

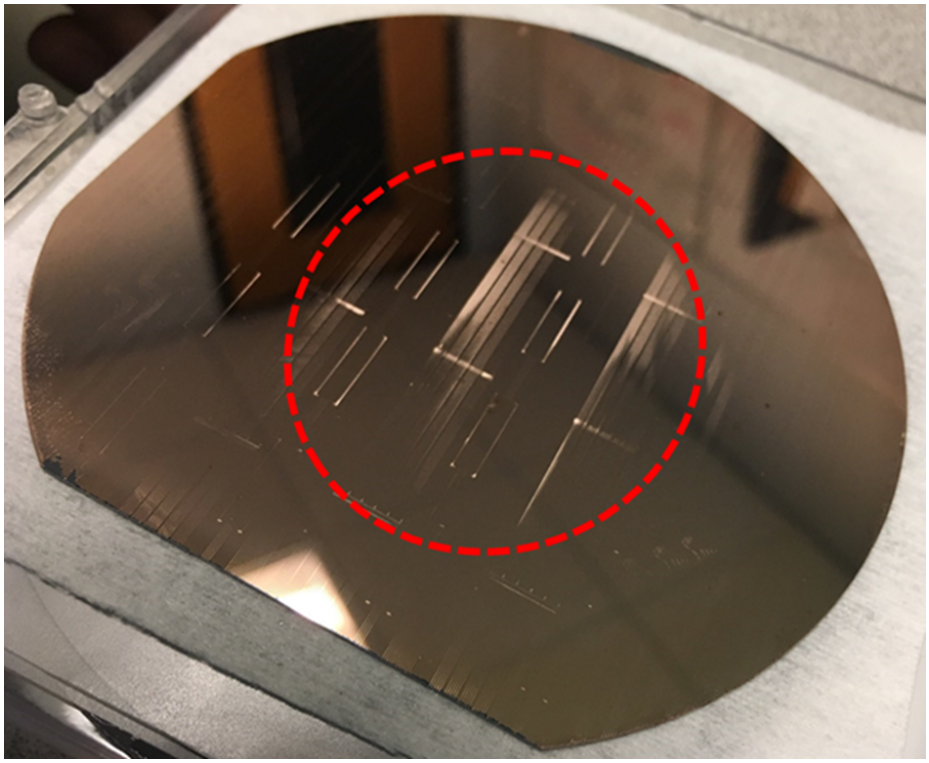
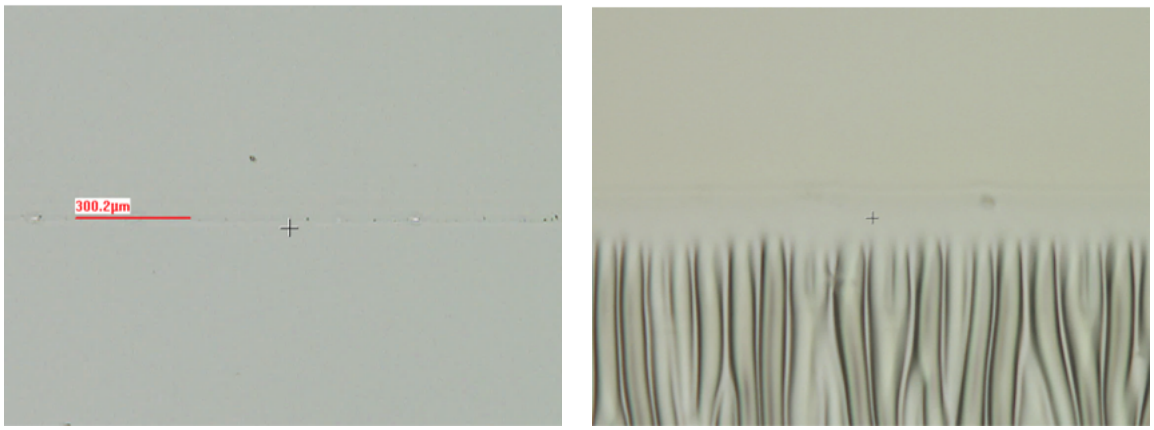


Figure 4.19: Patterns inside the red circles show diffuse reflection.

flection, which is different from patterns in other regions. It could be observed under the microscope as wrinkles at the surface. Wrinkles emerge during cure, but they do not always show up. It is believed that wrinkles are caused by overdevelopment. A wafer coated with CYCLOTENE^{TM} 6505 was divided into three regions, undeveloped, developed in TMAH solution for 60 s, and developed in TMAH solution for 120 s. The two optical images capturing the difference between two regions are shown in Figure 4.20. Figure 4.20(a) is a comparison between an undeveloped region and a region which is developed with 60 s immersion process. There is a line in the middle (at the red mark) dividing the two regions, but it is not quite clear. Figure 4.20(b) shows a comparison between an undeveloped region and the overdeveloped region, and it is distinguishable. It has not been tested but it is believed that in the extra time of overdevelopment, base molecules diffuse into the dielectric material, and it causes certain chemical reactions with components in the material at a high temperature.



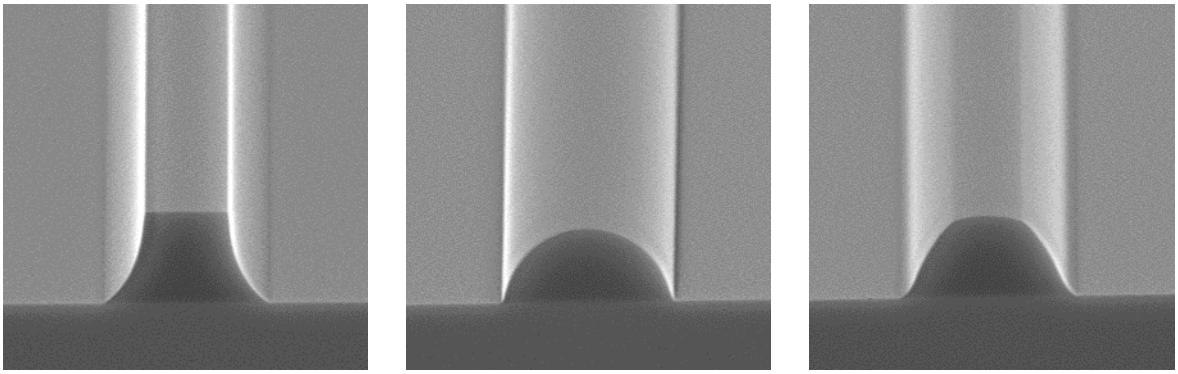
(a) (b)

Figure 4.20: (a) An optical image of the undeveloped region (bottom) and the developed region (top), and (b) an optical image of the undeveloped region (top) and the overdeveloped region (bottom).

To completely remove the wrinkles and reduce the possibility of wrinkles happening, development time is set to 60 s, and after development, the sample is placed in a water bath for 120 s. Wrinkles disappear after using this optimized development process.

Four types of defects were identified and addressed. The new process is listed in Table 4.7, and changes are marked in red.

4.3.2 Shape Control of Waveguide Cores



(a) (b) (c)

Figure 4.21: A 10 µm wide polymer line (a) after development, (b) after the original cure process, and (c) after an optimized cure process. Courtesy of DuPont Electronics & Imaging.

Table 4.7: Optimized waveguide core patterning process.

Process	Step	Condition
Glass substrate cleaning	Plasma clean	Plasma chamber, O_2, 100 W, 100 °C, 10 min
	Solvent clean	Acetone, methanol, IPA, DI water rinse, N_2 dry
	Drying	Hot plate, 150 °C, 5 min
Surface activation	Adhesion promoter AP9000c application	Spin coater, 2000 RPM, 45 s
	Bake	Hot plate, 150 °C, 1 min
Waveguide core patterning	CYCLOTENE™ 6505 application	Spin coater, 1250 RPM, 45 s
	Soft bake	Hot plate, 90 °C, 90 s
	Post coat delay	15 min
	Exposure	i–line stepper, 400 mJ/cm^2
	Post exposure delay	15 min
	Development	0.14 N TMAH, immersion with gentle agitation, 60 s, immersion in DI water, 120 s

After waveguide cores were developed, the monomers in patterned waveguide cores polymerized during cure process. The suggested cure process has two cure stage, a thermal set temperature at 130 °C, and a thermal cure temperature above 200 °C. The corners at the top after development are very sharp and clear, as shown in Figure 4.21(a). However, after following through the process, the shape of the polymer lines with straight sidewalls and sharp corners would have a round top, as shown in Figure 4.21(b). The polymer lines change from shapes with sharp features to shapes without them, so it could be inferred that the shape change is due to reflow and surface tension. Although such a process reduces the stress, consequently, enhance reliability, shape change like this will introduce extra difficulty in waveguide core design and development. By lowering the thermal set temperature and increasing the time at that temperature, thermal set could still happen without soften-

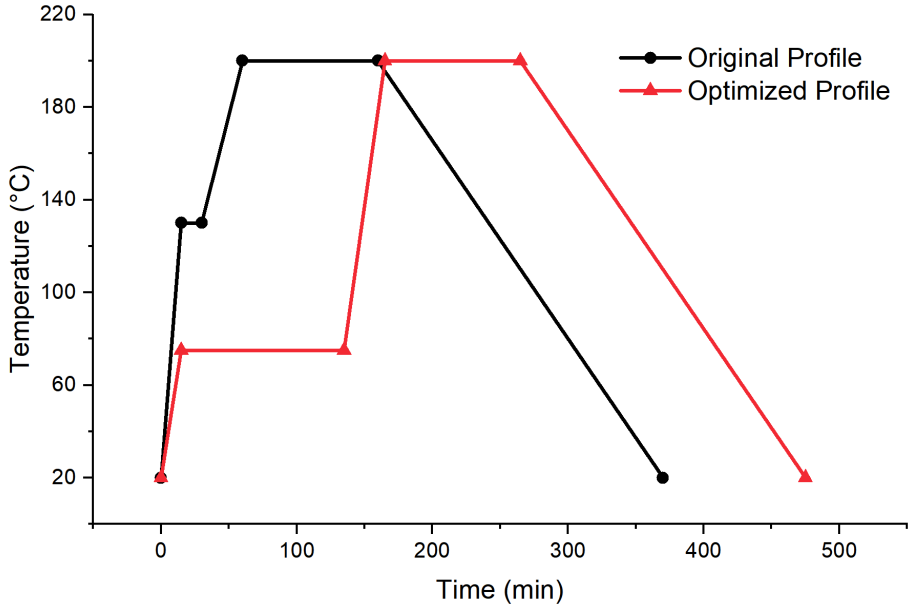


Figure 4.22: The temperature profiles of the original cure process and the optimized cure process.

ing the polymer lines to enable shape change during cure. Figure 4.21(c) shows a polymer line after cure with a thermal set temperature at 90 °C for 90 min, and the improvement is evident. However, the shape change still happened. After further optimization, 75 °C for 120 min was chosen as the thermal set condition. The cure profiles are shown in Figure 4.22, and the updated process is listed in Table 4.8.

Table 4.8: Optimized cure process.

Process	Step	Condition
Cure	Thermal set	Nitrogen oven, 75 °C, 120 min
	Thermal cure	Soft cure: 200 °C, 100 min Hard cure: 250 °C, 10 min
	Descum	Plasma chamber, 4:1 O_2:CF_4, 100 W, 100 °C, 10 min

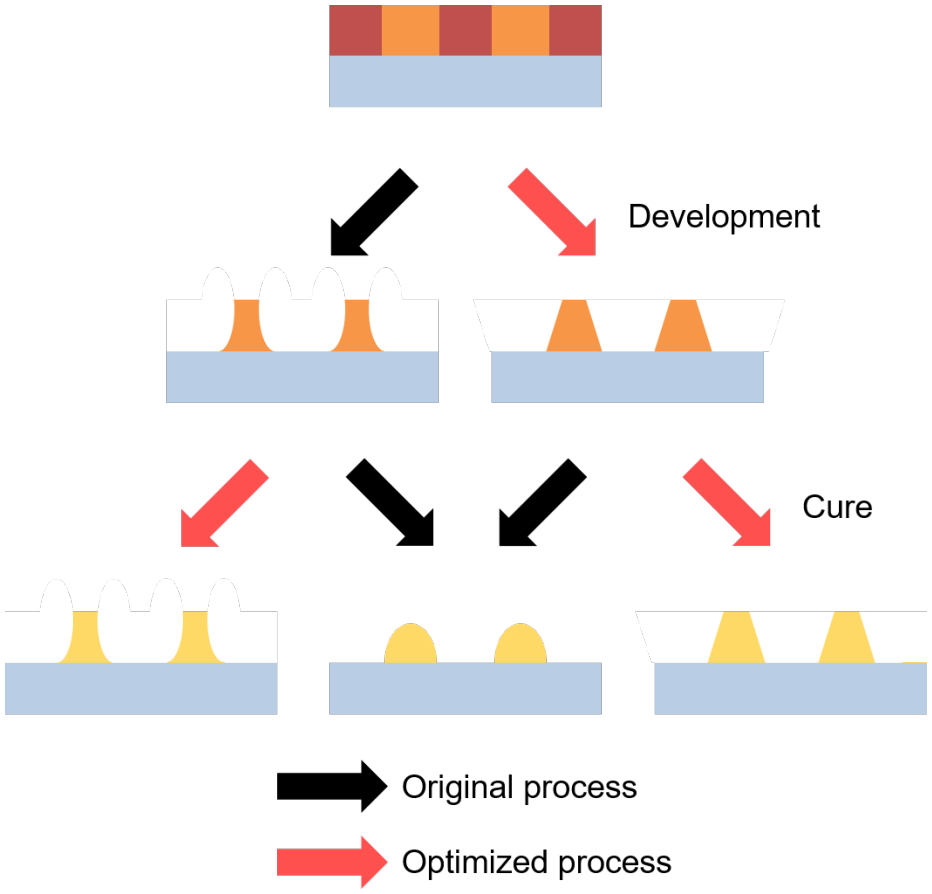


Figure 4.23: Impacts of process conditions on shape control of the waveguide cores.

4.3.3 Fabrication of SMWGs on Glass

The whole fabrication process has been optimized and summarized in Table 4.9 below, and the impact of different processes on the shape is illustrated in Figure 4.23.

SMWG cores were then fabricated using the optimized process. The cross sections of the fabricated waveguide cores are listed in Table 4.10 below. Heights and widths of the waveguide cores are the same as what they are designed to be, and the cross sections retain their trapezoidal shapes after cure, which were used for modeling and simulation earlier in this chapter. The propagation loss and data rate measurement discussed later were performed on waveguides with 8 μm bottom width cores fabricated using the optimized process.

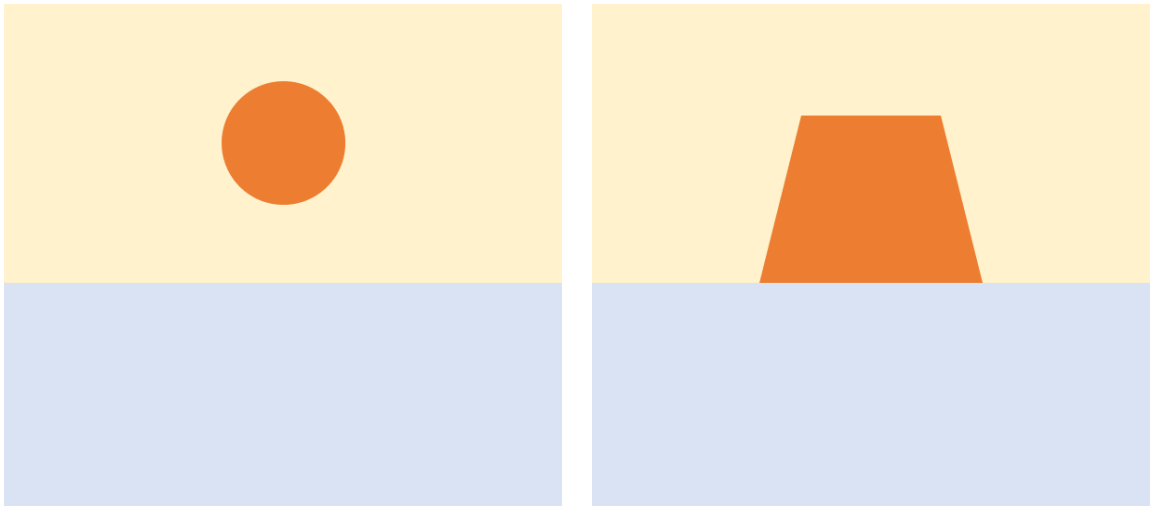
Even though the shape control was investigated to keep the shape of polymer lines the

Table 4.9: Optimized waveguide fabrication process.

Process	Step	Tool	Condition
Glass substrate cleaning	Plasma clean	Plasma chamber: Plasma Etch BT–1	O_2, 100 W, 100 °C, 10 min
	Solvent clean	NA	Acetone, methanol, IPA, DI water rinse, N_2 dry
	Drying	Hot plate: LABCONCO 728040010814	150 °C, 5 min
Surface activation	Adhesion promoter AP9000c application	Spin coater: SCS 6800	2000 RPM, 45 s
	Bake	Hot plate: LABCONCO 728040010814	150 °C, 1 min
Waveguide core patterning	CYCLOTENE™ 6505 application	Spin coater: SCS 6800	1250 RPM, 45 s
	Soft bake	Hot plate: LABCONCO 728040010814	90 °C, 90 s
	Post coat delay	NA	15 min
	Exposure	Projection aligner: Ushio UX–44101	400 mJ/cm^2
	Post exposure delay	NA	15 min
	Development	NA	0.14 N TMAH, immersion with gentle agitation, 60 s, immersion in DI water, 120 s
Cure	Thermal set	Nitrogen oven: Blue M Furnace	75 °C, 120 min
	Thermal cure		Soft cure: 200 °C, 100 min Hard cure: 250 °C, 10 min
	Descum	Plasma chamber: Plasma Etch BT–1	4:1 O_2:CF_4, 100 W, 100 °C, 10 min
Surface activation	Adhesion promoter AP3000 application	Spin coater: SCS 6800	2000 RPM, 45 s
	Bake	Hot plate: LABCONCO 728040010814	150 °C, 1 min
Top clad lamination	Vacuum lamination	Vacuum laminator: Meiki MVLP 300	110 °C, 0.25 MPa, 30 s vacuum, 60 s pressure
	Exposure	Mask aligner: TAMARACK 152–1000–20	100 mJ/cm^2
	Cure	Nitrogen oven: Blue M Furnace	250 °C, 100 min

Table 4.10: Cross sections of fabricated waveguides.

Cross section				
Design width (μm)	7.0	8.0	9.0	10.0
Actual width (μm)	7.0	8.0	9.0	10.1
Height (μm)	6.0	6.0	6.0	6.0

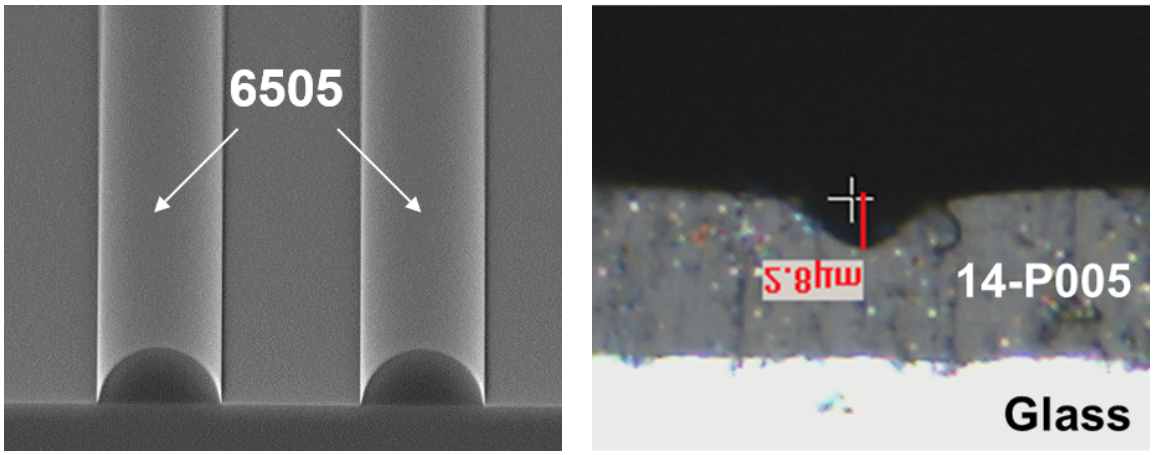


(a) **(b)**

Figure 4.24: Schematic cross sections of (a) a circular core waveguide and (b) a trapezoidal waveguide.

same before and after cure, polymer lines with round tops could also be used to fabricate waveguide cores. A new type of waveguide cores, circular cores, was proposed, as shown in Figure 4.24(a). In circular core waveguides, cores are buried in the top clad layer. The geometry of such waveguides is similar to SMFs. The dimension of circular cores to maintain the single mode operation is determined by

$$V = \frac{2\pi \times a \times NA}{\lambda} < 2.405 \tag{4.21}$$



(a) (b)

Figure 4.25: Two crucial parts for circular core SMWGs, (a) round top of the core, courtesy of DuPont Electronics & Imaging, and (b) semi-circular trench from the clad.

where V is the normalized frequency, which has to be smaller than 2.405 for single mode operation, a is the radius of the core, NA is the numerical aperture defined in Equation 4.10, and λ is the wavelength of interest. The maximum diameter of the core determined by Equation 4.21 is 5.6 µm for single mode operation.

For circular core SMWGs, the top round shape is from the reflow of the core in the cure process as shown in Figure 4.25(a), and the bottom round shape is inspired by the semi–circular trench in the clad layer after exposure and develop, as shown in Figure 4.25(b).

The fabrication of circular core SMWGs involves two steps. The first was the fabrication of semi–circular trenches in the clad. After the dry film 14–P005 was laminated on top of the glass substrate, the film underwent photolithography. Since the width of the trench is smaller than the resolution of the film, which is around 20 µm, the fine features wouldn't be fully resolved, and they could not completely shield the underneath material from exposure. After smaller features were transferred to the film by UV exposure, the developer could not fully penetrate the whole layer down to the substrate, and it had to stop in the middle of the film, which created a semi–circular trench.

The second step was the core fabrication. CYCLOTENE^{TM} 6505 was coated on a developed 14–P005 film with trenches on it. Then the film was patterned in the same way

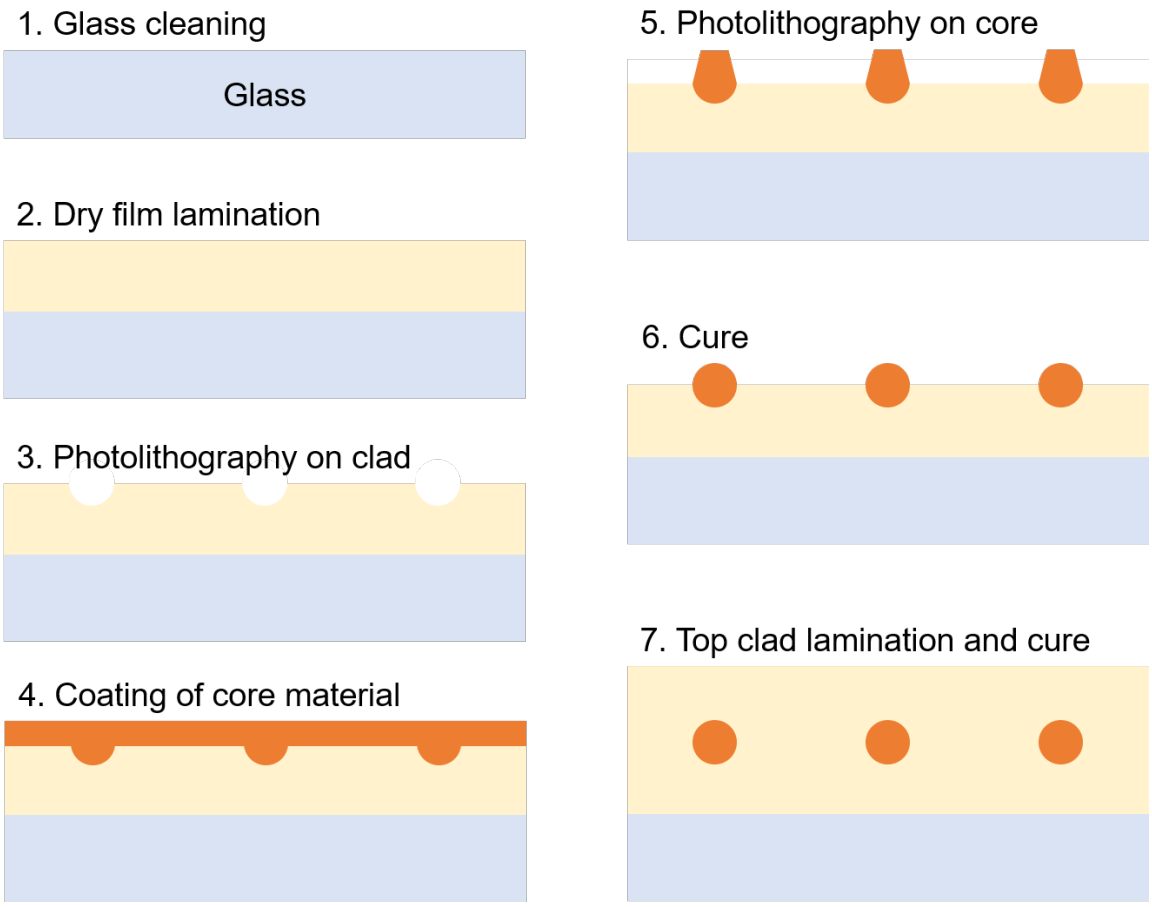
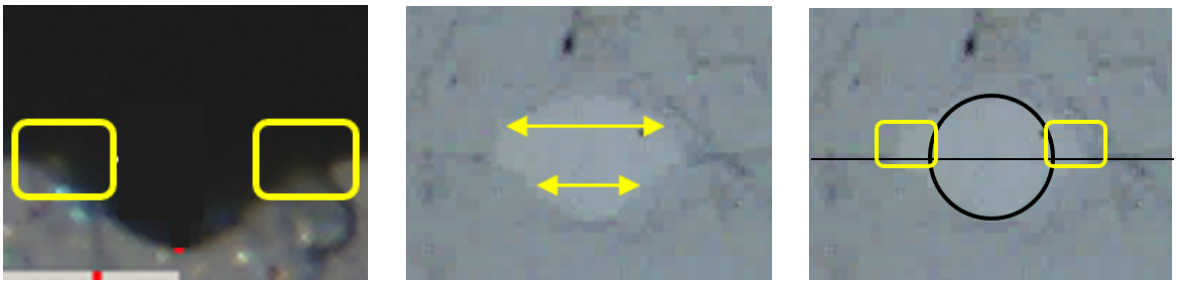


Figure 4.26: Process flow of circular core waveguide fabrication.

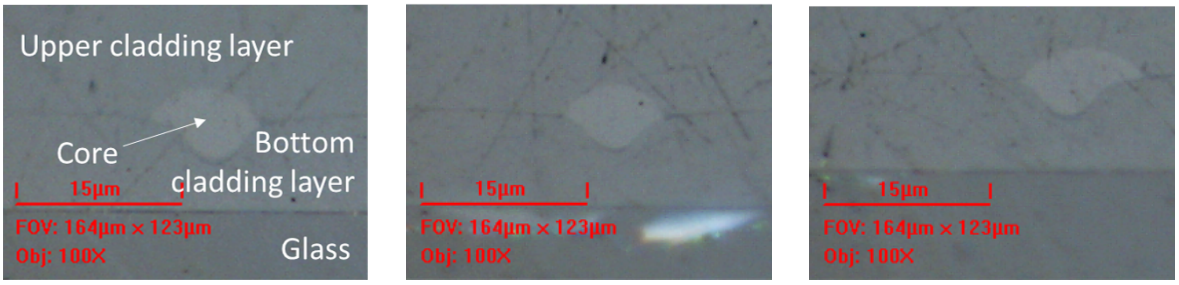
it is patterned for trapezoidal core fabrication. The patterned core layer was then developed and cured with the original process so that the surface tension and reflow would lead to round tops. Another layer of dry film 14–P005 was laminated on top of the cured core layer with round tops, and cured again to serve as protection and top clad. The process flow is shown in Figure 4.26.

Fabrication of circular core SMWGs is extremely challenging, and there are three aspects. The first challenge is the structural issues with semi–circular trenches. As shown in Figure 4.27(a), the shape of the trench roughly follows normal distribution curve, which is not perfectly circular and leaves two long tails on both sides of the trench. This is due to the develop process and reflow of the dry film. It might be addressed by carefully designed develop process and temperature control on the cure process, but since the chemistry in



(a) (b) (c)

Figure 4.27: (a) Long tails on both sides of the trench, (b) difference in widths between the top half of the core and the bottom half of the core, and (c) width expansion of the core.



(a) (b) (c)

Figure 4.28: Cross sections of a waveguide at different locations. (a) A right–skewed core, (b) a no–skew core, and (c) a left–skewed core. © 2017 IEEE

the dry film is different than the liquid, temperature control in the cure process might not work. The depth of the trench is 2.8 µm, same as the design, however the full width at half maximum is smaller than that of a semi–circular trench.

The second challenge is the geometry of the top half of the core. With careful spin speed adjustment, the core height could be controlled to be 2.8 µm as designed. However, the top half of the core is wider than the bottom half of the core as shown in Figure 4.27(b), and the core would expand due to surface tension during cure so the whole core is larger than the designed circular as shown in Figure 4.27(c).

The last and most challenging issue is the alignment of the core to the trench. The mask for photolithography on the core and the clad usually contains thin and long patterns up to 9 cm. The alignment tolerance of the core to the trench is less than 1 µm over 9 cm, which is a very high requirement for the alignment tool. Cross sections of a waveguide at different

locations are shown in Figure 4.28. The core goes from right–skewed to left–skewed along the waveguide. Assuming both the core and the trench are straight, it is clear that the core and the trench is not parallel. This tilt is unacceptable for optical communication since it will introduce tremendous propagation loss. This issue could be addressed with alignment tools with higher accuracy, but it is still extremely challenging for most tools.

Facing so many challenges, circular core SMWGs were not pursued. Trapezoidal core SMWGs were used for the subsequent characterization steps.

4.4 Characterization of SMWGs on Glass

After waveguides were fabricated, characterization of SMWGs which includes propagation loss measurement and data rate measurement were performed on waveguides.

Optical loss is defined as

$$\mathrm{Loss(dB)} = 10 \log \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} \tag{4.22}$$

There are two parts in the optical insertion loss, one is the loss due to the propagation through the waveguide which includes the absorption coefficients of the materials and the roughness of the core surface, the other is the coupling loss caused by reflection at the interface and the coupling. The loss due to propagation through the waveguide is dependent on the length of the waveguide while the coupling loss is not, so it is easy to separate these two types of losses by measuring insertion losses of waveguides with different lengths. The cut back method was used for propagation loss and coupling loss measurement. In the cut back method, the insertion loss of a long waveguide is measured, then it is cut short and measured again, until enough insertion losses with regard to its lengths are gathered for the subsequent linear regression to calculate the slope as the propagation loss, and the intercept as the coupling loss. A variant to the cut back method is to fabricate waveguides with different lengths instead of cutting one waveguide short again and again. This way the

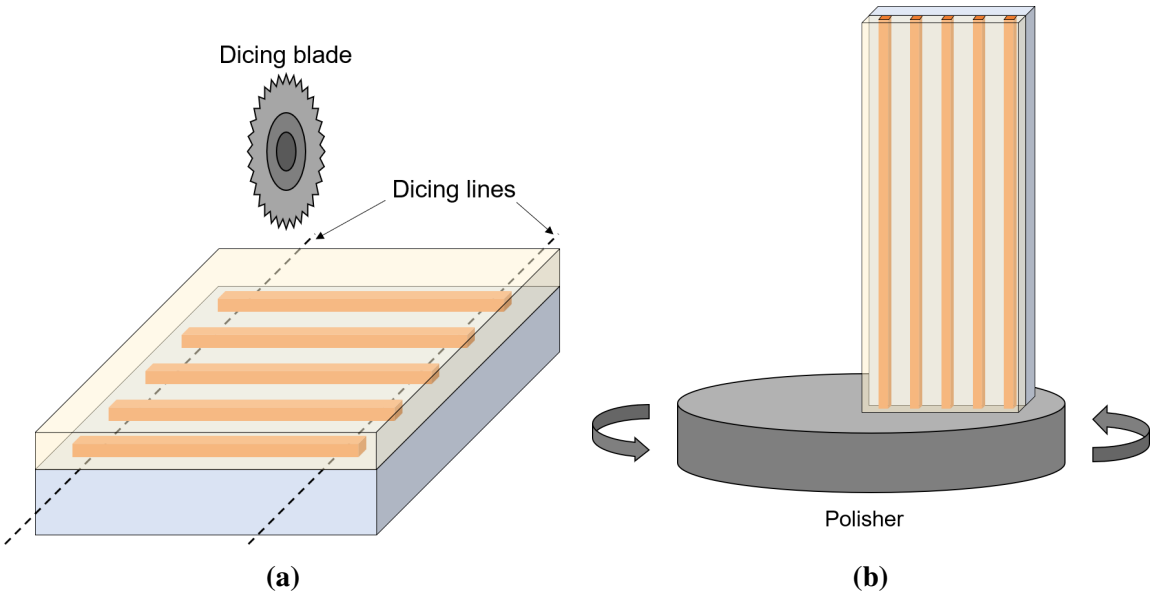


Figure 4.29: Sample preparation for waveguide characterization: (a) dicing of waveguides to expose ends for coupling, and (b) polishing of the edge to improve coupling.

measurement could be reproduced without damaging samples.

4.4.1 Sample Preparation for Characterizations

After final cure of the top clad in waveguide fabrication process, waveguides are fabricated but they are not ready for the measurement since the waveguide ends are far away from the edge of the substrate due to fabrication restrictions. Further steps are required to prepare the waveguide samples for the measurement. Traditional sample preparation steps are cutting the sample so that both ends of the waveguides are exposed for fiber coupling, and then polishing the exposed waveguide ends to optical smoothness, as shown in Figure 4.29.

There are three issues with the traditional sample preparation steps on the polymer–on–glass type waveguides fabricated in this study. First is that polishing might break the sample due to the brittleness of glass as substrates. Since the polishing is manual, samples need to be held tightly to address the constant lateral force from the polishing table. A sudden external force or large particles on the polishing surface might break the sample. In order to make the sample robust, thicker glass substrates (300 µm) were used, and a silicon

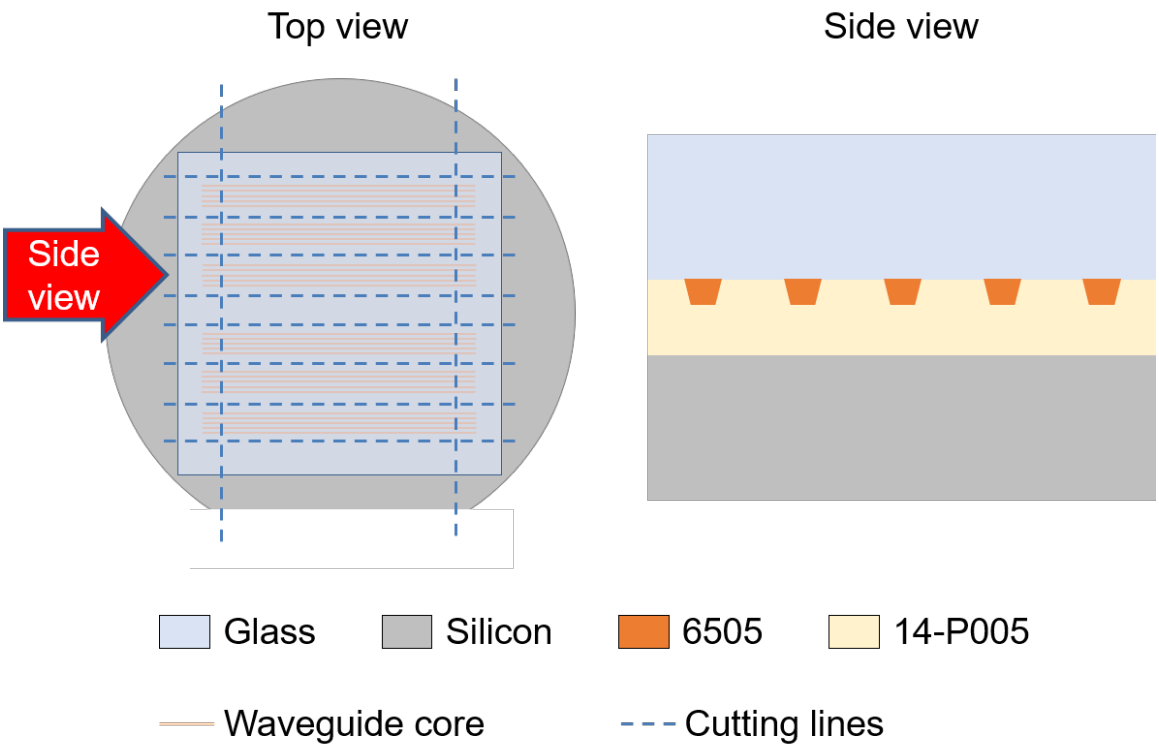


Figure 4.30: Process flow of circular core waveguide fabrication.

wafer is bonded on top of the polymer layer to form a sandwich structure as protection for waveguides, as shown in Figure 4.30. Since glass is transparent, waveguide cores are still visible for inspection and alignment through glass from the top.

The second issue is the difference in hardness between polymers and glass or silicon plays an important role on the edge quality of the waveguides, which in turn affects the coupling efficiency. The waveguide layer is composed of polymers, which are softer than either glass or silicon. When the sample is being polished, the polishing particles on the polishing paper or the polishing felts would remove polymers faster than other materials. Eventually, there will be a concave surface at the edge for samples without silicon wafer bonding as shown in Figure 4.31(a). The bonded silicon wafer improves the edge quality as shown in Figure 4.31(b), but it does not solve the issue completely.

The last issue with manual polishing of the waveguide sample is the polishing quality control of the edge. The geometry of the edges varies due to different polishing pressures,

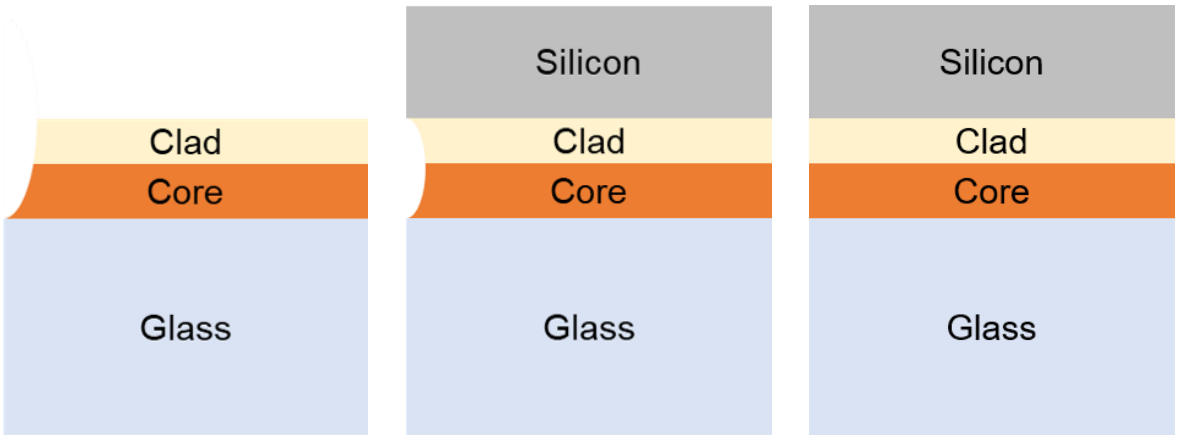


Figure 4.31: Schematics of side views of (a) a concave edge on a polymer–on–glass sample, (b) a concave edge on a sandwiched waveguide sample, and (c) a flat edge on a sandwiched waveguide sample.

polishing angles, durations, etc. These factors will cause a huge variation on the quality of the edge, which in turn affects the waveguide measurement. To address the second and the third issues, a sample preparation method without polishing was proposed and developed. By only dicing the sample without the subsequent polishing, the challenges from manual polishing would be completely removed. Since the dicing saw is operating at 30 000 RPM and the particle on the dicing saw is small enough, the dicing quality is better than dicing and polishing. The comparison is shown in Figure 4.32. A cross section of a diced and polished sample is shown in Figure 4.32(a). The image is focused on the surface of the glass, and it is clear that the core and clad layer is out of focus, which indicates more materials are removed in the polishing process, as shown in Figure 4.32(c). Since the polymer layer is sandwiched between a silicon wafer and a glass substrate, the concave surface would preserve the scratches and contamination like polishing particles inside. The geometry of the surface and the defects inside the concave surface will negatively impact the coupling efficiency in the measurement. A cross section of a diced only sample is shown in Figure 4.32(b) as a comparison. It is evident that the edge surface of the glass is shattered due to its brittleness. However, the polymer layer is still in focus, and the

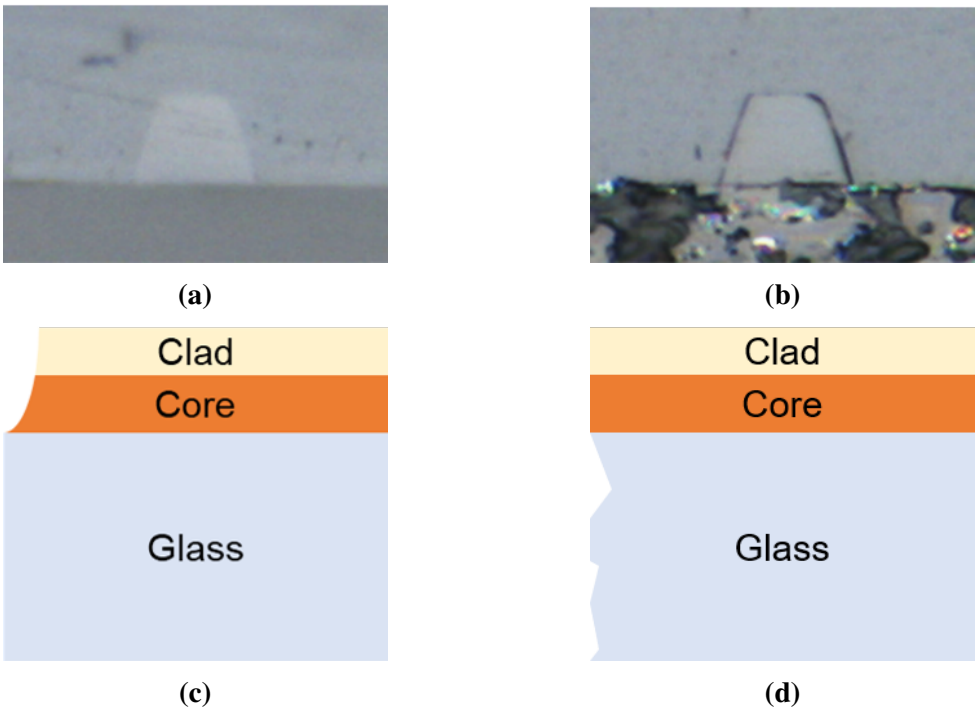


Figure 4.32: (a) A cross section of a diced and polished sample, (b) a cross section of a diced only sample, (c) a schematic side view of the diced and polished sample, and (d) a schematic side view of the diced only sample.

contamination is not as serious as the diced and polished sample. The edge quality of the diced only sample is better than the diced and polished sample.

So, after the waveguides were fabricated, the waveguide sample was bonded on a silicon wafer with the same clad material 14–P005. This step could be combined with top clad lamination to reduce the fabrication complexity. The sandwiched sample was then diced using Disco DAD3360 automatic dicing system into long slabs of waveguide samples with both ends of waveguides exposed to the air. No polishing process is needed after the dicing process. Waveguide samples with different lengths then underwent insertion loss measurement.

4.4.2 Measurement of Propagation Losses

Insertion losses are the values measured manually in this measurement. The measurement setup is shown in Figure 4.33. The whole measurement system was setup on a vibration

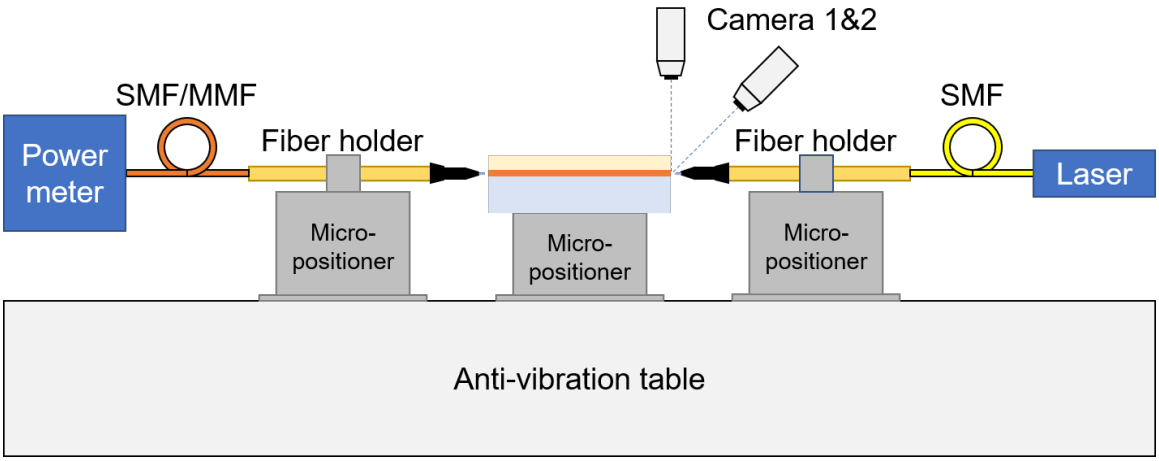


Figure 4.33: A schematic of the insertion loss measurement setup.

isolation table. A laser source at 1310 nm was connected to a SMF, or a lensed SMF for better coupling, as a power input. The input fiber was assembled in a fiber holder, which was held by a micro–positioner, Newport 561D ULTRAlign^{TM} stage. This micro–positioner provides control in x, y, z, θ_y, and θ_z directions with 1 µm sensitivity. The tip of the lensed fiber was then aligned to the waveguide core in the waveguide sample sitting on a micro-positioner Newport 462 with control in x, y, z directions. At the other end of the waveguide core after the laser beam propagates along the waveguide, the beam was coupled out of the waveguide and into a fiber. This fiber could be a SMF or a multimode fiber (MMF). The type of the fibers does not affect the measurement significantly, but using a MMF could help increase the measurement speed. This fiber was assembled in a fiber holder held by another micro–positioner Newport 561D, and the other end of this fiber was connector to a power meter to measure the power output from the waveguide.

In the measurement process, the alignment is the crucial step for better coupling and better measurement consistency. There are two alignment locations, the lensed SMF to the waveguide, and the waveguide to the MMF. At both alignment locations, two cameras were used visually align the fiber to the waveguide. As shown in Figure 4.33, the top camera was used for alignment in the x and z directions, and the side camera was used for alignment in the x and y directions. First, the input fiber was brought close to the sample in

the z direction using the top camera. Then θ_z was adjusted so that the fiber parallel to the waveguide. The position of the fiber in the x direction was then adjusted so that the tip of the fiber is aligned to the waveguide core. Since the sample is a sandwiched structure and the polymer layer is around 20 μm thick, the polymer layer is identifiable in the side camera for the tip of the lensed fiber to be repositioned in the y direction in that range. However, the resolution of the camera and the extremely close refractive indices of the core and the clad materials make it impossible to see the core from the camera. θ_y was also adjusted using the side camera. θ_y and θ_z were adjusted only in the visual alignment process. The same process was used to align the output MMF to the waveguide core too, but there was no tip at the end of the MMF, so visually align it to the waveguide core was challenging. However, the large core diameter in the MMF means the alignment does not have to be accurate to get a good coupling. Unlike the alignment of the lensed fiber to the waveguide core whose alignment window is within 2 μm in both x and y directions, alignment of the MMF to the waveguide core has an alignment window an order of magnitude larger than that.

After the visual alignment, both fibers were roughly aligned to the waveguide. The laser connected to the lensed fiber was then powered up for the further fine adjustment by hand. By turning the knobs to adjust the fiber position in x and y directions, within an approximately 2 μm range, the power meter showed a sudden increase in output power. By finer adjustment on both fibers, the optimum output was located.

The actual insertion loss measurement involves two parts. The first part was the measurement of the power out of the lensed fiber, as the zero point. The alignment was the same as the process mentioned above but instead of aligning both fibers to the waveguide, the alignment for the measurement of the zero point was to align the lensed fiber to the MMF. Then waveguide samples of different lengths were inserted in between the lensed SMF and the MMF, and the power meter measured the output power through the waveguides. Insertion loss values are the zero–point power minus the measured output powers

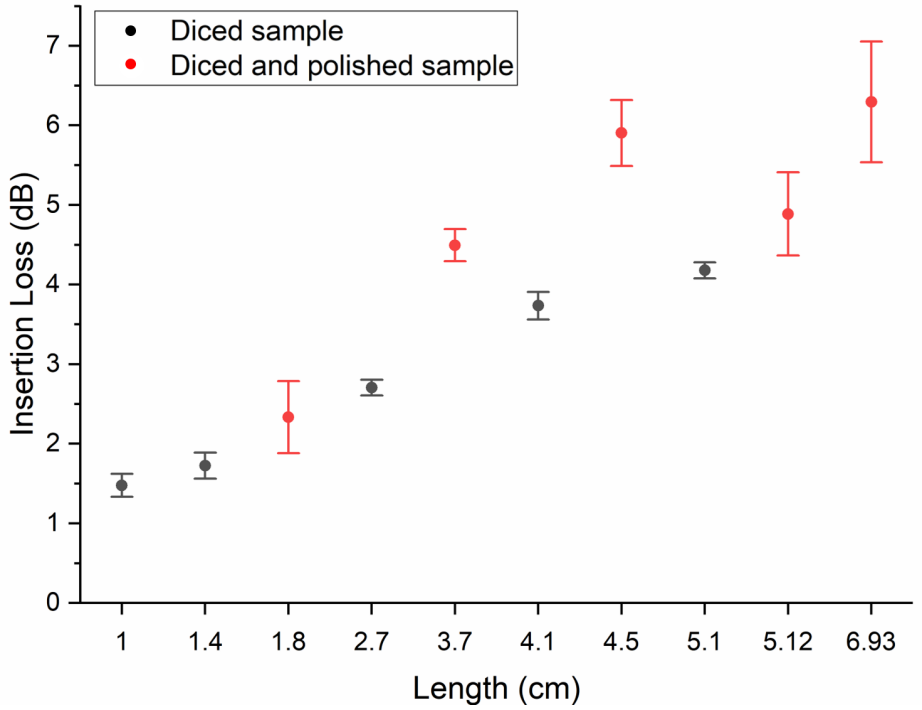


Figure 4.34: Measured insertion losses of waveguide samples.

through waveguides of different lengths. The measured insertion loss values are plotted in Figure 4.34. At each length, multiple waveguides were fabricated. However, several fabrication defects were found under visual inspection. These defects consist of dirt on the core and voids in the core, which adversely impact the waveguide performance. The selected well fabricated waveguides were used for insertion loss measurement.

Comparing the measurement for both diced sample and diced and polished sample from Figure 4.34, one can infer that insertion losses of waveguides on diced only sample are more consistent than those on diced and polished sample. Figure 4.35 shows the calculated propagation loss and coupling loss of waveguide samples using linear regression on the averages of measured insertion losses at each length. The propagation losses of the diced only samples and diced and polished samples are 0.68 dB/cm and 0.61 dB/cm, respectively, which are close. However, the coupling losses of the diced only samples and diced and polished samples are 0.41 dB/facet and 1.18 dB/facet, respectively. It is evident that the manual polishing has negative impact on the surface quality which subsequently increases

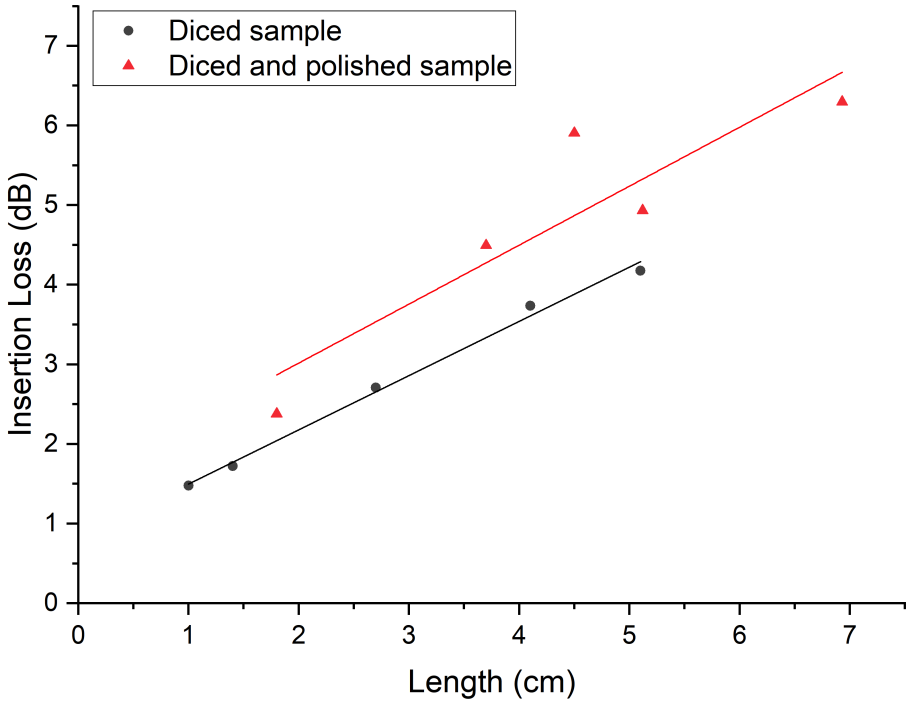


Figure 4.35: Calculated propagation losses and coupling losses of waveguide samples.

the coupling loss. Compared to previous work reported by our group [25], the coupling loss has been reduced from 1.3 dB/cm down to half of it, however, compared to the state–of–the–art polymer waveguides, the propagation loss of the fabricated waveguides is still relatively higher. There are several reasons behind this. First, the cleanroom and the tools especially the oven used to fabricate these waveguides might not be clean enough for optical applications. Second, the absorption of the glass substrates might be high since it's not designed specifically for telecommunication purpose. Third, the sensitivity of the micro–positioners and the manual operation on the high-accuracy requirement in alignment might negatively affect the measured results. The measurement here in this thesis is a time–consuming active alignment tool operated manually. By replacing manual operation with computer controlled active alignment, the measurement could be more efficient with higher accuracy.

One index matching liquid to reduce coupling loss was also investigated. The liquid used is Norland Optical Adhesive 81 (NOA81), and the refractive index of the cured

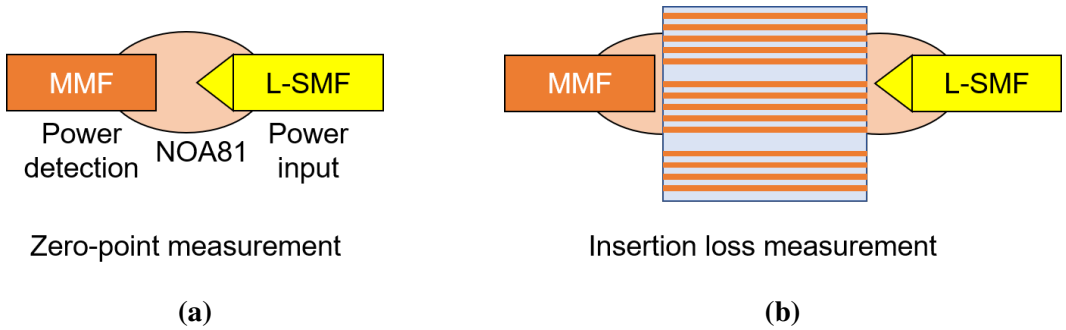


Figure 4.36: (a) Zero–point measurement with the index matching liquid, and (b) insertion loss measurement with the index matching liquid.

polymer is 1.56. The index matching liquid was added at both input and output coupling locations between the fiber and the waveguide, as shown in Figure 72. For zero-point measurement as shown in Figure 4.36(a), adding NOA81 enhanced power transmission by 0.1 dB, which is a negligible improvement. However, for insertion loss measurement on waveguides as shown in Figure 4.36(b), adding NOA81 worsened the coupling efficiency. Several factors could cause this phenomenon. First, the refractive index of the liquid is unknown, so even though the cured polymer has a refractive index close to the fiber or the waveguide materials, the uncured liquid might not match. Second, the liquid is a viscous fluid with surface tension. After the fibers were aligned to the waveguide without the liquid, adding the liquid would pull the fiber away from the aligned position due to surface tension. Another alignment process is needed, but due to the viscosity of the liquid, there is a delay between adjusting the fiber using the micro–positioner and the fiber tip moving to the aligned position. The feedback was instant without the liquid, but with the liquid at the gap, it took some time for the power meter to show a stable output. Several approaches could be pursued to reduce the coupling loss in the future. Using an automatic polishing tool could potentially reduce the deviation caused by manual operation. Alternative index matching liquids could be investigated for such applications instead of the one used in this research. Computer controlled active alignment could also help to find the optimal position of the fibers for the best coupling.

4.4.3 Measurement of Data Rates

Waveguides fabricated on glass are designed to replace electronic interconnects for on–package communications due to the attenuation and dispersion on copper wires over a long distance. Optical communication systems usually have a broader bandwidth compared to electronic communication. Such a broad bandwidth lead to higher data rates. Data rates supported by the fabricated waveguides were also characterized in this thesis.

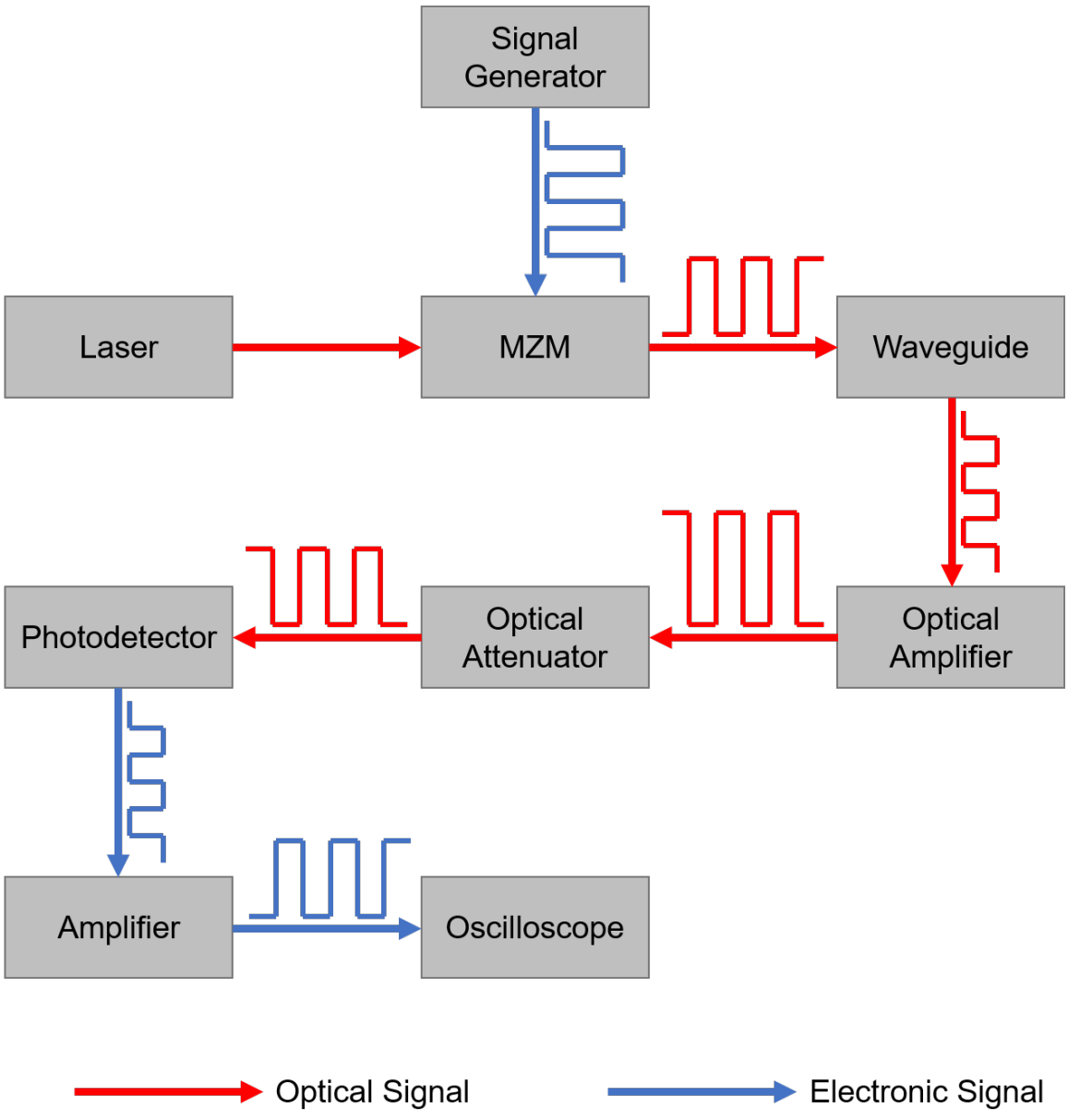


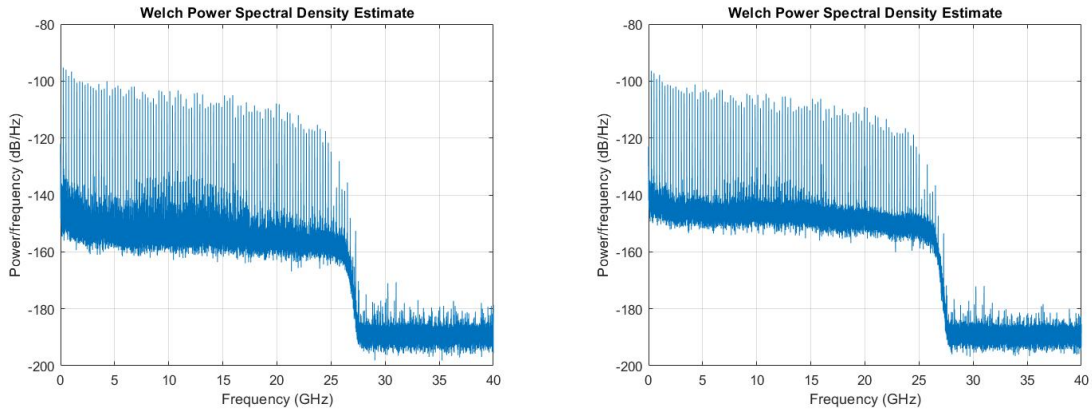
Figure 4.37: Device setup for data rate measurement.

The measurement system is set up is shown in Figure 4.37. A continuous wave laser at 1550 nm was powered on, and it was connected to a Mach–Zehnder modulator (MZM). Electronic signals generated from a signal generator were transmitted into the MZM for signal modulation. The modulated optical signal then propagated through a lensed SMF aligned to a fabricated waveguide. Then another SMF aligned to the output side of the waveguide was connected to an optical amplifier to amplify the optical signal. Then a power monitor/attenuator was connected after the amplifier to monitor the optical power so that the input power through the attenuator to the photodetector would not exceed the allowed maximum. After the photodetector converted the optical signal into the electronic signal, it was connected to a signal amplifier to increase the electronic signal power for the oscilloscope. Details of the devices used for the measurement are listed in Table 4.11.

Table 4.11: Devices used in the data rate measurement.

Device	Manufacture	Model	Critical Parameters
Laser	Pure Photonics	PPCL100	Wavelength:1550 nm
Signal generator	Keysight	M8195A	Bandwidth: 25 GHz Sample rate: 64 GSa/s
Modulator	JDS Uniphase	100–13001 Alpha 1	Bandwidth: 40 GHz
Waveguide	–	–	–
Optical amplifier	Amonics	AEDFA–13–B–FC	–
Optical attenuator	EigenLight	410	–
Photodetector	u2t	XPDV2120R	Bandwidth: 50 GHz Wavelength: 1550 nm
Amplifier	SHF AG	810	Bandwidth: 40 GHz
Oscilloscope	Keysight	DSOZ254A	Bandwidth: 25 GHz Sample rate: 80 GSa/s

The bandwidth of the waveguides was measured first. For passive optical components like waveguides, bandwidths are usually very high compared to electronic components.



(a) **(b)**

Figure 4.38: Sample preparation for waveguide characterization: (a) dicing of waveguides to expose ends for coupling, and (b) polishing of the edge to improve coupling.

A multitone test was performed on the whole system with and without the waveguide to test the frequency responses of the system and the waveguide. The results are shown in Figure 4.38. Figure 4.38(a) indicates that the system without the waveguide supports modulation up to 25 GHz, which is the limit of the signal generator and the oscilloscope. The frequency response with the waveguide in Figure 4.38(b) shows that the system with the waveguide inserted supports bandwidth up to 25 GHz too, which proves that the bandwidth of the waveguide is larger than 25 GHz and it won't be the limiting factor for modulation and data rates.

The modulation for data rate measurement was on–off keying (OOK). Since the sampling rate of the signal generator is 64 GSa/s, and the measurement requires at least 2 measuring points per bit, the maximum data rate that could be generated by the signal generator is 32 Gbps. Due to accuracy concern, 3 points per bit was selected for the maximum data rate measurement, which brought the maximum data rate that could be generated to 21.3 Gbps. The eye diagrams of the measurement are shown in Figure 4.39.

In Figure 4.39(e), the eye is still open at 21.3 Gbps. It is evident that the waveguide supports data rates up to 21.3 Gbps error free with OOK modulation. It must be noted that the potentially supported data rate could be much higher but there are several factors limiting

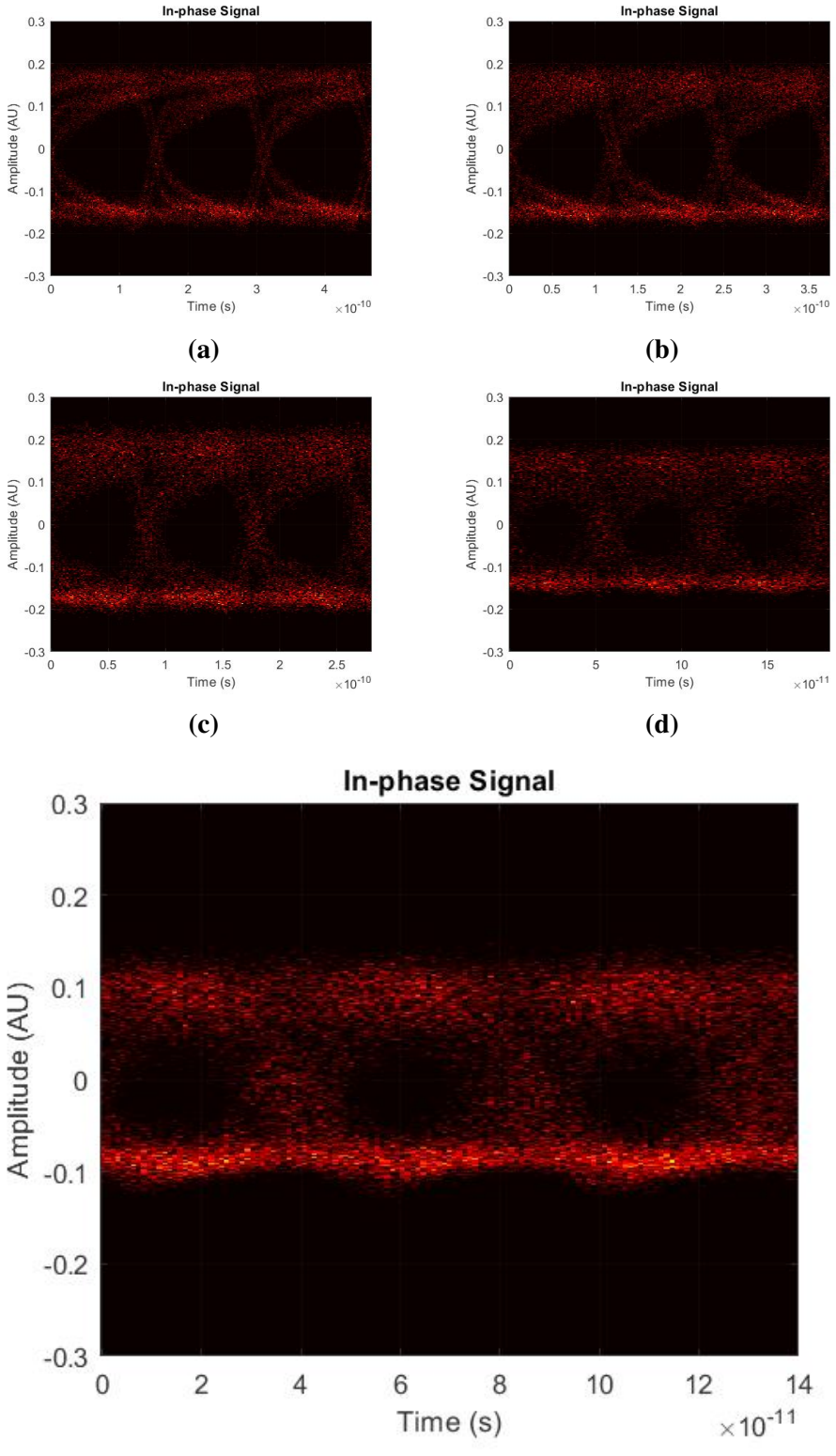


Figure 4.39: Eye diagrams at data rates of (a) 6.4 Gbps, (b) 8.0 Gbps, (c) 10.7 Gbps, (d) 16.0 Gbps, and (e) 21.3 Gbps.

the maximum data rate measurement. The first is the bandwidth supported by the system is limited by the components, especially the signal generator and the oscilloscope. In the multitone test, the signal generator can only generate signals up to 25 GHz, and the waveguide can support even higher bandwidths. With better signal generators, modulators, photodetectors, and oscilloscopes, the potential of the waveguide could be measured. The second is the wavelength used for the measurement. Since there is no available photodetector at 1310 nm in the lab, measurement could only be done at 1550 nm, where the waveguide materials have an absorption peak. The insertion loss at 1550 nm is 10 dB higher than the insertion loss at 1310 nm, which adversely affects the signal–to–noise ratio (SNR), which subsequently prohibits advanced modulations for higher data rates. All these limitations are from the tool availability in the lab, which could not be addressed by the time the thesis is being written.

4.5 Summary

Polymer–based single mode optical waveguides on glass for on–package communications were investigated in this chapter. For electronic interconnects, a 2 Gbps signal on a transmission line was analyzed and the maximum length it could propagate without the rise time increasing beyond 0.2 UI is 50 mm. Optical interconnects should be considered to replace electronic interconnects beyond 50 mm. The SMWGs fabricated on glass consists of a trapezoidal core fabricated using CYCLOTENE^{TM} 6505 photosensitive liquid, a top clad fabricated using CYCLOTENE^{TM} 14–P005 dry film dielectric, and a bottom clad, SGW3 glass from Corning Inc.. Coupling of two closely placed waveguide cores has been analyzed and the maximum density of waveguides is 31 per millimeter. The propagation loss of the fabricated waveguides after extensive process optimization is around 0.6 dB/cm at 1310 nm, which is brought down from 1.3 dB/cm according to the previous work in our group. It is still relatively high possibly due to the contamination on the surface of the core. The coupling losses of the diced only samples and diced and polished samples are

0.41 dB/facet and 1.18 dB/ facet, respectively. It is evident that manual polishing adversely affects the coupling between fibers to the waveguides, and it also increases deviation on measured values.

Data rates were also measured on a data transmission system through fabricated waveguides. The maximum data rate measured is 21.3 Gbps which is limited by the bandwidths of other components in the system and the measuring wavelength. The potentially supported data rate could be much higher with proper measurement equipment.

CHAPTER 5

FIBER COUPLING AND INTEGRATION ON GLASS

For an optical communication system, signals propagating into the board or out of the board require fiber connections. Fibers need to be connected to either an active optical device like lasers or photodetectors, or other passive components like another fiber or waveguides on package. In either case, fiber alignment is required to achieve low coupling losses for fiber coupling and integration.

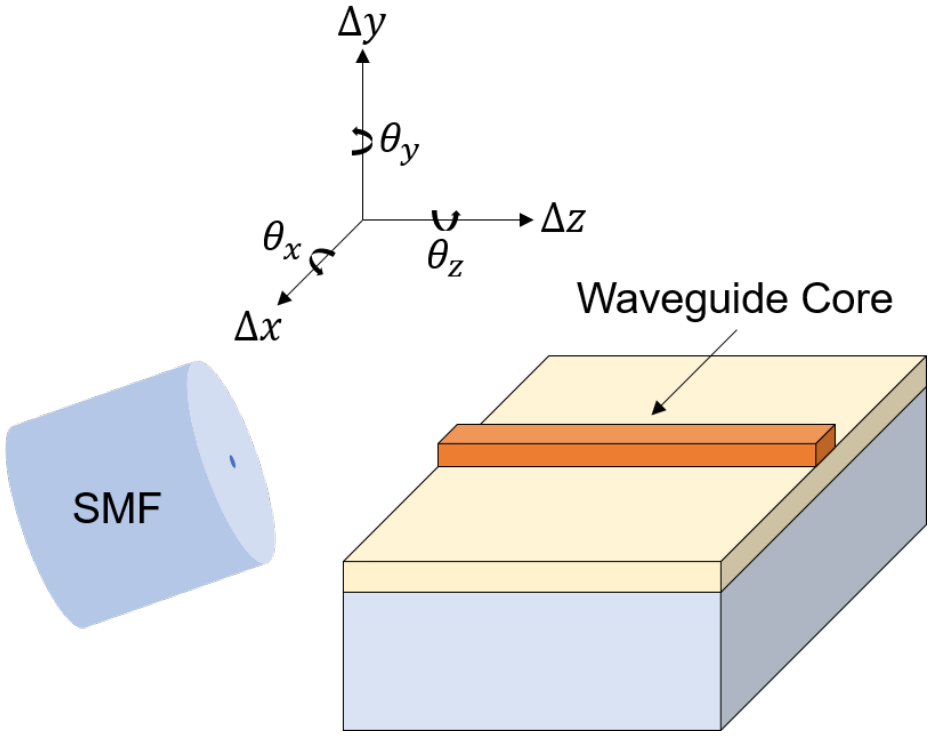


Figure 5.1: Fiber alignment and its six degrees of freedom.

Fiber alignment is a huge challenge for academia and the industry due to its six degrees of freedom as shown in Figure 5.1. When we align a fiber to a waveguide core or another fiber, not only the translational movement in X–, Y–, and Z–axis (Δx, Δy, and Δz, respectively) but also the rotational movement around the X–, Y–, and Z–axis (θ_{x}, θ_{y}, and θ_{z}, respectively) need to be adjusted and aligned to reduce the coupling loss. According

to [25], 1–dB misalignment tolerance for the rotational movement around all three axis is $\pm 2°$, the tolerance in the x and y directions is around $\pm 2\,\mu m$, and the tolerance in the z direction is around $40\,\mu m$. In a typical fiber alignment structure, coupling loss caused by the rotational movement is not significant compared to that caused by the translational movement. The coupling loss is more sensitive to the misalignment in x and y directions than that in the z direction, which was also confirmed in the measurements of the waveguide coupling loss in Chapter 4.

Fibers are either actively aligned with computer controlled micro–positioners and then fixed with optical adhesive or laser jointing, or passively aligned by placing fibers in fabricated structures to confine movement of fibers. Active alignment is widely used to align SMFs for its high coupling efficiency in the industry. It utilizes a computer controlled micro–positioner to hold the fiber, a laser to launch a beam with a certain power into the fiber, and a power meter at the other end to measure the output power. By moving the fiber and observing the output, A feedback is set up to find the position with the maximum coupling from the fiber to the waveguide core. Active alignment could achieve the maximum coupling efficiency. However, the coupling equipment is usually costly, and the alignment is a time–consuming serial process. Recent studies have been focusing on the algorithm to find the optimal position.

In the passive alignment approach, alignment structures like v–grooves are mechanically or chemically fabricated to hold the fiber in place and confine its movement. V–grooves are usually formed on a silicon wafer with $54.7°$ sidewalls due to the intrinsic crystallinity of silicon and the anisotropic wet etching. It could also be fabricated on other crystalline materials like quartz, which is very costly compared to regular semiconductor grade or optical grade glass. The glass used in this study is an amorphous and brittle material, so precise machining or chemical etching on regular glass for passive fiber alignment is not an option.

In this chapter, the efforts to couple and integrate fibers onto the glass interposer in-

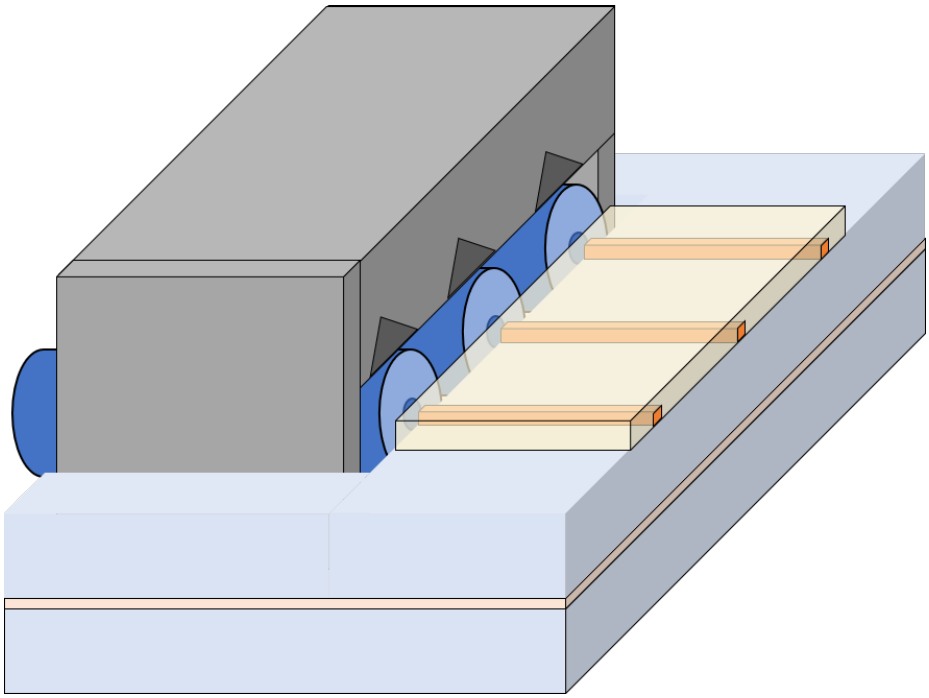


Figure 5.2: A schematic of the flip v–groove approach for fiber integration on glass.

cluding glass–to–glass bonding and flip v–groove for fiber integration will be reported.

5.1 Flip V-groove Approach for Fiber Integration on Glass Interposers

Due to the limitations of choices, a flip v–groove approach has been proposed and investigated for fiber–to–waveguide coupling and integration. A schematic of this approach is shown in Figure 5.2. The key to successful fiber integration is to reduce the degrees of freedom of the fiber. Since it is not feasible to fabricate accurate alignment structures on glass, accurate structure could be integrated using external chips like commercially available v–groove chips specifically for fiber integration with a precise pitch of 250 µm. The detailed stack–up is shown in Figure 5.3.

The stack–up is designed to work as follows. First, a 50 µm glass spacer is bonded on the glass substrate with a 10 µm thick bonding adhesive. There are cavities for the v–groove chip assembly in the glass spacer. Then the waveguide cores are fabricated on the glass spacer, which brings the center of the core 63 µm above the surface of the glass

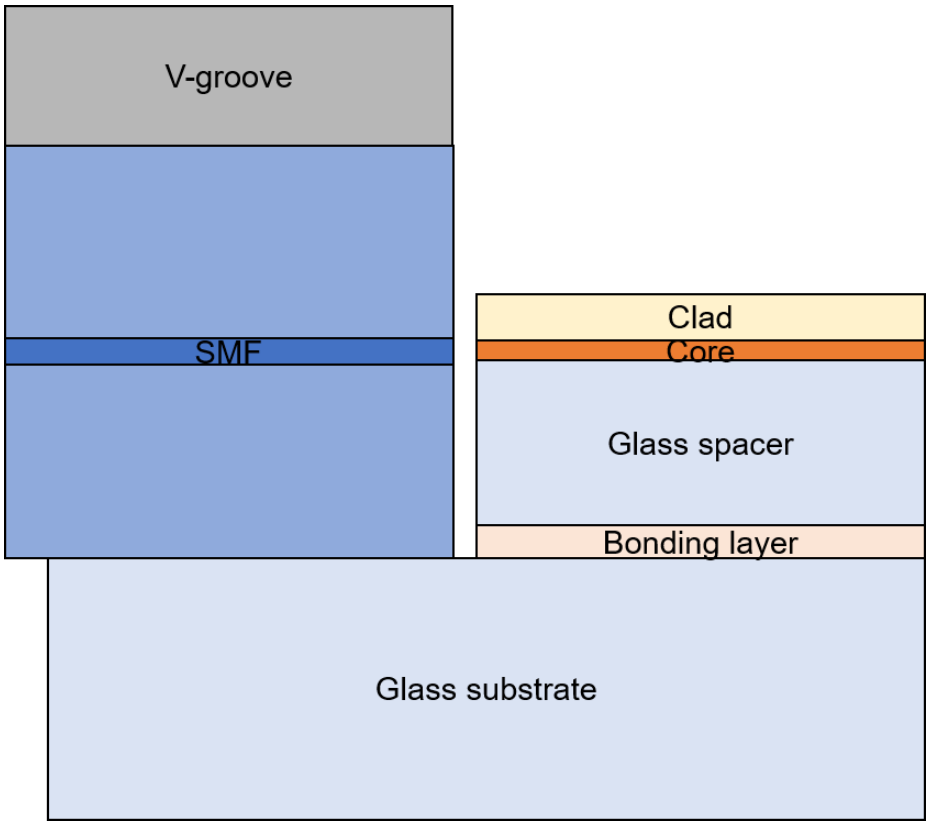
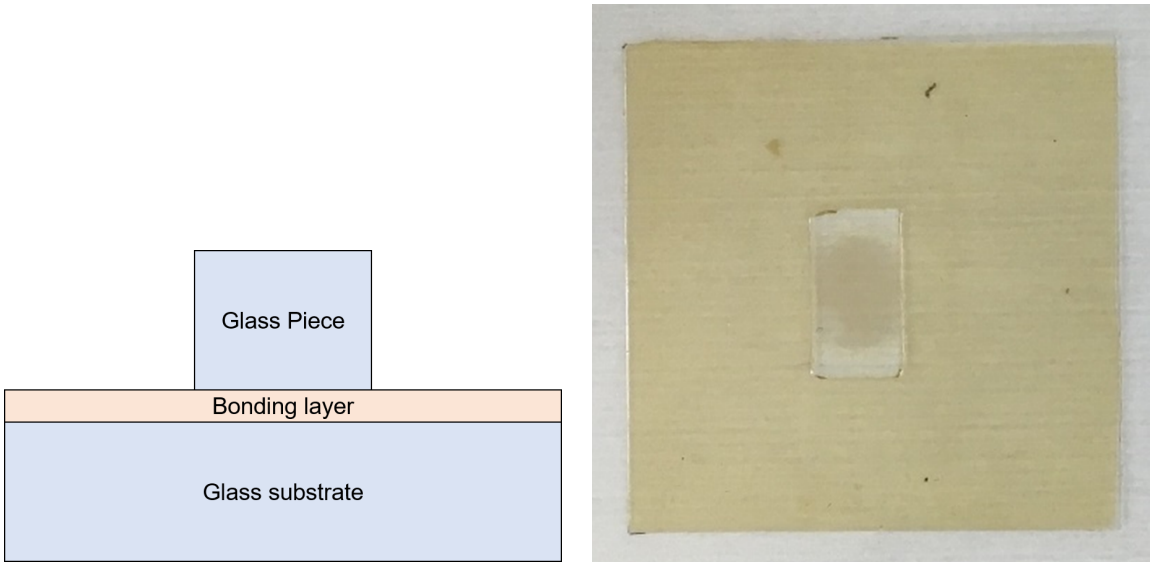


Figure 5.3: A cross section of the fiber alignment stack–up.

substrate. Following this, the clad is fabricated on top of the core. The glass substrate with SMWGs have now been fabricated. On the fiber integration side, the fibers are assembled on to the v–groove chip and fixed with an optical adhesive. Then the v–groove chip is flipped and mounted onto the glass substrate. Since the surface of the glass substrate is used as a reference, the height of the fiber core is the radius of the fiber, 62.5 µm. So in this stack–up, the difference in heights between the center of the fiber and the center of the polymer waveguide core is 0.5 µm, which is well below the 1–dB misalignment tolerance (2 µm). Both the development of glass–to–glass bonding and the fibers assembled in a v–groove chip will be presented in detail in this chapter.



(a) (b)

Figure 5.4: (a) A schematic cross section of the testing structure, and (b) a top view image of the testing structure.

5.1.1 Glass–to–Glass Bonding

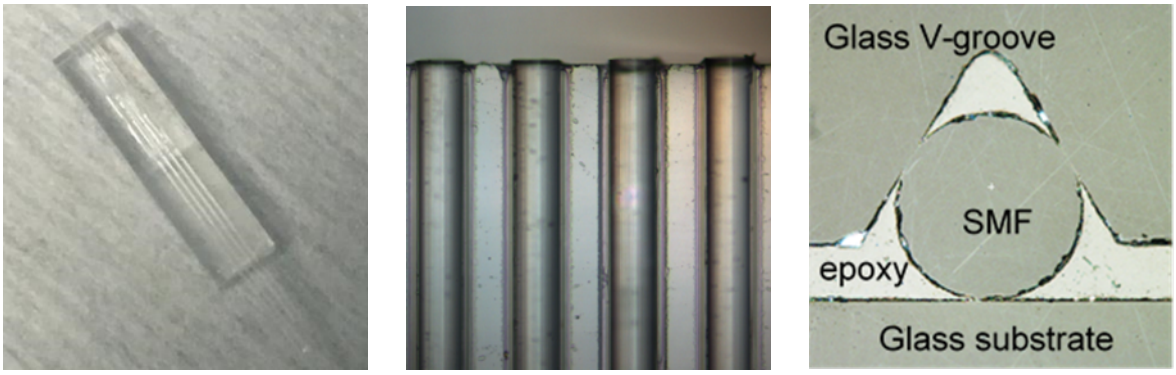
The glass–to–glass bonding test structure is shown in Figure 5.4. The glass bonded to the glass substrate via a bonding layer is 6.3 mm (a quarter inch) by 12.7 mm (half an inch) rectangular thin glass piece. The thicknesses of the glass substrate and the glass piece are both 150 µm, with a 10–µm thick bonding layer in between.

Three adhesives were investigated to test the glass–to–glass bonding strength, and they are EPR–129, a liquid adhesive from MicroChem, NC0201, a dry film from NAMICS Technologies Inc., and 14–P005, a dry film from DuPont Electronics & Imaging, which is also the material used as polymer waveguide clad. The bonding equipment is from Brewer Science, and the bonding strength was tested on Xyztec Condor Sigma. And the die shear test results are listed in Table 5.1.

All three adhesives exhibit adequate performance in glass–to–glass bonding. 14–P005 has a low optical absorption at telecommunication wavelengths. Using 14–P005 in glass–to–glass bonding enables vertical optical interconnects which might be of great interests in the future.

Table 5.1: Die shear test results on three adhesive materials.

Material	Load (N)	Die shear strength (MPa)
14–P005	107	1.34
EPR–129	145	1.80
NC0201	247	3.06



(a) **(b)** **(c)**

Figure 5.5: (a) A glass v–groove chip with four fibers assembled, (b) a magnified image of the edge of the v–groove chip, and (c) the cross section of a fiber assembled v–groove chip flipped and bonded on the glass substrate.

5.1.2 Fibers Assembled in a V–groove Chip

In the flip v–groove approach, fibers were first placed in the grooves of either silicon or quartz v–groove chips. Quartz (glass) v–groove chips from Precision Micro–Optics Inc. were chosen in this thesis due to its transparency during the later processing steps. There are typically 4, 8, or 12 grooves on a v–groove chip, with a pitch of 250 µm. Once the fibers were placed in the v–grooves, an UV curable optical adhesive NOA81 was applied on the chip to fill the gaps between fibers and the bottom of the grooves. The volume of the adhesive should not exceed the necessary amount such that it won't cover the top of the fibers which would contribute to effective change in the size of the fibers. Figure 5.5(a) shows a glass v–groove chip with four fibers assembled in the grooves. Before the adhesive was cured by UV exposure, a blockage was placed right at the edge of the v–groove chip

to make sure each cleavage of fibers is in the same surface, which was the edge of the chip. Figure 5.5(b) presents a top view of the edge of the v–groove chip with fibers assembled. The assembly was then flipped and attached to the glass substrate, NOA81 was then applied to fill the gap between the assembly and the substrate, and the optical adhesive was cured under UV light. A cross–sectional image of the flip v–groove with fiber on it assembled onto the glass substrate is shown in Figure 5.5(c). As shown in the picture, the SMF is in good contact with the two sidewalls of the groove and the glass substrate. The height of the center of the fiber is half of the diameter of the fiber, which is precisely controlled during manufacturing. The measured heights are 62 8$\pm$0.1 μm.

Since the fibers are fixed in the grooves, there is no degree of freedom in y and θ_z directions. Since the surface of the glass substrate is used as a reference for fibers too, the height of the fiber core or the fiber center is exactly one half of the fiber diameter, which is 62.5 μm, and this will make fiber cores automatically align to the fabricated waveguide cores in the y direction. The alignment in z and θ_y directions could be achieved by aligning the edge of the v–groove chip to the edge of the fabricated waveguides. Only alignment in the x direction is needed for this alignment structure.

5.2 Summary

Fiber integration on glass were investigated for communication in and out of the package. A flip v–groove approach was proposed and developed to confine fibers and reduce degrees of freedom. Using the surface of the glass substrate as a reference and the diameter of the fiber as the core height control brought the center of the fiber core to be 62 8$\pm$0.1 μm, which is very close to the height of the fabricated waveguide cores which is 63 μm. Such a structure could achieve a high precision alignment in y and z directions, as well as confining three degrees of freedom on rotations. Active alignment in x direction only is faster than fibers with six degrees of freedom.

CHAPTER 6
CONCLUSIONS

The objective of the research is to integrate high-density electronic interconnects with low loss single mode optical interconnects along with fiber integration on glass interposers for high speed communications. The motivation for this research arose from the ever-increasing high bandwidth demands for chip-to-chip communications on a package. Three technical challenges were identified to achieve the objective proposed above:

1. Ultra–fine microvia fabrication in RDLs to match the density of routing wires.
2. Low loss optical interconnects on glass interposers for on–package high–speed communication.
3. Passive fiber coupling and integration for communication into and out of the glass interposer.

Microvias together with routing wires as electrical interconnects, polymer–based SMWGs on glass interposers as optical interconnects, and fiber coupling and integration, were the three focus topics of this research.

This dissertation presented some of the first research results on glass interposers integrated with high density electronic and optical interconnects to address the ever–increasing bandwidth demand between chips on a package. Compared to silicon photonics and other on–board integration approaches, glass interposers achieve high density interconnects in both electrical and optical domains. Ultra–fine microvias down to 1.3 μm in diameter were demonstrated, which is 15x higher in interconnect density than previously reported. Fabrication of polymer–based SMWGs on glass were optimized and demonstrated, to exhibit a measured propagation loss that is one half of previously reported loss value. A passive integration method using flip v–groove chips to confine degrees of freedom of fibers was

proposed and developed. This chapter summarizes the research results, technical and scientific contributions, and recommends directions of future work.

6.1 Summary of Results

The research tasks, targets, and results on integration of high–density electronic interconnects and optical interconnects are summarized in Table 19.

Table 6.1: Summary of research tasks, targets and results.

	Research tasks	Targets	Results
Electronic interconnects	Ultra–fine microvias	5 μm in via diameter	1.3 μm fabricated
Optical interconnects	Low loss SMWGs on glass	< 0.3 dB/cm	0.6 dB/cm
Fiber integration	Passive fiber integration on glass	< 1 μm alignment accuracy	< 1 μm variance in y direction achieved

6.1.1 High–Density Electronic Interconnects

The study presented here focuses ultra–small microvias as vertical interconnects in RDLs. Following this approach, we have developed high density I/O by carefully analyzing photolithography mechanisms, and Gaussian beam analysis, as well as optimized process development and characterization.

To meet the electrical design rules, high aspect ratio lines are desired for ultra–fine routing wires. A novel embedded trench method was developed to address the shortcomings of traditional SAP for the fabrication of routing wires on the glass substrate. By using PID instead of photoresists, the complexity of the fabrication process was reduced, and the seed layer removal process which causes serious reliability issues for ultra–fine routing wires in SAP was eliminated. By adopting the embedded trench approach, 3 μm line

width was achieved in a PID polymer. The same PID material was also used to develop 3 µm microvias at 6 µm pitch and 2 µm microvias at 12.5 µm pitch in this material using photolithography.

Scaling of microvias has not progressed as much recently compared to the advances in routing wires. Picosecond UV laser was employed in this study to develop ultra–small microvias. Gaussian beam analysis was performed on the laser beam to understand the interaction of lasers with materials. The finest microvias directly fabricated by UV laser ablation were scaled from 20 µm down to 5 µm in diameter in a widely used dielectric dry film ABF. However, by adding an 80–nm–thick copper which has a higher ablation threshold, the same UV laser power was demonstrated to ablate a smaller opening in the copper layer, which formed a mask for the underneath polymer. By adding this thin metal barrier layer, microvias were scaled down to 3 µm in diameter. Fabrication of smaller microvias in ABF and others is challenging due to the presence of fillers in the polymer material which are larger compared to the openings, so a dielectric material without any added filler was used to continue the scaling of microvias. 1.5 µm microvias in a 3 µm thick film and 1.3 µm microvias in a 2 µm thick film were achieved in this way. In addition to the demonstration of the ultra–small microvias, the landing accuracy of the laser beam was also analyzed using optical image processing to address the reliability of microvia fabrication. Based on this study, we have characterized the distance between the drilling spot and the landing spot to be 0.24 µm on average.

6.1.2 Low Loss Optical Interconnects on Glass

Polymer based SMWGs on glass were designed and demonstrated. Mode calculation was performed to design the geometry of the core in waveguides, and the bottom width was set to 8 µm. The coupling between two closely placed SMWG cores was analysed to determine the density of the waveguides on glass. If cores are all covered underneath the clad, the minimum distance between two cores is 24 µm, and the density of waveguides is 31 per

millimeter. However, if there's an air gap between two waveguides, the density could be increased depending on the fabrication capability.

The fabrication process was thoroughly optimized to remove defects like wrinkles and residues and to control the cross–sectional geometry of the cores. After optimization, waveguide cores with 8 µm bottom width and straight sidewalls were fabricated. Different sample preparation methods were studied and analysed for insertion loss measurements. The propagation loss measured was 0.6 dB/cm at 1310 nm, which is half of the 1.3 dB/cm loss values reported in the previous work. The coupling loss of diced-only samples was 0.41 dB/facet, compared to a higher loss of 1.18 dB/ facet from diced and polished sample. Data rates were also measured on the waveguides. The measurement was performed using a laser at 1550 nm, at which the waveguide has higher loss. The maximum data rate measured is 21.3 Gbps error free with OOK modulation, but it is limited by the capability of electronic equipment used in the measurements. The potential maximum data rate supported by the waveguide could be much higher.

6.1.3 Fiber Coupling and Integration on Glass

The flip v–groove method was proposed and investigated for passive fiber alignment and integration. By placing and fixing fibers in a v–groove chip, the pitch between fibers is well controlled. The v–groove chip with fibers assembled was then flipped and attached to the glass substrate. By using the glass substrate as a reference, and the radius of the fiber as the core height, the location of the fiber in the y direction could be precisely controlled. On the other side of the substrate, a glass spacer of 50 µm was bonded to the glass substrate using a 10 µm film, and the polymer–based SMWG cores were fabricated on top of the spacer, which brought the height of the cores to 63 µm. The measured heights of the fiber cores were 62 8$\pm$0.1 µm, which was very close to the height of the polymer SMWG cores, so the alignment in the y direction with high accuracy was achieved. The alignment in the z direction could be achieved by placing the v–groove chip against to the edge of the glass

spacer as a stopper, which left the alignment in the x direction to be addressed.

6.2 Technical and Scientific Contributions

The key technical and scientific contributions from this thesis could be summarized as follows:

1. Demonstration of ultra–fine routing wires and microvias for high–density RDLs
   (a) The embedded trench technology was developed to address the reliability and bonding issue faced by the traditional routing wire fabrication method.
   (b) Microvias fabricated using laser ablation were scaled from 20 µm in diameter to 1.3 µm in diameter, corresponding to a 15x increase in the density of microvias.
2. Design and demonstration of polymer–based SMWGs on glass for on–package high speed communications.
   (a) The propagation loss of SMWGs was optimized to be half of the previously reported value.
   (b) The data rate through fabricated SMWGs measured is 21.3 Gbps error free, which is the limit of the measurement tools used.
3. Development of a passive fiber coupling and integration on glass method using flip v–groove chips to reduce degrees of freedom of fibers down to one direction.

6.3 Recommendations for Future Work

While this research investigated several aspects of high–density electronic interconnects for short–distance communication and optical interconnects on glass for long–distance on–package communication, there are still more questions that need to be addressed and hence there is more room for improvement. Potential future work has been identified as follows.

Even though the diameter of microvias has been scaled down to less than 2 µm, modeling and characterization on the electrical performance of ultra–fine microvias are still pending investigation. The non–uniform size of microvias and the sidewall roughness will have a huge impact on the electrical performance, when high speed signals travel through ultra–fine routing wires and microvias. Fabrication processes of microvias still need to be optimized for high yield and uniform microvia fabrication. Reliability of ultra–fine microvias as in mechanical and thermal response are pending analysis as well.

System–level integration of glass photonic interposers and silicon photonic chips might be the future of optoelectronics for on–package high–speed communications. Glass photonics and silicon photonics are not competing technologies. Glass photonic interposers are a great candidate as packaging technologies for silicon photonic chips. Further study on optical coupling between chips and interposers and the system–level integration of silicon photonic chips and glass photonic interposers together might be of great interest in the future.

Further investigation on passive fiber integration is recommended as well. Although efforts have been made in this dissertation to confine degrees of freedom of fibers when assembled onto the substrate, fiber movement in one direction is still free.

6.4 List of Publications

6.4.1 Journal Publications

- Liu, F., **Zhang, R.**, Khurana, G., Deprospo, B. H., Tummala, R. R., & Swaminathan, M. (2020). Smaller Microvias for Packaging Interconnects by Picosecond UV Laser With a Nanometer Metal Barrier Layer: A Feasibility Study. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 10(8), 1411-1418.

- **Zhang, R.**, Liu, F., Kathaperumal, M., Swaminathan, M., & Tummala, R. R. (2020).

Cointegration of Single–Mode Waveguides and Embedded Electrical Interconnects for High–Bandwidth Communications. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 10(3), 393-399.

- Liu, F., Khurana, G., **Zhang, R.**, Watanabe, A., DeProspo, B. H., Nair, C., ..., & Swaminathan, M. (2019). Innovative Sub–5–μm Microvias by Picosecond UV Laser for Post–Moore Packaging Interconnects. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 9(10), 2016-2023.

6.4.2 Conference Publications

- Watanabe, A. O., Ali, M., **Zhang, R.**, Ravichandran, S., Kakutani, T., Raj, P. M., ..., & Swaminathan, M. (2020, June). Glass–Based IC–Embedded Antenna–Integrated Packages for 28–GHz High–Speed Data Communications. In *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)* (pp. 89-94). IEEE.

- Liu, F., **Zhang, R.**, DeProspo, B. H., Dwarakanath, S., Nimbalkar, P., Ravichandran, S., ..., & Swaminathan, M. (2020, June). Advances in High Performance RDL Technologies for Enabling IO Density of 500 IOs/mm/layer and 8–μm IO Pitch Using Low–k Dielectrics. In *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)* (pp. 1132-1139). IEEE.

- **Zhang, R.**, Liu, F., Gallagher, M., Anzures, E., Sundaram, V., & Tummala, R. (2018, May). Co–integration of High–Bandwidth Photonic and Electronic RDL on 2.5D Glass Interposers Using Low Optical Absorption Photoimageable Dielectric Polymer. In *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)* (pp. 1130-1135). IEEE.

- Liu, F., Ito, H., **Zhang, R.**, DeProspo, B. H., Benthaus, F., Akimaru, H., ..., & Tummala, R. R. (2018, May). Low cost panel–based 1–2 micron RDL technologies

with lower resistance than Si BEOL for large packages. In *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)* (pp. 613-618). IEEE.

- Liu, F., Nair, C., Kubo, A., Ando, T., Lu, H., **Zhang, R.**, . . . , & Tummala, R. R. (2017, May). Via–in–trench: A revolutionary panel–based package RDL configuration capable of 200–450 I/O/mm/layer, an innovation for more–than–moore system integration. In *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)* (pp. 2097-2103). IEEE.

- **Zhang, R.**, Liu, F., Sundaram, V., & Tummala, R. (2017, May). First demonstration of single–mode polymer optical waveguides with circular cores for fiber–to–waveguide coupling in 3D glass photonic interposers. In *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)* (pp. 1606-1611). IEEE.

6.4.3 Book Chapter Publications

- Chou, B., Chang, G., Guidotti, D., & **Zhang, R.** (2019). Chapter 12 Fundamentals of Optoelectronics Packaging. In *Fundamentals of Device and System Packaging: Technologies and Applications* (2nd ed.). New York, NY: McGraw-–Hill Education.

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[10] F. Liu, C. Nair, A. Kubo, T. Ando, H. Lu, R. Zhang, H. Chen, K. S. Lee, V. Sundaram, and R. R. Tummala, "Via–in–Trench: A Revolutionary Panel–Based Package RDL Configuration Capable of 200–450 IO/mm/Layer, an Innovation for More–

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