

**TRADE-OFFS BETWEEN PERFORMANCE AND
RELIABILITY OF SUB 100-NM RF-CMOS
TECHNOLOGIES**

A Thesis
Presented to
The Academic Faculty

by

Rajan Arora

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
Dec 2012

TRADE-OFFS BETWEEN PERFORMANCE AND RELIABILITY OF SUB 100-NM RF-CMOS TECHNOLOGIES

Approved by:

Professor John D. Cressler, Advisor
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor Shyh-Chiang Shen
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor Jeffrey A. Davis
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor John Papapolymerou
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor Paul A. Kohl
School of Chemical and Biomolecular
Engineering
Georgia Institute of Technology

Date Approved: 11 September 2012

To my mother Mrs. Raj Arora

*For having confidence in my abilities and supporting me through all
those difficult times*

ACKNOWLEDGEMENTS

I would first like to express my deepest gratitude to Prof. John D. Cressler for his guidance and support as my doctorate advisor. His teaching and research are instrumental in my decision to pursue a Ph.D. in the field of silicon based microelectronics. Thank you Sir for being so patient with me, and working so hard to bring us the best opportunities and resources for research!

I would like to acknowledge Prof. John Papapolymerou, Prof. Shyh-Chiang Shen, Prof. Jeff Davis, and Prof. Paul Kohl for serving in my dissertation committee and offering invaluable insights into my research.

I have benefitted from the guidance and knowledge provided by Prof. Ron Schrimpf, Prof. Dan Fleetwood, and Dr. Enxia Zhang during my master's education at Vanderbilt University and throughout my Ph.D. program. They remain great mentors and awesome friends.

A big thank you to all members of the SiGe team at Georgia Tech. Without their support and friendship this work could not have been possible. I must thank the infamous "Dunkin" run group for all those life related discussions on the way to buy coffee. It was probably the company of those cool friends that took me to the shop every day rather than the quality of the coffee (No offense Dunkin!).

I must thank the GEDC support staff Lisa and Roosevelt for their friendship and support.

Big thanks to Stewie, Peter, Meg, Bryan, Chris, Louis, Quagmire, Joe, and Cleveland for making me laugh through all these years. I would also like to thank all friends over the past 27 years whom I have not mentioned above.

Last, but not least, I have to thank my family for their love and being there for

any sort of help whenever I needed it. Love you all!

TABLE OF CONTENTS

DEDICATION	iii
ACKNOWLEDGEMENTS	iv
LIST OF TABLES	x
LIST OF FIGURES	xi
SUMMARY	xx
I INTRODUCTION	1
1.1 Origin and History of the Problem	1
1.2 Sub 100-nm CMOS Technologies	4
1.2.1 Strained-Silicon CMOS	4
1.2.2 Silicon-on-Insulator Technology	4
1.2.3 Digital-CMOS vs. RF-CMOS	6
1.2.4 BEOL in Short-Channel CMOS Technologies	7
1.3 Reliability Mechanisms in a CMOS Technology	8
1.3.1 Hot-Carrier Effects	8
1.3.2 Negative/Positive Bias Temperature Instability (NBTI/PBTI)	9
1.3.3 Dielectric Breakdown	9
1.3.4 Large RF Stress Effects in CMOS	9
1.3.5 Latchup	10
1.3.6 Ionizing Radiation Damage	10
1.3.7 Single-Event Effects (SEE)	11
1.3.8 Low- or High- Temperature Effects	12
1.3.9 Electro-Migration	12
1.3.10 Electro-Static Discharge (ESD)	12
1.3.11 Antenna Effects	13
1.4 Organization and Contributions of the Dissertation	14

II	OPERATING VOLTAGE CONSTRAINTS IN 45-NM SOI NFETS AND CASCODE CORES	17
2.1	Overview	17
2.2	Motivation	17
2.3	Device Technology and Experimental Details	19
2.4	Device Voltage Constraints	21
2.4.1	Impact of Gate and Drain Bias on the Power-Gain and Single-Tone Linearity of a FB and BC Device	21
2.4.2	Hot-Carrier Reliability of a Single FB and BC Device	21
2.5	Circuit Voltage Constraints	25
2.5.1	Cascode Cores in 45-nm CMOS-on-SOI	25
2.5.2	Impact of Gate and Drain Bias on the Power-Gain and Linearity of a Cascode Core	25
2.5.3	Hot-Carrier Reliability of the Cascode Cores	26
2.5.4	Voltage Drop Across the Cascode and the Common-Source Device in a Cascode Core	30
2.6	Summary	31
III	USING BODY-BIAS TO MODULATE PERFORMANCE AND RELIABILITY OF SOI MOSFETS AND CIRCUITS	33
3.1	Overview	33
3.2	Introduction	33
3.3	Impact of Body Bias on the Device Performance and Reliability	35
3.4	Using Body-Contact to Mitigate Ionizing Radiation Damage	39
3.5	Impact of Body Bias on the Performance and Reliability of Single-Pole-Double-Throw (SPDT) Switches	43
3.6	Summary	52
IV	IMPACT OF DEVICE WIDTH ON PERFORMANCE AND RELIABILITY	53
4.1	Overview	53
4.2	Introduction	53
4.3	Effect of Finger Width on Device RF Performance	57

4.4	Effect of Finger Width on Device Reliability	58
4.5	Model for Hot-Carrier Degradation in CMOS Technologies	63
4.6	Summary	67
V	IMPACT OF CMOS SOURCE/DRAIN METAL CONTACT SPACING AND GATE-FINGER TO GATE-FINGER SPACING ON PERFORMANCE AND RELIABILITY	68
5.1	Overview	68
5.2	Introduction	68
5.3	Impact on RF Performance and DC Reliability	70
5.4	Impact on RF Reliability	73
5.5	Mechanisms	78
5.6	Impact of Asymmetric Halo Doping on the Performance and Reliability of Sub 100-nm CMOS	82
5.7	Summary	85
VI	CRYOGENIC LATCHUP IN SHORT-CHANNEL CMOS TECHNOLOGIES	86
6.1	Overview	86
6.2	Introduction	86
6.3	Latchup Fundamentals	88
6.4	Latchup Device Physics	88
6.5	Latchup Characterization at Room Temperature	91
6.6	Latchup Characterization Across Temperature	94
6.7	Single-Event Latchup at Cryogenic Temperature	95
6.8	TCAD Modeling of Latchup in CMOS Technologies	98
6.9	Summary	101
VII	USING TCAD TO MODEL MIXED-MODE DAMAGE IN SIGE HBTS	102
7.1	Overview	102
7.2	Introduction	102
7.3	Model for Interface Trap Formation due to Mixed-Mode Stress	104

7.4	TCAD Modeling Damage in SiGe HBTs due to Mixed-Mode Stress .	105
7.5	Summary	108
VIII TOTAL-DOSE TOLERANCE OF 32-NM CMOS ON SOI AND THE IMPACT OF TECHNOLOGY SCALING ON NFET RELIABILITY		110
8.1	Overview	110
8.2	Introduction	110
8.3	Device Technology and Experimental Details	111
8.4	Total-Dose Tolerance of 32-nm CMOS-on-SOI Technology	112
8.4.1	Gate-Only Bias During Total-Dose Radiation (Worst Case) .	112
8.4.2	Combined Gate and Drain Bias During Total-Dose Radiation (Device On)	114
8.5	Effect of Device Finger Width and Body-Contact on the Reliability of 32-nm nFETs	120
8.6	Impact of Technology Scaling on Performance, Hot-Carrier and Total-Dose Response	120
8.7	Summary	125
IX CRYOGENIC PERFORMANCE OF SHORT-CHANNEL SOI CMOS TECHNOLOGIES		126
9.1	Overview	126
9.2	Introduction	126
9.3	Results and Discussion	127
9.4	Summary	131
X CONCLUSIONS AND FUTURE WORK		132
10.1	Conclusions	132
10.2	Future Work	134
REFERENCES		136
VITA		145

LIST OF TABLES

1	Voltage and current across the cascode devices	29
2	Devices used to study the impact of width on performance and reliability	58
3	Devices used to study the impact of source/drain metal contact and gate-finger to gate-finger spacing on performance and reliability . . .	70

LIST OF FIGURES

1	Cut-off frequency (f_T) as a function of drain current for the nFETs from different sub 100-nm RF-CMOS technologies [10].	2
2	SRAM bit cell area and bit density as a function of CMOS technology node [10].	2
3	Operation count and the design rule count of a single integrated circuit as a function of technology scaling [20].	3
4	Evolution of CMOS transistor architecture in the last decade, from a non-strained oxide/poly gate structure to a high-k/metal-gate strained-silicon transistor at the 32-nm node.	5
5	Top-view layout comparison of (a) single-finger digital nFET and (b) multi-finger RF nFET.	7
6	Side-view layout of a multi-finger RF nFET.	7
7	SEM images of 130-nm six layer metal stack vs. 32-nm eight layer metal stack [10].	8
8	Schematic representing the fundamental radiation induced electron-hole pair generation with bulk hole trapping and movement of the charge centroid to the interface under bias [38].	11
9	Possible radiation-induced leakage paths along the (a) surface of buried-oxide (BOX) and (b) STI sidewalls.	12
10	Trade-offs between performance and reliability in sub 100-nm CMOS technologies.	14
11	Transistor threshold voltage and supply voltage as function of technology node [48].	18
12	Measured (a) drain current as a function of drain voltage, (b) drain current as a function of gate voltage, (c) cut-off frequency as a function of gate voltage, and (d) power-gain as a function of RF input power of a FB and BC device.	20
13	Measured (a) power-gain as a function of RF input-power of a FB device with varying drain voltage ($V_{GS} = 0.6$ V) and (b) power-gain as a function of RF input-power of a FB device with varying gate voltage ($V_{DS} = 1.0$ V).	22
14	Electric field in the channel region of a 45-nm nMOSFET for varying drain bias.	22

15	(a) Shift in threshold voltage as a function of stress time of FB and BC devices. (b) Lifetime (in seconds) as a function of the inverse of drain voltage of FB and BC devices.	23
16	(a) Electric field in the channel region of a FB and BC device at constant gate and drain voltage ($V_{GS} = 1.0$ V, $V_{DS} = 1.0$ V). (b) Conduction band energy in the channel region of a FB and BC device. (c) Electrostatic potential in the channel region of a FB and BC device. (d) Impact ionization induced avalanche generation rate in the channel region of a FB and BC device.	24
17	Cascode test structure with (a) FB common-source and cascode device (b) FB common-source and BC cascode device (c) BC common-source and BC cascode device.	26
18	(a) Measured drain current as a function of the drain voltage and (b) drain current as a function of M1 gate voltage of the FB-FB, BC-FB and BC-BC cascode cores.	27
19	Cut-off frequency as a function of M1 gate voltage of the FB-FB, BC-FB and BC-BC cascode cores.	27
20	(a) Power-gain as a function of RF input-power of FB-FB, BC-FB, and BC-BC cascodes ($V_{D-M2} = 1.5$ V, $V_{G-M2} = 1.0$ V, $V_{G-M1} = 0.6$ V). (b) Power-gain as a function of RF input-power of BC-BC cascode for varying bias voltage.	28
21	(a) Shift in threshold voltage as a function of stress time of the three cascodes. (b) Lifetime (in seconds) as a function of the inverse of drain voltage of the cascodes.	28
22	(a) Electric field in the channel region of a FB-FB, BC-FB and BC-BC cascode at constant gate and drain voltage. (b) Conduction band energy in the channel region of a FB-FB, BC-FB, and BC-BC cascode at constant gate and drain voltage. (c) Avalanche generation in the channel region of a FB-FB, BC-FB and BC-BC cascode at constant gate and drain voltage ($V_{D-M2} = 2.7$ V, $V_{G-M2} = 1.5$ V, $V_{G-M1} = 1.0$ V).	29
23	Gate current as a function of the common-source device gate voltage for varying stress conditions of the BC-FB cascode (Stress voltage: $V_{D-M2} = 3.3$ V, $V_{G-M2} = 1.5$ V, $V_{G-M1} = 1.0$ V).	30
24	TCAD simulated body current as a function of M1 gate voltage of the BC-BC and BC-FB cascode.	31
25	Schematic layout of (a) Floating-body, (b) T-body, (c) Notched-T-body, and (d) H-body device.	34

26	Small-signal equivalent circuit of (a) BC and (b) FB device.	34
27	(a) Drain current as a function of gate voltage of FB and BC device for varying body bias. (b) Drain current as a function of drain voltage of FB and BC device for varying body bias (Data on 180-nm CMOS-on-SOI technology (IBM 7RFSOI)).	36
28	Effect of body bias on a SOI MOSFET threshold voltage.	36
29	Effect of body bias on a nFET hot-carrier reliability [50].	37
30	Electrostatic potential of (a) FB and (b) BC device.	38
31	Current density in the body-region of (a) FB and (b) BC device. . . .	38
32	(a) Comparison of current density of FB and BC device in the body region. (b) Simulated $I_{DS} - V_{GS}$ characteristics of FB and BC device.	39
33	ARACOR X-ray radiation source.	40
34	(a) Drain current as a function of gate voltage of FB device for varying ionizing dose. (b) Drain current as a function of gate voltage of BC device for varying ionizing dose.	41
35	3D TCAD simulated electron current density for (a) FB device, (b) T-body device, and (c) H-body device.	41
36	TCAD simulated drain current as a function of gate voltage of (a) FB device, (b) T-body device, and (c) H-body device for varying trap concentrations at the active-STI edge.	42
37	Schematic of a SPDT switch.	43
38	Die photograph of the SPDT switch.	43
39	Insertion loss and isolation as a function of frequency of a FB and BC switch with grounded body.	44
40	Effect of gate bias on switch performance.	44
41	(a) Effect of negative body bias on IL. (b) Effect of negative body bias on isolation.	46
42	(a) Output power as a function of input power of the switch for varying body bias. (b) Insertion loss as a function of input power of the switch for varying body bias.	46
43	Effect of body bias of series and shunt nFETs on switch performance.	47
44	(a) Space charge contour diagram of a nFET for $V_G = 1.0$ V, $V_D = 1.0$ V, $V_S = 0.0$ V, and $V_{BODY} = -1.0$ V. (b) Space charge contour diagram for a nFET of $V_G = 1.0$ V, $V_D = 1.0$ V, $V_S = 0.0$ V, and $V_{BODY} = 0.0$ V.	48

45	Space charge at the source-body junction of the nFETs for negative and zero body bias.	49
46	(a) Effect of proton irradiation on insertion loss. (b) Effect of proton irradiation on isolation.	49
47	(a) Effect of gate and body stress on insertion loss. (b) Effect of gate and body stress on input return loss (S11).	50
48	(a) Electric field in the channel region for varying body bias. (b) Impact ionization in the body region for varying body bias. (c) Electric field in the gate oxide region for varying body bias.	51
49	(a) TCAD simulated drain current and body current as a function of gate voltage for a $2\ \mu m$ channel length nFET. (b) TCAD simulated drain current and body current as a function of gate voltage for a 45-nm channel length nFET.	55
50	(a) TCAD simulated impact ionization in the channel region for a $2\ \mu m$ channel length nFET. (b) TCAD simulated impact ionization in the channel region for a 45-nm channel length nFET.	56
51	Maximum oscillation frequency (f_{MAX}) and cut-off frequency (f_T) as a function of gate voltage of the devices with varying finger width. . . .	57
52	(a) Power-gain as a function of input RF power (frequency = 9 GHz) of the devices with varying finger width. (b) Output-third-order-intercept point (OIP3) as a function of gate voltage of the devices with varying finger width.	59
53	(a) Shift in threshold voltage as a function of stress time of the nFETs with varying finger width. (b) Total-dose irradiation induced increase in off-state current of the nFETs with varying finger width.	61
54	TCAD simulated interface trap density as a function of stress time for device of width $0.1\ \mu m$ and $0.7\ \mu m$	62
55	TCAD simulated electron mobility enhancement factor along the channel direction for device of width (a) $0.1\ \mu m$ and (b) $0.7\ \mu m$	62
56	Schematic diagram of enhanced trap formation along the STI edge for un-strained MOSFET, and trap formation in the middle of channel for strained MOSFET.	63
57	TCAD simulated electric field lines of a nFET with varying gate voltage.	65
58	TCAD simulated I_{DS} vs. V_{DS} , I_{BODY} vs. V_{DS} , $M - 1$ vs. V_{DS} characteristics of a nFET with varying gate voltage.	66

59	Layout of the floating-body devices. Device with (a) tight gate-finger to gate-finger and tight source/drain (S/D) metal contact spacing, (b) loose gate-finger to gate-finger and tight S/D metal contact spacing, (c) tight gate-finger to gate-finger and loose S/D metal contact spacing, and (d) loose gate-finger to gate-finger and loose S/D metal contact spacing.	69
60	(a) Cut-off frequency (f_T) as a function of gate voltage of the devices with varying contact spacing. (b) Maximum oscillation frequency (f_{MAX}) as a function of gate voltage of the devices with varying contact spacing.	71
61	(a) Output-power as a function of input-power of the nFETs with varying contact spacing. (b) Output-third-order-intercept point (OIP3) of nFETs with varying contact spacing.	72
62	Threshold voltage shift of nFETs with the same dimensions ($L = 45$ nm, $W_f = 2 \mu m$), but varying contact spacing.	73
63	(a) Transfer characteristics of device A with tight S/D contact and gate-finger to gate-finger spacing. (b) Transfer characteristics of device C with loose S/D contact and gate-finger to gate-finger spacing. . . .	73
64	Off-state drain current as a function of total irradiation dose of the four devices with varying contact spacing.	74
65	Power-gain as a function of input-power of the devices with varying contact spacing (pre- and post-irradiation).	74
66	(a) TCAD simulated I_{DS} - V_{GS} characteristics of the devices with varying contact spacing. (b) Simulated electric-field along the channel region of the devices with varying contact spacing.	75
67	Block diagram of the load-pull measurement setup used for RF measurements.	76
68	Shift in threshold voltage with RF stress (at $V_{GS} = 0.6$ V, $V_{DS} = 0.9$ V) of nFETs with loose and tight S/D contact spacing (Frequency = 9 GHz, $P_{in} = 0$ dBm).	76
69	Comparison of S21 degradation with increasing (a) RF stress time for 1000 s, 2000 s, and 3000 s stress (for constant power = 0 dBm) and (b) input RF power of +5, +6, +7 dBm (for constant stress time = 100 s) of nFETs (at peak f_T bias).	78
70	(a) Transfer characteristics of nFET (device C) with varying RF power stress ($V_{GS} = 0.6$ V, $V_{DS} = 0.9$ V). Stressed for 100 s at each power step (frequency = 9 GHz). (b) Gate current characteristics of nFET (device C) with varying RF power stress ($V_{GS} = 0.6$ V, $V_{DS} = 0.9$ V).	80

71	Gate-to-drain capacitance (C_{GD}) as a function of gate voltage of nFETs with varying contact spacing.	81
72	Comparison of (a) I_{DS} degradation (percentage) as a function of RF stress time (at peak f_T bias) (b) C_{GD} degradation (percentage) as a function of RF stress time of nFETs (at peak f_T bias).	81
73	Comparison of (a) I_{DS} degradation (percentage) as a function of RF input-power (b) C_{GD} degradation (percentage) as a function of RF input-power of nFETs (at peak f_T bias).	82
74	(a) TCAD simulations showing the doping concentration for the asymmetric device. Asymmetric devices have a large lateral gradient doping profile with a source-side halo pocket of $1 \times 10^{19} \text{cm}^{-3}$ concentration and a low-doped drain channel doping of $5 \times 10^{17} \text{cm}^{-3}$ (a change of 20-fold). (b) TCAD simulations showing the active doping concentration for the symmetric control device. The symmetric control devices have a uniform profile with a channel doping concentration of $3 \times 10^{18} \text{cm}^{-3}$ [25].	83
75	(a) Electric-field in the channel region of asymmetric and symmetric halo doping nFETs. (b) Threshold voltage shifts of asymmetric and symmetric halo doping nFETs with the same dimensions ($L = 45 \text{ nm}$, $W_f = 2 \mu\text{m}$).	83
76	Total-dose irradiation induced increase in off-state current of nFETs with asymmetric halo doping ($L = 45 \text{ nm}$, $W_f = 2 \mu\text{m}$).	84
77	(a) Measured body current as a function of gate voltage of nFETs with asymmetric halo doping and symmetric halo doping. (b) Measured body current as a function of gate voltage of nFETs with asymmetric halo doping for varying channel length.	85
78	Schematic of the parasitic transistors present in a CMOS inverter circuit.	90
79	Latchup process flow.	90
80	SEM image of a metal line damaged from the large current generated by a latchup event [74].	91
81	Gummel characteristics of (a) parasitic PNP and (b) parasitic NPN transistor present in a p-n-p-n doping structure.	92
82	Latchup characteristics of a p-n-p-n structure without any protection (Basic), with a N-ring (NS), and with a deep-trench (DT).	93
83	Latchup characteristics of a p-n-p-n structure without any protection (Basic) and with variation in anode-to-cathode spacing. Device 2 has a larger anode-to-cathode spacing than device 1.	94

84	Effect of temperature on the latchup characteristics of a basic p-n-p-n structure.	95
85	(a) Trigger-current and trigger-voltage of a basic p-n-p-n structure as a function of temperature. (b) Holding-current and holding-voltage of a basic p-n-p-n structure as a function of temperature.	96
86	Device cross sections for hard SEL events versus temperature. All data was measured at 60° incidence using 15 MeV/u Kr with $LET_{eff} = 64.4$ and $R_p = 43$. The downward arrows indicate limiting cross sections [5].	97
87	Anode current as a function of anode voltage for varying (a) temperature and (b) substrate doping.	99
88	Anode current as a function of anode voltage for varying (a) sub-collector doping and (b) deep trench (DT) depth.	100
89	Cross section of a SiGe HBT showing the interface trap formation at the EB-spacer and STI interface with silicon during a mixed-mode stress condition [78].	103
90	Majority-carrier current density (a) before stress (b) after stress, for traps only at the EB-spacer.	106
91	Majority-carrier current density (a) before stress (b) after stress, for traps only at the STI edge.	106
92	Interface trap density as a function of stress time for STI and EB-spacer oxides.	107
93	(a) Collector- and base- current as a function of base-emitter voltage for traps at EB-spacer oxides. (b) Collector- and base- current as a function of base-emitter voltage for traps at STI oxides.	108
94	Measured and modeled DC current gain (Beta) as a function of stress time.	109
95	TEM cross-section of a 32-nm CMOS device (after [86]).	112
96	Schematic energy band diagram of the gate-stack of a 32-nm SOI CMOS device.	112
97	Transfer characteristics of the nFET as a function of radiation dose ($L = 32$ nm, $W = 0.325$ μm).	113
98	Output characteristics of the nFET as a function of radiation dose ($L = 32$ nm, $W = 0.325$ μm).	113
99	Transfer characteristics of the nFET as a function of radiation dose ($L = 490$ nm, $W = 0.325$ μm).	115

100	Output characteristics of the nFET as a function of radiation dose ($L = 490$ nm, $W = 0.325$ μm).	115
101	Transconductance characteristics of the nFET as a function of radiation dose ($L = 490$ nm, $W = 0.325$ μm).	116
102	On-Off current ratio of the nFETs with varying channel length as a function of radiation dose.	116
103	Hot-carrier degradation induced shift in threshold voltage as a function of stress time for transistors of different channel length in the 32-nm technology.	117
104	Body current as a function of gate voltage for the body-contact device with varying drain voltage.	117
105	Transfer characteristics of the pFET as a function of radiation dose ($L = 32$ nm, $W = 0.425$ μm).	118
106	Transfer characteristics of the nFET as a function of radiation dose ($L = 32$ nm, $W = 0.325$ μm).	118
107	Shift in threshold voltage as a function of hot-carrier stress time for the nFETs with varying device width.	119
108	Shift in threshold voltage as a function of hot-carrier stress time for the floating-body (FB) and body-contacted (BC) nFETs.	119
109	Measured (a) drain current as a function of gate voltage, (b) transconductance as a function of gate voltage, and (c) gate current as a function of gate voltage for the smallest channel length devices from 65-, 45- and 32- nm technologies.	122
110	On-Off current ratio as a function of radiation dose for the three technology nFETs.	123
111	Shift in threshold voltage as a function of hot-carrier stress time for the three technology nFETs.	123
112	Electric field in the gate oxide for the three technology nFETs.	124
113	Impact ionization in the channel region for the three technology nFETs.	125
114	(a) Drain current as a function of gate voltage of a 45-nm floating-body SOI CMOS device for varying temperature. (b) Transconductance as a function of gate voltage of a 45-nm floating-body SOI CMOS device for varying temperature.	128

115	(a) AC Current gain (H21) as a function of frequency of a 45-nm floating-body SOI CMOS device at 300 K and 80 K. (b) Cut-off frequency as a function of gate voltage of a 45-nm floating-body SOI CMOS device at 300 K and 80 K.	129
116	(a) Transfer characteristics of a 45-nm floating-body SOI CMOS device for increasing stress time (at $V_{GS}=1.0$ V and $V_{DS}=1.5$ V) at 300 K. (b) Transfer characteristics of a 45-nm floating-body SOI CMOS device for increasing stress time (at $V_{GS}=1.0$ V and $V_{DS}=1.5$ V) at 80 K.	130
117	Shift in threshold voltage as a function of stress time of a 45-nm floating-body SOI nFET for varying temperature.	131
118	Different phenomenon studied in this dissertation in sub-100 nm CMOS-on-SOI technologies, and their impact on performance and reliability of MOSFETs.	134

SUMMARY

The objective of this research is to develop an understanding of the trade-offs between performance and reliability in sub 100-nm silicon-on-insulator (SOI) CMOS technologies. Such trade-offs can be used to demonstrate high performance reliable circuits in scaled technologies. Several CMOS reliability concerns such as hot-carrier stress, ionizing irradiation damage, RF stress, temperature effects, and single-event effects are studied. These reliability mechanisms can cause temporary or permanent damage to the semiconductor device and to the circuits using them. Several improvements are made to the device layout and process to achieve optimum performance. Parasitics are shown to play a dominant role in the performance and reliability of sub 100-nm devices. Various techniques are suggested to reduce these parasitics, such as the use of the following: a) optimum device-width, b) optimum gate-finger to gate-finger spacing, c) optimum source/drain metal contact spacing, and d) floating-body/body-contact. The major contributions from this research are summarized as follows:

- 1) Role of floating-body effects on the performance and reliability of sub 100-nm CMOS-on-SOI technologies is investigated for the first time [1], [2]. It is demonstrated through experimental data and TCAD simulations that floating-body devices have improved RF performance but degraded reliability compared to body-contacted devices.
- 2) Floating-body effects in a cascode core is studied. Cascode cores are demonstrated to achieve much larger reliability lifetimes than a single device. A variety of cascode topologies are studied to achieve the trade-offs between performance and reliability for high-power applications [2].

- 3) The use of body-contact to modulate the performance of devices and single-pole-double-throw (SPDT) switches is studied. The SPDT switch performance is shown to improve with a negative body-bias.
- 4) The impact of device width on the RF performance and reliability is studied. Larger width devices are shown to have greater degradation, posing challenging questions for RF design in strained-Si technologies [3].
- 5) A novel study showing the effect of source/drain metal contact spacing and gate-finger to gate-finger spacing on the device RF performance is carried out. Further, the impact of above on the hot-carrier, RF stress, and total-dose irradiation tolerance is studied [3], [4].
- 6) Latchup phenomenon in CMOS is shown to be possible at cryogenic temperatures (below 50 K), and its consequences are discussed [5].
- 7) A time-dependent device degradation model has been developed in technology computer aided design (TCAD) to model reliability in CMOS and SiGe devices.
- 8) The total-dose irradiation tolerance and hot-carrier reliability of 32-nm CMOS-on-SOI technology is reported for the first time. The impact of HfO_2 based gate dielectric on the performance and reliability is studied [6].
- 9) The impact of technology scaling from 65-nm to 32-nm on the performance and reliability of CMOS technologies is studied [6].
- 10) Cryogenic performance and reliability of 45-nm nFETs is investigated. The RF performance improves significantly at 77 K. The hot-carrier device reliability is shown to improve at low temperatures in short-channel CMOS technologies.

CHAPTER I

INTRODUCTION

1.1 Origin and History of the Problem

CMOS-based radio-frequency (RF) and analog systems have made rapid inroads into the analog/wireless market in the last decade [7]-[9]. The digital-driven CMOS scaling into the sub 100-nm range has produced transistors with competitive RF performance characteristics (f_T , f_{MAX} , linearity, power-gain, noise, etc.)(see Figure 1) [10]. Today, a lot of the CMOS-based commercial analog/RF circuits and systems are based on the 180-nm or 130-nm technologies. This is because of better device models, tolerable process-variation, and lower cost of these matured technologies. However, many digital/memory products have come out in the market with short-channel CMOS technologies. For example, Apple iPad 2 and iPhone 4S use 45-nm CMOS A5 microprocessor [11]. Intel is building microprocessors at 22-nm technology node with three-dimensional transistors [12]. Figure 2 shows the advantages of scaling in digital circuits with decreasing SRAM cell area and increasing SRAM bit density. A smaller form-factor of the integrated-circuit and improved functionality can be achieved at highly scaled technology nodes.

Clearly, deep sub-micron CMOS technologies are essential for building mixed-signal systems. However, using these short-channel technologies in analog/RF circuits is a challenge because of several reasons. With such scaling, the short-channel effects can degrade circuit performance. Silicon-on-insulator (SOI) technology is widely adopted to help mitigate these short-channel effects [13]-[14]. Decreasing device dimensions at similar power supply levels has resulted in transistors with increasing intrinsic electric-fields and hence increasing reliability concerns. In general, there is expected to

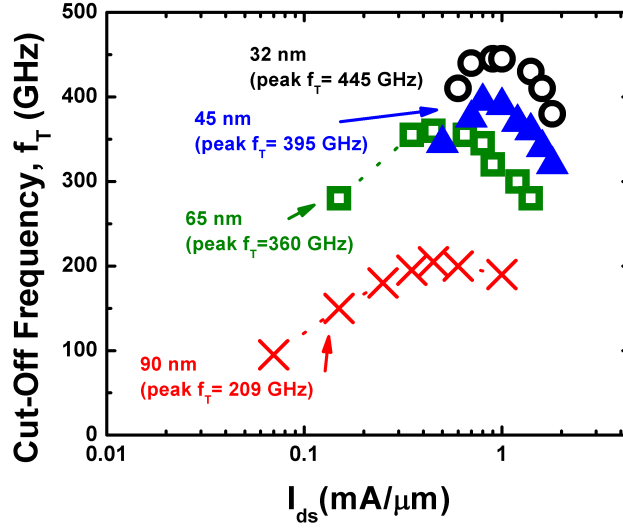


Figure 1: Cut-off frequency (f_T) as a function of drain current for the nFETs from different sub 100-nm RF-CMOS technologies [10].

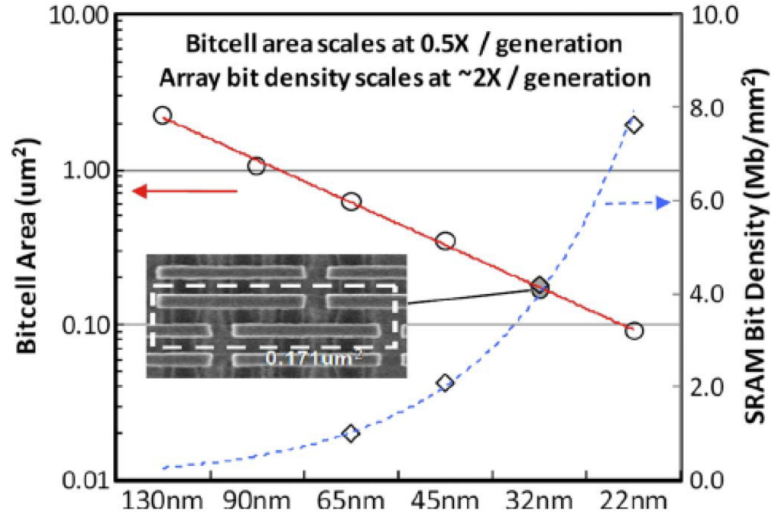


Figure 2: SRAM bit cell area and bit density as a function of CMOS technology node [10].

be some degradation in device parameters under extreme operating conditions, such as large voltage swings, large RF stress, etc. [15]-[17]. This can lead to degradation in circuit and system-level performance [18]-[19]. In sub 100-nm CMOS technologies, the device parasitics have a large impact on the performance and reliability of the device itself and to the circuits using them. Thus the knowledge of the trade-offs

between performance and reliability are essential for the design of high performance and reliable circuits, and will be the focus of this work. Ideally, such trade-offs should be included in the transistor compact models for designers to simulate circuit reliability at design stage. However, building such models can be a challenge because of their high cost and complexity. Thus, the onus is upon the sub 100-nm CMOS circuit designers to understand and apply these trade-offs to achieve the design specifications, and at the same time, meet the ten-year product lifetime requirement [20]. Scaling, for enhanced performance and cost reduction reasons, has pushed existing CMOS materials much closer to their intrinsic reliability limits. Future robust designs will require a strong team effort whereby the design engineer must clearly understand the process variability and its impact on reliability. This strong team effort, between design and process, will become critically important as the industry is seeking to replace the very materials that has made the industry so successful: Si substrates, SiO_2 gate-dielectric, Aluminum-based metallization and SiO_2 interconnect-dielectrics [21]. These increasing number of variables in process technology has resulted in increasing design rules with technology scaling (Figure 3).

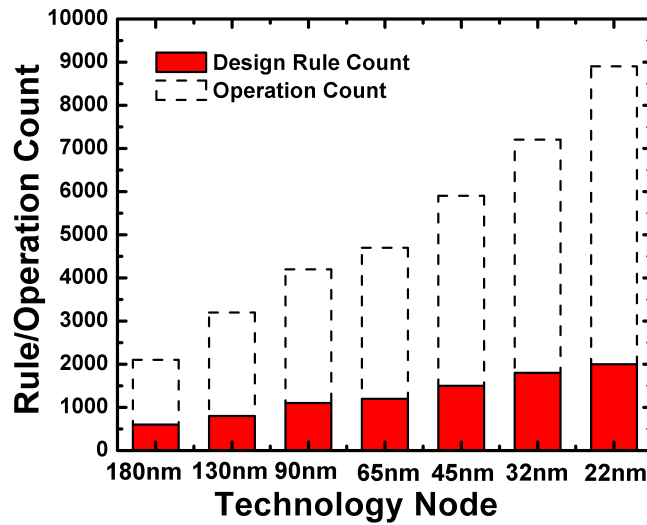


Figure 3: Operation count and the design rule count of a single integrated circuit as a function of technology scaling [20].

1.2 Sub 100-nm CMOS Technologies

Until the 130-nm technology node standard CMOS scaling rules had been followed [22]. However, from the 90-nm technology node, it was realized that scaling alone cannot meet the technology performance requirements, and novel ideas like strained-silicon, high-k dielectrics, and SOI have been implemented.

1.2.1 Strained-Silicon CMOS

Strain (deformation of a material as a result of applied stress) in the Si crystal lattice improves the carrier mobility, resulting in improved device performance [23]. Stress can be introduced with the formation of the silicon-nitride (SiN) cap over the polysilicon gate. Depending on how the SiN is deposited, this stress may be either tensile or compressive. Silicon germanium (SiGe) can be introduced into the source/drain for PMOS to create compressive stress in the channel region. The germanium atom is larger than the silicon atom, and when it replaces a silicon atom, the crystal lattice is strained. For a device mobility improvement, this strain must be present in the silicon where the FET channel is formed. The modifications to a MOSFET structure over four technology generations from 130-nm to 32-nm are shown in Figure 4. The major changes to a MOSFET structure have been the addition of strain-enhancing layers on top of the gate electrode (for NMOS), SiGe source/drain (for PMOS), and the replacement of SiO_2 gate-dielectric with high-k gate-dielectrics (for both NMOS and PMOS).

1.2.2 Silicon-on-Insulator Technology

A thin-film silicon-on-insulator (SOI) technology is advantageous because of a number of factors. An SOI technology provides a simple device isolation. SOI MOSFETs have charge coupling between the front and back gates [24]. The performance advantage of SOI over bulk Si is caused by the elimination of area junction capacitance, the lack of a reverse body-effect in stacked circuits, and because the SOI body is slightly

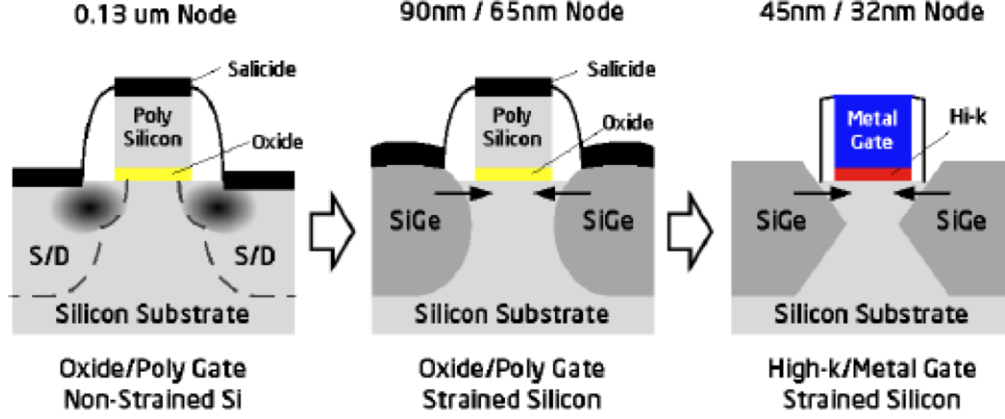


Figure 4: Evolution of CMOS transistor architecture in the last decade, from a non-strained oxide/poly gate structure to a high-k/metal-gate strained-silicon transistor at the 32-nm node [10].

forward-biased under most operating conditions. No p-n-p-n path exists in a SOI structure and hence latchup is eliminated. With SOI, the floating-body voltage is a function of applied source/drain (S/D) voltages and prior operation. This can be used to reduce the switching time, and the voltage drop across pass gate and source follower circuits. The reduction of the S/D capacitance improves the technologies power performance. SOI technologies eliminate the risk caused by single-event effects (SEE). The coupling between digital and analog circuits in a SOI platform is naturally eliminated. The technologies used in this work (IBM 65-nm, 45-nm, and 32-nm SOI) have partially-depleted FETs [25]. In the partially-depleted devices, the source/drain doping does not extend all the way to the BOX layer permitting varying threshold voltage. Another feature of SOI MOSFETs is that the local substrate ('body') of the device floats electrically, and therefore, the substrate-source bias voltage (V_{BS}) is not fixed. As V_{BS} changes, the device threshold voltage (V_{TH}) will change. This instability in V_{TH} is what has made SOI device design quite challenging. There are some drawbacks in partially-depleted devices, namely, History- and Kink- effects that need to be considered. History-effect causes a delay variation in circuits as a result of dynamic switching conditions ensuing from previously applied voltages [13]. These

delay variations can be quite large and some application may not be tolerant of them. Body-contacted FETs can be used to minimize this effect in SOI. Silicon-on-insulator (SOI) technology is widely adopted to mitigate drain-induced-barrier-lowering (DIBL) and to suppress fringing fields and charge sharing effects that have become dominant in short-channel CMOS technologies [13]-[14]. SOI technology has been used in 65-nm, 45-nm, and 32-nm CMOS technologies [26], [27]. SOI also offers additional design advantages over traditional bulk CMOS technologies. These advantages include a significant reduction in cross-talk between on-chip RF and digital circuitry, and the ability to integrate high quality, passive elements on-chip (thanks to larger substrate resistivity).

Therefore, SOI technology has an advantage in performance over bulk technologies (at an added cost of course!). However, the different reliability mechanisms of SOI technologies are still an active area of research.

1.2.3 Digital-CMOS vs. RF-CMOS

Digital technologies are optimized for digital circuits and RF technologies are optimized for analog/RF circuits. Most of the digital CMOS circuits require narrow width devices ($W < \sim 1 \mu m$), whereas RF-CMOS circuits require much larger width devices ($W \sim 100 \mu m$). Large width is required in RF devices to get sufficient current and gain from the device. Because of the large widths, the devices are laid-out in multiple gate-finger configuration (see Figure 5).

The gate resistance of a MOSFET is given by (Eqn. 1):

$$R_g = \frac{R_{poly}W_F}{3n^2L}, \quad (1)$$

where R_{poly} is the poly-silicon gate sheet resistance, W_F is the gate-finger width, n is the number of gate contacts, and L is the channel length. Therefore, W_F is made smaller, and n is made larger to minimize R_g . A smaller R_g results in smaller noise. Device width has a significant effect on the performance and reliability of a CMOS

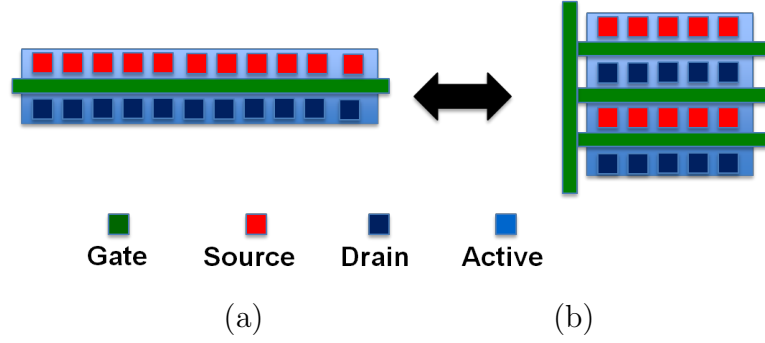


Figure 5: Top-view layout comparison of (a) single-finger digital nFET and (b) multi-finger RF nFET.

device (as will be shown later). Thus, a digital-CMOS device behaves very different from a RF-CMOS device. The side-view layout of FETs connected in a multi-finger configuration is shown in Figure 6.

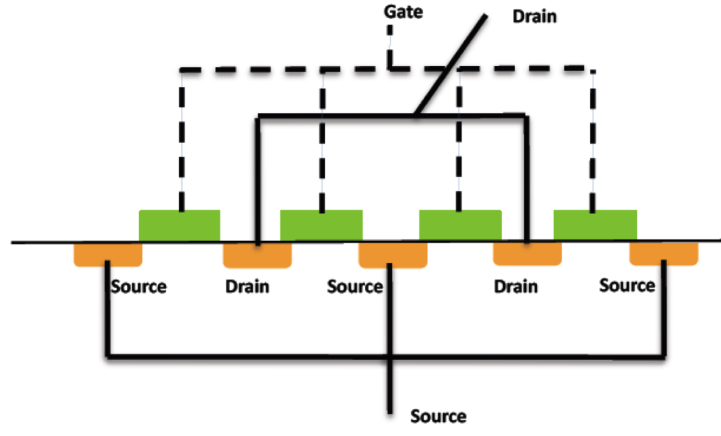


Figure 6: Side-view layout of a multi-finger RF nFET.

1.2.4 BEOL in Short-Channel CMOS Technologies

Back-End-of-Line (BEOL) in semiconductor technology refers to the transmission lines and passives (inductors, capacitors, resistors, and transformers). In a bulk CMOS technology, the silicon wafer doping is relatively high to prevent latchup. A high wafer-doping results in poor quality of transmission lines and passives on silicon. With technology scaling the BEOL has also scaled down (Figure 7).

The metal line thicknesses and the spacing between two metal layers have decreased.

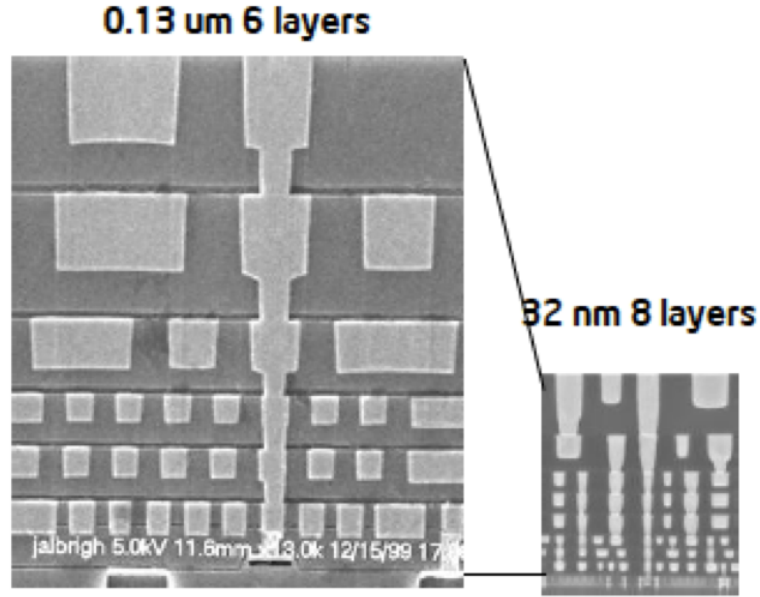


Figure 7: SEM images of 130-nm six layer metal stack vs. 32-nm eight layer metal stack [10].

This has resulted in further lower quality factors of transmission lines and passives. SOI technologies have improved passive quality factors because of larger resistivity of the substrate. BEOL metal layers can affect a transistor performance through parasitics.

1.3 Reliability Mechanisms in a CMOS Technology

The following are the major reliability concerns for any CMOS technology:

1.3.1 Hot-Carrier Effects

Hot-carrier effects are caused by the high electric-field induced impact-ionization in a semiconductor. The high electric-field creates highly energetic carriers ('hot' electrons/holes) that can create defects at the interface of two different materials (e.g. at the semiconductor-oxide interface in a MOSFET) [28], [29]. These defects at the material interface trap electrons/holes and result in shift in device parameters, such as threshold voltage, transconductance, off-state and on-state current, output resistance, etc. Both bulk and SOI processes are prone to this degradation mechanism.

For long-channel length MOSFETs, the worst hot-carrier stress condition is at $V_{GS} = \sim V_{DD}/2$ (peak substrate-current gate bias). However, this classical prediction does not work for short-channel MOSFETs [30].

1.3.2 Negative/Positive Bias Temperature Instability (NBTI/PBTI)

NBTI/PBTI is a physical phenomenon that occurs when pFETs/nFETs are operated at high temperatures. NBTI/PBTI testing of a pFET/nFET is done at a constant negative/positive bias applied to the gate electrode at high temperatures, with source, drain, and substrate grounded. When the MOSFET operates at high temperatures, a reaction-diffusion process causes the diffusion of hydrogen species from the semiconductor-oxide interface, creating interface traps [31], [32]. These interface traps can cause a shift in device threshold voltage, transconductance, etc. Both bulk and SOI processes are prone to this degradation mechanism.

1.3.3 Dielectric Breakdown

State-of-the-art short-channel length MOSFETs have gate-dielectrics as thin as ~ 1 -nm. However, the supply voltages have not scaled down at the same rate as the gate-oxide thickness. Thus large electric-fields exist across the thin gate-oxide. This large electric-field can cause carriers to tunnel across the oxide. These energetic carriers can create damage paths through the gate-oxide and can eventually cause large leakage currents to flow. Such a situation is called a dielectric breakdown [33]. Once the dielectric breaks down the transistor is rendered useless and cannot be used for switching or amplification applications anymore. Both bulk and SOI MOSFETs are sensitive to this degradation mechanism.

1.3.4 Large RF Stress Effects in CMOS

Large input RF stress can cause significant damage in BiCMOS technologies [34]. RF signal superimposed on a DC bias can cause voltage swings across a device, which

are beyond the safe-operating area of the device. This can cause the creation of traps in the gate-oxide and/or gate-oxide dielectric breakdown. Creation of interface traps at the silicon to gate-oxide interface causes decrease in carrier mobility and hence decrease in on-state current, transconductance, small-signal gain, power-gain, etc. Dielectric breakdown can result in catastrophic degradation of device parameters, rendering a device useless.

1.3.5 Latchup

Latchup can be caused in a semiconductor when there is a p-n-p-n doping path. Such a doping path exists in various circuits, e.g. a CMOS inverter having a pMOSFET and nMOSFET [35], [5]. Such a p-n-p-n doping path results in the existence of parasitic PNP and NPN bipolar transistors connected in a positive feedback loop. Once the gain of this parasitic feedback loop becomes larger than one ($\beta_{PNP} \beta_{NPN} > 1$), a negative differential resistance action happens (current increases even at lower voltages) and results in excessive current through the p-n junctions, which can break them down. Latchup can also cause electro-migration and gate-oxide breakdown. Latchup is a significant concern in bulk technologies. Guard-ring structures are added in bulk technologies to prevent latchup. Latchup is automatically avoided in a SOI structure because of no p-n-p-n doping paths.

1.3.6 Ionizing Radiation Damage

Ionizing radiation effects are a concern in MOSFETs operating in space environments or in terrestrial applications with high radiation dose (e.g. nuclear reactors or medical facilities). Ionizing radiation creates electron-hole pairs in a semiconductor or oxide. The electron-hole pairs can re-combine quickly in a semiconductor. However, holes get trapped in the oxides because of their lower mobility than electrons. The holes can be trapped in gate-oxide bulk-traps, gate-oxide interface traps, and/or isolation oxide (field oxide or shallow trench oxides) traps [36]-[38] (Figure 8). These hole traps

can cause shift in MOSFET parameters, such as threshold voltage, transconductance, off-state current, etc. SOI technologies are more prone to ionizing radiation effects because of the presence of buried oxide, which also traps the radiation generated holes and causes MOSFET parameter shifts (Figure 9).

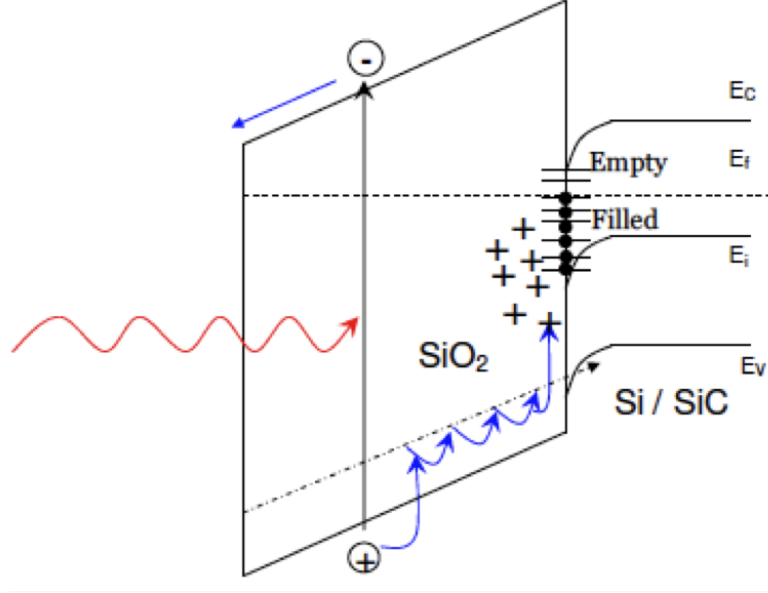


Figure 8: Schematic representing the fundamental radiation induced electron-hole pair generation with bulk hole trapping and movement of the charge centroid to the interface under bias [38].

1.3.7 Single-Event Effects (SEE)

SEE are caused in space environments where particles such as heavy ions (oxygen, helium, etc.) can strike a semiconductor material. These ion strikes create electron-hole pairs in semiconductors that are collected at one of the transistor terminals. Such a collection of carriers causes current spikes at transistor terminal, which can corrupt the digital circuit operation state. Single-event effects have become a significant concern for short-channel length MOSFETs as a single ion strike can cause current spikes in multiple devices [39], [40]. Heavy ion strikes can also cause single-event-gate-rupture (SEGR), single-event-latchup (SEL). SOI technologies are immune to SEE to a first-order.

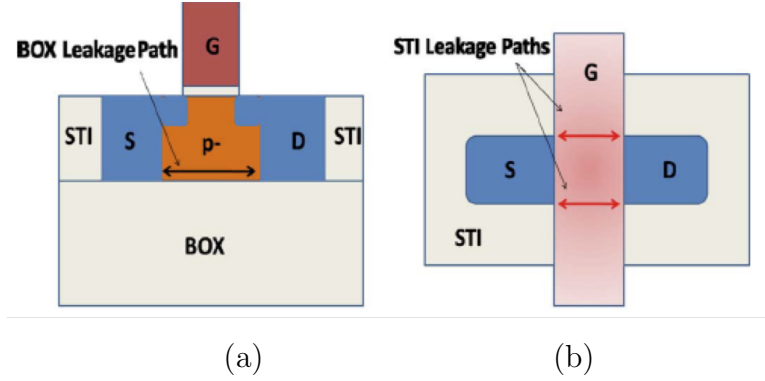


Figure 9: Possible radiation-induced leakage paths along the (a) surface of buried-oxide (BOX) and (b) STI sidewalls.

1.3.8 Low- or High- Temperature Effects

Temperature plays a major role in the operation of semiconductor devices. Devices are designed such that they can operate across a wide temperature range. Carrier mobility in a semiconductor increases at low temperatures and decreases at high temperatures. The carrier recombination-generation is also affected by temperature, which affects the off-state current of MOSFETs. Threshold voltage of nMOSFETs increases at low temperatures and decreases at high temperatures. Both SOI and bulk transistors behave in a similar way across temperature to a first-order [41]-[43].

1.3.9 Electro-Migration

Electro-migration is the opening of metal lines on an integrated circuit as a result of the material voids created by high currents flowing through them. The thickness of the metal lines and of the vias should be chosen carefully considering the current flowing through those lines. Electro-migration can be an issue in both bulk and SOI technologies [44].

1.3.10 Electro-Static Discharge (ESD)

ESD is a serious concern for integrated circuits. Spurious ESD pulses like those arising from handling of packaged devices can damage the devices, and can cause manufacturing yield loss and reliability failures. The scaling trend towards thinner

gate-oxides aggravates this problem. ESD can cause large current pulses (of the order of amperes) to flow through the miniature MOSFETs, thereby damaging the gate-oxides. ESD protection circuits are commonly used to prevent such large currents from flowing into the input MOSFET gate [45]. Both bulk and SOI processes are susceptible to ESD failure.

1.3.11 Antenna Effects

Process plasma charging during fabrication processes and the resulting gate-oxide damage is a major reliability concern for sub 100-nm CMOS technologies. During plasma processing, current passes through the thin gate-oxide as if it was under high electric field stress. The large metal lines present on the wafer act as antennas and the plasma charge moves from antenna to antenna destroying the thin gate-oxides of the MOSFETs connected to those antennas [46]. Foundries normally supply antenna rules, which are rules that must be obeyed to avoid this problem. Antenna rules are normally expressed as the allowable ratio of metal area to gate area. There is one such ratio for each interconnect layer. Antenna diodes are connected in parallel to the susceptible MOSFET gate to prevent gate-oxide damage. Both bulk and SOI processes are susceptible to antenna effects.

For a partially-depleted SOI device, alongside the above mentioned reliability concerns, the floating-body effect poses major challenge for large-scale design. The kink-effect and the history-effect resulting from floating-body device is a major problem [13], [47]. In a SOI technology, both floating-body and body-contacted MOSFET options are available. A body-contacted device allows a contact to the MOSFET body, which can be grounded or biased to a specific value. In this work, the results are presented for 65-nm, 45-nm, and 32-nm RF-CMOS on SOI technology, however, these results are valid for any short-channel SOI technology. Several trade-offs exist between

performance and reliability mechanisms in these sub 100-nm CMOS technologies, and will be the focus of this work (Figure 10).

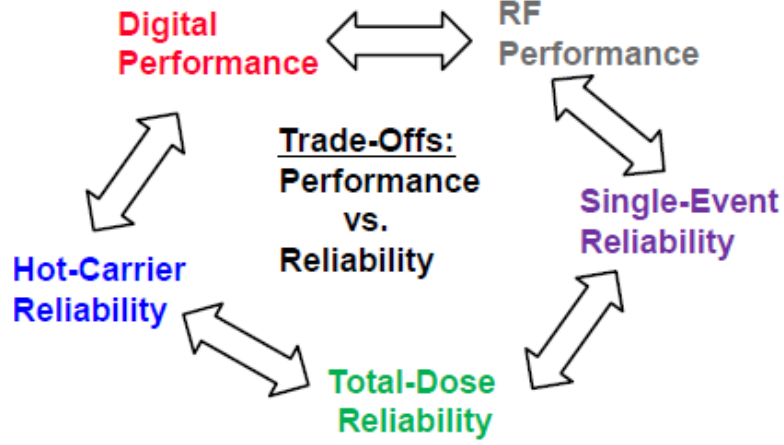


Figure 10: Trade-offs between performance and reliability in sub 100-nm CMOS technologies.

1.4 *Organization and Contributions of the Dissertation*

The objective of this research is to enhance the understanding of different reliability mechanisms in CMOS devices and circuits, and to understand the trade-offs between performance and reliability of sub 100-nm CMOS technologies. In this direction, several reliability-performance trade-offs studies have been carried out. Such trade-offs are used to demonstrate high performance reliable circuits. This research has leveraged access to the IBM 180-nm (7RFSOI), 65-nm (11soi), 45-nm (12soi), and 32-nm (32soi) RF-CMOS platforms as well as multiple generations of commercially available SiGe BiCMOS technologies.

Chapter 2 discusses the role of floating-body effects on the performance and reliability of sub-100 nm CMOS-on-SOI technologies [1], [2]. It is demonstrated through experimental data and TCAD simulations that floating-body devices have improved RF performance but worse reliability compared to body-contacted devices. Further, the floating-body effects in cascode cores is studied. Cascode cores are demonstrated

to achieve much larger reliability lifetime than a single device. A variety of cascode topologies are studied to achieve the trade-offs between performance and reliability for high-power applications [2].

Chapter 3 discusses the use of body bias to modulate the performance and reliability of devices and single-pole-double-throw (SPDT) switches. The SPDT switch performance is shown to improve with a negative body-bias.

Chapter 4 discusses the impact of device width on the RF performance and reliability in sub 100-nm CMOS. Larger width devices are shown to have greater degradation, posing challenging questions for RF design in strained-Si technologies [3].

Chapter 5 shows a novel study showing the effect of source/drain metal contact spacing and gate-finger to gate-finger spacing on the device RF performance. Further, the impact of above on the hot-carrier, RF stress, and total-dose irradiation tolerance is studied [3], [4].

Chapter 6 shows that the latchup phenomenon in CMOS technologies is possible at cryogenic temperatures (below 50 K), and its consequences are discussed [5]. The results of this section are crucial for latchup hardness of circuits operating in extreme conditions.

Chapter 7 discusses a time-dependent device degradation model developed in technology computer aided design (TCAD) to model reliability in CMOS and SiGe devices. Mixed-mode and reverse EB-bias stress in a SiGe technology is modeled.

Chapter 8 discusses the total-dose irradiation tolerance and hot-carrier reliability

of 32-nm CMOS-on-SOI technology. The impact of HfO_2 based gate dielectric on the performance and reliability is studied [6]. The impact of technology scaling from 65-nm to 32-nm on the performance and reliability of CMOS technologies is studied [6].

Chapter 9 discusses the cryogenic performance and cryogenic hot-carrier reliability of 45-nm CMOS-on-SOI technology. The MOSFET reliability is shown to improve at cryogenic temperatures.

CHAPTER II

OPERATING VOLTAGE CONSTRAINTS IN 45-NM SOI NFETS AND CASCODE CORES

2.1 *Overview*

Operating voltage constraints and hot-carrier reliability (HCR) in 45-nm SOI RF nMOSFETs and cascode cores is investigated. Devices with ‘floating’ body and ‘contacted’ body are investigated. It is shown through experimental results that floating-body (FB) devices have greater HCR degradation compared to body-contacted (BC) devices. The physical mechanisms responsible for this phenomenon are investigated in detail through technology CAD (TCAD) simulations. Cascode cores with both FB devices, with FB and BC devices, and with both BC devices are studied. The trade-offs in the DC and radio-frequency (RF) performance of these cascodes is examined. A HCR study is done on the cascodes and it is shown that the cascodes have a much longer lifetime compared to a single device operating at similar bias conditions. BC-BC cascode is shown to have a much longer lifetime than BC-FB and FB-FB cascodes. The physical mechanisms behind HCR degradation in these cascodes is studied through TCAD simulations. Taken together, these results have serious consequences for high performance-reliability RF circuit design in 45-nm CMOS-on-SOI.

The contents of this chapter have been published in part at [2].

2.2 *Motivation*

Every technology has a fixed defined maximum operating voltage (V_{DD}). This is the maximum voltage that can be applied across the gate and drain of a MOSFET, at which there is no significant performance degradation over the device lifetime. With

technology scaling, the maximum operating voltage (V_{DD}) has scaled down (Figure 11). However, the device threshold voltage (V_{TH}) has not scaled down by the same factor as the technology V_{DD} . For a 45-nm technology the V_{DD} is 1.0 V. A variety of circuit applications require high performance devices which can also take large voltage swing across the drain-source and/or gate-source junctions. Examples of such circuits include Class-AB push-pull amplifiers, radio-frequency (RF) power amplifiers etc. Hybrid use of thick (high breakdown) and thin (high performance) gate-oxide devices has been used in such applications [48]. However, the thick gate-oxide device slows down the circuit. In this chapter we will show that a combination of BC and FB devices can be used for these applications. We studied the trade-offs and show which particular SOI device work best for a cascode type amplifier for high performance-reliability applications.

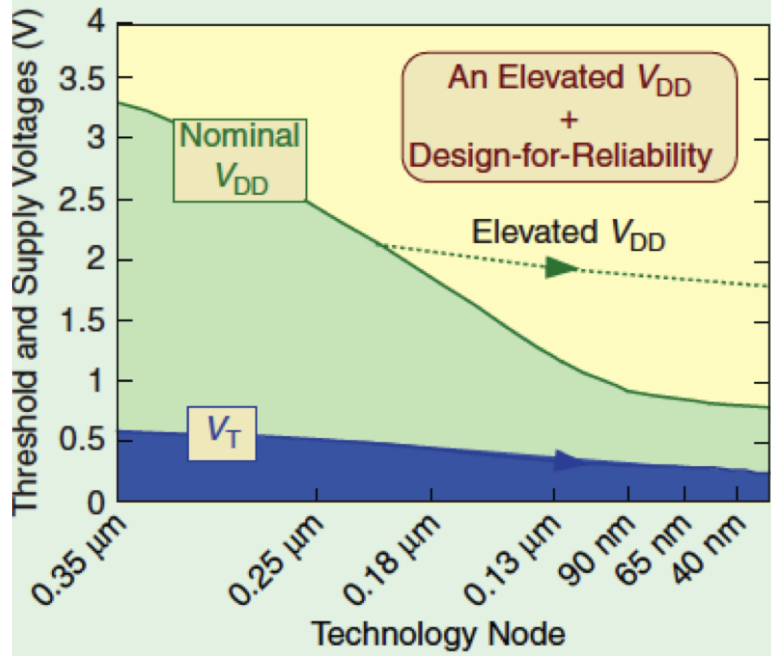


Figure 11: Transistor threshold voltage and supply voltage as function of technology node [48].

It remains to be seen how the devices actually behave at voltages above V_{DD} . i.e. What is the device lifetime at higher than V_{DD} drain bias?. The device performance

normally increases at higher V_{DD} . The impact of FB effects on a single device are also relatively unknown at the circuit level. In this chapter we study cascode cores as a test circuit to show the impact of FB effects in a 45-nm nMOSFET on a circuit. Another question is how much voltage swing can a cascode configuration device commonly used in amplifiers take. Should the V_{DD} of a cascode amplifier be the same as the V_{DD} of a single device? Some of these safe-operating area (SOA) related issues have been looked into on 130-nm SiGe heterojunction bipolar transistor based cascodes [34]. For low power applications its important to know the minimum voltage on gate and drain of a single device or cascode to get a good gain? These questions will be answered through SPICE, TCAD simulations, and measurements in this work.

2.3 Device Technology and Experimental Details

The process details of the 45-nm partially depleted RF-CMOS SOI technology have been published previously [25], [26]. The devices have an asymmetric halo doping which improves the device performance [25]. Asymmetric halo doping devices also have less hot-carrier reliability problems as compared to symmetric halo doping devices [1]. FB and BC device options are available within this platform. In general, FB devices have improved RF performance (power-gain, linearity, f_T , f_{max}), as compared to BC devices. However, BC devices exhibit better reliability, forcing a trade-off between performance and reliability. The devices used in this study were laid out in multiple gate finger (20 fingers) arrangements, similar to that commonly used in RF circuit design, in order to minimize the gate resistance ($W_{FINGER} = 2.0 \mu m$, $L = 45 \text{ nm}$, $W_{TOTAL} = 40.0 \mu m$). These devices are from a commercial silicon technology and have not been radiation hardened in any way. For hot-carrier stress testing, the devices were stressed in the drain avalanche hot-carrier condition (DAHC). The measurements were made in-situ. The RF measurements are performed at X-band (10 GHz) on a custom integrated S-parameter and load-pull system, which allows both small- and

large-signal measurements with a single probe contact. Each device was measured at least two times with the same set of conditions to check for data fidelity. Figure 12 shows the DC and RF characteristics of the FB and BC devices. FB devices have a larger DC on-state current and a larger cut-off frequency and power-gain than BC devices.

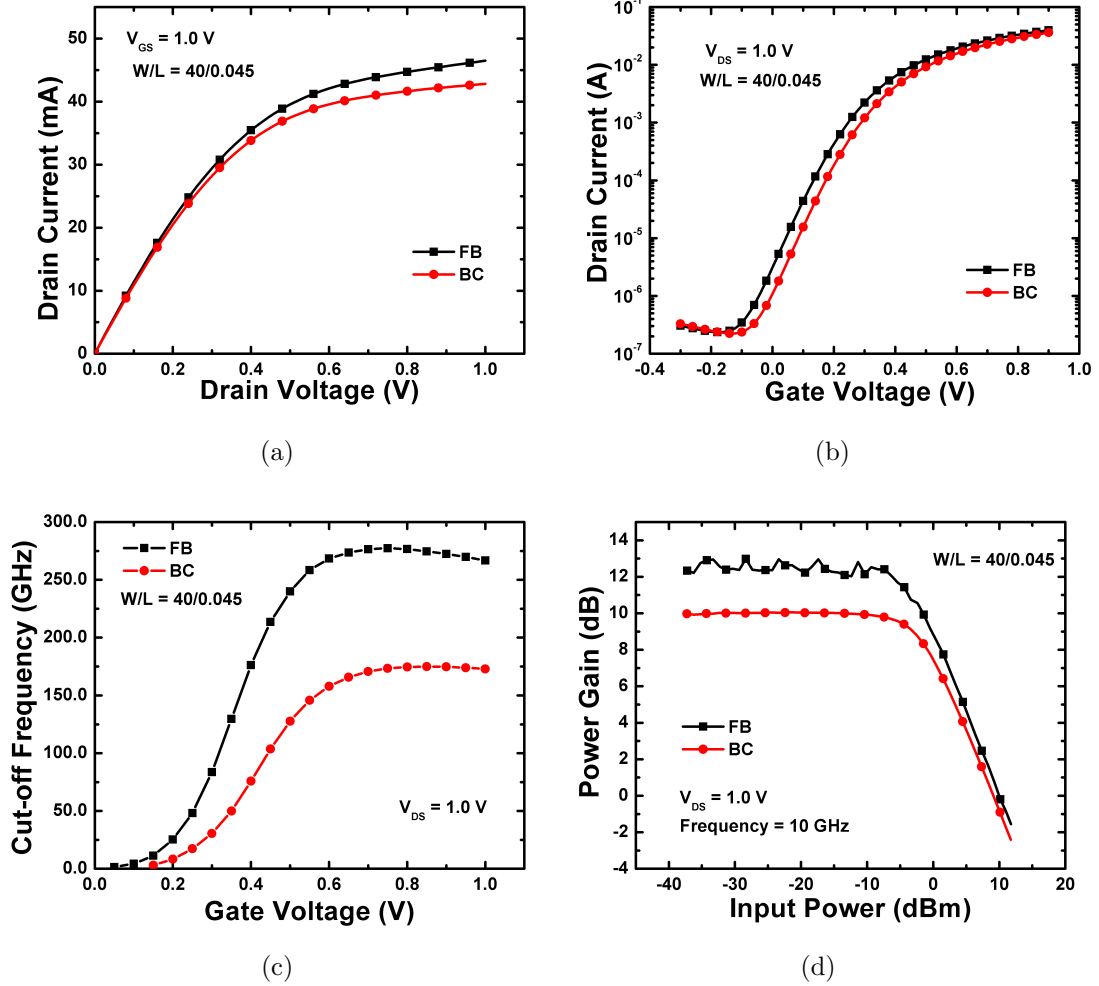


Figure 12: Measured (a) drain current as a function of drain voltage, (b) drain current as a function of gate voltage, (c) cut-off frequency as a function of gate voltage, and (d) power-gain as a function of RF input power of a FB and BC device.

2.4 Device Voltage Constraints

2.4.1 Impact of Gate and Drain Bias on the Power-Gain and Single-Tone Linearity of a FB and BC Device

The power-gain of a FB and BC device increases slightly with increasing drain-voltage, going from ~ 11.9 dB to ~ 13.0 dB (Figure 13(a)). The major advantage of increasing drain voltage is the increasing linearity. The 1 dB compression point of the FB devices increases with increasing drain voltage from ~ -7 dBm to ~ 3 dBm (Figures 13(a)). Figure 13(b) shows the impact of the gate bias on the power-gain and linearity of a FB device. The threshold voltage of the device is ~ 0.25 V. Below the threshold voltage, the power-gain is really small. However, just above the threshold voltage the power-gain is significant and does not increase significantly with increasing gate bias. This shows the potential of the technology for low-power sub-threshold applications. Significant gain and linearity can be achieved from the devices at low-current levels. The BC devices show similar trends, and are excluded here for brevity. Figure 14 shows the electric field in the channel region for a 45-nm FB nMOSFET for varying drain bias. At small drain bias, the electric field at the drain-body and source-body junction is similar. At larger drain bias, the electric field at drain-body junction is greater compares to source-body junction.

2.4.2 Hot-Carrier Reliability of a Single FB and BC Device

The FB and BC devices were tested in worst-case degradation condition ($V_{GS} = V_{DD} = 1.0$ V). In sub 100-nm nMOSFETs, the maximum substrate/body current is observed close to $V_{GS} = V_{DD}$ [30]. The drain was biased under drain avalanche hot-carrier (DAHC) condition at $V_{DS} = 1.5$ V. The devices were stressed at room temperature. The shift in threshold voltage as a function of the stress time for FB and BC device is shown in Figure 15(a). FB devices have larger positive shift in threshold voltage (and larger on-state current degradation) as compared to BC devices. A positive shift in threshold voltage is caused by hot-electron trapping in the gate-oxide. The device

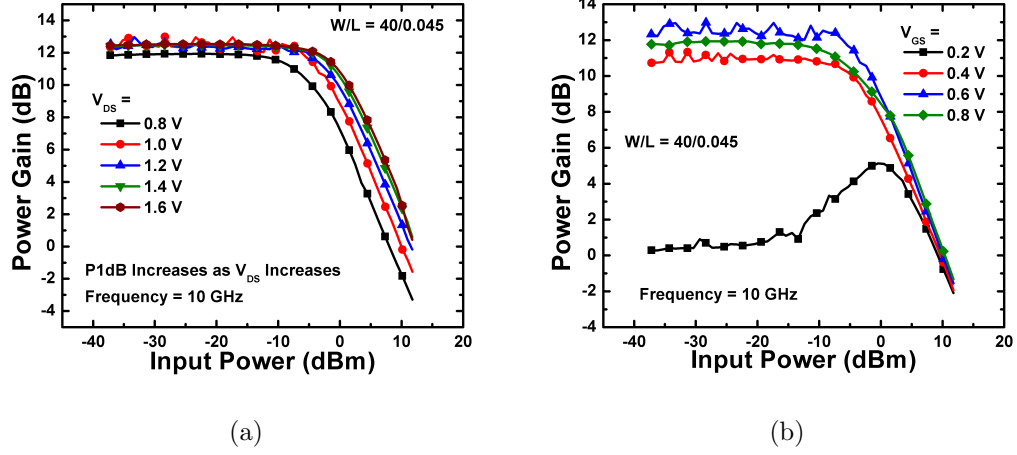


Figure 13: Measured (a) power-gain as a function of RF input-power of a FB device with varying drain voltage ($V_{GS} = 0.6$ V) and (b) power-gain as a function of RF input-power of a FB device with varying gate voltage ($V_{DS} = 1.0$ V).

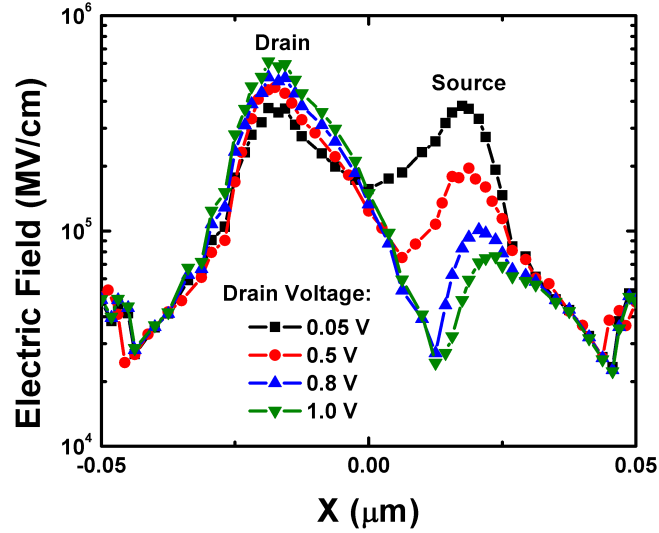


Figure 14: Electric field in the channel region of a 45-nm nMOSFET for varying drain bias.

lifetime for varying drain stress conditions is shown in Figure 15(b). The FB devices have about an order of magnitude smaller lifetime compared to BC devices.

Calibrated 2-D TCAD models were developed for the 45-nm FB and BC nMOSFETs. The electric fields in the FB and BC devices are extracted from these calibrated TCAD models. The electric field distribution in the channel region for the devices

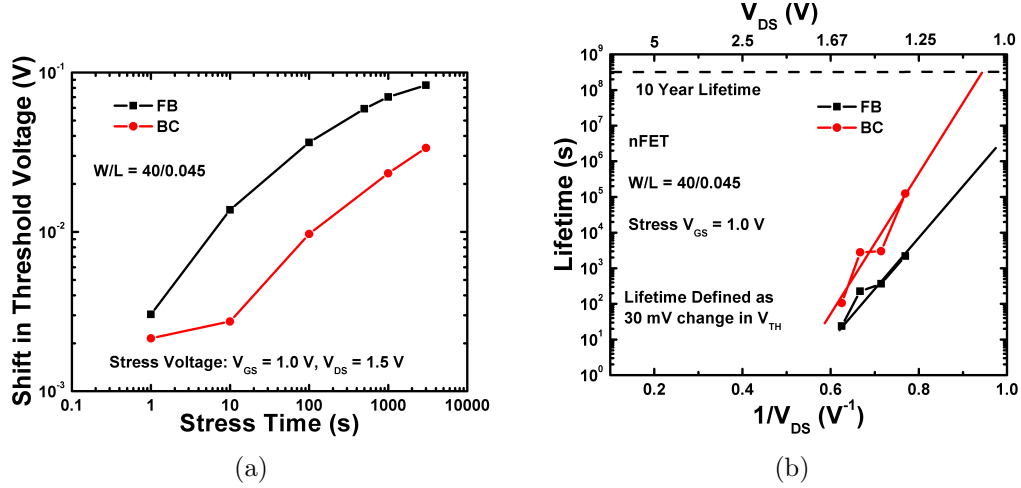


Figure 15: (a) Shift in threshold voltage as a function of stress time of FB and BC devices. (b) Lifetime (in seconds) as a function of the inverse of drain voltage of FB and BC devices.

are shown in Figure 16(a). The electric field values are very similar for the FB and BC devices near drain. However, the electric field values are much larger for the BC device near the source. The BC devices have a larger electric field because the body potential is much closer to 0 V (body terminal grounded). However, for a FB device the body terminal floats to a potential greater than 0 V ($\sim 0.2 - 0.3$ V in this case). Hence the larger potential difference for the BC device results in larger electric field. This phenomenon can be explained by looking at the energy band diagram in the channel region (Figure 16(b)). The larger energy difference in the channel region results in larger electric field for the BC device. Also, the BC devices have a larger electric field at the source-body junction compared to the drain-body junction. This is because of the larger change in potential over distance for the source-body junction as compared to the drain-body junction (Figure 16(c)).

Larger device lifetime for BC devices can be explained by looking at the impact ionization induced avalanche generation in the channel region (Figure 16(d)). A larger avalanche generation results in highly energetic carriers in the channel region in FB devices. These energetic carriers reach the silicon-oxide interface and have a tendency to get trapped (or create traps) in the gate oxide at either the oxide or interface traps.

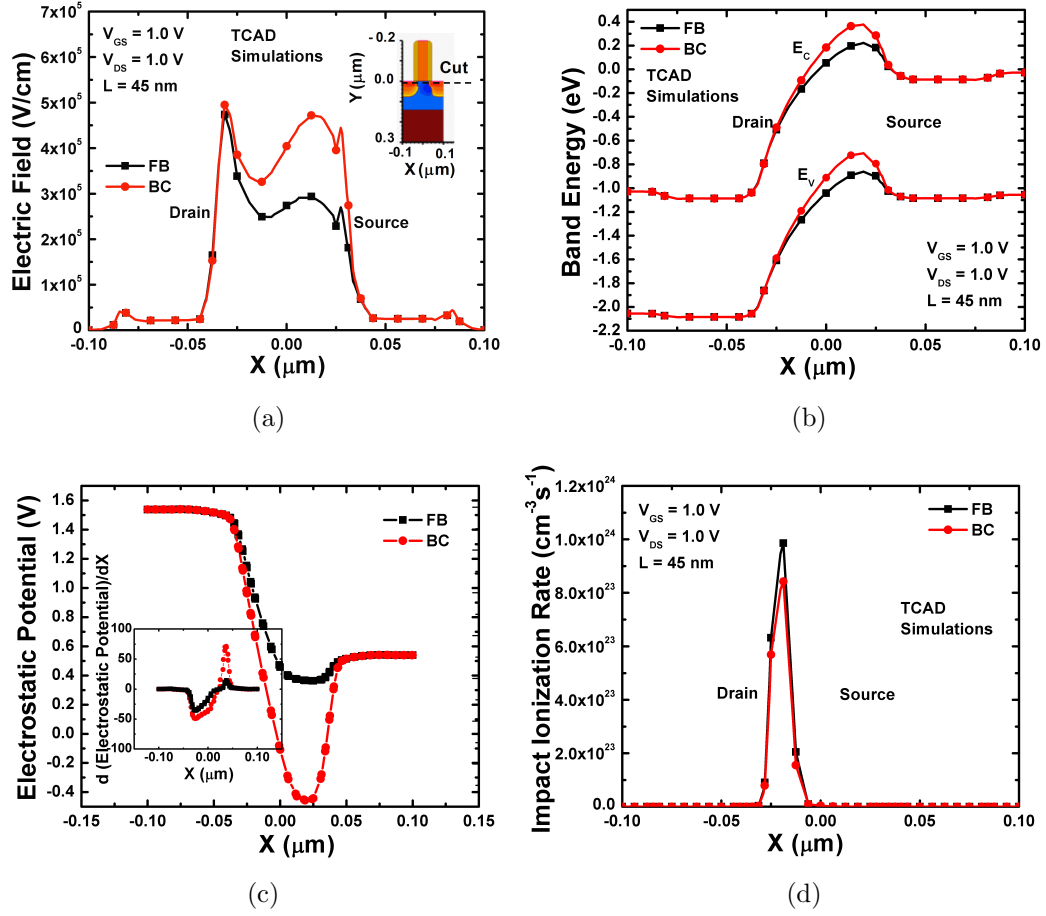


Figure 16: (a) Electric field in the channel region of a FB and BC device at constant gate and drain voltage ($V_{GS} = 1.0$ V, $V_{DS} = 1.0$ V). (b) Conduction band energy in the channel region of a FB and BC device. (c) Electrostatic potential in the channel region of a FB and BC device. (d) Impact ionization induced avalanche generation rate in the channel region of a FB and BC device.

The trapped electrons in the gate oxide cause the positive threshold voltage shift observed in the devices. A large electric field and wide space charge region results in electron-hole pair production due to avalanche generation. If the width of the space charge region is larger than the mean free path between the ionizing impacts, charge multiplication can occur. The reciprocal of the mean free path is called the ionization coefficient α [49]. The avalanche generation rate is given by:

$$G^{ii} = \alpha_n n v_n + \alpha_p p v_p \quad (2)$$

where n and p are the electron and hole concentrations, respectively. v_n and v_p are

the electron and hole velocity, respectively. Larger the ionization coefficient, carrier concentration, and carrier velocity, larger the avalanche generation rate. The carrier velocity is a product of the carrier mobility and electric field. The ‘University of Bologna’ avalanche generation model was used in our simulations.

2.5 Circuit Voltage Constraints

2.5.1 Cascode Cores in 45-nm CMOS-on-SOI

Cascode configurations are used in a variety of circuit topologies. They are used in analog applications to improve the output resistance (r_O), and hence the self-gain ($g_m \cdot r_O$). They are used in RF circuits such as low-noise amplifiers, and power amplifiers to increase the gain and isolation from input to output. We designed three cascode test structures with a) FB common-source and FB cascode device (FB-FB), b) FB common-source and BC cascode device (BC-FB), and c) BC common-source and BC cascode device (BC-BC) (Figure 17). The FB and BC device size in the cascodes is the same as for the individual devices shown above ($L = 45$ nm, $W_F = 2.0$ μm , $N_F = 20$). The body contact of the BC devices is connected to the source of that device (Figures 17(b), 17(c)). The DC characteristics of the cascode structures are shown in Figure 18. FB-FB have larger current than BC-FB test structures. FB-FB structures show the floating-body effects with kinks in the I - V characteristics (and also a smaller r_O). The cut-off frequency (f_T) as a function of the common-source gate voltage is shown in Figure 19. FB-FB cascode has the largest f_T and BC-BC has the smallest. The larger f_T for FB-FB cascodes is because of larger g_m and smaller parasitics capacitances (C_{GS} and C_{GD}).

2.5.2 Impact of Gate and Drain Bias on the Power-Gain and Linearity of a Cascode Core

The cascodes were source and load matched for the power measurements. Figure 20 shows the power-gain as a function of input power of the FB-FB and BC-FB cascodes.

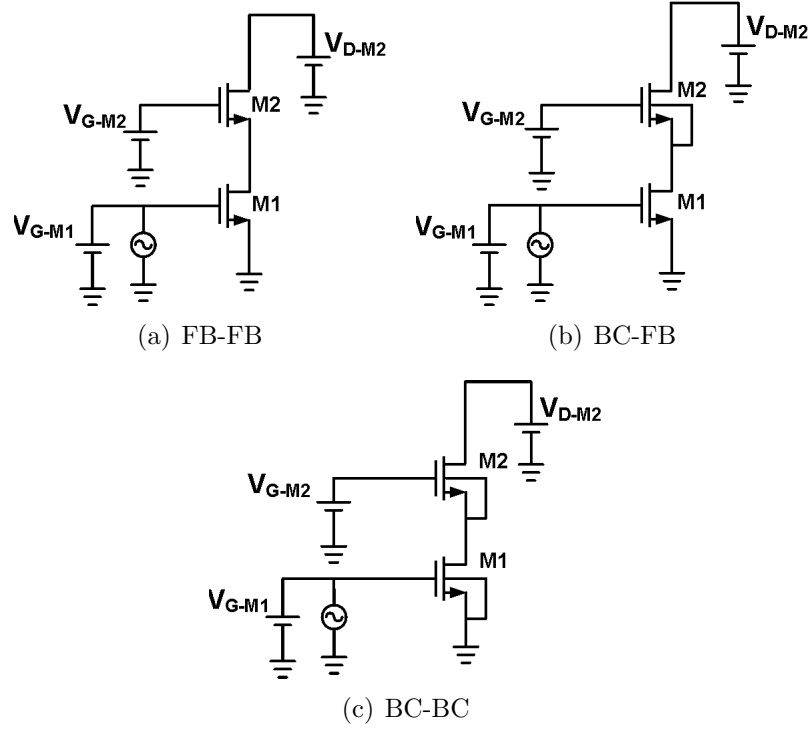


Figure 17: Cascode test structure with (a) FB common-source and cascode device (b) FB common-source and BC cascode device (c) BC common-source and BC cascode device.

FB-FB cascode has a larger power-gain than the BC-FB cascode. However, the BC-FB cascode has a larger 1 dB power compression point. BC-FB cascode has a larger power added efficiency (PAE) because of the lower DC power dissipation. Comparison of Figures 13(a) and 20 shows that the single devices have a larger linearity than the cascode test structures. Increasing drain bias also helps improve the 1 dB compression point of cascodes (Figure 20(b)).

2.5.3 Hot-Carrier Reliability of the Cascode Cores

The cascode test structures were tested for HCR at the same bias condition ($V_{G-M2} = 1.5$ V, $V_{G-M1} = 1.0$ V, varying drain bias). The shift in threshold voltage at the same bias condition for the three cascodes are shown in Figure 21(a). The BC-FB cascode has the largest shift in threshold voltage. The threshold voltage shift of the FB-FB cascodes is very close to the BC-FB cascode. BC-BC cascode has a very small

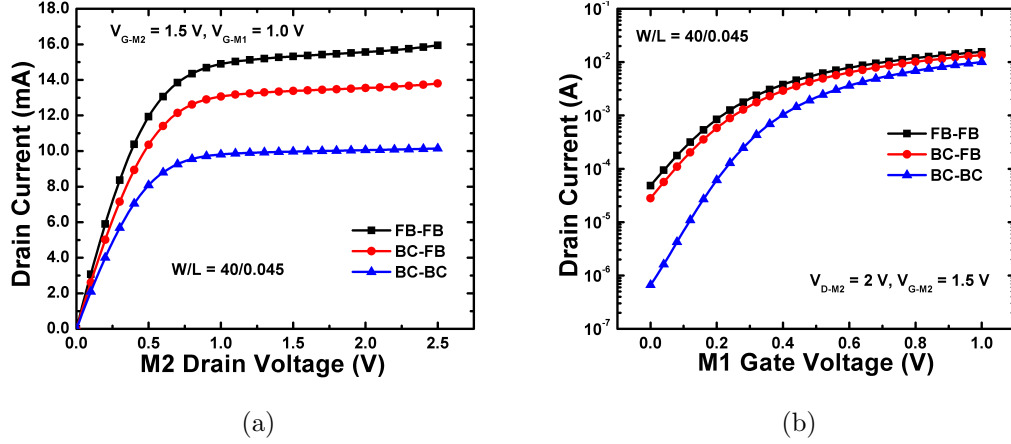


Figure 18: (a) Measured drain current as a function of the drain voltage and (b) drain current as a function of M1 gate voltage of the FB-FB, BC-FB and BC-BC cascode cores.

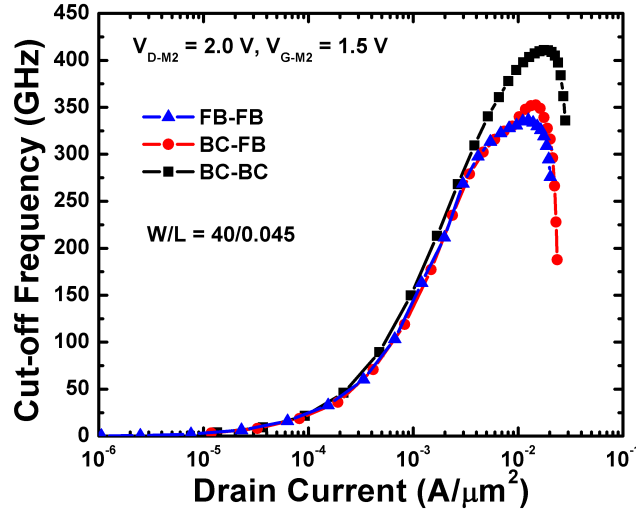


Figure 19: Cut-off frequency as a function of M1 gate voltage of the FB-FB, BC-FB and BC-BC cascode cores.

change in threshold voltage. The device lifetime as a function of the inverse of V_{DD} is shown in Figure 21(b). The FB-FB and BC-FB have very similar device lifetimes, which are much smaller than those of the BC-BC cascode. FB-FB cascodes actually have a slightly larger lifetime than BC-FB cascodes.

The cascode test structures were simulated in TCAD to understand the physical mechanisms. The source of the cascode device and the drain of the common-source device were connected through copper. The electrostatic potential of the source of the

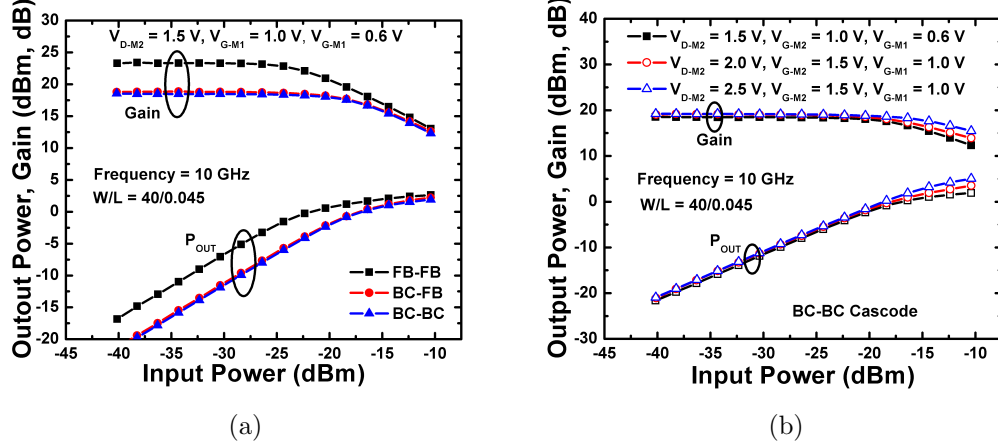


Figure 20: (a) Power-gain as a function of RF input-power of FB-FB, BC-FB, and BC-BC cascodes ($V_{D-M2} = 1.5$ V, $V_{G-M2} = 1.0$ V, $V_{G-M1} = 0.6$ V). (b) Power-gain as a function of RF input-power of BC-BC cascode for varying bias voltage.

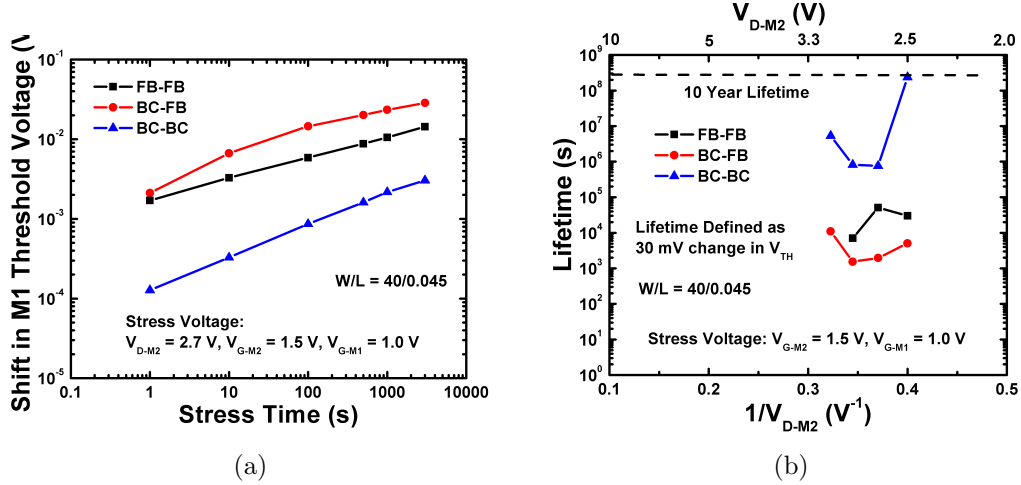


Figure 21: (a) Shift in threshold voltage as a function of stress time of the three cascodes. (b) Lifetime (in seconds) as a function of the inverse of drain voltage of the cascodes.

cascade device and the drain of the common-source device match. The electric field distribution in the channel region for the three cascodes is shown in Figure 22(a). The cascodes with BC devices have larger electric field than FB-FB cascode. The BC-BC cascode has the largest electric field in the common-source device. The conduction and valence band energies for the three cascodes in the channel region are shown in Figure 22(b). The BC-FB cascodes have the largest voltage drop across the cascode device and FB-FB cascode has the smallest voltage drop. The BC-BC cascodes have a larger

Table 1: Voltage and current across the cascode devices

Cascode	V_{D-M2} (V)	V_{G-M2} (V)	V_{G-M1} (V)	V_{DS-M2} (V)	V_{GS-M2} (V)	V_{DS-M1} (V)	I_{DS-M2} (mA)	V_{BS-M2} (V)	V_{BS-M1} (V)
FB-FB	2.7	1.5	1.0	2.031	0.831	0.669	20.70	0.651	0.249
BC-FB	2.7	1.5	1.0	2.252	1.052	0.447	18.44	0.040	0.179
BC-BC	2.7	1.5	1.0	2.112	0.911	0.588	14.96	0.037	0.002

electric field because of a larger change in potential over distance. The avalanche generation rates for the three cascodes are shown in Figure 22(c). The FB-FB cascode has the largest generation rate in the common-source device and the BC-FB cascode has the largest generation rate in the cascode device.

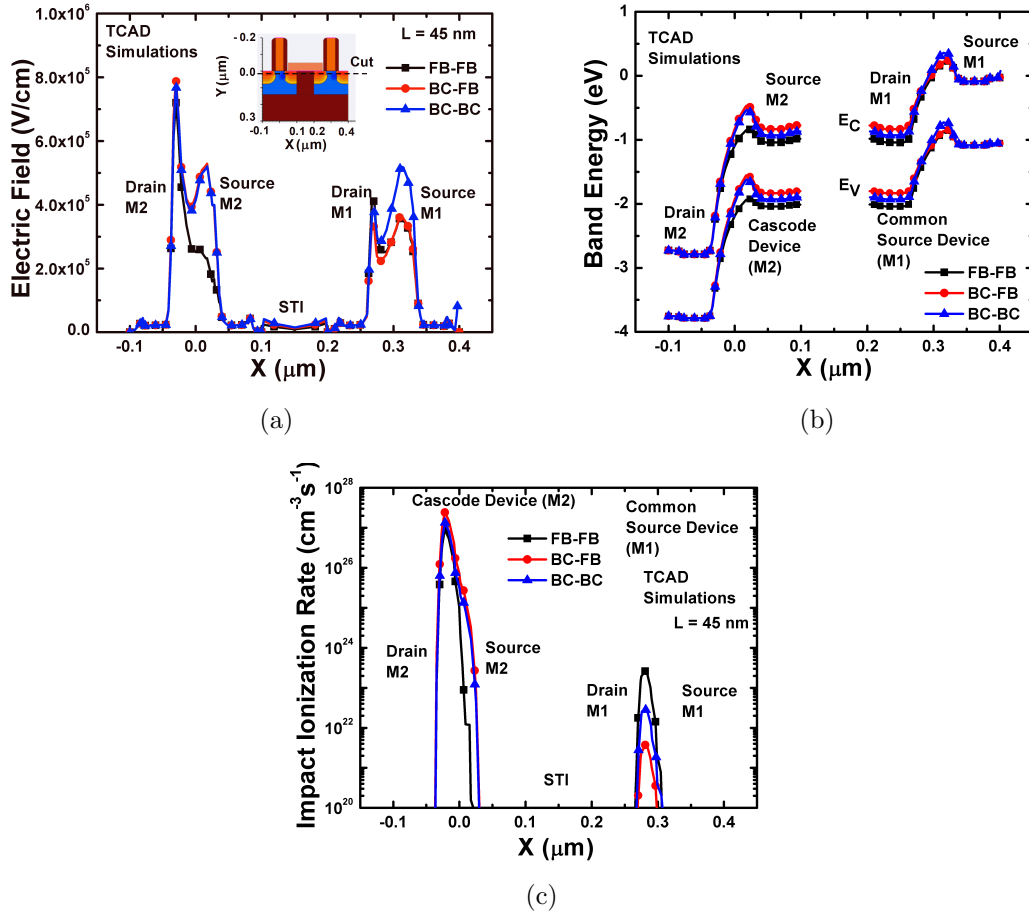


Figure 22: (a) Electric field in the channel region of a FB-FB, BC-FB and BC-BC cascode at constant gate and drain voltage. (b) Conduction band energy in the channel region of a FB-FB, BC-FB, and BC-BC cascode at constant gate and drain voltage. (c) Avalanche generation in the channel region of a FB-FB, BC-FB and BC-BC cascode at constant gate and drain voltage ($V_{D-M2} = 2.7$ V, $V_{G-M2} = 1.5$ V, $V_{G-M1} = 1.0$ V).

The measured maximum DC voltage swing of a stand-alone 45-nm nMOSFET is ~ 1.6 V. Catastrophic breakdown is observed at a voltage swing across the drain larger than this voltage. The voltage swing across a cascode device can be much larger than a stand-alone device. The FB-FB cascode operates upto ~ 3 V V_{DD} . The BC-FB device operates upto ~ 3.2 V V_{DD} , and the BC-BC cascode operates upto ~ 3.3 V V_{DD} . The BC-FB cascode has the largest voltage drop among the three cascodes across the cascode device. For cascode operating above these maximum drain voltages, the cascode device gate-oxide breaks down as shown in Figure 23. Figure 24 shows the TCAD simulated body currents of the cascode and common-source transistors for the BC-BC cascode core, and the body current of the cascode transistor for the BC-FB cascode core. The body current of the BC-FB cascode transistor is much larger than the BC-BC transistors (as expected).

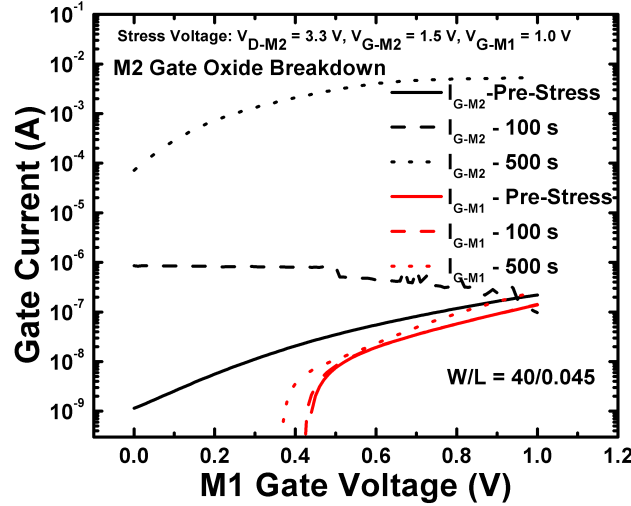


Figure 23: Gate current as a function of the common-source device gate voltage for varying stress conditions of the BC-FB cascode (Stress voltage: $V_{D-M2} = 3.3$ V, $V_{G-M2} = 1.5$ V, $V_{G-M1} = 1.0$ V).

2.5.4 Voltage Drop Across the Cascode and the Common-Source Device in a Cascode Core

SPICE simulations were carried out to calculate the voltage drop across the cascode device and the common-source device in a cascode test structure. Table 1 shows the

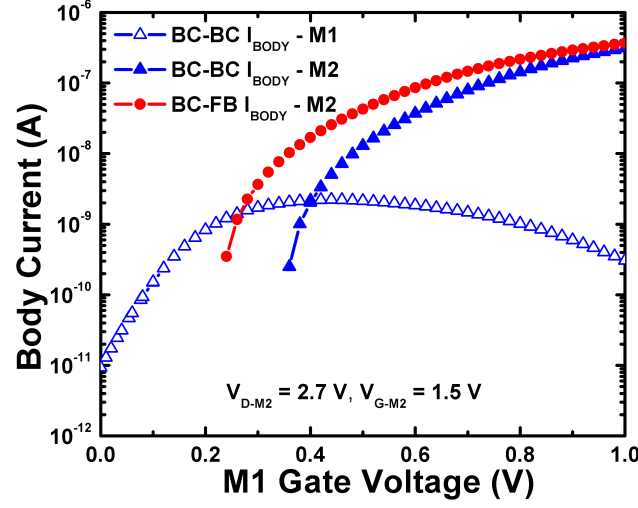


Figure 24: TCAD simulated body current as a function of M1 gate voltage of the BC-BC and BC-FB cascode.

voltage drop across the drain-source and gate-source junctions in the cascode and common-source devices for the three cascodes. BC-FB cascode has the largest voltage drop across the drain-source and gate-source junction of the cascode device among the three cascodes. FB-FB cascode has the smallest voltage drop across the drain-source junction of the cascode device. The same trends are observed looking at the energy band diagrams in Figure 22(b). The voltage drop across the drain-source junction for the cascode device is much larger than the common-source device. At high drain bias voltage, the cascode device gate oxide breaks down first. Similar results are observed from TCAD simulations as well. Also the voltage across the source-body junction of the cascode device in FB-FB cascode is the largest (Table 1). Therefore, the floating body effects are pronounced for the FB-FB cascode.

2.6 Summary

Operating voltage constraints in FB and BC 45-nm SOI nMOSFETs and cascode cores are investigated. Several guidelines are laid down to achieve the best trade-offs between performance and reliability in the devices and cascodes. FB devices demonstrate a

higher performance but a smaller device lifetime than BC devices. Larger impact-ionization induced carrier generation is responsible for a greater degradation for FB devices. The performance across varying gate and drain bias is demonstrated for the devices. It is shown that significant RF performance can be achieved at small gate and drain bias for this technology. The cascodes are studied for performance-reliability trade-offs as well. FB-FB cascodes have a similar device lifetime to BC-FB cascodes. The BC-BC cascodes have the largest device lifetime. The FB-FB cascode provides the best power gain and provides gain up to higher frequencies. The BC-BC and BC-FB cascodes have larger gain compression point.

CHAPTER III

USING BODY-BIAS TO MODULATE PERFORMANCE AND RELIABILITY OF SOI MOSFETS AND CIRCUITS

3.1 Overview

The use of body-contact to modulate the performance and reliability of devices and single-pole-double-throw (SPDT) switches is studied. The nFET threshold voltage and currents changes with body-bias. The nFET reliability is also shown to be dependent on body-bias. The SPDT switch performance is shown to improve with a negative body-bias. However, the switch performance degrades at large negative body bias. The impact of different body-contacting layouts on the radiation tolerance is also investigated.

The contents of this chapter have been published in part at [1].

3.2 Introduction

Floating-body (FB) devices are SOI MOSFETs with body terminal ‘floating’ at some potential and body-contacted (BC) devices have body terminal ‘contacted’ to source (or some other bias). Different device layouts can be used for contacting the body with their associated trade-offs. Figure 25 shows a top-view layout of the (a) floating-body, (b) T-body, (c) notched-T-body, and (d) H-body device. Floating-body devices have the smallest silicon area and smallest parasitics. T-body device has a body-contact on one side. The larger silicon area results in greater parasitics and lower RF performance. To improve the RF performance the silicon area of the body-contact can be notched, resulting in a notched-T-body contact device. The notched-T-body has better RF performance than T-body, however slightly larger TID leakage than T-body. The

H-body device can potentially totally eliminate radiation induced leakage, however the larger silicon area results in a degraded RF performance. Figures 26(a) and 26(b) shows the small-signal equivalent circuits of the BC and the FB devices, respectively. A FB device has a non-zero body to source potential, hence the body effect plays a larger role in its performance. The body effects are modeled using the $g_{mb} \cdot V_{BS}$ and C_{BS} parameters.

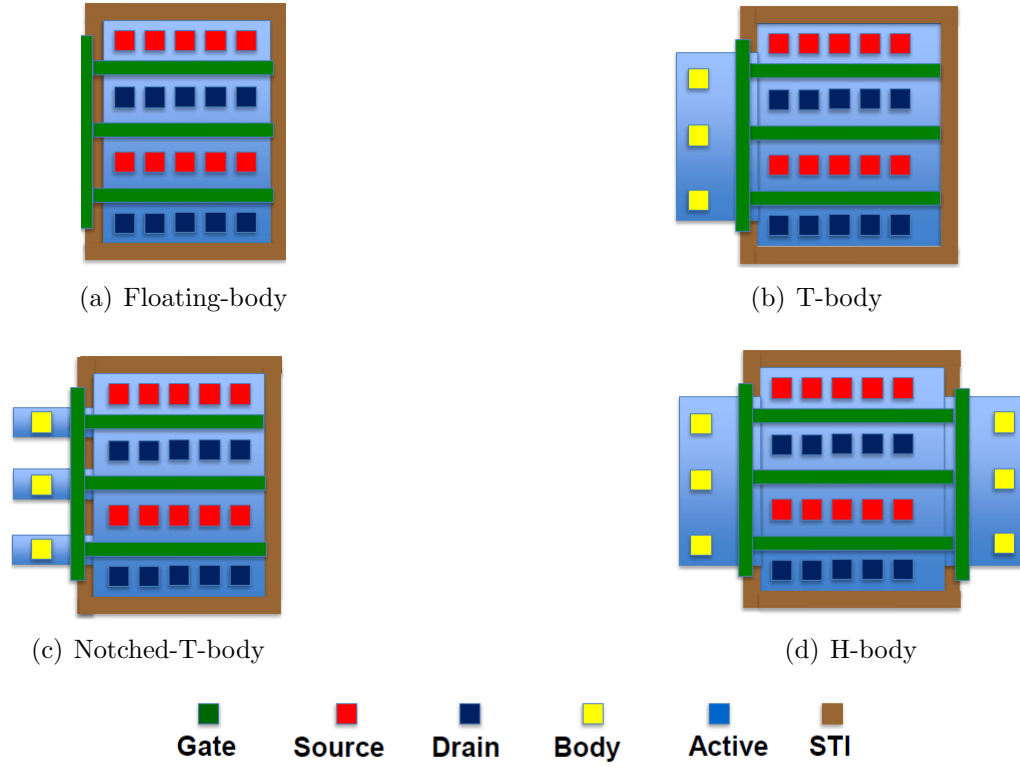


Figure 25: Schematic layout of (a) Floating-body, (b) T-body, (c) Notched-T-body, and (d) H-body device.

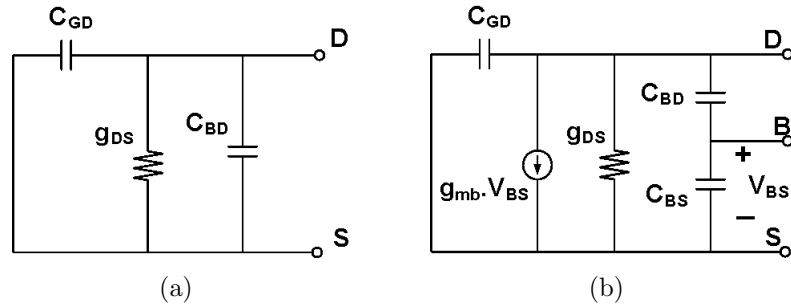


Figure 26: Small-signal equivalent circuit of (a) BC and (b) FB device.

3.3 Impact of Body Bias on the Device Performance and Reliability

Body effect refers to the change in the transistor threshold voltage resulting from a voltage difference between the transistor source and body. Because the voltage difference between the source and body affects the threshold voltage, the body can be thought of as a second gate that helps determine how the transistor turns on and off. Strong body effect enables a variety of effective body biasing techniques, and these techniques were used effectively in older process generations. However, body effect has diminished with transistor scaling, and conventional deep-submicron transistors have very little body effect. For this reason body bias is not widely used for 65-nm and smaller process technologies. Instead, the transistor bodies are generally connected along with the transistor source to either power (V_{DD}) for p-channel or ground (V_{SS}) for n-channel transistor. Although, the body bias becomes important in SOI technologies.

The body bias can be supplied from an external (off-chip) source or an internal (on-chip) source. In the on-chip approach, the design usually includes a charge pump circuit to generate a reverse body bias voltage and/or a voltage divider to generate a forward body bias voltage. Reverse body bias, which involves applying a negative body-to-source voltage to an n-channel transistor, raises the threshold voltage and thereby makes the transistor both slower and less leaky (Figure 27). Forward body bias, on the other hand, lowers the threshold voltage by applying a positive body-to-source voltage to an n-channel transistor and thereby makes the transistor both faster and leakier. The device hot-carrier reliability degrades with reverse body bias and improves with forward body bias [50]. However, kink effects in SOI devices can be removed by grounded body or reverse body bias (Figure 27). Figure 28 shows a qualitative trend of the change in a nMOSFET threshold voltage as a function of body bias. The threshold voltage increases for negative body bias and saturates

at large reverse or forward body bias. The device performance and reliability can be modulated by body bias tuning. Figure 29 shows the variation in a bulk device reliability with substrate bias [50]. The device reliability improves with a positive body bias and degrades with a negative body bias.

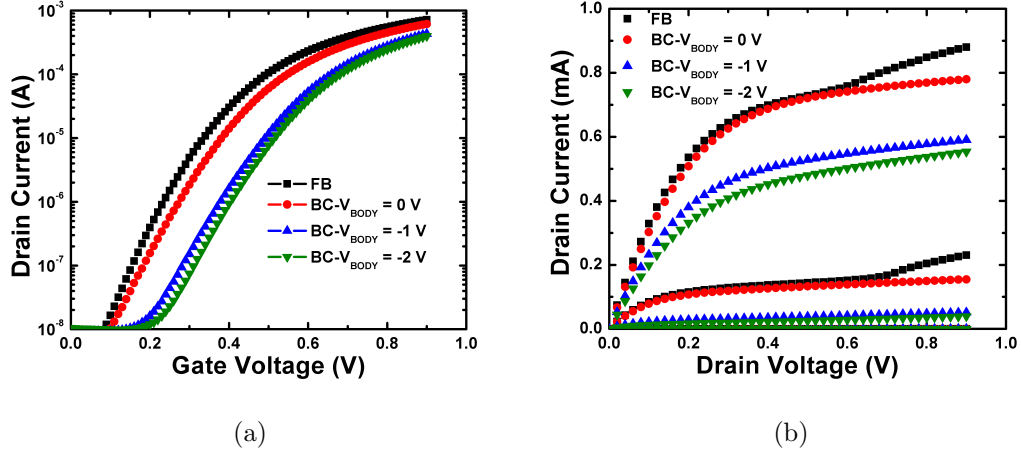


Figure 27: (a) Drain current as a function of gate voltage of FB and BC device for varying body bias. (b) Drain current as a function of drain voltage of FB and BC device for varying body bias (Data on 180-nm CMOS-on-SOI technology (IBM 7RFSOI)).

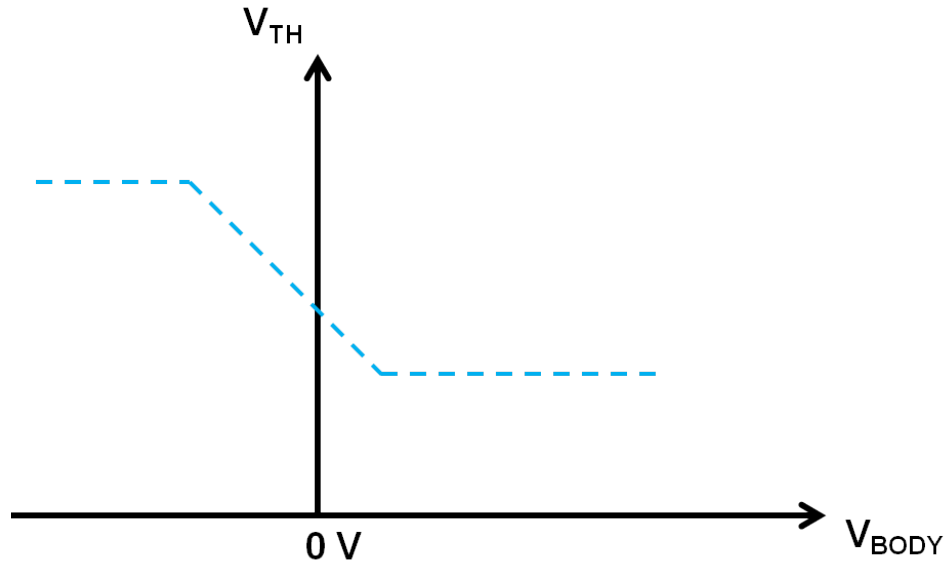


Figure 28: Effect of body bias on a SOI MOSFET threshold voltage.

A BC device has a better control over the body-effects associated with MOSFETs,

because of a fixed body potential. FB devices have better RF performance than BC devices [26] (Figures 12(c), 12(d)). Figure 15(a) shows a comparison of the effects of hot-carrier stress on the FB and the BC devices. We observe threshold voltage shifts (stress condition: $V_{GS} = 1.0$ V, $V_{DS} = 1.5$ V for nFET) with hot-carrier stressing, indicating formation of gate-oxide traps. The BC (both T-body and notched-T-body) devices exhibit smaller threshold voltage shift than the FB devices. This effect is believed to be as a result of the larger avalanche generation induced hot-carriers in FB devices. The body potential for FB devices is at a positive potential as shown by the TCAD simulations (Figure 30).

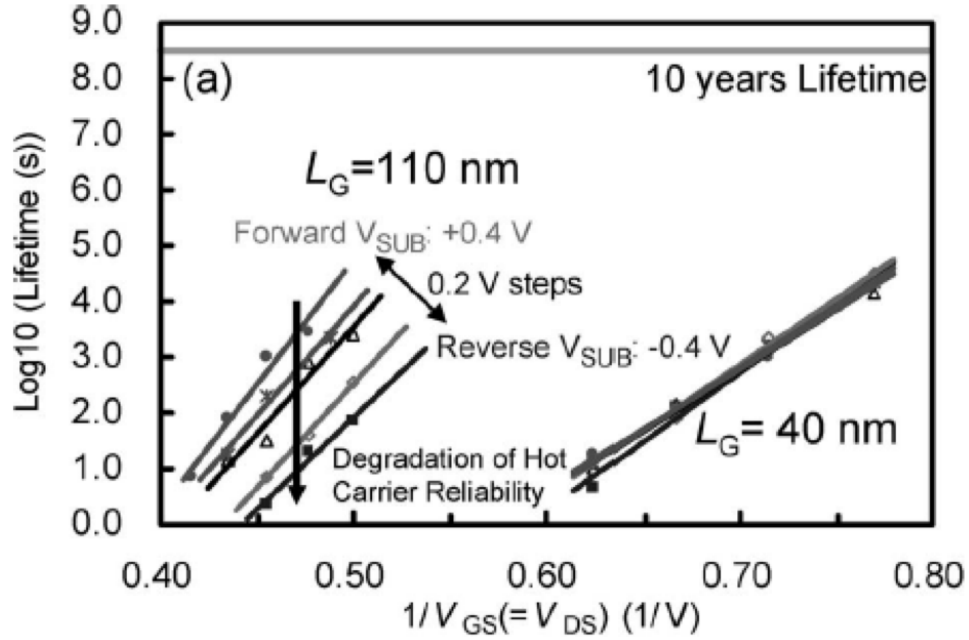


Figure 29: Effect of body bias on a nFET hot-carrier reliability [50].

The effect of electron collection by the body-contact for thin-film SOI BC devices is shown in Figure 31. Figure 31 shows the TCAD model for the total current density for the FB and BC device respectively. Figure 32(a) shows the total current density comparison for FB and BC device at y-axis cut. This demonstrates that the FB devices have a greater current density in the body region than the BC devices.

Figure 32(b) shows the difference in I_{DS} - V_{GS} characteristics of FB and BC device.

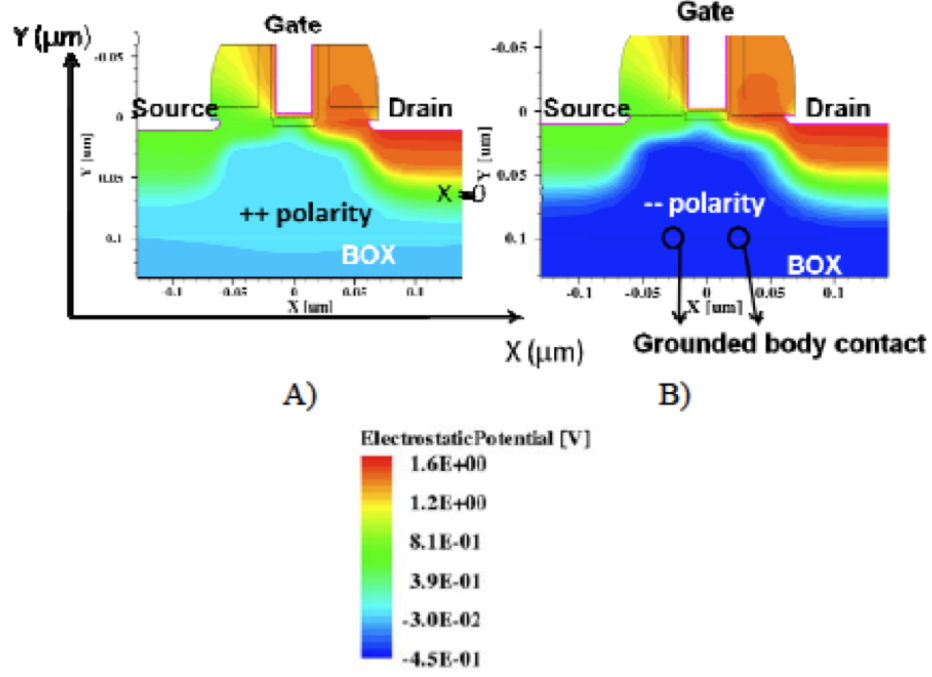


Figure 30: Electrostatic potential of (a) FB and (b) BC device.

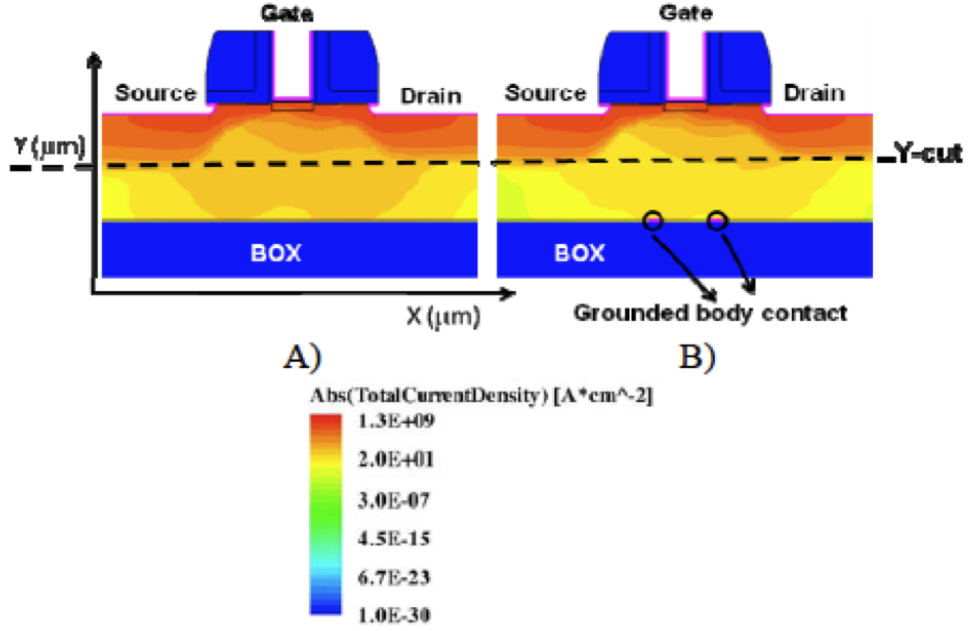


Figure 31: Current density in the body-region of (a) FB and (b) BC device.

FB device has a greater current than the BC device, and the body-contact for the BC device also collects some current. The body-current magnitude increases as the body thickness decreases. The difference in currents between the FB device and the BC

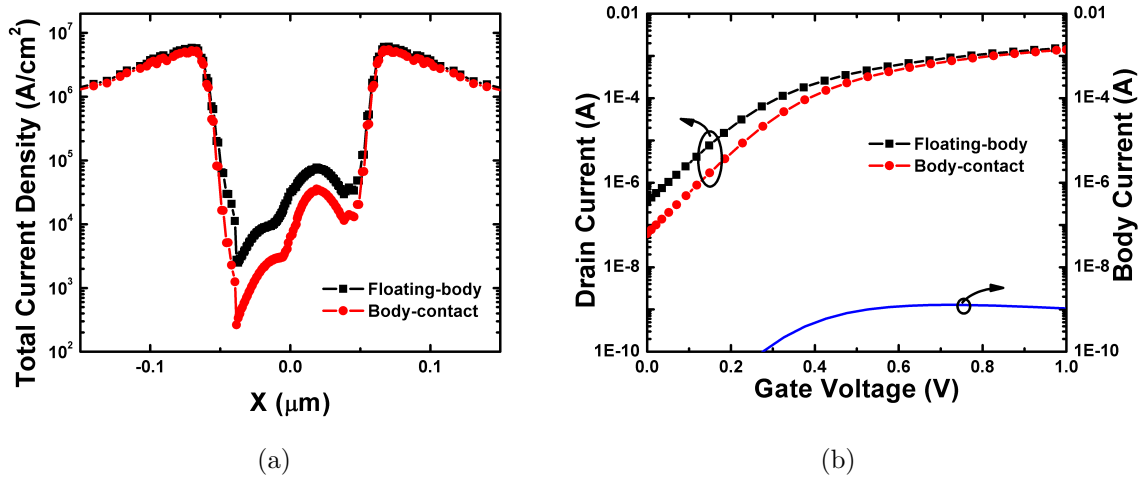


Figure 32: (a) Comparison of current density of FB and BC device in the body region. (b) Simulated $I_{DS} - V_{GS}$ characteristics of FB and BC device.

device is because of greater avalanche generation currents for the FB device. Thus the BC devices have improved hot-carrier reliability response as a result of the charge collection by the body-contact and lower generation currents. Also the electric fields in the FB devices are lower than the BC devices (Figure 16(a)).

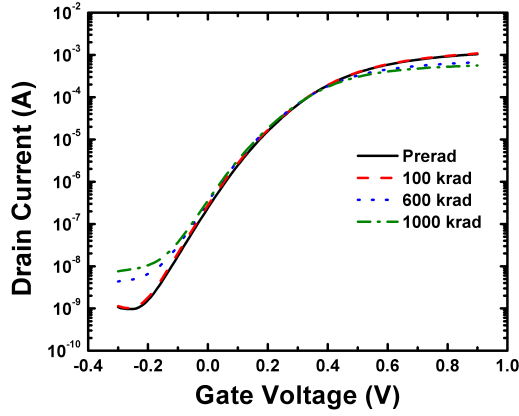
3.4 Using Body-Contact to Mitigate Ionizing Radiation Damage

Total-ionizing dose irradiation experiments were performed on FB and BC devices. The 10 keV x-ray irradiation facility at Vanderbilt University is shown in Figure 33. Because of the sensitivity of the short-channel CMOS devices to gate-oxide breakdown, the devices were probed during experimentation. The FB devices show significant increase in off-state leakage as compared to BC devices (Figures 34(a), 34(b)). The difference in total-dose radiation tolerance of the FB and BC device can be easily understood by looking at the top-schematic view of the device layout (Figure 25). The FB devices can have leakage current between source-drain on both sides of the gate finger. Whereas a T-body contact device can have a leakage path only on one side of the gate finger. Therefore, the FB devices show a much larger increase in

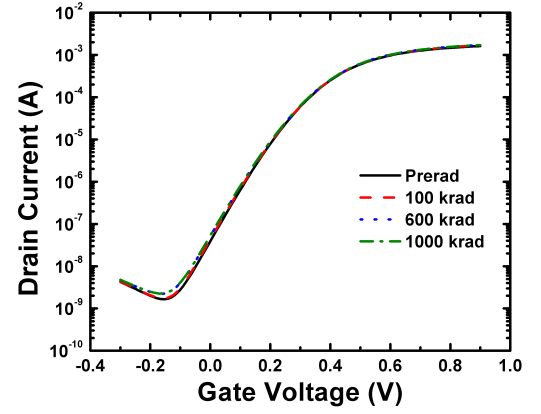
off-state leakage current compared to BC devices. 3D TCAD simulations were carried out to verify the explanation for the mechanisms. Figure 35 shows the simulated electron current density contours for the FB, T-body, and H-body devices. An equal concentration ($1 \times 10^{12} \text{ cm}^{-2}$) of traps were deposited at the active-STI edge to model radiation induced damage. The FB device shows an increased leakage current at the active-STI edge. T-body device shows minimal increase in leakage, and H-body device shows no increase in leakage current. The transfer characteristics for varying trap concentration at the active-STI edge is shown in Figure 36.



Figure 33: ARACOR X-ray radiation source.

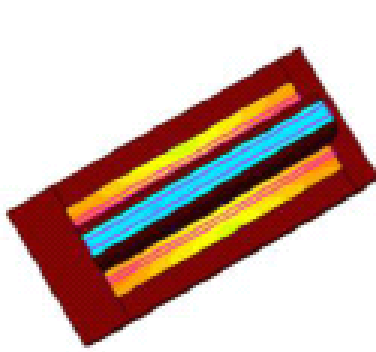


(a)

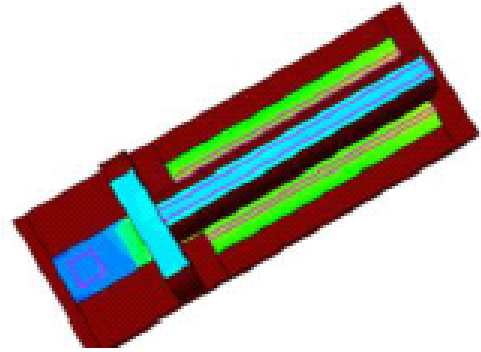


(b)

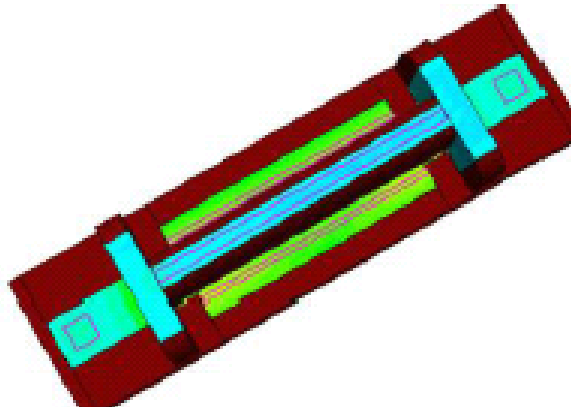
Figure 34: (a) Drain current as a function of gate voltage of FB device for varying ionizing dose. (b) Drain current as a function of gate voltage of BC device for varying ionizing dose.



(a)

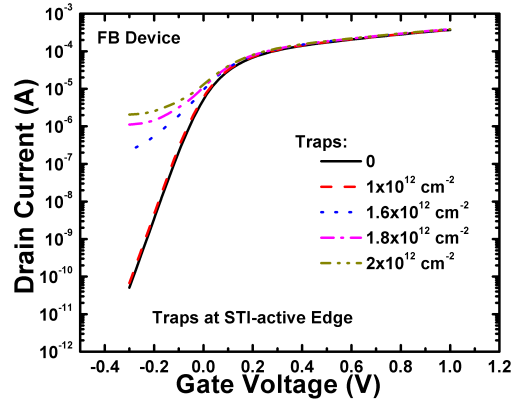


(b)

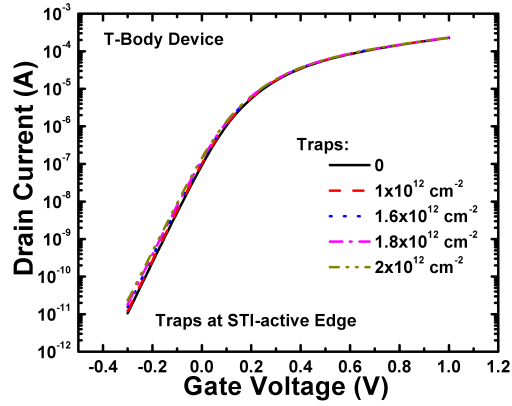


(c)

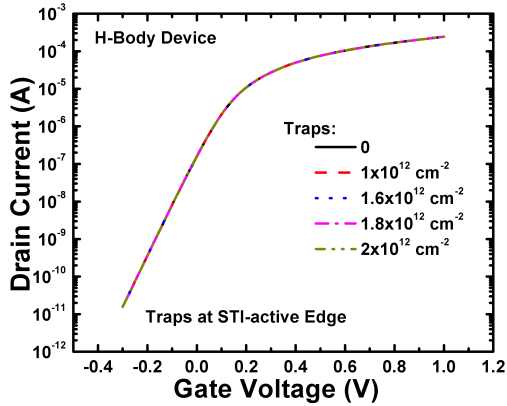
Figure 35: 3D TCAD simulated electron current density for (a) FB device, (b) T-body device, and (c) H-body device.



(a)



(b)



(c)

Figure 36: TCAD simulated drain current as a function of gate voltage of (a) FB device, (b) T-body device, and (c) H-body device for varying trap concentrations at the active-STI edge.

3.5 *Impact of Body Bias on the Performance and Reliability of Single-Pole-Double-Throw (SPDT) Switches*

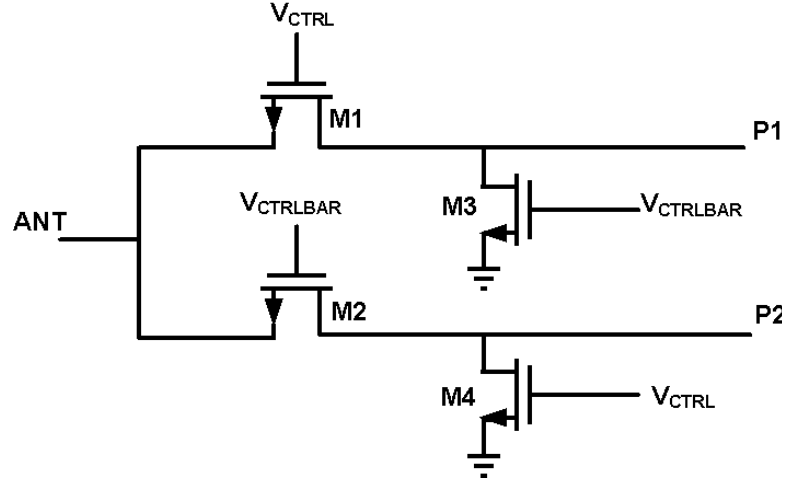


Figure 37: Schematic of a SPDT switch.

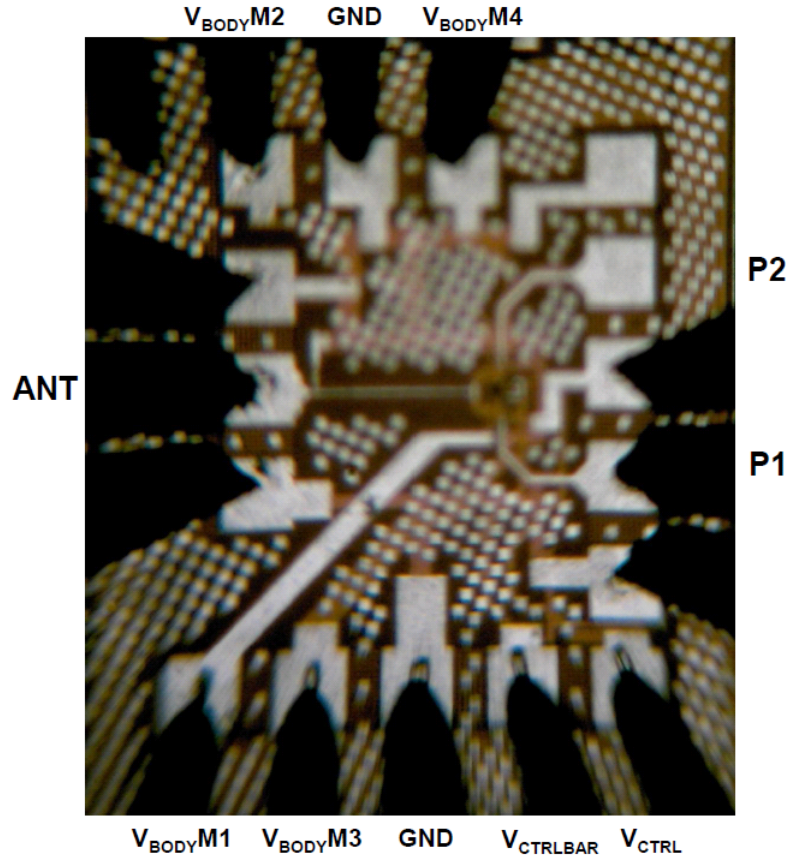


Figure 38: Die photograph of the SPDT switch.

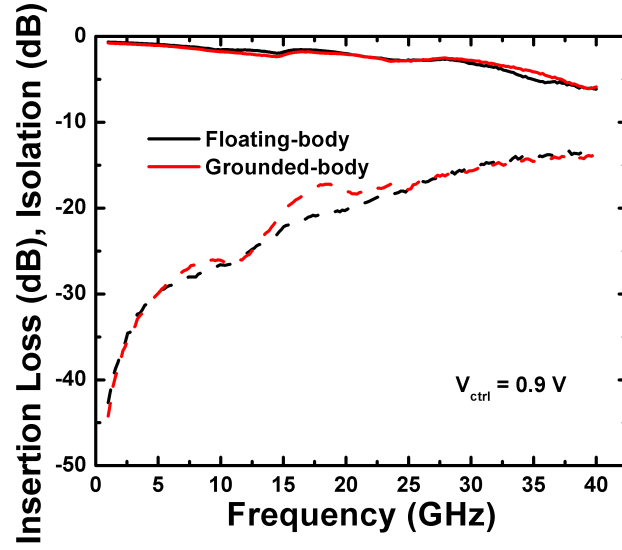


Figure 39: Insertion loss and isolation as a function of frequency of a FB and BC switch with grounded body.

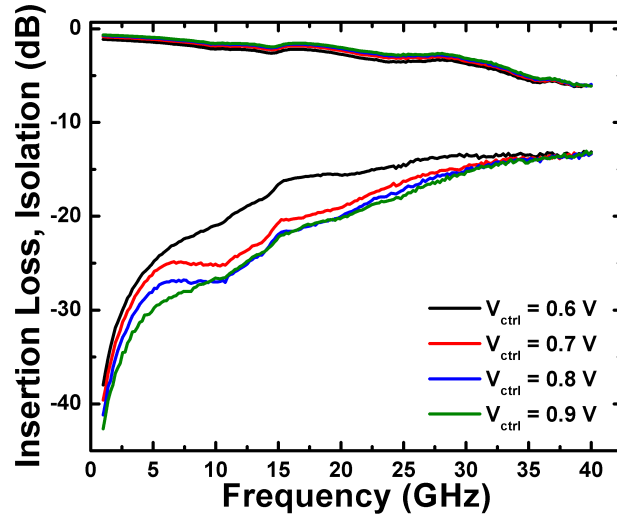
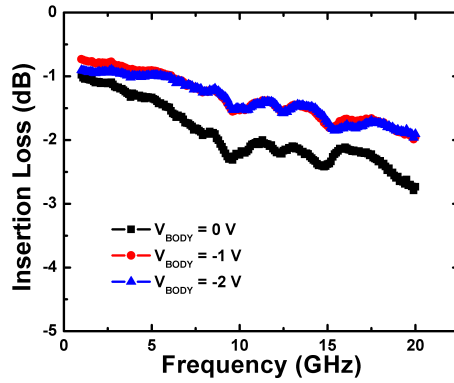


Figure 40: Effect of gate bias on switch performance.

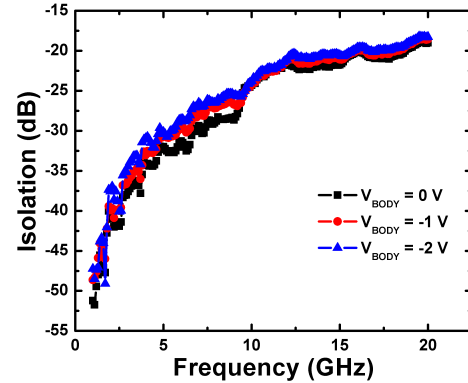
SPDT switches are used in RF transceivers to switch the signal path from the antenna to the transmitter or the receiver. A switch should provide the smallest loss between the antenna and transmitter/receiver when its on, and should have the largest possible isolation when off. Also, it should be able to handle a large amount of input power. A schematic diagram of the series-shunt SPDT switch designed is

shown in Figure 37. The circuit switches between antenna (ANT) and transmit (P1) or receive (P2) side depending on the control voltage (V_{CTRL} and $V_{CTRLBAR}$). nFET on-state resistance (R_{ON}) and off-state capacitance are two important figure of merits in determining its use as a switching device. Switches in CMOS-on-SOI technologies have been designed before making use of the high resistivity substrates [51]. Floating-body switches have been shown to have improved performance compared to body-tied switches. The improved performance of floating-body switches can be attributed to smaller sized floating-body transistors, and hence lower parasitics. The switches shown here were designed in a 180-nm CMOS-on-SOI process (IBM 7RFSOI). The die photograph of the switch is shown in Figure 38. The M1 and M3 width is $150\ \mu m$ ($W_f = 3\ \mu m$, $N_f = 50$), and M2/M4 width is $60\ \mu m$ ($W_f = 3\ \mu m$, $N_f = 20$). The transistor width was chosen to achieve the best trade-off between insertion loss and isolation. Figure 39 shows a comparison of the insertion loss (IL) and isolation of the floating-body and body-contact switch with grounded body. Very small difference is observed between the performance of the FB and BC switches in this technology. The small difference observed highlights the fact that the previously reported improved performance of FB switches is because of the smaller parasitics of a FB nFET as compared to a BC nFET, and the FB effects do not alter the switch performance. Figure 40 shows the effect of gate bias on the switch performance. The IL of the switch is similar above $V_{CTRL} = 0.9\text{ V}$ (upto 1.8 V). Therefore, a smaller V_{CTRL} can be used for longer switch lifetime (less device degradation). Insertion loss of the switch improves with negative body bias (Figure 41). Linearity of the switch also improves with negative body bias (Figure 42). The power measurements were made at 10 GHz for X-band applications.

Figure 43 shows the effect of body bias on series and shunt MOSFETs on the insertion loss of the switch. Only reverse body biasing the series MOSFET results in some improvement in IL. The improvement saturates at $V_{BODYM1} = -2.0\text{ V}$. Reverse

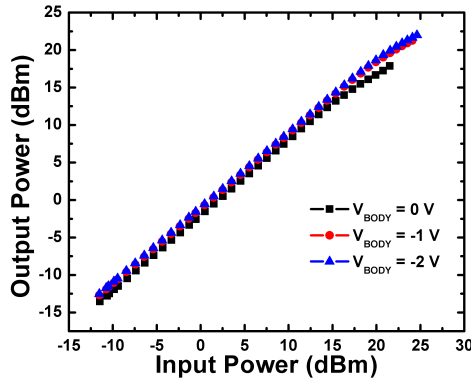


(a)

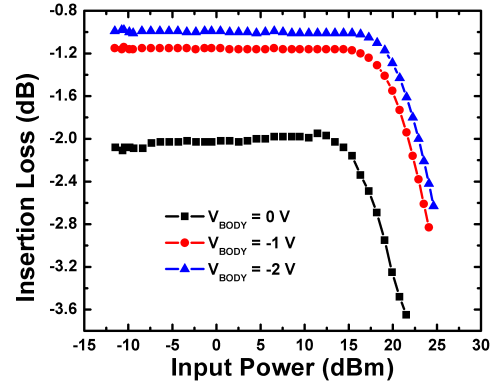


(b)

Figure 41: (a) Effect of negative body bias on IL. (b) Effect of negative body bias on isolation.



(a)



(b)

Figure 42: (a) Output power as a function of input power of the switch for varying body bias. (b) Insertion loss as a function of input power of the switch for varying body bias.

biasing both the series and shunt MOSFET results in further improvement in switch IL. Source/Drain to body capacitance decreases with negative body bias. Smaller capacitance can be used to explain better response. With reverse body bias, the depletion region at the source and drain becomes wider and hence the junction capacitance decreases (Figures 44, 45). Also proton irradiation experiments were carried out to determine the hardness of switches for extreme radiation applications. Figure 46 shows the effect of proton radiation on the IL and isolation of the switch. Very small

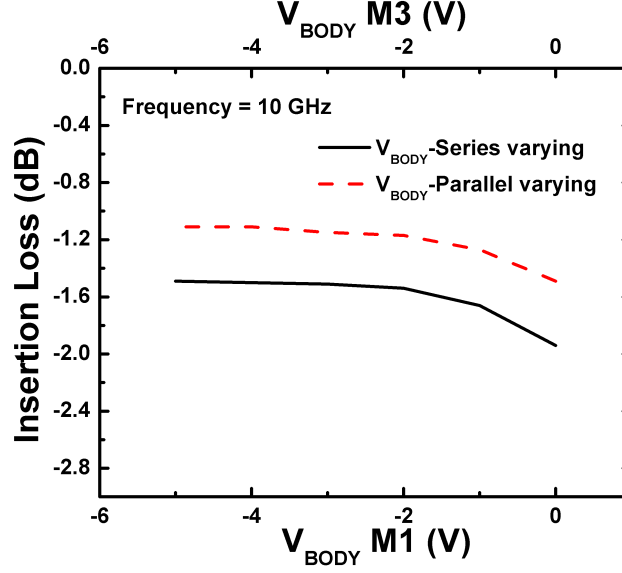


Figure 43: Effect of body bias of series and shunt nFETs on switch performance.

change in the switch performance is observed upto 3 Mrad (SiO_2) proton radiation. The switches were radiated with passive exposure. A small increase in insertion loss observed with radiation can be attributed to increased hole trap concentration at the buried oxide to silicon interface. This increased trap concentration at the interface can deplete silicon of holes at the interface and can lead to increased depletion region width. This physical effect is similar to the above described improvement in insertion loss with reverse body bias. The increased depletion region width results in smaller parasitic source/drain to body depletion capacitances.

Also the switches were tested for gate oxide reliability. The switches were stressed at constant DC bias for varying time ($V_{CTRL} = 1.8$ V, $V_{BODY} = -3.0$ V). Figure 47 shows the effect of stress on insertion loss and input return loss of the switch. Clearly the switch characteristics change significantly at this extreme stress condition. The change in switch characteristics can be attributed to a soft-breakdown of the gate oxide. Soft-breakdown of a gate oxide is characterized by gate current increase from a few picoamperes to hundreds of nanoamperes. If the stress is applied further it can lead to hard-breakdown of the gate oxide characterized by microamperes to

milliamperes of gate current. The switch is rendered useless in a hard-breakdown condition.

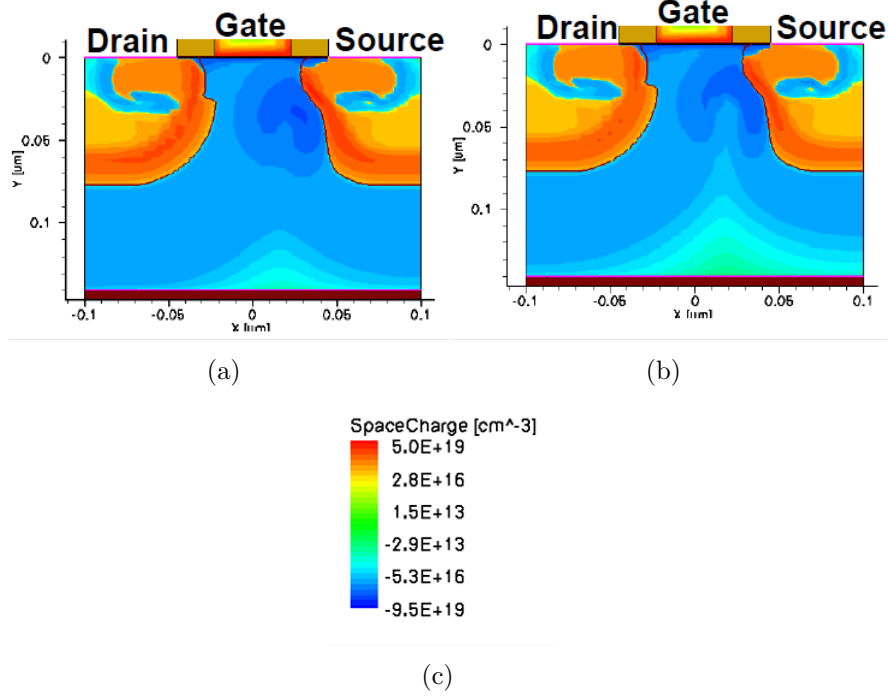


Figure 44: (a) Space charge contour diagram of a nFET for $V_G = 1.0$ V, $V_D = 1.0$ V, $V_S = 0.0$ V, and $V_{BODY} = -1.0$ V. (b) Space charge contour diagram for a nFET of $V_G = 1.0$ V, $V_D = 1.0$ V, $V_S = 0.0$ V, and $V_{BODY} = 0.0$ V.

To understand the impact of body bias on the device reliability, we performed TCAD simulations. Figure 48(a) shows the electric field in the channel region for varying body bias. Figure 48(b) shows the impact of body bias on the impact ionization in the channel region. Significant variation in electric field and impact ionization in channel region is observed with variation in body bias. The electric field in the gate oxide is however not very sensitive to variation in body bias (Figure 48(c)). Hence degradation in device characteristics with negative body bias can be attributed to larger electric field and impact ionization generated hot-carriers in the body region.

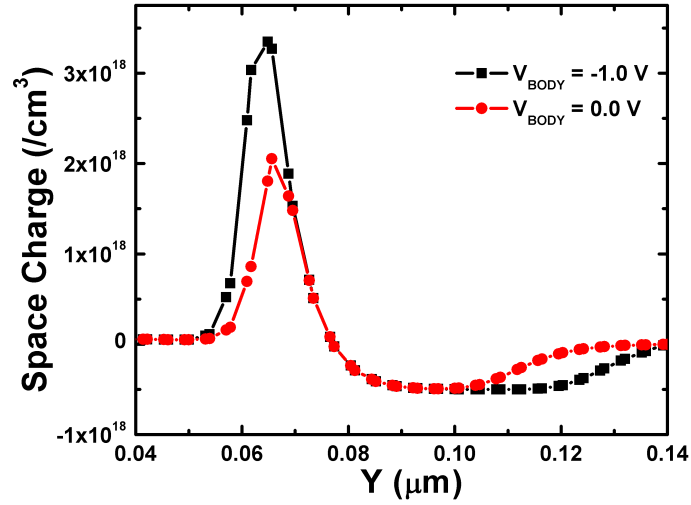


Figure 45: Space charge at the source-body junction of the nFETs for negative and zero body bias.

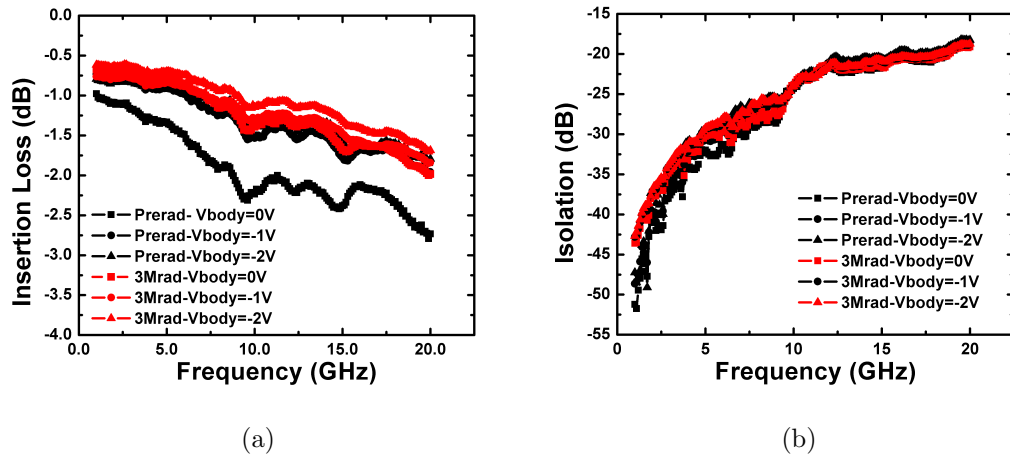
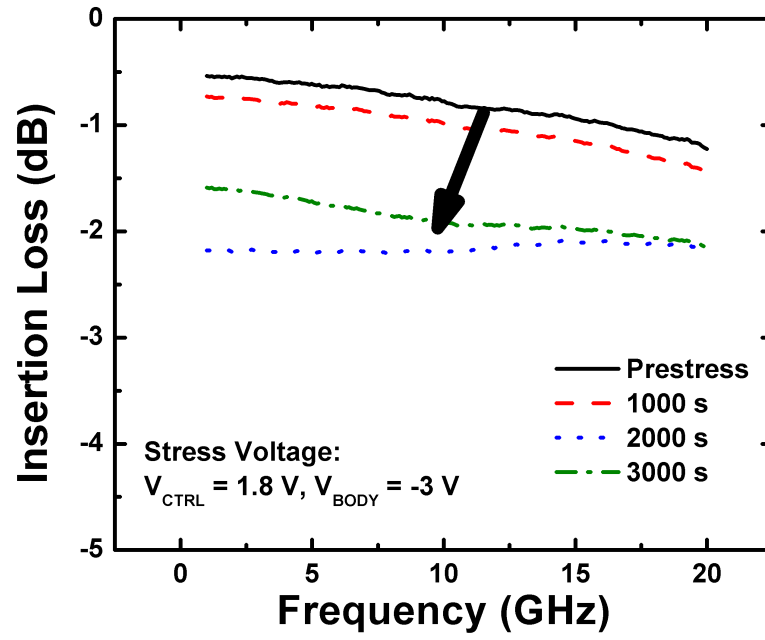
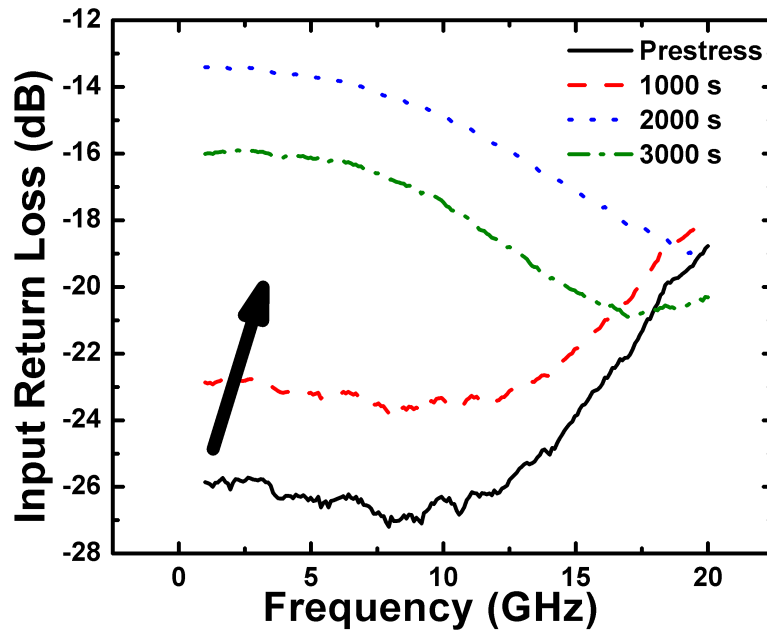


Figure 46: (a) Effect of proton irradiation on insertion loss. (b) Effect of proton irradiation on isolation.

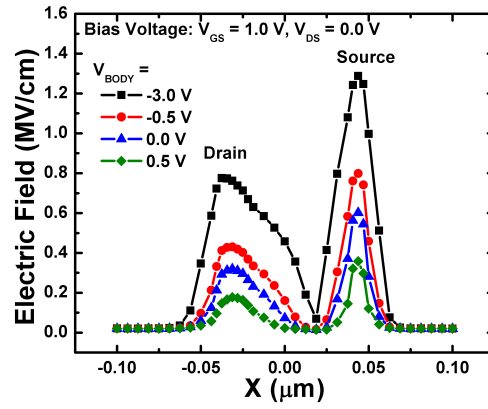


(a)

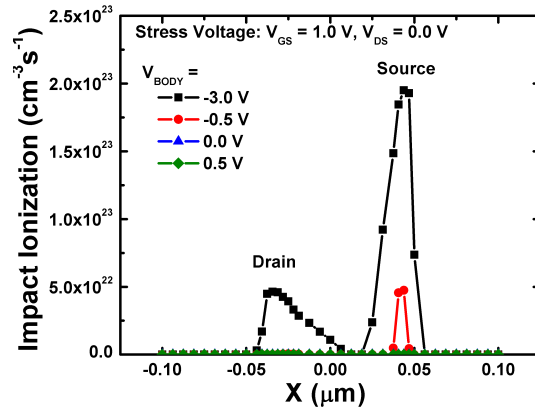


(b)

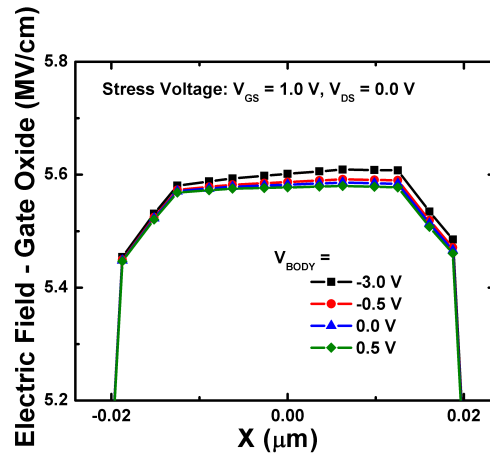
Figure 47: (a) Effect of gate and body stress on insertion loss. (b) Effect of gate and body stress on input return loss (S11).



(a)



(b)



(c)

Figure 48: (a) Electric field in the channel region for varying body bias. (b) Impact ionization in the body region for varying body bias. (c) Electric field in the gate oxide region for varying body bias.

3.6 Summary

The use of body contact to modulate the performance and reliability of MOSFETs is shown in this chapter. The device threshold voltage, on/off-state current, etc. change with body bias. The nFET reliability degrades at negative body bias. The impact of body bias on a SPDT switch is shown, and the switch performance is shown to improve at negative body bias. However, the switch reliability degrades at negative body bias, thus demonstrating a trade-off between performance and reliability. Different body-contact device layouts are compared for their total-dose radiation tolerance.

CHAPTER IV

IMPACT OF DEVICE WIDTH ON PERFORMANCE AND RELIABILITY

4.1 Overview

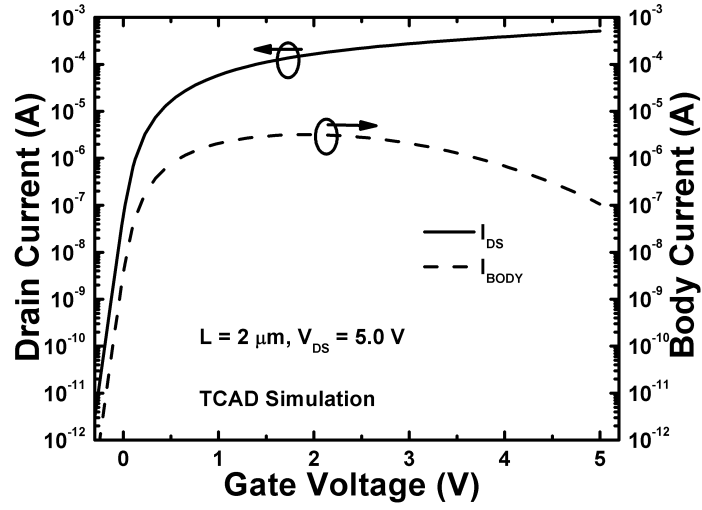
The impact of device width on the RF performance and reliability is studied. Larger width devices are shown to have greater degradation, posing challenging questions for RF design in strained-Si technologies.

The contents of this chapter have been published in part at [3].

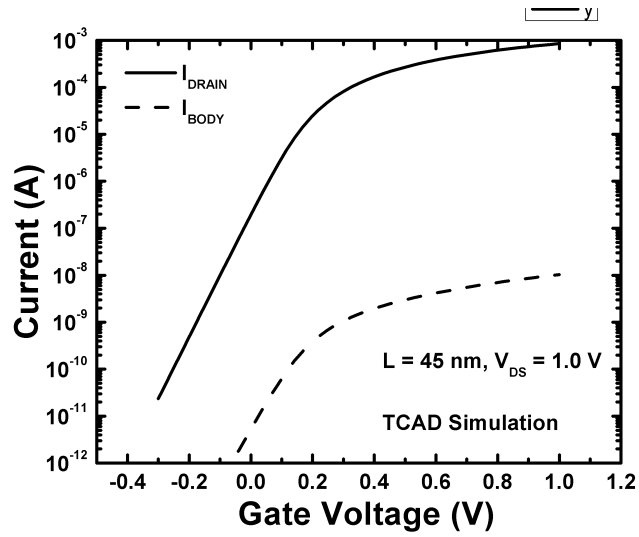
4.2 Introduction

We investigate the effects of device width in strained-Si 45-nm nFETs on both their hot-carrier and total-dose tolerance. It has been shown previously that narrow finger width devices are more prone to hot-carrier and total-dose irradiation damage, as compared to larger finger width devices [52]-[54]. Narrow finger devices have larger compressive stress in the channel region as a result of the proximity of STI. The compressive stress in the STI is created as the device cools down following the trench fill process. The different coefficients of thermal expansion of silicon and oxide cause a compressive lateral stress from the oxide in the silicon. The enhanced irradiation sensitivity for narrow width devices may be related to the influence of stress in STI oxide on the amount of positive trapped charge. This has been shown for longer channel length (above 100-nm) MOSFETs that do not have tensile nitride capping layer induced intentional strain in the channel region. It has been shown before that strain in the channel can result in greater hot-carrier degradation [55]. Here, we show that larger width strained-Si devices (in a 45-nm CMOS platform) show

enhanced damage compared to narrow width devices (both for nFETs and for pFETs). RF circuits, such as low-noise-amplifiers and power-amplifiers require large width devices to ensure adequate performance ($\sim 100 \mu m$). For such circuits requiring large device widths, the results of this study are quite important. The trade-offs between RF performance and reliability of these varying finger width 45-nm RF-nFETs are investigated. For the hot-carrier reliability experiment, the gate bias was chosen for worst-case degradation. In long-channel length CMOS technologies the worst-case gate bias is close to $V_{DD}/2$ (Figure 49(a)). However, for short-channel technologies the maximum damage (and body current) occurs at $V_{GS} = V_{DD}$ (Figure 49(b)). The above result can be explained by looking at the impact ionization in the channel region for the long- and short- channel technologies (Figure 50). The impact ionization increases with increasing gate voltage for short-channel length nFET. However, for a long-channel length nFET the maximum impact ionization occurs at a gate voltage less than V_{DD} . Impact ionization causes electron-hole pair generation in the channel region. The holes are collected at the body terminal.

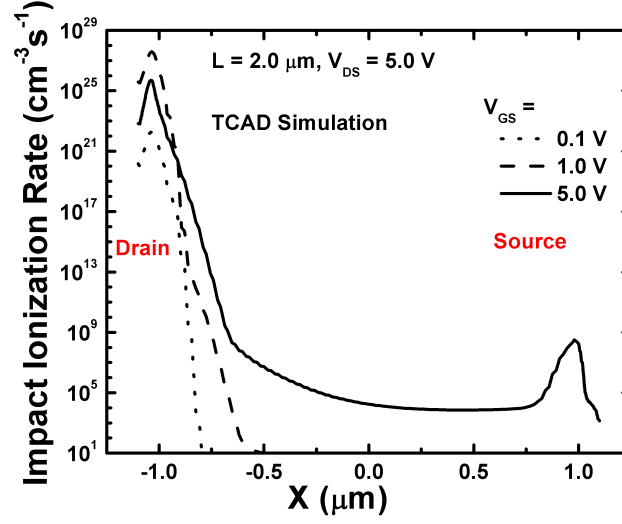


(a)

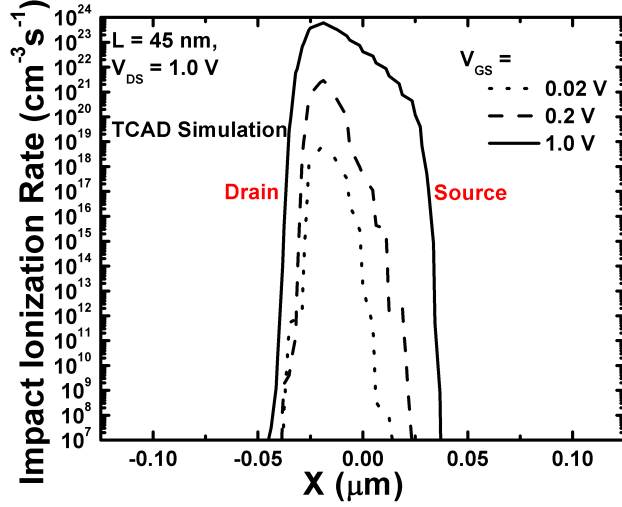


(b)

Figure 49: (a) TCAD simulated drain current and body current as a function of gate voltage for a 2 μm channel length nFET. (b) TCAD simulated drain current and body current as a function of gate voltage for a 45-nm channel length nFET.



(a)



(b)

Figure 50: (a) TCAD simulated impact ionization in the channel region for a $2 \mu\text{m}$ channel length nFET. (b) TCAD simulated impact ionization in the channel region for a 45-nm channel length nFET.

4.3 Effect of Finger Width on Device RF Performance

The details of the devices used for this study are described in Table 2. Devices with a small finger width ($W_f = 0.4 \mu m$) have significantly higher maximum oscillation frequency (f_{MAX}) when compared with the device with a larger finger width ($W_f = 2 \mu m$) (Figure 51). This can be attributed to the smaller gate resistance and parasitic capacitances for the device with smaller finger width. In addition, a small finger width device ($W_f = 0.4 \mu m$) has a higher cut-off frequency (f_T) when compared with the device with a larger finger width ($W_f = 2 \mu m$). However, the power-gain provided by narrower width devices is much smaller (for the same number of fingers). The power characteristics of the devices are shown in Figure 52. Figure 52(a) shows the power-gain as a function of input power (frequency = 9 GHz). In addition, the two-tone intermodulation distortion of the narrow width devices is much worse, as shown by the output third-order intercept point as a function of gate voltage for the devices with different widths (Figure 52(b)). Therefore, large width devices are typically optimal for RF amplifiers in this technology.

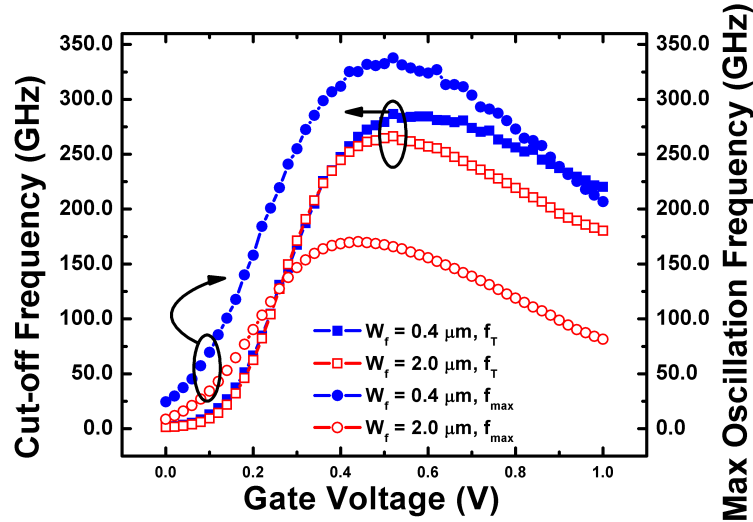


Figure 51: Maximum oscillation frequency (f_{MAX}) and cut-off frequency (f_T) as a function of gate voltage of the devices with varying finger width.

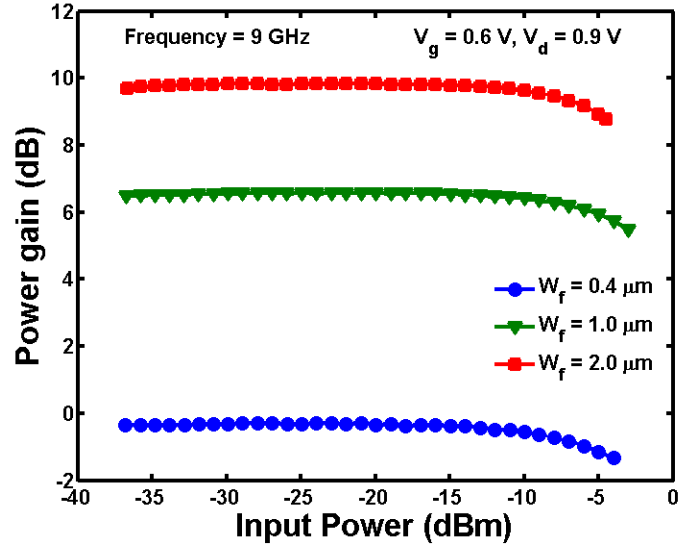
Table 2: Devices used to study the impact of width on performance and reliability

Device Parameter	$W_f = 0.4 \mu m$	$W_f = 0.6 \mu m$	$W_f = 1.0 \mu m$	$W_f = 2.0 \mu m$
W/L (μm)/(μm)	0.4/0.045	0.6/0.045	1.0/0.045	2.0/0.045
Number of Fingers	20	20	20	20
Gate-finger to gate-finger spacing (μm)	0.150	0.150	0.150	0.150
CA-Gate spacing (μm)	0.045	0.045	0.045	0.045
Source/Drain contact spacing (μm)	0.084	0.084	0.084	0.084

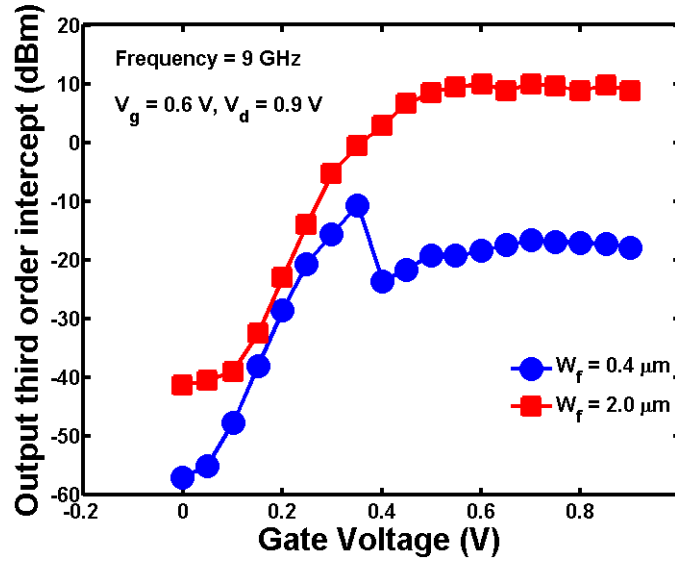
4.4 *Effect of Finger Width on Device Reliability*

Figure 53(a) shows the shift in threshold voltage as a function of hot-carrier stress time for nFETs with varying finger width. Positive threshold voltage shifts as a result of electron traps are observed, as expected. Increasing finger width results in enhanced threshold voltage shifts (and mobility degradation). Figure 53(b) shows a comparison of the off-state leakage current for devices with varying finger width as a function of irradiation dose. The off-state current increases as a result of hole traps in the STI. An increase in off-state leakage current with finger width is observed. In previous studies, it has been reported that larger longitudinal compressive stress (along the width) in the narrow width device channel region (as a result of STI) results in greater degradation [52]-[54]. However, in the strained-Si devices enhanced mechanical stress caused by the over-layers on the gate electrode plays a greater role in determining the hot-carrier reliability [55].

Larger finger width nFETs show enhanced degradation because of higher impact ionization caused by a larger strain than narrow finger width devices [3]. pFETs also show a greater hot-carrier threshold voltage shift for wider devices, although the differences are smaller than for the nFETs. For pFETs, the SiGe source/drain has more impact ionization near the drain region. In addition, mechanical strain deteriorates the gate-oxide and/or generates significant numbers of interface traps



(a)



(b)

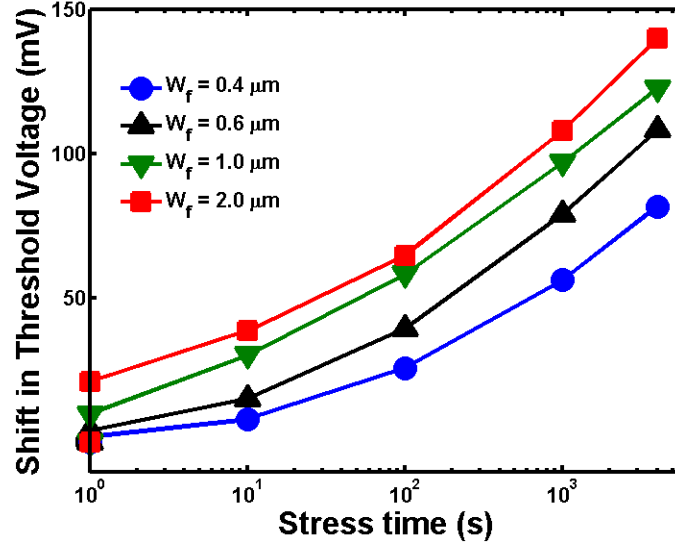
Figure 52: (a) Power-gain as a function of input RF power (frequency = 9 GHz) of the devices with varying finger width. (b) Output-third-order-intercept point (OIP3) as a function of gate voltage of the devices with varying finger width.

[56]. Therefore, more degradation is observed for wider pFETs as compared to narrow pFETs. This theory is further confirmed by examining the stress distribution along the three dimensions for a strained-Si device as a function of device width [57]. For pFETs, with increasing device width the transverse tensile stress (perpendicular to channel

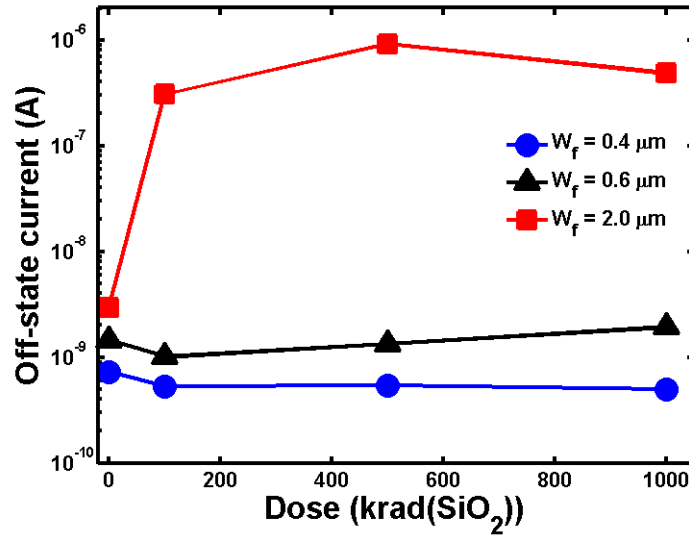
direction) increases (until the device width = $2\ \mu\text{m}$), and then finally saturates. To eliminate this problem, small single finger width devices (and larger total number of fingers) should be used in RF designs. Layout modifications, such as gate-finger pitch optimization and source/drain contact spacing optimization can also help satisfy the required performance-reliability trade-offs [1], [4].

3D TCAD time dependent degradation simulations were carried out to study the effects of varying device width of strained-Si CMOS technology on their hot-carrier reliability. A time-dependent power-law hot-carrier degradation model was used to simulate the degradation [58]. Figure 54 shows the interface trap density (at the gate-oxide to silicon interface) as a function of hot-carrier stress time for devices with different widths. Larger increase in interface trap density is observed for larger width device. The simulated devices had a tensile strain capping layer on the gate poly. The capping layer creates a tensile strain along the channel direction (Figure 55). Figure 55(a) and 55(b) show the tensile stress induced electron mobility enhancement factors for simulated device of width $0.1\ \mu\text{m}$ and $0.7\ \mu\text{m}$, respectively. Clearly, the tensile strain in the channel region increases with increasing device width. This can be attributed to the larger volume of tensile capping layer present in the larger width device. Larger strain in the channel region results in more impact ionization and hence more hot-carriers. For unstrained MOSFETs, a larger trap formation occurs at the STI-active edge. However, in a strained-silicon MOSFET the trap formation occurs throughout the channel (Figure 56).

Therefore, wider devices show enhanced degradation compared to narrow width devices. Large device width is required to achieve sufficient gain and linearity from the device, hence posing problems for RF circuit design. Strain in the channel region is responsible for enhanced degradation of nFETs.



(a)



(b)

Figure 53: (a) Shift in threshold voltage as a function of stress time of the nFETs with varying finger width. (b) Total-dose irradiation induced increase in off-state current of the nFETs with varying finger width.

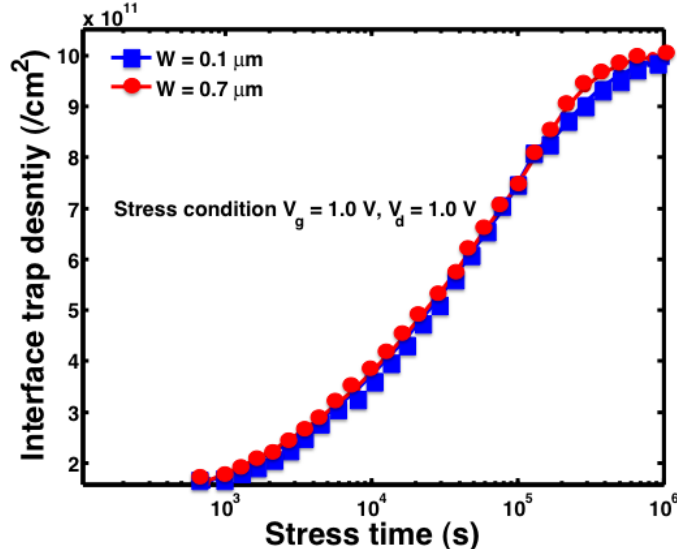
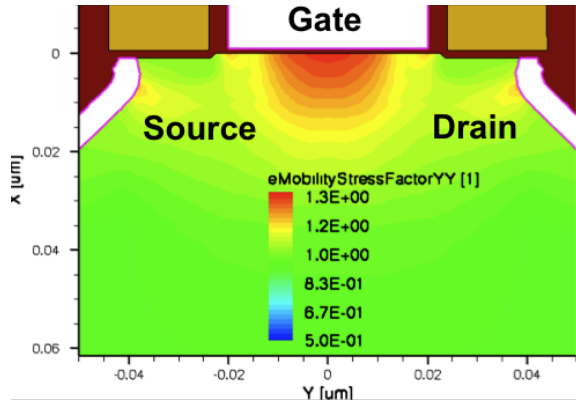
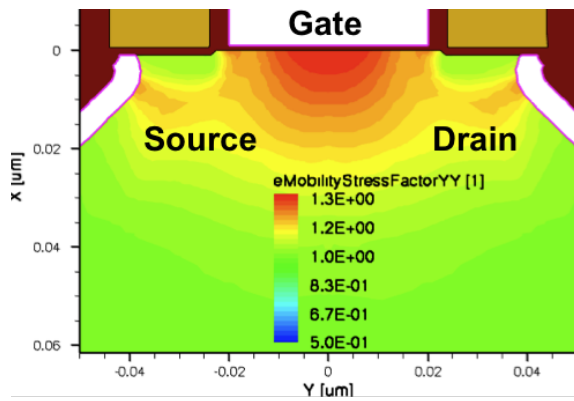


Figure 54: TCAD simulated interface trap density as a function of stress time for device of width $0.1 \mu m$ and $0.7 \mu m$.



(a) Width = $0.1 \mu m$



(b) Width = $0.7 \mu m$

Figure 55: TCAD simulated electron mobility enhancement factor along the channel direction for device of width (a) $0.1 \mu m$ and (b) $0.7 \mu m$

4.5 Model for Hot-Carrier Degradation in CMOS Technologies

Hot-carrier stress induced threshold voltage shift and transconductance decrease in MOSFETs follows a stress time dependent exponent model with a constant slope [59]:

$$\Delta V_t = At^n, \quad (3)$$

$$\frac{\Delta g_m}{g_m} = Kt^n, \quad (4)$$

For MOSFET's the slope n is approximately 0.2. This model can be used to extract the CMOS device lifetime by fitting the curve to data and finding the time for a given threshold voltage shift.

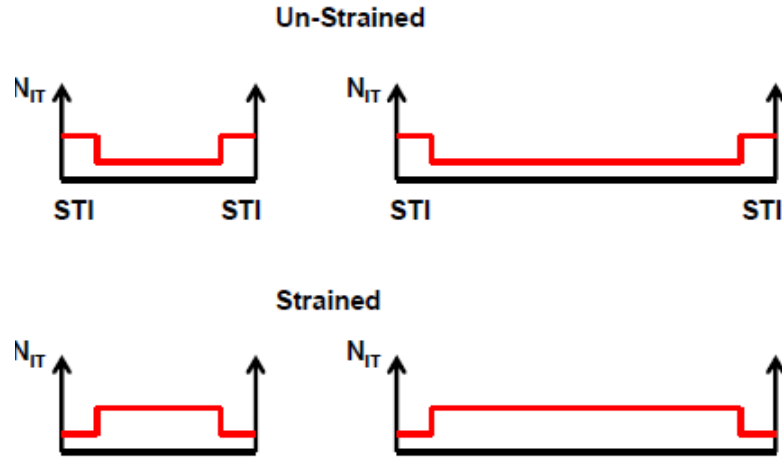
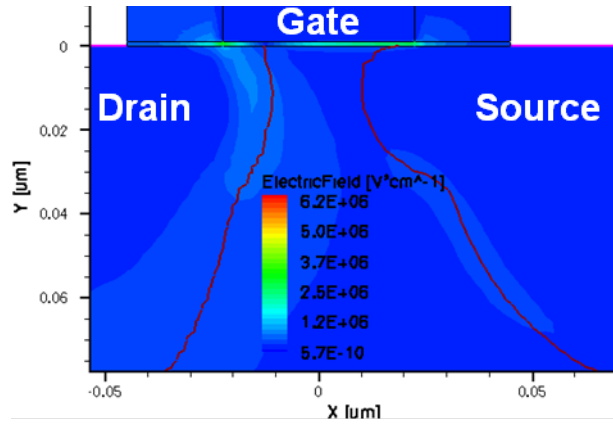


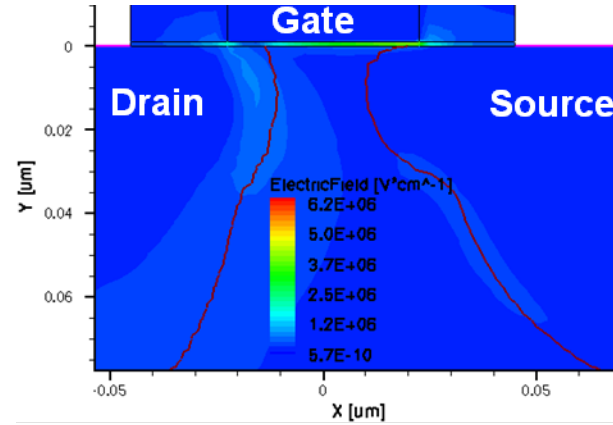
Figure 56: Schematic diagram of enhanced trap formation along the STI edge for un-strained MOSFET, and trap formation in the middle of channel for strained MOSFET.

Figure 57 shows the TCAD simulated electric field lines in the device for varying gate voltage. The simulated device is an asymmetric halo doping device with low electric field at the drain-body junction. Interestingly, the electric field at the gate-drain junction is larger for lower gate bias. Thus, larger hot-carrier degradation is expected at the gate-drain junction for lower gate voltage. However, as the gate

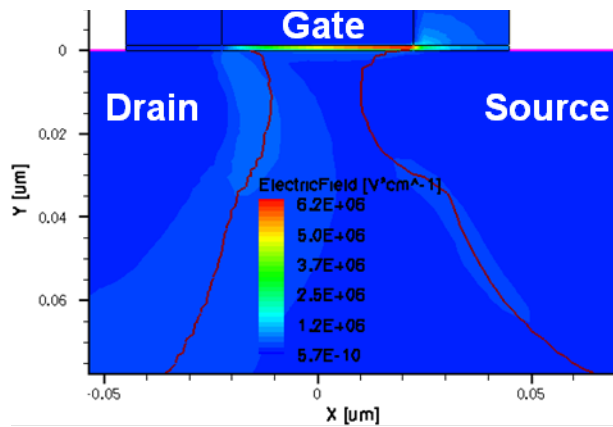
voltage increases the electric-field at the gate-source junction increases. Therefore, larger hot-carrier degradation occurs at the gate-source junction for increasing gate voltage. Looking at the device electrical characteristics we see similar results. Figure 58 shows the electrical characteristics of the above simulated device for varying gate voltage. Figure 58(a) shows the $I_{DS} - V_{DS}$ characteristics for varying gate voltage. Figure 58(b) shows the $I_{BODY} - V_{DS}$ characteristics and Figure 58(c) shows the $M - 1$ vs. V_{DS} characteristics. As can be seen from Figure 58(c) the impact ionization induced generation current (denoted by $M - 1$) is larger for smaller V_{GS} . A reduced multiplication factor ($M - 1$) implies a longer device lifetime. Note that the body current is a function of both V_{GS} and V_{DS} . At smaller V_{DS} the maximum body current occurs at smaller V_{GS} . For larger V_{DS} the maximum body current occurs at larger V_{GS} .



(a) $V_{GS}=0.3$ V, $V_{DS}=1.0$ V

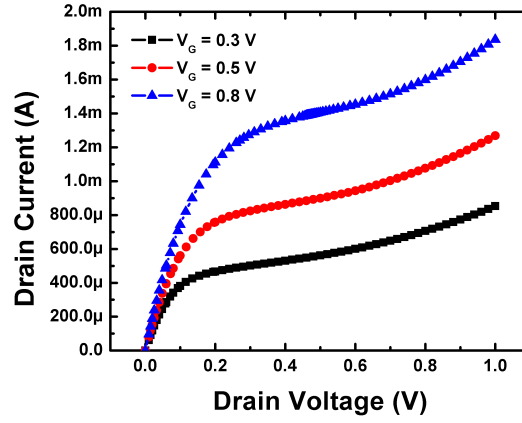


(b) $V_{GS}=0.5$ V, $V_{DS}=1.0$ V

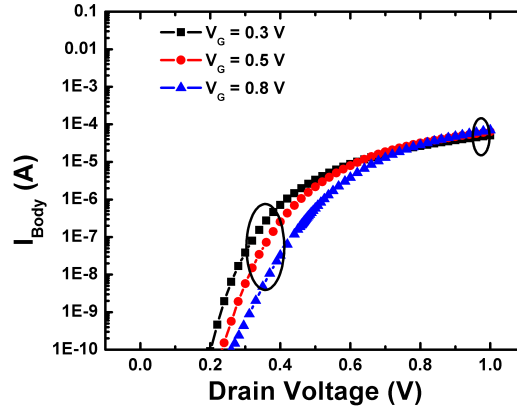


(c) $V_{GS}=0.8$ V, $V_{DS}=1.0$ V

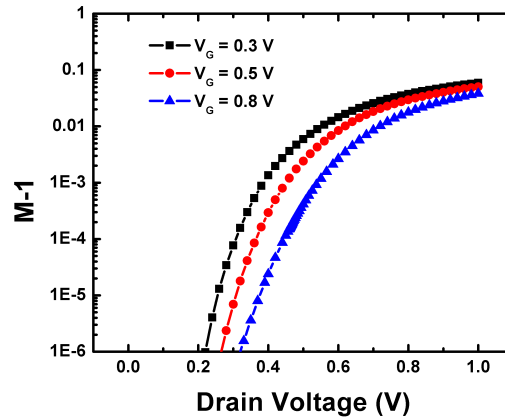
Figure 57: TCAD simulated electric field lines of a nFET with varying gate voltage.



(a) I_{DS} vs. V_{DS} characteristics



(b) I_{BODY} vs. V_{DS} characteristics



(c) $M-1$ vs. V_{DS} characteristics

Figure 58: TCAD simulated I_{DS} vs. V_{DS} , I_{BODY} vs. V_{DS} , $M-1$ vs. V_{DS} characteristics of a nFET with varying gate voltage.

4.6 Summary

Larger width devices show enhanced degradation compared to narrow width devices. Large device width is required to achieve sufficient gain and linearity from the device, hence posing problems for RF circuit design. Strain in the channel region is responsible for enhanced degradation for nFETs.

CHAPTER V

IMPACT OF CMOS SOURCE/DRAIN METAL CONTACT SPACING AND GATE-FINGER TO GATE-FINGER SPACING ON PERFORMANCE AND RELIABILITY

5.1 *Overview*

A novel study showing the effect of source/drain metal contact spacing and gate-finger to gate-finger spacing on the device RF performance is carried out. Further, the impact of above on the hot-carrier, RF stress, and total-dose irradiation tolerance is studied.

The contents of this chapter have been published in part at [3], [4].

5.2 *Introduction*

Floating-body devices have improved RF performance (power-gain, linearity, f_T , f_{MAX}), as compared to body-contacted devices (Figures 12(c), 12(d)). However, body-contacted devices exhibit better reliability owing to better control over short-channel effects, forcing a trade-off between performance and reliability (Figure 15). In this work, we show device layout modifications can be used for floating-body devices to improve their reliability. In addition, devices with symmetric and asymmetric halo doping are investigated here. Source/drain metal contact spacing has been shown to have significant impact on device parasitics and thus RF performance [1], [4]. The devices used in this study were laid out in multiple gate-finger (20 fingers) arrangements, similar to that commonly used in RF circuit design. These devices are from a commercial silicon technology and have not been radiation hardened in any way. To compare the impact of S/D metal contact (S/D CA-CA) spacing and

gate-finger to gate-finger (PC-PC) spacing on RF performance and radiation tolerance, four device layouts are examined here (see Figure 59, Table 3).

For hot-carrier stress testing, the devices were stressed in the drain avalanche hot-carrier condition ($V_{GS} = 1.0$ V; $V_{DS} = 1.5$ V). Radiation experiments were performed with an ARACOR 10-keV x-ray source at a dose rate of 31.5 krad(SiO_2)/min (Figure 33). The devices were biased at constant voltage during the total-dose irradiation testing ($V_{GS} = 1.0$ V; $V_{DS} = 1.5$ V). The measurements were made in-situ. The RF measurements were performed on a custom integrated S-parameter and load-pull system, which allows both small- and large- signal measurements with a single probe contact. Each device was measured at least two times with the same set of conditions to check for data fidelity.

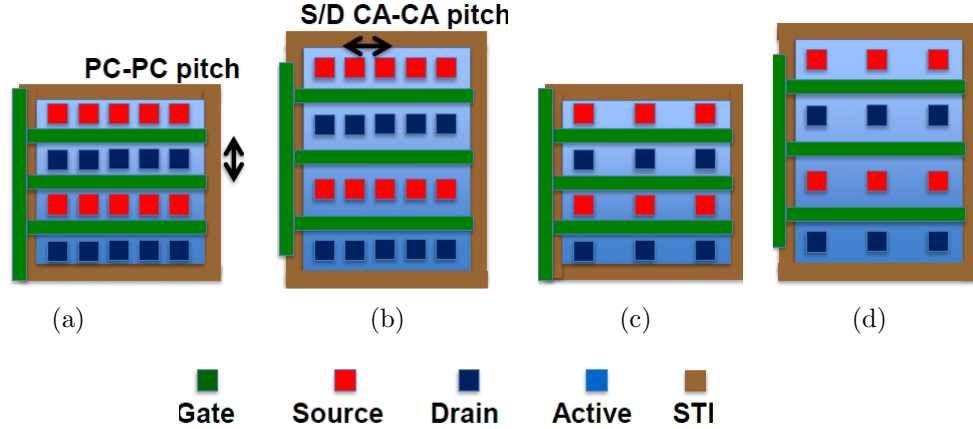


Figure 59: Layout of the floating-body devices. Device with (a) tight gate-finger to gate-finger and tight source/drain (S/D) metal contact spacing, (b) loose gate-finger to gate-finger and tight S/D metal contact spacing, (c) tight gate-finger to gate-finger and loose S/D metal contact spacing, and (d) loose gate-finger to gate-finger and loose S/D metal contact spacing.

Table 3: Devices used to study the impact of source/drain metal contact and gate-finger to gate-finger spacing on performance and reliability

Device Parameter	A	B	C	D
W/L (μm)/(μm)	2.0/0.045	2.0/0.045	2.0/0.045	2.0/0.045
Number of Fingers	20	20	20	20
Gate-finger to gate-finger spacing (μm)	0.150	0.340	0.150	0.340
CA-Gate spacing (μm)	0.045	0.140	0.045	0.140
Source/Drain contact spacing (μm)	0.084	0.084	2.000	2.000

5.3 Impact on RF Performance and DC Reliability

The unity gain cut-off frequency of the four devices with varying S/D contact spacing and gate-finger to gate-finger spacing is shown in Figure 60(a). The devices with the tightest S/D contact spacing have higher cut-off frequency (f_T) (devices A, B) than the devices with the largest S/D contact spacing (devices C, D). This is attributed to larger electric-field in the channel region for devices with a tighter S/D contact spacing. Devices with optimum gate-finger to gate-finger spacing (devices B, D) have the highest f_T . This can be attributed to smaller parasitic capacitances for devices with optimum gate-finger to gate-finger spacing. Similar trends are observed in the maximum oscillation frequency (f_{MAX}), with devices B and D having larger f_{MAX} than devices A and C, respectively (Figure 60(b)).

Figure 61(a) shows the RF output-power of the device plotted as a function of the RF input-power. The power measurements are made at a CW frequency of 9 GHz. Devices A and B exhibit higher power-gain and 1-dB gain compression point than devices C and D. The same trend as observed in the device f_T is also seen in the power-gain performance (Figure 61(a)). These devices were tested in a hot-carrier stress condition to study the impact of contact spacing on hot-carrier reliability [1]. Devices with the tight S/D contact spacing have the largest hot-carrier stress-induced threshold voltage shifts compared to devices with the largest contact spacing (Figure 62). Devices with optimum gate-finger to gate-finger spacing had lower threshold

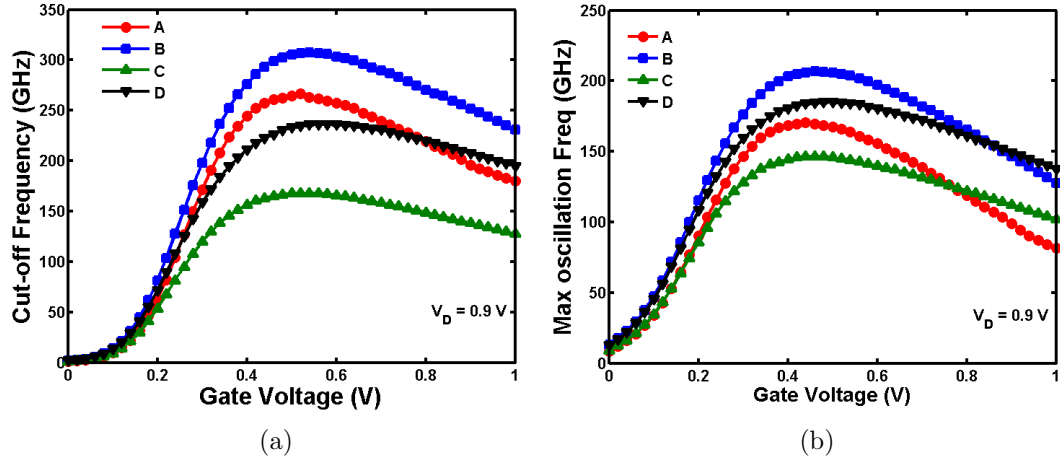


Figure 60: (a) Cut-off frequency (f_T) as a function of gate voltage of the devices with varying contact spacing. (b) Maximum oscillation frequency (f_{MAX}) as a function of gate voltage of the devices with varying contact spacing.

voltage shifts (Figure 62).

The devices were tested in a total-dose irradiation environment under identical bias conditions. The sub-threshold I_{DS} - V_{GS} characteristics for a device with the tight S/D contact spacing (device A) are shown as a function of irradiation dose in Figure 63(a). There is a significant increase in the off-state leakage current of this device with increasing total-dose radiation (to 1 Mrad(SiO_2)). The threshold voltage shifts observed under biased radiation exposure are smaller than those observed under the hot-carrier stress. This is because of the neutralization of the hot-carrier stress-induced electron trapping in the gate-oxide by the radiation-generated holes [60]. Charge trapping in the shallow trench isolation (STI) produces the increase in off-state leakage. The sub-threshold I_{DS} - V_{GS} characteristics of the device with loose S/D contact spacing are shown in Figure 63(b). This device exhibited almost no change in off-state current with total-dose irradiation. The impact of total-dose radiation on the off-state leakage of the four devices with varying contact spacing is shown in Figure 64.

Devices A and B show a significant increase in off-state leakage compared to devices C and D. Device A had a greater increase in off-state current compared to

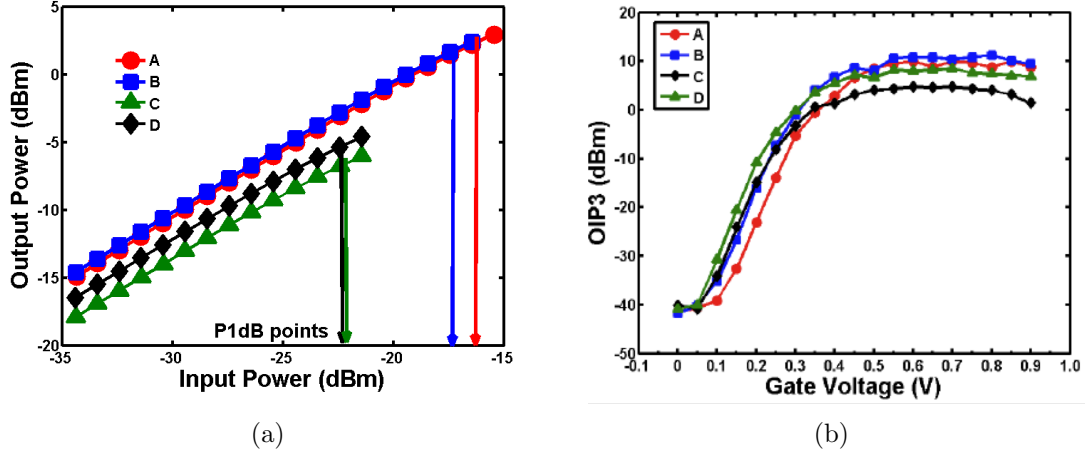


Figure 61: (a) Output-power as a function of input-power of the nFETs with varying contact spacing. (b) Output-third-order-intercept point (OIP3) of nFETs with varying contact spacing.

device B. The enhanced damage for devices A and B can be attributed to the larger electric-fields across the device gate-drain depletion region than for devices C and D [1]. The RF performance degradation of the devices follows the same trend (Figure 65). 3D TCAD models were created to understand the impact of S/D metal contact spacing on the MOSFET reliability. The device with tight S/D contact spacing has larger on-state current (Figure 66(a)). Figure 66(b) shows the electric-field in the channel region for loose and tight S/D contact spacing devices. The device with tight S/D contact spacing has larger electric-field at the source and drain region. This larger electric-field in the ‘active’ region results in larger numbers of hot-carriers (as a result of enhanced impact ionization) and hence enhanced hot-carrier degradation. Also, the current crowding effects are enhanced for devices with tight S/D contact spacing.

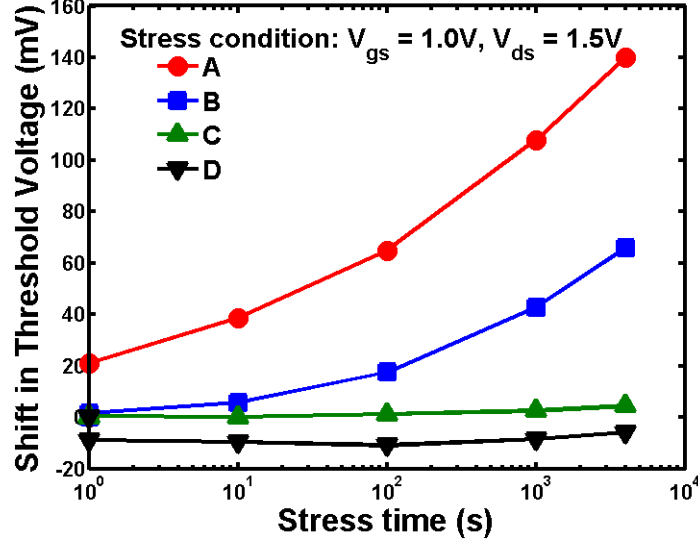


Figure 62: Threshold voltage shift of nFETs with the same dimensions ($L = 45$ nm, $W_f = 2$ μ m), but varying contact spacing.

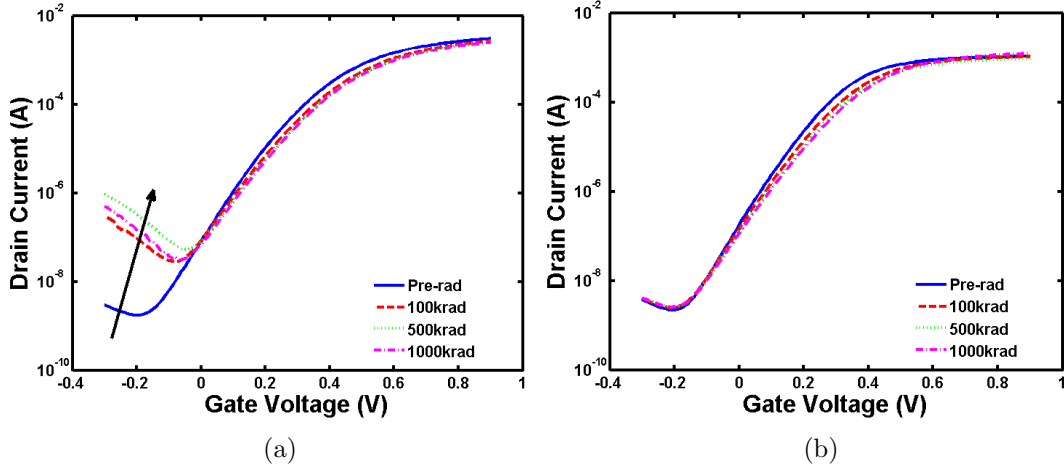


Figure 63: (a) Transfer characteristics of device A with tight S/D contact and gate-finger to gate-finger spacing. (b) Transfer characteristics of device C with loose S/D contact and gate-finger to gate-finger spacing.

5.4 Impact on RF Reliability

The ESD and DC hot-carrier reliability dependence on contact spacing has been reported previously [1], [61]. NMOS devices with tight drain contact spacing had more ESD damage, which was attributed to a non-uniform current flow in this case [61]. The devices with tighter S/D contact spacing were shown to be more susceptible to hot-carrier damage [1]. Device A and B show larger threshold voltage shifts in the

hot-carrier stress condition than devices C and D (Figure 62) [1]. The pFETs show similar trends as the nFETs. Devices with tighter S/D contact spacing have larger electric-field at the drain than devices with looser spacing, as a result of the decreased silicide diffusion resistance (Figure 66(b)) [1].

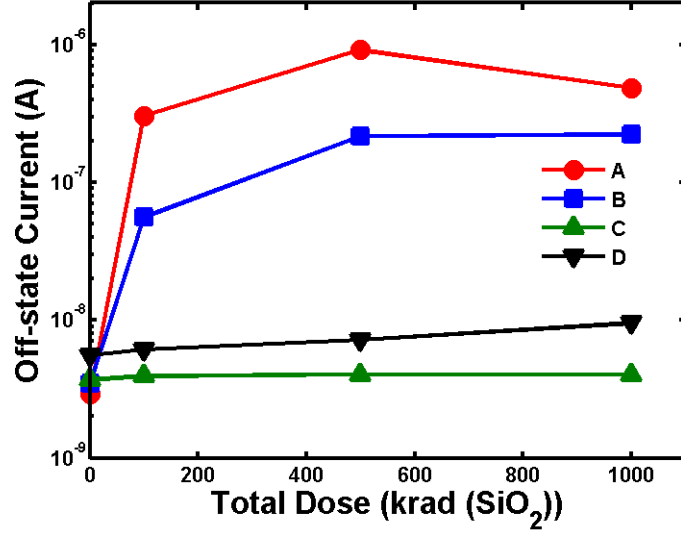


Figure 64: Off-state drain current as a function of total irradiation dose of the four devices with varying contact spacing.

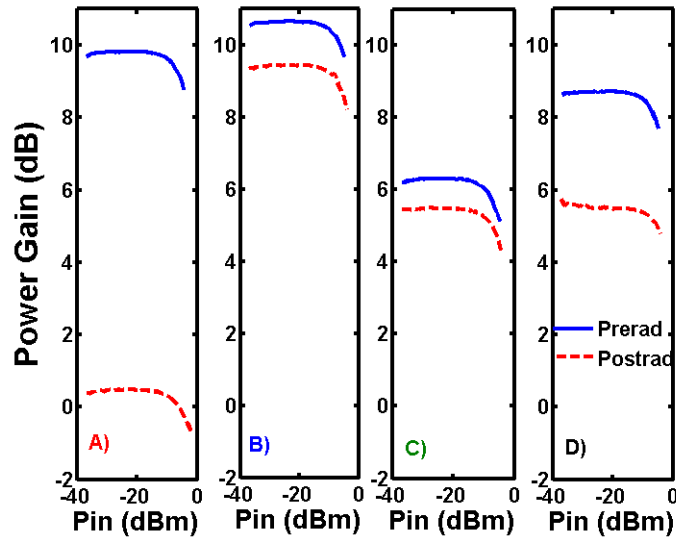


Figure 65: Power-gain as a function of input-power of the devices with varying contact spacing (pre- and post-irradiation).

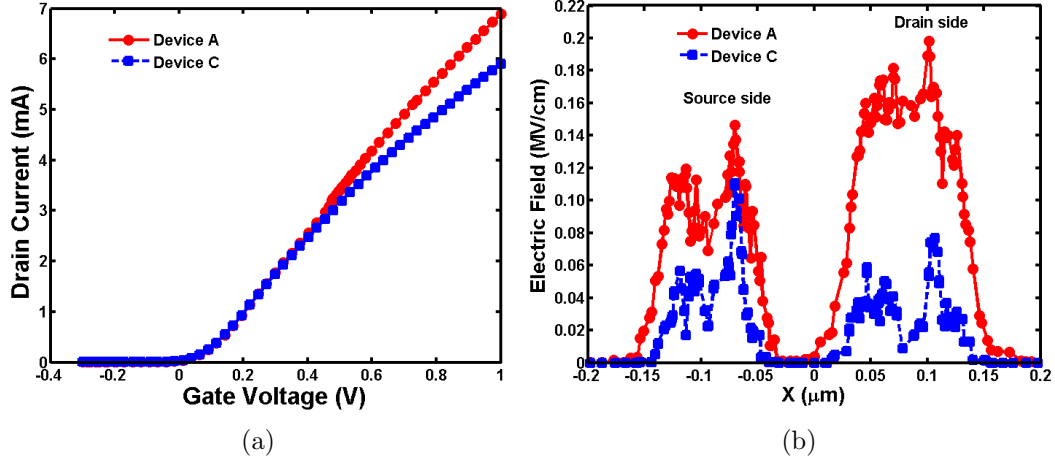


Figure 66: (a) TCAD simulated I_{DS} - V_{GS} characteristics of the devices with varying contact spacing. (b) Simulated electric-field along the channel region of the devices with varying contact spacing.

The RF measurements were performed on a custom integrated S-parameter and load-pull system, which allows both small- and large-signal measurements with a single probe contact (Figure 67). The device source and load impedances are matched for maximum gain. The RF stressing is performed in the impedance matched configuration with the device biased at peak f_T conditions ($V_{GS} = 0.6$ V, $V_{DS} = 0.9$ V). A two-step de-embedding technique based on the open/short calibration test structures is used. For the RF parameter extraction (C_{GD} , R_G , R_D), a physics-based RF model is assumed and fitted to the measured S-parameters [62]. All measurements are performed at room temperature. Three samples of each device were tested and the results are repeatable.

Here we describe the effects of contact spacing and gate-finger to gate-finger spacing on RF stress results of nFETs. The devices are stressed at constant RF input-power (0 dBm) (CW frequency = 9.0 GHz) for varying stress times and also stressed with varying RF power for constant time ($t = 100$ s) at the peak f_T bias condition ($V_{GS} = 0.6$ V, $V_{DS} = 0.9$ V). Consistent degradation in DC and RF parameters is observed with increasing stress time and power. We observe a positive shift in threshold voltage

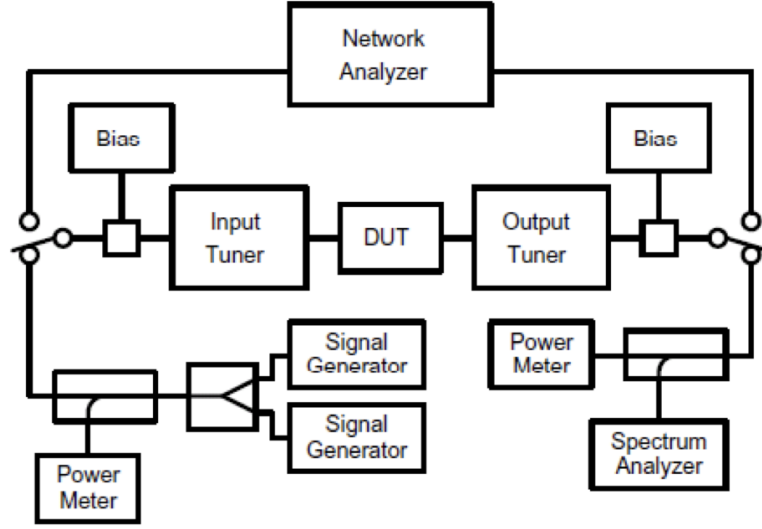


Figure 67: Block diagram of the load-pull measurement setup used for RF measurements.

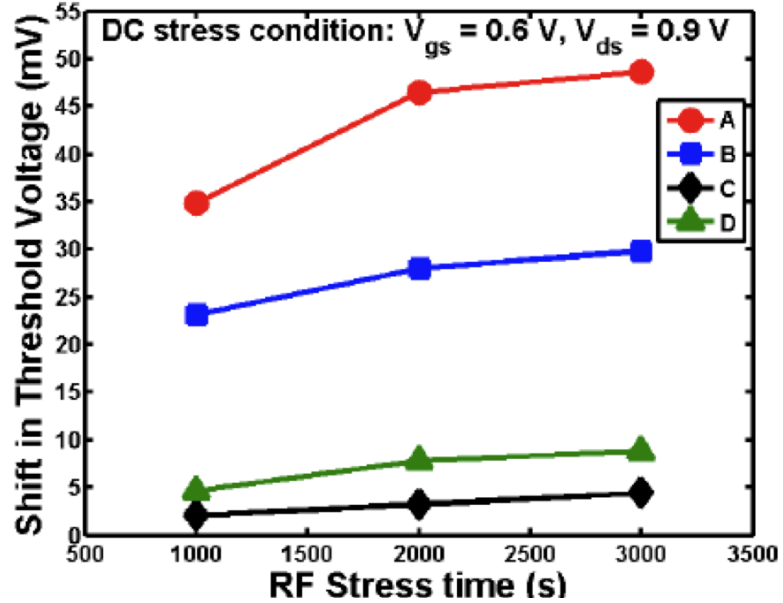


Figure 68: Shift in threshold voltage with RF stress (at $V_{GS} = 0.6$ V, $V_{DS} = 0.9$ V) of nFETs with loose and tight S/D contact spacing (Frequency = 9 GHz, $P_{in} = 0$ dBm).

(indicating electron traps in gate-oxide) and a decrease in drive current (mobility degradation) (Figure 68). The threshold voltage shifts in the RF stress condition (Figure 68) are a result of the hot-carrier degradation due to DC bias. The magnitudes of threshold voltage shifts in Figure 68 are much smaller than Figure 62 because of lower DC voltages applied for peak f_T bias condition. The devices are stressed up to

3000 s under constant RF power stress (RF power = 0 dBm) (Figure 69(a)). The device with wider S/D contact spacing (devices C, D) is able to operate for longer times and shows smaller threshold voltage shifts than devices with tight contact spacings (devices A, B). The devices are stressed at the same RF input-power (although they have different P1dB). The P1dB power level defines the maximum power level where the device provides gain. It does not limit the maximum input-power that can be applied to the device. Therefore, for a fair evaluation of the impact of layout on device RF stress reliability, the same input-power levels are applied. The devices are stressed at up to 13.6 dBm of RF power for constant stress time (time=100 s) (Figure 69(b)). This high power would be a representation of the worst case scenario for a device used for example in a SPDT switch. The RF parameters of interest, small-signal gain (S21), isolation (S12), cut-off frequency (f_T), maximum oscillation frequency (f_{MAX}) and unilateral power-gain all degrade with applied stress (Figure 69). As shown in Figure 69(a), Device C shows much smaller degradation in RF parameters for varying stress time than device A. In addition, device C (with wider Source/Drain CA-CA spacing) can operate up to higher RF power levels (Figure 69(b)).

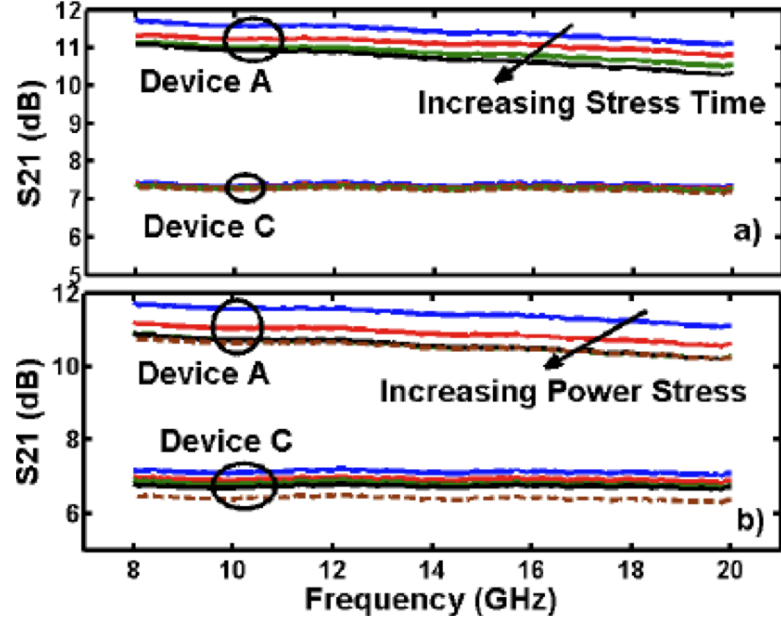


Figure 69: Comparison of S21 degradation with increasing (a) RF stress time for 1000 s, 2000 s, and 3000 s stress (for constant power = 0 dBm) and (b) input RF power of +5, +6, +7 dBm (for constant stress time = 100 s) of nFETs (at peak f_T bias).

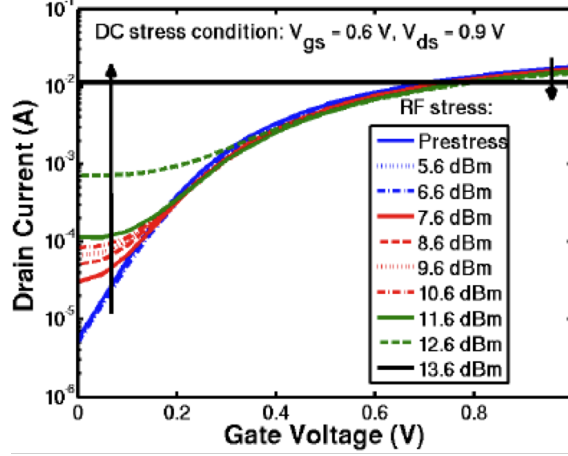
5.5 Mechanisms

For the three stress conditions (hot-carrier, constant power stress for varying time, and constant time stress for varying power) the physical mechanisms causing the degradation are not the same. With hot-carrier stress as a function of increasing stress time only threshold voltage shift and mobility degradation is observed. This is because of the hot electron trapping in the gate-oxide [1]. These DC parametric shifts further show up in RF parameter degradation [1].

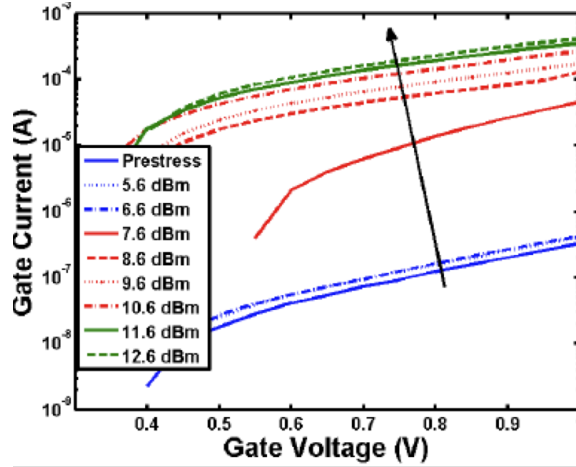
With constant RF power stress for varying time threshold voltage shift and mobility degradation is observed at moderately high input-power levels ($P_{in} = 0$ dBm) [4]. The shifts are mostly as a result of the hot-carrier stress by DC bias on the device. The device input is looking at an impedance of $49 + j119$ in the source matched condition. That corresponds to around 0.36 V at input (for $P_{in} = 0$ dBm). These DC parametric shifts further show up in RF parameter degradation. Thus under normal

device operating conditions of circuits like low-power LNA/switches, the device is expected to operate without much degradation for long time.

In the catastrophic instance of leakage of RF power to an unintended port (e.g power transmission from the power amplifier to the receiver on the same chip), it is important to study parameter degradation as a function of varying power level. For varying RF power stress (constant time), the off-state leakage current continuously increases along with positive threshold-shifts and mobility degradation (Figure 70(a)). The gate current increases continuously with increasing power stress, initially soft oxide breakdown is observed (upto $P_{in} \sim 10$ dBm) followed by hard oxide breakdown (Figure 70(b)). Device A, B show soft gate-oxide breakdown at much lower power levels than device C, D. This increased off-state leakage can be attributed to the Fowler-Nordheim (FN) tunneling of electrons from the gate to the drain above certain power levels [63]. Further, higher RF power results in gate-oxide breakdown. High RF power stress (above 0 dBm) results in large electric-field in the drain region under the gate-drain overlap. In a 50 Ohm system, 10 dBm corresponds to 0.7 V. The device input is looking at an impedance of $49 + j119$ in the source matched condition. This corresponds to around 1.2 V at input. This voltage stress as a result of RF signal when added to the DC bias causes significant damage as shown in Figures 69, 70(a). The high frequency RF signal can also pass through the parasitic gate drain overlap capacitance (C_{GD}) and also gate-source overlap capacitance (C_{GS}) to directly appear at the drain/source terminal of the FET. This can form a positive feedback loop and hence causing enhanced degradation [8]. This fact is supported by the observation that device A, B degrade at lower power levels compared to device C, D (Figure 69). The reason being that device A, B have greater parasitic capacitance (C_{GS} , C_{GD}) than device C, D as a result of the greater interaction between S/D contacts (Figure 71). Also Device A, C degrade at lower power levels compared to device B, D again as a result of the greater parasitic capacitance (C_{GS} , C_{GD}).



(a)



(b)

Figure 70: (a) Transfer characteristics of nFET (device C) with varying RF power stress ($V_{GS} = 0.6$ V, $V_{DS} = 0.9$ V). Stressed for 100 s at each power step (frequency = 9 GHz). (b) Gate current characteristics of nFET (device C) with varying RF power stress ($V_{GS} = 0.6$ V, $V_{DS} = 0.9$ V).

The devices with closely spaced source/drain CA-CA spacing (devices A, B) exhibit greater degradation of drive current than devices with looser source/drain CA-CA spacing (device C, D) (Figures 72 and 73). This may be attributed to the higher electric-field in the device with tightly spaced contacts, which in turn results in greater damage of the gate-oxide. The gate-to-drain capacitance (C_{GD}) decreased after stress, indicating an increase in drain junction depletion region width (eventually leading to punch-through). We observe the same tradeoffs in hot-carrier stress as devices

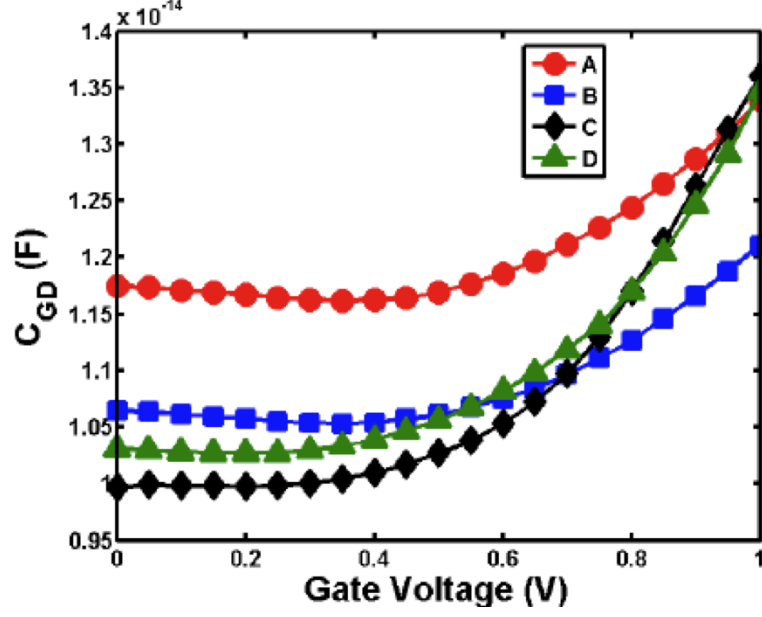


Figure 71: Gate-to-drain capacitance (C_{GD}) as a function of gate voltage of nFETs with varying contact spacing.

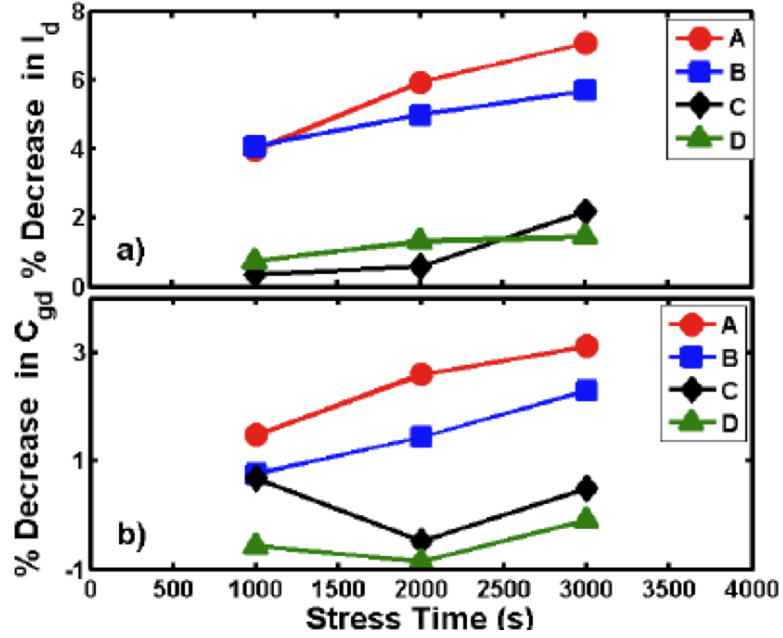


Figure 72: Comparison of (a) I_{DS} degradation (percentage) as a function of RF stress time (at peak f_T bias) (b) C_{GD} degradation (percentage) as a function of RF stress time of nFETs (at peak f_T bias).

with wider S/D contact spacing can work under higher RF input power levels without catastrophic failure. The device on-state drain current and gate-to-drain capacitance decreases for all four device variants with increasing power (Figure 73). Devices C

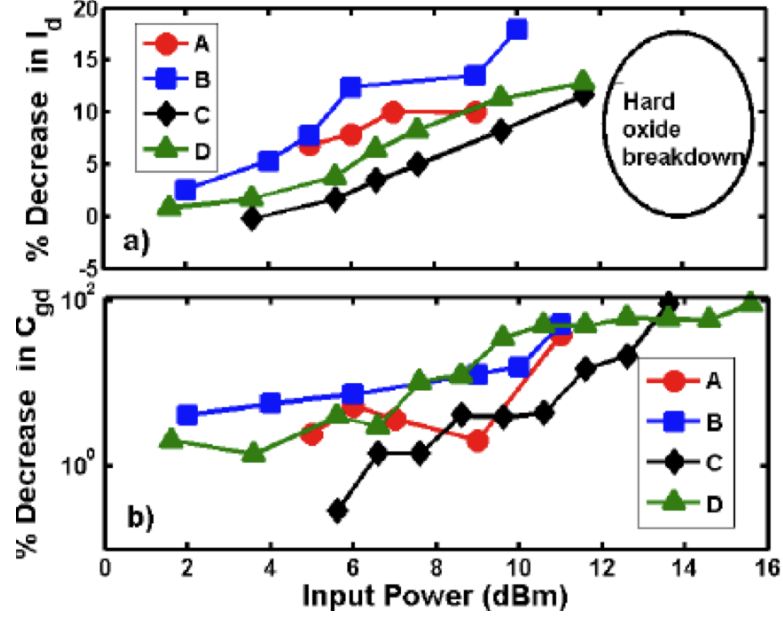


Figure 73: Comparison of (a) I_{DS} degradation (percentage) as a function of RF input-power (b) C_{GD} degradation (percentage) as a function of RF input-power of nFETs (at peak f_T bias).

and D are able to operate at higher power levels without catastrophic failure (despite the fact that they have a lower P1dB).

5.6 Impact of Asymmetric Halo Doping on the Performance and Reliability of Sub 100-nm CMOS

Asymmetric halo devices have better DC, RF performance than symmetric halo devices [25]. Asymmetric halo doping devices have larger halo doping near the source but no halo doping on the drain end of the channel. In this technology, asymmetric devices have a source-side halo pocket of $1 \times 10^{19} \text{ cm}^{-3}$ concentration and a low doped drain channel doping of $5 \times 10^{17} \text{ cm}^{-3}$ (a factor of 20-fold) (Figure 74(a)). The symmetric control devices are shown to be close to a uniform profile with a channel doping concentration of $3 \times 10^{18} \text{ cm}^{-3}$ (Figure 74(b)).

Thus, the electric-field at the drain terminal for asymmetric devices is expected to be much lower than for symmetric halo doping devices. Results from TCAD simulations confirm this hypothesis (Figure 75(a)). Symmetric and asymmetric halo

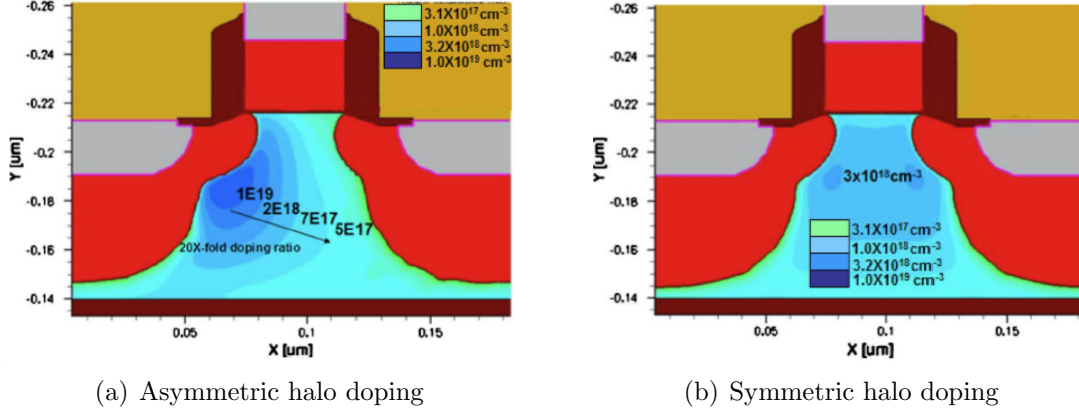


Figure 74: (a) TCAD simulations showing the doping concentration for the asymmetric device. Asymmetric devices have a large lateral gradient doping profile with a source-side halo pocket of $1 \times 10^{19} \text{ cm}^{-3}$ concentration and a low-doped drain channel doping of $5 \times 10^{17} \text{ cm}^{-3}$ (a change of 20-fold). (b) TCAD simulations showing the active doping concentration for the symmetric control device. The symmetric control devices have a uniform profile with a channel doping concentration of $3 \times 10^{18} \text{ cm}^{-3}$ [25].

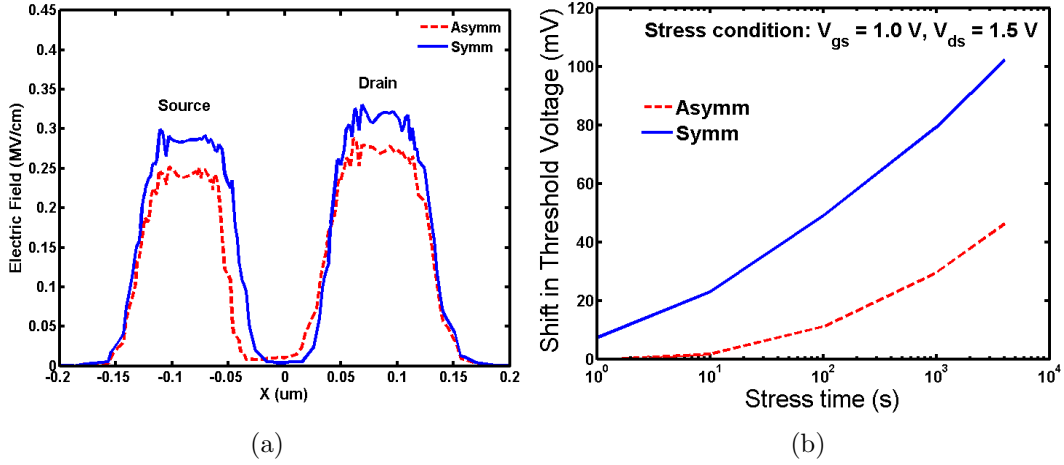


Figure 75: (a) Electric-field in the channel region of asymmetric and symmetric halo doping nFETs. (b) Threshold voltage shifts of asymmetric and symmetric halo doping nFETs with the same dimensions ($L = 45 \text{ nm}$, $W_f = 2 \mu\text{m}$).

doping devices of identical dimensions ($L = 45 \text{ nm}$, $W_f = 2 \mu\text{m}$) were measured for both hot-carrier and total-dose irradiation response. Figure 75(b) shows the shift in threshold voltage observed for hot-carrier stress condition. Asymmetric devices have over a 50 % reduction in threshold voltage shift compared to the symmetric devices, and a significant reduction in off-state leakage current for increasing total-dose is

also observed for the asymmetric devices (Figures 63(a), 76). Figure 77(a) shows the measured data for the body current for asymmetric and symmetric nFETs for different channel length. Asymmetric nFETs have a smaller body current (and hence a smaller impact ionization in the channel region) than symmetric nFETs for both channel length. Hence explaining the improved reliability of asymmetric nFETs. Figure 77(b) shows the measured body current for varying channel length. The body current has clear peak at $V_{GS} = \sim V_{DD}/2$ for $L = 0.472 \mu m, 0.736 \mu m$. However, the peak of body current shifts to $V_{GS} = \sim V_{DD}$ for $L = 0.188 \mu m, 0.056 \mu m$.

Thus, asymmetric halo doping can be used to improve the performance and reduce the hot-carrier degradation for short-channel MOSFETs.

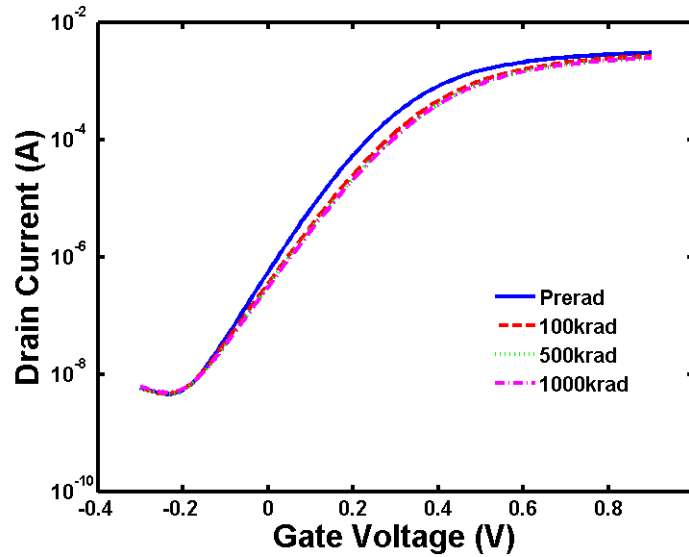


Figure 76: Total-dose irradiation induced increase in off-state current of nFETs with asymmetric halo doping ($L = 45 \text{ nm}$, $W_f = 2 \mu m$).

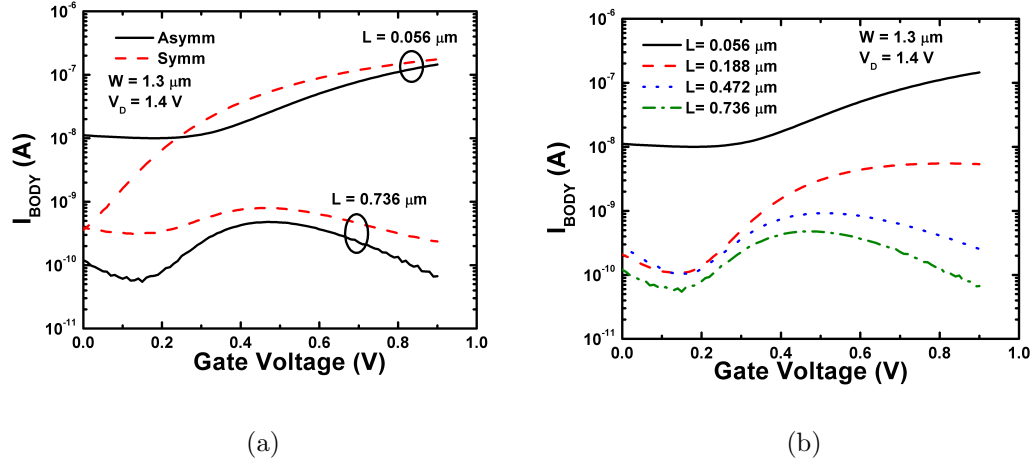


Figure 77: (a) Measured body current as a function of gate voltage of nFETs with asymmetric halo doping and symmetric halo doping. (b) Measured body current as a function of gate voltage of nFETs with asymmetric halo doping for varying channel length.

5.7 Summary

We demonstrated the effects of source/drain metal contact spacing on the hot-carrier, total-dose, and RF reliability. The resulting RF performance vs. reliability trade-offs are shown. Devices with tight S/D contact spacing demonstrate better RF performance, but enhanced total-dose degradation. Devices with optimum gate-finger to gate-finger spacing had the best RF performance and the least radiation-induced degradation. For circuit designs in ultra short channel length FETs, device layout optimization can result in improved RF performance and acceptable reliability.

CHAPTER VI

CRYOGENIC LATCHUP IN SHORT-CHANNEL CMOS TECHNOLOGIES

6.1 Overview

Latchup phenomenon in CMOS technologies is shown to be possible at cryogenic temperatures (below 50 K), and its consequences are discussed. Different latchup hardening techniques are also studied.

The contents of this chapter have been published in part at [5].

6.2 Introduction

This chapter describes the electrical latchup characterization at low-temperatures, and also the single-event latchup characterization at low-temperatures conducted in collaboration with NASA GSFC. The first observation of single particle-induced latchup (SEL) in CMOS circuitry operated under cryogenic conditions is reported. Conventionally it has been believed that the probability for particle-induced SEL in CMOS circuitry decreases significantly as the temperature is lowered and becomes impossible below ~100 K [64]-[73]. For this reason until recently, NASA flight projects have not tested cryogenic temperature operated CMOS circuitry for SEL. A current NASA flight project is going to use a high performance commercially available readout integrated circuit (ROIC) that will be indium bump bonded to a detector array for operation at 40 K. The ROIC is designed in a 0.5 μm bulk CMOS process. It is fabricated on a very lightly doped p-substrate with no specific latchup hardening mitigations considered in the design process. Although the unit cell is not aggressively

sized as compared to the amount of intra-cell circuitry, external circuits include high-speed precision analog and high-density digital logic circuits. In addition, another ROIC from the same manufacturer and process with comparable logic circuitry is known to be susceptible to heavy ion-induced SEL at room temperature. Although SEL is not observed at the operational temperature of 40 K, our investigation has shown that the ROIC chosen for flight is very sensitive to SEL in the region around 16-20 K. Recently, another NASA flight project operating a ROIC from a different vendor at 210 K has performed cryogenic SEL testing. Once again, SEL is not observed at the mission temperature, but is observed well below 300 K. The generally quoted conditions for latchup are that (1) the loop gain of the parasitic p-n-p-n structure exceeds unity, (2) a bias condition must exist such that both cross-coupled parasitic bipolar junction transistors (BJTs) are turned on long enough to achieve trigger-current (I_T) and trigger-voltage (V_T) sufficient to overcome the blocking state, and (3) the power supply and associated circuits are capable of providing the minimum holding-current (I_H) and holding-voltage (V_H) to maintain the latched condition [72], [73].

$$\beta_{npn}\beta_{pnp} > 1 \quad (5)$$

where β_{npn} and β_{pnp} are the common base current gains of the parasitic npn and pnp BJTs. This expression is greatly simplified because the geometry and the associated spreading resistances in the well and substrate regions that connect the parasitic transistors to each other and to the external power supply must be considered. Partially as a result, a myriad of expressions for the gain product as well as the holding-current and voltage exist in the literature.

A review of the literature reveals no experimental particle-induced SEL studies at cryogenic temperatures although there is a considerable electrical LU literature indicating increased LU immunity at temperatures below room temperature [64]-[73].

The variation in the holding-current in various CMOS logic gates which have been triggered in to a latched state was measured, and a substantial increase in both trigger- and holding- currents at 77 K was found [67].

A common misconception describes the dominant factor determining the LU probability as the temperature dependent reduction in the gain product of the parasitic BJTs. However, the relevant gain product is generally sufficient over a wide range of temperatures to sustain LU [67], [72], [73]. In general, one might expect the gain product to exceed unity possibly as low as ~ 100 K, but quite probably as low as about ~ 200 K. Other factors, such as the temperature dependence of the well and substrate resistances, and the base-emitter voltage required to sustain a given collector current in a parasitic BJT are also important and should be considered [72].

6.3 *Latchup Fundamentals*

Latchup in SOI technologies stems from a parasitic p-n-p-n structure formed when nFETs and pFETs are placed in close proximity, as in an inverter circuit. The p-n-p-n structure is comprised of a parasitic pnp and an npn transistor with coupled base-collector terminals. This parasitic p-n-p-n structure, also referred to as an SCR or thyristor, can be triggered from a high-resistance blocking state in to a low-resistance conducting state as a result of the large voltage swings on its anode (p^+ terminal) or cathode (n^+ terminal). Once triggered, the result is a short between V_{DD} and GND that could result in catastrophic damage to the IC if the current is not limited. This phenomenon of triggering the parasitic p-n-p-n structure from a blocking to conducting state is referred to as latchup.

6.4 *Latchup Device Physics*

The equivalent circuit representation of the parasitic SCR structure is shown in Figure 78. The parasitic npn (Q1) and pnp (Q2) transistors that make up the latchup structure and their interconnections are shown. One of the key features of the structure

is that the collector of the pnp transistor is connected to the base of the npn, and the collector of the npn is connected to the base of the pnp. The configuration can lead to a self-sustained regenerative feedback. The parasitic well resistances R_{WELL} and R_{SUB} play an important role in the triggering of latchup. These resistances are determined by the distance of the well contact from the source/drain diffusion. The latchup phenomena flow can be described as follows (Figure 79):

- a) PMOS p^+ drain junction becomes forward biased during power supply spikes, and/or single-event strikes. Holes are injected in to the n-well. These holes diffuse in the n-well with some reaching the n-well/substrate depletion region (Figure 79(a)).
- b) The holes are swept in to the substrate across the depletion region because of the built-in field of the p-n junction (Figure 79(b)).
- c) These holes must leave through the p^+ substrate contact, and cause a voltage drop across the substrate resistance (Figure 79(c)).
- d) The voltage drop across R_{SUB} can forward-bias the NMOS drain-substrate junction, which injects electrons into the substrate. These electrons can diffuse to the n-well to substrate depletion region and are swept in to the n-well (Figure 79(d)).
- e) These electrons must leave through the n^+ V_{DD} contact. The electron flow through the n-well causes voltage drop in n-well (Figure 79(e)).

The drop across R_{WELL} enhances PMOS p^+ drain junction forward bias and can lead to latchup condition.

There are two basic latchup categories: internal latchup and external latchup. Internal latchup can be induced by supply bounce or on-chip generation of carriers, which can trigger the parasitic SCR. External latchup can be induced from off-chip signals that can be received by the I/O and cause the parasitic SCR to trigger. These off-chip signals can generate large voltage bounces that can be responsible for the latchup event to occur either at the I/O or at the weakest internal circuits adjacent to the I/O cells. The consequences of latchup are large current flow through the

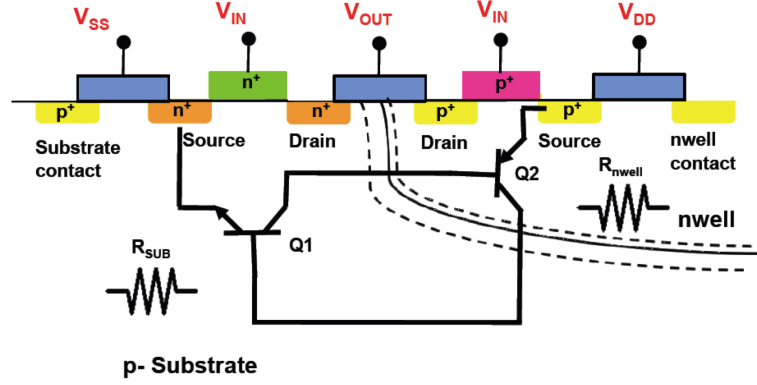


Figure 78: Schematic of the parasitic devices present in an inverter.

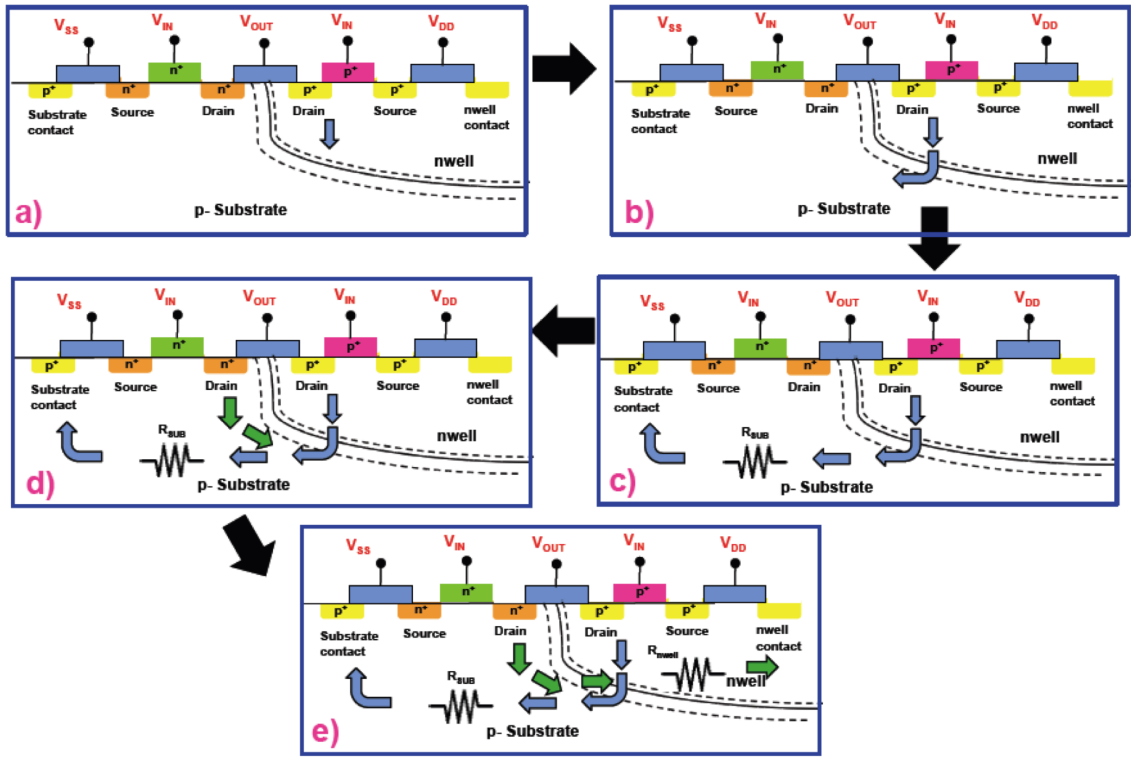


Figure 79: Latchup process flow.

semiconductor, which can cause oxide/junction breakdown and/or electro-migration.

Figure 80 shows an example of an electro-migration failure of a metal line on chip [74].

6.4.0.1 Latchup Characterization

a) Overshoot: In this test condition the p^+ to n-well junction becomes forward biased by a large positive voltage spike at the p^+ terminal. Thus holes flow from p^+ region

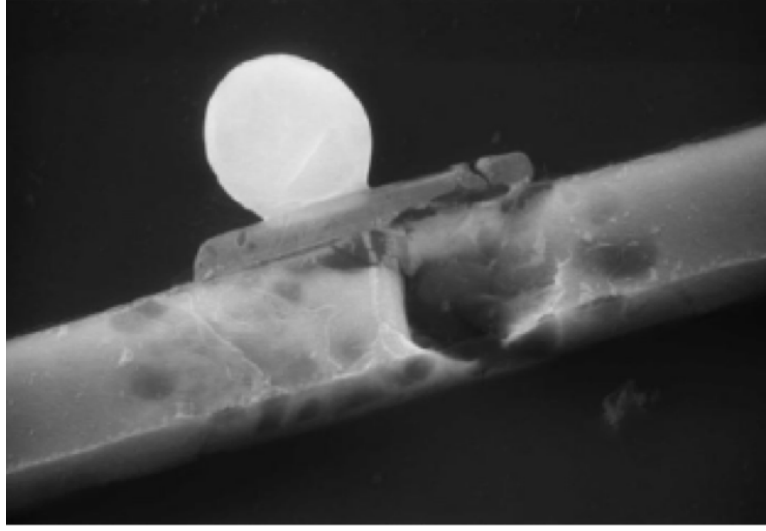


Figure 80: SEM image of a metal line damaged from the large current generated by a latchup event [74].

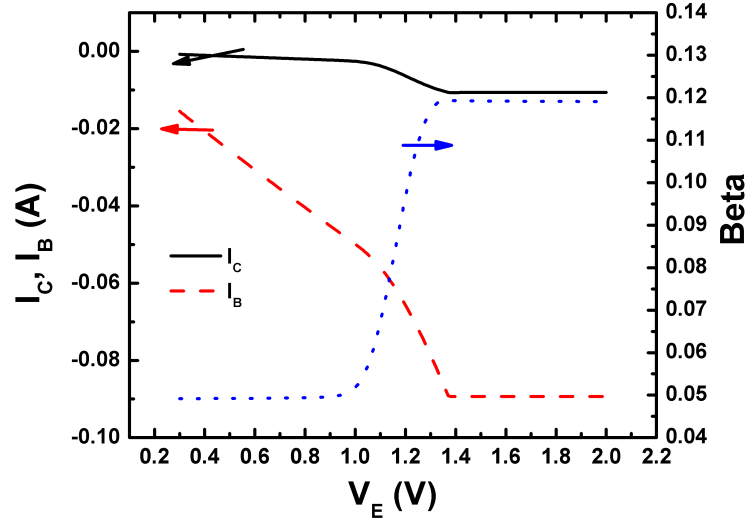
to the n-well and are finally swept through the depletion region in to the substrate. Thus the pnp parasitic bipolar (Q2) triggers first in overshoot testing.

b) Undershoot: In this test condition, the n^+ -substrate junction becomes forward biased by a large negative voltage spike at the n^+ terminal. Thus electrons flow from n^+ region to the substrate and are finally swept through the depletion region in to the n-well. Thus the npn parasitic bipolar (Q1) triggers first in undershoot testing.

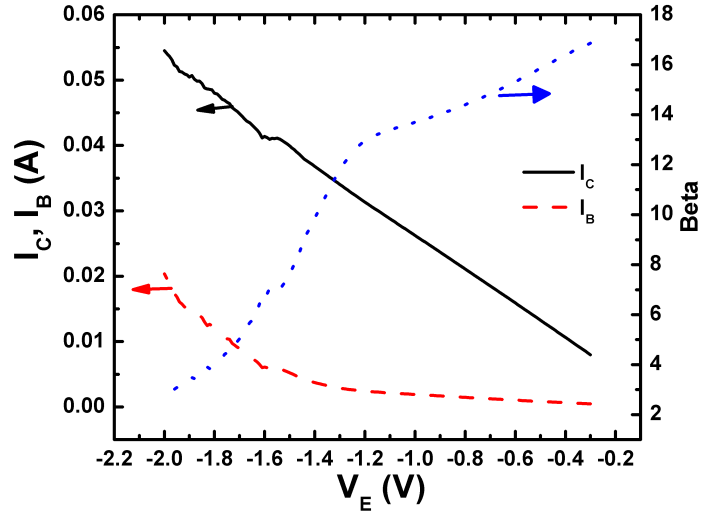
6.5 Latchup Characterization at Room Temperature

IBM 8HP (130-nm) p-n-p-n electrical latchup test structures were characterized. The parasitic bipolar transistors in a p-n-p-n structure were characterized. The ‘gummel’ characteristics and beta as a function of base-emitter voltage are shown in Figure 81. The npn parasitic bipolar has a larger gain than the pnp bipolar, as expected.

Figure 82 shows the anode current as a function of the anode voltage (latchup characteristics) for three different latchup structures: a) structure without any latchup protection (Basic); b) structure with n-ring (NS) protection; c) structure with deep-trench (DT) protection. The basic test structure shows classical latchup behavior with a negative resistance region, and clearly defined trigger and hold region. The



(a) PNP



(b) NPN

Figure 81: Gummel characteristics of (a) parasitic PNP and (b) parasitic NPN transistor present in a p-n-p-n doping structure.

test structure with n-ring protection has a larger trigger- and holding- voltage, and thus prevents latchup. The test structure with deep-trench isolation has no latchup characteristics and did not latchup at the applied bias conditions. Thus the structure with DT is most effective at preventing latchup (at an added cost of device area!). Distance between anode (p^+) and cathode (n^+) contacts also determines the latchup

conditions for a circuit. Figure 83 shows the latchup characteristics for two devices with different anode-to-cathode contact spacing. Device 1 has a smaller and device 2 has a larger anode-to-cathode spacing. The electrical characteristics show that device 2 with greater anode-to-cathode spacing has a larger holding-voltage and holding-current than device 1. Thus, during layout of a circuit the contact spacing between anode and cathode terminals must be chosen to meet latchup design requirements.

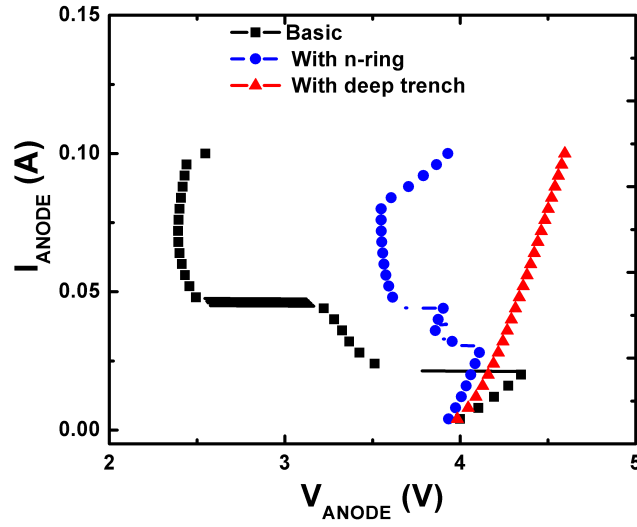


Figure 82: Latchup characteristics of a p-n-p-n structure without any protection (Basic), with a N-ring (NS), and with a deep-trench (DT).

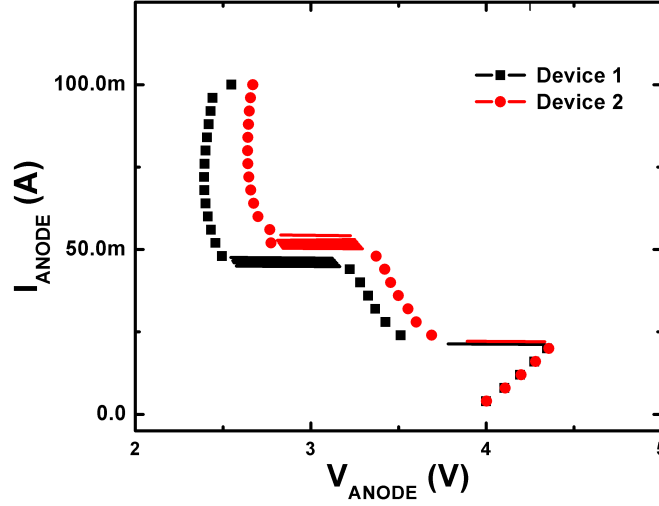


Figure 83: Latchup characteristics of a p-n-p-n structure without any protection (Basic) and with variation in anode-to-cathode spacing. Device 2 has a larger anode-to-cathode spacing than device 1.

6.6 Latchup Characterization Across Temperature

The latchup test structures were characterized across temperature (from 450 K to 20 K). Figure 84 shows the latchup characteristics across temperature. With increasing temperature, the trigger- and holding- voltages and currents decrease monotonically. Thus the structure becomes latchup sensitive at high temperatures, as expected. The trigger current-voltage and holding current-voltage characteristics are shown in Figure 85. The trigger- voltage and current increase with decreasing temperature (Figure 85(a)). However, the holding current-voltage characteristics are more complex (Figure 85(b)). The holding- current, voltage increase with decreasing temperature to ~100 K. However, below ~100 K the holding-current decreases. The holding-voltage increases with decreasing temperature to ~50 K and then starts decreasing.

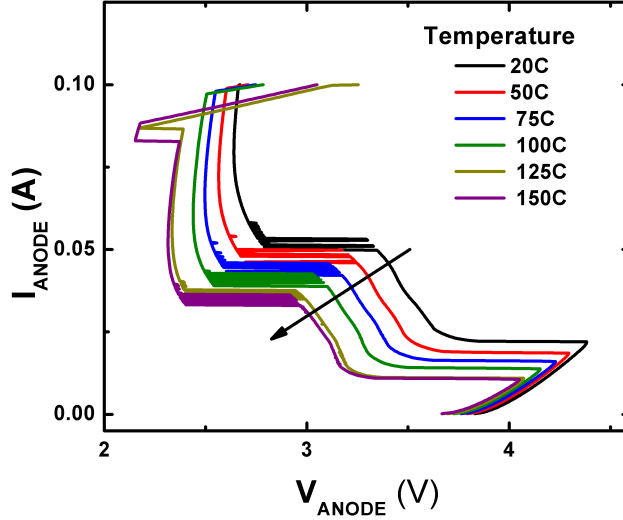
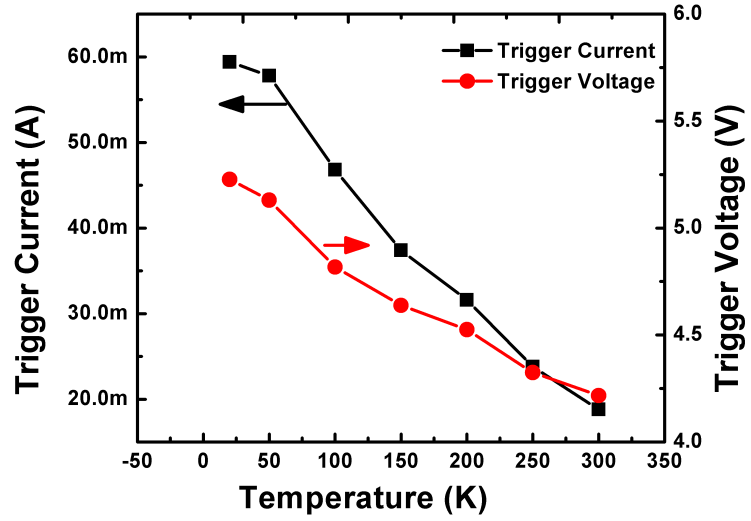


Figure 84: Effect of temperature on the latchup characteristics of a basic p-n-p-n structure.

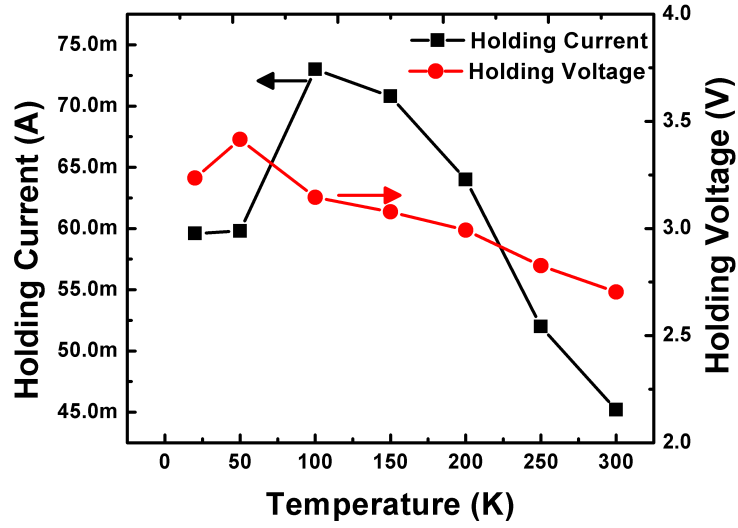
6.7 *Single-Event Latchup at Cryogenic Temperature*

Single-event latchup (SEL) experiments were performed at Texas A&M cyclotron. Ion-induced SEL is observed both at deep cryogenic temperatures (< 50 K) and over the classical LU regime (> 100 K), as shown in Figure 86 [5]. All data in the figure were acquired on a CMOS read-out integrated circuit (ROIC) at a $LET_{eff} = 64.4$ $MeVcm^2/mg$ and $R_p = 43$ μm . It is clear that the transition regions are quite narrow both at ~ 25 K and at ~ 135 K. The observed cross sections are the same to within experimental error for temperatures below 20 K as compared to the cross sections in the classical regime from ~ 200 -300 K. Free carriers from the ion strike initiates a shallow level impact ionization process that creates significant current flow and enables conditions required for a sustained single-event latchup at cryogenic temperatures.

In this work, we demonstrated that latchup can occur under cryogenic conditions. New latchup characterization techniques were developed. Single-event latchup was also shown to occur under cryogenic conditions. Process and layout changes were shown, which prevent latchup.



(a)



(b)

Figure 85: (a) Trigger-current and trigger-voltage of a basic p-n-p-n structure as a function of temperature. (b) Holding-current and holding-voltage of a basic p-n-p-n structure as a function of temperature.

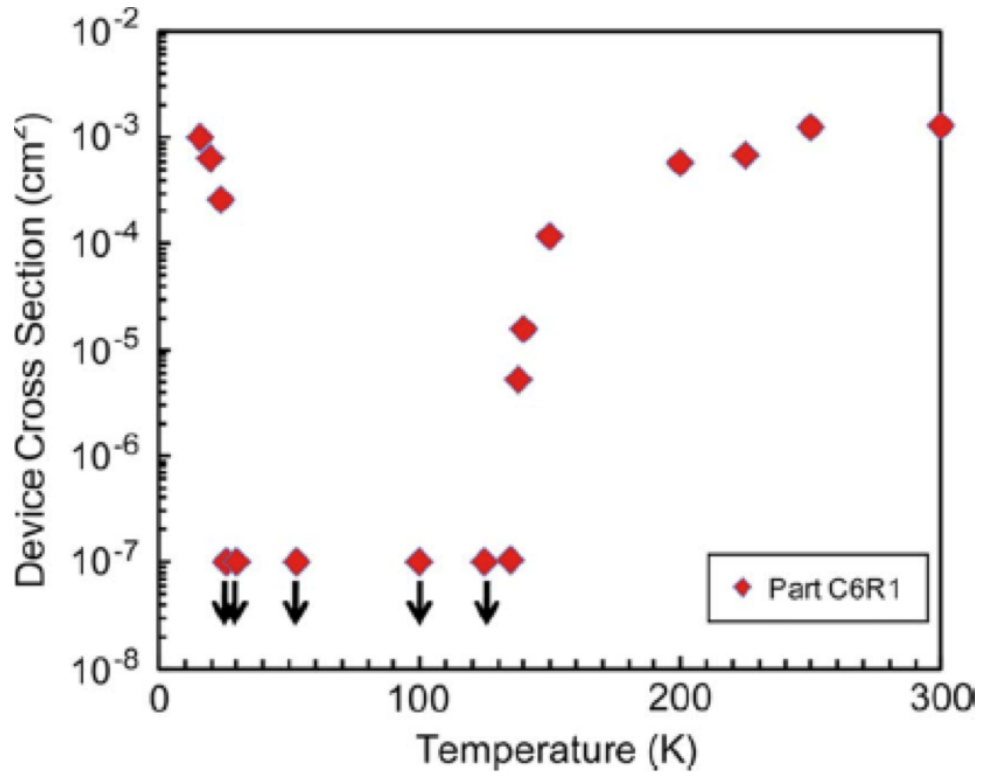
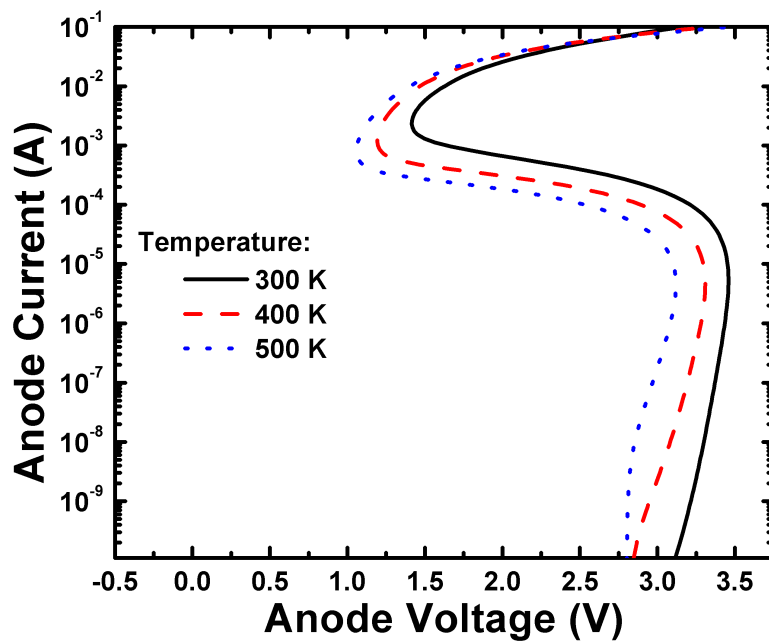


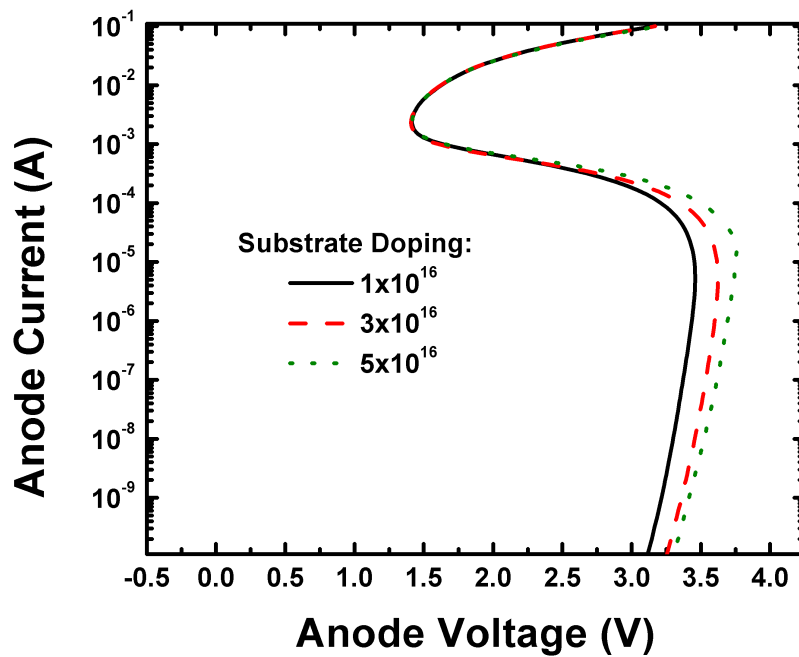
Figure 86: Device cross sections for hard SEL events versus temperature. All data was measured at 60° incidence using 15 MeV/u Kr with $LET_{eff} = 64.4$ and $R_p = 43$. The downward arrows indicate limiting cross sections [5].

6.8 TCAD Modeling of Latchup in CMOS Technologies

A p-n-p-n parasitic SCR structure was simulated in Synopsys Sentaurus tools. The doping profiles chosen are similar to a 130-nm technology node. A variety of physical mechanisms can be understood in the latch-up structure through TCAD simulations. Overshoot testing is performed on the latch-up structure. The TCAD simulations do not converge with a voltage overshoot sweep. Therefore, here we swept the current through the anode and measured the voltage at the anode. Simulations converge much easily with this approach. Figure 87(a) shows the anode current as a function of anode voltage for varying temperature (going from room temperature to 500 K). Simulation convergence is still much harder to achieve at temperatures below room temperature. The anode holding/trigger voltage and current decreases with increase temperature. Figure 87(b) shows the anode current as a function of anode voltage for varying substrate doping concentration. Increasing the substrate doping results in smaller substrate parasitic resistances, hence the trigger voltage and current increase with increasing substrate doping. Similar phenomenon is seen for increasing sub-collector doping (Figure 88(a)). Latch-up can also be prevented using deep trench (DT) isolation. Figure 88(b) shows the impact on the latch-up characteristics with increasing DT depth. Increasing DT results in smaller parasitic bipolar gain for the parasitic pnp and npn bipolar transistors. Hence the holding/trigger voltage and current increase with increasing DT depth. Figure 88(b) shows that the simulated structure becomes immune to latch-up at DT depth greater than $1\text{ }\mu\text{m}$.

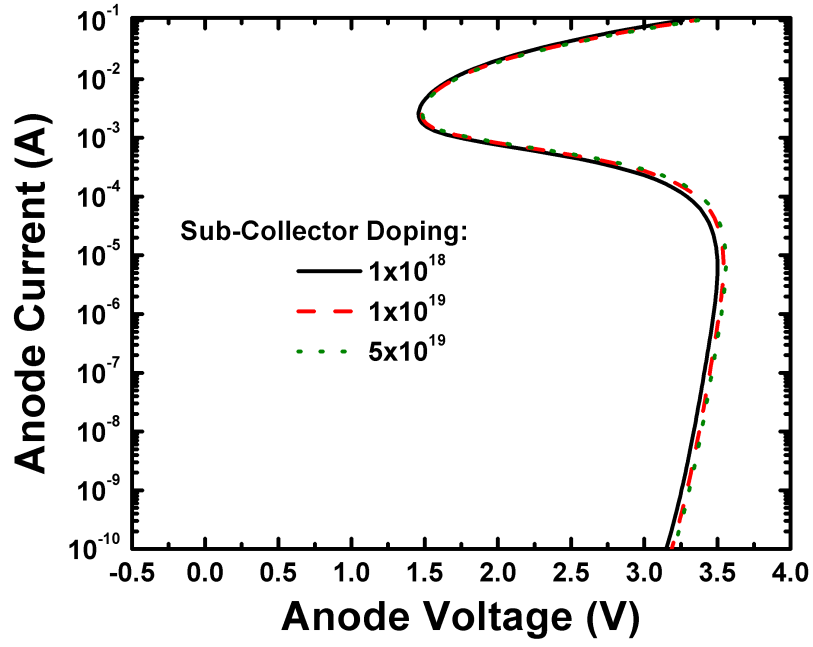


(a)

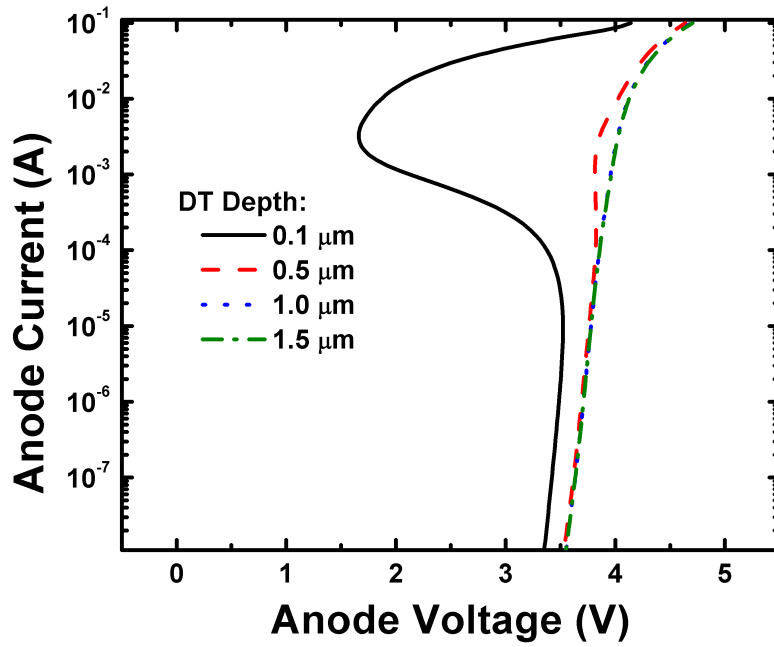


(b)

Figure 87: Anode current as a function of anode voltage for varying (a) temperature and (b) substrate doping.



(a)



(b)

Figure 88: Anode current as a function of anode voltage for varying (a) sub-collector doping and (b) deep trench (DT) depth.

6.9 Summary

Latchup phenomenon is shown to be possible below 100 K in 130-nm CMOS technology. Different latchup characterization and hardening techniques are discussed. Finally, a TCAD model for latchup is created, and impact of process variations on latchup characteristics are shown.

CHAPTER VII

USING TCAD TO MODEL MIXED-MODE DAMAGE IN SIGE HBTS

7.1 Overview

A time-dependent device degradation model has been developed in technology computer aided design (TCAD) to model reliability in CMOS and SiGe devices. The model can be used to develop time-dependent TCAD models for hot-carrier degradation induced threshold voltage shifts in MOSFETs, ionizing radiation induced STI leakage in MOSFETs, reverse-bias emitter-base stress induced base leakage current in bipolars, and mixed-mode stress induced base leakage current in bipolars.

7.2 Introduction

Silicon-germanium (SiGe) technology is used in a variety of mixed-signal circuit applications [75], [76]. Since SiGe HBTs possess larger breakdown voltages than MOSFETs at a fixed technology node and device performance, they are often preferred for large voltage swing applications. Under such conditions, the SiGe HBT can experience degradation because of the large electric-fields within the device, which can cause impact ionization, thereby producing highly energetic carriers (hot-carriers). The two degradation stress conditions typically encountered in SiGe HBTs are: a) reverse emitter-base (EB) bias-induced current-gain (β) degradation b) mixed-mode (high V + high I) stress-induced current gain degradation. Figure 89 shows the structure of a SiGe HBT showing interface trap formation at EB-spacer and STI edge after applied mixed-mode stress. A necessary part to predict reliability is to simulate the time dependence of interface trap generation. In this work we use TCAD to model

the mixed-mode stress condition in SiGe HBTs.

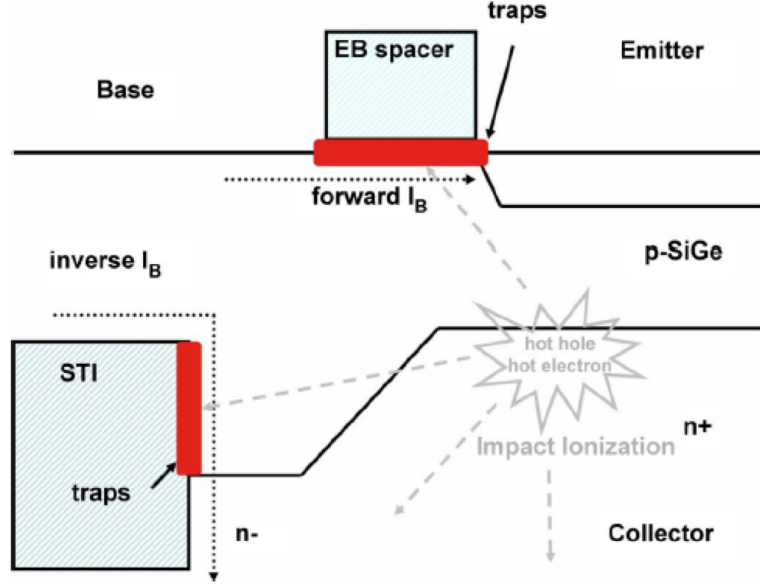


Figure 89: Cross section of a SiGe HBT showing the interface trap formation at the EB-spacer and STI interface with silicon during a mixed-mode stress condition [78].

Mixed-mode stress condition is defined as simultaneously applied voltage and current stress. The SiGe HBT is subjected to this stress condition in its on-state (forward-active mode). Therefore, it is a serious concern for several applications since the circuit performance can degrade over time when the HBT is in the on-state. Experimental reports of current gain degradation with mixed-mode stress condition have been reported previously [77]-[78]. In the present work, we present a TCAD model for the mixed-mode stress that helps understand the physical mechanisms underlying the degradation and allows the prediction of long-term reliability. For SiGe HBTs in particular, it is difficult to experimentally extract the interface trap density at the EB-spacer or STI edge, therefore, this model can be very useful. The proposed stress model does not add significantly to the TCAD simulation time and predicts reliability data for the device that would otherwise take days to measure directly. The model is based on the power-law interface trap formation model developed for MOSFET hot-carrier stress induced threshold voltage shifts [58]. We show that this

model can be applied to simulate the EB-spacer and/or shallow trench isolation (STI) induced leakage in a SiGe HBT. The model in its present form can also be used to simulate the off-state leakage current in MOSFETs.

7.3 Model for Interface Trap Formation due to Mixed-Mode Stress

The model is based on the disorder-induced variations among the Si-H activation energies at the passivated Si-SiO₂ interface, which lead to a sub-linear time dependence of the trap generation process [49] (Equation 6). Diffusion of hydrogen from the passivated interface was used to explain the observed time dependence. The activation energy of the bond-breaking process depends parametrically on the device electric-field and hot-carrier current (Equations 7-10). The main assumption about trap formation is that initially dangling silicon bonds at the Si-SiO₂ interface were passivated by hydrogen (H), and degradation is a depassivation process where hot-carrier interactions with Si-H bonds takes place. Empirically it has been shown that the time dependence of interface trap generation can be described by a simple power law expression:

$$N_{it} - N_{it}^0 = \frac{N_{hb}^0}{[1 + (vt)^{-\alpha}]} \quad (6)$$

where, N_{it}^0 is the initial interface trap density, N_{hb}^0 is the initial concentration of hydrogen bonds at the Si-SiO₂ interface, N_{it} is the final concentration of interface traps after stress, t is the stress time, the power α is stress dependent and varies between 0 and 1, v is a reaction constant defined by:

$$v = v_0 \exp\left(\frac{\epsilon_A^0}{kT_0} - \frac{\epsilon_A^0 + \Delta\epsilon_A}{\epsilon_T}\right) k_{FN} k_{HC} \quad (7)$$

$$\epsilon_A = \epsilon_A^0 + (1 + \beta)kT \ln\left(\frac{N - N_{hb}}{N - N_{hb}^0}\right) \quad (8)$$

$$\Delta\epsilon_A = -\delta_{\perp}|F_{\perp}|^{\rho_{\perp}} + (1 + \beta)\epsilon_T \ln\left(\frac{N - N_{hb}}{N - N_{hb}^0}\right) \quad (9)$$

$$\beta = \beta_0 + \beta_{\perp}F_{\perp} + \beta_{\parallel}F_{\parallel} \quad (10)$$

where, ϵ_A is the Si-H bond activation energy, F_{\perp} and F_{\parallel} are the perpendicular and parallel components of the electric-field F to the interface.

7.4 TCAD Modeling Damage in SiGe HBTs due to Mixed-Mode Stress

Using the above model, an initial interface trap concentration ($N_{IT} = 1 \times 10^{10} / \text{cm}^2$) was defined at the oxide-silicon interface and the time dependence of the generation of these interface traps was simulated. The traps were acceptor type at the middle of the band-gap. Every thing else in the device simulation model remains the same as for a calibrated TCAD model. Gummel characteristics were measured at different time intervals (similar to a stress-measure-stress measurement procedure).

One important question here is whether EB-spacer or STI edge contributes to the base-current leakage in a mixed-mode stress condition? Such a question can be answered through this kind of a model and simulation setup.

Figures 90 and 91 show the majority-carrier current density contours in the base region for traps at EB-spacer and STI edge respectively. Figure 90(a) shows the majority-carrier current density before stress and Figure 90(b) shows the majority-carrier current density after mixed-mode stress for the condition where traps were present only at EB-spacer to silicon edge. A mixed-mode stress of $V_{CE}=1.2 \times BV_{CEO}$ and $I_E=0.2 \times I_{PEAK}$ was applied to the device. A clear increase in majority-carrier current density (and hence base-current) is observed at the EB-spacer edge. Figure 91(a) shows the majority-carrier current density before stress and Figure 91(b) shows the majority-carrier current density after stress for the condition where traps were

present at the STI-silicon edge only. No significant change in the majority-carrier current density is observed in this case. However, the interface trap density increase is larger at the STI edge than the EB-spacer edge (Figure 92). The interface trap density is larger at the STI-silicon interface because the collector-current density flowing through this interface is much larger than the base-current density flowing through the EB-spacer to silicon interface. This larger collector-current density creates greater number of defect sites at the STI-silicon interface.

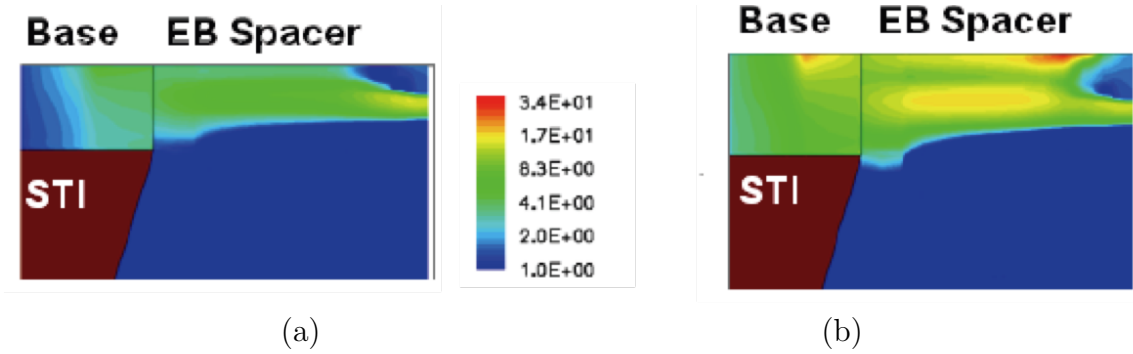


Figure 90: Majority-carrier current density (a) before stress (b) after stress, for traps only at the EB-spacer.

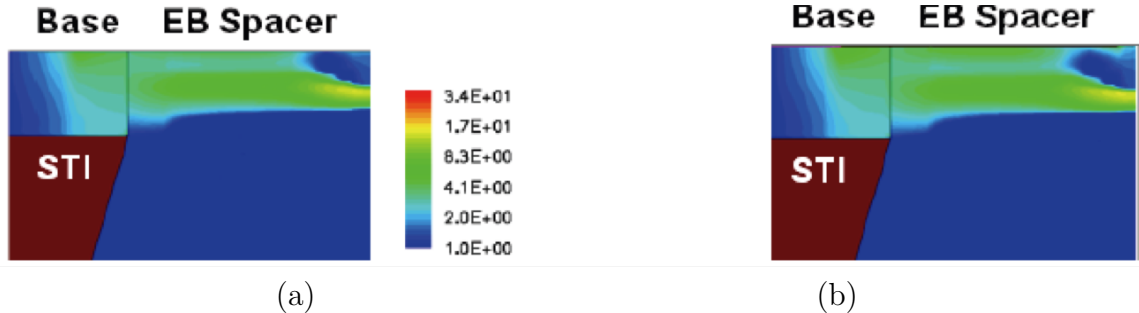


Figure 91: Majority-carrier current density (a) before stress (b) after stress, for traps only at the STI edge.

Therefore, a larger density of traps at the STI edge are not contributing to increase in the forward-mode base-current and only traps at EB-spacer seems to have the major effect. Figure 93(a) shows the Gummel characteristics for varying stress time for the device with traps only at the EB-spacer edge. An increase in base-current is observed as expected from the results in Figure 90. Figure 93(b) shows the Gummel

characteristics for varying stress time for the device with traps only at the STI edge. No significant increase in base-current is observed as expected from the results in Figure 91. Figure 94 shows the modeled DC current gain degradation for device with traps at EB-spacer. The excellent fit achieved with measured data shows that traps are generated at the EB-spacer to silicon edge during experiment. A larger doping at the EB-spacer edge can be used to prevent this current gain degradation.

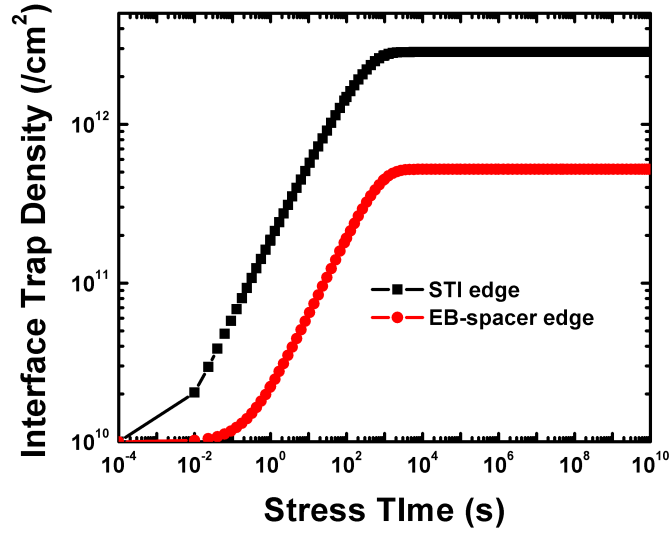
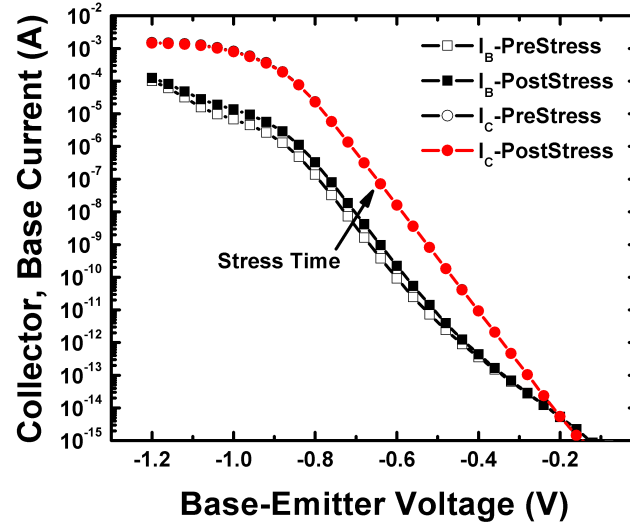
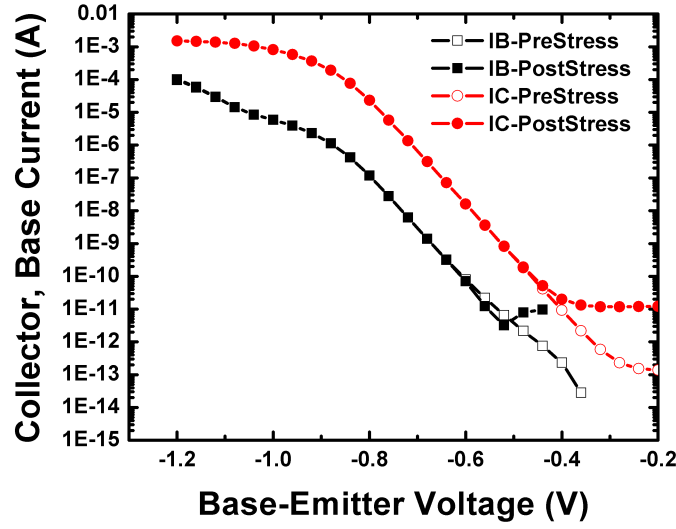


Figure 92: Interface trap density as a function of stress time for STI and EB-spacer oxides.

A time-dependent degradation power law has been used to model the mixed-mode stress induced damage in a SiGe HBT. Such a model can predict device lifetime and help at the device modeling stage to improve reliability. Also, the reliability measurements are long and tedious, therefore, such a model is very useful for foundries to use during technology development phase to save on measurement resources.



(a)



(b)

Figure 93: (a) Collector- and base- current as a function of base-emitter voltage for traps at EB-spacer oxides. (b) Collector- and base- current as a function of base-emitter voltage for traps at STI oxides.

7.5 Summary

A TCAD model for mixed-mode stress phenomenon in SiGe HBTs is demonstrated. The model matches beta degradation under mixed-mode stress for a 250-nm SiGe

technology.

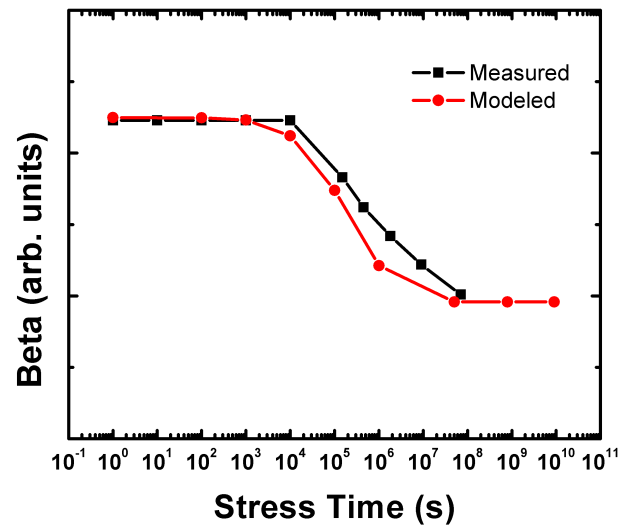


Figure 94: Measured and modeled DC current gain (Beta) as a function of stress time.

CHAPTER VIII

TOTAL-DOSE TOLERANCE OF 32-NM CMOS ON SOI AND THE IMPACT OF TECHNOLOGY SCALING ON NFET RELIABILITY

8.1 *Overview*

The total-dose radiation tolerance and hot-carrier reliability of 32-nm CMOS-on-SOI technology is reported for the first time. The impact of HfO_2 based gate dielectric on the performance and reliability is studied. Also, the impact of technology scaling from 65-nm to 32-nm on the performance and reliability of CMOS technologies is studied.

The contents of this chapter have been published in part at [6].

8.2 *Introduction*

In the present chapter, we investigate for the first time the total-dose tolerance of 32-nm MOSFETs within an RF-CMOS on SOI platform. Notably, we find significant electron trapping in the high-k gate dielectric for nFET devices irradiated under positive bias, which is not observed in previous generations of technology. Threshold voltage shifts are observed under positive bias, and hot-carrier stressing in high-k gate stacks. Greater charge trapping is observed at positive voltage stressing in HfO_2 as compared to SiO_2 -based gate dielectrics [83]-[85].

The impact of technology scaling on the radiation tolerance and device reliability is an important question too. It is believed that with technology scaling the MOSFET reliability degrades. However, the structural and materials changes in the scaled technologies complicate the reliability response. The impact of technology scaling (from 65-nm to 32-nm) on the total-dose and hot-carrier reliability response is reported

here through experimental data, and an explanation for the observed data trends is provided through qualitative TCAD simulations.

8.3 Device Technology and Experimental Details

The process details of this 32-nm RF-CMOS technology have been published previously [86]. A TEM cross-section of a 32-nm nFET is shown in Figure 95 [86]. This technology features high-k dielectric, (HfO_2)-based gate oxide and a thin metal gate electrode capped with polycrystalline silicon. Hafnium has a high dielectric constant ($\epsilon \sim 20-25$), and also has an adequate bandgap ($>5\text{eV}$) and band offsets with silicon ($>1\text{eV}$). A schematic energy-band diagram of the gate oxide to silicon interface is shown in Figure 96. The HfO_2 - SiO_2 interface has a high density of interface defects. The bulk of the HfO_2 layer also has a high density of bulk oxide traps. The strained-silicon components of this technology include an embedded SiGe source/drain in the pFETs and dual stress liners (DSL) for the nFET. The pFET drive current was improved using a higher Ge percentage in the source/drains, and additional improvements in the nFETs were added in the strained SiN liners. This technology allows up to 11 levels of copper metallization. Floating-body, partially-depleted, and various body-contacting device options are available within this platform. In general, floating-body devices have improved RF performance compared with body-contacted devices. However, body-contacted devices exhibit better reliability, forcing a trade-off between performance and reliability. The devices used were laid out in single gate finger arrangements, similar to what is used in digital design. Radiation experiments were performed using an ARACOR 10-keV X-ray source, at a dose rate of $31.5 \text{ krad}(SiO_2)/\text{min}$. As described below, the devices were biased at various constant voltage conditions during the radiation exposure, some of which represented worst-case conditions. No significant hysteresis was observed in the device characteristics.

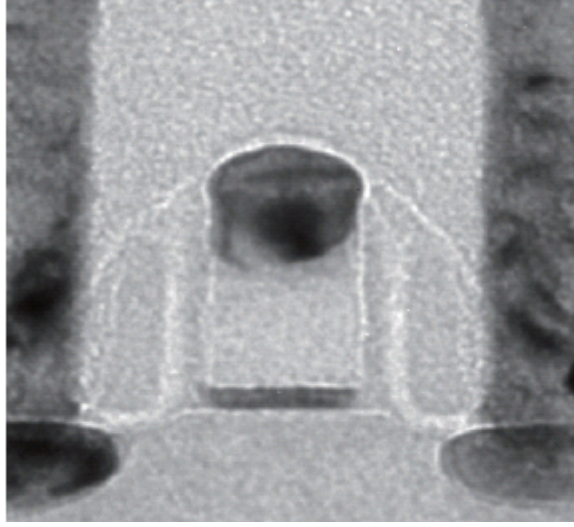


Figure 95: TEM cross-section of a 32-nm CMOS device (after [86]).

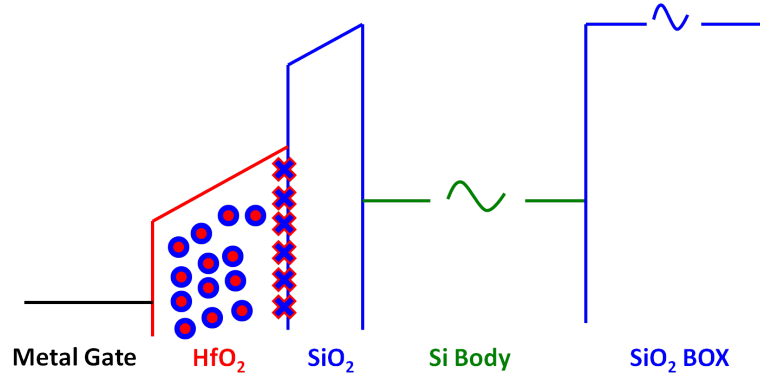


Figure 96: Schematic energy band diagram of the gate-stack of a 32-nm SOI CMOS device.

8.4 Total-Dose Tolerance of 32-nm CMOS-on-SOI Technology

8.4.1 Gate-Only Bias During Total-Dose Radiation (Worst Case)

The transfer characteristics of a 32-nm nFET at various total-doses are shown in Figure 97. The gate was biased at +1.0 V and all other terminals were grounded during radiation (i.e., worst case). The off-state leakage current increases significantly as a result of radiation. In this stress condition, the major degradation mechanism is hole trapping in the shallow trench isolation (STI), which results in off-state leakage current between source and drain. In addition, a positive shift in the threshold voltage

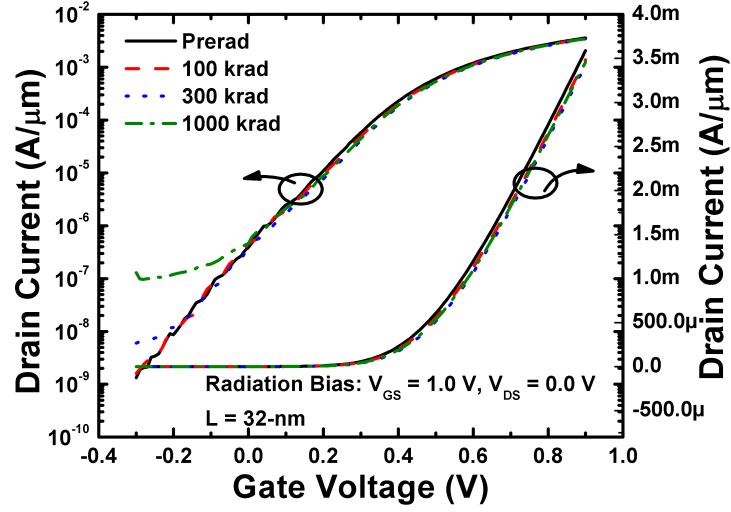


Figure 97: Transfer characteristics of the nFET as a function of radiation dose ($L = 32$ nm, $W = 0.325$ μm).

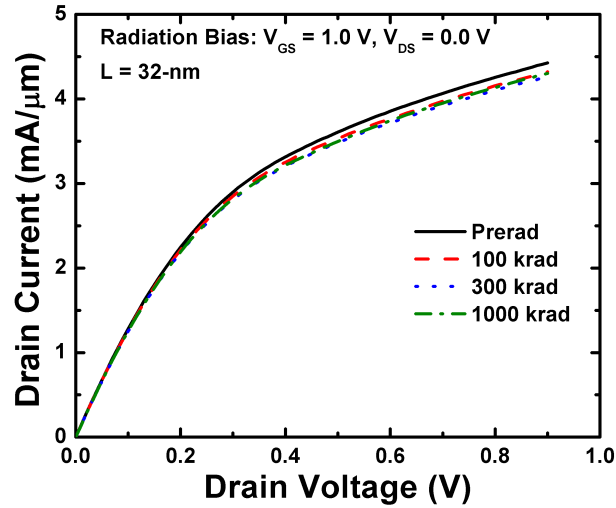


Figure 98: Output characteristics of the nFET as a function of radiation dose ($L = 32$ nm, $W = 0.325$ μm).

is observed with radiation, as shown in Figure 97. The positive shift represents electron trapping in pre-existing traps in HfO_2 [84], [85]. The electron injection from the Si dominates, as compared to the hole injection from the metal under positive gate bias due to lower conduction band offsets on the oxide/Si interface vs. the metal/oxide interface (Figure 96).

The increasing threshold voltage also results in decreased on-state current, as shown in the output characteristics (Figure 98). No significant change in output resistance is observed. Longer-channel length devices, however, do not show an increase in off-state leakage current with radiation (Figure 99), although a significant increase in threshold voltage due to electron traps is observed. The larger change in threshold voltage for the longer channel length device is due to the greater electron trapping in the thicker gate oxides. In addition, a significant decrease in on-state current is seen (Figures 100, 101). The transconductance characteristics show the decreased on-state current in the longer length devices is also due to mobility degradation (Figure 101). A plot of the on-off current ratio (an important figure-of-merit of a digital CMOS device) of the nFETs with varying channel length is shown in Figure 102. The smallest length (32-nm) nFETs show the maximum degradation in on-off current ratio with total-dose. This is due to the increasing off-state leakage current with radiation. The hot-carrier degradation of the nFETs with varying channel length is shown in Figure 103. The smallest channel length transistor shows the maximum shift in threshold voltage with increasing stress time. In short channel length technologies the maximum body/substrate current is observed at $V_{GS} = V_{DD}$ (Figure 104). Therefore, $V_{GS} = V_{DD}$ condition was chosen for worst case degradation in the hot-carrier experiments. The transfer characteristics of a pFET after radiation are shown in Figure 105. Significant hole trapping in the gate oxide is observed, however, resulting in an increase in the magnitude of the threshold voltage.

8.4.2 Combined Gate and Drain Bias During Total-Dose Radiation (Device On)

The transfer characteristics of a 32-nm nFET at various total-doses are shown in Figure 106. The gate and drain were biased at 1.0 V and 1.0 V, respectively, during radiation. This bias condition corresponds to worst case for hot-carrier stress. A positive threshold voltage shift is observed, which corresponds to electron trapping

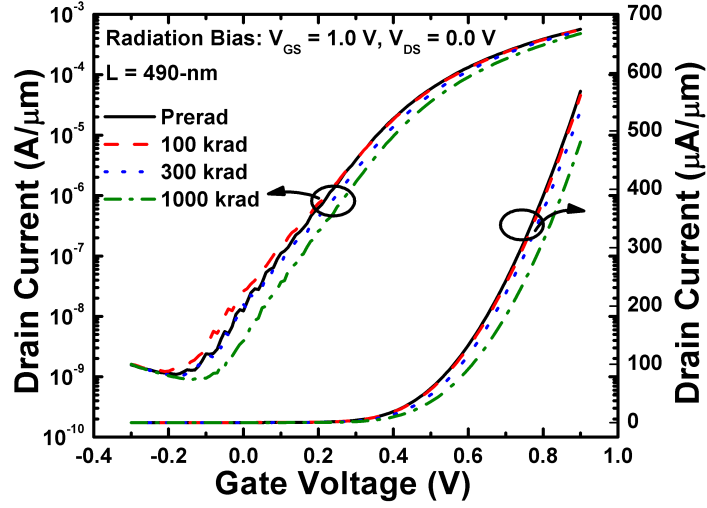


Figure 99: Transfer characteristics of the nFET as a function of radiation dose ($L = 490$ nm, $W = 0.325$ μm).

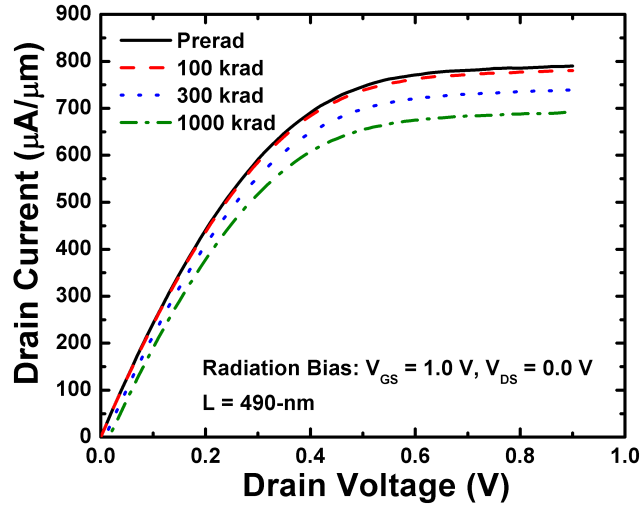


Figure 100: Output characteristics of the nFET as a function of radiation dose ($L = 490$ nm, $W = 0.325$ μm).

in the gate oxide. The electron trapping is a result of hot-carrier stress and the gate-bias induced electron tunneling into the gate oxide. In addition, an increase in off-state leakage current is observed. The leakage current increase saturates above 300 krad(SiO_2). The increasing off-state leakage current can be attributed to the hole traps in the shallow trench isolation (STI) oxide. The increase in off-state leakage

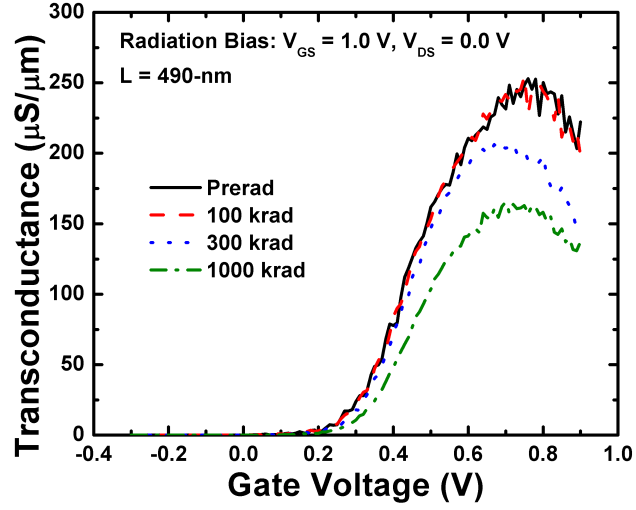


Figure 101: Transconductance characteristics of the nFET as a function of radiation dose ($L = 490$ nm, $W = 0.325$ μm).

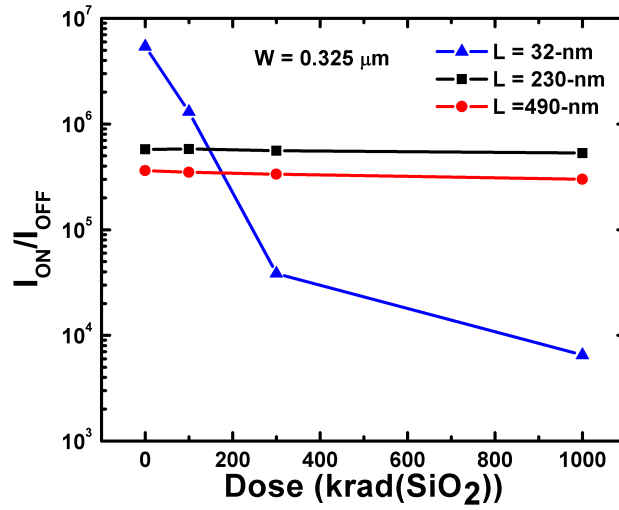


Figure 102: On-Off current ratio of the nFETs with varying channel length as a function of radiation dose.

current with radiation is smaller in the hot-carrier stress condition. This can be attributed to a smaller density of hole traps in the STI.

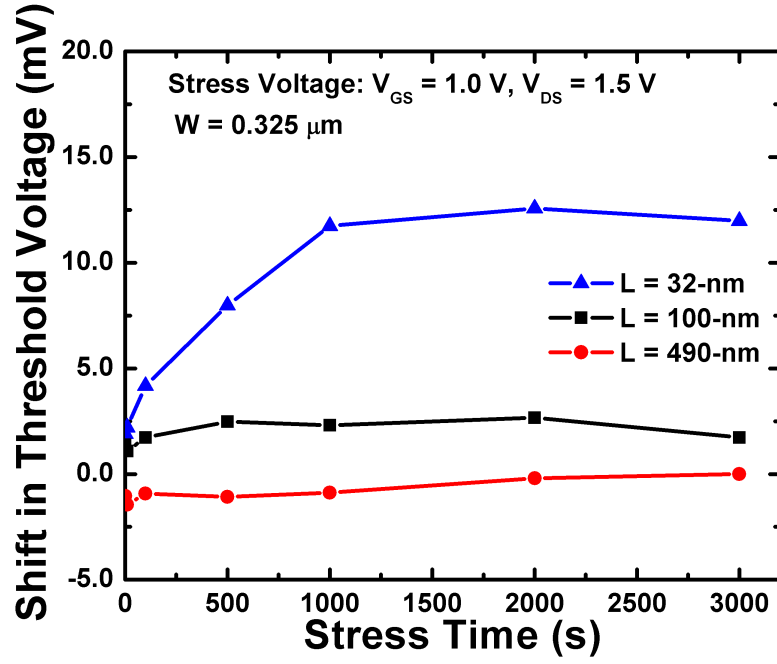


Figure 103: Hot-carrier degradation induced shift in threshold voltage as a function of stress time for transistors of different channel length in the 32-nm technology.

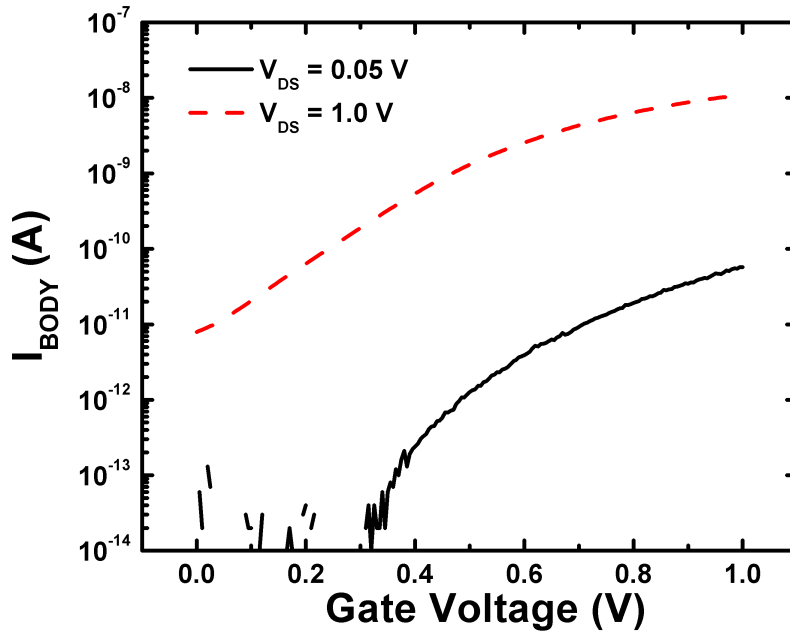


Figure 104: Body current as a function of gate voltage for the body-contact device with varying drain voltage.

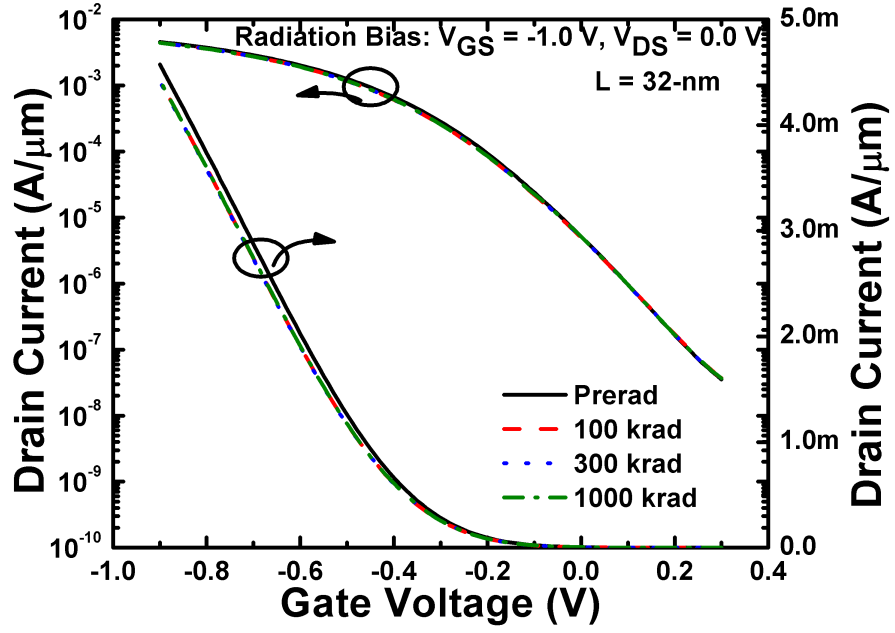


Figure 105: Transfer characteristics of the pFET as a function of radiation dose ($L=32$ nm, $W = 0.425$ μm).

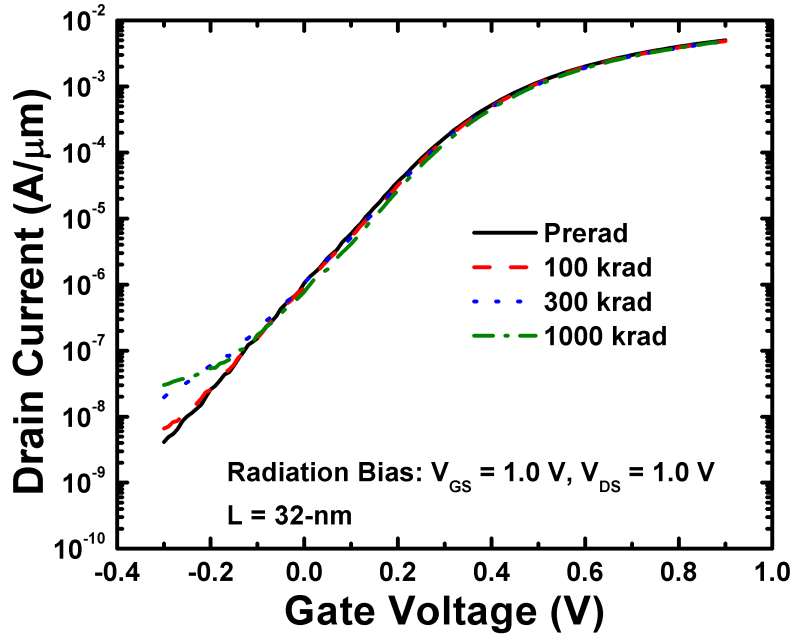


Figure 106: Transfer characteristics of the nFET as a function of radiation dose ($L=32$ nm, $W = 0.325$ μm).

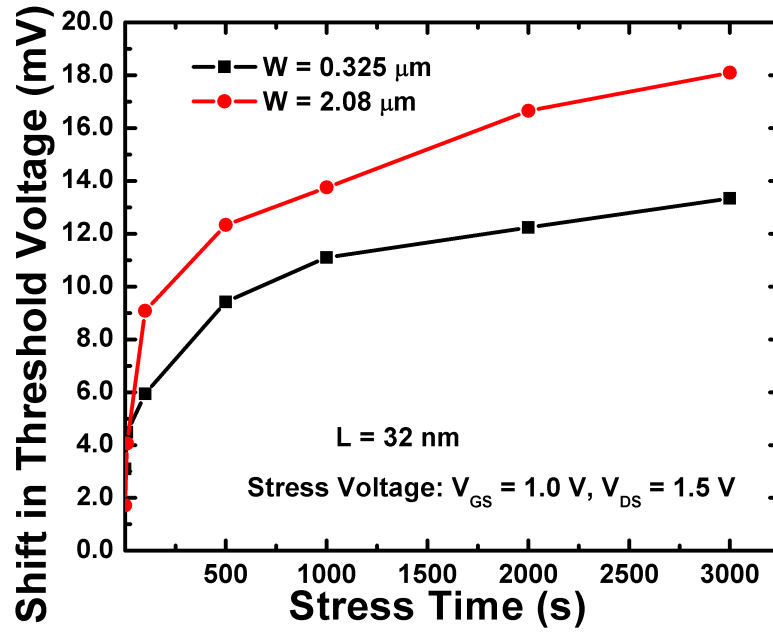


Figure 107: Shift in threshold voltage as a function of hot-carrier stress time for the nFETs with varying device width.

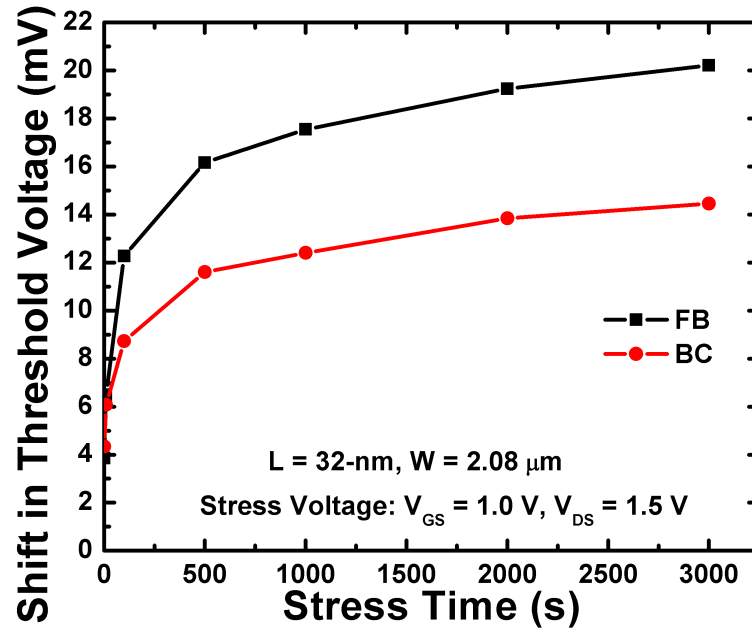


Figure 108: Shift in threshold voltage as a function of hot-carrier stress time for the floating-body (FB) and body-contacted (BC) nFETs.

8.5 Effect of Device Finger Width and Body-Contact on the Reliability of 32-nm nFETs

Figure 107 shows the shift in threshold voltage as a function of hot-carrier stress time for nFETs with varying finger width. Positive threshold voltage shifts due to electron traps are observed, as expected. Increasing finger width results in enhanced threshold voltage shifts (and mobility degradation). A similar trend is also observed in 45-nm nFETs (Figure 53(a)) [3]. In longer channel length nFETs ($L > 90$ -nm), it has been reported that larger longitudinal compressive stress (along the width) in the narrow width device channel region (due to STI) results in greater degradation [52]-[54]. However, in the strained-Si devices enhanced mechanical stress caused by the over-layers on the gate electrode plays a greater role, in determining the hot-carrier reliability of single finger DC devices [55]. Figure 108 shows the impact of body-contact on the hot-carrier response of 32-nm nFETs. Floating-body nFETs have a greater change in threshold voltage than body-contacted devices. The same trend has also been reported for 45-nm nFETs [1], [2]. Larger impact ionization in the channel region for floating-body nFETs results in greater degradation [2]. The larger impact ionization for floating-body nFETs despite a smaller electric field is because of the smaller mean free path of the carriers.

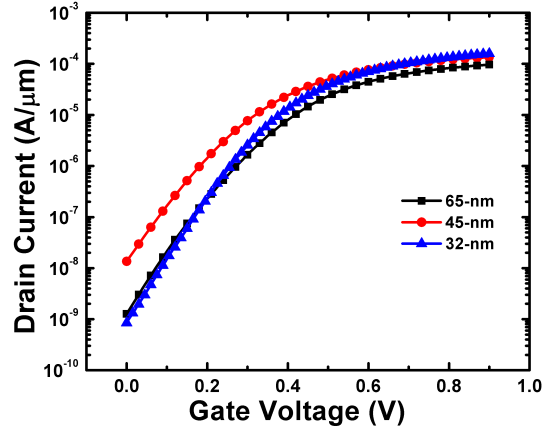
8.6 Impact of Technology Scaling on Performance, Hot-Carrier and Total-Dose Response

65-nm, 45-nm and 32-nm CMOS-on-SOI technologies are investigated here. The process of details of the 65-nm technology has been published previously [27], [87]. The 65-nm technology features nFETs with 340 GHz peak f_T and pFETs with 240 GHz peak f_T . The technology features 35-nm L_{poly} , dual stress nitride layers, and embedded SiGe-enhanced pFET, and stress memorization techniques. The technology features 10 metallization levels. The total-dose radiation response of the 65-nm

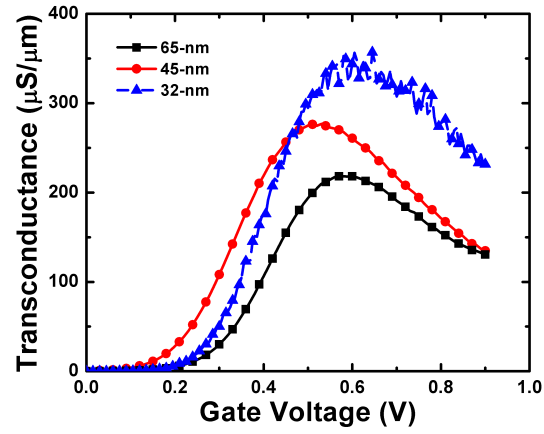
technology has been studied [81]. The process details of the 45-nm CMOS technology has been published [25]-[26]. The 45-nm CMOS technology features 1.16-nm gate oxide, dual stress liners, embedded SiGe pFETs, advanced activation annealing, and stress memorization techniques. The technology features 29-nm L_{poly} nFETs and 31-nm L_{poly} pFETs with 485 GHz and 345 GHz peak f_T , respectively. The total-dose radiation tolerance of 45-nm CMOS technology has been studied [3].

Figure 109(a) shows the transfer characteristics of the FB nFETs from the 65-nm, 45-nm, and 32-nm technologies. The transistors from the three technologies have the same device width for a fair comparison. An increase in on-state current can be observed with transistor scaling, as expected. The sub-threshold slope of 32-nm nFETs is also significantly improved compared to 65-nm and 45-nm nFETs (thanks to the high-k gate oxide). Figure 109(b) shows the transconductance as a function of gate voltage for the three transistors. Figure 109(c) shows the gate current as a function of gate voltage for the three transistors. An increase in gate current is observed with scaling from 65-nm to 45-nm. This can be attributed to a reduced gate oxide thickness for 45-nm nFET. However, the use of a thicker high-k HfO_2 results in much smaller gate current at 32-nm technology node.

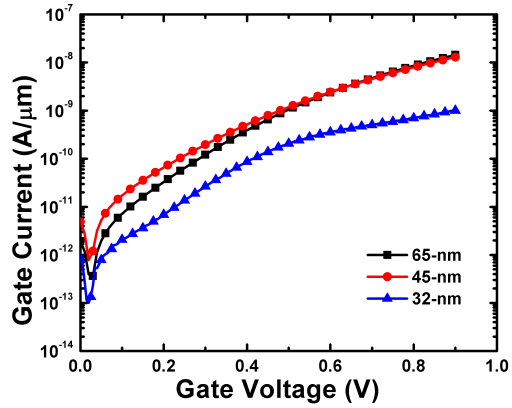
The impact of technology scaling on the radiation induced on-off current ratio degradation of nFETs is shown in Figure 110. The transistors were all irradiated at the same bias condition ($V_{GS} = 1.0$ V, $V_{DS} = 1.5$ V). First of all, the pre-radiation on-off current ratio follows the scaling trend, as expected. A decrease in on-off current ratio is observed with radiation bias because of increasing off-state leakage current and decreasing on-state current. The 65-nm technology shows very small degradation in on-off current ratio with radiation. The 32-nm technology has better radiation tolerance than the 45-nm technology. The transistors were also tested for hot-carrier degradation. The hot-carrier degradation increases with technology scaling (Figure 111).



(a)



(b)



(c)

Figure 109: Measured (a) drain current as a function of gate voltage, (b) transconductance as a function of gate voltage, and (c) gate current as a function of gate voltage for the smallest channel length devices from 65-, 45- and 32- nm technologies.

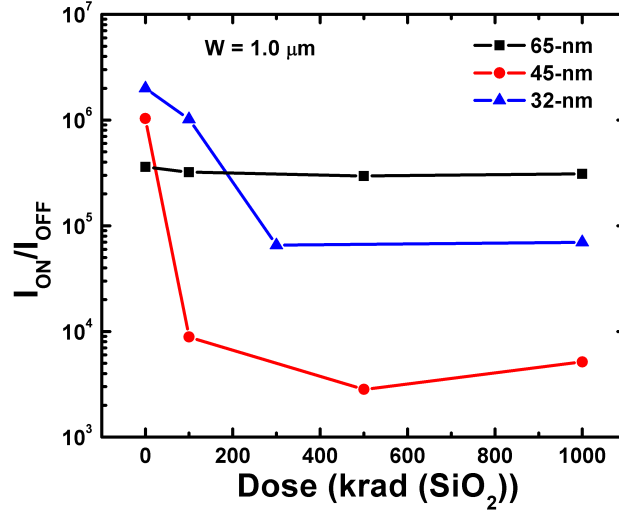


Figure 110: On-Off current ratio as a function of radiation dose for the three technology nFETs.

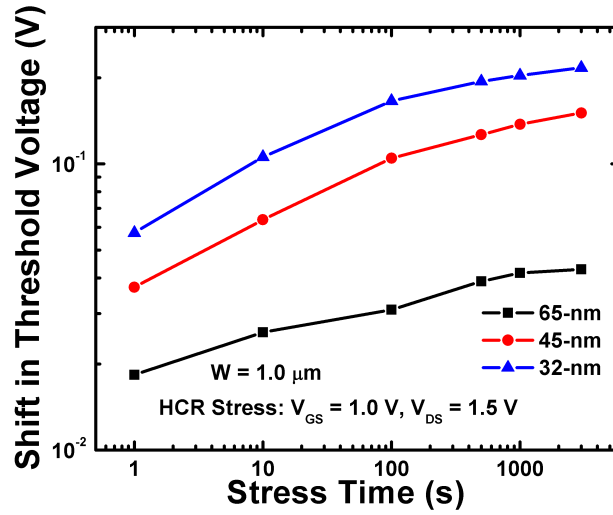


Figure 111: Shift in threshold voltage as a function of hot-carrier stress time for the three technology nFETs.

TCAD models were developed for 65-, 45-, and 32-nm nFETs with estimated doping profiles. Hydrodynamic models were used for the simulations. Figure 112 shows the electric field in the gate oxide along the channel region. Going from 65-nm to 45-nm the gate oxide is scaled from ~ 1.4 -nm to ~ 1.1 -nm. Hence, an increase in electric field is observed across the gate oxide for the same gate bias. However,

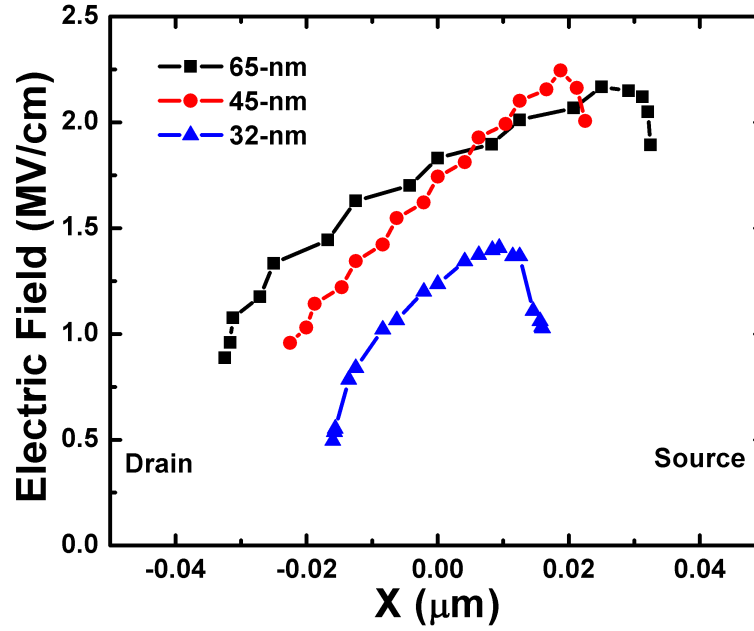


Figure 112: Electric field in the gate oxide for the three technology nFETs.

the gate oxide thickness for 32-nm is ~ 1.6 -nm (thanks to high-k HfO_2). Therefore, the electric field is much smaller for 32-nm nFETs. However, the impact ionization in the channel region keeps increasing with technology scaling from 65-nm to 32-nm because of increasing substrate and source/drain doping concentration (Figure 113). Therefore, an interplay of electric field across the gate oxide and impact ionization in the channel region decides the reliability of these technologies. 45-nm nFETs have large electric-field in the gate oxide and impact ionization in the channel region, hence the worse total-dose degradation. 32-nm nFETs have a smaller electric field in the gate oxide but a larger impact ionization in the channel region, hence an improved radiation response but worse hot-carrier degradation compared to 45-nm nFETs. 65-nm nFETs have a smaller electric field in the gate oxide and impact ionization in the channel region, and hence the best radiation and hot-carrier reliability.

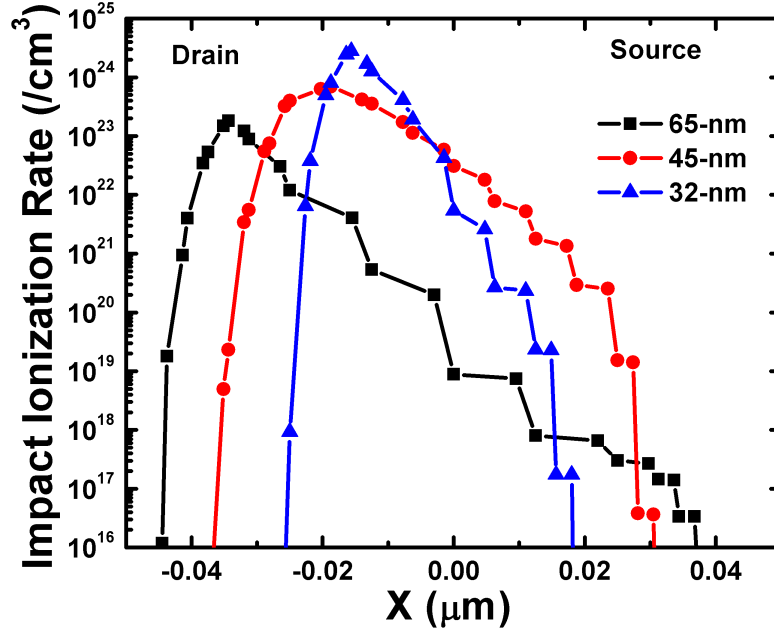


Figure 113: Impact ionization in the channel region for the three technology nFETs.

8.7 Summary

The total-dose tolerance of 32-nm RF-CMOS on SOI is investigated. Significant increase in off-state leakage current is observed for the 32-nm nFETs. Electrons are trapped in the high-k dielectric under positive radiation bias, resulting in increasing threshold voltage. The 32-nm pFETs capture holes during negative-bias radiation. Also, the impact of technology scaling (from 65-nm to 32-nm) on the total-dose tolerance and hot-carrier reliability is investigated through experimental data and TCAD simulations. The 32-nm nFETs have less total-dose degradation but worse hot-carrier degradation compared to 45-nm CMOS. An interplay of electric-field in the gate oxide and impact ionization in the channel region is responsible for the degradation mechanisms in the three technologies.

CHAPTER IX

CRYOGENIC PERFORMANCE OF SHORT-CHANNEL SOI CMOS TECHNOLOGIES

9.1 *Overview*

Cryogenic performance and reliability of 45-nm nFETs is investigated. The RF performance increases significantly at 77 K. The hot-carrier device reliability is shown to improve at low temperatures in short-channel CMOS technologies.

9.2 *Introduction*

Silicon mobility increases with decreasing temperature from 300 K to 77 K (-196 C) by a factor of 4 to 6 because of the reduced carrier scattering [88]. Thus, the CMOS/SiGe device on-state current, transconductance, f_T , f_{MAX} , etc. improve with decreasing temperature. The objective of this research is to explore these improvements in CMOS parameters going down to 4 K temperature. Also in long-channel length technologies (larger than $0.5 \mu m$) it has been shown that the CMOS device has worse hot-carrier reliability at low-temperatures [89]-[91]. This is believed to be because of the increased carrier mobility at low-temperatures, and the fact that the carriers travel farther before colliding with the silicon lattice. However, for sub 100-nm technologies (reduced V_{DD}), the temperature dependence is reversed. Carriers with sufficient energy for impact ionization lie only in the tail of the energy distribution. When the temperature is lowered, the number of carriers with enough energy for impact ionization decreases. This reduces I_{SUB} and hot-carrier degradation. Direct tunneling gate oxide leakage shows very weak temperature dependence, suggesting that cooled operation has a negligible impact on gate oxide reliability. The hot-carrier reliability of

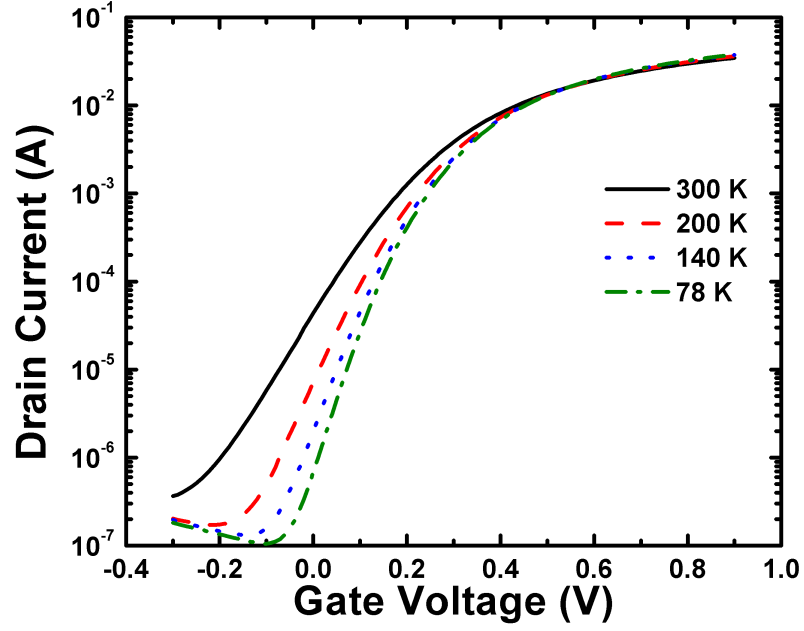
short-channel CMOS technologies (45-nm, 65-nm) is studied here at low-temperatures. This research shows that the short-channel CMOS reliability is non-classical at room temperature. The results of this study are very useful for future lunar missions where such technologies will be used in extreme conditions, such as 77 K operation.

9.3 Results and Discussion

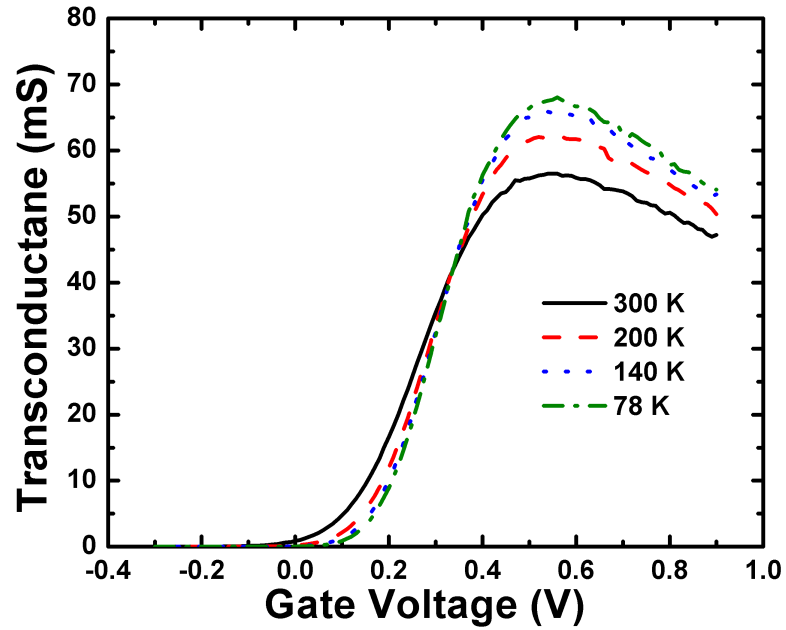
nFETs from the 45-nm CMOS-on-SOI technology were measured across temperature. Figure 114 shows the drain current and transconductance as a function of gate voltage for varying temperature (going down to 77 K). The threshold voltage increases with decreasing temperature and the on-state current increases.

Figure 115(a) shows the AC current gain of a 45-nm floating-body device at 300 K and 77 K. An increase in current gain is observed at cryogenic temperatures. Figure 115(b) shows the extracted cut-off frequency (f_T) at varying temperature. These are record high f_T numbers at cryogenic temperatures. The 45-nm floating-body SOI nFETs were tested for hot-carrier reliability at room-temperature and cryogenic temperatures. Conventionally, for longer channel length nFETs it has been shown that the hot-carrier reliability degrades at cryogenic temperatures. However, there is no report on HCR of scaled CMOS technologies at cryogenic temperatures. Figures 116(a) and 116(b) shows the transfer characteristics of a 45-nm floating-body nFET for varying stress time at room-temperature and 80 K, respectively. Figure 117 shows the hot-carrier degradation induced shift in threshold voltage as a function of stress time for 45-nm nFETs at 373 K (100 C), 300 K (room-T), and 77 K respectively. In the 45-nm technology we observe that the hot-carrier degradation reduces at lower temperatures.

Similar results were also reported for technologies from 0.35 μm to 45-nm [92].

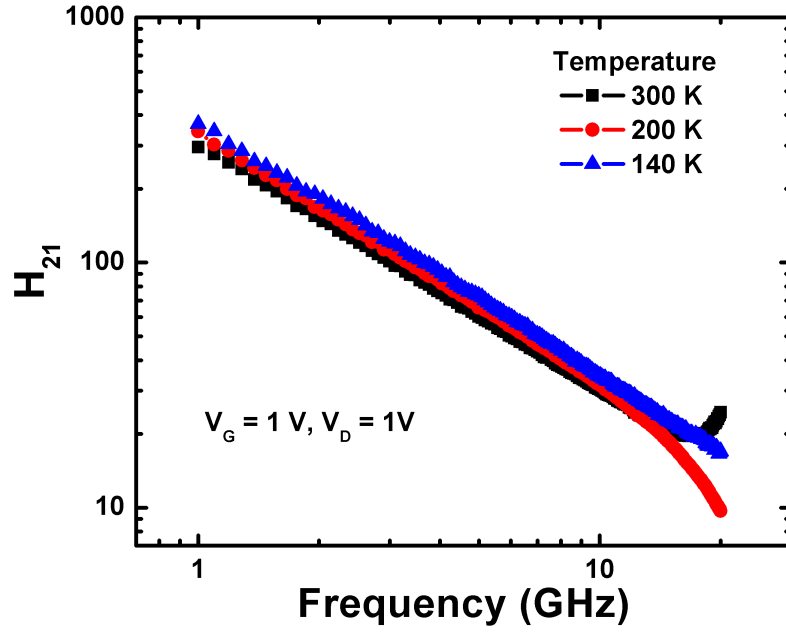


(a)

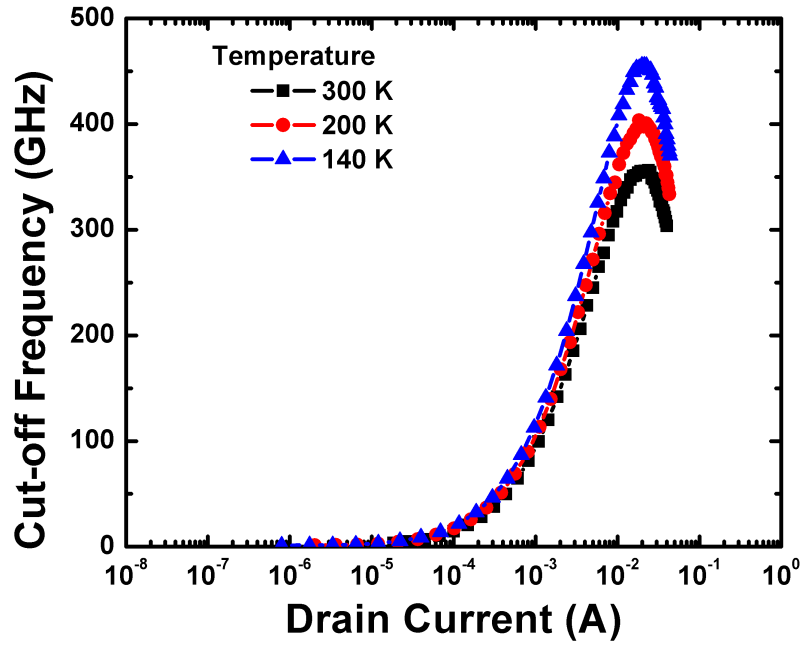


(b)

Figure 114: (a) Drain current as a function of gate voltage of a 45-nm floating-body SOI CMOS device for varying temperature. (b) Transconductance as a function of gate voltage of a 45-nm floating-body SOI CMOS device for varying temperature.

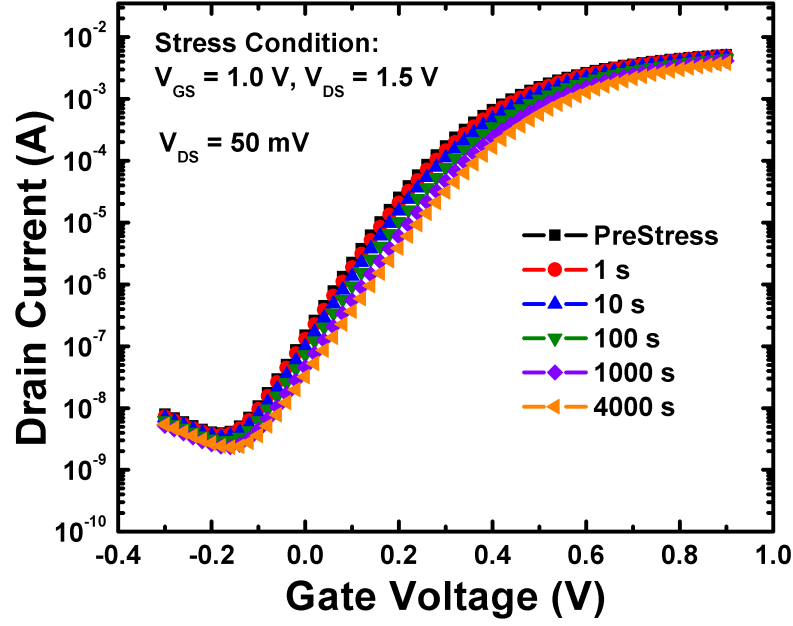


(a)

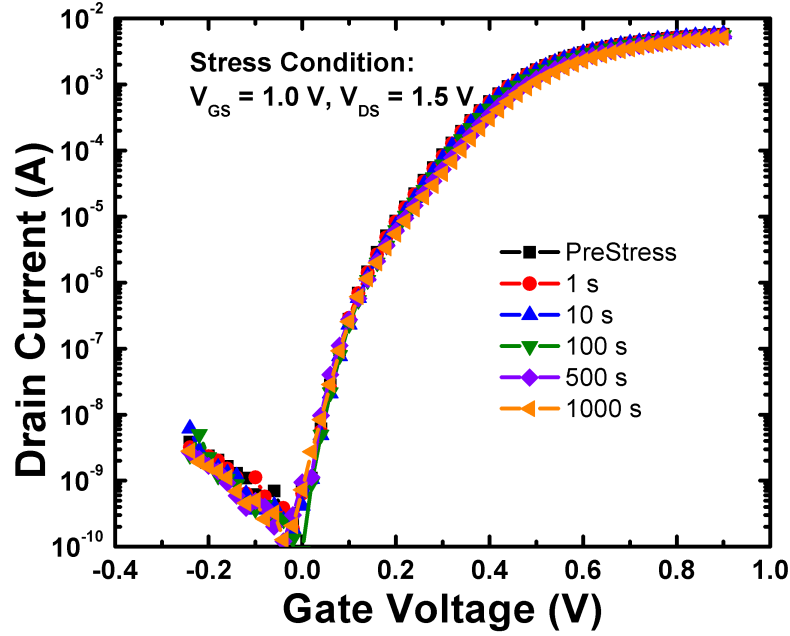


(b)

Figure 115: (a) AC Current gain (H_{21}) as a function of frequency of a 45-nm floating-body SOI CMOS device at 300 K and 80 K. (b) Cut-off frequency as a function of gate voltage of a 45-nm floating-body SOI CMOS device at 300 K and 80 K.



(a)



(b)

Figure 116: (a) Transfer characteristics of a 45-nm floating-body SOI CMOS device for increasing stress time (at $V_{GS}=1.0$ V and $V_{DS}=1.5$ V) at 300 K. (b) Transfer characteristics of a 45-nm floating-body SOI CMOS device for increasing stress time (at $V_{GS}=1.0$ V and $V_{DS}=1.5$ V) at 80 K.

9.4 Summary

Cryogenic performance of 45-nm nFETs is demonstrated. Record RF performance is achieved at cryogenic temperatures. The hot-carrier reliability of short-channel nFETs is shown to improve at cryogenic temperatures.

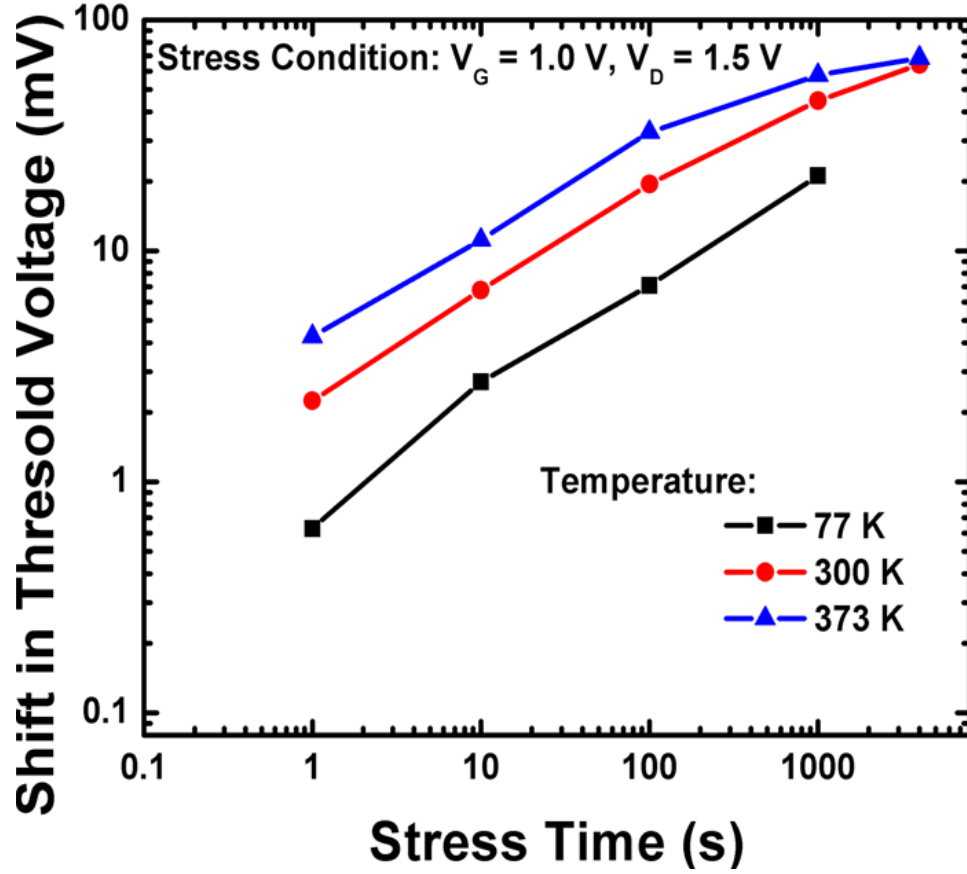


Figure 117: Shift in threshold voltage as a function of stress time of a 45-nm floating-body SOI nFET for varying temperature.

CHAPTER X

CONCLUSIONS AND FUTURE WORK

10.1 Conclusions

This dissertation tries to develop an understanding of different reliability mechanisms and the trade-offs between performance and reliability in sub 100-nm CMOS technologies. In this direction, several performance-reliability trade-offs studies have been carried out (Figure 118). Such trade-offs are used to demonstrate high performance reliable circuits. The major contributions of this research are summarized as follows:

1) The role of floating-body effects on the performance and reliability of sub-100 nm CMOS-on-SOI technologies is discussed [1], [2]. It is demonstrated through experimental data and TCAD simulations that floating-body devices have improved RF performance but worse reliability compared to body-contacted devices. Further, the floating-body effects in cascode cores is studied. Cascode cores are demonstrated to achieve much larger reliability lifetime than a single device. A variety of cascode topologies are studied to understand the trade-offs between performance and reliability for high-power applications [2].

2) The use of body-contact to modulate the performance of devices and single-pole-double-throw (SPDT) switches is demonstrated. The SPDT switch performance is shown to improve with a negative body-bias.

3) The impact of device width on the RF performance and reliability in sub 100-nm CMOS is demonstrated. Larger width devices are shown to have greater degradation,

posing challenging questions for RF design in strained-Si technologies [3].

4) A novel device phenomenon involving the impact of source/drain metal contact spacing and gate-finger to gate-finger spacing on the device RF performance is demonstrated. Further, the impact of above on the hot-carrier, RF stress, and total-dose radiation tolerance is studied [3], [4].

5) The latchup phenomenon in CMOS technologies is shown to be possible at cryogenic temperatures (below 50 K), and its consequences are discussed [5]. The results of this section are crucial for latchup hardness of circuits operating in extreme conditions.

6) A time-dependent device degradation model is developed in technology computer aided design (TCAD) to model reliability in CMOS and SiGe devices for the first time. Mixed-mode and reverse EB-bias stress in a SiGe technology is modeled.

7) The total-dose irradiation tolerance and hot-carrier reliability of 32-nm CMOS-on-SOI technology is demonstrated. The impact of HfO_2 based gate dielectric on the performance and reliability is studied [6].

8) The impact of technology scaling from 65-nm to 32-nm on the performance and reliability of CMOS technologies is studied [6]. The hot-carrier degradation increases with technology scaling from 65-nm to 32-nm. This is attributed to increasing impact ionization induced electron trapping in the gate oxide. However, the total-dose response is more complicated. 45-nm nFETs are shown to have the largest total-dose degradation [6].

9) The cryogenic performance and cryogenic hot-carrier reliability of 45-nm CMOS-on-SOI technology is demonstrated. Record RF performance is demonstrated at cryogenic temperatures. The MOSFET reliability is shown to improve at cryogenic temperatures.

	Performance	Reliability
Body contacting	✗	✓
Close S/D contact spacing	✓	✗
Optimum gate fingers spacing	✓	✓
Large device width	✓	✗
Low - Temperature	✓	✓

Figure 118: Different phenomenon studied in this dissertation in sub-100 nm CMOS-on-SOI technologies, and their impact on performance and reliability of MOSFETs.

10.2 Future Work

There are several research problems related to this dissertation which should be pursued. Some examples of such research problems are:

1) A reliability compact model that a circuit/system designer can use to test the circuit lifetime is the holy-grail of this research field. Multiple research opportunities exist towards achieving this goal. A good starting point is compact modeling of CMOS reliability problems such as hot-carrier effects, NBTI, total-dose degradation, latch-up etc. This is a very relevant (and complicated!) problem for semiconductor companies, and some companies have some tools which simulate such effects. But there is no standardized methodology to implement this yet.

2) Compact modeling of the effects of device layout on its performance.

3) Performance-reliability fundamental trade-offs need to be explored further. Usually some performance needs to be traded-off to achieve higher reliability. Innovative process/layout modifications such as the use of asymmetric halo-doping etc. need to be explored.

4) Impact of device layout on the single-event response can be studied. Source/Drain metal contact spacing, gate-finger to gate-finger spacing, and gate finger width should have an impact on the single event response.

5) Impact of technology scaling on the single-event response is very important to understand for space-system circuit designers.

5) The single-event response of 45-nm cascode devices should be investigated. The TCAD models built in this work can be used to understand the radiation tolerance of cascode devices.

6) Body-bias can be used to design tunable circuits in sub 100-nm SOI CMOS technologies.

7) High performance robust systems can be demonstrated with a wise use of the floating-body/body-contacted device options.

8) Mixed-mode (TCAD + Spectre) simulations using the CFDRC tool can be carried out in short-channel CMOS technologies to study the effect of single event transients on circuits.

REFERENCES

- [1] R. Arora, K. A. Moen, A. Madan, J. D. Cressler, E. Zhang, D. M. Fleetwood, R. D. Schrimpf, A. K. Sutton, and H. M. Nayfeh, "Impact of body tie and source/drain contact spacing on the hot carrier reliability of 45-nm RF-CMOS," in *Proceedings of the 2010 IEEE International Integrated Reliability Workshop*, 2010, pp. 56-60.
- [2] R. Arora and J. D. Cressler, "Operating Voltage Constraints in 45-nm nMOSFETs and Cascodes," (submitted) *IEEE Transactions on Electron Devices*, 2012.
- [3] R. Arora, E. X. Zhang, S. Seth, J. D. Cressler, D. M. Fleetwood, R. D. Schrimpf, G. L. Rosa, A. K. Sutton, H. M. Nayfeh, and G. Freeman, "Trade-offs between RF performance and total-dose tolerance in 45-nm RF-CMOS," *IEEE Transactions on Nuclear Science*, vol. 57, pp. 2830-2837, 2011.
- [4] R. Arora, S. Seth, C. H. J. Poh, J. D. Cressler, A. K. Sutton, H. M. Nayfeh, G. L. Rosa, and G. Freeman, "Impact of source/drain contact spacing on the RF reliability of 45-nm RF nMOSFETs," in *Proceedings of the 2011 IEEE International Reliability Physics Symposium*, 2011, pp. 5A.6.1 - 5A.6.6.
- [5] C. J. Marshall, P. W. Marshall, R. L. Ladbury, A. Waczynski, R. Arora, R. D. Foltz, J. D. Cressler, D. M. Kahle, D. Chen, G. S. Delo, N. A. Dodds, J. A. Pellish, E. Kan, N. Boehm, R. A. Reed, and K. A. LaBel, "Mechanisms and temperature dependence of single event latchup observed in a CMOS readout integrated circuit from 16300 K," *IEEE Transactions on Nuclear Science*, vol. 57, pp. 3078-3086, 2010.
- [6] R. Arora, E. X. Zhang, N. Lourenco, J. D. Cressler, D. M. Fleetwood, R. D. Schrimpf, A. K. Sutton, G. Freeman, and B. Greene, "Total-dose tolerance of 32-nm RF-CMOS on SOI and the impact of technology scaling on nFET reliability," (submitted) *IEEE Transactions on Nuclear Science*, 2012.
- [7] A. A. Abidi, "RFCMOS comes of age," *IEEE Journal of Solid State Circuits*, vol. 39, pp. 549-561, 2004.
- [8] B. Razavi, *Design of analog CMOS integrated circuits*, Boston, MA: McGraw Hill, 2000.
- [9] T. H. Lee, *The design of CMOS radio-frequency integrated circuits*, Cambridge, UK: Cambridge University Press, 2004.
- [10] C. -H. Jan, M. Agostinelli, H. Deshpande, M. A. El-Tanani, W. Hafez, U. Jalan, L. Janbay, M. Kang, H. Lakdawala, J. Lin, Y. -L. Lu, S. Mudanai, J. Park,

- A. Rahman, J. Rizk, W. -K. Shin, K. Soumyanath, H. Tashiro, C. Tsai, P. VanDerVoorn, J. -Y. Yeh, and P. Bai, "RF CMOS technology scaling in high-k/metal gate era for RF SoC (System-on-chip) applications," in *Proceedings of the 2010 IEEE International Electron Devices Meeting*, 2010, pp. 27.2.1 - 27.2.4.
- [11] <http://www.chipworks.com/en/technical-competitive-analysis/resources/recent-teardowns/2010/04/teardown-of-the-apple-ipad-tablet-computer/>
- [12] <http://www.intel.com/content/www/us/en/silicon-innovations/intel-22nm-technology.html>
- [13] G. G. Shahidi, "SOI technology for the GHz era," *IBM Journal of Research and Development*, vol. 46, pp. 121-131, 2002.
- [14] J. Pretet, S. Monfray, S. Cristoloveanu, and T. Skotnicki, "Silicon-on-nothing MOSFETs: performance, short-channel effects, and backgate coupling," *IEEE Transactions on Electron Devices*, vol. 51, pp. 240-245, 2004.
- [15] C. Yu and J. S. Yuan, "MOS RF reliability subject to dynamic voltage stress-modeling and analysis," *IEEE Transactions on Electron Devices*, vol. 52, pp. 1751-1758, 2005.
- [16] C. -H. Liu, R. -L. Wang, Y. -K. Su, C. -H. Tu, and Y. -Z. Juang, "DC and RF degradation induced by high RF power stresses in 0.18-um nMOSFETs," *IEEE Transactions on Device and Materials Reliability*, vol. 10, pp. 317-323, 2010.
- [17] G. T. Sasse, F. G. Kuper, and J. Schmitz, "MOSFET degradation under RF stress," *IEEE Transactions on Electron Devices*, vol. 55, pp. 3167-3174, 2008.
- [18] T. Quemerais, L. Moqillon, V. Huard, J. M. Fournier, P. Benech, N. Corrao, and X. Mescot, "Hot-carrier stress effect on a CMOS 65-nm 60-GHz one-stage power amplifier," *IEEE Electron Device Letters*, vol. 31, pp. 927-929, 2010.
- [19] E. Xiao and J. S. Yuan, "Hot carrier and soft breakdown effects on VCO performance," in *Proceedings of the 2002 IEEE Radio Frequency Integrated Circuits Symposium*, 2002, pp. 459-462.
- [20] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog circuit design in nanoscale CMOS technologies," *Proceedings of the IEEE*, vol. 97, pp. 1687-1714, 2009.
- [21] J. W. McPherson, "Scaling-induced reductions in CMOS reliability margins and the escalating need for increased design-in reliability efforts," in *Proceedings of the 2001 IEEE International Symposium on Quality Electronic Design*, 2001, pp. 123-130.
- [22] R. H. Dennard, F. H. Gaensslen, H. -N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. SC-9, pp. 256-268, 1974.

- [23] S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C. -H. Jan, C. Kenyon, J. Klaus, K. Kuhm, Z. Ma, B. McIntyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, "A 90-nm logic technology featuring strained-silicon," *IEEE Transactions on Electron Devices*, vol. 51, pp. 1790-1797, 2004.
- [24] J. G. Fossum, J. -Y. Choi, and R. Sundaresan, "SOI design for competitive CMOS VLSI," *IEEE Transactions on Electron Devices*, vol. 37, pp. 724-729, 1990.
- [25] H. M. . Nayfeh, N. Rovedo, A. Bryant, S. Narasimha, A. Kumar, X. Yu, N. Su, J. W. Sleight, R. R. Robison, W. Rausch, H. Mallela, and G. Freeman, "Impact of lateral asymmetric channel doping on 45-nm-technology N-type SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 56, pp. 3097-3105, 2009.
- [26] S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J. -O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, "Record RF performance of 45-nm SOI CMOS technology," in *Proceedings of the 2007 IEEE International Electron Devices Meeting*, 2007, pp. 255-258.
- [27] W. -H. Lee, A. Waite, H. Nii, H. M. Nayfeh, V. McGahay, H. Nakayama, D. Fried, H. Chen, L. Black, R. Bolam, J. Cheng, D. Chidambarrao, C. Christiansen, M. Cullinan-Scholl, D. R. Davies, A. Domenicucci, P. Fisher, J. Fitzsimmons, J. Gill, M. Gribelyuk, D. Harmon, J. Holt, K. Ida, M. Kiene, J. Kluth, C. Labelle, A. Madan, K. Malone, P. V. McLaughlin, M. Minami, D. Mocuta, R. Murphy, C. Muzzy, M. Newport, S. Panda, I. Peidous, A. Sakamoto, T. Sato, G. Sudo, H. VanMeer, T. Yamashita, H. Zhu, P. Agnello, G. Bronner, G. Freeman, S. -F. Huang, T. Ivers, S. Luning, K. Miyamoto, H. Nye, J. Pellerin, K. Rim, D. Schepis, T. Spooner, X. Chen, M. Khare, M. Horstmann, A. Wei, T. Kammler, J. Hontschel, H. Bierstedt, H. -J. Engelmann, A. Hellmich, K. Hempel, G. Koerner, A. Neu, R. Otterbach, C. Reichel, M. Trentsch, P. Press, K. Frohberg, M. Schaller, H. Salz, J. Hohage, H. Ruelke, J. Klais, M. Raab, D. Greenlaw, and N. Kepler, "High performance 65 nm SOI technology with enhanced transistor strain and advanced-low-k BEOL," in *Proceedings of the 2005 IEEE International Electron Devices Meeting*, 2005, pp. 56-59.
- [28] C. Hu, "Future CMOS scaling and reliability," *Proceedings of the IEEE*, vol. 81, pp. 682-689, 1993.
- [29] L. A. Akers, M. A. Holly, and C. Lund, "Hot carriers in small geometry CMOS," in *Proceedings of the 1984 IEEE International Electron Devices Meeting*, 1984, pp. 80-83.
- [30] E. Li, E. Rosenbaum, J. Tao, G. C. -F. Yeap, M. -R. Lin, and P. Fang, "Hot carrier effects in nMOSFETs in 0.1um CMOS technology," in *Proceedings of the 1999 IEEE International Reliability Physics Symposium*, 1999, pp. 253-258.

- [31] G. La Rosa, F. Guarin, S. Rauch, A. Acovic, J. Lukaitis, and E. Crabbe, "NBTI-channel hot carrier effects in PMOSFETs in advanced CMOS technologies," in *Proceedings of the 1997 IEEE International Reliability Physics Symposium*, 1997, pp. 282-286.
- [32] M. A. Alam and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," *Microelectronics Reliability*, vol. 45, pp. 71-81, 2005.
- [33] K. C. Boyko and D. L. Gerlach, "Time dependent dielectric breakdown of 210A oxides," in *Proceedings of the 1989 IEEE International Reliability Physics Symposium*, 1989, pp. 1-8.
- [34] C. M. Grens, P. Cheng, and J. D. Cressler, "Reliability of SiGe HBTs for power amplifiers-Part I: large-signal RF performance and operating limits," *IEEE Transactions on Device and Materials Reliability*, vol. 9, pp. 431-439, 2009.
- [35] B. L. Gregory and B. D. Shafer, "Latch-up in CMOS integrated circuits," *IEEE Transactions on Nuclear Science*, vol. 20, pp. 293-299, 1973.
- [36] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, "Radiation effects in SOI technologies," *IEEE Transactions on Nuclear Science*, vol. 50, pp. 522-538, 2003.
- [37] R. Arora, E. Simoen, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, K. F. Galloway, B. K. Choi, J. Mitard, M. Meuris, C. Claeys, A. Madan, and J. D. Cressler, "Effects of halo doping and Si capping layer thickness on total-dose effects in Ge p-MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 57, pp. 1933 - 1939, 2010.
- [38] T. P. Ma and P. V. Dressendorfer, *Ionizing radiation effects in MOS devices and circuits*, New York, NY: John Wiley and Sons, 1989.
- [39] J. C. Pickel, "Effect of CMOS miniaturization on cosmic-ray-induced error rate," *IEEE Transactions on Nuclear Science*, vol. 29, pp. 2049 - 2054, 1982.
- [40] O. Musseau, "Single-event effects in SOI technologies and devices," *IEEE Transactions on Nuclear Science*, vol. 43, pp. 603 - 613, 1996.
- [41] W. F. Clark, B. El-Kareh, R. G. Pires, S. L. Titcomb, and R. L. Anderson, "Low temperature CMOS-a brief review," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15, pp. 397 - 404, 1992.
- [42] F. Assaderaghi, W. Rausch, A. Ajmera, E. Leobandung, D. Schepis, L. Wagner, H. -J. Wann, R. Bolam, D. Yee, B. Davari, and G. Shahidi, "A 7.9/5.5 psec room/low temperature SOI CMOS," in *Proceedings of the 1997 IEEE International Electron Devices Meeting*, 1997, pp. 415 - 418.

- [43] D. Flandre, S. Adriaense, A. Akheyar, A. Crahay, L. Demeus, P. Delatte, V. Dessard, B. Iniguez, A. Neve, B. Katschmarskyj, P. Loumaye, J. Laconte, I. Martinez, G. Picun, E. Raully, C. Renaux, D. Spote, M. Zitout, M. Dehan, B. Parvais, D. Vanhoenacker, and J. -P. Raskin, "Fully depleted SOI CMOS technology for heterogeneous micropower, high-temperature or RF microsystems," *Solid-State Electronics*, vol. 45, pp. 54 - 549, 2001.
- [44] L. Arnaud, P. Lamontagne, R. Galand, E. Petitprez, D. Ney, and P. Waltz, "Electromigration induced void kinetics in Cu interconnects for advanced CMOS nodes," in *Proceedings of the 2011 IEEE International Reliability Physics Symposium*, 2011, pp. 297-306.
- [45] C. Duvvury, R. N. Rountree, Y. Fong, and R. A. McPhee, "ESD phenomena and protection issues in CMOS output buffers," in *Proceedings of the 1987 IEEE International Reliability Physics Symposium*, 1987, pp. 174-180.
- [46] K. P. Cheung and C. P. Chang, "Plasma-charging damage: A physical model," *Journal of Applied Physics*, vol. 75, pp. 4415-4426, 1994.
- [47] R. S. Muller, T. I. Kamins, and M. Chan, *Device electronics for integrated circuits*, New York, NY: John Wiley and Sons, 2003.
- [48] P. -I. Mak, and R. P. Martins, "High-/mixed-voltage RF and analog CMOS circuits come of age," *IEEE Circuits and Systems Magazine*, Fourth Quarter, pp. 27-39, 2010.
- [49] Sentaurus device user manual, *Synopsys Inc.*, 2010.
- [50] A. Hokazono, S. Balasubramanian, K. Ishimaru, H. Ishiuchi, C. Hu, and T. -J. King, "MOSFET hot-carrier reliability improvement by forward-body bias," *IEEE Electron Device Letters*, vol. 27, pp. 605-608, 2006.
- [51] C. Tinella, J. M. Fournier, D. Belot, and V. Knopik, "A high-performance CMOS-SOI antenna switch for the 2.5-5-GHz band," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1279-1283, 2003.
- [52] J. F. Chen, K. Ishimaru, and C. Hu, "Enhanced hot-carrier induced degradation in shallow trench isolated narrow channel PMOSFET's," *IEEE Electron Device Letters*, vol. 19, pp. 332-334, 1998.
- [53] K. Ishimaru, J. F. Chen, and C. Hu, "Channel width dependence of hot-carrier induced degradation in shallow trench isolated PMOSFET's," *IEEE Transactions on Electron Devices*, vol. 46, pp. 1532-1536, 1999.
- [54] N. Rezzak, R. D. Schrimpf, M. L. Alles, E. Zhang, D. M. Fleetwood, and Y. A. Li, "Layout-related stress effects on radiation-induced leakage current," *IEEE Transactions on Nuclear Science*, vol. 57, pp. 3288-3292, 2010.

- [55] M. H. Lin, E. R. Hsieh, S. S. Chung, C. H. Tsai, P. W. Liu, Y. H. Lin, C. T. Tsai, and G. H. Ma, "The understanding of strain-induced device degradation in advanced MOSFETs with process-induced strain technology of 65 nm node and beyond," in *Proceedings of the 2010 IEEE International Reliability Physics Symposium*, 2010, pp. 1053-1054.
- [56] C. Y. Cheng, Y. K. Fang, J. C. Hsieh, H. Hsia, W. M. Chen, S. S. Lin, and C. S. Hou, "Impact of the strained SiGe source/drain on hot carrier reliability for 45 nm p-type metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, vol. 92, pp. 133504, 2008.
- [57] J. Wu and X. Wang, "Stress engineering for 32 nm CMOS technology node," in *Proceedings of the 2008 IEEE International Conference on Solid-State and Integrated-Circuit Technology*, 2008, pp. 113-116.
- [58] O. Penzin, A. Haggag, W. McMahon, E. Lyumkis, and K. Hess, "MOSFET degradation kinetics and its simulation," *IEEE Transactions on Electron Devices*, vol. 50, pp. 1445-1450, 2003.
- [59] P. Heremans, R. Bellens, G. Groeseneken, and H. E. Maes, "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFET's," *IEEE Transactions on Electron Devices*, vol. 35, pp. 2194-2209, 1988.
- [60] D. M. Fleetwood, "Radiation-induced charge neutralization and interface-trap buildup in metal-oxide-semiconductor devices," *Journal of Applied Physics*, vol. 67, pp. 580-583, 1990.
- [61] J. -H. Lee, Y. -H. Wu, C. -H. Tang, T. -C. Peng, S. -H. Chen, and A. Oates, "A simple and useful layout scheme to achieve uniform current distribution for multi-finger silicided grounded-gate NMOS," in *Proceedings of the 2007 IEEE International Reliability Physics Symposium*, 2007, pp. 588-589.
- [62] Y. Cheng, M. J. Deen, and C.H. Chen, "MOSFET modeling for RF IC design," *IEEE Transactions on Electron Devices*, vol. 52, pp. 1286-1303, 2005.
- [63] K. Roy, S. Mukhopadhyay, and H. M-. Meimand, "Leakage current mechanisms and leakage reduction techniques in deep sub-micrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, pp. 305-323, 2003.
- [64] W. L. Kaufmann and A. A. Bergh, "The temperature dependence of ideal gain in double diffused silicon transistors," *IEEE Transactions on Electron Devices*, vol. ED-15, pp. 732-735, 1968.
- [65] R. V. Martinelli, "The temperature dependence of the dc base and collector currents in silicon bipolar transistors," *IEEE Transactions on Electron Devices*, vol. ED-23, pp. 1218-1224, 1976.

- [66] W. P. Dumke, "The effect of base doping on the performance of Si bipolar transistors at low temperatures," *IEEE Transactions on Electron Devices*, vol. ED-28, pp. 494-500, 1981.
- [67] J. G. Dooley and R. C. Jaeger, "Temperature dependence of latchup in CMOS circuits," *IEEE Electron Device Letters*, vol. 5, pp. 41-43, 1984.
- [68] H. Hanamura, M. Aoki, T. Masuhara, O. Minato, and T. Hayashida, "Operation of bulk CMOS devices at very low temperatures," *IEEE Journal of Solid-State Circuits*, vol. SSC-21, pp. 484-490, 1986.
- [69] E. Sangiorgi, R. L. Johnston, M. R. Pinto, P. F. Bechtold, and W. Fichtner, "Temperature dependence of latch-up phenomena in scaled CMOS structures," *IEEE Electron Device Letters*, vol. EDL-7, pp. 28-31, 1986.
- [70] C. Yao, J. Tzou, R. Cheung, and H. Chan, "Temperature dependence of latch-up characteristics in LDD CMOS devices," *IEEE Electron Device Letters*, vol. EDL-7, pp. 92-94, 1986.
- [71] C. Yao, J. Tzou, R. Cheung, and H. Chan, "Temperature dependence of CMOS reliability," in *Proceedings of the 1986 IEEE International Reliability Physics Symposium*, 1986, pp. 175-182.
- [72] R. R. Troutman, *Latchup in CMOS technology*, Boston, MA: Kluwer Academic, 1986.
- [73] S. H. Voldman, *Latchup*, West Sussex, U. K.: Wiley, 2007.
- [74] T. F. Miyahira, A. H. Johnston, H. N. Becker, S. D. LaLumondiere, and S. C. Moss, "Catastrophic latchup in CMOS analog-to-digital converters," *IEEE Transactions on Nuclear Science*, vol. 48, pp. 1833-1840, 2001.
- [75] J. D. Cressler and G. Niu, *Silicon-germanium heterojunction bipolar transistors*. Norwood, MA: Artech House, 2003.
- [76] J. D. Cressler, "On the potential of SiGe HBTs for extreme environment electronics," *Proceedings of the IEEE*, vol. 93, pp. 1559-1582, 2005.
- [77] G. Zhang, J. D. Cressler, G. Niu, and A. J. Joseph, "A new 'mixed-mode' reliability degradation mechanism in advanced Si and SiGe bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 49, pp. 2151-2156, 2002.
- [78] P. Cheng, C. Zhu, A. Appaswamy, and J. D. Cressler, "A new current-sweep method for assessing the mixed-mode damage spectrum of SiGe HBTs," *IEEE Transactions on Device and Materials Reliability*, vol. 7, pp. 479-487, 2007.
- [79] B. Jun, R. Diestelhorst, M. Bellini, G. Espinel, A. Appaswamy, A. P. G. Prakash, J. D. Cressler, D. Chen, R. D. Schrimpf, D. M. Fleetwood, M. Turowski, and A. Raman, "Temperature-dependence of off-state drain leakage in X-ray irradiated

- 130 nm CMOS devices,” *IEEE Transactions on Nuclear Science*, vol. 53, pp. 3203-3209, 2006.
- [80] A. Appaswamy, B. Jun, R. Diestelhorst, G. Espinel, A. P. G. Prakash, J. D. Cressler, P. W. Marshall, C. J. Marshall, Q. Liang, G. Freeman, T. I.- Smith, and J. R. Willaims, “The effects of proton irradiation on 90 nm strained Si CMOS on SOI devices,” in *Proceedings of the 2006 IEEE Radiation Effects Data Workshop*, 2006, pp. 62-65.
 - [81] A. Madan, R. Verma, R. Arora, E. P. Wilcox, J. D. Cressler, P. W. Marshall, R. D. Schrimpf, P. F. Cheng, L. Y. Del Castillo, Q. Liang, and G. Freeman, “The enhanced role of shallow-trench isolation in ionizing radiation damage of 65 nm RF-CMOS,” *IEEE Transactions on Nuclear Science*, vol. 56, pp. 3256-3261, 2009.
 - [82] B. Gill, N. Seifert, V. Zia “Comparison of alpha-particle and neutron-induced combinational and sequential logic error rates at the 32nm technology node,” in *Proceedings of the 2009 IEEE International Reliability Physics Symposium*, 2009, pp. 199-205.
 - [83] S. Zafar, A. Kumar, E. Gusev, and E. Cartier “Threshold voltage instabilities in high-k gate dielectric stacks,” *IEEE Transactions on Device and Materials Reliability*, vol. 5, pp. 45-64, 2005.
 - [84] G. Bersuker, J. H. Kim, C. S. Park, C. D. Young, S. V. Nadkarni, R. Choi, and B. H. Lee “Mechanism of electron trapping and characteristics of traps in HfO_2 gate stacks,” *IEEE Transactions on Device and Materials Reliability*, vol. 7, pp. 138-145, 2007.
 - [85] S. K. Dixit, X. J. Zhou, R. D. Schrimpf, D. M. Fleetwood, S. T. Pantelides, R. Choi, G. Bersuker, and L. C. Feldman “Radiation induced charge trapping in ultrathin HfO_2 -based MOSFETs,” *IEEE Transactions on Nuclear Science*, vol. 54, pp. 1883-1890, 2007.
 - [86] B. Green, Q. Liang, K. Amarnath, Y. Wang, J. Schaeffer, M. Cai, Y. Liang, S. Saroop, J. Cheng, A. Rotondaro, S. -J. Han, R. Mo, K. McStay, S. Ku, R. Pal, M. Kumar, B. Dirahoui, B. Yang, F. Tamweber, W. -H. Lee, M. Steigerwalt, H. Weijtmans, J. Holt, L. Black, S. Samavedam, M. Turner, K. Ramani, D. Lee, M. Belyansky, M. Chowdhury, D. Aime, B. Min, H. van Meer, H. Yin, K. Chan, M. Angyal, M. Zaleski, O. Ogunsola, C. Child, L. Zhuang, H. Yan, D. Permana, J. Sleight, D. Guo, S. Mittl, D. Ioannou, E. Wu, M. Chudzik, D. -G. Park, D. Brown, S. Luning, D. Mocuta, E. Maciejewski, K. Henson, and E. Leobandung “High performance 32 nm SOI CMOS with high-k/metal gate and $0.149 \mu m^2$ SRAM and ultra low-k back end with eleven levels of copper,” in *Proceedings of the 2009 IEEE Symposium on VLSI Technology*, 2009, pp. 140-141.
 - [87] S. Lee, J. Kim, D. Kim, B. Jagannathan, C. Cho, J. Johnson, B. Dufrene, N. Zamdmmer, L. Wagner, R. Williams, D. Fried, K. Rim, J. Pekarik, S. Springer,

- J. -O. Plouchart, and G. Freeman, "SOI CMOS technology with 360 GHz f_T NFET, 260 GHz f_T PFET, and record circuit performance for millimeter-wave digital and analog system-on-chip applications," in *Proceedings of the 2007 IEEE Symposium on VLSI Technology*, 2007, pp. 54-55.
- [88] <http://www.ioffe.rssi.ru/SVA/NSM/Semicond/Si/electric.html>
- [89] P. Heremans, G. V. D. Bosch, R. Bellens, G. Groesenken, and H. E. Maes, "Temperature dependence of the channel hot-carrier degradation of n-channel MOSFET's," *IEEE Transactions on Electron Devices*, vol. 37, pp. 980-993, 1990.
- [90] J. -K. Lee, N. -J. Choi, C. -G. Yu, J. -P. Colinge and J. -T. Park, "Temperature dependence of the hot-carrier degradation in silicon-on-insulator dynamic threshold voltage MOS transistors," *IEEE Electron Device Letters*, vol. 23, pp. 673-675, 2002.
- [91] T. Chen, C. Zhu, L. Najafizadeh, B. Jun, A. Ahmed, R. Diestelhorst, G. Espinel, and J. D. Cressler, "CMOS reliability issues for emerging cryogenic lunar electronics applications," *Solid-State Electronics*, vol. 50, pp. 959-963, 2006.
- [92] Z. Chen, X. Ji, F. Yan, Y. Shi, Y. Song, J. Wu, and Q. Guo, "Worst case stress conditions for hot carrier degradation with technology nodes from 0.35 μm to 45nm," *ECS Transactions*, vol. 44, pp. 1151-1155, 2012.

VITA

Rajan Arora received his Bachelors degree in Electronics and Communication Engineering from Punjab Engineering College, India in Spring, 2007. He received his Master's degree in Electrical Engineering in Summer, 2009 from Vanderbilt University, TN. His research at Vanderbilt focussed on alternative substrate materials (germanium, silicon carbide) for CMOS technologies. He moved to Georgia Tech in Fall, 2009 to pursue a doctorate degree in Electrical Engineering. His research at Georgia Tech has focussed on sub 100-nm RF-CMOS on SOI technologies and their reliability. He interned at Texas Instruments in Summer, 2011 where his work focussed on bipolar reliability modeling and analog design. He was one of the co-recipients of "Outstanding Conference Paper" award at the Nuclear and Space Radiation Effects Conference, 2010.