

HIGH FREQUENCY VOLTAGE CONTROLLED RING OSCILLATORS IN STANDARD CMOS

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High Frequency Voltage Controlled Ring Oscillators in Standard CMOS

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*To my parents, Habibe and Sabri,
my brother, Ali Erdem,
my fiancée, Nazlı,
and the memory of Dr. John P. Uyemura*

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TABLE OF CONTENTS

DEDICATION	iii
ACKNOWLEDGEMENTS	iv
LIST OF TABLES	xi
LIST OF FIGURES	xiii
SUMMARY	xx
I INTRODUCTION	1
1.1 Motivation	1
1.2 Thesis Organization	4
II INTEGRATED OSCILLATORS	6
2.1 Oscillator Principles	6
2.2 Types of Integrated Oscillators	8
2.2.1 LC Oscillators	10
2.2.2 Oscillators w/o Resonators: Ring Oscillators	10
2.2.3 Oscillators w/o Resonators: Relaxation Oscillators	12
2.3 Important Characteristics of Oscillators and Applications	13
III CMOS RING OSCILLATORS	16
3.1 Ring Oscillator Basics	16
3.1.1 Frequency Domain Analysis	17
3.2 Single-Ended Ring oscillators	20
3.3 Differential Ring oscillators	22
3.4 Ring oscillator Design Challenges and Techniques	27
3.4.1 Frequency	27
3.4.1.1 Two-Stage Ring Oscillators	28
3.4.1.2 Subfeedback Loops	29
3.4.1.3 Output Interpolation Technique	30

3.4.2	Phase Noise	31
3.4.3	Stability	33
IV	VCO PHASE NOISE MODELS	37
4.1	Leeson's Phase Noise Model	37
4.1.1	Oscillator Phase Noise Spectrum	38
4.2	Razavi's Phase Noise Model	39
4.2.1	Classical Definitions of Q	39
4.2.2	Q Factor of a Ring Oscillator	40
4.3	Hajimiri's Phase Noise Model	43
4.3.1	Impulse Sensitivity Function	44
4.3.2	VCO Phase Noise from ISF	46
4.3.3	Modelling of Cyclostationary Noise Sources	47
4.3.4	Calculation/Simulation of ISF for Multiple Noise Sources/Nodes	48
4.3.5	Using Hajimiri's Model	49
4.4	Harjani's Phase Noise Model	51
4.4.1	Phase Noise of a Three-Stage Ring VCO	52
4.4.2	Phase Noise of an N-Stage Ring VCO	54
V	PROPOSED RING OSCILLATOR DESIGNS	56
5.1	Architecture	56
5.1.1	Quantitative Analysis	57
5.1.1.1	Time-Domain Analysis	57
5.1.1.2	Odd Number of Stages	60
5.1.1.3	Even Number of Stages	70
5.2	Gain Stage	77
5.2.1	Saturated Stage	78
5.2.2	Delay Control	79
5.2.3	Type-I Saturated Stage	81
5.2.4	Type-II Saturated Stage	82

5.3	Multiple-Pass Ring Design Example	87
5.3.1	Single-Loop Ring-Oscillator	87
5.3.2	Multiple-Pass Ring-Oscillator	90
5.3.3	Frequency Improvement	91
VI	HIGH PERFORMANCE RING OSCILLATORS	99
6.1	Design for Maximum Frequency	99
6.1.1	Three-stage Ring Oscillators	101
6.2	Phase Noise Calculation & Simulation	107
6.2.1	Phase Noise Calculations	107
6.2.2	Phase Noise Simulations	111
6.3	Noise & Frequency Tradeoff	115
6.3.1	Four-stage Ring Oscillators	116
6.3.2	Phase Noise Model, Revisited	122
6.4	Designs with Various Configurations	126
6.4.1	Lower Frequency Designs	128
6.5	Tuning Range Considerations	128
6.5.1	Control of The Tuning Range	131
6.5.2	Dual Control-Path Ring Oscillators	133
6.6	Parameter Variations	135
6.6.1	Temperature Variations	136
6.6.2	Physical Parameters	137
6.6.3	Power Supply/Ground Disturbances	139
6.7	Summary	148
VII	BENCHMARK DESIGNS	149
7.1	Current Starved Ring Oscillator	149
7.2	Differential Oscillator with Maneatis Loads	155
7.3	Summary of the Designs	160

VIII EXPERIMENTAL RESULTS	167
8.1 Physical Design	167
8.2 Testing Considerations	169
8.3 Characterization of the Parts	176
8.3.1 Multiple-Pass Ring Oscillators Test Results	176
8.3.2 LC Oscillator Test Results	182
8.4 PLL Test	189
IX PERFORMANCE COMPARISON	197
9.1 LC vs Ring Oscillators	197
9.2 Published Designs	199
9.3 Where Does This Work Fit?	203
9.4 CMOS Minimum Feature Size	207
X CONCLUSION AND FUTURE WORK	210
10.1 Summary	210
10.2 Applications	212
10.3 Contributions	214
10.4 Future Research	216
APPENDIX A — PLL INTRODUCTION	220
REFERENCES	228
VITA	236

LIST OF TABLES

Table 1	Maximum effective Q factor of ring oscillators in various technologies	54
Table 2	Frequency improvement factors and gain requirements of multiple-pass loop configurations for $3 \leq N \leq 7$	75
Table 3	Frequency improvement factors and gain requirements of multiple-pass loop configurations for $8 \leq N \leq 9$	76
Table 4	Transistor sizes of 4-stage single-loop ring design in $0.18 \mu m$ CMOS	88
Table 5	Final transistor sizes of 4-stage single-loop ring design in $0.18 \mu m$ CMOS	90
Table 6	Characteristics of fabrication technologies used in this work	101
Table 7	Transistor sizes of a 3-stage ring design in $0.25 \mu m$ CMOS with $f_{max} = 5.3GHz$	101
Table 8	Transistor sizes of a 3-stage ring design in $0.18 \mu m$ CMOS with $f_{max} = 9.5GHz$	103
Table 9	Transistor sizes of a 3-stage ring design in $0.13 \mu m$ CMOS with $f_{max} = 14.4GHz$	105
Table 10	Calculation of phase noise for the 3-stage oscillators in various technologies	109
Table 11	Phase noise simulation results for the 3-stage oscillators in $0.25 \mu m$ and $0.18 \mu m$ CMOS	113
Table 12	Transistor sizes of the 4-stage ring design in $0.25 \mu m$ CMOS	116
Table 13	Transistor sizes of the 4-stage ring design in $0.18 \mu m$ CMOS	117
Table 14	Calculation of phase noise for the 4-stage oscillators in various technologies	118
Table 15	Phase noise of various $0.18 \mu m$ designs extracted from simulations and calculations	124
Table 16	Phase noise of the $0.25 \mu m$ multiple-pass designs extracted from simulations and calculations using the modified formula (Equation (106))	126
Table 17	Phase noise of the $0.18 \mu m$ multiple-pass designs extracted from simulations and calculations using the modified formula (Equation (106))	126

Table 18	Transistor sizes of the type-I saturated stage used in various 0.18 μm ring oscillators	128
Table 19	Output frequencies, power dissipations, and frequency improvement factors of multiple-pass loop configurations for $3 \leq N \leq 7$	129
Table 20	Output frequencies, power dissipations, and frequency improvement factors of multiple-pass loop configurations for $8 \leq N \leq 9$	130
Table 21	Performance comparison of three and five stage rings oscillating at the same frequency	131
Table 22	Transistor sizes of the 4-stage wide-tuning range ring design in 0.18 μm CMOS	132
Table 23	Transistor sizes of the type-II stage employed in the 3-stage 0.25 μm ring design with dual control-paths	134
Table 24	Transistor sizes of the differential input current control circuitry of the 3-stage 0.25 μm ring design with dual control-paths	134
Table 25	Performance comparison of 3-stage dual-control and single-control ring oscillators in 0.25 μm	136
Table 26	Transistor sizes of the 3-stage current starved VCO	152
Table 27	Comparison of the 3-stage current starved ring design with the wide tuning range 4-stage multiple-pass ring design	154
Table 28	Transistor sizes of the 3-stage differential VCO with Maneatis loads	157
Table 29	Comparison of the three-stage Maneatis ring design with the three-stage multiple-pass ring design	159
Table 30	Comparison of the multiple-pass and other ring oscillators discussed in this work - A	163
Table 31	Comparison of the multiple-pass and other ring oscillators discussed in this work - B	164
Table 32	Transistor sizes of the Type-I saturated stage used in the prototype ring oscillators	176
Table 33	Phase noise of ring oscillators extracted from measurements, simulations and calculations at 1 MHz offset from center frequencies	184
Table 34	Phase noise comparison of implemented and previously published VCOs (at 1 MHz offset)	190
Table 35	PLL Design Parameters and Measurements	195

LIST OF FIGURES

Figure 1	Positive feedback oscillatory system modeled in s-domain	7
Figure 2	Resonator tank model	10
Figure 3	LC oscillator model	11
Figure 4	Ring oscillator block model	11
Figure 5	Relaxation oscillator	12
Figure 6	Ring oscillator structure	16
Figure 7	Ring oscillator linear model	18
Figure 8	Current starved inverter	20
Figure 9	(a) Capacitive load control, (b) Resistive load control	21
Figure 10	Frequency tuning by control of V_{dd}	21
Figure 11	4-Stage differential ring oscillator	23
Figure 12	Simple differential pair	24
Figure 13	Differential pair with current mirror	24
Figure 14	Differential pair with symmetrical loads	25
Figure 15	Differential pair with symmetrical loads & amplitude control circuitry	26
Figure 16	Double differential delay stage	28
Figure 17	Subfeedback loop architecture	29
Figure 18	Output interpolation technique	30
Figure 19	Isolation of delay stage from the power supply	33
Figure 20	Temperature compensated delay stage	35
Figure 21	Phase noise PSD regions of an oscillator	39
Figure 22	Quality factor of ring oscillators found using Razavi's model	42
Figure 23	Phase noise of different rings relative to a three-stage ring oscillator	43
Figure 24	Phase shift resulting from impulses injected at different instants . .	45
Figure 25	Representation of waveforms with sharp transitions using a clipped sinusoidal	51
Figure 26	Modified linear model of a three-stage ring oscillator	52

Figure 27	3-stage ring oscillator with multiple-pass loop architecture	57
Figure 28	3-stage single-ended ring oscillator	58
Figure 29	3-stage single-ended ring oscillator with multiple-pass loop architecture	58
Figure 30	N-stage multiple pass ring-oscillator with (a) noninverted feedfor- ward connections (b) inverted feedforward connections	61
Figure 31	Ring-oscillator stage first-order model	62
Figure 32	N-stage multiple pass ring-oscillator redrawn with G_m blocks moved out of the gain stages	63
Figure 33	Multiple pass ring-oscillator with $(N,x,sign)=(3,2,+)$	68
Figure 34	Multiple pass ring-oscillator with $(N,x,sign)=(5,3,-)$	69
Figure 35	Multiple pass ring-oscillator with $(N,x,sign)=(4,2,-)$	71
Figure 36	Multiple pass ring-oscillator with $(N,x,sign)=(6,4,+)$	72
Figure 37	Saturated delay stage with PMOS cross-coupled transistors	78
Figure 38	Saturated delay stage with (a) a tail current source for frequency control (b) variable loads for frequency control	80
Figure 39	Saturated delay stage with feedback control	80
Figure 40	Saturated delay stage with feedback control for multiple pass loop architecture implementation	82
Figure 41	Saturated delay stage with double control paths	84
Figure 42	Differential input current control circuitry	85
Figure 43	Simplifications on the type-II saturated stage	85
Figure 44	Type-II saturated stage, simplified	86
Figure 45	Type-II saturated stage, p+ switched from high to low	86
Figure 46	4-stage single-loop ring oscillator frequency vs load size	89
Figure 47	4-stage single-loop ring oscillator power dissipation vs frequency . .	89
Figure 48	4-stage single-loop ring oscillator frequency-voltage characteristics for various load sizes	90
Figure 49	4-stage multiple-pass ring oscillator frequency for various secondary input transistor sizes	92
Figure 50	4-stage multiple-pass ring oscillator power dissipation for various sec- ondary input transistor sizes	93

Figure 51	4-stage multiple-pass ring oscillator power dissipation vs frequency	93
Figure 52	Left half of type-1 saturated stage	94
Figure 53	Transient drain currents of the transistors for M1-M2: $16\ \mu m/0.18\ \mu m$, M7-M8: $18\ \mu m/0.18\ \mu m$	95
Figure 54	Transient drain currents of the transistors for M1-M2: $16\ \mu m/0.18\ \mu m$, M7-M8: $2\ \mu m/0.18\ \mu m$	95
Figure 55	Frequency improvement of multiple-pass architecture, $(N,x,sign)=(4,2,+)$	98
Figure 56	Frequency vs control voltage characteristics of the 3-stage ring VCO in $0.25\ \mu m$ CMOS	102
Figure 57	Power dissipation vs control voltage characteristics of the 3-stage ring VCO in $0.25\ \mu m$ CMOS	103
Figure 58	Frequency vs control voltage characteristics of the 3-stage ring VCO in $0.18\ \mu m$ CMOS	104
Figure 59	Power dissipation vs control voltage characteristics of the 3-stage ring VCO in $0.18\ \mu m$ CMOS	104
Figure 60	Frequency vs control voltage characteristics of the 3-stage ring VCO in $0.13\ \mu m$ CMOS	106
Figure 61	Power dissipation vs control voltage characteristics of the 3-stage ring VCO in $0.13\ \mu m$ CMOS	106
Figure 62	Single-ended and differential output signals of the 3-stage ring in $0.25\ \mu m$ CMOS	110
Figure 63	Single-ended and differential output signals of the 3-stage ring in $0.18\ \mu m$ CMOS	110
Figure 64	Single-ended and differential output signals of the 3-stage ring in $0.13\ \mu m$ CMOS	111
Figure 65	Phase noise simulation of the 3-stage ring in $0.25\ \mu m$ CMOS	112
Figure 66	Phase noise simulation of the 3-stage ring in $0.18\ \mu m$ CMOS	113
Figure 67	Phase noise simulation of the 3-stage ring in $0.18\ \mu m$ CMOS with flicker noise parameters included in the models	114
Figure 68	Comparison of the phase noise simulations of the 3-stage ring in $0.18\ \mu m$ CMOS with and without including the flicker noise	115
Figure 69	Single-ended and differential output signals of the 4-stage ring in $0.25\ \mu m$ CMOS	117

Figure 70	Single-ended and differential output signals of the 4-stage ring in 0.18 μm CMOS	118
Figure 71	Phase noise simulation of the 4-stage ring in 0.25 μm CMOS	120
Figure 72	Phase noise simulation of the 4-stage ring in 0.18 μm CMOS	120
Figure 73	Frequency vs control voltage characteristics of the 4-stage ring VCO in 0.25 μm CMOS	121
Figure 74	Frequency vs control voltage characteristics of the 4-stage ring VCO in 0.18 μm CMOS	122
Figure 75	Power dissipation vs control voltage characteristics of the 4-stage ring VCO in 0.25 μm CMOS	123
Figure 76	Power dissipation vs control voltage characteristics of the 4-stage ring VCO in 0.18 μm CMOS	123
Figure 77	Frequency-voltage characteristics of narrow and wide tuning range 4-stage ring designs in 0.18 μm CMOS	132
Figure 78	Frequency vs control voltage characteristics of the 3-stage 0.25 μm ring design with dual control-paths	135
Figure 79	f-V characteristics of the 4-stage 0.18 μm multiple pass design at different ambient temperatures	138
Figure 80	f-V characteristics of the 4-stage 0.18 μm multiple pass design at different process corners	139
Figure 81	f-V characteristics of the 4-stage 0.18 μm multiple pass design at different ambient temperatures and process corners	140
Figure 82	f-V characteristics of the 4-stage 0.18 μm multiple pass design at different power supply voltages	141
Figure 83	Period shift of 4-Stage multiple-pass ring under 100 mV_{p-p} , 5 GHz sinusoidal noise on Vdd	142
Figure 84	Period shift of 4-Stage multiple-pass ring under 100 mV_{p-p} , 5 GHz sinusoidal noise on ground	142
Figure 85	Phase shift of 4-Stage multiple-pass ring under 100 mV_{p-p} , 5 GHz sinusoidal noise on Vdd	143
Figure 86	Phase shift of 4-Stage multiple-pass ring under 100 mV_{p-p} , 5 GHz sinusoidal noise on ground	143
Figure 87	Output and V_{DD} signals of the 4-stage multiple-pass ring oscillator when a V_{DD} glitch occurs at the most vulnerable moment	145

Figure 88	Period shift of the 4-stage multiple-pass ring oscillator when a V_{DD} glitch occurs at the most vulnerable moment	145
Figure 89	Phase shift of the 4-stage multiple-pass ring oscillator when a V_{DD} glitch occurs at the most vulnerable moment	146
Figure 90	Output and ground signals of the 4-stage multiple-pass ring oscillator when a ground glitch occurs at the most vulnerable moment	146
Figure 91	Period shift of the 4-stage multiple-pass ring oscillator when a ground glitch occurs at the most vulnerable moment	147
Figure 92	Phase shift of the 4-stage multiple-pass ring oscillator when a ground glitch occurs at the most vulnerable moment	147
Figure 93	Current starved inverter	150
Figure 94	Current starved ring oscillator frequency control	150
Figure 95	Current starved ring oscillator frequency vs transistor sizes	151
Figure 96	Current starved ring oscillator frequency vs control current curve	152
Figure 97	Current starved ring oscillator power dissipation vs control current curve	153
Figure 98	Differential pair with Maneatis loads	156
Figure 99	Maneatis ring oscillator frequency control	157
Figure 100	Maneatis ring oscillator frequency vs control current curve	158
Figure 101	Maneatis ring oscillator power dissipation vs control current curve	158
Figure 102	Comparison of the multiple-pass and other ring oscillators discussed in this work, phase noise vs frequency plot	161
Figure 103	Comparison of the multiple-pass and other ring oscillators discussed in this work, phase noise vs power plot	161
Figure 104	Comparison of the multiple-pass and other ring oscillators discussed in this work, frequency vs power plot	162
Figure 105	Photograph of the prototype chip	168
Figure 106	Auxiliary circuits for oscillator testing	170
Figure 107	Front-end buffer schematics	172
Figure 108	Divide-by-two circuit schematics	172
Figure 109	Multiplexer schematics	173
Figure 110	Differential DFF schematics	173

Figure 111 Differential to single-ended converter schematics	174
Figure 112 Layout of the three-stage multiple-pass ring oscillator with the test- ing circuitry	175
Figure 113 Three-stage multiple-pass ring oscillator layout	177
Figure 114 Nine-stage multiple-pass ring oscillator layout	177
Figure 115 Three-stage multiple-pass ring oscillator characterization - I	178
Figure 116 Three-stage multiple-pass ring oscillator characterization - II	179
Figure 117 Nine-stage multiple-pass ring oscillator characterization	179
Figure 118 Phase noise simulation results of the implemented multiple-pass ring oscillators	180
Figure 119 Measured power spectrum at the (a) divide-by-four output of the three-stage ring oscillator (b) divide-by-two output of the nine-stage ring oscillator	183
Figure 120 LC oscillator schematics	185
Figure 121 Inductor layout	186
Figure 122 LC oscillator frequency-voltage curves extracted from simulations .	187
Figure 123 LC oscillator frequency-voltage curves extracted from measurements	188
Figure 124 Measured power spectrum at the divide-by-16 output of the LC os- cillator	188
Figure 125 Differential PFD	191
Figure 126 Half of the differential CP	192
Figure 127 Differential CP	193
Figure 128 Differential PLL	194
Figure 129 Phase noise limits of ring and LC oscillators	199
Figure 130 Phase noise vs frequency performance of published LC oscillators and 20 dB/decade limit curve	200
Figure 131 Phase noise vs frequency performance of published LC oscillators and 27 dB/decade limit curve	201
Figure 132 Phase noise vs frequency performance of published ring oscillators and limit curves	202
Figure 133 Phase noise vs frequency performance of published ring oscillators and introduced designs compared with the limit curves	202

Figure 134 Phase noise/frequency performance of published ring and LC oscillators	203
Figure 135 FOM of published ring and LC oscillators	204
Figure 136 Phase noise/frequency performance of published ring and LC oscillators vs introduced designs	205
Figure 137 FOM of published ring and LC oscillators vs introduced designs . .	206
Figure 138 Maximum frequencies of various ring oscillators as a function of the minimum feature size	207
Figure 139 Phase noise performance of various ring oscillators as a function of the minimum feature size	208
Figure 140 Phase locked loop block diagram	221
Figure 141 PLL waveforms for $y(t)$ lagging $x(t)$	222
Figure 142 Phase Frequency Detector	224
Figure 143 PFD response for $\omega_{Ref} > \omega_{Fback}$	225
Figure 144 PFD response for Ref signal lagging $Fback$ signal	225
Figure 145 Charge Pump PLL	226
Figure 146 Charge Pump PLL with the stabilization resistor and the ripple reduction capacitor	226

SUMMARY

This dissertation presents a study of high-frequency low-noise CMOS voltage-controlled ring oscillators. The objective is to understand the limitations of voltage-controlled ring oscillators that are implemented in standard CMOS technologies when they are extended to multiple gigahertz applications. This study explores the maximum frequency limitations and the associated noise performance levels of ring oscillators that can be constructed using different design styles. Important metrics also include the tuning range, linearity of frequency-control characteristics, stability across temperature and process corner variations, and power consumption of the circuits. Simplicity and the low cost provide the motivation for selecting a ring structure over competing LC-based architectures.

To fulfill the requirements of this study, various ring and LC oscillators were designed in several state-of-the-art CMOS processes. A multiple-pass differential architecture along with a saturated-type delay-stage utilizing cross-coupled transistors has been found to have promising characteristics. A new ring oscillator design, which mixes the analog and digital elements, is proposed to solve the problems related with the single-ended control and the high gain of conventional ring oscillator designs. By using these techniques, it may become possible to extend the applications of ring VCOs into some areas that previously required the performance of LC oscillators.

CHAPTER I

INTRODUCTION

1.1 Motivation

The design and implementation of integrated high-speed communications systems, operating at gigabits per second rates, exhibit many challenges. Some of these challenges are minimizing cost and decreasing power consumption while maintaining the speed and the bit error rate (BER) of the system. These performance parameters are directly related to the timing scheme of the system. All modern communications systems require a stable periodic signal to provide the timing basis for functions such as sampling, synchronization, frequency synthesis, etc. This periodic signal is called the clock signal. In the majority of the applications, this clock signal is created in the system, either by using an off-chip crystal oscillator or an integrated oscillator. In some other applications, the clock information can be extracted from the input signal. Even if the input signal has the timing information, usually a local clock signal at a different phase or frequency is required. Data retiming in data recovery applications and clock synchronization/deskewing in clock distribution applications are examples. Phase locked loops (PLLs) or similar structures such as delay locked loops (DLLs) are used to create the required local clock signal that is referenced to the input clock.

The generation of this periodic clock signal is the main bottleneck especially in high-speed communications applications that push the fabrication technologies to their limits. With increasing data transfer speeds, the clock periods become shorter, decreasing the amount of absolute timing uncertainty (jitter) that can be tolerated at the output. This makes the design of such systems very challenging. In some applications such as analog to digital converters (ADC), data recovery networks, or mixers,

clock edges determine the sampling instant. Random and systematic variations in the sampling time degrade the performance of the system by limiting the maximum resolution. In some other applications including clock generators, clock recovery networks, and frequency synthesizers, the generated clock is the output signal. Thus the output signal clarity, which is quantified in terms of phase noise and spurious tones, is directly dependent upon the performance of the periodic signal generator.

The raw periodic signal of a local clock generator is either created by an integrated voltage controlled oscillator (VCO) or a current controlled oscillator (CCO). From now on, VCOs and CCOs will be considered equivalent structures and the abbreviation "VCO" will be used to refer to both of them. This periodic signal is usually buffered and/or amplified before driving other circuitry that requires the timing information. In communications systems, VCOs are often utilized within a closed loop structure, specifically in a phase locked loop, although standalone applications are also available. PLLs are crucial when the local clock signal needs to be synchronized to an input frequency or when precise control of the output frequency is essential. Frequency synthesis is also achieved by using an adjustable divider inside the PLL.

The design of the high performance systems requiring VCOs to be employed in phase locked loops is the most challenging because of the increased complexity. In such systems, VCOs operate in conjunction with other parts of the PLL; phase-frequency detectors (PFDs), charge pumps (CPs), loop-filters (LPs) and dividers. Hence, the output signal characteristics depend on many factors including the loop transfer function. PLL applications include clock/data recovery networks (CDRs) used in fiber optic data transceivers, disk drive channels, local area network (LAN) transceivers, and DSL transceivers. Clock generators for microprocessors, digital signal processing (DSP) systems and dynamic random-access memories (DRAM) rely on PLLs for stable clock generation referenced to a crystal oscillator. Zero delay clock buffers use PLLs to synchronize the clock inputs of circuits at different parts

of the chip to reduce clock skew and timing errors. Standalone applications of VCOs include analog-to-digital and digital-to-analog converters (ADC and DAC), and direct frequency synthesizers.

Noise requirements of the radio frequency (RF) functions, such as RF frequency synthesis and frequency modulation/demodulation, are the most demanding. Very low phase noise oscillators are needed which can be implemented by using an external resonator with a high quality factor, such as a varactor tuned LC tank. However, using external parts increases the cost of the system and therefore fully monolithic designs are highly desirable. Other high-speed communications applications also benefit from the full-monolithic implementation since it gives an advantage in the cost and the performance of a system by eliminating interface circuits while reducing power dissipation and parasitic levels.

Among many available integrated circuit fabrication technologies, complementary metal-oxide-semiconductor (CMOS) is being used more and more in high-speed communications systems dominating the market [1]. This domination results in enormous research sources spent on the improvement of CMOS technology. The performance improvement is obtained by reducing the minimum channel lengths of the field effect transistors (FETs). The development of sub-micron CMOS fabrication lines with transistor ft values in excess of 60 gigahertz (GHz) [2] has allowed for the rapid expansion of CMOS circuits into frequency ranges historically dominated by more complex technologies such as BiCMOS and GaAs. Since CMOS provides the ability to integrate both analog and digital circuits on the same chip, high frequency system-on-chip (SoC) designs using standard CMOS have become more attractive due to CMOS' high-integration and high-yield capabilities.

A VCO can be built using ring architectures, relaxation circuits, or an LC resonant circuit. The LC design has the best phase-noise [3] and frequency performance [4] owing to the large quality factor Q achievable with resonant networks. However,

adding high quality integrated inductors to a CMOS process flow increases the cost and complexity of the chip, and also introduces problems such as the control of eddy currents in the substrate. Ring oscillators, on the other hand, can be built in any standard CMOS process and may require less die area than LC designs. The design is straightforward and ring architectures can be used to provide multiple output phases and wide tuning ranges. Wider tuning range and the multiple output phases of ring oscillators are especially useful for some specific applications including frequency synthesizers and oversampling circuits.

The challenges found in the design and implementation of high frequency low noise CMOS voltage controlled ring oscillators to be used in PLLs and standalone multi-GHz communications applications provide the main motivation for this research.

1.2 Thesis Organization

In chapter two, major VCO types are introduced with a brief discussion of the oscillator fundamentals. Chapter three starts with a first-order frequency domain analysis of ring oscillators and then describes the basic architectural choices for ring designs, i.e. single-ended or differential. Some published techniques that improve the overall characteristics of ring oscillators are also presented in this chapter. In chapter four, existent oscillator phase noise models are reviewed in detail, and generalization of them to N-stage rings is described. After discussing design techniques for implementing high-frequency low-noise CMOS voltage controlled ring oscillators in chapter five; in chapter six, it is demonstrated how to actually apply these techniques in sub-micron CMOS technologies by introducing various high-performance ring VCO designs. In addition to the phase noise and maximum frequency of the oscillators, other important characteristics, such as the tuning range and the stability under parameter variations, are also analyzed in chapter six. Chapter seven introduces the design of two different conventional ring oscillators, which was aimed to provide a

frame of reference for the introduced designs. Next chapter, chapter eight, provides experimental results of a prototype chip that was implemented to verify and validate the theoretical and simulation results presented in the previous chapters. In the following chapter, chapter nine, designed VCOs are compared with other ring and LC oscillators published in the open literature. Finally, in chapter ten, a brief summary of the introduced work is presented along with discussions on the major contributions of this work and the future directions.

CHAPTER II

INTEGRATED OSCILLATORS

2.1 *Oscillator Principles*

Oscillators are usually characterized by using linear analysis techniques. This approach is common although they are highly nonlinear feedback systems. The resulting frequency-domain (or s-domain) analysis cannot yield the exact response. Nevertheless, frequency-domain analysis techniques are applied to the oscillators to gain insight about the operation and they work particularly well for oscillators using analog gain stages. Linear system-analysis proves to be a reasonable first-order approximation for most cases.

An oscillator is a system employing positive feedback. As shown in Figure 1, it is constructed from an amplifier block and a frequency-selective network connected in a positive-feedback loop. Although an actual oscillator does not have an input $X(s)$ to drive the oscillator as shown in Figure 1, the assumption of this input signal simplifies the s-domain analysis of the feedback loop. A simple analysis of this system shows that the transfer function can be written as [5]

$$H(s) = \frac{X(s)}{Y(s)} = \frac{A(s)}{1 - A(s)\alpha(s)} \quad (1)$$

where $A(s)$ is the s-domain transfer function of the amplifier block, and $\alpha(s)$ is the s-domain transfer function of the frequency-selective network. Let us define the loop gain $L(s)$ as

$$L(s) = A(s)\alpha(s) \quad (2)$$

where $L(s)$ is simply the open loop gain of the loop.

According to the standard oscillator definition, this system must have a finite

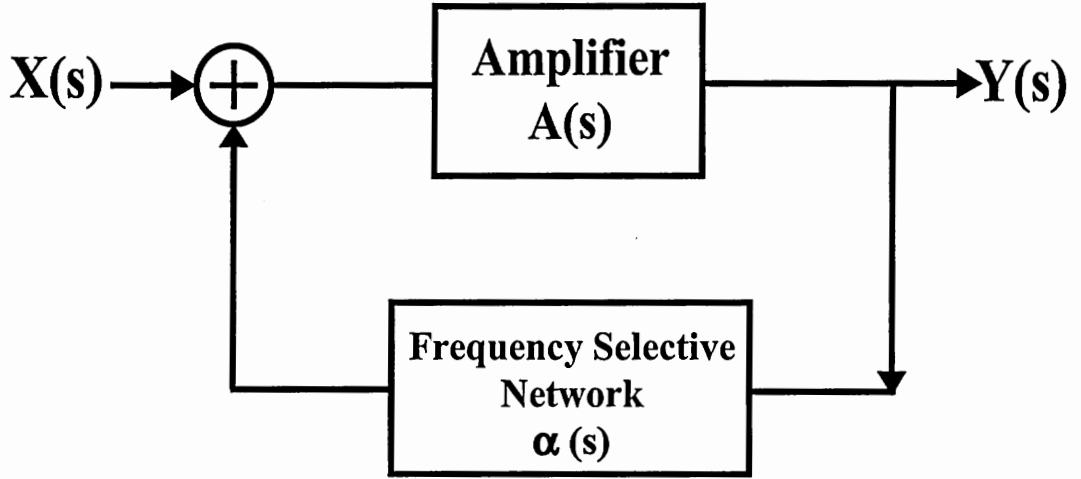


Figure 1: Positive feedback oscillatory system modeled in s-domain

output even in the absence of an input signal. From the above equations, it is easily seen that this condition occurs if the transfer function converges to infinity at a specific frequency, implying that the loop gain $L(s)$ should be equal to one at this frequency. Thus the magnitude of the loop gain should be equal to unity and the phase of the loop gain should be an integer multiple of 2π for the feedback loop to provide stable oscillations. This condition is called the Barkhausen criterion. Note that this criterion only guarantees that the oscillation will be sustained after it starts but it does not guarantee that the oscillation will start. Practically, the magnitude of the loop gain should be designed to be slightly larger than unity for the oscillation to start. This suggests that because of the positive feedback, any possible oscillation will grow indefinitely unless there is a nonlinear mechanism to stop the growth of the signals. Older designs use nonlinear amplitude control circuitry to achieve this but modern integrated oscillator designs usually rely on the hard-limiting of the power supplies and the gain drop of FETs at large signal levels. Physically, any internal noise in the system at the specific oscillation frequency will be amplified by the help of the positive feedback gain, resulting in a periodic signal at the output. The gain of the feedback will then drop to unity as the signals get larger because of the amplitude limiting mechanism to yield a steady-state oscillatory signal.

The gain of the loop function determines if the oscillator will start or not but it is the phase characteristics of the feedback loop that determines the oscillation frequency. From the previous discussion, the feedback system oscillates when the phase is zero or an integer multiple of 2π . This leads one to the conclusion that the frequency stability of an oscillator depends on how the phase characteristics $\phi(\omega)$ of the loop varies with changing frequency. Large values of $d\phi(\omega)/d\omega$ indicates an oscillator with a stable output frequency since any change in loop phase, which can occur due to a slight variance in one of the circuit parameters or temperature, will correspond to less disturbance at frequency and vice-versa [6]. The relation of this simple statement with the Q-factor of an oscillator will be discussed in the following chapters.

2.2 Types of Integrated Oscillators

Integrated VCOs for high-frequency communications applications can be implemented using ring architectures, relaxation circuits, or LC based networks. Among these, LC oscillators have the best phase-noise [3] and frequency performance [4] because of their use of passive resonant elements with high quality Q factors. LC oscillators have been constructed using bonding wires, integrated inductors, or external inductors. Using external parts, however, raises the cost of the system and introduces other problems such as increased parasitic levels and increased power dissipation; therefore fully monolithic designs are highly desirable. There are other problems related with the utilization of bonding wires as the high Q inductor of the LC oscillator such as the lack of accurate control of the inductance value. In state-of-the-art CMOS processing, it is possible to fabricate integrated inductors with high quality factors ($Q \sim 85$ [7]). They can be implemented monolithically at the expense of adding processing steps that significantly increase the cost and the complexity of the system. Micro-Electro-Mechanical-Systems (MEMS) designers, for example, use various etching techniques

to obtain high-performance monolithic inductors. Addition of inductors to a CMOS process also introduces problems such as the control of eddy currents in the substrate and magnetic coupling.

Ring oscillators, on the other hand, are suitable for monolithic system design using any digital CMOS fabrication process. Ring designs may require less die area when compared to the LC counterparts because of the lack of area-consuming passive elements (inductors and varactors). In addition, the design of ring oscillators is straightforward using integrated circuit design techniques. Other properties of ring oscillators, such as the availability of multiple phases at the output and the wide tuning range can be useful for some specific applications including frequency synthesizers and oversampling circuits. These characteristics of ring oscillators lead to the conclusion that they are still important in modern integrated communications systems. As implied above, the noise performance of a ring oscillator is generally worse than LC oscillators because of the low quality factor Q of the ring structure [6, 8]. However, by using different ring architectures and circuit techniques, it is possible to achieve frequencies and noise levels comparable to LC designs.

The final candidate for the high frequency integrated VCO design is the relaxation oscillator. A relaxation oscillator employs the same elements as a ring oscillator without the need for high-quality inductors. The only difference is the use of an additional capacitive element. This is in contrast to high-speed ring oscillator designs, which utilize the capacitive parasitics of the metal-oxide-semiconductor (MOS) transistors. Only a few CMOS relaxation oscillator designs have been published, with the fastest running at 900 MHz [8]. They also do not match the noise performance of LC and ring oscillators because of their relatively low effective quality Q factor.

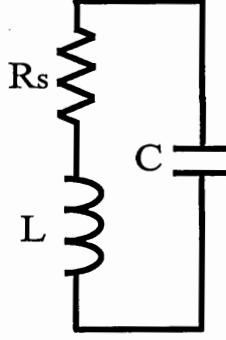


Figure 2: Resonator tank model

2.2.1 LC Oscillators

The core of an LC oscillator is a resonator tank that is constructed from on-chip inductors and varactors. This tank performs as the frequency-selective network that was shown in the oscillator model of Figure 1. As shown in Figure 2, the resonator tank can be simply modelled as a parallel connected LC network along with the series parasitic resistance R_s of the inductor. As discussed before, the tank might have a very high quality Q factor; however, the tank, alone, is not sufficient for steady oscillations because of the energy loss on the parasitics. After excitation, the resonator will only oscillate for approximately Q many cycles until all the stored energy is dissipated on the R_s unless the energy loss is accompanied for. Therefore, every LC oscillator employs an active circuitry that cancels the parasitic resistance with its negative effective resistance by providing the required energy at every cycle. This active circuitry is shown as the $-R$ component in the oscillator model of Figure 3. The frequency of the LC oscillator is strictly determined only by the characteristics of the resonator, that is $\omega_r = (1/\sqrt{L_{eq}C_{eq}})$, and ideally is not effected by the active circuitry if the capacitive loading of the $-R$ element is ignored.

2.2.2 Oscillators w/o Resonators: Ring Oscillators

It is interesting to note that although the oscillator model in Figure 1 contains an amplifier and a frequency-selective network, it is possible to build oscillators that

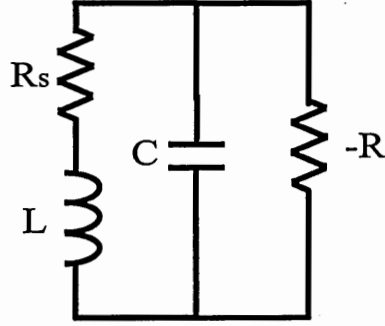


Figure 3: LC oscillator model

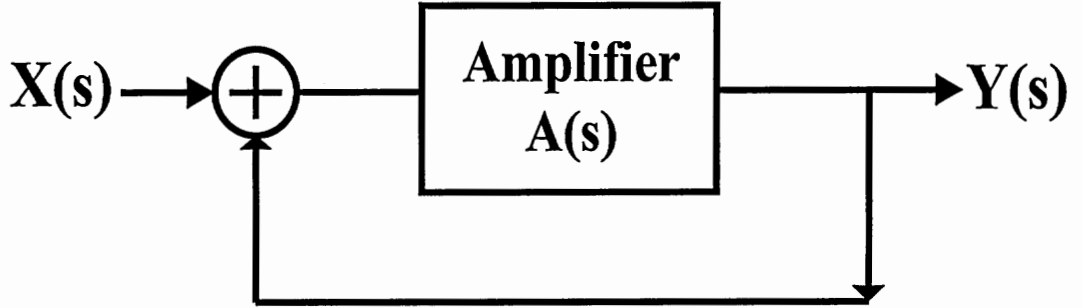


Figure 4: Ring oscillator block model

satisfy the Barkhausen criterion without any resonator. As illustrated in Figure 4, a ring oscillator is the most widely used type that does not contain a frequency-selective structure. The lack of a high-Q resonator makes it harder to obtain sufficient noise and frequency performance especially for high-frequency RF applications. Nevertheless, ring oscillators are extensively used in communications systems due to their simplicity and ease of implementation. Furthermore, various optimization and circuit design techniques are available to boost their performance close to their LC counterparts.

A basic ring oscillator consists of an odd number N of inverter stages connected in a positive feedback loop. Therefore there are an odd number of inversions in the loop. If one of the nodes is excited, the pulse will propagate through all the stages and will reverse the polarity of the initially excited node. The frequency of the oscillation will be $1/(2 * N * T_d)$ where T_d is the propagation delay of a single stage. Ring oscillators will be discussed extensively in the following chapters.

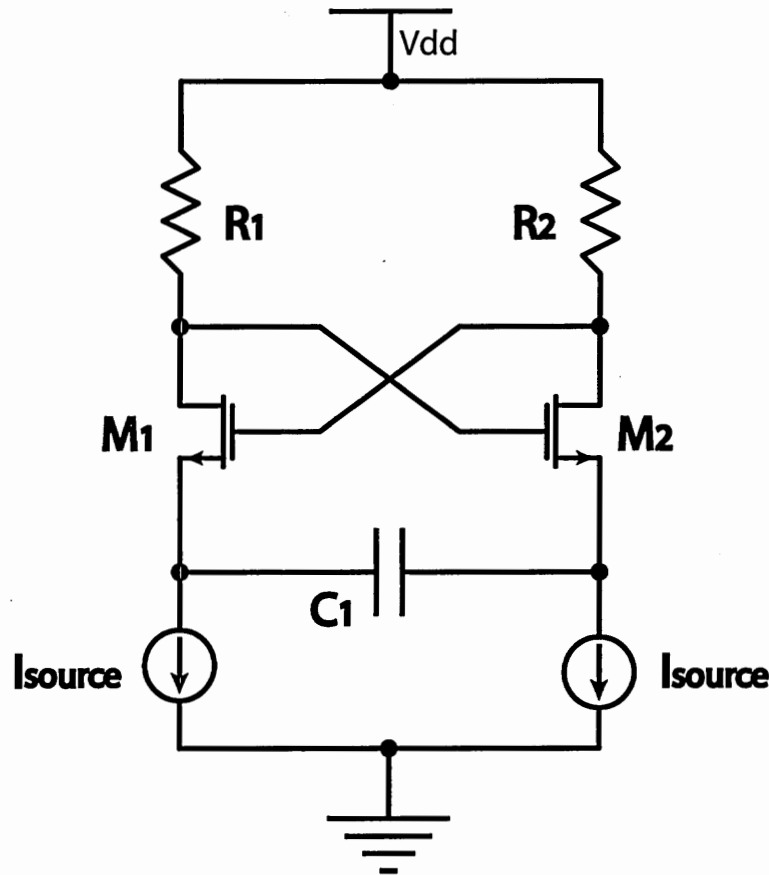


Figure 5: Relaxation oscillator

2.2.3 Oscillators w/o Resonators: Relaxation Oscillators

The other type of oscillator that lacks a frequency-selective network is the relaxation oscillator. The operation of a relaxation oscillator is similar to that of a multivibrator. In each cycle, a capacitor is charged by an active element, a transistor most of the time, until a predetermined threshold is exceeded to trigger an event which quickly discharges the capacitor. After returning to the initial state, this cycle is repeated to yield a steady state oscillation. Schematics of an example integrated design is shown in Figure 5 [8].

Relaxation oscillators can be built in a standard CMOS process with less complexity even when compared to ring oscillators due to the single-stage design. At high frequencies, however, they are harder to stabilize due to diminishing hysteresis, which

is required for a stable oscillation. They also do not match the noise performance of LC and ring oscillators because of their relatively low effective quality Q factor [8].

2.3 Important Characteristics of Oscillators and Applications

The important characteristics of an oscillator strongly depend on the application. Multiple-GHz RF communications systems, for example, are probably the most demanding of all applications. Because of the extremely lossy transmission media (air), the receiver circuitry is required to have exceptionally low noise levels to reduce the BER of the received signal. The design of data/clock recovery networks or frequency synthesizers employing PLLs, therefore, is very challenging in RF applications. LC oscillators are most widely used in these systems because of their low noise characteristics although some ring designs come close to challenging LC counterparts at lower frequencies [9,10].

Most systems requiring a high-frequency VCO, on the other hand, have more relaxed noise requirements. When the transmission media is closer to being ideal, such as in fiber-optical data transmission systems including local area network transceivers and DSL transceivers, noise specifications may ease a bit [11]. Clock generators, which are used to supply the timing information to microprocessors, digital signal processing systems, and dynamic random-access memory arrays, do not have such strict noise specifications and modern ring oscillator designs are usually sufficient for these applications. Zero delay clock buffers usually employ PLLs with ring oscillators for synchronizing the timing of circuits at different parts of the chip or the printed circuit board (PCB) reducing clock skew and timing errors.

Maximum frequency required from an oscillator depends on the data transmission and/or data processing rate specifications of the system. Design of higher frequency systems are more challenging due to a number of reasons. First of all, the switching

capability of a transistor is limited by the characteristics of the fabrication process. Maximum switching speed is usually limited to approximately $1/5$ of the transistor f_t (unity gain frequency) of the process. In a standard $0.25\ \mu\text{m}$ CMOS technology, for example, f_t is approximately 25 GHz. An LC oscillator's center frequency appears to depend only on the inductance and the capacitor values such that reducing them would increase the frequency. The maximum frequency, however, cannot be indefinitely increased due to the reduction of the self-resonance frequency of the inductor and the parasitic capacitances. Furthermore, other specifications of the oscillator get more stringent when operation frequency is increased. Noise requirement of the system is an example. With increasing data transfer speeds, the clock periods become shorter, decreasing the amount of absolute timing uncertainty (jitter) that can be tolerated at the output. Finally, there are other problems related with the design of systems when operation frequencies exceed a few GHz such as the skin effect or the increased bulk-node currents.

Power dissipation of a system is directly dependent upon the data transmission and/or processing rate of the system. That is, a faster system dissipates more power which can be seen from the dynamic power dissipation equation [5]

$$P = V_p^2 C_L f, \quad (3)$$

where P is the power that is dissipated on a node with capacitance of C_L oscillating at a frequency of f with a peak voltage amplitude of V_p . Power dissipation may not be significantly important if the system does not depend on batteries to operate, i.e. if it is not mobile. Even for such cases, extreme power dissipation is not desired because of the problems related with the increase in temperature of the system due to high power dissipation. Noise characteristics of a circuit also depend on the maximum available power. Larger signal levels correspond to better signal-to-noise-ratio (SNR) improving the phase noise of the oscillator.

Stability of the system under parameter variations is another important issue.

The output parameters of the system should stay inside the specifications when the temperature of the system is varied as specified. Changes due to fabrication parameter variations are really an issue of yield and must be minimized to increase the yield, which in turn reduces the cost. Military rated products are the most demanding ones in that sense requiring the circuit to operate at extreme conditions.

Other than these major issues, there are some other desirable properties of oscillators in some specific applications. Analog-to-digital converters (ADC) or over-sampling networks, for example, benefit from multiple output phases of the clock generator. Some of these networks use sampling circuitry with multiple clock inputs, each individually triggering the sampling event at signal transitions, to multiply the sampling rate by the number of available phases. Multiple phases are naturally available from ring oscillators although a couple of ring LC designs were published in the literature [12,13] to supply multiple phases. Tuning range of an oscillator is another characteristic that needs close attention. Narrow tuning range may create problems in meeting the frequency specification with a single fabrication run, and multiple iterations may be necessary. On the other hand, wide tuning range increases the gain of the VCO resulting in a higher sensitivity to control line noise. Therefore, the tuning range of a VCO should be optimized according to the specifications of the application. Generally ring oscillators have much wider tuning range than their LC counterparts although there are different design techniques available to implement wide tuning range LC oscillators (digital tuning and analog tuning applied together) [14].

CHAPTER III

CMOS RING OSCILLATORS

3.1 Ring Oscillator Basics

As discussed in the previous chapter, the Barkhausen criterion for oscillation can be satisfied with a positive feedback loop that does not contain any frequency-selective elements. Referring to the oscillator model of the previous chapter, a ring oscillator can be constructed by closing the feedback loop around an amplifier block while an LC oscillator needs both the amplifier block and the frequency-selective network to operate properly. A ring oscillator is realized by connecting a number of amplification stages in series, as shown in Figure 6. Then, the loop is closed by connecting the output of the last element to the input of the first element forming the positive feedback.

The most basic ring oscillator employs single-ended inverters in place of the amplification stages. In this case, an odd number N of inverter stages is needed for steady oscillations. Otherwise the oscillator latches up at a DC level which corresponds to the satisfaction of Barkhausen criterion at zero frequency. From another perspective, an odd number of stages will oscillate because if one of the nodes is excited, the pulse

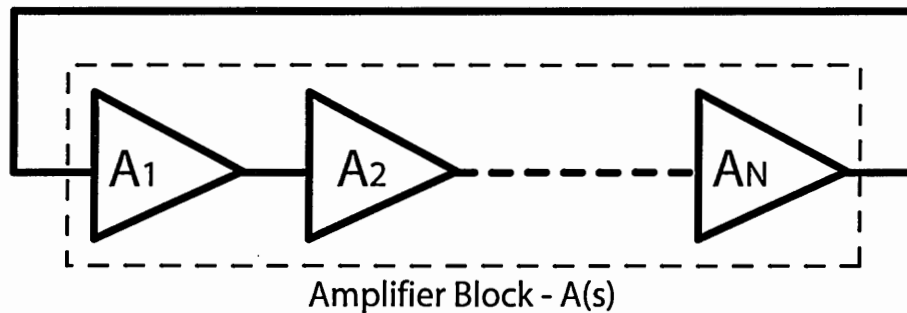


Figure 6: Ring oscillator structure

will propagate through all the stages and will reverse the polarity of the initially excited node starting the oscillations. On the other hand, for an even number of stages, the pulse will still propagate through the stages but will not reverse the polarity of the initial node. In the previous chapter, it was already implied that the frequency of the oscillation will be $1/(2 * N * T_d)$ where T_d is the propagation delay of a single stage for this case.

3.1.1 Frequency Domain Analysis

This discussion, however, does not tell anything about the oscillation criteria of ring oscillators when different types of stages are used or when a differential architecture is utilized. Therefore, let us generalize this discussion to ring oscillators with gain stages that can be characterized by a transfer function. In this case, we can define the loop gain $L(s)$ as

$$L(s) = A_1(s)A_2(s)A_3(s)...A_N(s) \quad (4)$$

where $A_1(s)$, $A_2(s)$, $A_3(s)$, and $A_N(s)$ are the s-domain transfer functions of individual delay stages. For most practical applications, the gain stages are identical so that the loop gain reduces to

$$L(s) = A^N(s) \quad (5)$$

where N is the number of stages, and $A(s) = A_1(s) = A_2(s) = A_3(s) = A_N(s)$.

According to the Barkhausen criterion, the total phase difference should be equal to a multiple of 2π and the magnitude of the loop function should be equal to one. This implies that a single stage should be able to provide a phase shift of $2k\pi/N$ at the unity gain frequency, where k is an integer. Therefore, the oscillation criterion can be alternatively written as

$$\angle A(j\omega_0) = 2k\pi/N \quad \text{and} \quad (6)$$

$$|A(j\omega_0)|^N = 1 \quad (7)$$

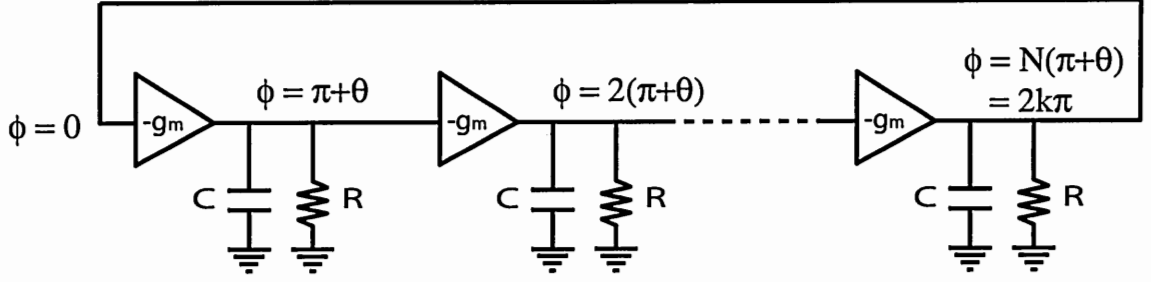


Figure 7: Ring oscillator linear model

for ring oscillators at the oscillation frequency. If the ring oscillator stages are replaced with their linear equivalents, i.e. small-signal equivalents that consists of a negative transconductance and an RC load, the simple ring loop can be redrawn as given in Figure 7. In this model, every stage has a phase shift of $(\pi + \theta)$ as shown on the figure, π coming from the DC inversion and θ from the RC load delay. To satisfy the oscillation criteria, the total phase shift around the loop must be equal to a multiple of 2π , with $N\pi$ of this supplied by the odd number of inversions in the loop. The general practice is to minimize the required phase shift to reduce the number of the required stages and, therefore, the total phase shift of the RC delays should be equal to $\pm\pi$. Now, θ can be written as

$$\theta = \pm \frac{\pi}{N}. \quad (8)$$

Next, using this phase relationship among the stages, oscillation frequency can be found after a simple derivation. From the given linear model, the transfer function of a single stage can be written as

$$A(j\omega) = \left[\frac{-g_m R}{1 + RCj\omega} \right]. \quad (9)$$

At the oscillation frequency, phase of this transfer function is

$$\angle A(j\omega_0) = -\tan^{-1}(RC\omega_0) \pm \pi. \quad (10)$$

Note that, because of the phase criteria that was found above, we also have $\angle A(j\omega_0) = -(\pi + \theta)$. Equating these two relations, we can get

$$\tan^{-1}(RC\omega_0) = \theta, \quad (11)$$

and finally the oscillation frequency can be found as

$$\omega_0 = \frac{\tan(\theta)}{RC}. \quad (12)$$

This reduces to $\sqrt{3}/RC$ for a three-stage ring and $1/RC$ for a four-stage one.

Phase requirement is automatically satisfied for different ring loops because of the connections in the loop, assuming that the structure oscillates. However, the gain requirement as given in Equation (7) should also be satisfied. By replacing $|A(j\omega_0)|$ with $(g_m R)/(\sqrt{1 + (RC\omega_0)^2})$, the gain requirement can be written as

$$\left[\frac{g_m R}{\sqrt{1 + (RC\omega_0)^2}} \right]^N = 1. \quad (13)$$

By substituting $RC\omega_0$ with $\tan\theta$ using the frequency relationship found above, this can be reduced to

$$(g_m R)^N = \frac{1}{\cos^N \theta}. \quad (14)$$

Since g_m , R , and $\cos\theta$ are positive identities as defined before, we can cancel the N_{th} exponents and simplify this argument as

$$g_m R \geq \frac{1}{\cos\theta}, \quad (15)$$

remembering that the gain should at least be equal to one at the oscillation frequency. Therefore, the gain requirement of a three-stage loop is $g_m R \geq 2$, whereas the requirement is $g_m R \geq \sqrt{2}$ for a four-stage one. This equation shows that it is easier to satisfy the criteria for longer chains because each stage is required to have a smaller gain at the oscillation frequency.

When single-pole amplifier stages are used in a regular oscillator loop, the minimum required number of stages is three. According to the analysis provided in this section, this is because a single-pole amplifier stage can provide only $\theta = \pi/2$ phase shift at an infinite frequency. Designs employing only two stages utilizing multiple-pole gain stages have been published [15–17].

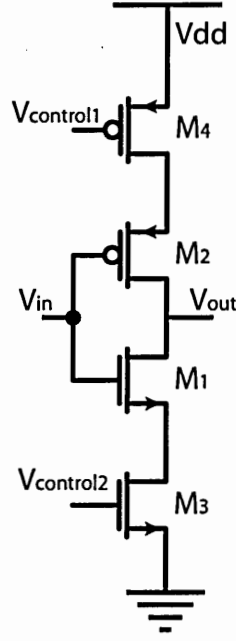


Figure 8: Current starved inverter

3.2 *Single-Ended Ring oscillators*

The simplest ring oscillator designs employ a single-ended architecture, which was already shown in Figure 6. Single-ended structures are usually preferred over the differential architectures whenever the simplicity is essential. They are also desirable when power dissipation is the most important consideration since they include less number of active elements that dissipate power.

The most widely used single-ended ring oscillator stage is a CMOS inverter that consists of an NMOS transistor and a PMOS transistor. This design, however, does not include any means to control the operation. A control method can be added in various ways, such as by changing the strength of an inverter in the loop, by changing the loads, or by varying V_{dd} . Figure 8 shows an implementation where the strength of an inverter is changed by adding two more transistors, M3 and M4, to the inverter structure, which is called the current starved inverter. Figures 9(a) and 9(b) illustrate how the load can be modified to tune the frequency of oscillation, and Figure 10 demonstrate how V_{dd} can be used to tune the frequency.

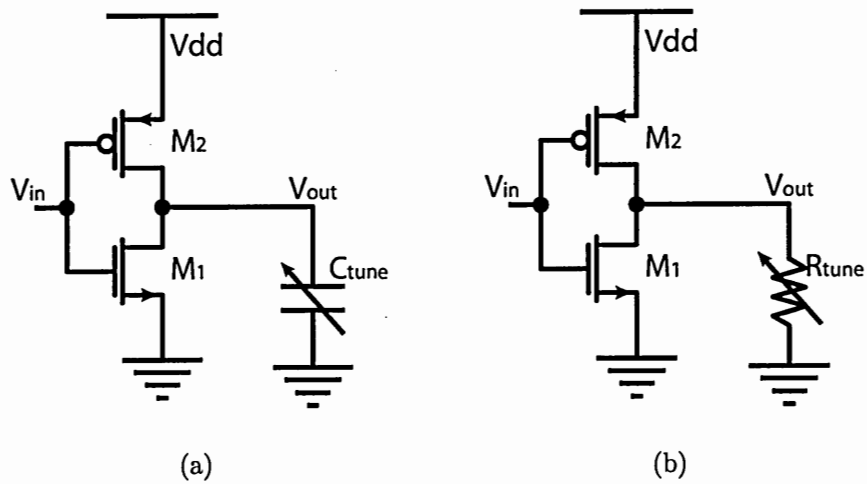


Figure 9: (a) Capacitive load control, (b) Resistive load control

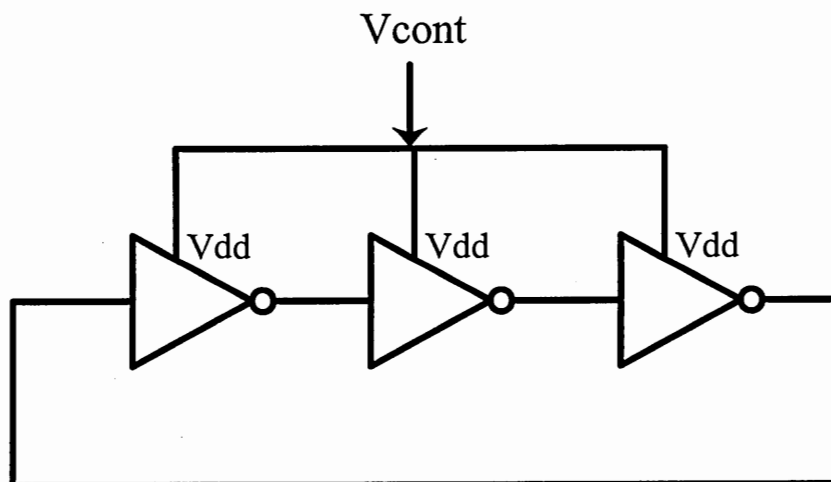


Figure 10: Frequency tuning by control of V_{dd}

Note that load tuning is not widely used for single-ended ring oscillators because of the difficulty in implementing controllable resistors and capacitors in CMOS technologies. Although power supply control can be used for both single-ended and differential ring oscillator architectures, use of a low power supply voltage results in smaller output swings. This results in a reduction in the phase noise performance and the circuits get more susceptible to supply and ground disturbances. Shift of DC levels with the change of supply voltage is also undesirable.

Although this type of stage offers great simplicity, an output with digital voltage levels, and fast operation, adding the electronic control transistors reduces some of the desirable features of the inverter-based design. The single-ended construction makes it susceptible to common mode problems such as power supply and substrate bounces. In addition, the output does not provide a 50% duty cycle under practical conditions, and it is more susceptible to process and temperature variations when compared to oscillators incorporating standard current control techniques. This type of oscillator can be useful either as a benchmark design for comparison [18–20] or for testing new architectural techniques [21] where it is preferred because of its simplicity.

3.3 Differential Ring oscillators

Single-ended ring oscillator structures are not widely used in state-of-the-art high-frequency communications systems. Differential architectures tend to be preferred over the single-ended designs because of their inherent advantages. This includes better immunity to common-mode noise, improved spectral purity, and 50% duty cycle at the output. Differential ring oscillators can be constructed with an even number of stages, unlike their single-ended counterparts. The required extra phase shift (π) can be obtained by reversing one of the connections in the architecture introducing a DC phase inversion. Figure 11 shows a four-stage differential ring oscillator where the DC phase inversion is between the fourth and the first stages.

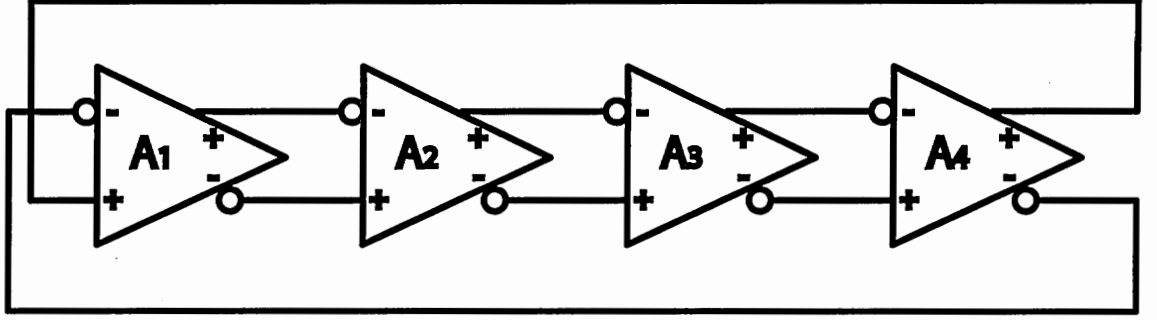


Figure 11: 4-Stage differential ring oscillator

The most widely used differential ring oscillator stage is perhaps the differential pair with active loads and a tail current supply. The differential pair is utilized frequently in analog circuit designs, even in high-frequency digital networks employing current switching techniques. It is, therefore, considered to be well studied in terms of noise and small-signal transfer characteristics. Figure 12 shows the simplest differential pair structure, with active loads biased in the saturation region. Note that, although the frequency control appears to be through the input node $V_{control}$, general practice is to use a current mirror and to control the stage using the mirrored current, as illustrated in Figure 13.

Assuming full switching of the mirrored current by the differential pair, the delay of the differential stage in Figure 13 can be written as

$$T_D = \frac{C_L V_{p-p}}{I_{control}} \quad (16)$$

where C_L is the total load capacitance at each output node, V_{p-p} is the voltage swing at the output, and $I_{control}$ is the mirrored current. Therefore, the oscillation frequency of an N stage ring oscillator employing this stage is

$$f_{osc} = (2 * N * \frac{C_L V_{p-p}}{I_{control}})^{-1} \quad (17)$$

From this equation, one can see that the oscillation frequency of the oscillator can be controlled linearly by varying the mirrored current. Note that this structure does not offer any way to control the output DC voltage levels or the output amplitude.

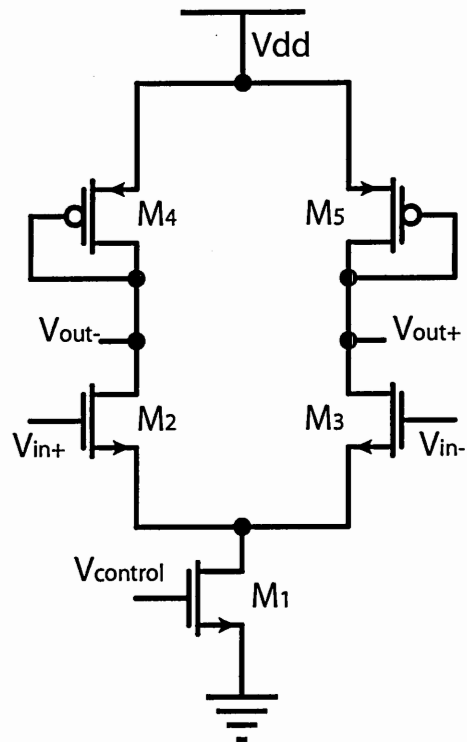


Figure 12: Simple differential pair

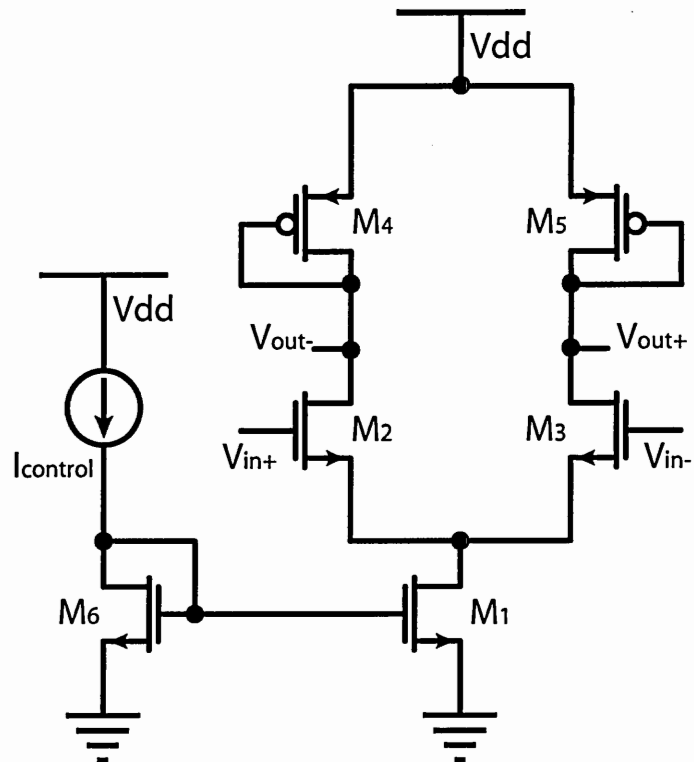


Figure 13: Differential pair with current mirror

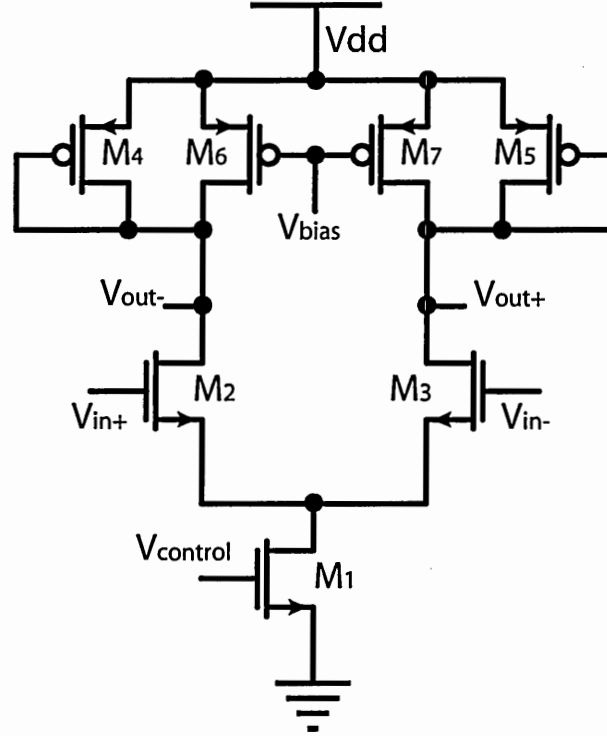


Figure 14: Differential pair with symmetrical loads

As the control currents are varied, the DC levels of the output will fluctuate. This may create a problem if the output signal is used to drive circuitry that is sensitive to the input DC levels. In addition, an amplitude control option might be desirable to limit the output signal amplitude.

One improvement on the simple active load differential pair structure is the use of symmetrical loads, as shown in Figure 14 [21]. Each load consists of a PMOS transistor pair. One PMOS device is biased in the triode region with an additional bias circuitry, while the other is a diode-connected transistor biased in the saturation region. This load provides symmetrical I-V characteristics and an amplitude control option through V_{bias} , which is used to change the resistance of the triode-region transistors. This way, the output swing is kept between V_{dd} and V_{bias} . In addition, the symmetrical load configuration makes it easier to achieve the necessary gain for sustaining the oscillation since the transconductances (g_m) of the load transistors does not directly depend on the control current. Note that the utilization of symmetrical

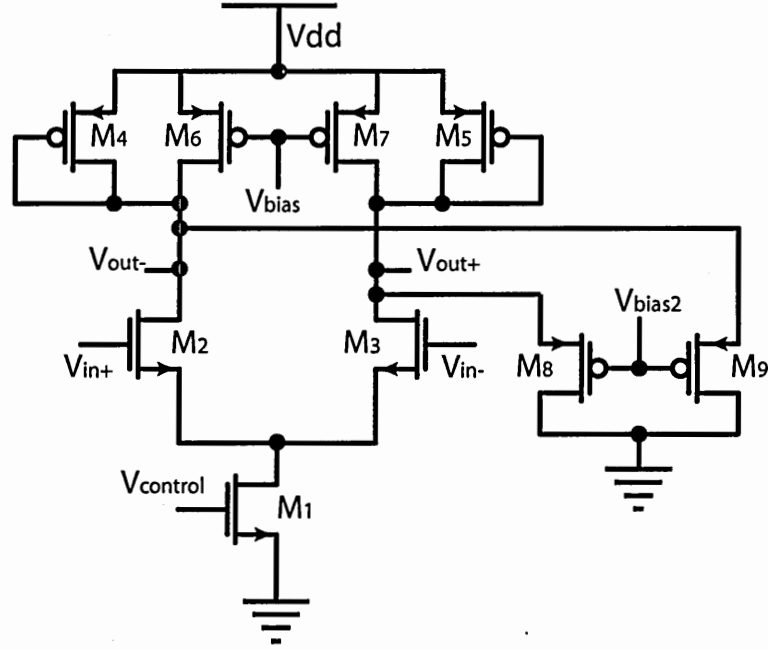


Figure 15: Differential pair with symmetrical loads & amplitude control circuitry

loads may not be the best choice for a low-noise VCO since this configuration is more susceptible to deterministic jitter because of device mismatches [22].

A more complicated design that exhibits better amplitude and output DC level control is shown in Figure 15. This is a differential pair with symmetric loads. Additional transistors, M8 and M9, are utilized as a voltage limiter. V_{bias} controls the lower limit of the output voltage, while V_{bias2} controls the upper limit of the output voltage such that the output swing is between $V_{bias2} + V_{Tp}$ and V_{bias} . One problem with this scheme is that the additional active devices may decrease the maximum frequency and increase the phase noise. Resistor loading can be used instead of transistors to increase linearity and to decrease $1/f$ (flicker) noise. This implementation, however, requires more layout area and high-quality resistors.

3.4 Ring oscillator Design Challenges and Techniques

In the previous chapter, the important characteristics of oscillators in various applications were discussed. A single-loop ring oscillator with an inverter stage or a differential pair stage may be sufficient for some low performance applications. Enhanced designs, however, can be introduced when better performance or improved characteristics are critical. Important characteristics of ring oscillators include maximum frequency, phase noise, and robustness. This section briefly discusses some of the design techniques that might be used to improve these characteristics of ring oscillators.

3.4.1 Frequency

The oscillation frequency of a ring design is directly dependent upon the total delay around the loop. For a fixed number of stages, the maximum oscillation frequency is limited by the minimum delay of a single stage. This delay can be reduced to increase the oscillation frequency by modifying the stage design. However, there is a limit to this reduction imposed by the characteristics of the fabrication process. Another way to increase the oscillation frequency is to decrease the number of stages. Most practical ring oscillators need at least three stages to sustain stable oscillations, although [15–17] introduce ring oscillators using only two stages. The delay stages used in these oscillators, however, cannot be approximated as having a dominant pole and the available number of phases is limited. There are also other architectural techniques that can be used to increase the maximum frequency of ring oscillators. Some of these include the use of feedforward architectures [9, 23–27], output interpolation methods [28], and coupling [15].

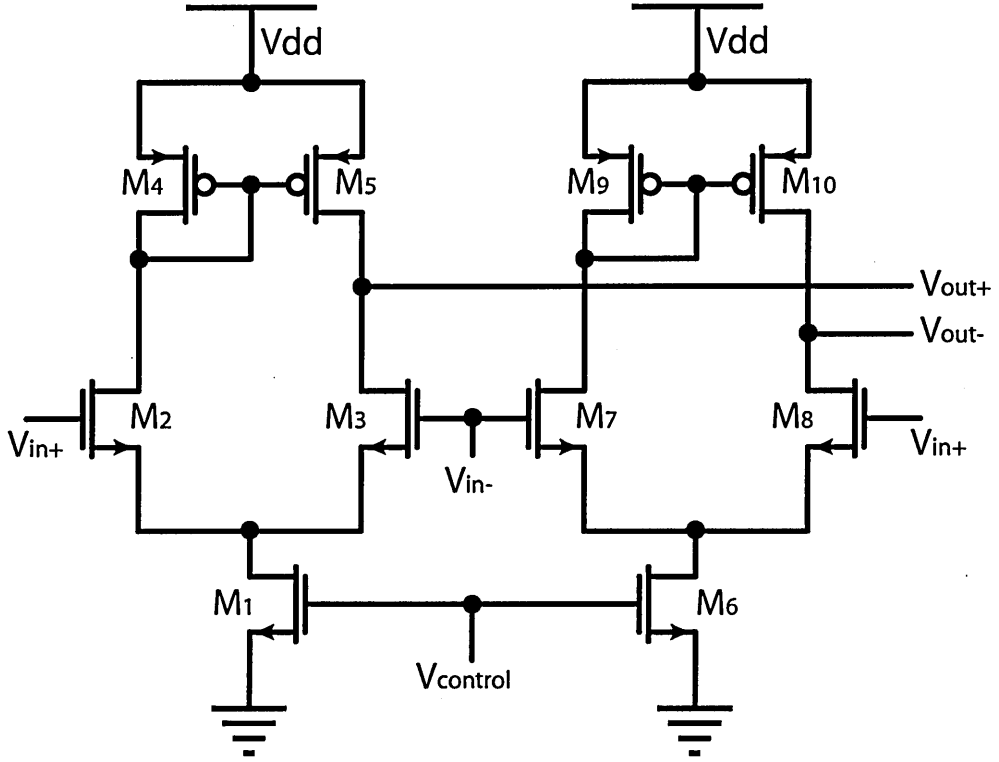


Figure 16: Double differential delay stage

3.4.1.1 Two-Stage Ring Oscillators

As discussed previously, to satisfy the Barkhausen oscillation criterion, one must use a minimum number of three stages for a ring oscillator with single-pole delay stages. For some applications such as image rejection and delay interpolation, however, in-phase/quadrature (I/Q) outputs might be necessary. Minimum practical number of delay stages that can be used for obtaining I/Q outputs is "four." An increase in the number of stages, however, may not be desirable because it increases the power consumption and decreases the maximum frequency. One solution to this problem is incorporating a two-stage design. Figure 16 shows a two stage ring oscillator employing a double differential gain stage to supply the required extra phase and gain [17].

The small-signal characteristics of the half-circuit are similar to a differential amplifier with a current mirror load. The current mirror load doubles the gain of the

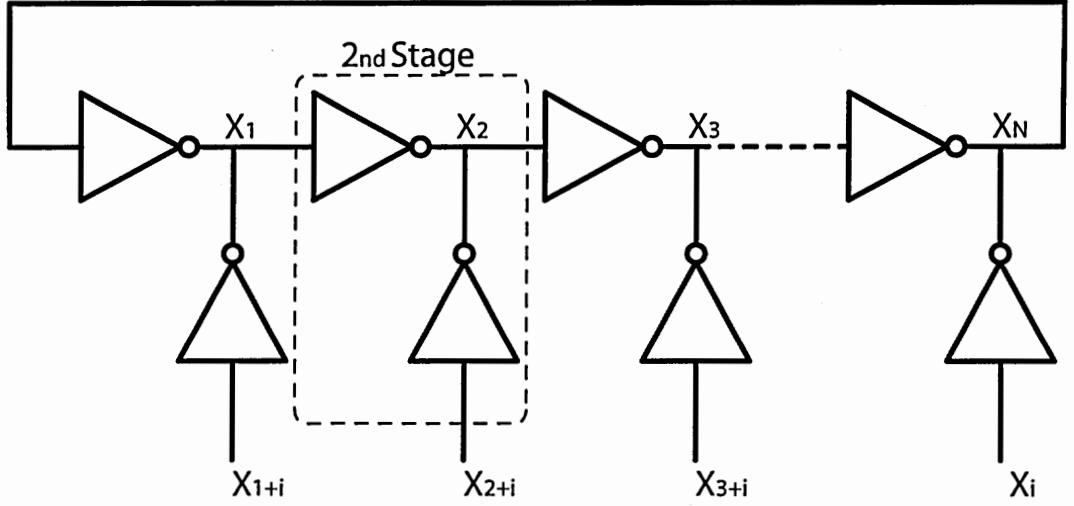


Figure 17: Subfeedback loop architecture

differential amplifier by folding the small signal current at one side and by combining it with the small signal current of the other side. When compared to the standard differential pair stage, this design inhibits an additional pole-zero pair resulting from the extra nodes created at the drains/gates of the unbalanced current mirror loads. This supplies the required extra phase shift to sustain a steady oscillation.

3.4.1.2 Subfeedback Loops

Sun [23] proposes a method that increases the maximum frequency while retaining the number of phases at the output by the use of subfeedback loops. As illustrated in Figure 17 for an oscillator with N gain stages, N intercoupled subfeedback loops are created by nesting additional stages outside the main loop. The frequency of oscillation is controlled by altering the strength of the subfeedback loops and the main loop by routing the power distribution. A minimum number of stages are used for each subfeedback loop, so that the oscillation frequency can be tuned between that of an N -stage ring oscillator and a three-stage ring oscillator. This gives a wide tuning range and a high oscillation frequency while retaining the amount of output phases. Subfeedback loops with a different number of stages can be used in different applications. One problem is that, if the number of stages in the subfeedback loops

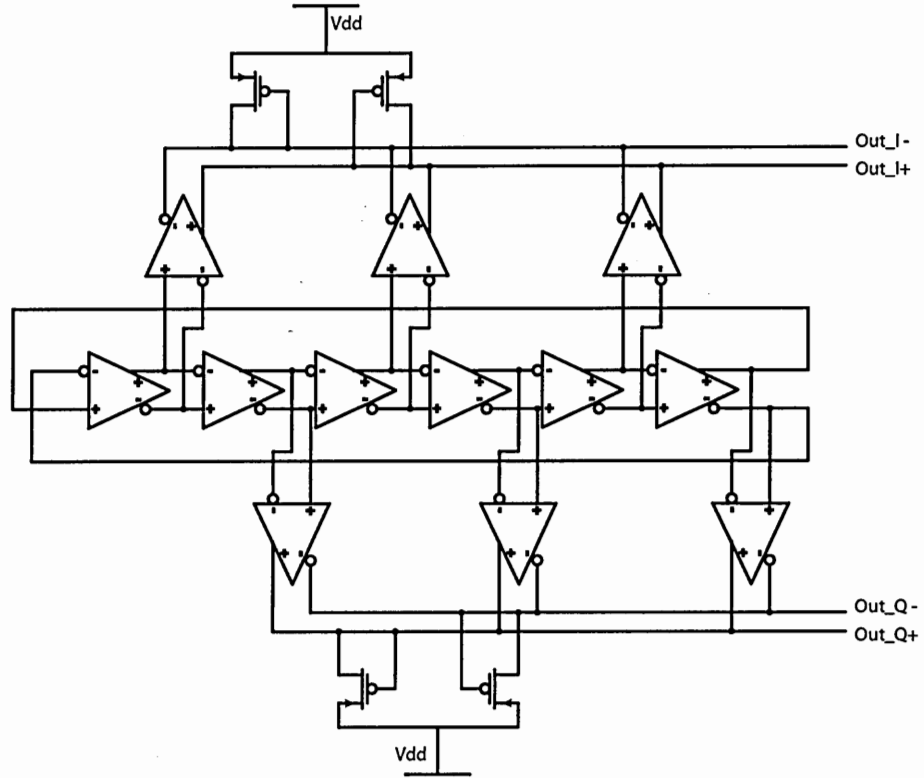


Figure 18: Output interpolation technique

is not chosen carefully, the maximum frequency may decrease. A detailed analysis of this technique that describes how to select the number of stages in the main-loop and the subfeedback loops is discussed in [23].

3.4.1.3 Output Interpolation Technique

The output interpolation technique relies on combining the outputs of several stages to create faster switching outputs. This technique might be useful if higher frequencies are desired and the number of phases at the output is not critical. It is usually implemented by converting the output voltages of the delay cells to currents using transconductance stages. Two or more current signals of this type are combined to give a higher frequency current signal. Finally, this current signal is passed through a load, such as standard diode connected PMOS transistors, to convert the signal back to voltage domain. Figure 18 illustrates an implementation [28] in which two sets of

three outputs of a six-stage ring oscillator are combined to create two new outputs with an I/Q phase relationship oscillating at a higher frequency.

The main advantage of this architecture is an increase in the frequency without a need to modify the internal structure of the ring oscillator. This technique can potentially be applied to almost any ring oscillator structure to achieve maximum frequencies higher than that existing in the ring. The frequency increase depends on which phases are combined together. The output signal, however, has a reduced amplitude that may degrade the noise performance.

3.4.2 Phase Noise

Timing uncertainty of a periodic signal is either referred to as phase noise or jitter. Phase noise is the undesired and uncontrolled fluctuations of the phase of a signal. While phase-noise is used to define the uncertainty in the frequency domain, jitter is used to define the uncertainty in time domain. Thus they refer to the same phenomenon, and phase noise will be used to refer to both through this dissertation in qualitative discussions.

The factors that contribute to the phase noise of an oscillator can be classified into two categories. The first is the random factors that create random variations of the timing of the signal edges. Major part of this noise originates from thermal noise and flicker noise ($1/f$ noise) of active and passive devices that constitute the circuits. Note that at temperatures higher than absolute zero, every active and passive device in a circuit exhibit thermal and $1/f$ noise. It is possible to reduce this noise to some degree using different circuit design techniques but the effect of the device noise is fundamental and it is often the major contributor of the total phase noise [6]. The second is the systematic factors that can generally be avoided by a careful design of the system. Systematic variations are mostly because of interfering signals from other parts of the integrated system. The interaction usually occurs through the power

supply and ground lines although signal leak may even be through the substrate if circuits are placed close. Of course inputs of system components, such as the control input of an oscillator, are also susceptible to this kind of disturbance. The effect of mismatches between devices and the delays of different oscillator stages is also considered to be part of the systematic factors.

There are various methods available to reduce the output noise of a ring oscillator. Some of these methods are intended to lower the effect of a specific noise source while others improve the overall noise characteristics of the circuits. Utilization of a differential architecture, for example, provides the circuit a better immunity against common mode disturbances such as power supply and substrate bounces. If the power lines are the most significant noise sources in the system, additional techniques to decouple the circuit from the power lines might be useful when used along with the differential architecture. The ring oscillator stage shown in Figure 19, for example [29], employs the uppermost PMOS transistor M7 to isolate node-A from the power supply. This increases the power supply rejection ratio (PSRR) of the circuitry. The power supply sensitivity of a four-stage ring oscillator constructed with this stage is reported as 0.05 %/V [29], which is an order of magnitude better than that expected from a regular differential stage. The addition of M7, however, will induce noise up-conversion that tends to increase the overall noise-figure. A full differential architecture, including a differential control input, is usually desirable in a voltage controlled ring oscillator design to reduce the effect of common mode noise that may couple to the control lines. A lower VCO gain is also advantageous to reduce the control related noise since any disturbance on the control line will translate into smaller timing jitter at the output.

Utilization of gain stages having rail-to-rail signal levels with sharp transitions helps to reduce the overall noise of a ring oscillator. First, larger signal levels correspond to an increase in the signal-to-noise-ratio (SNR) of the system. This is

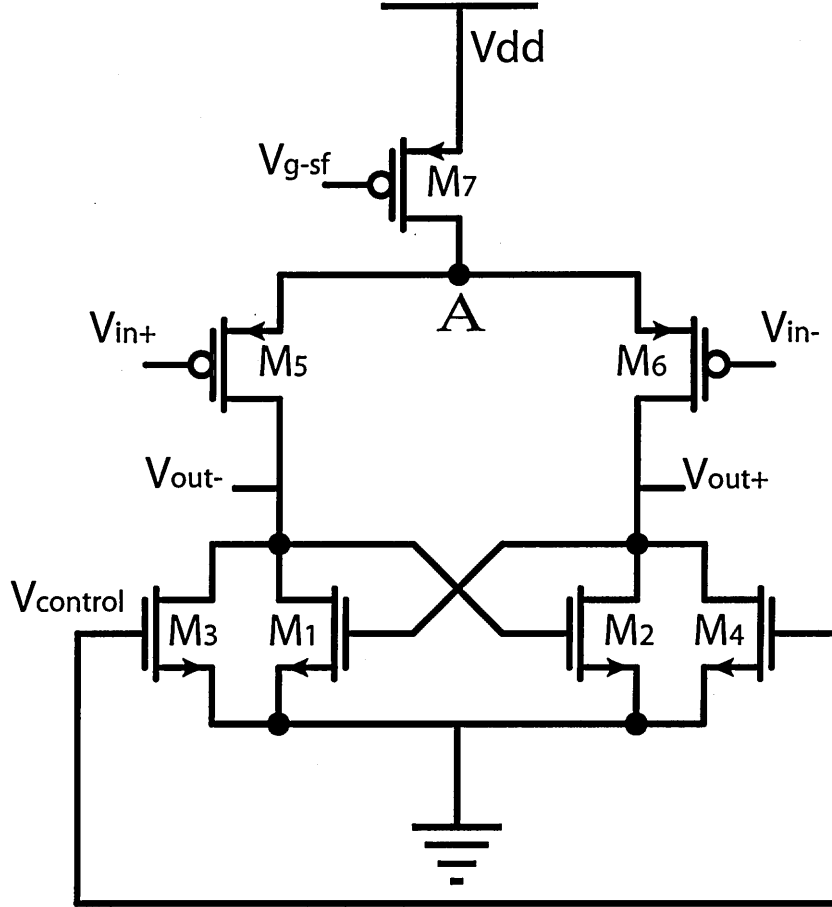


Figure 19: Isolation of delay stage from the power supply

important since the relative value of the noise to signal is crucial for most of the applications instead of the absolute noise. Rail-to-rail signal levels reduce the noise contribution of transistors by turning them on and off periodically [9]. Finally, sharp transition edges increase the quality Q factor of a ring oscillator [6]. These concepts will be explained in more detail in the following sections.

3.4.3 Stability

One of the most critical challenges in the design and implementation of an integrated VCO is meeting the design specifications across parameter variations. These parameters include the ambient temperature of the system, power supply voltage fluctuations, and possible variances of physical parameters such as the gate-oxide thickness

and dopant diffusion densities. Physical parameters might change significantly even on the same die. The joint effect of these variations might have a huge impact on the characteristics and the performance of circuits. Various advanced circuit design techniques, therefore, are required for more robust oscillators.

Physical parameter variations are highly random in nature; therefore, statistical analysis of multiple runs are used to define the characteristics of a specific process. Process corners such as slow, typical, or fast are defined and modelled this way. Designers are required to meet the design specifications at all corners to guarantee a reliable operation of the circuits and to increase the fabrication yield. Parameter gradients throughout a single die can be compensated for by using averaging layout design techniques such as a common-centroid topology.

Any variations in the main power supply voltage can change the circuit characteristics significantly because all other node voltages and currents depend on its value. For a ring oscillator, higher voltages may result in extremely high oscillation frequencies and vice-versa. Even more vital, the shift of DC levels may result in complete failure of the operation. Bandgap reference networks and voltage regulators are utilized widely to stabilize the voltage/current values in a circuit.

Ring oscillators that employ standard differential pair stages are not stable with respect to temperature variations because of large temperature dependencies of transconductances and threshold voltages of MOS transistors. The frequency drift can be as high as 1000-2000 ppm/C [30], and this may drive the oscillator out of the specified operating region. To overcome this drift problem, different temperature compensation techniques have been offered in the literature using either resistors or complicated operational amplifiers. Resistors, however, have large temperature coefficients, and the addition of operational amplifiers complicates the circuits. [30] proposes a new gain stage design with a load consisting of cascade connected PMOS and NMOS transistors to obtain temperature stability, as shown in Figure 20.

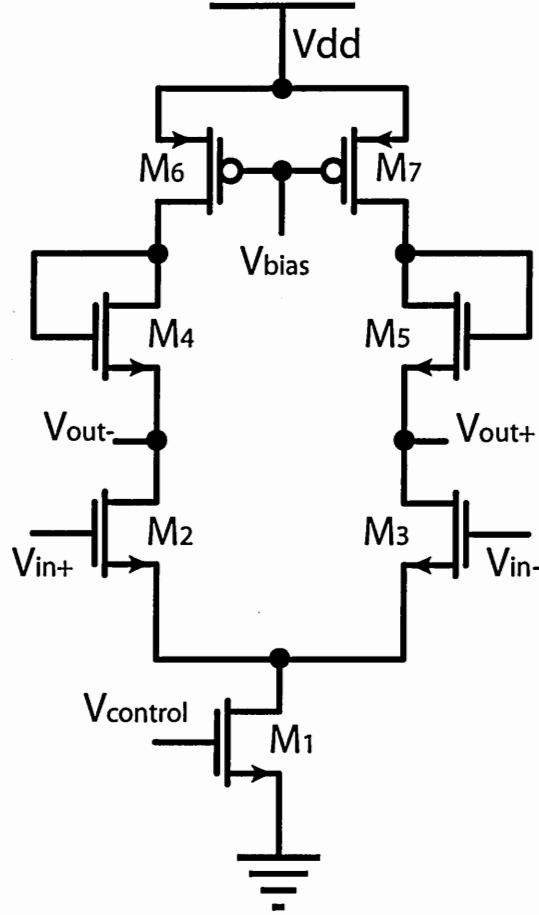


Figure 20: Temperature compensated delay stage

The main idea is the use of an NMOS/PMOS transistor stack. This attempts to nullify the temperature dependency by using the reverse signed temperature coefficients of the two types of transistors. Assuming that both the NMOS and the PMOS are biased in the saturation region, the temperature dependency of the output voltage at a single node can be written as [30]

$$\frac{\partial V_{out-}}{\partial T} = - \left(\sqrt{\frac{K_p (W/L)_p}{K_n (W/L)_n}} \frac{\partial V_{T_p}}{\partial T} + \frac{\partial V_{T_n}}{\partial T} \right) \quad (18)$$

The temperature dependencies of the transconductance parameters (K_p and K_n) are proportional to $T^{-3/2}$, which are cancelled out. The threshold voltages have reverse signed temperature dependencies. Hence, with the adjustment of the sizes of NMOS and PMOS transistors, the output voltage can be made independent of

the temperature, at least from the theoretical viewpoint. [30] claims a temperature sensitivity of $86.3 \text{ ppm}/^{\circ}\text{C}$ for temperatures between $15\text{-}125^{\circ}\text{C}$.

CHAPTER IV

VCO PHASE NOISE MODELS

The estimation of phase noise of a VCO has always been a challenging task because of the difficulties found in the comprehension of the VCO phase noise mechanics. A number of different approaches, fortunately, have been proposed in the literature. Earlier models, Leeson [31] and then Razavi [8], depend on simple linear time invariant (LTI) analysis and work well for some specific cases: LC oscillators and small-signal ring oscillators. Although these models were not sufficient to model the phase noise of ring oscillators exhibiting strong nonlinearity and time variance, they constructed a good foundation for better understanding of oscillator phase noise. Recent models, on the other hand, considers nonlinearity and cyclostationary effects for more accurate phase noise analysis of ring oscillators with full-switching and rail-to-rail signals [6, 32]. This chapter reviews some of these LTI and more complex models for better understanding of the next chapters.

4.1 Leeson's Phase Noise Model

In 1966, Leeson [31] proposed an oscillator phase noise model without any formal proof, which turned out to be the most widely known model. His model can be stated as

$$L(\Delta\omega) = S_{\Delta\theta}(\Delta\omega) \left[1 + \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right] \quad (19)$$

$$S_{\Delta\theta}(\Delta\omega) = \frac{\alpha}{\Delta\omega} + \frac{2FkT}{P_s}, \quad (20)$$

where $L(\Delta\omega)$ is the single-sideband phase noise, $S_{\Delta\theta}(\Delta\omega)$ is the spectrum of the input noise, and $[1 + (\frac{\omega_0}{2Q\Delta\omega})^2]$ is the noise shaping function. $S_{\Delta\theta}(\Delta\omega)$, which is given by

Equation (20), has an additive component ($2FkT/P_s$) due to white noise terms, and a low frequency component ($\alpha/\Delta\omega$) due to flicker noise terms. The other parameters of interest in these equations are the loaded quality factor Q , the angular frequency offset $\Delta\omega$ from the center frequency ω_0 , flicker noise constant α , an excess empirical noise factor F , the Boltzmann's constant k , and the absolute temperature T .

4.1.1 Oscillator Phase Noise Spectrum

Considering that flicker noise is bandwidth limited to a few hundreds of kHz in CMOS processes, Leeson's model predicts three different regions for the output noise spectrum. For small offset frequencies ($\frac{\omega_0}{2Q\Delta\omega}$)² $\gg 1$, and hence we can simplify Equation (19) as

$$L(\Delta\omega) = S_{\Delta\theta}(\Delta\omega) \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2. \quad (21)$$

In the first region, where the offset frequency is closest to the center frequency, phase noise is proportional to $1/\Delta\omega^3$, which corresponds to 30 dB/decade drop, because of the flicker and thermal noise sources. The first region starts from the center frequency and extends up to $\omega_0 + BW_{1/f}$, where $BW_{1/f}$ is the bandwidth of the flicker noise. In the second region, thermal noise dominates the overall phase noise and phase noise is proportional to $1/\Delta\omega^2$, which corresponds to 20 dB/decade drop. The second region is usually the most important one because the phase noise of most systems are specified in this region, which extends from a few hundreds of kHz to tens of MHz for modern communications systems. In this region, the single-sideband phase noise equation can be simplified as

$$L(\Delta\omega) = \frac{2FkT}{P_s} \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2. \quad (22)$$

At larger offset frequencies, for ($\frac{\omega_0}{2Q\Delta\omega}$)² $\ll 1$, the phase noise equation reduces to

$$L(\Delta\omega) = \frac{2FkT}{P_s}. \quad (23)$$

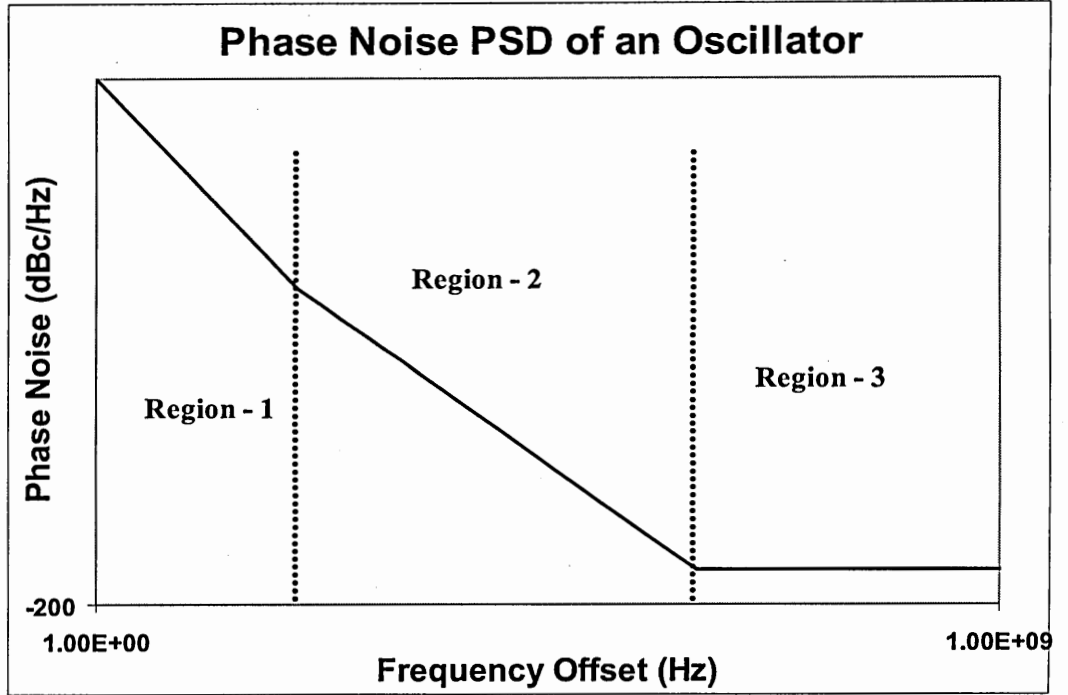


Figure 21: Phase noise PSD regions of an oscillator

Therefore, the input white noise is directly transferred to the output and causes a flat region in the output noise spectrum. These three regions are shown in Figure 21.

4.2 *Razavi's Phase Noise Model*

4.2.1 Classical Definitions of Q

The classic definitions of Q factor are only provided for, and thus make sense for, RLC circuits. For an RLC tank, some of these definitions can be given as [8]

- Q is the ratio of the center frequency of the tank to the two-sided -3dB bandwidth:

$$Q = \frac{\omega_0}{\Delta\omega} \quad (24)$$

- Q is 2π times the ratio of the stored energy to the dissipated energy in each cycle.

$$Q = 2\pi \frac{\text{Energy Stored}}{\text{Energy Dissipated per Cycle}} \quad (25)$$

- Q is a measure of how much the feedback oscillatory system opposes the variations in the frequency of oscillation, and given by

$$Q = \frac{\omega_0}{2} \frac{d\phi}{d\omega}, \quad (26)$$

where ϕ is the phase of the open-loop system transfer function.

Noting that an LC oscillator is basically an RLC circuit considering the parasitic resistances, one can conclude that quality Q factor of an LC oscillator is a well defined phenomena. Because of the high Q factors of varactors in CMOS process, Q factor is limited by the design of the inductor.

4.2.2 Q Factor of a Ring Oscillator

For a ring oscillator, on the other hand, Q factor is not well defined because the load capacitors are charged and discharged in every cycle and there is no energy storage, eliminating the first two definitions of the Q . Razavi [8] showed that the third definition is also not sufficient for ring oscillators by applying the equation to an ideal two-integrator oscillator, which turned a Q factor of zero! Using a linear time-invariant (LTI) analysis and some basic approximations, he derived the noise shaping function for ring oscillators as [8]

$$\left| \frac{Y}{X} [j(\omega_0 + \Delta\omega)] \right|^2 = \frac{1}{(\Delta\omega)^2 \left[\left(\frac{dA}{d\omega} \right)^2 + \left(\frac{d\phi}{d\omega} \right)^2 \right]}, \quad (27)$$

where A and ϕ are the magnitude and the phase of the open-loop transfer function respectively. Remembering that the noise shaping function of an LC oscillator is given by Leeson [31] as

$$\left(\frac{\omega_0}{2Q\Delta\omega} \right)^2$$

for small offset frequencies, the Q factor of a ring oscillator can be found as [8]

$$Q = \frac{\omega_0}{2} \sqrt{\left[\left(\frac{dA}{d\omega} \right)^2 + \left(\frac{d\phi}{d\omega} \right)^2 \right]}, \quad (28)$$

which reduces to the third definition of Q for LC oscillators.

Qualitatively, if there is any noise or disturbance in the system, the open-loop transfer function will deviate from its original value that satisfies the Barkhausen's criterion. In response, the positive feedback in the ring loop will try to correct this deviation. As told above, this definition of the Q factor can be understood as a measure of how much the feedback oscillatory system opposes the variations in the frequency of oscillation. A larger Q factor means more deviation from the stable state and, therefore, means stronger feedback to correct this variance. Using our previous linear analysis of ring oscillators given in Chapter III, the frequency derivatives of A and ϕ are found as

$$\frac{dA}{d\omega} = -NRC \tan\theta (g_m R)^N (\cos\theta)^{N+2} \quad (29)$$

$$\frac{d\phi}{d\omega} = NRC \cos^2(\theta). \quad (30)$$

After substituting these in Equation (28), the quality Q factor of an N stage ring oscillator can be found as

$$Q(N - \text{stage}) = \frac{N \tan\theta \cos^2\theta}{2} \sqrt{1 + (g_m R \cos\theta)^{2N} \tan^2\theta}. \quad (31)$$

By using simple trigonometric transformations, replacing $g_m R$ with $1/\cos\theta$ (gain requirement), and θ with π/N , Q of an N-stage ring oscillator can be finally written as

$$Q(N - \text{stage}) = \frac{N}{2} \sin\left(\frac{\pi}{N}\right). \quad (32)$$

Figure 22 gives the Q factor of ring oscillators for various number of stages. According to this analysis, ring oscillators' Q factor improves as the number of stages increase until it saturates at 1.56 predicting better noise performance for longer chains. For an N stage ring oscillator, however, there are N equivalent elements that add noise to the output. Therefore, for ring oscillators, Leeson's [31] phase noise model should

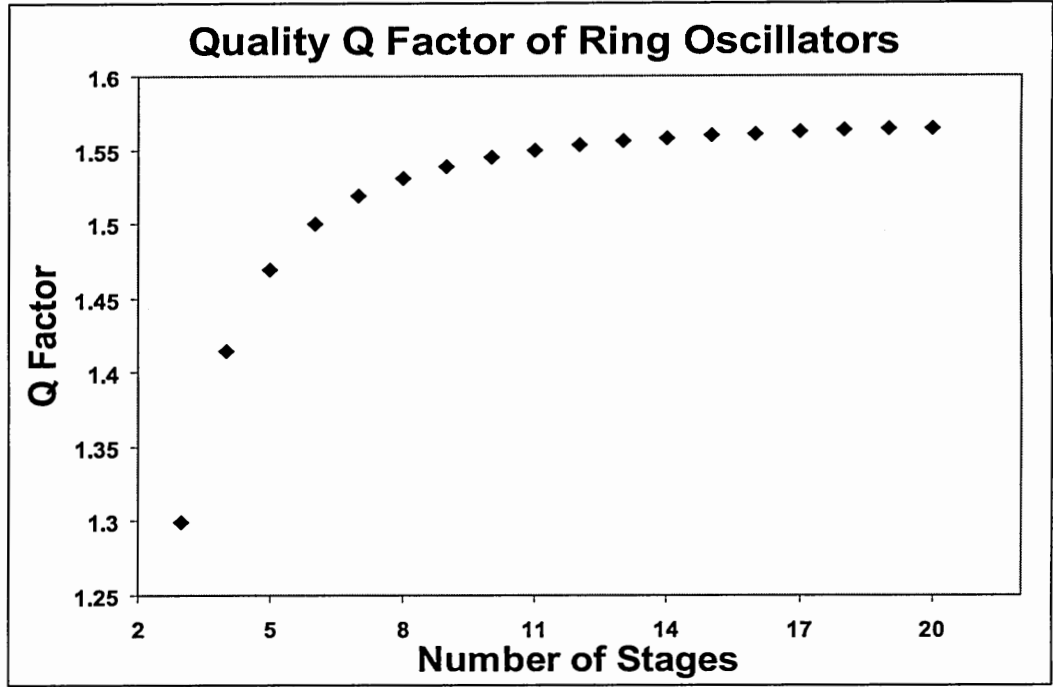


Figure 22: Quality factor of ring oscillators found using Razavi's model

be modified by adding the number of stages to the equation. This is shown in [8]

$$L(\Delta\omega) = \frac{2NFkT}{P_s} \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2. \quad (33)$$

for small offset frequencies. The most important conclusion derived from this equation is that increasing the number of stages does not help to reduce noise; in fact, the output noise increases if the power consumption is kept constant. By taking the three-stage ring as the reference, Figure 23 gives the relative change of the ring oscillator single-sideband phase noise assuming a constant power dissipation.

For typical LC oscillators, the loaded Q factors of up to 8-14 [13,33] are reported in standard CMOS technologies, whereas Q factors of up to 85 [7] are possible in modified processes. Considering that the given equations predict the best phase noise performance from a three-stage design having an effective Q factor of ~ 1.3 , the superior noise performance of LC oscillators can be understood.

The major weakness of the Leeson's and Razavi's phase noise models is that they do not consider nonlinearity because they depend on LTI system assumptions. As the

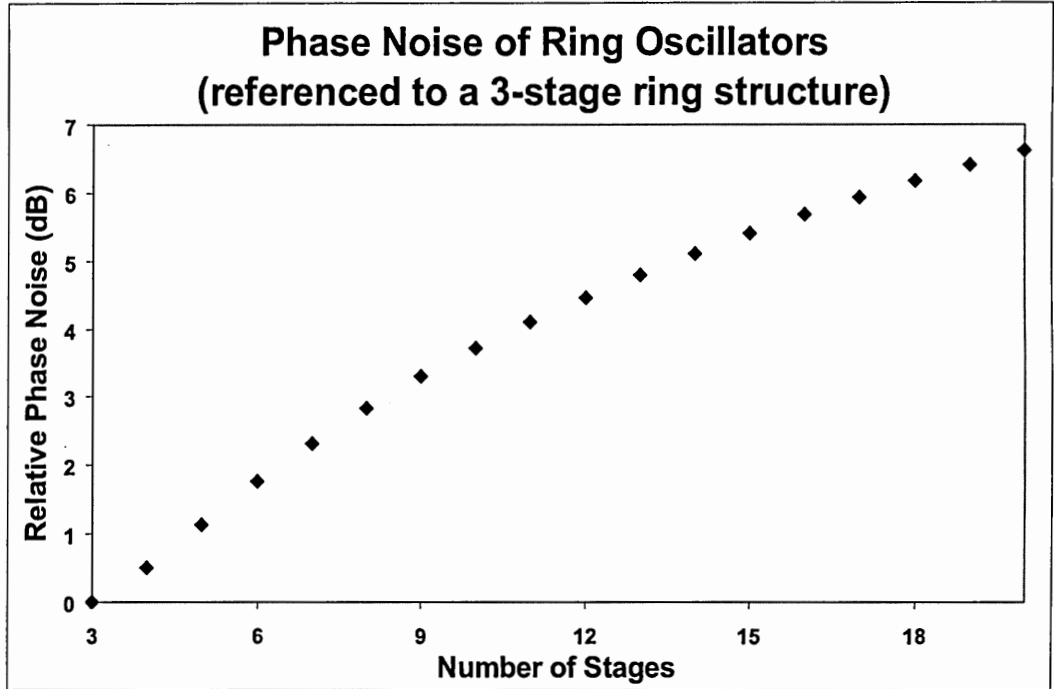


Figure 23: Phase noise of different rings relative to a three-stage ring oscillator

circuits deviate from the linear operation, the error given by these models increase. This corresponds to more square shaped output waveforms instead of ideal sinusoidals. Therefore, nonlinearity is more pronounced for rings with more number of stages. Assuming that the rise/fall times stay constant, this is because signal transitions appear sharper for a longer chain having a lower oscillation frequency. Razavi [8], for example, implies that his model fails by 1 dB for a four-stage ring, whereas the error increase with the number of stages reaching 6 dB for an 8-stage oscillator. It is interesting to note that these models overestimates the noise of nonlinear ring oscillators.

4.3 *Hajimiri's Phase Noise Model*

For ring oscillators exhibiting full-switching of the FETs in the stage and rail-to-rail signal swings, LTI models lack accuracy. Fortunately, there are other phase noise calculation techniques proposed in the literature modelling nonlinearity and time

variance. Among these, Hajimiri's analysis [32] is the most general one that includes nonlinearity, time variance, and cyclostationary effects leading to an accurate phase noise analysis. His analysis is derived as discussed in the following section.

4.3.1 Impulse Sensitivity Function

If a current impulse is injected into one of the nodes of an oscillator, the amplitude and the phase of the output waveform will experience an instantaneous change. Most practical oscillators employ a strong automatic level control (ALC) mechanism to stop the growth of the oscillations. The amplitude fluctuations, therefore, will diminish after a certain time depending on the time-constant of the ALC mechanism. The phase of the oscillator, on the other hand, will permanently shift because of the lack of the original phase information. The permanent excess phase is proportional to the ratio of the injected charge to the maximum charge swing on that node, i.e. $\phi(t) \sim \Delta q/q_{max}$. Note that, while the excess phase changes linearly with $\Delta q/q_{max}$, the absolute value of the phase shift is time-dependent. That is, the injection of an impulse at the peak of the output waveform will generate a small phase shift because of the ALC; whereas a charge injection at the transition edges will result in a larger phase shift [32]. This is illustrated in Figure 24. Because of the periodical behavior of the system, the time dependence of the excess phase is also periodical with the same period as the system.

Therefore, impulse response of the output phase is a step function whose amplitude depends periodically on the time τ when the charge impulse is injected into the node of interest. This leads to the Equation (34) [32] defining the phase response of the oscillator.

$$h_\phi(t, \tau) = \frac{\Gamma(\omega_0 \tau)}{q_{max}} u(t - \tau) \quad (34)$$

In this function, $u(t)$ is the unit step function and Γ is the so called impulse sensitivity

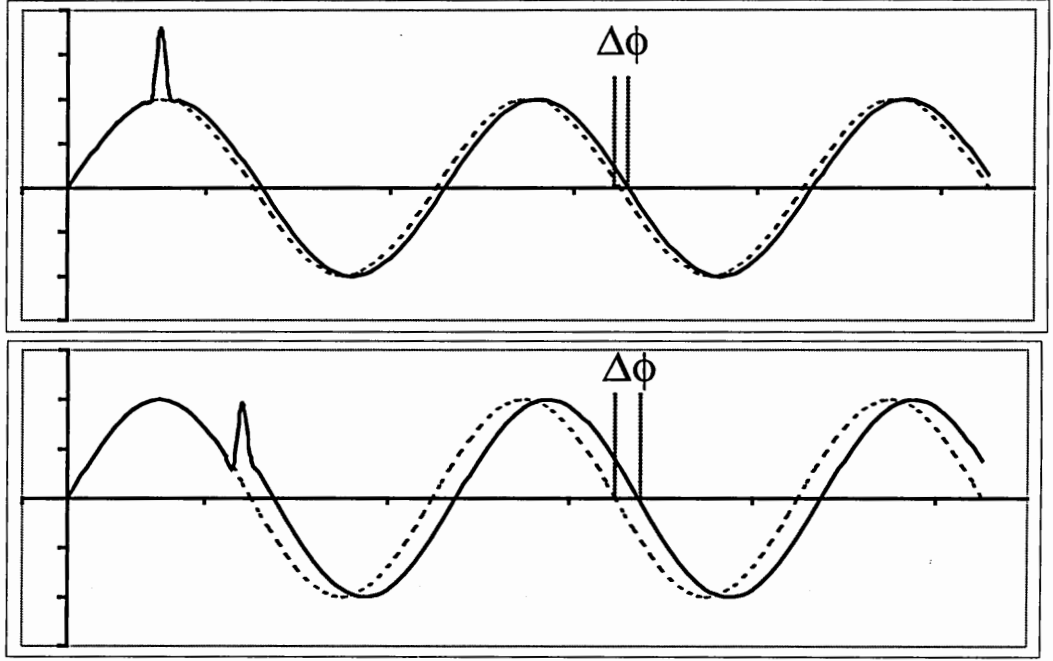


Figure 24: Phase shift resulting from impulses injected at different instants

function (ISF). Hajimiri [32] defines ISF as a dimensionless, frequency- and amplitude-independent periodic function with a period 2π that describes the amount of phase shift resulting from an injection of charge impulse at time $t = \tau$. ISF strongly depends on the output waveform or, equivalently, on the oscillator architecture.

With the knowledge of the ISF for a specific oscillator, the excess phase $\phi(t)$ can be found using the superposition integral as

$$\phi(t) = \frac{1}{q_{max}} \int_{-\infty}^t \Gamma(\omega_0 \tau) i(\tau) d\tau \quad (35)$$

where $i(t)$ is the input noise current injected into the circuit. Since ISF is a periodic function at frequency ω_0 , it can be expanded in a Fourier series

$$\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \theta_n) \quad (36)$$

where c_n are the real valued Fourier coefficients and θ_n is the phase of the n^{th} harmonic. For random noise, θ_n will be neglected [32]. With the knowledge of ISF, and thus the Fourier coefficients c_n , excess phase can be calculated by substituting

Equation (36) into Equation (35) [32]

$$\phi(t) = \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^t i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0\tau) d\tau \right]. \quad (37)$$

Since $i(t)$ can also be decomposed into its Fourier coefficients, Equation (37) tells that only noise close to the harmonics of ω_0 and DC will result in non-zero excess phase. This is because of the averaging nature of the integral, i.e. $\int_{-\infty}^t \cos(\omega_1 t) \sin(\omega_2 t) dt = 0$ for $\omega_1 \neq \omega_2$.

Note that, noise performance of an oscillator is usually characterized using the single-sideband phase noise values instead of the absolute excess phase. This information can be obtained from the output power spectral density (PSD) of the oscillator; which, in turn, requires the conversion of the resulting phase shift to the voltage domain.

4.3.2 VCO Phase Noise from ISF

For a VCO, the relationship between the output voltage and the excess phase can be written as

$$V_{out}(t) = A(t) \cdot f[\omega_0 t + \phi(t)]. \quad (38)$$

Using this, the single-sideband phase noise of a VCO is found as [32]

$$L(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\bar{i}_n^2 / \Delta f}{2\Delta\omega^2} \quad (39)$$

in the $1/f^2$ region of the phase noise spectrum, and as [32]

$$L(\Delta\omega) = \frac{c_0^2}{q_{max}^2} \cdot \frac{\bar{i}_n^2 / \Delta f}{8\Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \quad (40)$$

in the $1/f^3$ region of the phase noise spectrum. In these equations $\bar{i}_n^2 / \Delta f$ is the white power spectral density of the input device noise, $\omega_{1/f}$ is the device $1/f$ corner frequency, and Γ_{rms} is the root-mean-square (rms) value of the ISF, i.e.

$$\Gamma_{rms} = \frac{1}{2} \sum_{n=0}^{\infty} c_n^2. \quad (41)$$

By equating equations (39) and (40), $1/f^3$ corner frequency of the phase noise spectrum can be found as

$$\omega_{1/f^3} = \omega_{1/f} \left(\frac{c_0}{2\Gamma_{rms}} \right)^2 \approx \omega_{1/f} \frac{1}{2} \left(\frac{c_0}{c_1} \right)^2, \quad (42)$$

indicating that $1/f^3$ phase noise corner is smaller than device $1/f$ noise corner by a factor of $c_0^2/(2\Gamma_{rms}^2)$, unlike the common thought that these two corner frequencies are equal. The DC Fourier coefficient of the ISF c_0 , which governs the close-in phase noise performance in Hajimiri's [32] model, can be reduced by making output signals more symmetric, i.e. equal rise/fall times and 50% duty cycle. Differential architectures, however, does not help to reduce the effect of $1/f$ noise since it is the signal symmetry in each half-circuit that is important for the reduction of c_0 . Henceforth, Hajimiri's model demonstrated that, for the first time, poor $1/f$ device noise does not necessarily mean poor oscillator close-in phase noise performance [32].

4.3.3 Modelling of Cyclostationary Noise Sources

For ring oscillators employing full-switching, transistors periodically turn ON and OFF, alternating between the triode, saturation and cutoff regions. Therefore, statistical properties of transistor noise sources vary periodically with time, referred as cyclostationary noise sources. Hajimiri [32] models the cyclostationary noise by introducing an effective ISF, which is given by

$$\Gamma_{eff}(x) = \Gamma(x) \cdot \alpha(x), \quad (43)$$

where $\alpha(x)$ is a periodic function with a maximum value of 1 representing the noise amplitude modulation because of the cyclostationary behavior. $\alpha(x)$ can be calculated using the device noise models and the circuit quiescent point. For LC oscillators, the peak values of the ISF and $\alpha(x)$ are usually off by a certain phase, predicting that $\Gamma_{eff}(x) < \Gamma(x)$. For ring oscillators, on the other hand, the peak values of ISF and $\alpha(x)$ tend to have the same phase [32] explaining why the LC networks have superior phase noise performance.

4.3.4 Calculation/Simulation of ISF for Multiple Noise Sources/Nodes

The most accurate way of computing the ISF of an oscillator is by using simulations. For a single noise-source and a single output node, a current impulse is injected into the current node from the current noise-source and the output excess phase is measured after a few cycles. In each simulation, the moment of injection is varied relative to the output signal phase such that the simulations will track one whole period of the waveform. With the knowledge of q_{max} , ISF can be calculated using Equation (34).

Alternatively, ISF can be calculated using the closed-form formula given for an n^{th} order system [32]

$$\Gamma_i(x) = \frac{f'_i}{|\vec{f}'|^2} = \frac{f'_i}{\sum_{j=1}^n f_j'^2}, \quad (44)$$

where f_i is the normalized waveform at node i , and f' is the derivative of this waveform. For ring oscillators, the denominator of (44), i.e. $\sum_{j=1}^n f_j'^2$, shows little variation, resulting in the following simplification of the closed-form ISF

$$\Gamma(x) = \frac{f'_i(x)}{f_{max}'^2}. \quad (45)$$

Equations (44) and (45) indicate that the maximum value of the ISF is observed during the transitions where the derivative of the output waveforms are maximum, which is consistent with previous discussions. Furthermore, the peak value of the ISF can be minimized by increasing the maximum of f' , which is equivalent to sharper/faster transitions. Therefore, the importance of the rail-to-rail signal levels and full-switching in the reduction of the phase noise of voltage controlled ring oscillators becomes apparent.

In the case of multiple noise sources and multiple oscillation nodes, such as for an N -stage ring oscillator, superposition can be used to compute the total contribution of the individual noise sources on the noise of a single node, and this can be applied to the other nodes to complete the analysis. Although the whole model is nonlinear

because of the excess-phase $\phi(t)$ to voltage transformation defined in Equation (38), superposition still holds because input disturbance $i(t)$ to excess-phase $\phi(t)$ transformation process, i.e. Equation (35), is linear. During the application of this method, correlation between different noise sources need to be considered and the power sum of the individual contributions should be computed to find the total noise.

4.3.5 Using Hajimiri's Model

Unlike the other phase noise models published in the literature, Hajimiri's model [32] is constructed without making any assumptions about the architecture of the VCO. This model, therefore, is the most comprehensive one among the available models and can be used for any type of oscillator employing positive feedback. These include LC networks as well as ring oscillators. In addition to the nonlinearity and time variance, which are automatically considered in the model, cyclostationary noise sources are modelled by introducing an effective ISF.

Important implications of this model can be summarized as:

- There are no empirical factors in the equations resulting in more accurate results for the estimation of phase noise. The excess noise factor F that depends on the oscillator architecture is hidden in the ISF.
- Increasing the maximum charge displacement q_{max} across the node capacitances reduces the phase noise. This corresponds to an increase of the dissipated power and was predicted by previous models [8, 31].
- Noise power around the harmonics of the oscillation frequency is converted to the vicinity of the oscillation frequency corrupting the output signal; whereas noise power at other frequencies is mostly diminished in the system because of the averaging. The converted noise power is scaled by the Fourier coefficients c_n of the ISF depending on the harmonic number. This is explained as high-frequency multiplicative noise components in Razavi's model [8].

- The close-in phase noise performance of a VCO is governed by the ISF Fourier coefficient c_0 . Smaller c_0 values resulting in an improvement of the phase noise in the $1/f^3$ region of the spectrum. Note that, c_0 can be reduced by making output signals more symmetric, i.e. equal rise/fall times and %50 duty cycle.
- Maximum value of the ISF is observed during the signal transitions indicating that the oscillator is more susceptible to noise injected in these intervals, which was intuitively discussed before. The peak value of the ISF can be minimized by having sharper transitions, which is equivalent to faster switching. This is especially important for the reduction of the phase noise of ring oscillators.

Although this model is the most accurate approach to the phase noise analysis of VCOs, it has some practical difficulties restricting its usage. These are

- For the calculation of the ISF, current impulses need to be injected into the circuit. An ideal impulse, however, has an infinite amplitude and zero width and thus can not be simulated. Injected current impulses, therefore, need to have a finite amplitude and a duration. Narrow pulses better approximate an impulse, and small amplitudes are preferred to keep the oscillator at its stable operating point. This, however, reduces the amount of charge injected resulting in smaller phase shifts increasing the importance of simulation numerical errors [6].
- Even for a single noise-source and a single node of interest, computation of the ISF requires multiple simulations with very small time-steps to accurately track the whole oscillation period. For a network having multiple noise sources and multiple nodes this process easily gets cumbersome, if not impossible.
- Using the ISF, phase noise calculation still requires the knowledge of the device noise of the individual transistors. In the case of cyclostationary noise sources, the application of this method gets more complex.

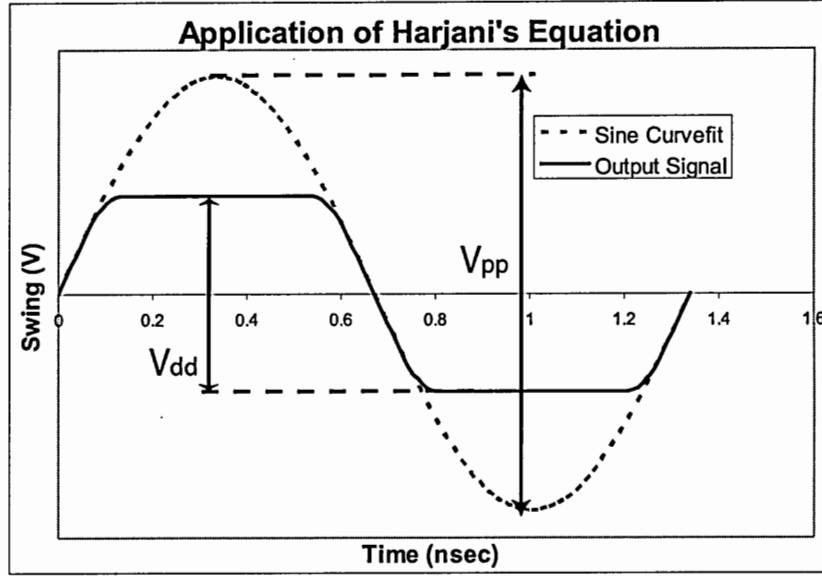


Figure 25: Representation of waveforms with sharp transitions using a clipped sinusoidal

In the next section, we will discuss how a simplified extension of Hajimiri's phase noise model [32], given by Harjani [6], can be used to accurately calculate the phase noise of different ring oscillators.

4.4 *Harjani's Phase Noise Model*

Harjani, in his work [6], discusses a special case of the Hajimiri's conclusions in more detail: ring oscillators exhibiting sharp transitions and rail-to-rail output swings. His analysis uses the ISF concept along with the derivations of Leeson [31] and Razavi [8] to come up with a simplified model for the computation of phase noise of nonlinear ring oscillators.

When the transistors in a ring oscillator stage experience full-switching and rail-to-rail signal levels, signal transition speeds improve and output signals no longer look like perfect sinusoids. Harjani models these kind of signals with sinusoids having larger amplitudes clipped at the power supply and ground levels as illustrated in Figure 25. This clipping is equivalent to addition of limiters into the ring oscillator linear model. The modified model is given for a three-stage ring in Figure 26 [10].

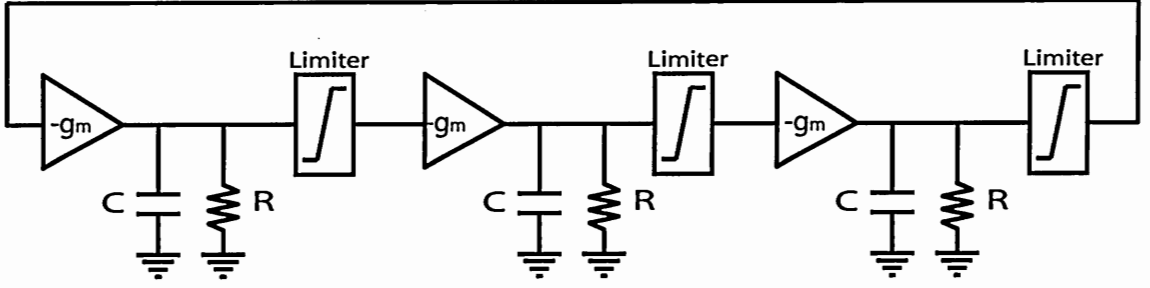


Figure 26: Modified linear model of a three-stage ring oscillator

4.4.1 Phase Noise of a Three-Stage Ring VCO

Initially, assuming the linear operation such that the node voltages are sinusoidals and there is no voltage clipping, output voltage is given as $v(\omega_0 t) = \frac{V_{pp}}{2} \sin(\omega_0 t)$ centered around the mid-voltage $V_{dd}/2$. For this waveform, Razavi's single-sideband phase noise equation, Equation (33), can be alternatively written as

$$L(\Delta\omega) = \frac{64FkTR}{9V_{pp}^2} \left(\frac{\omega_0}{\Delta\omega} \right)^2, \quad (46)$$

where $L(\Delta\omega)$ is the single-sideband phase noise, F is the excess noise factor, V_{pp} is the peak-to-peak signal amplitude, $\Delta\omega$ is the angular frequency offset from the center frequency ω_0 , kT is the thermal energy, and R is the equivalent output resistance of a delay cell. Here, the Q factor of the three stage linear ring oscillator was replaced by its calculated value of $3\sqrt{3}/4$.

Hajimiri gives the approximate closed-form ISF of an N-stage ring oscillator in Equation (45). For the linear case, this can be simplified as given in Equation (47), and its RMS value can be found as demonstrated in Equation (48) [10].

$$\Gamma(\omega_0 t) \approx \frac{\frac{dv(\omega_0 t)}{d(\omega_0 t)}}{\left| \frac{dv(\omega_0 t)}{d(\omega_0 t)} \right|_{max}} = \frac{2\cos(\omega_0 t)}{V_{pp}} \quad (47)$$

$$\Gamma_{rms}^2 = \frac{\omega_0}{2} \int_0^{2\pi/\omega_0} |\Gamma(\omega_0 t)|^2 dt = \frac{2}{V_{pp}^2} \quad (48)$$

Using this result, Equation (46) can be rewritten in terms of Γ_{rms} as in

$$L(\Delta\omega) = \frac{32FkTR\Gamma_{rms}^2}{9} \left(\frac{\omega_0}{\Delta\omega} \right)^2. \quad (49)$$

Harjani [10] claims that although this expression is derived for a ring oscillator under linear operation; because ISF considers nonlinearity, time-variance, and cyclostationary effects; Equation (49) can also be applied to nonlinear cases. Note that, this model only considers the thermal noise. Remembering the Hajimiri's explanation on the upconversion of the flicker noise, one can conclude that the current model is only valid for offset frequencies that are much larger than the $1/f^3$ noise corner given by Hajimiri [32] in Equation (42).

For ring designs that operate outside the linear regime, such that $V_{pp} \gg V_{dd}$ referencing Figure 25, the node voltages have faster rise-fall rates and can be assumed as clipped. Since the clipping is rarely hard in an actual oscillator, soft clipping is modelled as [10]

$$v(\omega_0 t) = \frac{V_{dd}}{2} \tanh\left[\frac{V_{pp}}{V_{dd}} \sin(\omega_0 t)\right]. \quad (50)$$

The approximate root-mean-square value of the ISF of this signal is given in

$$\Gamma_{rms}^2 = \frac{16V_{dd}}{3\pi V_{pp}^3}. \quad (51)$$

Finally, by substituting this into Equation (49), the single-sideband phase noise of a ring oscillator can be found as

$$L(\Delta\omega) = \frac{512FkTRV_{dd}}{27\pi V_{pp}^3} \frac{\omega_0}{\Delta\omega}, \quad (52)$$

for $V_{pp} \gg V_{dd}$. By combining equations (46) and (52), the full model is written in Equation (53) [10].

$$L(\Delta\omega) = \begin{cases} \frac{64FkTR}{9V_{pp}^2} \left(\frac{\omega_0}{\Delta\omega}\right)^2 & (for V_{pp} \ll V_{dd}) \\ \frac{512FkTRV_{dd}}{27\pi V_{pp}^3} \left(\frac{\omega_0}{\Delta\omega}\right) & (for V_{pp} \gg V_{dd}) \end{cases} \quad (53)$$

It is crucial to repeat that, in this equation, V_{pp} does not represent the actual clipped output swing of the oscillator. It represents the peak-to-peak swing of an ideal sinusoidal wave that has the same maximum slew-rate as the actual output signal.

Table 1: Maximum effective Q factor of ring oscillators in various technologies

Process	f_T (GHz)	Q_{eff}
TSMC 0.35 μm	22.99	2.51
TSMC 0.25 μm	27.65	3.02
TSMC 0.18 μm	42.51	3.63

Figure 25 shows how the amplitude of this sinusoidal signal can be calculated using the clipped output signal of the ring oscillator. Alternatively, V_{pp} can simply be calculated by using the maximum slew rate of the output signal with the following equation [10]

$$V_{pp} = \frac{2|dv/dt|_{max}}{\omega_0}. \quad (54)$$

Both Hajimiri's and Harjani's, naturally since it was derived from Hajimiri's model, models predict an improvement in the phase noise performance of ring oscillators exhibiting clipped signals with sharp transitions and rail-to-rail output swings. Referring to the previous models given by Leeson [31] and Razavi [8], this improvement can be alternatively expressed as an increase of the effective Q factor in Equation (33). By comparing equations (52) and (33), the modified effective Q factor can be found as [10]

$$\begin{aligned} Q_{eff} &= \frac{9}{8} \sqrt{\frac{\pi V_{pp}}{2V_{dd}}} \\ &= \frac{9}{8} \sqrt{\frac{\pi SR_{max}}{\omega_0 V_{dd}}}. \end{aligned} \quad (55)$$

Using this result, Harjani computes the maximum effective Q factor of three-stage ring oscillators implemented in various technologies. The designs are assumed to operate at 900 MHz for a fair comparison. Table 1 [10] summarizes this comparison for TSMC processes.

4.4.2 Phase Noise of an N-Stage Ring VCO

It is important to note that Harjani's analysis is performed only for a three-stage ring oscillator and, therefore, the model needs to be modified for different rings. This

modification is performed as follows.

First, Razavi's single-sideband phase noise equation, Equation (33), can be rewritten as

$$L(\Delta\omega) = \frac{16FkTR}{NV_{pp}^2 \sin^2(\frac{\pi}{N})} \left(\frac{\omega_0}{\Delta\omega}\right)^2, \quad (56)$$

by using closed-form definition of Q factor for an N stage ring oscillator, i.e. $Q(N - \text{stage}) = \frac{N}{2} \sin(\frac{\pi}{N})$. This definition of the single-sideband phase noise in the linear regime replaces the one given by 46 for an N-stage ring. Following the previous derivation for the three-stage ring, this equation is modified by replacing $2/V_{pp}^2$ with Γ_{rms}^2

$$L(\Delta\omega) = \frac{8FkTR\Gamma_{rms}^2}{N \sin^2(\frac{\pi}{N})} \left(\frac{\omega_0}{\Delta\omega}\right)^2. \quad (57)$$

Using Equation (51), the single-sideband phase noise of an N-stage ring oscillator with clipped signals is found as

$$L(\Delta\omega) = \frac{128FkTRV_{dd}}{3\pi N \sin^2(\frac{\pi}{N}) V_{pp}^3} \left(\frac{\omega_0}{\Delta\omega}\right)^2, \quad (58)$$

for $V_{pp} \gg V_{dd}$. By combining equations (56) and (58), the full model is given in Equation (59) for an N-stage ring oscillator.

$$L(\Delta\omega) = \begin{cases} \frac{16FkTR}{NV_{pp}^2 \sin^2(\frac{\pi}{N})} \left(\frac{\omega_0}{\Delta\omega}\right)^2 & (\text{for } V_{pp} \ll V_{dd}) \\ \frac{128FkTRV_{dd}}{3\pi N \sin^2(\frac{\pi}{N}) V_{pp}^3} \left(\frac{\omega_0}{\Delta\omega}\right)^2 & (\text{for } V_{pp} \gg V_{dd}) \end{cases} \quad (59)$$

Similar to the previous derivation, the modified effective Q factor of an N-stage ring oscillator can be found as

$$\begin{aligned} Q_{eff} &= \frac{N}{2} \sin(\frac{\pi}{N}) \sqrt{\frac{3\pi V_{pp}}{8V_{dd}}} \\ &= \frac{N}{2} \sin(\frac{\pi}{N}) \sqrt{\frac{3\pi SR_{max}}{4\omega_0 V_{dd}}} \end{aligned} \quad (60)$$

by comparing equations (58) and (33). This finalizes Harjani's analysis and completes Chapter IV.

CHAPTER V

PROPOSED RING OSCILLATOR DESIGNS

5.1 *Architecture*

The simplest ring oscillators have a single-loop architecture. While straightforward to design, the basic ring is limited to lower frequencies. The maximum oscillation frequency of a ring oscillator is determined by the minimum delay time through the feedback path, which is the product of the number of stages and the delay of a stage. For a fixed number of stages, the maximum frequency depends on the minimum delay of a single stage, which is strictly determined by the characteristics of the specific fabrication process. Most practical ring-oscillators need at least three stages to sustain stable oscillations. While it is possible to construct a ring oscillator using only two stages [15–17], only two output phases can be extracted which restricts its usage in some systems; in addition, the two-stage network can be difficult to stabilize. These show the necessity to apply other architectural techniques to increase the maximum frequency of ring oscillators. Some of these include the use of subfeedback loops [23], multi-feedback loops [24], dual-delay paths [9,25], output interpolation methods [28], and oscillator coupling [15].

The multiple-pass loop architecture, which is shown in Figure 27 for a three-stage ring oscillator, is one of the promising techniques and is the basic architecture chosen in this work. P- and P+ are the primary inputs of a gain stage and S- and S+ are the secondary inputs. This technique adds auxiliary feedforward loops that work in conjunction with the main loop. The main idea is to reduce the delay of the stages below the smallest delay that is possible inside a simple ring oscillator loop. This is accomplished by adding a set of secondary inputs to every stage and

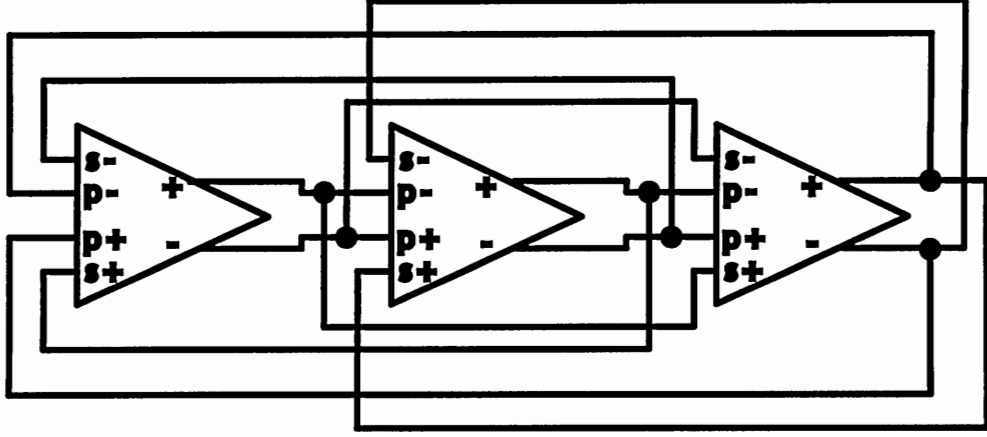


Figure 27: 3-stage ring oscillator with multiple-pass loop architecture

switching these secondary inputs earlier than the primary inputs during the operation. Note that the auxiliary loops should not be stronger than the main loop to avoid undesired oscillation modes. Preliminary observations on this architecture shows that the auxiliary loops are nested within the main loop, in contrast to a subfeedback loop architecture which employs additional stages outside the main loop. The frequency of the oscillation depends on the number of stages in both the main and the auxiliary loops, such that the maximum frequency is determined by the fastest signal path.

It is important to note that the majority of the frequency-increase techniques discussed above [9, 23–25] depends on the use of intercoupled feedback loops to increase the maximum frequency, similar to the multiple-pass loop architecture used in this work. Basically, all of these methods are fundamentally same and they are based on a one-dimensional variation of the coupled-oscillator structure introduced by Maneatis in [21] and discussed as the look-ahead ring oscillator in [26] again by Maneatis.

5.1.1 Quantitative Analysis

5.1.1.1 Time-Domain Analysis

For a first pass analysis of the multiple-pass loop architecture, consider the three stage single-ended ring oscillator given in Figure 28. If the propagation delay of a single inverter is t_d , the oscillation frequency can be written as $f_{osc} = 1/(6t_d)$.

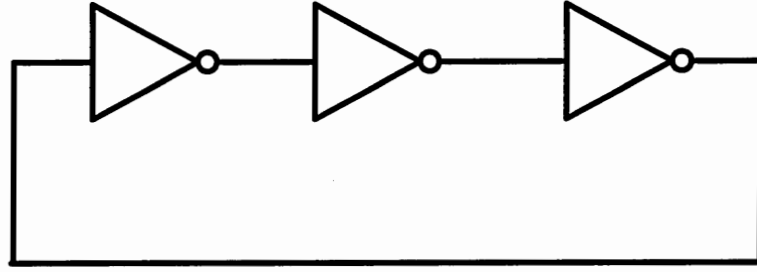


Figure 28: 3-stage single-ended ring oscillator

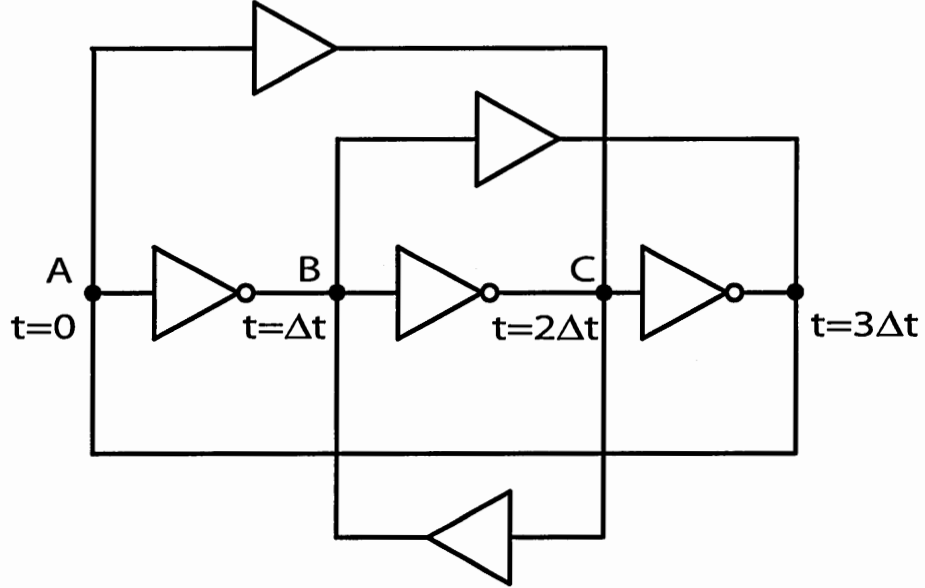


Figure 29: 3-stage single-ended ring oscillator with multiple-pass loop architecture

Next, this structure is modified in Figure 29 by adding auxiliary stages to convert it to a multiple-pass architecture. As will be discussed later, this connection scheme is equivalent to the one given in Figure 27 with the auxiliary non-inverting buffers representing the secondary input-to-output connections of the main-loop inverters. Because of the additional loops, the propagation delay in the main-loop will change from t_d to a Δt . Therefore, if one of the nodes experience switching at $t = 0$, the following node will switch at $t = \Delta t$, and the next one at $t = 2\Delta t$, inverting the initial node at $t = 3\Delta t$ creating an oscillation with frequency $f_{osc} = 1/(6\Delta t)$. This time/phase relationship among the stages is shown on the Figure 29. Now, to find the new oscillation frequency, one needs to find the relationship between t_d and Δt .

Assuming that the non-inverting buffers have the same load/driving characteristics as the inverters, there will be even delay interpolation at the output nodes. That is, the output transition will be at the time midpoint of the transitions created by the main-loop stages and the feedforward loop stages. Consider the two buffers connected to node C on Figure 29. The inverting buffer is driven by a signal at phase $t = \Delta t$, whereas the non-inverting buffer is driven by a signal at phase $t = 0$. The transition due to the inverter, therefore, starts at time $t = \Delta t + t_d$ and that due to the non-inverting buffer starts at $t = t_d$. Because of the even delay interpolation, taking the arithmetic average of these two time points should give the actual transition time as

$$t_{node-C} = \frac{t_d + (\Delta t + t_d)}{2} = t_d + \frac{\Delta t}{2}. \quad (61)$$

This switching time is also equal to $2\Delta t$ because of the phase relationship among the stage imposed by the main-loop. Therefore, we can write

$$\begin{aligned} 2\Delta t &= t_d + \frac{\Delta t}{2} \\ \Delta t &= \frac{2}{3}t_d. \end{aligned} \quad (62)$$

And, finally, the oscillation frequency of the three-stage multiple-pass ring oscillator is found as

$$f_{3-stage\ multiple-pass} = \frac{1}{2N\Delta t} = \frac{1}{4t_d}. \quad (63)$$

Thus a 50% improvement over the single-pass architecture.

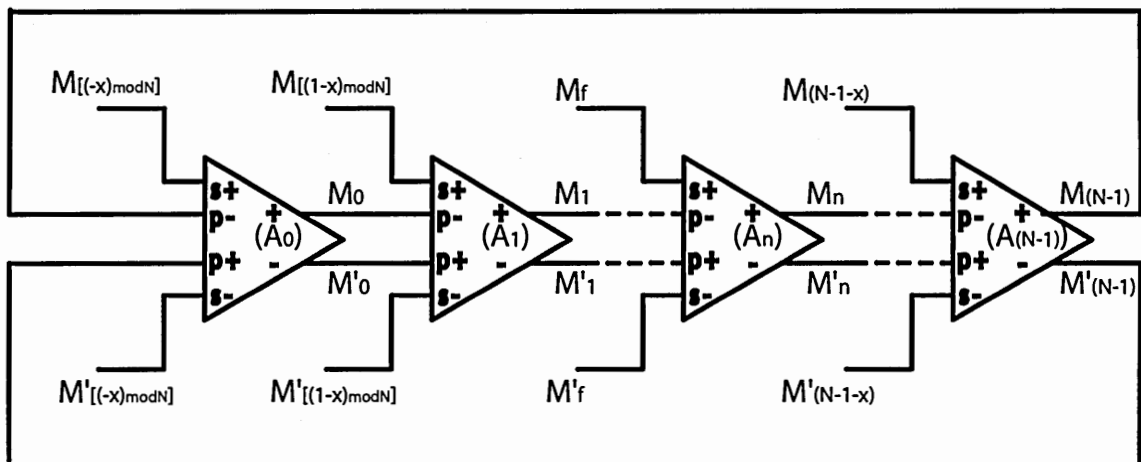
Although the above discussion explains the operation of multiple-pass loops in an intuitive way, it lacks generality. To understand the operation for different number of stages with different feedforward configurations, a frequency-domain approach is more desirable. The mathematical analysis will be performed for a full differential architecture without losing the generality for the single-ended case. Differential architecture allows the utilization of an even number of stages in the main loop unlike the single-ended architecture. While half of the required phase shift, which is π , is

obtained by an odd number of phase inversions in the loop for an odd number of stages, even number of stages require the reversing of one of the connections in the loop. Therefore, we have slightly different cases for loops with odd number of stages and even number of stages. Analysis will be carried out for a symmetrical loop having odd number of stages, and then it will be shown how to extend the analysis to loops with even number of stages.

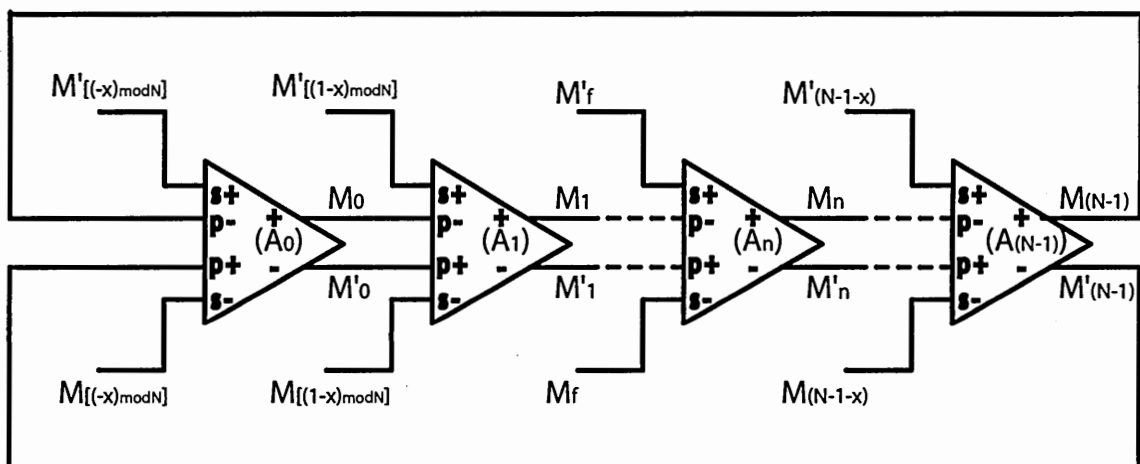
5.1.1.2 Odd Number of Stages

Figure 30(a) shows a general multiple-pass differential ring oscillator topology with N stages where N is an odd integer. Auxiliary feedforward loops are formed by connecting the outputs of the f^{th} stage to the secondary inputs of the n^{th} stage, where n is equal to $[(f + x) \bmod N]$, and $(x - 1)$ is the number of stages that feedforward loops pass over. The general case should include both the direct and the inverted (DC phase inversion) connections of feedforward loops, where Figure 30(b) shows how the inverted connections are achieved. The previous 3-stage structure of Figure 27, for example, has non-inverted feedforward loops with x parameter being equal to two.

Now, let's use the first-order single-pole approximation for the gain stages assuming that the oscillation amplitude remains small and sinusoidal shaped, which are the main requirements of the small-signal circuit analysis. Figure 31 shows the model of a single differential stage, where g_m and G_m represent the equivalent transconductances from the primary inputs M_n to the outputs M_{n+1} and from the secondary inputs M_{f+1} to the outputs M_{n+1} respectively. In addition, R and C represent the equivalent output resistance and the equivalent output capacitance at each differential output respectively. Note that a ring oscillator is a highly non-linear large signal feedback system. Therefore, under normal operating conditions, there is no constant



(a)



(b)

Figure 30: N-stage multiple pass ring-oscillator with (a) noninverted feedforward connections (b) inverted feedforward connections

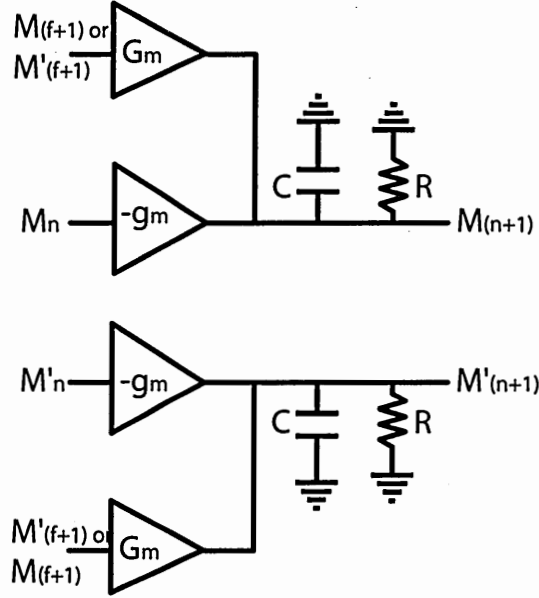


Figure 31: Ring-oscillator stage first-order model

operating point and parameters shift from their small-signal values. Transconductances of transistors, for example, decrease when signals get larger. Nevertheless, the main aim of this analysis is not finding the exact oscillation frequency but to gain an insight about the characteristics of the architecture such as the frequency improvement over a single-loop architecture.

At this point, the general multiple-pass topology is drawn again by moving the G_m blocks out of the gain stages without changing the connections, as shown in Figure 32. When this structure is compared with the subfeedback loop architecture, Figure 17 [23], one realizes that the connections are exactly the same. This discussion leads us to the conclusion that multiple-pass loop architecture and the subfeedback loop architecture are different interpretations of the same topology! This is in agreement with our previous discussion stating that all feedforward type architectures are based on the same concept. For the mathematical analysis, therefore, the approach given in [23] will be followed with the generalization of the conclusions to ring oscillators with even and odd number of stages and with positive and negative polarity feedforward loop connections.

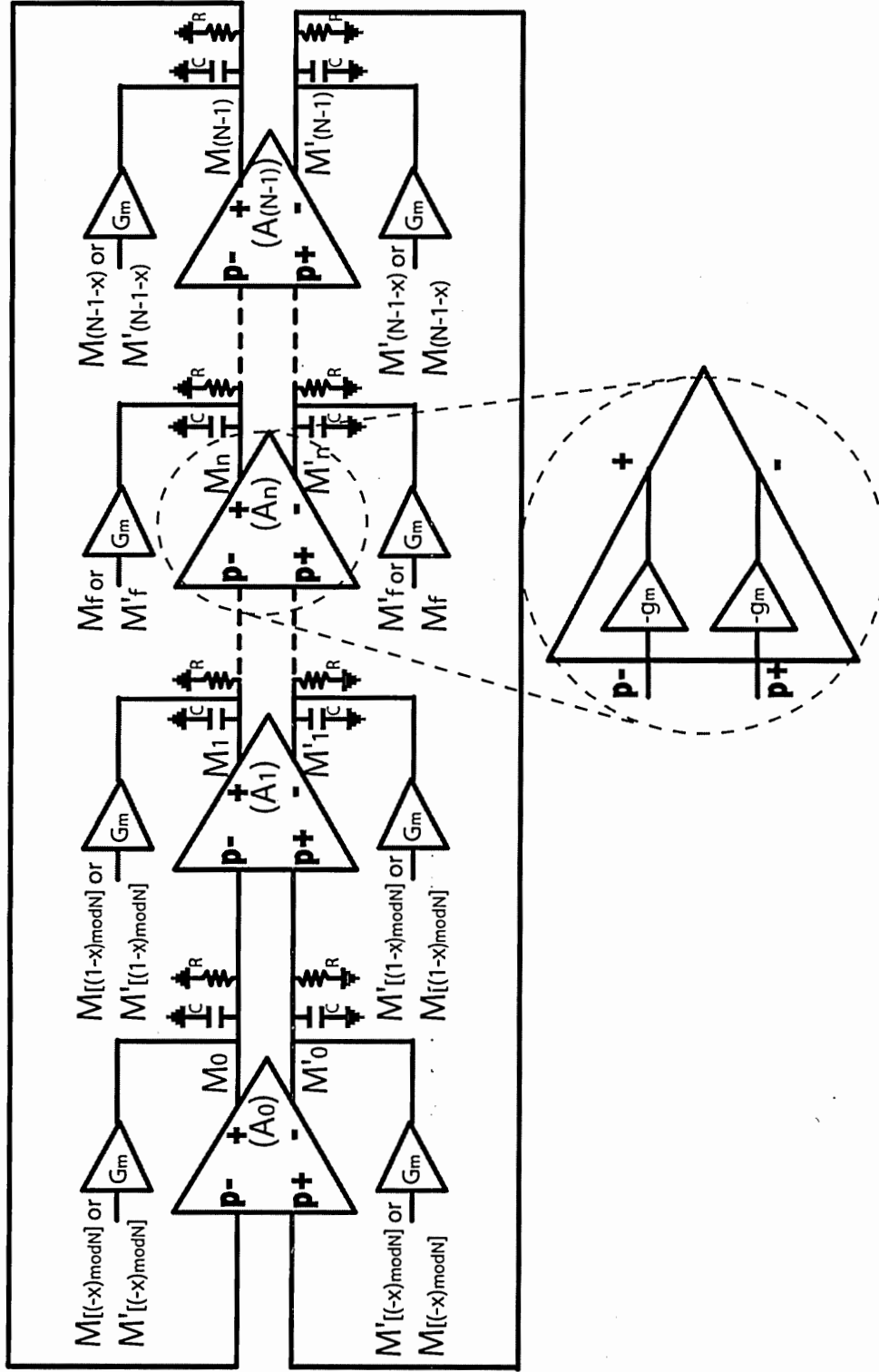


Figure 32: N-stage multiple pass ring-oscillator redrawn with G_m blocks moved out of the gain stages

For the oscillation mode that is desired, the phase relationship between the stages is strictly determined by the main loop. Next, the transfer function of a single stage will be derived from node M_n to M_{n+1} . The other set of input-output will have the same relationship. Defining θ as the phase difference between the output M_{n+1} and the input M_n ; and ϕ as the phase difference between the output M_{n+1} and the node connected to the secondary positive input $s+$ (M_{f+1} or M'_{f+1}), we have the following phase relationships

$$\begin{aligned} V_{n+1} &= V_n e^{-j\theta} \\ V_{n+1} &= V_{f+1} e^{-j\phi}, \end{aligned} \quad (64)$$

where $V_{n+1} = V(M_{n+1})$, $V_n = V(M_n)$, and $V_{f+1} = V(M_{f+1})$ or $V(M'_{f+1})$ depending on the connection scheme. Kirchhoff's current law at node M_{n+1} can be written as

$$V_{n+1} = \frac{R}{1 + j\omega RC} (-V_n g_m + V_{f+1} G_m). \quad (65)$$

Substituting $V_{f+1} = V_{n+1} e^{j\phi}$ we get

$$V_{n+1} = \frac{-Rg_m}{1 + j\omega RC} V_n + \frac{RG_m}{1 + j\omega RC} V_{n+1} e^{j\phi}. \quad (66)$$

Rearranging the V_n and V_{n+1} terms we get

$$V_{n+1} \left(\frac{1 + j\omega RC - RG_m e^{j\phi}}{1 + j\omega RC} \right) = -\frac{Rg_m}{1 + j\omega RC} V_n. \quad (67)$$

Therefore the transfer function $H(j\omega)$ can be written as

$$H(j\omega) = \frac{V_{n+1}}{V_n} = -\frac{Rg_m}{1 + j\omega RC - RG_m e^{j\phi}}, \quad (68)$$

and by distributing the $e^{j\phi}$ component into its imaginary and real components, transfer function can be written in this form

$$H(j\omega) = -\frac{Rg_m}{1 - G_m R \cos \phi + j(\omega RC - G_m R \sin \phi)}. \quad (69)$$

Phase of $H(j\omega)$ can be written as

$$\angle H(j\omega) = -\tan^{-1} \left(\frac{\omega RC - G_m R \sin \phi}{1 - RG_m \cos \phi} \right) \mp \pi. \quad (70)$$

We know that this phase is equal to $-\theta$, hence we have the following relationship

$$\mp \pi + \theta = \tan^{-1} \left(\frac{\omega RC - G_m R \sin \phi}{1 - RG_m \cos \phi} \right). \quad (71)$$

Taking tangent of both sides we get

$$\tan(\theta \mp \pi) = \tan \theta = \frac{\omega RC - G_m R \sin \phi}{1 - RG_m \cos \phi}. \quad (72)$$

Barkhausen criterion state that the loop should have unity gain and a phase shift of an integer multiple of 2π at the frequency of oscillation. According to this requirement the magnitude of the transfer function of a single stage should satisfy the following condition

$$|H(j\omega)| = \frac{|Rg_m|}{\sqrt{(1 - G_m R \cos \phi)^2 + (\omega RC - G_m R \sin \phi)^2}} \geq 1 \quad (73)$$

$$Rg_m \geq \sqrt{(1 - G_m R \cos \phi)^2 + (\omega RC - G_m R \sin \phi)^2}. \quad (74)$$

We can simplify this expression by using the relationship between $\tan \theta$ and $\cos \theta$ and substituting

$$\sqrt{(1 - G_m R \cos \phi)^2 + (\omega RC - G_m R \sin \phi)^2} = \left| \frac{1 - G_m R \cos \phi}{\cos \theta} \right|, \quad (75)$$

where we end up with [23]

$$g_m R \geq \left| \frac{1 - G_m R \cos \phi}{\cos \theta} \right|, \quad (76)$$

which shows the minimum required gain from a single stage to satisfy the oscillation criterion. To find the oscillation frequency, using Equation (72), we can come up with the relationship

$$\omega RC - G_m R \sin \phi = \tan \theta - RG_m \cos \phi \tan \theta. \quad (77)$$

Next, we can write the frequency in terms of the other parameters as

$$\omega = \frac{\tan \theta}{RC} + \left[\frac{G_m}{C} \sin \phi - \tan \theta \frac{G_m}{C} \cos \phi \right], \quad (78)$$

and finally [23]

$$\omega = \frac{\tan \theta}{RC} + \frac{G_m}{C} [\sin \phi - \tan \theta \cos \phi]. \quad (79)$$

When the secondary transconductance stages are removed by setting $G_m = 0$, the frequency converges to $\tan \theta / RC$, which is the oscillation frequency of a single-loop ring oscillator. Therefore, the second term corresponds to the frequency change because of the auxiliary feedforward loops. It is easily seen from this equation that to improve the maximum frequency of the oscillator the second term should be positive, that is

$$\sin \phi - \tan \theta \cos \phi > 0. \quad (80)$$

This constant is defined as the frequency improvement factor " F_{imp} " [23]. From this equation one can conclude that for the highest frequency, the feedforward configuration with the highest frequency improvement factor should be selected. The absolute increase in the maximum frequency, however, also depends on the other factors such as the change of the time constant RC of the stages. For an increase in the frequency, the additional loading of the secondary transconductance stage should be minimal. If we assume that by the addition of feedforward stages the output resistance and the load capacitance of a single stage changes from R to R' and C to C' respectively, the absolute frequency increase can be written as [23]

$$\frac{\omega'}{\omega} = \frac{RC}{R'C'} + F_{imp}(\tan \theta)^{-1} R G_m \left(\frac{C}{C'} \right) \quad (81)$$

where ω' is the frequency of the multiple-pass architecture and ω is the frequency of the single-loop architecture.

Here, it is crucial to note that even by taking the output resistance and the load capacitance variances into account, optimizing the frequency improvement factor may not be sufficient to obtain the maximum possible frequency. The Barkhausen oscillation criterion should also be considered during the design. For the configuration with the highest frequency improvement factor, the design parameters that are needed to satisfy the minimum required gain, which is defined by Equation (76), may result in a lower maximum frequency when compared to an another configuration with a lower frequency improvement factor.

To apply the multiple-pass loops with a specific configuration, the required connection scheme is straightforward for a ring oscillator with an odd number of stages. The architecture is symmetric and phase relationship between the stages should be kept same for stable steady state oscillations to exist in the loop. We already defined θ as the phase difference between a positive input terminal and a negative output terminal of a single stage, and vice versa. θ is same for every single stage due to the symmetry of the structure. The other constraint is on the ϕ , which is the phase difference between the output and the input of the transconductance stages forming the feedforward loops. Connections should be arranged such that ϕ is same in every feedforward connection. Figures 33 and 34 show the connections schemes for configurations with $(N, x, sign) = (3, 2, +)$ and $(N, x, sign) = (5, 3, -)$, where N is the number of stages in the main loop, x is the number of stages between the input and the output of the additional transconductance stages, and $sign$ determines if the feedforward loops are directly connected or inverted. Note that this definition of x is slightly different from the previous definition of x that was defined at the beginning of this chapter. Phase relationships between nodes are also shown on the figures.

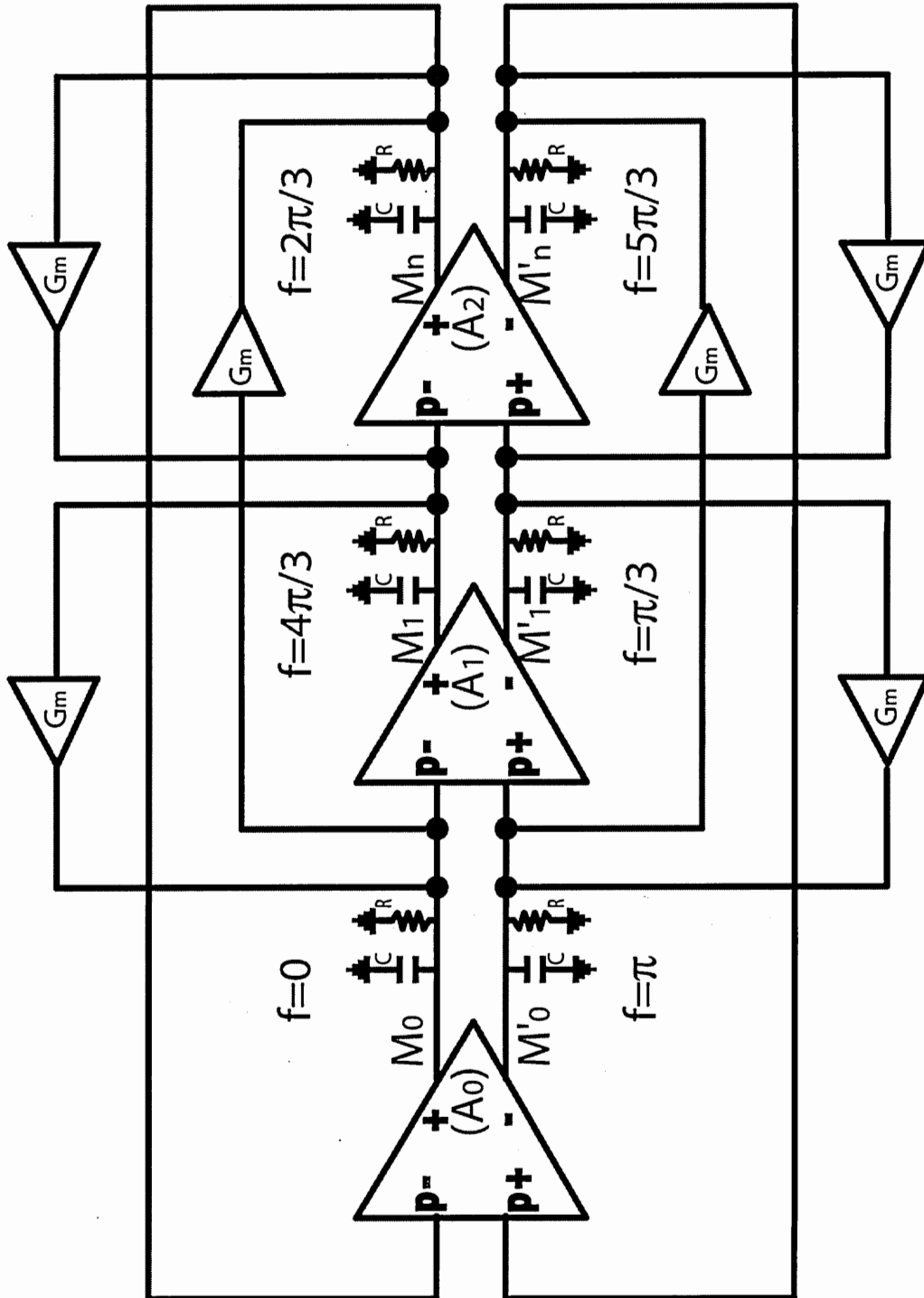


Figure 33: Multiple pass ring-oscillator with $(N, x, \text{sign}) = (3, 2, +)$

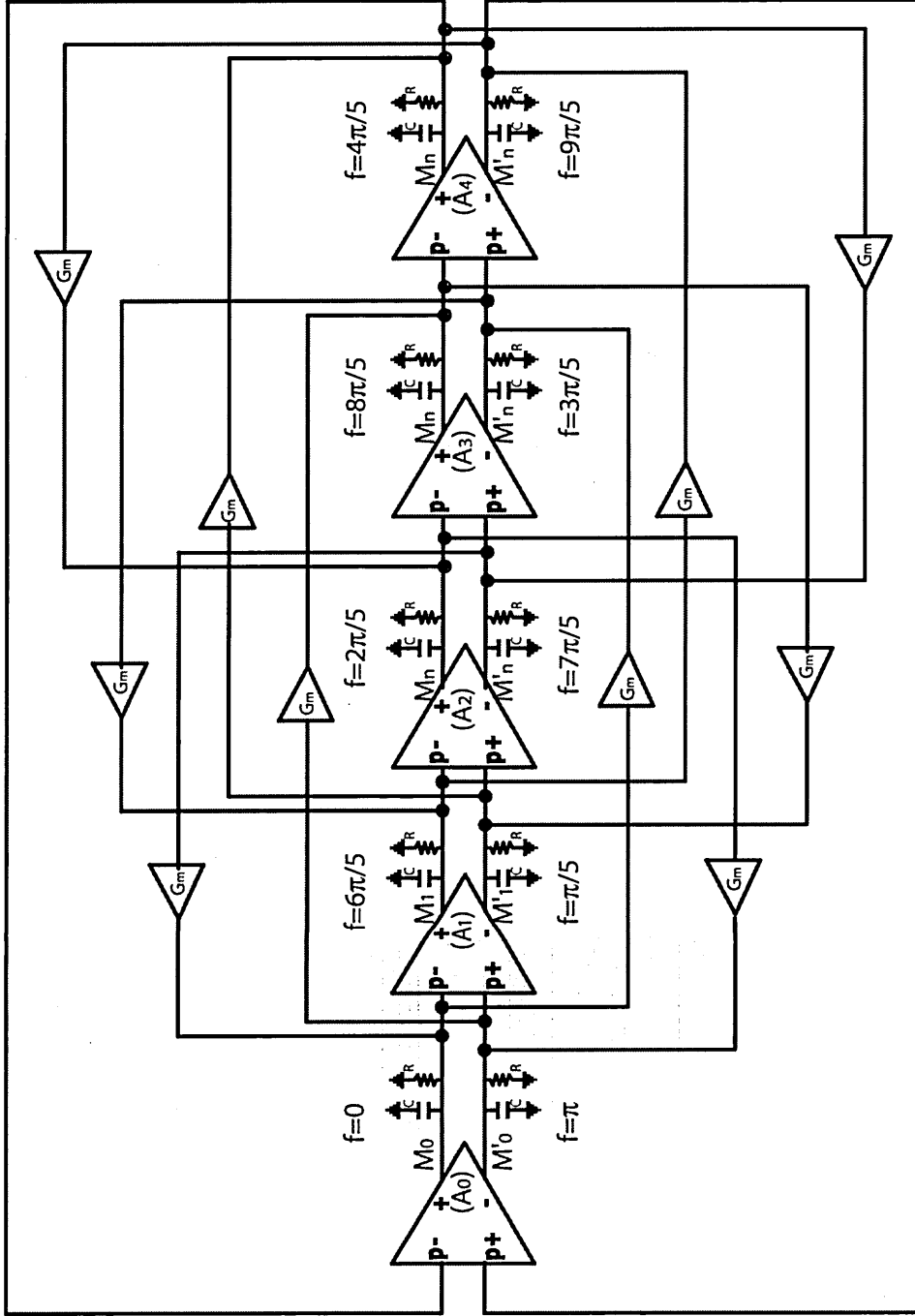


Figure 34: Multiple pass ring-oscillator with $(N, x, \text{sign}) = (5, 3, -)$

5.1.1.3 Even Number of Stages

For an even number of stages, connection scheme is not trivial due to the asymmetric connections in the loop. In the main loop, one set of the connections is reversed when compared to the other connections to provide the required extra π radians phase shift to satisfy the Barkhausen phase criteria. Regardless of this connection scheme, for stable steady state oscillations, ϕ relationship in the feedforward loops should be kept same for every connection. This means that if any of the auxiliary transconductance stages bridge over the reversed connection, the output of it should be connected in reverse polarity. Figures 35 and 36 show how this is achieved for configurations with $(N, x, sign) = (4, 2, -)$ and $(N, x, sign) = (6, 4, +)$.

Now, it will be shown how these frequency and gain equations apply to ring oscillators with even number of stages. First of all, first order single pole model of Figure 31 still holds since the internal structure of the stages are not modified; only connections are modified. Therefore, transfer function of each stage will remain same as

$$H(j\omega) = -\frac{Rg_m}{1 - G_m R \cos \phi + j(\omega RC - G_m R \sin \phi)}, \quad (82)$$

with the exception of the one with reversed input connections, which can be written as

$$H_1(j\omega) = \frac{Rg_m}{1 - G_m R \cos \phi' + j(\omega RC - G_m R \sin \phi')}. \quad (83)$$

Here $\phi' = \phi$ because of the connection scheme; therefore, Equation (83) reduces to Equation (82) with a sign difference because of the DC inversion. The total phase difference around the loop can be written as

$$2\pi k = \angle H_1(j\omega) + \angle H_2(j\omega) + \angle H_3(j\omega) + \dots + \angle H_N(j\omega), \quad (84)$$

where $H_1(j\omega)$, $H_2(j\omega)$, $H_3(j\omega)$, ..., $H_N(j\omega)$ are the transfer functions of gain stages,

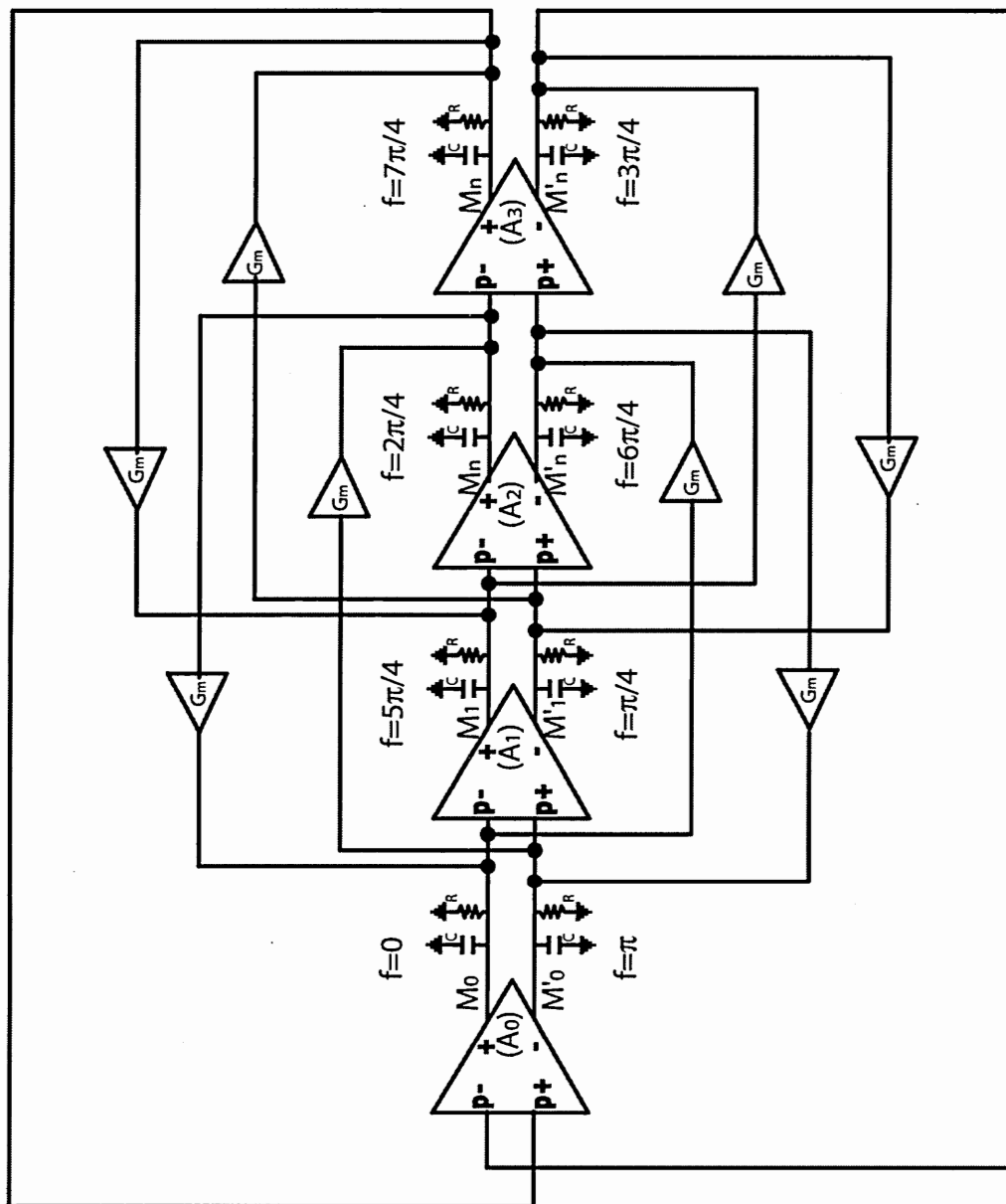


Figure 35: Multiple pass ring-oscillator with $(N, x, \text{sign}) = (4, 2, -)$

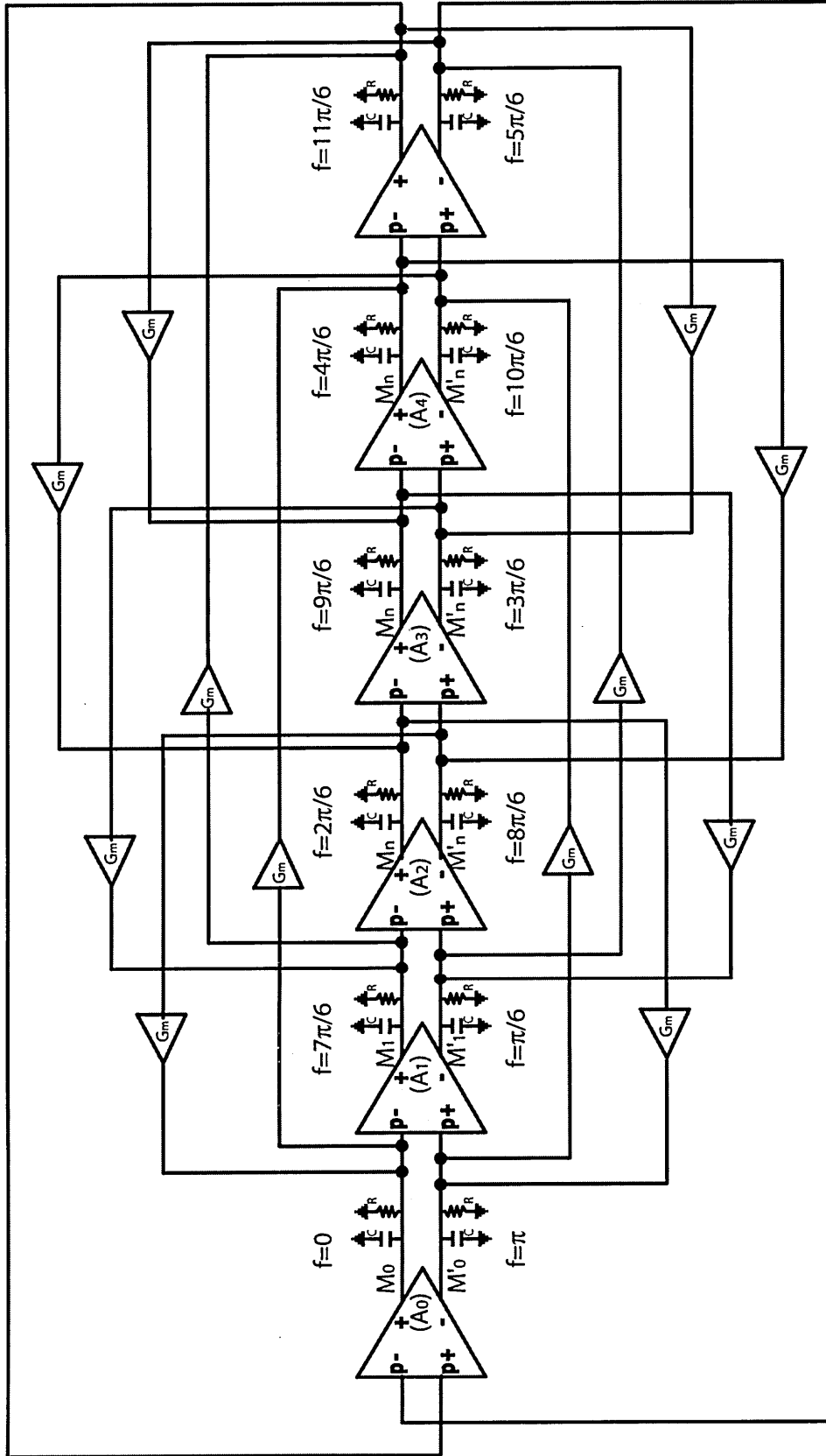


Figure 36: Multiple pass ring-oscillator with $(N, x, \text{sign}) = (6, 4, +)$

and k is an integer. This leads to

$$2\pi k = \angle H_1(j\omega) - (N - 1)\theta, \quad (85)$$

where $H_1(j\omega)$ is the transfer function of the gain stage with the inverted primary input connections. Due to the phase relationship between the stages that is imposed by the connections in the main loop, we have

$$\angle H_1(j\omega) = -\theta \pm \pi, \quad (86)$$

and

$$\theta = \frac{(2n - 1)\pi}{N}, \quad (87)$$

where n is an integer. Because the derivation of the transfer functions were performed from an inverting input to a non-inverting output, θ should be the angle that is greater than π and closest to π among all the possibilities given by Equation (87). For the connections of Figure 35, this reduces to $\theta = 5\pi/4$, and for the loop of Figure 36, to $\theta = 7\pi/6$. If we follow the previous derivation of frequency, we will end up with the Equation (79) for every node excluding the output nodes of the main loop stage with reversed inputs. Equating the phase of that stage, which is $-\theta \pm \pi$, to the phase of the transfer function in Equation (83), we get

$$-\theta \pm \pi = -\tan^{-1} \left[\frac{\omega RC - G_m R \sin \phi'}{1 - RG_m \cos \phi'} \right], \quad (88)$$

and

$$\tan(\theta \mp \pi) = \tan \theta = \frac{\omega RC - G_m R \sin \phi'}{1 - RG_m \cos \phi'}. \quad (89)$$

Substituting $\phi' = \phi$, we end up with

$$\omega = \frac{\tan \theta}{RC} + \frac{G_m}{C} [\sin \phi - \tan \theta \cos \phi]. \quad (90)$$

which is exactly same as Equation (79), as it should be. Following a similar analysis that we performed for the minimum gain requirement of stages, for the stage with reversed inputs we have

$$g_m R \geq \left| \frac{1 - G_m R \cos \phi'}{\cos(\theta \pm \pi)} \right|, \quad (91)$$

which reduces to

$$g_m R \geq \left| \frac{1 - G_m R \cos \phi}{\cos(\theta)} \right|, \quad (92)$$

by substituting $\phi' = \phi$ and $|\cos(\theta \pm \pi)| = |-\cos(\theta)| = |\cos(\theta)|$, which is exactly same as Equation (76). Other stages also have the same requirement.

This finalizes the analysis for differential ring oscillators with multiple-pass loop architectures. Tables 2 and 3 tabulate the frequency improvement factors F_{imp} and minimum gain requirements for different ring oscillator configurations. Note that the sign of the frequency improvement factor changes between different configurations. A positive frequency improvement factor, for example, means that the feedforward connections help to improve the switching speed by providing extra drive power at the output. For the non-inverted connection scheme, this happens whenever an even number of stages are bridged over by the feedforward loop. This corresponds to the improvement of the frequency because the outputs start switching earlier in time with the help of the feedforward loops. If an odd number of stages are bridged over by the feedforward loops, the frequency decreases because the feedforward loops oppose the switching by trying to switch the outputs at the reverse direction. For the inverted connection scheme, that is $(N, x, \text{sign}) = (N, x, -)$, the opposite is true as seen in Tables 2 and 3.

In the next sections, it will be explained how the theory relates to the actual implementations by comparing the simulations and the calculations.

Table 2: Frequency improvement factors and gain requirements of multiple-pass loop configurations for $3 \leq N \leq 7$

N	x	sign	F_{imp}	θ	ϕ	Gain requirement
3	2	+	1.730	$4\pi/3$	$2\pi/3$	$g_m R \geq 2 1 + 0.5G_m R $
3	2	-	-1.730	$4\pi/3$	$\pi + 2\pi/3$	$g_m R \geq 2 1 - 0.5G_m R $
4	2	+	1	$5\pi/4$	$2\pi/4$	$g_m R \geq 1.414$
4	2	-	-1	$5\pi/4$	$\pi + 2\pi/4$	$g_m R \geq 1.414$
4	3	+	-1.414	$5\pi/4$	$7\pi/4$	$g_m R \geq 1.414 1 - 0.707G_m R $
4	3	-	1.414	$5\pi/4$	$\pi + 7\pi/4$	$g_m R \geq 1.414 1 + 0.707G_m R $
5	2	+	0.727	$6\pi/5$	$2\pi/5$	$g_m R \geq 1.236 1 - 0.309G_m R $
5	2	-	-0.727	$6\pi/5$	$\pi + 2\pi/5$	$g_m R \geq 1.236 1 + 0.309G_m R $
5	3	+	-1.176	$6\pi/5$	$8\pi/5$	$g_m R \geq 1.236 1 - 0.309G_m R $
5	3	-	1.176	$6\pi/5$	$\pi + 8\pi/5$	$g_m R \geq 1.236 1 + 0.309G_m R $
5	4	+	1.176	$6\pi/5$	$4\pi/5$	$g_m R \geq 1.236 1 + 0.809G_m R $
5	4	-	-1.176	$6\pi/5$	$\pi + 4\pi/5$	$g_m R \geq 1.236 1 - 0.809G_m R $)
6	2	+	0.577	$7\pi/6$	$2\pi/6$	$g_m R \geq 1.155 1 - 0.5G_m R $
6	2	-	-0.577	$7\pi/6$	$\pi + 2\pi/6$	$g_m R \geq 1.155 1 + 0.5G_m R $
6	3	+	-1	$7\pi/6$	$9\pi/6$	$g_m R \geq 1.155$
6	3	-	1	$7\pi/6$	$\pi + 9\pi/6$	$g_m R \geq 1.155$
6	4	+	1.155	$7\pi/6$	$4\pi/6$	$g_m R \geq 1.155 1 + 0.5G_m R $)
6	4	-	-1.155	$7\pi/6$	$\pi + 4\pi/6$	$g_m R \geq 1.155 1 - 0.5G_m R $
6	5	+	-1	$7\pi/6$	$11\pi/6$	$g_m R \geq 1.155 1 - 0.866G_m R $
6	5	-	1	$7\pi/6$	$\pi + 11\pi/6$	$g_m R \geq 1.155 1 + 0.866G_m R $
7	2	+	0.481	$8\pi/7$	$2\pi/7$	$g_m R \geq 1.109 1 - 0.623G_m R $
7	2	-	-0.481	$8\pi/7$	$\pi + 2\pi/7$	$g_m R \geq 1.109 1 + 0.623G_m R $
7	3	+	-0.867	$8\pi/7$	$10\pi/7$	$g_m R \geq 1.109 1 + 0.222G_m R $
7	3	-	0.867	$8\pi/7$	$\pi + 10\pi/7$	$g_m R \geq 1.109 1 - 0.222G_m R $
7	4	+	1.082	$8\pi/7$	$4\pi/7$	$g_m R \geq 1.109 1 + 0.222G_m R $
7	4	-	-1.082	$8\pi/7$	$\pi + 4\pi/7$	$g_m R \geq 1.109 1 - 0.222G_m R $
7	5	+	-1.082	$8\pi/7$	$12\pi/7$	$g_m R \geq 1.109 1 - 0.623G_m R $
7	5	-	1.082	$8\pi/7$	$\pi + 12\pi/7$	$g_m R \geq 1.109 1 + 0.623G_m R $
7	6	+	0.868	$8\pi/7$	$6\pi/7$	$g_m R \geq 1.109 1 + 0.901G_m R $
7	6	-	-0.868	$8\pi/7$	$\pi + 6\pi/7$	$g_m R \geq 1.109 1 - 0.901G_m R $

Table 3: Frequency improvement factors and gain requirements of multiple-pass loop configurations for $8 \leq N \leq 9$

N	x	sign	F_{imp}	θ	ϕ	Gain requirement
8	2	+	0.414	$9\pi/8$	$2\pi/8$	$g_m R \geq 1.08 1 - 0.707G_m R $
8	2	-	-0.414	$9\pi/8$	$\pi + 2\pi/8$	$g_m R \geq 1.08 1 + 0.707G_m R $
8	3	+	-0.765	$9\pi/8$	$11\pi/8$	$g_m R \geq 1.08 1 + 0.382G_m R $
8	3	-	0.765	$9\pi/8$	$\pi + 11\pi/8$	$g_m R \geq 1.08 1 - 0.382G_m R $
8	4	+	1	$9\pi/8$	$4\pi/8$	$g_m R \geq 1.08$
8	4	-	-1	$9\pi/8$	$\pi + 4\pi/8$	$g_m R \geq 1.08$
8	5	+	-1.082	$9\pi/8$	$13\pi/8$	$g_m R \geq 1.08 1 - 0.382G_m R $
8	5	-	1.082	$9\pi/8$	$\pi + 13\pi/8$	$g_m R \geq 1.08 1 + 0.382G_m R $
8	6	+	1	$9\pi/8$	$6\pi/8$	$g_m R \geq 1.08 1 + 0.707G_m R $
8	6	-	-1	$9\pi/8$	$\pi + 6\pi/8$	$g_m R \geq 1.08 1 - 0.707G_m R $
8	7	+	-0.765	$9\pi/8$	$15\pi/8$	$g_m R \geq 1.08 1 - 0.923G_m R $
8	7	-	0.765	$9\pi/8$	$\pi + 15\pi/8$	$g_m R \geq 1.08 1 + 0.923G_m R $
9	2	+	0.364	$10\pi/9$	$2\pi/9$	$g_m R \geq 1.06 1 - 0.766G_m R $
9	2	-	-0.364	$10\pi/9$	$\pi + 2\pi/9$	$g_m R \geq 1.06 1 + 0.766G_m R $
9	3	+	-0.684	$10\pi/9$	$12\pi/9$	$g_m R \geq 1.06 1 + 0.5G_m R $
9	3	-	0.684	$10\pi/9$	$\pi + 12\pi/9$	$g_m R \geq 1.06 1 - 0.5G_m R $
9	4	+	0.922	$10\pi/9$	$4\pi/9$	$g_m R \geq 1.06 1 - 0.174G_m R $
9	4	-	-0.922	$10\pi/9$	$\pi + 4\pi/9$	$g_m R \geq 1.06 1 + 0.174G_m R $
9	5	+	-1.048	$10\pi/9$	$14\pi/9$	$g_m R \geq 1.06 1 - 0.174G_m R $
9	5	-	1.048	$10\pi/9$	$\pi + 14\pi/9$	$g_m R \geq 1.06 1 + 0.174G_m R $
9	6	+	1.048	$10\pi/9$	$6\pi/9$	$g_m R \geq 1.06 1 + 0.5G_m R $
9	6	-	-1.048	$10\pi/9$	$\pi + 6\pi/9$	$g_m R \geq 1.06 1 - 0.5G_m R $
9	7	+	-0.922	$10\pi/9$	$16\pi/9$	$g_m R \geq 1.06 1 - 0.766G_m R $
9	7	-	0.922	$10\pi/9$	$\pi + 16\pi/9$	$g_m R \geq 1.06 1 + 0.766G_m R $
9	8	+	0.684	$10\pi/9$	$8\pi/9$	$g_m R \geq 1.06 1 + 0.94G_m R $
9	8	-	-0.684	$10\pi/9$	$\pi + 8\pi/9$	$g_m R \geq 1.06 1 - 0.94G_m R $

5.2 Gain Stage

By changing the architecture, the maximum oscillation frequency of a ring oscillator can be increased, but phase noise and jitter are also important considerations. Many ring oscillators use analog gain stages, but biasing the transistors into continuous (Q-point) conduction increases their contribution to the total noise in the circuit. To overcome this problem, the gain transistors can be periodically switched in and out of conduction, which reduces the noise. This is shown by [9]

$$P_{noise} = \frac{\Delta T}{T} \frac{4kTR}{1 + (2\pi f_m RC)^2}, \quad (93)$$

where P_{noise} is the approximate noise power of an oscillator, T is the oscillation period, ΔT is the conducting time of the transistors in a period, f_m is the offset frequency, and RC is the time constant of the delay cell.

Note that this result is consistent with the predictions of the phase noise models discussed in Chapter IV proposed by Hajimiri [32] and Harjani [6]. Closed form of the ISF of ring oscillators given in Equation (44), for example, suggests that the peak value of ISF can be minimized by having sharper transitions. This is equivalent to an increase in the rise/fall rates of the output signals that can be obtained by full-switching of the transistors. Ring oscillator phase noise equations given in Equation (59) leads to a similar conclusion by stating that clipped signals are necessary for noise reduction.

Furthermore, all of the given phase noise models pronounce that phase noise values improve with increasing signal power. This is, in fact, straightforward to deduce because phase noise is defined as the ratio of the noise power to the carrier power and thus can be improved by increasing the signal-to-noise-ratio (SNR) of the system. SNR can be improved by letting circuits dissipate more power, which leads to the conclusion that rail-to-rail signal levels and increased current feed is necessary for a low noise circuit.

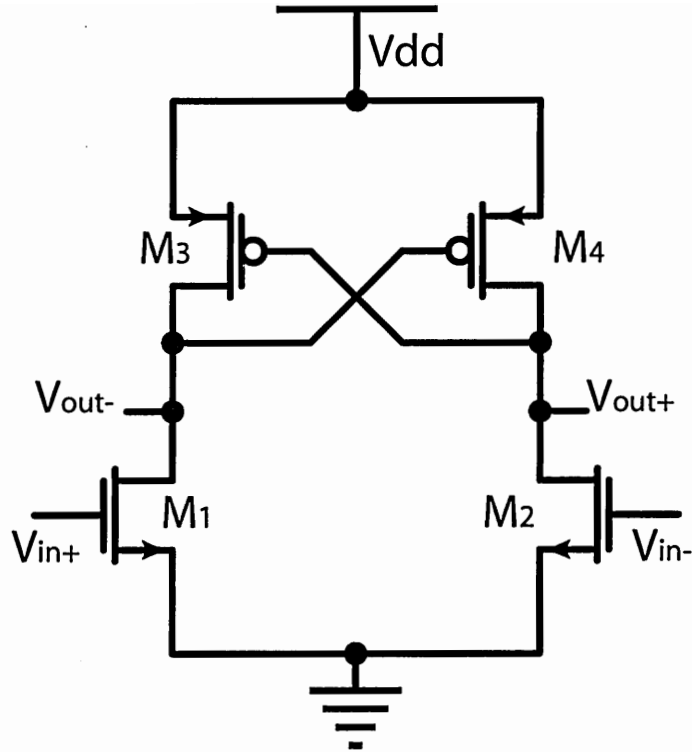


Figure 37: Saturated delay stage with PMOS cross-coupled transistors

5.2.1 Saturated Stage

A simple design that provides both of these characteristics is the saturated gain stage with regenerative cross-coupled PMOS transistors as shown in Figure 37. This provides for rail-to-rail output signals and full switching of the FETs in the stage. From a qualitative viewpoint, it can be seen that the feedback properties of the latching transistors M_3 and M_4 speed up the signal transitions at the output. Instead of relying solely on the stage gain mechanism, the latch circuitry causes the outputs to change once the voltages pass the value needed to trigger the switching event. This improves both the oscillation frequency and the noise performance of the VCO. The saturated gain stage produces rail-to-rail voltage swings at the output, which precludes the use of linear circuit analysis techniques.

Applying equations (59) and (93) to this circuit shows the reduction of the thermal

noise at the output node. In addition, it is known that periodic switching of the gate-source voltage of a MOS transistor with rail-to-rail signals reduces the flicker ($1/f$) noise [34].

5.2.2 Delay Control

Notice that this simple structure does not include any means to control the frequency of a ring oscillator employing this stage, i.e. it does not have a control input. There are a couple of different approaches on how to modify this stage to add frequency control option. Addition of a tail current source is one of these methods, as shown in Figure 38(a). However, cascaded connections result in a loss of the signal swing range, which is undesirable for noise performance. Also, the tail current source used in conjunction with a current mirror may result in excessive upconversion of the transistor low frequency noise near the oscillation frequency degrading the noise performance of the oscillator [8, 32]. Another approach is controlling the output loading by using controllable capacitors/resistors connected to the output nodes as shown in Figure 38(b). Additional loading reduces the oscillation frequency and controllable varactors/resistors usually do not have linear characteristics resulting in non-linear frequency-voltage characteristics, which is undesirable.

Delay characteristics of this saturated stage can also be controlled by varying the strength of the latch. This can be accomplished by inserting MOS switches inside the feedback path as shown in Figure 39 [9, 35]. It avoids the use of cascaded-connections and a tail-current source transistor that would limit the signal-swing and add more noise to the output. Therefore, this kind of frequency control based on the control of the latch strength is preferable over the other frequency control techniques for a high-frequency low-noise voltage controlled ring oscillator design. NMOS transistors M_3 and M_4 are used to control the strength of the latching by altering the positive feedback from the coupled-pair M_1 and M_2 . Once the latch is triggered, it helps

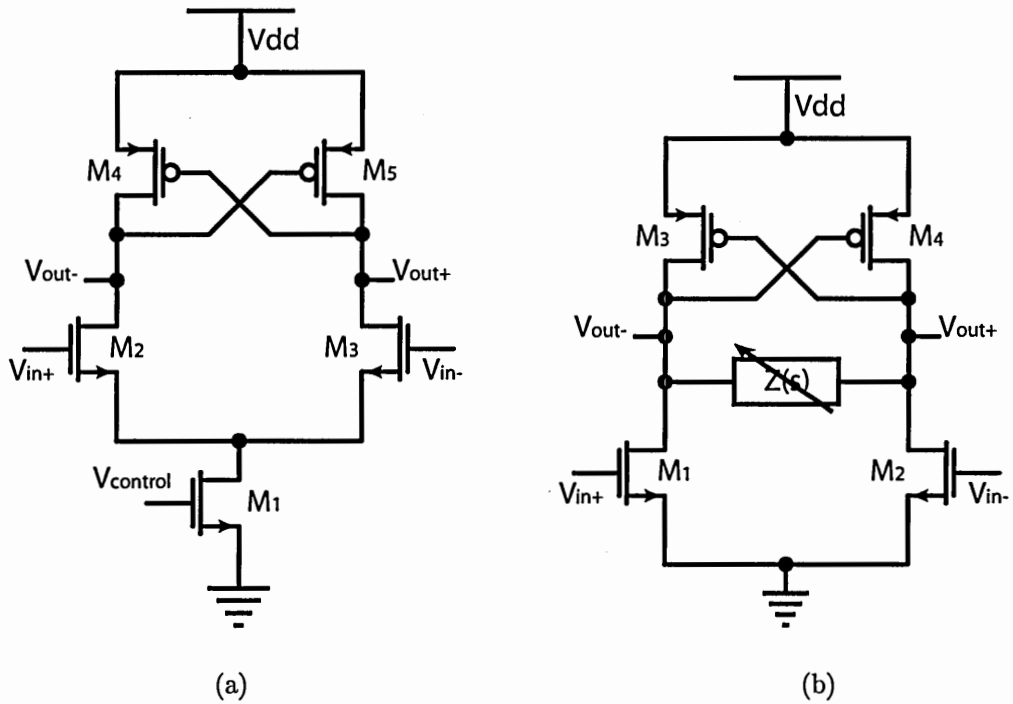


Figure 38: Saturated delay stage with (a) a tail current source for frequency control (b) variable loads for frequency control

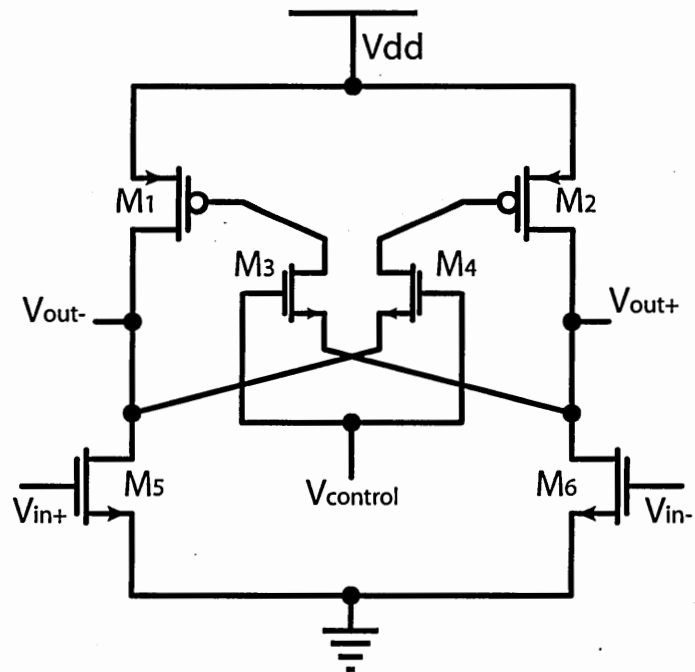


Figure 39: Saturated delay stage with feedback control

pull up the voltage on one side while simultaneously reducing it on the other. The control voltage V_{cont} is connected to the gates of M_3 and M_4 such that increasing V_{cont} increases the positive feedback gain in the latch by reducing the FET resistance. This makes it more difficult to change the output voltage, thus increasing the stage delay which reduces the oscillation frequency. Decreasing the control voltage has the opposite effect: the feedback is reduced and the outputs are allowed to switch faster, thus increasing the frequency. Tuning range of an oscillator utilizing this stage can be varied simply by modifying the sizes of the feedback switches, M_3 and M_4 . At a fixed control voltage, increasing the switch sizes reduces the minimum resistance of the switches that allows the feedback to get relatively stronger. This increases the frequency tuning range at the low-end with a slight reduction of the maximum frequency because of the additional loading at the output. On the other hand, using smaller sized switches reduces the tuning range by limiting the strength of the latch, which gives more linear frequency-voltage characteristics. Therefore, there is a tradeoff between the tuning range and the linearity, and the optimum switch sizes should be selected according to the specifications of the system.

5.2.3 Type-I Saturated Stage

Note that two pairs of inputs are needed to adapt the stage to a multiple-pass architecture, which is equivalent to the addition of secondary transconductance stages to form the auxiliary feedforward loops. As shown in Figure 40 [9], transistors M_5 and M_6 are the primary input transistors that are used to build the main ring oscillator loop; while M_7 and M_8 are the secondary input transistors, or secondary transconductance stages. This stage will be called the "type-I saturated stage" from now on. Intuitively, one can deduce that the feedforward loops should be designed to be weaker than the main loop to obtain the desired frequency increase without disturbing the operation of the oscillator. Our previous assumption dictating that

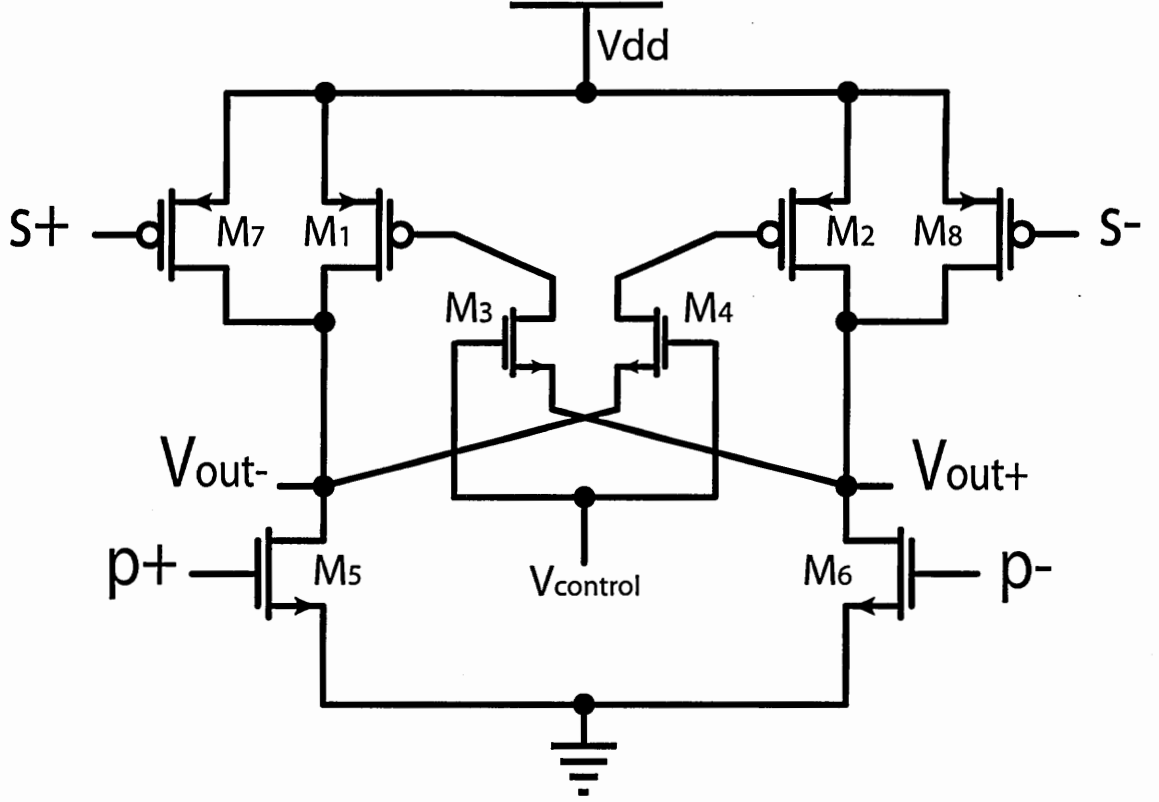


Figure 40: Saturated delay stage with feedback control for multiple pass loop architecture implementation

the phase relationship between the stages should be solely determined by the main loop also requires the secondary loops to be designed weaker. Otherwise, race conditions may take place in the oscillator where it would not be clear which loop takes over and establishes the phase relationship between stages resulting in undesired oscillation modes, or the oscillator simply may not oscillate at all. Quantitatively, Equation (76) shows that the transconductance g_m of main stages should be designed to be larger than the transconductance G_m of the feedforward stages to satisfy the Barkhausen oscillation criterion. Therefore, the secondary input transistors, M_7 and M_8 , are purposely designed to be weaker than the primary devices, M_5 and M_6 .

5.2.4 Type-II Saturated Stage

Type-I saturated stage offers a wide tuning range, high oscillation frequency and low noise with a simple structure. It's control network, however, is single ended. It is

well known that a differential control network reduces the susceptibility to noise on the control lines. Furthermore, depending on where the control voltage is referred to, ground and supply bounces may create a problem in single-ended control schemes. Another problem related with using the type-I saturated stage is the high voltage-to-frequency gain of the designs. This is undesirable since noise on the control line will translate into larger jitter at the output. Figure 41 shows a gain stage design employing multiple control paths that overcomes these problems in the expense of increased complexity. This stage will be called "type-II saturated stage" throughout this thesis.

Charge pumps, which are synchronized with the primary inputs, have been added on both differential sides to provide the desired control. The latch feedback control provides coarse tuning, while fine tuning is achieved using a differential input current control circuit, which is illustrated in Figure 42. Note that, both of the control paths are integrated in to the delay cell structure without current starving the cell. This helps to increase the output signal levels and prevent a reduction in the noise performance.

The operation of the circuit can be described using a simplified model of the gain stage. As illustrated in Figure 43, the simplified model is constructed by replacing the fine-tuning circuitry (charge pumps and the differential current source) with ideal switches and current-sources, and the multiple-pass stage core with a simple gain stage with active loads. The simple form of the gain stage is shown in Figure 44. Assuming that the initial state is given as $[V_{out+} \ V_{out-} \ p+ \ p-] = [\text{High Low High Low}]$; the circuit takes the form given in Figure 45 upon switching of the positive input $p+$ from high to low at $t = 0$ ($p-$ switched from low to high); C_{out+} and C_{out-} representing the total capacitance at the output nodes of the stage. Therefore, the fine-tuning circuitry helps to charge/discharge the output nodes by providing an additional amount of current.

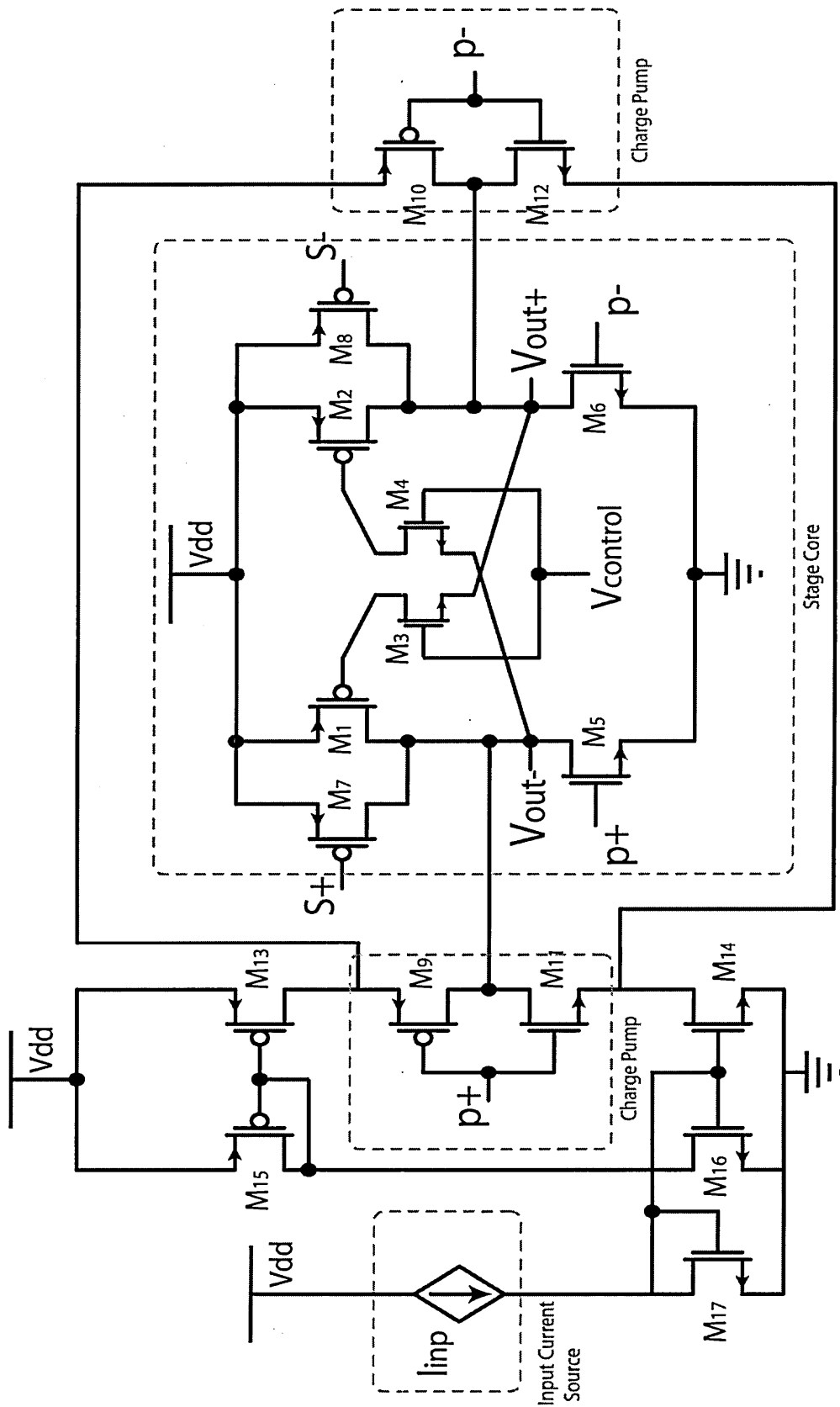


Figure 41: Saturated delay stage with double control paths

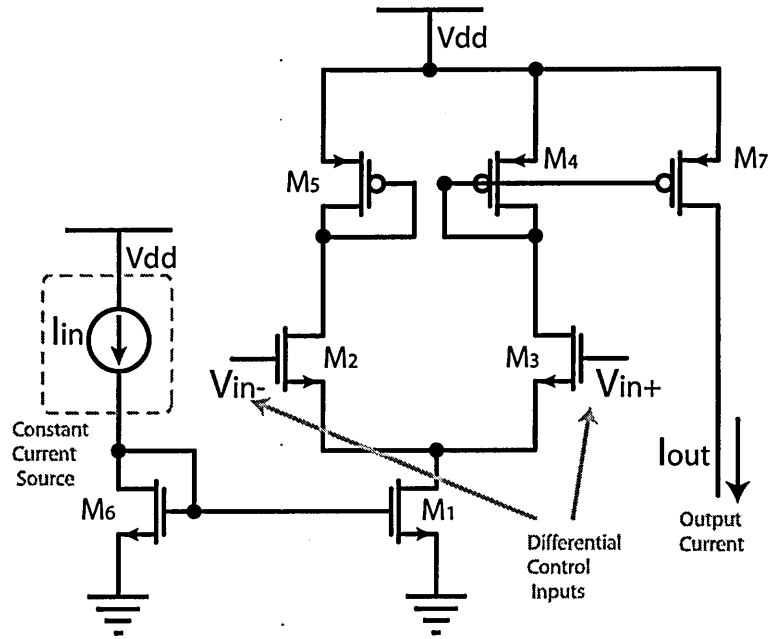


Figure 42: Differential input current control circuitry

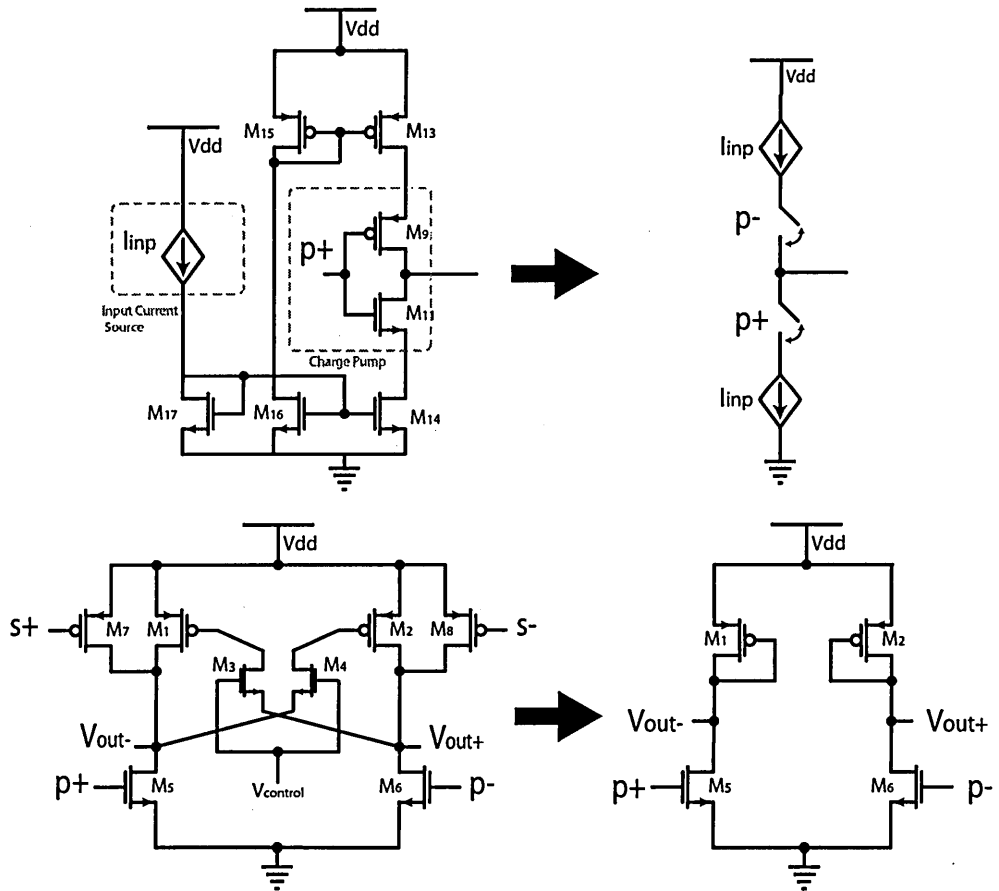


Figure 43: Simplifications on the type-II saturated stage

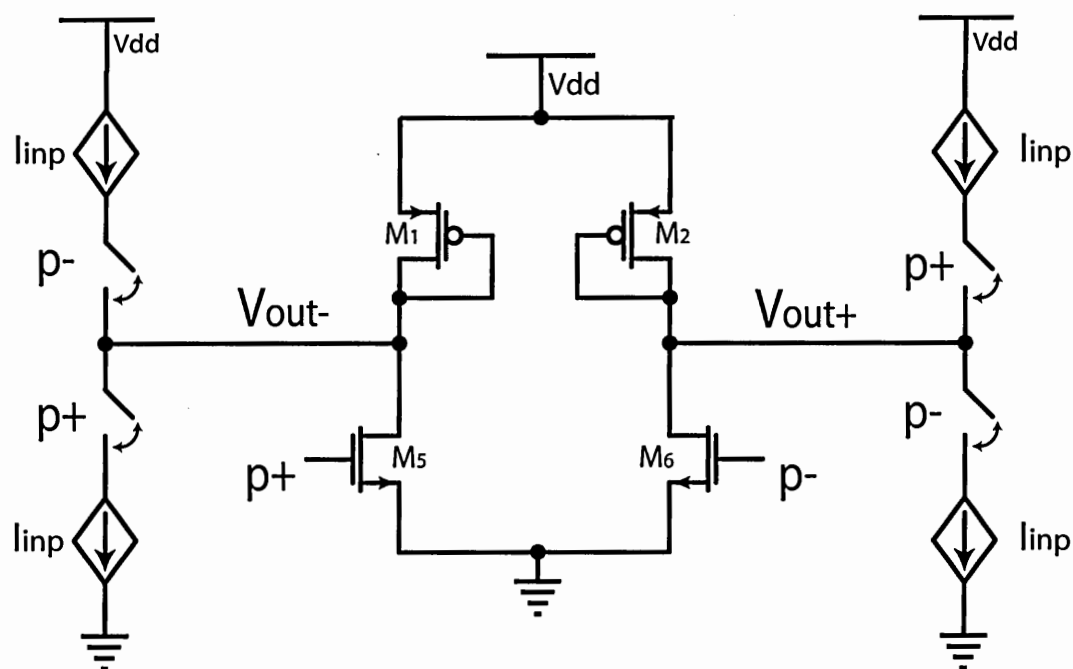


Figure 44: Type-II saturated stage, simplified

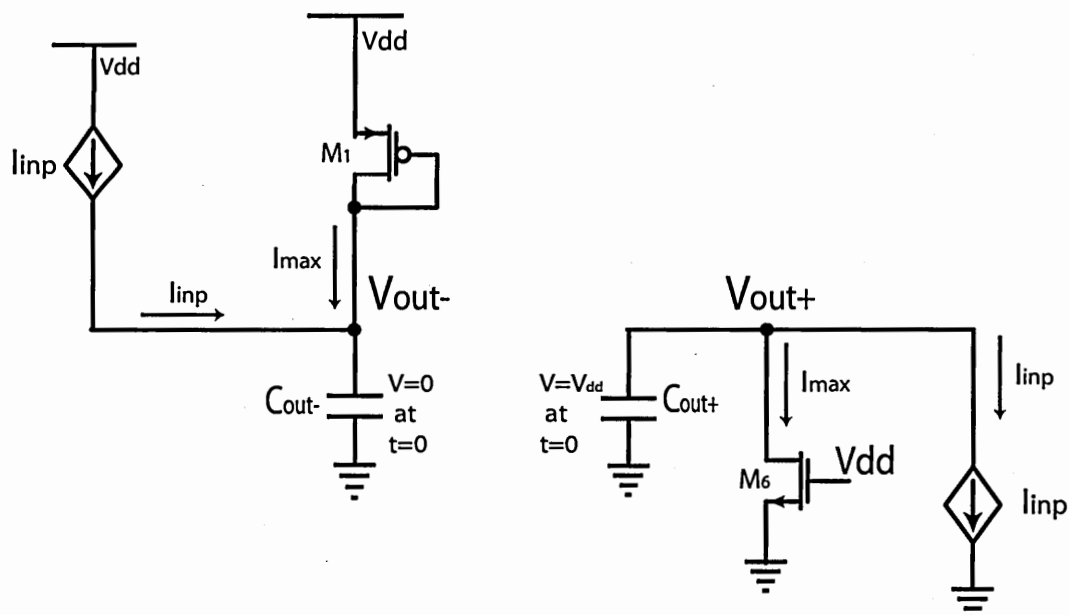


Figure 45: Type-II saturated stage, p+ switched from high to low

If the additional charge supplied by the charge pumps is minuscule when compared to the total charge swing during a single cycle, the corresponding fine-tuning range is approximately given by

$$\frac{\Delta f}{f_0} = \frac{M I_{inp}}{I_{max}} \quad (94)$$

where Δf is the frequency tuning range around the center frequency f_0 , M is the current-mirror ratio $W(M_{14})/W(M_{17})$ (in Figure 41), I_{inp} is the input current, and I_{max} is the maximum output current swing.

5.3 *Multiple-Pass Ring Design Example*

In the first section of this chapter, the multiple-pass loop architectures were quantitatively analyzed by deriving equations that give the frequency improvement of a particular configuration when compared to a single-loop architecture. After the derivation, we ended up with same equations as given in [23] for subfeedback loops. The analysis given in this work, however, is extended to a general case where ring structures with both even and odd number of stages are considered along with both inverted and non-inverted feedforward connections.

In this section, an example multiple-pass ring-oscillator design with the configuration $(N, x, \text{sign}) = (4, 2, +)$ will be discussed and it will be shown how to apply Equation (81) to an actual case.

5.3.1 Single-Loop Ring-Oscillator

Although a multiple-pass ring-oscillator can be directly designed from scratch, a single-loop structure is needed for comparison. The applicability of Equation (81) can be checked using this comparison. For that purpose, a 4-stage differential single-loop ring-oscillator will be designed with the connection scheme shown in Figure 11. The saturated gain stage that was shown in Figure 39, which is the same as type-I

Table 4: Transistor sizes of 4-stage single-loop ring design in 0.18 μm CMOS

Transistor	Width	Length
M5-M6	18 μm	0.18 μm
M3-M4	1 μm	0.18 μm

saturated stage with the secondary input transistors removed, will be used in this design.

The design starts with selecting the input transistor and the feedback control transistor sizes. Then, the load transistor sizes can be selected according to the desired oscillator characteristics such as the maximum frequency and the power dissipation. The input transistor size will directly effect all the major characteristics of the oscillator and the final load transistor sizes. On the other hand, the feedback control transistor sizes will only have a major effect on the tuning range and the gain of the stages. As a starting point, moderate sizes are selected as shown in Table 4.

After fixing these sizes, various simulations were performed while sweeping the load transistor sizes. Figure 46 shows the change of oscillation frequency with different load transistor sizes while Figure 47 gives the power dissipation at these frequencies. The control voltage was chosen to be 1.2 V in these simulations. The load transistor size is swept up to 20 μm after which point the oscillator ceases oscillation due to inadequate gain.

The simulations demonstrated that the oscillation frequency and power increases as the load size increases. The designs with larger load sizes, however, are more difficult to stabilize and they have a narrower stable operation range in terms of control voltages. This can also be seen using the small signal approximation where the gain of the stage is given by $Gain = g_m(inp)/g_m(load)$ and noting that $g_m(load)$ increases as load sizes increase. Figure 48 illustrates the stable operation range of various designs by providing the frequency-voltage characteristics. Among these possibilities,

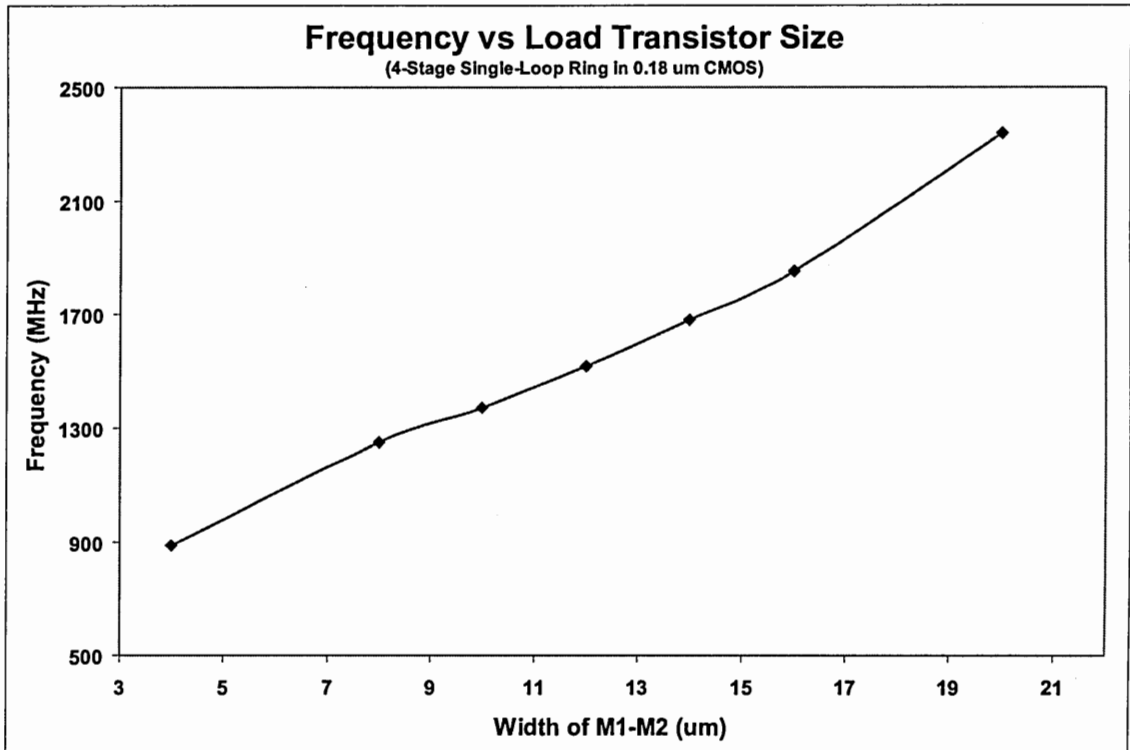


Figure 46: 4-stage single-loop ring oscillator frequency vs load size

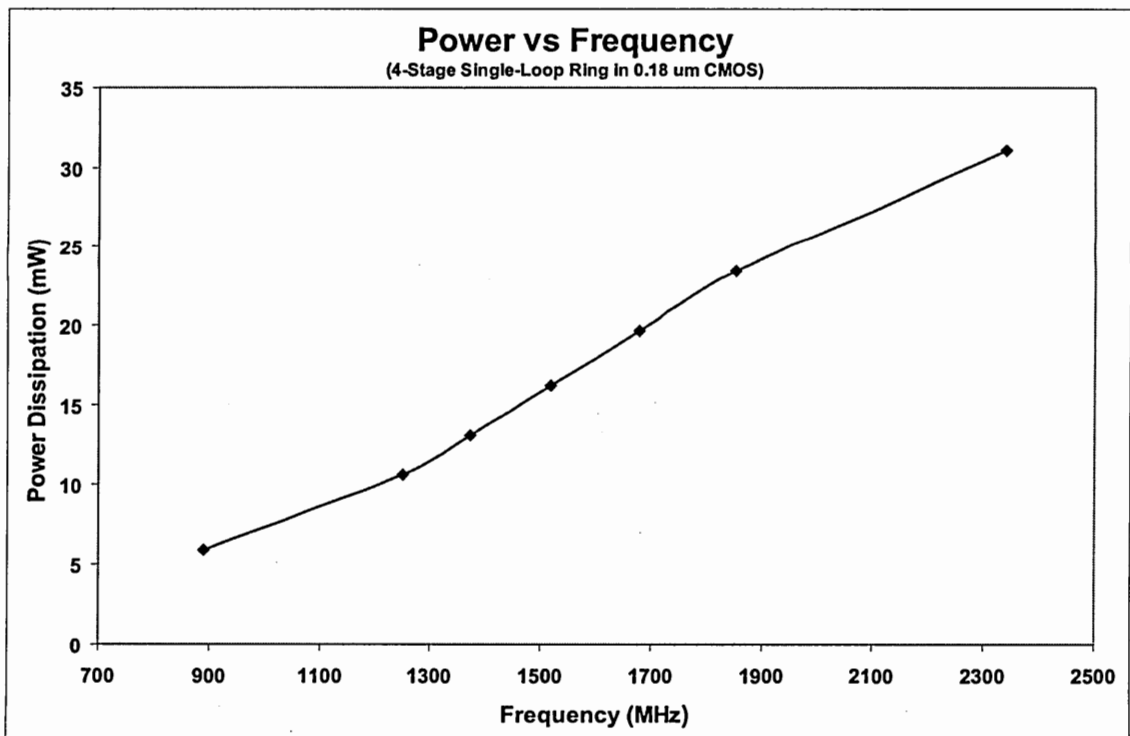


Figure 47: 4-stage single-loop ring oscillator power dissipation vs frequency

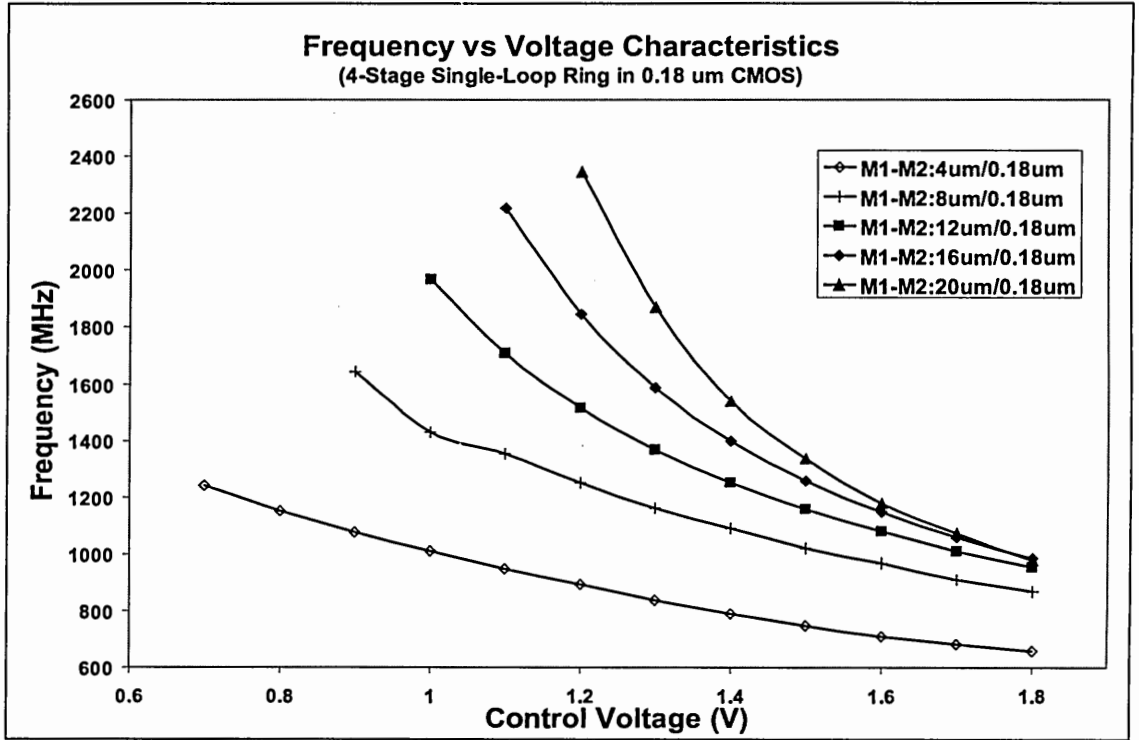


Figure 48: 4-stage single-loop ring oscillator frequency-voltage characteristics for various load sizes

Table 5: Final transistor sizes of 4-stage single-loop ring design in 0.18 μm CMOS

Transistor	Width	Length
M5-M6	18 μm	0.18 μm
M3-M4	1 μm	0.18 μm
M1-M2	16 μm	0.18 μm

the load transistor widths were selected to be 16 μm by comparing the curves in Figure 48 for the maximum frequencies and the stable operation ranges. The final transistor sizes of the single-loop oscillator is given in Table 5

5.3.2 Multiple-Pass Ring-Oscillator

Next, we will see how the characteristics of this design change when we add the feedforward loops for multiple-pass architecture. As implied above, the $(N,x,\text{sign}) = (4,2,+)$ configuration is chosen for the multiple-pass loop implementation along

with the type-I saturated stage. Frequency characteristics of the oscillator is strongly correlated to the sizing of the secondary input transistors, M7 and M8. This is demonstrated in Figure 49, which shows the oscillation frequency when the sizes of M7 and M8 are varied. Figure 50 shows the power dissipation of the oscillator as a function of the secondary input transistor sizes, whereas Figure 51 gives power dissipation vs frequency characteristics. In these simulations, control voltage was again chosen to be 1.2 V as in the single-loop ring oscillator simulations for accurate comparison. These plots show that the output frequency increases almost linearly with the aspect ratios of M7-M8 until the width of M7-M8 reaches 24 μm . After this point, the output frequency saturates and the increase of M7-M8's aspect ratios have little effect on the output frequency. Dissipated power, on the other hand, increases with the aspect ratios of M7-M8 without saturating. From these results we deduce that the practical sizes of M7-M8 are limited to 24 μm for this particular design. Increasing the sizes of M7-M8 above this value helps to slightly increase the output frequency at the expense of greatly increased power consumption.

5.3.3 Frequency Improvement

According to the analysis of multiple-pass loops given in the previous sections, the absolute frequency improvement can be calculated using [23]

$$\frac{\omega'}{\omega} = \frac{RC}{R'C'} + F_{imp}(\tan \theta)^{-1} RG_m \left(\frac{C}{C'} \right) \quad (95)$$

where ω' is the oscillation frequency of the multiple-pass architecture and ω is the oscillation frequency of the single-loop architecture. In [23], authors assumed that the output resistance of a gain stage stays approximately constant after the addition of feedforward loops and, therefore, Equation (95) reduces to

$$\frac{\omega'}{\omega} = \frac{C}{C'} [1 + F_{imp}(\tan \theta)^{-1} RG_m], \quad (96)$$

by the cancellation of the resistance terms.

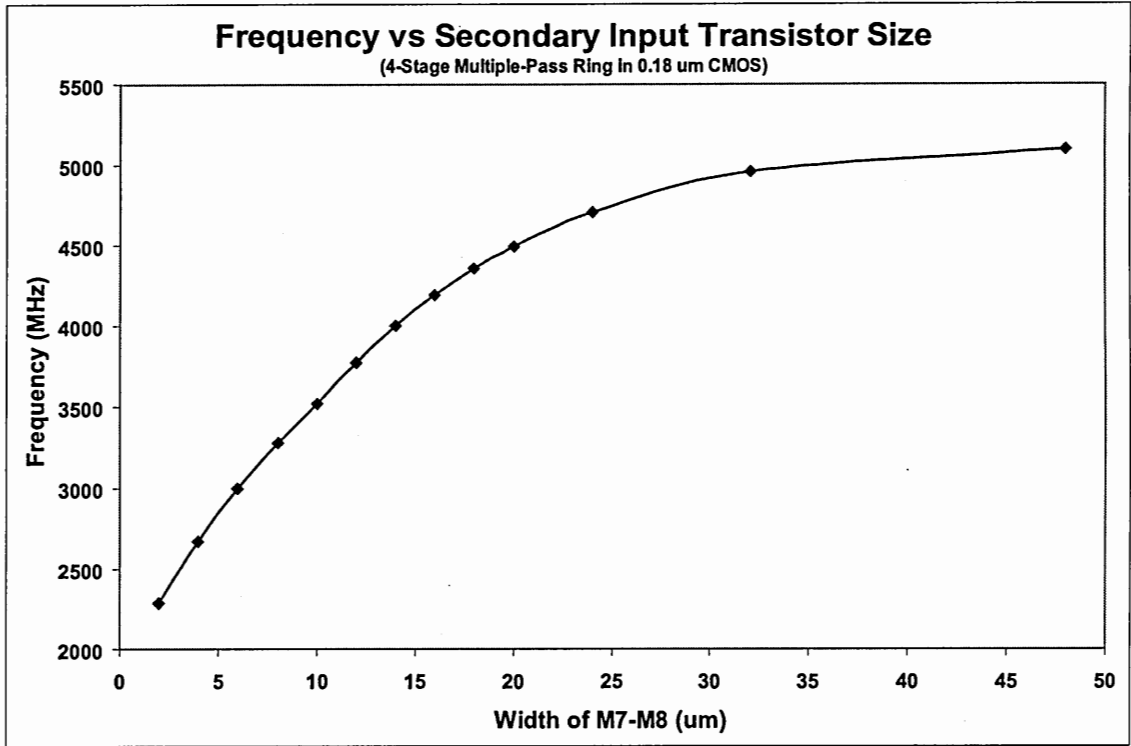


Figure 49: 4-stage multiple-pass ring oscillator frequency for various secondary input transistor sizes

As will be seen shortly, however, if the secondary input transistors have driving strengths comparable to the load transistors, the equivalent output resistance changes significantly by the addition of the feedforward loops. This invalidates the assumption of constant output resistance. This argument can be checked by observing the instantaneous currents flowing through the transistors of a single stage. Figure 52 illustrates the left half of the type-1 saturated stage with drain currents labelled on the transistors. Figure 53, for example, shows the transient drain currents of the transistors for the case where the width of load transistors are $16\ \mu\text{m}$ and that of secondary input transistors are $18\ \mu\text{m}$. Here, the most important time interval for our consideration is the transition period, or the midpoint of the output voltage. This is because the switching characteristics of a gain stage is mostly dependent on the transition interval rather than the saturated, i.e. clipped, regions. This time period is also important because the switching of the next stage is triggered during this

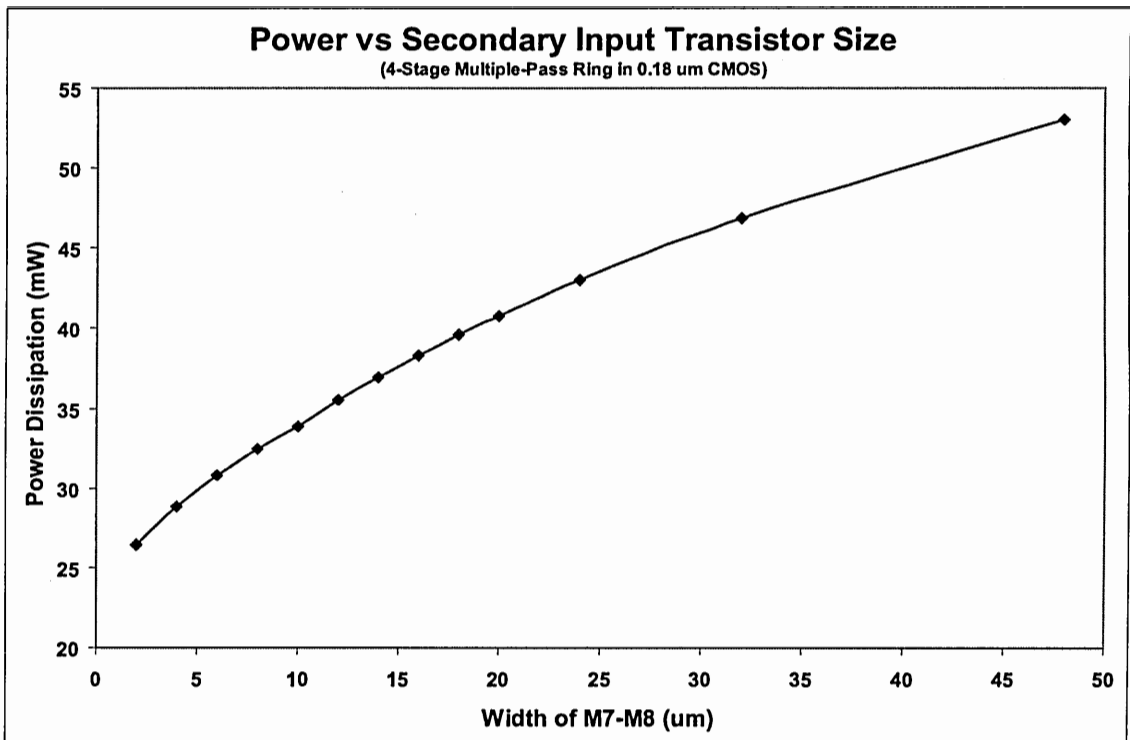


Figure 50: 4-stage multiple-pass ring oscillator power dissipation for various secondary input transistor sizes

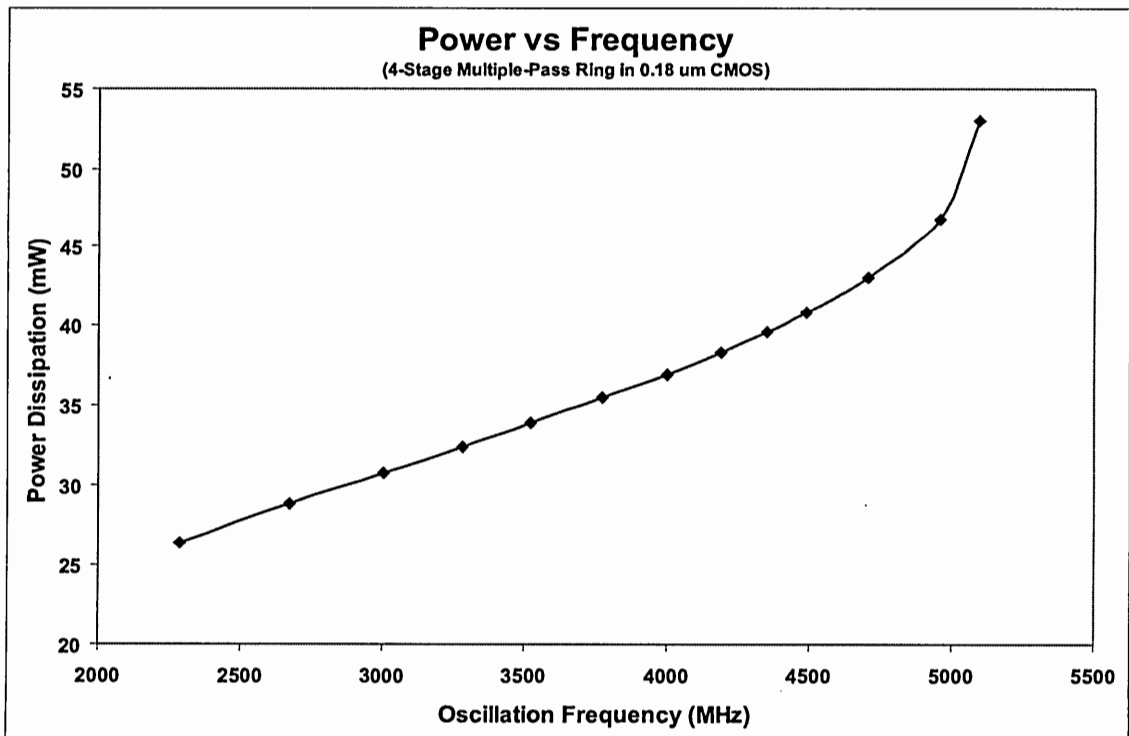


Figure 51: 4-stage multiple-pass ring oscillator power dissipation vs frequency

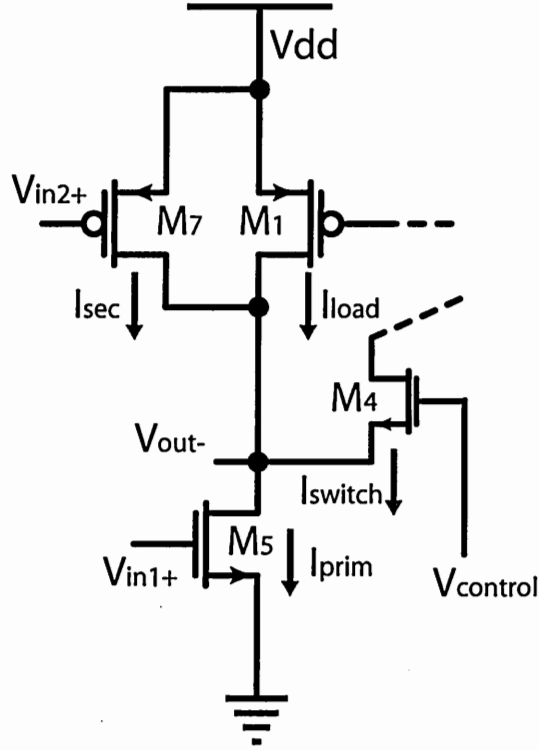


Figure 52: Left half of type-1 saturated stage

interval.

The high-to-low transition of the output voltage is dominantly governed by the current steering capability of the primary input transistors. The low-to-high transition, on the other hand, depends on both the current sourcing capability of the load transistors and the secondary input transistors. As demonstrated in Figure 53, the secondary input transistor dominates the total charging current in the low-to-high transition interval. The equivalent output resistance in this region, therefore, significantly shifts from its original value. If the secondary input transistors have much smaller driving strengths when compared to the load transistors, the low-to-high transition is dominated by the load transistors corresponding to a minor variation in the equivalent output resistance. In this case, Equation (96) can be used with small errors. Figure 54 shows the transient drain currents of the transistors for the case where the width of load transistors are $16\ \mu\text{m}$ and that of secondary input transistors are $2\ \mu\text{m}$.

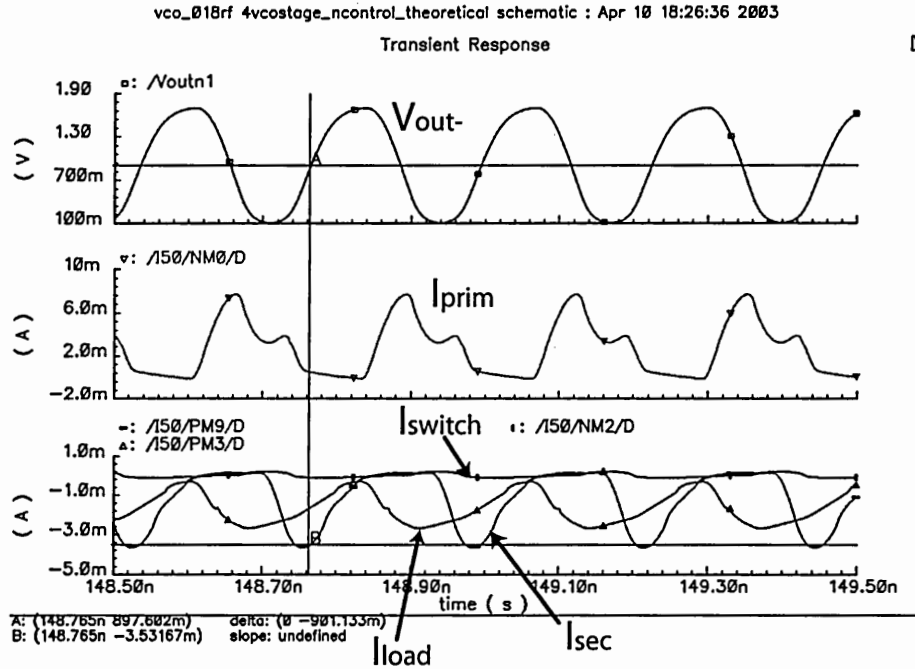


Figure 53: Transient drain currents of the transistors for M1-M2: $16\ \mu\text{m}/0.18\ \mu\text{m}$, M7-M8: $18\ \mu\text{m}/0.18\ \mu\text{m}$

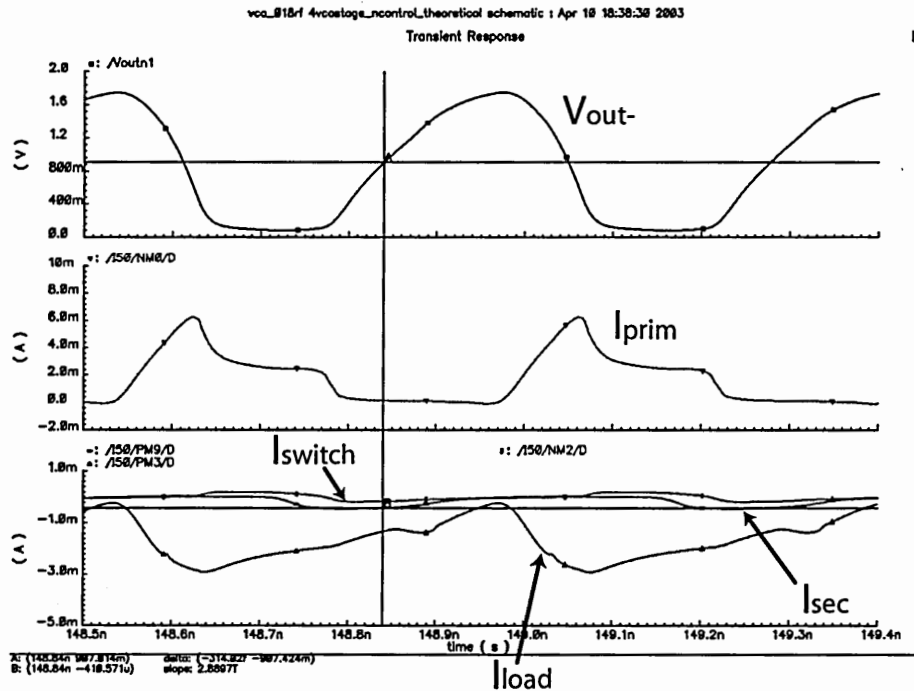


Figure 54: Transient drain currents of the transistors for M1-M2: $16\ \mu\text{m}/0.18\ \mu\text{m}$, M7-M8: $2\ \mu\text{m}/0.18\ \mu\text{m}$

From the above discussion, it is clear that Equation (96) can not be used unless the feedforward transistors are chosen to be much weaker than the cross-coupled transistors in the gain stage. Equation (95), on the other hand, is not straightforward to apply because of the difficulty in extracting the single pole model parameters R , C , R' , and C' .

For a step function excitation, the output response of single-pole inverter model can be written as

$$V_{out} = V_{pp} [1 - e^{-t/RC}], \quad (97)$$

where V_{pp} is the amplitude of the step function, and RC represents the time constant of the inverter. Taking the time derivative of the output signal, we get

$$\frac{d(V_{out})}{dt} = \frac{V_{pp}}{RC} e^{-t/RC}. \quad (98)$$

The value of this function at $t = 0$ gives the maximum slew rate of the output signal, which is

$$\frac{d(V_{out})}{dt}(t = 0) = SR_{max} = \frac{V_{pp}}{RC}. \quad (99)$$

Assuming that the output signal swing does not change significantly by the addition of the multiple-pass loops, we can rewrite Equation (81) as

$$\frac{\omega'}{\omega} = \frac{SR'_{max}}{SR_{max}} + \frac{F_{imp} G_m RC}{\tan \theta C'} \quad (100)$$

by using the maximum slew rates instead of the time constants. Here, SR_{max} represents the maximum slew rate of the output signals for the single-loop architecture, and SR'_{max} represents that of the output signals for the multiple-pass architecture. This can be simplified as

$$\frac{\omega'}{\omega} = \frac{SR'_{max}}{SR_{max}} \left[1 + F_{imp} \frac{G_m R'}{\tan \theta} \right] \quad (101)$$

Because these ring-oscillators are non-linear large signal systems, transconductance and output resistance parameters are not well defined. The previous discussions

stated that the transition region is the most important period that determines the frequency properties of the gain stage. Output resistance values from the transition periods, therefore, will be used in this equation. For a small signal circuit, G_m of a transistor can be calculated using the equation

$$G_m = \sqrt{2K'(W/L)I_D}, \quad (102)$$

where W and L are the physical parameters of the transistor, I_D is the operating point current, and K' is the transconductance parameter. A first order approximation would be using the average current passing through the transistor to find an equivalent average transconductance. Using these, the absolute frequency improvements are calculated using Equation (101) for the multiple-pass ring design discussed in this section. Finally, Figure 55 gives the absolute frequency improvements found using the simulations, the Equation (96), and the Equation (101) that is derived in this section. In the calculations, the equivalent output resistance was evaluated by taking the arithmetical average of the output resistances at the mid-rail point of rising and falling edges. This plot shows that the frequency improvements calculated using Equation (101) are in good agreement with simulations for reasonable transistor sizes. Sun's equation [23], Equation (96), on the other hand, greatly underestimates the frequency improvement because of the constant output resistance assumption.

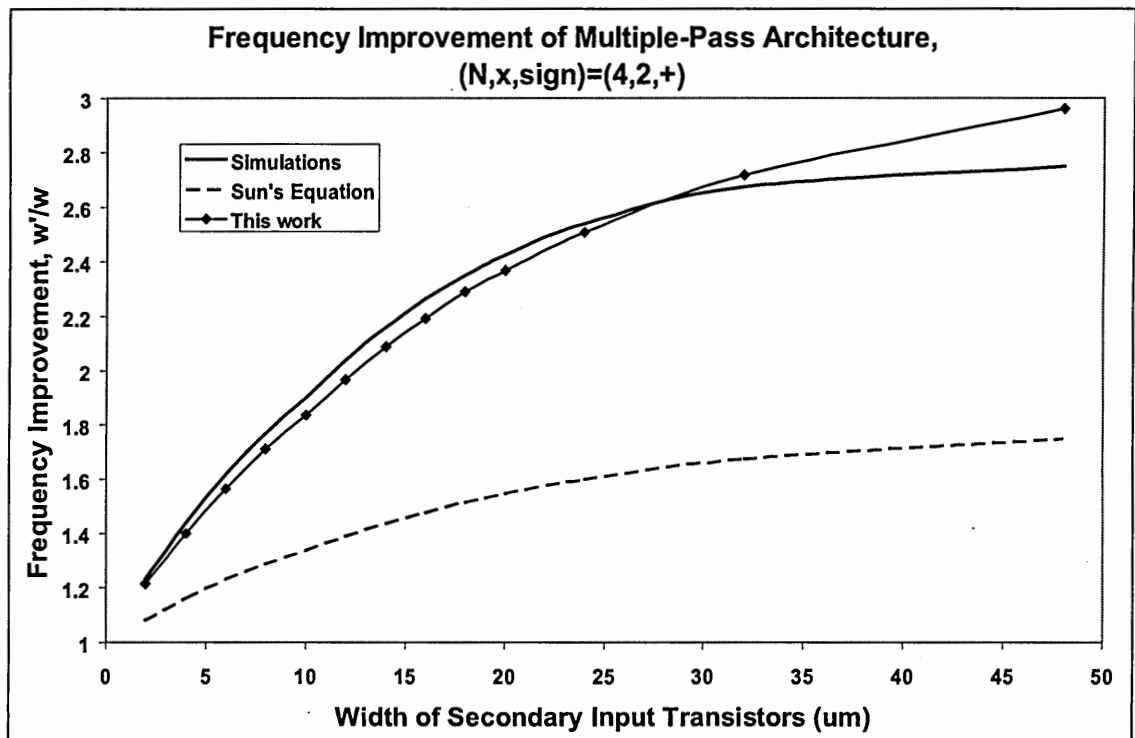


Figure 55: Frequency improvement of multiple-pass architecture, $(N,x,\text{sign})=(4,2,+)$

CHAPTER VI

HIGH PERFORMANCE RING OSCILLATORS

In the previous chapter, design techniques for pushing the frequency and noise performance limits of voltage controlled ring oscillators were described. These include the use of the feedforward loops, which is also cited as multiple-pass or subfeedback loop architectures, to increase the maximum frequency of ring oscillators above the frequencies that can be obtained by regular ring loops. It was also shown how the use of gain stages involving regenerative elements, called saturated stages, may help to enhance the noise performance and sharpen the signal transitions. Moreover, an example design that compares the theoretical analysis with simulation results was provided.

In this work, various ring oscillators were designed using type-I and type-II saturated gain stages along with multiple-pass architectures. By using these techniques, it may become possible to expand the applications of ring VCOs into some areas that previously required the performance of LC oscillators. This section explains the characteristics of these designs in detail.

6.1 Design for Maximum Frequency

The maximum oscillation frequency of a ring oscillator is determined by the minimum delay time through the feedback path. Therefore, there are two basic ways to increase the frequency of a ring oscillator. For a fixed number of stages, the maximum oscillation frequency can be increased by reducing the minimum delay of a single stage. It was already discussed how multiple-pass loop architecture can be used to reduce the effective delay of stages by exciting the output nodes earlier in time using a secondary

set of inputs.

Stage delay can also be reduced by careful sizing of the transistors. Considering the stage model of Figure 31, delay of a stage is inversely dependent on the available current for charging/discharging and is directly dependent on the total output capacitance, i.e. $T_d \propto C_{load}/I_{in}$. Characteristics of a fabrication process impose a limit on the reduction of the minimum delay: because of the high frequency fall-of in transconductances of transistors, switching current may become limited. Reducing the signal swings is one solution to increase the frequency such that the output nodes do not need to be charged/discharged all the way up/down to the rails. However, noise performance is compromised if lower voltage swings are used [31]. Output capacitance of a ring oscillator stage is composed of three elements: parasitic capacitance of the output transistors, input capacitance of the next stage, and other parasitic capacitances including the line parasitics and the buffer input capacitances. First two elements can be reduced by reducing the sizes of transistors in a gain stage but this also reduces the available current for switching. Therefore, ideally, sizing should not affect the frequency performance. Because of the nonlinearity of these dependencies, however, maximum frequency actually tends to improve when transistors with larger aspect ratios are used. This also helps to reduce the effect of the last capacitance element on the delay of the stage: input capacitances of buffers and parasitic line capacitances are more or less independent of the sizing of the delay stage, which means that more current increases the charging pace without any tradeoffs. The actual tradeoff in transistor sizing is the power consumption and the increase of layout area that should be kept within acceptable limits.

The second way to increase the oscillation frequency is decreasing the number of stages. Although ring designs with as few as two stages were reported in literature [15–17], only two output phases can be extracted from these oscillators restricting their usage in some systems; in addition, the two-stage network can be difficult to

Table 6: Characteristics of fabrication technologies used in this work

Technology	Minimum Length	Transistor f_t	Power Supply
0.25 μm CMOS	0.24 μm	27.65 GHz	2.5 V
0.18 μm CMOS	0.18 μm	42.51 GHz	1.8 V
0.13 μm CMOS	0.13 μm	60 GHz	1.2 V

Table 7: Transistor sizes of a 3-stage ring design in 0.25 μm CMOS with $f_{max} = 5.3GHz$

Transistor	Width	Length
M1-M2	8 * 5 μm	0.24 μm
M3-M4	2 * 0.6 μm	0.24 μm
M5-M6	16 * 3.5 μm	0.24 μm
M7-M8	8 * 3 μm	0.24 μm

stabilize under all operating conditions. Like most practical ring designs, multiple-pass loop architecture needs a main loop with at least three stages to sustain stable oscillations. As shown in Table 2, the frequency performance of a ring oscillator with three stages can be improved by using the multiple-pass architecture with x parameter chosen as two and with non-inverted feedforward connections.

6.1.1 Three-stage Ring Oscillators

To explore the maximum frequency performance of proposed designs, which employ multiple-pass architectures along with saturated gain stages, several ring oscillators using the type-I stage with the configuration $(N, x, sign) = (3, 2, +)$ were designed in various state-of-the-art fabrication technologies. Characteristics of these technologies are given in Table 6.

The three-stage ring oscillators that were designed in 0.25 μm CMOS performed well up to frequencies of 5.3 GHz. A particular design, with the transistor sizes given in Table 7, has a linear operation range of 4.15-5.3 GHz when control voltages are varied between 0.9-2.5 V. This corresponds to a tuning range of 24.3% and a gain of

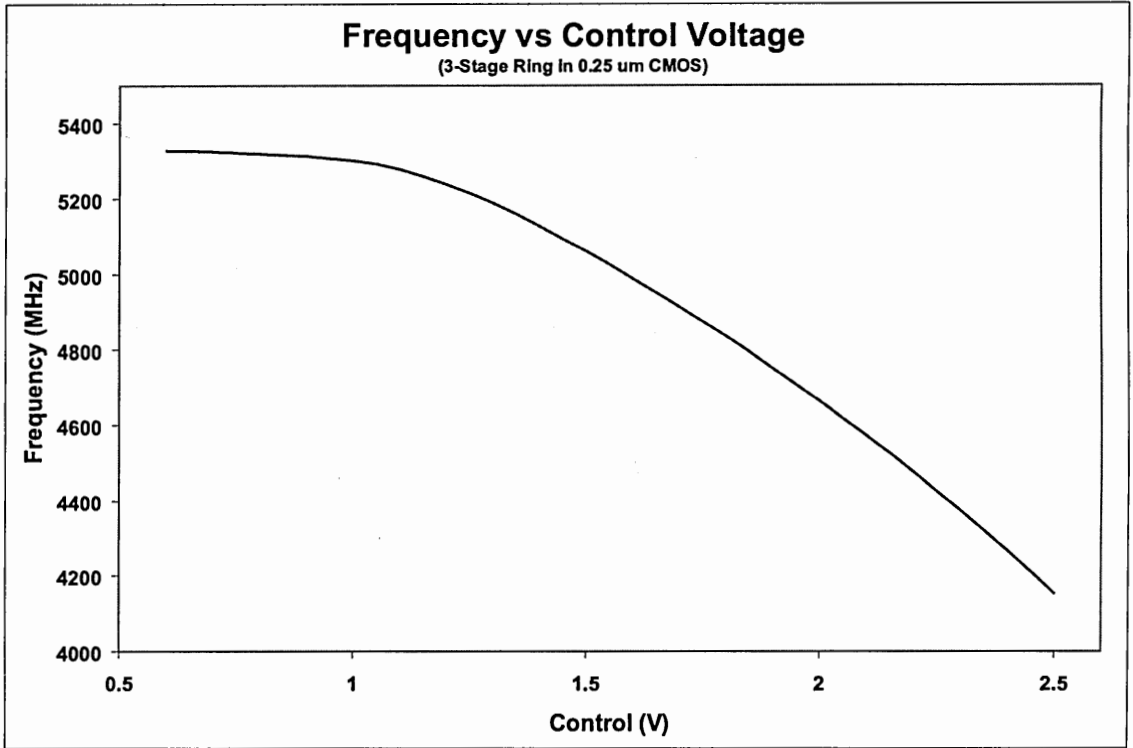


Figure 56: Frequency vs control voltage characteristics of the 3-stage ring VCO in $0.25\ \mu\text{m}$ CMOS

0.72 GHz/V. The frequency-voltage characteristics of this design is shown in Figure 56. The differential output voltage swing is between 3.16-3.33 V peak-to-peak, and the power dissipation is between 98-121 mW. The power dissipation throughout the control range is given in Figure 57.

By switching to $0.18\ \mu\text{m}$ CMOS, maximum frequency of the three-stage ring designs is increased to 9.5 GHz. Table 8 provides the transistor sizes of a design that has a linear operation range of 8.1 GHz to 9.5 GHz when control voltages are varied between 0.7-1.8 V. This corresponds to a tuning range of 16% and a gain of 1.27 GHz/V. The frequency-voltage characteristics of this design is demonstrated in Figure 58. The differential output voltage swing is between 2.2 V and 2.6 V peak-to-peak, and the power dissipation is between 63 mW and 82 mW within the desired operation range. The power dissipation throughout the control range is given in Figure 59.

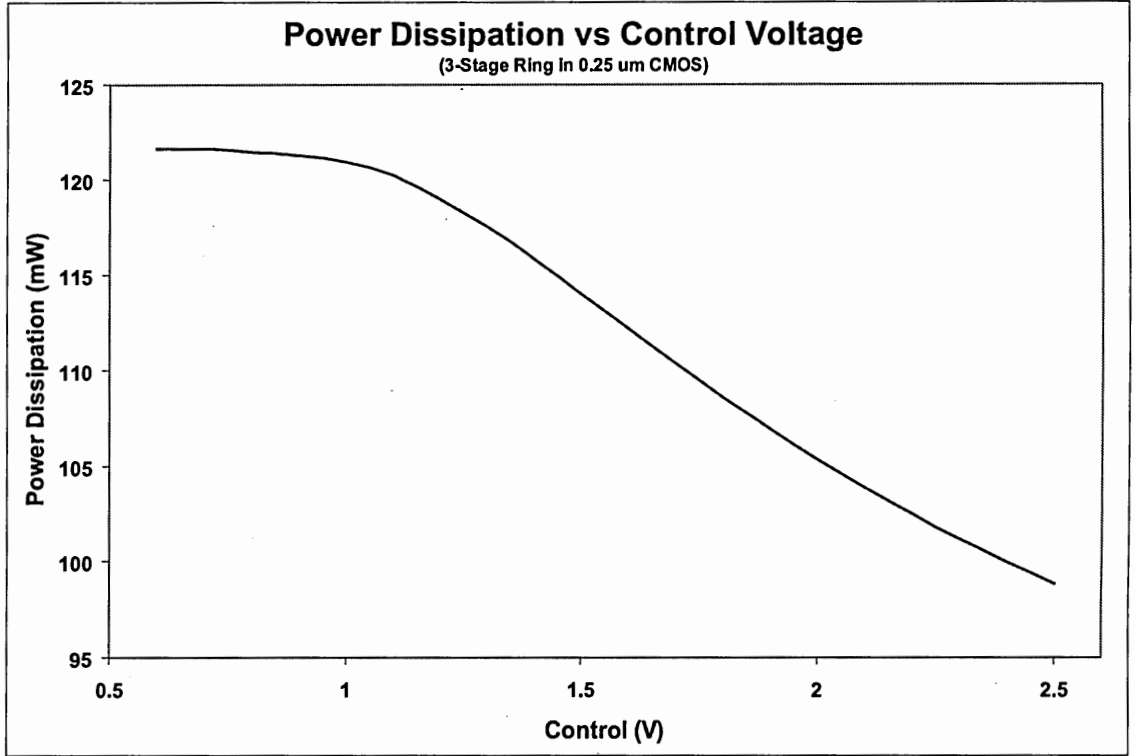


Figure 57: Power dissipation vs control voltage characteristics of the 3-stage ring VCO in 0.25 μm CMOS

Table 8: Transistor sizes of a 3-stage ring design in 0.18 μm CMOS with $f_{max} = 9.5\text{GHz}$

Transistor	Width	Length
M1-M2	8 * 5 μm	0.18 μm
M3-M4	2 * 0.5 μm	0.18 μm
M5-M6	16 * 3.38 μm	0.18 μm
M7-M8	8 * 3.25 μm	0.18 μm

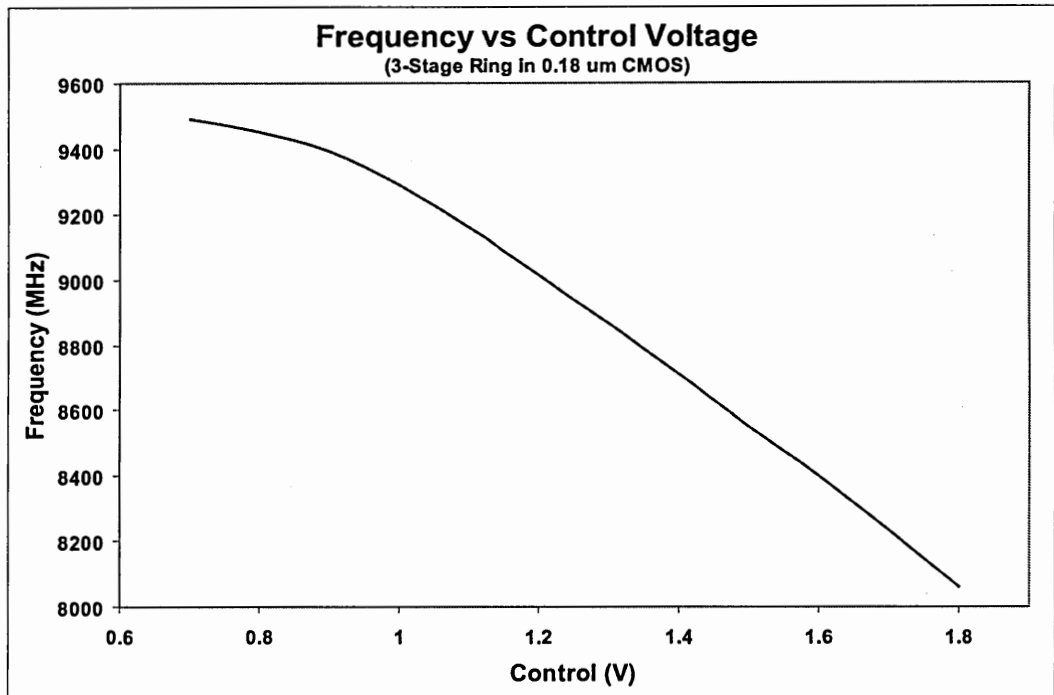


Figure 58: Frequency vs control voltage characteristics of the 3-stage ring VCO in 0.18 μm CMOS

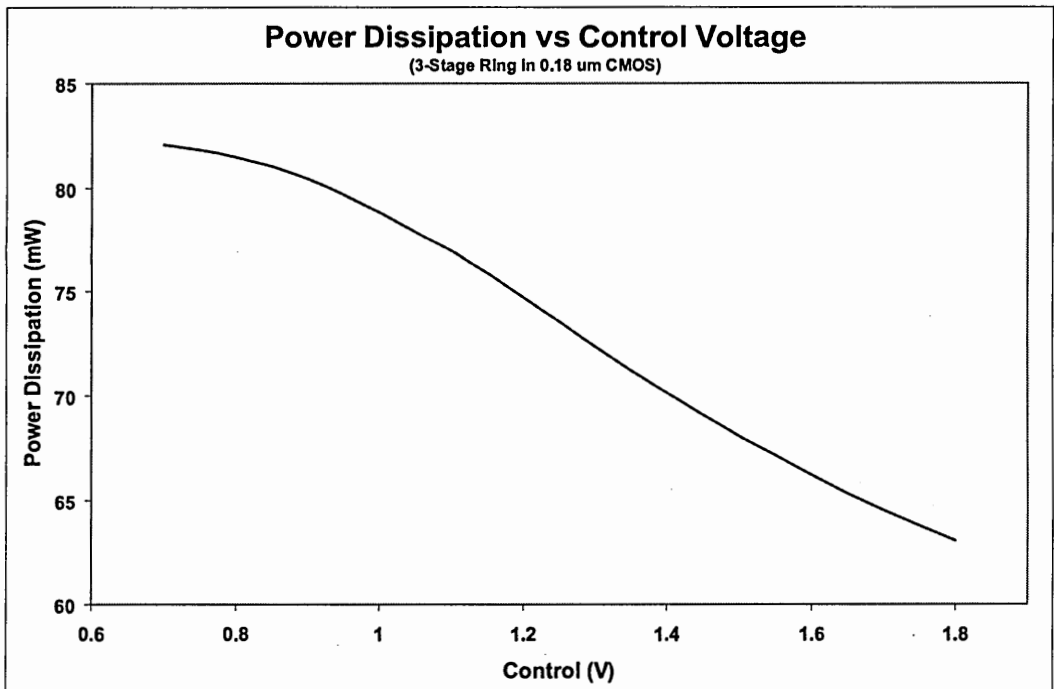


Figure 59: Power dissipation vs control voltage characteristics of the 3-stage ring VCO in 0.18 μm CMOS

Table 9: Transistor sizes of a 3-stage ring design in 0.13 μm CMOS with $f_{max} = 14.4GHz$

Transistor	Width	Length
M1-M2	12 * 3.5 μm	0.13 μm
M3-M4	1 * 0.5 μm	0.13 μm
M5-M6	12 * 4.5 μm	0.13 μm
M7-M8	8 * 2 μm	0.13 μm

Despite the reduction of the power supply voltage to 1.2 V, which does not leave sufficient headroom for voltage swings considering that $(V_{Tn} + V_{Tp})$ is close to this value, maximum frequency is increased to more than 14 GHz in 0.13 μm CMOS technology. Table 9 gives the transistor sizes of a design that has an operation range of 8.75-14.4 GHz when control voltages are varied between 0.0-1.2 V. This corresponds to a tuning range of 49% and a gain of 4.7 GHz/V. The frequency-voltage characteristics of this design is shown in Figure 60. The differential output voltage swing is between 1.45-1.7 V peak-to-peak, and the power dissipation is between 31-59 mW within the desired operation range. The power dissipation throughout the control range is given in Figure 61.

Note that the frequency-voltage curves of the 3-stage oscillators designed in 0.13 μm , 0.18 μm , and 0.25 μm CMOS technologies experience different characteristics when control voltages drop below 0.5 V for the 0.13 μm CMOS, and 0.7 V for the 0.18 μm CMOS and the 0.25 μm CMOS processes. That is, the gain of the VCO increases for the 0.13 μm CMOS technology, and the frequency starts saturating with the decreasing control voltages for the other technologies. This is accounted to the transistors entering into the subthreshold regions giving different responses in different technologies.

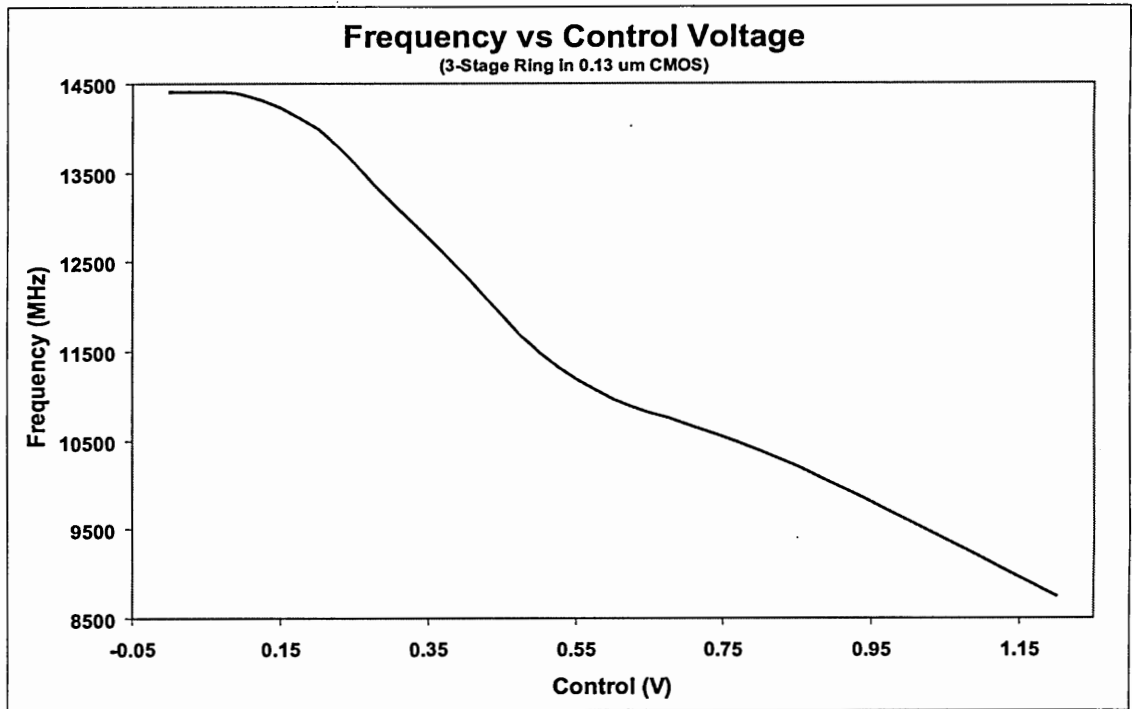


Figure 60: Frequency vs control voltage characteristics of the 3-stage ring VCO in 0.13 μm CMOS

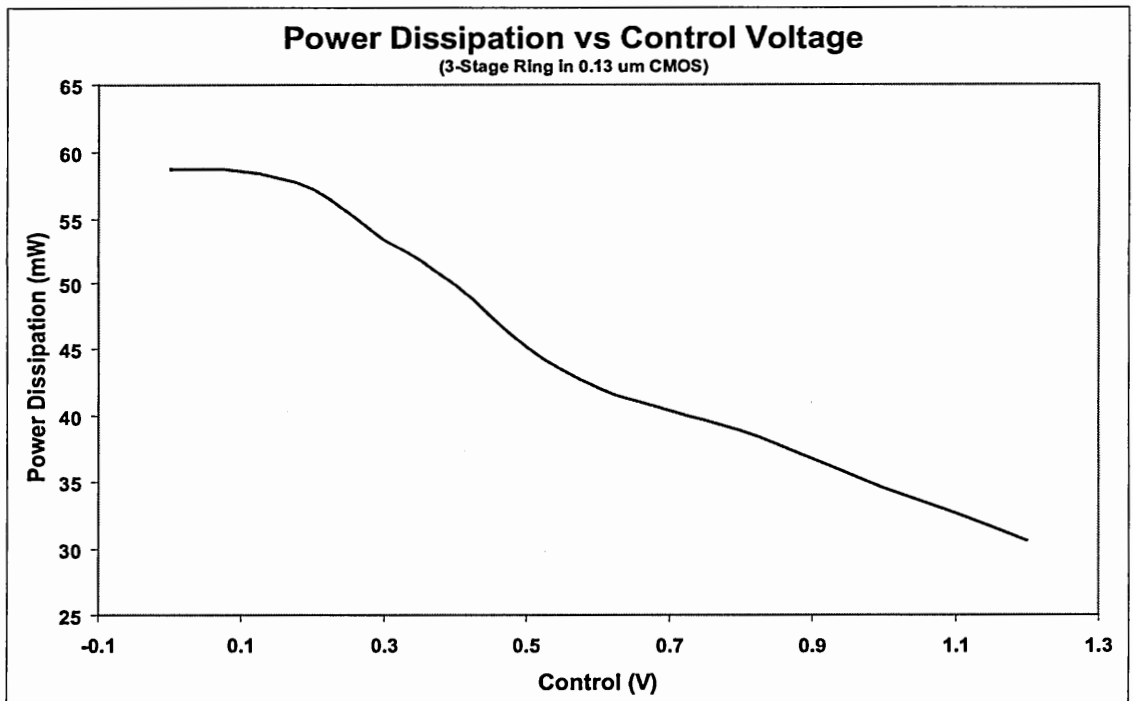


Figure 61: Power dissipation vs control voltage characteristics of the 3-stage ring VCO in 0.13 μm CMOS

6.2 Phase Noise Calculation & Simulation

Phase noise is another important consideration for voltage controlled oscillators. The factors that contribute to the phase noise of an oscillator can be classified into two categories. Thermal noise of transistors and resistors as well as flicker noise ($1/f$ noise) contribute to the random part of the phase noise. This part of phase noise can be reduced to some degree by using low-noise circuit design techniques but the effect of device noise is fundamental and can not be completely removed. Second part of the phase noise originates from systematic factors that can ideally be avoided by a careful design of the system. These factors include cross-talk, power supply/ground fluctuations, and device mismatches. Although there are some approximate methods available that predict the systematic noise by making estimations about the power supply/ground fluctuation levels and/or coupling of circuits, an accurate quantitative analysis is not available due to the lack of noise statistics. Random noise of voltage controlled oscillators, on the other hand, can be simulated using tools such as Spectre RF or can be calculated using various methods from literature as discussed in the previous chapters. Both of these methods, simulations and calculations, have their advantages and disadvantages. For example, calculation of the phase noise may not be trivial if complex gain stages and architectures are involved; whereas simulation tools are usually designed for LC oscillators and ring oscillator noise simulations may be hard to converge if not impossible, and the results might be inaccurate. Therefore, it is better to use both techniques and consider both results when evaluating the noise performance.

6.2.1 Phase Noise Calculations

Ring oscillators with saturated stages have nonlinear characteristics, and they cannot be analyzed by using the linear circuit theory. The noise should be modelled as a cyclostationary random process in a saturated cell because of the periodical switching of

the transistors. As discussed in Chapter IV, various techniques have been published in the literature [6, 8, 31, 32] for the estimation of the phase noise of a ring oscillator. Among these, Leeson's model [31] assumes an LC tank, therefore it is not directly applicable to ring oscillators. Razavi [8], on the other hand, defines an effective Q factor for ring and relaxation oscillators, which extends the Leeson's model to these type of oscillators. However, it does not handle the noise calculation of nonlinear stages well, such as in this case where saturated stages are employed. Hajimiri's model [32], which introduces the impulse sensitivity function (ISF), is more precise considering the effects of nonlinearity, time-variance and cyclostationary noise. Practically, however, application is quite cumbersome requiring many high precision simulations to be performed to characterize the noise. Harjani's phase noise calculation method [6], on the other hand, which is an extension of Hajimiri's model for ring oscillators, simplifies the computation of single-sideband phase noise of nonlinear ring oscillators and thus chosen for this work. Harjani's model, however, is only provided for three-stage oscillators. In this work, this model is modified by using effective Q definition of Razavi and derivation of Harjani leading to the following formulation

$$L(\Delta\omega) = \begin{cases} \frac{16FkTR}{NV_{pp}^2 \sin^2(\frac{\pi}{N})} (\frac{\omega_0}{\Delta\omega})^2 & (for V_{pp} \ll V_{dd}) \\ \frac{128FkTRV_{dd}}{3\pi N \sin^2(\frac{\pi}{N}) V_{pp}^3} (\frac{\omega_0}{\Delta\omega})^2 & (for V_{pp} \gg V_{dd}) \end{cases} \quad (103)$$

that gives the single-sideband phase noise of an N-stage ring oscillator.

Using this equation, phase noise of the 3-stage ring oscillators that were discussed in the previous section are calculated as shown in Table 10.

Equation (59) tells that phase noise of an oscillator is dominantly dependent upon the shape of the output signal. That is, sharper signal edges result in better phase noise characteristics. This leads to the conclusion that an ideal ring oscillator has a perfect square shaped output signal. For actual circuits, however, this is not possible due to slew rate limitations that slow down the transitions. For oscillators with higher frequencies, this limitation may dominate the signal transitions changing the

Table 10: Calculation of phase noise for the 3-stage oscillators in various technologies

Number of Stages	3	3	3
Technology, TSMC CMOS	0.25 μm	0.18 μm	0.13 μm
V_{dd}	2.5	1.8	1.2
Temperature (Celcius)	300	300	300
Excessive Noise Factor, F	4	4	4
Control Voltage (V)	1.5	1.2	0.6
f_0 (MHz)	5070	9046	10970
Output Swing (V)	1.65	1.23	0.84
Maximum Slew Rate (GV/sec)	31.30	38.3	28.65
V_{pp} (V)	1.74	1.35	0.84
R (Ω)	54.57	61.56	43.9
Δf (MHz)	1	1	1
Phase Noise (-dBc/Hz)	102.64	94.90	90.54

signal shapes to sinusoidal instead of a square wave. For the 3-stage ring oscillators that are discussed in this work, this is actually the case. A 3-stage multiple-pass structure oscillates with large output amplitudes at frequencies more than $1/5$ of the transistor f_t 's pushing the limitations of the processes. The sinusoidal shape of the output signals can be seen in Figures 62, 63, and 64; where Figures 62, 63, and 64 demonstrate the single-ended and differential output signals of the 3-stage ring designs in 0.25 μm CMOS, 0.18 μm CMOS, and 0.13 μm CMOS technologies respectively. This can also be checked using Table 10, where the calculated V_{pp} is approximately equal to the output voltage swing showing that there is no major clipping.

From the above discussion, it is clear that for ring oscillator designs with better noise performance, V_{pp} values that are larger than the power supply voltage are needed. This is the second condition in Equation (59) leading to a reduction in phase noise. In the next section, it will be demonstrated how 4-stage ring oscillators provide better noise performance in the expense of maximum frequency and power.

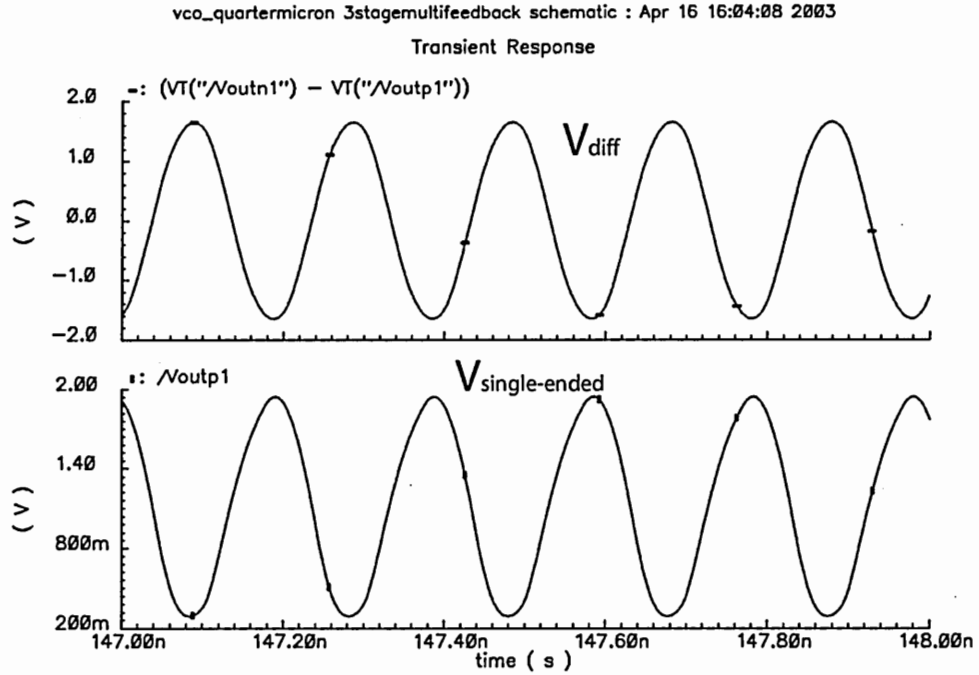


Figure 62: Single-ended and differential output signals of the 3-stage ring in 0.25 μm CMOS

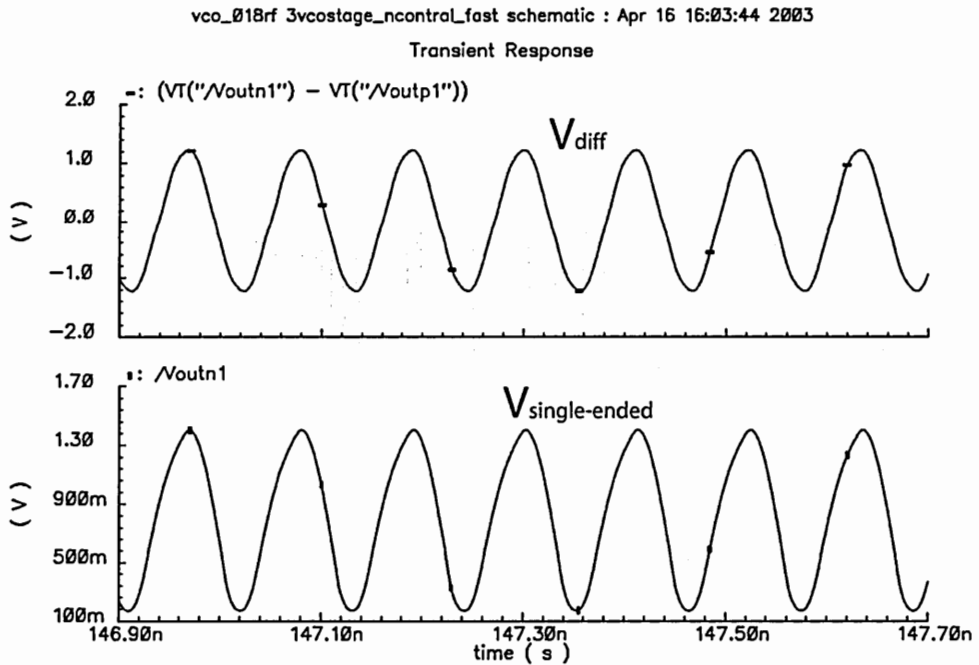


Figure 63: Single-ended and differential output signals of the 3-stage ring in 0.18 μm CMOS

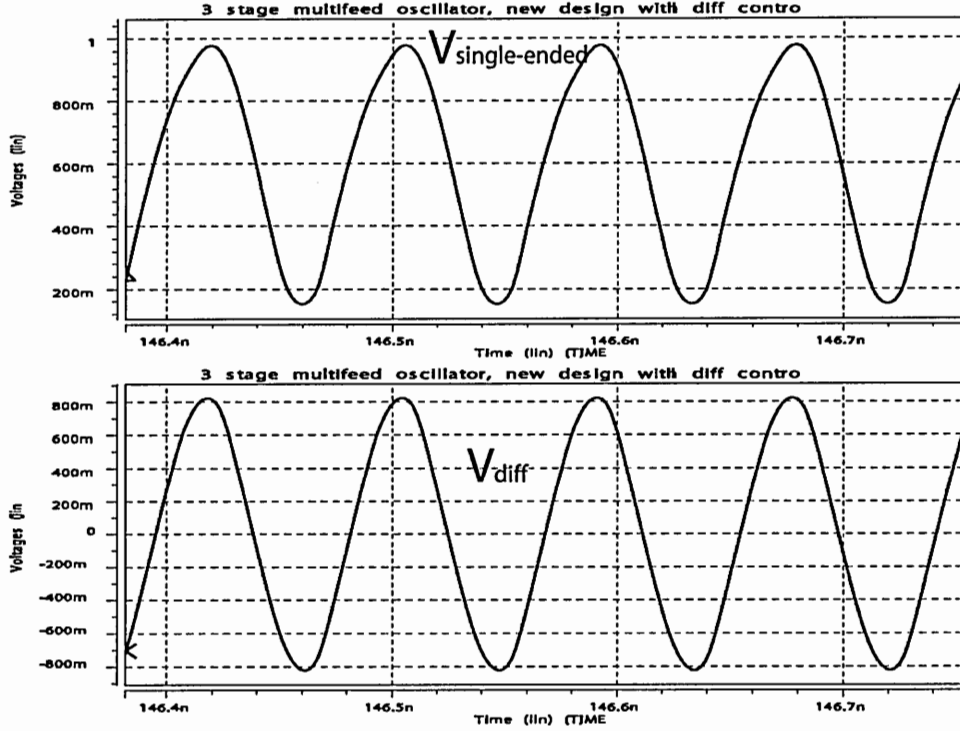


Figure 64: Single-ended and differential output signals of the 3-stage ring in 0.13 μm CMOS

6.2.2 Phase Noise Simulations

For phase noise simulations, periodic steady state analysis (PSS) function of Spectre RF simulation tool was used for the 0.25 μm and 0.18 μm designs. Spectre models were not available for 0.13 μm CMOS. PSS calculates the steady-state response of a circuit, which should have a periodic operation, at a specified fundamental frequency. Shooting method is used for this computation. This method computes the steady-state result using a time-domain, iterative method by finding the initial condition that leads to a steady state response [36]. Phase noise and other desired analysis types can be performed after PSS is done on the circuit. Spectre RF is capable of performing the phase noise calculation including both the thermal and the flicker noise sources. Harjani's model [6], however, takes only the thermal noise into account as implied before. For better comparison, noise simulations were, therefore, performed after removing the flicker noise components from 0.18 μm transistor models. The available

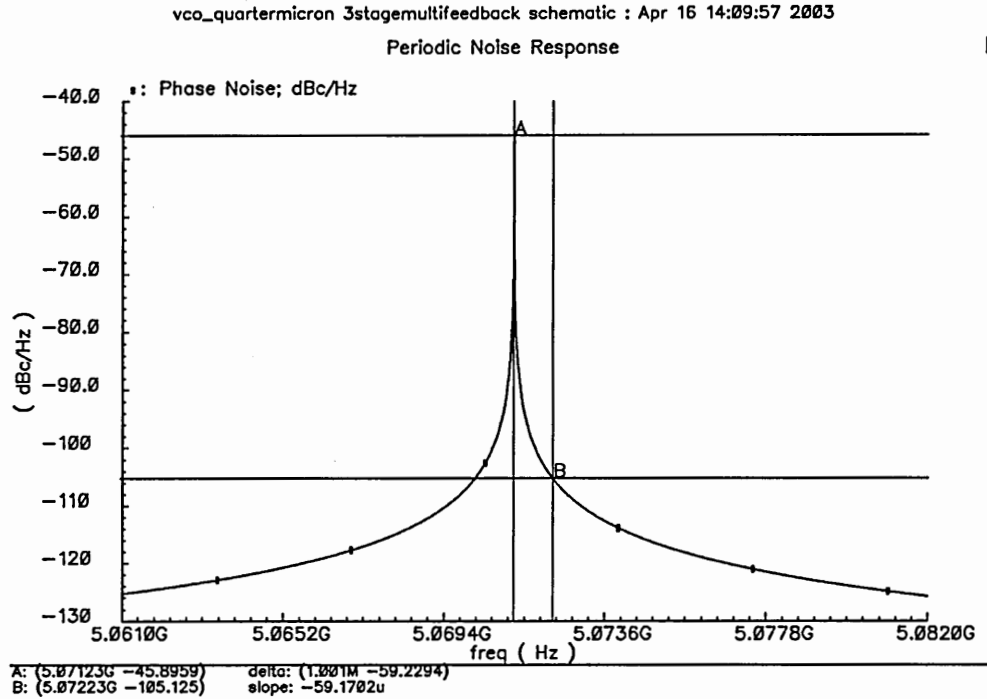


Figure 65: Phase noise simulation of the 3-stage ring in $0.25 \mu\text{m}$ CMOS

$0.25 \mu\text{m}$ CMOS models did not have low-frequency-noise components. Figures 65 and 66 show the phase noise simulation results for the 3-stage oscillators designed in $0.25 \mu\text{m}$ CMOS and $0.18 \mu\text{m}$ CMOS, with the transistor sizes given in Tables 7 and 8. As labelled on the figures, phase noise of the $0.25 \mu\text{m}$ ring oscillator is -105.20 dBc/Hz at a 1 MHz offset from a 5.071 GHz center frequency, and that of the $0.18 \mu\text{m}$ design is -99.2 dBc/Hz at a 1 MHz offset from a 9.047 GHz center frequency. Table 11 shows the phase noise values extracted from simulations at various offset frequencies.

Spectre RF phase noise simulations demonstrated that provided phase noise calculations are overestimating the single-sideband phase noise by 2.6 dB ($0.25 \mu\text{m}$) to 4.3 dB ($0.18 \mu\text{m}$). This discrepancy will be discussed later in this chapter.

Simulation results also showed that phase noise of ring oscillators had a 20 dB/dec drop with offset frequencies, which is apparent from both the phase noise plots and the tabulated values. This is because of the absence of the flicker noise parameters and, therefore, this result was expected. One should anticipate an increase in the phase

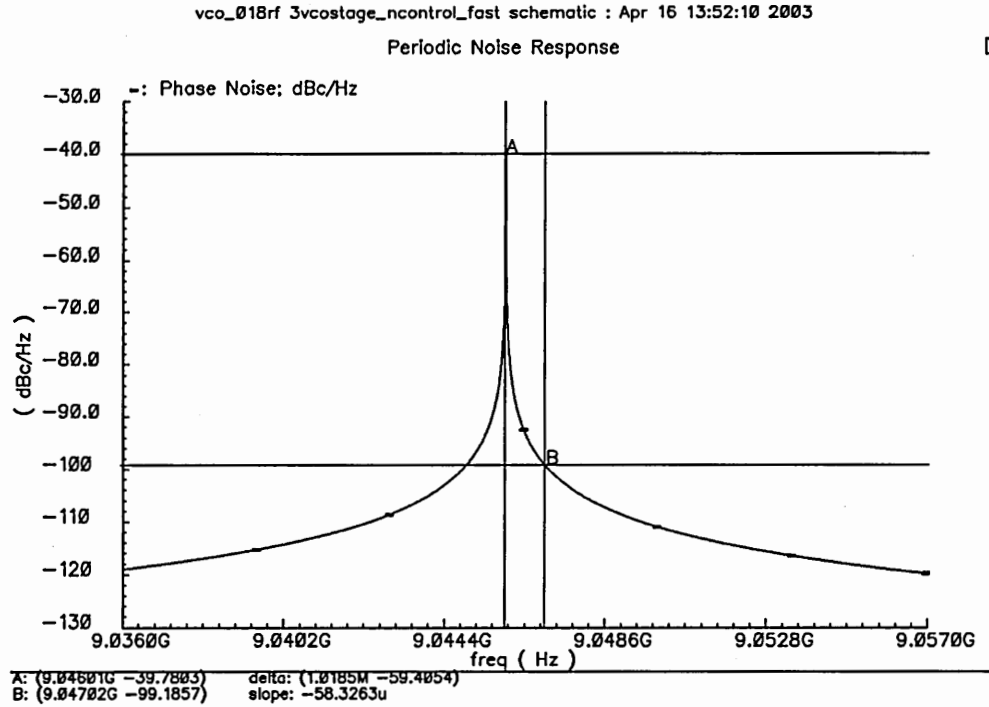


Figure 66: Phase noise simulation of the 3-stage ring in 0.18 μm CMOS

Table 11: Phase noise simulation results for the 3-stage oscillators in 0.25 μm and 0.18 μm CMOS

Number of Stages	3	3
Technology, TSMC CMOS	0.25 μm	0.18 μm
Phase Noise at $\Delta f = 0.6$ MHz (-dBc/Hz)	100.9	94.6
Phase Noise at $\Delta f = 1$ MHz (-dBc/Hz)	105.2	99.2
Phase Noise at $\Delta f = 3$ MHz (-dBc/Hz)	114.7	108.6
Phase Noise at $\Delta f = 5$ MHz (-dBc/Hz)	119.2	112.9
Phase Noise at $\Delta f = 10$ MHz (-dBc/Hz)	125.1	119.0

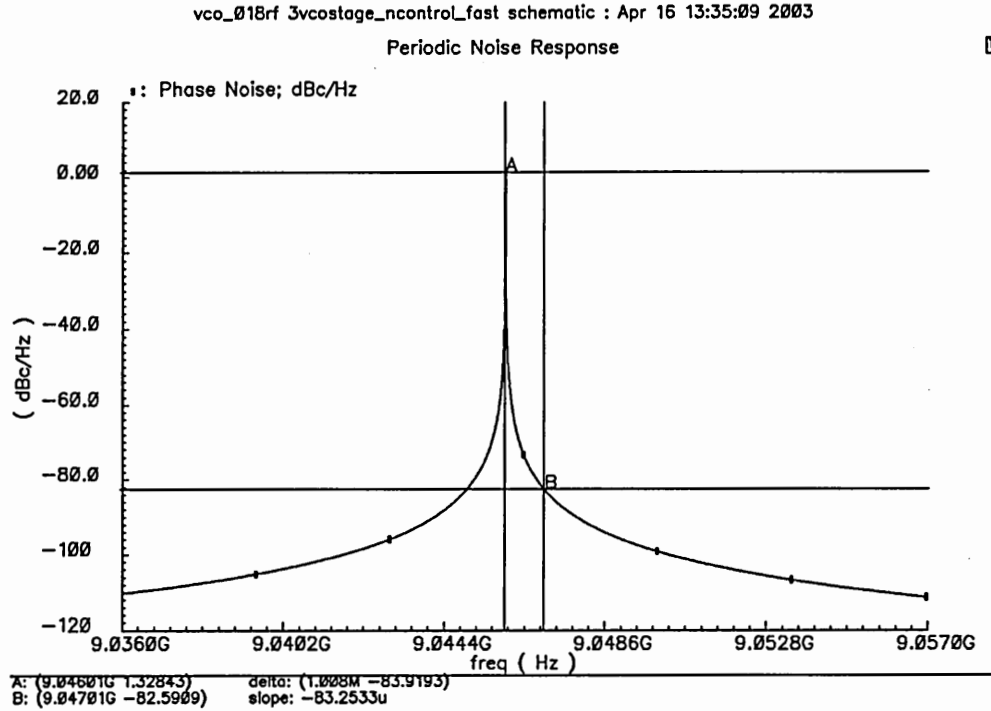


Figure 67: Phase noise simulation of the 3-stage ring in $0.18 \mu\text{m}$ CMOS with flicker noise parameters included in the models

noise at low offset frequencies when these parameters are included in the transistor models. Figure 67 shows the phase noise simulation results of the $0.18 \mu\text{m}$ CMOS three-stage multiple-pass ring oscillator after including the flicker noise parameters. In the given plots, frequency axis is not in logarithmic scale so it is not easy to see the discussed phase noise regions. For that reason, another plot is created by extracting the phase noise data from the simulations, both including and excluding the flicker noise. This data is plotted with respect to a logarithmic frequency axis as illustrated in Figure 68.

In this plot comparing the phase noise power-spectral-density (PSD) with and without including the flicker noise parameters, it can be seen that PSD does not enter into the flat region in the simulated range of 100 MHz. Another important observation is that in the simulations including only the thermal noise, phase noise had a perfect 20 dB/decade drop. In the simulations involving both noise sources,

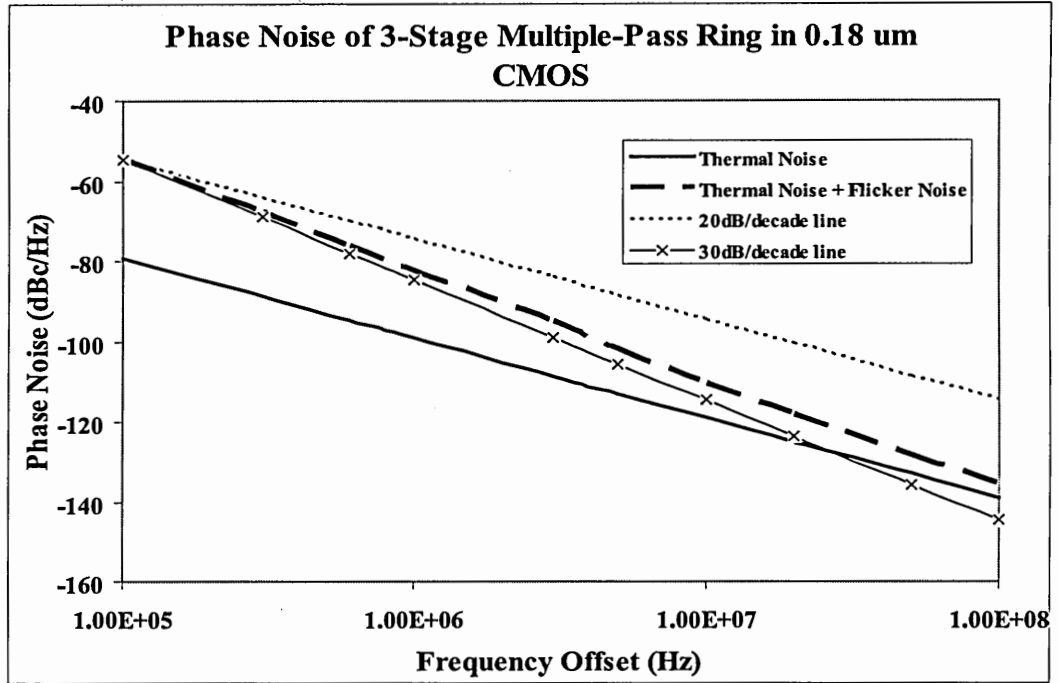


Figure 68: Comparison of the phase noise simulations of the 3-stage ring in 0.18 μm CMOS with and without including the flicker noise

thermal and flicker, however, expected $1/f^2$ and $1/f^3$ regions were not observed and the phase noise had a 27 dB/decade constant drop. For metal-oxide semiconductor (MOS) transistors, the bandwidth of the flicker noise is usually limited to a few hundreds of kHz. This constant 27 dB/decade drop of the phase noise, therefore, is accounted to inaccurate simulation and/or inaccurate modelling of the flicker noise. For this reason, in the following sections, flicker noise will be excluded from the noise simulations.

6.3 Noise & Frequency Tradeoff

In the previous section, it was mentioned that to reduce the phase noise of a ring oscillator, sharper signal transitions are needed. Quantitatively, this can be explained as the increase of V_{pp} values in Harjani's model, Equation (59), that leads to better phase noise values. Referring to Hajimiri's [32] phase noise analysis, this corresponds to the shrinkage of the noise sensitive time interval inside an oscillation period, which

Table 12: Transistor sizes of the 4-stage ring design in 0.25 μm CMOS

Transistor	Width	Length
M1-M2	16 * 3.7 μm	0.24 μm
M3-M4	2 * 0.6 μm	0.24 μm
M5-M6	16 * 3.5 μm	0.24 μm
M7-M8	16 * 2.7 μm	0.24 μm

is the transition edge, corresponding to a reduction in the phase noise. The three-stage designs of the previous section have sinusoidal shaped outputs due to slew rate limitations. This results in signal transition edges take a considerable portion of the period worsening the noise performance. In a particular fabrication technology, designs with lower frequencies, therefore, are expected to have signal transitions that appear sharper. That is, the absolute value of the edge rate may stay approximately same but the transitions will cover a smaller percentage of the period because the period is longer for lower frequencies. This is also shown by the effective Q factor definition given in Equation (60), predicting a reduction in the Q factor of ring oscillators at higher frequencies. Note that the discussed improvement in the noise performance is not because of the $(\omega_0/\Delta\omega)^2$ factor given in the phase noise models, which predicts further improvement in the phase noise values at lower frequencies.

6.3.1 Four-stage Ring Oscillators

In this sense, 4-stage designs offer a good tradeoff between the phase noise and the maximum oscillation frequency. For that reason, 4-stage multiple-pass ring oscillators were designed in 0.25 μm and 0.18 μm CMOS technologies with the transistor sizes given in Tables 12 and 13 respectively. In these designs, type-I stage is used along with the multiple-pass configuration $(N, x, sign) = (4, 2, +)$. The reason of selecting the configuration $(N, x, sign) = (4, 2, +)$ over the configuration $(N, x, sign) = (4, 3, -)$, which provides a higher frequency improvement factor F_{imp} , will be explained in the next section.

Table 13: Transistor sizes of the 4-stage ring design in 0.18 μm CMOS

Transistor	Width	Length
M1-M2	$16 * 4 \mu m$	$0.18 \mu m$
M3-M4	$2 * 0.5 \mu m$	$0.18 \mu m$
M5-M6	$16 * 3.5 \mu m$	$0.18 \mu m$
M7-M8	$16 * 3 \mu m$	$0.18 \mu m$

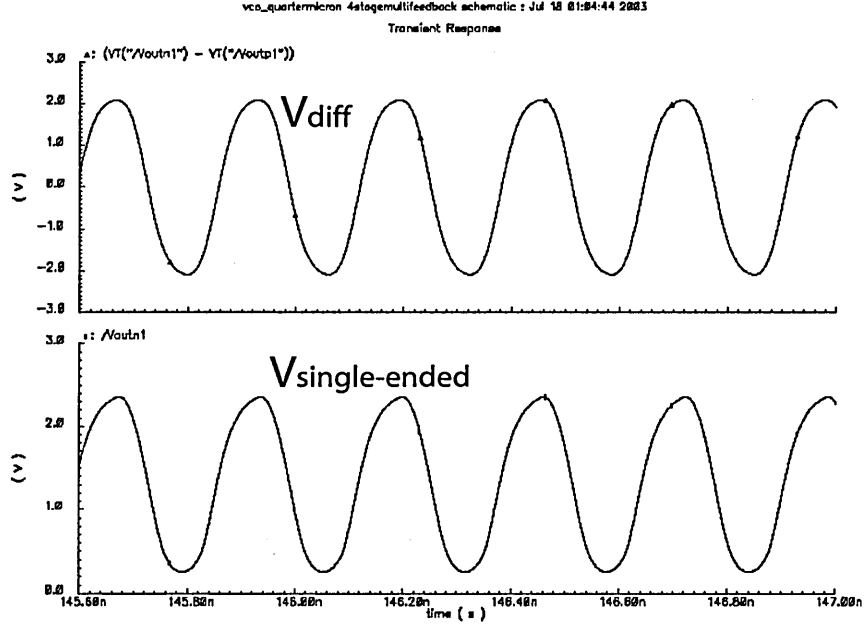


Figure 69: Single-ended and differential output signals of the 4-stage ring in 0.25 μm CMOS

Figures 69 and 70 show the differential and single ended output signals of the 4-stage ring oscillators designed in 0.25 μm CMOS and 0.18 μm CMOS technologies respectively. The waveforms appear to have sharper transitions when compared to the outputs of the 3-stage designs predicting a better noise performance. The improvement in the noise performance can be seen in Table 14, where Table 14 shows the calculation of the phase noise of the 4-stage ring designs using Equation (59).

According to these calculations, phase noise of the 0.25 μm 4-stage ring oscillator is -109.70 dBc/Hz at a 1 MHz offset from a 3.809 GHz center frequency, and that

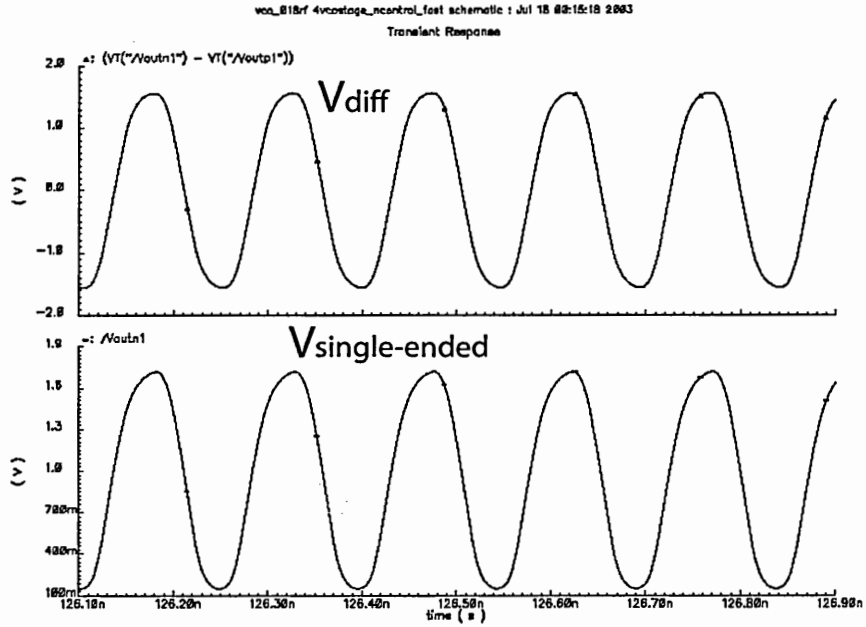


Figure 70: Single-ended and differential output signals of the 4-stage ring in 0.18 μm CMOS

Table 14: Calculation of phase noise for the 4-stage oscillators in various technologies

Number of Stages	4	4
Technology, TSMC CMOS	0.25 μm	0.18 μm
V_{dd}	2.5	1.8
Temperature (Celcius)	300	300
Excessive Noise Factor, F	2	2
Control Voltage (V)	1.5	1.2
f_0 (MHz)	3809	6794
Output Swing (V)	2.08	1.57
Maximum Slew Rate (GV/sec)	33.4	42.60
V_{pp} (V)	2.79	1.98
R (Ω)	57.02	38.34
Δf (MHz)	1	1
Phase Noise ($-dBc/Hz$)	109.70	103.35

of the 0.18 μm design is -103.35 dBc/Hz at a 1 MHz offset from a 6.794 GHz center frequency, demonstrating a 7.06 dB (0.25 μm) to 8.45 dB (0.18 μm) improvement over the 3-stage designs. Phase noise, however, depends upon the center frequency with the relation

$$L(\Delta\omega) \propto \omega_0^2. \quad (104)$$

Therefore, some of this improvement, which is calculated to be 2.48 dB, is accounted to the reduction in the oscillation frequency. Using this, actual noise improvement is found as 4.58 dB in 0.25 μm CMOS, and 5.97 dB in 0.18 μm CMOS. The main source of this improvement is the sharper signal transitions in the four-stage oscillators, resulting in 5.29 dB (0.25 μm) and 4.45 dB (0.18 μm) improvements. Increase of the effective Q factor in four-stage rings, as defined in Razavi's model, also helps to improve the phase noise by 0.73 dB. Four-stage ring oscillators, however, have more number of noise sources, resulting in a 1.25 dB worsening of the phase noise. With the change in the output resistances considered, given calculations account for the noise improvement.

To validate the calculation results, phase noise simulations were again performed using Spectre RF. Figures 71 and 72 provide the phase noise simulation results for the 4-stage oscillators designed in 0.25 μm CMOS and 0.18 μm CMOS, with the transistor sizes given in Tables 7 and 8 respectively. As labelled on the figures, phase noise of the 0.25 μm ring oscillator is -111.46 dBc/Hz at a 1 MHz offset from a 3.810 GHz center frequency, and that of the 0.18 μm design is -105.31 dBc/Hz at a 1 MHz offset from a 6.803 GHz center frequency. The simulated phase noise values are 1.8 dB (0.25 μm) to 2 dB (0.18 μm) smaller than the calculated values.

Other than the increase in the noise performance and the reduction in the maximum frequency, 4-stage oscillators have some other characteristics that need to be considered. First of all, naturally, they provide an increased amount of phases at

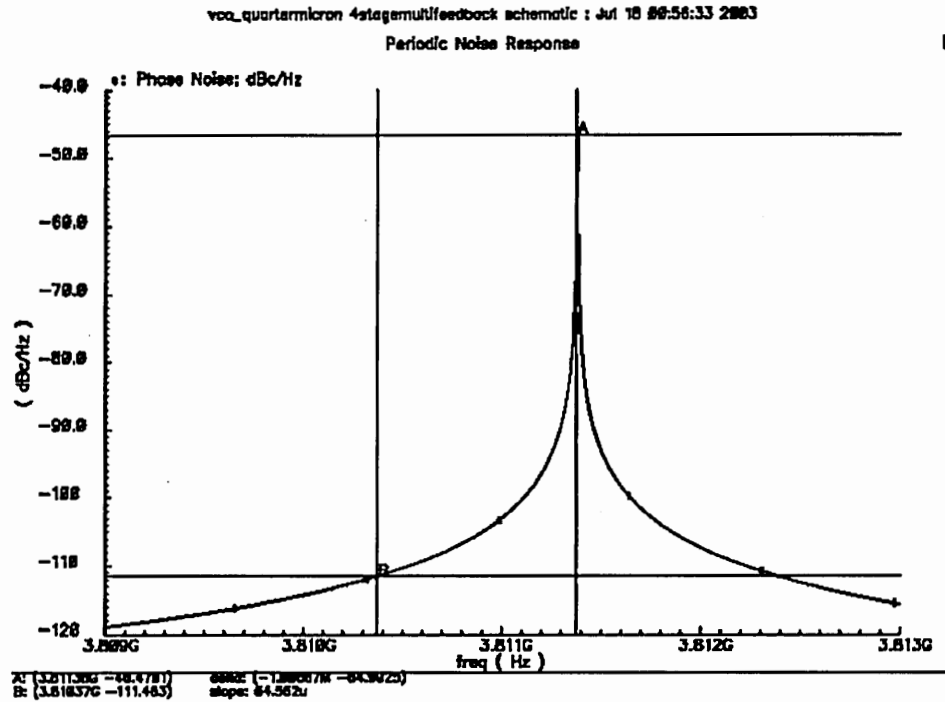


Figure 71: Phase noise simulation of the 4-stage ring in $0.25 \mu\text{m}$ CMOS

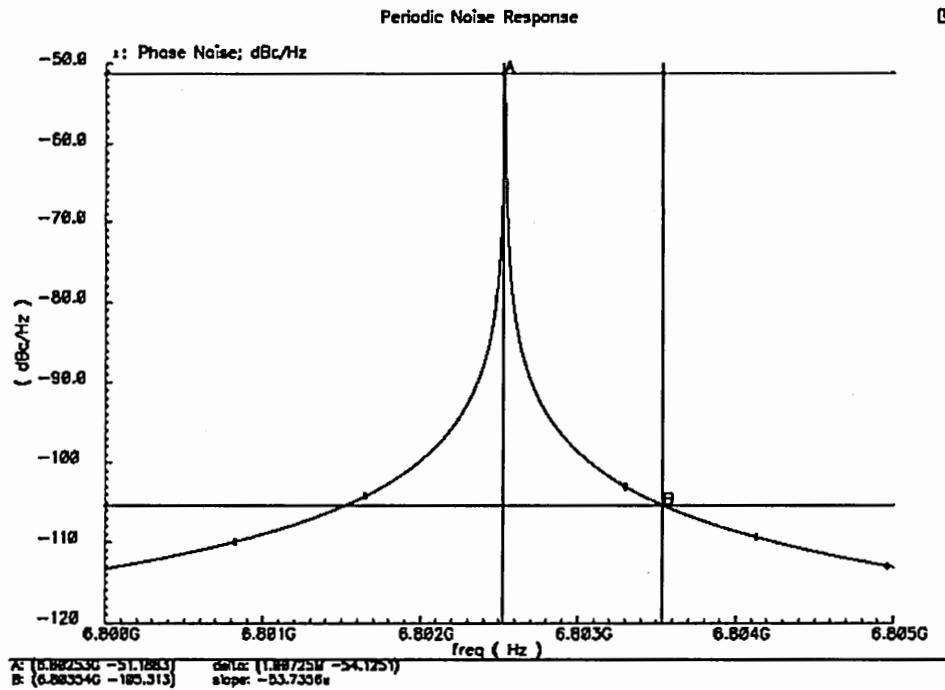


Figure 72: Phase noise simulation of the 4-stage ring in $0.18 \mu\text{m}$ CMOS

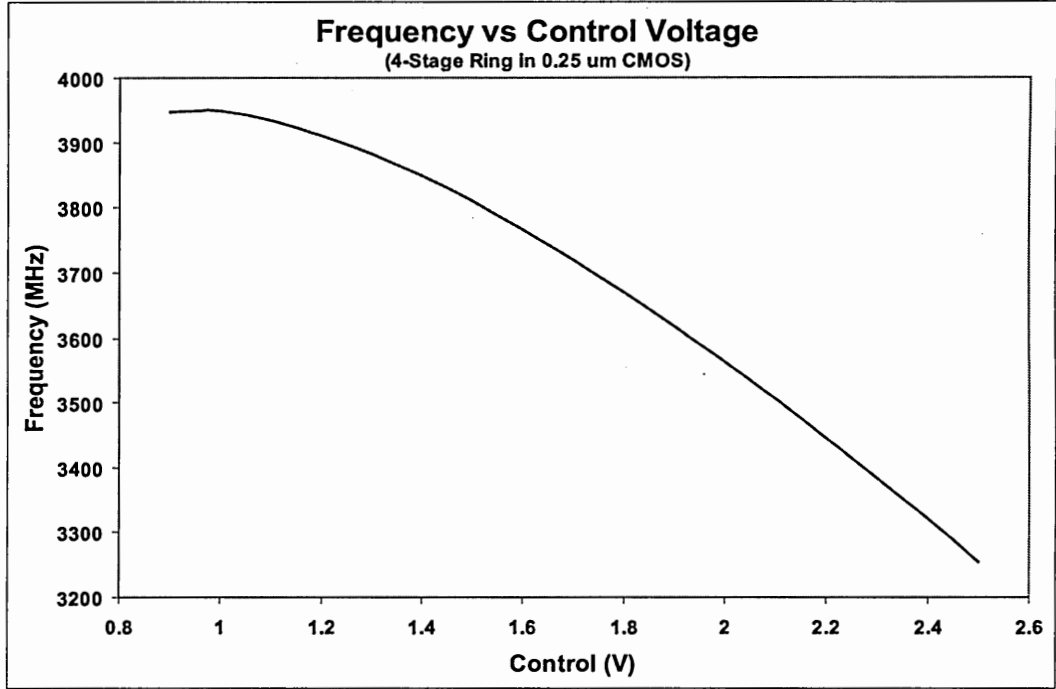


Figure 73: Frequency vs control voltage characteristics of the 4-stage ring VCO in 0.25 μm CMOS

the output when compared to the 3-stage designs that might be crucial in some applications requiring multiple phases. The in-phase/quadrature (I/Q) relationship of the output phases are especially important in image rejection systems and frequency multipliers. On the other hand, 4-stage designs dissipate more power when compared to their 3-stage counterparts due to additional active devices. They also require more layout area slightly increasing their implementation cost.

For the 4-stage ring designs described in this section, Figures 73 and 74 provide the frequency-voltage characteristics for 0.25 μm and 0.18 μm designs respectively. According to these, the 0.25 μm design has a linear operation range of 3.25-3.95 GHz when control voltages are varied between 0.9-2.5 V. This corresponds to a tuning range of 20% and a VCO gain of 0.44 GHz/V. The differential output swing of this design is between 4.2-4.3 V peak-to-peak, and the power dissipation is between 172-205 mW within the desired operation range. Power dissipation characteristics are given in Figure 75. The 0.18 μm 4-stage multiple-pass ring oscillator has a linear

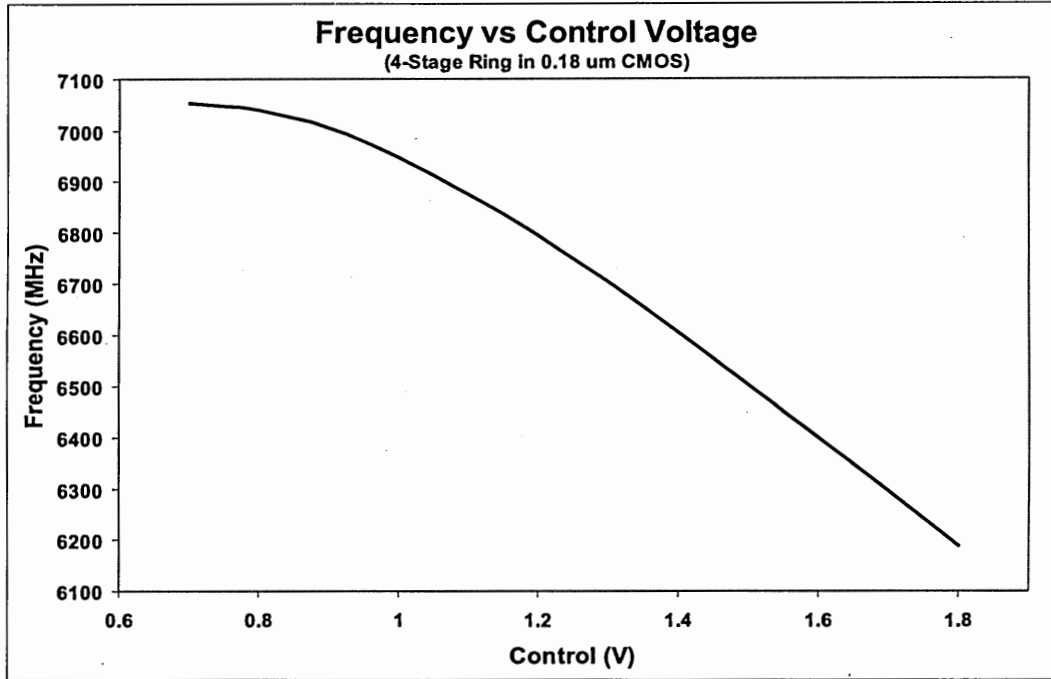


Figure 74: Frequency vs control voltage characteristics of the 4-stage ring VCO in $0.18\ \mu\text{m}$ CMOS

operation range of 6.19-7.05 GHz for control voltages of 0.7-1.8 V, which corresponds to a tuning range of 13% and a gain of 0.78 GHz/V. The differential output swing of this design is ~ 3.2 V throughout the whole control range with power dissipation varying between 122-147 mW. Power dissipation characteristics of the $0.18\ \mu\text{m}$ design is given in Figure 76.

6.3.2 Phase Noise Model, Revisited

Spectre RF simulation results showed that the four-stage designs have 6.11 dB ($0.18\ \mu\text{m}$) to 6.26 dB ($0.25\ \mu\text{m}$) better phase noise when compared to the three-stage designs. Subtracting the 2.48 dB accounting for the frequency difference, the actual improvements are found as 3.63 dB for the $0.18\ \mu\text{m}$ designs and 3.78 dB for the $0.25\ \mu\text{m}$ designs. As will be seen shortly, the cost of this phase noise reduction is the increased power dissipation. The four-stage ring oscillators discussed here dissipate $\sim 33\%$ more power per stage compared to the three-stage rings. Considering the number of

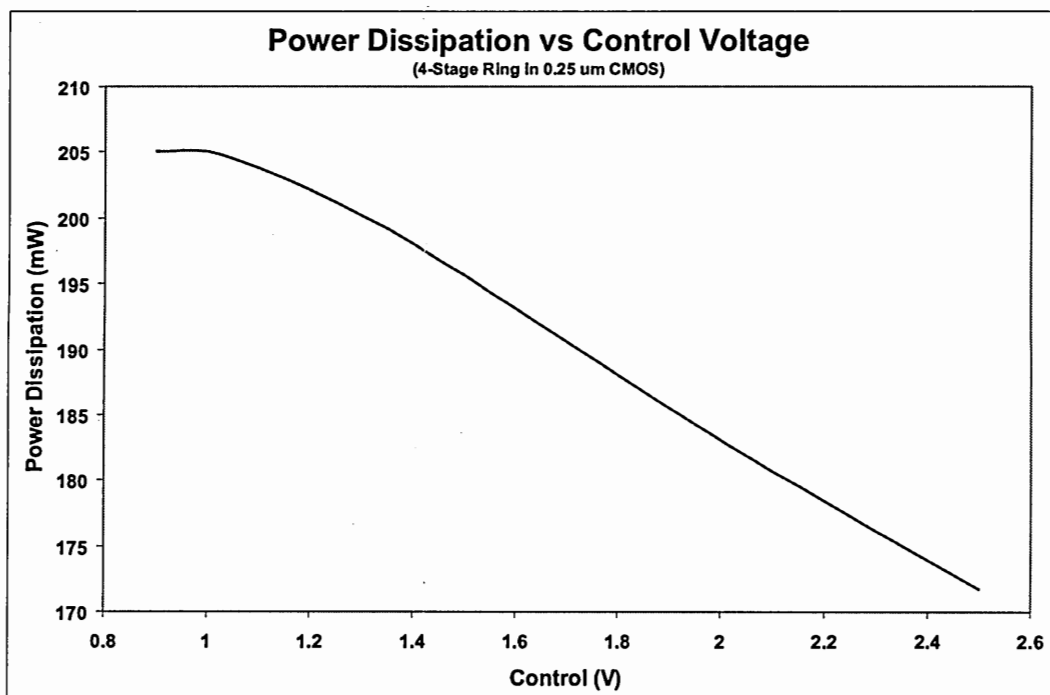


Figure 75: Power dissipation vs control voltage characteristics of the 4-stage ring VCO in 0.25 μm CMOS

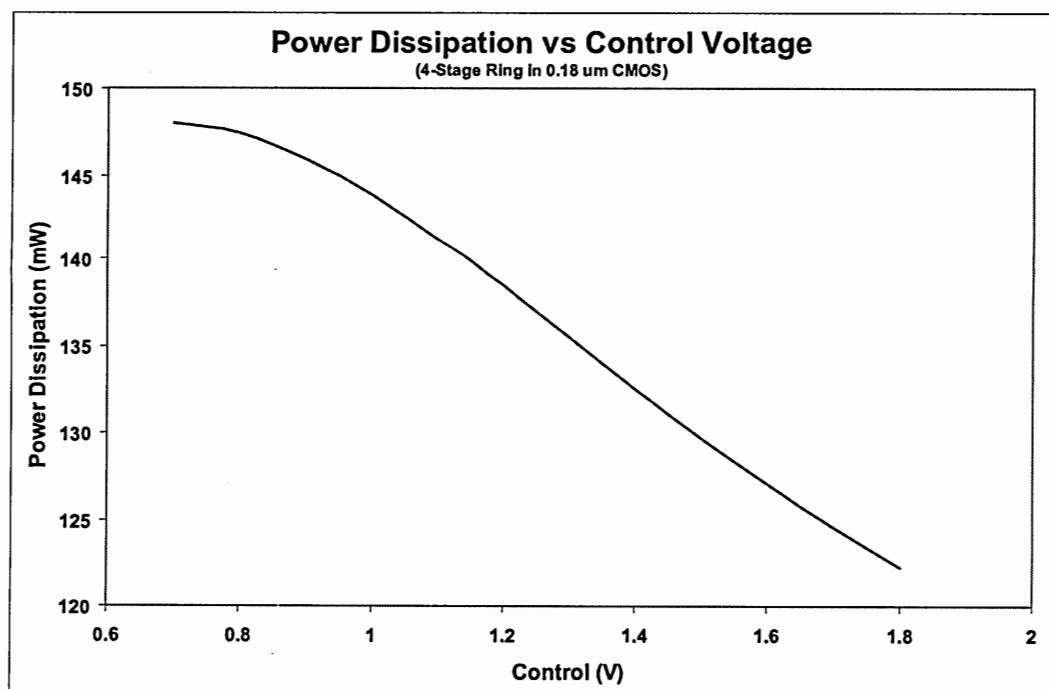


Figure 76: Power dissipation vs control voltage characteristics of the 4-stage ring VCO in 0.18 μm CMOS

Table 15: Phase noise of various $0.18\ \mu m$ designs extracted from simulations and calculations

Number of Stages	3	4	5	9
Calculated Phase Noise ($-dBc/Hz$)	94.90	103.35	105.39	115.26
Simulated Phase Noise ($-dBc/Hz$)	99.20	105.31	105.04	112.84
Noise Overestimation of Calculations (dB)	4.30	1.96	-0.35	-2.42

stages, total power increase is $\sim 78\%$.

Another observation is that the phase noise reduction estimated by the simulations are smaller than the improvements predicted by the calculations. This is because the difference between the simulated and calculated phase noise is larger for the three-stage designs. In fact, our further work on this issue demonstrated that for a 5-stage $0.18\ \mu m$ design running at 4.24 GHz, the calculations predict 0.35 dB better noise performance; whereas for a 1.8 GHz 9-stage $0.18\ \mu m$ design, the underestimation of the theory is 2.42 dB. The results for the $0.18\ \mu m$ CMOS designs are tabulated in Table 15 for comparison.

The derivation of the phase noise equations involve a number of approximations and an empirical excess noise factor F . Therefore, one can conclude that the simulations are more accurate in the computation of the phase noise since both of these factors are handled better, i.e. less number of approximations and no empirical factors similar to ISF model [36]. Therefore, the difference between the simulations and calculations is accounted to the noise mechanisms that are not considered in the used noise model.

One of these mechanisms is high-frequency multiplicative noise as discussed in Razavi's model [8]. This effect describes the folding of the noise components in the vicinity of the output harmonic frequencies around the oscillation frequency because of the nonlinearities. Alternatively, in the same model, this effect is described as the sampling of the output noise by the differential pair, and gets stronger as switching

gets harder. High-frequency multiplicative noise phenomena is automatically included in Hajimiri's model [32] using higher order terms c_n of the ISF. Razavi estimates that noise folding would approximately double the noise power of VCOs using simple differential pairs, i.e. 3 dB increase in the phase noise. Our simulations, however, showed that the noise folding is more pronounced for longer ring oscillators. For our three-stage designs, for example, the noise folding resulted in a ~ 2 dB increase of the phase noise; whereas for a nine-stage ring oscillator, the increase is ~ 5 dB. This is because nonlinearity increases as the number of stages increase such that transistors operate under full-switching instead of the linear regime. All the Spectre RF phase noise simulations in this work are performed with considering the noise folding effects by including four to eight harmonics and sidebands in the simulations.

Excess noise factor F depends on the structure of the oscillators and assumed as a constant 4 up to this point referring to the previous work discussing LC and single-loop ring oscillators. In this work, however, a first order correction to the excess noise factor F is introduced by linking it to the number of stages with a second order curve-fit function given in Equation (105).

$$F \approx -0.0674 N^2 + 1.6808 N - 2.6683. \quad (105)$$

This corrects the phase noise model for the effects of high-frequency multiplicative noise and multiple-pass loops. Using the new definition of excess noise factor F , Equation (59) is modified as

$$L(\Delta\omega) = \begin{cases} \frac{16 (-0.0674 N^2 + 1.6808 N - 2.6683) kTR}{NV_{pp}^2 \sin^2(\frac{\pi}{N})} \left(\frac{\omega_0}{\Delta\omega}\right)^2 & (for V_{pp} \ll V_{dd}) \\ \frac{128 (-0.0674 N^2 + 1.6808 N - 2.6683) kTR V_{dd}}{3\pi N \sin^2(\frac{\pi}{N}) V_{pp}^3} \left(\frac{\omega_0}{\Delta\omega}\right)^2 & (for V_{pp} \gg V_{dd}) \end{cases} \quad (106)$$

Single-sideband phase noise of the multiple-pass ring oscillators are recalculated using Equation (106). The new calculation results are provided in Tables 16 and 17.

Table 16: Phase noise of the 0.25 μm multiple-pass designs extracted from simulations and calculations using the modified formula (Equation (106))

Number of Stages	3	4
Calc. Phase Noise ($-\text{dBc}/\text{Hz}$)	106.19	110.98
Sim. Phase Noise ($-\text{dBc}/\text{Hz}$)	105.20	111.46
Overestimation of Calc. (dB)	-0.99	0.48

Table 17: Phase noise of the 0.18 μm multiple-pass designs extracted from simulations and calculations using the modified formula (Equation (106))

Number of Stages	3	4	5	9
Calc. Phase Noise ($-\text{dBc}/\text{Hz}$)	98.45	104.63	105.44	112.83
Sim. Phase Noise ($-\text{dBc}/\text{Hz}$)	99.20	105.31	105.04	112.84
Overestimation of Calc. (dB)	0.75	0.68	-0.40	-0.01

6.4 Designs with Various Configurations

As discussed above, 3-stage multiple-pass designs provide the highest oscillation frequencies while 4-stage designs offer a good tradeoff between the maximum frequency and the phase noise performance. Other than these designs, however, multiple-pass ring oscillators with different configurations can also be useful in some applications requiring lower frequencies and/or other features such as an increased number of output phases.

Increasing the number of stages in the oscillator loop naturally reduces the maximum attainable frequency because of the increased delay through the loop. The phase noise performance, on the other hand, referring to Equation (106), is expected to improve because of the lower center frequencies and signal transitions that take a smaller percentage of the whole period resulting in higher V_{pp} values. The improvement in the noise performance, however, may not be as much as expected because of an increase in the number of active devices that contribute to the output noise. Longer chains also result in stronger nonlinearity increasing noise folding effects. Additional

number of output phases may prove useful in oversampling applications that operate with multiple clock phases while the increased area requirement and the increased power consumption may be a problem in low-cost low-power systems.

For studying the characteristics of multiple-pass ring oscillators with different number of stages and different multiple-pass configurations, several ring oscillators were designed in $0.18\ \mu\text{m}$ CMOS. These designs have number of stages from three up to 9 and use type-I saturated stage with the transistor ratios given in Table 18. Tables 19 and 20 summarizes the output frequencies and the power dissipation of these designs. These tables also include the frequency improvement factors F_{imp} for comparison purposes. The control voltage was fixed at 1.8 V for all designs.

From the comparison of the frequency improvement factors with the oscillation frequencies, one can conclude that the oscillation frequencies are approximately on par with the frequency improvement factors. That is, positive frequency improvement factors F_{imp} result in much higher frequencies when compared to negative F_{imp} values. Furthermore, oscillation frequencies tend to increase with increasing F_{imp} values and vice versa. Note that when the frequency improvement factors are close together, the previous statement fails to be correct for some cases. For these cases, the configurations with larger F_{imp} values have increased power dissipation and sharper signal transitions although they have slightly reduced oscillation frequencies. This is accounted to the inaccuracy of the linear modelling of the ring oscillators involving rail-to-rail signal levels. Nevertheless, this behavior can be used to improve the phase noise performance of long ring oscillators at the cost of increased power dissipation. Another observation is the failure of the oscillators to oscillate when the configuration is selected to be $(N, N - 1, \pm)$, i.e. feedforward loops bridge over $N-2$ number of stages, with the exception of the 3-stage architecture. This is because these specific configurations have the most stringent gain requirements referring to Tables 2 and 3.

Table 18: Transistor sizes of the type-I saturated stage used in various $0.18\ \mu m$ ring oscillators

Transistor	Width	Length
M1-M2	$8 * 4\ \mu m$	$0.18\ \mu m$
M3-M4	$2 * 0.5\ \mu m$	$0.18\ \mu m$
M5-M6	$8 * 4.5\ \mu m$	$0.18\ \mu m$
M7-M8	$8 * 2.25\ \mu m$	$0.18\ \mu m$

6.4.1 Lower Frequency Designs

When lower frequency oscillators are required, configurations with increased number of stages is not the only solution. Alternatively, gain stages can be modified to reduce the frequency of the ring loops with three or four stages. When designed to run at the same oscillation frequency, ring loops with less number of stages are capable of working at much lower power levels and require less area at the expense of the noise performance. The noise performance of the designs with less number of stages might be improved by letting them dissipate extra power but this results in an increase in the layout area because of the increased transistor sizes. These trends can be seen in the simulation results comparing three and five stage $0.18\ \mu m$ CMOS ring oscillators oscillating at similar frequencies as illustrated in Table 21.

6.5 *Tuning Range Considerations*

Tuning range of a VCO is another characteristic that needs close attention. Low tuning range may create problems in meeting the frequency specification within a single fabrication run because the frequency of interest may fall out of the tuning range if process variations are not considered. This may result in the requirement of multiple fabrication iterations to meet the specifications. A wide tuning range, on the other hand, increases the gain of the VCO resulting in a higher sensitivity to control line noise. Tuning range, therefore, should be optimized according to the application.

Table 19: Output frequencies, power dissipations, and frequency improvement factors of multiple-pass loop configurations for $3 \leq N \leq 7$

N	x	sign	F_{imp}	Frequency (MHz)	Power (mW)
3	2	+	1.730	6967	55.85
3	2	-	-1.730	1290	68.12
4	2	+	1	4201	70.84
4	2	-	-1	869	70.51
4	3	+	-1.414	849	46.47
4	3	-	1.414	XX	XX
5	2	+	0.727	2780	90.85
5	2	-	-0.727	665	76.52
5	3	+	-1.176	649	69.61
5	3	-	1.176	2913	97.06
5	4	+	1.176	XX	XX
5	4	-	-1.176	644	62.18
6	2	+	0.577	2059	94.96
6	2	-	-0.577	538	86.87
6	3	+	-1	531	80.35
6	3	-	1	2177	102.6
6	4	+	1.155	2148	108.3
6	4	-	-1.155	523.8	72.8
6	5	+	-1	520.3	65.29
6	5	-	1	XX	XX
7	2	+	0.481	1663	70.57
7	2	-	-0.481	452	69.57
7	3	+	-0.867	448	63.09
7	3	-	0.867	1747	78.62
7	4	+	1.082	1740	85.03
7	4	-	-1.082	441	56.01
7	5	+	-1.082	439	48.27
7	5	-	1.082	1747	91.53
7	6	+	0.868	XX	XX
7	6	-	-0.868	436	40.71

Table 20: Output frequencies, power dissipations, and frequency improvement factors of multiple-pass loop configurations for $8 \leq N \leq 9$

N	x	sign	F_{imp}	Frequency (MHz)	Power (mW)
8	2	+	0.414	1409	71.16
8	2	-	-0.414	389	77.33
8	3	+	-0.765	368	70.80
8	3	-	0.765	1472	79.25
8	4	+	1	1499	86.93
8	4	-	-1	383	64.13
8	5	+	-1.082	379	56.54
8	5	-	1.082	1455	92.5
8	6	+	1	1484	99.58
8	6	-	-1	378	48.76
8	7	+	-0.765	375	41.16
8	7	-	0.765	XX	XX
9	2	+	0.364	1226	72.24
9	2	-	-0.364	342	85.52
9	3	+	-0.684	339	78.95
9	3	-	0.684	1278	80.37
9	4	+	0.922	1307	88.33
9	4	-	-0.922	338	72.34
9	5	+	-1.048	333	65.23
9	5	-	1.048	1283	94.61
9	6	+	1.048	1269	100.9
9	6	-	-1.048	333	57.46
9	7	+	-0.922	1293	108
9	7	-	0.922	331	49.66
9	8	+	0.684	329	42.05
9	8	-	-0.684	XX	XX

Table 21: Performance comparison of three and five stage rings oscillating at the same frequency

Design	5-Stage	3-Stage Low Power	3-Stage High Power
M1-M2	32 μm /0.18 μm	32 μm /0.285 μm	80 μm /0.315 μm
M3-M4	1 μm /0.18 μm	1 μm /0.285 μm	1 μm /0.315 μm
M5-M6	36 μm /0.18 μm	36 μm /0.285 μm	90 μm /0.315 μm
M7-M8	18 μm /0.18 μm	18 μm /0.285 μm	45 μm /0.315 μm
Control Voltage	1.2 V	1.2 V	1.2 V
f_0	4235 MHz	4323 MHz	4421 MHz
Power	86.21 mW	33.8 mW	77.55 mW
Δf	1 MHz	1 MHz	1 MHz
Phase Noise	-105.04 dBc/Hz	-101.8 dBc/Hz	-104.34 dBc/Hz

6.5.1 Control of The Tuning Range

As already implied in the previous chapter, the tuning range of a ring oscillator employing the type-I saturated gain stage can be varied by modifying the sizes of the switches, M_3 and M_4 in Figure 40, that control the regeneration. Smaller switch sizes limit how much the feedback gain changes throughout the control range and result in narrow tuning ranges, whereas increasing the switch aspect ratios lead to a larger change in the feedback amount resulting in a wider tuning range. This way, tuning range can be increased at the low-frequency end while slightly reducing the maximum frequency because of the extra loading. Wider tuning ranges also result in increasingly nonlinear frequency-voltage characteristics. Figure 77, for example, shows how the frequency-voltage characteristics of a 4-stage 0.18 μm oscillator changes when the switch widths are increased from $2*0.5 \mu\text{m}$ to $12*0.5 \mu\text{m}$. By increasing the switch sizes, tuning range is increased to 37 % from 16 % with a 125 MHz decrease in the maximum frequency. From the plots, it is clear that linearity is worse for the wide tuning range design. The transistor sizes of the wide tuning range design is provided in Table 22.

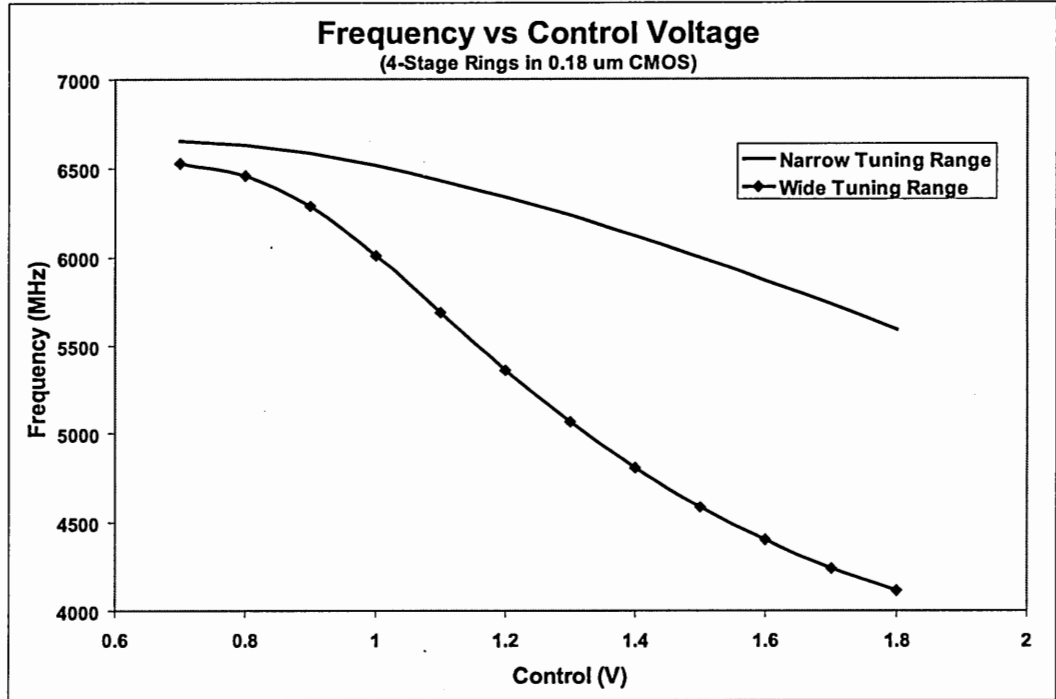


Figure 77: Frequency-voltage characteristics of narrow and wide tuning range 4-stage ring designs in 0.18 μm CMOS

Table 22: Transistor sizes of the 4-stage wide-tuning range ring design in 0.18 μm CMOS

Transistor	Width	Length
M1-M2	16 * 4 μm	0.18 μm
M3-M4	12 * 0.5 μm	0.18 μm
M5-M6	16 * 3.5 μm	0.18 μm
M7-M8	16 * 3 μm	0.18 μm

6.5.2 Dual Control-Path Ring Oscillators

The ring oscillator designs that were discussed up to this point all use the type-I stage that employs a single-ended control network. Differential control is more desirable because this reduces the oscillators' noise sensitivity to disturbances on the control lines. Depending on where the control voltage is referred to, ground and supply bounces may also create a problem in single-ended control schemes. Another issue related with using the regeneration control alone, as in the type-I stage, is the tradeoff between the tuning range and the VCO gain/linearity that was discussed above. Type-II saturated stage, Figure 41, overcomes these problems by introducing multiple control paths. The single-ended regeneration control provides coarse tuning, while fine tuning is achieved using differentially controlled charge pumps synchronized with the primary inputs. The additional charge supplied by the charge pumps is minuscule when compared to the total charge swing during a single cycle. Therefore, the noise performance of the oscillator is expected not to vary significantly by switching from type-I saturated stage to type-II saturated stage. The additional loading may cause a slight reduction in the maximum frequency.

For verifying these statements, a three stage multiple-pass ring oscillator was designed in $0.25\ \mu\text{m}$ by using the type-II stage. Table 23 shows the transistor size of this design. The stage core was kept same as the three stage $0.25\ \mu\text{m}$ ring design, with the transistor sizes given in Table 7, for understanding the consequences of adding the fine control path. The input current was generated by the differential current control circuitry of Figure 42, where the input current was selected to be $600\ \mu\text{A}$. The transistor sizes of the current control circuitry are provided in Table 24.

The frequency-control characteristics of the dual control-path design is shown in Figure 78. According to the simulations, the overall tuning range is 1.3 GHz for a maximum frequency of 5.05 GHz, whereas the fine tuning range is between 160-230 MHz when the differential control is varied from -1.5 V to 1.5 V. Fine-tuning range is

Table 23: Transistor sizes of the type-II stage employed in the 3-stage $0.25\ \mu m$ ring design with dual control-paths

Transistor	Width	Length
M1-M2	$8 * 5\ \mu m$	$0.24\ \mu m$
M3-M4	$2 * 0.6\ \mu m$	$0.24\ \mu m$
M5-M6	$16 * 3.5\ \mu m$	$0.24\ \mu m$
M9-M10	$12 * 0.72\ \mu m$	$0.24\ \mu m$
M11-M12	$4 * 0.72\ \mu m$	$0.24\ \mu m$
M13-M14	$16 * 4.5\ \mu m$	$1\ \mu m$
M15-M16	$8 * 4.5\ \mu m$	$1\ \mu m$
M17	$8 * 4.5\ \mu m$	$1\ \mu m$

Table 24: Transistor sizes of the differential input current control circuitry of the 3-stage $0.25\ \mu m$ ring design with dual control-paths

Transistor	Width	Length
M1	$16 * 4.5\ \mu m$	$1\ \mu m$
M2-M3	$4 * 1\ \mu m$	$2\ \mu m$
M4-M5	$8 * 4.5\ \mu m$	$1\ \mu m$
M6	$16 * 4.5\ \mu m$	$1\ \mu m$
M7	$8 * 4.5\ \mu m$	$1\ \mu m$

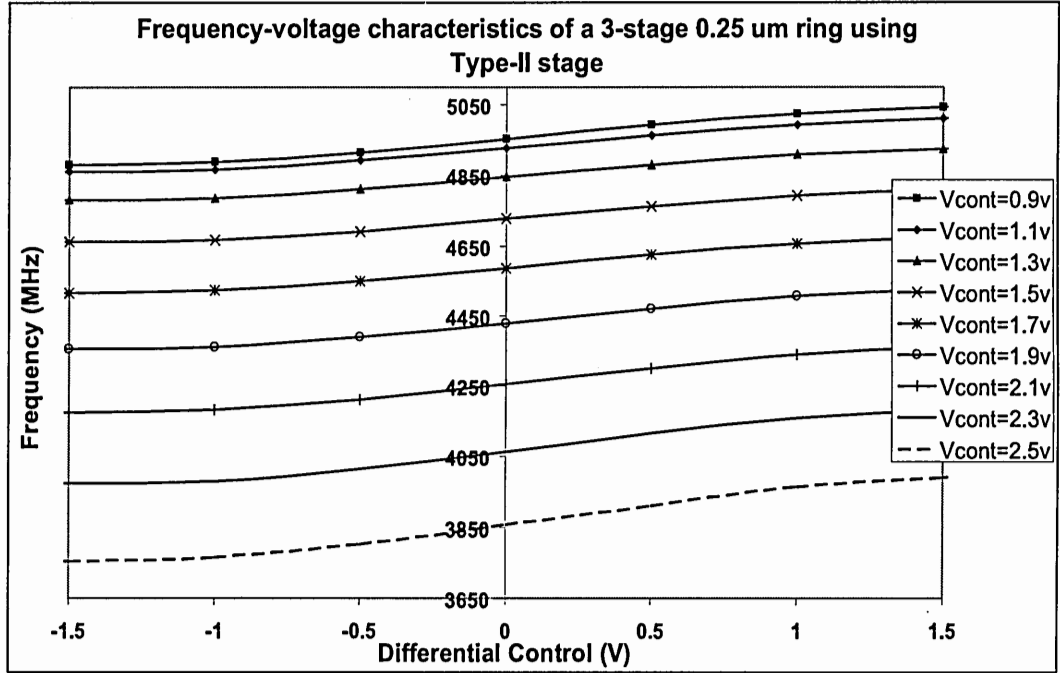


Figure 78: Frequency vs control voltage characteristics of the 3-stage 0.25 μm ring design with dual control-paths

calculated to be 181-233 MHz using Equation (94) demonstrating a good agreement between simulations and calculations. By switching from type-I saturated gain stage to type-II saturated gain stage, oscillator gain is reduced to 53-77 MHz/V from 720 MHz/V with an increase of the overall tuning range from 22% to 26%. The additional loading at the output resulted in a 5% reduction of the maximum frequency. The phase noise of the multiple-control design was calculated to be -106.01 dBc/Hz at a 1 MHz offset from a 4.73 GHz center frequency while the value extracted from the simulation is -105.83 dBc/Hz. As expected, noise performance did not change significantly. Table 25 summarizes the simulation results of the 3-stage dual control-path and single control-path ring designs.

6.6 Parameter Variations

One of the most critical challenges in the design and implementation of an integrated VCO is the stability across temperature and process corner variations. These

Table 25: Performance comparison of 3-stage dual-control and single-control ring oscillators in $0.25\ \mu m$

Stage Structure	Type-I (single control)	Type-II (dual-control)
Number of Stages	3	3
Technology, TSMC CMOS	$0.25\ \mu m$	$0.25\ \mu m$
Maximum Frequency (MHz)	5300	5050
Tuning Range (%)	22	26
VCO Gain (MHz/V)	720	53-77
f_0 (MHz)	5071	4740
Δf (MHz)	1	1
Phase Noise (-dBc/Hz) - simulation	105.20	105.83
Phase Noise (-dBc/Hz) - calculation	106.19	106.01

parameters include the ambient temperature of the system, possible variances of physical parameters such as the gate-oxide thickness and dopant diffusion densities, and power-supply/ground fluctuations. The joint effect of these variations might have a huge impact on the characteristics and the performance of the integrated circuits. In this section, by using an example design, the behavior of the designed multiple-pass ring oscillators will be observed under different conditions. The analysis will be performed on the wide tuning range 4-stage multiple-pass design with the frequency-voltage characteristics shown in Figure 77.

6.6.1 Temperature Variations

All CMOS analog circuits exhibit some sort of temperature dependency because the transconductances and the threshold voltages of MOS transistors change with temperature. The carrier mobility μ , and therefore the transconductance, of a transistor, for example, is dependent upon the temperature with the relation [37]

$$\mu = K_\mu T^{-1.5}, \quad (107)$$

where K_μ is a constant. Note that, the I-V curve and transconductance equations of MOS transistors both include the transconductance parameter K' , which is equal to

$\mu_0 * C_{ox}$. The temperature dependence of the threshold voltage, on the other hand, can be written as [37]

$$V_T(T) = V_T(T_0) - \alpha(T - T_0), \quad (108)$$

where α is approximately $2.3 \text{ mV}/^\circ\text{C}$. This equation can be used for $200^\circ\text{K} < T < 400^\circ\text{K}$, with α depending on the substrate doping level and the implant dosages. For a ring oscillator, unless the frequency is controlled by a stable current supply referenced to a bandgap circuit, the frequency drift can be as high as 1000-2000 ppm/ $^\circ\text{C}$ [30]. In our circuits, since all the input and load transistors are directly connected to the power busses, the oscillation frequency is strongly dependent upon the transconductances and the threshold voltages of the devices. Therefore, the temperature dependency should be within the given range. For the 4-stage ring oscillator, the center frequency changes 372 MHz for a nominal value of 5291 MHz when the temperature is varied between 0°C and 85°C . This corresponds to a temperature dependence of 827 ppm/ $^\circ\text{C}$. The effect of the temperature change on the frequency-voltage characteristics of this design is given in Figure 79.

6.6.2 Physical Parameters

In a typical semiconductor foundry, the physical characteristics of the fabricated devices vary slightly among different fabrication runs. Furthermore, even a single die may exhibit physical parameter gradients. These parameters include the gate-oxide thickness of the devices that affect the transconductances, dopant diffusion densities that affect the resistivities of various layers, etc. Note that only a small variation of these physical parameters may affect electrical characteristics of the devices significantly. Physical parameter variations are highly random in nature; therefore, statistical analysis of multiple runs are used to define the characteristics of a specific process. Process corners such as slow-slow, typical-typical, or fast-fast are defined and modelled in this way. Slow-slow, for example, refers to slow models exhibiting

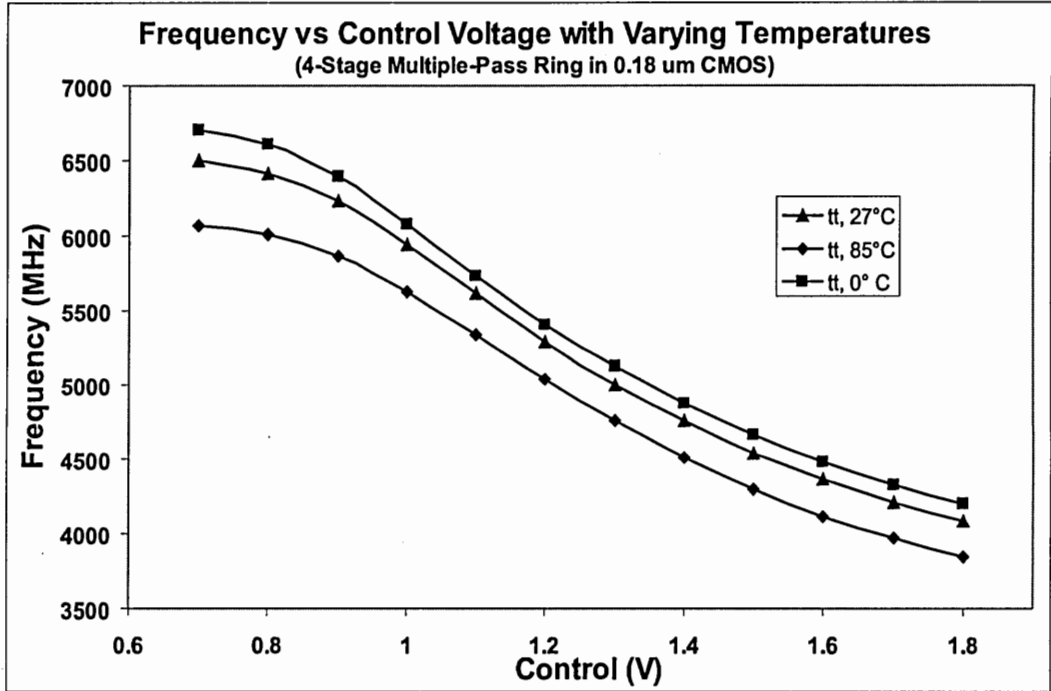


Figure 79: f-V characteristics of the 4-stage 0.18 μm multiple pass design at different ambient temperatures

smaller NMOS and PMOS transconductances when compared to nominal values. In this work, the 4-stage multiple-pass design was characterized in three corners: slow-slow (ss), typical-typical (tt), and fast-fast (ff). The results are summarized in Figure 80, which shows the frequency-voltage curves at different process corners. This plot demonstrates that the center frequency varies from 4400 MHz at the slow-slow corner up to 6310 Mhz at the fast-fast corner, with nominal center frequency being 5290 MHz. This corresponds to a 35.8 % change of the frequency among the process corners.

Note that, temperature changes and the process variations have a cumulative effect on the circuits. That is, the circuit characteristics may vary significantly if ambient temperature changes and process variations push the oscillator in the same direction, slowing it down if the temperature is high and the process corner is slow-slow and vice-versa. To examine the cumulative effects, the 4-stage design was simulated at the slow-slow corner with the ambient temperature selected as 85 °C, and at the

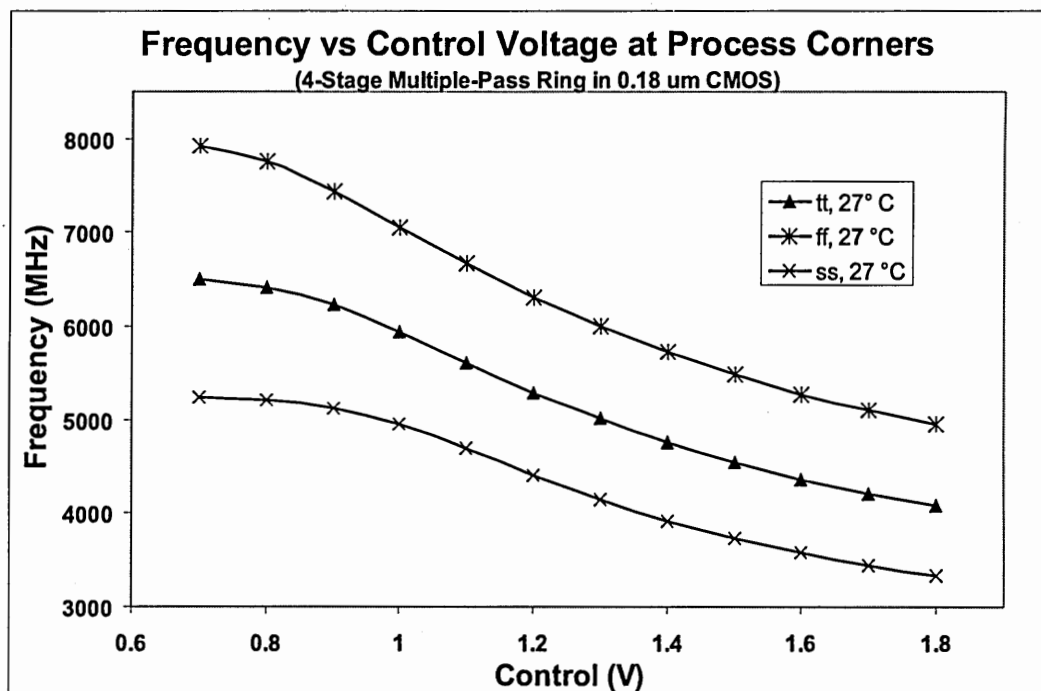


Figure 80: f-V characteristics of the 4-stage 0.18 μm multiple pass design at different process corners

fast-fast corner with the ambient temperature selected as 0 °C, in addition to the typical-typical corner at 27 °C. As shown in Figure 81, the center frequency varies from 4170 MHz at the slow-slow corner, 85 °C up to 6440 Mhz at the fast-fast corner, 0 °C, with nominal center frequency being 5290 MHz. This corresponds to a 42.9 % change of the frequency under these variations.

6.6.3 Power Supply/Ground Disturbances

Variation of the main power supply voltage or the ground level can change the characteristics of the analog circuits significantly because all other node voltages and currents depend on these reference voltages. Transconductances, for example, may increase with increasing power supply voltage and so may the device currents. For a ring oscillator, therefore, higher voltages may result in extremely high oscillation frequencies and vice-versa. The effect of static power supply variation on the frequency-voltage characteristics of the 4-stage multiple-pass ring oscillator is illustrated in

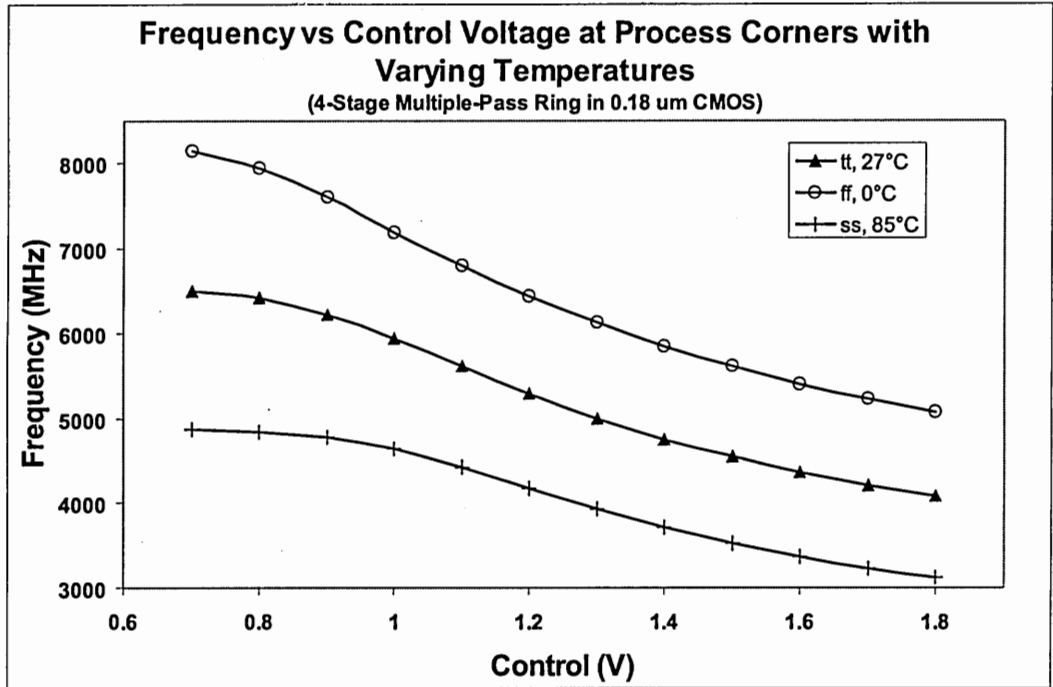


Figure 81: f-V characteristics of the 4-stage 0.18 μm multiple pass design at different ambient temperatures and process corners

Figure 82 . According to the simulation results, the center frequency of the ring oscillator varies between 4600-5900 MHz when the power supply voltage is changed from 1.65 V to 1.95 V with the nominal center frequency being 5290 MHz at a power supply voltage of 1.8 V. This shift of the frequency-voltage curve may be prevented by using a voltage regulator.

Differential circuits have some level of immunity against the common mode disturbances such as power supply and substrate variations. This immunity comes from the fact that any signal that appears at both outputs of a differential circuit will be cancelled completely. All analog differential circuits, nevertheless, suffer from some sensitivity to supply and substrate noise. This is because during the operation of a dynamic differential circuit, node voltages switch continuously such that the circuit almost never exists in a balanced state. Outputs of the differential circuit, therefore, respond differently to any disturbance on the power bus or on the ground bus.

The power-supply/ground noise response of the 4-stage multiple-pass ring design

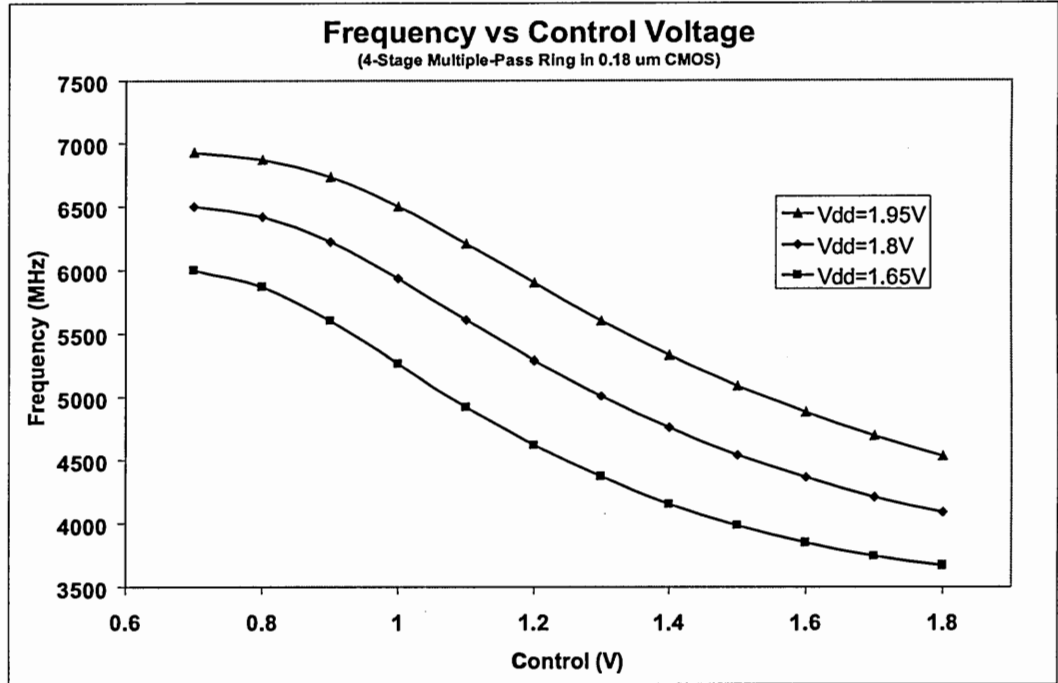


Figure 82: f-V characteristics of the 4-stage 0.18 μm multiple pass design at different power supply voltages

was studied by simulating the oscillator in time-domain with different types of noise placed on top of the power supply and the ground. Figures 83, and 84 show how the period of the output signal changes when 100 mV_{pp} , 5 GHz sinusoidal noise is injected on top of the power-supply and the ground respectively. These plots show that the oscillator exhibits a negligible instantaneous period jitter under the influence of sinusoidal V_{DD} noise, while the sinusoidal ground noise creates a 2 psec instantaneous period jitter and 0.7 psec peak-to-peak periodic jitter.

Note that, analog circuits are more susceptible to ground variations because every parameter in the network are referenced to the ground. The ground node, for that reason, is usually designed to be the most stable node in any IC. Figures 85, and 86 show the total phase jitter accumulation due to the period jitter for the cases with sinusoidal V_{DD} and sinusoidal ground noise respectively. According to these plots, the phase jitter due to sinusoidal V_{DD} noise is negligible, whereas sinusoidal ground noise effectively slows down the oscillator resulting in negative phase accumulation.

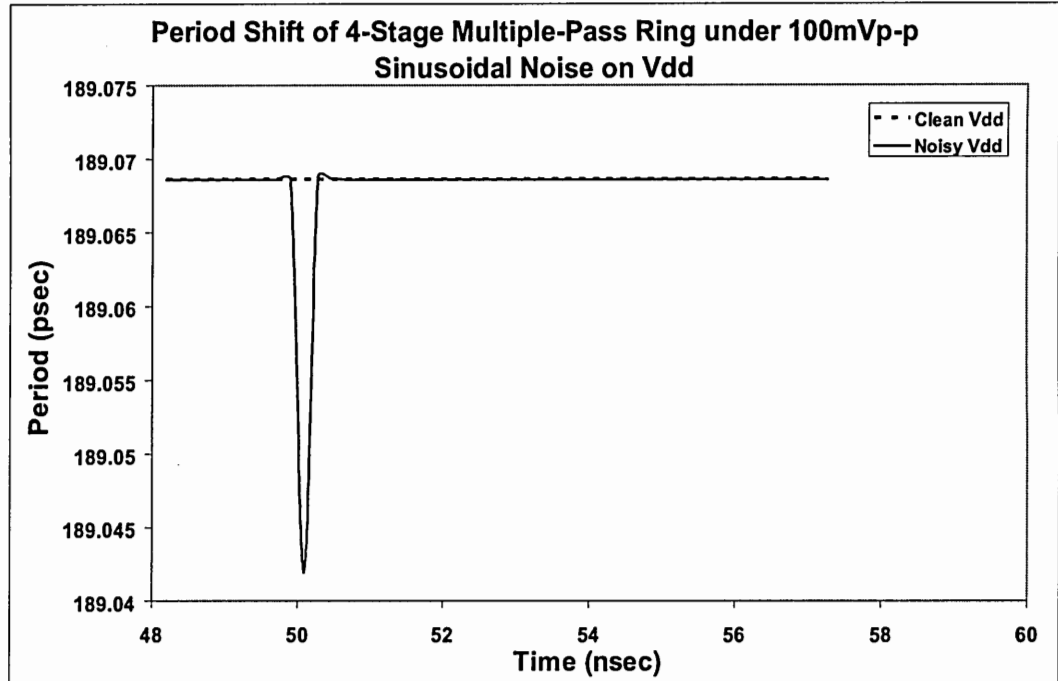


Figure 83: Period shift of 4-Stage multiple-pass ring under 100 mV_{p-p} , 5 GHz sinusoidal noise on Vdd

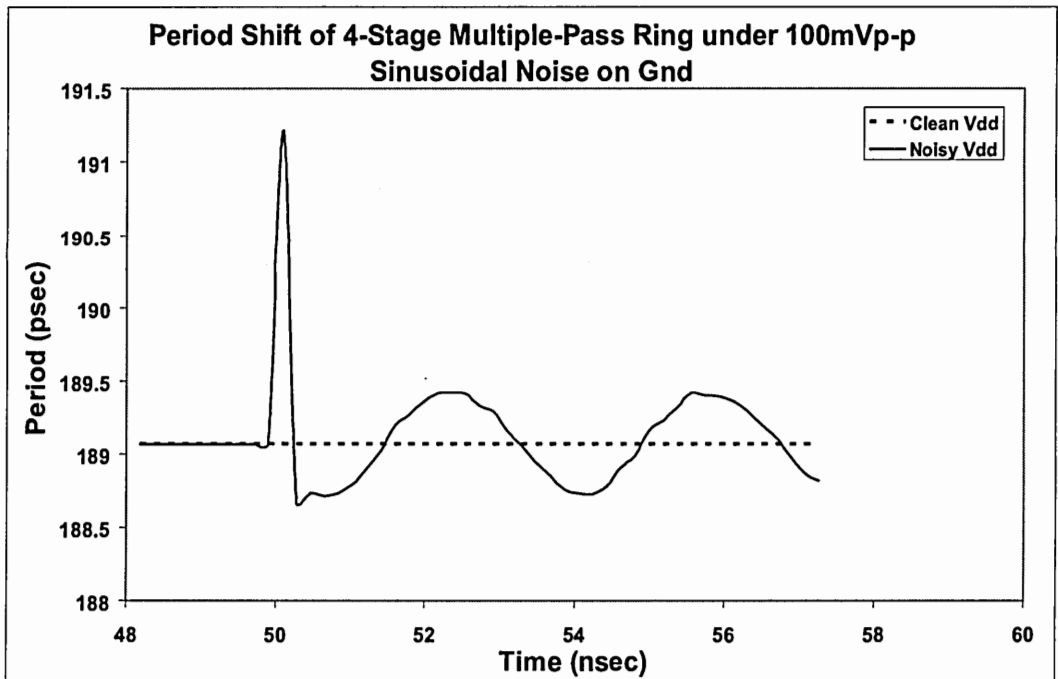


Figure 84: Period shift of 4-Stage multiple-pass ring under 100 mV_{p-p} , 5 GHz sinusoidal noise on ground

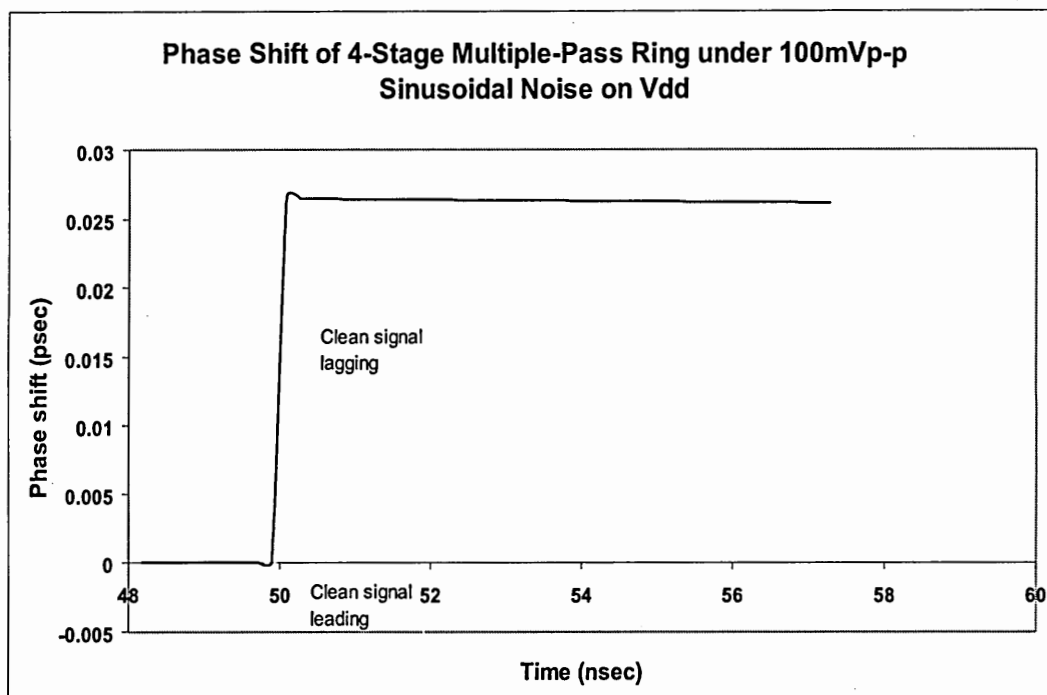


Figure 85: Phase shift of 4-Stage multiple-pass ring under 100 mV_{p-p} , 5 GHz sinusoidal noise on Vdd

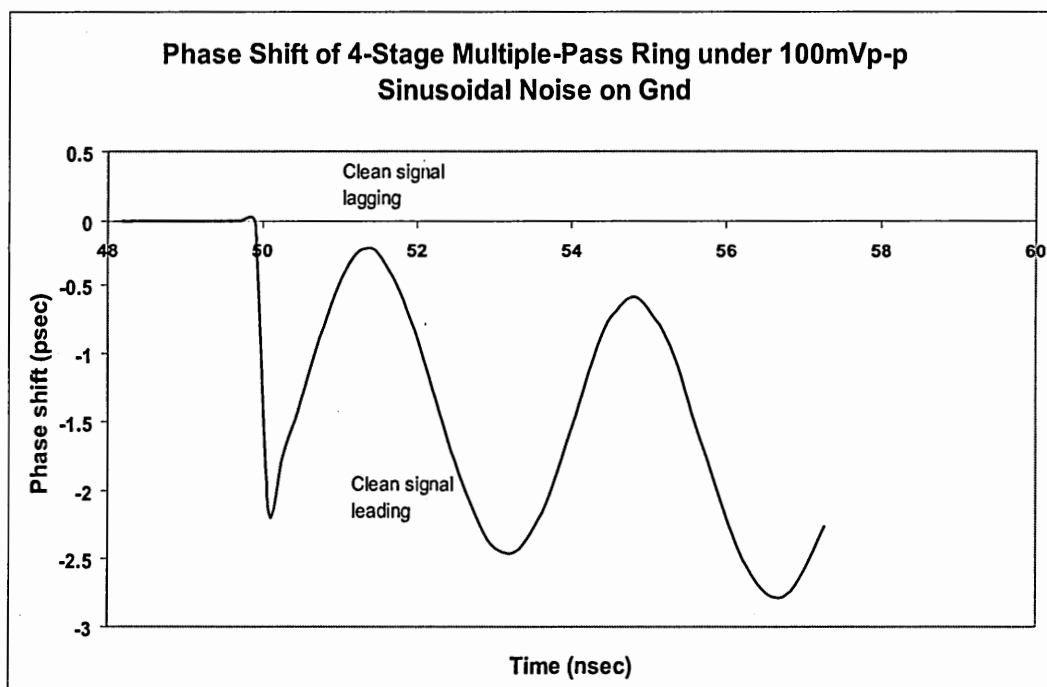


Figure 86: Phase shift of 4-Stage multiple-pass ring under 100 mV_{p-p} , 5 GHz sinusoidal noise on ground

Another type of supply/substrate noise that needs to be considered is the supply-substrate bounces. That is, large amplitude short pulses that resemble the delta-dirac impulse function. There are various events that might result in glitches on the V_{DD} or ground busses. The switching of the digital gates on the same chip, for example, create glitches on the V_{DD} bus via cross-talk or by changing the total sourced current instantaneously. Turning on/off the circuits in an electronic system may also create glitches through the same mechanics. In this work, glitch effects were simulated by injecting an impulse signal to the supply and ground busses. This noise signal has an amplitude of 1 V and a width of 10 psec, sufficiently short when compared to one period of the output but powerful enough to create a significant shift in the operating point.

One of the major observations from the simulations is that the output response strongly depends on the phase of the glitch, that is when it occurred with respect to the output signal period. Simulations showed that the most vulnerable intervals of the output signal are the rising and falling edges resulting in the largest period/phase jitter. When the glitch hits at the peaks of the periodic wave at the output, the effect is smaller. This observation is in accordance with Hajimiri's noise model [32]; that is, ISF is larger during the transitions and smaller at the signal peaks. Figure 87 shows the time domain output and V_{DD} signals for the V_{DD} glitch that results in the worse jitter. This glitch results in an instantaneous period jitter of 2.5 psec, and a slowly diminishing phase jitter of 4 psec as illustrated in Figures 88 and 89 respectively. Figure 90 shows the time domain output and ground signals for the ground glitch that results in the worse jitter. As expected, ground bounce results in larger jitter when compared to the V_{DD} bounce of same magnitude. The instantaneous period jitter is 9 psec, and the phase jitter is approximately 9 psec as illustrated in Figures 91 and 92 respectively.

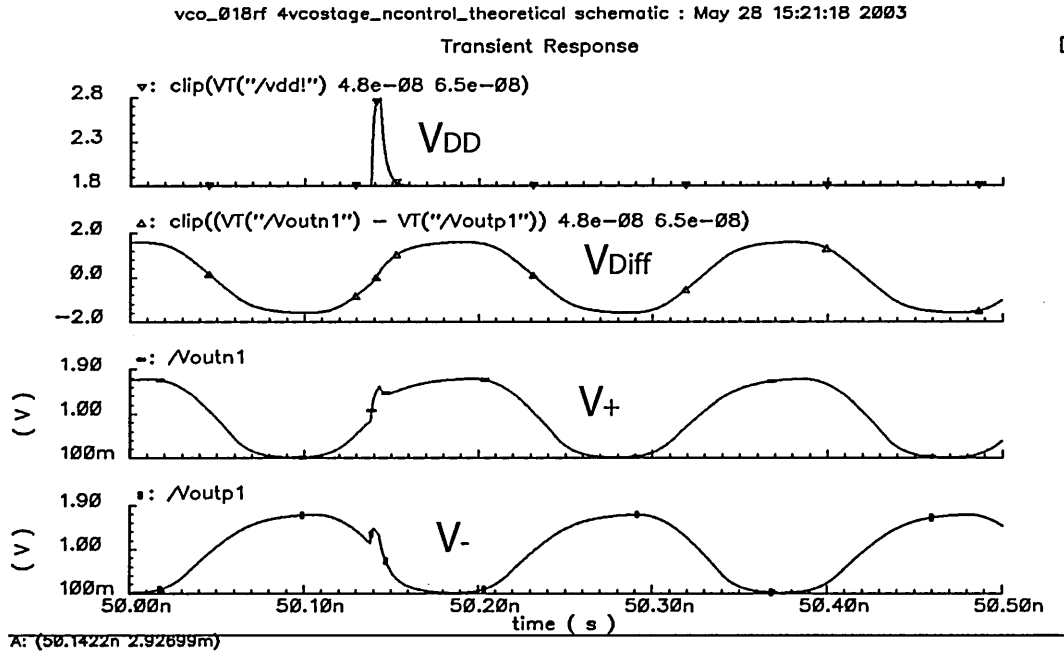


Figure 87: Output and V_{DD} signals of the 4-stage multiple-pass ring oscillator when a V_{DD} glitch occurs at the most vulnerable moment

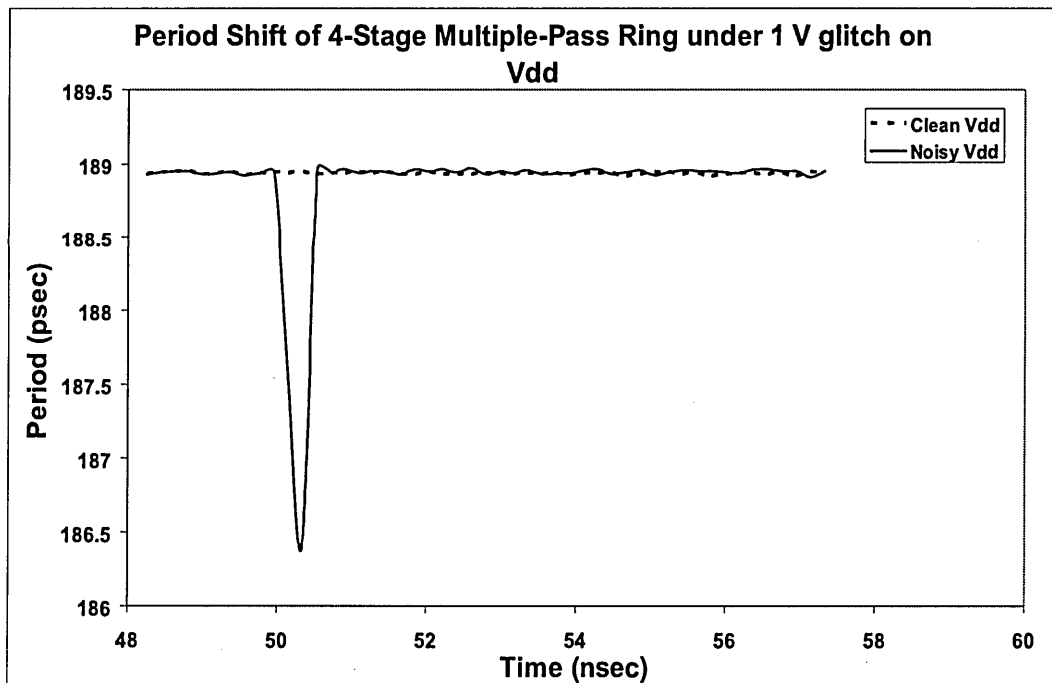


Figure 88: Period shift of the 4-stage multiple-pass ring oscillator when a V_{DD} glitch occurs at the most vulnerable moment

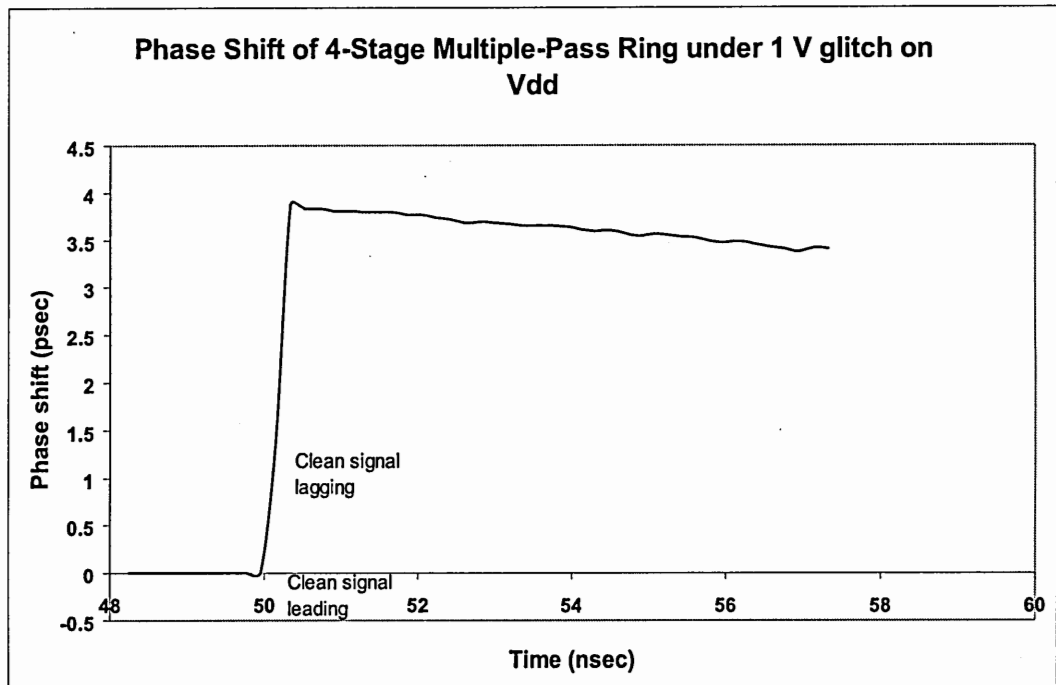


Figure 89: Phase shift of the 4-stage multiple-pass ring oscillator when a V_{DD} glitch occurs at the most vulnerable moment

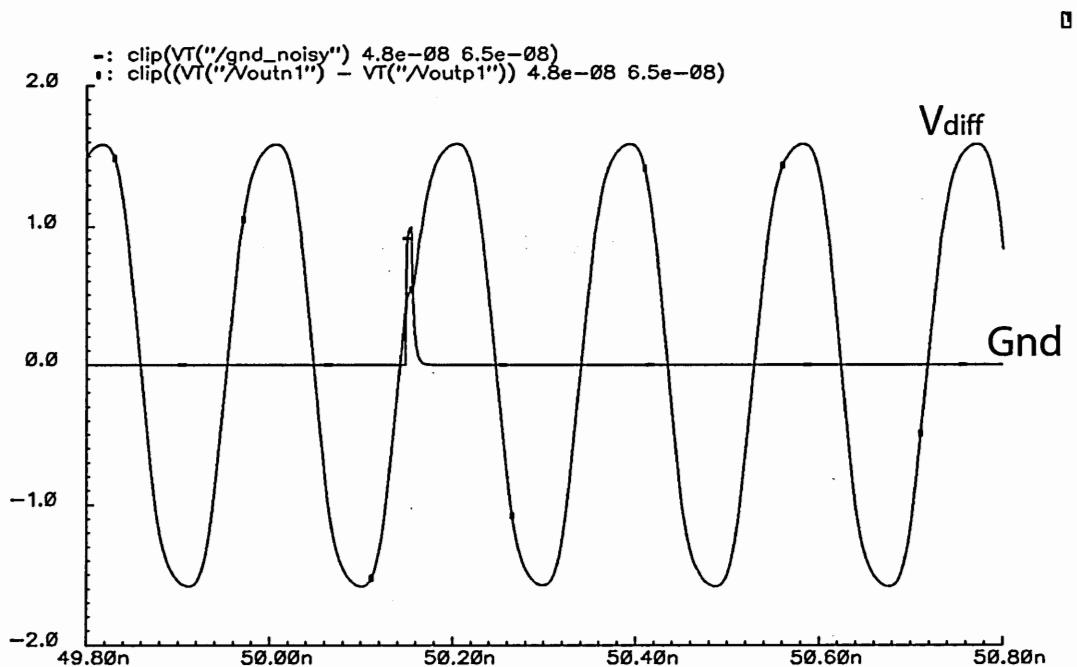


Figure 90: Output and ground signals of the 4-stage multiple-pass ring oscillator when a ground glitch occurs at the most vulnerable moment

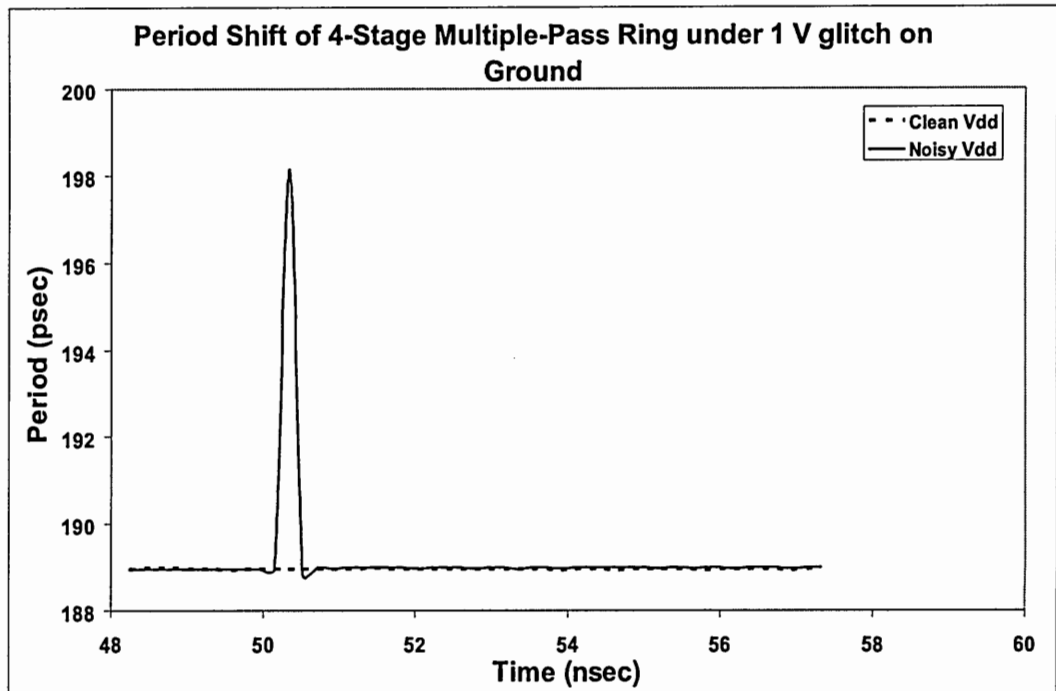


Figure 91: Period shift of the 4-stage multiple-pass ring oscillator when a ground glitch occurs at the most vulnerable moment

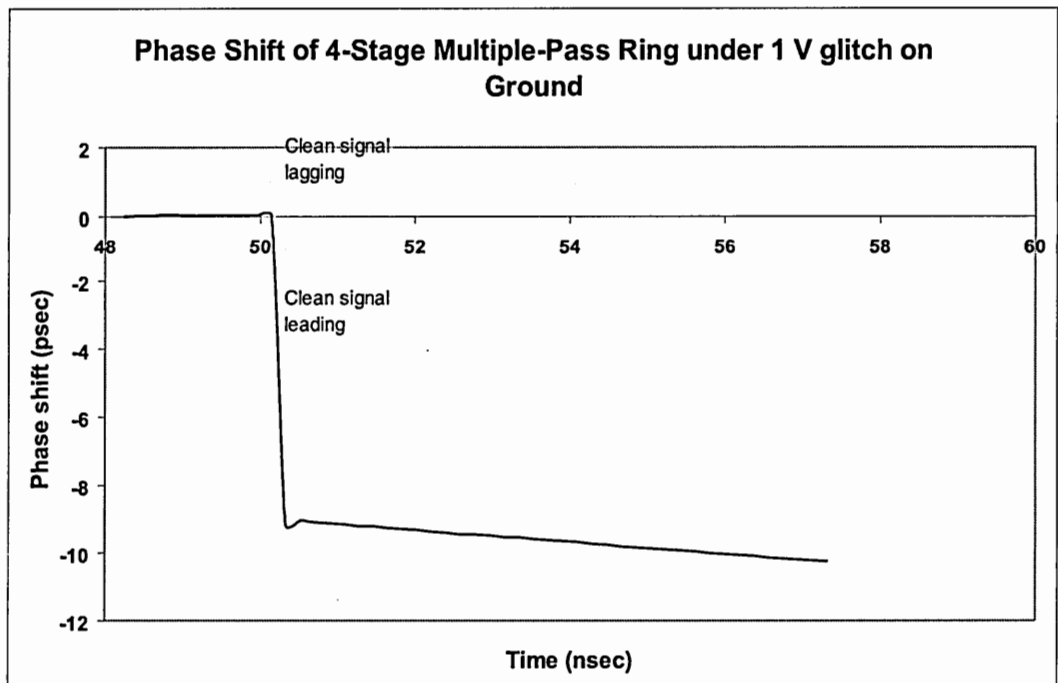


Figure 92: Phase shift of the 4-stage multiple-pass ring oscillator when a ground glitch occurs at the most vulnerable moment

6.7 *Summary*

After discussing design techniques for implementing high-frequency low-noise voltage controlled ring oscillators in the previous chapter, in this chapter, by introducing various high-performance ring VCO designs, it was demonstrated how to actually apply these techniques in sub-micron CMOS technologies. The practical application of the previously provided noise models (Chapter IV), was also described. The results showed that three-stage designs provide the highest frequencies, four-stage designs provide a good trade-off between the maximum frequency and the phase noise, and longer chains may be feasible when additional output phases are required. In addition to the phase noise and maximum frequency of the oscillators, other important characteristics are also analyzed including the tuning range and the stability under parameter variations. Although the introduced designs are compared with each other, a frame of reference is required to better evaluate the provided performance levels. In the next chapter, for this purpose, conventional ring oscillators are designed and the performances are compared.

CHAPTER VII

BENCHMARK DESIGNS

Up to this section of this thesis, the design of multiple-pass ring oscillators were extensively studied and various performance criteria were provided to characterize the designed oscillators. For the given performance levels to make sense, however, reference designs are needed. Two widely used ring oscillator designs were chosen for this purpose: a single loop ring oscillator with current-starved inverter stages, and a differential ring oscillator employing a differential pair stage with Maneatis loads [21].

7.1 Current Starved Ring Oscillator

The current starved inverter is constructed from two pairs of NMOS and PMOS transistors, first pair M1-M2 used as a simple inverter, while the second pair M3-M4 is used to control the driving strength of the inverter as illustrated in Figure 93.

The 0.18 μm current starved ring oscillator uses a three stage architecture for obtaining the highest maximum frequency. The main modification over the simple current starved structure is the use of current for frequency control. Note that the original current starved inverter is controlled by two different control voltages $V_{control1}$ and $V_{control2}$. Figure 94 illustrates, how a controlled current source is used to generate the required control voltages. The optimization of the oscillator was performed by fixing the width W_n of the NMOS transistor M1 and by sweeping the width W_p of the PMOS transistor M2. This process was carried out for multiple M1 sizes turning out the frequency characteristics given in Figure 95. According to these curves, the maximum frequency is obtained at a PMOS to NMOS ratio W_p/W_n of approximately two, while larger transistors correspond to higher frequencies with an increase of

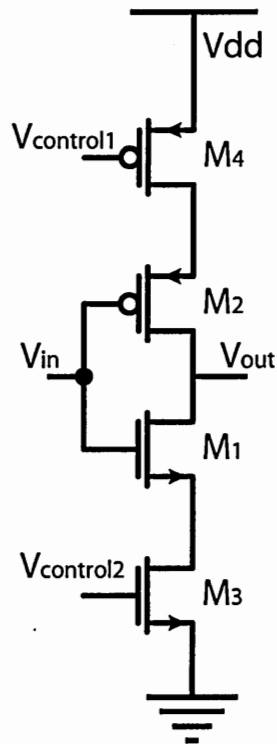


Figure 93: Current starved inverter

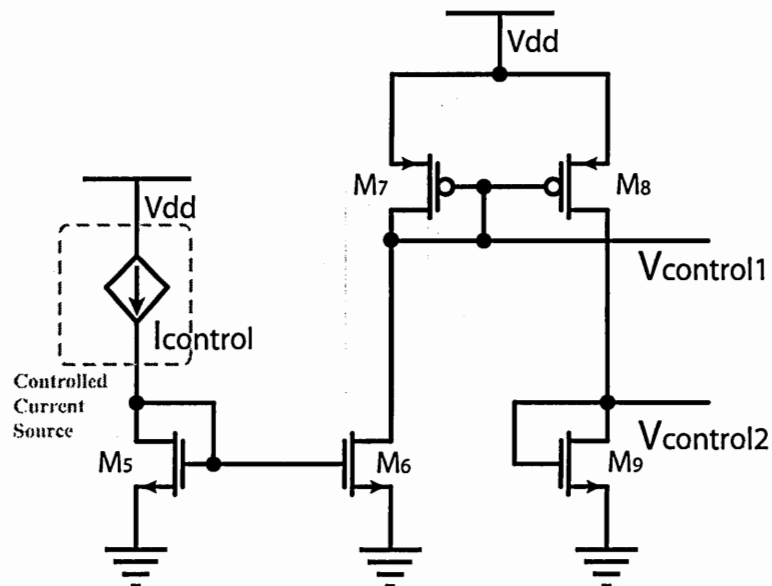


Figure 94: Current starved ring oscillator frequency control

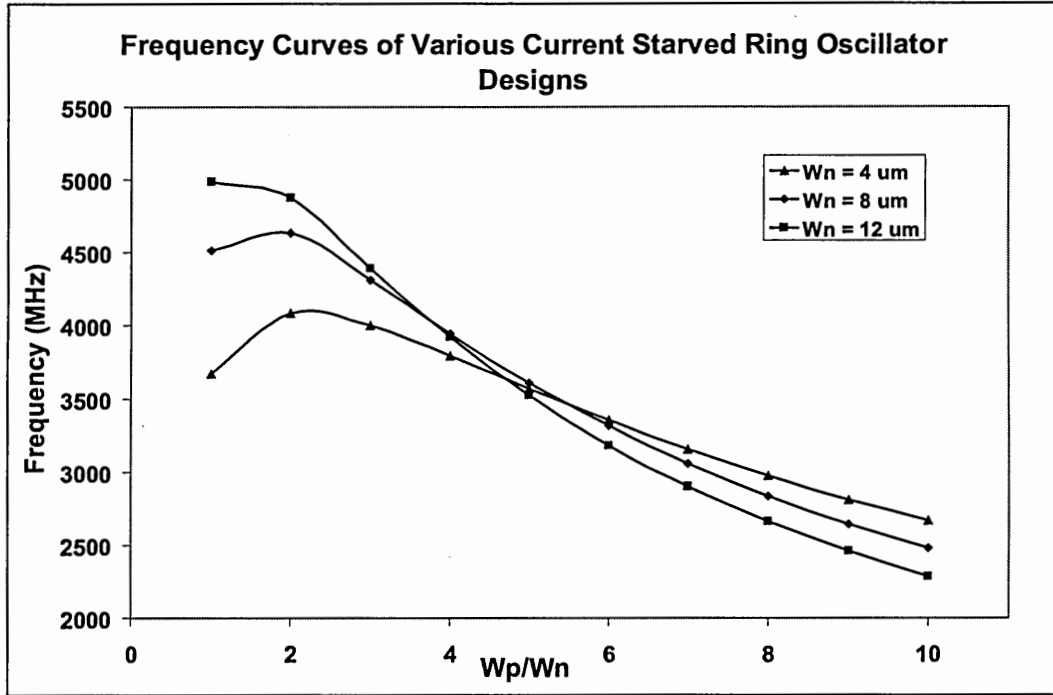


Figure 95: Current starved ring oscillator frequency vs transistor sizes

dissipated power. The sizes of M4 and M3 were selected such that they won't have a significant effect on the operation.

The current starved VCO was designed by taking these factors into account with the final transistor sizes given in Table 26. The frequency-current curve and the power dissipation-current curve of the design are provided in Figures 96 and 97 respectively. These curves show that the 3-stage current starved ring oscillator operates from 3.1 GHz up to 5.3 GHz with a power dissipation of 9-58 mW.

For the comparison of the current starved ring oscillator with the multiple-pass designs, other important parameters include the duty cycle, phase noise, and the behavior of the oscillator under parameter variations as discussed in the previous chapter. Various simulations and calculations were, therefore, performed to analyze the discussed characteristics of the current starved ring oscillator. Table 27 summarizes the characterization results and compares the current starved design with a

Table 26: Transistor sizes of the 3-stage current starved VCO

Transistor	Width	Length
M1	12 μm	0.18 μm
M2	18 μm	0.18 μm
M3	64 μm	0.18 μm
M4	128 μm	0.18 μm
M5	64 μm	0.18 μm
M6	64 μm	0.18 μm
M7	128 μm	0.18 μm
M8	128 μm	0.18 μm
M9	64 μm	0.18 μm

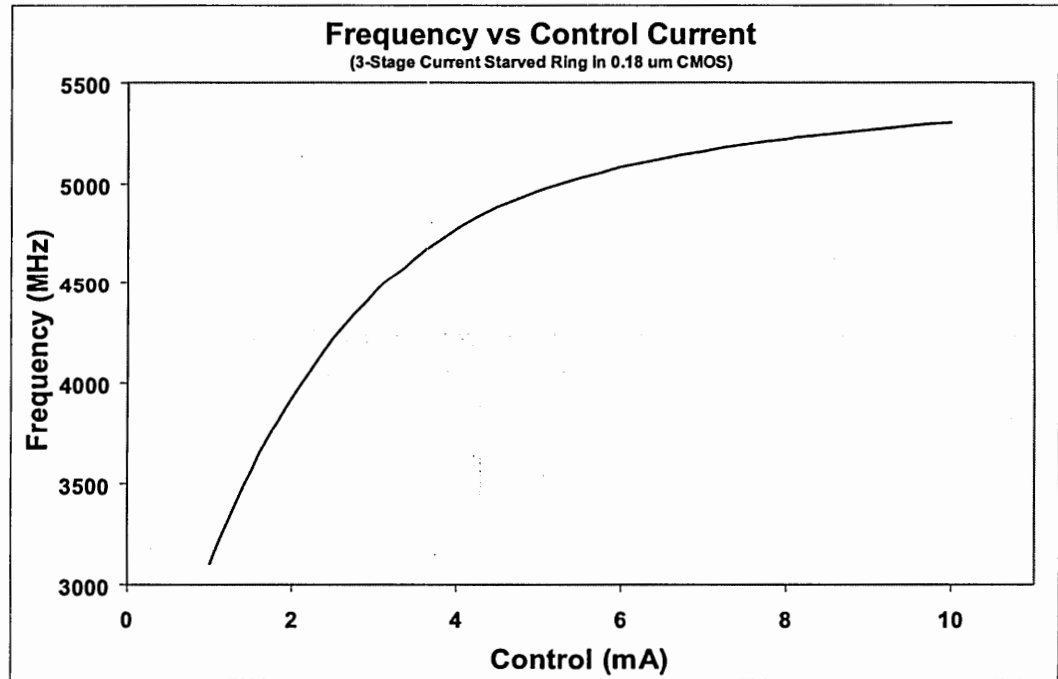


Figure 96: Current starved ring oscillator frequency vs control current curve

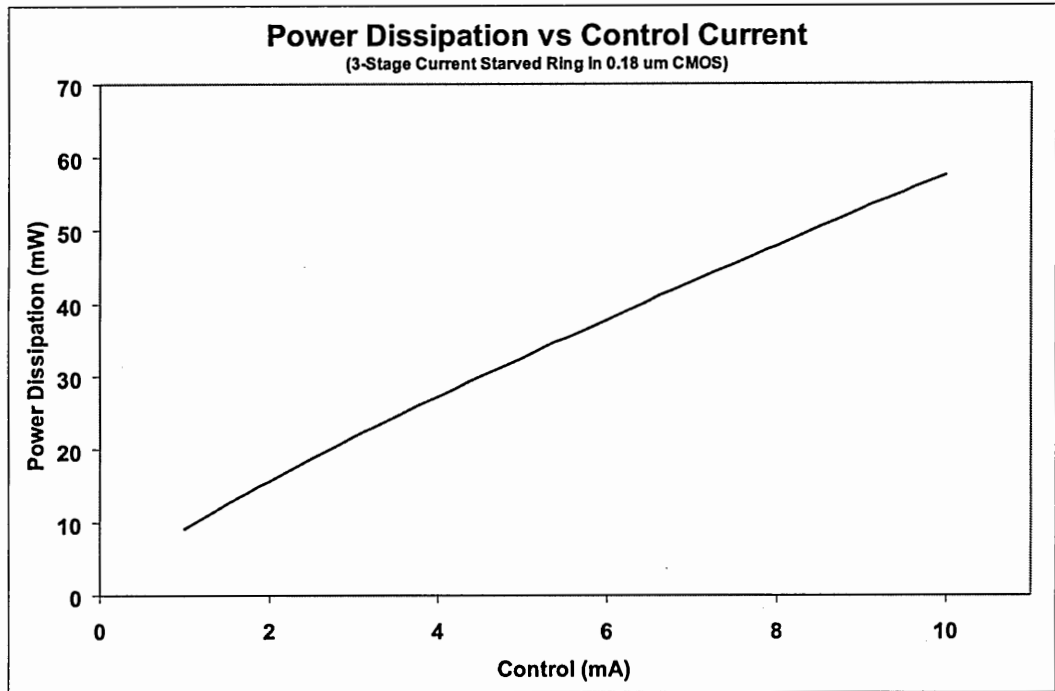


Figure 97: Current starved ring oscillator power dissipation vs control current curve

multiple-pass ring design by providing the values for both oscillators. The wide tuning range 4-stage multiple-pass ring oscillator was chosen for the comparison because it was designed in the same $0.18\ \mu\text{m}$ CMOS technology and it demonstrates a similar frequency range.

From this comparison, the main observations can be listed as follows:

- The multiple-pass design offers a greater maximum frequency when compared to the current starved design, 6.5 GHz versus 5.3 GHz, while providing a larger number of output phases with an I/Q relationship. A three-stage multiple-pass design, on the other hand, can oscillate up to 9.5 GHz in a $0.18\ \mu\text{m}$ CMOS technology. Using simple inverters instead of current starved inverters may boost the maximum frequency of a 3-stage single-loop oscillator up to 6 GHz by sacrificing control capability.
- The current starved design dissipates less power at similar frequencies owing to its single ended structure. Differential architecture of the multiple-pass design,

Table 27: Comparison of the 3-stage current starved ring design with the wide tuning range 4-stage multiple-pass ring design

Architecture	Single-loop	Multiple-Pass
Stage Structure	Current Starved Inverter	Type-I Saturated
Number of Stages	3	4
Technology, TSMC CMOS	0.18 μm	0.18 μm
Frequency Range (MHz)	3098-5295	4086-6502
Power Dissipation (mW)	9.2-57.7	59.3-88.7
Tuning Range (%)	41.5	37.2
Systematic Duty Cycle (%)	48.9	50
f_0 (MHz)	4435	5290
Δf (MHz)	1	1
Phase Noise (-dBc/Hz) simulation	95.02	104.21
Phase Noise (-dBc/Hz) calculation	95.72	105.14
Δf_0 for $0^\circ\text{C} < T < 85^\circ\text{C}$ (ppm/ $^\circ\text{C}$)	886	827
Δf_0 for corners: ss, tt, ff (%)	43.03	36.10
Δf_0 for corners: ss(85 $^\circ\text{C}$), ff(0 $^\circ\text{C}$)(%)	50.10	42.94
Δf_0 for $1.65\text{ V} < V_{dd} < 1.95\text{ V}$ (%)	13.70	24.17
Period Jitter V_{dd} sin. noise (psec)	1.1 (p-p sinus)	0.03 (glitch)
Phase Jitter V_{dd} sin. noise (psec)	3.5 (p-p sinus)	0.03 (constant)
Period Jitter Gnd sin. noise (psec)	1.5 (p-p sinus)	0.7 p-p (sinus)
Phase Jitter Gnd sin. noise (psec)	5.3 (p-p sinus)	2.2 p-p (sinus)
Period Jitter V_{dd} glitch (psec)	4.4 (glitch)	3.6 (glitch)
Phase Jitter V_{dd} glitch (psec)	4.4 (constant)	4 (decreasing)
Period Jitter Gnd glitch (psec)	13.4 (glitch)	9 (glitch)
Phase Jitter Gnd glitch (psec)	-4.6 (falling fast)	-9 (falling slow)

on the other hand, provides a perfect 50 % duty cycle in contrast to the current starved design that has a 1.1 % systematic duty cycle distortion.

- The multiple-pass design provides 9-10 dB better phase noise performance even with the 1.5 dB penalty because of the higher center frequency, 5.3 GHz versus 4.44 GHz. This is due to the saturated stage design involving a regenerative structure resulting in sharper signal transitions and increased power dissipation.
- Both designs illustrate similar behavior under ambient temperature changes, 830-890 $ppm/^{\circ}C$, although the multiple-pass design is more stable against process corner shifts, 7 % less change of center frequency. The current starved oscillator is more robust against power supply variations owing to the current controlled architecture.
- The current starved oscillator is more susceptible to power-supply/ground noise because of the single-ended structure. The difference is more pronounced for periodic noise on V_{dd} and Gnd.

7.2 *Differential Oscillator with Maneatis Loads*

A differential ring oscillator with Maneatis loads [21] is the second design that is used in this work to provide a performance benchmark for better understanding of the frequency and noise performance levels of the multiple-pass designs. A differential architecture with an analog gain stage can be designed to operate at higher frequencies when compared to a current starved design because of the reduced signal amplitudes. In addition, the use of symmetric loads as illustrated in Figure 98, named as Maneatis loads after its inventor [21], provide linear transfer characteristics promising good phase noise performance [32]. This compensates for the noise increase because of the reduction in the voltage swings. Because of these reasons, this is one of the most widely used ring oscillator stages in communications systems.

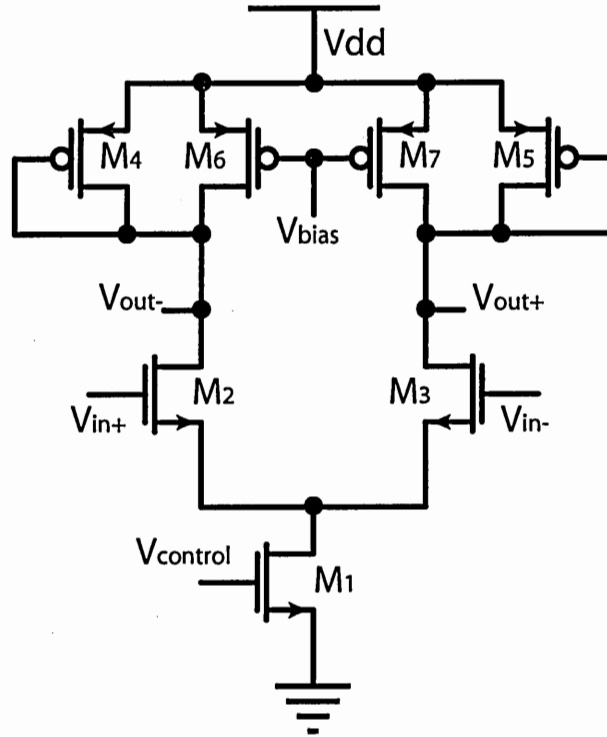


Figure 98: Differential pair with Maneatis loads

For a fair comparison of the maximum frequencies and associated noise levels, a three-stage ring oscillator with Maneatis loads was designed in a $0.18\ \mu\text{m}$ CMOS technology with an approximately same maximum power dissipation as the 9.5 GHz three-stage multiple-pass design. A basic current mirror was used to bias the circuit as shown in Figure 99. For the bias circuitry, including the current mirrors and the tail current source transistor, the general practice is to use longer gates than the minimum allowed. In the current design, bias transistors' gate lengths were chosen as $0.5\ \mu\text{m}$ to keep the common mode of the differential pair at a high resistance. Furthermore, a high mirror multiplication ratio, 8X from the bias circuit to the tail current source, was utilized to reduce the power consumption of the bias mirrors. These, along with a need for current steering capacity of $\sim 13\ \text{mA}$ resulted in extremely large transistor sizes for the tail current source transistors: $576\ \mu\text{m}$ by $0.5\ \mu\text{m}$. Aspect ratios of the differential input transistors, $W/L = 244$, and the load transistors, $W/L = 267$, also kept large enough for efficient switching of $\sim 13\ \text{mA}$ and for increasing the maximum

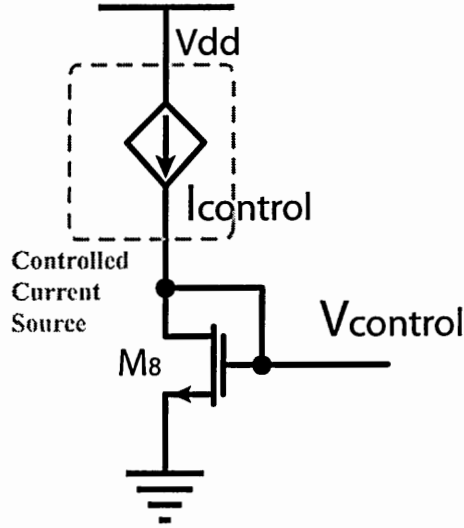


Figure 99: Maneatis ring oscillator frequency control

Table 28: Transistor sizes of the 3-stage differential VCO with Maneatis loads

Transistor	Width	Length
M1	576 μm	0.5 μm
M2	44 μm	0.18 μm
M3	44 μm	0.18 μm
M4	48 μm	0.18 μm
M5	48 μm	0.18 μm
M6	48 μm	0.18 μm
M7	48 μm	0.18 μm
M8	72 μm	0.5 μm

frequency. The final design, with the transistor sizes provided in Table 28, oscillates up to 8.57 GHz while dissipating 88.7 mW power. The maximum frequency decreases to 8.47 GHz at a power dissipation of 82.5 mW, equivalent to the three-stage multiple-pass design's maximum power dissipation.

The frequency-current and power-current curves are provided in Figures 100 and 101 respectively. These characteristics show that the Maneatis design has a linear operation range of 6.1 GHz to 7.6 GHz when the control current is varied between 0.75 mA and 1.75 mA. The output frequency gets higher with increasing input current saturating at approximately 8.5 GHz. The power dissipation in the linear range is

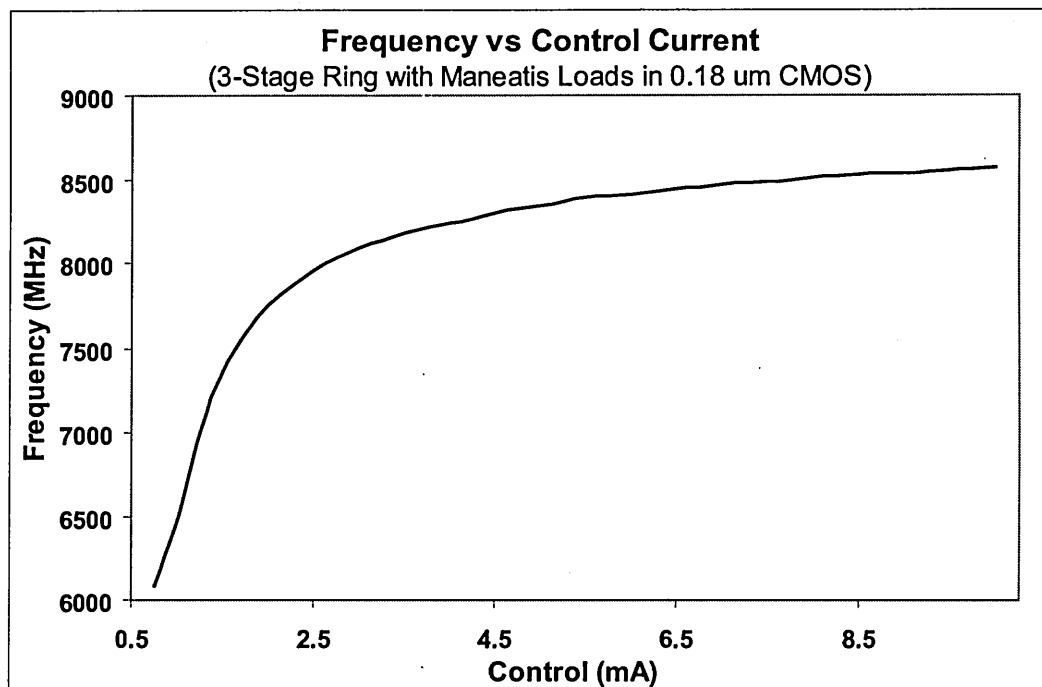


Figure 100: Maneatis ring oscillator frequency vs control current curve

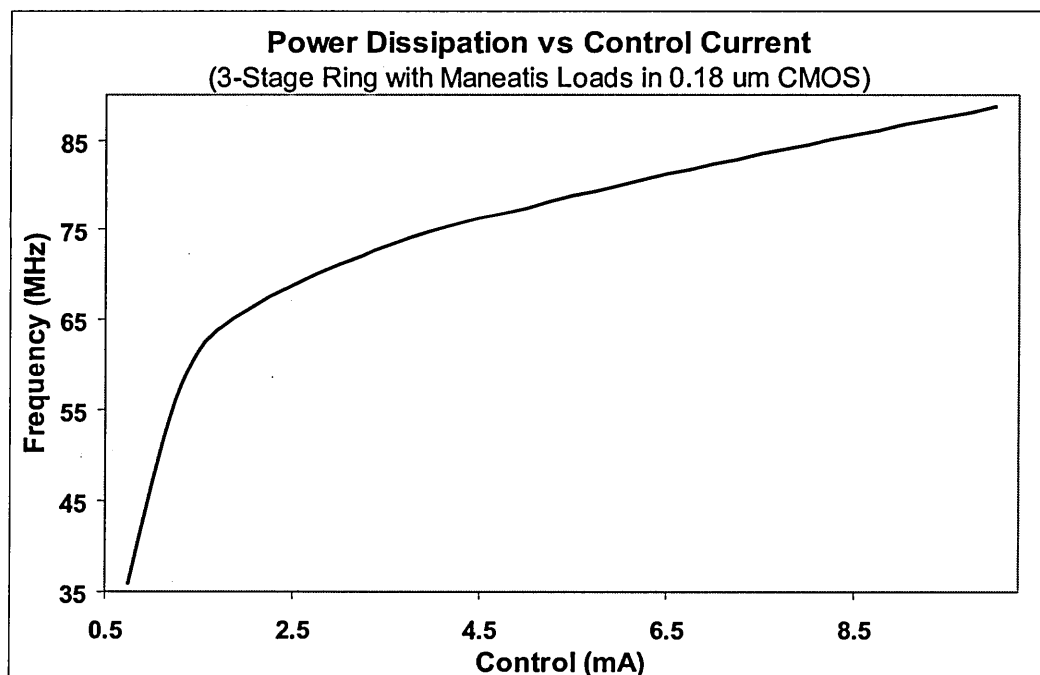


Figure 101: Maneatis ring oscillator power dissipation vs control current curve

Table 29: Comparison of the three-stage Maneatis ring design with the three-stage multiple-pass ring design

Architecture	Single-loop	Multiple-Pass
Stage Structure	Differential Pair with Maneatis Loads	Type-I Saturated
Number of Stages	3	3
Technology , TSMC CMOS	0.18 μm	0.18 μm
Frequency Range (MHz)	6083-8570	8061-9490
Linear Frequency Range (MHz)	6083-7591	8061-9490
Power Dissipation (mW)	35.95-88.68	63.05-82.08
Linear Tuning Range (%)	22.07	16.28
f_0 (MHz)	8456	9046
Δf (MHz)	1	1
Phase Noise (-dBc/Hz) simulation	89.74	99.20
Phase Noise (-dBc/Hz) calculation	88.49	98.45

36-64 mW; whereas this increases to 82.5 mW at 8.47 GHz.

From SpectreRF simulations, phase noise of the differential ring oscillator with Maneatis loads was extracted as -89.74 dBc/Hz at a 1 MHz offset from a 8.457 GHz center frequency; whereas the calculations predicted the phase noise as -88.49 dBc/Hz at the same center and offset frequencies. For the comparison of the three-stage Maneatis ring oscillator with the three-stage multiple-pass design, Table 29 was created.

These performance values displayed that a differential three-stage ring oscillator with Maneatis loads have a capacity of operating at high frequencies in a 0.18 μm CMOS, as much as 8.5 GHz, by brute-forcing it. Although signal swings are limited to ~ 600 mV, it provides good phase noise performance, -89.74 dBc/Hz at a 1 MHz offset at these frequencies forcing the limits of the technology. This is mainly due to the use of the symmetrical loads. The upper end of the linear control range, however, is limited to 7.6 GHz for the same design. The output frequency saturates after 8 GHz

but the power dissipation continues to increase suggesting that the power is not used efficiently at higher frequencies. In addition, high current steering requirement of the biasing circuitry results in extreme transistor sizes, up to $576\ \mu\text{m}$ by $0.5\ \mu\text{m}$. Because of these reasons, the use of this simple differential ring oscillator with Maneatis loads is questionable at more than 7 GHz in a $0.18\ \mu\text{m}$ CMOS process.

The three stage multiple-pass design with a saturated gain stage, however, is capable of providing frequencies as high as 9.5 GHz still staying in the linear control region. Although the stage is highly nonlinear, the use of regenerative structures and the feedforward loops increase the signal transition rates enhancing the phase noise performance considerably. The multiple-pass design, considering the 0.5 dB because of the frequency difference, provides ~ 10 dB better phase noise performance at the same power dissipation level as illustrated in Table 29. This behavior suggests that the use of a multiple-pass architecture along with a regenerative saturated stage results in more efficient use of available power at high frequencies. Furthermore, the saturated stages do not exploit a tail current source transistor thus do not suffer from extreme transistor sizes and increased noise upconversion.

7.3 Summary of the Designs

After comparing our multiple-pass ring oscillator designs with well-known ring oscillator structures, various scatter plots and tables were created summarizing the performance levels of the multiple-pass and other ring oscillator designs discussed up to this point. Figures 102, 103, and 104 include the phase noise versus center frequency, phase noise versus power dissipation, and maximum frequency versus power dissipation plots of the ring oscillators respectively. In the scatter plots, labels provide information on the number of stages (3-9), type of the oscillator (MP: multiple-pass, CS: current starved, SYM: Maneatis loads), and minimum feature size in this order. Tables 30 and 31, on the other hand, provide a more detailed comparison including

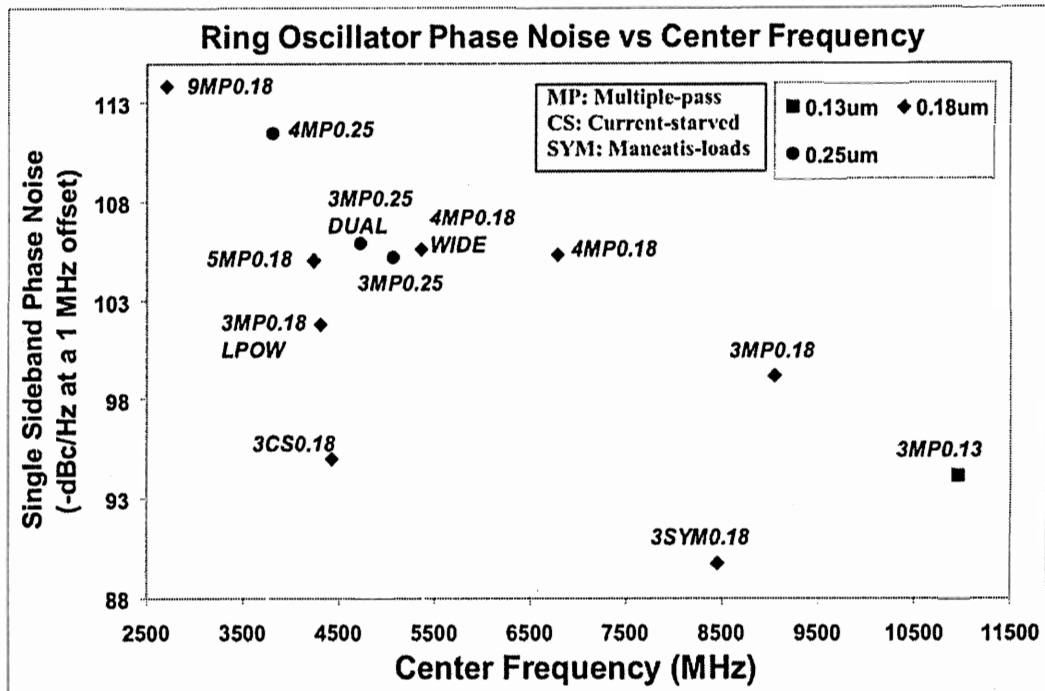


Figure 102: Comparison of the multiple-pass and other ring oscillators discussed in this work, phase noise vs frequency plot

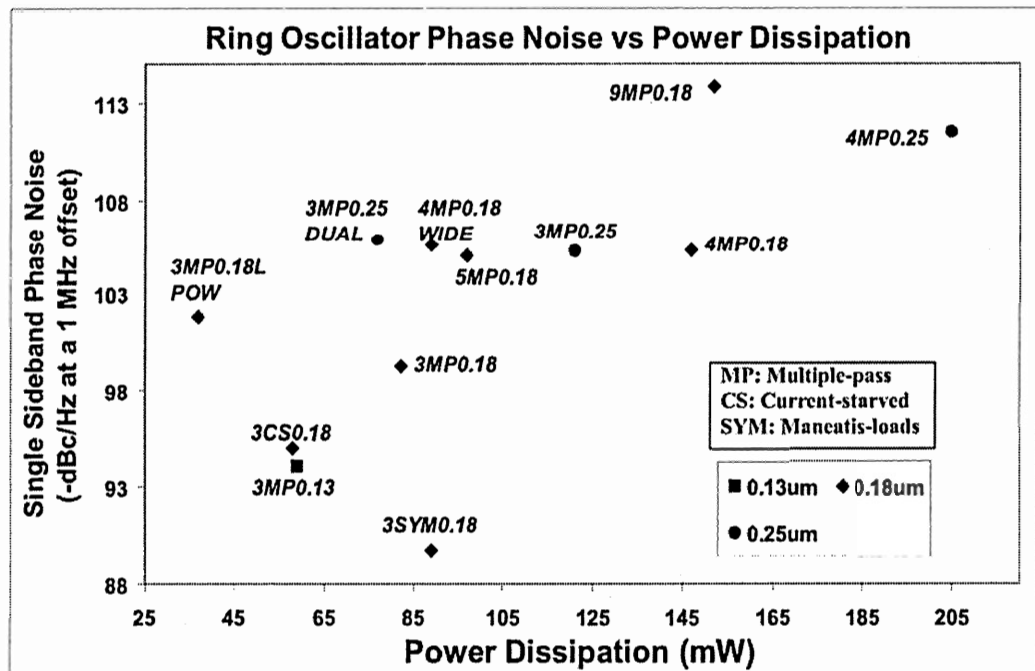


Figure 103: Comparison of the multiple-pass and other ring oscillators discussed in this work, phase noise vs power plot

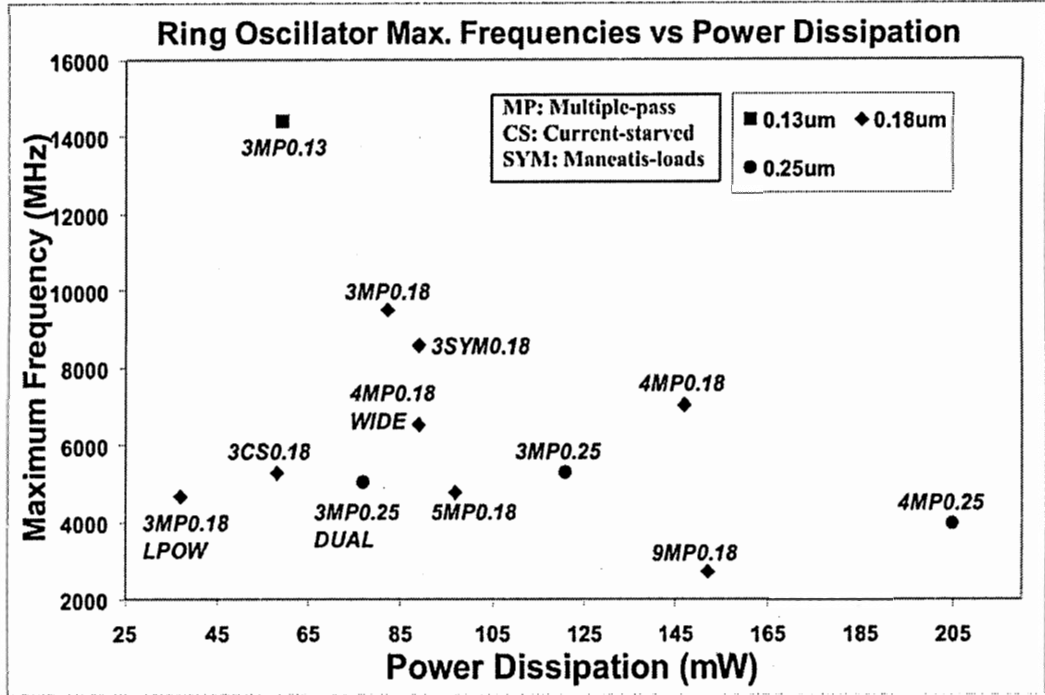


Figure 104: Comparison of the multiple-pass and other ring oscillators discussed in this work, frequency vs power plot

the VCO gains, tuning ranges, and center frequencies for the phase noise values.

From this comparison, the general trends of the proposed ring oscillator designs can be extracted as:

- Multiple-pass ring oscillators are capable of oscillating at higher oscillation frequencies than that possible by basic single-loop architectures; three-stage designs resulting in 14.4 GHz, 9.5 GHz and 5.3 GHz in 0.13 μm , 0.18 μm , and 0.25 μm CMOS respectively.
- Although the use of a simple differential stage with Maneatis loads can provide high output frequencies, up to 8.5 GHz, the noise performance suffers because of the reduction in the signal swings. Furthermore, the tail current source transistor and nonlinearity of the frequency-voltage characteristics limit the practical frequencies to about 7 GHz in a 0.18 μm CMOS.
- During the operation of the multiple-pass architecture, the on times of the

Table 30: Comparison of the multiple-pass and other ring oscillators discussed in this work - A

Label	3MP0.13	3MP0.18	3CS0.18	3SYM0.18	3MP0.25	3MP0.25DUAL
Architecture	Multi-Pass	Multi-Pass	Single-Loop	Single-Loop	Multi-Pass	Multi-Pass
Stage Structure	Type-I Saturated	Type-I Saturated	Current-Starved Inverter	Differential with Mismatch Loads	Type-I Saturated	Type-II Saturated
Number of Stages	3	3	3	3	3	3
Technology, TSMC CMOS	0.13 μm	0.18 μm	0.18 μm	0.18 μm	0.25 μm	0.25 μm
Frequency Range (MHz)	8750-14400	8061-9490	3098-5295	6083-8570	4150-5300	3750-5050
Linear Tuning Range (MHz)	8750-14400	8061-9490	3098-4712	6083-7591	4150-5300	3750-5050
(%)	49.0	16.3	41.0	22.1	24.3	29.5
VCO Gain (MHz/V)	4700	1270			720	53-77
(MHz/mA)			583	1508		
Power Dissipation (mW)	31-59	63-82	9-58	36-89	98-121	XXX
Power Dissipation per stage (mW)	10.3-19.7	21-27.3	3-19.3	12-29.7	32.7-40.3	XXX
f_0 (MHz)	10970	9046	4435	8456	5070	4727
Δf (MHz)	1	1	1	1	1	1
Phase Noise sim. (-dBc/Hz)	XXX	99.20	95.02	89.74	105.20	105.83
Phase Noise (-dBc/Hz) calculation	94.09	98.45	95.72	88.49	106.19	106.01
Phase Noise (-dBc/Hz) Scaled to 900 MHz	115.81	119.33	109.57	109.20	120.22	120.81
Q Factor	1.18	1.22	1.38	0.84	1.18	1.18
Q Factor Scaled to 900 MHz	4.13	3.88	3.08	2.61	2.80	2.71

Table 31: Comparison of the multiple-pass and other ring oscillators discussed in this work - B

Label	4MP0.18	4MP0.25	5MP0.18	3MP0.18LPOW	4MP0.18WIDE	9MP0.18
Architecture	Multi-Pass	Multi-Pass	Multi-Pass	Multi-Pass	Multi-Pass	Multi-Pass
Stage Structure	Type-I Saturated	Type-I Saturated	Type-I Saturated	Type-I Saturated	Type-I Saturated	Type-I Saturated
Number of Stages	4	4	5	3	4	9
Technology , TSMC CMOS	0.18 um	0.18 um	0.18 um	0.18 um	0.18 um	0.18 um
Frequency Range (MHz)	6190-7050	3250-3950	2780-4777	3547-4661	4112-6526	XXX
Linear Tuning Range (MHz) (%)	6190-7050 13.0	3250-3950 20.0	2780-4777 53.0	3547-4661 27.1	4112-6526 45.4	XXX XXX
VCO Gain (MHz/V)	780	440	1997	1114	2194	XXX
Power Dissipation (mW)	122-147	172-205	57-97	27-37	60-89	XXX
Power Dissipation per stage (mW)	30.5-36.8	43-51.3	11.4-19.4	9-12.3	15-22.3	XXX
f_0 (MHz)	6794	3809	4235	4313	5359	2705
Δf (MHz)	1	1	1	1	1	1
Phase Noise (-dBc/Hz) simulation	105.31	111.46	105.04	101.8	XXX	113.35
Phase Noise (-dBc/Hz) calculation	104.63	110.98	105.44	XXX	105.57	114.44
Phase Noise (-dBc/Hz) Scaled to 900 MHz	122.86	123.99	118.89	XXX	121.07	122.89
Q Factor	1.61	1.62	1.91	1.22	XXX	2.68
Q Factor Scaled to 900 MHz	4.44	3.34	4.14	3.88	XXX	4.65

primary and secondary inputs overlap creating momentary short-paths between the power bus and the ground bus. This may increase the power dissipation. Another consequence is that the earlier switching of the secondary inputs results in sharper signal transitions helping to improve the noise performance.

- In contrast to the above argument about increased power dissipation; however; in this work, it was demonstrated that when designed to use the same power, multiple-pass designs operate at higher frequencies with significantly better phase noise levels when compared to the conventional ring oscillator designs. This behavior suggests that the use of a multiple-pass architecture along with a regenerative saturated stage results in more efficient use of available power at high frequencies.
- When the phase noise values are scaled to the same center frequency, the proposed designs provide 10-12 dB better phase noise performance when compared to the conventional ring oscillator designs.
- The proposed designs demonstrate phase noise performance levels resembling their LC counterparts [11, 38, 39]. Scaling the center frequencies down to 900 MHz, for example, results in phase noise levels from -116 dBc/Hz to -124 dBc/Hz at a 1 MHz offset. The same trend can also be seen by calculating the effective Q factors, which vary between 2.80-4.65 at 900 MHz.
- In CMOS technologies, as the gate lengths are scaled down, effective Q factor of the multiple-designs improve. This is in accordance with Harjani's calculations in [6].
- In a given technology, four-stage designs offer the best phase noise performance while still providing high frequencies and output phases with an I/Q relationship. The increase in the phase noise performance is attributed to the improved

effective Q factor and relatively sharp signal transitions. When compared to the three-stage multiple-pass designs, the scaled phase noise is ~ 4 dB better, and the Q factors are larger by 0.55 at 900 MHz. The tradeoff is the power dissipation.

- Rings with more number of stages are also feasible when lower frequency designs or an increased number of output phases are crucial. The noise performance, however, does not improve in spite of the faster switching (relative to the signal period) resulting in higher V_{pp} values. This is because there are more noise sources in longer chains and nonlinearity gets worse resulting in more noise folding from harmonic frequencies. Power consumption, in addition, increases.
- Characteristics of the designs can be changed by modifying the gain stage. Increase of the feedback control switch sizes, for example, stretch the tuning range at the low frequency end. By using smaller transistor sizes, the maximum frequency and power dissipation can be controlled.
- By the use of dual frequency control paths, fine tune and coarse tune, the high voltage-frequency gain of the multiple-pass designs can be reduced, down to 53 MHz/V. This is realized by adding differentially controlled charge-pumps to the basic saturated stage that are synchronized with the primary inputs. The additional charge injected/pulled by the charge-pumps kept much smaller than the maximum charge swing at the output nodes. The additional circuitry, therefore, does not significantly effect the circuit characteristics.
- For the multiple-pass designs, the linearity of the frequency-voltage characteristics is maintained in the whole control range; whereas other designs tend to experience large gain changes.

CHAPTER VIII

EXPERIMENTAL RESULTS

This chapter explains experimental and simulation results of a prototype chip that was implemented to verify and validate the theoretical and simulation results presented in the previous chapters. The prototype chip was designed and fabricated in a non-epi TSMC 0.18 μm CMOS process with a power supply value of $V_{dd} = 1.8\text{V}$. The circuits were designed with MOSIS Scalable CMOS (SCMOS) rules that required a minimum drawn channel length of 0.20 μm , whereas the submission was in native TSMC rules. The test chip included the following parts: a three-stage multiple-pass ring oscillator, a 9-stage multiple-pass ring oscillator, an integrated LC oscillator, two different charge-pump/PFD (phase-frequency detector) designs, a new digital-type PLL, and a voltage regulator circuit. Figure 105 is a photograph of the entire chip.

Addition of an LC oscillator on the same chip allow comparisons to be made between ring oscillators and LC oscillators that are fabricated under the same conditions.

8.1 Physical Design

One of the most challenging steps during the design of sensitive and high-speed analog circuits, such as VCOs and PLLs, is the physical design, i.e. layout design. For any integrated circuit design, the theoretical calculations and schematic level simulations may display good results; without careful planning of the layout, however, the silicon output may not meet the expectations. In this work, test structures were laid out with using various advanced layout design techniques to insure that the actual circuits

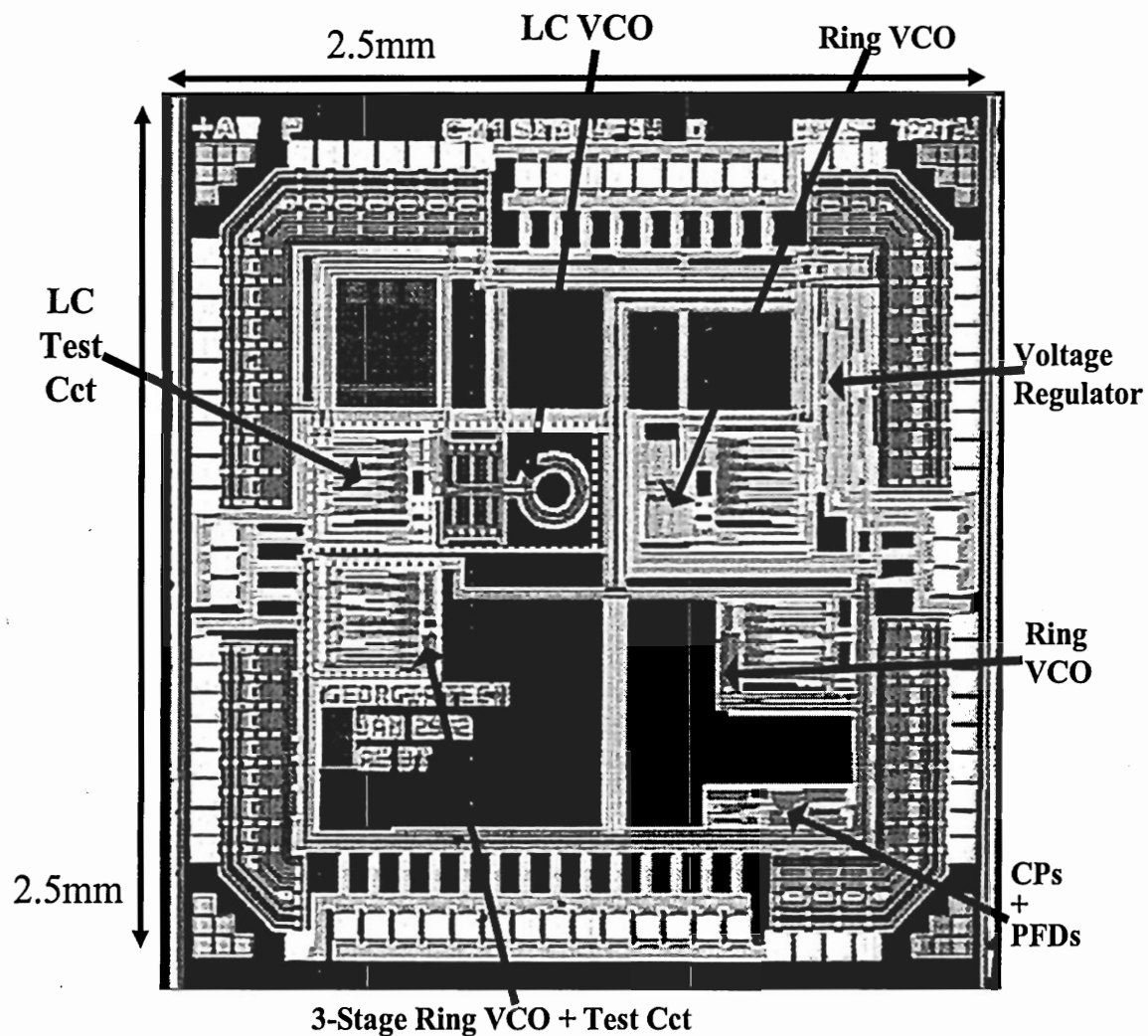


Figure 105: Photograph of the prototype chip

operate as expected. Some of these techniques include, but are not limited to, the following:

- Fingered FETs for better matching and for minimization of parasitic capacitances
- Common-centroid topology for better matching and for reduction of the fabrication-parameter gradient effects throughout the die (i.e. gradients in oxide thickness)
- Matched and minimized bus lengths to reduce phase mismatches between the stages and to decrease parasitic capacitances
- Guard-rings to prevent latch-up and for better isolation of the parts
- Multiple-vias to reduce the parasitic resistances and to increase reliability
- Electrostatic discharge (ESD) protection structures inside the custom-designed analog I/O pads

8.2 Testing Considerations

The biggest challenge in the testing of high-speed mixed-signal circuits is sending the test signals out of the die into the test equipment without upsetting the signal quality. Another problem arises when the signal frequencies reach multiple-GHz levels, the need of specialized test equipment to process these high frequency signals. To ease the requirements on the needed testing equipment and setup, therefore, high-speed current mode logic (CML) frequency dividers were used to divide the frequency of the oscillators from 1/2 to 1/64 of their actual values. Other auxiliary circuits that were designed and implemented for proper testing of the oscillators include the turn-off circuitries, buffers, differential to single-ended converters (DTOS), and the output inverter chains. The schematics of an oscillator with the typical testing circuitry is shown in Figure 106.

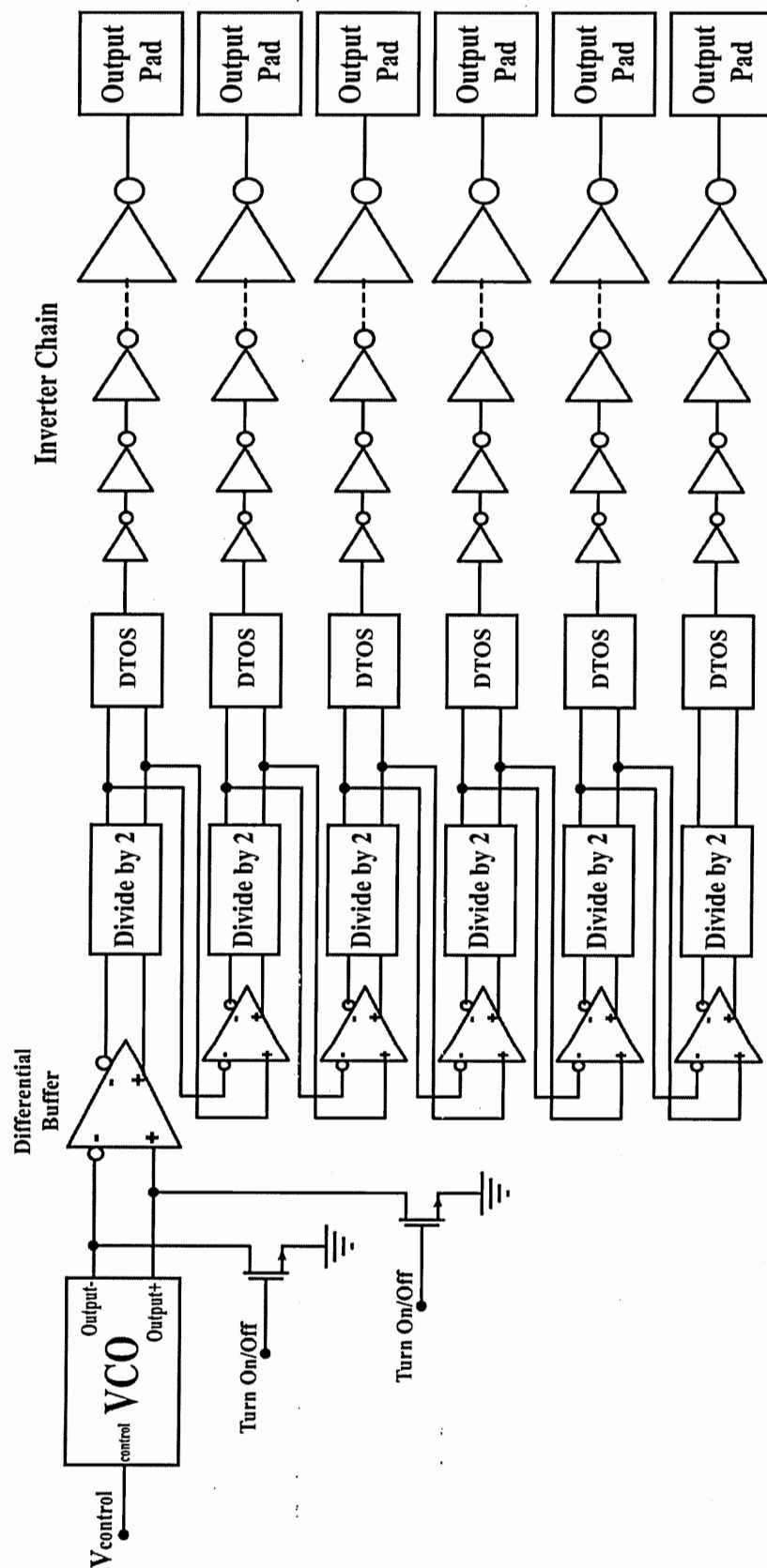


Figure 106: Auxiliary circuits for oscillator testing

On the prototype chip, all parts are both physically and electrically coupled, and the chip, therefore, is prone to strong cross-talk among the parts. The physical coupling is through the semiconducting silicon die, naturally, while the electrical coupling is mainly through the power busses. The reason of connecting the ground and power supply busses of all the components was because testing of some of the aspects of the chip required the operation of more than one part at the same time. Turn on/off option, therefore, was added to the implemented oscillators to reduce cross-talk during the separate testing of the parts. This was simply achieved by pulling the output nodes of a ring oscillator towards the ground level by using NMOS switches as illustrated in Figure 106. As will be shown shortly, the main disadvantage of this technique is the drop in the maximum frequency of the oscillator because of the additional loading.

The front-end buffers, which are connected to the outputs of the oscillators, were used to reduce the loading affect of the other testing circuitry on the oscillator. These buffers were build using a simple differential amplifier structure as shown in Figure 107.

In the oscillator testing scheme, the divider chain is connected to the output of the front-end buffer right before the DTOS structures. The divider network is constructed from six differential divide-by-two circuits, providing output frequencies from $1/2$ up to $1/64$ of the VCO running frequency. Buffers are used between divide-by-two circuits to reduce the loading effects because the dividers exhibit larger input capacitances when compared to the buffers. The divider is build by connecting a high-speed differential D-flip-flop (DFF) inside a feedback loop as shown in Figure 108, a well known architecture. A simple differential multiplexer, with the schematics given in Figure 109, is the core component of the differential master-slave DFF as illustrated in Figure 110. The simulations indicated that the divider chain is capable of operating with an input frequency of 6+ GHz.

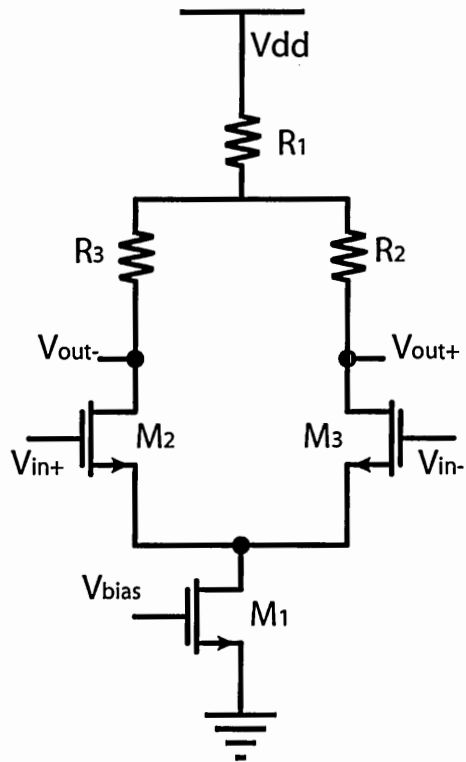


Figure 107: Front-end buffer schematics

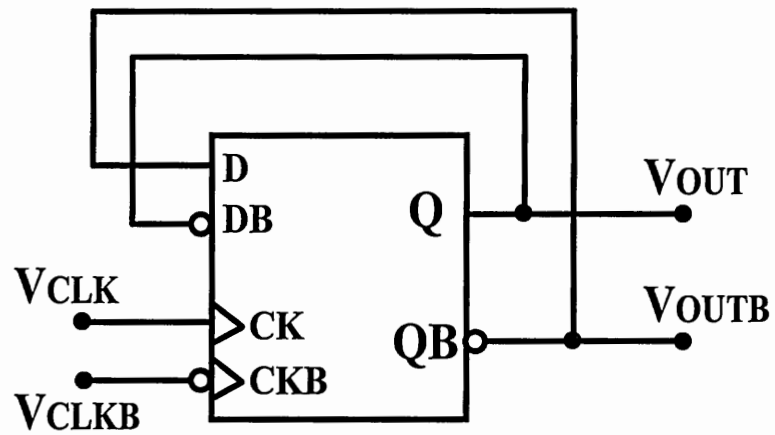


Figure 108: Divide-by-two circuit schematics

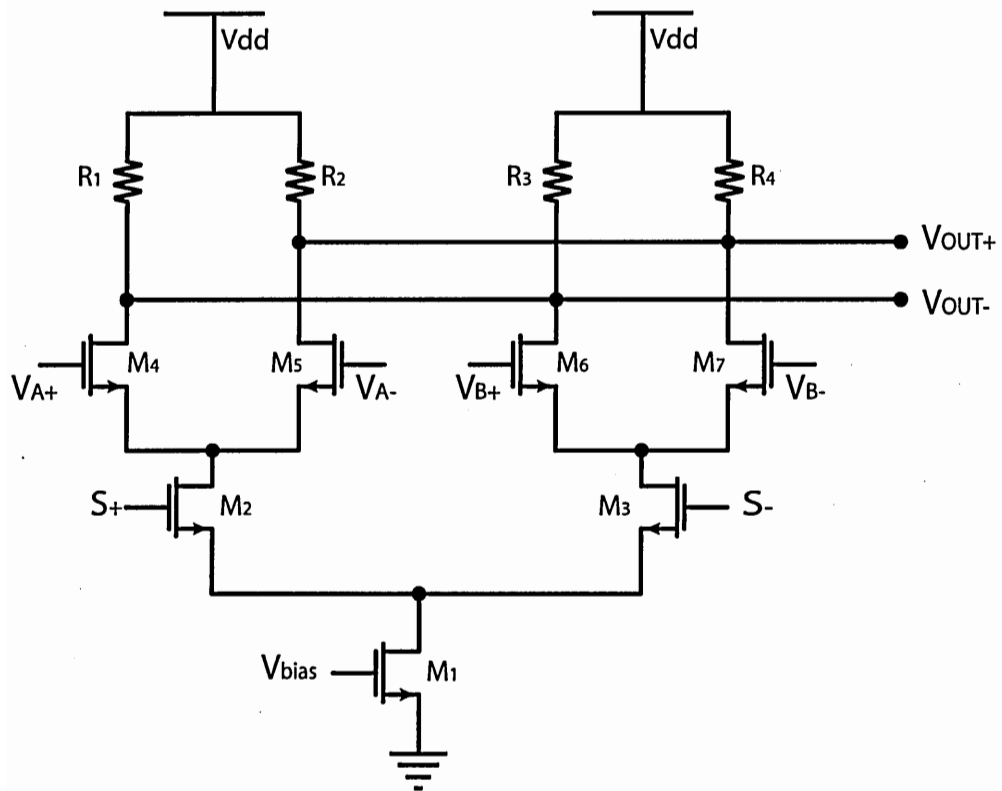


Figure 109: Multiplexer schematics

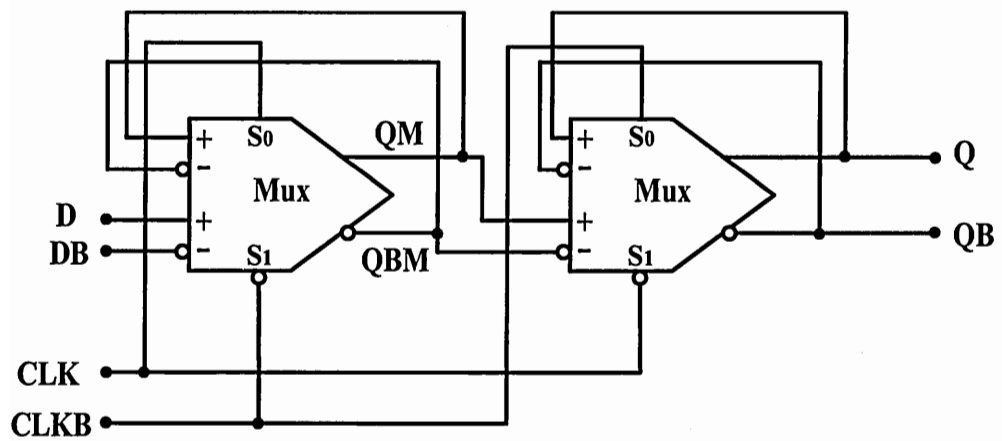


Figure 110: Differential DFF schematics

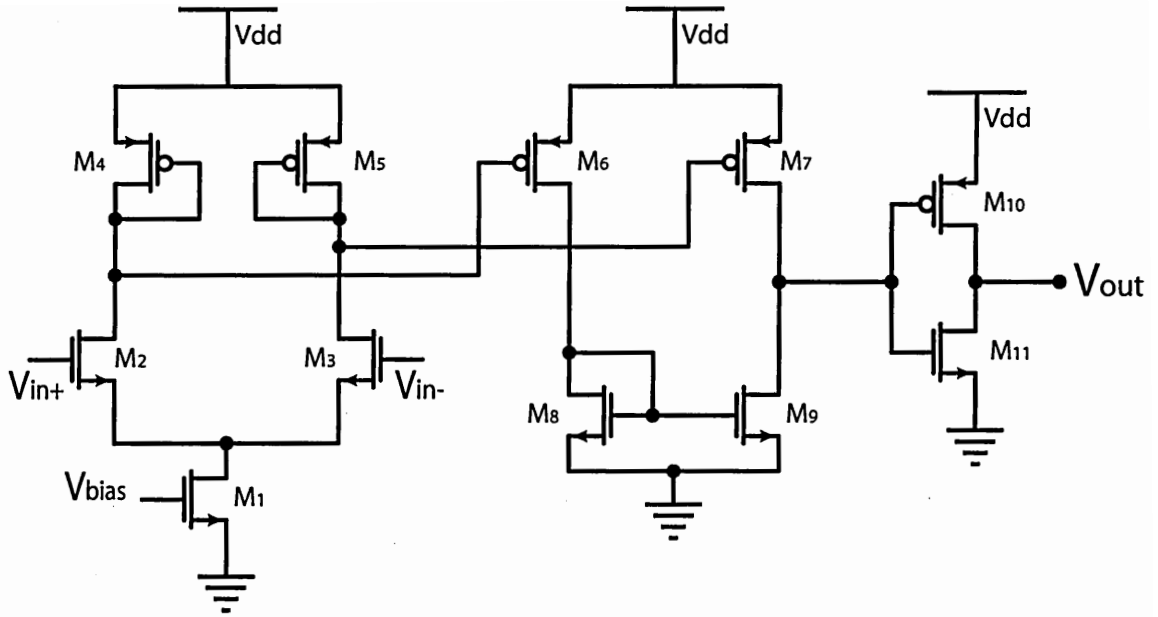


Figure 111: Differential to single-ended converter schematics

After the oscillator frequency is scaled to lower values, the DTOS circuit converts the differential signal to single-ended. This is required to simplify the testing requirements because most testing equipment do not handle differential signals. Furthermore, it is not trivial to match the skew of the differential signals because of the bus length or load mismatches. The DTOS uses a differential input pair that converts the input signal to a pair of differential current signals, which are then folded and combined to form the single-ended voltage signal, finally buffered by an inverter. This is depicted in Figure 111.

In addition to the auxiliary circuits that are discussed in this section, other circuitry were laid out for reliability/noise concerns such as the ESD protection transistors and capacitors connected to the line that provides the bias current for the dividers/buffers. Physical placement of the auxiliary circuits are given in Figure 112 for the three-stage multiple-pass ring oscillator.

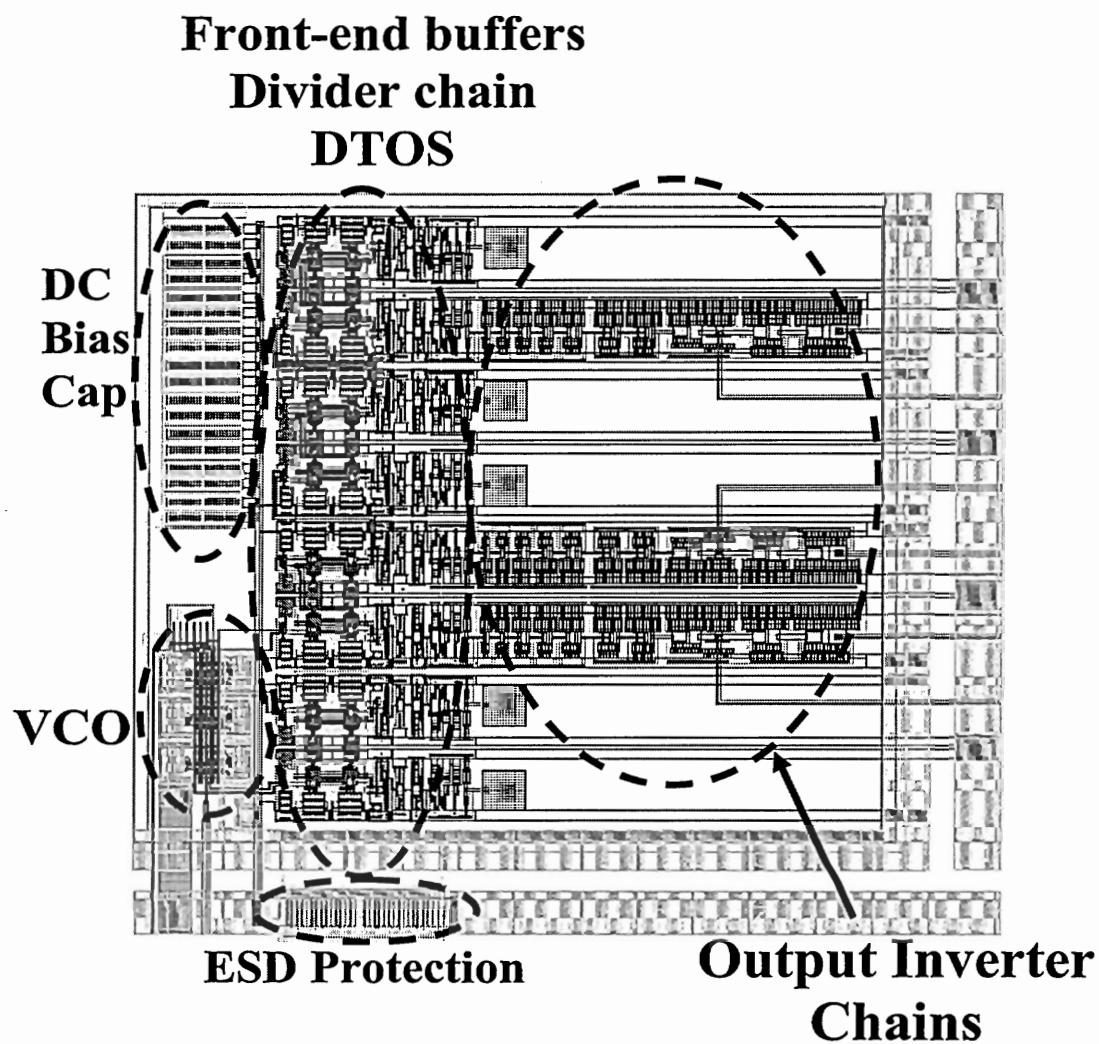


Figure 112: Layout of the three-stage multiple-pass ring oscillator with the testing circuitry

Table 32: Transistor sizes of the Type-I saturated stage used in the prototype ring oscillators

Transistor	Width	Length
M1-M2	27 μm	0.20 μm
M3-M4	0.6 μm	0.40 μm
M5-M6	36 μm	0.20 μm
M7-M8	16 μm	0.20 μm

8.3 Characterization of the Parts

This section summarizes the test results of the implemented VCOs: the three-stage multiple-pass ring oscillator, the 9-stage multiple-pass ring oscillator, and the LC oscillator.

8.3.1 Multiple-Pass Ring Oscillators Test Results

The prototype ring oscillators employ the Type-I saturated stage design with the transistor ratios provided in Table 32. The three-stage ring oscillator uses the configuration $(N, x, \text{sign}) = (3, 2, +)$ to reach the highest oscillation frequency, whereas the nine-stage network was designed to provide lower frequencies with the configuration $(N, x, \text{sign}) = (9, 2, +)$. The chip area occupied by the three-stage ring oscillator is $40 \mu\text{m} \times 60 \mu\text{m}$, and the nine-stage circuit dimensions are $60 \mu\text{m} \times 160 \mu\text{m}$; these values do not include the buffers or divide-by-N circuits. The layout of the three- and nine-stage ring oscillators are shown in Figures 113 and 114 respectively.

The performance of the three-stage multiple-pass design was simulated and measured with the results given in Figure 115. Spectre simulations of the oscillator predicted an operation range of 5.18 to 6.11 GHz as the control voltage was varied between 0.3 V to 1.8 V. The power dissipation was estimated as 38-50 mW in this range. The measured silicon output was from 5.35 GHz up to 6.11 GHz indicating a maximum difference of 3% with the simulations. Using a 2 V power supply instead of 1.8 V resulted in a maximum output frequency of 6.70 GHz. The peaking

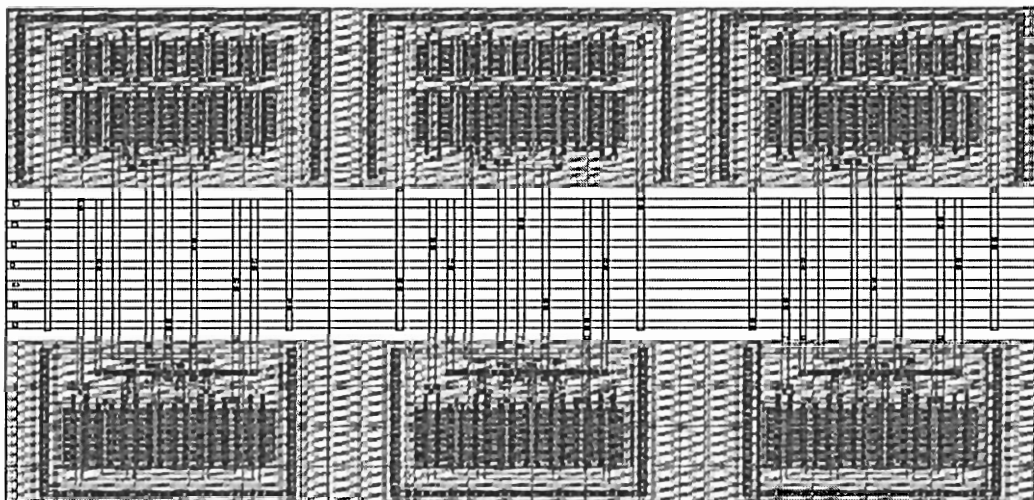


Figure 113: Three-stage multiple-pass ring oscillator layout

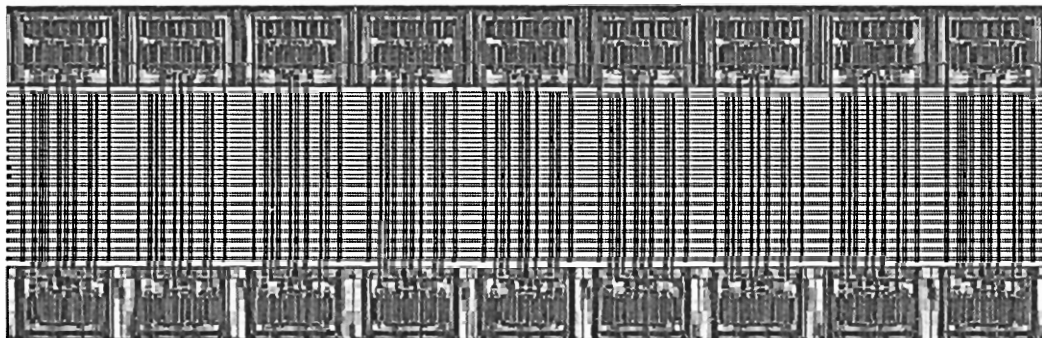


Figure 114: Nine-stage multiple-pass ring oscillator layout

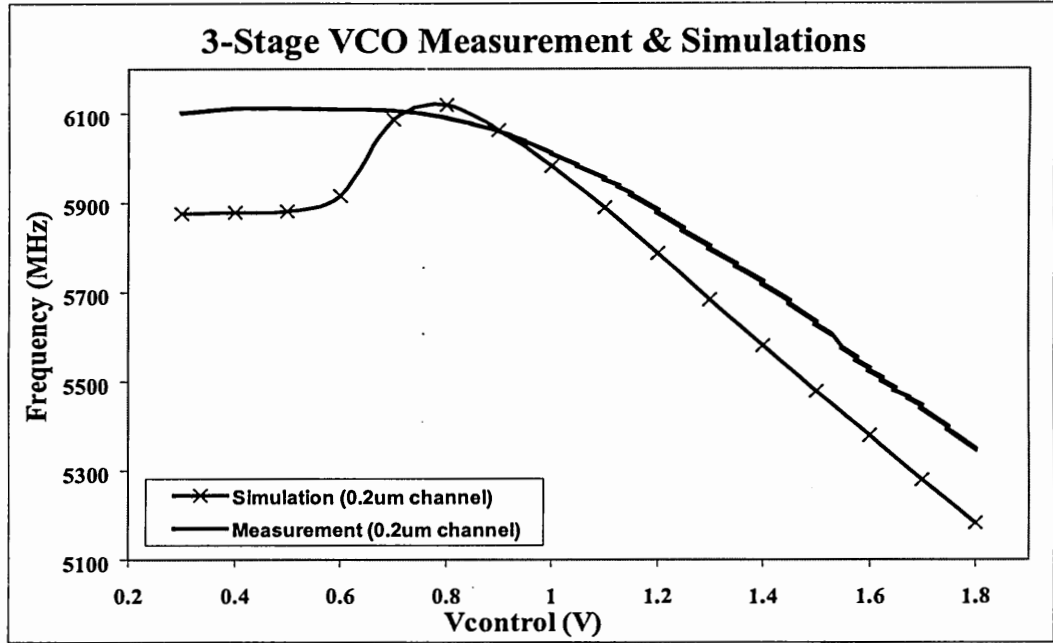


Figure 115: Three-stage multiple-pass ring oscillator characterization - I

of the simulated characteristics is attributed to the limitations of our simulator tool in modelling the transistors in the subthreshold region. Removing the test circuitry and reducing the drawn channel length from $0.20 \mu\text{m}$ to $0.18 \mu\text{m}$ predicts a maximum oscillation frequency of 7.7 GHz as shown in Figure 116. This is a 26% increase over the maximum frequency of the fabricated design.

As in the three-stage network, the multiple-pass architecture for the nine-stage design is implemented by connecting the secondary inputs of a stage to the outputs of a stage that is two stages before the delay stage, thus the configuration $(N, x, \text{sign}) = (9, 2, +)$. The frequency-voltage curves shown in Figure 117 were extracted from simulations and measurements and show good agreement with a maximum difference of 4%. The simulated oscillator frequencies were between 1.16 GHz and 1.93 GHz when control voltage was varied from 0.3 V to 1.8 V. The use of additional gain stages increased the power consumption to 92-112 mW within the control range. The measured silicon output was from 1.1 GHz up to 1.86 GHz in the same control range. The frequency-voltage curves exhibited linear characteristics for a control range of

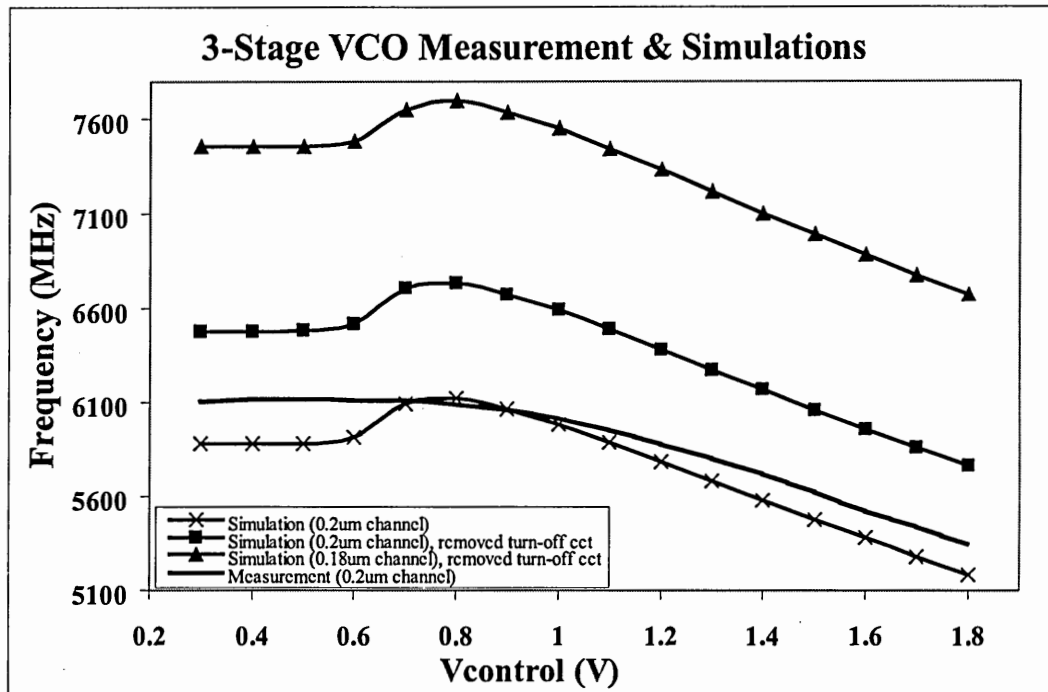


Figure 116: Three-stage multiple-pass ring oscillator characterization - II

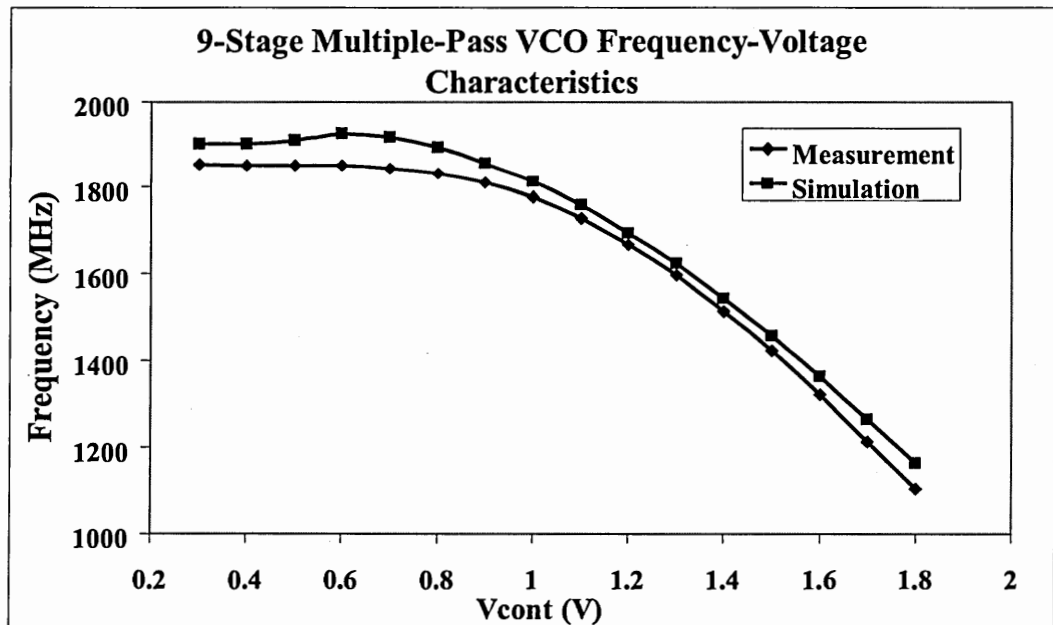


Figure 117: Nine-stage multiple-pass ring oscillator characterization

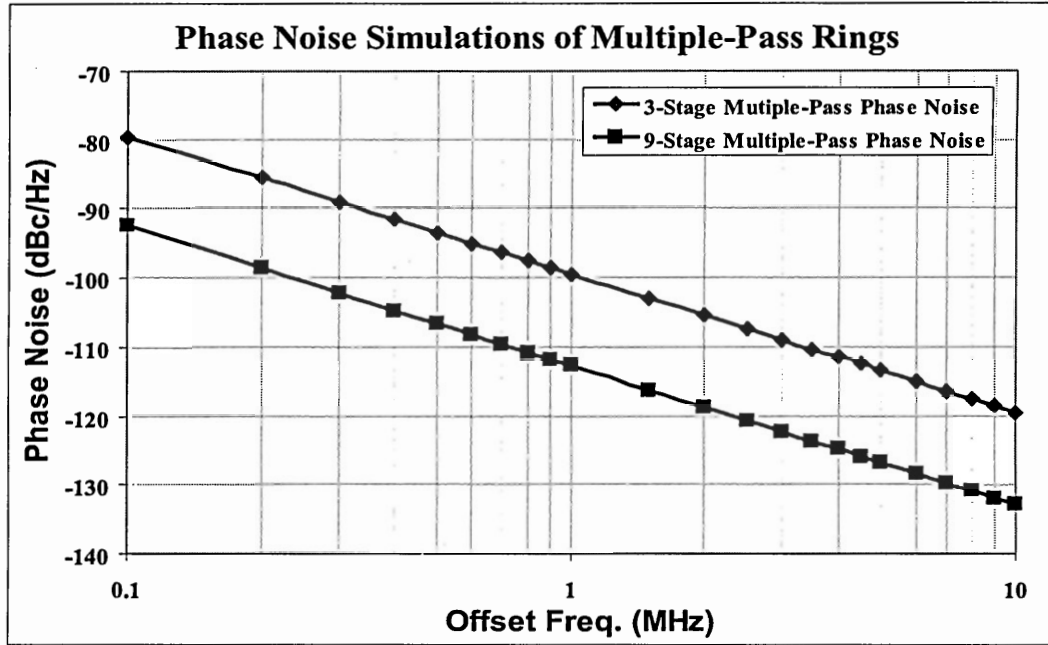


Figure 118: Phase noise simulation results of the implemented multiple-pass ring oscillators

0.9-1.8 V. It should be noted that frequency range of a multiple-pass architecture does not scale linearly with the number of stages. Hence, the frequency relation of these oscillators is different than the three times difference that one would expect.

The phase noise values were estimated using SpectreRF simulations and Equation (59) with excess noise factor F defined as in Equation (105). As illustrated in Figure 118, simulations predicted the phase noise of the three-stage design as -99.5 dBc/Hz at a 1 MHz offset from a 5.79 GHz center frequency, whereas the value for the nine-stage design was -112.84 dBc/Hz at a 1 MHz offset from a 1.82 GHz center frequency. Using Equation (106), phase noise of the three- and nine-stage multiple-pass ring oscillators were calculated to be -99.40 dBc/Hz and -113.77 dBc/Hz respectively at the same offset and center frequencies as given in the simulation results. The simulations and calculations agree well within 1.1 dB.

Figure 119(a) shows the measured power spectrum (PS) at the divide-by-four output of the three-stage ring oscillator, whereas Figure 119(b) gives the PS at the

divide-by-two output of the nine-stage design. From this data, phase noise of the ring oscillators can be found using the formula

$$L(\Delta\omega) = SB - 10\log(RBW) - 20\log(\Delta\omega/\Delta\omega_{meas}) + 20\log(\omega_0/\omega_{out}), \quad (109)$$

where $L(\Delta\omega)$ is the single sideband phase noise, SB is the measured sideband level with respect to the carrier, RBW is the resolution bandwidth of the spectrum analyzer, $\Delta\omega$ is the desired angular frequency offset from the oscillator center frequency ω_0 , and $\Delta\omega_{meas}$ is the angular frequency offset from the measured center frequency ω_{out} at which the sideband levels are measured.

Using Equation (109), single-sideband phase noise of the three-stage design was extracted as -97.5 dBc/Hz at a 1 MHz offset from a 6.08 GHz center frequency. Phase noise of the nine-stage ring oscillator, on the other hand, was found to be -105.5 dBc/Hz at a 1 MHz offset from a 1.81 GHz center frequency.

For the comparison of the estimated and measured phase noise values it is important to consider the effect of the testing circuitry on the phase noise. Whereas the phase noise was measured at the output of the testing circuitry, that is after the output of the oscillators are divided and buffered, the quoted phase noise estimations are given for the actual outputs of the oscillators.

The effect of the buffers can be considered minimal because there is no integration of the jitter in the stand-alone buffers as in the ring oscillator loop and only cycle-to-cycle jitter is important due to the lack of a reference. The digital inverters of the buffer chain, furthermore, have rail-to-rail signal levels improving the SNR of the signals and CMOS inverters are known to have much better phase noise performance when compared to the phase noise levels of the discussed oscillators with noise contribution of the larger inverters being smaller [40].

As for the frequency dividers, there are two issues that needs to be considered: additional noise of the dividers and the spectrum transformation resulting because of the frequency translation. Previous work on frequency dividers, including ECL

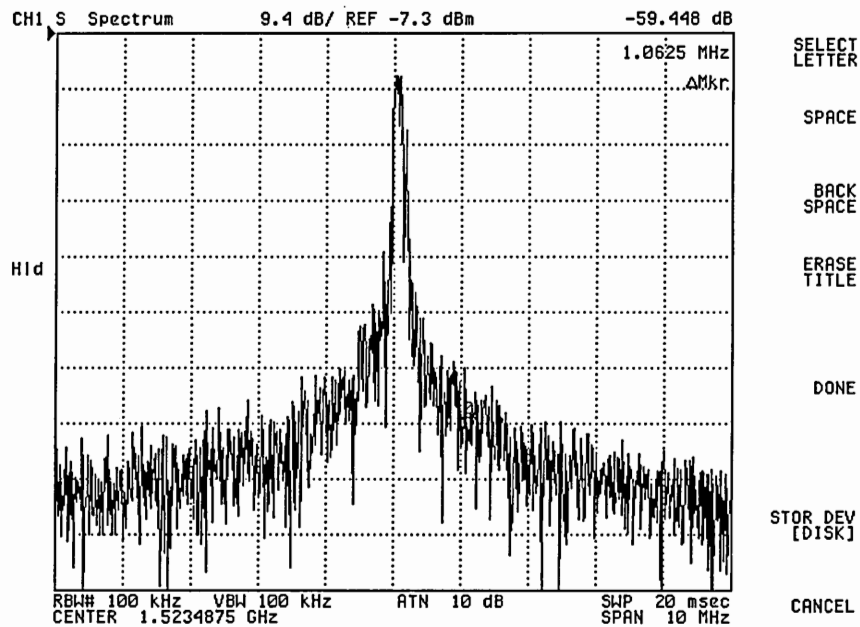
and TTL dividers [41] as well as CMOS dividers based on DFFs [42], estimates that divide-by-two circuits exhibit -127 to -139 dBc/Hz phase noise at a 1 MHz offset from a 2 GHz operating frequency, while the phase noise is approximately -122 to -130 dBc/Hz at a 1 MHz offset from a 6 GHz operating frequency. Comparison of these values with the estimated phase noise of the three- and nine-stage ring oscillators show that these values are 15-20 dB lower than the internal noise of the VCOs. Considering that there are only one (nine-stage) or two (three-stage) dividers used for phase noise testing, noise contribution of the divider chain can be assumed negligible. Frequency translation because of the frequency division, on the other hand, has already been taken into account in Equation (109) such that phase noise drops by 20 dB/decade at lower oscillation frequencies.

For confirming the above estimations, phase noise was probed both at the oscillator outputs and the testing circuitry outputs in further SpectreRF simulations. According to these results, the dividers and the buffers have negligible contribution to the output phase noise.

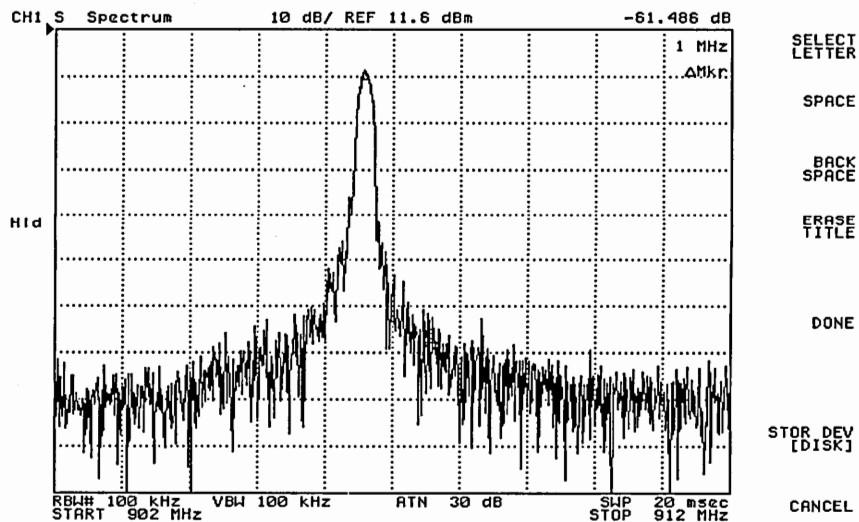
Table 33 summarizes the phase noise results. Power-supply/ground disturbances, flicker noise sources, and cross-talk among the frequency divider outputs are considered to be the main sources of the difference between the measurements and the estimations. The large discrepancy between the estimations and the measurements of the nine-stage oscillator phase noise is attributed to the non-symmetrical turn-off circuitry connections for this particular design.

8.3.2 LC Oscillator Test Results

The architecture of the implemented LC oscillator is based on the symmetrical LC design [13] that uses both NMOS and PMOS latches to realize the negative resistance. When compared to conventional LC designs, this structure promises lower power dissipation because of the current reuse [43], and better noise performance [44]. The



(a)



(b)

Figure 119: Measured power spectrum at the (a) divide-by-four output of the three-stage ring oscillator (b) divide-by-two output of the nine-stage ring oscillator

Table 33: Phase noise of ring oscillators extracted from measurements, simulations and calculations at 1 MHz offset from center frequencies

Ring Oscillator	3-stage	9-stage
Simulations		
f_0 (GHz)	5.79	1.82
Phase Noise (dBc/Hz)	-99.5	-112.84
Calculations		
f_0 (GHz)	5.79	1.82
Phase Noise (dBc/Hz)	-99.4	-113.77
Measurements		
f_0 (GHz)	6.08	1.81
Phase Noise (dBc/Hz)	-97.5	-105.5

circuit, which is given in Figure 120, has been modified by adding a tail current-source transistor to have better control over the output characteristics. Note, however, that this may worsen the noise performance by increasing the flicker noise terms and by inserting low-frequency multiplicative noise components [8].

Thick top metal of the TSMC Mixed-Mode (MM) process was used to realize an inductor with a low series-parasitic-resistance. The three-turn circular inductor shown in Figure 121 has an outer radius of $113 \mu m$, and is designed for a 2.4 nH inductance using the equations given in the TSMC manuals [45]. This yielded a total coil length of 1.7 mm, and a width of $15 \mu m$. For these design parameters, series parasitic resistance was found as 2Ω . TSMC data on previously fabricated inductors [45] in this process show that Q factor of the implemented inductor is close to 9.5. In the fabrication of the prototype chip, however, the center area of the inductor was filled with dummy metal and poly layers by MOSIS for meeting chemical-mechanical-polishing (CMP) specifications. The actual Q factor, therefore, is expected to be less than this value.

The VCO uses metal-insulator-metal (MiM) capacitors along with junction varactors to control the frequency. Both NMOS and PMOS varactors are used for differential fine tuning [13]; whereas MiM capacitor banks are used at each side for 8-bit

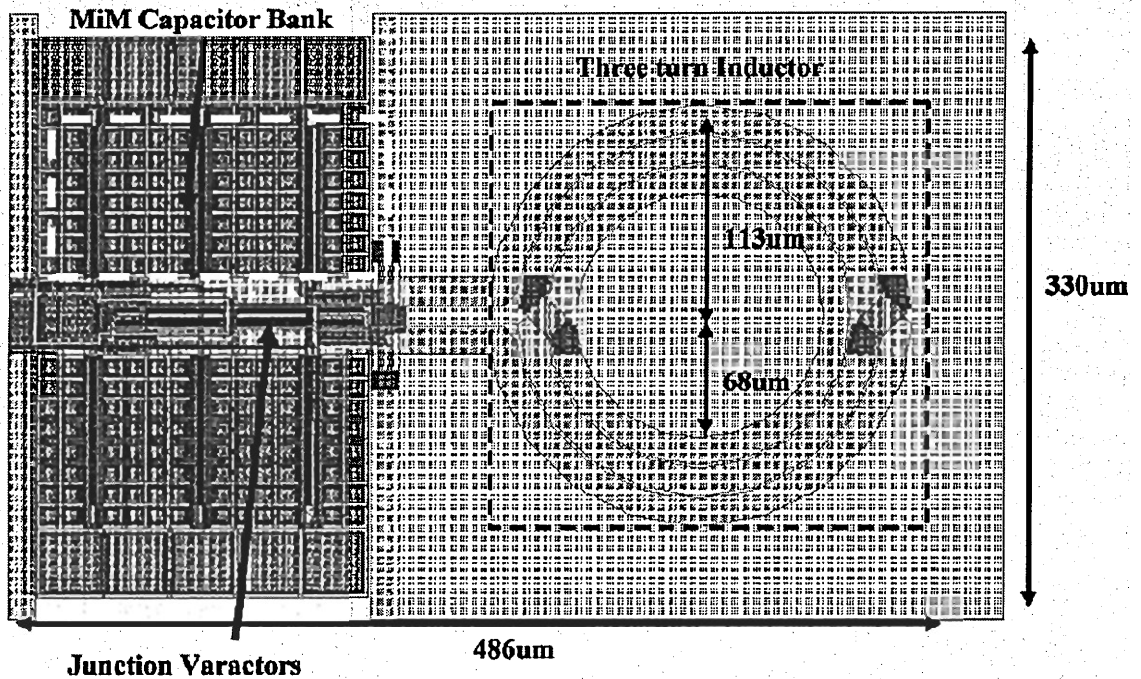


Figure 121: Inductor layout

digital coarse tuning. Proportionally sized NMOS transistors are used to switch the capacitor banks on/off. This is known as switched tuning [46].

A coarse and a fine control path are used to tune the frequency by varying the amount of output capacitance. SPICE simulations of the LC oscillator predicted an operation range of 2.03 GHz to 3.53 GHz as demonstrated in Figure 122. In this plot, various curves correspond to different digital words used for coarse-tuning; some of the curves are excluded for clarity. According to the simulated frequency-voltage curves, the coarse tuning range was 60% whereas the fine tuning range varied between 3.6% and 14.2%. As shown in Figure 123, the measured silicon output was from 1.89 GHz to 3.05 GHz indicating a maximum difference of 16.9% with the simulations. This difference is attributed to the parasitic line and transistor capacitances that were not included in the simulation models. From the measurements, the coarse tuning range was found to be 42.7% whereas the fine tuning range was between 2.7%, in the low frequency end, and 8.9%, in the high-frequency end. Power dissipation was estimated

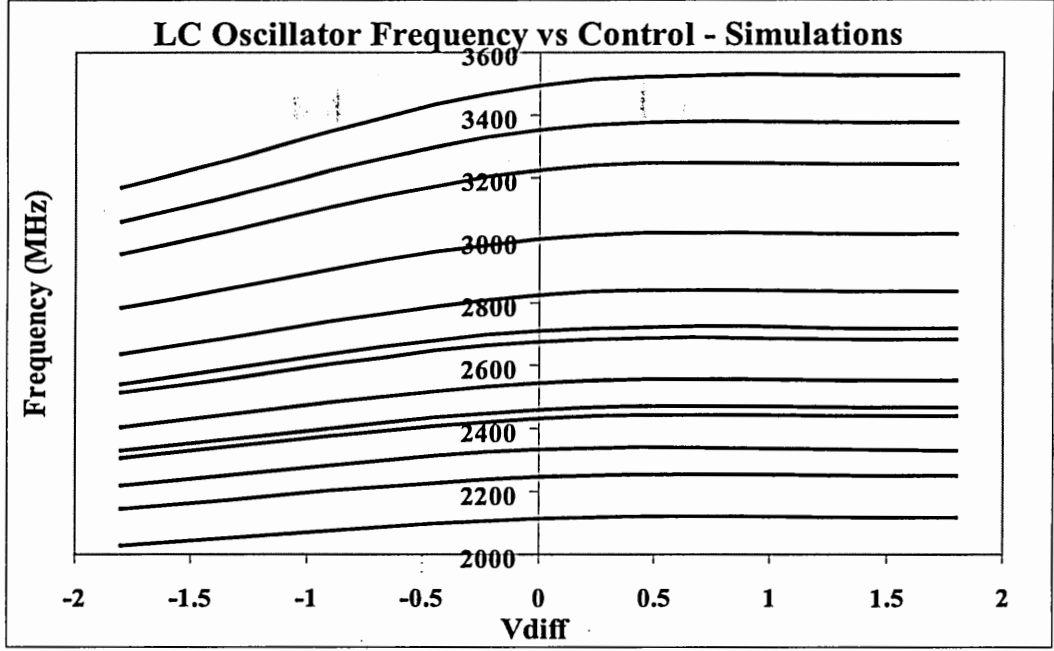


Figure 122: LC oscillator frequency-voltage curves extracted from simulations

as 3.6 mW for a bias current I_{bias} of 2 mA.

Figure 124 illustrates the measured power spectrum at the divide-by-16 output of the LC oscillator. According to this measurement, this output exhibits a sideband level of -65.37 dB with respect to the carrier at a 10 kHz offset from the 157 MHz center frequency. From this data, phase noise of the LC oscillator was computed as -111.37 dBc/Hz at a 1 MHz offset from a 2.51 GHz center frequency.

In Table 34, we compare the measured phase noise and maximum frequencies of the implemented VCOs. Published multi-GHz ring designs are also included to represent the state-of-the-art. In addition to the phase noise of the oscillators at their center frequencies, phase noise values scaled to a 900 MHz center frequency and figure-of-merit (FOM) values are also provided for a fair comparison of the oscillator performances. The standard FOM definition [13], given as

$$FOM = L(\Delta\omega) + 10\text{Log}\left(\left(\frac{\Delta f}{f_0}\right)^2 P_{VCO}(mW)\right), \quad (110)$$

is used for the LC oscillators; whereas a modified FOM is used for ring oscillators by

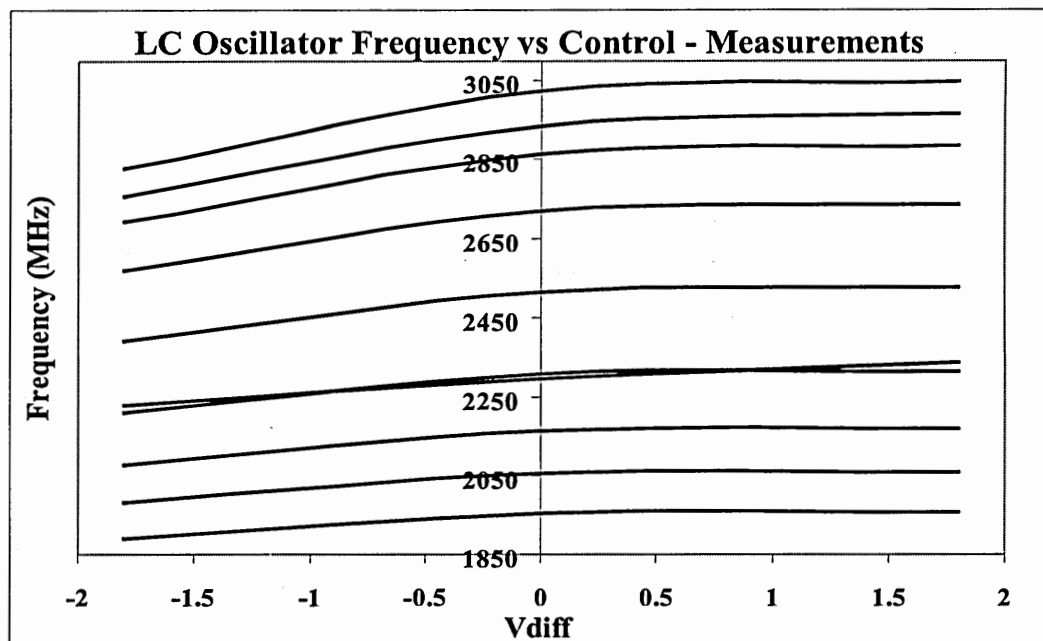


Figure 123: LC oscillator frequency-voltage curves extracted from measurements

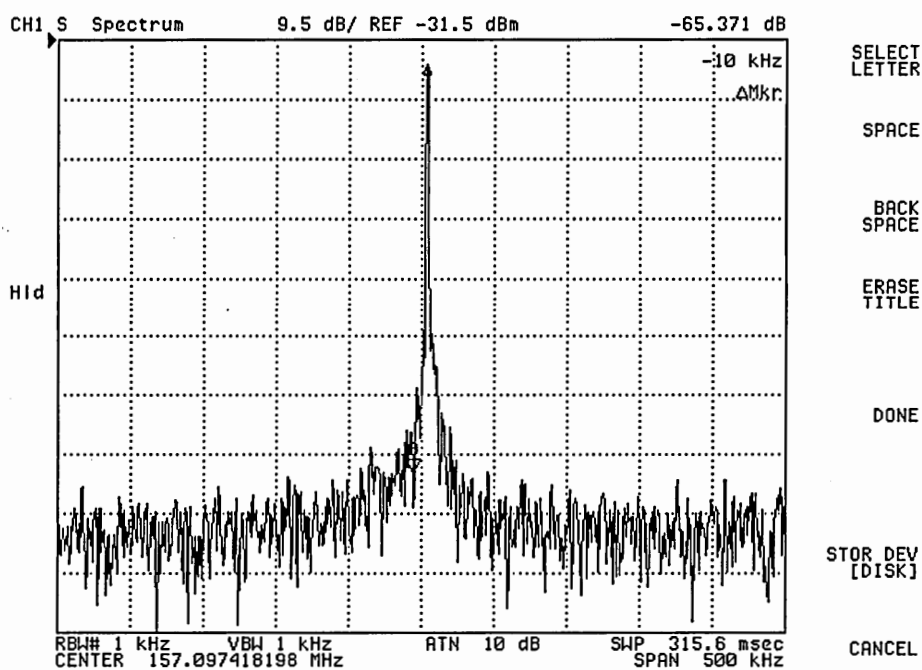


Figure 124: Measured power spectrum at the divide-by-16 output of the LC oscillator

linearly scaling the power dissipation to an oscillation frequency of 1GHz, i.e.

$$FOM = L(\Delta\omega) + 10\text{Log}\left(\left(\frac{\Delta f}{f_0}\right)^2 P_{VCO}(mW) * \frac{1GHz}{f_0}\right). \quad (111)$$

This is because higher frequency ring VCOs naturally dissipate more power. In these equations, $P_{VCO}(mW)$ is the power dissipation of the VCO in mili-watts at its center frequency. Lower values of FOM corresponds to better noise performance.

The results show that, when fabricated under similar conditions, introduced ring oscillators are capable of providing phase noise levels comparable to LC oscillators. This is obtained at the expense of increased power dissipation explaining the difference in the FOMs. Although wireless transceivers require the circuits to operate at low power levels, wired transceivers have more relaxed power requirements. Introduced designs, therefore, may replace LC oscillators in wired transceiver applications such as Gigabit Ethernet, 10 Gigabit Ethernet, SONET, etc.

8.4 PLL Test

In this chapter, we demonstrated the proper operation of the proposed ring oscillators by providing measurement results for three- and nine-stage rings. Test results of an LC oscillator, which was implemented on the same die, was also given so that performance values of different architectures can be compared. The output frequency of a standalone VCO, however, cannot be precisely controlled unless the VCO is employed in a feedback control loop, i.e. a PLL. Most high performance communications systems, therefore, use the VCO in a PLL to better control the output frequency. Moreover, meeting the noise specifications of some of the systems, such as Gigabit Ethernet, requires the close-in phase noise suppression capabilities of a PLL.

Because of these reasons, in this work, we constructed various charge-pump PLLs with the implemented oscillators to show the operation of our circuits in a practical system. The prototype chip was initially designed for this purpose by the addition of the other parts that are used in the construction of a PLL. These include a differential

Table 34: Phase noise comparison of implemented and previously published VCOs (at 1 MHz offset)

VCO	3-stage ring	9-stage ring	LC	[15]	[19]	[47]
Technology, CMOS (μm)	0.18	0.18	0.18	0.18	0.25	0.18
Minimum Feature Size (μm)	0.20	0.20	0.18	0.18	0.25	0.18
Power Supply (V)	1.8 (2.0)	1.8	1.8	1.8	2.5	2.0
f_{max} (GHz)	6.11 (6.70)	1.86	3.05	9.00	5.43	6.10
f_0 (GHz)	6.08	1.81	2.51	5.00	5.43	5.00
Phase Noise (dBc/Hz)	-97.5	-105.5	-111.4	-82.0	-98.5	-85.0
Phase Noise (dBc/Hz) scaled to 900 MHz	-114.12	-111.5	-120.3	-96.89	-114.11	-99.89
Power Dissipation (mW)	50	112	3.6	135	80	80
FOM (dBc/Hz)	-164.1	-152.7	-173.8	-144.2	-161.5	-147.8

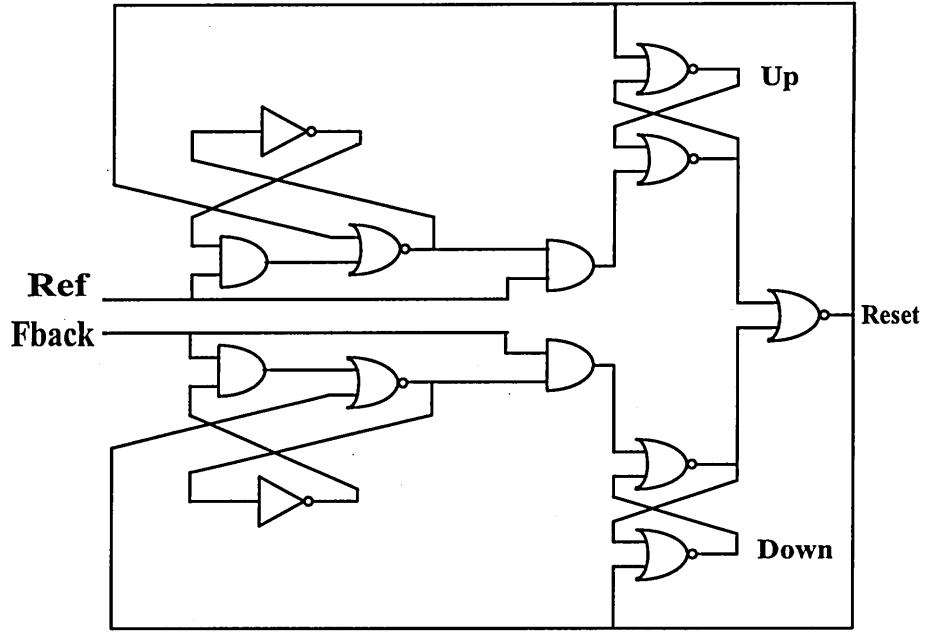


Figure 125: Differential PFD

PFD and a differential charge-pump. An external loop filter was utilized to have flexibility in the adjustment of the loop bandwidth and the phase margin.

The differential PFD used in the loop is basically same as the one discussed in Appendix-A, Figure 142, that is constructed from DFFs. The gate level schematics of this PFD is provided in Figure 125. The transistor sizes of the gates are adjusted such that the PDF would drive the inputs of the differential CP. The PFD was designed for a setup delay of 500 psec, and a reset delay of 200 psec. This reset delay is aimed for the reduction of the dead-zone effects.

In contrast to the conventional charge-pump architecture, Figure 145, the differential CP on our chip has the current source transistors (M2 and M5) connected to the outputs and the switches (M1 and M4) connected to the power/ground busses [48], i.e. reversed connections. The schematics of the half-circuit is given in Figure 126. This helps to reduce the glitches resulting from charge-sharing. In addition, the switches are converted into full-inverters with M3 and M6 to reduce the fall-time of the current pulses by providing low-impedance charge/discharge paths. These transistors,

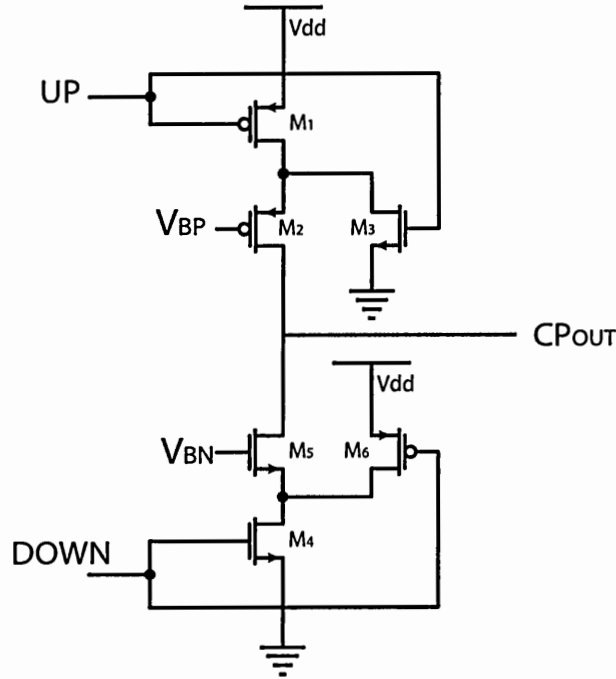


Figure 126: Half of the differential CP

however, narrow down the usable output range of the structure by causing reverse currents at the output nodes. Differential CP can simply be constructed by using two half-circuits with the switching scheme presented in Figure 127. To stabilize the common mode of the output levels, a regular common-mode-feedback (CMFB) circuit was used. For the PLL, the charge-pump current was chosen as $70 \mu A$ resulting in a combined PFD/CP gain of $K_{PFD-CP} = I_{CP}/2\pi = 11.14 \mu A/rad$.

A third order differential loop filter was selected for better reference spur attenuation. As implied above, off-chip surface-mount-technology (SMT) components were used to construct the filter for added flexibility in the adjustment of the loop parameters. Because the feedback loop was closed externally, the PLL automatically involves a divide-by-N circuitry. The division ratio varies between 16 and 32 depending on the VCO. Including all the components, the block-diagram of the implemented PLL is given in Figure 128.

For the optimization of the PLL with different VCOs, resulting in different VCO

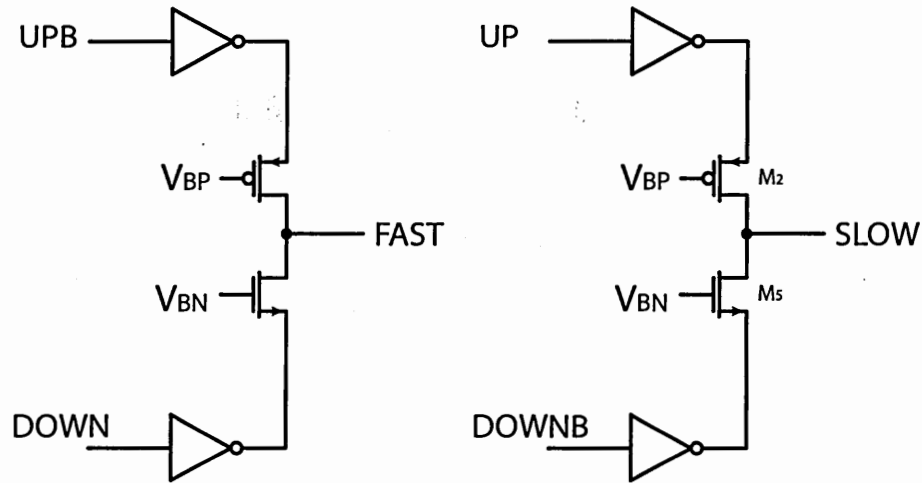


Figure 127: Differential CP

gains and division ratios, EasyPLL software from National Semiconductor was utilized. Design parameters of the constructed PLLs along with the measurement results are summarized in Table 35.

Next, some important considerations regarding the design and testing of the PLLs are given concluding Chapter VIII.

- The implemented multiple-pass ring oscillators have single-ended frequency control inputs. The PLLs employing these oscillators, therefore, were constructed using the slow output of the charge-pump with a single 3rd order loop filter.
- Lock-in ranges of the PLLs are slightly narrower than the corresponding VCO tuning ranges. This is because the designed charge-pump has a smaller output voltage range when compared to the VCO input ranges.
- All the designed PLLs properly tune-in to the input frequency and keep following the input frequency within the lock-in range.
- Phase margins of our PLLs vary between 55° and 74° promising a stable operation.
- The output period jitter was measured by using the statistical functions of a

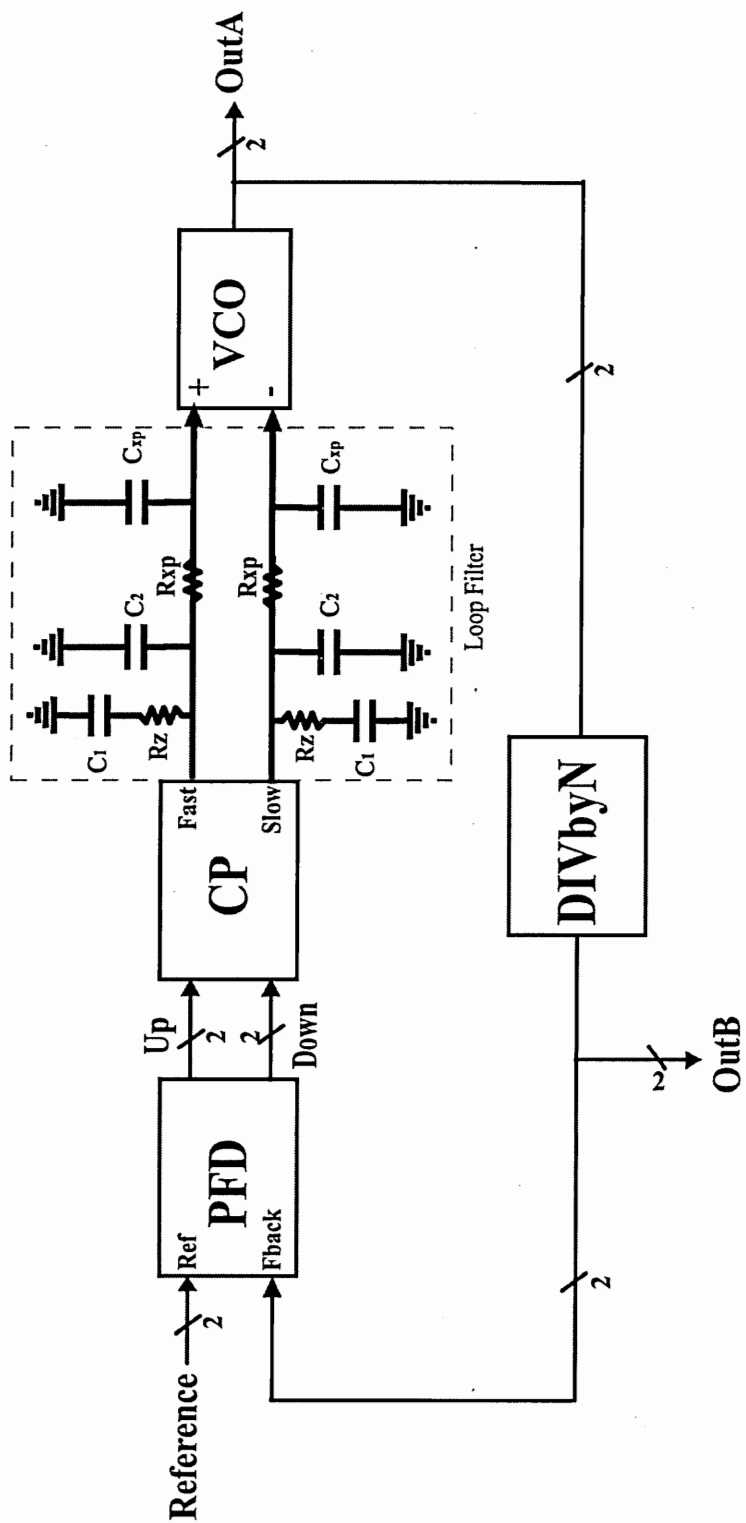


Figure 128: Differential PLL

Table 35: PLL Design Parameters and Measurements

VCO Type	9-Stage Multi-Pass	3-Stage Multi-Pass	LC Digital Input = 0001111
VCO Range (MHz)	1120-1860	5160-5930	2392-2525
Lock-in Range Output (MHz)	1180-1840	5310-5840	2402-2518
Lock-in Range (MHz) Input (MHz)	74-115	166-182.5	150.1-157.4
VCO Gain (MHz)	770	793	68
Division Ratio	16	32	16
Charge Pump Gain ($\mu A/rad$)	11.14	11.14	11.14
C_1 (nF)	10	10	10
C_2 (pF)	50	50	50
C_{xp} (pF)	50	50	50
R_z (Ω)	680	680	680
R_{xp} (Ω)	1500	1500	3300
Phase Margin (Degrees)	68.66	73.38	54.92
Closed Loop 3-dB Bandwidth (kHz)	529.58	248.37	54.36
RMS Jitter at OutB (psec)	1.63	2.63	3.63

digital oscilloscope. Because of the limitations of this instrument in measuring small jitters, jitter was measured by comparing the lengths of multiple periods. That is, the variance of the time difference between the rising edge of the first cycle and the falling edge of the last cycle is measured for a large number of cycles. Using jitter's dependence on the square root of the length of the measurement interval [49], i.e. $J_{N*\Delta t} = \sqrt{N}J_{\Delta t}$, the period jitter of the various PLL configurations were found by measuring the jitter over 64 cycles and dividing the measured values by 8.

- Loops were designed with different closed-loop bandwidths to observe the noise filtering characteristics of the loops. A quiet signal generator was used as the reference signal leaving the VCO as the major source of the PLL output noise. Therefore, it is expected that wide bandwidths would result in more suppression of the VCO noise and smaller output jitter and vice-versa. This behavior was actually seen in the jitter tests; PLL constructed with the LC oscillator resulting in the largest output jitter because of the small bandwidth.
- For all the PLLs, output cycle-to-cycle jitter exhibits periodicity when measured in consecutive periods of the signal. Same behavior was also observed in the statistical analysis of the jitter showing the bimodal characteristics. This was accounted to the fact that during PLL testing, multiple oscillators and their corresponding dividers were operating simultaneously creating multiple frequencies and their subharmonics on the chip. Because of the cross-talk among these signals, the measured jitter values were larger than the expected. Note that the testing of the PLLs required to turn-on all the parts on the chip.

CHAPTER IX

PERFORMANCE COMPARISON

In this chapter, we will first discuss the performance limitations of ring and LC oscillators. Using the phase noise models given in Chapter IV, the attainable noise levels from both of these architectures will be quantified as a function of the oscillation frequencies. In addition, these performance levels will be compared to actual ring and LC oscillator designs published in the open-literature to see the trends. Next, it will be explained where this work fits in this comparison. For this purpose, scatter plots containing information about the phase noise and the maximum frequency of the designs will be utilized.

9.1 LC vs Ring Oscillators

For typical LC oscillators, loaded Q factors of up to 8-14 [13,33] were reported in standard CMOS technologies. Considering that ring oscillators employ multiple stages that contribute to the output noise and they have smaller effective Q factors, 1.3-1.55 for conventional rings [8], LC VCOs superior noise performance can be understood. In terms of the maximum achievable frequencies, ring oscillators are limited by the minimum propagation delay of the gain stages, whereas an LC oscillator's oscillation frequency is strictly determined by the resonator implemented by the L and C. This provides for higher oscillation frequencies than that achievable using ring VCOs.

Adding high quality integrated inductors into a CMOS process flow, however, increases the cost and complexity of the chip, and also introduces problems such as the control of eddy currents in the substrate. Ring-oscillators, on the other hand, can be built in any standard CMOS process and may require less die area than LC

designs. For a fully integrated system, therefore, a ring oscillator is highly desirable if the system requirements can be met.

Although basic ring oscillators have phase noise and frequency limitations, it is possible to boost the maximum frequencies and phase noise levels of ring oscillators close to their LC counterparts by using different ring architectures and circuit design techniques. This work, for example, discusses the design of low phase noise ring oscillators with oscillation frequencies up to 14 GHz by using a multiple-pass loop architecture along with a saturated gain stage. Furthermore, using Harjani's [6] definition of the ring oscillator Q factor, this work showed that Q factor of ring oscillators can be much higher than that predicted by Razavi [8], up to 4.5 at 900 MHz, with the use of saturated stages providing clipped signals. This model, however, also predicts a drop in the Q at higher frequencies.

Using Leeson's model, Equation (22), for LC oscillators; and Razavi's modification of this model, Equation (33), along with Harjani's definition of Q factor [6] for ring oscillators; some phase noise limits for both architectures were extracted. Most LC oscillators discussed in the publications are designed for a power level of 5-30 mW [11, 38, 39, 43, 50-56], and their Q factors vary between 2-8 [13, 54, 56] in standard CMOS processes. Considering these, two limits were found for the LC oscillators for 5 mW power dissipation and 30 mW power dissipation by taking the Q factor as 6 in both. For ring oscillators, three- and four-stage rings provide the best phase noise performance [8], and a power dissipation of 30-130 mW [9, 15, 19, 47, 57] is typical. Therefore, a three-stage ring with a power dissipation of 80 mW and a 900 MHz scaled Q factor of 3.6 [6] was assumed. For the given cases, the phase noise limit curves are shown in Figure 129 for a logarithmic frequency axis.

These limit curves demonstrate that even with a significant power penalty, ring oscillators exhibit 17 dB more phase noise at 5 GHz. The difference, however, drops to 10 dB if ring oscillators are compared with lower-power LC oscillators. For a system,

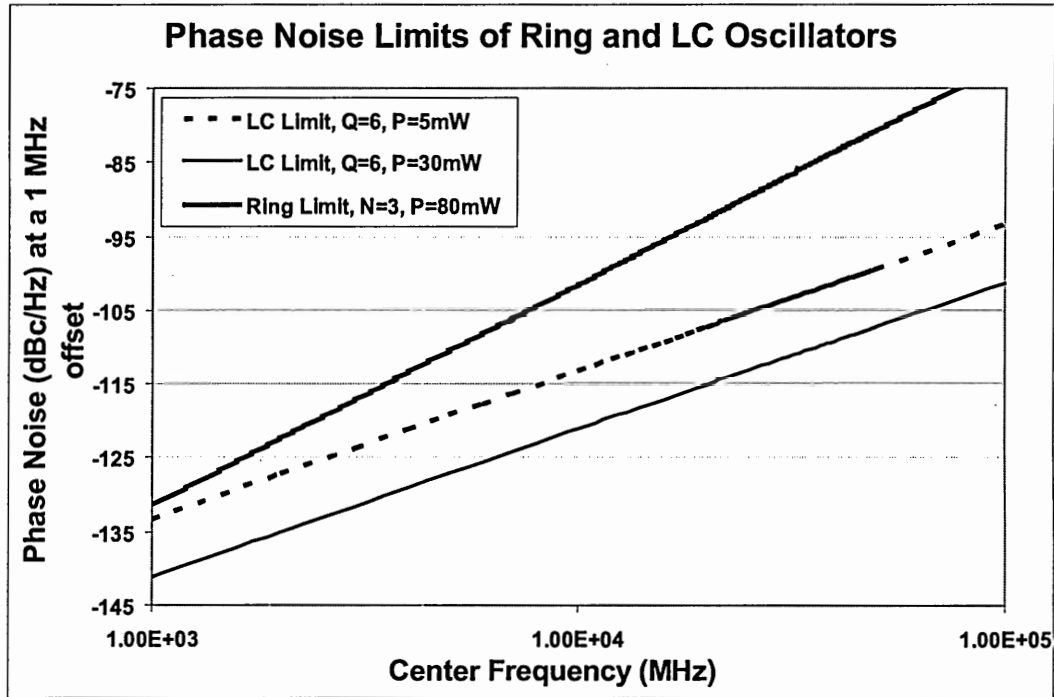


Figure 129: Phase noise limits of ring and LC oscillators

therefore, if power dissipation is not the main consideration, ring VCOs can still be useful at frequencies more than 10 GHz. Some practical applications will be provided later.

9.2 Published Designs

After defining the theoretical phase noise limits using fundamental phase noise models, it will be demonstrated how the published designs compare with these limits. To provide consistency in the following comparison, phase noise data from the papers were scaled to a 1 MHz offset from the maximum frequencies with an assumed 20 dB/decade drop with the offset and 20 dB/decade increase with the oscillation frequency.

For CMOS LC oscillators, the theory predicts a best case phase noise of -141 dBc/Hz at a 1 MHz offset from a center frequency of 1 GHz, with a 20 dB/decade drop at increasing frequencies. This performance estimation forecasts that CMOS

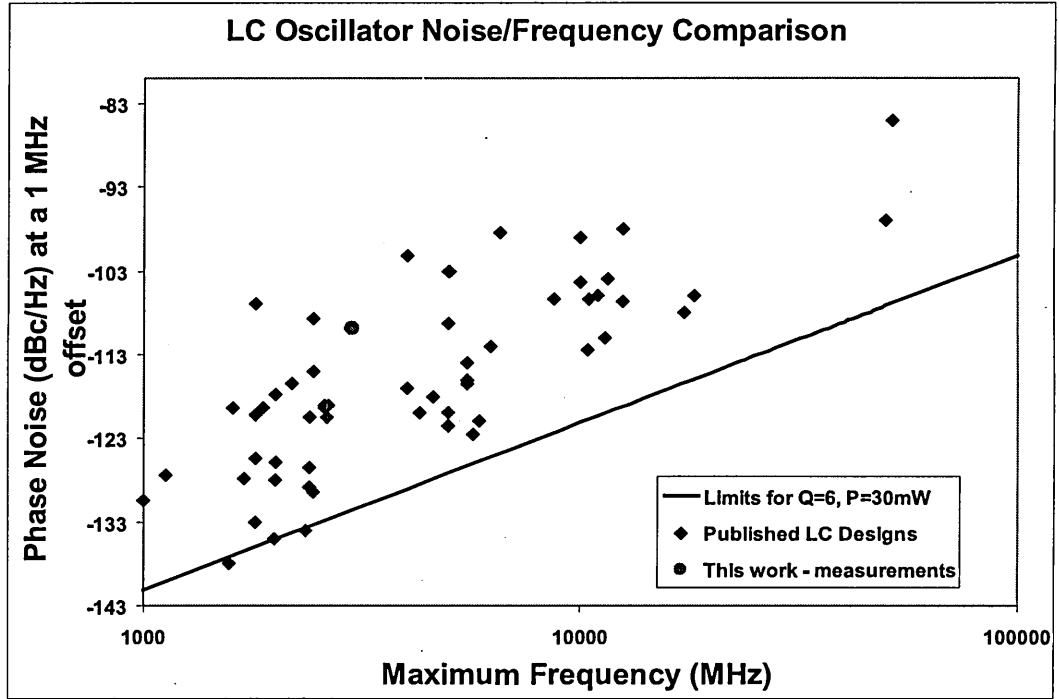


Figure 130: Phase noise vs frequency performance of published LC oscillators and 20 dB/decade limit curve

LC oscillators might be useful in demanding applications up to 100 GHz in a CMOS process. At these frequencies, however, transistors fail to operate as expected even in the most advanced technologies because of the process f_t limitations, and the self-resonance frequency of the inductors become important. Figure 130 compares this limit curve with various designs published in the open literature [3,4,11,13,33,38,39,43,48,50–56,58–89].

This scatter plot shows that few LC designs come close to or exceed this performance limit at lower frequencies, up to 2.4 GHz, whereas the phase noise performance of the published designs tend to stay further below this limit at higher frequencies. In fact, the dashed limit curve that follows the actual designs in Figure 131 has a 27 dB/decade drop. This additional increase in the phase noise at higher frequencies is accounted to the inductor and transistor limitations discussed above.

There are two different models, Razavi's [8] and Harjani's [6], that govern the

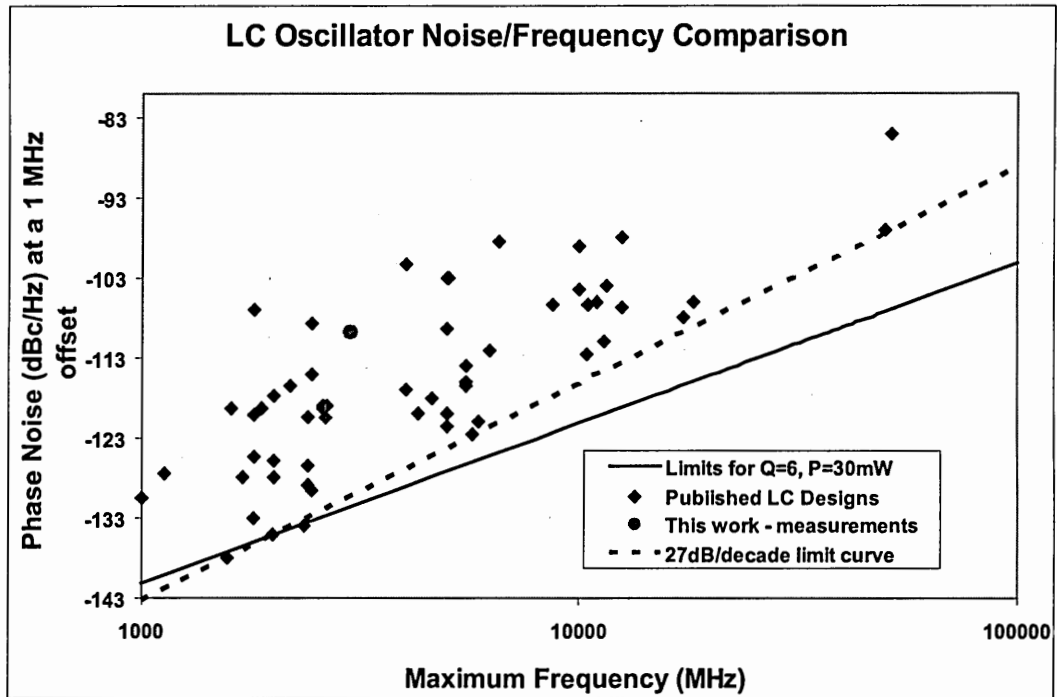


Figure 131: Phase noise vs frequency performance of published LC oscillators and 27 dB/decade limit curve

phase noise limits of ring oscillators. In contrast to Razavi's model, Harjani's model considers nonlinear effects and thus is expected to provide a better estimation. Figure 132 compares the limit curves found using both models with various ring oscillator designs published in the open literature [8–10,15,16,19,23,47,57,58,90–99].

Because of the common belief that ring oscillators are not capable of meeting the requirements of the high frequency RF and optical transceiver applications, there are a limited number of publications with the maximum reported frequency being 9 GHz. Therefore, it is not clear which phase noise model better defines the phase noise limits of ring oscillators. If additional data points regarding this work are inserted into this scatter plot, one can see that Harjani's limit curve predicting a 30 dB/decade drop is more accurate at higher frequencies, whereas Razavi's limit gives a better estimation for lower frequencies. This is illustrated in Figure 133.

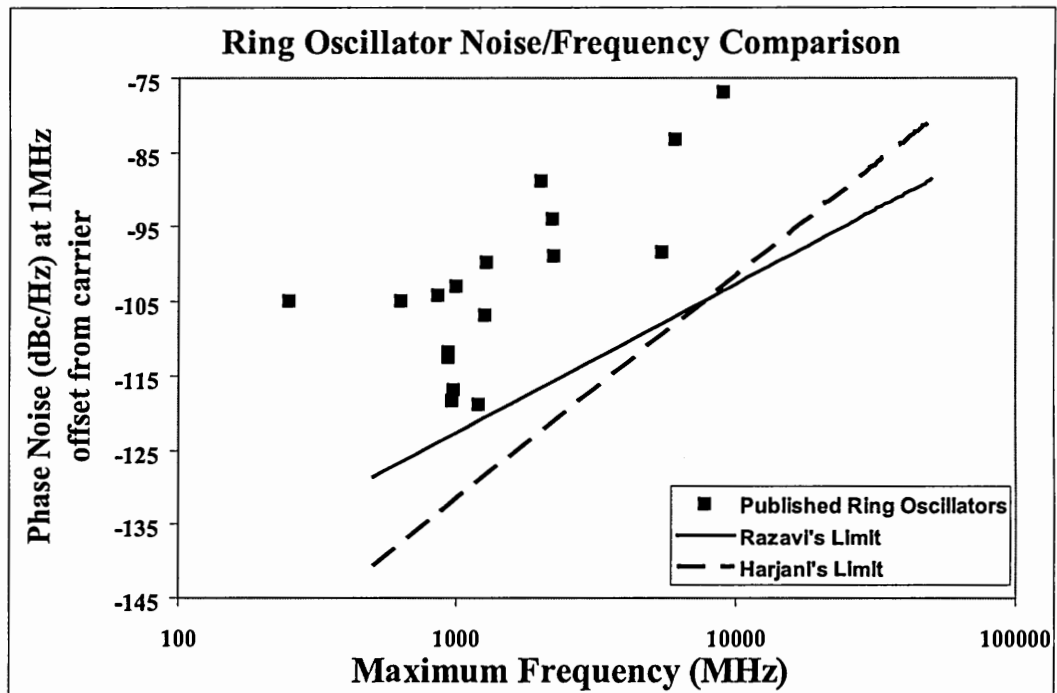


Figure 132: Phase noise vs frequency performance of published ring oscillators and limit curves

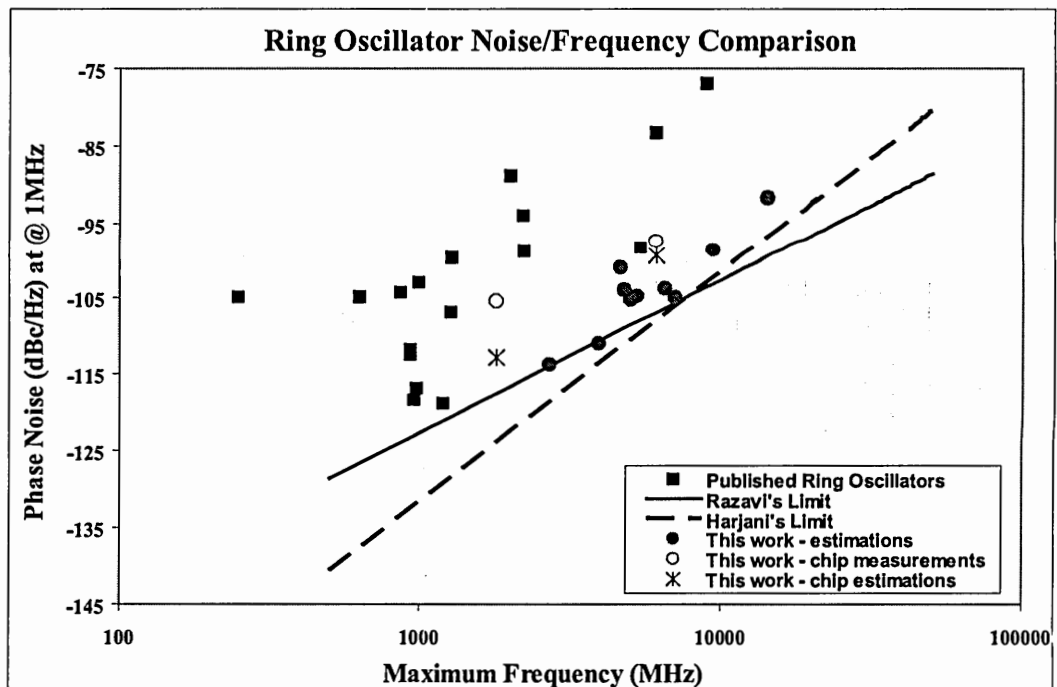


Figure 133: Phase noise vs frequency performance of published ring oscillators and introduced designs compared with the limit curves

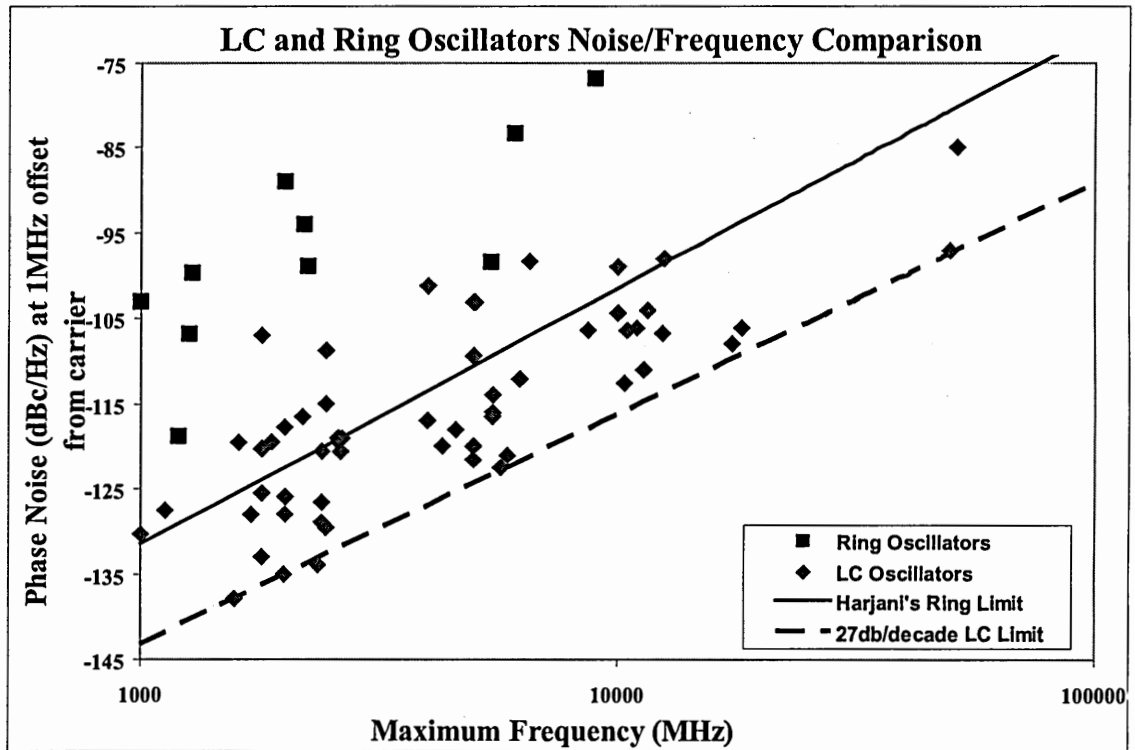


Figure 134: Phase noise/frequency performance of published ring and LC oscillators

9.3 Where Does This Work Fit?

This work already compared various LC and ring oscillators published in the open literature with their own kinds, i.e. LCs with LCs and rings with rings. Next, the question is how do these designs compare with each-other. To answer this question, another scatter plot was created in an effort to evaluate the relative performance of the actual designs. This plot, given in Figure 134, was constructed for frequencies above 1 GHz and includes the phase noise/frequency data points as well as the limit curves. The difference between the phase noise levels of ring and LC oscillators at similar frequencies is observed again in Figure 134. This result, therefore, is in agreement with the previous estimations.

The reason that some LC and some ring designs provide better noise performance is because of the difference in the power dissipation levels and the dissimilarity in the implementations. VCO figure-of-merit (FOM), previously defined in Equations

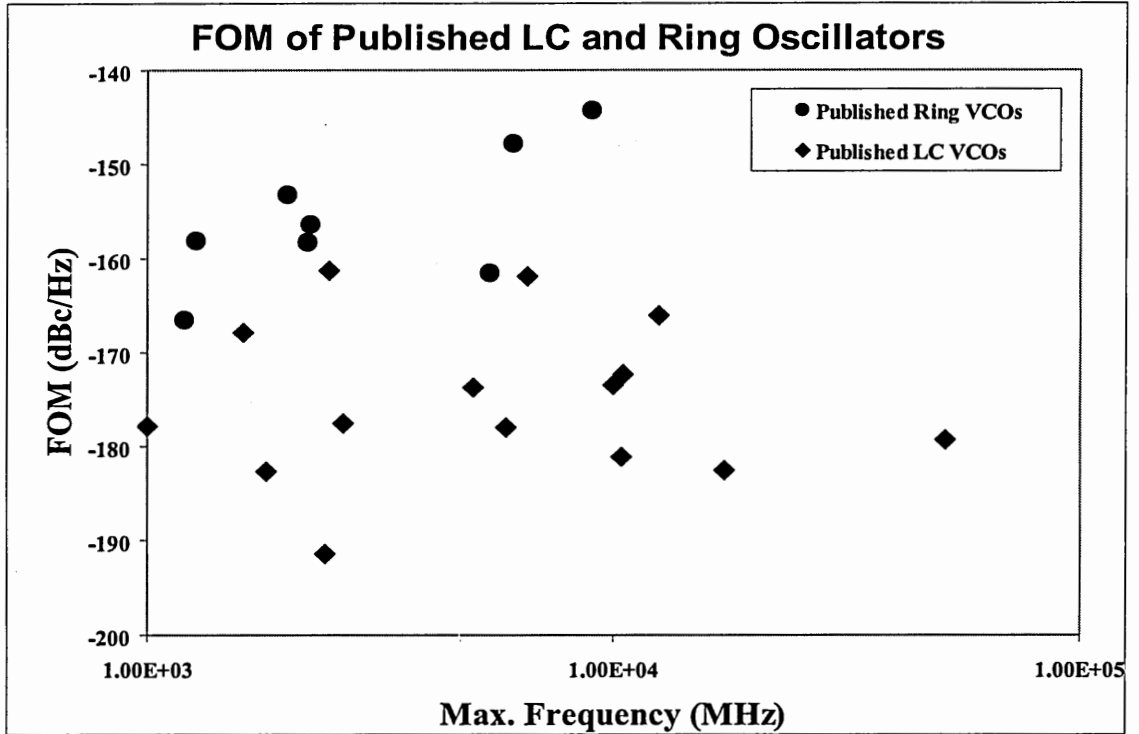


Figure 135: FOM of published ring and LC oscillators

(110) and (111), includes the effect of the power dissipation and, therefore, provides a more fair comparison of the performances. Figure 135 compares the FOM of various ring [8, 9, 15, 16, 19, 47, 94] and LC [4, 11, 33, 38, 39, 43, 50–56, 74] oscillators. Superior noise performance of the LC architecture is also evident from this comparison.

A close examination of the scatter plots reveals that there are not many published ring oscillators capable of providing phase noise levels close to the Harjani's limit [6]. In fact, there are only two such publications above 1 GHz [9, 19] and only one above 5 GHz [19], both with phase noise values 9–10 dB worse than the limits. Introduced multiple-pass ring oscillators designs, on the other hand, match or come closer to the phase noise limits extracted using Harjani's model. This is illustrated in Figure 136, where data points for introduced designs are added to the scatter plot given in Figure 134. From this plot, one can also see that the ring oscillator designs of this work provide phase noise levels comparable to some of the published LC oscillators,

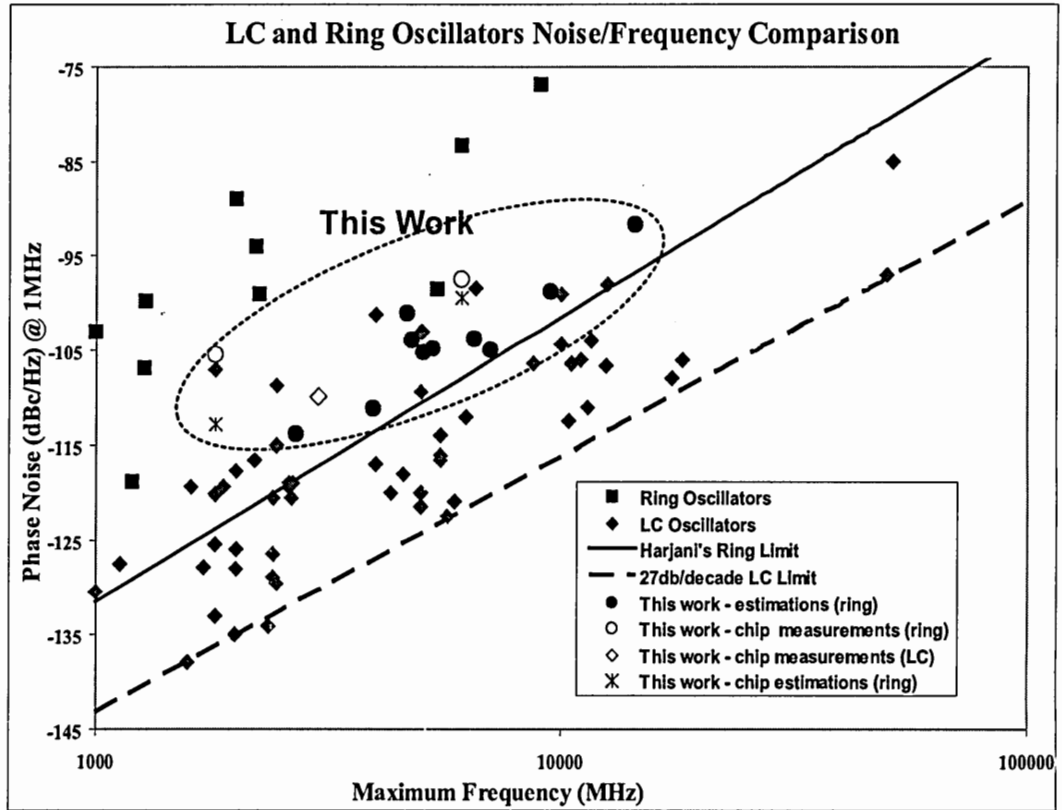


Figure 136: Phase noise/frequency performance of published ring and LC oscillators vs introduced designs

significantly better than the previous work on ring oscillators.

FOMs of the introduced ring oscillator designs were also compared with other designs in Figure 137. This comparison shows that the introduced ring oscillators provide the best FOM values in their frequency ranges when compared to previously published ring oscillators demonstrating that introduced designs' improved noise and frequency levels are not obtained at the expense of increased power dissipation but because of the efficient use of power. The FOM value extracted from the estimations is slightly better than that extracted from the measurements for the implemented three-stage ring oscillator while the difference is larger for the nine-stage design. This is accounted to the unbalanced turn-off circuitry of the longer chain and the higher nonlinearity of this design leading to increased noise conversion. Another important observation from this plot is that, in contrast to the published designs, the FOM values

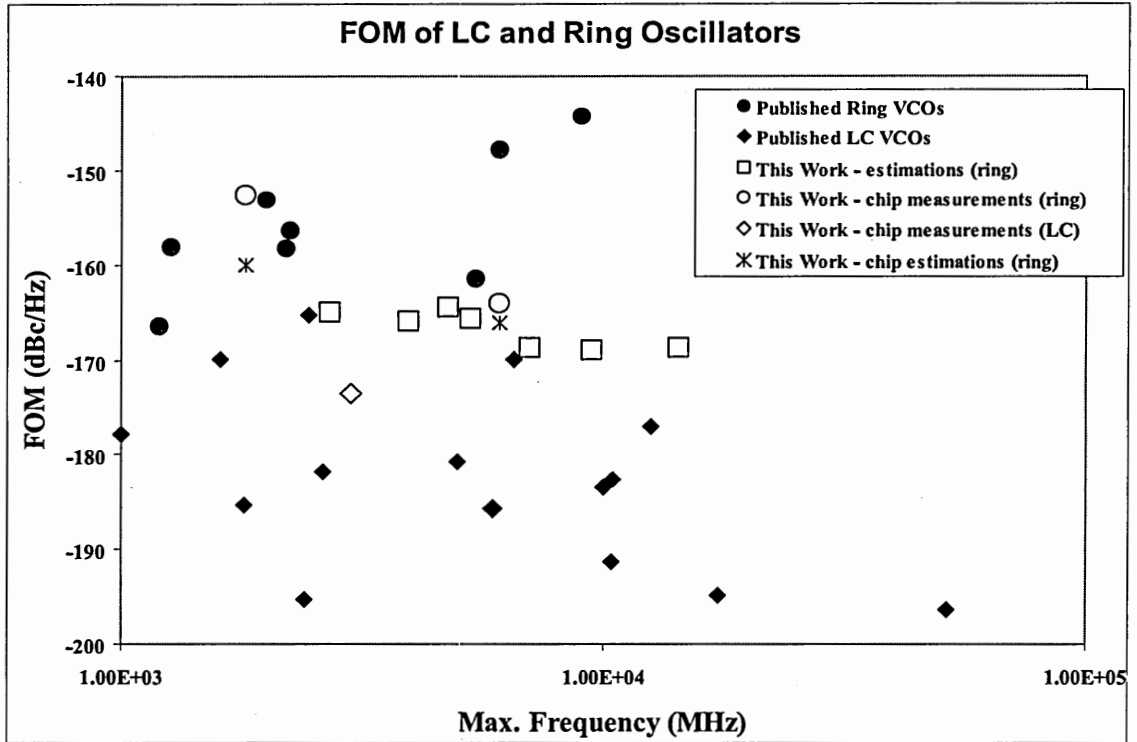


Figure 137: FOM of published ring and LC oscillators vs introduced designs

of the introduced ring VCO designs stay almost constant over a wide frequency range; only a 4 dB change over a $5 \times$ frequency difference. This is accounted to the fact that all of these oscillators use similar architectures such that they have similar power dissipation and phase noise performance values if scaled to same maximum and offset frequencies, and that these values are extracted from simulations that does not model some second-order effects.

Finally, from the given comparisons, one can conclude that it may become possible to expand the applications of ring VCOs into some areas that strictly required the performance of LC oscillators. Examples of these applications will be provided in the concluding chapter of this thesis.

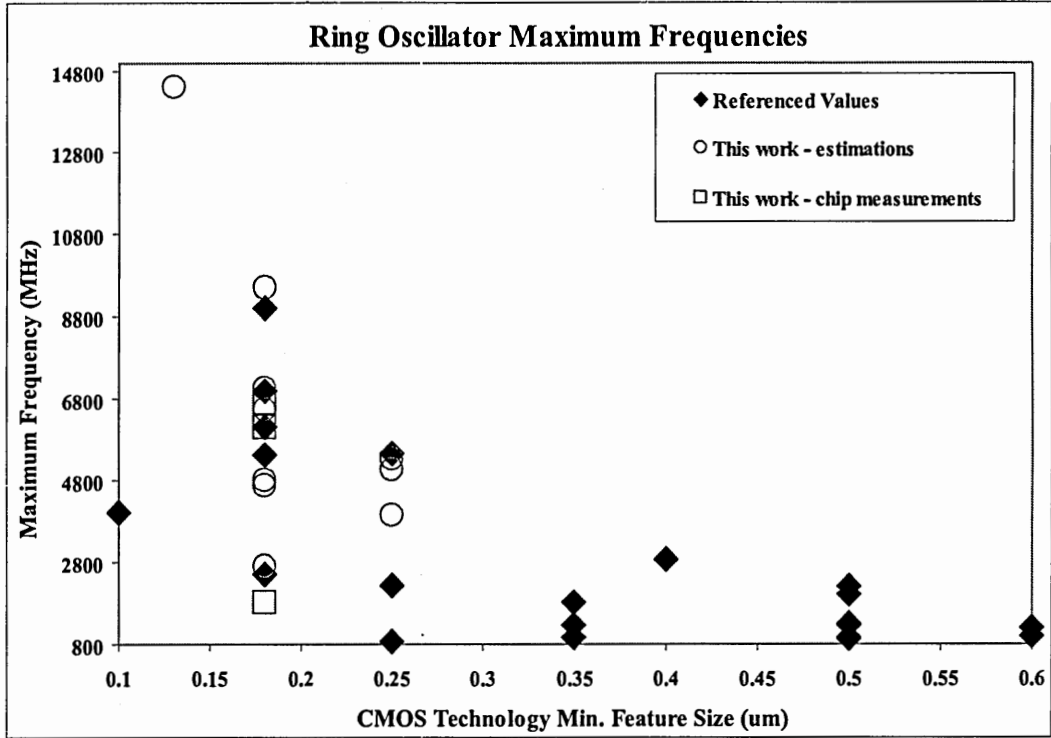


Figure 138: Maximum frequencies of various ring oscillators as a function of the minimum feature size

9.4 CMOS Minimum Feature Size

In the final section of this chapter, maximum frequencies and associated phase noise levels of various ring VCOs will be discussed by grouping the designs according to their technologies. For this purpose, two scatter plots are created using this work and published designs. Figure 138 shows the maximum oscillator frequency as a function of the minimum feature size, whereas Figure 139 provides information on the phase noise.

Comparison of the maximum frequencies with the minimum feature size shows that achievable frequencies exponentially increase with the reduction in the channel-lengths. For a given technology, the maximum demonstrated frequency is approximately proportional to the inverse $(3/2)^{th}$ power of the channel-length, i.e. $f_{max} \sim L_{min}^{-3/2}$. In more advanced technologies exhibiting smaller channel-lengths, however, this exponential dependence is expected to flatten out because of the reduction in the

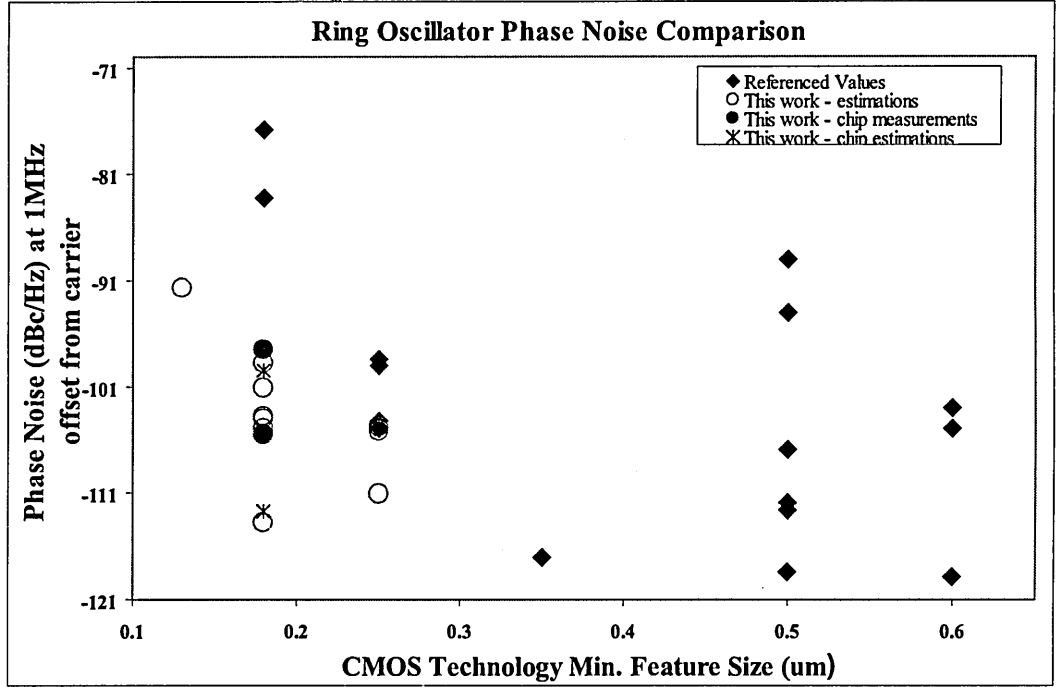


Figure 139: Phase noise performance of various ring oscillators as a function of the minimum feature size

power supply voltages. For an example, if the power supply voltage can be kept same as in a $0.13 \mu\text{m}$ CMOS technology, maximum frequencies of 30 GHz might be possible in a $0.08 \mu\text{m}$ CMOS process. The data points given on Figure 138 also demonstrate that a $0.25 \mu\text{m}$ CMOS or better is required for a 5 GHz ring oscillator, whereas a 10 GHz ring oscillator can be designed in a $0.18 \mu\text{m}$ CMOS process or better.

Referring to Figure 139 and this work's previous discussions, one can see that ring oscillators provide better phase noise performance at a constant frequency as the technologies improve. With reducing gate lengths, transistor f_t s increase resulting in faster signal transitions. This, in turn, improves the effective Q factor of the ring oscillator enhancing the phase noise performance. The provided data illustrates that there are a couple of published ring oscillator designs providing good noise performance, close to -120 dBc/Hz, at frequencies close to 1 GHz. This work, however, introduced various multiple-pass ring oscillators with saturated gain stages that extend the low noise capability of ring oscillators to higher frequencies. Thus the capability of ring

oscillators replacing LC networks in some demanding multi-GHz applications has been demonstrated.

CHAPTER X

CONCLUSION AND FUTURE WORK

In the concluding chapter of this thesis, a brief summary of the introduced work is presented along with discussions on the major contributions of this work and the future directions.

10.1 Summary

This dissertation presented a study of high-frequency low-noise CMOS voltage controlled ring oscillators. By examining various techniques that improve the overall characteristics of ring oscillators, limitations of the ring architectures were explored when they are extended to multiple-GHz applications. A feedforward type differential architecture, i.e. multiple-pass loop architecture, along with a saturated-type delay-stage utilizing cross-coupled transistors has been found to have promising characteristics to increase the maximum frequency and to reduce the output phase noise of ring oscillators. In the earlier chapters, this architecture/delay-stage combination was mathematically analyzed using linear frequency domain analysis techniques leading to an accurate formulation for the increase in the maximum frequency. Existent ring oscillator phase noise models were also modified making them utilizable for the introduced designs using simple equations. In addition, a new ring oscillator design, which mixes analog and digital elements, was proposed to solve the problems related with the single-ended control and the high gain of conventional ring oscillator designs.

After discussing design techniques for implementing high-frequency low-noise voltage controlled ring oscillators in Chapter V, it was demonstrated how to actually apply these techniques in sub-micron CMOS technologies by introducing various high-performance ring VCO designs. The practical application of the provided phase noise models was also described. In this part, SpectreRF and SPICE simulations are used to verify the theoretical results. The results showed that three-stage designs provide the highest frequencies, four-stage designs provide a good trade-off between the maximum frequency and the phase noise, and longer chains may be feasible when additional output phases are required. In addition to the phase noise and maximum frequency of the oscillators, other important characteristics were also analyzed including the tuning range and the stability under parameter variations.

In Chapter VII, the design of two different conventional ring oscillators, which was aimed to provide a frame of reference for the introduced designs, were discussed; and various performance metrics are compared. These demonstrated the superior performance of the introduced ring oscillators when compared to the conventional architectures. The performance curves also showed that the ring designs discussed in this work can be extrapolated to other processes with good results.

Chapter VIII provided experimental results of a prototype chip that was implemented to verify and validate the theoretical and simulation results presented in the previous chapters. The prototype chip was fabricated using a standard 0.18 μm CMOS process and included various multi-GHz ring VCOs as well as a symmetrical LC VCO. On this chip, proper operation of the introduced ring VCOs were demonstrated up to 6.7 GHz. The ring oscillator test results were in good agreement with the estimations verifying the claims of this study. With this prototype, in addition, multi-GHz CMOS ring and LC VCOs, for the first time, are implemented on the same chip and tested under similar conditions for a fair comparison. For demonstrating the operation of these VCOs in a practical system, various charge-pump PLLs were

also constructed and successfully tested.

In the final chapter of this thesis, designed VCOs were compared with other ring and LC oscillators published in the open literature. This comparison shows that multiple-pass ring oscillator designs of this work provide phase noise levels comparable to some of the published LC oscillators, significantly better than most of the previous work on ring oscillators. The results also suggest that, when fabricated under similar conditions, multi-GHz ring oscillators may have phase noise levels close to LC networks at the expense of increased power dissipation. Note that, this work's designs' improved noise and frequency levels are not obtained at the expense of increased power dissipation but that the power is used more efficiently; which can be verified by checking the plotted ring VCO FOM factors.

The presented results, in conclusion, suggest that it may become possible to extend the applications of cost effective ring VCOs into some areas that previously required the performance of LC oscillators. The attractive features of this approach are the simplicity of the design and the fact that rings can be implemented in any CMOS process.

10.2 Applications

In the previous discussions, it was mentioned that the ring VCOs of this work may replace LC oscillators in some multi-GHz applications. In this section, a discussion of these applications will be provided along with a list of other practical applications.

The results of this study suggest that, at low power levels, LC oscillators are capable of providing better phase noise levels at higher oscillation frequencies owing to their high-Q resonator elements. The use of an LC VCO, therefore, is considered to be essential for RF transceivers that have the most stringent phase noise and power requirements. The implemented symmetrical LC design, for example, satisfies the phase noise and frequency specifications of various RF applications including

Bluetooth and HomeRF while dissipating only 3.6 mW.

Although wireless systems require the circuits to operate at low power levels, wired transceivers have more relaxed power requirements. Introduced ring oscillators, therefore, may replace LC oscillators in wired transceiver applications such as 1/10 Gigabit Ethernet and SONET [11] (STS-24, STS-48, STS-192) that previously required the performance of an LC network. Note that the discussed multiple-pass ring VCOs satisfy the phase-noise/frequency specifications of some demanding wireless RF applications such as Bluetooth and HomeRF; however, with a high power requirement questioning their ability to serve in low-power wireless transceiver applications. Considering these, some practical applications of this work's ring designs are provided in the following list.

- Phase locked loops
 - Clock generation for CPUs, DSP chips, and DRAMs
 - Frequency synthesizers
 - Clock/data recovery networks
 - Serializer/deserializers
 - Wired transceivers
 - * Gigabit Ethernet
 - * 10 Gigabit Ethernet (IEEE 802.3ae)
 - * SONET (STS-192, STS-96, STS-48, STS-36, STS-24,...)
- Stand-alone applications
 - Direct frequency synthesizers
 - Clock generation

- System synchronization (deskewing) applications such as zero-delay-clock-buffers
- Oversampling A/D converters

10.3 Contributions

The key contributions of this work are:

1. Discussion of the existing VCO phase noise models and derivation of a simple closed form formula for the effective Q factor of a ring oscillator using Razavi's model [8]. Generalization of Harjani's [6] phase noise model to N-stage non-linear ring oscillators.
2. An extensive linear frequency domain analysis of multiple-pass loop architectures, as well as a qualitative discussion of the operation principles. Presentation of guidelines for the construction of multiple-pass loops with odd or even number of stages.
3. Derivation of a formula defining the increase in maximum operating frequency using multiple-pass architectures for both strong and weak secondary loops; an enhancement over the analysis given in [23] that greatly underestimates the frequency increase for strong secondary loops.
4. Introduction of a family of ring-oscillator designs using saturated gain stages mixing analog and digital elements along with a multiple-pass ring architecture to optimize the maximum operating frequency while maintaining phase noise performance.
5. Design of the three-stage multiple-pass ring oscillators that offer the highest frequencies in a specific technology, up to 9.5 GHz in a 0.18 μm CMOS and

14.4 GHz 0.13 μm CMOS; and four-stage multiple-pass ring oscillators with the optimum trade-off between the frequency and the phase noise performance.

6. Discussion of multiple-pass ring oscillators with increased number of stages for obtaining low frequency and/or increased number of phases. Introduction of a first order correction to the phase noise model [6] considering high-frequency multiplicative noise and multiple-pass loop effects.
7. Presentation of a differentially-controlled stage design that uses analog amplification and charge pumps in conjunction with a digital latching mechanism to solve the problems related to the single-ended control and the high voltage-to-frequency gain of the studied ring oscillators.
8. Description of experimental results and SpectreRF/HSPICE simulations of a prototype chip fabricated in a standard 0.18 μm , single-poly six-metal CMOS process. Illustration of the good agreement between the estimations and measurements in terms of oscillator frequency-voltage and phase-noise characteristics. Demonstration of the proper operation of voltage controlled ring and LC oscillators with oscillation frequencies up to 6.7 GHz. Demonstration of the operation of integrated PLLs employing these oscillators.
9. Extraction of quantitative guidelines for the selection of oscillator architecture, ring or LC, for a specific application by comparing various high-performance ring and LC designs from literature with the predictions of the phase noise models.
10. Comparison of the introduced ring oscillator designs with other ring- and LC VCO designs from literature and discussion of the limits and capabilities of introduced designs when they are extended to new processes.
11. Demonstration of the possibility to expand the applications of ring VCOs into

some areas that previously required the performance of LC oscillators, i.e. low-noise multiple-GHz communications systems.

12. Suggestion of practical applications for the introduced multiple-pass ring oscillators.

10.4 Future Research

This section will provide some of the possible future research directions that can be taken based on this work.

First, further prototype oscillators can be implemented on silicon to verify the trends of designs with different number of stages and different feedforward configurations. These prototypes, in addition, can be constructed using the dual control-path delay stage design (type-II saturated stage) to observe the improvement in the control-line noise suppression because of the differential control and the reduction in the VCO gain.

Future research efforts can also focus on the improvement of the stability of the presented oscillators under parameter variations. Although the saturated stage design is expected to have better immunity against the effects of device mismatches because of the digital switching, the use of cross-coupled transistors increase the interaction between the differential ports. A ring oscillator using this type of stage, therefore, will potentially be more susceptible to the common mode disturbances such as supply/ground variations when compared to a simple design using a differential input pair along with active loads. In an application requiring better stability, for example, one can use an adaptive compensation technique that employs an integrated sensor to sense the parameter variations and correct the operation of the circuits by feeding this information back. Here, the integrated sensor can simply be a bias circuitry with an output voltage level that is dependent on the system parameters such as the process corners and the ambient temperature. The relation between the output voltage

and the system parameters should be adjusted such that when this bias voltage is connected to the coarse tuning input (feedback control input) of the type-II saturated stage, the center frequency of the ring VCO stays constant under parameter variations. Then, the fine tuning input can be used to control the frequency of the VCO.

Another suggestion is on the use of multiple feedforward loops to obtain different oscillation characteristics. Note that the introduced designs had only single feedforward loops connected to the output nodes. Multiple feedforward loops means that various feedforward configurations are implemented on the same oscillator. This idea was previously introduced in [24] for a four-stage design but an extensive study is not available yet.

On the theoretical side, the discussed phase noise models require modifications to correct them for the strong noise folding effects found in nonlinear ring oscillators. Although a first order curve-fit correction is proposed and used in this work, better understanding of this effect is highly desirable. The formulations estimating the frequency increase of multiple-pass loops, in addition, involve parameters that cannot be easily calculated. These include the output capacitance and resistance values in the single-pole approximation of the delay stages, and also the output slew-rates. Equations that only depend on the available parameters of the devices such as transistor sizes, threshold voltages, transconductance parameters, etc., should be derived.

An important question that needs to be answered is what the maximum frequency limitations of introduced ring oscillators are when they are extended to newer CMOS processes with smaller gate-lengths. In the previous chapter, by interpolating from the current designs, it was mentioned that 30 GHz might be possible in a 80 nm CMOS process if the power supply can be kept at 1.2 V. This number was found by taking a three-stage design as the base. In an extension of this work [100], however, the use of frequency doublers are examined to further extend the maximum frequency of ring

oscillators. By feeding the I/Q outputs of a 7 GHz four-stage multiple-pass design (4MP0.18) into a regenerative symmetric frequency-multiplier, a 14 GHz output with a 600mV voltage swing was obtained in a 0.18 μm CMOS technology. Nexsys, the newest 90 nm process of TSMC [101], performs with a gate delay of 8.4 psec (high-speed version with a minimum gate-length of 50 nm), a $3.3 \times$ improvement over the standard TSMC 0.18 μm CMOS process. Using a linear approximation, this suggests that maximum frequencies as much as $14\text{GHz} \times 3.3 \approx 46\text{GHz}$ might be possible in advanced CMOS processes; thus meeting the frequency requirements of some millimeter-wave applications such as SONET-768.

Although the above discussion states that operation frequencies as much as 40 GHz may be possible in advanced CMOS technologies, phase noise performance should also be considered. Another important question, therefore, is what the phase noise of a ring oscillator would be at these frequencies. Dai [6] showed that the effective Q factor of a ring oscillator depends on the process parameters with the relation

$$Q_{eff} \propto \sqrt{f_t \left(1 - \frac{V_T}{V_{dd}}\right)}, \quad (112)$$

where f_t is the transistor unity gain frequency, V_T is the threshold voltage, and V_{dd} is the power supply voltage. For the standard TSMC 0.18 μm CMOS process, $[f_t \ V_T \ V_{dd}] = [42.5\text{GHz} \ 0.55\text{V} \ 1.8\text{V}]$, whereas $[f_t \ V_T \ V_{dd}] = [\sim 85\text{GHz} \ 0.23\text{V} \ 1\text{V}]$ for the TSMC high-speed 90nm CMOS process. The effective Q factor, therefore, is expected to improve by 50% at a fixed oscillation frequency. Since phase noise is proportional to the inverse square of the Q factor, the expected phase noise improvement is ~ 3.5 dB. Note that the 0.18 μm four-stage multiple-pass design exhibits a phase noise level of -105.31 dBc/Hz at a 1 MHz offset from a center frequency of 6.8 GHz. Considering the frequency difference, therefore, the phase noise of the 46 GHz design is estimated as ~ -92 dBc/Hz at a 1 MHz offset. This result, however, is rather optimistic because the noise contribution of the frequency doublers as well as the effects of low-frequency noise ($1/f$) and systematic noise sources (power-supply, control-line)

are ignored. Secondary order effects related with the reduction of the gate-lengths to sub-100nm values may also result in an increase of the phase noise. Nevertheless, these estimations show that CMOS ring oscillators can still be usable at 40+GHz frequencies.

APPENDIX A

PLL INTRODUCTION

A.1 PLL Introduction

In this section, a brief introduction to phase locked loops (PLLs) will be given. Please refer to Razavi's [102] and Harjani's [6] books for a more detailed analysis of the PLLs.

A PLL is basically a negative feedback system in which the parameter of interest is the excess phase of the periodic signals instead of the voltage or current amplitudes. PLL is mainly used to generate an output signal, or output signals in the case of multiple-phase oscillators, whose phase is locked to that of the input signal. This condition is satisfied if and only if the output frequency of the PLL is an integer multiple of the input frequency, i.e. $f_{out} = N * f_{in}$ where N is an integer. Here, *locked* means that the input and output signals of the PLL has a constant and finite phase difference, and the discussed frequency relationship exists.

PLLs are used in many applications in which a stable clock signal is required. Examples include the local oscillators of the transceivers that are used for modulation/demodulation of the communication signals, clock generators that supply the timing information to complex digital systems including microprocessors and digital signal processing systems, A/D converters, etc. Frequency synthesizers, skew correction systems, data/clock recovery networks, frequency division/multiplication circuits are other applications where the use of a PLL is essential.

There are two main classes of PLLs depending on the characteristics of the phase error detection. The first is the Linear or Analog PLL which employs a linear phase detection circuitry, while the other is called the Digital PLL because it uses a digital phase error detector. Note that both of these PLL types use analog VCOs and loop

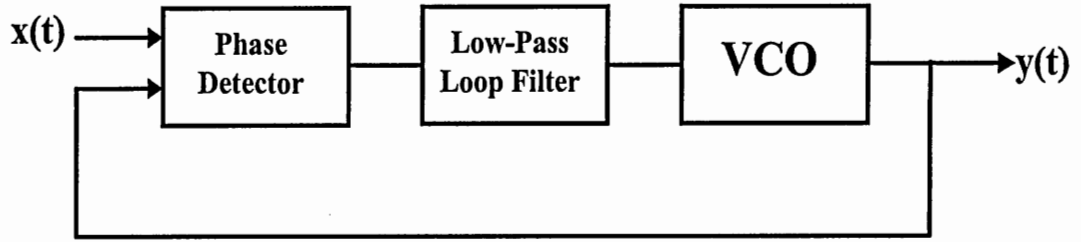


Figure 140: Phase locked loop block diagram

filters. On the other hand, there is another type of PLL, called the All Digital PLL (ADPLL), which is implemented by programming the digital signal processing (DSP) chips. ADPLL is not suitable for high-frequency communications applications, therefore it is beyond the scope of this thesis.

Figure 140 shows the block diagram of a typical PLL, consisting of a phase detector (PD), a loop filter (LF), and a VCO. In addition to these components, a frequency divider can be used in the feedback loop when the output frequency is required to be different than the input reference frequency, for example for frequency synthesizers. A phase detector is a device that senses the phase difference between the input and the output signals of the PLL and provides a voltage level proportional to the phase difference. Therefore, the PD acts like an error amplifier inside the PLL.

Naturally, a PLL tries to reduce the phase difference $\Delta\phi$ between its input and output because it is a negative feedback system employing an error amplifier. When the input and output frequencies are equal, assuming that there is no frequency divider in the feedback loop, and $\Delta\phi$ is constant with time, PLL is said to be locked. Under this condition, all the signals in the loop are strictly periodic and reached the steady state. The phase detector outputs an error signal whose average value is proportional to $\Delta\phi$. This signal is then filtered by the low pass LF, and the high frequency components are removed to produce a DC signal equal to the average of the PD output. Finally, VCO is controlled by this average value that forces the VCO to operate at a frequency equal to the input frequency with a phase difference of $\Delta\phi$.

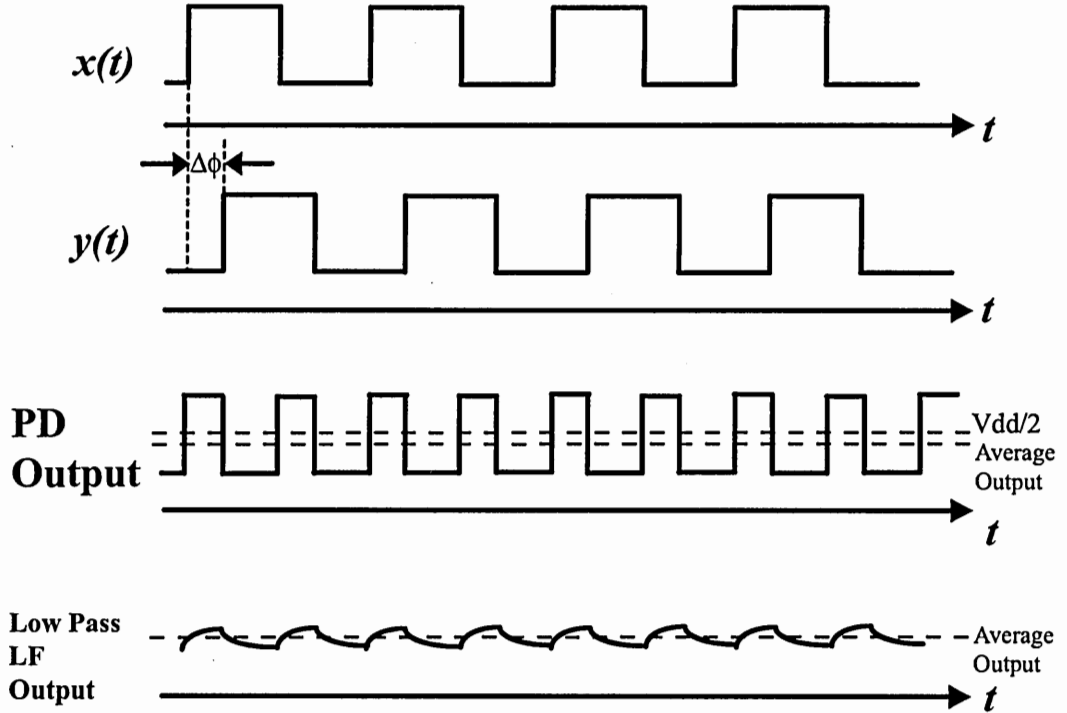


Figure 141: PLL waveforms for $y(t)$ lagging $x(t)$

Figure 141 shows the typical signals at various nodes of a locked PLL when there is a finite phase difference between the output and the input.

PLLs are generally considered to be highly nonlinear feedback systems because a PD has nonlinear characteristics for large $\Delta\phi$. The characteristics of a PD, moreover, is periodic and will repeat itself with a period of 2π radians. This is expected since every single signal in the PLL is also periodic and unchanged under a phase shift of 2π radians. For a small phase difference, a PLL can be approximated as a linear time-invariant (LTI) system, and transfer function analysis can be used to characterize it as will be shown shortly.

Analog PLLs use an analog multiplier as the linear phase detector. For two sinusoidal signals, $x_1(t) = A * \cos(\omega_1 t + \Phi_1)$ and $x_2(t) = A * \sin(\omega_2 t + \Phi_2)$, the output of the multiplier is $y(t) = \frac{A^2}{2}(\Phi_1 - \Phi_2)$ for $\omega_1 = \omega_2 = \omega$, assuming that the high frequency component at frequency of $2\omega t$ is filtered by the lowpass LF. Because phases of input signals are taken to be different, one is a cosine wave and the other is

a sine wave, there is a $\pi/2$ systematic phase error between the input and the output signals of the PLL. The output characteristics of the linear PD is sinusoidal shaped thus nonlinear for large $\Delta\phi$. This type of PD is not widely used in practical PLL applications because the PD gain is dependent upon the amplitudes of the input signals and the average output is zero for $\omega_1 \neq \omega_2$, both of which are undesired. The second property means that the PD does not provide any information to pull the PLL towards the locking frequency if the input and output signals are running at different frequencies.

Digital PLLs, on the other hand, use digital logic gates to implement the PD. An XOR gate, for example, can be used since it is basically a digital multiplier. For a digital PD, the output does not depend on the amplitude of the input signals assuming that the digital signals operate with rail-to-rail signal levels. The $\pi/2$ systematic phase error, however, still exists and the PD output does not provide any information about the frequency difference of the inputs.

Most practical PLL designs use a phase-frequency detector (PFD) combined with a charge-pump (CP) instead of a simple PD because this significantly increases the acquisition range and the lock speed of the PLL. Another advantage of using a PFD charge-pump pair is that the static phase shift observed in PLLs using simple analog or digital PDs is eliminated. As the name suggests, a PFD both detects the phase difference and the frequency difference of the signals. A PFD is a state machine that contains memory elements such as latches. Figure 142 shows an implementation of a PFD using D flip-flops (DFF). This type of PFD outputs two non-complimentary signals that carry information about the phase and the frequency difference of the input signals. Sample PFD input and output signals are given in Figures 143 and 144 for two different cases. For the first case, Figure 143, there is a frequency difference between the two input signals, while the second case shows the signals when there is a finite phase difference between the inputs running at the same frequency as illustrated

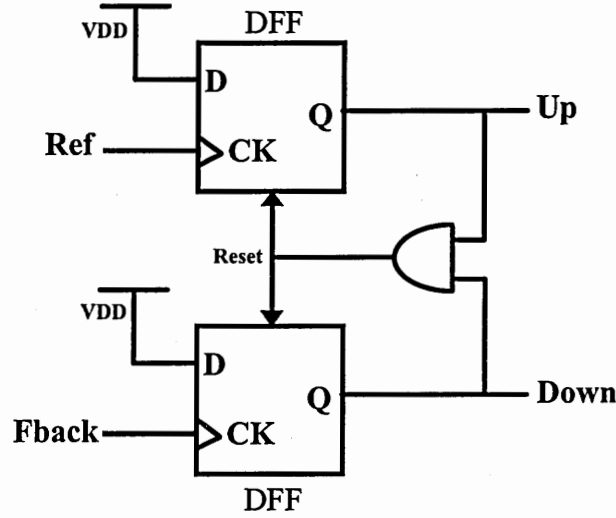


Figure 142: Phase Frequency Detector

in Figure 144. Figure 145 shows the block diagram of a PLL employing a PFD and a CP, called a charge-pump PLL. This is the most widely used PLL architecture.

Next, the transfer function of a charge pump PFD, shown in Figure 145 will be derived without going into the details. Because the charge pump exhibits integration, the transfer function of the PFD-CP pair can be written as $H_{PFD-CP}(s) = \frac{K_{PFD}}{s}$, where $K_{PFD} = I_{cp}/2\pi$. That is the open-loop transfer function contains a pole at the origin. The transfer function of a VCO can be written as $H_{VCO} = K_{VCO}/s$, and hence there is another pole at the origin in the open-loop transfer function. Therefore, a charge-pump PLL cannot be stable without using a stabilization technique. A resistor connected in series with the LF capacitor can be used to add a zero into the PLL transfer function, thus stabilizing the PLL. With this resistor R_z included, the final transfer function of a charge-pump PLL can be written as

$$\frac{Ref(s)}{Out(s)} = H(s) = \frac{\frac{I_{cp}}{2\pi C_1}(R_z C_1 s + 1)K_{VCO}}{s^2 + \frac{I_{cp}}{2\pi}K_{VCO}R_z s + \frac{I_{cp}}{2\pi C_1}K_{VCO}}. \quad (113)$$

The natural frequency and the damping factor of this second order system can be given as

$$\omega_n = \sqrt{\frac{I_{cp}}{2\pi C_1}K_{VCO}}, \quad (114)$$

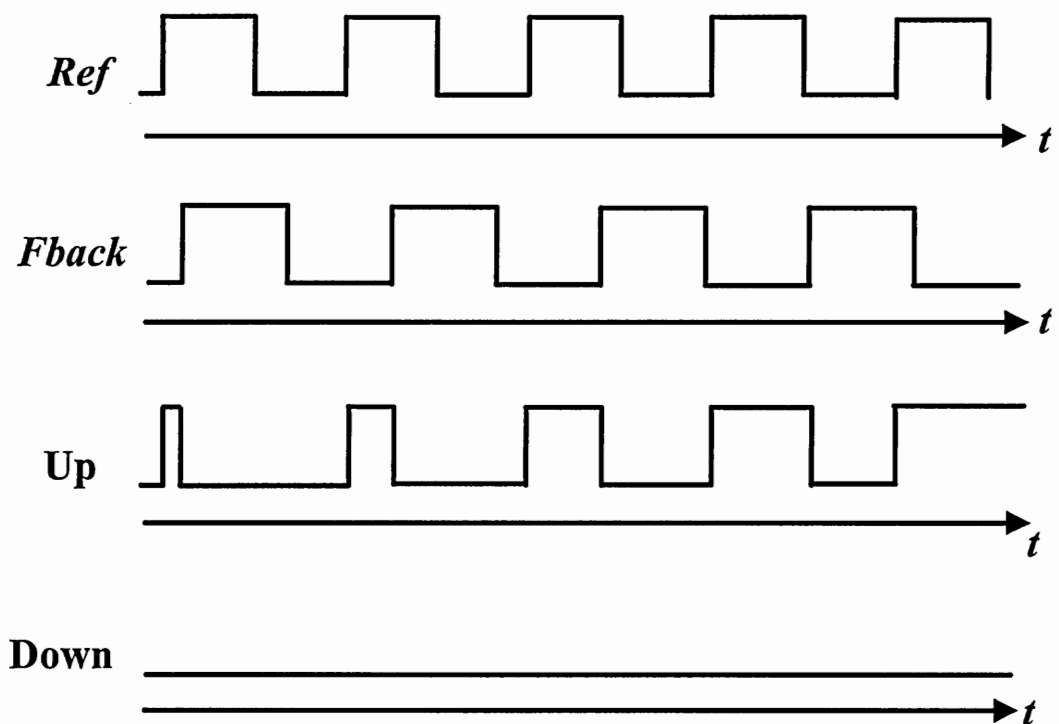


Figure 143: PFD response for $\omega_{Ref} > \omega_{Fback}$

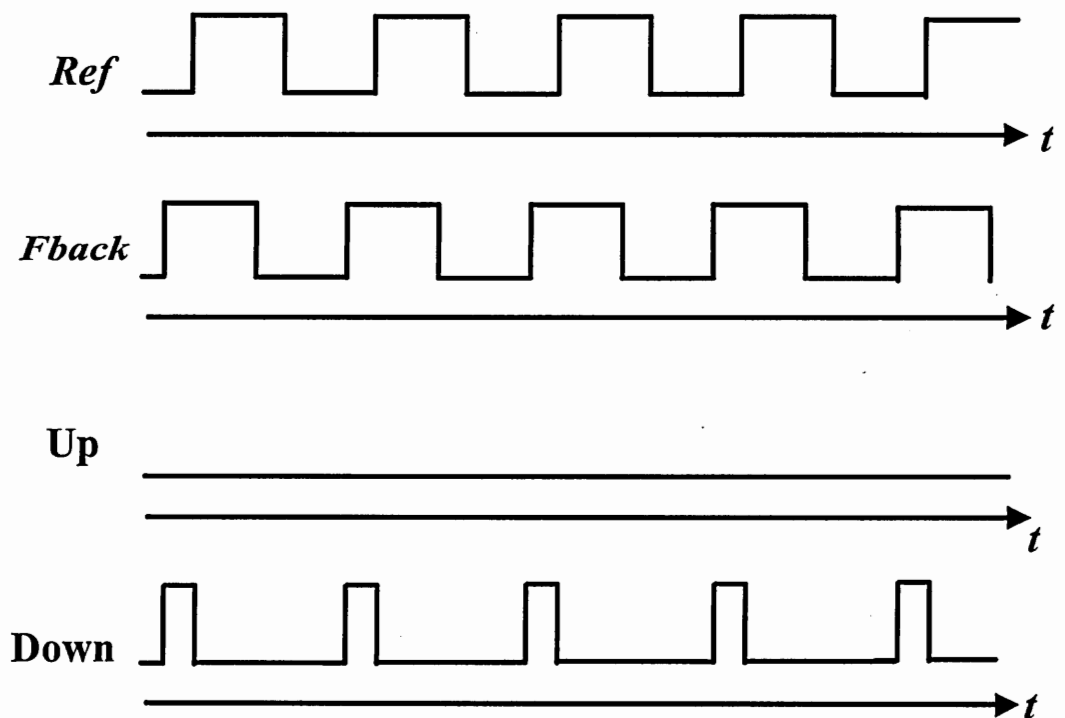


Figure 144: PFD response for *Ref* signal lagging *Fback* signal

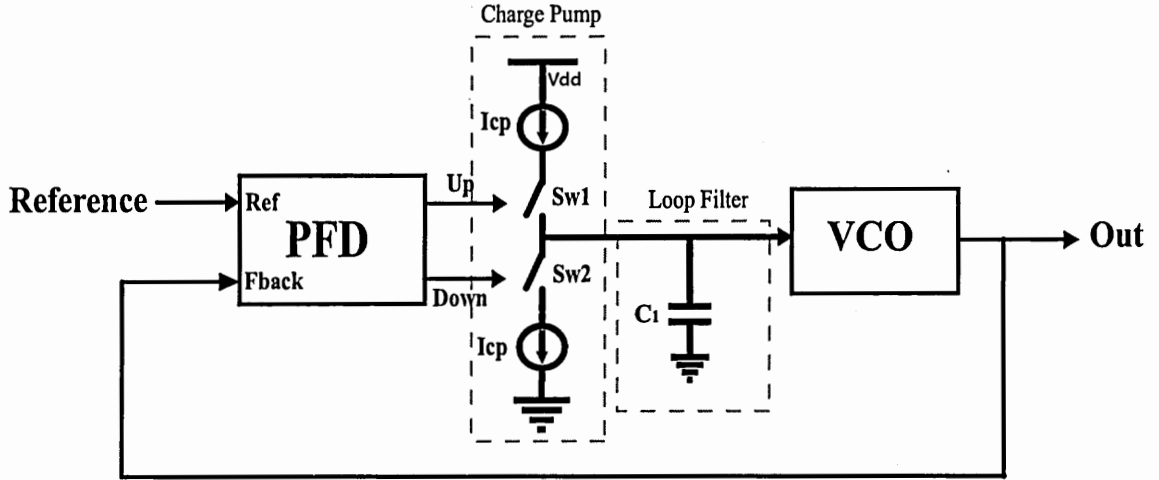


Figure 145: Charge Pump PLL

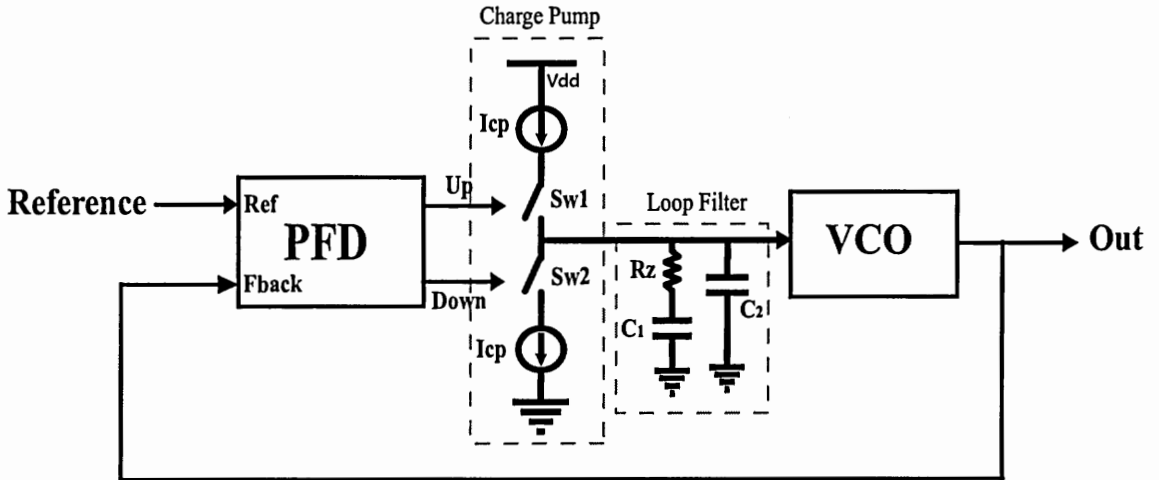


Figure 146: Charge Pump PLL with the stabilization resistor and the ripple reduction capacitor

$$\zeta = \frac{R_z}{2} \sqrt{\frac{I_{cp} C_1}{2\pi} K_{VCO}}. \quad (115)$$

Usually, however, another capacitor is added into the LF to reduce the ripple at the control voltage of the VCO thus providing better characteristics. The final charge-pump PLL block diagram, including this capacitor, is shown in 146.

Since the parameter of importance is the phase of the signals in a PLL, instead of the amplitudes, phase noise is an important issue that deserves special attention. In a PLL, there are two types of noise sources, the first is the input signal that might be

corrupted by phase noise, and the second is the electrical components that make up the PLL, such as transistors and resistors, adding up to the output uncertainty. All the blocks of a PLL, the PFD, the LF, the VCO, and the frequency divider, contribute to the output noise but VCO noise is the most significant one among them. Since a PLL acts like a low-pass filter for the input signal phase, which is apparent from Equation (113), the input phase noise spectrum is shaped by the low-pass transfer function of the PLL. Bandwidth of the PLL, therefore, determines the input noise rejection characteristics of the PLL, that is small bandwidths corresponds to better filtering of the input phase noise. The noise introduced by the VCO, in contrast, is shaped by a high-pass transfer function when it appears at the output. This high-pass transfer function can be written as

$$\frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (116)$$

Therefore, there is a tradeoff in the design of the bandwidth of the PLL in terms of the input and the VCO phase noise rejection. For systems involving heavily corrupted input signals, such as in clock recovery systems, the bandwidth can be kept low to reduce the contribution of the input phase noise. When VCO noise is more critical, on the other hand, wider bandwidths might be preferable. Please refer to references [6, 102] for a more detailed analysis and discussion of the phase noise in PLLs.

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VITA

Yalçın Alper Eken was born in Ankara, Turkey, in 1977. He received the B.S. degree in electrical and electronics engineering from Middle East Technical University (METU), Ankara, Turkey, in 1999 and the M.S. degree in electrical and computer engineering from Georgia Institute of Technology (GaTech), Atlanta, in 2001.

His interest on Analog/Mixed-Signal/RF integrated circuit design started with the implementation of on-chip released spiral MEMS inductors during his undergraduate years in Dr. Tayfun Akin's research group. In his first graduate year, in Dr. Farrokh Ayazi's group at Georgia Tech, he worked on high-precision switched-capacitor sensor readout circuits for the micro-g MEMS accelerometers that he designed and fabricated. This project involved the implementation of integrators, programmable gain amplifiers, folded cascode OTAs, and bandgap reference circuits; resulting in a prototype chip that was tested. In the following years of his PhD program, after joining Dr. John P. Uyemura's research group in the CMOS laboratory, he focused on the design of low-noise high-frequency CMOS voltage controlled oscillators and phase locked loops employing these oscillators in the Yamacraw 10 Gigabit Ethernet project. Related with this project, he successfully implemented and tested a prototype chip in a 0.18 μ m CMOS process containing 1-6.7 GHz ring and LC VCOs and PLLs, and introduced a family of ring VCOs operating at frequencies more than 10 GHz in standard CMOS.

During the summer of 2002, he was with the Integrated Device Technology (IDT), Atlanta, where he worked on a 300MHz PLL part that is currently in volume production. In this project, he focused on the design of the ring VCO, phase-frequency detector (PFD), charge pump (CP), voltage-to-current converter, and related bias

circuitry. He also characterized the similar products in the market for comparison. This characterization included the measurement of jitter, frequency performance, tap-to-tap delays, and variation around different temperature corners.

His current research interests include analog/mixed-signal/RF IC design for CMOS high speed communications systems, design and implementation of VCOs and PLLs for clock/data recovery networks to be integrated in LAN applications such as Gigabit Ethernet, 10-Gigabit Ethernet, or SONET STS-18..192, and VLSI system design.

Among more than a million high-school graduates, Mr. Eken ranked 184 in the 1995 university entrance examination of Turkey and chose to study in the Electrical and Electronics Engineering department of the region's leading institution, Middle East Technical University. He ranked 2nd in the Electrical and Electronics Engineering Department of METU, on his graduation in 1999, and he received the Bulent Kerim Altays Award six times, which is granted to the best two students of every semester.