HIGH-DENSITY CAPACITOR ARRAY FABRICATION ON SILICON SUBSTRATES

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HIGH-DENSITY CAPACITOR ARRAY FABRICATION ON SILICON SUBSTRATES

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Dedicated To My Parents and My Sister

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SUMMARY

System integration and miniaturization demands are driving integrated thin film capacitor technologies to ultra-high capacitance densities and lower leakage currents for power integrity and efficient power management. The emerging needs for voltage conversion and noise-free power supply in bioelectronics and portable consumer products require densities of above 100 $\mu F/cm^2$ with BDV 16-32 V with independent capacitor array terminals and non-polar dielectrics for design flexibility. In spite of these needs, the volumetric efficiency of high-density capacitors has only gone through incremental changes over the past few decades because of several fundamental limitations with existing capacitor technologies. Today's high-density capacitor technologies either suffer from low surface area because of the microscale electrodes or low permittivity dielectrics or both. Tantalum capacitor technologies provide highest surface area enhancement compared to other existing technologies but the dielectrics are limited to tantalum pentoxide with a permittivity of about 25. On the other hand, MLCC (Multilayered Ceramic Capacitors) do not have adequate area enhancement of more than 50 for a 100 micron device. Further, these devices are not compatible with thin silicon or organic packaging. The trend towards silicon trench capacitors does not lead to tremendous area enhancement either because of the limitations of silicon micromachining technologies. While the emerging electrochemical double layer capacitors addresses these limitations leading to extremely high capacitance densities, the technology has fundamental material barriers towards higher voltages and high-frequency operation.

The aim of this research, therefore, is to explore a new silicon-compatible thin film nanoelectrode capacitor technology that can meet all the above requirements. The proposed nanoelectrode capacitor approach enables two unique advances. The first advance is to achieve ultrahigh surface area thin film electrodes by sintering metallic nanoparticles directly on a silicon substrate at CMOS-compatible temperatures. The second advance of this study is to conformally-deposit high permittivity dielectrics over such particulate nanoelectrodes using Atomic Layer Deposition (ALD) process.

Thin film copper particle nanoelectrode with open-porous structure was achieved by choosing a suitable phosphate-ester dispersant, solvent and a sacrificial polymer for partial sintering of copper particles to provide a continuous high surface area electrode. Capacitors with conformal ALD alumina as the dielectric and Polyethylene dioxythiophene (PEDOT) as the top electrode showed 30X enhancement in capacitance density for a 20-30 micron copper particulate bottom electrode and 150X enhancement of capacitance density for a 75 micron electrode. These samples were tested for their mechanical and electrical properties by using characterization techniques such as SEM, EDS, I-V and C-V plots. A capacitance density of 30 $\mu F/cm^2$ was demonstrated using this approach. The technology is extensible to much higher capacitance densities with better porosity control, reduction in particle size and higher permittivity dielectrics.

1 INTRODUCTION

This chapter discusses the SOP paradigm to address multifunctional miniaturized systems. It then discusses power supply component integration as an important building block to realize SOP for the bioelectronics and portable consumer market industry, and the emerging need for ultra high-density capacitor structures for power components. It then briefly outlines the existing capacitor technologies and their limitations. Finally, a novel high-density capacitor approach is proposed to meet the emerging power supply needs.

1.1 Need for miniaturization at system level

From big and bulky workstations to an ultra slim smart phone with computing abilities better than huge computers, electronics industry has come a long way. Microelectronics products in the past have mostly been discrete systems that resulted in big and bulky workstations but the recent trend towards convergent digital systems has led to a huge industrial makeover for electronic products as reflected in **Figure 1.1** [1]

The main driving factors behind system level integration leading to miniaturization are:

- Higher performance of the systems
- Lower cost
- Better reliability
- Mega functionality

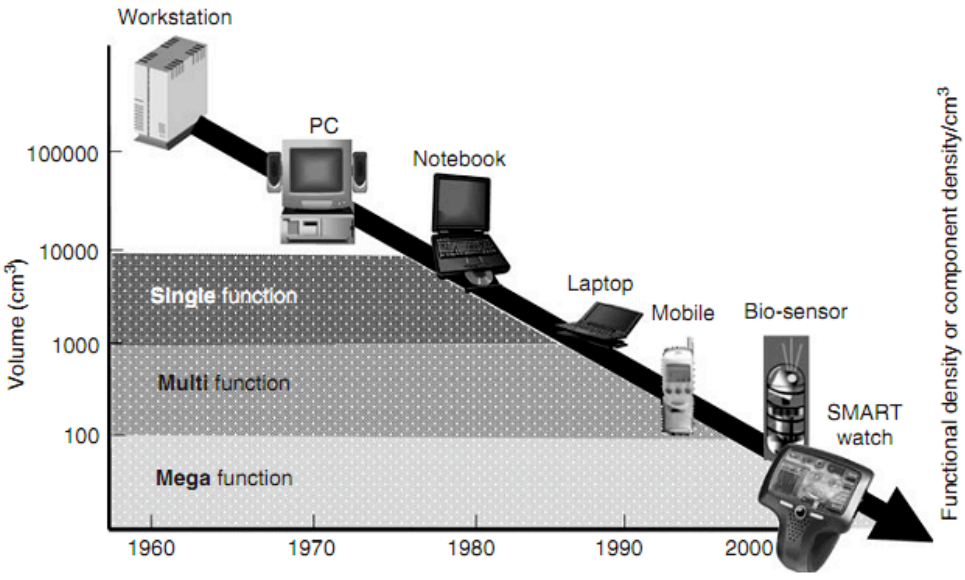


Figure 1.1 Electronic system trend towards digital convergence [1]

Any electronic system is made up of two major building blocks – active components and the system components which include passive components such as capacitors, inductors, and resistors, thermal structures, power sources and a substrate that provides wiring and interconnections to integrate all the system components.

Till recently, most of the integration efforts have been directed at silicon itself. This approach is known as System-on-Chip or SOC. SOC approach, fueled by the ever-shrinking dimensions of transistors in silicon, tends to integrate numerous system functions horizontally on the chip. However SOC approach suffers from some fundamental limitations due to very high costs involved in integrating disparate active devices such as CMOS, optoelectronic ICs, RF ICs. The fabrication itself is extremely complex involving dozens of photolithography steps and masks. Thus, in light of these

major technical and financial challenges, it is imperative for the industry and academia to look for other viable options leading to system integration [1, 2].

Stacked ICs and Package or (SIP) brings us one step closer to realize the ultimate vision of system miniaturization and integration. As is clear by the name, it refers to the stacking of similar or dissimilar bare chips or packages to create a 3-dimensional entity. Therefore, SIPs can be either IC-centric or package-centric. In package-centric SIPs, the individual ICs are first packaged and then stacked to form a 3-dimensional circuit. Though, this structure provides partial integration at the system level, package contribution is limited to providing wiring to connect ICs vertically. Such a structure is simply a multi-chip module (MCM), vertically packaged. On the other hand, IC-centric SIP structures that aim at stacking similar or dissimilar ICs vertically overcome some of the barriers presented by SOC, such as latency. However, as this approach also integrates at the device level rather than system level, it addresses only a small part of the problem[2].

It should be noted that systems not only include active devices but also consist of other system components such as passives, thermal structures, interconnections, substrates etc. Typically active devices occupy less that 10% of the total area of an electronic package while 90% of the area is occupied by the other system components. The silicon IC itself occupies very small area as compared to all the other system level components. Though the dimensions of Silicon based ICs are shrinking day by day as governed by Moore's law [3], miniaturizing the ICs alone do not provide an adequate solution for next

generation devices. These 3D ICs without system components create a huge gap that cannot be addressed by both SOC or SIP technologies as shown in Figure 1.2

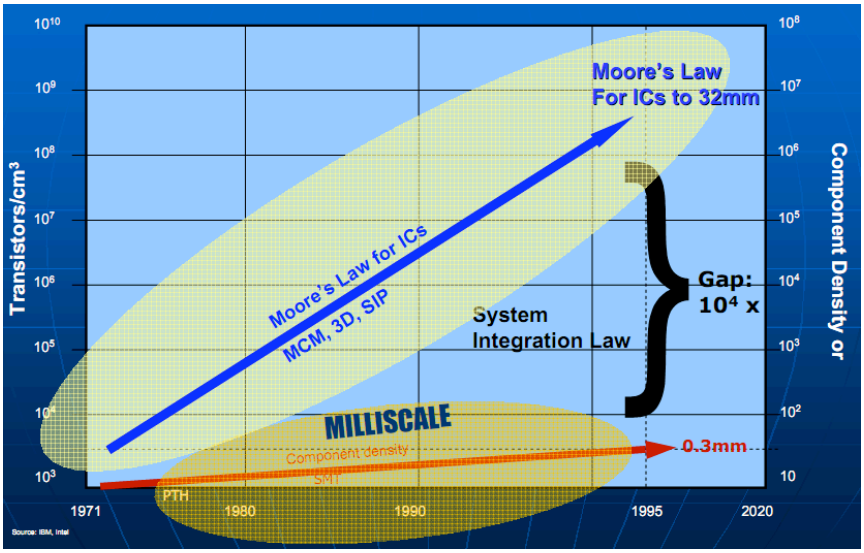


Figure 1.2 3D ICs without 3D systems - need for a new technology to address the gap(courtesy :PRC)

Thus in order to address this gap, Prof. Rao Tummala proposed the concept of System-on- Package (SOP) at the Packaging Research Center at Georgia Institute of Technology in the year 1994. SOP aims at system level integration by including both active as well as passive components in a synergistic combination to yield highly integrated, ultra miniaturized multifunctional systems at low cost [4]. This technology is discussed in more detail in the next section.

1.2 SOP Paradigm

SOP is a conceptual system technology paradigm that can be thought of as Moore's Law for system integration, being pioneered at Georgia Tech's Packaging Research Center

(PRC). In this concept, the package is the system. SOP combines the best of on-chip integration with the best of package integration, overcoming the current barriers and limitations of SOC and SIP as it aims at system level integration by: 1)Component integration using a variety of ultra-thin film embedded passive and active components 2.)Substrates that enable ultra-high wiring densities and 3) Fine pitch (< 30um) interconnections. The vision of SOP is to minimize the entire system by miniaturizing all the system components including passive components, power sources, thermal structures, substrates and interconnections. Thus SOP has the capability of integrating digital, RF, optoelectronic, micro-electro-mechanical sensors, and biomedical applications in one single package [1, 2, 4]. A schematic cross-section of SOP is shown Figure 1.3.

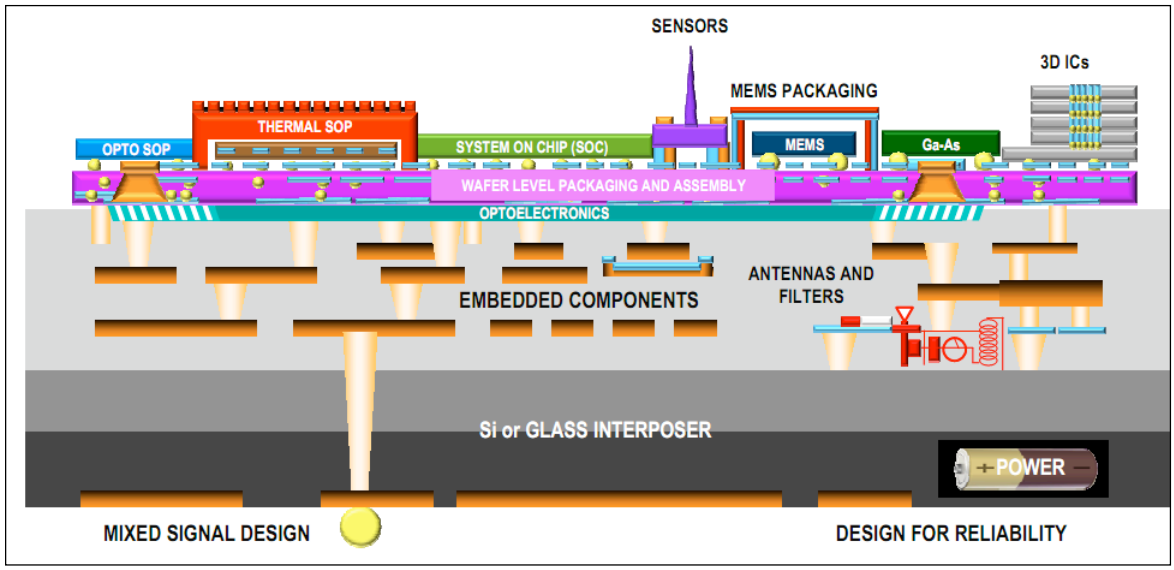


Figure 1.3 Cross-section of System on Package approach (Courtesy: PRC)

1.2.1 Key SOP technologies

There are three basic building blocks of SOP technology. These are high-density substrates, interconnections and embedded components. This section will briefly describe these three technologies.

High density interconnect substrate

Ultra high density SOP substrate is the backbone of the SOP concept. The substrate not only acts as a platform for system integration but it also supports RF, digital, optical and sensing applications simultaneously at very high frequencies. Moreover, the substrate should lend itself to embedding of both active as well as passive devices. Making very fine pitch (< 20 μm) via and 1-5 micron lines and spaces on the substrate is another challenge that needs to be overcome. The SOP substrate should have the following attributes

- Ultra-high density wiring with multi-layered thin film build-up dielectrics supporting fine pitch lines, vias, capture pads.
- Fine-pitch through-package via capability to address the signal routing needs.
- Thinner substrate core with high modulus to minimize warpage from build up layer processing
- Low coefficient of thermal expansion (CTE) for reduced interconnection stress leading to better reliability
- Low loss dielectric for efficient signal transmission and low cross-talk or noise
- Embedding of passive components such as resistors and capacitors for signal management and power noise control respectively

- Easy integration of thermal via structures for effective cooling
- Embedding of active components with high yield.

Conventional substrate materials such as BT and FR4 cannot meet all of these challenges and hence new materials are being developed to satisfy these requirements. Novel low-loss, low CTE, high Tg (glass transition temperature) thin organic laminate, glass or silicon with 50-100 microns for core and 5-10 microns for build-up dielectrics are currently pursued by PRC to address the emerging substrate needs.

Interconnections

Fine pitch interconnects is another important key technology for SOP. A large number of I/Os typically of the order of 20,000/cm^2 at pitch of 30 microns or below with high-current handling are needed to support today's advanced computing demands. Traditional solder interconnections may not be adequate to meet the fine pitch process constraints, thermo-mechanical and electrical reliability requirements in such packaging applications. In response to this need, semiconductor and packaging companies have migrated towards copper pillar or post technologies combined with solder bonding to make fine pitch interconnections. The copper bump enables easier processing because of its fine-pitch capability with BEOL compatible infrastructure, distributes the current density uniformly over the interconnection, lowers the bump temperature, minimizes the thermo-mechanical concerns by increasing the stand-off height and hence mitigates several reliability issues. Intel pioneered copper bump technology with 150 micron pitch

assembly and reliability using solders printed on organic substrate pads [14]. Since then, several companies have shown advanced interconnections with copper bump and electroplated solder caps. The GT-PRC has recently demonstrated 5X reduction in pitch and height at 30 microns and qualified it with complete substrate-level reliability studies using NCF bonding. For higher current densities, contact bonding with NCF may have constraints and hence metallurgical bonding with solders is usually preferred. Fine pitch copper interconnections with thin film metallurgical bonding are the key for high-density system interconnections.

Embedded Components

An electrical system can be envisioned as a collection of components that are connected in a systematic manner to perform desired electrical functions. These components can be classified as actives or passives based on their electrical characteristics. Active components such as transistors and diodes are defined by their ability to rectify, switch or amplify signals. On the other hand, passive components neither add any gain or amplification to the signal nor can they perform switching functions. They absorb and dissipate energy provided by active components. Major passive components in a system are resistors, capacitors and inductors.

Embedding actives and passives into the high-density substrate is an important technology that leads to small form factor systems with very high electrical performance. The technological attributes are same generally for embedding discrete passives or

actives so in this section embedding of active ICs is briefly discussed. Passive component technologies are discussed in the next section (1.2.2)

Chips can be embedded into the substrate or build up layers in three ways:

1) Chip-first: In this approach, embedding starts with the IC and the buildup of wiring generally takes place around it. Though this technology results in better electrical performance, it has many disadvantages such as yield loss, no reworkability as well thermal management issues.

2) Chip-Middle: In this approach, embedded chips end up in the middle of the build-up substrate. However this approach also suffers from similar drawbacks as chip-first such as low yield, no reworkability and thermal management.

3) Chip-Last: In this approach, the high-density substrate is build first and then the chip is embedded into it. Thus this allows for i) low process and yield loss, ii) reworkability as the defective chips can be taken out and replaced, iii) shorter interconnects and iv) better thermal management as the backside of the chip is directly exposed to the air and can also be bonded to a heat-sink.

1.2.2 Passive Components

Passive components such as resistors, inductors and capacitors form the majority components in any electronic system. A typical mobile product has 10 times more passive components than the active components. They perform various important functions such as decoupling, sensing, bias, termination etc. in a circuit and hence they are indispensable. These components are available as discrete components but that leads

to large board area and decreased electrical performance of the system. Integrating these passive components as thin film components into the package leads to significant miniaturization and also improves the electrical performance by using shorter interconnections between the chip and the package. It can also result in reduced packaging costs, low power loss, low volume, low weight and low profile [5]. These broadly include power supply components such as capacitors and inductors as well as RF components such as antennas and filters. These are briefly described below:

1.2.2.1 Power supply components

Portable multifunctional systems typically operate with 10-15 power rails on multiple voltage levels. Capacitors are widely employed for voltage conversion and ripple-free voltage supply over a broad frequency range. Thin film power supply capacitors have been the biggest barrier for system miniaturization because of the lack of low-cost, low temperature thin film material and process technologies with high permittivity that are compatible with silicon and organic substrate technologies. High-density capacitor technology needs are discussed in more detail in section 1.2.3

Power conversion for portable applications that demand high current with high efficiency depend on inductive energy storage elements. Inductors on silicon do not meet either the Quality Factor (Q) or the size requirements for several applications such as RF power amplifiers, DC-DC power converters, and high Q RF components. Costly MEMS fabrication routes are frequently invoked to increase the inductance density and the quality factor. Novel magnetic nanocomposite layers with innovative silicon and organic

substrate compatible fabrication techniques are being developed to miniaturize inductors while retaining their high frequency stability and Q[8].

1.2.2.2 RF components

RF front-end modules form the backbone of any mobile communication product. With emerging handsets supporting multiple bands at higher frequencies, components for supporting various RF functions such as antennas, oscillators as RF power generators, filters, and Analog-to-Digital convertors become the biggest challenge. The most important RF components include signal inductors, signal capacitors, decoupling capacitors, terminating resistors and signal resistors. In conventional packages, most of these RF components are present as discrete surface mount devices. For high frequency applications, the physical dimensions of these interconnects become a significant portion of the signal wavelength, thus inducing large number of parasitics. Using the system-on-package technology, the entire system, including digital devices and the RF front end, can be integrated into a single package. This methodology has many advantages as described in section 1.2. However, embedding RF components requires a new generation of low-loss stable dielectrics with high permittivity and permeability using organic-compatible processes. This forms the biggest challenge for RF module integration in a package.

1.2.2.3 Sensing components

Integration of bio and chemical sensing with wireless and digital signal processing using the SOP concept can lead to the next-generation mega-functional systems with real-time

health monitoring, early disease detection and therapy and improved home-land security. To detect biological and chemical species, large and cumbersome analytical methods are used. The probes and sensors used for this purpose are not only huge but also take a lot of time to analyze the results. Emerging detection methods based on nanoscale sensing elements are capable of detecting gases and biomolecules at ultra-low concentrations. Using nanopackaging technologies, it is possible to integrate these sensors with electrical, optical and mechanical functions resulting in an ultra-miniaturized, portable and low power, ultra light weight, autonomous bio-sensing systems.

1.2.2.4 Thermal Structures

Thermal management remains to be the showstopper for realizing ultra miniaturized and mega functional systems. The ITRS power dissipation projection of 350W/cm^2 by 2020 will be higher if the IC's are implemented in a 3D stacked IC or SOP configuration. Current passive and active cooling techniques may not be sufficient to meet the demands of such devices and hence novel materials as well as processes need to be designed. Although a variety of Thermal Interface Materials (TIM) such as solders, phase change materials, and polymer composites have been used in the IC industry, the low thermal conductivities (~2 W/mK) limit the thermal management in high power ICs. Therefore novel materials and processes need to be designed to meet these thermal challenges. Novel and highly conducting, compliant and gap filling interface materials such as carbon-nanotubes and thin solder nano-composites can be used as thermal interface materials in next generation electronic packages.

1.3 Power Supply as a grand challenge – need for high density capacitors

The trend towards ultra miniaturized, multifunctional consumer and mobile electronics and mobile healthcare systems imposes unprecedented size and storage density demands. The operating voltages and power levels are becoming increasingly varied with multiple devices working at different levels to serve various functions. Portable consumer products operate with 10-15 power rails on multiple voltage levels. Power convertor modules are incorporated in various parts of the system to step-up or step-down the battery voltage and current to address these diverse current and voltage requirements. A typical voltage convertor consists of an active network that works in conjunction with power storage components such as capacitors and inductors to perform the voltage conversion. Capacitors are also used in most power supply modules as noise filters. For low-current but stable voltage requirements, charge-pumps or linear regulators that depend on high-density capacitors are frequently used. Power conversion that require high current with high efficiency are based on switching regulator topologies that depend on inductors.

In summary, while the active components are migrating to nanoscale with CMOS scaling combined with 3D stacked architectures, the energy storage components that are critical for any power conversion, are still at microscale within the storage device and milliscale outside the device, making them the bulkiest component in a mobile system. Passive components such as capacitors and inductors, therefore, remain as the biggest bottlenecks in system miniaturization.

1.3.1 Decoupling for high-speed digital applications

In digital or mixed signal application circuits, the simultaneous switching of circuits cause voltage variation across all circuits that are on the same power rail. This results in noise. Decoupling capacitors help in suppressing this noise. These capacitors should have low impedance at high frequencies and should be able to retain the capacitance at all relevant frequencies. High-speed digital applications operate over a broad range of frequencies and hence they require a large number of decoupling capacitors in different frequency domains. Further, to minimize inductance coming from interconnections, decoupling capacitors are required to be placed as close to the IC as possible.

Embedding the decoupling capacitors enables miniaturization and also helps in placing these capacitors close to the IC. Current approaches for embedding involves planar thin film capacitors, polymer-ceramic capacitors and embedding surface mount capacitors such as MLCC and Ta capacitors. Surface mount decoupling capacitors such as MLCC or Ta capacitors are ineffective at higher frequencies because of their inherent high inductance and additional inductance coming from the package. Planar capacitors typically use ferroelectrics but they generally show temperature and voltage dependent behavior. All these approaches will be discussed in great detail in Chapter 3.

1.3.2 Voltage convertors and regulators

In mixed signal applications, where products operate at multiple voltage levels, voltage convertors and regulators are used to step-up or step-down the battery voltage and current

to address the diverse current and voltage requirements of different applications. These voltage convertors or regulators also help to maintain a constant voltage level at the load. They achieve this by sensing the voltage near the load and adjusting the output current to regulate the voltage [6]. Voltage convertors and regulators can be classified as capacitor-centric, for example charge pumps or linear regulators, and inductor-centric such as switching convertors. For capacitor centric regulators, the typical capacitance requirements range from 5 μF to 10 μF. Such capacitance values are traditionally met by using large and bulky capacitors. To obtain the same capacitance at millimeter scale dimensions of the capacitor, capacitance density of more than 100 $\mu F/cm^2$ is desired. Currently, there is no capacitor technology that can meet such high capacitance density demands cost effectively and hence there is a need for developing novel capacitor technologies with ultra-high capacitance densities.

1.4 Objective of the study

The aim of this study is to develop a novel silicon-compatible particulate electrode based capacitor with microfarads of capacitance to meet the advanced voltage regulation and power supply needs of emerging bioelectronics as well as consumer electronic market.

The objectives and targets for this research are:

- To explore and optimize a novel particulate electrode structure for high-density capacitors by sintering metal particles to achieve 15X enhancement in area over trench capacitors with atleast 15 V breakdown voltage.

- To study the conformality of the dielectric deposited by using Atomic Layer Deposition process on complex particulate electrode structures

- To study and develop conducting polymer electrodes for use as top electrode in the above capacitor structure.

1.4.1 Challenges and barriers

There are several major challenges with the proposed approach. These are:

- Forming and sintering porous particulate electrode as thin interposers that are silicon stack compatible
- Conformal dielectric thin films on presumably rough and high surface area particulate electrodes
- Top electrode material and process that can easily penetrate the complex particulate electrode structure but does not chemically interact with the dielectric.
- Reliability and stability with thin film dielectrics over particulate electrodes

1.4.2 Proposed approach to address barriers

This section describes the approach followed in this study to address the above-mentioned challenges and barriers. These are also shown in Table 1.1

Table 1.1 Proposed approach to address barriers

Challenges and Barriers	Approach to address barriers
To develop an open porosity structure on silicon	• Use standard paste printing techniques, print copper paste on silicon and sinter • Characterize for porosity
Conformality of ALD on particulate electrode	• Characterize electrical properties of ALD Alumina process on planar electrodes • Use SEM and EDS to study conformality of ALD Alumina on particulate electrodes
Top electrode selection and compatibility	• Explore and optimize the conducting polymer PEDOT as top electrode by using planar alumina film • Study the interaction of conducting polymer with metal oxide dielectrics using planar alumina and tantalum pentoxide films • Study the penetration on particulate electrodes using SEM, EDS etc.

Copper powder is used to prepare the porous bottom electrode. A paste is formed by using copper powder, a sacrificial polymer and a suitable solvent. This paste is printed onto the silicon substrate and sintered in the temperature range of 400-600^{o}C to achieve a 3D porous structure. Alumina is used as the dielectric and is deposited by using Atomic Layer Deposition. Finally the capacitor structure is completed by using polyethylene dioxythiophene (PEDOT), which is a conducting polymer, as the top electrode. Extensive electrical characterization including DC leakage measurement testing and impedance spectroscopy are performed on these test structures and the observed properties and

results are correlated to the morphology and structure of the devices by using characterization techniques such as high resolution scanning electron microscopy (SEM) and energy dispersive x-ray spectroscopy (EDS).

Chapter 2 provides a discussion on various issues mentioned in the literature with regards to this work. Current state-of-the-art capacitor technologies along with the materials and processes are described in great detail. The advantaged and limitations of the proposed approach are also discussed.

Chapter 3 describes all the fabrication and synthesis steps involved in making these particulate electrode capacitors. Details about all the experimental and characterization techniques used in this study are also provided.

Chapter 4 covers the results and discussions pertaining to the fabrication and electrical characterization of high-density particulate electrode capacitors. The conclusions and recommendations for future work are presented in chapter 5.

2 BACKGROUND

This chapter summarizes various materials and processes reported in literature for power supply and decoupling capacitors. The current state of the art capacitor technologies to meet the power supply demands are described in detail along with their limitations. A classification scheme based on their silicon compatibility and structure (planar or 3D) is also presented. Detailed description of the key materials and processes used in this study are also described.

2.1 Current Approaches/ State of the art

For any capacitor, the capacitance can be calculated using the formula given in equation 1 below

$$C = \varepsilon_o \varepsilon A/d$$

Where C is the capacitance, ε_o is the permittivity of free space, ε is the dielectric constant of the material, A is the area of the electrode and d is the thickness of the dielectric film. It can be seen from equation 1 that all basic capacitor technologies depend on one or all of the following three fundamental parameters in order to meet their capacitance:

1. Surface area enhancement
2. Thinner dielectric films
3. Higher permittivity dielectrics

Based on these parameters, capacitor technologies can be classified as either planar thin film capacitors that depend on thin film dielectrics or 3D capacitors that benefit from

surface area enhancement. Alternatively, these capacitor technologies can also be classified based on their silicon compatibility. Planar capacitors can be easily integrated on silicon but they result in very large area devices in order to achieve higher capacitance densities[6]. On the other hand some 3 D capacitors such as multilayered ceramic capacitors (MLCCs) or Tantalum particulate capacitors that are capable of providing very high capacitance density cannot be easily processed on silicon. Figure 2.1 shows a broad classification of various available capacitor technologies.

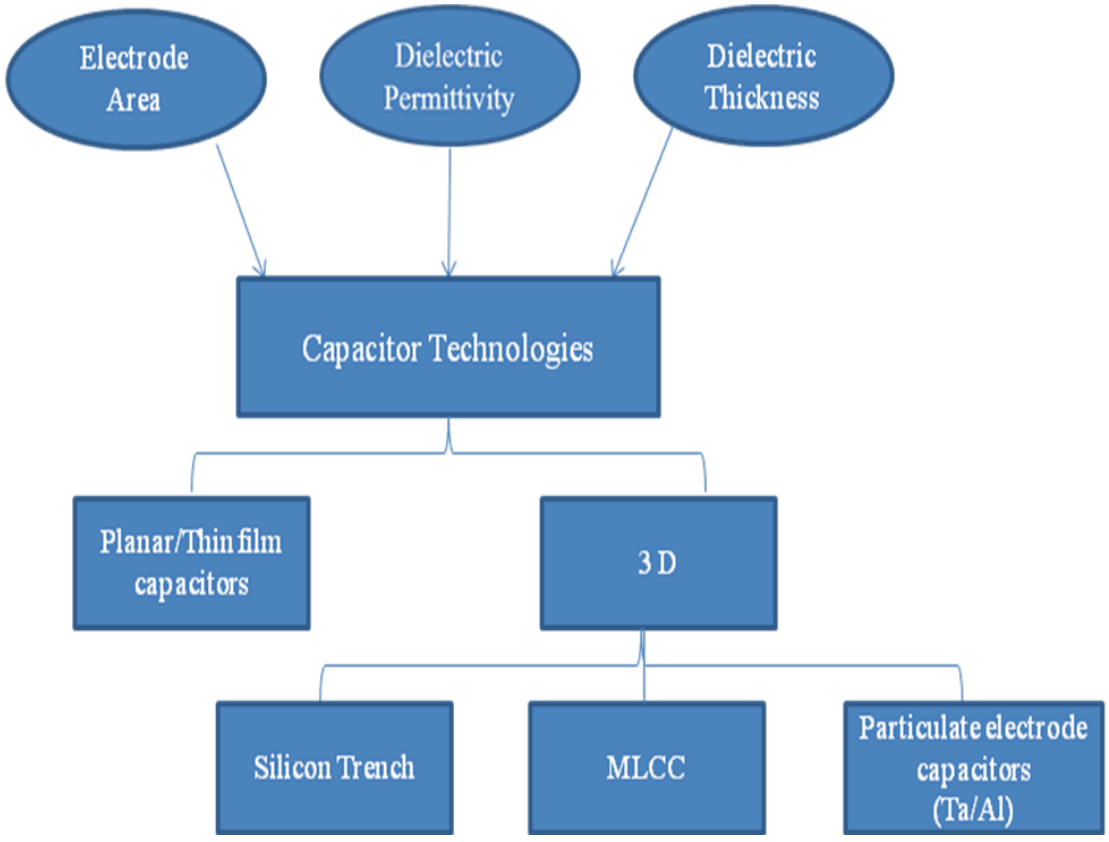


Figure 2.1 Classification scheme of capacitors

2.1.1 Planar thin film capacitors

Thin film capacitors are perhaps a very simple realization of a parallel plate capacitor model. These are very easy to integrate on silicon but often lead to large area devices.

As capacitance is directly proportional to permittivity and inversely proportional to the thickness of the dielectric film, these capacitors depend on thinner and higher dielectric constant films to achieve high capacitance values. Even though materials with permittivity in the range of 8-1000 are available, it is not possible to obtain very high capacitance densities with adequate breakdown voltage (BDV) and leakage current range. Typically, higher permittivity films have lower breakdown strength and thus these need to be thicker in order to meet the BDV requirements[7]. This is depicted in Figure 2.2

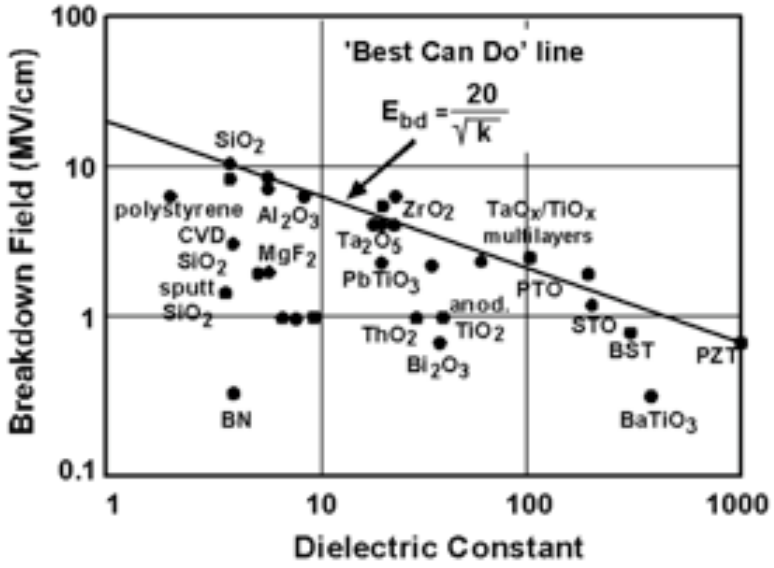


Figure 2.2 Relationship of BDV with dielectric constant for various materials[7]

Figure 2.2 indicates that out of all available dielectric materials, oxides, nitrides and oxynitrides have the highest breakdown voltages. This implies that these dielectric films can be easily thinned down to a few nanometers without compromising on their reliability. These materials have dielectric constants in the range of 5-7 and thus these are also known as low dielectric constant films. These technologies are very compatible with front end semiconductor processing and it is very easy to integrate devices on silicon, as the processing temperature of these films is seldom higher than 300^{o} C. Moreover, the coefficient of thermal expansion (CTE) of these films is very close to silicon so there is no issue of thermo mechanical incompatibility. For example Si_3N_4 having a dielectric constant around 7 can be directly deposited over silicon by Plasma enhanced chemical vapor deposition (PECVD) at 250^{o} C. C.T.E of Si_3N_4 is 3 ppm/K, which is almost equal to the C.T.E of silicon (2.3 ppm/K). The typical capacitance densities of such capacitors are around 0.2-0.3 $\mu F/cm^2$. Such capacitors are mostly used for high frequency RF components where capacitance demands are not very stringent (1 pF – 100 pF) but the focus is on achieving the required capacitance with low loss and low temperature dependence [8].

Oxides of certain metals, such as aluminum, hafnium or zirconium, show additional ionic polarization resulting in permittivities ranging from 8-80. These oxides have breakdown strength in the range of 500-800 V/micron and are mostly developed for use as gate dielectric in CMOS devices beyond 45 nm [9]. An important requirement for gate dielectrics is their extremely low leakage current. Hence, it is imperative that the band gap of the material be high as a larger band gap means low leakage current. At the same

time, a higher band gap material has generally lower permittivity. Figure 2.3 shows how band gap varies with dielectric constant for various materials[10] .

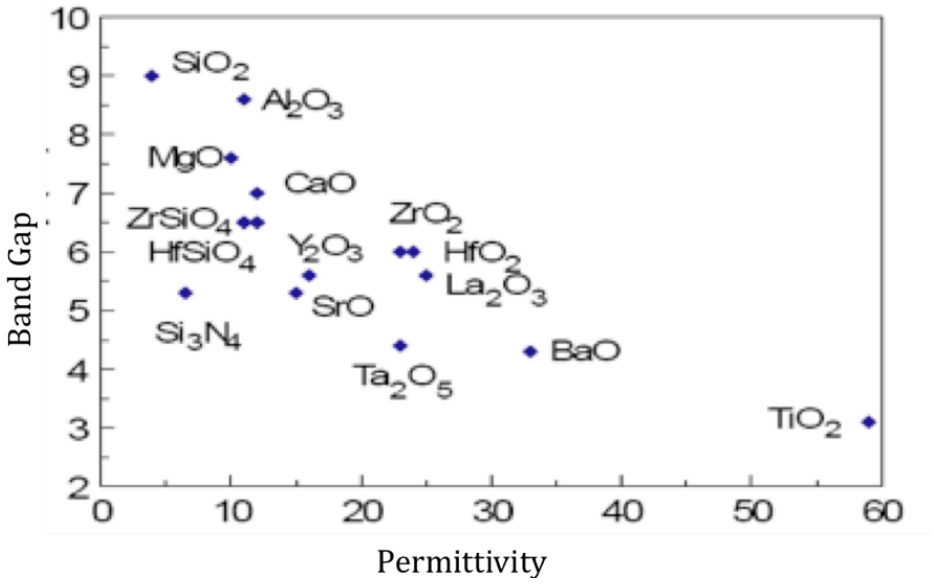


Figure 2.3 Band gap vs. dielectric constant for various materials[10]

Process classification:

These thin films can be deposited by using a variety of thin film deposition techniques such as Chemical vapor deposition (CVD), RF sputtering and Atomic layer deposition (ALD). Out of these ALD is perhaps one of the most important technologies because it leads to uniform, conformal and defect free coatings. This technology is discussed at length in section 2.1.3.1

Anodization is another important technology that can be used to yield films with moderate dielectric constant. Films of valve metals such as tantalum, aluminum and niobium can be easily anodized to yield their corresponding oxides. This technology however is more prevalent in case of particulate electrode and will be discussed in section

2.1.4. These moderate dielectric constant films can generate capacitance densities around 0.2 $\mu F/cm^2$.

For power component applications, where higher capacitance densities are required (1 - 1000nF), higher dielectric constant films are used to make smaller and thinner form factor devices. In organic packaging domain, polymer ceramic composite thick films are employed to attain high capacitance densities. These films have permittivity in the range of 15-20 but are generally thicker (15-20 microns) and are not silicon compatible because of high temperatures associated with them. To make silicon compatible high-density planar capacitors, high dielectric constant ferroelectric films with permittivity around 5000 are used. The breakdown voltage (BDV) of these films is about 50-500V/micron and that requires these films to be thicker. This is the reason that a capacitance density of only 2-3 $\mu F/cm^2$ can be obtained from these films as opposed to an expected 4-5 $\mu F/cm^2$. There are several factors that limit this high k film technology and these are listed below:

- Lower BDV that requires thicker films
- Dependence of permittivity on particle or grain size as well as thickness reduction
- Susceptibility to defects that leads to conduction and hence lossy films
- Interfacial defects or interfacial reactions that lead to a lower effective dielectric constant of the film [11, 12]

Based on all the above discussion about planar thin film capacitors, it can be seen that the maximum capacitance density obtainable from them is limited to 4-5 $\mu F/cm^2$.

Table 2.1 compares the capacitance densities obtained by various planar thin film technologies that adequately meet the voltage and leakage current requirements. These may be sufficient for some RF component application but they cannot meet the ever-increasing voltage regulation and power supply demands for futuristic portable consumer products and bio-medical industry. To attain higher capacitance densities, 3D capacitors are needed and these will be the focus of the following sections.

Table 2.1 Thin film capacitor materials than can withstand 25 volts

High K ferroelectrics Barium titanate Lead-based perovskites	Lower breakdown voltages require thicker films K reduces with film thickness	ε = 3000; t = 1 um	3 $\mu F/cm^2$
High K superparaelectrics Strontium titanate, BST	Dielectric constant low but stable with lower loss	ε = 600; t = 150 nm	4 $\mu F/cm^2$
Moderate K paraelectrics Tantalum oxide	Higher breakdown voltages allow thinner films	ε = 40 t = 40 nm	1 $\mu F/cm^2$
Oxides and oxynitrides	High BDV allows 30 nm films Standard semiconductor tools	ε = 8 t = 30 nm	0.2 µF/cm2

2.1.2 Multilayered ceramic capacitors (MLCC)

Multilayered ceramic capacitors consist of multiple stacks of metal electrodes and dielectric films that are alternately connected to form a layered capacitor structure. Volumetric efficiency of these MLCCs increases with decrease in the dielectric and electrode thickness as that implies more number of layers can be packed for the same

equivalent thickness of capacitor structure. These dielectric films are cast by using fine-grained ceramic powder dispersions such as barium titanate. The electrode is in the form of a metal dispersion in a suitable organic solvent. The end connections are often terminated at the sides by using metal paint most commonly silver palladium paint. These paint typically require high firing temperatures in the range of 700-800^{o}C [13]. A schematic cross section of MLCC showing current direction is shown in Figure 2.4

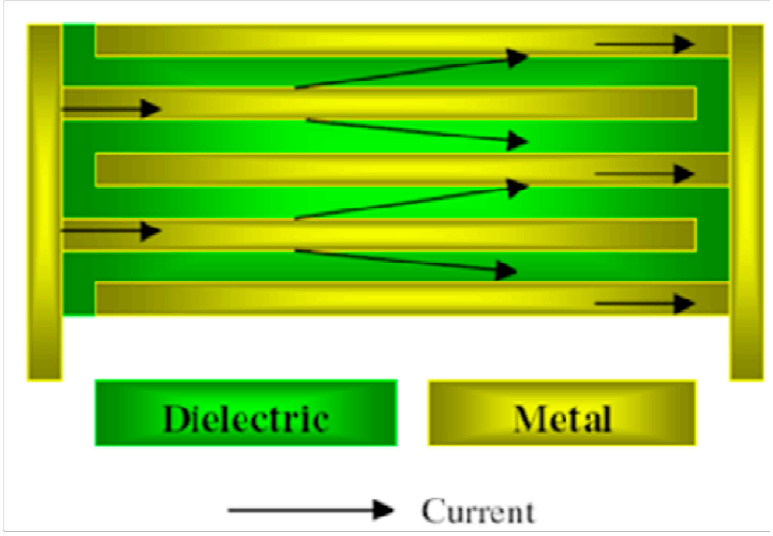


Figure 2.4 Schematic cross section of MLCC[1]

This technology has been around for years and thus is a very mature technology with volumetric efficiency doubling almost every 14 months. Kemet, AVX, Panasonic, Murata and Vishay are some of the leading MLCC suppliers.

As already stated, the volumetric efficiency of these capacitors depends on electrode and dielectric thicknesses that are continuing to decrease at a steady pace. However as the dielectric thickness approaches a few hundred nanometers, the lower BDV and higher leakage current pose serious reliability issues. These capacitors are most commonly used

as surface mount decoupling capacitors. They often suffer from very high inductance that renders them ineffective at higher frequencies. These capacitors are not silicon compatible and their size also hinders system level integration and miniaturization.

2.1.3 Silicon Trench Capacitors

Trench capacitors are fabricated by etching holes or trenches in silicon. Etching creates side-walls leading to higher surface area and enhanced capacitance densities. These capacitors were originally introduced in 80's for miniaturizing the stortage capacitor in DRAM modules. The ratio of the surafce opening to the depth of the trench is termed as aspect ratio. Over the years, higher aspect ratio trenches have been used to achieve higher and higher capacitance densities,. However, as will be discussed in this section, it is both very challenging as well as expensive to etch, metalllize and deposit a conformal dielectric on these silicon trenches. Based on the etching conditions, silicon trench processes can be classified either as wet etching or dry etching processes. Wet etching is a low cost anisotropic process whereas dry etching is expensive but can be directional[15].

Bosch process is the most common method of etching silicon. It is a dry-etching process that utilizes high energy ions to etch silicon (typically SF_6) while the side-wall is passivated with a Teflon polymer. This side-wall passivation gives directionality to the process [14]. Figure 2.5 shows a typical Bosch process flow using SF_6 as the etching

species and C_4F_8 as the passivation layer. Bosch process is expensive. Therefore, wet etching is frequently used to create low-to-medium aspect ratio trenches[15] .

Conformal dielectric deposition is the most important aspect of trench capacitor fabrication. Traditionally chemical vapor deposition (CVD) techniques have been used for dielectric deposition in these trenches. Liquid phase CVD (LPCVD) and thermal oxynitridation result in conformal and uniform coatings that are compatible with active circuitry and hence these are widely pursued as the oxynitride deposition route.

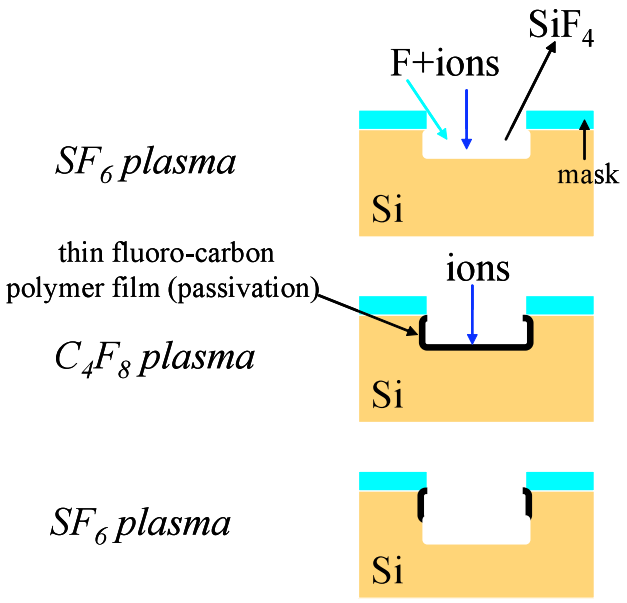


Figure 2.5 Typical Bosch process flow[14]

For DRAM applications, silicon dioxide is the most commonly used dielectric material because of its compatibility with silicon and high breakdown strength. To obtain higher capacitance densities, oxide dielectrics are often replaced by nitrides [16]. Though CVD

has been the preferred route for dielectric deposition on trenches, this process cannot support dielectric deposition on very high aspect ratio (>50) trenches that are needed to increase the capacitance density. Films deposited by CVD are not very conformal in high aspect ratios trenches. Research and development on conformal dielectric deposition is mostly based on a comparatively new Atomic Layer Deposition (ALD) technique. ALD is the most versatile technique to deposit high dielectric constant, defect free, uniform and conformal films on high aspect ratio features. Due to its unique nature and its capability to coat high aspect ratio surfaces uniformly, this technology is very critical for emerging high-density capacitor technologies, and hence is discussed in detail below:

2.1.3.1 Atomic Layer Deposition

Atomic layer deposition (ALD) is used for depositing thin, conformal and defect-free inorganic film structures on large and complex surfaces down to a few nanometers thickness range. ALD is widely pursued for depositing moderate permittivity films such as hafnia and zirconia as gate dielectrics. Shrinking dimensions and increasing aspect ratios in silicon based microelectronics have further fueled the need for the development of ALD based deposition techniques[17, 18] .

The principle of ALD is based on sequential pulsing of precursor vapors into the chamber, each pulse separated by inert gas purging. These reactions are self-terminating and that results in the deposition of one monolayer of reactant species during each pulse. Thus one ALD cycle consists of four steps:

- Step 1 – Introduction of first reactant/precursor in the chamber
- Step 2 – Inert gas purging to evacuate the chamber and get rid of all the unreacted reactant vapor
- Step 3- Introduction of second reactant/precursor in the chamber
- Step 4- Inert gas purging to evacuate the chamber and get rid of by-products of the reactants.

The schematic of a typical ALD cycle is shown in the Figure 2.6 as shown by R. Puurunen[19] . The thickness of the deposited film can be easily controlled by controlling the number of cycles.

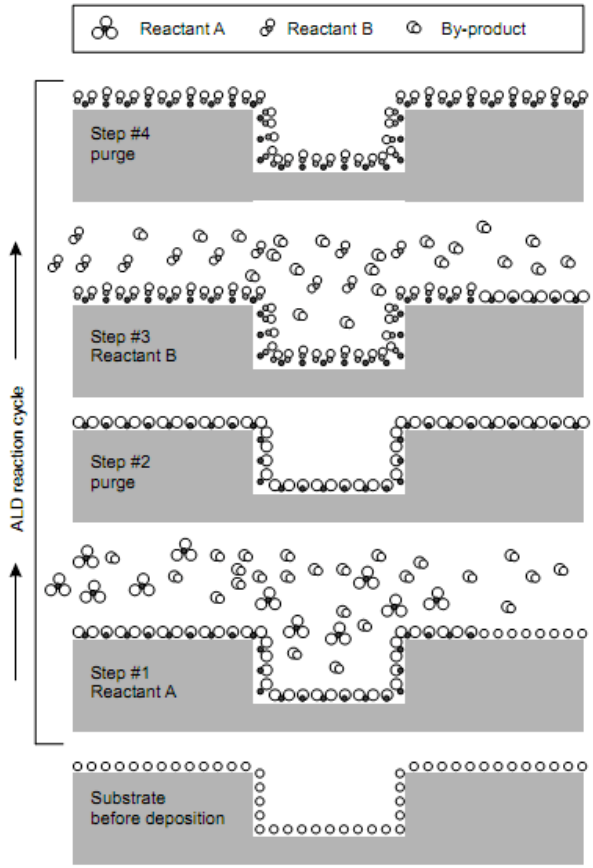


Figure 2.6 Schematic of ALD growth[19]

ALD is a surface-controlled process because it uses self-terminating reactions. This results in the deposition of highly conformal and uniform thin films [19]. A typical ALD process is independent of the deposition time as it depends only on the number of precursor cycles. It depends on the formation of strong chemical bonds between the reactant species with the substrate and this requires overcoming certain activation energy barrier. The energy to overcome this barrier can be provided by temperature, UV radiation or plasma. When this activation energy barrier is overcome, the reactant that is pulsed into the chamber gets chemisorbed on the surface to form one monolayer. When the whole surface is saturated with the reactant species, the reaction automatically stops due to lack of available sites. Thus, as long as there is sufficient availability, the precursor covers all the reactant sites. Under these conditions, the deposition happens independent of the precursor dose [20-22]. The conformal nature of ALD films is widely reported in the literature. SEM image of a silicon trench structure demonstrating uniform step coverage of ALD Al_2O_3 and TiN by Ritala et al. is shown in **Figure 2.7** [23].

Another very important aspect of ALD is that it enables the deposition of thin films at relatively lower temperatures. ALD has wide processing window which makes it very easy to control. To make sure that the deposition happens in the ALD mode, the temperature should always be within the "ALD window" as illustrated in Figure 2.8. For example in case of a thermal ALD, the reaction will not take place if the temperature is too low to overcome the activation energy barrier. This limit is little bit more relaxed in

case of plasma enhanced ALD. Again, the temperature should not be so low so as to cause precursor condensation or so high so as to cause precursor decomposition. In some cases, if the temperature is too high, it also causes the re-evaporation of the chemisorbed layer leading to a decreased growth rate [24].

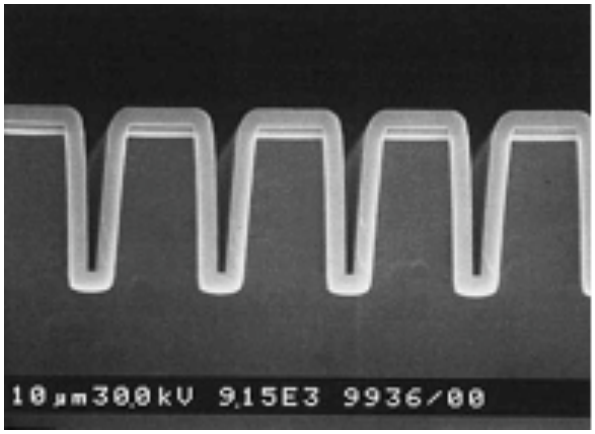


Figure 2.7 Cross sectional image of a Si trench showing uniform step coverage by ALD Al_2O_3 [23]

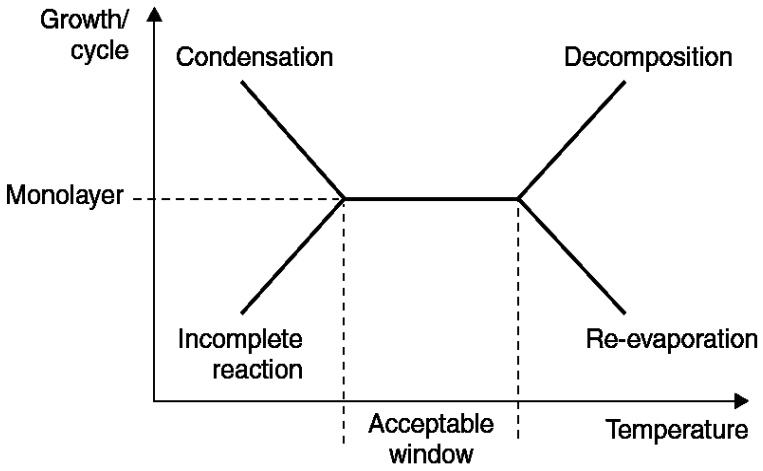


Figure 2.8 ALD process window adapted from ref [24]

In order to obtain uniform step coverage and excellent conformality, it is very important to maintain an adequate dosage of the precursor material. While dealing with very high aspect ratio features, it is also imperative that sufficient time be provided for the diffusion of molecules to take place. The product of the partial pressure of the precursor (dosage) and the pulse time is used to calculate the exposure of the substrate to the precursor. When precursors are exposed to high aspect ratio complex features, the flat surface gets coated first and after that deposition in holes or trenches begins [25, 26]. Inadequate exposure will lead to thickness non uniformity at the top and bottom surfaces as shown in Figure 2.9 by Elam et al.[25]. They deposited Al_2O_3 on high aspect ratio hollow anodic aluminum oxide templates (AAO) and observed that the Al_2O_3 film thickness deposited on top and bottom was higher as compared to middle when the exposure times were not sufficient.

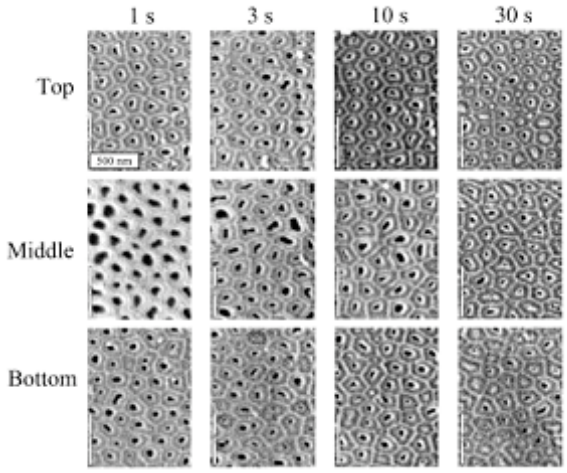


Figure 2.9 Effect of exposure time on ALD Al_2O_3 conformality on porous anodic aluminium oxide template [25]

There are a wide variety of materials that can be deposited using ALD. The most common use of ALD is to deposit binary metal oxides such as Al_2O_3, HfO_2, ZrO_2, TiO_2, Ta_2O_5 etc. The typical metal precursors utilized for metal deposition are halide, alkyl or metal alkoxides. Other precursors can also be used as long as they have enough volatility or vapor pressure and are stable at the reaction temperature. For binary oxides, H_2O is the most commonly used oxidizer. [18, 27-29]. It is also being extensively exploited to deposit high dielectric constant ternary films such as $SrTiO_3$ or $BaTiO_3$. These films are capable of giving permittivity values close to 200 after annealing and hence can be used to develop next generation DRAM devices.[30, 31].

ALD Al_2O_3 is, by far, the most developed and studied metal oxide system. It can be deposited at temperatures as low as 200^o C and is known to give a permittivity value of 7-9 [32]. The most commonly used precursors for Al_2O_3 are trimethylaluminium (TMA) and water [18, 19].

Capacitance density equivalent to 40 $\mu F/cm^2$ has been reported using layered structures of ALD Al_2O_3 and HfO_2 on silicon trenches to form metal-insulator-silicon and metal-insulator-metal capacitors[33]. A similar stacked capacitor for deep-trench DRAM applications showing good electrical and thermal properties was also shown by Tung-Ming Pan et al.[34].

Inspite of all the advances in trench capacitors, Si trench capacitors still constitute only about 10% the total capacitor market because of the following reasons:

- Multiple stacking of different ALD layers makes it difficult to establish electrical connections
- Slow nature of ALD process makes the overall process very expensive
- To further increase the capacitance density, ultra high aspect ratios are desired and that poses a serious challenge towards silicon etching capability as well as dielectric deposition using ALD.

2.1.4 Electrolytic capacitors – Aluminum and Tantalum

Electrolytic capacitors are capable of providing very large capacitance densities. They achieve this by coupling the benefits of using an ultra thin dielectric film with a very large surface area. First generation electrolytic capacitors consisted of a liquid electrolyte but such capacitors had very poor low temperature performance. The conductivity of the liquid electrolyte depends on the mobility of the ions. The mobility of the ions decreases with temperature, thus lowering the electrolyte conductivity. These liquid electrolytes were thus replaced by solid electrolytes to improve performance and reliability of the capacitors. The two most common types of electrolytic capacitors are based on aluminum and tantalum and are discussed below.

2.1.4.1 Aluminum Electrolytic Capacitors

In its simplest form, aluminum electrolytic capacitors consist of two etched aluminum foils, one of which is coated with a very thin layer of aluminum oxide. These two etched

aluminum foils are separated by using a spacer immersed in an electrolyte that acts as the cathode. Extremely thin dielectric layer coupled with the increased surface area due to etching of the foils results in very high capacitance densities. The dielectric is grown by dipping the foil in an electrolyte usually an adipate or phosphate salt [35]. The thickness of the oxide depends on the applied voltage. Figure 2.10 shows a schematic of aluminum electrolytic capacitor[35]. The electrolyte that acts as cathode can either be liquid or solid. Traditionally materials such as TCNQ[36, 37] and MnO_2 have been employed as solid electrolytes but these materials have higher resistivity that leads to increase in equivalent series resistance (ESR) .

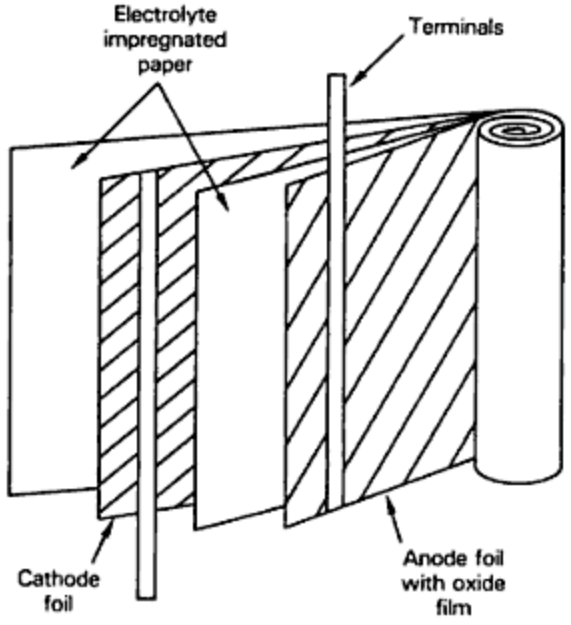


Figure 2.10 Construction of Aluminum electrolytic capacitor [35]

Conducting polymers such as polyaniline and polypyrrole with higher conductivity are increasingly being used as cathode materials. Capacitors with polypyrrole have very low ESR and are often termed as SP-CAP or specialty polymer capacitors [38-40]. Some of these materials will be discussed in more detail in a later section. Once the required

cathode material is formed, the foils are rolled in stacks and finally packaged in the form of a cylinder.

Electrolytic capacitors are highly polar. For reliable operation, the anode should always be positive and cathode should always be negative. Reversing the polarity causes the electrolyte reaction to be reversed. This results in the formation of the oxide at the cathode as well. This oxide film formation is accompanied by a lot of heat and thus often causes the capacitor to burst or fail[35].

2.1.4.2 Tantalum Capacitors

Tantalum capacitors can be either in the form of a foil (similar to aluminum electrolytic capacitors) or sintered body. The most common and popular type of tantalum capacitor is in the form of a porous sintered body, anodized to obtain tantalum pentoxide (Ta_2O_5) and coupled with a solid electrolyte such as MnO_2 or conducting polymer. Ta_2O_5 has a dielectric constant around 25, which is 3 times more than that of Al_2O_3. Thus Ta capacitors benefits both from a higher surface area and dielectric constant.

Tantalum capacitors are manufactured from powder, either in the form of grains or flakes that are formed into a pellet around a single tantalum wire protruding out from the center of the structure. This pellet is then sintered at a temperature around 1600^{o} C to form a compacted anode structure[41]. This pellet is highly porous and its structure can be compared to that of a sponge. Thus, such a particulate structure offers enormous surface area enhancement. The dielectric formation is similar to aluminum electrolytic capacitors. Anodization is carried out to convert Ta to tantalum pentoxide (Ta_2O_5). The pellet is

immersed in an electrolyte system typically consisting of an aqueous solution of phosphoric acid. The depth and thickness of the dielectric film depends on time, current and voltage of the process. Finally to form the top electrode, this pellet is then dipped in an aqueous solution of manganese nitrate and heated to a temperature of 400^{o} C. At this temperature manganese nitrate decomposes and gets converted to conducting manganese dioxide (MnO_2)[35]. After this, the top electrode is coated with carbon and silver paint to finally make electrical connections. A schematic of a Ta capacitor is shown in Figure 2.11

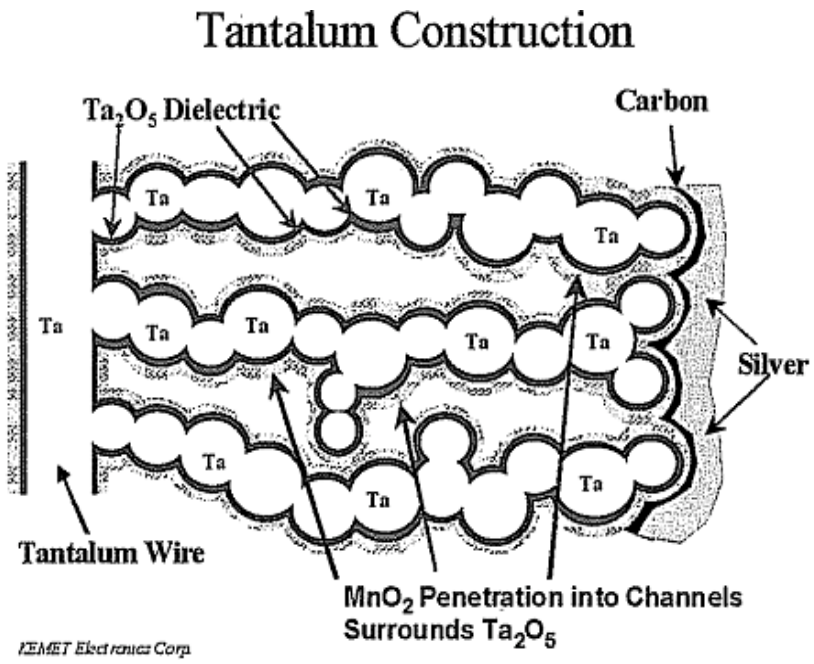


Figure 2.11 Schematic of the anode and cathode in a tantalum capacitor [35]

Effect of particle size and shape

By using finer size tantalum particles, the capacitance densities can be further increased. The tantalum powder is basically characterized in terms of the product of capacitance and voltage known as "powder charge". It is a means to calculate the volumetric efficiency or

the surface area enhancement that can be obtained from a given size of tantalum powder [41, 42]. Tantalum powder with particles in the sub-micron range (~0.5 micron) carry around 30,000 to 50,000 CV/gram charge. This means that if 1 gram of such a powder is used to form a dielectric film at 30 V, then the ideal capacitance that can be obtained from the sample should be 30,000/30 = 1000 μF[41]. By controlling the shape and size of the tantalum particles very high capacitance density values can be obtained. Figure 2.12 shows how shape and size of the tantalum powder affect the capacitance density[42].

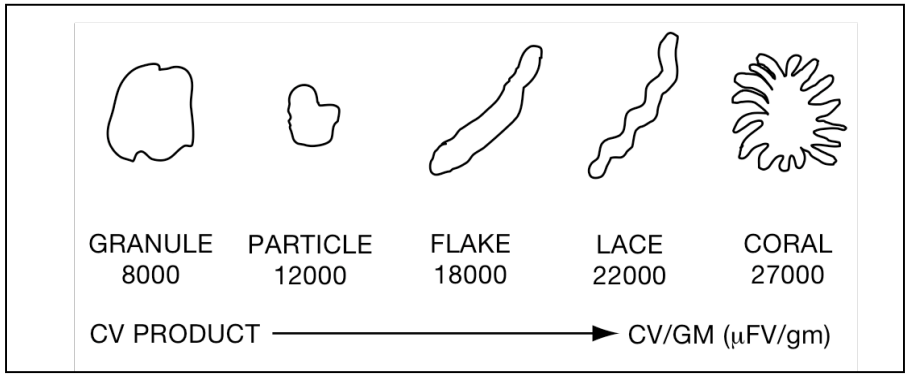


Figure 2.12 Effect of shape of tantalum powder on capacitance density[42].

It is advisable that very small size tantalum particles should not be chosen because of the risk of isolation of individual particles during dielectric formation by anodization. In anodization, the oxide not only grows on the outer surface of the metal but it also grows inside it. So if the particle is too thin or too small in size, then the metal particle is either totally consumed or completely isolated from each other.

2.2 Top electrodes for solid electrolytic capacitors

In this section, various materials that are used as top electrode with solid aluminum or tantalum capacitors are described.

2.2.1 MnO_2

MnO_2 has been the traditional material of choice for solid electrolytic tantalum and aluminum capacitors[43]. This semiconductor material is a conductive solid state oxide that can easily fill the porous tantalum electrode. MnO_2 electrodes are formed by dipping the tantalum pellet in $Mn(NO_3)_2$ solution followed by pyrolyzing the salt to convert into the oxide. This process is repeated to fill the tantalum pellet. Typically this conversion process takes place at a temperature range of 400°C to 480°C. [35, 44, 45]. A very unique property of MnO_2 is known as self-healing. This property makes it very suitable to be used in electrolytic capacitors. When MnO_2 comes in contact with a defect on the dielectric film, due to the large amount of localized current focused on that point, a lot of heat is generated. This heat converts the conducting MnO_2 to insulating Mn_2O_3, thus blocking off the site. Thus MnO_2 removes that site from the capacitor or heals the capacitor[46, 47]. This is represented by the following equation:

$$MnO_2 \xrightarrow{+heat} Mn_2O_3 + O^*$$

This self-healing behavior of MnO_2 is shown in Figure 2.13

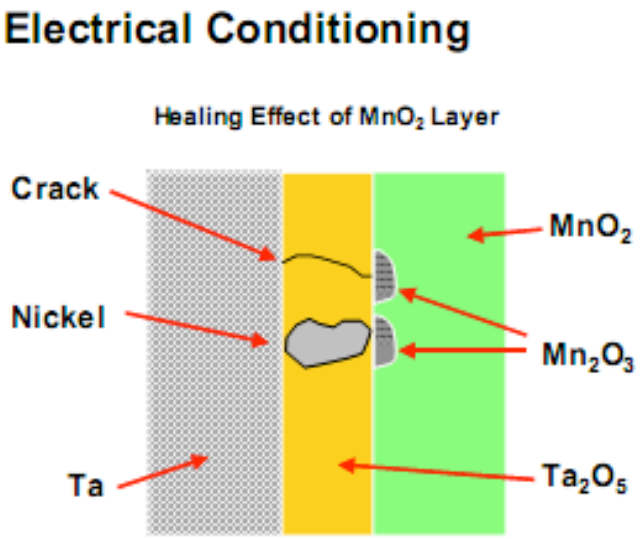


Figure 2.13 Self-healing behavior of MnO_2 electrode

There are however two major drawbacks to MnO_2 technology:

(i) High ESR – The conductivity of MnO_2 is around 10^{-1} S/cm. This results in very high equivalent series resistant values of the total capacitive circuit and leads to RC delay at higher frequencies. The arrangement is schematically shown in Figure 2.14. Due to this arrangement, the MnO_2 covering the particles at the bottom has higher resistance due to longer path as compared to MnO_2 covering the particles at the top. This results in a longer time constant for such particles. For a higher ESR value and same capacitance, the time constant would be longer for the particles lying at the bottom. This results in a capacitance loss at higher frequencies as these bottom particles will become activated at a lower frequency. This leads to

capacitance roll-off at higher frequencies and the effect is known as RC ladder effect [44].

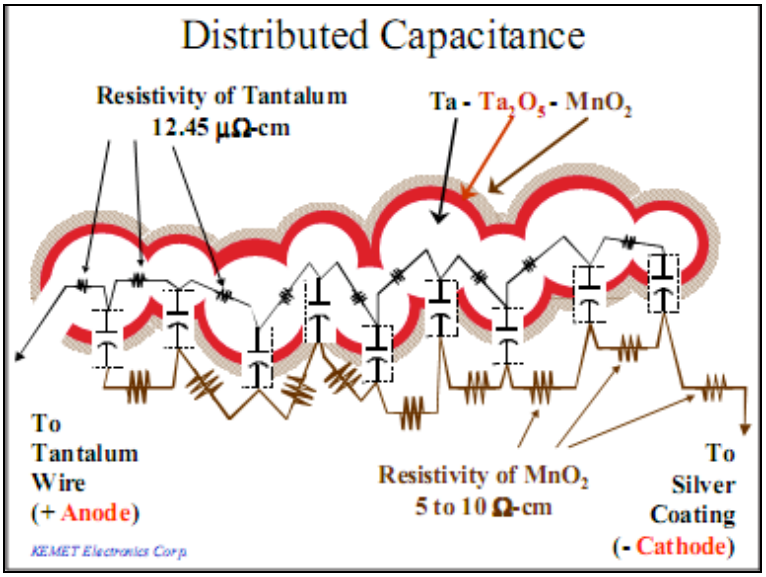


Figure 2.14 RLC ladder effect with MnO_2 as electrode

(ii) Ignition Failure: A major drawback of MnO_2 top electrode is that it leads to catastrophic failure of the tantalum particulate electrode. The conversion of amorphous Ta_2O_5 to conductive crystalline Ta_2O_5 occurs at about 500°C, which is very close to the temperature at which MnO_2 shows the self-healing behavior. This conversion enlarges the point of contact of MnO_2 with the defect site and thus further degrades the properties. MnO_2 acts as a an oxidizing source for tantalum and this exothermic reaction continues consuming all the tantalum and ultimately leads to ignition failure[47, 48].

2.2.2 TCNQ

Tetracyano-quinodimethane is a charge transfer salt that can conduct electricity[36]. TCNQ is an electron acceptor that when coupled with donor molecules such as N-methyl phenazinium (NMP) is capable of giving conductivity in the range of 0.29 S/cm to 100 S/cm[41, 49]. These salts retain their conductivity even in the molted state. They are melted at a temperature around 200^{o}C and impregnated into the porous sintered body. Aluminum solid capacitors using TCNQ have been commercially available by the name of OS-CON through Sanyo[36, 49].The main limitation of this technology lies in carefully maintaining the melting temperature of TCNQ without decomposing it. In many cases, there is an overlap between the melting temperature and decomposition temperature of TCNQ which makes it very difficult to impregnate it into the porous structure[40].

2.2.3 Polypyrrole (PPY)

Polypyrrole is an intrinsically conducting polymer that was one of the first organic polymers used in the manufacture of both aluminum and tantalum capacitors[50]. Polypyrrole has the following advantages over both TCNQ and MnO_2:

- Higher conductivity
- Ease of preparation (both chemical and electrochemical)
- Stability

For chemical polymerization, the porous sintered body is alternately dipped into the monomer and the oxidizer solution to initiate polymerization. The electrochemical polymerization involves deposition of a conductive seed layer followed by dipping the structure into the doped monomer solution. When electric current is passed through the solution, oxidation of the monomer is initiated resulting in the deposition of PPY inside the sintered structure[51, 52]

2.2.4 PEDOT

Polyethylene-dioxythiophene (PEDOT) has many advantages over conventional electrodes that make it an ideal candidate to be used as a top electrode for particulate electrodes[53]. These are listed below[54]:

- Very high electrical conductivity (300 S/cm to 600 S/cm) that leads to lower ESR values and hence mitigates the RC ladder effect seen with MnO_2 as already explained.
- Chemical and thermal stability
- Insensitivity to moisture
- Self-healing property similar to MnO_2. When the polymer comes in contact with a fault site that is drawing a lot of current, then due to the high heat generated the polymer vaporizes thus vacating the fault site. According to another theory, this polymer starts to oxidize and thus absorbs the excess oxygen generated. This makes the polymer insulating and the defect site is isolated, thus causing the capacitor to heal. This is also illustrated Figure 2.15 (a) and (b) [16, 44, 47].

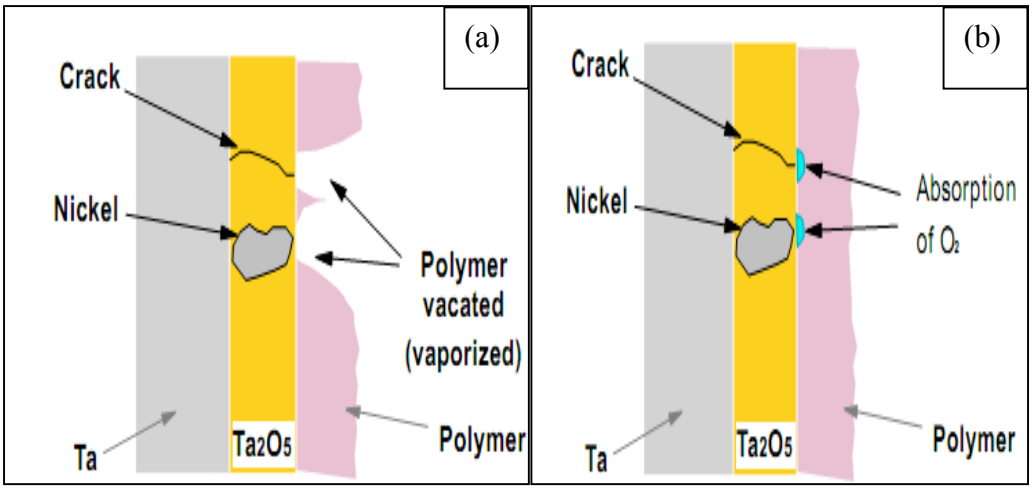


Figure 2.15 Self healing in PEDOT (a) evaporation of conducting polymer and (b) oxidation of polymer layer

PEDOT is polymerized by using iron(iii) p-toluenesulfonate as the oxidizer to polymerize ethylene dioxythiophene (EDT) monomer. This chemistry is sold commercially under the trade name of Baytron by HC Starck, Germany[54] and the structure is shown in Figure 2.16 [55].

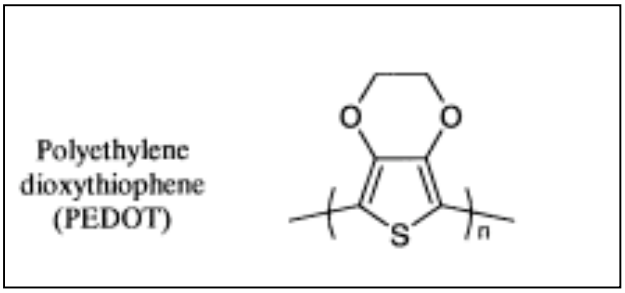


Figure 2.16 Molecular structure of PEDOT

Polymerization can be carried either in-situ where the porous electrode is alternately dipped into the monomer and oxidizer solutions or it can be pre-polymerized where the

monomer and oxidizer are mixed together in one beaker and then the porous body is dipped into it.

2.3 Limitations of the current approaches

Emerging biomedical applications require ultra miniaturized capacitors with ultra-high capacitance density above 100 μF/cm^2 with thinner geometries. These capacitors, used for DC filter and pacing applications, require very low leakage currents (30 nA/μF) and high breakdown voltages. Simple planar thin-film capacitors cannot yield such a high performance. These have to be combined with high surface area architectures with thinner interposer-like geometries to yield capacitors with the highest volumetric efficiency. Three technologies are prominent for such high-density capacitors – Trench, MLCC, and tantalum capacitors.

Silicon trench technologies are silicon compatible but they do not lead to significant area enhancement. This limits trench technologies to about 60 μF/cm^2 unless high k stack structures are used in conjunction with trenches. MLCCs are built with high k ferroelectrics. Ferroelectrics generally show temperature and voltage dependent behavior, and are susceptible to more intrinsic failure modes because of their tendency to form defects that can assist leakage and failures. Most importantly, MLCC thick film technologies are based on metal-ceramic cofiring and are not easily amenable to silicon integration. The technology is also reaching fundamental limits as the electrodes become 1 micron thick and the dielectrics approach 0.5 micron. The equivalent capacitance

densities reach as high as 150 μF/cm^2 with 6 V operations. For 15 V operations, the capacitance densities only reach an equivalent value of 50 μF/cm^2. On the other hand, with tantalum capacitors, the capacitance densities demonstrated are equivalent to 20 μF/cm^2 for 15 BDV and 140 μF/cm^2 for 6 V BDV. However, these are made by sintering Ta pellets at 1900^o C. Such high sintering temperatures make these capacitors incompatible with silicon. The leakage currents for ultrathin anodized tantalum capacitors are generally higher than MLCC thick fill ceramics.

The best capacitance density can hence be obtained by combining conformal dielectric film technologies with leading-edge high surface area geometries using next generation of particulate electrode technologies. Therefore, the objective of this study is to use a synergistic combination of thick and high surface area copper particulate electrode and thin alumina dielectric deposited using ALD to form a high density capacitor array on silicon at CMOS-compatible temperatures. This nanoelectrode capacitor approach leads to tremendous surface area enhancement which, when coupled with high permittivity dielectrics, can provide capacitance densities as high as 100 μF/cm^2. Figure 2.17 depicts the proposed research with respect to the current state-of-the-art technologies.

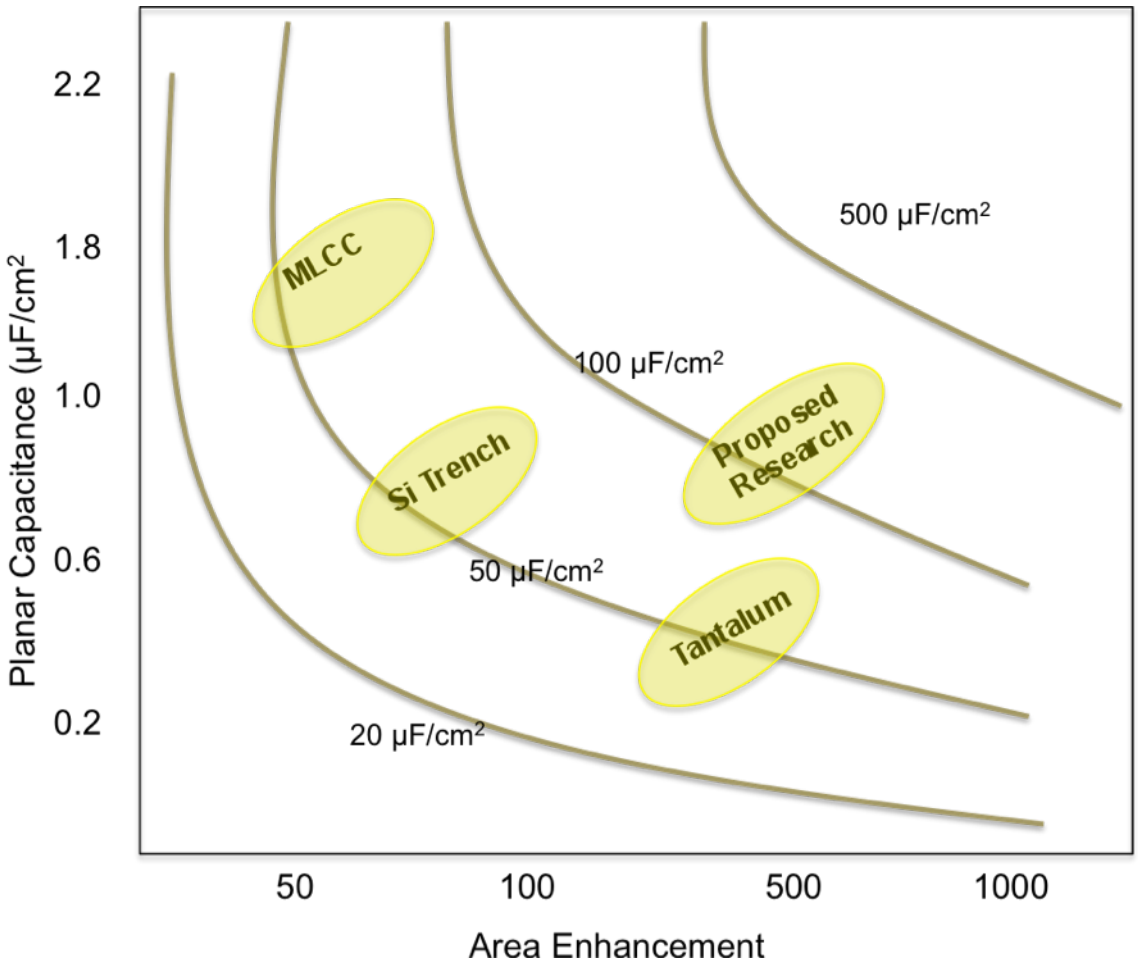


Figure 2.17 Proposed research vs. current state-of-the-art

All the steps as well as the experimental techniques used in fabricating these capacitors are described in Chapter 3.

3 EXPERIMENTAL PROCEDURES

This section describes the fabrication and characterization of particulate-based capacitors on silicon substrates. All the experimental details for fabricating the silicon substrate, the bottom electrode, dielectric deposition and top electrode deposition are discussed in great detail. Figure 3.1 shows the cross-section of the finished capacitor structure. First of all, a silicon substrate with appropriate routing layer is patterned in order to obtain isolated capacitor structure. Then the bottom electrode is printed and sintered

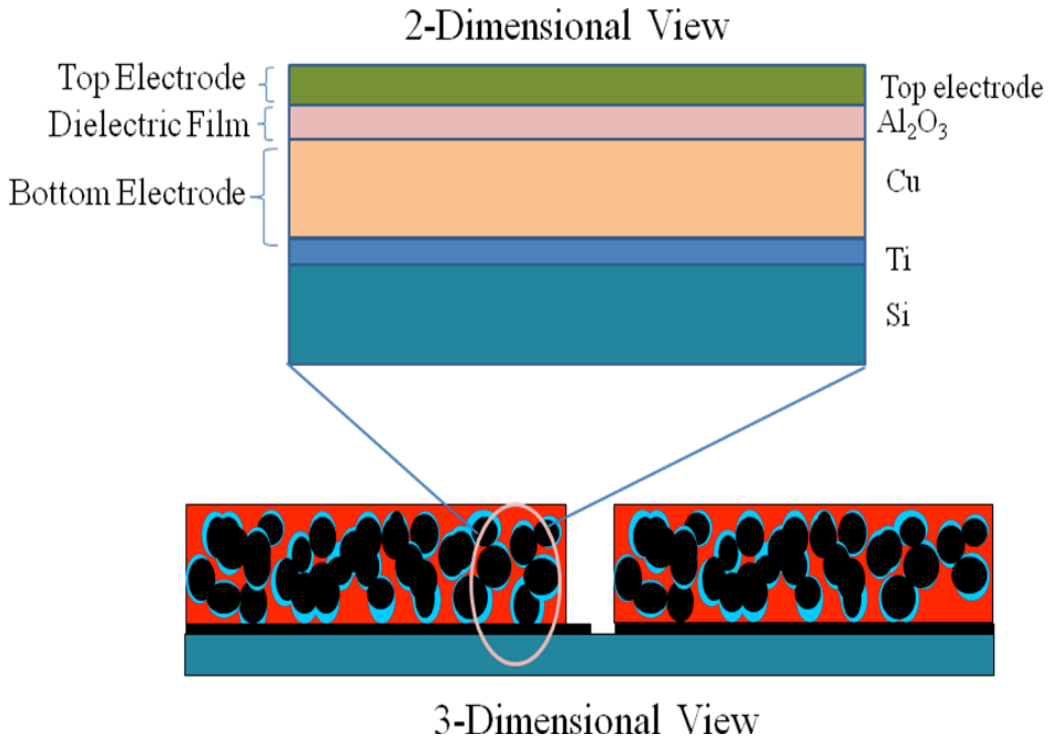


Figure 3.1 Cross section of the capacitor structure

After the dielectric is deposited using atomic layer deposition process, the top electrode is deposited to complete the structure. For the sake of comparison and to estimate the surface area enhancement, planar capacitor structures with only copper acting as bottom electrode were prepared. The complete process flow is shown in Figure 3.2

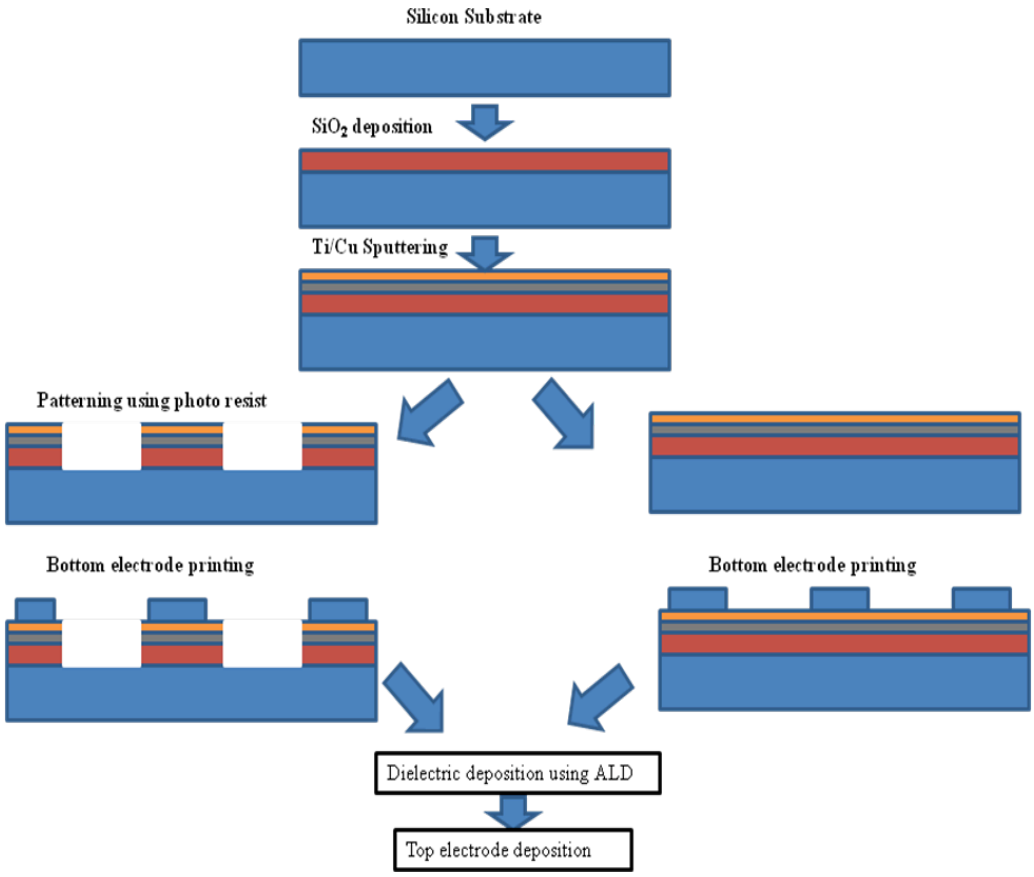


Figure 3.2 Process flow for nanoelectrode capacitors on a silicon wafer

3.1 Barrier layer deposition using PECVD

Plasma enhanced chemical vapor deposition (PECVD) was used to deposit 1 μm thin layer of SiO_2 on a standard 4 inch silicon wafer. The purpose of this layer is to provide electrical insulation to the capacitor structures. At the same time it acts as a barrier to the diffusion of metal ions into silicon at high temperatures. The PECVD tool is widely used in the semiconductor industry to deposit silicon oxide or silicon nitride films. It uses radio frequency (RF)- induced plasma to deposit metal oxide or nitride films. The advantage of using plasma is that it enables deposition of such films at low temperatures. To deposit SiO_2 , 2% silane in nitrogen (SiH_4/N_2) and nitrous oxide (N_2O) was reacted in a radio frequency (RF) -induced plasma. Flow rates of SiH_4 and N_2O were kept at 900 sccm (standard cubic centimeters per minute) and the power was kept constant at 25 W. The operational frequency was 13.56 MHz. The deposition was carried out at 250^o C for 20 minutes. The average deposition rate of SiO_2 was measured to be around $500A^o$/min.

3.2 Sputtering of titanium and copper

DC magnetron sputtering was used to deposit thin metal layers of titanium and copper on Si/SiO_2 substrates. In a DC sputterer, metal films are deposited by bombarding the metal target with highly accelerated argon ions. These metal ions then get deposited on the substrate acting as the cathode. The advantage of using a magnetron sputterer is that it uses high electric and magnetic field to trap electrons close to the surface of the target

thus ionizing more argon gas and hence leading to higher deposition rates at low argon pressure. 3 inch Ti and 6 inch Cu targets were used to deposit 20 nm of Ti and 500 nm of Cu film respectively. The chamber was first pumped down to 2.0 X 10^{-5} torr and after the injection of argon, the pressure increased to 6mTorr. The chamber was maintained at these conditions for the rest of the process. Both metal layers were deposited simultaneously in the same run. The sputtering conditions used are summarized in Table 3.1

Table 3.1 DC sputtering conditions

Metal	Power Used	Deposition Rate/Time	Final thickness
Ti(3'' target)	350 W (7%)	1 A/sec 200 sec	~20 nm
Cu (6'' target)	1000 W (20%)	160 A/min 1875 sec	~500 nm

3.3 Patterning the routing layer

In some cases, it was necessary to pattern the bottom layer for easy accessibility to the test pads. For this purpose a special mask was designed as shown in Figure 3.3

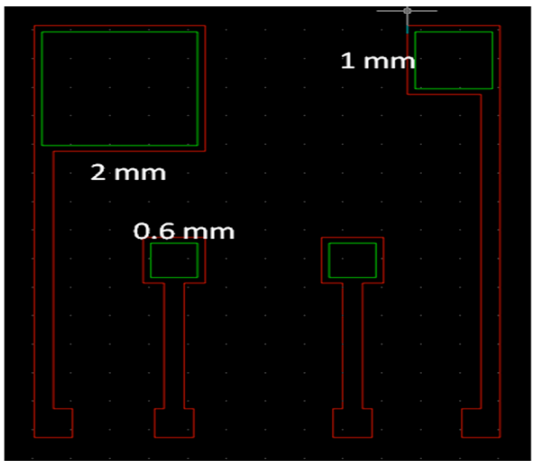


Figure 3.3 Design of the mask used for patterning the routing layer

The routing layer was patterned using a Karl Suss mask aligner with Shipley 1827 photoresist. For a 11 μm photoresist film (spin-coated at 1000 rpm and dried at 100^{o}C for 5 minutes), an exposure dose of 90 seconds was used at 7 mW/cm^2 lamp intensity. Clariant's MF-319 was used as the developer. The routing layer was then etched using H_2O_2/H_2SO_4 and the titanium film was etched using 10% HF.

3.4 Bottom electrode fabrication

In this study, three different types of bottom electrodes were used as described below:

3.4.1 Planar electrode

In this case the sputtered copper film on the silicon substrate was used as the bottom electrode. The purpose of doing this was to establish a baseline for the comparison of surface area enhancement.

3.4.2 Free standing copper foils as bottom electrode

Copper foils (obtained from Oak-Mitsui) of 30 μm thickness were used as bottom electrode to study and optimize atomic layer deposition conditions for better conformality of the dielectric on rough surfaces.

3.4.3 Particulate electrode

Copper paste was prepared and printed onto the silicon substrates with Ti/Cu routing layer and then sintered to obtain a very high surface area particulate electrode structure. Copper powder from two different suppliers with different shapes and sizes was explored for this purpose. Table 3.2 provides the details of the copper powder morphology available from different suppliers.

Table 3.2 Copper powder suppliers and morphology

Supplier	**Morphology**
Tatsuta	Spherical Particles 1-5 μm
NanoDynamics	Equiaxed and Polygonal 1-2 μm

Paste Processing :

The paste was made by adding 0.25 g of the dispersant (BYK 9010) to 7 g of solvent propyl glycol methyl ether acetate (PGMEA) from Alfa-Aesar, followed by the addition of 3 g of the copper powder. The dispersant BYK 9010 is a phosphate ester that is added

to prevent the aggregation of copper particles. Finally, 1-1.5 g of a 30 % solution (by weight) of polypropylene carbonate in gamma Butyrolactone (GBL) were added. Polypropylene carbonate provides strength and viscosity essential for printing and acts as a sacrificial binder. The purpose of this sacrificial polymer was to generate open porosity in the structure by complete decomposition without leaving any residue post sintering. The paste was then kept for milling for 3 hours with zirconia balls. It was heated at 95^{o}C to obtain the right viscosity for printing. The paste was screen/stencil printed on to the given substrate to yield bottom electrode structures. The entire process flow is shown in Figure 3.4. The thickness of the film was controlled by the thickness of the screen or the stencil used. Films with thicknesses ranging from 25 micron to 100 micron were printed using different stencil and screens to study the dielectric conformality and top electrode penetration.

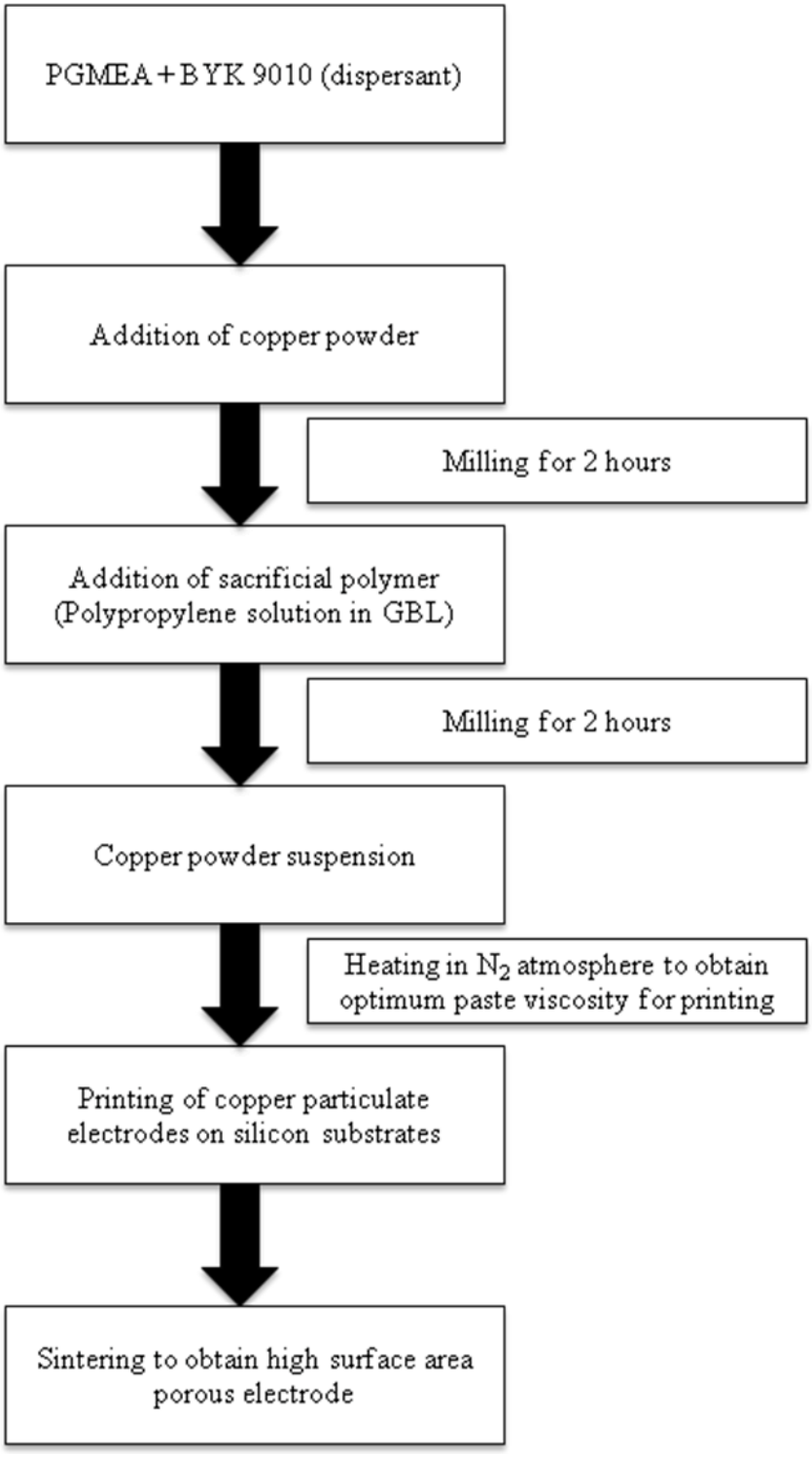


Figure 3.4 Process flow for particulate electrode fabrication

Alternatively, copper powder dispersions were spin coated (CEE 100CB Spinner) on to the silicon substrates to yield 5-10 micron particulate electrode films. The spin speed was kept at 400 rpm and the time was varied from 40 sec to 60 sec.

These particulate electrode films were then sintered in a reducing atmosphere using forming gas (5-10% H_2 in N_2) in Lindberg furnace at temperatures ranging from 400^{o}C to 600^{o}C for different time periods. The sintering profile is shown in Figure 3.5

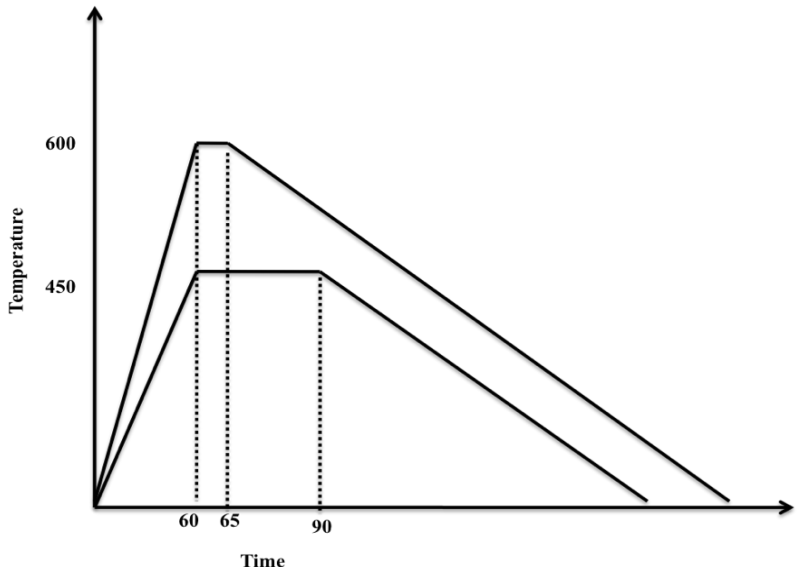


Figure 3.5 Sintering profile for particulate electrodes

This was done to study the effect of sintering temperature and time on the porosity of the final sintered product. All these observations are thoroughly explained in chapter 4.

3.5 Dielectric Deposition

In- house manufactured flow type atomic layer reactor (ALD) was used to deposit Al_2O_3 on the bottom electrode structure. The tool schematic is shown in Figure 3.6 where V1 and V2 represent the precursor valves and PV represents the pressure valve.

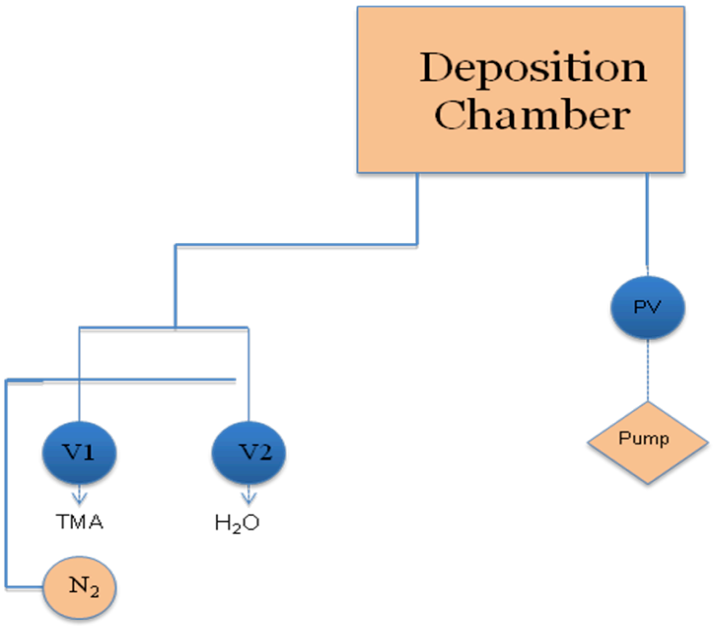


Figure 3.6 ALD tool schematic

The temperature of the reactor was kept constant at 250^{o}C. The deposition was carried out by using Trimethyl aluminum (TMA) and water as the precursors with pulse times of 15 ms and 5 ms respectively. The purge times were varied from 0 sec to 3 seconds. 99.5% pure N_2 was used both as the purge and carrier gas. Thus two precursor pulses and two inert gas purges constitute one ALD cycle. The two half reactions that lead to the growth of Al_2O_3 are given below where the asterisks indicate surface species [42]

$$(A)\quad AlOH^* + Al(CH_3)_3 \rightarrow Al-O-Al(CH_3)_2^* + CH_4$$

$$(B)\quad AlCH_3^* + H_2O \rightarrow AlOH^* + CH_4$$

The deposition rate was calculated to be around 1.1-1.4 A^o/cycle. As-deposited Al_2O_3 films were found to be amorphous with a dielectric constant around 8. Film thicknesses ranging from 35 nm to 100 nm were investigated for their conformality and stability using morphological as well electrical characterization techniques.

3.6 Top electrode deposition

Two different top electrodes were used to complete the capacitor structure. These are described below:

3.6.1 Gold as top electrode

Gold was used as a reference electrode with planar copper acting as the bottom electrode.100 nm to 200 nm of Au was deposited using a shadow mask that had 0.6 mm openings using CVC E-beam evaporator. This resulted in the formation of a 10 X 10 capacitor array on Al_2O_3 film deposited over planar copper. Such planar capacitor structures were used to study and optimize the properties of the ALD Al_2O_3 acting as the dielectric. These also provided base line information such as capacitance density, yield, breakdown voltage and leakage current for comparison with particulate electrode.

3.6.2 PEDOT as top electrode

As explained in chapter 2, in order to benefit from the entire surface area enhancement obtained by the particulate electrode, it is important to choose a top electrode that can penetrate deep into the structure thus accessing most of the surface area. In short, the top electrode should meet following requirements:

- Good conductivity
- Chemically stable interface
- Conformal coating on particulate electrodes

Based on these conditions, Poly-(3,4-ethylenedioxythiophene (PEDOT) or PEDOT was chosen as the main candidate for top electrode. PEDOT monomer (EDT, Clevios M^{TM}) was mixed with oxidizer Fe(III)tosylate (Clevios CB^{TM}) in the weight ratio of 1:25 and then quickly dispensed on to the surface of the dielectric film on the bottom electrode using a syringe. It was then allowed to polymerize and dry at 50^{o} C on hot plate in air for about 60 minutes. In order to make good contacts and to planarize the capacitor structure, PEDOT was coated with carbon black dispersion in PGMEA and left to dry at 50^{o}C for 1 hour. This was then coated with silver paste (Loctite 3880) which is basically a conductive adhesive with silver particles in epoxy binder. This structure was cured at 125^{o}C for 10 minutes. The resultant capacitor structure is shown in Figure 3.7. This capacitor structure was then tested for its electrical properties and reliability.

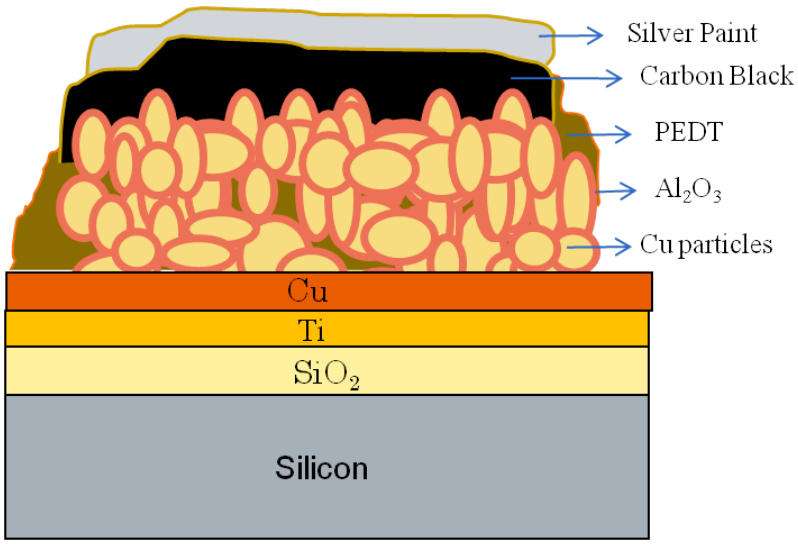


Figure 3.7 Schematic cross-section view of the test capacitor

3.7 Device Characterization

Various characterization techniques such as SEM, EDS, etc were used to study these devices. Electrical measurements were made in order to study the properties of the dielectric. All the characterization techniques and tool used in this study are described in the following sections.

3.7.1 Field emission scanning electron microscope (FESEM)

Field emission scanning electron microscopy (FESEM LEO 1530) was used to study the morphology of the electrode and the dielectrics. The cross-section images of the particulate electrode and the metal-dielectric interface provided useful insights regarding the porosity of the bottom electrode and the conformality of the dielectric film.

In FESEM, electrons are generated by a field emission gun (typically made of tungsten) in vacuum. This electron beam is focused onto the target by using electromagnetic lenses. When this electron beam strikes the target, different types of electrons are emitted that are detected by a detector. Most of the imaging is done in secondary electron mode where the detector detects the secondary electrons emitted by the target and constructs an image by comparing the intensity of these electrons to the primary electron beam emitted by the gun.

3.7.2 Energy dispersive x-ray spectroscopy (EDX)

EDX is an analytical technique that is used to study the chemical composition of a system and is always coupled with SEM. EDX utilizes the X-rays emitted by the target that is bombarded by high energy electrons from the field emission gun in an SEM and analyzes them to determine the chemical composition.

In this study, EDX was used to determine ALD conformality on high surface area bottom electrode.

3.7.3 X-ray Photoelectron Spectroscopy (XPS)

XPS is a quantitative spectroscopic technique that measures the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy and number of electrons that escape from the top 1 to 10 nm of the material being analyzed. XPS requires ultra high vacuum

(UHV) conditions. This technique was used to study the effect of PEDOT of ALD alumina.

3.7.4 Capacitance measurement

The capacitance and loss measurements were done at room temperature by using HP 4285 A Precision LCR meter (75 kHz-30 MHz) at 100 kHz and at 1 Volt. Frequency dependence of the capacitors was studied by using Solartron impedance analyzer. The capacitance vs. frequency plots were obtained over a frequency range of 1 Hz to 1 MHz

3.7.5 Leakage current measurement

Depending upon the type of measurement, two different leakage current measurement tools were used. Keithley 236 Source Measure Unit was used to measure the DC breakdown voltage and leakage current. This equipment can apply a maximum of 110 volts and can measure current from 100 fA to 100 mA. Keithley 6487 Pico ammeter with Voltage source was used to measure leakage current in the nanoampere range. This tool can apply a maximum voltage of 505 volts and can measure currents from 20 fA to 20mA.

3.7.6 Impedance Spectroscopy

Impedance is described as a measure of opposition to alternating current. It has two parts-real and imaginary. The real part corresponds to the resistance of the system while the

imaginary part is known as the reactance and that can be either capacitive or inductive. Impedance spectroscopy is used to study the impedance response of a system over wide range of frequencies. Based on this, various important properties of the system such as capacitance, resistance, admittance can be studied.

In the present study, Impedance spectroscopy was used to study the interaction of PEDOT with Al_2O_3 along with several other characterization techniques such as EDS and XPS . Solatron impedance analyzer was used to plot the imaginary part of impedance against its real part. Such a plot is referred to as Cole-Cole plot or Nyquist plot. These plots were obtained for Au- Al_2O_3-Cu , PEDOT- Al_2O_3-Cu and PEDOT-Al_2O_3-Particulate electrode systems and the resistance of the Al_2O_3 dielectric in each case was obtained. All these findings have been reported in chapter 4.

4 RESULTS AND DISCUSSIONS

A synergistic combination of thick and high-surface area copper particulate electrodes and thin alumina dielectric deposited using ALD was used to form a high-density capacitor array on silicon at CMOS compatible temperatures. This chapter presents the results and discusses the key findings of this research. The results are explained in four descriptive sections- (i) bottom electrode, (ii) dielectric deposition, (iii) top electrode and (iv) electrical characterization of capacitors.

4.1 Bottom Electrode

High surface area bottom electrode forms the backbone of high-density capacitors. Therefore, this task focuses on the fabrication of low temperature silicon-compatible high surface area bottom electrode. For this purpose, copper paste with micron sized particles was printed onto the silicon substrate using standard printing techniques as explained in chapter 3 and then sintered at temperatures ranging from 400^{o}C-600^{o}C. SEM was used to study the effect of sintering temperature on the structure of the bottom electrode. Effect of particle size, shape and binder concentration on resultant porosity was also studied.

4.1.1 Generating an open porous structure to increase surface area

Well-dispersed copper paste suspension was used to print high surface area electrodes on silicon. The rheology of the paste was controlled by optimizing the dispersant and binder

content. In this study, propylene glycol methyl ether acetate (PGMEA) was used for making copper powder suspension. PGMEA was selected because of its compatibility with copper and ease of processing.

4.1.1.1 Selection of the Dispersant

The selection of the dispersant strongly depends on the solvent and the material to be dispersed. A good dispersant should be soluble in the dispersing medium and should possess a strong affinity to the particle surface [56]. Hitesh et al investigated the compatibility of various dispersants with PGMEA and found that phosphate esters had the best solubility with PGMEA[57]. Based on their findings, BYK 9010, which is a phosphate ester, was selected as the dispersant. This phosphate ester being acidic in nature was ideal for dispersing copper particles, which can be assumed to be covered invariably with a thin layer of basic copper oxide due to surface oxidation. The dispersion mechanism has been explained by Fowkes et al.[59] They suggested that when a dispersant is added to a low polarity solvent, stabilization occurs due to the formation of an adsorbed layer owing to acid-base reactions occurring between the particle surface and the dispersant. This mechanism has been shown schematically in the Figure 4.1.

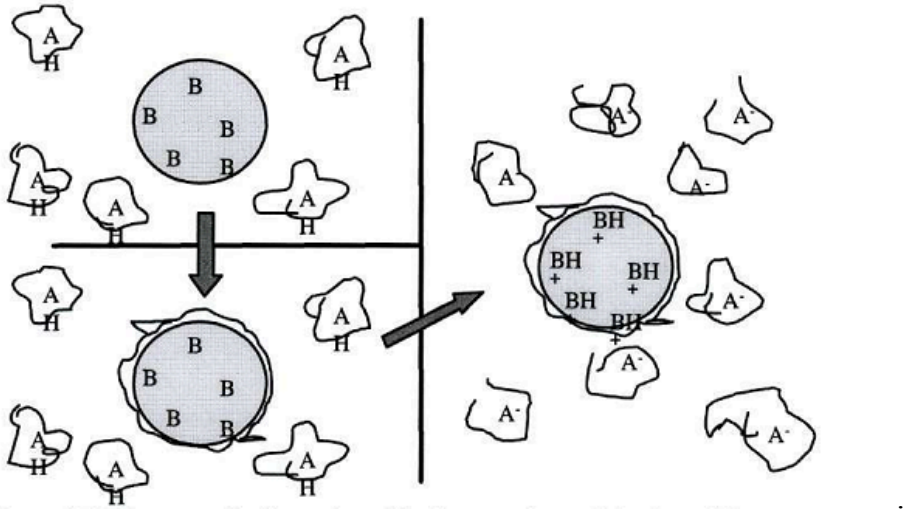


Figure 4.1 Electrostatic dispersion of basic particles by acidic dispersant in low polarity solvents.(A: dispersant molecules and B : metal particles)[57]

The adsorbed ions desorb into the solution as counter ions and make the particle surface positively charged by leaving behind positively charged hydrogen ions. As can be seen from the above figure, particle B (in this case copper oxide) gets electrostatically charged by an acidic dispersant AH (phosphate ester) in a low polarity solvent leading to its stabilization. AH desorbs into the solvent as A- counter ions, leaving behind H+, thus making the surface positively charged.

4.1.1.2 Selection of compatible sacrificial polymer

According to the dispersant-first rule established by Cannon et al.[60], for efficient de-agglomeration, binder should be added after a suitable dispersion of powder had been obtained. Therefore, after an optimally dispersed suspension of copper powder had been prepared, a polymer binder was added to the suspension as a subsequent step. The purpose of the binder was to provide green strength to the body until it was sintered. In

the present study, sacrificial polymers or porogens were used as binders. These sacrificial polymers or porogens acted as porosity generators to facilitate the formation of high surface area open porous structure. Such polymers decompose completely at low temperature evolving some volatile gaseous by product. Most commonly used sacrificial polymers require air to burn off completely with the evolution of CO_2 and water. However, the present study required a sacrificial polymer that would burn completely in inert or reducing atmosphere. Polypropylene carbonate (PPY) is one of the most widely used sacrificial binder known to decompose completely at 400^{o} C in oxidizing, reducing or inert atmospheres.

Figure 4.2 shows the thermogravimetric analysis of this polymer provided by the commercial manufacturer (Empower Materials, New Jersey, USA)[61]. TGA is a thermal testing that is performed on materials to estimate the weight change in relation to temperature. This weight change is often attributed to decomposition or combustion of the materials. As can be seen from the plot, this polymer burns off completely at temperatures above 360^{o} C irrespective of the processing atmosphere.

Copper paste was sintered at temperatures in the range of 400^{o}C- 600^{o}C in reducing atmosphere. Polypropylene carbonate easily decomposes under these conditions without leaving any residue that might interfere with the conductivity of the bottom electrode. Therefore, polypropylene carbonate presented itself as a suitable candidate for use as a sacrificial binder.

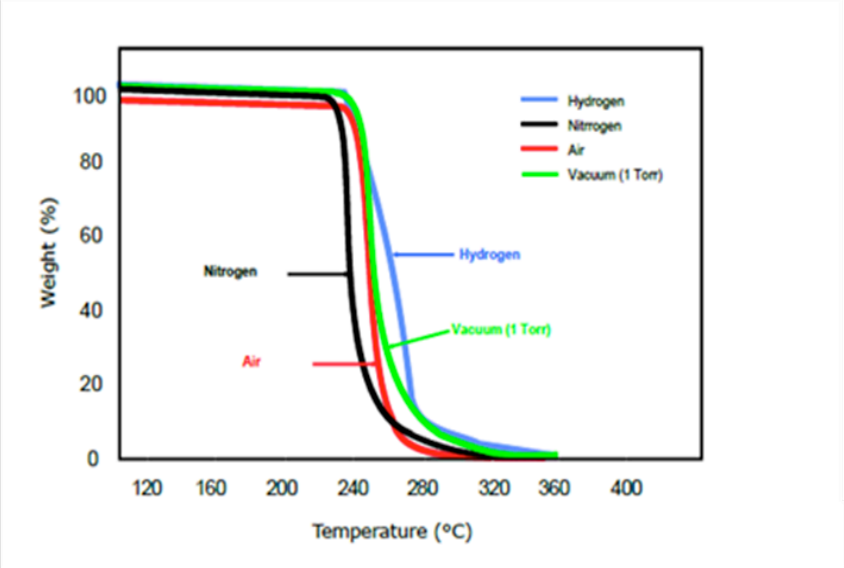
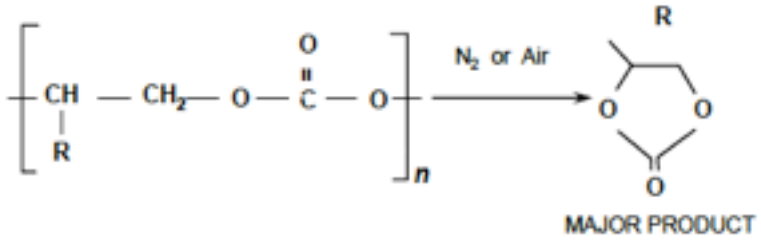


Figure 4.2 Thermo gravimetric analysis (TGA) of Polypropylene carbonate provided by Empower materials.

20 % by weight of polypropylene carbonate was dissolved in gamma butyrolactone (GBL) and this was then added to the copper powder suspension. The volumetric ratio of copper powder to the polymer was optimized to be 1:1 for generating adequate porosity. This suspension was ball milled for 2 hours. Milling facilitated the dispersion of copper particles and polymer granules by mechanically breaking down metal particle agglomerates and homogenously dispersing them. The suspension was made into a paste by modifying the viscosity and rheology by heating it. Sintering was carried out in a reducing atmosphere using 10 % forming gas after printing this paste on silicon substrates. During sintering, polypropylene carbonate decomposes completely to generate a volatile cyclic carbonate as shown by following reaction:



Here the reaction by-product is a cyclic carbonate that would evaporate quickly without leaving any substantial residue[46].

Figure 4.3 shows this concept schematically where the dark blue particles are polymer granules that would burn completely under a given set of conditions leaving behind open pores.

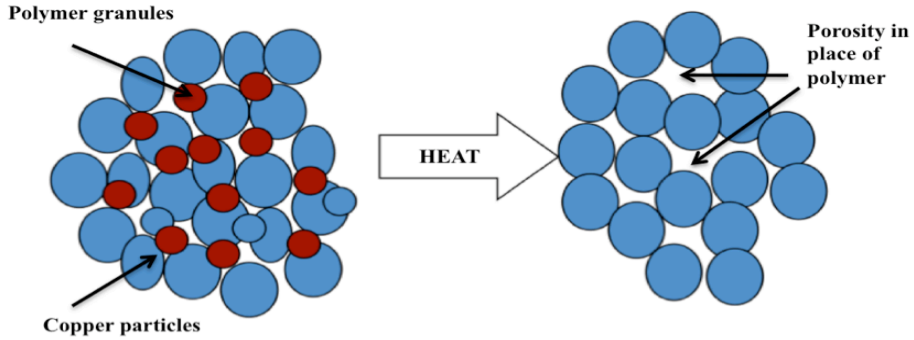


Figure 4.3 Schematic showing generation of open porosity using sacrificial polymer.

4.1.2 Effect of particle shape and size

The effect of particle shape and size on the resultant porosity was studied by using two different sets of copper powders as explained in chapter 3. Batch 1 had a very wide distribution of particle size while Batch 2 had very narrow particle size distribution with particle size varying from 1 μm to 2 μm.

Batch 1:

For batch 1, the particle size varied from 1 micron to 5 micron. Due to a large particle size variation, smaller particles tended to block the open pores by sitting between two large sized particles. Figure 4.4(a) illustrates this schematically and the corresponding micrograph is shown in Figure 4.4(b). As can be seen from the micrograph, the resultant structure is very tightly packed. Such a tightly packed compact structure reduced the overall porosity and blocked the diffusion path or channels for subsequent dielectric and top electrode deposition. As shown later from capacitance measurements in section 4.2, an area enhancement of 10-15 X was achieved using this structure.

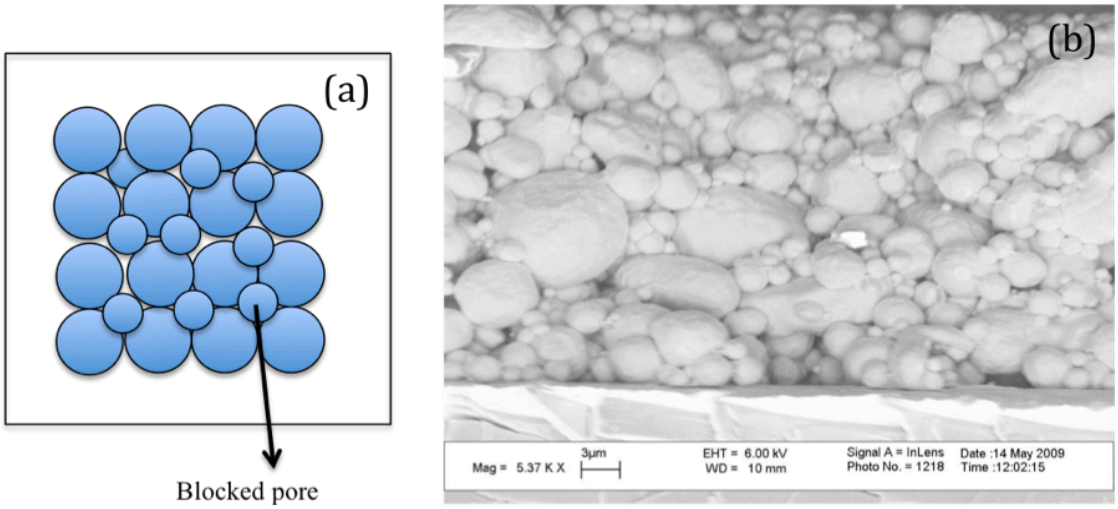


Figure 4.4 (a) Schematic illustration of pore blocking by smaller particles when wide size particle distribution is used (b) Corresponding SEM image showing a very compact structure.

Batch 2:

Powder with uniform particle size distribution, on sintering, resulted in a much more open and porous structure. Figure 4.5 (a) shows schematically how uniform particle size distribution results in larger pores. The SEM of the resultant structure is shown in Figure

4.5(b). The particle size of this batch varied from 1-2 μm and hence the structure was much more uniform with large number of open and continuous pores. These continuous and open pores increased the accessible surface area and provided multiple diffusion channels for dielectric deposition. Using this morphology, an area enhancement of 30X - 40X was obtained from the bottom electrode; keeping the thickness of the electrode equal to that of batch 1. By optimizing the polymer content from 30% to 50%, area enhancement of 150 X was achieved for thicker electrodes. All these capacitance measurements will be discussed in section 4.2

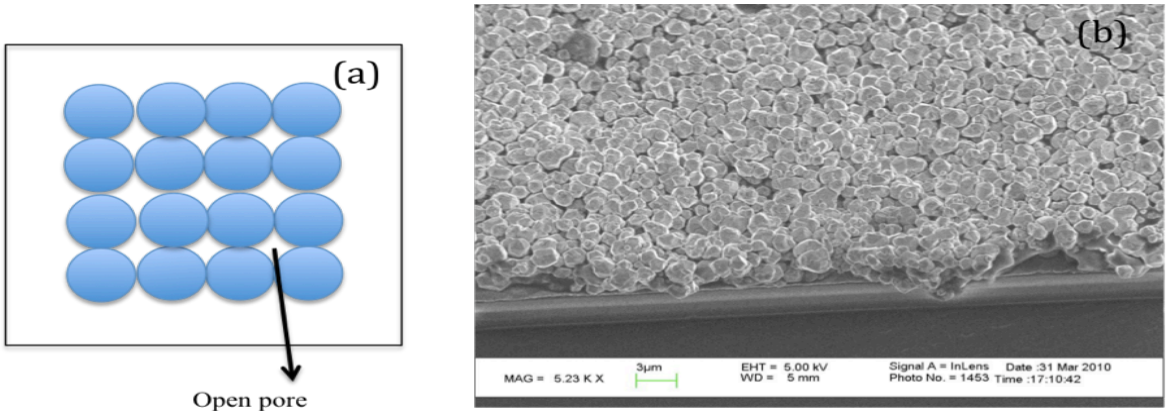


Figure 4.5 (a) Schematic illustration showing how uniform size distribution particles result in an open porous structure (b) Corresponding SEM image showing the presence of continuous porosity throughout the structure.

4.1.3 Optimizing sintering conditions

Sintering is done to obtain a coherent metal mass ,with sufficient mechanical integrity and strength, from the metal powder without actually melting the particles. Sintering temperature is normally 2/3rds of the melting temperature of the material. For fine

powders, sintering at lower temperature is possible. The driving force during sintering is the decrease in the excess surface energy of the system. During sintering, densification of the structure occurs by the replacement of high-energy solid-vapor interfaces by low-energy solid-solid interfaces, thereby lowering the surface energy of the system. This results in a decrease in surface area as well as porosity. Sintering occur in three stages. In the first stage rearrangement of the particles occur to increase contact area to facilitate neck formation through volume diffusion. The driving force for the neck formation is the chemical potential difference between the neck and the particle surface. The second stage is accompanied by large amount of shrinkage owing to particle reduction and pore elimination. In the final stage, the porosity is completely eliminated and grain coarsening is achieved. Since, the aim of the present study was to achieve a porous sintered body, a careful control of sintering temperature was required so as to attain only first two stages of sintering. Partial sintering of copper powder was carried out to lend strength to the structure without compromising the porosity. The melting temperature of copper is 1083^{o}C and therefore sintering temperatures in the range of 400-600^{o}C were investigated. Copper paste was sintered in reducing atmosphere to eliminate the entire organic residue from the dispersant, solvent and polymer added during the paste processing. It was found that by sintering the copper paste at 450^{o} C for 30 min at ramp rate of 8^{o}C/ min, it was possible to get rid of the entire organic residue. Though this sintering temperature was adequate to eliminate the organics, it was not high enough to adequately sinter the particles and form a strong neck with rounded edges at the triple point of the neck. Figure 4.6 shows the SEM of the sample sintered at 450^{o} C. The highlighted portions show the presence of triple points.

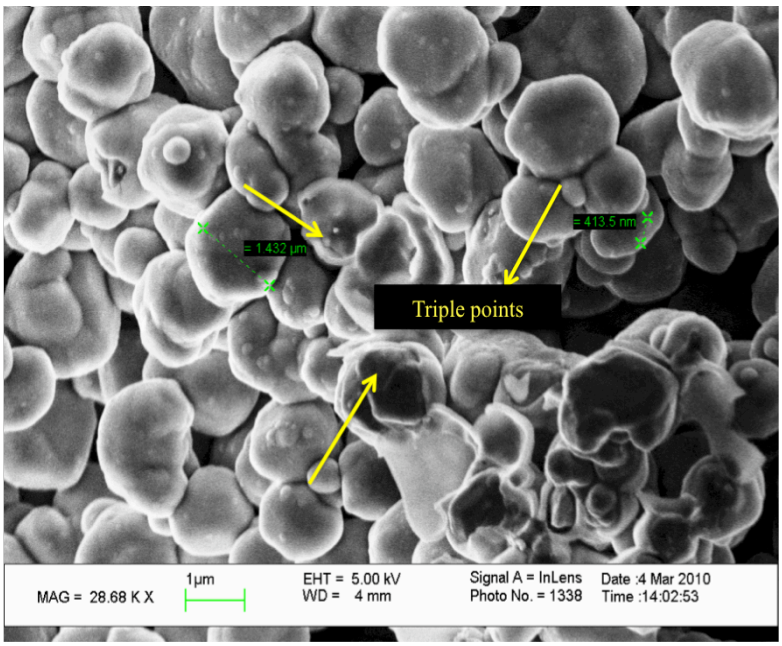


Figure 4.6 SEM of the sample sintered at 450^{o} C showing the presence of large number of unstable triple points (inadequate neck formation).

These triple points represent weakly bonded copper particles that are highly unstable. Consequently, the ALD film on them is also unstable and under high stress as shown schematically in Figure 4.7(a). During testing, when micro-probes are placed on the device, these triple points break and hence damage the ALD film. Therefore, it was important to achieve proper bonding between copper particles to eliminate these triple points by neck formation as shown in Figure 4.7(b).

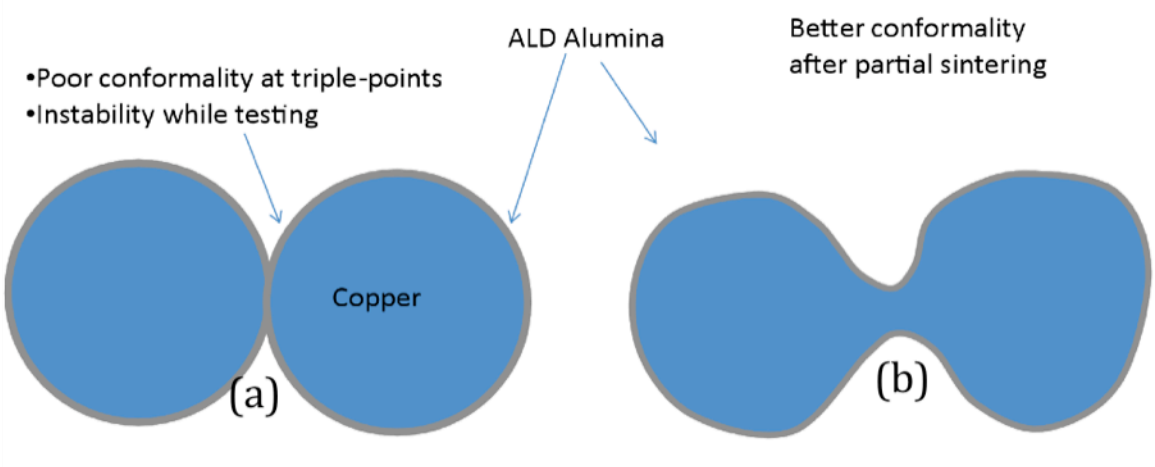


Figure 4.7 (a) Schematic illustration of unstable triple point and (b) mechanism of neck formation during sintering.

In order to facilitate efficient volumetric transport between copper particles, the sintering temperature was raised to 600^{o}C and the time was reduced to 5 minutes keeping the ramp rate constant. The resultant structure is shown in Figure 4.8. This image showed sufficient neck formation between adjacent copper particles

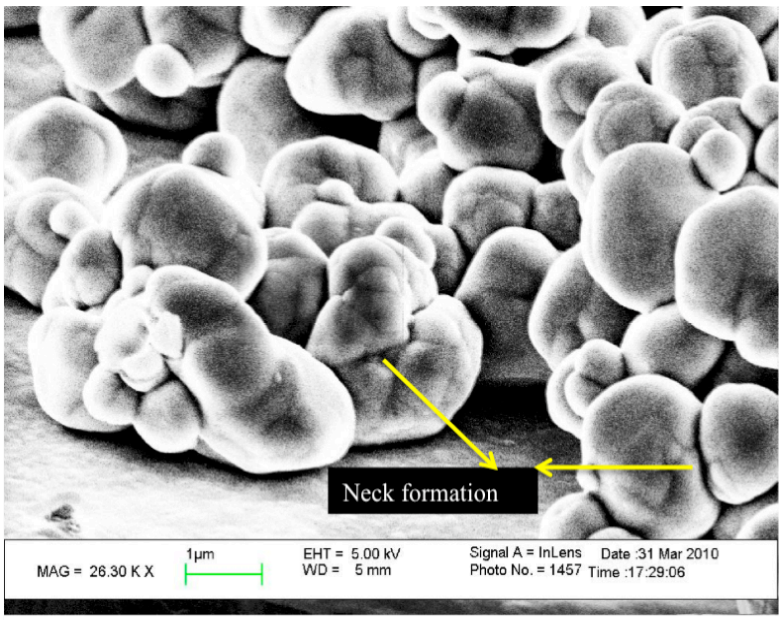


Figure 4.8 SEM of the sample sintered at 600^{o}C showing neck formation between adjacent particles.

By increasing the sintering temperature moderately, it was possible to get rid of the weakly bonded copper-copper interface. This improved the overall capacitor structure and resulted in the increased yield of the resultant capacitors.

4.2 Conformal dielectric deposition using atomic layer deposition technique

The second objective of this study was to develop and deposit conformal dielectric films on high surface area bottom electrodes. Atomic layer deposition is a self- limiting technique used to deposit conformal and defect free thin films on high aspect ratio features. Therefore, this technique was used to deposit Al_2O_3 as dielectric on planar and particulate electrode structures. All the background details regarding atomic layer deposition of Al_2O_3 have already been discussed in section 2.2. In this section, the properties of the ALD Al_2O_3 thin films deposited on planar copper films as well as on particulate copper electrode have been reported.

4.2.1 Characteristics of ALD Alumina on planar copper

Planar copper and ALD Al_2O_3 interaction was studied in order to characterize the intrinsic properties of the deposited film. 90 nm of ALD alumina was deposited on as-sputtered copper and oxidized planar copper films. Gold was evaporated using shadow mask to make planar capacitor structures as explained in chapter 3. The corresponding I-V plots are shown in Figure 4.9

Table 4.1 summarizes the processing conditions of the planar samples and compares the leakage current values of alumina over as-sputtered copper, thermally oxidized copper and sintered coppers at 3 V. The corresponding I-V plots are shown in Figure 4.9

Table 4.1 Effect of heat treatment of copper on leakage current

Bottom Electrode	**Heat Treatment**	**Alumina Thickness (nm)**	**Top Electrode**	**Leakage Current at 3 V (nA/μF)**
$Si/SiO_2/Ti/Cu$	None	90	Sputtered Cu	42
$Si/SiO_2/Ti/Cu$	600C- 5 min (Forming Gas)	90	Sputtered Cu	48
$Si/SiO_2/Ti/Cu$	200C-3 min (Air)	90	Sputtered Cu	516

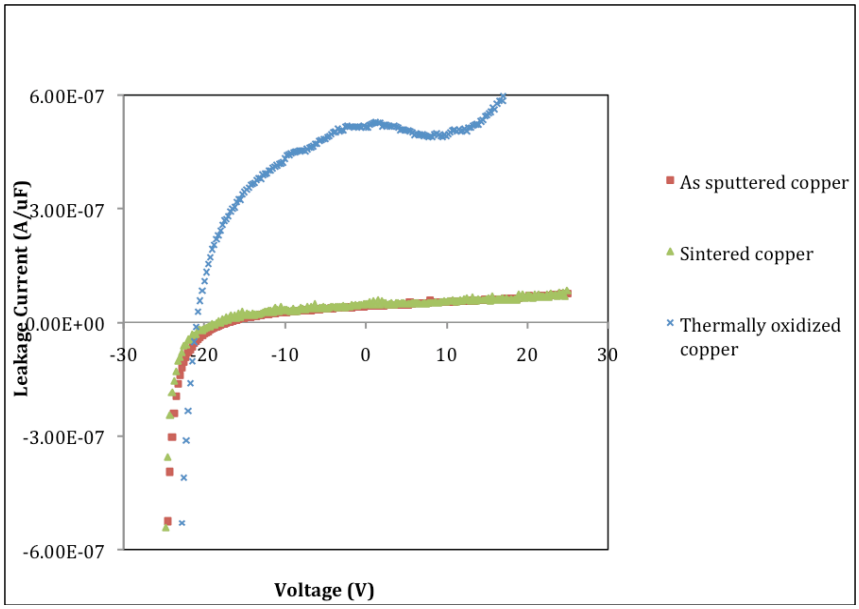


Figure 4.9 I-V plots of Al_2O_3 (i) As-sputtered copper, (ii) sintered copper and (iii) thermally oxidized copper

4.2.1.1 Leakage from as-sputtered copper electrode

I-V characteristics of the planar ALD alumina on the as-sputtered copper film with gold as top electrode are shown in Figure 4.9. These devices exhibited excellent dielectric properties with leakage current as low as 75nA/μF at 25V. These results were in accordance with literature findings [19-22]. The films showed non-polar characteristics till 20 V, beyond which a rapid increase in leakage current was observed suggesting film deterioration under negative bias. The results of these planar ALD alumina film on as-sputtered copper were benchmarked against thermally oxidized and sintered copper electrode devices. These results indicated a defect free ALD film on pristine copper with superior dielectric properties.

4.2.1.2 Leakage from heat-treated copper electrodes

ALD films on pristine copper exhibited excellent properties in terms of leakage current and breakdown voltage. However, the high surface area copper particles can be assumed to be covered with a thin layer of copper oxide owing to surface oxidation. Hence, it was imperative to study the effect of surface oxidation of copper on the dielectric properties of Al_2O_3 films. In order to study the characteristics of Al_2O_3 on the oxidized copper surfaces, the as-sputtered planar copper was thermally treated at 200^oC for 3 min in air, before depositing 90 nm ALD alumina on them. I-V characteristics of the planar device with thermally oxidized copper electrode were obtained using gold as top electrode. These results are shown in Figure 4.9. The leakage current of the device was much higher than the pristine as-sputtered copper electrode, suggesting lower alumina quality. The

leakage current at 3 V was recorded to be 516 nA/μF which is 10 times more when compared to 42 nA/μF for a pristine copper at 3V. Thus, this suggested that alumina on copper oxide is more stressed and defective than on the pristine copper surface. This can be attributed to the inter-diffusion and chemical interaction between copper oxide and alumina.

On the other hand, when as-sputtered copper substrate was annealed at 600^{o}C for 5 min in forming gas and ALD alumina deposited on it, no significant change in leakage current behavior was observed as can be seen from Figure 4.9. Since annealing was done in reducing atmosphere, it can be assumed that no surface oxidation of copper occurred. These results indicated that copper-alumina interface was more stable as compared to copper oxide-alumina interface.

4.2.2 ALD Al_2O_3 conformality study

As discussed in chapter 2, conformality is determined by the amount of the reactant as well as the time the reactant stays inside the chamber. The pulse times or the amount of the reactant entering the chamber was optimized based on the tool manufacturer's recommendations. The dwell time or the amount of time the reactant stays inside the chamber was modified in order to ensure uniform and conformal deposition. To determine the dwell time, ALD process was first optimized for copper foils where the aspect ratio was less than 5. The capacitor devices were fabricated on these copper foils and measured for the yield and electrical properties. The results obtained were then used

to modify the process conditions to improve the conformality of the alumina film over particulate electrodes.

4.2.2.1 ALD Al_2O_3 on rough copper foils

ALD Al_2O_3 was deposited on rough copper foils to study the conformality of the film on rough surfaces and also to optimize the conditions for subsequent deposition on particulate electrodes. For this purpose, 90 nm of ALD Al_2O_3 was deposited on rough and etched copper foils. The dwell time was set to zero. Two sets of foils with different roughness scales were considered. In first case, the roughness of the foil was determined to be of the order of 1 μm. The top view of the foil is shown in Figure 4.10(a), illustrating uniform copper particulate topography. The alumina distribution was validated by EDS spectra which showed strong Al peaks over the entire foil as can be seen from Figure 4.10(b). Due to the limitation of the tool used, it was not possible to detect any oxygen signals.

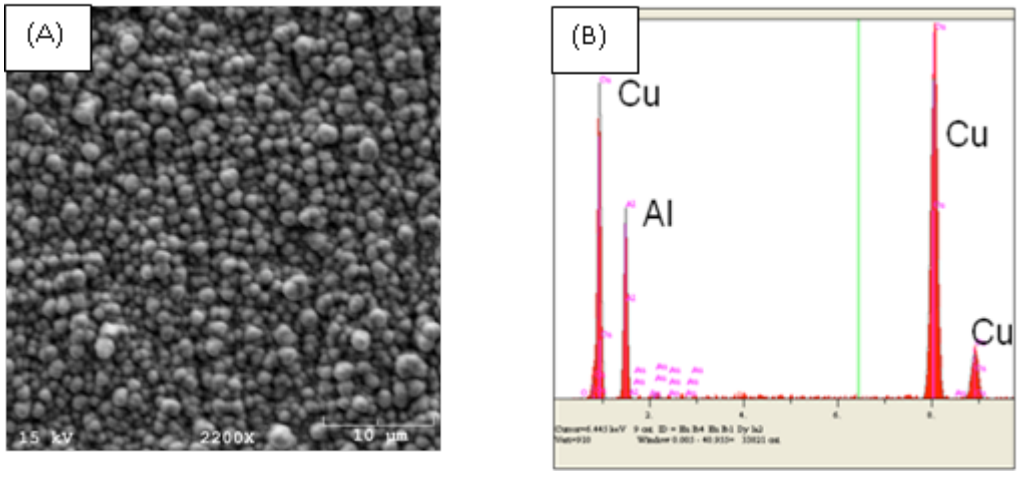


Figure 4.10 (a) SEM showing particulate like topography of copper foil (b) EDS showing Al peaks indicating presence of Al_2O_3.

In the second case, this foil was chemically etched to smoothen out the rough edges and again 90 nm of ALD Alumina was deposited on it. The SEM and EDS of this foils is shown in Figure 4.11 (a) and (b). The strong Cu peaks in both EDS was attributed to the underlying copper foil.

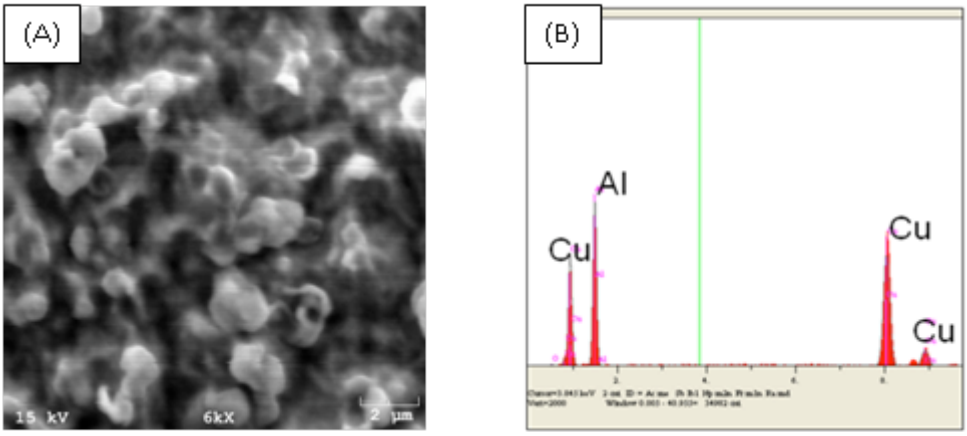


Figure 4.11 (a) SEM showing smoother topography of etched copper foil (b) EDS showing Al peaks indicating presence of Al_2O_3.

Capacitor structures were fabricated on these foils by evaporating gold and were characterized for their capacitance density and yield. For rough copper foils, a capacitance density of 0.12 μF/cm^2 was obtained against a baseline of 0.07 μF/cm^2 for 90 nm ALD film. The increase in capacitance was attributed to the roughness of the copper film leading to increase in surface area. The yield of the devices was found to be 50%. Similar characterization on smoother copper foils showed a decreased capacitance value but the yield increased to 80%. The decrease in capacitance value is caused by the reduction in effective surface area due to smoothing of the rough foils. These results are shown in Table 4.2.

Table 4.2 Capacitance measurements with copper foil as bottom electrode (ALD dwell time = 0 sec).

Copper foil	**Size** (mm^2)	**Capacitance**	**Cap. Density** ($\mu F/cm^2$)	**Loss**	**Yield**
Rough (as received)	0.28	350 pF	0.12	0.015	50%
Smooth features (Chemically etched)	0.28	260pF	0.092	0.0048	80%
Planar Copper film) (Baseline)	0.28	200pF	0.07	0.001	90%

The capacitance measurements suggested that though the lateral area of the electrodes was same in both cases, the effective area in case of rough foils is twice as much as that on smooth foils. As seen from the above table, the yield of planar capacitors was 90% for a size of 0.28 mm^2 and with further increase in the effective surface area of the bottom electrode, the yield continued to decrease. This indicated that the alumina film over large area was not entirely defect free and consisted of thin spots. The formation of thin spots was attributed to insufficient exposure time (dwell time) of the ALD precursor molecules.

In case of particulate electrodes, though sintering parameters were modified to manage triple point strength, it was very difficult to eliminate all sharp edges without compromising the porosity. Therefore, for deposition on particulate electrode, the exposure time of the ALD process was increased to 3 seconds. This increased exposure

time facilitated easy diffusion of precursors in case of particulate electrode and hence led to a better coverage of the dielectric.

4.2.2.2 Conformality studies on particulate electrode

The porosity of the particulate electrode not only increases the surface area but also facilitates the easy diffusion of ALD precursor molecules which is essential to obtain a conformal coating. In case of ALD of Al_2O_3 using TMA and water, the diffusion of precursor molecules inside the porous structure can be assumed to occur due to molecular flow rather than gas phase collisions [25,26]. This can be justified by considering the mean free path of the TMA reactant inside the chamber. At gas pressures around 0.5-1 torr and temperatures ranging from 100^o C to 250^o C, the mean free path of TMA is of the order of 10 μm [26]. For particulate electrode, as can be seen from Figure 4.4 (b) and Figure 4.5(b) given in section 4.1.2, the pore diameter ranges from 100 nm to 500 nm which is much smaller than the mean free path of TMA. Thus, TMA molecules can diffuse into the pores by wall-assisted collisions without colliding between themselves in gas phase. These molecules first saturate the flat surface and then they coat the lower portion of the pore. As a result, a concentration gradient develops between the saturated flat surfaces and yet- unsaturated lower portion of the hole. This concentration gradient acts as a driving force for diffusion inside the pore to happen and tends to decrease as deposition proceeds because of the consumption of precursor molecules [25]. Therefore, it is very important to ensure adequate precursor dose in order to maintain an effective

concentration gradient. The dwell time was therefore increased to 3 seconds in case of particulate electrode to ensure conformal deposition.

Both SEM and EDS were employed to study the conformality of ALD alumina films on particulate electrodes. Thick electrodes were printed and tested for the presence of alumina by EDS. Dot mapping was performed over the entire thickness to check the conformality of ALD Alumina. These dot maps represent the X-ray scans colleted from a defined area. X-ray counts are generated over the entire area and are translated to form dot maps representing the distribution of the elements over the selected area.

Figure 4.12 (a) shows the SEM of a 250 μm thick copper electrode that was prepared to study conformality of ALD alumina. 50 nm of Alumina was deposited on it with dwell time of 3 seconds. The EDS of this sample is given in Figure 4.12 (b). EDS showed strong signals of copper, silicon, oxygen and aluminum. The copper and silicon signals were attributed to the particulate electrode and silicon substrate respectively. A weak carbon signal was also seen which could be due to residual carbon of the un-burnt polymer in the structure.

It can be easily seen from the EDS that aluminum and oxygen signals were detected even at the very bottom of this thick structure. Even though EDS confirmed the presence of alumina in a 250 μm thick electrode, it revealed little about the conformality of the alumina. Hence, dot mapping was performed over the entire area. Figure 4.13(a) shows

the elemental scan for aluminum for a 20 μm portion of this thick structure. The scan for oxygen can be seen in Figure 4.13 (b)

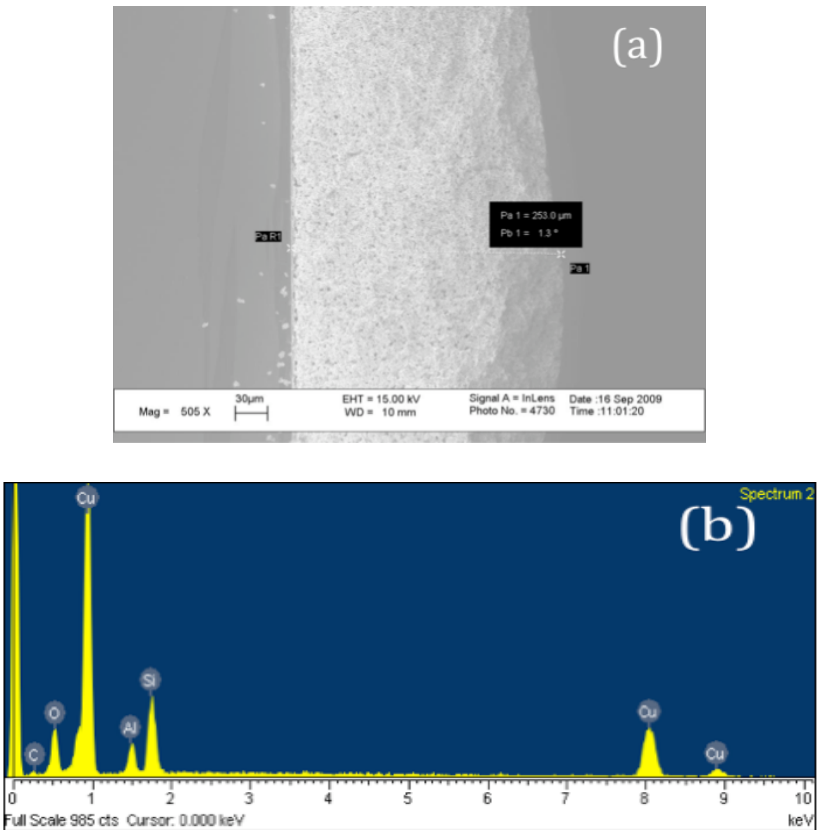


Figure 4.12 (a) SEM of a 250 μm copper electrode (b) EDS showing presence of Al and O at the bottom of this structure.

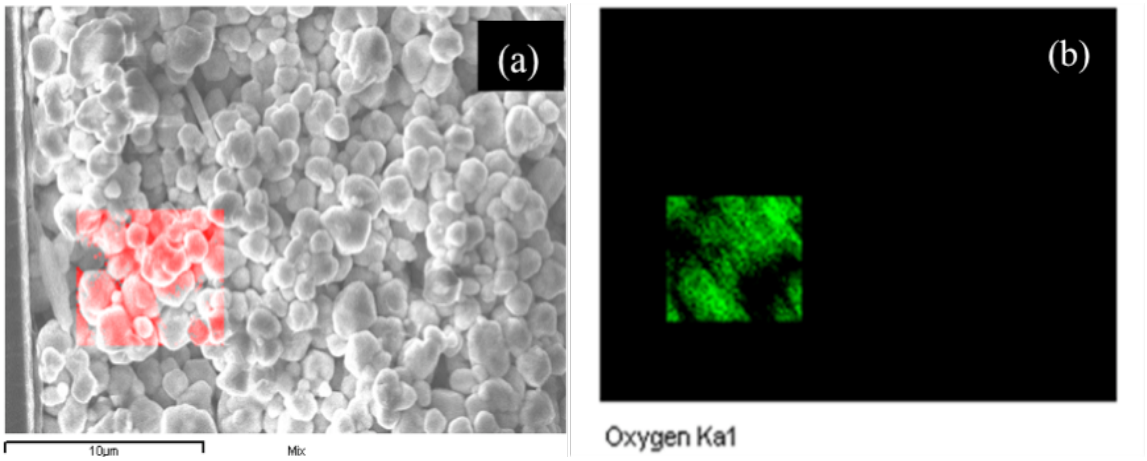


Figure 4.13 Elemental dot maps of (a) Aluminum (b) Oxygen over a 20 μm area of the copper electrode.

It can be seen that the dot map of oxygen exactly overlapped the dot map for aluminum thereby indicating the presence of alumina over the entire area.

Morphological evidence of Al_2O_3 coverage on copper particulate electrodes was confirmed with SEM. 100 nm thick Al_2O_3 films were deposited on the samples and high-resolution micrographs were taken to study these structures. The magnified image of the particulate electrode before and after Al_2O_3 deposition is shown in Figure 4.14 and Figure 4.15 respectively.

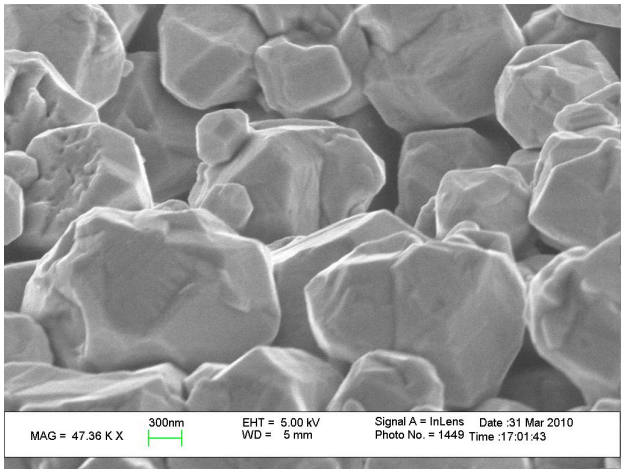


Figure 4.14 SEM of particulate electrode without Al_2O_3 deposition showing copper particle topography.

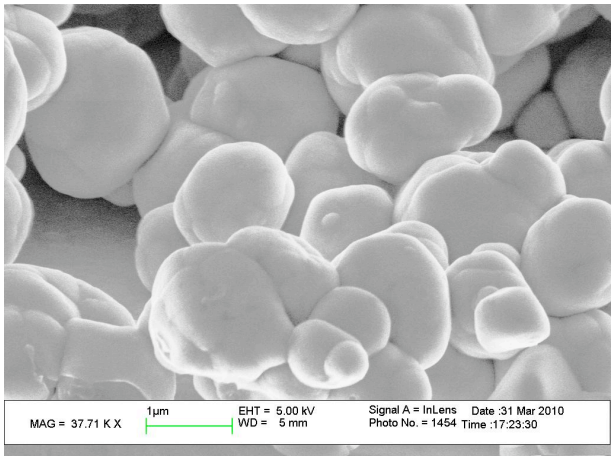


Figure 4.15 SEM of particulate electrode with Al_2O_3 deposition showing a smooth structure.

These micrographs clearly indicated the presence of conformal coating Al_2O_3 on copper particles after the dielectric deposition step.

The cross sectional view of the same sample is shown in Figure 4.16 and Figure 4.17. The electrode was subjected to 700 ALD cycles, which based on a deposition rate of 1.4A^o per cycle, was expected to be covered with 100 nm thick coating of Al_2O_3. Figure 4.16 shows 105 nm thick Al_2O_3 coating around the individual particles.

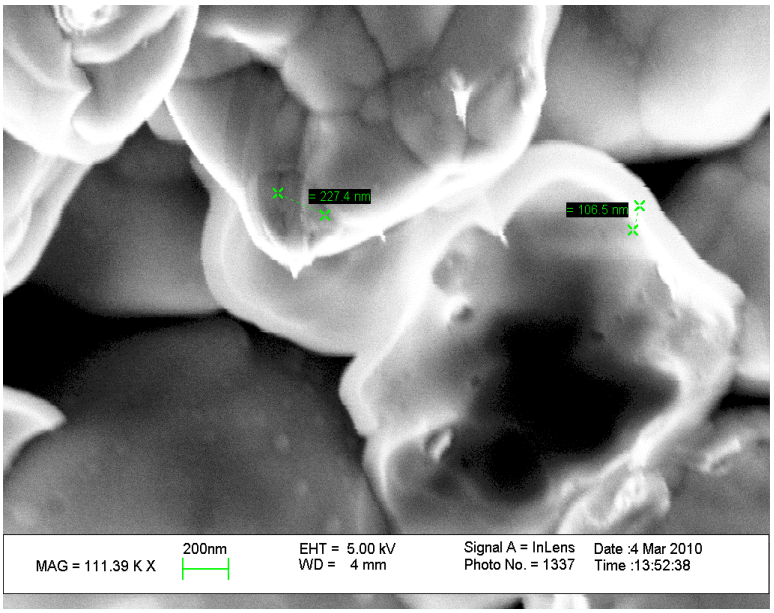


Figure 4.16 Cross-section showing 105 nm ALD film on copper electrode.

ALD Al_2O_3 on copper particulate electrodes showed similar morphological features as observed in Ta_2O_5 capacitors. For comparison sake, an SEM of tantalum particulate electrode showing conformal coating of anodized Ta_2O_5 is shown in Figure 4.18 [42]. By comparing it to Figure 4.17, it can be said that atomic layer deposited Al_2O_3 is as conformal as anodized Ta_2O_5

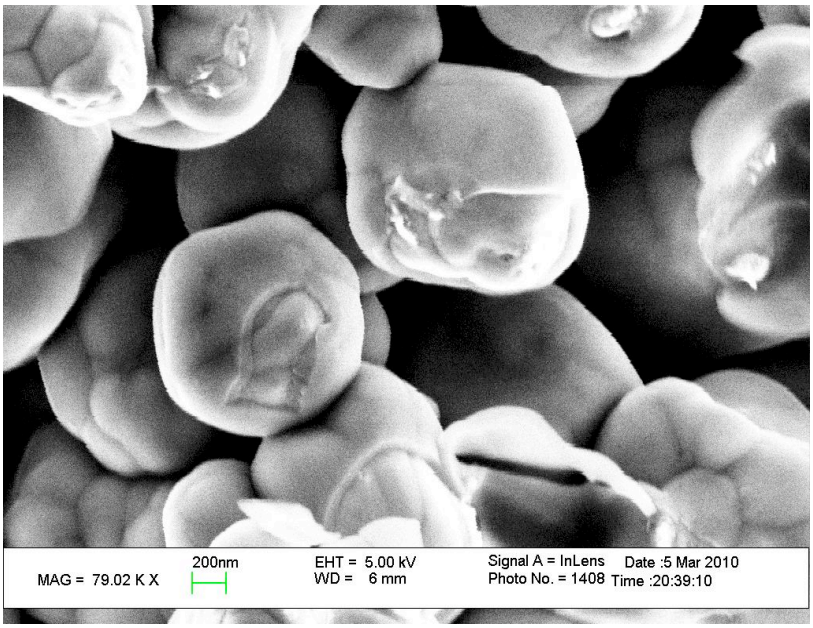


Figure 4.17 Cross-section of copper particulate electrode showing conformal coverage of ALD film.

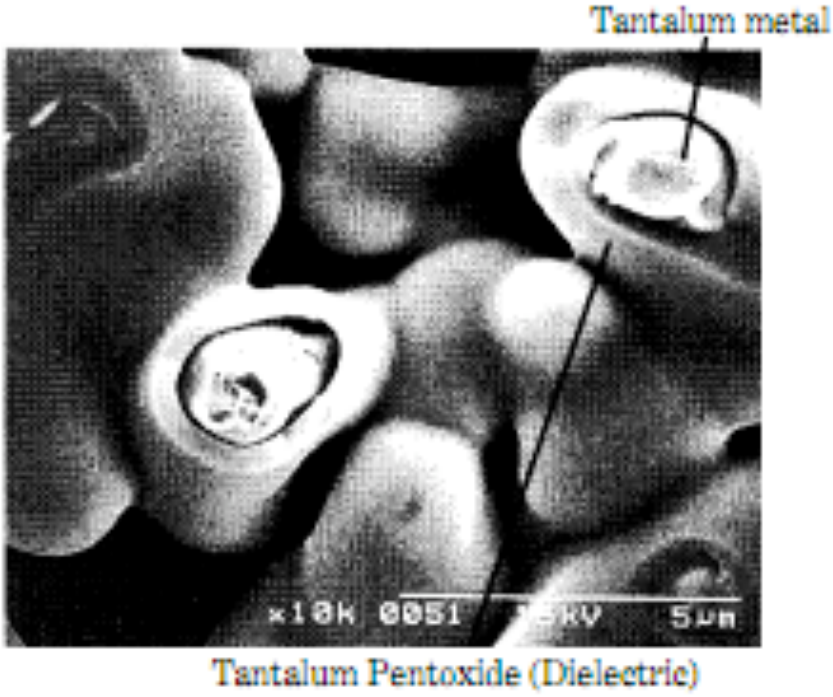


Figure 4.18 Cross-section of tantalum capacitor showing conformal anodized Ta_2O_5 on Ta particles.

Thus, by optimizing the sintering parameters and the ALD deposition conditions, a uniform and conformal coating of Al_2O_3 as dielectric was obtained on copper particulate electrode.

4.3 Top Electrode

In order to benefit from the high surface area bottom electrode, a top electrode meeting the following criterion is desired.

a. Good conductivity with resistance less than 1 ohm-cm
b. Chemically inert so as to have a stable interface with the dielectric
c. Fluid nature to conformally coat the complex 3-dimensional structure of the bottom electrode.

PEDOT (polyethylene dioxythiophene), a conducting polymer, was chosen for this purpose. It plays a dominant role in antistatic, electronic and photonic applications. Amid various applications the most relevant technical applications of PEDOT are its usage as counter electrodes in aluminum and tantalum capacitors. As discussed in section 2.5, the fore-most advantage comes from the ease of infiltration of PEDOT monomers in the high-aspect ratio electrodes used in silicon trench or particulate tantalum capacitors [44]. PEDOT has been shown to improve the safety aspects during the capacitor operation, which has always been a major concern with MnO_2 as the counter electrodes. MnO_2 forms an ignitable redox couple with metal at higher voltages [47]. In addition, PEDOT possesses self-healing ability, high temperature stability and outstanding electronic properties, in the doped as well as un-doped state.

In order to infiltrate PEDOT in the particulate electrode structure, it was prepared in the solution form by mixing the PEDOT monomer and the oxidizer iron(III) p-tolouenesulfonate in the weight ratio of 1:25. Polymerization started to take place immediately after the monomer and oxidizer were mixed and hence it was critical to immediately dispense the PEDOT on the bottom electrode before complete polymerization. Figure 4.19 (a) and (b) show the penetration of PEDOT polymer in the particulate electrode.

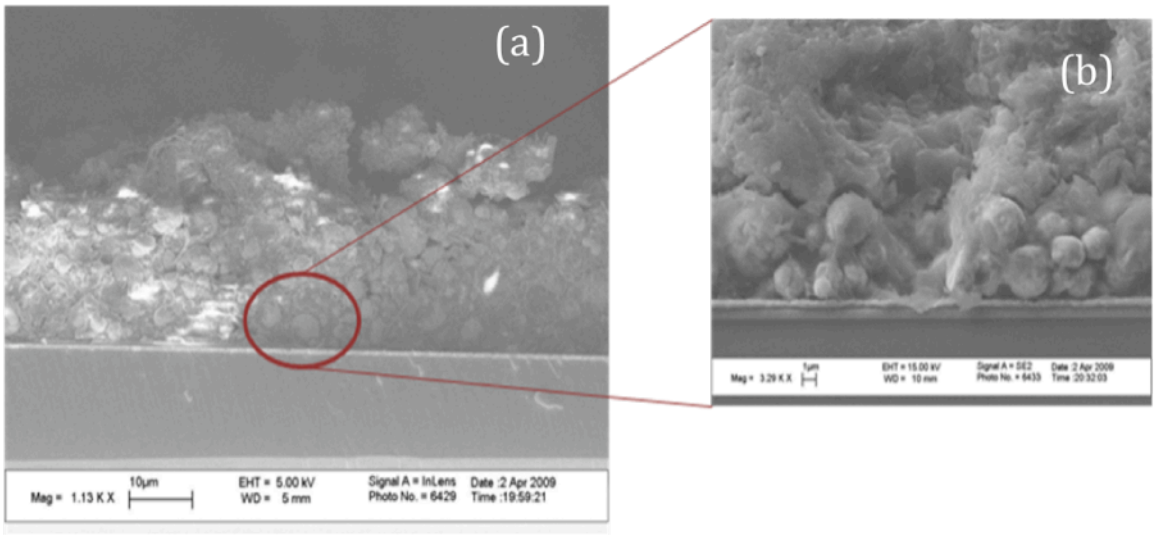


Figure 4.19 PEDOT infiltration (a) throughout the copper particulate electrode and (b) at the bottom.

The above images show compete coverage of copper particles by PEDOT. Thus, PEDOT penetration was found to be very conformal and complete making it a suitable candidate for top electrode.

4.4 Electrical characterization of capacitors

This section reports the capacitance measurements, leakage current and breakdown voltage of the fabricated capacitor structures. Firstly, planar capacitor structures are discussed so as to establish a baseline for capacitance and leakage current. Using this baseline the results obtained by high surface area copper particulate electrode are analyzed and discussed.

4.4.1 Standardizing the ALD Dielectric Using Planar Test Vehicle

The planar test vehicles had a standard design as shown in a cross sectional view in Figure 4.20. Thin copper film of 300 nm thickness was sputtered over Ti. Thin layer of Ti served as an adhesion and barrier layer to prevent the diffusion of copper into SiO_2 during subsequent high temperature sintering. Alumina was deposited as dielectric using ALD and finally the device size was determined by evaporating gold through a shadow mask that completed the capacitor structure. The area of the planar gold electrode was fixed at 0.2826 mm^2. The thickness of ALD Al_2O_3 was kept at 50 nm.

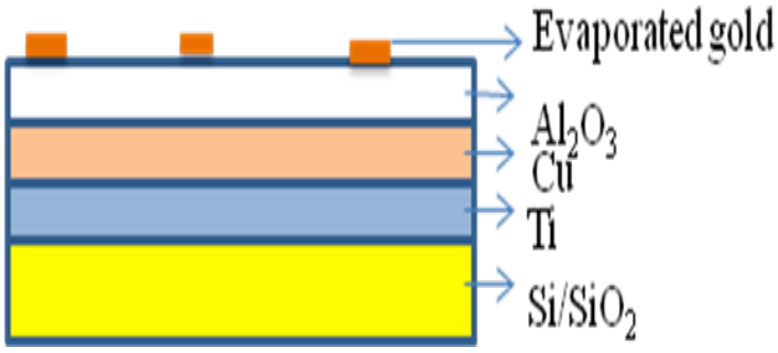


Figure 4.20 Test vehicle design of planar capacitor structure.

Figure 4.21 shows the capacitance vs. frequency plot of such a device. A capacitance of 336pF, corresponding to 0.12 μF/cm^2 capacitance density was obtained at a frequency of 100 kHz. The deposited dielectric film showed less than 3% variation in capacitance between 1 V and 16 V, suggesting the stability of dielectric film over a large voltage range.

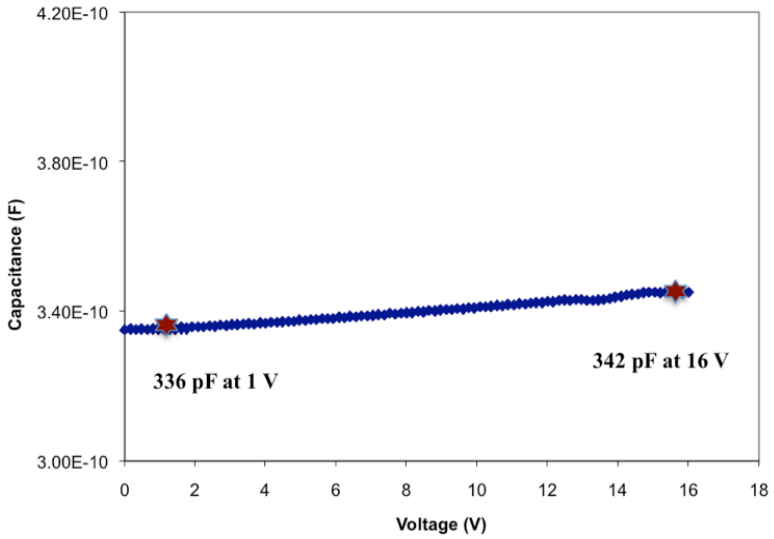


Figure 4.21 Capacitance variation of a planar test vehicle with voltage.

Low leakage current measurement was carefully done to obtain the I-V plot of the same device as shown in Figure 4.22. The leakage current was found to be in the range of 70 nA/μF. The yield of the devices was recorded at 90%.

The breakdown voltage of 50 nm ALD Al_2O_3 film was measured to be around 40 V as represented in Figure 4.22. Although the dielectric showed very low leakage current till 12V, soft breakdown was observed at around 15V followed by a constant increase in

leakage current until the device completely shorted at 40V. The soft breakdown of the film can be explained by the presence of few hydroxyl groups embedded in dielectric film during sequential ALD deposition of alumina. These unpassivated –OH groups created defects in the dielectric and thus increased the leakage current as suggested by Xiong et al[62]. Post deposition annealing of the dielectric film was done to improve the quality of the film by getting rid of the unpassivated OH groups.

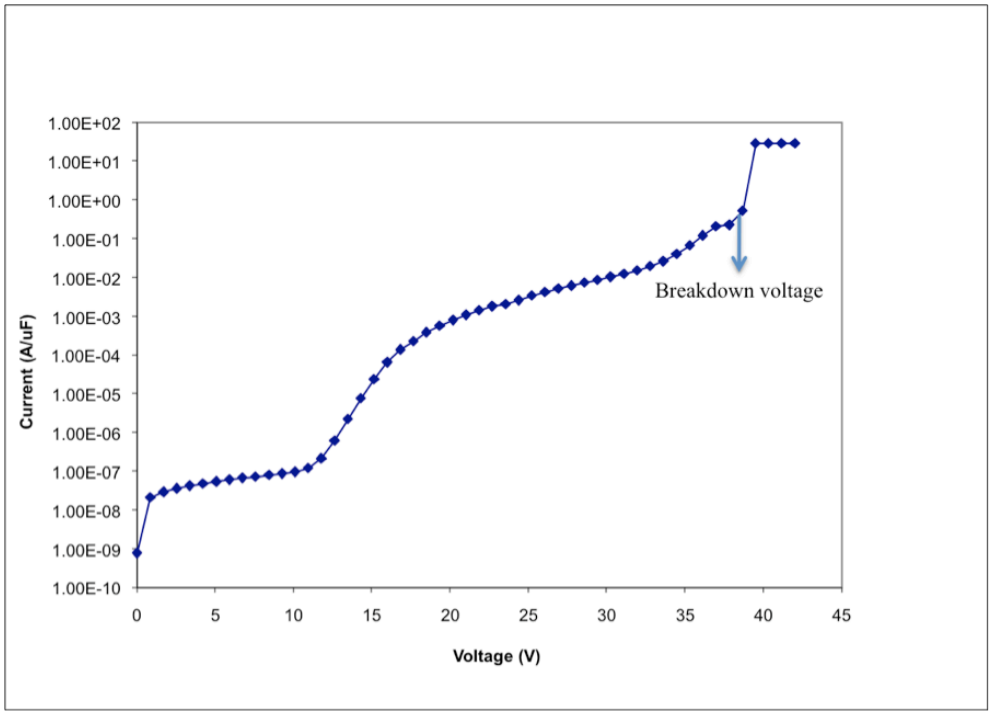


Figure 4.22 I-V plot showing breakdown voltage for 50 nm Al_2O_3 on planar copper.

4.4.2 Characterization of copper particulate capacitors

In this section the results obtained by using copper particulate electrode as the bottom electrode and PEDOT as the top electrode are reported. The structure of such a capacitor

is shown along with the cross-section of the real test device in Figure 4.23 (a) and Figure 4.23 (b) respectively. In Figure 4.23 (b), the dielectric Al_2O_3 cannot be seen because the image was taken at a low magnification. High-resolution images showing ALD Al_2O_3 on particulate electrode have been shown in section 4.2. Figure 4.23(c) shows the top view of the prototype of such a capacitor. Only the bottom electrode access pad and top electrode are visible in this image.

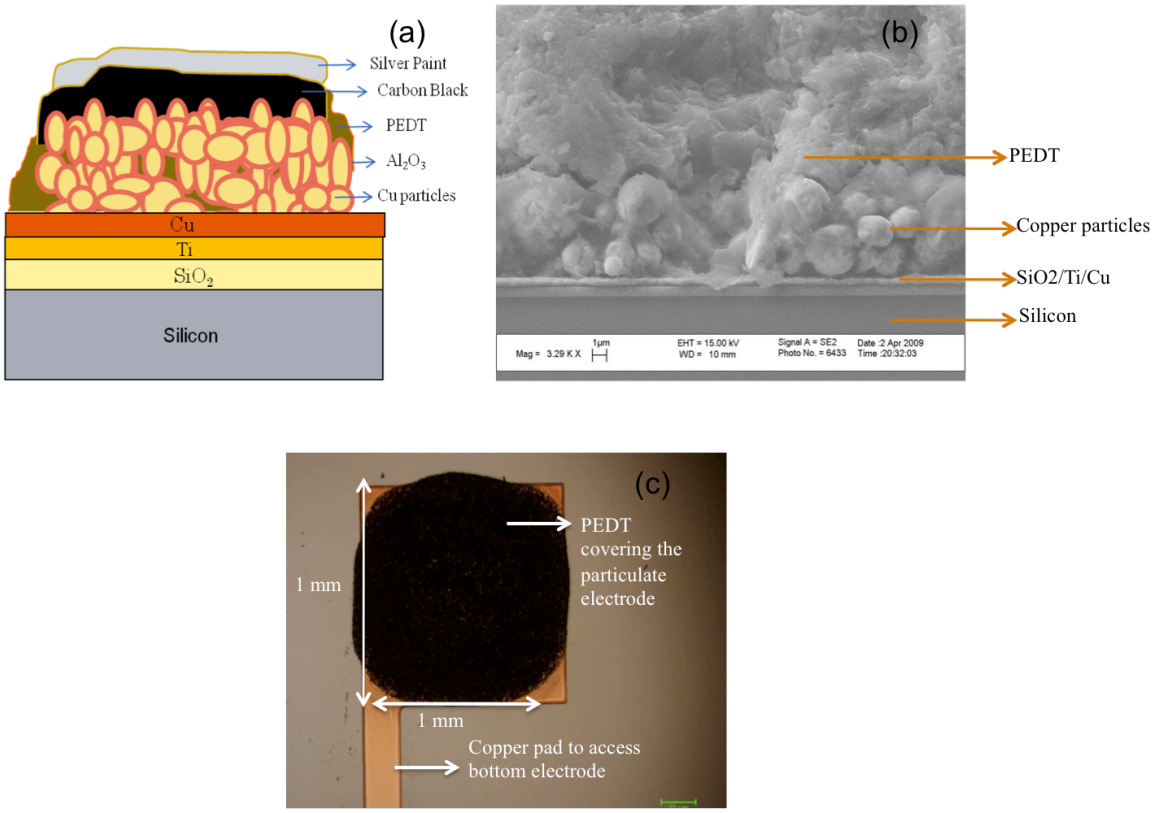


Figure 4.23 (a) schematic of test capacitor structure with particulate electrode, (b) SEM showing cross-section of the real device and (c) top view of the prototype capacitor prepared for electrical testing.

4.4.2.1 Capacitance measurements

As explained in section 4.1, two different sets of copper powders (Batch 1 and 2) were investigated for their use as bottom electrode. Batch 1 had a wide particle size distribution whereas Batch 2 had a narrow particle size distribution. The thickness of the printed electrode varied from 25 μm-35 μm. These samples were sintered at 450^{o}C for 30 minutes. The dielectric thickness was 50 nm. The baseline capacitance density obtained by using 50 nm of alumina on planar devices was 0.12 μF/cm^2. These results are tabulated in Table 4.3

Table 4.3 Effect of the copper particle size on overall enhancement in capacitance density (bottom electrode thickness = 25 – 30 μm)

Copper powder distribution	Area (mm^2)	Capacitance (nF)	Loss	Capacitance Density (μF/cm^2)	Enhancement in capacitance density
Batch -1 1-5 μm	0.5	8.5	0.64	1.7	~15 X
Batch-2 1-2 μm	1	42	0.19	4.2	~ 35 X

As can be seen from this table, only 15 X enhancement in capacitance density, as compared to the baseline value of 0.12 μF/cm^2, was observed when batch 1 was used to make bottom electrode. Such a small enhancement in capacitance density can be attributed to the tight-packed structure of the bottom electrode owing to the wide particle size distribution. This reduced the overall open porosity and hence resulted in a small enhancement. On the other hand, when mono dispersed copper particles were used to make the bottom electrode, the resulting structure was much more open and a 35X enhancement in capacitance density was observed for the same thickness of the dielectric

and the bottom electrode. During ALD, this enhanced porosity helped in the easy diffusion of precursor molecules, thus increasing the conformality of the film.

Though the total surface area enhancement for these particulate electrodes was greater than 1000X for a thickness of 50 μm, the above results indicated that only a small percentage of the total area was accessible. To access more surface area, thickness of these electrodes were increased from 25 μm to 50 μm. All other parameters were kept constant.

These capacitors showed a capacitance density of 8-9 $\mu F/cm^2$ that is around 75 times more than the baseline value of 0.12 $\mu F/cm^2$. These results are shown in Figure 4.24

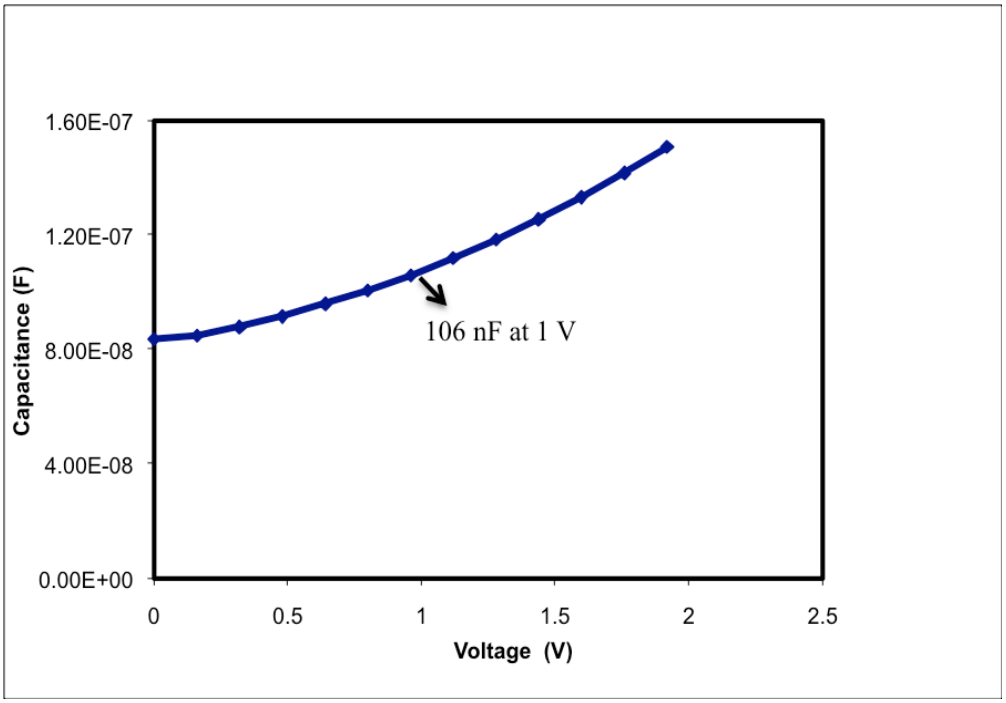


Figure 4.24 C-V plot of showing a capacitance density of 8 $\mu F/cm^2$ for particulate electrode thickness of 50 μm.

The next set of particulate electrodes was prepared with thickness ~ 75 μm. ALD Al_2O_3 with 35 nm thickness was deposited on the electrodes. The baseline capacitance density for such devices was established at 0.2 μF/cm2. These results are reported in Figure 4.25. These capacitors showed a capacitance density of 20 μF/cm^2 at 100 KHz. These electrodes showed an enhancement of 100 X in capacitance density for a thickness of 75 μm.

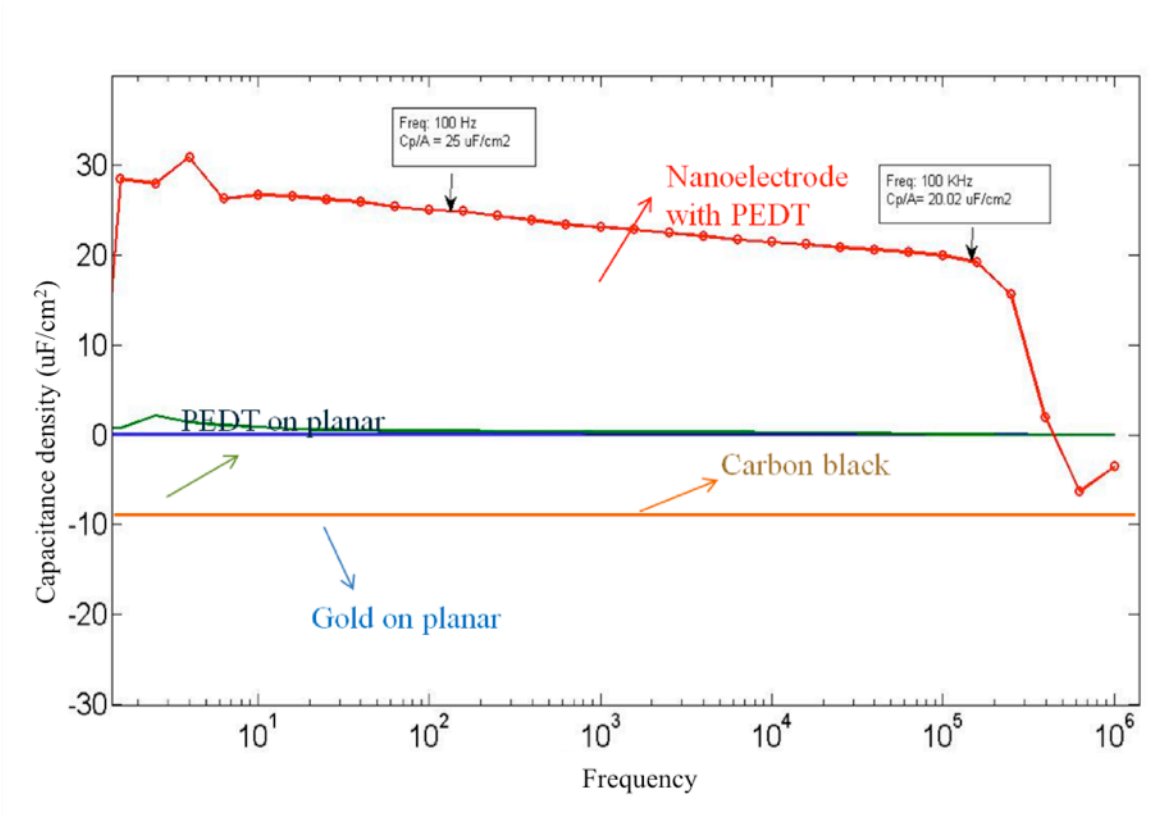


Figure 4.25 Graph showing 100X enhancement in capacitance density with particulate electrode over planar film.

Figure 4.25 showed that the capacitance of the particulate electrode based capacitors increased at lower frequencies. This increase in capacitance at low frequencies was also reported by Pyrmak et al for tantalum particulate electrode [48]. Due to the inherent resistance of the top electrode, PEDOT covering the electrode at the bottom has higher resistance due to longer conducting path as compared to PEDOT covering the particles at the top. This leads to different time constants for particles at the top and bottom, with time constant being higher for the latter. This results in increased capacitance as shown in the above figure as these bottom particles become activated at a lower frequency. Such an effect is an artifact of the bottom electrode structure and hence is not seen in planar capacitor structures.

Further improvement in the capacitor structure was made by improving the porosity of the bottom electrode. The polymer content of the paste was increased from 20% to 50%. Increase in sacrificial polymer content led to the generation of more open and continuous pores that contributed to the increase in capacitance density. These results are shown in Table 4.4.

Table 4.4 Capacitance measurements for 75 μm-thick bottom electrode.

Area (mm^2)	**Capacitance (nF)**	**Capacitance density μF/cm^2**
0.36	110	30
1	285	28

Thus using the particulate electrode approach, a capacitance density of 25 -30 μF/cm^2 was demonstrated for a 75 μm-thick bottom electrode.

4.4.2.2 Leakage current measurements

Though particulate electrode capacitors showed very high capacitance density values, the leakage current obtained from these devices was also very high.

Figure 4.26 shows the leakage current of a particulate electrode capacitor in comparison with the leakage current from planar copper electrodes using gold and PEDOT as top electrode.

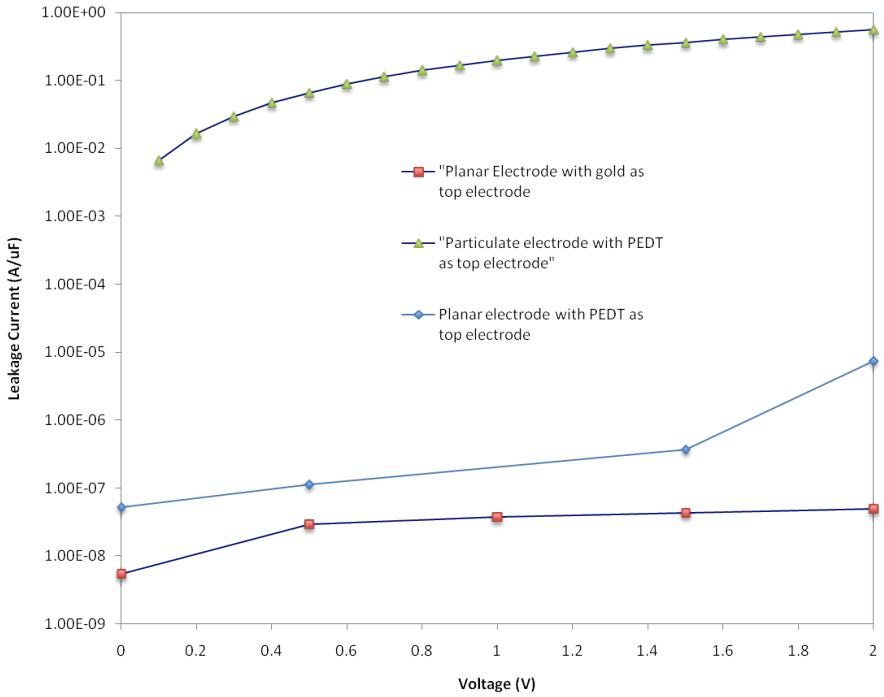


Figure 4.26 I-V plot showing high leakage current for particulate capacitors in comparison with their planar counterparts.

As can be seen from the graph, both planar electrodes as well as particulate electrodes using PEDOT as top electrode showed high leakage currents. Two different mechanisms were identified to explain such a high leakage current – (i) Interaction of PEDOT with the ALD film and (ii) Defects in the ALD film.

Interaction of PEDOT with the ALD film

The capacitor structures fabricated with PEDOT as top electrode showed higher leakage current compared to capacitor structures with gold. This high leakage current was attributed to the interaction of PEDOT with the alumina film. To further understand PEDOT-Al_2O_3 interaction, impedance spectroscopy was used to compare PEDOT-Al_2O_3 systems with Gold-Al_2O_3 systems. Gold being a noble metal does not interact with Al_2O_3 in any way and hence served as a reference electrode. Plots of imaginary vs. real part of the impedance for Al_2O_3 films were obtained for three different capacitor systems viz. (i) Cu particulate electrode-Al_2O_3-PEDOT, (ii) Planar Cu-Al_2O_3-PEDOT and (iii) Planar Cu-Al_2O_3-Au. Such plots are called Nyquist plots or Cole-Cole plots and are used to determine the ohmic resistance, double layer capacitance or charge transfer resistance of different materials. Since the real part of impedance represents the resistance, the intercept made on x-axis by the semi-circle or the diameter of the semi-circle represented the resistance of Al_2O_3 film. Figure 4.27 shows a comparative Nyquist plot on the effects of PEDOT on planar and particulate electrode.

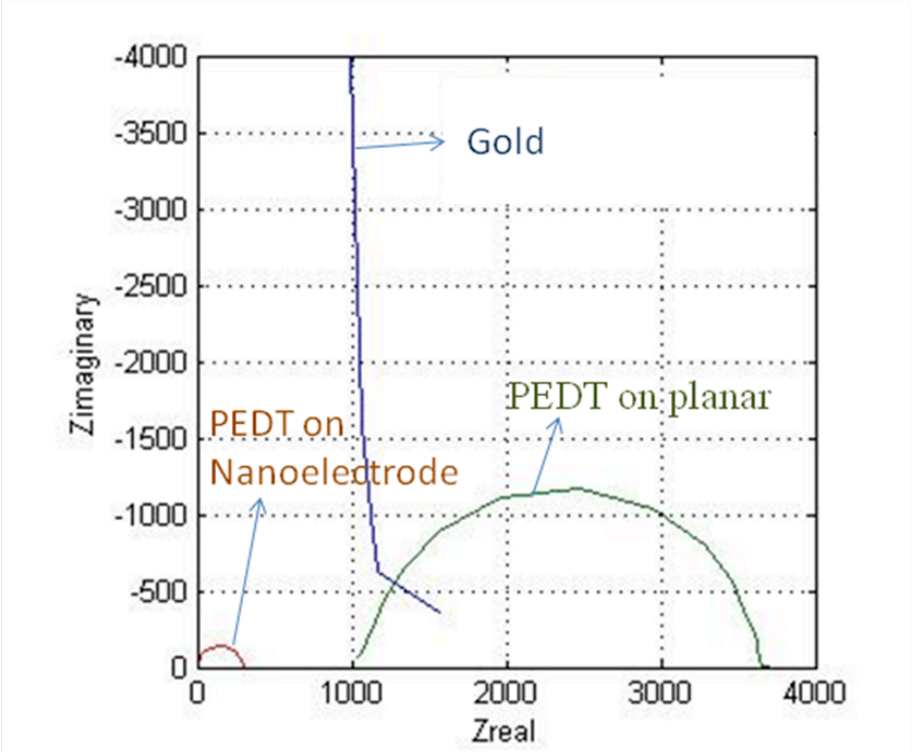


Figure 4.27 Nyquist plot showing very low resistance of Al_2O_3 when PEDOT is used as top electrode.

As already mentioned, the radius of the semicircle signifies the resistance of the dielectric film. For a large radius of semicircle such as for gold, it is inferred that the top electrode is not affecting the film in any way and therefore the resistance of the dielectric is very high. When the top electrode such as PEDOT starts interacting with the film, the resistance starts dropping and smaller radius of semi-circle is observed. The much smaller circle in case of particulate electrode is due to the large surface area enhancement that provides more room for the interaction of PEDOT and Al_2O_3 as defects in the ALD film. The high leakage current in such capacitors can be explained on the basis on metal-insulator-semiconductor (MIS) theory proposed by Freeman et al to account for high leakage currents in tantalum capacitors such capacitors due to PEDOT –Ta_2O_5 interaction[39]. According to this theory, the current flow in such capacitors is limited by

a potential barrier at the dielectric-semiconductor interface. In case of PEDOT, the residual oxidizer or the monomer leads to surface charge build up at the dielectric and PEDOT interface thus lowering this barrier and increasing the leakage current. According to another theory, the lower performance of the devices can be attributed to the in-situ chemical reaction of PEDOT resulting in a redox reaction at the interface leading to the creation of multiple oxygen vacancies on the outer layer of dielectric film. This leaves the dielectric oxygen deficient, MO_{2-x} [47-48,53]. According to Smyth et al , the leakage current is directly proportional to the oxygen loss [48]. In order to study the effect of polymer component on the alumina dielectric, core level of Al(2p) were scanned before and after the interaction and is shown in Figure 4.28

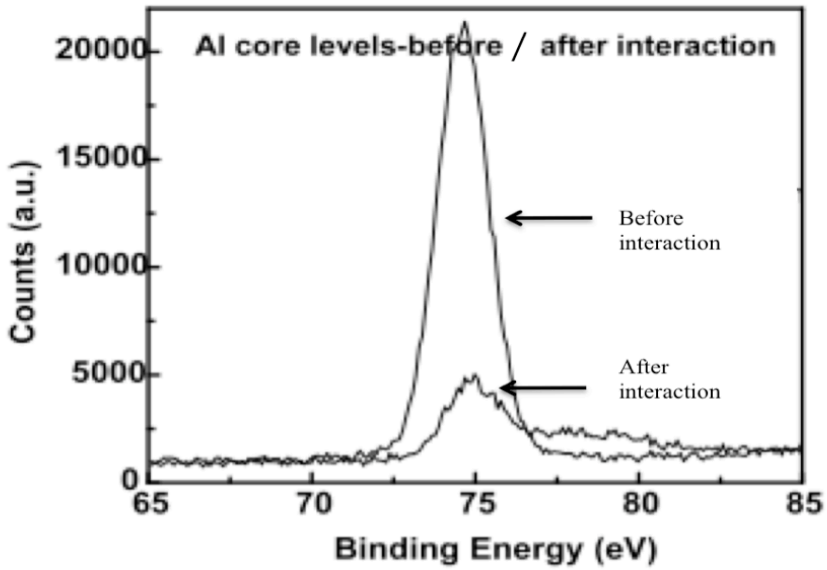


Figure 4.28 High-resolution spectrum of Al core levels (2p) for Al_2O_3 before and after interaction with PEDOT

As evident, the strong Al signal before the PEDOT attack has been reduced to almost one-fourth of the original signal following the interaction. It was also interesting to note that the aluminum signal post the chemical attack show a strong shoulder at the higher

binding energy, unlike Al peak before the PEDOT deposition. Figure 4.29 shows deconvulated core level of Al (2s) after interaction, which is fitted with 3 guassian peaks at 75eV, 77.5 and 79.3eV respectively.

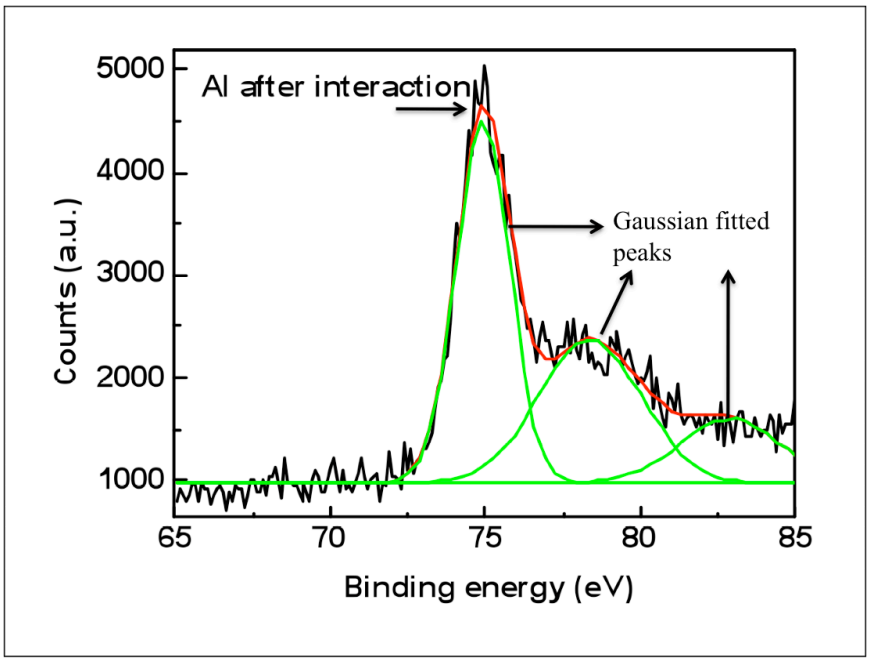


Figure 4.29 **Deconvulated Al core levels after PEDOT interaction showing various aluminum states**

The fact that the Al level shows a strong contribution at higher binding energy signifies that it has bonded with an electronegative element, which tends to pull the electron-cloud towards itself, thereby increasing the binding energy. It is believed that the free electronegative component of the PEDOT polymer is responsible for the interaction and the binding energy shift in Al core levels. This phenomenon is assumed to occur only in case of in-situ polymerized ICPs where the excess or un-reacted oxidizers remain in the cathode PEDOT.

For tantalum capacitors, since the dielectric is made by anodizing tantalum particles, a re-anodization step after polymerization helps in improving the dielectric quality. This re-anodization step heals the defects of the dielectric and hence reduces the leakage current. However such a re-anodization step is not possible in the present case as the bottom electrode is made of copper and not aluminum[64].

Defects in the ALD film on copper

In case of particulate electrodes, PEDOT-Al_2O_3 interaction coupled with the higher defect density in the Al_2O_3 film can be used to explain high leakage current values. Section 4.2 indicated that ALD alumina film was not entirely defect free over large areas. For particulate electrodes, the effective surface area was 150 times more than that of their planar counterparts, thus making these substrates more prone to defects. These defects, in the form of pin-holes and thin spots, can result in high leakage current values and lower BDVs. Thin-spots are formed due to insufficient exposure times as already discussed in section 4.2 and can be eliminated by optimizing the exposure time. The presence of pin-holes can be explained on the basis of nucleation problems during growth of alumina on copper substrates. Similar results were also reported by Zhang et. al. who found the defect density to be higher on copper substrates as compared to other substrates[63]. The origin of ALD nucleation defects on copper substrates is not very well understood but can be attributed to the absence of surface hydroxyl groups. Presence of impurities (organic residue from the polymer or the dispersant), surface roughness and surface oxidation may further prevent the nucleation of Al_2O_3 on copper. Thus it is extremely important to control the process parameters to ensure complete removal of all organic matter and

prevent surface oxidation of copper. To demonstrate the feasibility of defect free ALD film over copper, ultra-thin particulate electrode capacitors with sputtered copper as top electrode were fabricated as discussed in next section.

4.4.3 Demonstration of low leakage current particulate electrode capacitors

The high leakage current from particulate electrode was attributed to the interaction of PEDOT with Al_2O_3 dielectric and the inherent defects in the ALD film over large surface areas. Thus to obtain lower leakage, thin films of particulate electrode were fabricated and PEDOT was replaced by sputtered copper as top electrode. The thickness of the deposited ALD film was increased from 50 nm to 90 nm. This further helped in reducing the defect density. Compared to thick particulate electrode films (25-75μm), these thin films provided better control over the surface of copper particles that was required to reduce the defect density in the deposited alumina films. Ultra-thin bottom copper electrode was spin-coated on copper foils, so as to attain thickness less than 5 μm, with similar paste processing chemistry as reported in chapter 3. These thin films were sintered at 600^{o}C for 5 min under reducing atmosphere to eliminate all sharp edges and facets and a 90 nm of ALD alumina was deposited as the dielectric. The exposure time of ALD precursors was maintained at 3 seconds even for these thin films. Complete removal of all organic residues was ensured to eliminate nucleation defect sites. The higher exposure times helped in completely saturating the surface with precursor molecules, thereby resulting in a good quality alumina film. Possibility of nucleation delay over copper was reduced by increasing the number of cycles of the ALD film. Finally, copper

was sputtered using a shadow mask to complete the capacitor structure. Sputtering is able to coat only the top-most particle layer with very limited capability to reach the next layer of underlying particles. As a result, the capacitance enhancement observed in these devices was very low. The capacitance vs. voltage plot of such a device is shown in Figure 4.30.

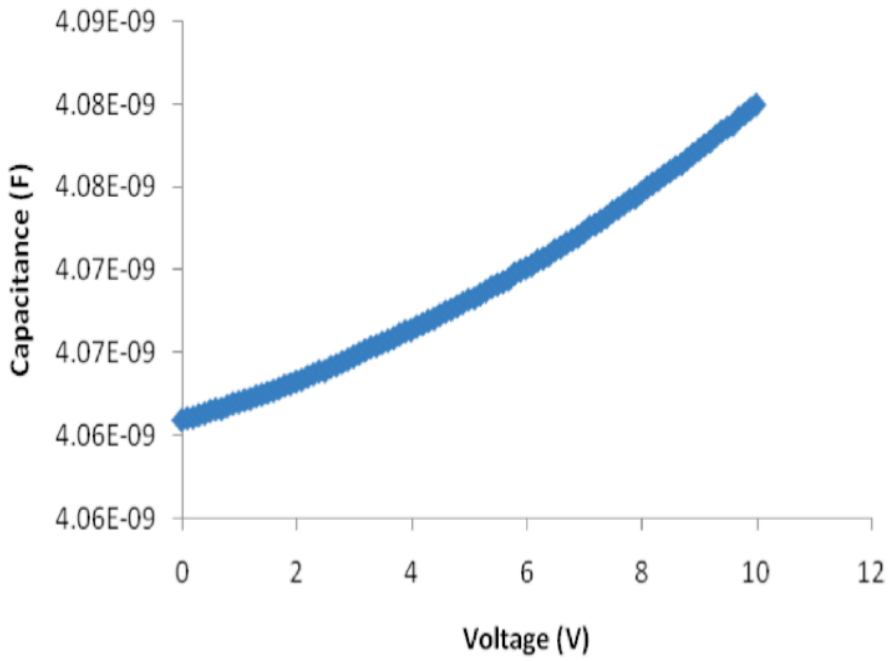


Figure 4.30 C-V plot of particulate electrode with sputtered copper as top electrode showing 2X enhancement in capacitance density.

As can be seen, a capacitance density of 0.12 μF/cm^2 was obtained which is twice when compared to the planar counterparts (baseline value 0.07 μF/cm^2) of these capacitors.

The leakage current for these devices is shown in Figure 4.31. These devices exhibited very low leakage current with a breakdown voltage higher than 40 V. The leakage current at 3 V for these devices was observed at 200 nA/μF which was comparable to the leakage current of Al_2O_3 on pristine copper and sintered copper as reported earlier in section 4.2. The I-V plot shows that when PEDOT was replaced by sputtered copper as top electrode, the leakage current of particulate electrode capacitors decreased dramatically.

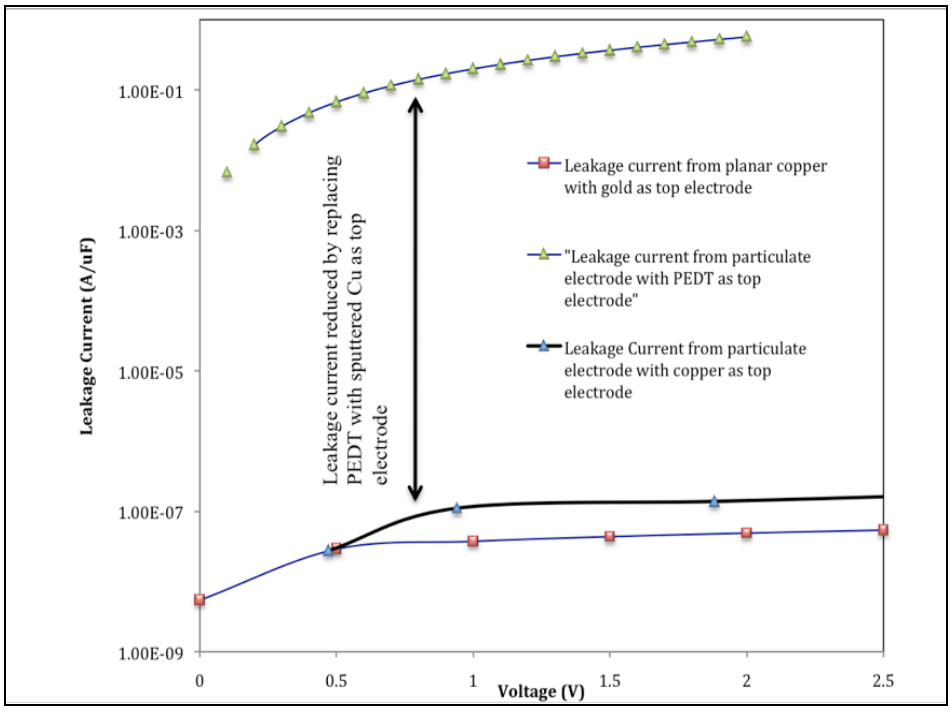


Figure 4.31 I-V plots of particulate electrode capacitors with (i) sputtered copper and (ii) PEDOT as top electrode.

Thus, using spin-coated copper particulate electrode films, ALD Al_2O_3 dielectric and sputtered copper as top electrode; it was possible to obtain very low leakage current capacitors with 2 times enhancement in capacitance density as compared to their planar

counterparts. This indicates that the key to obtain lower leakage current in particulate electrode lies in:

(i) Choosing a top electrode that is inert to the dielectric

(ii) Ensuring complete removal of nucleation defect sites by eliminating organic residue from the bottom electrode.

Therefore, by further process modifications during fabrication of bottom electrode, it is possible to obtain similar results using thicker films for high surface area enhancement. This makes the particulate electrode capacitor technology extensible to very high capacitance density values with acceptable leakage current values. Depositing thicker ALD films on particulate electrodes would further help in overcoming the nucleation delay problems by providing sufficient time for the surface preparation.

5 CONCLUSIONS AND RECOMMENDATIONS

Over the past few decades, the volumetric efficiency of high-density capacitors has only gone through incremental changes because of several fundamental limitations with existing capacitor technologies. Today's high-density capacitor technologies either suffer from low surface area because of the micro scale electrodes or low permittivity dielectrics or both. In this work, a silicon-compatible, novel particulate electrode capacitor approach with a surface area enhancement of 150 X leading to a capacitance density of 30 $\mu F/cm^2$ is demonstrated. To achieve this surface area enhancement, micron sized copper particles were used to fabricate thin film electrodes directly on silicon at CMOS-compatible temperatures. A thin film of Al_2O_3 as dielectric was conformally deposited on these high surface area electrodes using ALD technique. Finally, polyethylene dioxthiophene (PEDOT), which is a conducting polymer, was used as a top electrode to complete the capacitor structure.

Fabrication of high surface area bottom electrode was the most challenging part of this study as it necessitated the printing of a well-dispersed copper paste on silicon substrates and further sintering them at low temperatures. Careful process control was required to obtain a highly porous structure with adequate strength and integrity. Various parameters such as particle size distribution, paste processing conditions and sintering temperatures were studied and optimized to achieve 150 X enhancement in surface area for a 1 mm^2 device with 75 micron thickness.

Conformal deposition of moderate permittivity dielectrics on these complex 3D structures constituted another challenge for this study. ALD was used to deposit Al_2O_3 films as dielectric and the intrinsic properties were investigated on planar copper films. These films exhibited excellent dielectric properties. The leakage current for a 50 nm thick dielectric on planar copper electrode was observed to be less than 100 nA/μF till atleast 15V and the BDV was around 40V. The deposition process parameters were then modified by using rough copper foils before transferring the process to particulate electrodes. The exposure time of the ALD process was increased to 3 seconds in order to obtain conformal coatings on particulate electrode.

With PEDOT as the top electrode, particulate electrode capacitors showed a capacitance density of 30 μF/cm ^{2} at 100 Khz. However the leakage current from such capacitors remained very high. The leakage current was attributed to two factors (i) PEDOT-Al_2O_3 interaction that created defects in the films and (ii) intrinsic defects in the Al_2O_3 films deposited over particulate electrodes. By replacing PEDOT with sputtered copper and modifying the bottom electrode process parameters, it was possible to obtain leakage current < 150 nA/μF on particulate electrodes.

Recommendations

A capacitance density of 30 $\mu F/cm^2$ was demonstrated for particulate electrode capacitors using ALD Al_2O_3 as dielectric and PEDOT as top electrode. Defects in the dielectric film and the Al_2O_3 –PEDOT interface put forward critical challenges that resulted in high leakage currents. In order to further increase the capacitance density and improve the electrical properties of the film, some modifications and additions in the processes were identified and recommended below:

1) HRTEM/FIB Characterization: High-resolution transmission electron microscopy (HRTEM) can be used to study the cross-section of the electrodes prepared by focused-ion beam (FIB). FIB would generate cleaner cross-sections for inspection and examining them with HRTEM would provide more insight on the conformality of the dielectric film over particulate electrode. It would also help in understanding the nature of defects in the dielectric film. PEDOT-Al_2O_3 interface study would provide a better understanding of the leakage current mechanism prevalent in particulate electrodes.

2) Well-dispersed copper suspension for a more open structure: Obtaining a well-dispersed copper suspension is the first step for fabrication of high surface area particulate electrodes. The porosity not only increases the surface area but also enhances the conformality of the dielectric film as it facilitates easy diffusion of precursor molecules. By controlling the dispersant and the sacrificial polymer

content, a well-dispersed suspension of copper powder can be obtained that would eventually lead to highly open and porous structure.

3) Replacing Al_2O_3 with higher permittivity dielectrics: By replacing Al_2O_3 with higher permittivity dielectrics such as HfO_2, ZrO_2 or composite films such as HfO_2 doped with Er, $SrTiO_3$ etc. capacitance densities as high as 100 $\mu F/ cm^2$, with enhanced electrical properties ,can be obtained from these capacitors.

4) Alternative top electrodes: Replacing PEDOT with other solution-derived electrodes that have better compatibility with ALD Al_2O_3 films can improve the electrical characteristics of these capacitors. Solution derived metal oxides such as MnO_2 or RuO_2 can be potential candidates to replace PEDOT as top electrode. Alternatively ALD metal (Pt or Ru) can also be pursued as a top electrode.

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