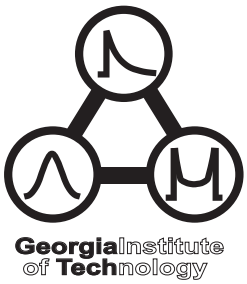

The Propagation Group

Broadband Spatio-Temporal Channel Sounder for the 2.45 GHz ISM Band

Document ID: PG-TR-050828-RJP

Date: 28 August 2005

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EXECUTIVE SUMMARY

This report documents the research efforts of the Propagation Group at Georgia Tech towards the construction of a broadband spatio-temporal channel sounder for the Aerospace Corp. The final channel sounder, a valuable research tool in radio frequency (RF) channel and direction finding (DF) measurement, was constructed from the 8-element antenna array receiver setup on loan from Aerospace Corp. to support this collaborative project.

Upon completion of the 2005 portion of this on-going collaboration, the following upgrades were made to the system:

- A custom broadband *pseudo-random noise generator* was designed and built.
- A custom *vector RF signal generator* was designed and built.
- Software for controlling the RF equipment, acquiring data, and processing spatio-temporal waveforms was written.
- The new 8-channel analog-to-digital converter unit provided by the Aerospace Corp. was integrated into the system and shown to operate adequately.

In addition to these improvements, a sample measurement was taken to demonstrate basic channel sounding operation. Collectively, these outputs fulfill the research deliverables for the year 2005 collaborative project between Aerospace Corp. and Georgia Tech.

Future work for this ongoing collaboration will likely involve more measurements and further miniaturization of the array channel sounder. The ultimate goal of the research should be a single compact receiver box containing all RF components and analog-to-digital conversion hardware. This box could then be plugged into a laptop computer and an arbitrary array manifold for portable direction-finding and channel measurement. When coupled with the array processing software developed during the 2004 phase of this collaborative project, the end result will be a dynamic, portable unit capable of both spatio-temporal channel sounding and/or accurate DF location of 2.45 GHz radios in a complicated radioscape.

Chapter 1

INTRODUCTION

This technical report describes the construction of a broadband spatio-temporal channel sounder operating at the 2.45 GHz frequency band. Based on the core 8-element receiver system provided by the Aerospace Corp., Georgia Tech graduate student researchers Chris Durkin and Ryan Pirkl designed and built new hardware that allows broadband RF channel sounding with increased mobility for measurement. Key contributions include a new high-speed *pseudo-random noise (PN) generator* for transmitting a broadband waveform, a *vector RF signal generator* for generating stable, programmable frequencies to drive receiver hardware, and spatio-temporal data acquisition software.

This work is a continuation of the direction-finding research collaboration conducted by the Aerospace Corp. and the Propagation Group at the Georgia Institute of Technology. The new channel sounding system is capable of resolving multipath with up to 20 ns of time-of-arrival delay. To demonstrate this capability, Chapter 4 presents an example measurement conducted indoors at 2.45 GHz. The measurement system is shown capturing a channel sounding waveform with 100 MHz RF bandwidth on the 8 different antenna elements simultaneously.

1.1 Motivation

All terrestrial direction-finding (DF) receivers must contend with the distorting effects of multipath propagation as well as the ever-increasing number of in-band radio interferers. This is especially true when ranging mobile wireless terminals such as those operating in the 2.4 GHz *industrial-scientific-medical* (ISM) band, which operate in high multipath, high interference environments.

The combination of broadband channel sounding capability with the 8-element receiver array is a powerful research tool for illuminating the spatio-temporal characteristics of the radio channel at 2.4 GHz. A new, custom array manifold must be built, however, and calibrated for use in scientific measurements. Once completed, the existing 8-channel receiver structure illustrated in Figure 1.2 can be used to acquire and store signals in software. PN correlations may then be performed in software to extract channel information as a function of delay; direction finding (DF) algorithms may simultaneously be performed in software to extract spatial channel information.

Not only are conventional space-time statistics (angle-of-arrival, time-of-arrival, delay spread, angle spread, etc.) available with such measurements, but we propose a new technique for extracting multipath characteristics from within a measured delay "bin". Each delay "bin" contains a variety of multipath components which will produce small-scale fading in space. An example of such broadband fading is illustrated in Figure 1.1.

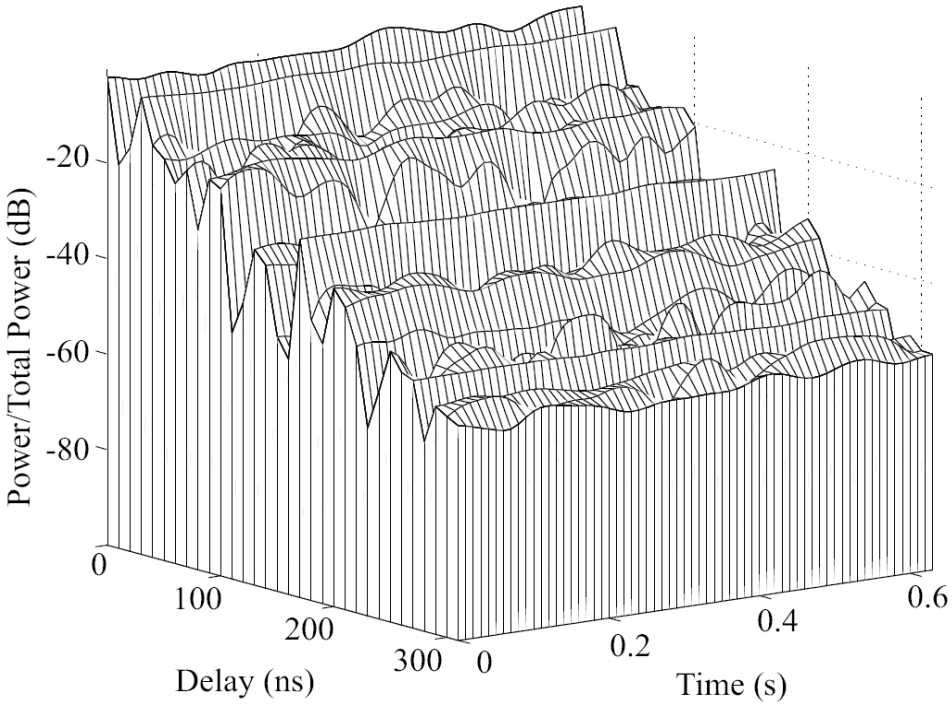


Figure 1.1 Example of a broadband channel fading as a function of motion. The various delay samples undergo various levels of Rician fading, revealing the underlying multipath structure of the channel [Dur03a].

Usually, the intra-bin multipath consists of one or two dominant, specular wave components and a group of smaller multipath waves that can collectively be regarded as *diffuse* power. By dragging the receiver antennas through space, it is possible to collect a histogram of fading power for each delay "bin". The unique shape of the histogram will illuminate the underlying multipath structure [Abd00], [Dur02].

1.2 Synopsis of Upgrades

The central goal of the 2005 collaboration between Aerospace Corp. and the Propagation Group of Georgia Tech was to improve hardware of the Aerospace Corp.'s 2.45 GHz 8-element array receiver. With several modifications, the array measurement system was upgraded into a scientific-quality

broadband measurement system. As shown in the block diagram in Figure 1.2, the following improvements were made to the system:

A A high-speed pseudo-noise (PN) sequence generator was designed and constructed for use as a transmit waveform. Capable of using the entire 2.45 GHz ISM band, the waveform allows temporal channel sounding by a *sliding correlator* receiver and spatio-temporal channel sounding by an antenna array receiver [New96a], [New96b]. See Chapter 2 for more details.

B Custom-built transmitter monopole antennas allow uniform illumination of the environment. These quarter-wavelength monopoles may be used as array elements as well.

C A custom *vector RF signal generator* was designed and build to drive the additional system ports requiring oscillators. This programable unit drives 3 different oscillators based on a common, highly stable reference. Built in a light-weight enclosure, the vector RF signal generator replaces 3 bulky test-and-measurement signal generators from the receiver, thus increasing the system mobility for measurement campaigns. See Chapter 3 for more details.

D The Aerospace Corp. provided us a new, high-speed Analog-to-Digital converter that was meant to correct several data acquisition problems with the old unit. This new unit was integrated and tested into the current set-up. The new A/D board was found to function adequately.

E Acquisition software was written for controlling, acquiring, and interpreting the channel sounding waveform at 2.45 GHz from up to 8 simultaneous antenna elements. See Chapter 4 for more details.

These improvements are demonstrated in Chapter 4 with a simple indoor data acquisition using the 8-element dipole array.

1.3 Future Work

In 2004, the collaboration between Aerospace Corp. and Georgia Tech resulted in a suite of software capable of analyzing the various direction-finding algorithms for measurement data. In 2005, the collaboration resulted in a working spatio-temporal channel sounder with an 8-element array. Future collaboration should focus on two areas. First, we are now in a position to conduct some very interesting and revealing scientific measurements in the 2.4 GHz band. This, by itself, would produce fascinating research.

Second, our recent progress in hardware development has demonstrated the value of miniaturizing the data acquisition system. A smaller, low-powered measurement system could prove extremely valuable, both as a research tool and as a platform for commercial direction-finding applications.

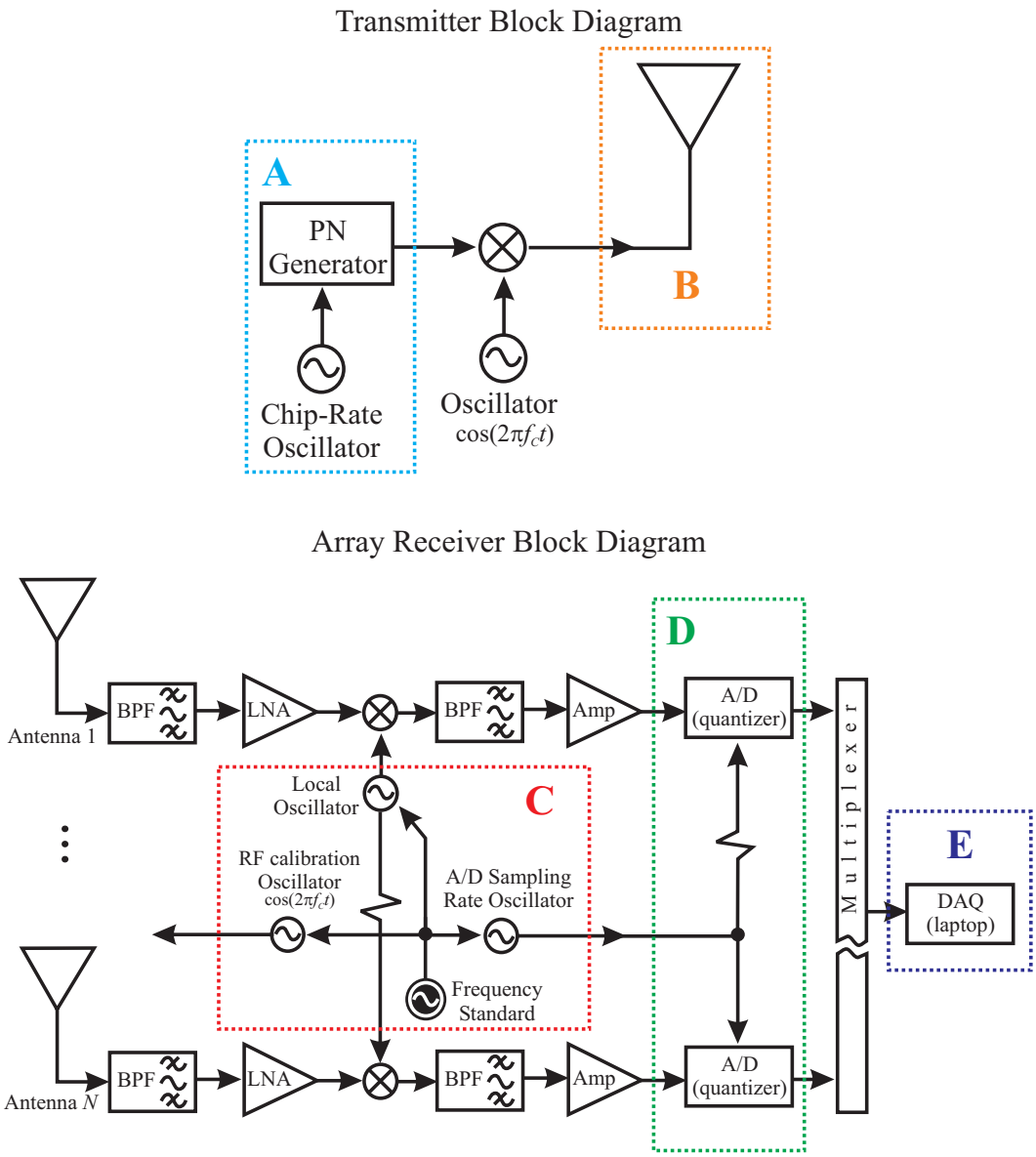


Figure 1.2 Transmitter and receiver block diagrams of the array channel measurement system.

It is one of our ambitions at Georgia Tech to collapse the entire measurement hardware – from RF front end to digital output of the D/A boards – into a small, portable box that interfaces directly to a laptop computer.

Chapter 2

PSEUDO-RANDOM NOISE GENERATOR DESIGN

2.1 Basics of Channel Sounding

This section presents the basic principles of channel sounding using spread spectrum waveforms.

2.1.1 Properties of m-Sequences

A channel sounder works by sending a broadband signal over a given channel using a technique called *spread spectrum* [And02]. Spread spectrum originated as a means of secure communication for the military, spreading a signal out in the frequency domain to give it a very low peak power. To observers, a spread spectrum signal looks similar to white noise, and thus has a Low Probability of Intercept (LPI). The noise-like properties of a spread spectrum signal are achieved by modulating the signal with a pseudo-random noise (PN) code, which is a pseudo-random binary sequence. PN codes are generated by shift registers configured with linear feedback taps, and this will be detailed in a later section. The PN code exhibits the following properties:

1. The Maximal Length Linear Shift Register (MLSR) sequence has a period of L chips, with $L = 2N - 1$. (That is, an N bit shift register can generate a PN code of L bits, where the maximum value of L is $2N - 1$.)

2. The statistical distribution of "1's" and "0's" is the same as in a random sequence with the exception that the total number of "1's" is always one larger than the total number of "0's", independent of the length of the code. (Note that this implies only codes of odd length are possible.)

3. The modula-2 sum of any m-sequence with a shifted version of itself produces another shifted version of the same sequence.

4. All possible N-bit words will appear in the sequence exactly once, except for the all-zeros

combination. (The all-zeros combination should never occur because the shift register will become locked in this state.)

5. The ideal autocorrelation of the PN sequence is given by $R_{xx}(\tau)$:

$$R_{xx}(\tau) = -\frac{1}{L}\sum_{l=-\infty}^{l=+\infty}\left(1+\frac{1}{L}\right)\Delta\left(\frac{\tau - lLT_c}{T_c}\right) \tag{2.1.1}$$

where T_c is the chip period and $\Delta(\cdot)$ is the triangle function:

$$\Delta\left(\frac{t}{\tau}\right) = \begin{cases} 1 - \left|\frac{t}{\tau}\right| & |t| \leq \tau \\ 0 & |t| > \tau \end{cases}$$

The spectrum of the PN code follows a $\text{sinc}^2(f)$ envelope, with the nulls occurring at integral multiples of the clock frequency [And02]. The spectrum is made up of discrete peaks between envelope nulls. The number of peaks between nulls is given by $L-1$ where L is the length of the PN sequence. Figures 2.1 and 2.2 show the spectrum and autocorrelation of the PN code.

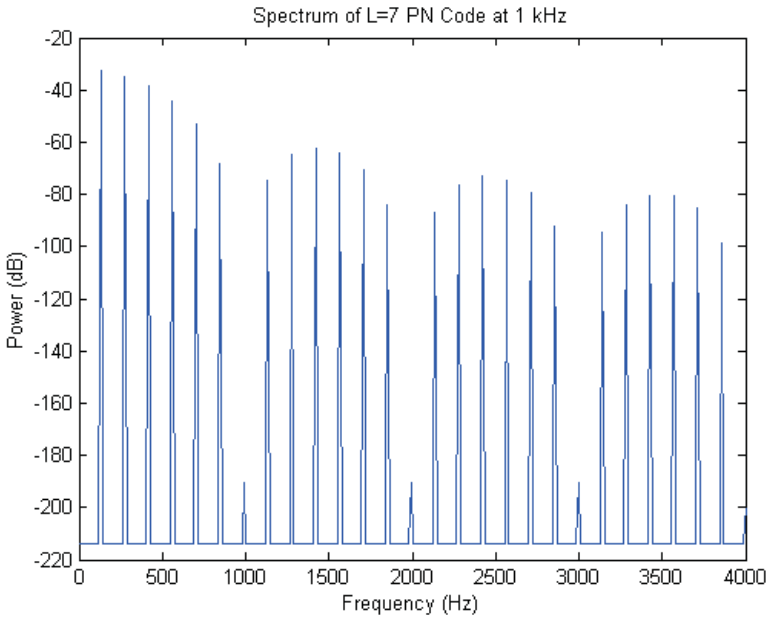


Figure 2.1 Spectrum of an $L = 7$, $f_c = 1$ kHz PN sequence.

2.1.2 Channel Sounder Fundamentals

The sliding correlator channel sounder clocks the PN codes at very high frequencies to fill a wireless channel with noise-like content [New96b], [New96a], [And02]. The PN codes are modulated onto the

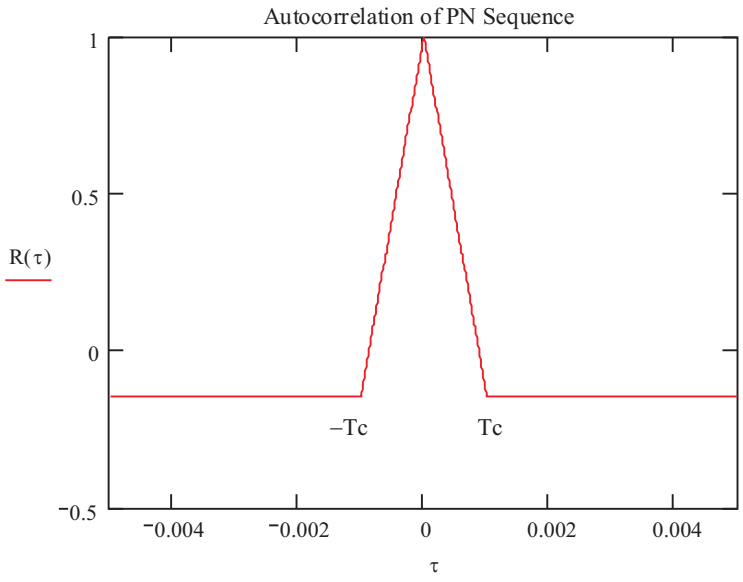


Figure 2.2 Normalized autocorrelation of an $L = 7$, $f_c = 1$ kHz PN sequence.

carrier frequency and transmitted across the channel. Some distance away, a receiver demodulates the signal and performs the "sliding correlation". The received PN code, which is clocked by the transmitter at some frequency f_T, is mixed with an identical PN code clocked by the receiver at some slightly slower frequency f_R. Because the received PN code is clocked at a higher frequency than the PN code generated at the receiver, the received code slides past the slower receiver-generated code in time.

When the faster code slides past the slower code such that they are momentarily perfectly aligned, the crosscorrelation will be very large. At points of poor alignment, the crosscorrelation will be $-1/N$. This was indicated by the autocorrelation of the PN code. A series of alignments due to the multipath environment will generate a series of triangular peaks in the crosscorrelation. This effectively is the impulse response of the channel. By taking the Fourier Transform of this impulse response, the frequency response of the channel may be found.

2.1.3 PN Generation

The PN generator is based around a shift register configured with linear feedback [Ins]. Certain registers on the shift register are selected as feedback taps. The bits at these taps are XOR-ed together (modulo-2 addition). The output of the modulo-2 addition is sent to the input of the shift register. This configuration is the Fibonacci architecture for a linear feedback shift register. Another

configuration, called the Galios architecture, is functionally equivalent but performs operations in parallel, rather than in series. The Galois PN generator is generally faster than the Fibonacci PN generator due to its parallel architecture. Figure 3 compares a Galois and Fibonacci implementation.

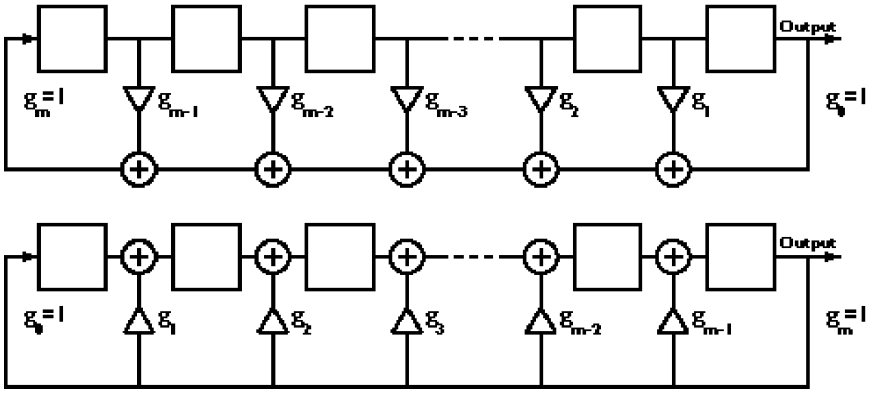


Figure 2.3 Fibonacci (top) and Galois (bottom) linear feedback [Ins].

Note that the Galois architecture requires parallel I/O for the shift register, while the Fibonacci implementation requires shift-in/parallel out for the shift register. One other item of interest is that the "output" of a PN generator can be taken from basically anywhere in the circuit. All registers and XOR gates will output the same PN code, though they will all be out of phase from each other.

Selecting the correct registers to use as feedback taps is an important in designing the PN generator. Only certain feedback configurations give rise to what is called a maximal-length sequence, or m-sequence for short. M-sequences are the longest possible codes that a PN generator can produce before repeating. For an N-bit shift register, its m-sequence length is given by L:

$$L = 2^N - 1 \tag{2.1.2}$$

All other feedback tap configurations will result in a sequence length that is less than L. Therefore, to make the best use of the shift register, it is important to choose feedback taps that give rise to an m-sequence. This is not a difficult task, as data tables abound that provide the proper feedback taps for a given shift register size [Ins].

In order to begin outputting the PN code, the shift register must be initialized to some non-zero value. Typically, the shift register is filled with 1's via the use of an OR gate between the final XOR gate and the shift register [And99]. One of the OR gate inputs is the XOR gate output. The other OR gate input is used to switch the PN generator between initialization mode and normal operation. A diagram of this setup is shown in Figure 2.4.

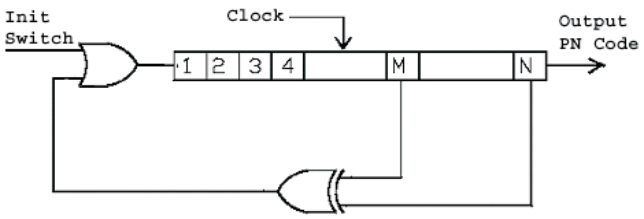


Figure 2.4 Diagram of a two-tap linear feedback shift register.

2.1.4 PN Generation Schemes

There are two principle variables that had to be determined before design could begin. These were the clock frequency fc of the PN generator and the size of the shift register N. The choice for these variables has a tremendous effect on the performance of the sliding correlator channel sounder, as is indicated in Table 2.1.

Table 2.1 System Parameter Dependencies [And02].

System Parameter	PN Generator Property	Dependence
Time Domain Resolution of Multipath Signals	Clock frequency, f_c	$T_{Res} = \frac{1}{f_c}(\text{sec})$
Dynamic Range	Code length, L_{PN}	$D_R = 20\log(L_{PN})(\text{dB})$
Maximum Resolvable Multipath Delay Time	Code length and Clock frequency	$T_{Max} = \frac{L_{PN}}{f_c}(\text{sec})$
Process Gain	Slide factor, k, and Clock frequency	$G_P = 10\log\left(\frac{0.88 f_c}{k}\right)(\text{dB})$
Maximum Doppler Shift Resolution	Slide factor, Clock frequency, and Code length	$f_{D_{MAX}} = \frac{f_c}{2kL_{PN}}(\text{Hz})$
RF Bandwidth	Clock frequency	$BW = 2f_c\,(\text{Hz})$

The dynamic range and RF bandwidth can be calculated from this table. The dynamic range is related to the peak value of the autocorrelation and thereby, the length of the sequence. When a longer sequence is autocorrelated, its peak value will be greater than that of a shorter sequence. Greater dynamic range allows for more accurate analysis of the channel and a greater SNR of the

output impulse response. The initial PN design in this project used a 9-bit shift register architecture.

The RF bandwidth refers is directly related to the clock frequency. The sliding correlator channel needs to produce a wide band signal to determine the frequency response of the wireless channel. Therefore, the PN generator must be clocked at a very high frequency. Recall that the PN code spectra resembles $\text{sinc}^2(f)$ with nulls occurring at the integer multiples of the clock frequency. The RF bandwidth is a measure of the size of the main hump in the envelope, as much of the spectral power is in the range of $\pm f_c$. Thus, the faster the PN generator is clocked, the larger the bandwidth of the signal. It is desired to sound the channel with signals that have a bandwidth of 1 GHz or more, so the PN generator must be able to operate at extremely high frequencies. Clocking at these frequencies requires a special family of integrated circuits called Emitter-Coupled Logic (ECL). See Appendix A for more information about ECL circuit design.

2.2 Circuit Design

The PN generator was designed using ECL devices. There were five main components of the PN generator design: the 3 Volt sink, the shift register clock, the bias voltage, the initialization circuit, and the linear feedback shift register (LFSR).

2.3 3 Volt Current Sink

It was mentioned earlier that the Thevenin equivalent termination scheme seemed to be the preferred method, but for some reason this scheme had implementation problems that resulted in the destruction of several devices. Therefore, after much difficulty, the 3 V supply scheme was chosen. However, this presented another problem, because with the exception of the ground terminal, most power supply terminals do not sink current very well. Tests showed that voltage would build up on the 3 V supply terminal if one tried to sink too much current into the terminal, leading to an actual voltage greater than 3 V. To resolve this problem, it was found that by connecting a resistor from the 3 V terminal to ground allowed the power supply to divert any current going into the 3 V terminal to ground. The value of this resistor should be chosen so that the current from 3 V to ground is always equal to or greater than the current being sunk into 3 V.

Of course, this is not a very elegant scheme, and still requires an extra supply. To avoid this, a 3 Volt sink was designed using an op-amp and a PNP transistor. The op-amp was configured as a voltage-follower to produce 2.3 V at the base of the transistor. The transistor was operated in the forward-active region to ensure approximately a 0.7 V drop from the emitter to the base. By grounding the collector terminal, the voltage drop from emitter to collector was approximately 3.0 V. Looking into the transistor from the emitter, the transistor has a very low impedance and thereby acts as an excellent current sink.

To generate the 2.3 V at the op-amp output, a simple voltage divider was used. The actual voltage generated by the voltage divider was 2.27 V. However this was acceptable, as it was better for the 3 Volt sink to be a slightly less than 3 V rather than greater. This would mean that the ECL outputs would source slightly more current than nominal, but also makes it less likely for V_{TT} to ever be greater than V_{OL}. Another caveat of the current sink was that, in order for the transistor to operate in the forward-active region and thereby have $V_{EB} = 0.7$ V, the transistor had to sink at least 20 mA of current. When an ECL output is low, it sources $0.25/50 = 5$ mA, and when high, $1.05/50 = 21$ mA. Obviously it is not difficult to meet this requirement simply by connecting devices to the current sink. However, to ensure that the 3 Volt sink is always approximately 3 Volts, a 100 ohm resistor to V_{CC} was used to sink 20 mA of current into the transistor's emitter. The final 3V current sink circuit is shown in Figure 2.5.

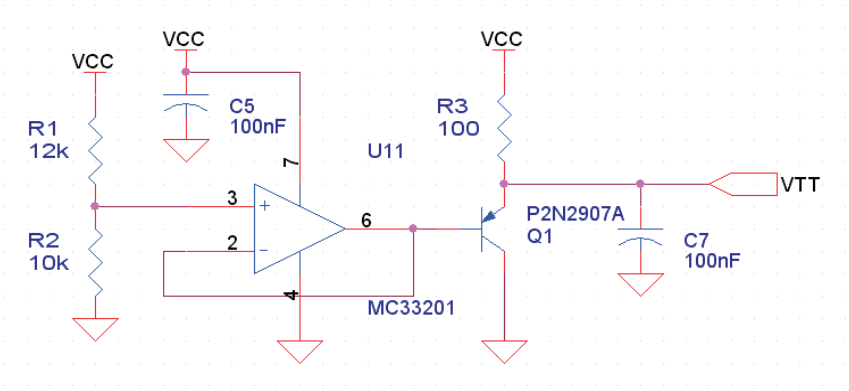


Figure 2.5 Schematic of 3V current sink (V_{TT}).

When implementing this sink, there were several other considerations. For one, all the current entering the emitter will be divided between the collector and the base, with the majority going to the collector as defined by $i_E = i_C + i_B = (\beta + 1)i_B$ where β is the current gain for the transistor. This means that a very small amount of current will go through the op-amp to ground, and it is important to ensure that the amount of current is within the op-amp's current sinking limits. The op-amp used in the circuit, which was an MC33201 could sink or source up to 80 mA. Also, the transistor used here, which was a P2N2907A, can sink at most 600 mA of current. If we assume all ECL outputs connected to this sink are high and generously estimate an output high current of 30 mA (corresponding to $V_{OH} = 4.5$ V), taking into account the 20 mA provided by the pull-down resistor the current sink can support at most (600 mA - 20 mA)/(30 mA) = 19.3, or 19 ECL outputs. Even with a current gain as low $\beta = 50$ the base current is only 12 mA – well within the specifications of the op-amp.

2.3.1 Shift Register Clock

The shift register clock was designed around the MC10EP16 differential receiver. This chip has a V_{BB} pin to be connected to the unused input of its differential input, as described in an earlier section. This proved to be the only V_{BB} source available in the overall design, so this pin was connected to an op-amp configured as a voltage-follower. This provided a steady V_{BB} source that could be connected to other chips where a single-ended output was connected to a differential input. Additionally this alleviated the need to consider how much current the V_{BB} pin was actually sourcing. Note that the V_{BB} pin was not an actual ECL output and thus did not require current sourcing to reach the proper voltage level.

The circuit shown in Figure 2.6 was used to bias an 800mVp-p 0VDC square wave to the proper voltage levels required by the ECL devices. Early biasing circuits used V_{BB} to bring the input clock up to proper voltage levels. However, this coupled the clocks noisy signal onto V_{BB}. It was therefore decided to bias the clock using a voltage divider circuit that generated an approximation of V_{BB}.

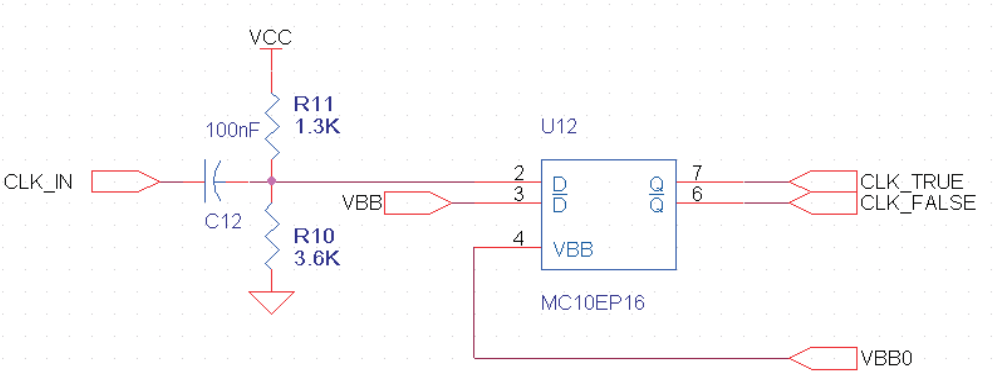


Figure 2.6 Schematic of clock-biasing circuit.

An 800 mVp-p, 0 VDC square wave is fed into the circuit via the capacitor. The capacitor serves as a DC block but allows the square wave to pass. The two resistors generate an approximation of V_{BB}, pulling the clock signal up to proper ECL voltage levels. This is then fed into the true input of the MC10EP16. The inverted input is tied to a buffered V_{BB}. According to the specifications for an ECL differential input, the input will be high when the true input is greater than the inverted, and the input will be low for the reverse case. The MC10EP16 essentially acts as a high-speed buffer.

2.3.2 Bias Voltage (V_{BB})

The ECL bias voltage, V_{BB}, was generated by an op-amp configured as a voltage-follower. The reference voltage was V_{BB0} generated by the MC10EP16 driver. Capacitors decouple V_{BB0} and

V_{CC}. The bias voltage circuit is shown in Figure 2.7.

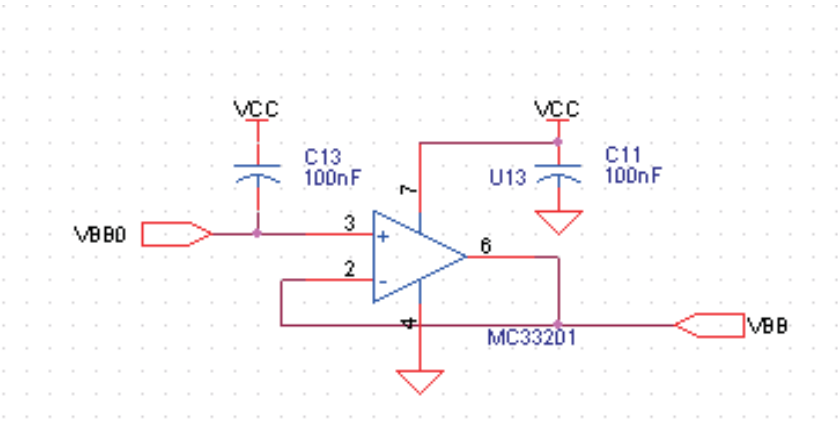


Figure 2.7 Bias voltage circuit.

2.3.3 Initialization Circuit

The initialization circuit shown in Figure 8 was used to set the output of the OR gate high. This caused the shift register to fill with binary '1's and initialized the PN sequence. A voltage divider was used to generate approximately 4.05 V. When the switch is pressed, PN_INIT goes high. When the switch is released, PN_INIT floats low, because it is connected to an input of the OR gate that defaults to '0' when open.

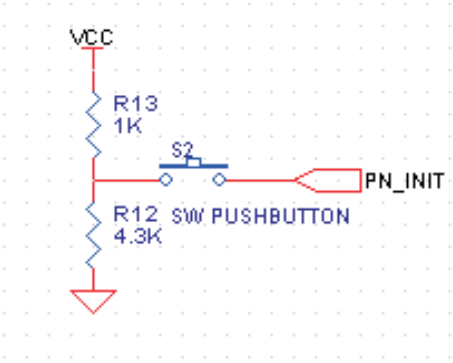


Figure 2.8 PN initilization circuit.

2.3.4 Linear Feedback Shift Register

The linear feedback shift register (LFSR) circuitry shown in Figure 9 consists of three ICs: the MC10EP142 9-bit shift register, the MC10EP08 differential XOR gate, and the MC10EP01, a single-ended quad-input OR gate. When properly configured, the LFSR's maximal length sequence is $2^9 - 1 = 511$ bits. To generate this sequence, the outputs of registers 5 and 9 were connected to the two true inputs of the XOR gate. The inverted inputs were tied to the buffered V_{BB}.

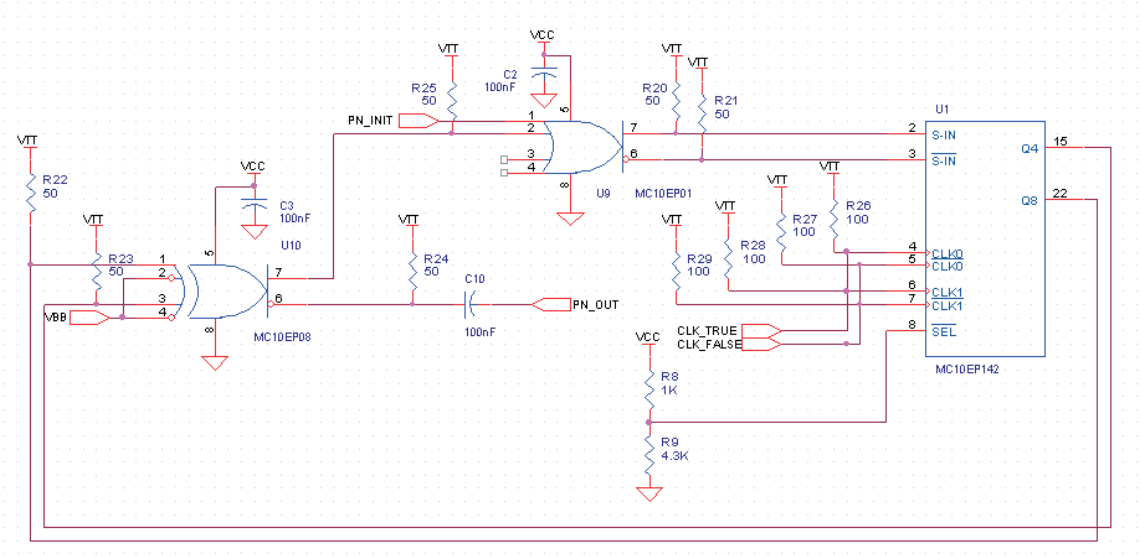


Figure 2.9 Schematic of LFSR.

The true output of the XOR's differential output was connected to one of the OR gate's input pins. Another one of the OR gate's input pins was connected to a switch that when pressed, provided V_{OH} at the pin via a voltage divider. When the switch was open the pin would be unconnected, and according to the specifications of the MC10EP01, all unused pins would default to VOL. The OR gate and switch act as an initialization circuit for the LFSR.

The differential output of the OR gate was connected to the differential S-IN input on the shift register, thereby completing the feedback loop. The differential output of the MC10EP16 was connected to both differential clocks on the shift register. This was necessary in order for the shift register to function properly. Finally, the SEL pin was pulled high via a voltage divider so as to set the shift register in "shift mode". Refer to the data sheets for additional information concerning each device.

2.4 Implementation

The circuit was designed, built, and tested on a protoboard before beginning a PCB layout of the circuitry. The protoboard implementation achieved a maximum clock frequency of 30 MHz. Figure 2.10 shows the protoboard implementation PN generator clocked at 1 MHz as well as the expected sinc-squared output.

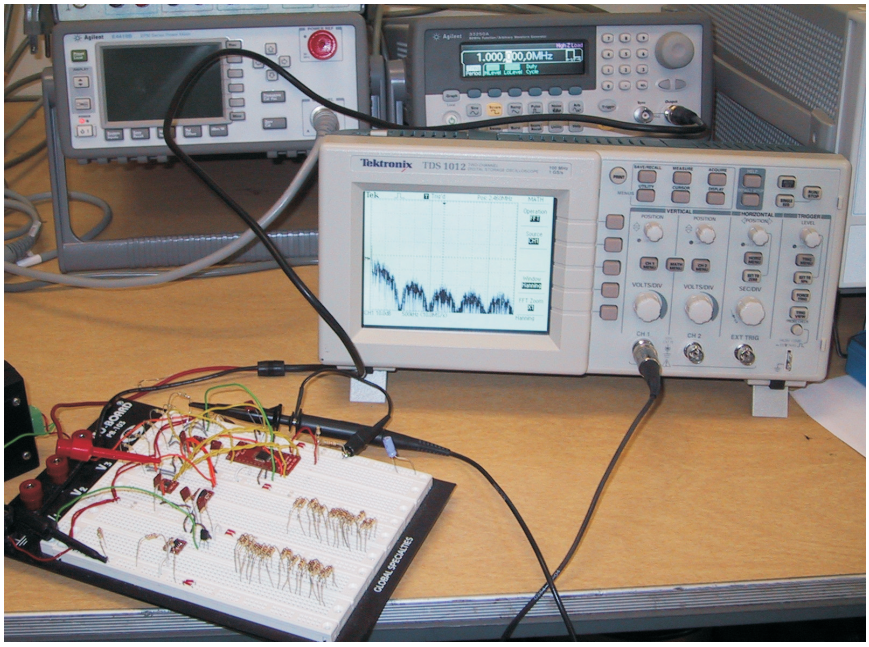


Figure 2.10 Photo of protoboard PN generator clocked at 1 MHz.

This satisfactory performance indicated the PN generator was ready to be implemented on a printed circuit board (PCB). Layout was performed in Cadence Layout Plus. The board's dimensions were 3 in. by 3 in. The layout is illustrated in Figure 2.11. Two such boards were manufactured. Figure 2.12 shows the fully assembled PN generator.

These boards served as prototypes for continued analysis of the system. They achieved a maximum clock frequency of 460 MHz, though at this frequency, the sinc-squared envelope was considerably degraded as compared to the envelope generated by a 300 MHz clock, as shown in Figure 2.13.

Figure 2.14 indicates that the PN generator is producing the correct PN sequence for 300 MHz and 460 MHz. Recall that there should be $L - 1 = (2^9 - 1) - 1 = 510$ peaks between envelope nulls. At 300 MHz, there is 600 kHz between peaks. (600 kHz)/(300 MHz) = 500 peaks. At 460 MHz, there is 900 kHz between peaks. (900 kHz/(460 MHz) = 511.1 peaks. Taking into account measurement error, this is a good indication that the PN sequence is correct.

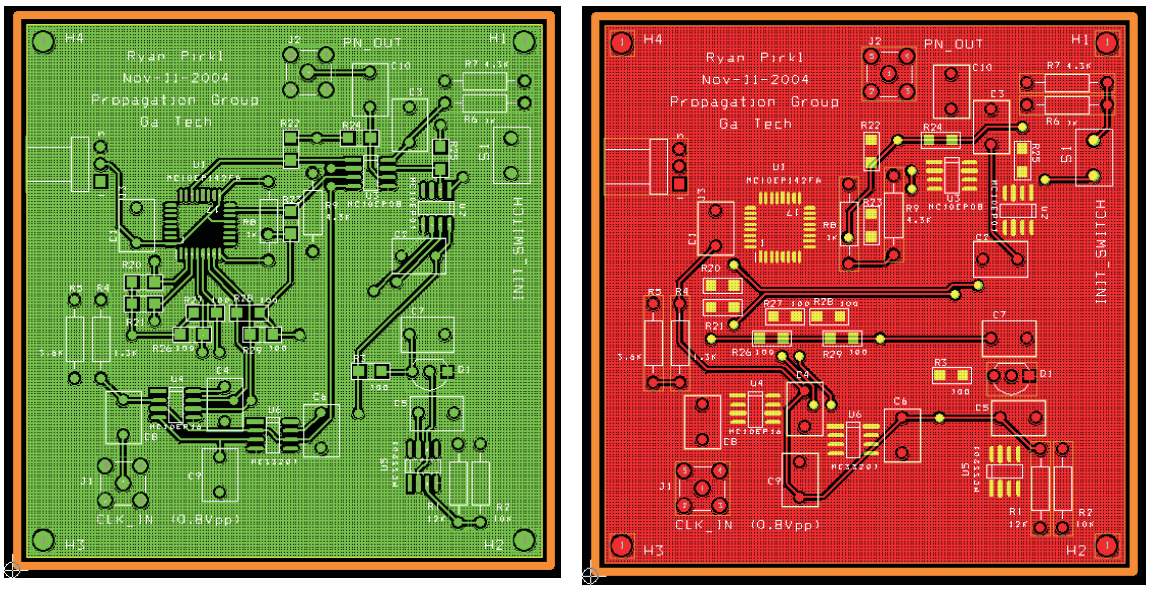


Figure 2.11 Board layout for top (left) and bottom (right) of the PN sequence generator.

2.5 Future Design Considerations

This first generation PCB was a single-layer board made of FR-4. A 50-ohm trace on single-layer FR-4 with thickness 0.062 in. must be 0.066 in. wide. The traces on this board were 0.012 in. wide, as such a wide trace was not practical. The traces had an impedance of 85-ohms, making impedance mismatches significant. In attempt to minimize the reflections, the traces were made as short as possible. The longest trace on the board had a length of roughly 2.2 in. Therefore, transmission line effects would become significant for a wavelength of 22 in. or 0.5588 meters. The traces had a velocity of propagation of 194.6×10^6 m/s. Thus, using the tenth of a wavelength rule of thumb for transmission lines, at any frequency beyond 350 MHz, impedance mismatches would begin to affect the performance of the PN generator.

The next generation of the PN generator must have 50Ω traces to push the maximum clock frequency up to one Gigahertz. Additionally, the next generation board will use two 9-bit shift registers to generate a PN sequence of length $2^{18} - 1 = 292,143$ bits. This longer sequence will drastically improve the dynamic range of the channel sounder.

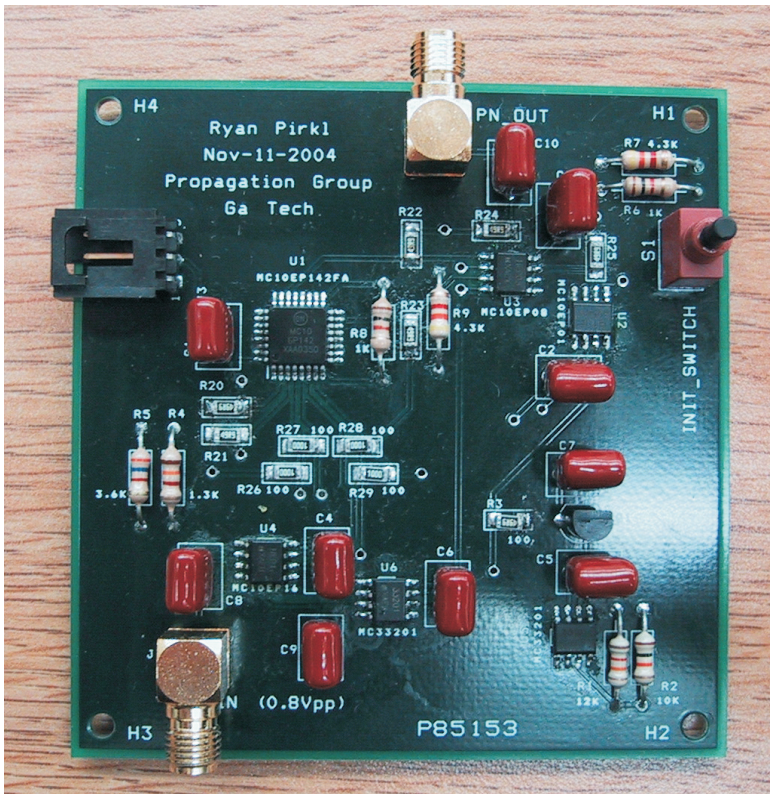


Figure 2.12 Photograph of the completed PN sequence generator.

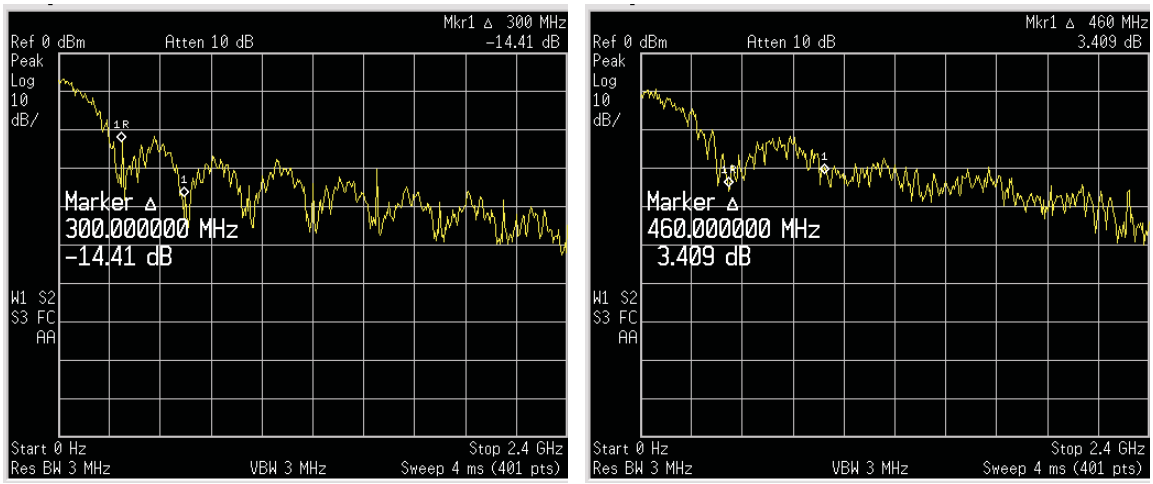


Figure 2.13 Spectrum for PN sequence clocked at 300 MHz (left) and 460 MHz (right).

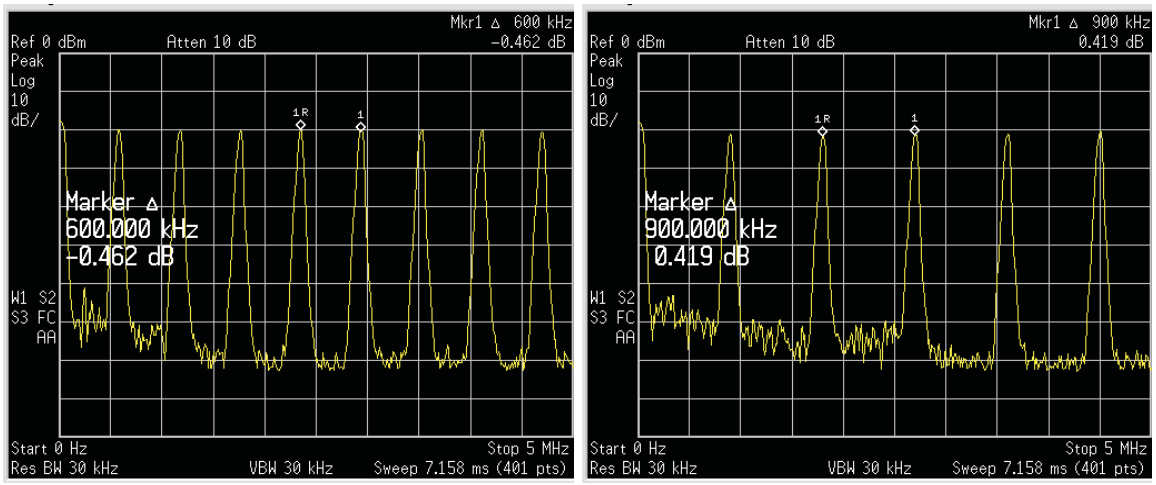


Figure 2.14 Spectral lines due to repetitive sequence for PN sequence clocked at 300 MHz (left) and 460 MHz (right).

2.A Full Schematic of PN Generator

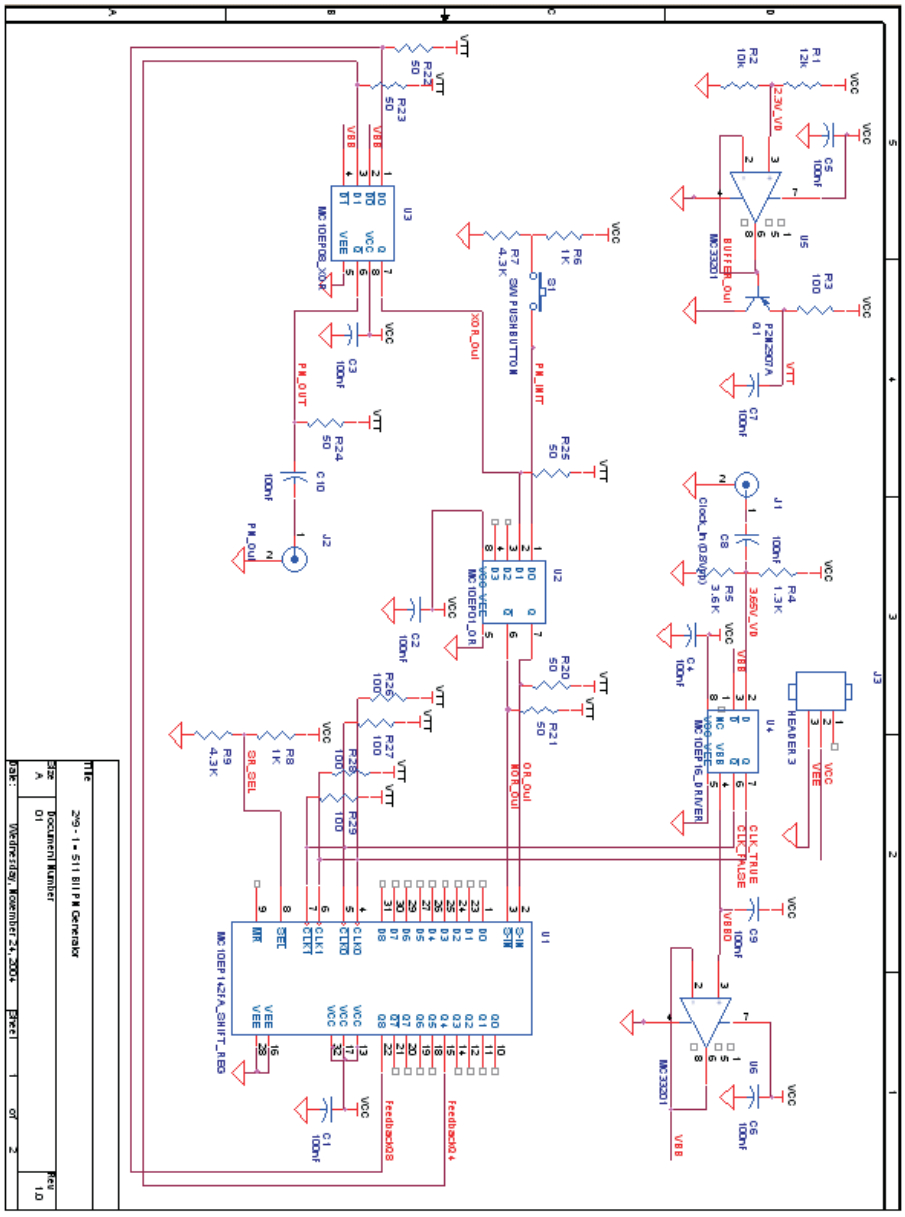


Figure 2.15 Full schematic for the PN sequence generator.

Chapter 3

VECTOR RF SIGNAL GENERATOR

3.1 Introduction

Accurate measurements of terrestrial RF channels are an important part of evaluating RF systems. Theoretical results are difficult to use directly in practical applications, and detailed measurements of realistic working conditions can assist in the design of robust systems.

Taking measurements from a mobile platform can be laborious because of the size and weight of the materials involved. Even simple measurements require multiple clock sources and RF sources, each of which requires a large, expensive signal generator which was most likely designed for use in a lab, so is neither portable nor rugged. The copious features of a lab signal generator are also unneeded for mobile measurements; normally a few distinct frequencies are all that is required, and these frequencies will not change over the course of a day of measurements.

It would be possible to use small oscillator modules at specific frequencies, but these have the drawback of being totally unchangeable and still somewhat bulky, as well as requiring additional cabling, mounting, and power supplies. The quality factor of such oscillators may also be insufficient.

Since signal generation is a basic requirement of taking RF measurements, it is beneficial to have a compact, portable, high-quality, variable multiple-output signal generator, to bridge the gap between the inflexibility of static oscillators and the unneeded complexity of bench signal generators. This chapter presents the design of a *vector signal generator*, a single programmable device capable of generating multiple high-quality clock, baseband, and RF sources simultaneously.

3.2 Design

Figure 3.1 shows a block diagram of the basic system layout. An external controller interfaces to a serial peripheral interface (SPI) controlling several phase-locked loop (PLL) signal generator channels. The output of the PLL passes through a gain stage and finally a variable attenuator. A high quality temperature-controlled crystal oscillator (TXCO) 10 MHz reference is used to drive the PLL chips. The output signal of each channel is provided by a standard voltage controlled oscillator

(VCO). A more detailed circuit schematic is included as an appendix to this chapter.

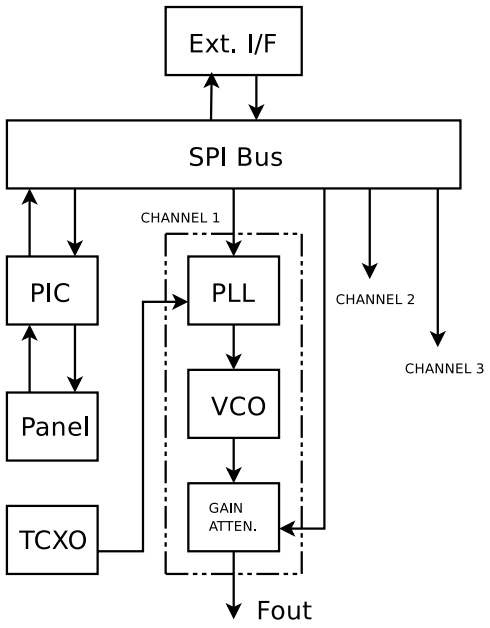


Figure 3.1 Block diagram of system.

Figure 3.2 shows a photograph of the final board design before it was populated with electronic components. Each white rectangle on the board marks a single bank of programmable output frequency. This board, along with a DC power supply, are the only components in the vector signal generator's enclosure, making the device small, light-weight, and portable.

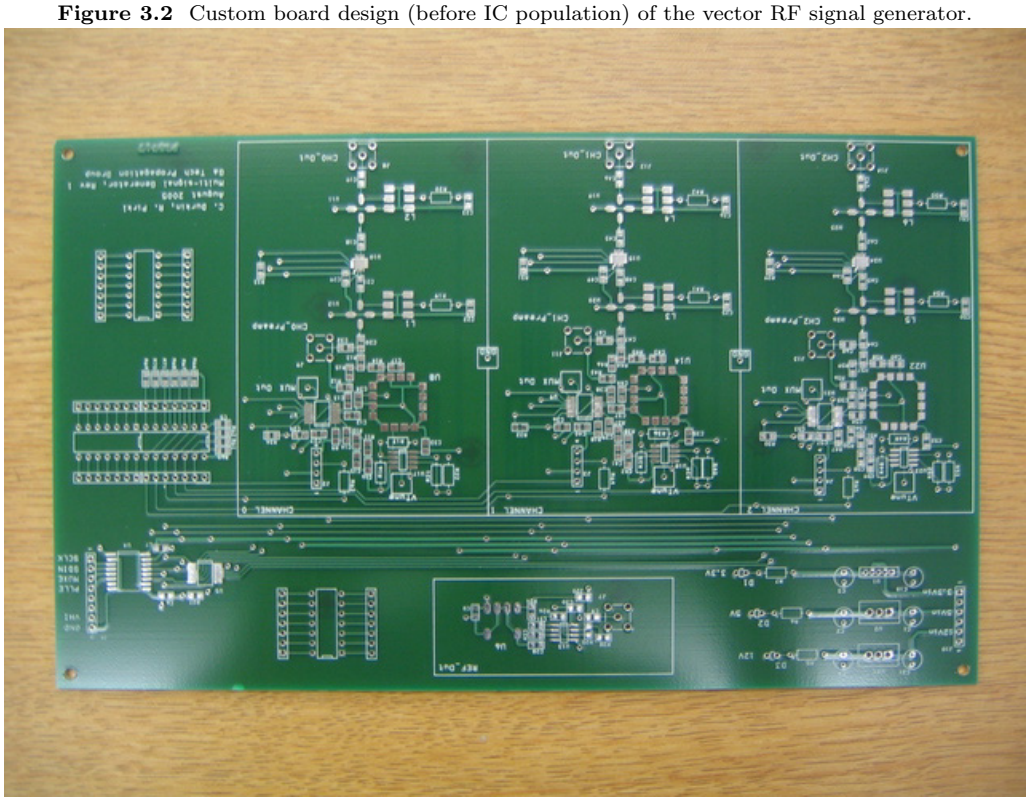
3.2.1 Control

Each PLL and attenuator is serially programmable using a standard SPI interface. They can be controlled from an external computer or internally from a PIC micro-controller. The PIC also controls the front panel LEDs and buttons.

The SPI interface consists of a clock bus and a data bus that all devices share, and a latch enable line for each device. Each device has a shift register that records data seen on the bus. Pulsing the latch enable line for a device instructs it to use clocked in data to program its internal registers.

The programming interface is simply the SPI clock and data lines, one latch enable for the input multiplexer, and the latch enable that is multiplexed for all other devices. This allows up to eight devices to be controlled with only four lines. The current implementation uses six devices: three PLLs and three attenuators. More than eight devices would require an additional multiplexer, but no additional control lines.

Figure 3.2 Custom board design (before IC population) of the vector RF signal generator.



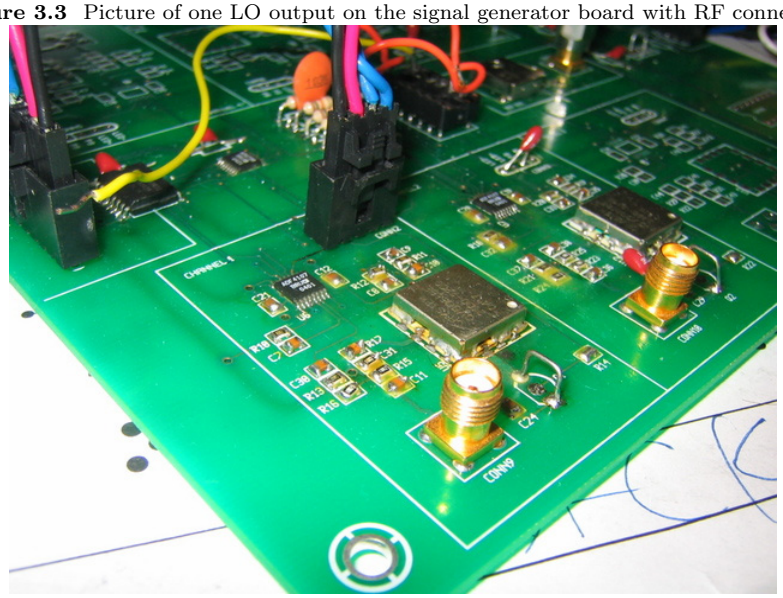
The PIC micro-controller can be used to program the SPI devices in the absence of an external computer. The various devices do not retain programmed values after power down, so the PIC can automatically program each PLL on power up. The particular frequencies programmed by the PIC are hard coded into the firmware, and can be changed by reprogramming the PIC. This operation is relatively simple, and different frequency setups could be kept on several PICs, and the PICs could be swapped in and out as needed.

3.2.2 Channels

Each channel consists of a phase-locked loop (PLL) circuit, a gain stage, and a variable attenuator. The counters and dividers in the PLL chip (the Analog Devices ADF4107) are serially programmed to produce the desired output frequency. The frequency range of each channel is determined by the range of the VCO in the channel. A typical VCO has a range of tens to hundreds of MHz around its center frequency. The channel spacing is set by the frequency of the reference, though there is a reference divider on-board the PLL chip, allowing very small channel spacing (10s of kHz). A photograph of one channel's electronic components on the printed circuit board is shown

in Figure 3.3.

Figure 3.3 Picture of one LO output on the signal generator board with RF connector.



3.2.3 Reference

The quality of the output signal is determined by several factors; most important is the reference frequency used by each PLL. Any instability, noise, or spurs present in the reference will appear in the output of the PLL. Thus, a highly stable, low noise, temperature-compensated oscillator is necessary for the reference. Only one reference is required for an arbitrary number of channels.

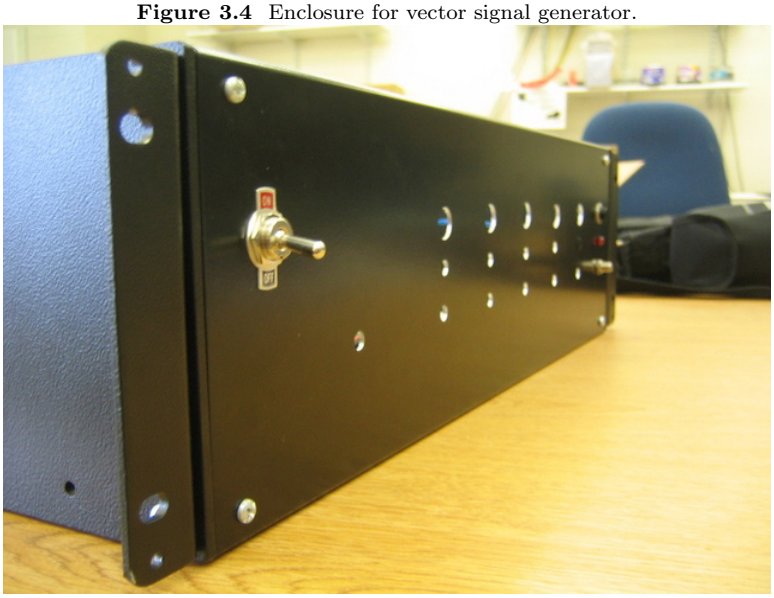
The VCO outputs on first revision of the board contained notable spurs as a result of insufficient decoupling of the VCO power supply from the reference frequency. These manifested as 10 MHz AM spurs about 30 dB down from the main signal. Additional decoupling of the VCO power supply and different routing of the reference frequency signal traces alleviated this problem in the second revision.

3.2.4 Enclosure

The device is contained within a small rack mount enclosure, providing LED indicators and toggle buttons for each channel on the front panel. A photograph of this enclosure is shown in Figure 3.4. The serial interface is accessible through a DIN connector on the back. A standard ATX power supply is used to power the device. External serial interface software was written for the Microsoft Windows platform using the parallel port, though the interface is very simple and could easily be implemented on other systems. The programming inputs are optically isolated so voltage levels on

the external programmer are not critical. Programming the PLLs can also be accomplished by the internal PIC with appropriate firmware (see section 3.2.1).

Figure 3.4 Enclosure for vector signal generator.



3.3 Future work

PLL circuits also have the added benefit of allowing additional signals to be modulated onto the carrier frequency without additional mixing hardware. In the channel sounding application, this could permit PN sequencers to be part of the signal generation itself, allowing a totally self-contained transmitter. The power requirements and size of the entire PLL circuit would not appreciably increase the size or complexity of the current PN module design.

There is also potential to bring a small embedded computer inside the enclosure which could then be remotely controlled through wired or wireless Ethernet. This may be useful for conducting tests with multiple transmitters in different locations.

3.A Vector RF Signal Generator Schematic

This section contains detailed schematics for the custom Vector RF Signal Generator developed under this project.

Figure 3.5 Full Schematic of Vector RF Signal Generator (power supply).

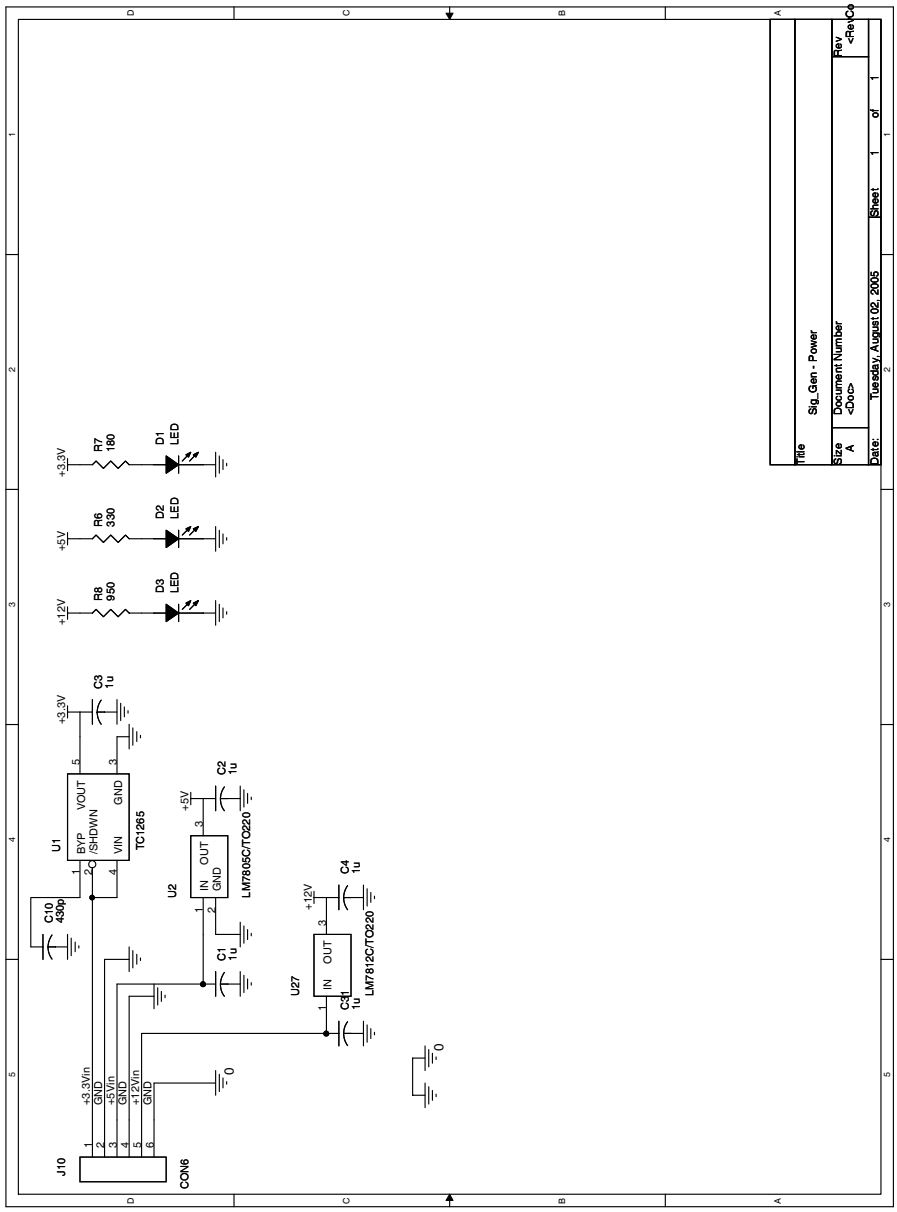


Figure 3.6 Full Schematic of Vector RF Signal Generator (controller).

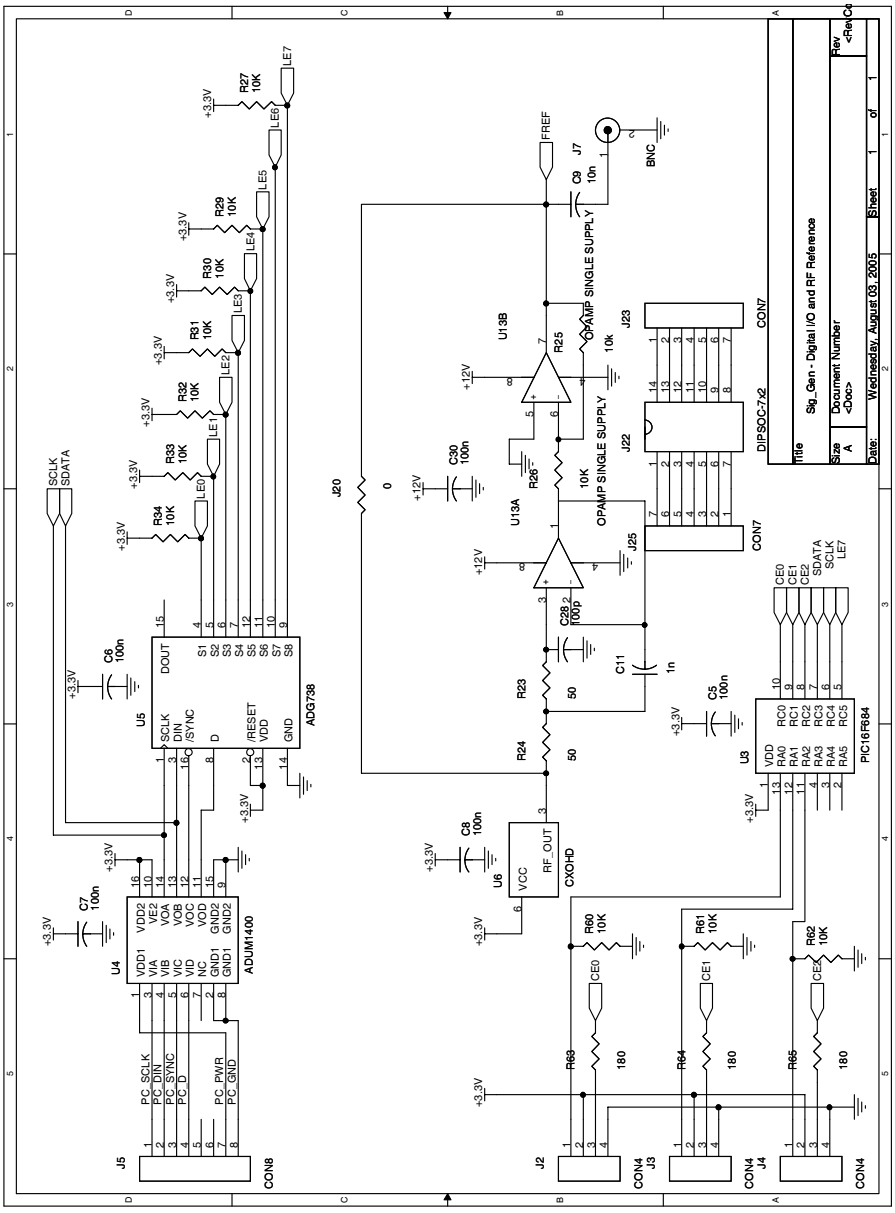


Figure 3.7 Full Schematic of Vector RF Signal Generator (channel 1).

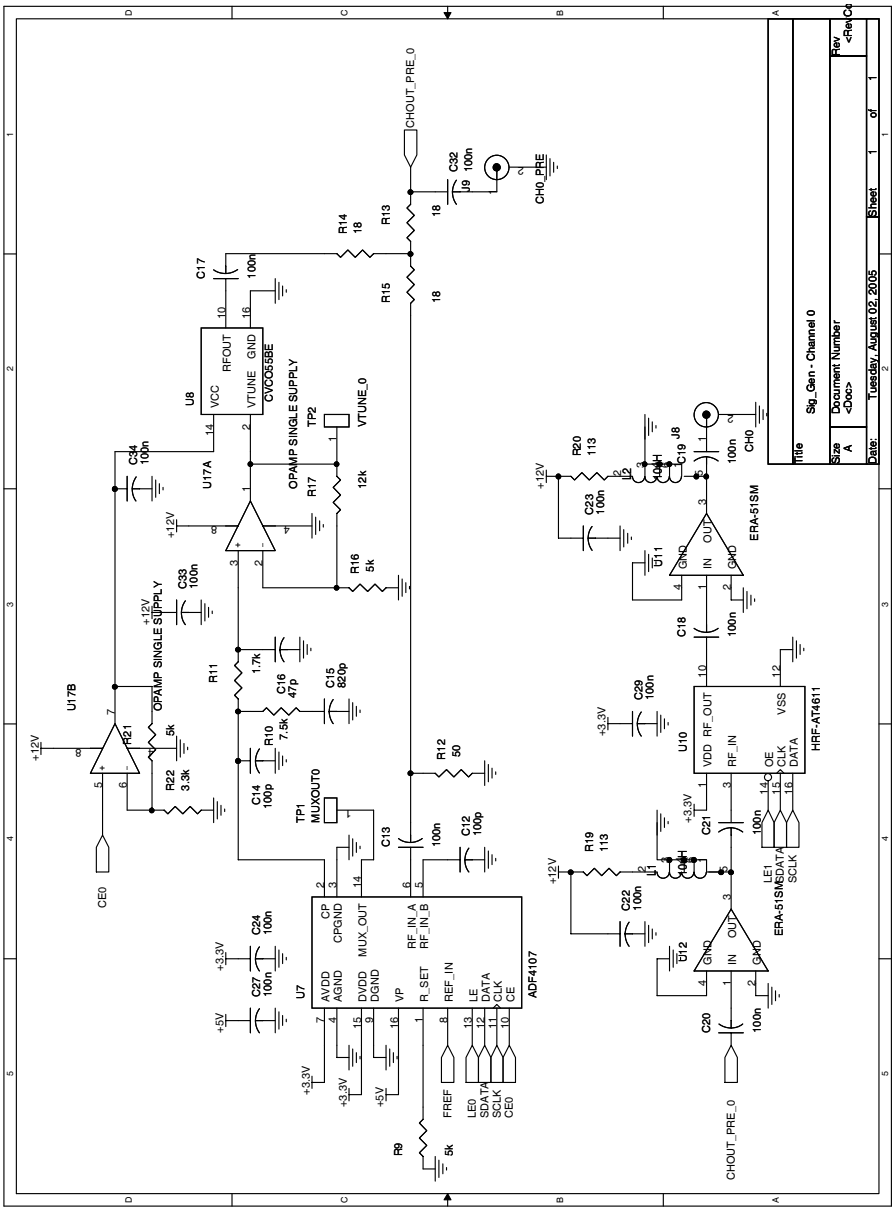


Figure 3.8 Full Schematic of Vector RF Signal Generator (channel 2).

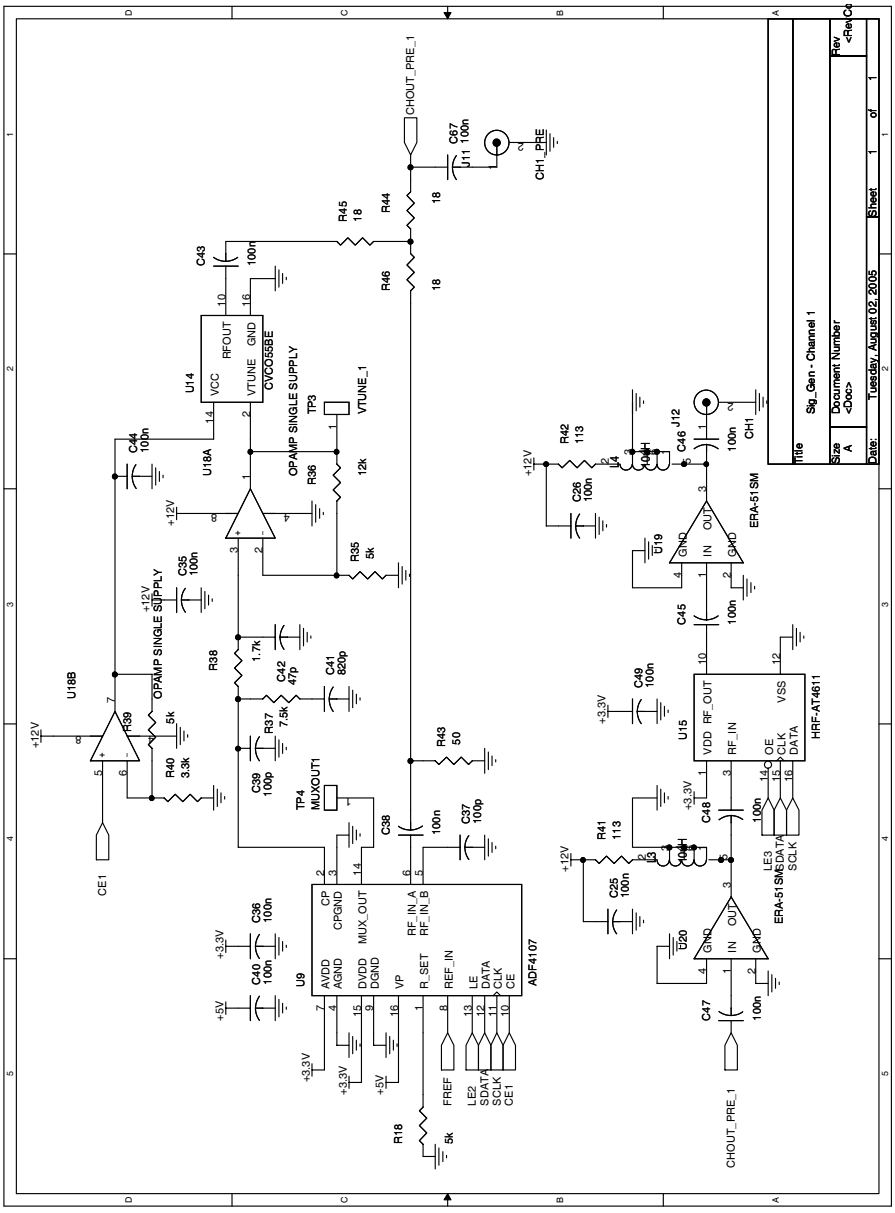
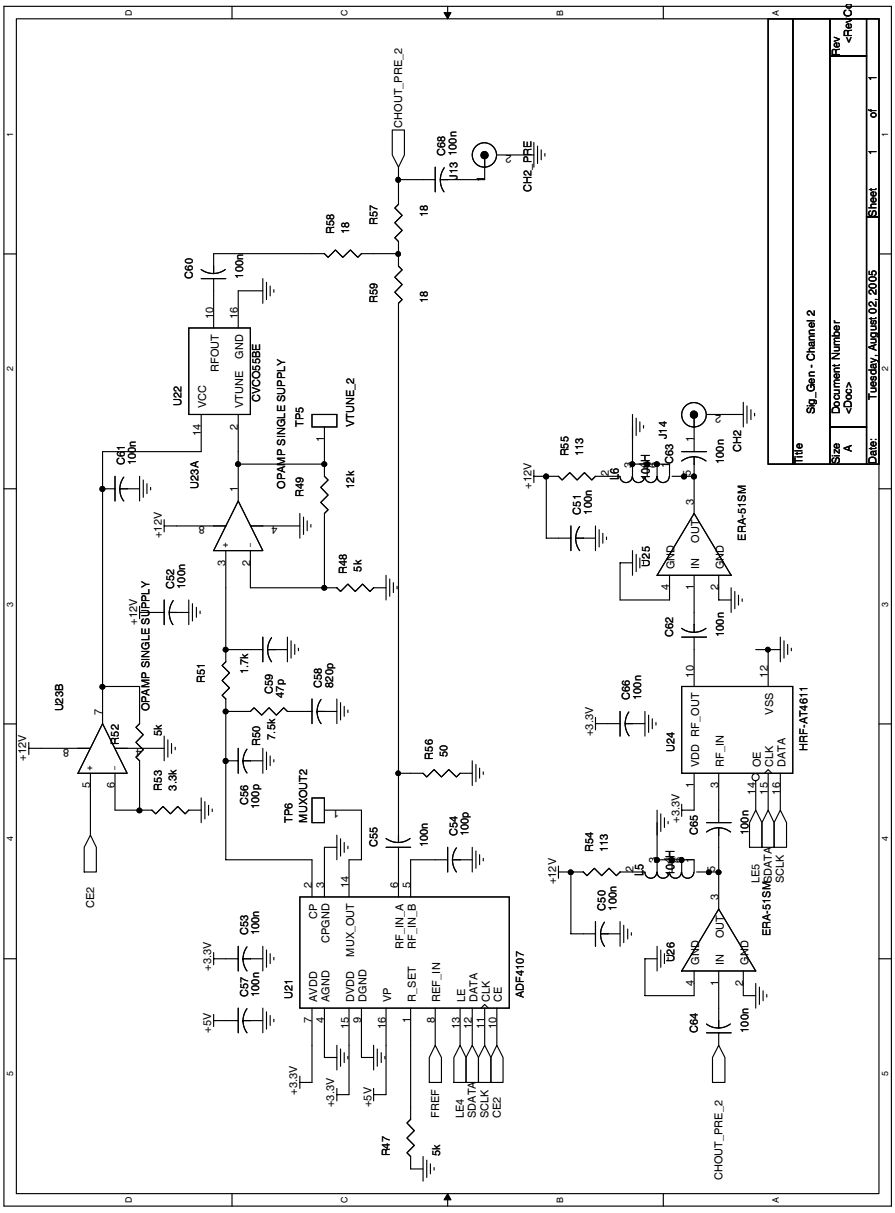


Figure 3.9 Full Schematic of Vector RF Signal Generator (channel 3).



Chapter 4

EXAMPLE OPERATION

This chapter presents a sample indoor 2.45 GHz measurement made with the new channel sounder system. The new hardware was used as well as custom software for acquiring and interpreting the spatio-temporal waveforms.

4.1 Equipment and Set-Up

For this test, a transmitter was assembled according to the block diagram in Figure 1.2. The PN sequence generator was clocked at 50 Mchips/sec and mixed with a 2.45 GHz continuous wave carrier generated by an RF signal generator. This signal was fed into a high-gain, broadband amplifier. The output of the amplifier was then sent into a custom-built quarter-wave monopole transmit antenna with a circular ground plane. This antenna transmits with an omnidirectional pattern in azimuth, uniformly illuminating the immediate indoor environment. A photograph of the monopole is shown in Figure 4.1, while Figure 4.2 shows the custom-built devices and off-the-shelf RF components used at the transmitter.

The transmitter was operated with 30 dBm of transmit power sent into the base of the antenna. The transmitter was placed in a room on the 5th floor of the Van Leer building on the Georgia Tech campus. The receiver and 8-element antenna array were placed in a different room on the same floor, approximately 25m away from the transmitter. Thus, the link was heavily obstructed.

4.2 Data Acquisition

Figure 4.3 show the resulting screen captures taken from the receiver for this link configuration. Each plot in the vertical direction corresponds to a data collection made on an antenna element in the array. All 8 data points were taken simultaneously. On the left-hand side are the time-domain correlations for each channel. The spikes are estimates of the power delay profiles seen by each of the antenna elements. Only a little dispersion – about two 20-ns bin's worth of signal – was observed on average for each channel. This result is consistent with the typically low RMS delay spreads of indoor channels [Dev87], [Dur03b]. Because signals extinguish quickly in an office building, the

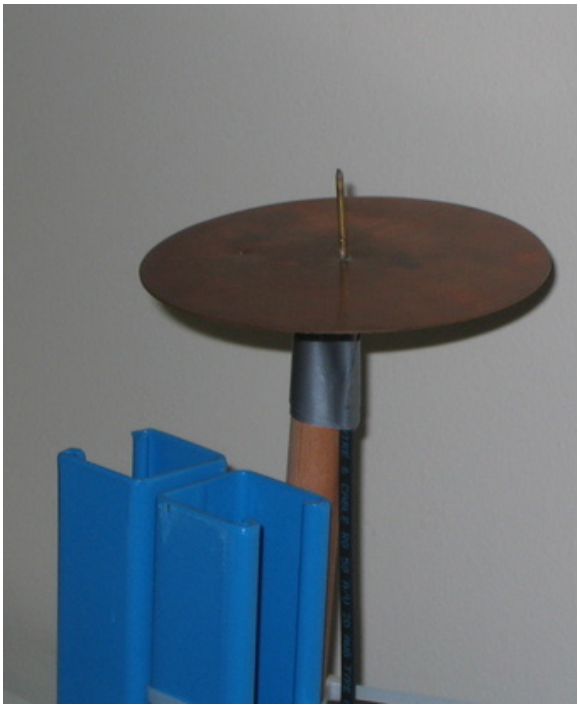


Figure 4.1 Picture of transmitter antenna, a custom-built 2.45 GHz quarter-wavelength monopole with circular ground plane.

RMS delay spread is usually between 30-50ns with spreads in excess of 100ns virtually unknown.

The right-hand side of Figure 4.3 shows the Fourier transform of each antenna element's measured power delay profile. Note that each channel exhibits frequency-selective fading – evidence of multipath in the power-delay profile. Furthermore, this frequency-selectivity is not the same for all channels, indicating that there is spatial multipath fading as well as delay and dispersion. This result provides validation of the new channel sounding system as well as compelling motivation to take measurements and reveal the interesting characteristics of the spatio-temporal channel.

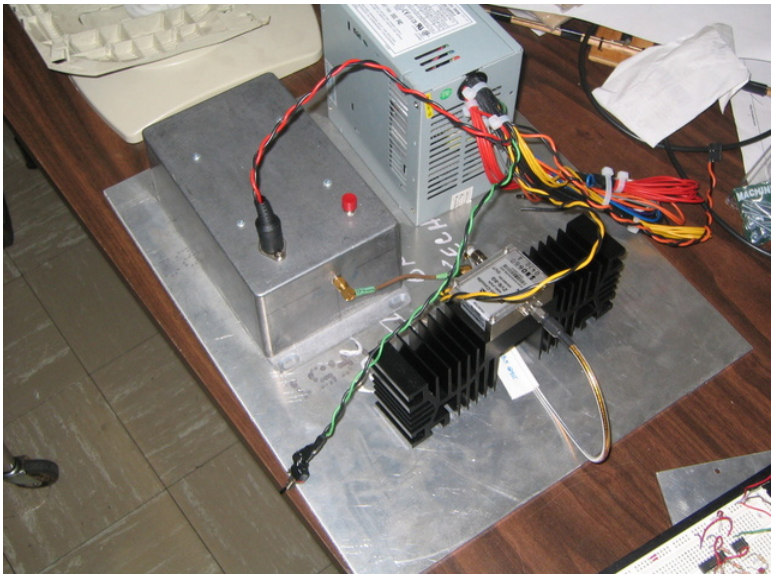
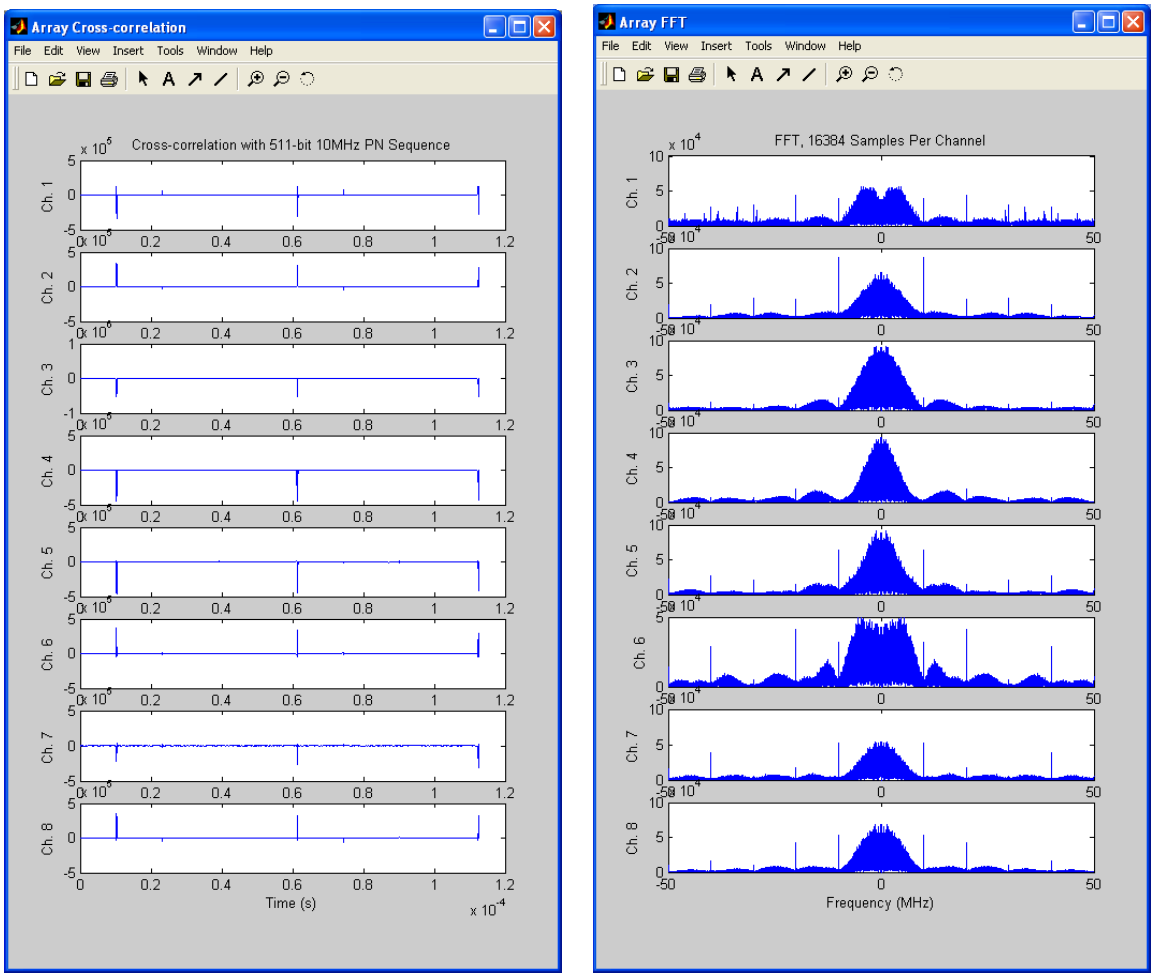


Figure 4.2 Transmitter setup for a 2.45 GHz modulated pseudo-noise generator with power RF amplifier. Setup consists of a PN generator (top left), a power supply (top right), and a broadband amplifier with mixer (bottom) mounted on a ground plane.

Figure 4.3 Screen captures of data taken from 8 channels simultaneously. Left side shows cross-correlation of the channel with the PN sequence. Right side shows the spectrum of the received signal.



Appendix A

ECL DESIGN GUIDE

A.1 Introduction

This section is included to illuminate some of the circuit design issues facing high-frequency PN generators.

A.1.1 Overview

Emitter-Coupled Logic (ECL) ICs are ideal for operating in the gigahertz range due to their picosecond propagation delays. Additionally, thanks to their use of differential inputs, they are able to drive long transmission lines in relatively noisy environments while maintaining signal integrity. However, ECL devices impose special design considerations. First, due to their high speed operation at up to several Gigahertzes, designers must take into account transmission line effects which can severely disrupt propagating signals. Secondly, ECL chips are designed to be used with negative supplies. While it is possible to use them with positive supplies, designers must be extra careful of coupling noise onto V_{CC}.

A.1.2 Power Supplies

ECL outputs are referenced to the most positive supply rail [Sem99]. This means that any noise appearing on the most positive supply rail will be directly coupled onto the output signal. For example, if the power supply is 5V and GND, then all outputs would be referenced to 5V, and any noise on the 5V supply would also be seen at the ECL outputs. Therefore, the older literature calls for ECL chips to be powered by a negative power supply, such as -5V and GND. By using GND as the most positive supply rail, it is easier to maintain cleaner signals at the ECL outputs. GND is generally found to be less noisy as compared to a non-GND potential. This does not mean it is impossible to use a positive power supply. It does mean that precautions must be taken to ensure very little noise is coupled onto the most positive supply rail in order to maintain clean outputs.

As a note, when designing with ECL and positive supplies, it is called positive ECL (PECL)[Sem99]. Likewise designing with negative supplies is called Motorola ECL (MECL) design, or more commonly

and intuitively, negative ECL (NECL). The 'P', 'M', or 'N' prefix merely describes the power supply configuration. It has no effect on the devices themselves. An ECL device is a PECL device is a NECL device.

A.1.3 Input/Output Configurations

ECL uses two input/output (I/O) configurations: single-ended and differential. Single-ended I/O is generally easier to implement, but differential I/O exhibits greater immunity to noise. It is important to note that for both single-ended and differential devices, $V_{IH/OH}$ and a $V_{IL/OL}$ do not correspond to the upper and lower supply rails, though as aforementioned, they are coupled to the upper rail. Table A.1 shows how V_{OH} and V_{OL} are generated relative to V_{CC}. Additionally, Table A.2 shows $V_{IH/OH}$ and a $V_{IL/OL}$ given a 10E type ECL device using a PECL setup (V_{CC} = 5.0V, V_{EE} = GND) operating at 25° C. Note V_{BB}, which is the bias voltage of a differential input. This is used for connecting single-ended outputs to differential inputs, and will be explained further in a later section. Also note that voltage swing for an ECL output is 800mV, and this voltage swing is roughly centered on V_{BB}.

Single-ended I/O is similar in function to the I/O used in CMOS and TTL. To determine if the signal is a '1' or '0', the input voltage is compared to a threshold voltage. If the input voltage is greater than the threshold, it is declared a '1'; if the input voltage is less than the threshold, it is declared a '0'. For ECL, this threshold voltage is V_{BB}.

Table A.1 ECL I/O Ranges (in Volts) Relative to V_{CC} [Sem99].

Symbol	V_{0H}	V_{OL}	V_{IH}	V_{IL}	V_{BB}
Max	V_{CC} - 0.81	V_{CC} - 1.63	V_{CC} - 0.81	V_{CC} - 1.48	V_{CC} - 1.25
Min	V_{CC} - 0.98	V_{CC} - 1.95	V_{CC} - 1.13	V_{CC} - 1.95	V_{CC} - 1.35

Table A.2 PECL I/O Ranges (in Volts) Relative to V_{CC}=5V [Sem99].

Symbol	V_{0H}	V_{OL}	V_{IH}	V_{IL}	V_{BB}
Max	4.19	3.37	4.19	3.52	3.75
Min	4.02	3.05	3.87	3.05	3.65

The differential I/O significantly reduces noise at the input through common-mode rejection. Each differential input takes in two signals, and likewise each differential output emits two signals. The two signals together are known as a differential pair. One of the signals is referred to as the "true" signal, and the other is the "inverted" signal. The difference of these signals ("true" minus

"inverted") distinguishes a binary '1' from '0':

$$\begin{aligned} 1: &\quad V_{\text{Diff, True}} - V_{\text{Diff, Inverted}} > 0 \\ 0: &\quad V_{\text{Diff, True}} - V_{\text{Diff, Inverted}} < 0 \end{aligned}$$

When connecting a differential output to a differential input, the wires or traces connecting the differential pair should be run adjacent to each other. Ideally, this will cause any noise coupled onto one of the signals to be coupled onto the other. When the differential input "subtracts" the inverted signal voltage from the true signal voltage, the noise will be removed. That is, any signal common to the differential pair (in this case noise) will be rejected.

A.2 Circuit Design Issues

A.2.1 Termination of ECL Devices

ECL outputs are bipolar junction transistors (BJT) configured as emitter followers. To maintain their fast switching rates, these emitter followers should operate in the forward active region at all times, requiring them to source current at all times. ECL inputs have large impedance (typically around 75 kΩ) that does not allow for the necessary current sourcing by the ECL output [Sem02a], [Sem02b]. Instead, this current sourcing is achieved by terminating the ECL output through a resistor, Rt, to a voltage, V_{TT}, such that

$$V_{TT} = V_{CC} - 2.0\text{V} \qquad R_t = Z_0$$

where Z_0 is the characteristic impedance of the transmission line connecting the ECL output to R_t. ECL outputs are typically 50Ω, thus the terminating resistor as well as the transmission line's characteristic should be approximately 50Ω.

There are two preferred termination schemes for ECL devices. One scheme, called *parallel termination*, terminates any signal carrying line via a resistor, R_T, to a supply operating at V_{TT}. The other, called "Thevenin parallel termination", involves a Thevenin equivalent circuit that creates a termination voltage and resistance equivalent to V_{TT} and R_T.

Thevenin Parallel termination, while avoiding the need for a secondary supply, consumes additional power as compared to parallel termination. Conversely, parallel termination consumes less power, but requires a supply operating at V_{TT}. An additional point to note is that for the Thevenin parallel termination, any noise on V_{CC} is partially coupled onto V_{TT}.

The most important factor when using ECL devices is to be sure that their output emitter follower always operates in the forward active region. Fluctuations in the supply voltages V_{CC} and V_{TT} may cause V_{OL} to be less than or equal to V_{TT}, which would make $I_{OL} = 0$ mA and place the emitter follower in cutoff. This would increase the propagation delay of the device due to the time

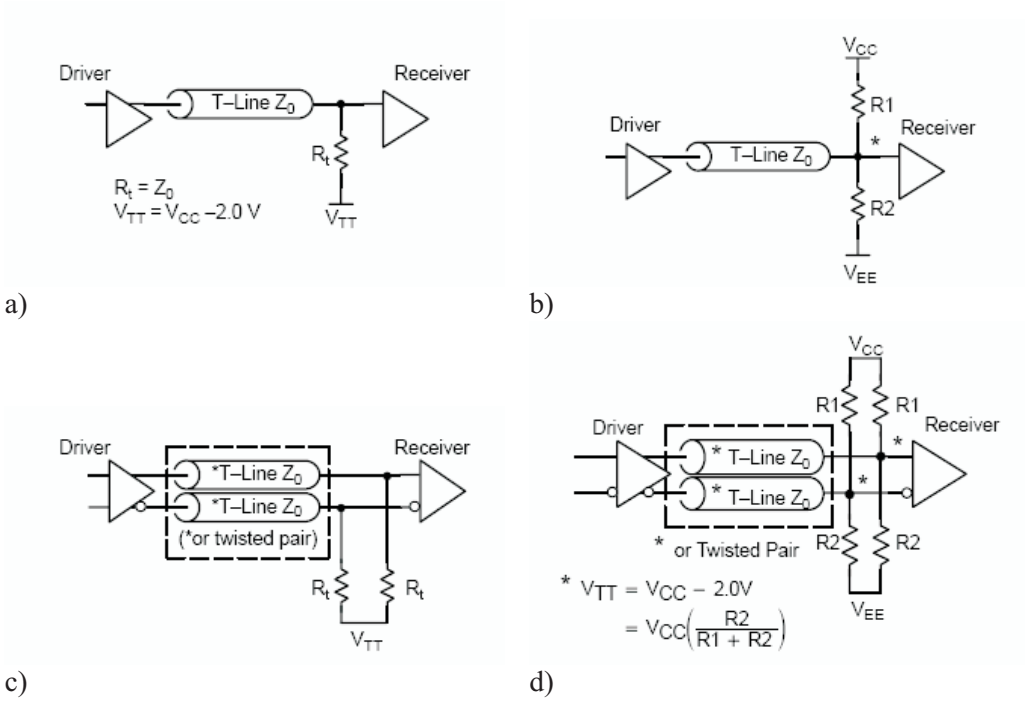


Figure A.1 Termination schemes for I/O interfaces: a) single-ended parallel, b) single-ended Thevenin parallel, c) differential parallel, d) differential Thevenin parallel.

required to pull the emitter follower out of the cutoff state. Therefore, it is necessary to ensure VOL always remains greater than V_{TT}.

The partial coupling of V_{CC} onto V_{TT} for the Thevenin parallel termination helps to keep $V_{OL} > V_{TT}$. This combined with the single supply design make it the preferred termination scheme for ECL devices, even though it imposes greater power requirements [Sem02b].

As a final note on terminations, placement of the termination circuit is important. When connecting an output on device A to an input on device B, the termination circuit should be implemented as close as possible to the input on device B. Differential and Single-Ended ECL I/O and Interfacing Both differential and single-ended I/O are popular interfacing schemes, resulting in four possible configurations.

Differential Output to Differential Input For interfacing a differential output to a differential input, connect the true and inverted outputs directly to the corresponding true and inverted inputs. Then, apply the preferred termination scheme.

Single-ended Output to Single-ended Input Single-ended I/O is just as straightforward: connect the signal output to the signal input and apply the preferred termination scheme.

A.2.2 Differential Output to Single-ended Input

For interfacing a differential output to a single-ended input, connect the true output to the single-ended input and apply the preferred termination [IC00]. The inverted output should also be terminated in a manner similar to the true output, even though it is not connected to another device.

Single-ended Output to Differential Input For interfacing a singled-ended output to a differential input, the general design rule becomes more complicated depending on the devices used. Recall that the binary value of a differential input is determined by the difference of the true and inverted input voltages. The signal output should be connected to the true input of the differential device. To make the differential device function correctly, the inverted input should be connected to a threshold voltage equivalent to $(V_{IH} + V_{IL})/2$. A quick comparison of V_{BB} to V_{IH} and V_{IL} in Table 1 and 2 shows that V_{BB} is not exactly midpoint voltage. However, V_{BB} is still used for as a threshold voltage.

If a V_{BB} pin is available on a device (i.e., MC10EP16) than it may be connected directly to the inverted pin of the ECL differential input on that device. V_{BB} is not a typical ECL output but rather a current source/sink. Therefore, it is not necessary to terminate V_{BB} to V_{TT} via some termination scheme. However, V_{BB} should be decoupled from V_{CC} via a small capacitance. A typical value is 0.01 μF.

Not all differential input devices may have V_{BB} available on chip, and unfortunately, when unconnected, the inverted input pin generally defaults to $V_{CC}/2$ rather than V_{BB}. For devices without V_{BB}, it is necessary to generate the bias voltage externally and connect it to the inverted input. This can be done via a voltage divider network or a "16" type buffer device. It may be necessary to buffer V_{BB} via an op-amp configured as a voltage follower to allow sufficient current sourcing/sinking. Further details on connecting single-ended and differential devices can be found in ON Semiconductor's application note "AND8020/D: Termination of ECL Logic Devices" [Sem02b] as well as Maxim's application note "HFAN-1.0.1: Interfacing Single-Ended PECL to Differential PECL and Differential PECL to Single-Ended PECL" [IC00].

A.2.3 Interfacing to 50Ω Test Equipment

Many instruments feature high-impedance inputs, which allow the direct connection of a terminated ECL output. However, this is not ideal for monitoring an ECL output, especially when the distance between the ECL termination and the test equipment becomes substantial. Instruments with a 50Ω load are also not ideal for directly connecting ECL outputs, because they terminate through 50Ω to GND rather than V_{TT}.

One method of interfacing with a 50Ω load is shown in Figure A.3 [Pul]. Resistor RS provides the constant DC current sourcing while the 50Ω load in parallel with R_S provides the sink/source for the AC currents. Capacitor C should be large to provide an AC short from the ECL output to

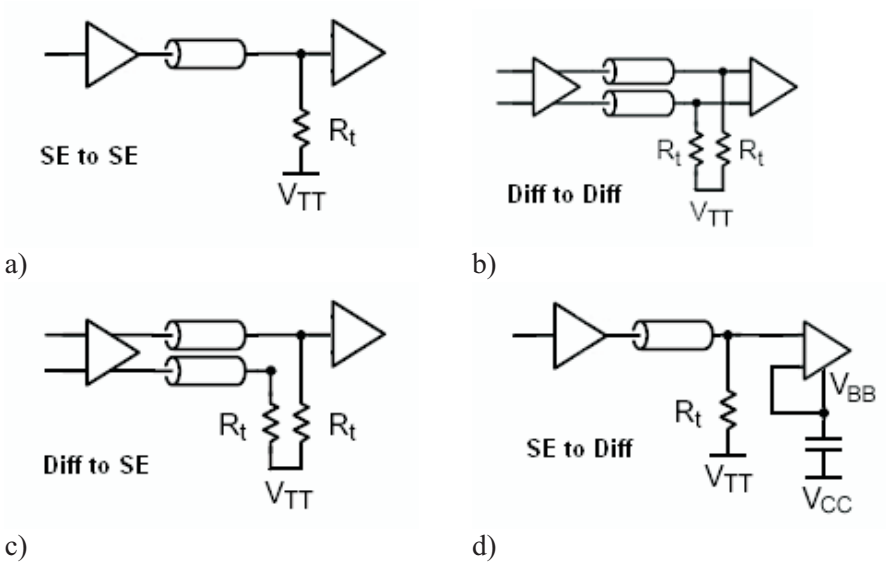


Figure A.2 Interfacing various I/O (using parallel termination): a) single-ended output to single-ended input, b) differential output to differential input, c) differential output to single-ended input, d) single-ended output to differential input [Sem02b].

the test equipment, but the precise value is dependent on the circuit's clock frequency. For a 5V PECL system, an R_S of approximately 274Ω will cause the ECL output to source 22.76mA for V_{OH} and 3.8mA for V_{OL}. This corresponds well with the typical sourcing of 21.1mA and 5.1mA for V_{OH} and V_{OL} respectively when the ECL output is terminated through 50Ω to V_{TT}.

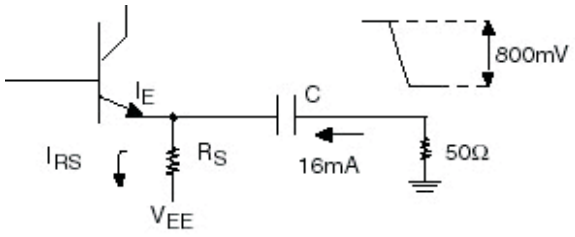


Figure A.3 ECL output connected to a 50Ω coupled load.

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