SIMULATION, FABRICATION AND CHARACTERIZATION OF PIEZORESISTIVE BIO-/CHEMICAL SENSING MICROCANTILEVERS

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By

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SIMULATION, FABRICATION AND CHARACTERIZATION OF

PIEZORESISTIVE BIO-/CHEMICAL SENSING MICROCANTILEVERS

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SUMMARY

Piezoresistive microcantilevers can be used for the detection of biological and chemical substances by measuring the change in surface stress. Design parameters for the cantilever and piezoresistor dimensions are investigated analytically and through finite element modelling. Based on these results, six optimized cantilever types are designed and fabricated with microfabrication methods. The electrical and mechanical properties of these devices as well as their deflection and surface stress sensitivities are characterized and compared to the models. A second generation of cantilevers that incorporates heater areas to trigger or enhance chemical reactions is designed and fabricated. In addition to the measurements done for the first generation devices, the thermal properties for both steady-state and transient operation of these microcantilevers are characterized.

CHAPTER 1

INTRODUCTION

The rapidly advancing field of Micro-Electro-Mechanical-Systems (MEMS) has enabled possibilities for sensing and actuation on the micrometer and nanometer scale. An important cornerstone of this development was the invention of the atomic force microscope in 1986 [1] , which made the development and usage of microcantilevers a fruitful research area. Today, this type of device is used not only for scanning topographies, its original purpose, but also for modifying surfaces and increasingly for the detection of chemical and biological substances in gases and liquids. The latter application shows great promise for extremely sensitive and selective sensors that can be used in both defense-related and civil applications.

1.1 Cantilever Sensors for Chemical and Biological Applications

Chemical microsensors usually consist of a chemically selective element that experiences a change in one or more of its physical properties upon chemical stimuli, and a transducer element to convert this property change into a measurable output signal. In the case of microcantilevers for chemical detection the former element is often a polymer layer that experiences an expansion and/or a change in mass when exposed to the analyte [2]. The transducer element is the cantilever itself which converts this change into a measurable physical quantity. In the case of a polymer expansion, the quantities of the system that change are its spring constant and the deflection of the free end. Biological

sensing can be obtained in a similar fashion by replacing the polymer layer with an activation layer that can be stimulated by biological analytes, e.g. the sensing layer could be made up of antibodies for attachment of the antigens of target cells.

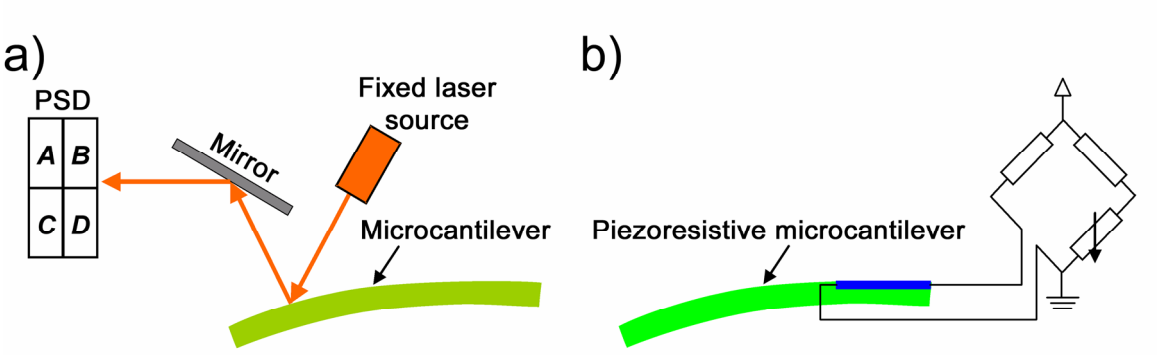

Figure 1.1 Chemical sensing with cantilever sensors is mostly done a) optically or b) piezoresistively; the former method uses a photosensitive device to detect the change in position of a reflected laser spot due to cantilever bending; the latter method uses doped silicon, which changes its resistivity due to the stresses upon bending; this resistance change can be read out electronically, e.g. using a Wheatstone bridge as shown in the figure

The physical signal can be measured either statically in the case that the activation layer induces a change in the cantilever stress state or dynamically in the case of a change in the stress state, the mass, or the spring constant. Most dynamic measurements monitor the shift in the resonance frequency, which can be caused by any of the three mentioned quantities. However, monitoring the quality factor, usually in addition to the resonance frequency can improve the significance of the output signal.

For the signal readout, two methods make up the majority of all chemical and biological sensing applications with microcantilevers. The first is naturally the optical method using an AFM, since this is the technology that initiated the development of microcantilevers in the first place. The second technology that, due to its simplicity, has become more popular within the last years is piezoresistive readout. The working principles of these two technologies are shown in Figure 1.1. Other methods that have

been used to measure mechanical signals in microcantilevers include piezoelectric and capacitive scanning. However, all of these technologies have not been able to show the same potential as the optical and the piezoresistive readout schemes. It should be noted that any readout scheme can be combined with either dynamic or static operation.

1.2 Previous Work

The first application of using microcantilevers to detect deflections due to surface stresses and resonance frequency shifts due to added mass was demonstrated by Thundat et al. in 1994 [3]. The group used a conventional AFM system to study the behavior of coated cantilevers while varying the environmental temperature and humidity. Early examples of chemical sensing using microfabricated cantilevers in AFM systems were published by Chen et al. [4] and Butt [5] in 1995. The former group studied the resonance frequency shift of gold coated cantilevers due to absorption of mercury vapor. The latter author functionalized the cantilevers with a layer of thiol to study the static deflection upon hexane and silane exposure. A comparable setup was first used for biological sensing in 1997 by Antonik et al. [6]. These researchers grew living cells on a microcantilever and measured the cantilever deflection upon exposure of the cells to certain toxins. In 1999, Raiteri et al. used microcantilevers that had one surface covered with a herbicide and showed concentration dependent response of specific antibodies in solution [7].

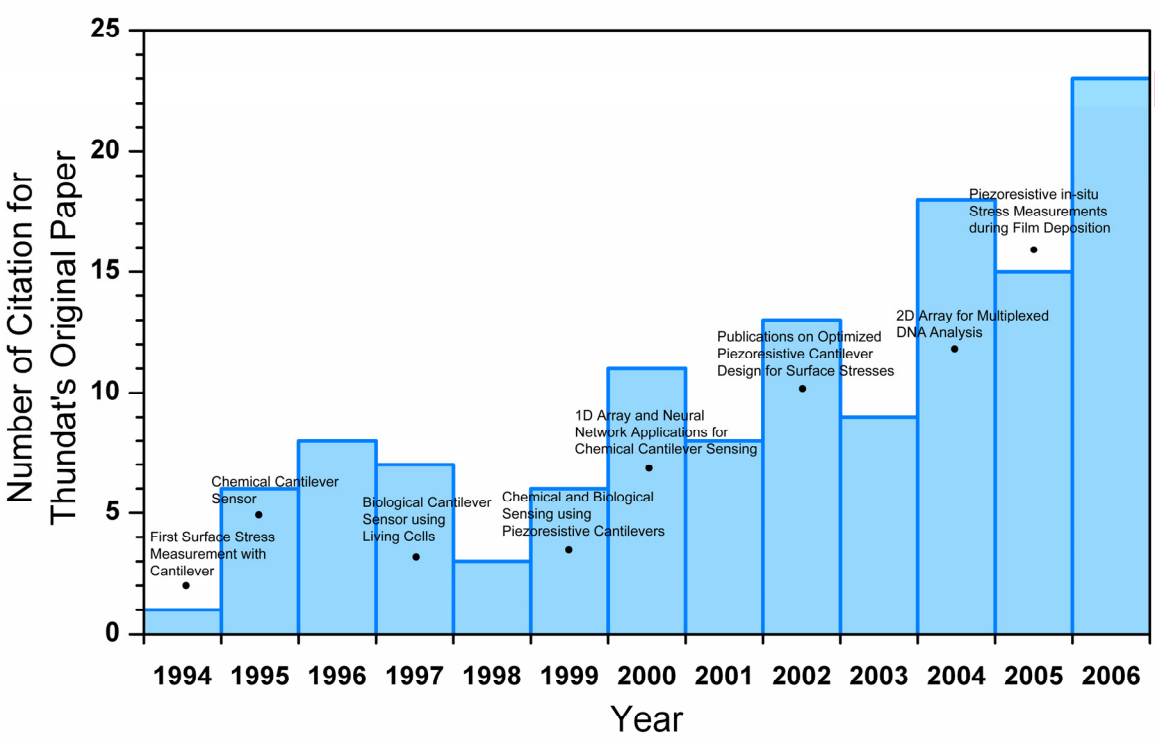

Figure 1.2 Timeline for surface stress measurements using microcantilevers; the number of citations for the original paper on the subject [3] and important publications are shown for each year between 1994 and 2006

These and most of the other early demonstrations of microcantilevers for biological and chemical detection were performed with regular, commercial cantilevers that were designed for surface topography scanning in AFM systems. This is also true for the first applications of piezoresistive sensors in this area [8]. Microcantilevers for surface stress sensing attracted significant interest for biomolecular and medical applications starting in 2000, and papers on these subjects have been published in some of the most prestigious journals [9], [10], [11]. Figure 1.2 indicates the growth of the field of chemical and biological microcantilever sensing by showing the number of citations of Thundat's original paper [3] per year. References to important innovations in this area are also shown in the figure.

1.3 Thesis Overview

The next chapters of this thesis will be divided up as follows:

- Chapter 2: Analytical and numerical analysis of microcantilevers for biological and chemical sensing.
- Chapter 3: Design, fabrication and characterization of first generation biological and chemical sensing microcantilevers.
- Chapter 4: Modeling, design, fabrication, and characterization for second cantilever generation, which includes on-chip heater areas.
- Chapter 5: Conclusion and future work.

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CHAPTER 2

MODELING THE CANTILEVER MECHANICAL RESPONSE TO SURFACE STRESS DURING CHEMICAL SENSING

In this chapter, the theoretical considerations for chemical sensing microcantilevers are discussed. In the first section, basic concepts of surface stress, piezoresistivity, and electrical conductivity in doped silicon are introduced. The second section deals with the modeling of microcantilevers for point force and surface stress sensing, and discusses the effects of their design parameters. In the third section, the modeling of the cantilever's electrical properties is discussed.

2.1 Theoretical Background

In this section, an overview of the concept of surface stresses on a substrate and their affect on the substrate's curvatures as defined by Stoney's formula are given. Furthermore, piezoresistivity in general and its occurrence in boron doped silicon in specific are given. Finally, the theoretical background for electrical conductivity in doped silicon and the relationship between resistivity, sheet resistance and total resistance are discussed.

2.1.1 Definition of Surface Stress

The term "surface stress" is often used very loosely and can apply to stresses involved with any combination of interfaces between solids, liquids, and gases. In the

field of chemical sensing using microcantilevers, the surface stress is used to quantize the effect of a reaction at the cantilever surface. If a film of thickness t_f experiences a mean stress of σ_m, e.g. a polymer film due to swelling in reaction to a chemical, the surface stress σ_s that this causes on the cantilever surface is given by

$$\sigma_m = \frac{\sigma_s}{t_f} \tag{2.1}$$

The unit of surface stress as defined in equation (2.1) is force per length. The surface stress is often referred to as membrane force [1], which is a more accurate term. It is inherently isotropic within the cantilever surface plane, i.e. its magnitude is not dependent on the direction. As early as 1909, Stoney [2] found a relationship between the stress in a film on a cantilever surface and the radius of curvature caused by this stress. Equation (1.2) is valid for rectangular cantilevers and it is commonly referred to as Stoney's formula [3].

$$\frac{1}{r} = \frac{6 \cdot \left(\Delta\sigma_1 - \Delta\sigma_2 \right)}{M_c \cdot t_c^{\,2}} \tag{2.2}$$

where r is the radius of curvature of the cantilever, M_c is the cantilever material's biaxial modulus, t_c is the thickness of the cantilever and $\Delta\sigma_1$ and $\Delta\sigma_2$ are the changes in the surface stresses at the cantilever top and bottom surfaces, respectively. So defined, the radius of curvature will be positive when the surface stress on the top surface is greater than on the bottom surface, i.e. the cantilever will curl upwards. The biaxial modulus is defined as

$$M_c = \frac{E_c}{1 - \nu_c} \tag{2.3}$$

where E_c and v_c are the Young's modulus and the Poisson's ratio of the cantilever material, respectively. Since the surface stress loading will cause the cantilever to deflect in a circular shape, the cantilever tip deflection δ can be derived from simple geometric considerations [4]. The deflection is

$$\delta = r - \sqrt{r^2 - l_c^{\,2}} \tag{2.4}$$

where l_c is the length of the rectangular cantilever. If the radius of curvature is much greater than the cantilever length, a first order approximation of equation (2.4) can be made, by executing a Taylor series expansion of the square root term about r^2:

$$\begin{aligned}\sqrt{r^2 - l_c^{\,2}} &= \sqrt{r^2} + \frac{\left(\sqrt{x}\right)'\Big|_{x=r^2}}{1!}\cdot\left(\left(r^2 - l_c^{\,2}\right) - r^2\right) + \frac{\left(\sqrt{x}\right)''\Big|_{x=r^2}}{2!}\cdot\left(\left(r^2 - l_c^{\,2}\right) - r^2\right)^2 + \ldots \\ &\approx r - \frac{1}{2r}\cdot l_c^{\,2} \\ &\Rightarrow \delta \approx \frac{l_c^{\,2}}{2r}\end{aligned} \tag{2.5}$$

For an AFM system, the output signal during chemical sensing needs to be modified to calculate the correct value for the surface stress from equation (2.2). The reason for this is that the AFM does not actually measure the tip deflection, but rather the tip deflection angle based on the assumption of a point force at the cantilever free end. Since the shapes for the deflected cantilever in the case of surface stress load and point force at the free end are different, the signal for the tip deflection δ_{cal} obtained from the AFM and calibrated for a force load must be converted to obtain the actual tip deflection δ. The relationship between the radius of curvature of a cantilever with a surface stress and δ_{cal} can be written as

$$\frac{1}{r} = \frac{3\cdot\delta_{cal}}{l_c\sqrt{4l_c^{\,2} + 9\delta_{cal}^{\,2}}} \tag{2.6}$$

Stoney's formula gives a simple relationship between the surface stresses and the radius of curvature in a cantilever, and it shows good accuracy in many cases. However, it is limited to cases in which the thickness of the surface stress causing film is negligible compared to the cantilever thickness. Another problem with Stoney's formula is that it is derived from the bending behavior of a free plate that has no constrictions. Obviously, the latter assumption can not be met in real systems, since (at least) one side of the body is attached to a fixed substrate. Sader [5], [6] suggested corrections to Stoney's formula for clamped cantilevers, which become especially important for cases in which the clamping has a significant effect on the stress state in the cantilever, i.e. for short and wide geometries. From equations (2.2) and (2.6), it becomes apparent that the favorable geometry for measurements of surface stress using an AFM are long, thin cantilevers since they will experience the largest tip deflection and therefore the highest AFM output signal [7]. This is quite similar to the case of AFM force measurements with a point load at the cantilever tip [8]. However, for the sensing of surface stresses using piezoresistive output schemes, the relationships are not as simple and other geometries turn out to be more favorable. This will be the subject of discussion later in this chapter.

2.1.2 Piezoresistivity in Silicon

The change of a material's resistance due to an external load was first discovered by Lord Kelvin (a.k.a. William Thomson) in 1856 [9]. This "piezoresistive" (from Greek: piezein – to squeeze) behavior can be seen in all electrically conductive materials and is in most cases a strictly geometric effect, e.g. when a wire is stretched it becomes longer and its cross-section shrinks, and both of these effects contribute to an increase in its resistance value. The piezoresistive sensitivity $\Delta R/R$ of an isotropic material to a uniaxial

strain ε_x is called the gauge factor K and for metals, it only depends on the Poisson's ratio by

$$K = \frac{\Delta R / R}{\varepsilon_x} = 1 + 2\nu \tag{2.7}$$

In 1954, Charles Smith [10] discovered that semiconductors, in this case germanium and silicon, can have gauge factors that are two orders of magnitude greater than those of metals, indicating that piezoresistivity in semiconductors is not only due to the geometric effect. It was found that the resistivity itself is a function of the stress level in these materials and that this effect is highly anisotropic for single crystalline structures. Rather than using a single gauge factor, three independent piezoresistive coefficients are employed to describe the relative resistance change in a given crystal direction in response to a three dimensional stress state in the material. These coefficients are given for p-doped (e.g. using boron) and n-doped (e.g. using phosphorus) single crystalline silicon in Table 2-1 [11].

Table 2-1 Resistivity and piezoresistivity coefficients at room temperature (in 10^{-11} Pa^{-1}), (100) silicon wafers and doping levels below 10^{18} cm^{-3}

	ρ (Ω·cm)	Direction	π_{11}	π_{12}	π_{44}	π_t	π_l
p-Si	7.8	<100>				0	0
		<110>	+6.6	-1.1	+138.1	-66	72
n-Si	11.7	<100>				+53.4	-102.2
		<110>	-102.2	53.4	-13.6	-18	-31

For practical purposes, it is more convenient to consider effective coefficients to calculate the resistance change of a conducting element from a 2-dimensional stress state

$$\Delta R/R = \sigma_l \cdot \pi_l + \sigma_t \cdot \pi_t \tag{2.8}$$

where σ_l and σ_l are the longitudinal (parallel to the current direction) and transversal (perpendicular to the current direction) stresses, respectively, and π_l and π_t are the according piezoresistive coefficients. Note that these effective coefficients depend on the elementary coefficients from table 2-1 and the crystal direction of the conductor. In most cases, silicon wafers with a crystal orientation of (100) or (110) are used and the piezoresistors are realized in-plane. This means that the magnitude of the effective piezoresistive coefficients can only be altered by the alignment of the conducting element within the wafer plane and this directional relationship can be conveniently displayed in polar plots as shown for (100) silicon wafers in Figure 2.1 [12].

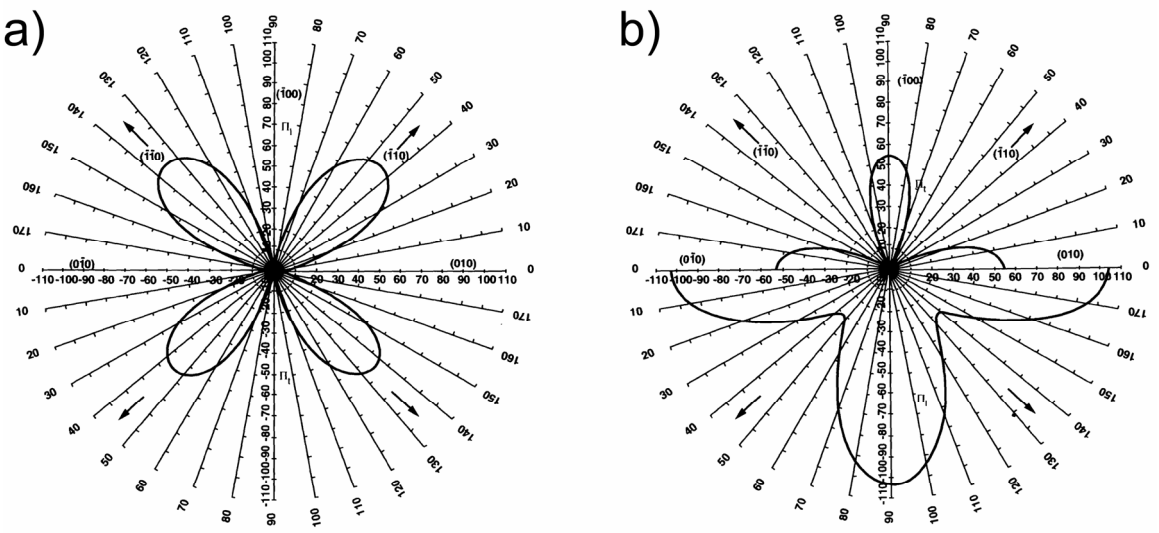


Figure 2.1 Piezoresistive coefficients π_l and π_t for (100) silicon in the (001) plane in 10^{-12} Pa^{-1} for a) p-type silicon and b) n-type silicon (from [11], [12])

It can be seen that the longitudinal and transversal coefficients have approximately the same absolute value (but opposite sign) for p-type silicon, and that they each have a maximum in the equivalent <110>-directions. For n-type silicon, the longitudinal coefficient has about twice the absolute value (and opposite sign) compared

to the transversal coefficient, and both of them are maximized in the equivalent <100>-directions. This work utilizes the piezoresistive effect of boron doped, i.e. p-type silicon, and therefore, only this type of piezoresistive sensing will be explained in more detail here. With the longitudinal coefficient ($\sigma_l = 72 \cdot 10^{-11} Pa^{-1}$) being of about the same absolute value but of different sign than the transversal coefficient ($\sigma_t = -66 \cdot 10^{-11} Pa^{-1}$), a good approximation of equation (2.8) is given as

$$\Delta R/R \approx \frac{\pi_l + \pi_t}{2} \cdot (\sigma_l - \sigma_t) = \frac{\pi_l + \pi_t}{2} \cdot \Delta\sigma_{lt} = 69 \cdot 10^{-11} Pa^{-1} \cdot \Delta\sigma_{lt} = \pi_{lt} \cdot \Delta\sigma_{lt} \qquad (2.9)$$

Therefore, any p-doped piezoresistive device should be designed to maximize the stress difference $\Delta\sigma_{lt}$ within the piezoresistive element. In the case of piezoresistive cantilever sensors, this can be done by modifying the geometry of the cantilever and the size and placement of the piezoresistors. In the following sections, these two parameters are investigated and weighed against other considerations for the cases of a point load at the cantilever's free end and a surface stress on the cantilever.

2.1.3 Properties of Doped Silicon

The piezoresistive regions in the cantilever are created by an ion implantation process in which boron atoms are accelerated to penetrate the silicon. A boron atom has a valency of three, i.e. there are three electrons in its valence shell. When the boron atoms take substitutional sites in the crystal lattice of silicon, which itself has a valency of four, the resulting hole, i.e. the absence of one valence electron, acts as the majority carrier for electrical current. The number of free electrons in the silicon lattice in these p-type doped regions is much smaller than the number of holes. Therefore, the electrons represent the minority carriers. The electrical resistivity ρ in doped silicon is a function of the doping

level. Since the doping level is usually a function of the coordinate along the cantilever thickness direction, it is more convenient to use the sheet resistance R_s, which is the resistance R of a block of same width and length of a material. The sheet resistance therefore takes into account the changing resistivity along the thickness direction and is a well-suited method to use for resistors of plane geometry. Although the unit of sheet resistance is Ω it is often written as Ω/□ (ohms per square) to clearly distinguish it from regular resistance values. The relationship between resistance of the piezoresistor R_p, sheet resistance R_s and resistivity $\rho(z)$ is given by

$$R_p = R_s \cdot \frac{l_p}{w_p} = \frac{1}{\int_0^{t_c} \frac{1}{\rho(z)} dz} \cdot \frac{l_p}{w_p} \tag{2.10}$$

where l_p and w_p are the length and width of the piezoresistor, respectively, and t_c is the thickness of the cantilever.

2.2 Modeling of Piezoresistive Cantilevers

In order to optimize piezoresistive cantilevers for sensitivity to surface stresses, the effect of design parameters needs to be well-understood. This section will start with a discussion of piezoresistive microcantilever for the sensing of point forces, for which an accurate analytical expression can be given. Then, an analytical model of surface stress sensing cantilevers will be given and its limitations will be pointed out. Finally, finite element modeling (FEM) will be used to predict the cantilever sensitivity for the surface stress loading case and to study design parameters of the microcantilever and its piezoresistive area.

2.2.1 Design of Piezoresistive Force Sensing Cantilevers

In this first part, design criteria for cantilever sensors optimized for measuring point loads at the free end are discussed. Applications of this kind of measurement technique could include nanoindentation [13] and biomolecular force measurements [14]. From simple two dimensional considerations, the stress in the cantilever x-direction can be derived as a function of the position in the beam as shown in Figure 2.2a by

$$\sigma_x(x,z) = \frac{F \cdot 12}{w_c \cdot t_c^{\,3}} \cdot (l_c - x) \cdot z \tag{2.11}$$

where F is the applied point force at the free end, and w_c, t_c, and l_c are the cantilever width, thickness, and length, respectively. The two dimensional model assumes that stress in the y-direction σ_y is always linearly related to σ_x through $\sigma_y = -\nu \cdot \sigma_x$. Thus, for a piezoresistor along the cantilever length direction ($\sigma_l = \sigma_x ; \sigma_t = \sigma_y$), the stress difference $\Delta\sigma_{lt}$ is

$$\Delta\sigma_{lt}(x,z) = \sigma_x - \sigma_y = (1+\nu_c) \cdot \sigma_x = \frac{F \cdot 12 \cdot (1+\nu_c)}{w_c \cdot t_c^{\,3}} \cdot (l_c - x) \cdot z \tag{2.12}$$

To check the accuracy of equation (2.11), the results are compared to an finite element (FE) model using the software package ANSYS. The model includes the cantilever and a part of the anchoring substrate, and it is shown in Figure 2.2b.

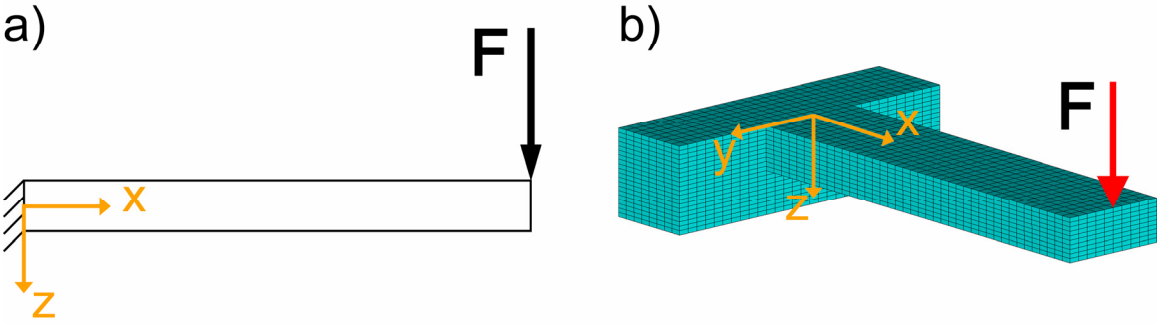


Figure 2.2 Schematics of the cantilever with point load at the free end for a) the analytical model b) the FE model

The cantilever length, width and thickness are chosen to be 100μm, 25μm, and 10μm, respectively. The outer areas of the anchoring substrate, except for the side that the cantilever is attached to and the top side, are fully constrained. Figure 2.3 shows the stress distributions in x- and y-direction from the analytical solution and the x-z-plane of the FEM solution for comparison.

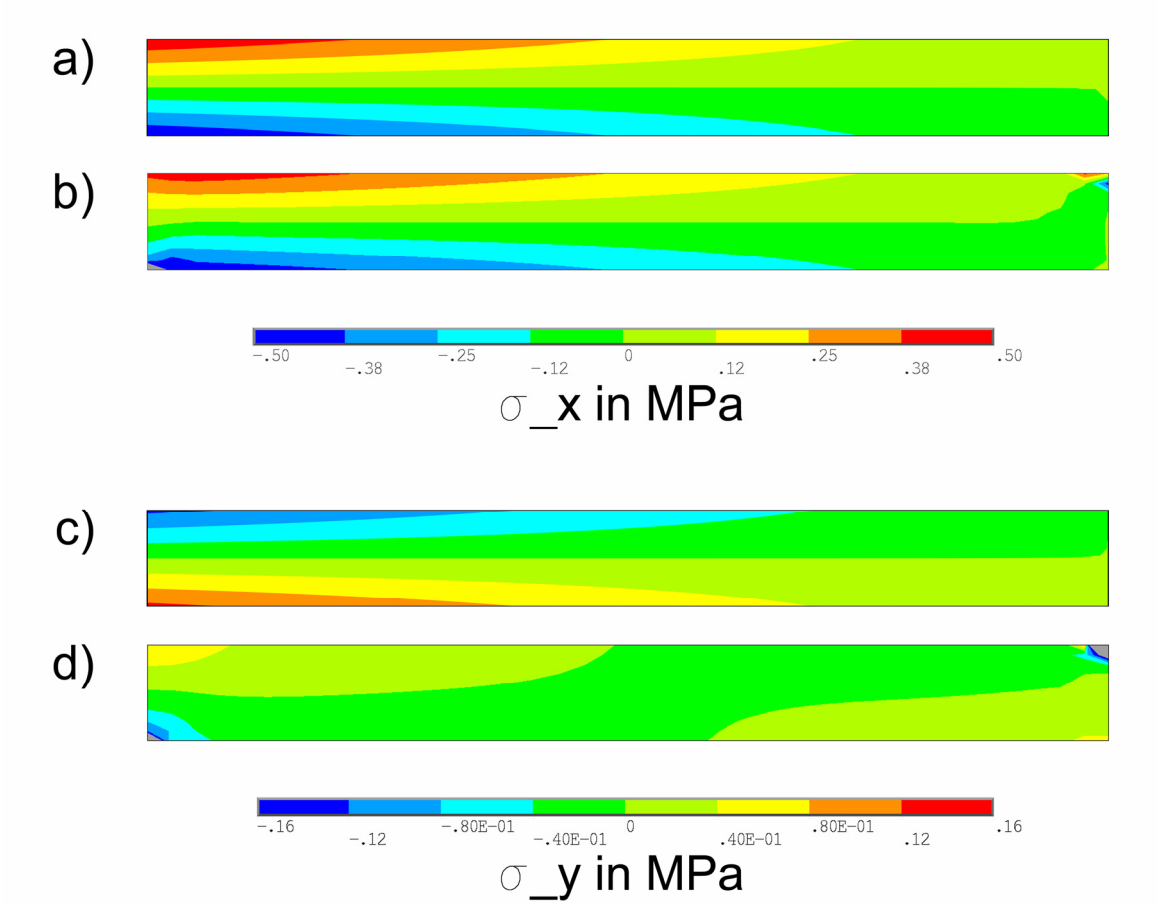


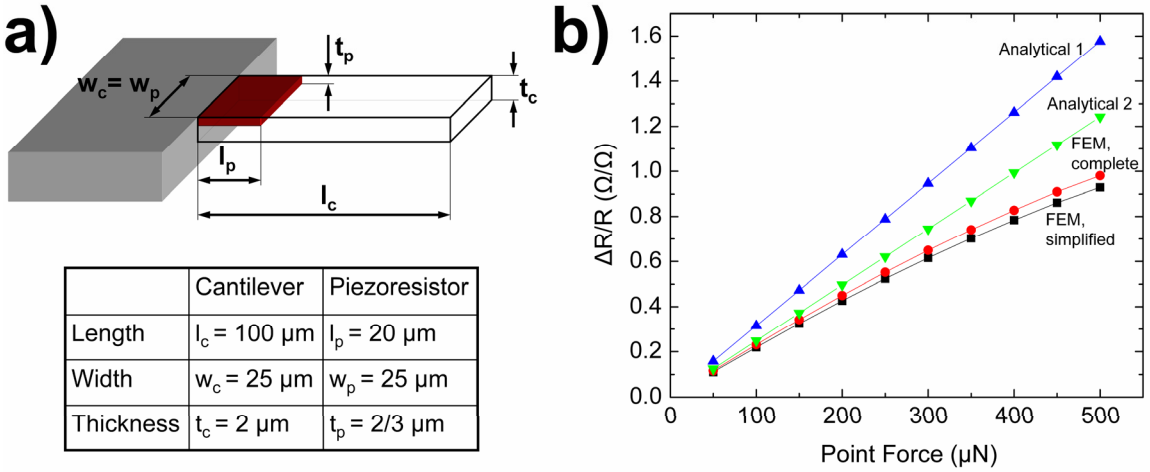
Figure 2.3 Distribution of the stress in x-direction (a and b) and y-direction (c and d) along the x-z-plane from the analytical model (a and c) and the FE model (b and d). The cantilever clamped base is on the left, the free end with point load is on the right.

The stress in x-direction is predicted in both its magnitude and distribution very well by the analytical model. The only differences that can be seen in the FE model are the stress concentrations due to the point force at the cantilever free end and to a smaller degree at the clamping, which are not considered in the analytical solution. The stress in y-direction differs significantly between the two models, which is mainly due to the more pronounced effect the clamping has on the stress in this direction. Only far away from the clamping and not directly at the free end do the two solutions show good agreement. However, if the stress difference is the important parameter, the analytical solution still has some validity because the stress in x-direction is much higher than the stress in y-

direction and it agrees well with the FE model. From the stress distribution, the resistance change $\Delta R/R$ of a piezoresistor within the cantilever can be determined. Assuming that the current direction within the cantilever is in the direction of the cantilever length, the average resistance change for the analytical model can be calculated by integrating equation (2.12) over the piezoresistive area, dividing by that area, and plugging the result into equation (2.9), which can be summarized as

$$\Delta R/R = \pi_{lt} \cdot \frac{1}{(x_2 - x_1)(z_2 - z_1)} \int_{x_1}^{x_2} \int_{z_1}^{z_2} \frac{F \cdot 12 \cdot (1+\nu_c)}{w_c \cdot t_c^{\,3}} \cdot (l_c - x) \cdot z \, dz \, dx \qquad (2.13)$$

where (x_1,z_1) and (x_2,z_2) are two opposite corners of a rectangular piezoresistive element within the cantilever. For the FE model, equations (2.8) or (2.9) can be used within each element in the piezoresistive area and the results are averaged over all elements. To compare the results for the resistance change from the analytical model to the FE model, a more realistic cantilever geometry than in Figure 2.2, i.e. a device with smaller thickness, was chosen.



	Cantilever	Piezoresistor
Length	l_c = 100 μm	l_p = 20 μm
Width	w_c = 25 μm	w_p = 25 μm
Thickness	t_c = 2 μm	t_p = 2/3 μm

Figure 2.4 a) Chosen cantilever and piezoresistor dimensions for the comparison of the different models; b) relative resistance change over point force at cantilever free end calculated by three different models

From the geometries of cantilever and piezoresistor as shown in Figure 2.4a, equation (2.13) becomes

$$\begin{aligned} \Delta R/R &= \pi_{lt} \cdot \frac{1}{l_p \cdot t_p} \int_{o}^{l_p} \int_{t_c/2-t_p}^{t_c/2} \frac{F \cdot 12 \cdot (1+\nu_c)}{w_c \cdot t_c^{\,3}} \cdot (l_c - x) \cdot z \, dz \, dx \\ &= \pi_{lt} \cdot \frac{12 \cdot (1+\nu_c)}{w_c \cdot t_c^{\,3}} \cdot \left(l_c - \frac{1}{2} l_p \right) \cdot \left(\frac{t_c}{2} - \frac{t_p}{2} \right) \cdot F \end{aligned} \tag{2.14}$$

where l_p and t_p are the length and thickness of the piezoresistor, respectively. Since the geometric variables x and z are linear in equation (2.13), the resistance change of the piezoresistor is simply the result of that equation evaluated at the center of the piezoresistor. Figure 2.4b shows the results from this analytical solution (Analytical 1) compared to the results from the FE model calculated from either the complete formulation as given in equation (2.8) or the simplified formulation using the stress difference as given in equation (2.9). It can be seen that the first analytical model overestimates the solution by at least 35%. This is due to the incapacity of the model to correctly describe the distribution of the stress in y-direction close to the cantilever base as previously discussed and shown in Figure 2.3. If the piezoresistor is placed very close to the clamped end, a better approximation is achieved by assuming zero stress in y-direction, thus taking out the factor of $(1+\nu)$ in equations (2.12)-(2.14). The resulting change is shown in Figure 2.4 (Analytical 2) and given by

$$\Delta R/R = \pi_{lt} \cdot \frac{12}{w_c \cdot t_c^{\,3}} \cdot \left(l_c - \frac{1}{2} l_p \right) \cdot \left(\frac{t_c}{2} - \frac{t_p}{2} \right) \cdot F \tag{2.15}$$

The deviation of the FEM solutions from the linear behavior is caused by geometric non-linearities at large tip deflections (47.0 μm at 500μN), which are accounted for in this type of analysis. The fact that the two FEM solutions differ by no

more than 5.3% indicates that the stress difference $\Delta\sigma_{lt}$ as defined in equation (2.9) is indeed a good measure for the piezoresistive response. Therefore, this parameter will be used in most cases throughout this work. In real cantilever devices, the density of the dopants varies gradually along the cantilever thickness direction, which is due to the microfabrication processes and natural diffusion. This dopant distribution impacts both the piezoresistive coefficients and the resistivity, so that the exact solution cannot be described by an analytical expression. It is also difficult to measure the dopant distribution within the silicon, but the results of dopant implantation and heat treatment processes can be predicted well with simulation tools (see section 2.3.1). When a dopant profile that approximates a step function is achieved, equation (2.15) can be a good estimate. Often, a fitting parameter β that accounts for the thickness and the dopant profile of the piezoresistors is used. Its value ranges from zero (even doping throughout the cantilever thickness) to 1 (dopants only at the top surface and concentration ideal for maximum sensitivity. Instead of using equation (2.15), the resistance change is then given by

$$\Delta R/R = \beta \cdot \pi_{lt} \cdot \frac{6}{w_c \cdot t_c^{\,2}} \cdot \left(l_c - \frac{1}{2} l_p \right) \cdot F \tag{2.16}$$

In summary, the results of this discussion indicate that force sensing cantilevers should be made long and thin, and the piezoresistive area should be short and thin and as close to the clamped base as possible. These results are qualitatively and for small displacements also quantitatively backed by both the simplified and the complete FE model. Furthermore, non-linear FEM can predict the behavior even for large deformations.

2.2.2 Analytical Modeling of Piezoresistive Surface Stress Sensing Cantilevers

In the previous section, FEM was briefly introduced as a method to improve the results obtained from analytical formulae in the case of a point load at the cantilever free end. For the analysis of cantilevers that experience a surface stress, FEM is much more important as will be seen below. Therefore, a more detailed description about the methods used in this work will be given in this section. All of the FEM was done using the software package ANSYS 10.0. The element type for microcantilevers is either "solid95" for isotropic behavior or "solid186" when the anisotropic elastic properties of single crystalline silicon are to be accounted for. To apply a surface stress to the top side of the cantilever, a layer of either three-dimensional or two-dimensional elements is simulated that is pre-stressed with a given stress value. If the equivalent surface stress on the cantilever is the input variable to the FE model, the latter case is more efficient since two-dimensional elements (in this case "plane82") require less computing power and the results are more accurate. If a more realistic system, e.g. a microcantilever with a polymer layer that experiences swelling upon exposure to an analyte, is to be modeled, three-dimensional elements ("solid95") that account for the finite thickness of the film, which causes the surface stress, are employed. All of the chosen element types are of high order, which gives more accurate results at a given mesh density and allows for the calculation of large, non-linear deformations. To apply a given stress to the film layer, whether simulated in 2D or in 3D, the command "istress" is employed. Note that the input variables for a given stress within the x- and y- plane are the mean stress levels given in the unit of pressure. To calculate the surface stress that is caused by this virtual (2D) or realistic (3D) layer, the film thickness has to be multiplied as given in equation

(2.1) and the unit of the resulting surface stress will be force/length. For all FE simulations in this work, the μMKS system of units is employed, in which the units for length, mass, time, force, stress (pressure), and surface stress are 1 μm, 1 kg, 1 sec, 1 μN, 1 MPa, and 1 N/m, respectively. These units are very convenient for MEMS because the typical length scale is on the order of 1-100 μm, and the typical stress levels are on the order of 1-100 MPa. In all calculations, part of the anchoring silicon substrate is modeled instead of just constraining one of the cantilever ends directly. This results in a more realistic stress distribution, especially at the cantilever base, i.e. the clamped end. Whenever possible, i.e. in all cases except for modal analyses, only one half of the cantilever is modeled and the cutting plane (along the cantilever length and thickness directions) is constrained with symmetry boundary conditions to reduce the computation time and required memory. The objective of the FE modeling is to find the stress distribution, especially the stress difference $\Delta\sigma_{lt}$, within the piezoresistive volume of the cantilever and to maximize this value by modifying the cantilever geometry as well as the piezoresistor geometry and placement. With the definition of the spring constant for a rectangular cantilever

$$k = \frac{F}{\delta} = \frac{w_c \cdot t_c^{\,3} \cdot E_c}{4 \cdot l_c^{\,3}} \tag{2.17}$$

the resistance change due to a point force, equation (2.16), can be converted into the resistance change due to a free end deflection by

$$\Delta R \big/ R = \beta \cdot \pi_{lt} \cdot \frac{3 \cdot E_c \cdot t_c}{2 \cdot l_c^{\,3}} \cdot \left(l_c - \frac{1}{2} l_p \right) \cdot \delta \tag{2.18}$$

If the stress state inside the cantilever for the case of a surface stress is assumed to be similar to that of a point load case, equation (2.18) can be combined with the equations from previous sections to determine the resistance change due to surface stress [15].

$$\delta \underset{(1.5)}{=} \frac{l_c^2}{2r} \underset{(1.2)}{=} \frac{l_c^2}{2} \cdot \frac{6 \cdot (\Delta\sigma_1 - \Delta\sigma_2)}{M_c \cdot t_c^2} \underset{(1.3)}{=} \frac{l_c^2}{2} \cdot \frac{6 \cdot (1-\nu) \cdot (\Delta\sigma_1 - \Delta\sigma_2)}{E_c \cdot t_c^2}$$

$$\underset{(1.17)}{\Rightarrow} \Delta R/R = \beta \cdot \pi_{lt} \cdot \frac{3 \cdot E_c \cdot t_c}{2 \cdot l_c^3} \cdot \left(l_c - \frac{1}{2} l_p \right) \cdot \frac{l_c^2}{2} \cdot \frac{6 \cdot (1-\nu) \cdot (\Delta\sigma_1 - \Delta\sigma_2)}{E_c \cdot t_c^2} \tag{2.19}$$

$$= \beta \cdot \pi_{lt} \cdot \frac{9 \cdot (1-\nu)}{2 \cdot t_c} \cdot \frac{l_c - \frac{1}{2} l_p}{l_c} \cdot (\Delta\sigma_1 - \Delta\sigma_2)$$

From equation (2.19), it can be assumed that the cantilever length and width as well as the piezoresistor width have no effect on the sensitivity to surface stress $(\Delta R/R)/(\Delta\sigma_1 - \Delta\sigma_2)$. The validity of this analytical approximation will be discussed in comparison to FEM in the following section.

2.2.3 Design of Piezoresistive Surface Stress Sensing Cantilevers

Equation (2.19) is based on the assumption that the stress distribution in a cantilever with surface stress is similar to that of a cantilever with a given tip deflection. In order to investigate the validity of this assumption, the most feasible approach is to look at the stress distribution in the cantilever at its top surface. Figure 2.5 compares the stresses in x- and y-directions, σ_x and σ_y, for the case of a cantilever with point load and a cantilever with surface stress. The loading levels are chosen, such that the piezoresistive change from equations (2.16) and (2.19) should be identical.

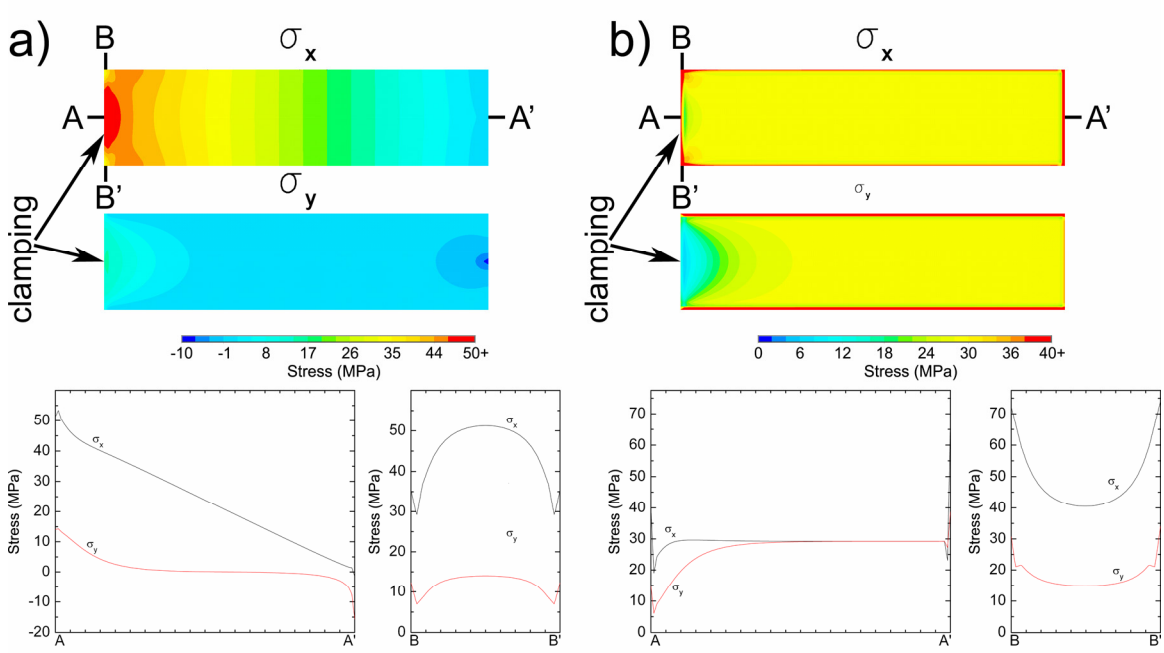


Figure 2.5 Stress distributions of a cantilever with a) a point force at the free end and b) a surface stress on the top surface

The comparison of the two loading cases clearly shows that the stress distributions within the cantilever and thus the piezoresistive output signal are very different. While the point force causes a stress distribution with a linearly decreasing stress in x-direction and a stress of much smaller magnitude in y-direction, this is not the case for the cantilever with surface stress loading.

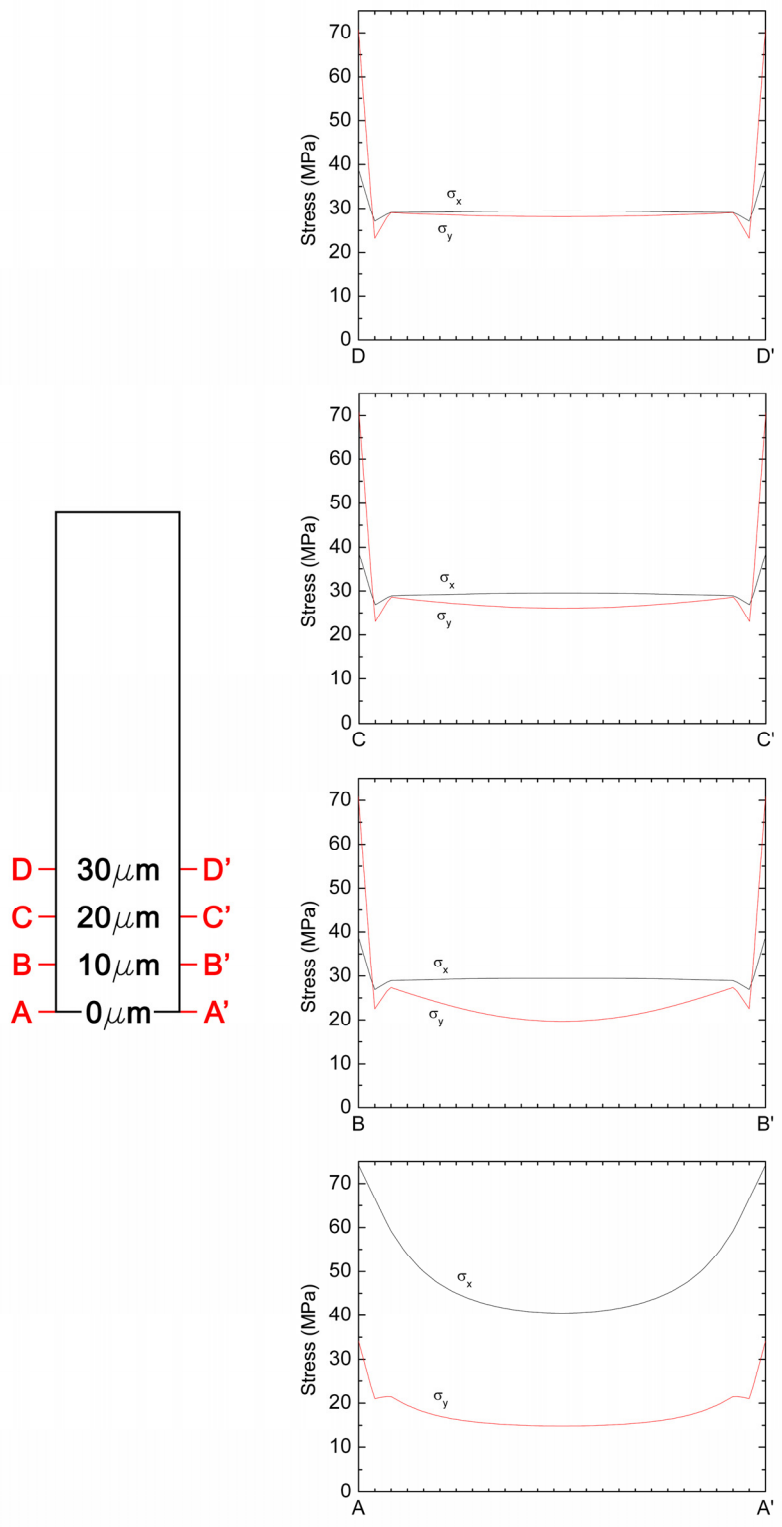


Figure 2.6 Distribution of stresses close to the surface in x- and y-direction for different cross-sections of a cantilever with surface Stress. The clamped base is at the cross-section A-A'.

In the latter case, both stresses are equal far away from the clamped base as the surface stress causes isotropic bending in all directions if the plate is not constricted. The bottom section of Figure 2.5b shows that the stress in x-direction reaches the constant value that is equivalent to the stress in a free plate much closer to the base than the stress in y-direction. The reason for this is that the clamping of the cantilever along its width is much more restrictive for bending in the y-direction since the width is much greater than the thickness. One immediate design consideration based on these results is the variation of the cantilever width to modify the amount to which the stress in y-direction is constricted at the base. This will be discussed later in this section.

It has been shown that the piezoresistor should be placed close to the cantilever base for greater sensitivity to surface stress. In this context, the question arises whether the placement in y-direction is important. Figure 2.5 seems to indicate that the stress difference is higher at a local stress concentration point on the outside of the cantilever than in the cantilever center. Therefore, it seems as though this would be the ideal placement for the piezoresistive element. However, Figure 2.6 indicates that the stress difference decreases much faster along the cantilever edges than it does in the center. Since the piezoresistor must always be of certain minimum dimensions set by the fabrication process (to be discussed later), placing the piezoresistor on the cantilever edge would result in a reduced sensitivity. The high spike at the very edge within each cross-section is yet another effect, which is very much localized at the edge and results from the singularity at the unconstrained side wall. In summary, it can be concluded that the ideal placement of the piezoresistive element is in the center close to the cantilever base.

Since the stress difference is highest along the centerline of the cantilever, the piezoresistor should also be made as narrow as possible.

Most microfabrication processes for microcantilevers involve a process step in which the wafer is etched through from the backside to release the free hanging devices. This requires the alignment of the photomask on the wafer backside to the features on the frontside of the wafer, as well as a long etch process. Both of these steps have an inherent uncertainty for the location at which the backside trench will meet the cantilever devices. Therefore, it is necessary to make the piezoresistors of a certain minimum length, so that at least the largest part of the piezoresistor at the cantilever base is within the free-hanging area of the cantilever. Furthermore, for a given piezoresistor length, there is also a minimum width so that the resistance of the sensing area can be kept within given design criteria. These effects will be discussed in more detail in chapter 3. Here, it will be assumed that the minimum length and width for the piezoresistive area are each on the order of 40-60 μm for the employed microfabrication process.

For a given piezoresistor placement and size, as discussed above, the shape of the cantilever can be altered to improve the piezoresistive signal due to a surface stress on the cantilever. The stress difference $\Delta\sigma_{lt}$ within the top third of a cantilever of 200 μm length, 50 μm width and 1 μm thickness, and loaded with a surface stress at the top surface is shown in Figure 2.7a. These dimensions are realistic for devices that have been used for chemical sensing in previous studies. The proposed piezoresistive area of 40 x 40 μm^2 at the center of the cantilever base is shown as a dashed line in the figure. It can be seen that the stress difference $\Delta\sigma_{lt}$, which is a measure for the piezoresistive output signal as previously discussed, is zero for all areas except close to the clamping. It can also be seen

that the stress state in this region does not vary significantly for cantilevers of the same width, thickness and surface stress loading when the length is changed to 100 µm, 50 µm, and 400 µm as shown in Figure 2.7b, c, and d, respectively. The average $\Delta\sigma_{lt}$ for the region marked with the dashed line in these figures is plotted vs. the cantilever length in Figure 2.7e.

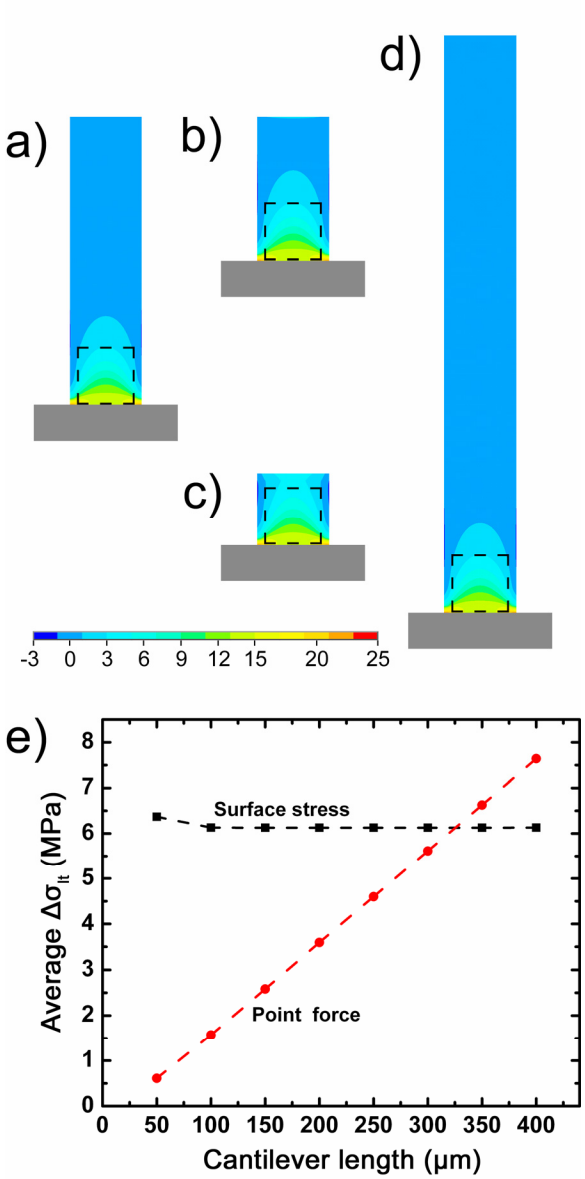


Figure 2.7 a)-d): Stress difference $\Delta\sigma_{lt}$ in the top third portion of cantilevers with a surface stress loading on the top surface, width 50 µm and length a) 200 µm b) 100 µm c) 50 µm and d) 400 µm; e) average stress difference $\Delta\sigma_{lt}$ within the piezoresistive element vs. cantilever length for surface stress and point force loading cases

It can be seen that in comparison to the case with a point force at the cantilever free end, the length of the cantilever does not affect the piezoresistive output signal significantly in the case of a constant surface stress. If the piezoresistive signal and thus the sensitivity cannot be improved by making the cantilever longer, it is interesting to investigate whether this effect can be achieved by increasing the cantilever width. In the previous discussion, it was supposed that a wider cantilever will be more resistive to bending in the width direction while the clamping has little influence on the stresses along the length direction. Therefore, the stress difference $\Delta\sigma_{lt}$ should be higher for wider cantilevers while keeping both the length and the surface stress loading constant. The stress differences $\Delta\sigma_{lt}$ in the top third of cantilevers with identical surface stress loading, a length of 200 μm and widths of 50 μm, 100 μm, 200 μm, and 400 μm are shown in Figure 2.8 a, b, c, and d, respectively. It can be seen that the magnitude of $\Delta\sigma_{lt}$ increases with the cantilever width. Furthermore, for wider cantilevers, the high stress values are present in larger parts of the previously defined piezoresistive area marked with dashed lines in the figure. Therefore, the average $\Delta\sigma_{lt}$ and consequently also the sensitivity to surface stress loading increase with the cantilever width. This is shown quantitatively in Figure 2.8e compared to the case for a point force at the free end, for which the sensitivity decreases with increasing width as expected from theory. It can be seen that for the given piezoresistor shape and cantilever length, the cantilever width should be at least 150 μm to be in the regime to the right of the steep increase in the sensitivity. In this regime, the sensitivity only increases moderately with cantilever width, so that there is a tradeoff between slightly improved sensitivity and greatly worsened compactness of the cantilever. An extremely wide cantilever is also disadvantageous for the design and

fabrication process as it requires a large space along the substrate and a backside etch process that is uniform enough to reach the right edge position at all points along the cantilever width. From these considerations, it can be concluded that a cantilever with width 200 µm, i.e. an length to width ratio of one, is a good compromise between sensitivity and compactness for the given piezoresistive area and cantilever length.

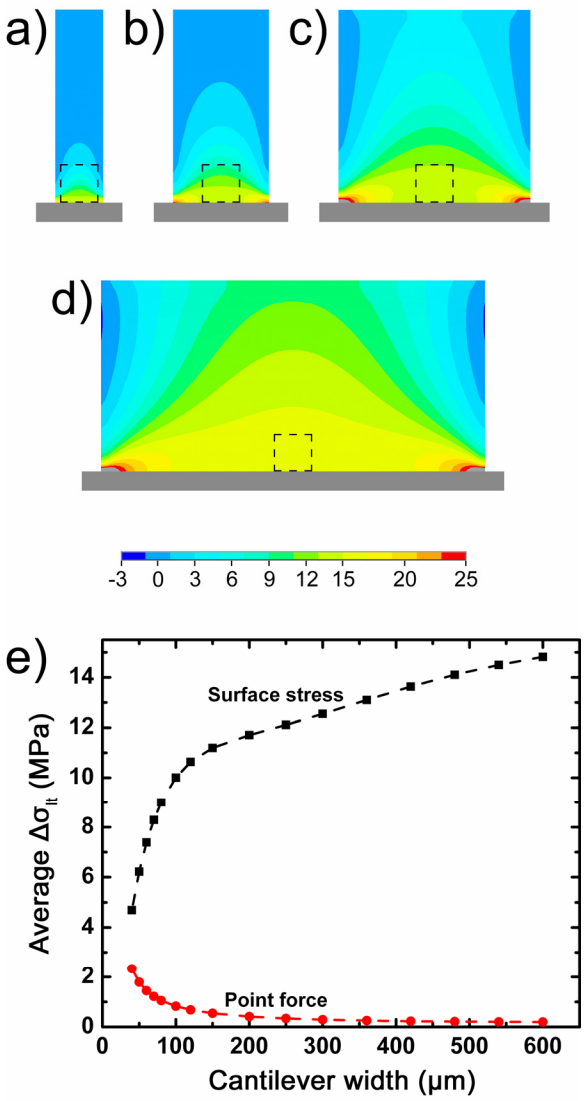


Figure 2.8 a)-d): Stress difference $\Delta\sigma_{lt}$ in the top third portion of cantilevers with a surface stress loading on the top surface, length 200 µm and width a) 50 µm b) 100 µm c) 200 µm and d) 400 µm; e) average stress difference $\Delta\sigma_{lt}$ within the piezoresistive element vs. cantilever width for surface stress and point force loading cases

If both the ratio of cantilever length to width and the piezoresistive area are fixed, it is interesting to see what effect the cantilever area has on the sensitivity. The average stress difference $\Delta\sigma_{lt}$ is plotted as a function of the cantilever area for the described scenario in Figure 2.9. It can be seen that an increase in the area beyond a certain value, in this case about 50000 μm^2, does not lead to an increase in sensitivity.

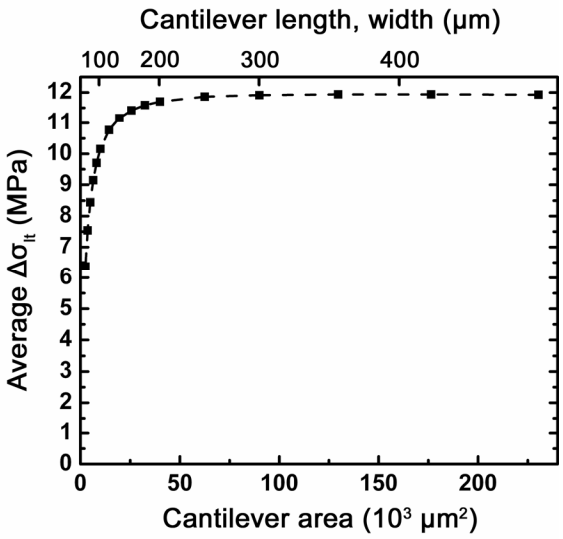


Figure 2.9 Average stress difference $\Delta\sigma_{lt}$ within the piezoresistive element as a function of cantilever area for a length to width ratio of one, thickness of 1 μm and constant surface stress loading

The figure also shows that increasing the cantilever length is actually counterproductive as the sensitivity does not reach the same values as in Figure 2.8 for large widths. Another important parameter for the sensitivity to surface stress is the cantilever thickness. As the cantilever stiffness increases with its thickness, thin cantilevers should be advantageous. In the case of a given point force at the free end, from equation (2.12) it can be seen that the maximum value for $\Delta\sigma_{lt}$ (at $z = l_c/2$) is proportional to the square of the cantilever thickness. However, in practical applications where the piezoresistor thickness is determined by the fabrication process, reducing the thickness is not always beneficial. In these cases, the centerline of the piezoresistor is

moved closer to the neutral axis of the cantilever as the cantilever thickness is decreased resulting in a decrease in sensitivity. For the case of a surface stress loading, the piezoresistive signal is shown as a function of the cantilever thickness in Figure 2.10. The length and width dimensions of the analyzed cantilever are 200 μm each and the piezoresistive area is 40 μm square.

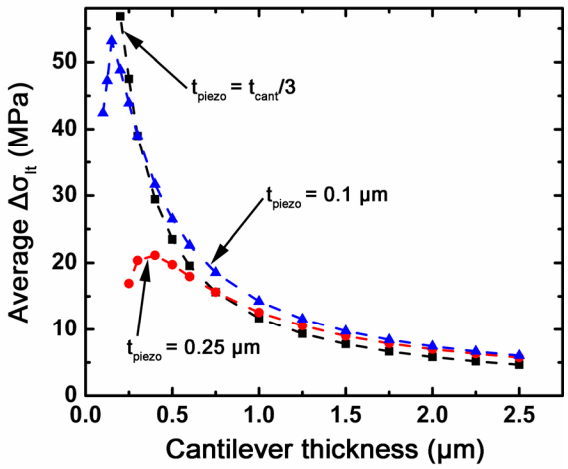


Figure 2.10 Average stress difference $\Delta\sigma_{lt}$ within the piezoresistive element as a function of cantilever thickness for the cases of two fixed piezoresistor thicknesses, 0.1 μm and 0.25 μm, and for the case of the piezoresistor thickness being one third of the cantilever thickness

The figure compares the cases of fixed piezoresistor thicknesses of 0.1 μm and 0.25 μm and the case in which the piezoresistor thickness is one third of the cantilever thickness. For the latter case, the output signal increases with decreasing cantilever thickness as expected. The relationship can be approximated very well as inversely proportional. For the cases in which the piezoresistor thickness is fixed, the sensitivity at first also increases with decreasing cantilever thickness. However, when the cantilever thickness gets below a certain value the signal decreases because of the piezoresistor's proximity to the neutral axis. Yet, as opposed to the point load case, the signal does not go to zero when the piezoresistor thickness is equal to the cantilever thickness. There are

two reasons for this effect. Firstly, in this loading case the stress distribution is a strong function of the position in cantilever width direction and the signal is only determined by a portion of the width. Secondly, due to the surface stress boundary condition, the beam does not have a free top surface, and thus the beam equations within the cantilever do not have to be fulfilled. This means that the result from integrating the stress in cantilever length direction over the cantilever thickness does not have to be zero. The maximum sensitivity for the given scenario is achieved when the piezoresistor thickness is about two thirds of the cantilever thickness. Furthermore, the cantilever thickness should be minimized to maximize the sensitivity.

In summary, it can be said that the cantilever width and thickness as well as the dimensions of the piezoresistor are the dominant parameters for the sensitivity to surface stress. The piezoresistor should be placed in the center of the clamped base, and it is always beneficial to minimize the piezoresistor length, width and thickness to achieve higher sensitivity. However, due to fabrication processes, such as etch uniformity, and design restrictions, such as maximum total resistance, these parameters often have lower limits. For a piezoresistor of finite dimensions, the sensitivity increases with increasing cantilever width, whereas the cantilever length has little effect on the sensitivity. Reducing the cantilever thickness increases the sensitivity until a maximum is reached when the cantilever thickness is about one and a half times the piezoresistor thickness.

2.3 Modeling of the Cantilever Electrical Behavior

This section discusses the methods used to predict electrical properties of microcantilever sensors, so that fabrication parameters can be chosen accordingly. An

introduction to the simulation of doping processes is followed by a discussion of the device resistance from its geometry and sheet resistance.

2.3.1 Simulation of Ion Implantation

The calculation of resistivity resulting from an ion implantation process for heated and piezoresistive microcantilevers has been discussed in detail in [16] and [17]. Therefore, only the basic concepts and only the implantation with boron atoms to create p-type regions will be addressed in this section. There are two possible processes to bring foreign atoms into silicon, diffusion from a solid or gaseous dopant source and ion implantation. The latter is usually preferred for piezoresistive areas, which should have a relatively sharply defined zone within the thickness direction of the silicon to increase sensitivity. This is not possible to achieve with a pure diffusion process since the dopant profile will always be half-Gaussian with a maximum at the surface. Ion implantation is done by ionizing the dopant atoms and accelerating them toward the silicon substrate. In this case, the dopants also form a Gaussian distribution along the cantilever thickness direction. However, by choosing the acceleration energy of the ions, the maximum of the distribution curve can be placed anywhere within the thickness direction, thus adding an additional degree of freedom to the process. The depth-dependent Gaussian dopant profile after ion implantation is given by

$$N_i(z) = \frac{Q_i}{\sqrt{2\pi}\Delta R_p} \cdot e^{-\frac{1}{2}\left(\frac{z-R_p}{\Delta R_p}\right)^2} \tag{2.20}$$

where N_i is the concentration of implanted atoms, Q_i is the total implanted dose and R_p and ΔR_p are the average implantation depth and its average variation, respectively.

The latter two parameters are functions of the acceleration energy, the ion mass and the stopping power of the substrate material. When the ions are accelerated perpendicular to the crystal lattice, channeling effects can occur that make equation (2.20) invalid. Therefore, a tilt angle of usually 7° between the incoming ions and the wafer surface is chosen to prevent channeling. After the ion implantation, the substrate needs to be heated to a high temperature, usually about 1000 °C, to heal crystal defects that were caused by the highly energetic boron ions. This anneal step can also be used to reshape the initially Gaussian distribution curve to a more favorable distribution by diffusing the implanted atoms according to Fick's second law

$$\frac{\partial N_i}{\partial t} = \frac{\partial}{\partial z}\left(D \frac{\partial N_i}{\partial z} \right) \tag{2.21}$$

where D is the diffusivity of boron in silicon, which depends strongly on temperature. Since the diffusivity is also a function of the dopant concentration, the final dopant profile can only be calculated numerically. The software SSUPREM3 by Silvaco Corp. can simulate this diffusion process as well as the prior ion implantation and has all necessary physical properties already built in. The input parameters are substrate type and thickness, intrinsic dopant type and concentration, ion implantation energy, dose and tilt angle, and thermal anneal temperature, anneal time and temperature ramp rate. Furthermore, a dielectric layer, e.g. silicon dioxide, can be simulated on the substrate, a step which is usually built into real processes to prevent dopant diffusion out of the surface. The output parameters of the simulation run are the final distributions of the intrinsic and the implanted species as well as the net dopant distribution. Furthermore, the resistivity as a function of depth is automatically calculated from the distribution profiles by

$$\rho(z) = \frac{1}{e\left(n(z)\mu_e + p(z)\mu_p\right)} \tag{2.22}$$

where e is the elementary charge, n is the number density of free electrons caused by donor atoms, e.g. intrinsic phosphorous, p is the number density of electron holes caused by acceptor atoms, e.g. implanted boron, and μ_e and μ_p are the mobilities of electrons and holes, respectively. Finally, the software calculates the sheet resistance as defined in section 2.1.3 by integrating the resistivity over the thickness.

2.3.2 Calculation of Device Resistance

When the sheet resistance is known the total resistance of a device can be calculated by multiplying with a factor for the geometry, as given in equation (2.10). In the case of a straight, rectangular resistor, this factor is the ratio of resistor length and width. For more complicated geometries an approximation for this ratio can be made or it can be calculated numerically, e.g. by using FEM. Figure 2.11a shows an exemplary piezoresistive element. Length and width of an approximately equivalent rectangular element are denoted by L and W, respectively. Figure 2.11b shows the FE mesh of a two-dimensional, electrical simulation. A voltage difference is applied at the appropriate faces and the elements are given an arbitrary sheet resistance $R_\square$. The resulting current density in the resistor is shown in Figure 2.11c and hotspots can be seen at concave corners. The equivalent length to width ratio of the device is calculated from the total dissipated power P_{diss}, which is gained from the current density for a given applied voltage V, by

$$\frac{L}{W} = \frac{R}{R_\square} = \frac{V/I}{R_\square} = \frac{V^2/P_{diss}}{R_\square} \tag{2.23}$$

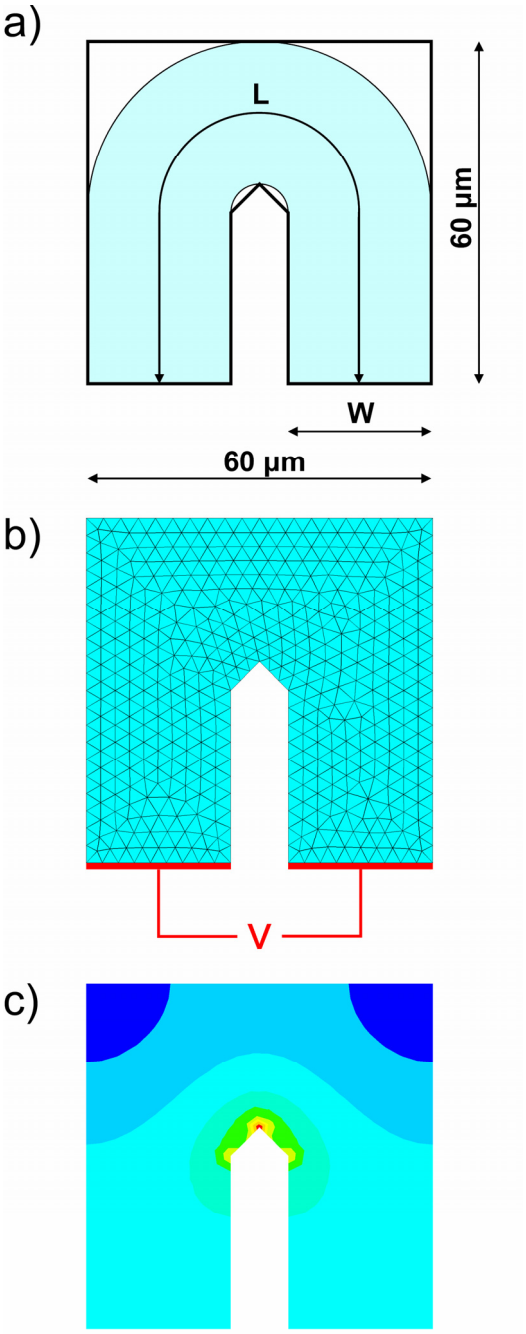


Figure 2.11 Calculation of the equivalent length to width ratio of a resistor by a) geometrical considerations and b) FE method; c) current density calculated from the system shown in b)

For the given piezoresistor geometry, the geometrical approximation yields an equivalent length-to-width ratio of 4.285 which is very close to the numerically calculated value of 4.030. For more complex geometries, the deviation between the two methods could be much higher with the numerical solution always converging to the real

solution with increasing mesh density. If the intrinsic silicon cannot be viewed as insulating, but rather as a material with a high resistivity, the geometrical approximation is no longer valid and a different model must be chosen. The resistive element can be approximated by a resistor network as shown in Figure 2.12.

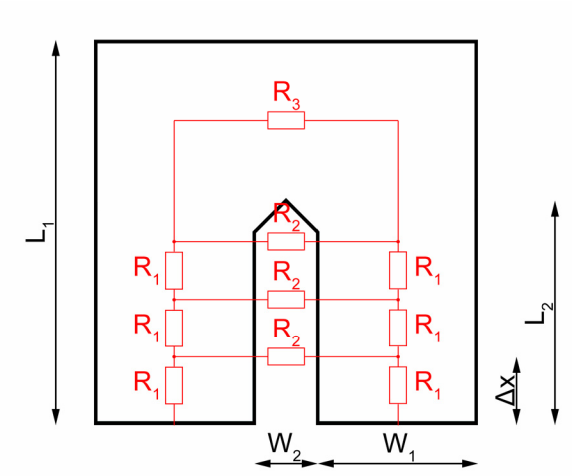


Figure 2.12 Schematic of the analytical model to calculate resistance if the intrinsic region is not insulating

The total resistance can be calculated by analyzing the network starting from resistor R_3 parallel to R_2, and adding $2R_1$ to the new value before setting that value parallel to another R_2 and so on:

$$R' = 2R_1 + \frac{R_3 \cdot R_2}{R_3 + R_2} \rightarrow R'' = 2R_1 + \frac{R' \cdot R_2}{R' + R_2} \rightarrow R''' = 2R_1 + \frac{R'' \cdot R_2}{R'' + R_2} \rightarrow \ldots \qquad (2.24)$$

The resistance values used in this expression can be calculated from geometrical approximations:

$$\begin{aligned} R_1 &= R_{\square 1} \cdot \frac{\Delta x}{W_1} \\ R_2 &= R_{\square 2} \cdot \frac{W_3}{\Delta x} \\ R_3 &\approx R_{\square 1} \cdot \frac{L_1 - L_2 + \frac{W_1 + W_2}{2}}{W_1} \end{aligned} \qquad (2.25)$$

The numerical calculation has to be performed $n = L_2/\Delta x$ times and the result converges to the real solution plus an error term caused by the approximation made for R_3 with decreasing Δx. The total resistance for this case can also be calculated from the FE model when the whole area is meshed and the elements in the intrinsic and the doped regions are given different sheet resistances.

2.4 Summary and Conclusion

In this chapter, basic concepts that are important to the understanding of microcantilevers for chemical sensing were introduced. An analytical model was shown to give good results for cantilevers with a point load at the free end, but to be insufficient to describe the behavior of microcantilevers with surface stress. It has been shown that the cantilever length has little effect on the output signal, but that the width has to be increased to optimize sensitivity. The ideal placement of the piezoresistor was found to be in the center of the cantilever's clamped end and the piezoresistor area should be minimized. In many cases, the piezoresistor thickness is constrained by the fabrication process. In this case, the cantilever thickness should be chosen so that the piezoresistor is about two thirds of the cantilever thickness. In contrast to the case of a cantilever with a point load at the free end, the sensitivity does not decrease dramatically when the piezoresistor thickness is close to the total thickness of the cantilever.

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CHAPTER 3

FABRICATION AND TESTING OF CHEMICAL SENSING CANTILEVERS

In this chapter, the development and testing of the first generation of chemical sensing microcantilevers is described. Six different cantilever designs are created based on the considerations from chapter 1. The detailed fabrication process for the devices is explained and results from basic electrical and mechanical testing are described. Tip deflection sensitivity experiments are performed and the results are compared to commercial cantilever devices. Finally, surface stress sensitivity is investigated by incorporating polymer coated cantilevers in a flow cell setup to detect gaseous analytes.

3.1 Design

The design of the first generation of chemical sensing cantilevers is based on the considerations in chapter 2. Six types of devices with different cantilever or piezoresistor geometries were designed to study the effect of these parameters on the sensitivity to surface stress. Schematics of these microcantilevers are shown in Figure 3.1. Dark areas in the figure indicate boron-doped and thus piezoresistive regions, and light areas indicate intrinsic and thus insulating or highly resistive regions. Type A is directly based on the results from chapter 2 with a low length to width ratio of one making it both highly sensitive to surface stress loading and compact. The piezoresistive element is placed in the center of the cantilever's clamped base, the region that has been found to have the

largest difference between stresses in length and width direction during chemical sensing, and therefore the highest resistance change. The piezoresistor length is chosen to be 60 μm in order to ensure that the majority of the piezoresistor is on the free-hanging part of the device even if the edge created by the backside etching process does not exactly line up with the intended edge position. Preliminary testing of the backside etching process showed that the non-uniformity over a sample substrate can be up to 15 μm. The effective piezoresistor length is between 35 and 60 μm because of the change in the current flow direction in this area due to the cross-connection of the two parts of the piezoresistive region as shown in Figure 3.1.

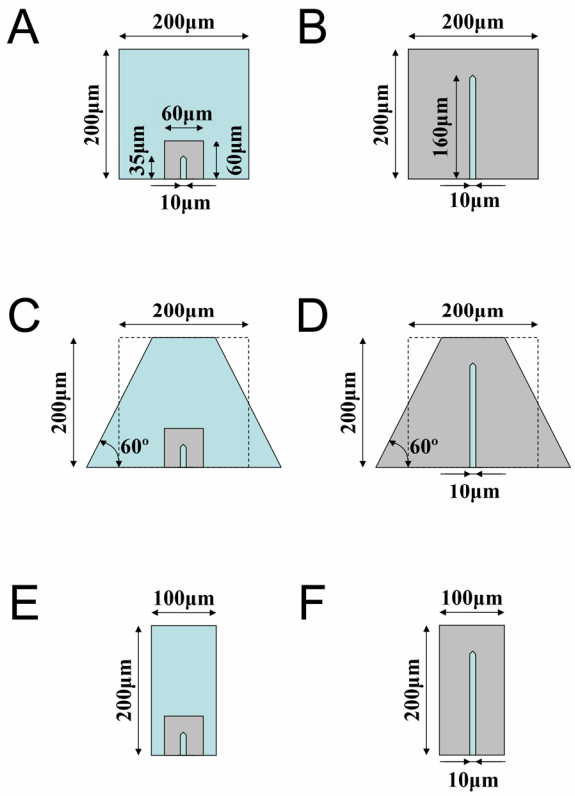

Figure 3.1 Schematic of geometry for six cantilever types; dark areas are doped silicon for piezoresistors and light areas are undoped, intrinsic silicon

Since in chapter 2 it was found that the width of the clamped cantilever base is an important parameter for the sensitivity, device type C is designed to increase this width while keeping the surface area the same as for type A. The resulting shape is a trapezoid with an angle of 60° between the base width and cantilever length directions. Cantilever type E is a more conventional design with a length to width ratio of two and same length as types A and C. The placement of the piezoresistors for device types C and E is the same as for type A. Device types B, D, and F have the same outer geometries as types A, C, and E, respectively, but are boron-doped on the whole area. They are designed to compare this design, which was found to be less favorable for the sensitivity in chapter 2, to the more optimized design of types A, C, and E with the piezoresistor at the center of the clamped base.

3.2 Fabrication

The fabrication process of the chemical sensing cantilevers is based on the fabrication process for heated microcantilevers developed by Tanya Wright during her graduate studies at Georgia Tech [1]. The general process flow is shown in Figure 3.2, a detailed process plan can be found in Appendix A. The starting substrate for the process is a standard Silicon-On-Insulator (SOI) wafer, 100 mm in diameter. A 1 μm thick layer of buried oxide (BOX) is sandwiched in between two layers of single crystalline silicon. The upper layer (device layer) is used to form the cantilevers and it is originally 2 μm thick. The bottom layer (handle layer) gives the wafer its structural stability and is 400 μm thick. The crystal orientation of the device layer is (100) and it is initially doped with phosphorous, an n-type dopant for silicon. This is done to ensure that the current traces,

which are made from p-type silicon, are well insulated from the bulk material by p-n-junctions. After the device layer is thinned down to the required thickness, the device outline is formed and the piezoresistive areas are created. A layer of silicon dioxide (SiO_2) is deposited and a high temperature treatment is performed. Through-holes (vias) are etched into the SiO_2-layer to electrically connect the piezoresistors to the subsequently deposited aluminum bond pads. The handle layer is locally etched away from the backside and the layer of buried oxide is dissolved to release the free hanging cantilever devices. These steps will be discussed in more detailed in the following sections.

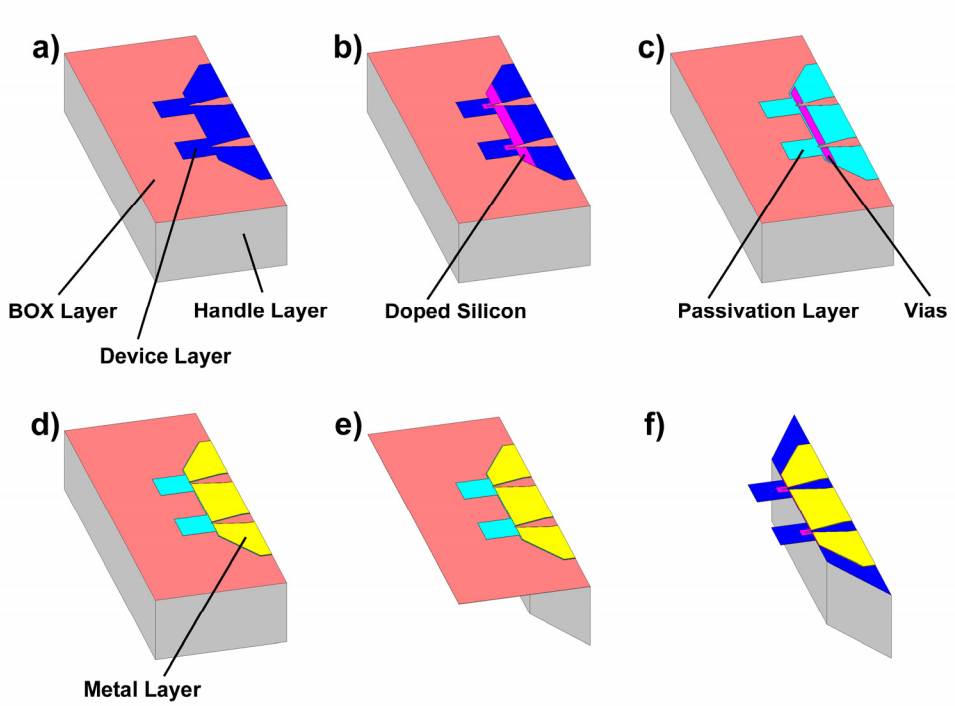

Figure 3.2 Schematic of the fabrication process; a) cantilever and metal pad outlines are etched into the device layer; b) piezoresistors are formed by boron implantation; c) oxide passivation layer is deposited and vias are opened in this layer to form electric connections between doped silicon and metal pads; d) metal is deposited in a liftoff process to form the bond pads; e) handle layer is selectively etched from the backside; f) for the final release, the buried oxide layer is removed

3.2.1 Creating the Cantilevers

The SOI wafers were purchased from Ultrasil Corp. The target thickness for the microcantilevers is 1 μm. Since wafers with 1 μm device layers are not available, wafers with 2 μm thick device layers were purchased and thinned down to the required thickness using a standard silicon etch process in a Plasma-Therm Corp. (PT) Inductively Coupled Plasma (ICP) machine. A Nanospec 3000 refractometer by Nanometrics Inc. was used to measure the device layer thickness before and after the etch steps. A two step process was employed in which the first step is used to determine the etch rate, which can vary depending on the machine condition and the second step is used to get to the required final thickness.

After adjusting the device layer to the required thickness the cantilever outline is formed in this layer using a Bosch process [2] in the PT ICP. This process was developed by researchers at Bosch GmbH, and allows for the creation of deep trenches with very high aspect ratios, i.e. the ratio of trench depth to trench width. In the PT ICP, the process consists of three steps, a step to deposit polymer as sidewall protection, a step to etch the polymer at the trench bottom and a step to deepen the trench by etching silicon. The ratio of process times for these steps as well as the processing gases and plasma power levels are crucial and need to be optimized to achieve straight sidewalls. The etch mask for the Bosch process is made with a standard photolithography process using Shipley 1827 positive-tone photoresist.

3.2.2 Creating the Piezoresistors

After the beam structures have been formed the wafers are cleaned and patterned again with the same type of photoresist for the ion implantation process that creates the piezoresistive areas and their connections to the metal. The implantation of boron atoms, which act as p-type dopants in silicon, is done at Core Systems Inc. The doping and subsequent rapid thermal anneal processes are simulated using SSUPREM3 software in combination with DeckBuild, both of which by Silvaco International. The target cantilever resistance on the order of 1-4 kΩ and the given length to width ratios of about 4.0 to 8.3 dictate that the square resistance of the doped silicon has to be between 250 and 480 Ω/□. Since lower doped, higher resistive silicon shows better piezoresistive behavior, as low a dopant concentration as possible that still fulfills the design requirements for total device resistance is chosen. The doping depth was chosen to be around 300 nm, which is about one third of the cantilever thickness.

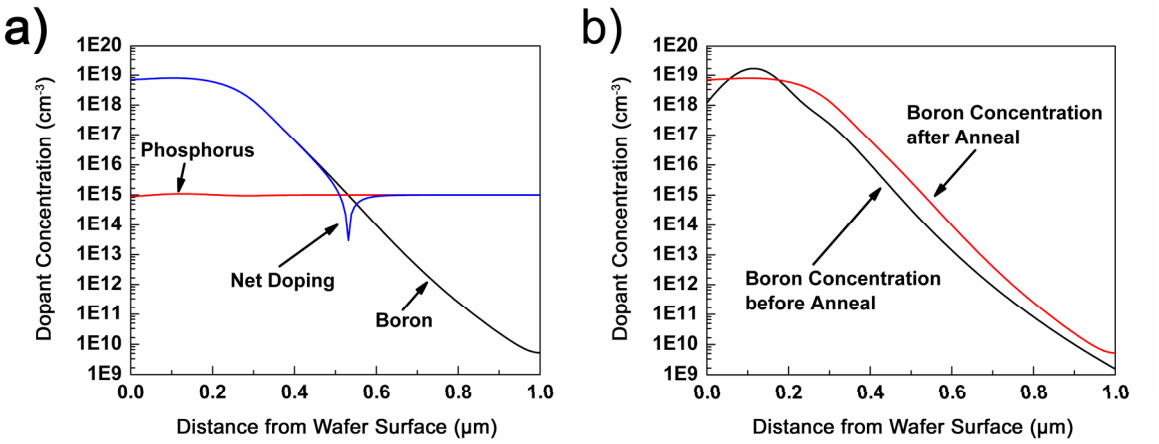

Figure 3.3 Dopant concentrations from ssuprem3 simulations vs. distance from cantilever surface; a) concentration of the intrinsic phosphorus, the implanted boron, and the net doping after anneal; b) concentration of implanted boron before and after anneal

The optimized doping process consists of an ion implantation step at a dosage of $2 \cdot 10^{14} cm^{-2}$ and a subsequent heat treatment step. The heat treatment is done in an AET addax rapid thermal processing (RTP) tool at 1000 °C for 20 minutes. Its purpose is to cure defects in the silicon lattice caused by the ion bombardment and to smoothen out the dopant profile within the doped region of the cantilever thickness as shown in Figure 3.3b. Between the ion implantation step with subsequent removal of the photoresist mask and the heat treatment, a 200 nm thick layer of silicon dioxide is deposited in a plasma enhanced chemical vapor deposition process (PECVD), which is used to insulate the silicon layer from the metal layer and to keep the dopants from diffusing out of the cantilever surface during high temperature steps. Figure 3.3a shows the resulting concentrations of boron and phosphorus and the net dopant concentration after the optimized implantation process.

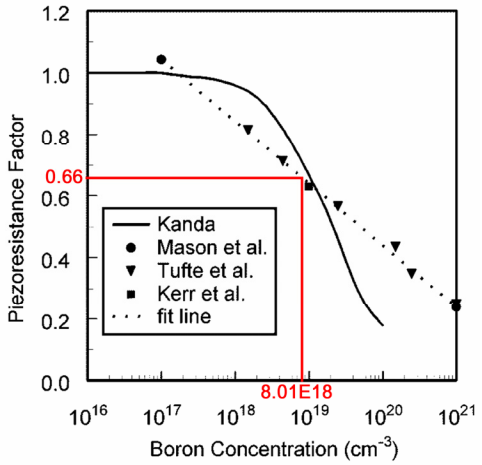

Figure 3.4 Normalized piezoresistance of boron-doped silicon vs. dopant concentration

The chosen process results in a maximum dopant concentration of $8.01 \cdot 10^{18} cm^{-3}$, a level at which the piezoresistivity is still at 66 % of its maximum value according to experimental data from Mason [3], Tufte [4], and Kerr [5] and shown in Figure 3.4 [6]. As discussed earlier in this section, the square resistance resulting from this process is

close to the upper limit of the allowable region for the design criteria and has a value of 457 Ω/□ according to the results of the simulation.

3.2.3 Creating the Bond Pads

After the implantation of the dopants into the silicon and the following heat treatment, the electrical connections that enable interfacing the cantilever sensors to external circuitry are created.

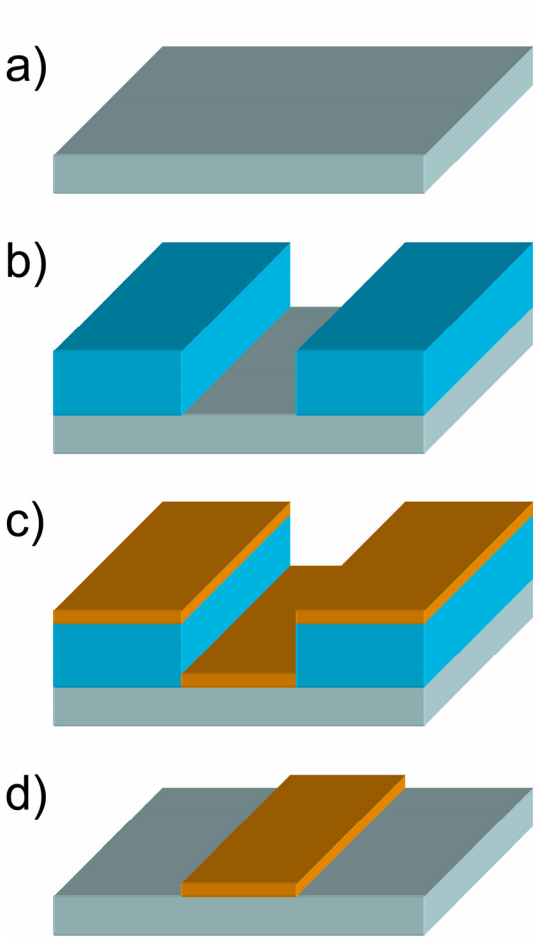

Figure 3.5 Schematic of the liftoff process for metal patterning; a) cleaning and dehydration of the silicon substrate; b) photoresist spin-on and patterning; c) evaporative deposition of aluminum film; d) removal of photoresist takes away aluminum in unwanted areas and leaves the desired aluminum structures

The main reason to choose aluminum for this purpose is that aluminum, like boron, is a p-type dopant in silicon, i.e. an element with a valency of three (trivalent). In this case, the semiconductor does not need a high-doped region to make good ohmic contact with the metal [7], and thus saves the high cost for an additional high energy ion implantation process. Other advantages of aluminum as the contact metal are its ability to be easily deposited with good adhesion, and its stability at process temperatures up to 400 °C. In comparison, gold, which is also a suitable candidate for electrical connections to the doped silicon regions, forms an unstable, purple alloy with silicon at these temperatures and is therefore not well-suited for applications with any subsequent process steps at elevated temperatures. Before the metal can be deposited, the silicon dioxide on the silicon device layer has to be removed locally to allow the metal to come into direct contact with the doped silicon. For this purpose, Shipley 1827 photoresist is patterned on the wafer leaving only the vias, small areas on the substrate close to the cantilever base, exposed. In these openings, the silicon dioxide is then removed with a selective etching process in the PT ICP. Afterwards, the metallization is performed in a lift-off process (see Figure 3.5), in which photoresist is patterned on the wafer in such a way that the areas, where the metal is supposed to remain on the substrate, are exposed. The wafer is then transferred into an electron beam evaporator by CVC Products Inc. that deposits an 800 nm thick layer of aluminum on both the exposed silicon and the photoresist covered areas. Right before the metallization, the wafer is dipped into buffered oxide etch (BOE) for about 10 seconds to remove any native oxide layer that may have formed since the vias have been created. After the metal deposition process, the wafer is moved into a bath of photoresist remover, which takes away the aluminum

covered photoresist and leaves only the desired metal patterns that contact the silicon at the vias on one side and have a large surface area to connect external electronics on the other side. After the metal deposition a heat treatment at 400 °C is performed to enhance the interdiffusion of the doped silicon with the aluminum to achieve good ohmic contact. This so called sintering step is done in a forming gas environment, i.e. a mixture of nitrogen gas with about 2% hydrogen, which has shown to be advantageous for the contact forming.

3.2.4 Final Device Release

The final process steps involve the separation of the cantilever from the substrate to achieve a free hanging device that can be used for chemical sensing. In the first of these steps, the handle layer is etched through from the backside with the same Bosch process as discussed in section 3.2.1. Since the uniformity of this process is not very good across a 100 mm wafer, the final device yield is improved by cleaving the wafer into four quadrants using a diamond scriber and etching each quadrant individually. The small pieces are mounted on carrier wafers that are previously spin-coated with photoresist for adhesion and to protect the carrier wafer during the etch process. Since 400 µm of silicon need to be etched and the selectivity of silicon to photoresist is about 40, a relatively thick layer of at least 10 µm of photoresist is needed for the etch mask. The negative-tone photoresist NR5-8000 by Futurrex Inc. is used for this purpose as the resulting film thickness when spin-coated at 1000 rpm is about 12.5-14.5 µm.

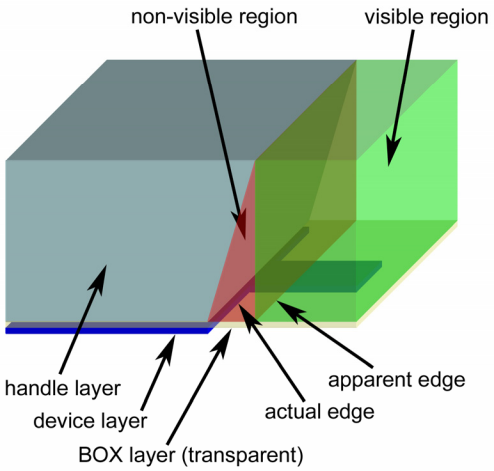

Figure 3.6 Schematic of trench inspection during backside etch process; the actual edge of the trench is not visible, so that the progress can not be determined unless the wafer is tilted

It has also been found that negative-tone resist is more stable during the plasma processing in the ICP and is therefore preferable to positive-tone resist. The lithography process is done by back side alignment, i.e. aligning the photomask on the backside of the wafer to the existing patterns on the front side. The etch rate is monitored by measuring the trench depth after every 150 cycles with an optical microscope, and it is found to be approximately 0.65 μm/cycle. When the trench depth indicates that the handle layer is almost completely etched through, the number of cycles per process run is reduced and the sample is optically inspected after each run. Since the process always results in sidewalls that are not completely straight but slanted to some extend, especially after the BOX layer has been reached in some areas of the trench but not in others, the sample needs to be angled under the microscope to see the actual edge of the etch trench as shown in Figure 3.6.

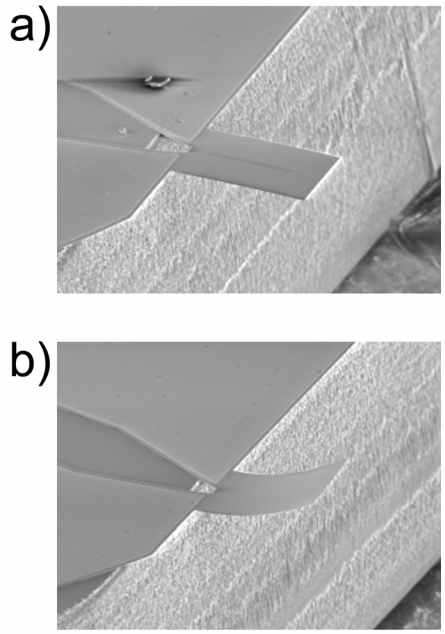

Figure 3.7 SEM images of a) a flat cantilever, where the BOX layer was completely removed and b) a cantilever bent by SiO_2-residue with intrinsic compressive stress under the cantilever

It is critical to terminate the etch process at the right time in order to achieve devices with no under- or over-etch because either of those could potentially have a negative effect on the sensitivity of the device during chemical sensing. When the backside through-wafer etch is finished the sample is transferred into a bath of photoresist remover until it detaches from the carrier wafer and all of the photoresist is dissolved from either side. The final step to release the free-hanging devices is the removal of the BOX layer in 49% concentrated hydrofluoric acid (HF). HF is preferred over other SiO_2-etchants including buffered oxide etch (BOE) because its selectivity to aluminum is better, so that the BOX-layer can be removed with less damage to the conductive paths. However, even HF will attack the aluminum patterns at a fairly high rate. Therefore, it is critical to remove the sample from the etch bath and flush it in a bath of de-ionized (DI) water as soon as all of the SiO_2 is removed. On the other hand, it is

also critical to make sure that no SiO_2-residues are remaining under the cantilever, because the intrinsic compressive stresses of the SiO_2 can cause the device to curl upwards as shown in Figure 3.7b. It is important to note that the SiO_2 under the cantilever, which is not visible under the optical microscope, is removed at a slower rate than that around the cantilever, so that visual inspection might be misleading. After the HF dip, the sample is thoroughly rinsed in DI water and dried on a hotplate before the single devices can be individualized by breaking the silicon arms that attach them to the sample.

3.2.5 Primary Packaging

To incorporate the individualized cantilever chips into a flow cell setup that allows their exposure to gases at controlled environmental conditions, the devices are mounted on a 24-pin dual-inline-package (DIP) sample holder as shown in Figure 3.8. These chip carriers of type "HYB02401" by Spectrum Semiconductors Inc. allow for fast and easy connection to existing electrical circuitry. Furthermore, the flat outer ring of the ceramic module is well-suited to be sealed off with a flow cell that attaches on top of it. This setup was designed for devices that are used for chemical analysis at Lawrence Livermore National Labs (LLNL). The chips are placed in close proximity to each other in order to expose them to identical environmental conditions during chemical testing.

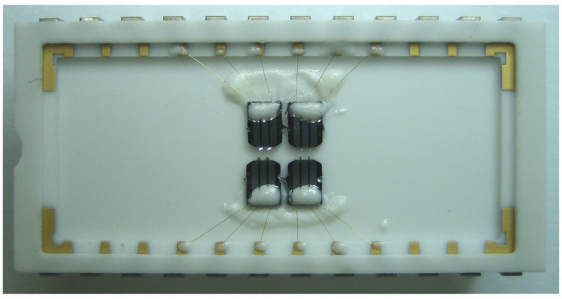

Figure 3.8 Set of four cantilever chips mounted on and wire-bonded to a 24-pin DIP package; special adhesive with low outgassing is used to attach the device chips and protect the wire-bonds on each side

The attachment of the sensing devices to the substrate as well as the protection of the bonding sites on the metal pads of the DIP and the cantilever chip are made with "Torr Seal" adhesive by Varian Vacuum Technologies, which is specially designed to produce low outgassing, so that the chemical measurements are not distorted by it.

3.3 Basic Testing of Devices

Figure 3.9 shows scanning electron microscope (SEM) images of the six types of cantilevers, whose design and fabrication were discussed in sections 3.1 and 3.2, respectively. Colored areas are overlaid to highlight the piezoresistive regions on each device. In the following sections, the methods and results of basic electrical, geometrical and mechanical testing are described.

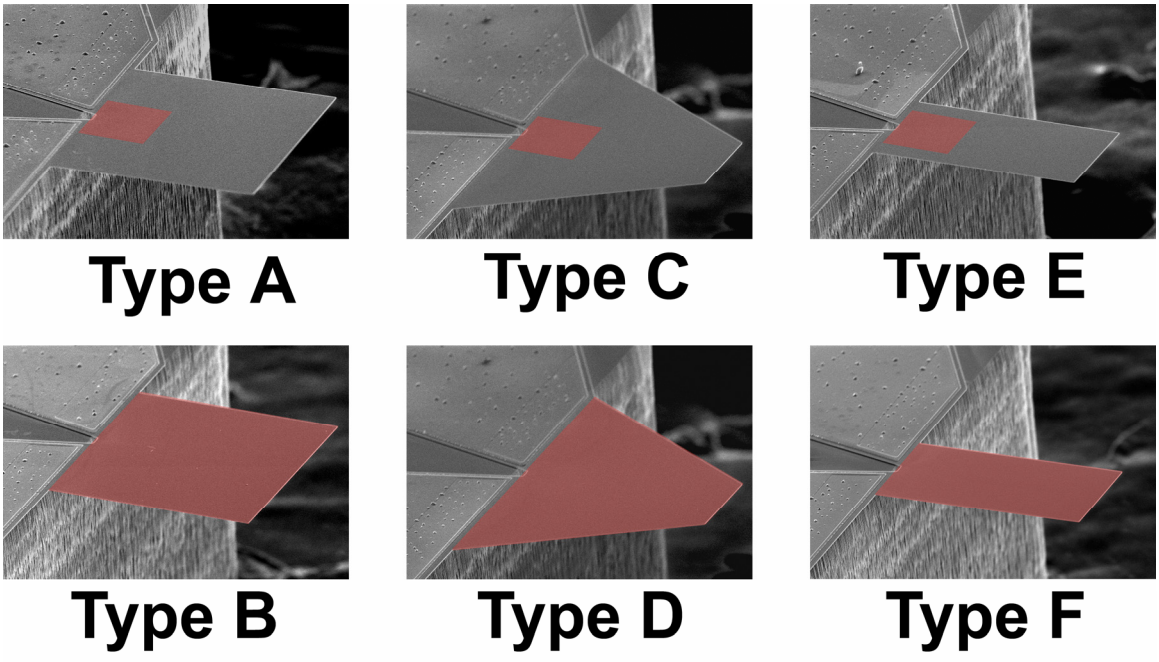

Figure 3.9 SEM images of six types of cantilevers; colored areas are overlaid to show the piezoresistive areas of the devices

3.3.1 Electrical Properties

In order to use the piezoresistive cantilevers for sensing applications, it is important to thoroughly characterize their electrical properties. For this purpose, a sense resistor is connected in series with the piezoresistor and a voltage is applied across the system. From the ratio of voltage drop across the sense resistor to the total voltage and the knowledge of the current in the circuit, the cantilever voltage, resistance and power can be calculated. Figure 3.10a shows the typical behavior of cantilever resistance vs. voltage applied to the device. It can be seen that the resistance is nearly constant at low cantilever voltages since the joule heating does not increase the device temperature significantly. As the voltage is increased, the cantilever resistance also increases due to the positive temperature coefficient of resistance (TCR) at lower temperatures. Once the voltage gets to a critical point the resistance drops suddenly. This is the well-known thermal runaway point of doped silicon, the temperature at which the intrinsic carriers

start to dominate over the current carriers from the dopants for the electrical conduction and the resistance therefore experiences a sharp decrease [8]. In Figure 3.10a, it can be seen that the electrical behavior for the two cantilevers on one chip is very similar, which enables the usage of one of the cantilevers as a reference device to cancel out parasitic effects during chemical sensing. Those effects can include surface stresses caused by surrounding media other than the analyte, as well as temperature and light fluctuations and external electromagnetic fields.

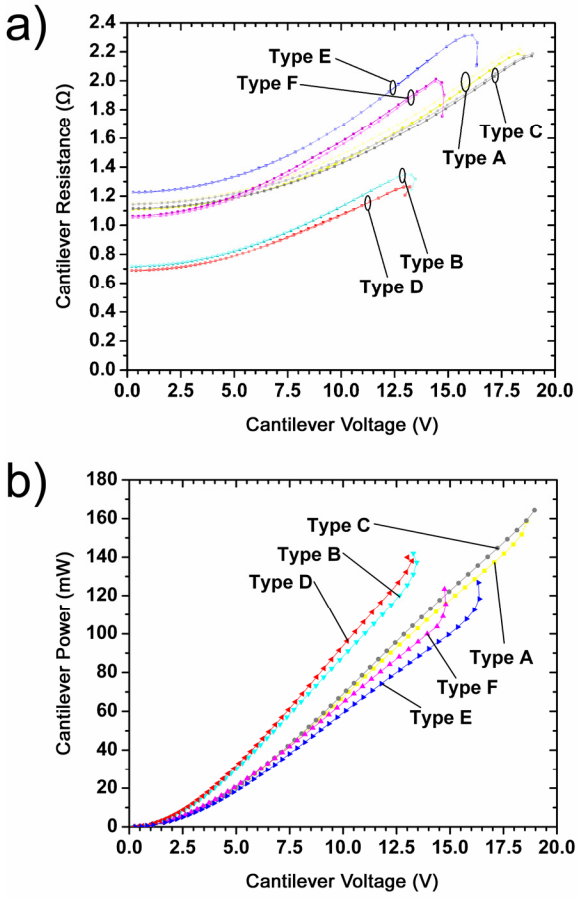

Figure 3.10 Electrical properties of six different types of cantilevers; similar colors indicate the left and right device on a single chip; a) cantilever resistance and b) cantilever power are plotted vs. cantilever voltage

Figure 3.10b shows the dissipated power in the cantilever device as a function of the cantilever voltage. The graphs show a strong increase at the thermal runaway point as the cantilever resistance drops and causes the current and power to increase sharply. This point can be regarded as the maximum power that can be dissipated in the device without experiencing thermal failure. It can be seen that those devices with piezoresistors close to the base and large surface areas (types A and C) are able to dissipate the most power. This is expected because the piezoresistor placement is close to the substrate, which acts as a heat sink while the large surface area acts as a fin for heat conduction into the surrounding air. Table 3-1 lists the measured low power resistance values for one device of each type. The equivalent length-to-width ratios for the piezoresistors calculated using FEM as described in section 2.3.2 is also given as well as the expected resistances calculated using the equivalent length-to-width ratios and the sheet resistance from the doping simulation.

Table 3-1 Equivalent piezoresistor length-to-width ratios, expected resistances and measured resistances for one device of six cantilever types

Cantilever	Equivalent L/W-ratio	Expected R (kΩ)	Measured R (kΩ)
A	4.0317	1.842	1.315
B	4.8613	2.222	0.854
C	4.0317	1.842	1.295
D	4.8701	2.226	0.797
E	4.0317	1.842	1.376
F	8.2939	3.790	1.262

It can be seen that in all cases the actual resistances are lower than the expected values. The resistances of types A, C, and E are very similar, which is expected because

the piezoresistive areas are equal. However, although types B and D have higher equivalent length-to-width ratios than types A, C, and E, their resistance values are significantly lower. Type F, which has an equivalent length-to-width ratio more than twice that of types A, C, and E, has roughly the same resistance as these types. These anomalies lead to the conclusion that the simple analytical model is not sufficient to predict the cantilever resistance. A possible reason for the lower than expected resistance values of types B, D, and F could be that the intrinsic silicon areas between the two sides of the piezoresistor are not completely insulating, but conductive with a high sheet resistance. To verify this hypothesis, the cross-connections of the cantilevers' piezoresistors were cut off using a wafer saw and the resistance was measured again. Optical microscope images and according resistance values of the cantilevers before (top row) and after (bottom row) the modification are shown in Figure 3.11.

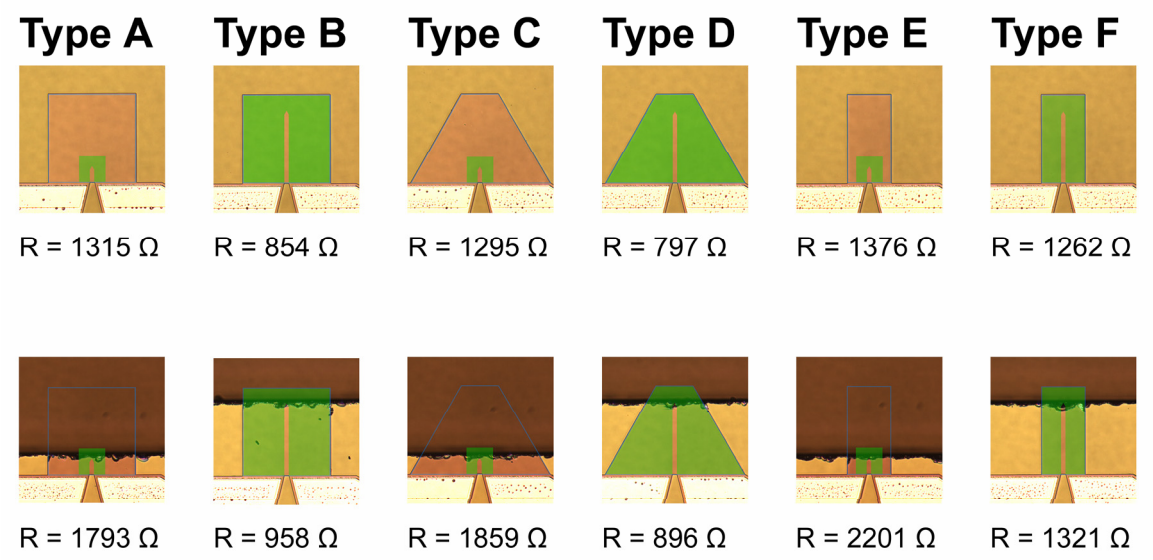

Figure 3.11 Optical microscope images of each cantilever type without backside etch of the handle layer and final release; blue cantilever outline and green piezoresistive areas overlaid for clarification; top row: unmodified devices, bottom row: cantilevers cut off to interrupt current path of piezoresistors

The cantilever outlines are overlaid in blue and the piezoresistive areas are overlaid in green for clarification. The simple analytical model predicts that this modification would completely insulate the two sides of the piezoresistor because it interrupts the current path. However, the measured resistance values after the modification did not go to infinity, but increased by only 5-60%. This indicates that there is indeed a finite amount of conduction through the intrinsic silicon between the two sides of the piezoresistor. The advanced analytical model as introduced in section 2.3.2 is used to gain a better understanding of the cantilevers' electrical properties. Table 3-2 compares the resistance values for all device types as predicted by the simple and the advanced analytical models.

Table 3-2 Comparison of simple analytical model and advanced analytical model to the measured resistances for six types before and after cutting off the cross-connection of the piezoresistor

Cantilever	Measured (kΩ)	Simple analytical model (kΩ)	Advanced analytical model (kΩ)
A	1.315	0.708	1.113
A, cut off	1.793	∞	3.092
B	0.854	0.854*	0.854*
B, cut off	0.958	∞	0.958*
C	1.295	0.708	1.113
C, cut off	1.859	∞	3.092
D	0.797	0.856	0.729
D, cut off	0.896	∞	0.871
E	1.376	0.708	1.113
E, cut off	2.201	∞	3.092
F	1.262	1.457	1.214
F, cut off	1.321	∞	1.278

*: values used to obtain fit parameters for sheet resistances

The sheet resistance for the boron-doped areas in the simple model is fitted from the resistance of the unmodified cantilever B, and the sheet resistances for the doped and the intrinsic areas in the advanced model are fitted from cantilever B before and after the modification. It can be seen that the advanced model yields more accurate predictions for the device resistance than the simple model. Furthermore, the fitted sheet resistance for the doped silicon of the advanced model (352 Ω/□) is much closer to the predicted sheet resistance from the doping simulation (457 Ω/□) than the fitted sheet resistance from the simple model (176 Ω/□). The fitted sheet resistance of the intrinsic silicon in the advanced model (9.65 kΩ/□) is also close to the range stated by the wafer manufacturer (10-100 kΩ/□). However, since the intrinsic silicon is n-type doped and the piezoresistors are p-type doped, the p-n-junctions should form diodes and thus insulate the piezoresistors from the intrinsic silicon. Although the advanced model cannot explain why these junctions are not effective and current leakage occurs, it can be used to predict the device resistance well.

3.3.2 Thickness Compliance

In chapter 2, it was shown that the device thickness affects the sensitivity of the microcantilevers to surface stress significantly. Therefore, in order to do comparative measurements between the different device types, it is necessary to determine the cantilever thickness accurately. This can be done by inspecting the cantilever cross-section in a SEM. Figure 3.12 shows SEM images of two cantilevers' cross-sections and the according thickness measurements.

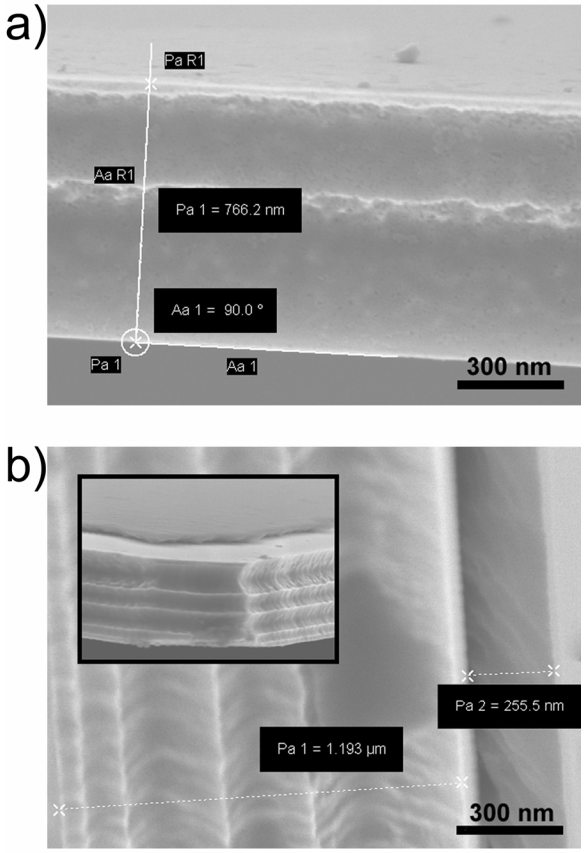

Figure 3.12 SEM images of cantilever cross sections a) without and b) with oxide layer; the inset in b) shows the corner of a cantilever with oxide layer (dark region on top)

The cantilever in Figure 3.12b has a 255.5 nm thick layer of silicon dioxide on one surface, which is a relict from an insufficient HF etch step as discussed in section 3.2.4. The silicon dioxide can clearly be seen as a black film in both the cross-sectional view and the inset, which shows the corner of the cantilever from an angle. Over 90% of the cantilevers measured with this method fall in the range between 700 and 1200 nm with the majority of them very close to the target thickness of 1 µm.

3.3.3 Mechanical Properties

The main application of the microcantilevers is static mode chemical sensing, i.e. the magnitude of the cantilever deflection is measured independent of time. However,

these devices can also be used for dynamic sensing if they are actuated externally and the shift in resonance frequency is measured. To maximize the signal, dynamic operation has to be performed close to one of the cantilever's resonant frequencies. The resonant frequencies can be obtained from the thermomechanical noise spectrum, which can be measured by interfacing the cantilever with a commercial AFM system. Figure 3.13 shows typical thermomechanical noise spectra for cantilever types A, C, and E.

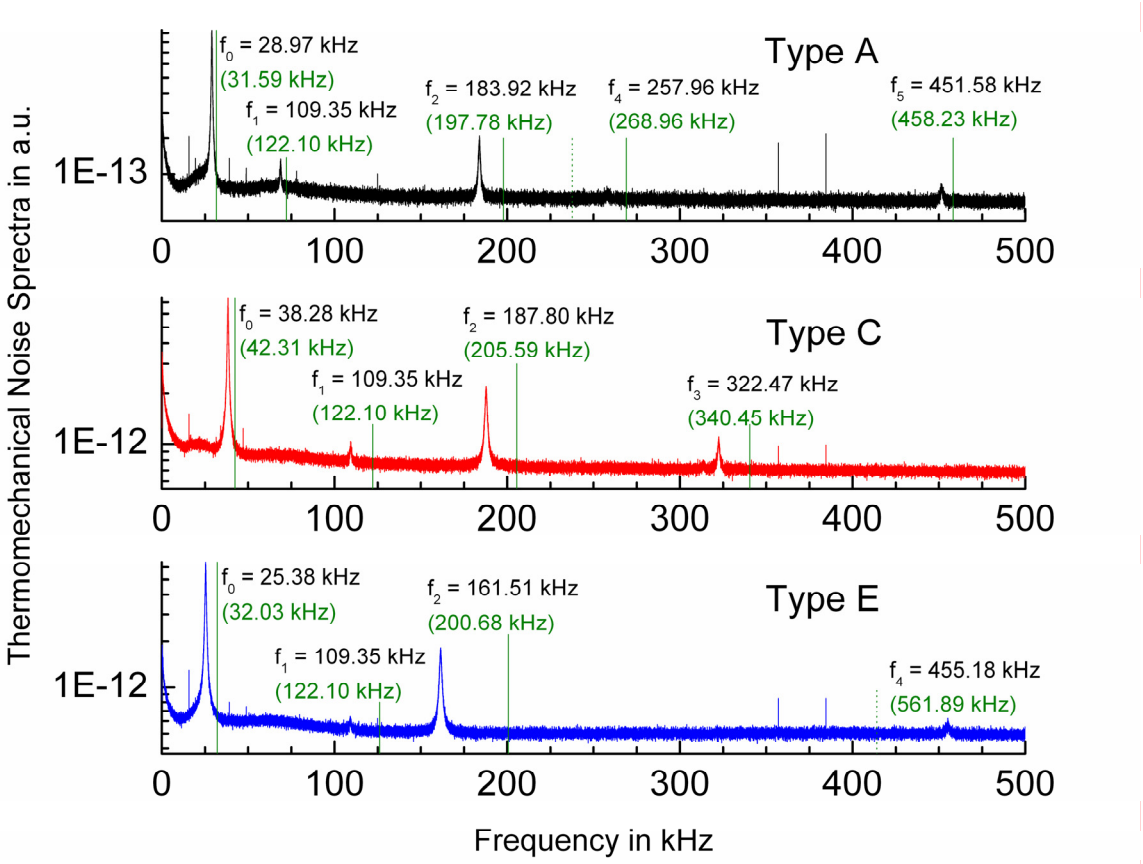

Figure 3.13 Thermomechanical noise spectra of three different cantilever types; black numbers indicate the measured resonance peaks of the devices and green numbers indicate the according calculated values from FEM

It can be seen that type C, which is the device with the widest base, has the highest 0^{th} resonant frequency and type E, which is the device with the narrowest base, has to lowest 0^{th} resonant frequency. The thicknesses of the devices were measured and used in the calculation of the resonance behavior with FEM, as shown by the green lines

and numbers in Figure 3.13. It can be seen that the FEM results consistently overestimate the actual values, which is expected to be caused by deviations of the cantilever's material properties from the values used in the simulations.

3.3.4 Deflection Sensitivity

In order to test the piezoresistance of the microcantilevers without actual chemical interaction, a setup to deflect the devices mechanically was designed as shown in Figure 3.14. The cantilever chip attached to the DIP carrier is mounted on a holder that can be positioned relative to a needle probe with micrometer screws.

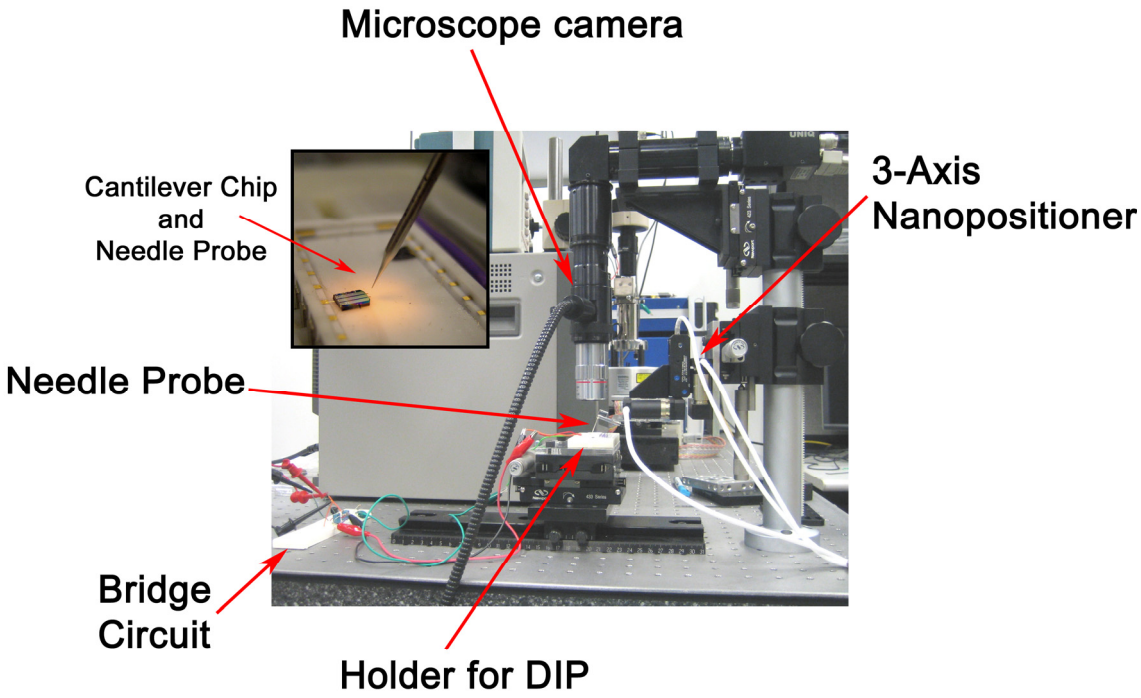

Figure 3.14 Photograph of setup for deflection sensitivity measurements of cantilever chips; the inset shows part of the DIP with attached cantilever chip, which is in close proximity to the needle probe

The needle probe is made of glass with high stiffness and has a small radius of curvature to position the force that is applied to the cantilever precisely in the center of the free end. The probe movement is controlled by a nanopositioner with nanometer

resolution made by Physik Instrumente GmbH. A charge coupled device (CCD) camera with attached 5x microscope objective lens is located above the needle probe to monitor the experiment. The resistance change of the cantilever's piezoresistor is measured with a Wheatstone bridge setup. The undeflected cantilever on the same chip is used in the same branch of the bridge as the tested device to cancel parasitic signals, e.g. the change in light intensity from the microscope lamp connected to the objective lens. The resulting resistance change is plotted vs. cantilever tip deflection in Figure 3.15 for one device of each type.

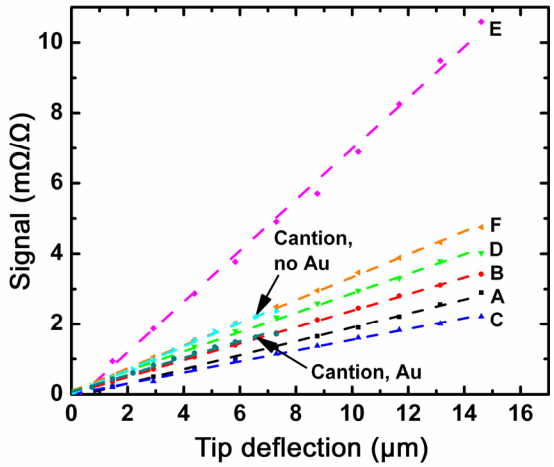

Figure 3.15 Resistance change vs. cantilever tip deflection for types A-F, for gold covered commercial device (Cantion, Au), and non-gold covered commercial device (Cantion, no Au)

The thicknesses of these devices were measured previous to the experiment and they are within 16% of each other. It is important to compare devices of similar thickness since thicker devices will show a higher signal for this experiment because their piezoresistors are located farther away from the neutral axis and because the input signal is the tip deflection rather than a point force at the free end. The measured sensitivity values are between 0.155 (type C) and 0.724 (type E) mΩ/Ω-μm. The deviation of type E from the other types is unreasonably high. Possible sources of error include long term

drift in the signal, which was not accounted for in this experiment and slight variations of the needle probe contact position on the cantilever. The sensitivity values for the fabricated devices are comparable to those of commercial devices by Cantion A/S. Four of these commercial devices with a gold layer on the top surface and four devices of the same type without gold layer were measured with the same setup. The average signal for each configuration is shown in Figure 3.15. The sensitivities for the gold covered and the non-gold covered devices are 0.239 and 0.336 mΩ/Ω-μm, respectively.

3.4 Surface Stress Testing

The main application of the cantilever devices is the static measurement of surface stresses due to chemical exposure on the cantilever surfaces. After the initial characterization, selected devices were sent to LLNL to be connected to a flow cell setup for chemical detection. One of the devices on each chip was covered with a polymer layer that is sensitive to a gaseous analyte as shown in Figure 3.16. An inert carrier gas is flown through the sealed flow cell and the analyte to be detected is mixed into the inert gas after an initial time step. After a certain exposure time to the chemical, the analyte flow is turned off. This cycle is repeated several times to investigate the repeatability of the process. Figure 3.17 shows the results from four such experiments with durations between 6000 and 14000 seconds and three to four analyte on/off cycles each. In each experiment three or four different cantilever types of comparable thickness were tested simultaneously. It can be seen that all types show significant responses to analyte exposure and that in most cases the effect is reversible. Comparing the magnitude of the different types' output signals with each other does not yield conclusive results. Some

types that show higher output signals in some cases show lower signals in others. Since the polymer layer gets removed and re-deposited in between the experimental runs, it is suspected that the layer thickness has an effect on the signal magnitude.

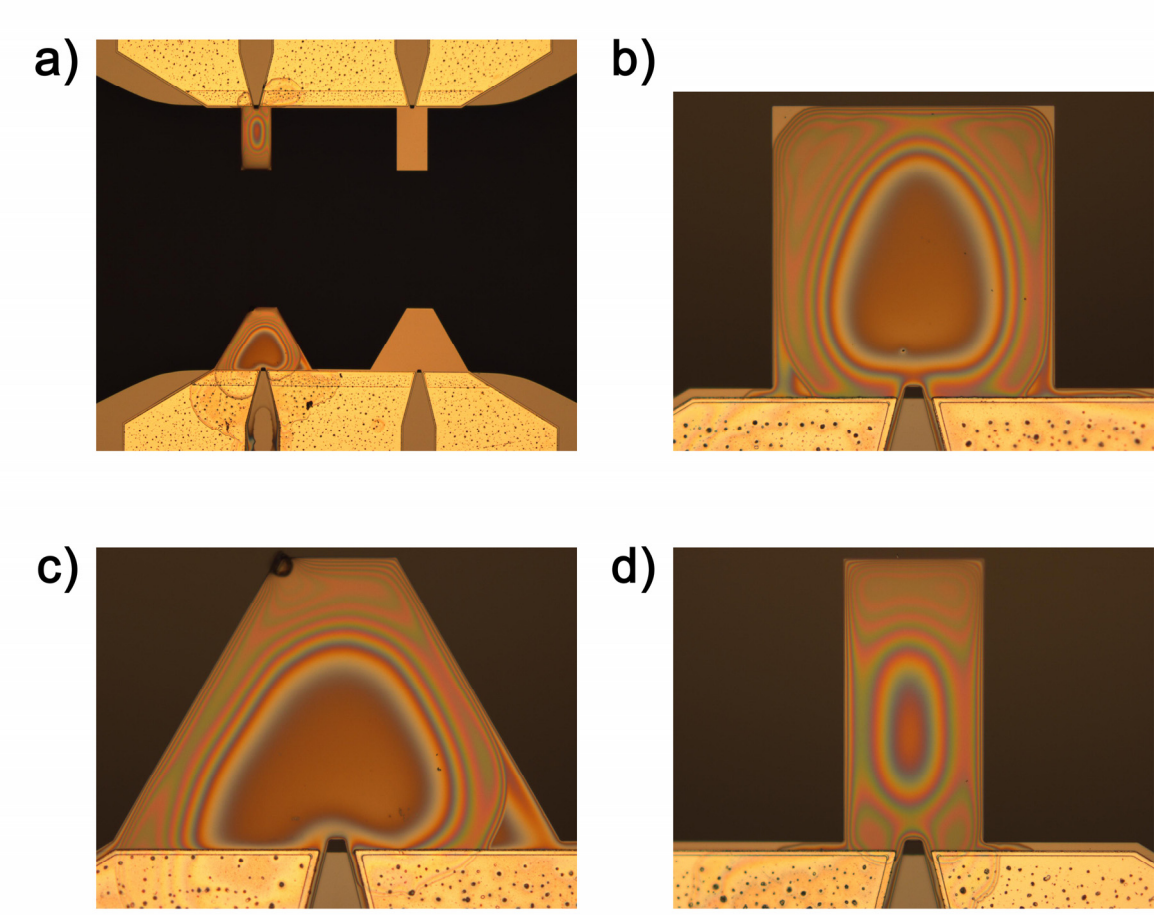

Figure 3.16 Polymer coated cantilevers for chemical testing; a) type A and C devices as they face each other in a flow cell for comparative measurements; b) coated type A cantilever; c) coated type C cantilever; d) coated type E cantilever

The time constants that govern the transition between steady states before and after changes in analyte flow are different for each type and experimental run. This indicates that the layers are indeed of different thickness as time constants of several tens or hundreds of seconds can only be caused by chemical processes in the system, e.g. diffusion in the polymer layer, and are several orders of magnitude longer than any mechanical, electrical, or thermal time constants of the microcantilevers themselves.

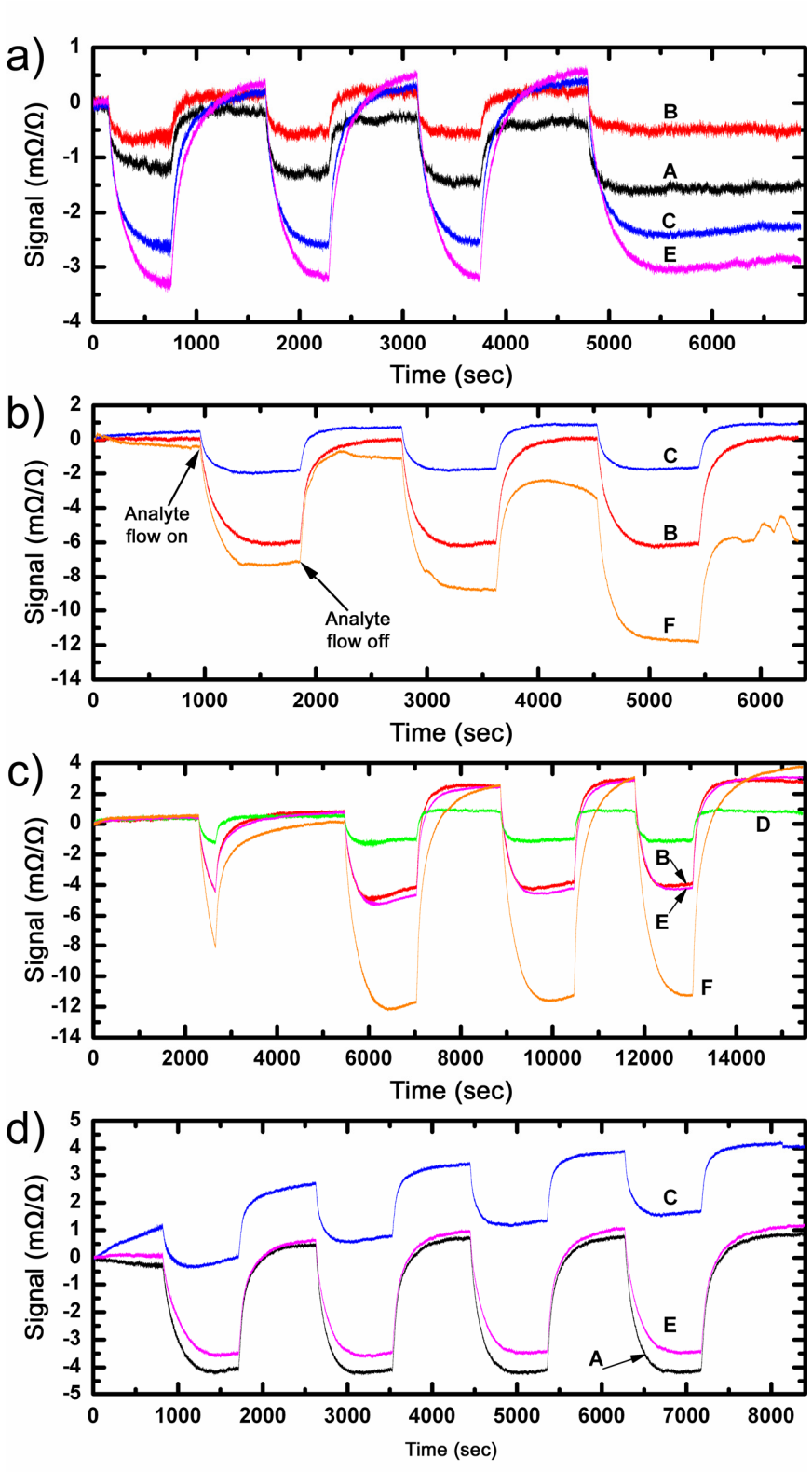

Figure 3.17 Output signals for four experimental runs with a set of three or four polymer covered cantilevers for chemical sensing; analyte flow is turned on and off several times during each experimental run

3.5 Summary and Conclusion

In this chapter, the fabrication and characterization methods for the first generation of chemical sensing cantilevers were described. The detailed fabrication process starting with SOI wafers and ending up with devices in primary housing ready to be connected to a flow cell setup were explained. It was shown that the assumption of insulating p-n-junctions between piezoresistors and intrinsic silicon is not valid and that an improved analytical model can predict the cantilever resistance more accurately. The typical thermal runaway behavior in the cantilever resistance due to the change in the type of dominant current carriers in doped silicon at elevated temperatures was obtained. The tip deflection sensitivity was measured with a custom setup and found to be comparable to that of commercial devices for all fabricated types. The incorporation of the microcantilevers into a flow cell setup at LLNL showed that they are suited for chemical detection. However, comparison between the device types was inconclusive for chemical detection, which is assumed to be attributed to variations in the analyte-sensitive polymer layer on the cantilevers

3.6 References

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CHAPTER 4

FABRICATION AND TESTING OF SECOND GENERATION CHEMICAL SENSING CANTILEVERS

The piezoresistive microcantilevers of the first generation are able to sense surface stresses that occur during chemical sensing. These stresses can, for example, be caused by the expansion of a polymer layer due to analyte exposure. The piezoresistive sensors are also known to be very sensitive to temperature changes. If it was possible to reduce this temperature sensitivity the field of potential sensing applications could be broadened significantly. One method to do this was already employed in the first generation devices by creating two identical microcantilevers on each chip. When both devices are connected into one branch of a Wheatstone bridge circuit, the influence of the testing environment on the signal output is greatly reduced.

However, for many applications a more sophisticated system is necessary. One example would be a testing environment, which is not in thermal equilibrium. In this case, the two cantilevers on one chip could be at significantly different temperatures and the resulting parasitic signal could be much greater than the measured signal from surface stress changes. Temperature deviations between the active cantilever and the reference device could also be caused by altered thermal properties due to the analyte-selective material on the cantilever surface, e.g. the mentioned polymer layer. In all of these cases, it would be desirable to have a temperature compensation scheme within the cantilever

itself, so that any variations outside the device could be filtered with high accuracy. The design and testing of such a system are one of the main objectives of this chapter.

The second emphasis lies on the implementation of heater structures into the microcantilever. Cantilever devices with the ability of independent heating and sensing operation that have a high sensitivity to surface stress could be used for a variety of sensor applications. A prominent example would be the calorimetry of thin material films on the cantilever surface. Chemical processes such as melting and evaporation and chemical reactions between substances could be triggered by the heaters while the changes in the surface stresses on the cantilever are monitored and can give information about the material or reaction properties. It is clear that the two aims of this chapter, integrated heating and temperature compensation of the mechanical signal, are closely related to each other for the mentioned types of applications.

4.1 Design

The design of the second generation microcantilevers for chemical sensing is based on the findings from the FEM in chapter 2 and the results of the first generation devices in chapter 3. Type A of the first generation devices showed good sensitivity to surfaces stress and its outer dimensions are therefore used for types A, C, and E of the second generation devices as shown in Figure 4.1. The length and width of these devices are 200 μm each, so that the resulting length-to-width ratio is one. To compare longer, narrower devices of equal surface area to these types, cantilevers B, D, and F have a length of 300 μm, a width of 133 μm and hence a length-to-width ratio of about 2.3.

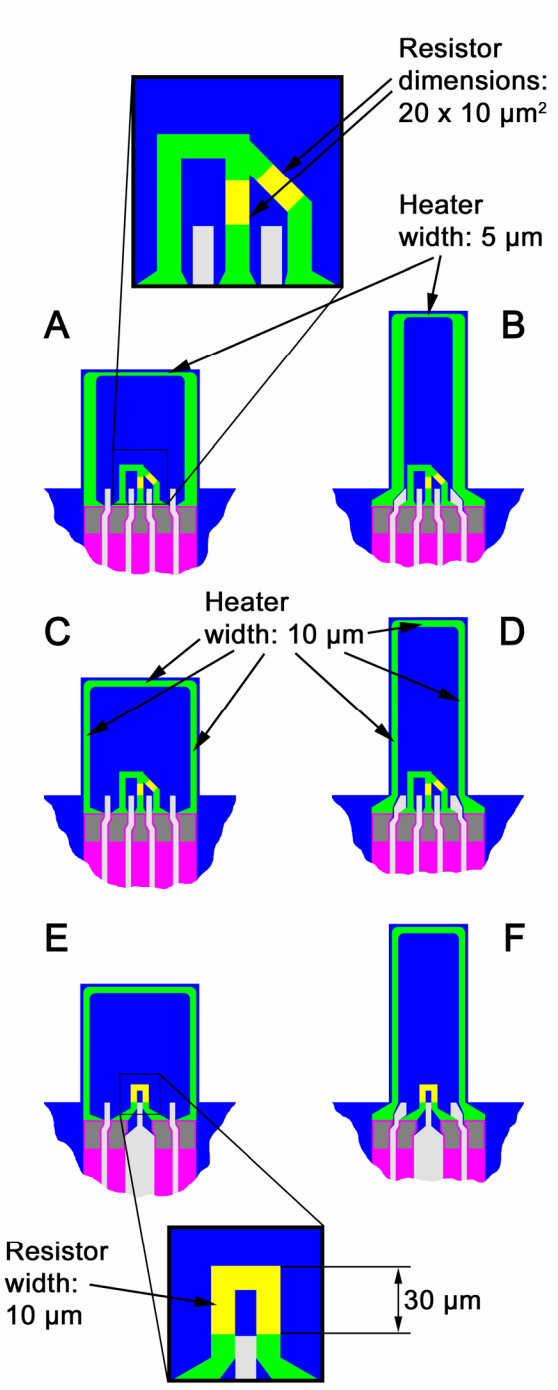

Figure 4.1 Schematic of six cantilever types of the second generation; blue areas are intrinsic silicon, green areas are high-doped silicon and yellow areas are low-doped silicon, aluminum lines are magenta and contact areas between doped silicon and aluminum are grey; upper detail shows resistor layout in types A through D and lower detail shows resistor layout in types E and F

One of the main differences to the first generation is the implementation of heater areas into the microcantilevers. These heaters are resistors made of doped silicon traces

and they are based on the joule heating from electrical current flowing through them. Two different heater geometries are implemented. Cantilever types A and B have wide current traces on the cantilever edges in length direction and a narrow path at the free end, thus concentrating the majority of the resistance and therefore also the largest portion of the heat generation at the free end. Types C-F have a current path of uniform width around the whole cantilever edge, thus creating homogeneous heat generation anywhere close to the edge.

In chapter 2, it was found that the ideal placement of the piezoresistors for surface stress sensing is close to the center of the clamped base. To maximize the sensitivity to surface stress the piezoresistor dimensions for the second generation are further decreased while keeping the position on the cantilever the same. Furthermore, in contrast to the first generation devices, the current flow direction of the piezoresistor is now aligned completely in the highly sensitive <110>-direction of the silicon device layer. A second resistor of equal dimensions is placed in close proximity to the piezoresistor, but with an angle of 45° to it, therefore aligning it to the <100>-crystal direction. The piezoresistive coefficients for p-type silicon in this direction are zero, so that the <100>-resistor should be insensitive to stresses in the cantilever, whereas the sensitivity of the <110>-resistor is maximized, as shown in Figure 4.2.

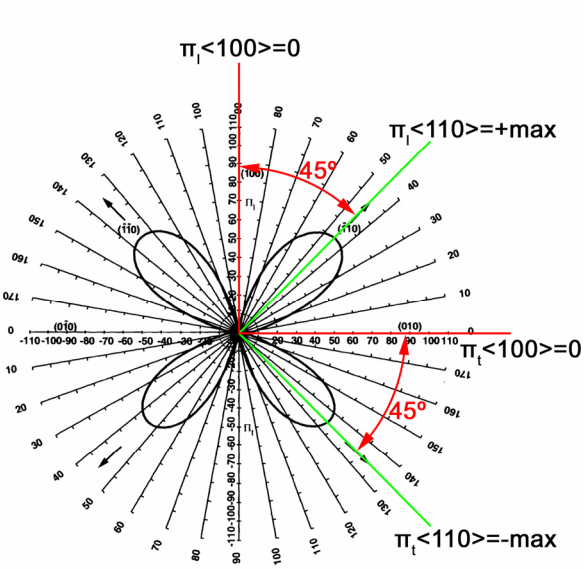

Figure 4.2 Longitudinal and transversal piezoresistive coefficients are zero in <100>-direction and their absolute values are maximized in <110>-direction; the two directions are at 45° to each other

Assuming that both resistors' responses to temperature changes are equal, their differential signal can be used to detect changes in the cantilever stress state due to tip deflection or surface stress loading independent of temperature changes. A similar concept has been demonstrated previously for an AFM cantilever with resistors in its two legs, which are angled at 45° to each other and provide effective temperature compensation [1]. To cancel the effect of temperature changes with the second generation devices the two resistors can be connected in one branch of a Wheatstone bridge and supplemented by two additional resistors. For chemical sensing, the other branch of the Wheatstone bridge can be formed by the resistors in the second cantilever on the same chip, thus cancelling effects that alter the surface stress other than those caused by the exposure to the analyte. Since the shape and placement of the resistors for the second generation devices are fixed by the preceding considerations, a different method to create the connecting current paths than used for the first generation devices needs to be employed. For this purpose, the electrical connections between the resistors and to the

bond pads are made with highly boron-doped silicon. There are several advantages to using high-doped silicon instead of using the same doping level as for the resistors or using a different electrically conductive material. The resistance of the current traces made of high doped silicon will be small compared to the resistance of the piezoresistors, which ensures a high ratio of resistance change to initial resistance during sensing operation, and thus a good sensitivity. The high doped silicon also has a reduced piezoresistive coefficient as shown in Figure 2.XXX, so that unwanted resistance change in the conductor areas is small. Furthermore, doping the silicon will have very little effect on the stress state inside the cantilever, whereas deposited layers might cause intrinsic stresses and lead to initial device deformation. Finally, the coefficients of thermal expansion (CTE) for intrinsic and doped silicon are expected to be very similar, so that changes in the cantilever stress state due to heating are minimized. The last requirement is impossible to achieve with most other electrically conductive materials that could otherwise be used to shape the current paths. The described arrangement of the piezoresistor and the additional resistor is used for cantilever types A-D.

Table 4-1 Implantation and heat treatment parameters and expected sheet resistances from doping simulations for high and low doped areas

		High doped areas	**Low doped areas**
Implantation dose	cm^{-2}	3e15	2e13
Implantation energy	keV	120	20
Anneal temperature	°C	1000	1000
Anneal time	min	60	30
Expected sheet resistance	Ω/□	32.85	2182

Types E and F have a single piezoresistive current path similar to the devices of the first generation for comparison of the new concept. A design requirement for the piezoresistor, the additional resistor and the heater is that the total resistance for each element is below 5 kΩ. Since the two resistors each have a length-to-width ratio of two, the sheet resistance of the low doped silicon has to be below 2.5 kΩ/□.

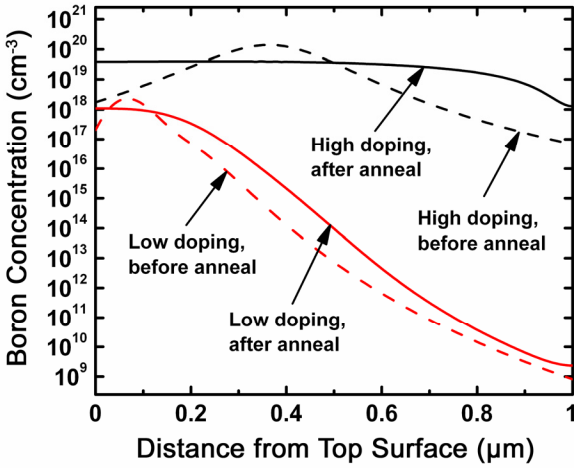

Figure 4.3 Simulation results of boron concentration for two different doping processes before and after the heat treatment step of each process

The heater traces could be made by the low doping process, the high doping process or a combination of the two. The approximated length-to-width ratios of the different cantilever types' heater paths is between 45 (type B) and 70 (type D). Since this is much higher than the ratio for the piezoresistor, it is clear that the heaters have to be formed by the high doping step. Since there is no design criterion for the minimum resistance, the sheet resistance of the high doped silicon should be much smaller than for the low doped areas. The sheet resistance for the low doped areas, on the other hand, should be high within the design criterion to maximize the piezoresistive coefficients as discussed in chapter 3. The implantation and heat treatment parameters for the two doping levels were simulated using SSUPREM3 and the optimized results are shown in

Table 4-1. It can be seen that the low doped areas have a sheet resistance almost two orders of magnitude higher than that of the high doped areas. The expected concentration distribution of the boron atoms is shown in Figure 4.3. It can be seen that the junction depth of the piezoresistor is about one third of the cantilever thickness. For the high doped areas that form the connecting traces of the piezoresistor and the additional resistor as well as the heater structures, the dopants are distributed more evenly to avoid current concentration in one layer.

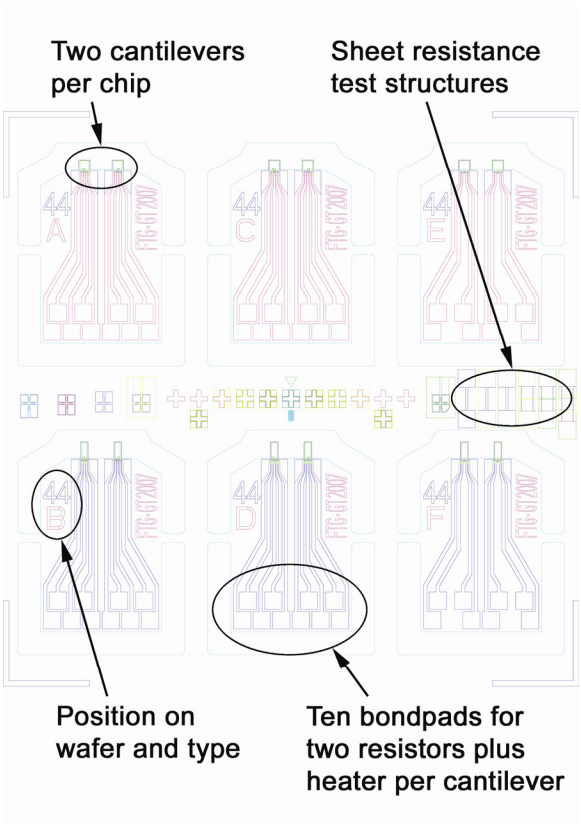

Figure 4.4 One of 69 unit cells on the mask set of the second generation microcantilever sensors with some important details

Figure 4.4 shows a compilation of the photomask layers for one unit cell of 1 cm square. Because of the added resistor and heater per cantilever, the number of bondpads is increased to 10 and in contrast to the first generation they are now aligned in two rows. For the second generation, there are a total of 69 unit cells per 100 mm wafer and each

device is numbered with a two-digit position number, which represents the row and column on the wafer. This is helpful when several measurements are to be made with the same device. It also helps in identifying devices from the same region on the wafer that are more likely to have similar properties, such as thickness. Another new feature in the mask design of the second generation is the implementation of test structures that are composed of traces of intrinsic, low doped, or high doped silicon or a combination of those. The test structures have metal pads so that they can be interfaces by wire-bonding and used to determine the sheet resistances of the materials as well as the interface resistances between them.

4.2 Fabrication

The fabrication process for the second generation chemical sensors is very similar to that of the first generation devices. Therefore, each process step will only be mentioned briefly and only the differences to the previous process will be discussed in more detail. The same SOI wafers as for the first generation were used to make the second generation devices. However, for the second generation, the device layer is not thinned down by etching the silicon directly in the PT ICP. Instead, silicon dioxide is thermally grown on the wafer surface and etched away with high selectivity. This process, which slowly and evenly consumes the silicon of the device layer, needs to be repeated several times while the remaining device layer thickness is monitored and the growth parameters are adjusted accordingly. This method takes much longer than etching the silicon directly, but the uniformity of the thermal oxide growth and removal across the wafer is expected to be superior to the etch uniformity in the ICP. After the thinning

of the device layer, the beam structures are patterned with photoresist and etched into the silicon with the Bosch etching process in the PT ICP. For this device generation, the doping process is more complex. The implantation at high energy and large dose, as given in Table 4-1, to create current traces and heaters is done first. Then, a 200 nm thick layer of silicon dioxide is deposited and the heat treatment is performed to anneal the silicon and to achieve a more uniform dopant distribution as shown in Figure 4.3. The heat treatment for this step is performed in the nitrogen atmosphere of a Lindberg furnace because the process time is too long for the RTP and the temperature ramp rate is not critical. After the high temperature step, the previously deposited silicon dioxide is removed in BOE to reveal the silicon for the second implantation step. To make sure that no silicon dioxide remains on the cantilevers, the BOX layer thickness is measured with the Nanospec before the oxide deposition and the etching is continued until this value has been reached again. Then, a new layer of photoresist is patterned with a different photomask that only reveals the two resistors per cantilever and covers all other areas. Ion implantation and heat treatment with the low doping parameters from Table 4-1 are performed in the same way as for the first generation devices. The vias that connect the doped silicon to the metal layer and the metal lines are also made with the same processing steps as for the previous device generation. The heat treatment to allow interdiffusion of doped silicon and aluminum is performed at 400 ºC in a forming gas environment.

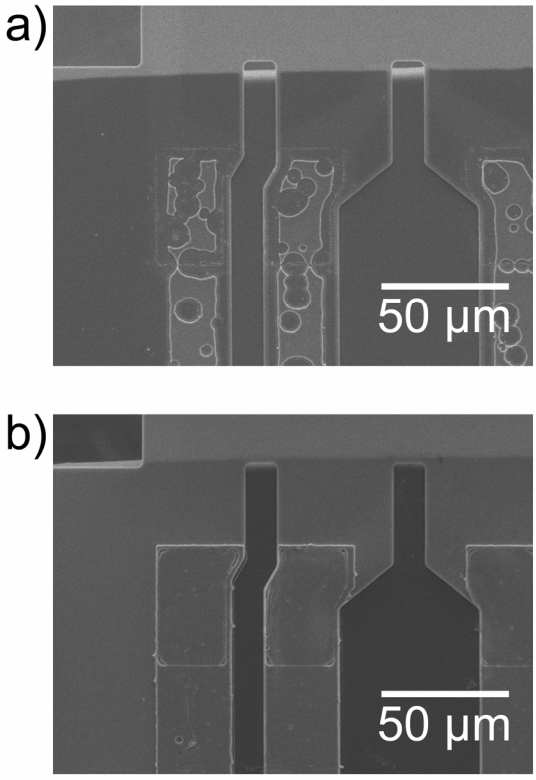

Figure 4.5 Quality of metal traces using a) the old process without metal protection during oxide etching and b) the improved process with photoresist protecting the metal during oxide etching

For the final release, the handle layer is etched through from the backside and the BOX layer is removed in HF. Since there are now five aluminum paths per cantilever to contact two resistors and the heaters traces independently, the individual metal lines are much narrower. Therefore, the damage of the SiO_2 etching to the metal lines that could be tolerated for the first device generation, results in device failure due to interrupted electrical connections in the second generation devices, as shown in Figure 4.5a. To circumvent this problem, an additional photolithography step is done after the backside through wafer etch. The same lithography mask that revealed the trenches on the backside of the wafer to get free-hanging cantilevers is now used to cover the same geometry on the topside leaving only the cantilever and the surrounding trench area

uncovered during the BOX-layer etching. This method effectively protects the aluminum from the HF and results in significantly increased yield. Figure 4.5b shows that there is no damage to the metal lines when the described new process was used.

4.3 Electrical Testing

The basic electrical testing was performed similarly to the first generation devices. First, the heater resistors were examined. Their resistances and power levels are plotted vs. the applied voltage in Figure 4.7a and b, respectively. It can be seen that both the low power resistances and the thermal runaway behaviors of types C and E are very similar, which is expected because the cantilever geometries and heater shapes are identical. The same is true for cantilever types D and F. The sheet resistance of the high doped areas calculated from the heater resistance and the according equivalent length-do-width ratio is between 29 and 32 Ω/□, which is very close to the predicted value of 32.85 Ω/□. In Figure 4.6b, it can be seen that cantilever types C and E, which have a square shape and the heater located around the whole edge, are able to dissipate the most power before thermal runaway occurs. This can be explained by the relatively closer placement of the heater to the cantilever substrate, which acts as a heat sink, compared to the other cantilever types.

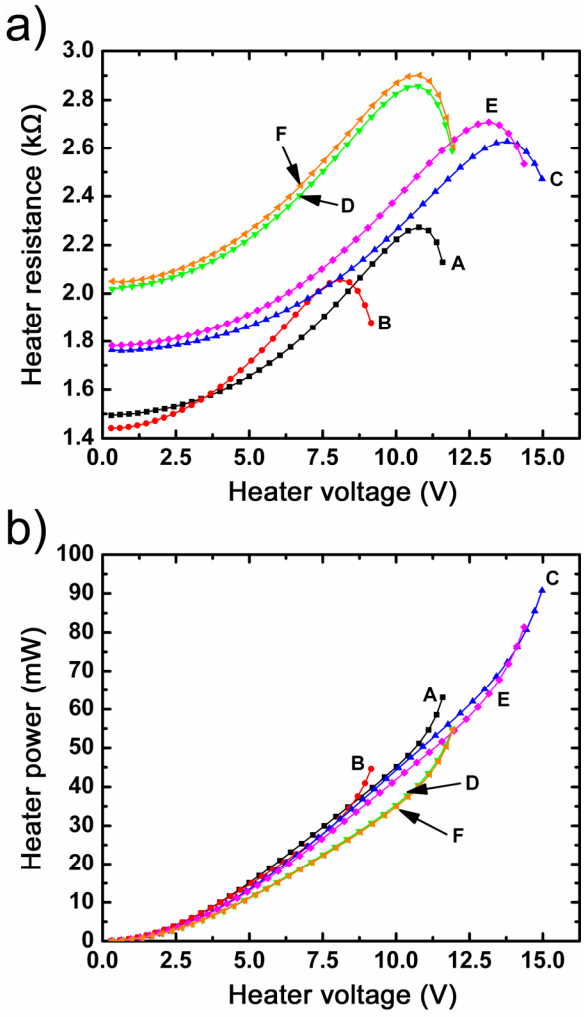

Figure 4.6 a) Heater resistance and b) heater power vs. heater voltage for six cantilever types

The same electrical characterization was done for the resistors in <110>-direction and <100>-direction as shown in Figure 4.7. It can be seen that the room temperature resistance is very similar for all types, which is expected since the resistor configuration is the same. It can also be seen that the alignment of the crystal directions does not affect the resistance, which is important in order to achieve a well-balanced bridge circuit for temperature compensation. The resistance change with voltage is very similar for each two resistors on a cantilever with the exception of the tested device of type C. Compared

to the small surface area of the resistors, the dissipated power at the thermal runaway point is very large, which is due to the proximity of the resistors to the clamped base.

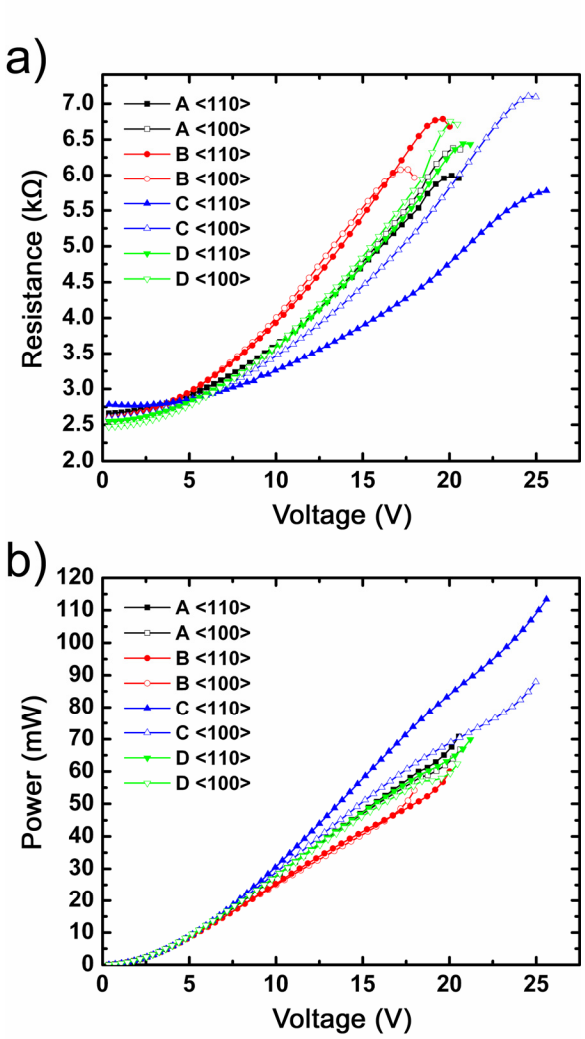

Figure 4.7 a) Resistance and b) power vs. voltage for the implemented resistors in <110>- and <100>-direction for four cantilever types

The shown relationship between resistance and voltage in Figure 4.7a and hence also the information about power vs. voltage in Figure 4.7b were obtained after the device was powered past the thermal runaway point several times. These thermal cycles were found to reduce the room temperature resistance and also modify the behavior of the resistance at increased voltages. After these experiments, one of the resistors was

connected to a digital multimeter and its resistance was monitored over the following 14 hours with one measurement taken every 60 seconds. The results are shown in Figure 4.8. The graph represents the actual data that was taken in the experiment and does not contain a fit curve.

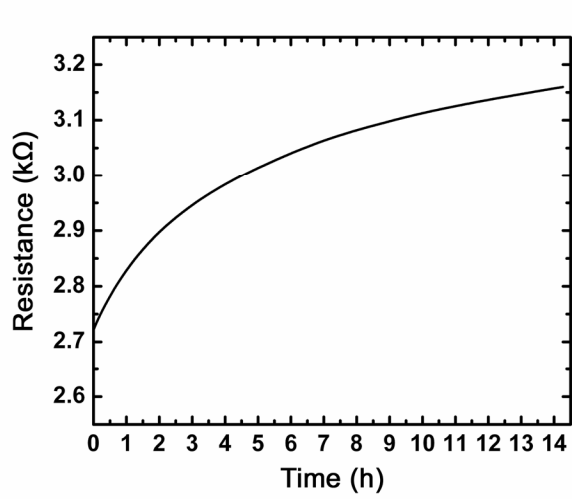

Figure 4.8 Actual data of one piezoresistor's resistance vs. time; the resistor was powered up to the thermal runaway point several minutes before time zero

It can be seen that the resistance increases monotonically and approaches a steady-state value asymptotically. The physical mechanisms of this effect are not well-understood, but the very long time constant of the signal change indicates that a diffusion process, e.g. between the high and low doped silicon areas, took place. From the steep increase in the beginning and the fact that the cantilevers had been stored under similar environmental conditions as during the experiments for several weeks previously, it is clear that this effect must have been triggered by the heating of the devices during the measurements of the voltage-dependent resistance. However, since the piezoresistor and the resistor for temperature compensation are not used at these high power levels during actual sensing operations, this behavior is not critical for the functioning of the devices.

4.4 Thermal Testing

Raman spectroscopy was used to determine the local temperature in the center of the heater trace at the free end. From previous work [2], it can be assumed that this is the hotspot location of the cantilever. Figure 4.9a shows the hotspot temperature of each device type for five different power levels.

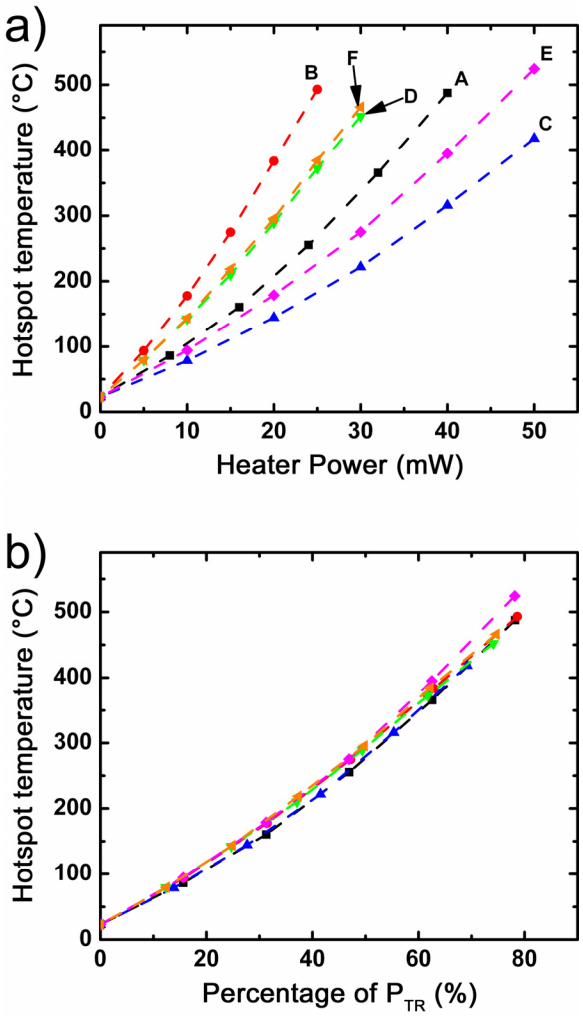

Figure 4.9 Hotspot temperature vs. a) total power of the implemented heaters and b) percentage of power at thermal runaway point for six cantilever types

It can be seen that the long, narrow devices of types B, D, and F reach the same temperatures as the other types at lower cantilever powers. Those cantilevers within each

geometry that have the heater around the whole outer edge, i.e. types C and E for the square shape and types D and F for the long, narrow shape, are able to dissipate more power at a given temperature than the devices with the heater only at the free end. This is expected because some heat will be generated closer to the clamped base and can be conducted more easily into the substrate. Cantilever types D and F, which have the same outer dimensions and heater geometries, show very similar behavior of temperature vs. power. However, the plots for types C and E, which also have the same geometries and heaters, differ from each other. Since all other properties are equal, it can be concluded that the tested devices were of different thickness. Since the type C device was able to dissipate more power than the type E device, it is assumed to be thicker thus allowing more conduction from the free end toward the base. If heat transfer with the surrounding environment is neglected the heat conduction from the free end to the clamped end for a given temperature difference ΔT can be written as:

$$q = k \cdot w_c \cdot t_c \frac{\Delta T}{l_c} \tag{1.1}$$

where k is the temperature dependent thermal conductivity of silicon and w_c, t_c and l_c are the cantilever width, thickness and length, respectively. The thermal conductivity for thinner devices can also be decreased due to boundary scattering of the phonons, thus adding to the effect of decreased ability to conduct heat [3]. Although the relationship of hotspot temperature to power level differs greatly for the different devices, the graphs are almost identical when the hotspot temperature is plotted vs. the heater power relative to the power level at which thermal runaway in each device occurs as shown in Figure 4.9b. The power level for the thermal runaway point was determined from the power at which the resistance was maximal during the electrical

characterization. These findings confirm the assumption that the thermal runaway temperature is a material property that is determined by the doping level of the silicon and independent of cantilever geometry [4]. By extrapolating the plots in Figure 4.9b thermal runaway for this material is predicted to occur at a temperature between 650 and 700 °C. It can be concluded that the temperature at the thermal runaway point only needs to be measured once for a given doping level to predict the hotspot temperature for any device with known electrical characteristics.

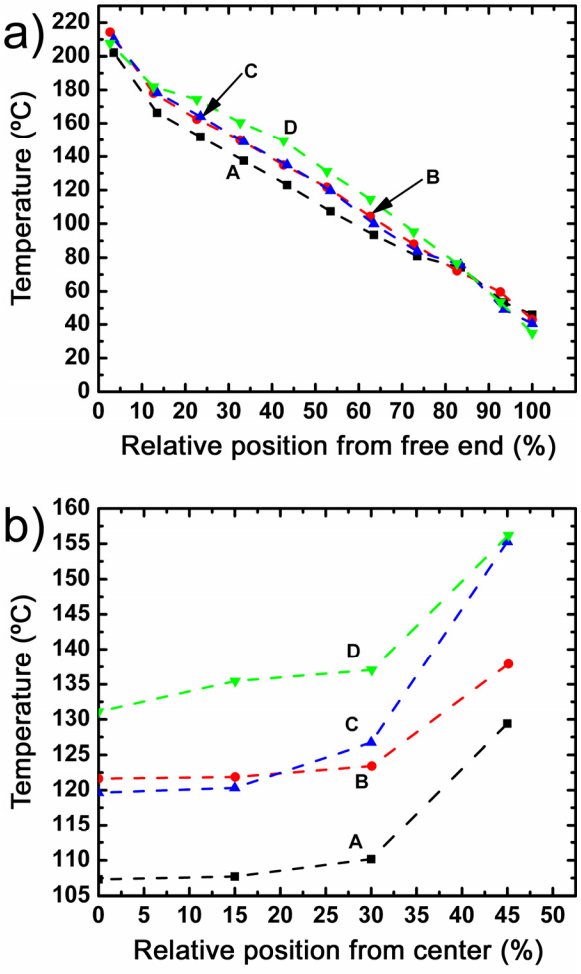

Figure 4.10 Raman measurement of temperature vs. relative position for types A-D a) along the cantilever length, where 0% is the center of the free end and 100% is the center of the clamped base and b) along the cantilever width, where 0% is at the cantilever center in length and width direction and 50% is at the edge in width direction and in the center of the length direction

After the relationship between power and hotspot temperature was determined for each cantilever type the same devices were used to investigate the spatial distribution of the temperature. For this purpose, the power was fixed at a level for which a hotspot temperature of 200 °C was expected and Raman measurements were taken in 11 different locations along the cantilever length direction between the hotspot and the clamped edge. The temperature distribution is plotted vs. the relative position, i.e. the ratio between distance from the free end and cantilever length, in Figure 4.10a. This plot style was chosen because it allows for a better comparison of the temperature trends of devices with different lengths. Although it can be seen that the distributions are almost linear and very close to each other, there are differences between the two heater shapes. Types C and D, which have the heater around the cantilever edge, have a slightly more uniform temperature distribution than their counterparts of identical cantilever geometry but with the heater at the free end. The added heat flow from the sides in types C and D causes the temperature to decrease more slowly. Figure 4.10b, which shows the temperature distribution along the width direction, seems to confirm this trend although the differences are marginal. The data points at about 2.5 and 82.5 % in Figure 4.10a and at 45% in Figure 4.10b show somewhat higher temperatures than expected from the adjacent data points. Since these positions were in the high doped silicon areas, the change in the temperature slope could have been caused by the higher thermal conductivity. The deviation could also be caused by the measurement error of the Raman system because the relationship between shift in peak position and temperature is calibrated for the intrinsic silicon. However, even if the temperature measurements at these single locations are erroneous this has no effect on the accuracy of the temperature

measurements in the intrinsic silicon areas, which is expected to have an error of 5 K or less [5].

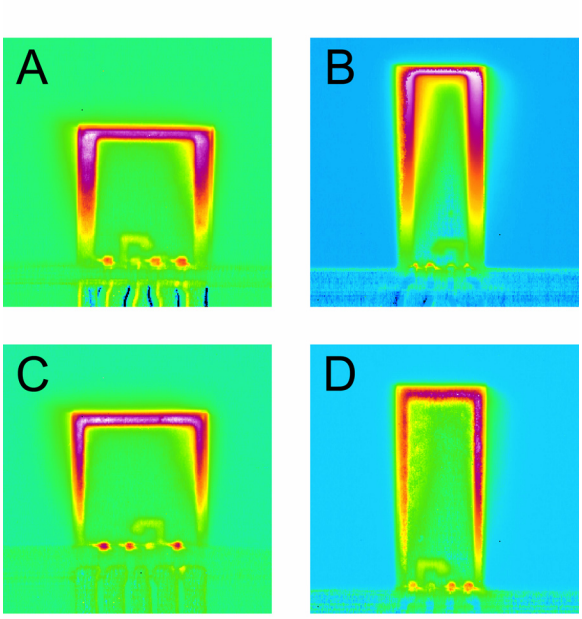

Figure 4.11 Temperature distribution on the cantilever from infrared (IR) microscopy for types A-D; problems with the emissivity data and deviation from Raman measurement make IR results questionable

To supplement the quantitative Raman spectroscopy measurements, which are expected to be of high accuracy, infrared (IR) microscopy was performed to determine the qualitative temperature distribution on the device surface. The results are shown for cantilever types A-D in Figure 4.11. It can be seen that the temperature distribution obtained from IR microscopy is conflicting with that obtained by the Raman measurements. The IR results show a very steep temperature gradient at the edges of the heater and almost uniform temperature in the intrinsic silicon regions. However, this behavior is not physically realistic. Since the thermal conductivity of doped silicon is expected to be lower than that of the intrinsic silicon, the temperature decline in the intrinsic silicon areas should be much more gradual.

4.5 Sensitivity and Combined Testing

The four cantilevers of types A-D, whose electrical and thermal properties were characterized in the previous sections, were used to perform deflection sensitivity measurements with the same setup as described in chapter 3. One of the main objectives of these investigations is to quantify the ability to perform temperature independent stress measurements by the use of the previously discussed temperature compensation scheme. For this purpose, the output signal was measured when the cantilever was deflected and either the resistor in <110>-direction or the resistor in <100>-direction was connected in addition to three external resistors in a Wheatstone bridge. The resulting signal is plotted vs. the tip deflection in Figure 4.12a. It can be seen that the sensitivity of the <100>-resistor to changes in the stress state is very small as compared to the sensitivity of the <110>-resistor. The experiment was then repeated with both resistors connected as one branch of the Wheatstone bridge and supplemented by two external resistors. It can be seen that the resulting signal is almost identical to the signal from the <110>-resistor alone.

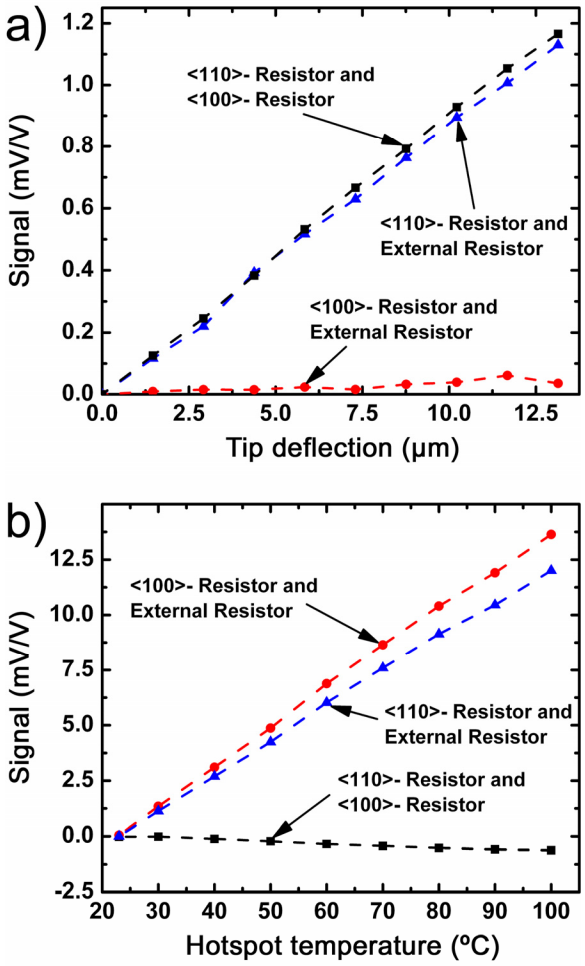

Figure 4.12 Output signals when the implemented <110>-resistor, the implemented <100>-resistor and both resistors are connected to the Wheatstone bridge circuit for a) deflection of the cantilever tip and b) heating of the implemented resistive heater

The three experimental runs were then repeated but instead of deflecting the free end of the cantilever, the hotspot temperature was modified by powering the implemented heater trace. Figure 4.12b shows that the bridge output signals were very similar to each other when either of the two resistors was connected alone. As a consequence, the signal when both resistors are connected in the same branch of the Wheatstone bridge is much smaller because the resistance changes due to the temperature variation are canceled out. The small signal that remains is assumed to be caused by the difference in the two resistors' average temperature due to their different locations on the

cantilever. As a result of Figure 4.12, it can be concluded that the novel resistor arrangement on the cantilever can indeed be used to measure changes in the cantilever stress with greatly reduced parasitic signals from temperature changes and without sacrificing mechanical sensitivity.

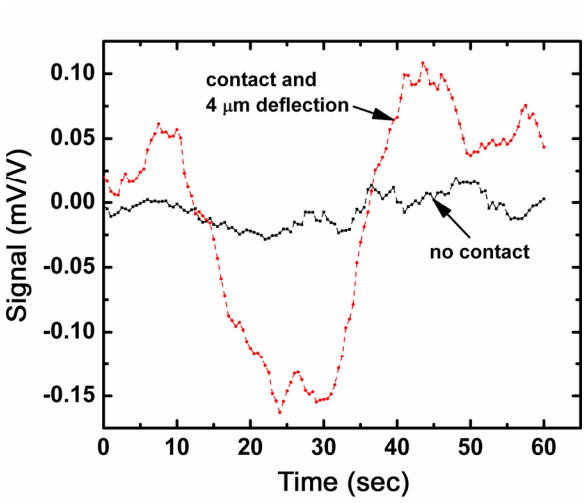

Figure 4.13 Signal drift over one minute time span for the case of free cantilever and cantilever in contact with and deflected by needle probe

During preliminary experiments, it was discovered that the bridge output signal experienced a drift of several tens of millivolts with time constants on the order of tens of seconds to minutes. Figure 4.13 shows the drift of the output signal when the cantilever is either not in contact with the needle probe of the deflection setup or in contact with the probe and slightly deflected. It can be seen that the mentioned drift signal is only present when the cantilever is contacting the needle probe. Therefore, it can be assumed that the drift is caused by the external setup, e.g. due to thermal expansion of the equipment with changing environmental temperature. Since the drift signal is caused by the experimental setup and not the cantilever itself, it is desirable to compensate for it in order to get more accurate results for the sensitivities to deflection and temperature changes. Therefore, during all of the measurements in this section, the zero point of the signal was measured

between each increase of the deflection or temperature. The real output signal is then calculated by subtracting the average of the zero point signals before and after the measurement. This approach assumes a linear progression of the signal drift in between the zero point measurements and hence cancels long-term drift with time constants greater than the duration of three measurements, which represents the majority of the error due to drift as shown in Figure 4.14.

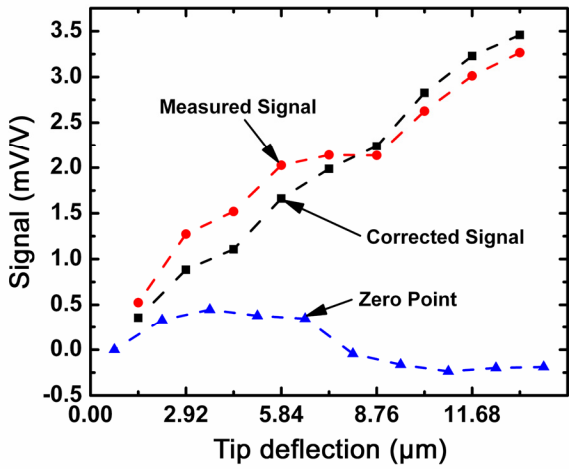

Figure 4.14 Measured signal for nine data points and zero point measurement at zero deflection in between each deflected measurement; the corrected signal is obtained by linearly interpolating the zero point drift and subtracting it from the measured signal

Figure 4.15 shows the deflection sensitivities so obtained for cantilever types A-D at room temperature. As expected, the devices of types A and C show higher tip deflection sensitivities because an equivalent absolute change in cantilever deflection will cause greater stresses in these square-shaped devices than in the longer, narrower devices of type B and D. The variations between types A and C and between types B and D are presumed to be caused by variations in cantilever thickness and the location of the needle probe contact.

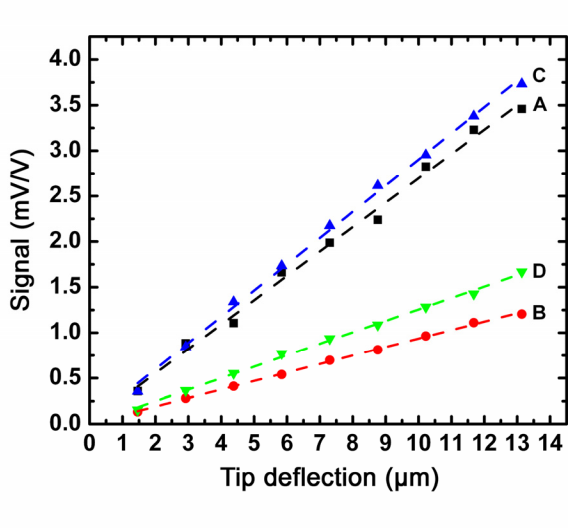

Figure 4.15 Tip deflection sensitivities for devices of types A-D

In Figure 4.16, the output signal of cantilever types A-D is plotted vs. the hotspot temperature. It can be seen that the temperature sensitivity is generally very low. A hotspot temperature of 200 °C, for example, which causes a signal change of about 0.75mV/V for the type C device, is equivalent to a tip deflection of about 2.5 um for the same device. The temperature sensitivity is very linear and similar for device types A, C, and D. However, type B shows a behavior that is strongly deviating from the other types. The physical reasons for this anomaly are not well-understood, but it is suspected that the temperature coefficients of resistance (TCR) for the two resistors on the cantilever of type B are different from each other.

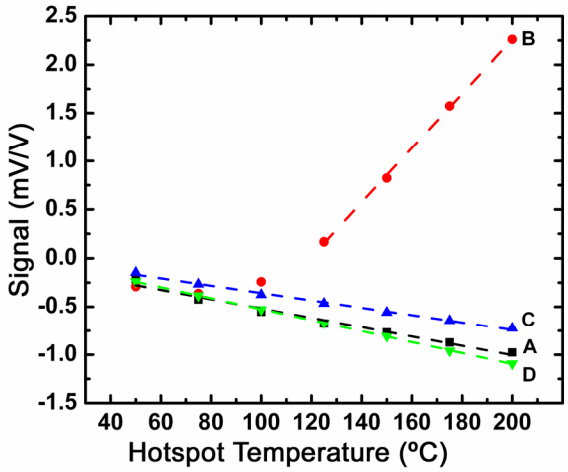

Figure 4.16 Output signal vs. hotspot temperature for devices types A-D without deflection; types A, C, and D show linear decrease, type B shows decrease, then a minimum, then strong increase

Besides being sensitive to deflections and having a low sensitivity to temperature changes, another requirement to enable measurements with integrated compensation for temperature variations is a small variation of the mechanical sensitivity with temperature, i.e. a small hotspot temperature coefficient of tip deflection sensitivity (TCS). Figure 4.17 shows a plot of the output signal vs. tip deflection of the type B cantilever for six different hotspot temperatures that are achieved by powering the heater. It can be seen that the sensitivity is not a very strong function of the hotspot temperature for the investigated values.

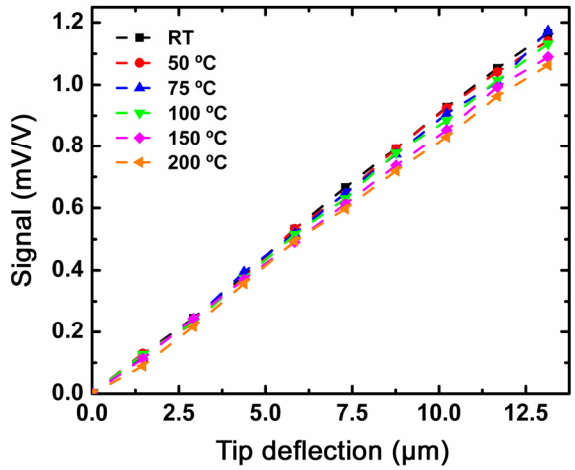

Figure 4.17 Output signal of Wheatstone bridge with both resistors connected vs. tip deflection for six different hotspot temperatures

Figure 4.18 shows the normalized deflection sensitivities vs. temperature derived from the slope of linear fits to the data points in Figure 4.17. The slope of the linear fits in the resulting figure represents the TCS and it is on the order of $-5 \cdot 10^{-4}\, K^{-1}$. The devices of type A, B, and D have very similar values, whereas the TCS for type C is slightly higher. However, the differences are not very significant compared to the scattering of the data points as seen in Figure 4.18.

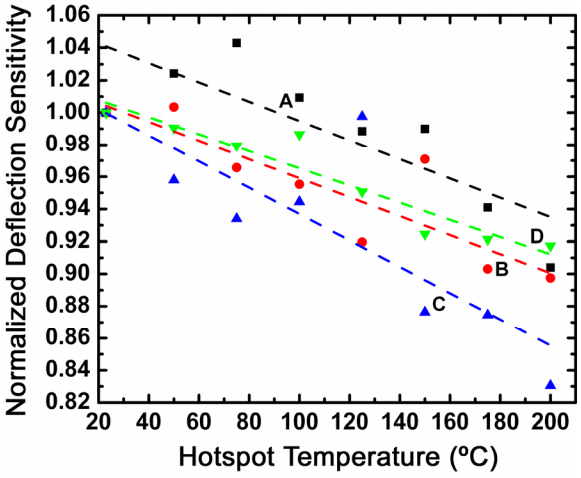

Figure 4.18 Normalized tip deflection sensitivity vs. hotspot temperature for devices of types A-D

The signal drift due to noise in the cantilever was investigated by monitoring the output signal for 60 seconds without contact of the needle probe. The results, as shown in Figure 4.19, indicate that the system noise below a hotspot temperature of 100 °C is not dominated by the temperature change from the implemented heater. Since the noise levels at 150 and 200 °C are significantly higher, the main cause of the signal drift for these temperatures is the internal heating.

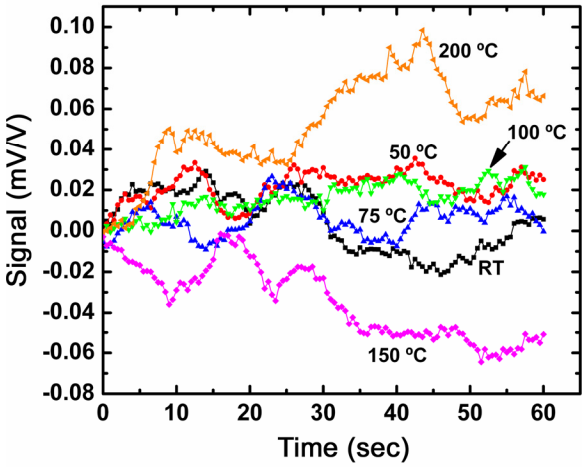

Figure 4.19 Output signal drift of Wheatstone bridge with both resistors connected over a time span of 60 seconds for six different hotspot temperatures

In an additional experiment, the response of the resistors to light changes was investigated. For this purpose, the needle probe was moved away from the cantilevers so as not to block the light irradiation on the cantilever surface. A microscope lamp was used as a light source for this experiment. Since the light intensity is not calibrated, only qualitative conclusions can be drawn from these experiments. The output signal was measured when either the resistor in <110>-direction or the resistor in <100>-direction was connected in addition to three external resistors in a Wheatstone bridge and the results are shown in Figure 4.20 along with the data obtained when both resistors were integrated into the bridge circuit.

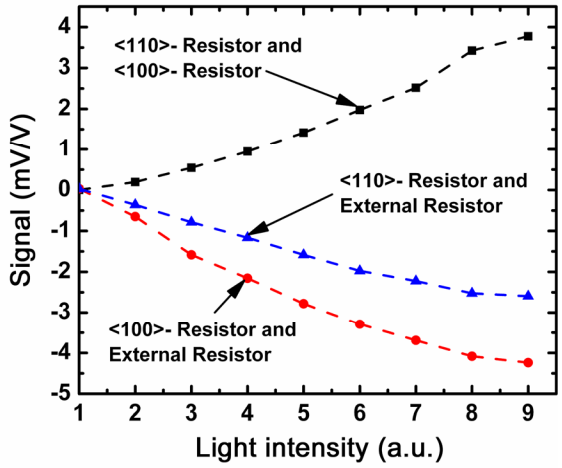

Figure 4.20 Output signal of Wheatstone bridge with either <100>-resistor, <110>-resistor or both resistors connected while exposed to different intensities of light from a microscope lamp

It can be seen that, although the trends of the two resistors' output signal changes were similar, the signals do not cancel out or reduce the sensitivity to light irradiation when both resistors are connected to the Wheatstone bridge. This effect is not fully understood, but it is suspected that besides altering the resistance values, the light also causes a photoelectric effect that is reflected in the output signal. For practical applications, the ability of the system to cancel out variations in light intensity is not as critical as the temperature compensation, since the chemical sensing setup can be constructed so that incoming light is absorbed before it reaches the cantilever.

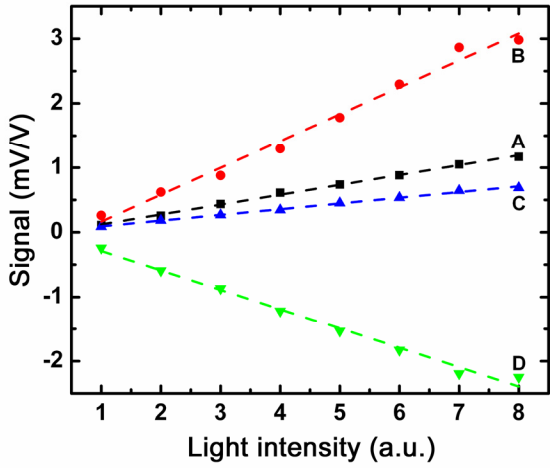

Figure 4.21 Light sensitivity for 4 device types; light intensity in arbitrary units (knob position of microscope lamp)

Figure 4.21 shows that both the trend and the magnitude of the light sensitivity vary greatly between the devices. These properties are not expected to be specific for the different cantilever types since the geometries of the resistors and current traces are identical.

4.6 Summary and Conclusion

Silicon microcantilevers with integrated heater and temperature compensation structures were designed, fabricated, and tested. Two different cantilever geometries were combined with two different shapes of heater traces. The hotspot temperatures that can be reached with these devices are greater than 500 °C without thermal failure. It was found that the temperature at which thermal runaway of the electrical resistance occurs is very similar for all device types, which supports previous claims that it is purely a material property that depends on the doping type and level. It can be concluded that the temperature calibration does not need to be performed for every single device, but instead

simple DC-voltage characterization is sufficient to predict the hotspot temperature. The temperature was found to decrease about linearly along the cantilever with the hotspot temperature at the free end and the coldest point at the clamped substrate, which acts as a heat sink. The temperature distribution in width direction is very uniform. The differences in the temperature profiles between the different heater geometries are marginal.

Table 4-2 Summary of Properties for second generation microcantilevers

Type		A	B	C	D	E	F
Room temperature resistance of heater	kΩ	1.494	1.442	1.764	2.019	1.782	2.051
Room temperature resistance of 90°-resistor	kΩ	3.165	3.557	3.354	3.204	n. m.	n. m.
Room temperature resistance of 45°-resistor	kΩ	3.560	3.777	3.360	2.995	n. m.	n. m.
Heater voltage at thermal runaway	V	10.8	8.1	13.8	10.8	13.2	10.8
Heater resistance at thermal runaway	kΩ	2.27	2.06	2.63	2.86	2.71	2.90
Heater power at thermal runaway	mW	51.4	31.8	72.4	40.8	64.3	40.2
Hotspot temperature at 80% of heater power at thermal runaway	°C	501	502	498	490	539	501
Base temperature at 200 °C hotspot temperature	°C	46.2	42.9	40.5	34.8	n. m.	n. m.
Room temperature tip deflection sensitivity (mV/V-µm)	mV/V-µm	0.2677	0.09318	0.2879	0.1258	n. m.	n. m.
Hotspot temperature coefficient of tip deflection sensitivity	10^{-4} K^{-1}	-5.97	-5.86	-8.15	-5.32	n. m.	n. m.
Hotspot temperature sensitivity	10^{-3} mV/V-K	-4.838	28.12*	-3.817	-5.699	n. m.	n. m.
Light sensitivity	mV/V-a.u.	0.1528	0.4168	0.08825	-0.3007	n. m.	n. m.

n. m.: not measured; *: above 100 °C; yellow background: lowest absolute value; lavender background: highest absolute value

Resistor structures with different crystal directions but in close proximity on the cantilever surface were also implemented in the design and their properties were characterized. The experiments showed that those resistors in <110>-direction showed

high sensitivity to both cantilever deflection and temperature changes, whereas the resistors in <100>-direction were only sensitive to temperature changes and had very little deflection sensitivity. It was shown that these resistors can greatly reduce parasitic signals due to temperature changes without sacrificing deflection sensitivity when combined in a Wheatstone bridge circuit. It was also shown that the deflection sensitivity is not a strong function of the temperature, thus enabling the accurate sensing of deflections during heater operation or exposure to external heat sources. A detailed summary of the cantilever properties is given in Table 4-2.

4.7 References

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CHAPTER 5

CONCLUSION AND FUTURE WORK

In this work, the design, fabrication, and testing of piezoresistive silicon microcantilevers for chemical sensing were investigated. The main objective of the theoretical discussions and the finite element modeling was the optimization of design parameters for these devices. It was found that improvements in surface stress sensitivity for piezoresistive readout are achieved by different design considerations than for piezoresistive tip deflection measurements or for surface stress measurements with optical readout. The surface stress sensitivity can be improved by placing the piezoresistive element at the center of the clamped base of the cantilever and by minimizing all of its dimensions. The cantilever length was found to be irrelevant for the piezoresistive surface stress sensitivity, whereas increasing the cantilever width can greatly improve the sensitivity. The improvement is not linear and the transition point between large improvement and marginal improvement with increasing cantilever width is determined by the piezoresistor shape. A good tradeoff between compactness and surface stress sensitivity for a piezoresistive area of 40 μm square, which is a realistic size based on the discussion of the microfabrication processes, was found to be a cantilever width of 200 μm or five times the side length of the piezoresistor. Other important parameters that impact the cantilever's surface stress sensitivity are the thickness of the cantilever and the piezoresistor. It is advantageous to minimize both of these parameters. In contrast to the sensing of point forces or tip deflections, the surface

stress sensitivity does not vanish when the dopant concentration along the thickness direction is uniform, but remains at a high level compared to the maximum sensitivity. When the piezoresistor thickness is fixed by the fabrication process the cantilever thickness should be chosen, so that the piezoresistive region makes up two thirds of the cantilever thickness for optimized sensitivity.

The second emphasis of this work lies on the establishment of stable microfabrication processes for chemical sensing microcantilevers. Although the initial results were quite promising, many process optimizations were performed to improve the final device quality and the yield. The parameters of the Bosch process, for example, were successfully modified to prevent the buildup of black silicon in the etch trenches, which had previously caused several processes to fail. The wafer tilting method to inspect the actual etching progress of the backside through wafer etch is another example of a simple but highly effective optimization that allows for better control over the backside edge position. Additional fabrication challenges were faced during the processing of the second generation devices. The development of an additional photolithography step to protect the metal lines became necessary because the damage to the aluminum of the second generation's narrower conductors from the HF dip was much more severe. Another improvement of the fabrication process for the second generation is the method used to thin down the device layer. Although it is more time-consuming to grow thermal oxide on the wafer several times and etch it away, this method is expected to give much better uniformity across the wafer than the direct silicon etching that was used previously.

Characterization of the fabricated devices represents the third focus area of this study. For the first generation devices, the DC-voltage characteristics were studied in

detail and it was found that current leakage through the intrinsic silicon areas exists. An improved analytical model was established that is able to predict resistance values for different geometries with much better accuracy than the simple model, which is based on the assumption of zero current flow out of the piezoresistor due to the p-n-junctions. For the second device generation, the problem of unwanted current flow through the intrinsic silicon was avoided or greatly reduced by creating highly conductive, high doped traces. The deflection sensitivities of all devices were tested with a custom deflection setup. The first generation cantilevers were then tested in a flow cell setup and all devices showed good sensitivity for chemical sensing. Due to uncertainties in the polymer deposition process, the comparison of the different cantilever types was not conclusive.

For the second generation, the focus of the characterization methods was shifted toward the analysis of thermal properties and the interplay between simultaneous heating and sensing operation. It was found that the implemented heater traces can reach hotspot temperature above 500 ºC without thermal damage. Furthermore, it was shown that thermal runaway in the silicon occurs at the same hotspot temperature for all devices, independent of geometry. A direct conclusion of this result is that the thermal properties of the heater structures do not need to be calibrated for every single cantilever. It is sufficient to know the DC-characteristics, in particular the power level at which thermal runaway occurs, to predict the device temperature for a given electrical input. From the comparison of the absolute power level at which thermal runaway occurs to that of a device, whose thickness has been calibrated, it is assumed that even the thickness of any device of the same type can be backed out of the DC-electrical testing.

The second emphasis of the heated devices lies on the temperature compensation scheme that was integrated into the cantilevers by creating two resistors at a 45º-angle. Deflection and heating experiments confirmed that the theoretical considerations correctly predicted the scheme's ability to significantly reduce the temperature sensitivity of the cantilevers without sacrificing sensitivity to mechanical input. The close proximity of the two resistors on the same cantilever assures that the temperature in them is always very similar, so that the signals are effectively canceled. In many situations, such as thermal non-equilibrium, this compensation would not be possible with an external compensation resistor, e.g. on a second cantilever.

The future work in the area of design and modeling should be directed toward designing new geometries with increased sensitivity to surface stresses based on the concepts that were developed in this study. The FE models should be enhanced and their results quantitatively compared to experimental data. Especially for the devices of the second generation with integrated heaters and temperature compensation schemes, there is a large number of possible applications ranging from explosive detection to calorimetric measurements of thin polymer films. A suggestion for improvement of these devices is an optimization of the implemented heater structures to produce a more uniform temperature distribution on the cantilever surface. FE modeling would be a suitable tool to design better heaters with a minimum of trial-and-error. The data of the temperature measurements from the second generation devices would be helpful to improve the validity of such FE models. A long-term objective could be the development of cantilever arrays, in which a large number of chemical processes could be triggered and measured simultaneously.

Appendix A.1 – First Generation Microfabrication Recipe

		Process Step	Equipment	Parameters	Expected value
Create beam outline	1.1	Measure device layer thickness	Nanospec refractometer	Recipe: SOI	Thickness: 2 µm
	1.2	Wet Oxidation	Furnace	Temperature: 1150 °C Time: variable Ramp rate: 20 °C/min H2O vapor flow rate: 8 l/min	
	1.3	Remove thermally grown silicon dioxide		Hydrofluoric acid (49%)	Etch rate: 2.3 µm/min
	1.4	Move from HF bath to DI water bath		Time: 10 sec	
	1.5	DI water rinse			
	1.6	Nitrogen dry			
	1.7	Repeat steps 1.1-1.6 until device layer thickness is correct			
	1.8	*Solvent wafer clean*			
	1.8.1	Agitated acetone bath	Ultrasonic bath	Time: 5 min	
	1.8.2	Acetone rinse			
	1.8.3	Methanol rinse			
	1.8.4	Isopropanol rinse			
	1.8.5	DI water rinse			
	1.8.6	Nitrogen dry			
	1.9	Dehydration	Vacuum oven	Temperature: 160 °C Time: 20 min	
	1.10	*Patterning of 3.3 µm Shipley 1827 photoresist*		*Mask: FTG 2nd Gen. Beam*	
	1.10.1	Spin coat 1827 photoresist	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 1000 rpm/sec Time: 35 sec	Thickness: 3.3 µm
	1.10.2	Softbake photoresist	Hotplate	Temperature: 115 °C Time: 3:30 min	
	1.10.3	Measure intensity of mask aligner	Karl Suss UV-meter	Channel: CI-2 Wavelength: 405 nm	Intensity: 20 mW/cm^2
	1.10.4	Expose wafer	Karl Suss MA 6	Mask: FTG 2nd Gen. Beam Dose: 220 mJ/cm^2	Time: 11 sec
	1.10.5	Develop photoresist		Developer: MF 354	Time: 35 sec
	1.10.6	Hardbake photoresist	Hotplate	Temperature: 115 °C Time: 10 min	
	1.11	*Structure device layer*	*Plasma-Therm ICP*		
	1.11.1	Chacterize etch rate on dummy wafer with same PR pattern	Plasma-Therm ICP	Recipe: FTG_SI2	Etch rate: 0.2 µm/cycle
	1.11.2	Etch sample with safe number of cycles	Plasma-Therm ICP	Recipe: FTG_SI2	Number of cycles: 7
	1.12	Make sure no silicon left in trenches	Nanospec refractometer	Recipe: SOI	Thickness: 0 µm
	1.13	*Piranha wafer clean*			
	1.13.1	Agitated acetone bath	Ultrasonic bath	Time: 5 min	
	1.13.2	DI water rinse			
	1.13.3	Nitrogen dry			
	1.13.4	Piranha bath	Hotplate	Sulfuric Acid (96%): 70 ml Hydrogen Peroxide (30%): 30 ml Temperature: 120 °C Time: 10 min	
	1.13.5	DI water rinse			
	1.13.6	Nitrogen dry			
High dosage implantation	2.1	Dehydration	Vacuum oven	Temperature: 160 °C Time: 20 min	
	2.2	*Patterning of 3.3 µm Shipley 1827 photoresist*		*Mask: FTG 2nd Gen. High Doping*	
	2.2.1	Spin coat 1827 photoresist	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 1000 rpm/sec Time: 35 sec	Thickness: 3.3 µm
	2.2.2	Softbake photoresist	Hotplate	Temperature: 115 °C Time: 3:30 min	
	2.2.3	Measure intensity of mask aligner	Karl Suss UV-meter	Channel: CI-2 Wavelength: 405 nm	Intensity: 20 mW/cm^2
	2.2.4	Expose wafer	Karl Suss MA 6	Mask: FTG 2nd Gen. High Doping Dose: 220 mJ/cm^2	Time: 11 sec
	2.2.5	Develop photoresist		Developer: MF 354	Time: 35 sec
	2.2.6	Hardbake photoresist	Hotplate	Temperature: 115 °C Time: 35 min	
	2.3	High Dosage Dopant implantation	Outside vendor	Species: Boron	

				Dose: 3e15 cm^-2	
				Energy: 120 keV	
				Tilt angle: 7 °	
	2.4	*Piranha wafer clean*			
	2.4.1	Agitated acetone bath	Ultrasonic bath	Time: 5 min	
	2.4.2	DI water rinse			
	2.4.3	Nitrogen dry			
	2.4.4	Piranha bath	Hotplate	Sulfuric Acid (96%): 70 ml	
				Hydrogen Peroxide (30%): 30 ml	
				Temperature: 120 °C	
				Time: 10 min	
	2.4.5	DI water rinse			
	2.4.6	Nitrogen dry			
	2.5	O2-plasma wafer clean (repeat until clean)	Gasonics Asher	Recipe A (High Temp., 1 min)	
High dosage drive-in	*3.1*	*PECVD silicon dioxide deposition*	*Unaxis PECVD*		
	3.1.1	Characterize deposition rate on dummy wafer	Unaxis PECVD	Recipe: FTGSIO	Deposition rate: 1.132 nm/sec
	3.1.2	Measure buried oxide layer thickness	Nanospec refractometer	Recipe: Oxide on silicon	Thickness: 1 µm
	3.1.3	Deposit 200 nm of silicon dioxide	Unaxis PECVD	Recipe: FTGSIO	Time: 177 sec
	3.1.4	Measure buried oxide layer thickness	Nanospec Refractometer	Recipe: Oxide on silicon	Thickness: 1.2 µm
	3.2	Dopant drive in	Furnace	Temperature: 1000 °C	
				Ramp rate: 20 °C/min	
				Time: 60 min	
				Nitrogen gas flow: 20 l/min	
	3.3	*Remove PECVD silicon dioxide*			
	3.3.1	Characterize BOE etch rate for PECVD oxide on dummy wafer			Etch rate: 80 nm/min
	3.3.2	Remove oxide in BOE			Time: 3 min
	3.3.3	Measure BOX-layer to make sure all PECVD oxide was removed			BOX-layer thickness: < 1um
Low dosage implantation	4.1	Dehydration	Vacuum oven	Temperature: 160 °C	
				Time: 20 min	
	4.2	*Patterning of 3.3 µm Shipley 1827 photoresist*		*Mask: FTG 2nd Gen. Low Doping*	
	4.2.1	Spin coat 1827 photoresist	CEE 100CB spinner	Spin rate: 3000 rpm	Thickness: 3.3 µm
				Ramp rate: 1000 rpm/sec	
				Time: 35 sec	
	4.2.2	Softbake photoresist	Hotplate	Temperature: 115 °C	
				Time: 3:30 min	
	4.2.3	Measure intensity of mask aligner	Karl Suss UV-meter	Channel: CI-2	Intensity: 20 mW/cm^2
				Wavelength: 405 nm	
	4.2.4	Expose wafer	Karl Suss MA 6	Mask: FTG 2nd Gen. Low Doping	Time: 11 sec
				Dose: 220 mJ/cm^2	
	4.2.5	Develop photoresist		Developer: MF 354	Time: 35 sec
	4.2.6	Hardbake photoresist	Hotplate	Temperature: 115 °C	
				Time: 35 min	
	4.3	Low Dosage Dopant implantation	Outside vendor	Species: Boron	
				Dose: 2e13 cm^-2	
				Energy: 20 keV	
				Tilt angle: 7 °	
	4.4	*Piranha wafer clean*			
	4.4.1	Agitated acetone bath	Ultrasonic bath	Time: 5 min	
	4.4.2	DI water rinse			
	4.4.3	Nitrogen dry			
	4.4.4	Piranha bath	Hotplate	Sulfuric Acid (96%): 70 ml	
				Hydrogen Peroxide (30%): 30 ml	
				Temperature: 120 °C	
				Time: 10 min	
	4.4.5	DI water rinse			
	4.4.6	Nitrogen dry			
	4.5	O2-plasma wafer clean (repeat until clean)	Gasonics Asher	Recipe A (High Temp., 1 min)	
Low dosage drive-in	*5.1*	*PECVD silicon dioxide deposition*	*Unaxis PECVD*		
	5.1.1	Characterize deposition rate on dummy wafer	Unaxis PECVD	Recipe: FTGSIO	Deposition rate: 1.132 nm/sec
	5.1.2	Measure buried oxide layer thickness	Nanospec refractometer	Recipe: Oxide on silicon	Thickness: 1 µm
	5.1.3	Deposit 200 nm of silicon dioxide	Unaxis PECVD	Recipe: FTGSIO	Time: 177 sec
	5.1.4	Measure buried oxide layer thickn.	Nanospec Refractometer	Recipe: Oxide on silicon	Thickness: 1.2 µm

	5.2	Rapid thermal anneal		AET RTP	Recipe: Jay2 Temperature: 1000 °C Time: 30 min Ramp rate: 90 °C/sec Nitrogen gas flow: 5 l/min	
Create vias in silicon dioxide	6.1	Dehydration		Vacuum oven	Temperature: 160 °C Time: 20 min	
	6.2	*Patterning of 3.3 µm Shipley 1827 photoresist*			*Mask: FTG 2nd Gen. Vias*	
	6.2.1		Spin coat 1827 photoresist	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 1000 rpm/sec Time: 35 sec	Thickness: 3.3 µm
	6.2.2		Softbake photoresist	Hotplate	Temperature: 115 °C Time: 3:30 min	
	6.2.3		Measure intensity of mask aligner	Karl Suss UV-meter	Channel: CI-2 Wavelength: 405 nm	Intensity: 20 mW/cm^2
	6.2.4		Expose wafer	Karl Suss MA 6	Mask: FTG 2nd Gen. Vias Dose: 220 mJ/cm^2	Time: 11 sec
	6.2.5		Develop photoresist		Developer: MF 354	Time: 35 sec
	6.2.6		Hardbake photoresist	Hotplate	Temperature: 115 °C Time: 10 min	
	6.3	*Etch vias into silicon dioxide*		*Vision RIE*		
	6.3.1		Characterize etch rate on dummy wafer	Vision RIE	Recipe: Standard Oxide	Etch rate: 8 nm/min
	6.3.2		Etch 5 min longer than necessary (selectivity to silicon very good)	Vision RIE	Recipe: Standard Oxide	Time: 30 min
	6.4	*Piranha wafer clean*				
	6.4.1		Agitated acetone bath	Ultrasonic bath	Time: 5 min	
	6.4.2		DI water rinse			
	6.4.3		Nitrogen dry			
	6.4.4		Piranha bath	Hotplate	Sulfuric Acid (96%): 70 ml Hydrogen Peroxide (30%): 30 ml Temperature: 120 °C Time: 10 min	
	6.4.5		DI water rinse			
	6.4.6		Nitrogen dry			
Create metal connections	7.1	Dehydration		Vacuum oven	Temperature: 160 °C Time: 20 min	
	7.2	*Patterning of 8 µm Futurrex NR5-8000 photoresist*			*Mask: FTG 2nd Gen. Metalization*	
	7.2.1		Spin coat NR5-8000 photoresist	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 500 rpm/sec Time: 35 sec	Thickness: 8 µm
	7.2.2		Softbake photoresist	Hotplate	Temperature: 150 °C Time: 1:30 min	
	7.2.3		Measure intensity of mask aligner	OAI UV-meter	Channel: CI-1 Wavelength: 365 nm	Intensity: 5 mW/cm^2
	7.2.4		Expose wafer	Karl Suss MA 6	Mask: FTG 2nd Gen. Metalization Dose: 168 mJ/cm^2	Time: 33.6 sec
	7.2.5		Post-exposure bake photoresist	Hotplate	Temperature: 100 °C Time: 2 min	
	7.2.6		Develop photoresist		Developer: RD-6	Time: 60 sec
	7.3	BOE dip to remove native oxide			6:1 Buffered Oxide Etch Time: 10 sec	
	7.4	DI water rinse				
	7.5	Nitrogen dry				
	7.6	Electron beam evaporative deposition of metal layer		CVC E-Beam evaporator	Metal: Aluminum Thickness: 800 nm Deposition rate: 0.3 nm/sec Pressure: 2e-6 torr (max.)	
	7.7	*Photoresist lift-off*				
	7.7.1		Acetone bath (covered)		Time: 8 h	
	7.7.2		Agitated acetone bath	Ultrasonic bath	Time: 30 sec	
	7.7.3		Acetone rinse			
	7.7.4		Methanol rinse			
	7.7.5		Isopropanol rinse			
	7.7.6		DI water rinse			
	7.7.7		Nitrogen dry			
	7.8	Sintering in forming gas			Temperature: 400 °C Time: 30 min	

				Ramp rate: 20 °C/min Hydrogen: 10% Nitrogen: 90% Flow rate: 10 l/min	
	7.9	Check if resistance of devices is within specifications	Multimeter		
Create backside etch mask	*8.1*	*Patterning of 14 µm Futurrex NR5-8000 photoresist*		*Mask: FTG 2nd Gen. Backside Etch*	
	8.1.1	Spin coat NR5-8000 photoresist on backside of quadrant	CEE 100CB spinner	Spin rate: 1000 rpm Ramp rate: 200 rpm/sec Time: 40 sec	Thickness: 14 µm
	8.1.2	Let photoresist level out	CEE 100CB spinner	Time: 10 min	
	8.1.3	Softbake photoresist	Hotplate	Temperature: 150 °C Time: 1:30 min	
	8.1.4	Measure intensity of mask aligner	OAI UV-meter	Channel: CI-1 Wavelength: 365 nm	Intensity: 5 mW/cm^2
	8.1.5	Expose quadrant - backside alignment	Karl Suss MA 6	Mask: FTG 2nd Gen. Backside Etch Dose: 300 mJ/cm^2	Time: 60 sec
	8.1.6	Post-exposure bake photoresist	Hotplate	Temperature: 100 °C Time: 2 min	
	8.1.7	Develop photoresist		Developer: RD-6	Time: 60 sec
	8.2	Hardbake photoresist, step 1	Hotplate	Temperature: 120 °C Time: 20 min	
	8.3	Take off hotplate and let cool down		Time: 2 min	
	8.4	Hardbake photoresist, step 2	Hotplate	Temperature: 140 °C Time: 20 min	
	8.5	Cleave wafer into four quadrants	Diamond scribe		
Attach quadrant	9.1	Deposit 6-7 µm of silicon dioxide on carrier wafer	Unaxis PECVD	Recipe: FTGSIO Time: 90 min	Thickness: 6.5 µm
	9.2	Place carrier wafer on hotplate	Hotplate	Temperature: 100 °C	
	9.3	Apply cool grease on perimeter of quadrant on device side			
	9.4	Place quadrant in center of carrier wafer and press down with tweezers			
	9.5	Take carrier wafer off hotplate			
Backside etch	10.1	First run with fewer cycles	Plasma-Therm ICP	Recipe: FTG_SI2 Cycles: 100	Etch rate: 0.65 µm/cycle Trench depth: 32.5 µm
	10.2	Second run with more cycles (rotate carrier wafer 90 °)	Plasma-Therm ICP	Recipe: FTG_SI2 Cycles: 200	Etch rate: 0.65 µm/cycle
	10.3	Measure trench depth	Microscope		Trench depth: 162.5 µm
	10.4	Repeat previous two steps; as trench depth increases reduce number of cycles	Plasma-Therm ICP Microscope	Recipe: FTG_SI2 Cycles: 100…50…25	Trench depth: 400 µm
	10.5	While etching in steps of 15 cycles monitor the cantilever/trench edge from backside with wafer at an angle	Plasma-Therm ICP Microscope (wafer at angle to see the edge)	Recipe: FTG_SI2 Cycles: 15	Stop when majority of devices has the right edge position
	10.6	Remove quadrant from carrier wafer	Acetone bath	Time: 2 h	
	10.7	Remove photoresist from quadrant	fresh Acetone bath	Time: 8 h	
	10.8	Acetone rinse			
	10.9	Methanol rinse			
	10.10	Isopropanol rinse			
	10.11	DI water rinse			
	10.12	Nitrogen dry			
	10.13	Inspect for photoresist residue	Microscope		
	10.14	Oxygen plasma to remove residue if necessary	Plasma-Therm RIE	Recipe: FTGPR Time: steps of 5 min	
Final Release	11.1	Dehydration	Vacuum oven	Temperature: 160 °C Time: 20 min	
	11.2	*Patterning of 8 µm Futurrex NR5-8000 photoresist*		*Mask: FTG 2nd Gen. Backside Etch*	
	11.2.1	Spin coat NR5-8000 photoresist on front side of quadrant	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 500 rpm/sec Time: 35 sec	Thickness: 8 µm
	11.2.2	Softbake photoresist	Hotplate	Temperature: 150 °C Time: 1:30 min	
	11.2.3	Measure intensity of mask aligner	OAI UV-meter	Channel: CI-1 Wavelength: 365 nm	Intensity: 5 mW/cm^2
	11.2.4	Expose wafer	Karl Suss MA 6	Mask: FTG 2nd Gen. Backside Etch Dose: 168 mJ/cm^2	Time: 33.6 sec
	11.2.5	Post-exposure bake photoresist	Hotplate	Temperature: 100 °C Time: 2 min	

	11.2.6	Develop photoresist		Developer: RD-6	Time: 60 sec
	11.3	HF dip to remove buried oxide layer		Hydrofluoric Acid (49%) Time: 30 sec	
	11.4	Move from HF bath to DI water bath		Time: 10 sec	
	11.5	2 more fresh DI water baths			
	11.6	Heat dry	Hotplate with Al foil	Temperature: 100 °C	Time: 3 min
	11.7	Inspect device flatness (repeat steps 11.3-11.6 if devices are not flat)	Microscope		
	11.8	Put quadrant on tex wipe and press centered with flat plastic piece to release single devices	Cut-off plastic swab		

Appendix A.2 – Second Generation Microfabrication Recipe

		Process Step	Equipment	Parameters	Expected value
Create beam outline	1.1	Measure device layer thickness	Nanospec refractometer	Recipe: SOI	Thickness: 2 µm
	1.2	*Etch device layer*	*Plasma-Therm ICP*	*Recipe: HJ_SI_02*	
	1.2.1	First run to calculate etch rate	Plasma-Therm ICP	Time: 25 sec	Etch rate: 28.4 nm/sec
	1.2.2	Second run to etch down to 1 µm	Plasma-Therm ICP		
	1.3	*Solvent wafer clean*			
	1.3.1	Agitated acetone bath	Ultrasonic bath	Time: 5 min	
	1.3.2	Acetone rinse			
	1.3.3	Methanol rinse			
	1.3.4	Isopropanol rinse			
	1.3.5	DI water rinse			
	1.3.6	Nitrogen dry			
	1.4	Dehydration	Vacuum oven	Temperature: 160 °C Time: 20 min	
	1.5	*Patterning of 3.3 µm Shipley 1827 photoresist*		*Mask: FG Beam*	
	1.5.1	Spin coat 1827 photoresist	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 1000 rpm/sec Time: 35 sec	Thickness: 3.3 µm
	1.5.2	Softbake photoresist	Hotplate	Temperature: 115 °C Time: 3:30 min	
	1.5.3	Measure intensity of mask aligner	Karl Suss UV-meter	Channel: CI-2 Wavelength: 405 nm	Intensity: 20 mW/cm^2
	1.5.4	Expose wafer	Karl Suss MA 6	Mask: FG Beam Dose: 220 mJ/cm^2	Time: 11 sec
	1.5.5	Develop photoresist		Developer: MF 354	Time: 35 sec
	1.5.6	Hardbake photoresist	Hotplate	Temperature: 115 °C Time: 10 min	
	1.6	*Structure device layer*	*Plasma-Therm ICP*		
	1.6.1	Chacterize etch rate on dummy wafer with same PR pattern	Plasma-Therm ICP	Recipe: Jay_Si	Etch rate: 0.2 µm/cycle
	1.6.2	Etch sample with safe number of cycles	Plasma-Therm ICP	Recipe: Jay_Si	Number of cycles: 7
	1.7	Make sure no silicon left in trenches	Nanospec refractometer	Recipe: SOI	Thickness: 0 µm
	1.8	*Piranha wafer clean*			
	1.8.1	Agitated acetone bath	Ultrasonic bath	Time: 5 min	
	1.8.2	DI water rinse			
	1.8.3	Nitrogen dry			
	1.8.4	Piranha bath	Hotplate	Sulfuric Acid (96%): 70 ml Hydrogen Peroxide (30%): 30 ml Temperature: 120 °C Time: 10 min	
	1.8.5	DI water rinse			
	1.8.6	Nitrogen dry			
Dopant implantation	2.1	Dehydration	Vacuum oven	Temperature: 160 °C Time: 20 min	
	2.2	*Patterning of 3.3 µm Shipley 1827 photoresist*		*Mask: FG Low Doping*	
	2.2.1	Spin coat 1827 photoresist	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 1000 rpm/sec Time: 35 sec	Thickness: 3.3 µm
	2.2.2	Softbake photoresist	Hotplate	Temperature: 115 °C Time: 3:30 min	
	2.2.3	Measure intensity of mask aligner	Karl Suss UV-meter	Channel: CI-2 Wavelength: 405 nm	Intensity: 20 mW/cm^2
	2.2.4	Expose wafer	Karl Suss MA 6	Mask: FG Low Doping Dose: 220 mJ/cm^2	Time: 11 sec
	2.2.5	Develop photoresist		Developer: MF 354	Time: 35 sec
	2.2.6	Hardbake photoresist	Hotplate	Temperature: 115 °C Time: 35 min	
	2.3	Dopant implantation	Outside vendor	Species: Boron Dose: 2e14 cm^-2 Energy: 30 keV Tilt angle: 7 °	
	2.4	*Piranha wafer clean*			
	2.4.1	Agitated acetone bath	Ultrasonic bath	Time: 5 min	
	2.4.2	DI water rinse			
	2.4.3	Nitrogen dry			

	2.4.4		Piranha bath	Hotplate	Sulfuric Acid (96%): 70 ml Hydrogen Peroxide (30%): 30 ml Temperature: 120 °C Time: 10 min	
	2.4.5		DI water rinse			
	2.4.6		Nitrogen dry			
Dopant drive-in	*3.1*	*PECVD silicon dioxide deposition*		*Unaxis PECVD*		
	3.1.1		Characterize deposition rate on dummy wafer	Unaxis PECVD	Recipe: FTGSIO	Deposition rate: 1.132 nm/sec
	3.1.2		Measure buried oxide layer thickness	Nanospec refractometer	Recipe: Oxide on silicon	Thickness: 1 µm
	3.1.3		Deposit 200 nm of silicon dioxide	Unaxis PECVD	Recipe: FTGSIO	Time: 177 sec
	3.1.4		Measure buried oxide layer thickness	Nanospec Refractometer	Recipe: Oxide on silicon	Thickness: 1.2 µm
	3.2	Rapid thermal anneal		AET RTP	Recipe: Jay1 Temperature: 1000 °C Time: 20 min Ramp rate: 90 °C/sec Nitrogen gas flow: 5 l/min	
Create vias in silicon dioxide	4.1	Dehydration		Vacuum oven	Temperature: 160 °C Time: 20 min	
	4.2	*Patterning of 3.3 µm Shipley 1827 photoresist*			*Mask: FG Via*	
	4.2.1		Spin coat 1827 photoresist	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 1000 rpm/sec Time: 35 sec	Thickness: 3.3 µm
	4.2.2		Softbake photoresist	Hotplate	Temperature: 115 °C Time: 3:30 min	
	4.2.3		Measure intensity of mask aligner	Karl Suss UV-meter	Channel: CI-2 Wavelength: 405 nm	Intensity: 20 mW/cm^2
	4.2.4		Expose wafer	Karl Suss MA 6	Mask: FG Via Dose: 220 mJ/cm^2	Time: 11 sec
	4.2.5		Develop photoresist		Developer: MF 354	Time: 35 sec
	4.2.6		Hardbake photoresist	Hotplate	Temperature: 115 °C Time: 10 min	
	4.3	*Etch vias into silicon dioxide*		*Plasma-Therm ICP*		
	4.3.1		Characterize etch rate on dummy wafer	Plasma-Therm ICP	Recipe: TLWSIO2A	Etch rate: 100 nm/min
	4.3.2		Etch 20 seconds longer than necessary	Plasma-Therm ICP	Recipe: TLWSIO2A	Time: 2:20 min
	4.4	*Piranha wafer clean*				
	4.4.1		Agitated acetone bath	Ultrasonic bath	Time: 5 min	
	4.4.2		DI water rinse			
	4.4.3		Nitrogen dry			
	4.4.4		Piranha bath	Hotplate	Sulfuric Acid (96%): 70 ml Hydrogen Peroxide (30%): 30 ml Temperature: 120 °C Time: 10 min	
	4.4.5		DI water rinse			
	4.4.6		Nitrogen dry			
Create metal connections	5.1	Dehydration		Vacuum oven	Temperature: 160 °C Time: 20 min	
	5.2	*Patterning of 8 µm Futurrex NR5-8000 photoresist*			*Mask: FG Metalization*	
	5.2.1		Spin coat NR5-8000 photoresist	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 500 rpm/sec Time: 35 sec	Thickness: 8 µm
	5.2.2		Softbake photoresist	Hotplate	Temperature: 150 °C Time: 1:30 min	
	5.2.3		Measure intensity of mask aligner	OAI UV-meter	Channel: CI-1 Wavelength: 365 nm	Intensity: 5 mW/cm^2
	5.2.4		Expose wafer	Karl Suss MA 6	Mask: FG Metalization Dose: 168 mJ/cm^2	Time: 33.6 sec
	5.2.5		Post-exposure bake photoresist	Hotplate	Temperature: 100 °C Time: 2 min	
	5.2.6		Develop photoresist		Developer: RD-6	Time: 60 sec
	5.3	BOE dip to remove native oxide			6:1 Buffered Oxide Etch Time: 10 sec	
	5.4	DI water rinse				
	5.5	Nitrogen dry				

	5.6	Electron beam evaporative deposition of metal layer		CVC E-Beam evaporator	Metal: Aluminum Thickness: 800 nm Deposition rate: 0.3 nm/sec Pressure: 2e-6 torr (max.)	
	5.7	*Photoresist lift-off*				
	5.7.1		Acetone bath (covered)		Time: 2 h	
	5.7.2		Agitated acetone bath	Ultrasonic bath	Time: 30 min	
	5.7.3		Acetone rinse			
	5.7.4		Methanol rinse			
	5.7.5		Isopropanol rinse			
	5.7.6		DI water rinse			
	5.7.7		Nitrogen dry			
	5.8	Sintering in forming gas			Temperature: 400 °C Time: 30 min Ramp rate: 20 °C/min Hydrogen: 10% Nitrogen: 90% Flow rate: 10 l/min	
	5.9	Check if resistance of devices is within specifications		Multimeter		
Make quadrants	6.1	Cleave wafer into four quadrants		Diamond scribe		
	6.2	Acetone rinse				
	6.3	Methanol rinse				
	6.4	Isopropanol rinse				
	6.5	DI water rinse				
	6.6	Nitrogen dry				
Create backside etch mask	*7.1*	*Patterning of 14 µm Futurrex NR5-8000 photoresist*			*Mask: FG Backside ICP*	
	7.1.1		Spin coat NR5-8000 photoresist on backside of quadrant	CEE 100CB spinner	Spin rate: 1000 rpm Ramp rate: 200 rpm/sec Time: 40 sec	Thickness: 14 µm
	7.1.2		Let photoresist level out	CEE 100CB spinner	Time: 10 min	
	7.1.3		Softbake photoresist	Hotplate	Temperature: 150 °C Time: 1:30 min	
	7.1.4		Measure intensity of mask aligner	OAI UV-meter	Channel: CI-1 Wavelength: 365 nm	Intensity: 5 mW/cm^2
	7.1.5		Expose quadrant - backside alignment	Karl Suss MA 6	Mask: FG Backside ICP Dose: 300 mJ/cm^2	Time: 60 sec
	7.1.6		Post-exposure bake photoresist	Hotplate	Temperature: 100 °C Time: 2 min	
	7.1.7		Develop photoresist		Developer: RD-6	Time: 60 sec
	7.2	Hardbake photoresist, step 1		Hotplate	Temperature: 120 °C Time: 20 min	
	7.3	Hardbake photoresist, step 2		Hotplate	Temperature: 140 °C Time: 20 min	
Attach quadrant	8.1	Spin coat NR5-8000 photoresist on carrier wafer		CEE 100CB spinner	Spin rate: 1000 rpm Ramp rate: 200 rpm/sec Time: 40 sec	Thickness: 14 µm
	8.2	Place quadrant in center of carrier wafer				
	8.3	Hardbake photoresist, step 1		Hotplate	Temperature: 120 °C Time: 20 min	
	8.4	Take off hotplate and let cool down			Time: 2 min	
	8.5	Hardbake photoresist, step 2		Hotplate	Temperature: 140 °C Time: 20 min	
Backside etch	9.1	First run to check machine status		Plasma-Therm ICP	Recipe: FTG_SI2 Cycles: 50	Etch rate: 0.65 µm/cycle Trench depth: 32.5 µm
	9.2	Second run with more cycles		Plasma-Therm ICP	Recipe: FTG_SI2 Cycles: 200	Etch rate: 0.65 µm/cycle
	9.3	Measure trench depth		Microscope		Trench depth: 162.5 µm
	9.4	Repeat previous two steps; as trench depth increases reduce number of cycles		Plasma-Therm ICP Microscope	Recipe: FTG_SI2 Cycles: 100…50…25	Trench depth: 400 µm
	9.5	While etching in steps of 15 cycles monitor the cantilever/trench edge from backside with wafer at an angle		Plasma-Therm ICP Microscope (wafer at angle to see the edge)	Recipe: FTG_SI2 Cycles: 15	Stop when majority of devices has the right edge position
	9.6	Remove quadrant from carrier wafer		RR4 or 1165	Time: 2 h Temperature: 80 °C	
	9.7	Remove photoresist from quadrant		RR4 or 1165 (fresh)	Time: 12 h Temperature: 80 °C	

	9.8	DI water rinse				
	9.9	Nitrogen dry				
	9.10	Inspect for photoresist residue		Microscope		
	9.11	Oxygen plasma to remove residue if necessary		Plasma-Therm RIE	Recipe: FTGPR Time: steps of 5 min	
Final Release	10.1	Dehydration		Vacuum oven	Temperature: 160 °C Time: 20 min	
	10.2	*Patterning of 8 µm Futurrex NR5-8000 photoresist*			*Mask: FG Backside ICP*	
	10.2.1		Spin coat NR5-8000 photoresist on front side of quadrant	CEE 100CB spinner	Spin rate: 3000 rpm Ramp rate: 500 rpm/sec Time: 35 sec	Thickness: 8 µm
	10.2.2		Softbake photoresist	Hotplate	Temperature: 150 °C Time: 1:30 min	
	10.2.3		Measure intensity of mask aligner	OAI UV-meter	Channel: CI-1 Wavelength: 365 nm	Intensity: 5 mW/cm^2
	10.2.4		Expose wafer	Karl Suss MA 6	Mask: FG Backside ICP Dose: 168 mJ/cm^2	Time: 33.6 sec
	10.2.5		Post-exposure bake photoresist	Hotplate	Temperature: 100 °C Time: 2 min	
	10.2.6		Develop photoresist		Developer: RD-6	Time: 60 sec
	10.3	HF dip to remove buried oxide layer			Hydrofluoric Acid (49%) Time: 30 sec	
	10.4	Move from HF bath to DI water bath			Time: 10 sec	
	10.5	2 more fresh DI water baths				
	10.6	Heat dry		Hotplate with Al foil	Temperature: 100 °C	Time: 3 min
	10.7	Inspect device flatness (repeat steps 10.3-10.6 if devices are not flat)		Microscope		
	10.8	Put quadrant on tex wipe and press centered with flat plastic piece to release single devices		Cut-off plastic swab		

Appendix B.1 – Plasma-Therm ICP Recipes

Recipe name: FTG_SI2

Step Name	Stabilize gases	High Density Plasma	Polymer Deposition	Polymer Etch	Silicon Etch
Time (sec)	30	10	4	3	7
Pressure (mTorr)	15	15	15	15	15
C4F8 flow (sccm)	20	20	70	0.5	0.5
SF6 flow (sccm)	0.5	0.5	0.5	50	100
O2 flow (sccm)	0	0	0	0	0
Ar flow (sccm)	40	40	40	40	40
RF1	0	30	1	12	10
RF2	0	825	825	825	825

Recipe name: JAY_SI

Step Name	Stabilize gases	High Density Plasma	Polymer Deposition	Polymer Etch	Silicon Etch
Time (sec)	30	10	4	2	6
Pressure (mTorr)	15	15	15	16	16
C4F8 flow (sccm)	20	20	70	0.5	0.5
SF6 flow (sccm)	0.5	0.5	0.5	50	100
O2 flow (sccm)	0	0	0	0	0
Ar flow (sccm)	40	40	40	40	40
RF1	0	30	1	9	7
RF2	0	825	825	825	825

Recipe name: HJ_SI_02

Step Name	Stabilize gases	High Density Plasma	Silicon Etch
Time (sec)	30	10	variable
Pressure (mTorr)	15	15	16
C4F8 flow (sccm)	20	20	0.5
SF6 flow (sccm)	0.5	0.5	100
O2 flow (sccm)	0	0	0
Ar flow (sccm)	40	40	40
RF1	0	30	9
RF2	0	825	825

Recipe name: TLWSIO2

Step Name	Stabilize gases	Silicon Oxide Etch
Time (sec)	30	variable
Pressure (mTorr)	5	5
CL2 flow (sccm)	0	0
BCL3 flow (sccm)	0	0
H2 flow (sccm)	5	5
Ar flow (sccm)	10	10
O2 flow (sccm)	0	0
CF4 flow (sccm)	65	65
C4F6 flow (sccm)	0.5	0
CHF3 flow (sccm)	0	0
RF1	0	250
RF2	0	400

Recipe name: TLWSIO2A

Step Name	Stabilize gases	Silicon Oxide Etch
Time (sec)	30	variable
Pressure (mTorr)	5	5
CL2 flow (sccm)	0	0
BCL3 flow (sccm)	0	0
H2 flow (sccm)	3	3
Ar flow (sccm)	0	0
O2 flow (sccm)	0	0
CF4 flow (sccm)	30	30
C4F6 flow (sccm)	0	0
CHF3 flow (sccm)	0	0
RF1	0	100
RF2	0	250

Appendix B.2 – Unaxis PECVD Recipes

Recipe name: FTGSIO

Step Name	Stabilize gases	Silicon Oxide Deposition
Time (sec)	60	variable
Pressure (mTorr)	850	850
SIH4 flow (sccm)	400	400
NH3 flow (sccm)	0	0
N2O flow (sccm)	900	900
HE flow (sccm)	550	550
N2 flow (sccm)	0	0
CH4 flow (sccm)	0	0
SF6 flow (sccm)	0	0
PH3SIH4H flow (sccm)	0	0
RF1	0	90

Appendix B.3 – Vision RIE Recipes

Recipe name: Standard Oxide Recipe

Pressure (mTorr):	20
RF (W):	200
Stabilization Time (sec):	15
Step Time (sec):	variable
CHF3 flow (sccm)	25
O2 flow (sccm)	2.5
Ar flow (sccm)	0
Etch Rate (nm/min):	10

Recipe name: Oxide w Argon

Pressure (mTorr):	12
RF (W):	350
Stabilization Time (sec):	15
Step Time (sec):	variable
CHF3 flow (sccm)	40
O2 flow (sccm)	6
Ar flow (sccm)	20
Etch Rate (nm/min):	20-50